İSTANBUL TECHNICAL UNIVERSITY ★ INSTITUTE OF SCIENCE AND TECHNOLOGY

VARIABLE GAIN AMPLIFIERS

M.Sc. Thesis by
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HAZİRAN 2011

FOREWORD

This master's thesis is dedicated to my mother who has unselfishly supported me with love during my studies.

I would like to express my deep appreciation and thanks for my advisor Prof. Dr. Ali TOKER for all his guidance, supports and encouragements to me.

In addition, I am earnestly thankful to Research Assistant Mustafa SAYGINER for all his efforts and spending valuable time on my thesis.

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Nazan İLTÜZER
Electronics Engineering

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ABBREVIATIONS

VGA	**:** Variable Gain Amplifier
AGC	**:** Automatic Gain Control
CDMA	**:** Code Division Multiple Access
UWB	**:** Ultra Wide Bandwidth
IF	**:** Intermediate Frequency
RF	**:** Radio Frequency
GSM	**:** Global System for Mobile Communications
ADC	**:** Analog Digital Converter
LAN	**:** Local Area Network
LNA	**:** Low Noise Amplifier
CMFB	**:** Common Mode Feedback

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SUMMARY

VARIABLE GAIN AMPLIFIERS

Nowadays, as a result of developing communication systems, increasing data transfer rates and communication speeds require sufficient electronic hardware and systems to be developed. For instance, many systems using wireless communication standards need high frequency and low noise transceiver structures which are also required to handle a wide dynamic range of signal amplitude.

Controlling of the signal amplitude, while keeping above the noise level, is a necessity when concerning with the amplitude modulated communication systems and data storage environments such as disk drivers.

Variable gain amplifiers are the key sub-block of the automatic gain control loops. In the scope of this thesis work, at first, variable gain amplifiers are classified in terms of the operating principles and circuit realizations. Moreover, the author implemented and simulated various variable gain amplifiers employing cascade gain structures given in the literature by using 0.35µm CMOS process for a performance comparison.

Secondly, two new variable gain amplifier topologies and a new gain model are proposed. The first proposed structure is composed of three cascaded variable gain amplifiers and designed in 0.35µm CMOS process providing 61dB dynamic range. Operating frequency of the circuit is between 1.2GHz and 2.2GHz in the control voltage range. The second proposed circuit structure is composed of one variable gain amplifier and two separate control blocks where there are two control voltage range. The circuit provides nearly 36.7dB dynamic range and the cut off frequency changes 716MHz to 795MHz in the control voltage range.

Moreover, a new pseudo exponential approximation function is obtained by optimizing the coefficients of terms of the second order Taylor series expansion. It is shown that 90dB dynamic range is possible to be obtained with the control circuit by using the new proposed approximation.

Finally, a new variable gain amplifier model is constructed with using operational transconductance amplifiers and the proposed model is experimented on circuit board to verify the model performance. LM13700 operational transconductance amplifiers are used to verify proposed model and performance metrics of the proposed model has been measured.

ÖZET

KAZANCI AYARLANABİLEN KUVVETLENDİRİCİLER

Günümüzde haberleşme sistemlerinin gelişmesiyle birlikte artan veri transferi ve iletişim hızları bu sistemlerde kullanılan elektronik donanım ve sistemlerinin de ihtiyaca cevap verecek şekilde geliştirilmesi ihtiyacını doğurmuştur. Örneğin kablosuz haberleşme standardını kullanan bir çok sistemde yüksek frekanslarda veri alışverişi yapabilen düşük gürültülü alıcı verici yapılarının gene geniş bir dinamik aralıkta çalışabilmesi gerekmektedir.

Bilginin işaret genliğinde saklı tutulduğu haberleşme sistemlerinde ve yine işaret genliğinin değişkenlik gösterebildiği veri depolama birimlerinde genlik bilgisinin kontrol edilebilir ve gürültü eşiğinin üzerinde tutulabilir olması önemlidir.

Kazancı ayarlanabilen kuvvetlendiriciler, otomatik genlik kontrolünün gerçekleştirildiği devrelerin en önemli alt yapı bloğudur. Bu çalışma kapsamında, başlangıç olarak literatürde önerilen kazancı ayarlanabilen kuvvetlendiriciler çalışma prensipleri ve devre gerçeklemeleri açısından sınıflandırılarak incelenmiştir. Ek olarak kaskod sınıfındaki kuvvetlendirici yapılar aynı CMOS proses içinde yeniden tasarlanıp başarımları görece karşılaştırılmıştır.

İkinci aşama çalışmalarda ise mevcut yapılara ek olarak yeni model ve devre yapıları önerilmiştir. Önerilen ilk devrede üç katlı kaskad yapı ile 61dB dinamik aralık ve 1.2GHz ile 2.2GHz arasında çalışma frekansı 0.35µm salt CMOS yapıdan elde edilmiştir. İkinci sunulan devre yapısında ise tek katlı kazancı ayarlanabilen kuvvetlendirici bloğu için kontrol geriliminin farklı iki aralığı için ayrı fonksiyonları gerçekleştiren bir kontrol devresi, dinamik aralığı arttıracak şekilde tasarlanmıştır. Önerilen yapı ile 36.7dB dinamik aralık 716MHz ile 795MHz arasındaki band genişliğinde elde edilmiştir.

Bunun dışında, yeni bir sözde üstel yaklaşım fonksiyonu Taylor serisinde ikinci dereceden terimlerinin katsayıları optimize edilerek elde edilmiştir. Önerilen yaklaşımı kullanan kontrol devresi ile tek katta 90dB dinamik aralığın elde edilebileceği gösterilmiştir.

Son olarak da yeni bir kazancı ayarlanabilen kuvvetlendirici modeli geçiş iletkenliği kuvvetlendiricileri kullanılarak oluşturulmuş ve deneysel olarak LM13700 geçiş iletkenliği kuvvetlendiricisi kullanılarak önerilen modelin başarımı gösterilmiştir.

1. INTRODUCTION

1.1 Motivation

Over the past few years, the wireless communication systems have developed due to the increasing demand for the information exchange. While the information exchange begins to get larger, one of the encountered major problems is the maximum range of data transfer, which could be interrupted by atmospheric effects or other environmental effects etc. Furthermore, when the input signal unexpectedly changes due to the obstacles, atmospheric effects etc., output signal should be constant to enlarge the range of data transfer. In order to provide an output signal with constant amplitude, an Automatic Gain Control circuit (AGC) including Variable Gain Amplifier (VGA) as a sub-block could be used. In the literature, it is possible to seem any proposed VGA structures using different gain control approaches to increase dynamic range.

In this thesis work, formerly proposed gain control functions are examined to classify and understand VGA operation. In order to obtain wide dynamic range, exponential gain control is made by using and optimizing exponential approximations.

1.2 Variable Gain Amplifiers and Their Applications

VGAs are widely used in many areas like communication systems, hard disk drivers, medical equipments, audio/video analog signal processing circuits etc. In communication systems, VGAs are usually used in the AGC feedback loop. In the early radios, because of slow variations in the amplitude of the received signals, AGC was implemented for maintaining a constant signal level at the output. Therefore, the output signal would be regardless of the signal variations at the input of the system where the amplitude of an incoming signal can vary over a wide dynamic range.

The AGC block consists of sub blocks such as VGA, detector, filter etc. as shown in Figure 1.1.

Generally, VGA operates in a feedback loop of an AGC block and the gain of the VGA is varied dynamically by the feedback control signal. Moreover, because the gain function of the AGC loop is dependent on the gain of the VGA, relationship between the control signal and the gain of the VGA should be set to a value that the overall gain of the AGC should be constant through the control signal range. Thus, settling time of the AGC loop is constant in time and the transient response becomes uniform [1].

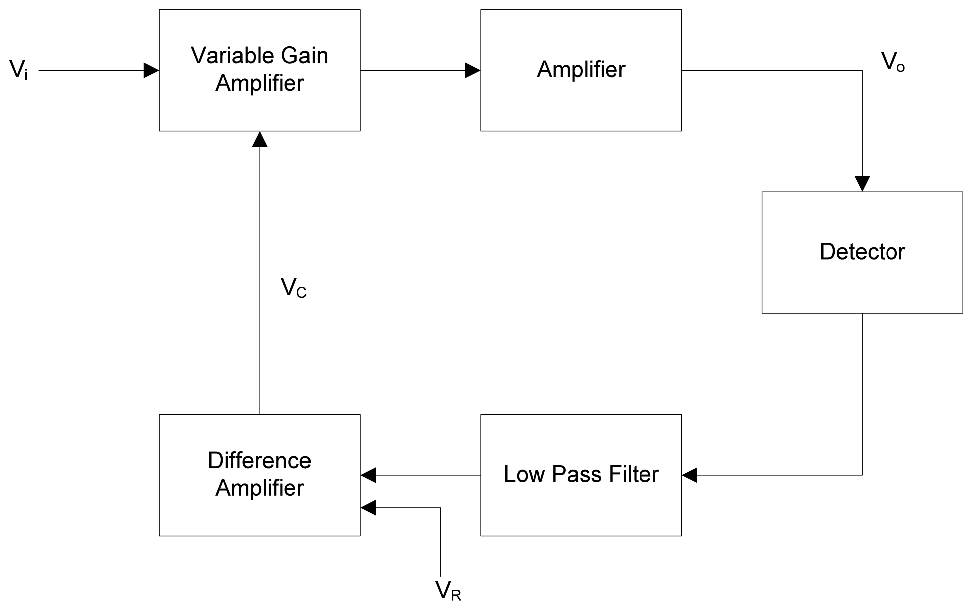


Figure 1.1: A simplified automatic gain control (AGC) block diagram.

Variable gain amplifier finds a very wide range of applications where AGC is needed, such as hearing aids, imaging and wireless communications. In these applications, the transmission signal power can be controlled and the received signal amplitude can be adjusted by the VGA [2].

Figure 1.2 shows the transceiver architecture for an example of DS-CDMA (Direct Sequence CDMA) UWB systems. Variable gain amplifiers are located in both transmitter and receiver part of the transmitter. Although the input signals are unpredictable in the receiver part of the transceiver, the VGA maintains constant output power and also maximize the dynamic range of receiver.

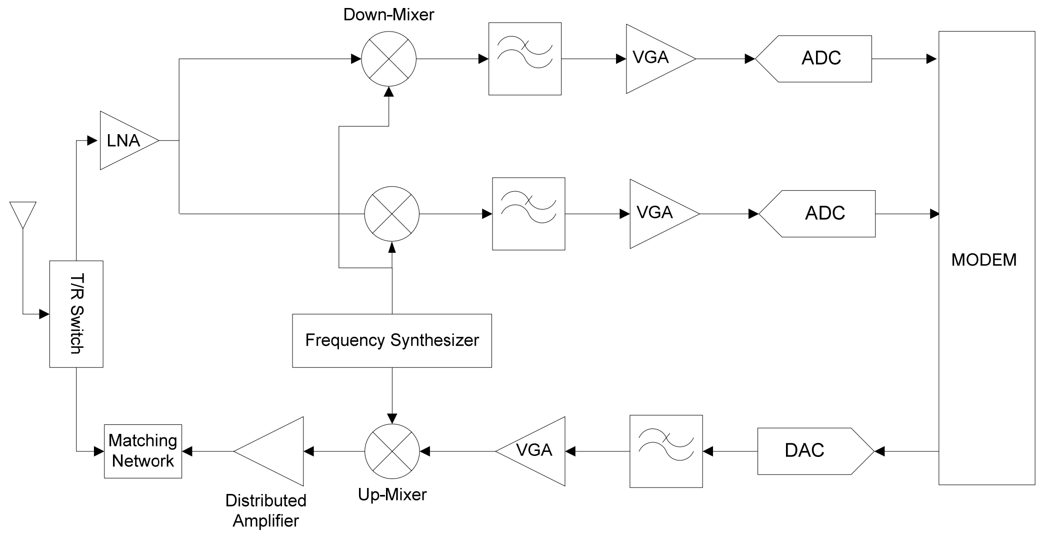


Figure 1.2: The transceiver architecture for DS-CDMA UWB systems [3].

For instance, the CDMA receiver requires at least 80 dB dynamic range which is much higher than GSM systems where the GSM systems requires 30 dB dynamic range [4, 5]. In addition, in the transmitter part of the transceiver, the VGAs are used to regulate each mobile unit transmit power, therefore equal power from each user is received at the base station so that the system capacity is optimized [1, 3, 5, 6, 7]. Moreover, VGA is following low noise amplifier (LNA), down-mixer and low pass filter in the receiving path as shown in Figure 1.3. The frequency is down converted to an intermediate frequency by down-mixer and unwanted high frequency terms are filtered by using low pass filter. Thus, VGA in the receiver part could operate with the intermediate frequency. If the VGA is used before mixer, VGA should operate in the radio frequency [8]. It is also said that VGAs operating in very high frequencies will be used in future wireless systems [9, 10, 11].

In Figure 1.3, after the frequency of the input signal is converted to a desired frequency by the mixers, the gain can be varied with the VGA, which operates in the desired frequency [12].

An example of multiple-band analog interface block is also shown in Figure 1.4 [13]. The IF front end provides to change the frequency of an input signal to a desired frequency and also controls the gain.

One another application area of the VGAs is disk drivers. In the disk driver systems, VGA normalizes the read channel average amplitude of the read pulses to a reference value before they are sent to the peak detector [14, 15]. For this application, dynamic range of VGA must be at least 30dB [16]. And also, signal to noise ratio should be low enough because the amplitude values of the read pulses are commonly between 0.1-2mV [14].

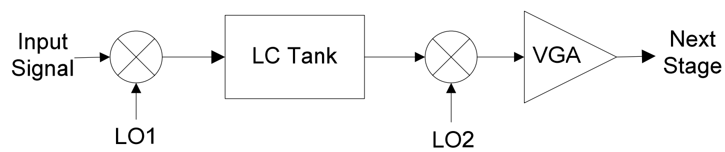


Figure 1.3: Dual conversion heterodyne Front-End [13].

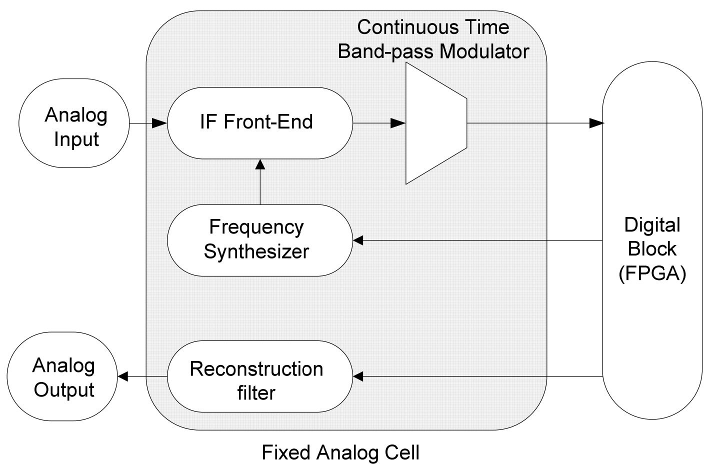


Figure 1.4: Multiple band analog interface block [13].

As an extended summary of applications, variable gain amplifiers can be widely used in:

- WCDMA systems [5, 7, 17],
- Audio/Video analog signal processing circuits [18],
- Portable communication drivers [17],
- Hard disk drivers [1, 14, 19,15,20],
- Medical equipments [20, 21],
- Hearing aids [2],
- Imaging and wireless communications [2],

- Digital cable TV, satellite television [22],
- Wireless communication systems [20], wireless LAN [23], broadband residential communications [22], radio communicated system [24].

In addition, there are many commercial VGA chip products to be used discretely and some of them could be listed as AD600 [25], MAX2035 [26], THS7530 [27], AD603 [28], LT5554 [29] and ADL5330 [30].

Functional Block Diagram of a Single Channel AD600/AD602 is shown in Figure 1.5. ADL5330, AD600/602 and AD603 have almost the same control structure. They have R-2R ladder or balanced ladder attenuator used in the feedback loop as shown in Figure 1.5.

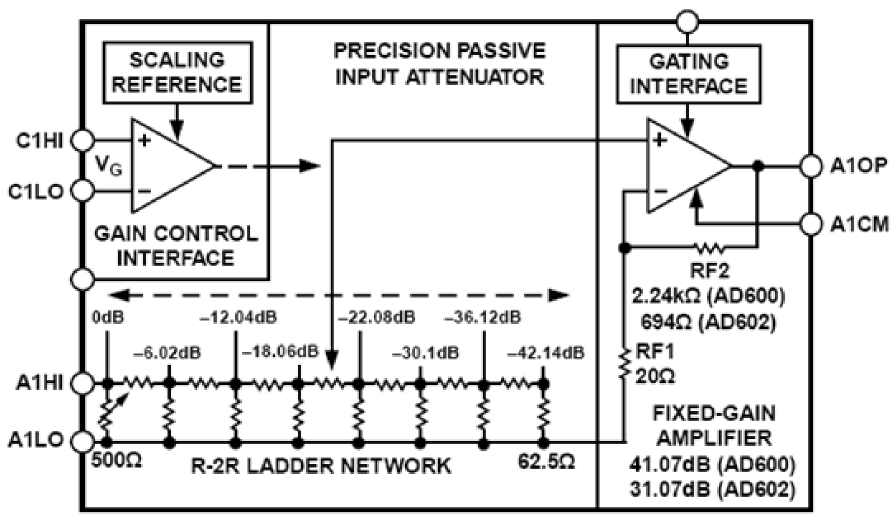


Figure 1.5: Functional block diagram of a single channel of the AD600/AD602.

There are two channels in AD600 and the gating input selects which channel to work. In the control block, there are gain control interface and input attenuator. If the input signal is small, the slider would be moved to right in the gain control interface and the gain would be increased. Otherwise, if the input signal is high, the slider would be moved to the left and the gain would be decreased.

To summarize the subject, the application fields of commercial VGAs are listed as shown in Table 1.1.

Table 1.1: The applications of the commercial VGAs.

Commercial VGAs	Applications of the Commercial VGAs
LT5554	IF Sampling Receivers
L5330	Transmit and receive power control at RF and IF
AD600, AD603	Signal measurement
AD603, THS7530	Video gain controls
AD600, AD603	A/D range extensions
MAX2035	Differential ADC Driver
AD600, AD603, THS7530	RF/IF AGC amplifier
AD600, AD603, THS7530	Imaging applications such as cellular radio, satellite receivers, global positioning, radar

1.3 Thesis Organization

VGA and its applications are examined in Section 1. As it is already mentioned, VGAs have many application areas such as an automatic gain control circuits, transceivers and receivers, medical equipments and hard disk drivers.

In section 2, a classification of the VGAs by means of the control voltage mechanism is studied. For this purpose, a detailed literature search is fulfilled and the proposed mathematical approaches for Taylor series approximation, pseudo exponential function and exponential function with using differential equations for the gain control operation are examined in details. MATLAB verifications are used to verify theoretical results.

In section 3, circuit implementations for gain blocks of the VGAs are examined and a topological classification is carried out. Gain blocks are classified into four groups of circuit topology which are variable feedback structure, variable biasing structure, cascade structure and current steering structure. Cascode examples are redesigned in 0.35µm CMOS process and simulated by using SPICE to compare their performance. There is also a general comparison of the structures for all the classified topologies.

In section 4, two new VGA circuits, a new exponential approximation, and also a new VGA model are given.

In section 5, conclusion and recommendations are presented.

2. CLASSIFICATION OF THE VGAs IN TERMS OF THE CONTROL FUNCTIONS

A VGA basically has three basic blocks which are an amplifier block, a control block and common mode feedback block as shown in Figure 2.1.

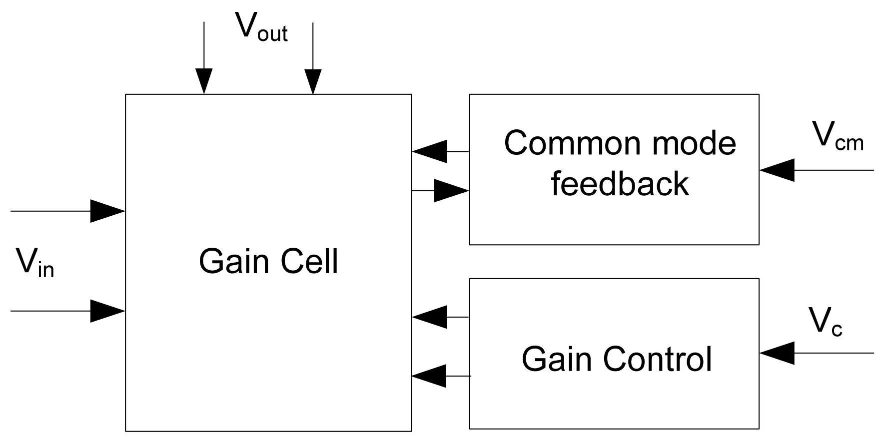


Figure 2.1: A basic VGA block.

A VGA can be classified as the function of the control block and there are mainly two types of VGA; if the control signal is switchable, VGA has discrete gain step and it is named as the digitally controlled VGA [29]. That is, the control signal can be implemented with switchable resistors as shown in Figure 2.2 [31], [32] or switch capacitors [33], [34]. The digitally controlled VGAs are used when the level of the gain is quantized to a known level and it is selected by the digital control system. When this information is sent through the control block of the VGA, it would have discrete gain step which is adjusted during noncritical periods in time slotted signal [35], [36]. On the other hand, the digitally controlled VGA has some deficiencies such as the digital control block does not know the information of the desired gain or the discontinuous phase signals can cause some problems. In order to obtain smooth gain transitions, the other type of VGA, which is controlled by an analog signal, can be used. This type of VGA has continuous gain levels and it can be adopted by a variable transconductance or a variable resistance to control the gain, as shown in Figure 2.3.

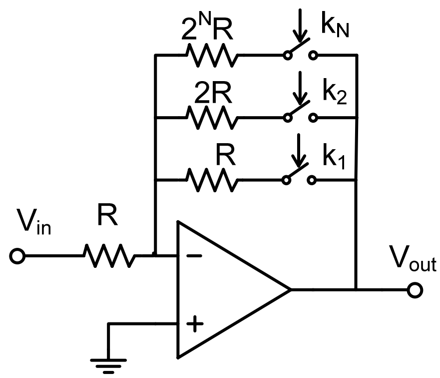


Figure 2.2: Digitally controlled VGA gain [35].

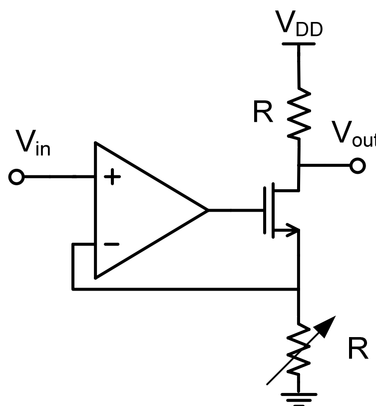


Figure 2.3: VGA controlled by analog signal [35].

Moreover, the VGA which is controlled by analog signal can be controlled exponentially or linearly. That is to say, VGA can also be classified such as linearly or exponentially controlled VGA.

2.1 Linear Gain Control of VGAs

If the gain of VGA changes linearly with variable control signal, the linear gain control can be obtained. In Figure 2.4, there is an example circuit for the linear gain control of VGAs, which has only an operational amplifier, constant and variable resistors. The gain of VGA can be varied with the coefficient of variable resistance.

The circuit in Figure 2.4 is simulated with using SPICE and linear variation between the gain and coefficient of variable resistance is shown in Figure 2.5.

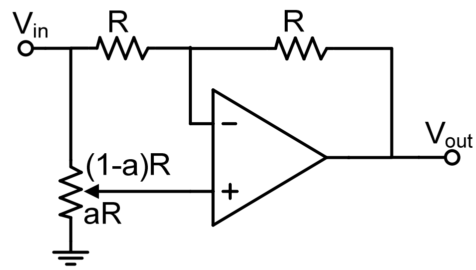


Figure 2.4: An example circuit for linear gain control of VGAs.

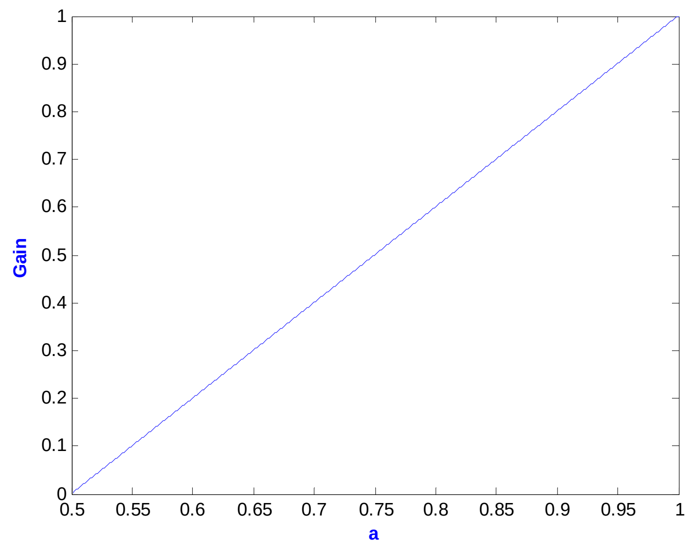


Figure 2.5: Variable gain and coefficient of variable resistance for Figure 2.4.

Linear gain control can be provided by variable feedback resistance [17, 37] and current steering technique [9, 38-41].

In Figure 2.6, the gain of VGA is varied by the feedback resistor R_S. The block diagram of the circuit in Figure 2.6 is shown in Figure 2.7.

As shown in Figure 2.7, the voltage gain of the VGA is the product of the gain of transconductance amplifier (G_m) and the gain of transimpedance amplifier (R_m). The transimpedance gain R_m is given in the equation (2.1). R_{in} is the input resistance and A_i is the gain of current amplifier.

$$R_m = -\frac{R_f A_i - R_{in}}{1 + A_i} \qquad \textbf{(2.1)}$$

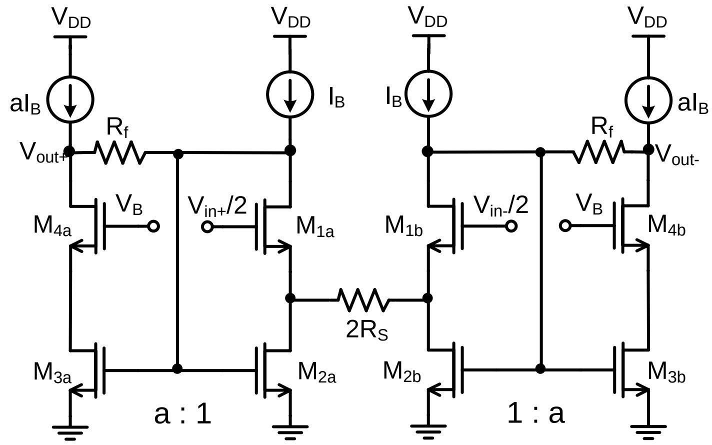


Figure 2.6: A VGA circuit whose gain varied linearly with variable feedback resistor R_S [17].

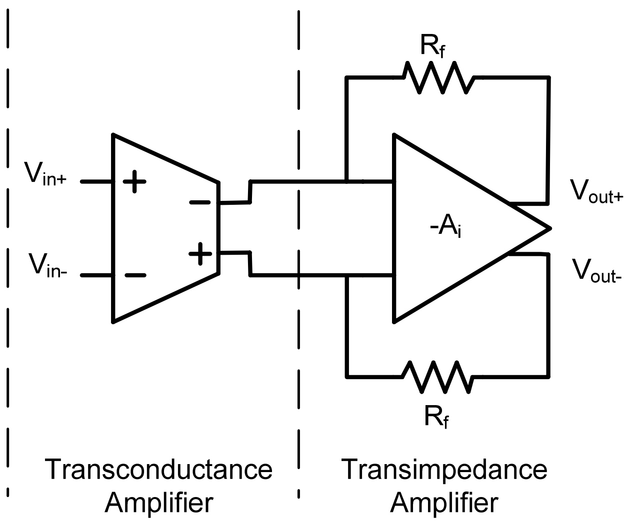


Figure 2.7: The block diagram of the VGA circuit in Figure 2.6 [17].

If the gain of current amplifier (A_i) is enough bigger than 1 ($A_i >> 1$),then the equation (2.1) turn into equation (2.2). Therefore, the gain of transimpedance amplifier is only dependent on R_f resistance. The value of resistance R_f is chosen to set a voltage gain range.

$$R_m \approx R_f \tag{2.2}$$

Therefore, the variable gain is provided by varying the source degeneration resistor R_s.

In Figure 2.8, a current steering linear VGA circuit is shown. The gain of the circuit can be calculated with the product of the transconductance of the input transistors and the output resistance.

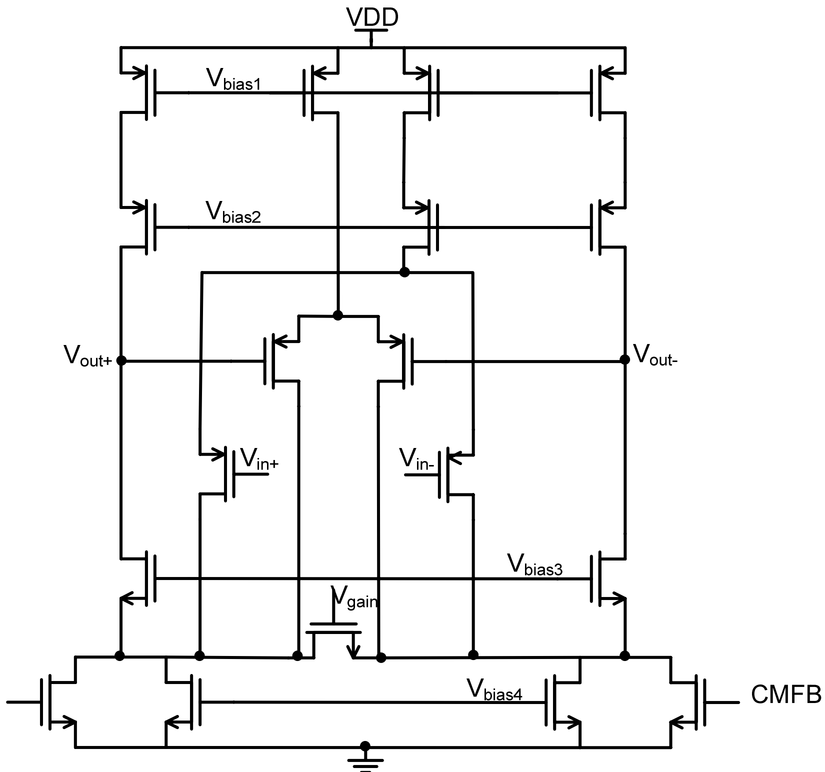


Figure 2.8: A current steering linear VGA circuit [38].

By varying the gate voltage of M_o (V_{gain}), the gain could be varied. When the M_o transistor is on, the current of the input transistors is decreased and the transconductance of the input transistors is also decreased. Otherwise, when M_o is off, the transconductance of the input transistors is increased. Therefore the gain is changed with the square root of the drain current of the input transistor.

2.2 Exponential Gain Control of VGAs

If the gain of VGA changes exponentially with variable control signal, an exponential gain control of VGA can be obtained. A block diagram of exponential current control VGA is shown in Figure 2.9.

The output current of multiplier is given in equation (2.3). Due to the changing the control voltage (V_c) or the control current (I_c) with (V_3-V_4) is exponential, the output current of multiplier changes exponential with V_c or I_c.

$$I_0 = \alpha(V_1 - V_2)(V_3 - V_4) \quad \textbf{(2.3)}$$

The exponential gain control of the VGA provides a wide dynamic range characteristic.

Wide dynamic range characteristic of VGA is useful in AGC circuits to minimize the settling time of the circuit, thus settling time of AGC would be independent from the input signal level and transient response of the AGC becomes uniform. As mentioned earlier, the CDMA systems are required almost 80dB gain range. In order to realize that wide dynamic range, the gain of VGA would be controlled exponentially.

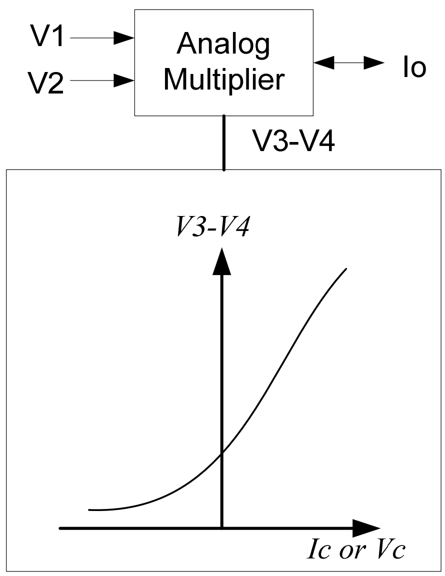


Figure 2.9: A block diagram of exponential gain control VGA.

The exponential gain control of the VGA provides a wide dynamic range characteristic. Wide dynamic range characteristic of VGA is useful in AGC circuits to minimize the settling time of the circuit, thus settling time of AGC would be independent from the input signal level and transient response of the AGC becomes uniform. As mentioned earlier, the CDMA systems are required almost 80 dB gain range. In order to realize that wide dynamic range, the gain of VGA would be controlled exponentially.

There are some ways in literature to provide the exponential control function. One of the ways to realize an exponential control function is to use DC current voltage characteristic of a bipolar transistor. The exponential gain control can easily be realized by this exponential DC characteristic of bipolar transistor.

On the other hand, the bipolar techniques are not compatible with CMOS technologies, while BiCMOS is not a cost efficient solution.

Another way to realize an exponential control function is to create the bipolar transistor in CMOS technology, which is known as parasitic bipolar transistor. Although the parasitic bipolar transistor provides wide dynamic range, it is strongly dependent on temperature and process variations.

Moreover, in CMOS process, there are two main ways to realize exponential function. One way to use MOSFET in subthreshold region, which has exponential current voltage characteristic, but it has disadvantages like noise and bandwidth. When realizing the circuit which MOSFETs operates in subthreshold region, this circuit operates in low frequency applications. Other way is to reach an approximated exponential equation with using the linear or saturation region characteristics of the MOSFET [4, 42].

Consequently, the classification of VGAs in the view of the control function is listed as below Figure 2.10.

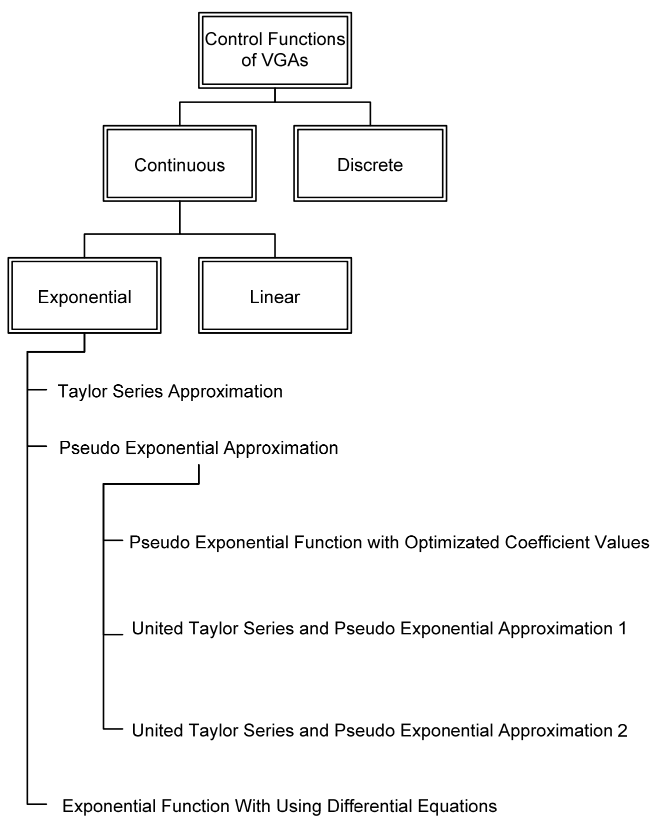


Figure 2.10: Classification of the VGAs in terms of the control functions.

2.2.1 DC characteristic of the bipolar transistor

The relationship between an input voltage and an output current of a bipolar transistor is given in equation (2.4). This exponential relationship of the equation easily provides to have an exponential control.

$$I_{EC} = I_S e^{\frac{-V_{BE}}{nV_T}} \quad \textbf{(2.4)}$$

On the other hand, bipolar technology is not compatible with analog and mixed mode circuits. Also, it is more expensive than CMOS technology [21].

2.2.1.1 Parasitic BJT in MOSFET

The parasitic bipolar transistors can be realized in CMOS technology, as shown in Figure 2.11. Both vertical and lateral parasitic bipolar transistors share the same base terminal. The collector of the vertical BJT is substrate of PMOS and the collector and emitter terminals of the lateral BJT are constructed by drain and source terminals of PMOS.

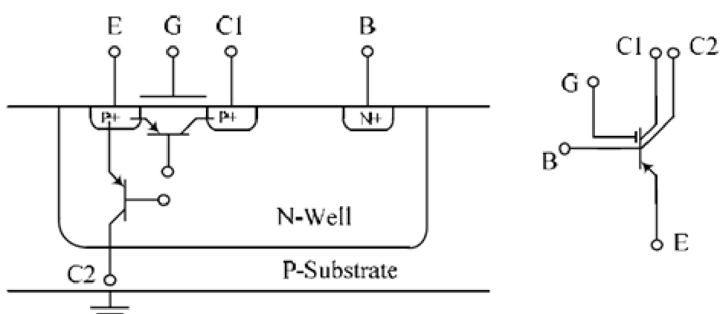


Figure 2.11: Vertical and parallel parasitic BJTs in PMOS.

In equation (2.4), the current flowing through base terminal to C_1 or C_2 have exponential characteristic. This current can be use to control the VGA and it provides wide dynamic range and low power consumption. On the other hand, this parasitic BJTs are also dependent on the temperature and process variations.

The gain control block of the VGA realized by a parasitic BJT is given in Figure 2.12. The current of loads (M_3, M_4) of VGA equals to the current of the parasitic BJT (I_{ctrl}). When the current of parasitic BJT varies exponentially with V_{ctrl}, the currents of the M_3 and M_4 change exponentially with V_{ctrl} too.

Therefore, the gain of VGA is shown in equation (2.5) and the exponential relationship between the control voltage and gain can be seen in equation (2.6).

$$A_V = \frac{g_{minput}}{g_{mload}} = \sqrt{\frac{(W/L)_{input} I_{bias}}{(W/L)_{load} I_{ctrl}}} \qquad \textbf{(2.5)}$$

$$A_V = \frac{g_{minput}}{g_{mload}} = \sqrt{I_{bias}} \times I_S e^{\frac{1}{2}\left(\frac{V_{ctrl} - V_E}{nkT/q}\right)} \qquad \textbf{(2.6)}$$

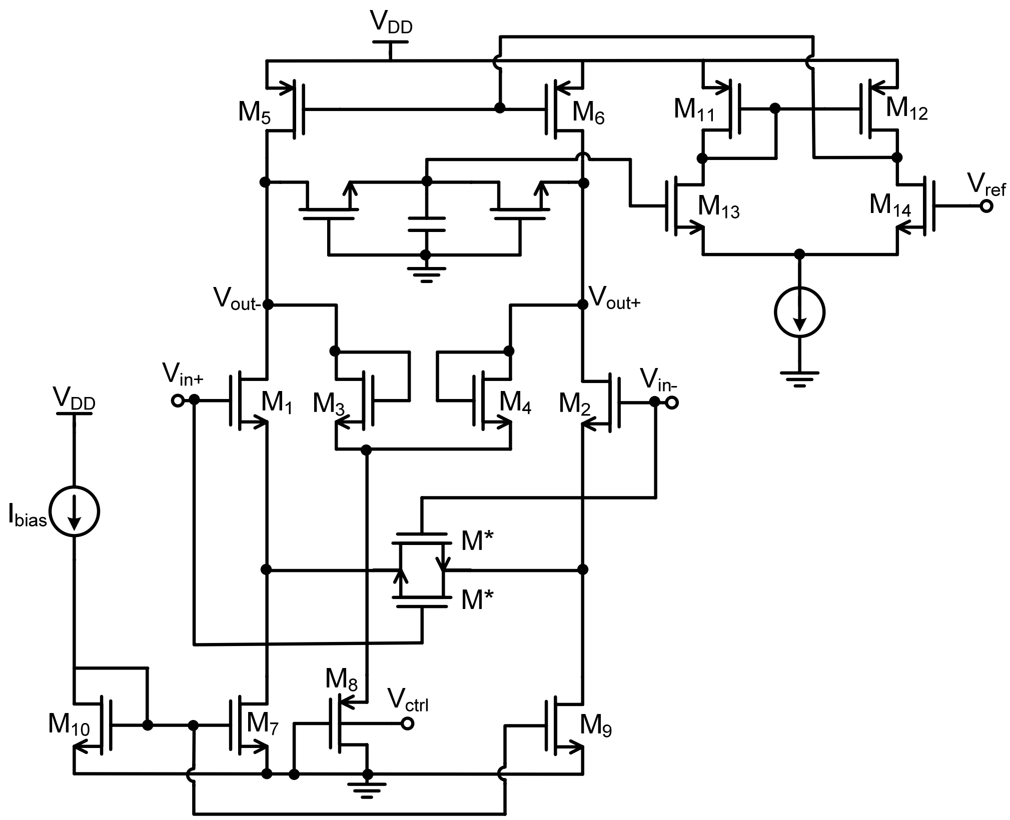


Figure 2.12: A VGA circuit using parasitic BJT in gain control block [4].

2.2.2 MOSFET in subthreshold region

When MOSFET operates in subthreshold region, it has an exponential DC current voltage characteristic. Also, it has low power consumption and operates in low frequency applications [21].

In Figure 2.13, M_1-M_4 transistors operate in subthreshold region of MOSFET. The DC characteristic equations of transistors M_1-M_4 are shown in equations (2.7), (2.8), (2.9) and (2.10).

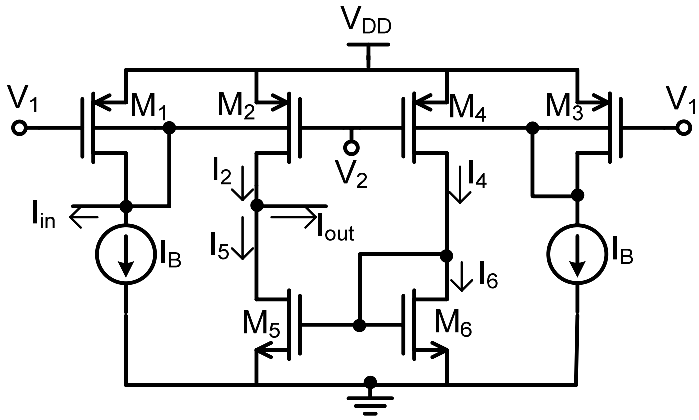


Figure 2.13: A VGA circuit with MOSFETs which operate subthreshold region in gain control block [12].

$$I_1 = I_{DO}e^{\frac{(V_{DD}-V_1+(n-1)V_{SB1})}{nV_T}} \tag{2.7}$$

$$I_2 = I_{DO}e^{\frac{(V_{DD}-V_2+(n-1)V_{SB2})}{nV_T}} \tag{2.8}$$

$$I_3 = I_{DO}e^{\frac{(V_{DD}-V_1+(n-1)V_{SB3})}{nV_T}} \tag{2.9}$$

$$I_4 = I_{DO}e^{\frac{(V_{DD}-V_2+(n-1)V_{SB4})}{nV_T}} \tag{2.10}$$

From the Kirchhoff's current law, the equations (2.11) and (2.12) can be written.

$$I_1 = I_{in} + I_B \tag{2.11}$$

$$I_3 = I_B \tag{2.12}$$

If the product of I_2 and I_1 is divided by I_1, then (2.13) is obtained.

$$I_2 = (I_{in} + I_B)e^{\frac{V_1-V_2}{nV_T}} \tag{2.13}$$

If the product of I_3 and I_4 is divided by I_3, then (2.14) is obtained.

$$I_4 = I_B e^{\frac{V_1-V_2}{nV_T}} \tag{2.14}$$

Also, equation (2.15) is written from the current mirror which realizes by M_5 and M_6 transistors.

$$I_5 = I_6 = I_4 \tag{2.15}$$

Finally, it can be reached the current gain equation (2.16) which can be changed exponentially with V_1 and V_2.

$$I_{out} = I_2 + I_5 = I_{in} e^{\frac{V_1 - V_2}{nV_T}} \tag{2.16}$$

2.2.3 Taylor series approximation

To realize an exponential function with MOSFET in saturation region, there are some approximation methods. One of these methods is Taylor series approximation. An exponential function can be expressed by Taylor series which is given equation (2.17).

$$e^{\frac{b}{a}x} = 1 + \frac{b}{a}x + \frac{1}{2!}\left(\frac{b}{a}x\right)^2 + \cdots + \frac{1}{n!}\left(\frac{b}{a}x\right)^n + \cdots \tag{2.17}$$

$$x\left|\frac{b}{a}\right| \leq 1 \tag{2.18}$$

If the equation (2.18) is substituted to the equation (2.17), then the series can be approximated as equation (2.19) and (2.20).

$$e^{\frac{b}{a}x} \cong 1 + \frac{b}{a}x + \frac{b^2}{2a^2}x^2 \tag{2.19}$$

$$2a^2 e^{\frac{b}{a}x} \approx a^2 + (a + bx)^2 \tag{2.20}$$

Due to the ideal exponential function, the error function of the Taylor series approximation is shown in Figure 2.14 with by using MATLAB. When the error is between positive and negative five percent, x will be between -0.57 and 0.81. The comparison between an ideal exponential function and Taylor series approximation (b/a = 1) is shown in Figure 2.15 with by using MATLAB.

In the equation (2.20), the zero order term can be realized as a constant current, the first order term can be realized as a V-I converter and the second order term can be realized as a V-I squarer.

A block diagram of the Taylor series approximation function circuit is composed of V-I converter, V-I squarer and constant current biasing circuit is shown in Figure 2.16.

Taylor series approximation function also realizes with using the DC characteristic function of MOSFET in saturation region [43].

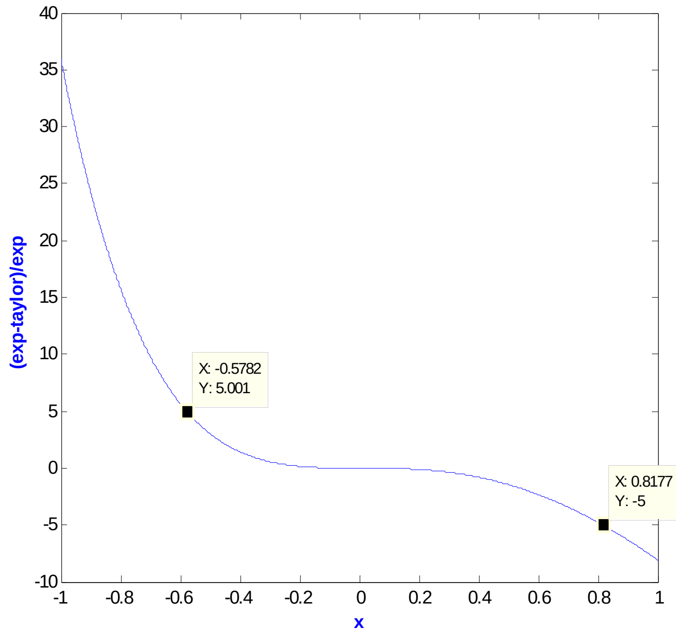


Figure 2.14: The error function of Taylor series approximation function.

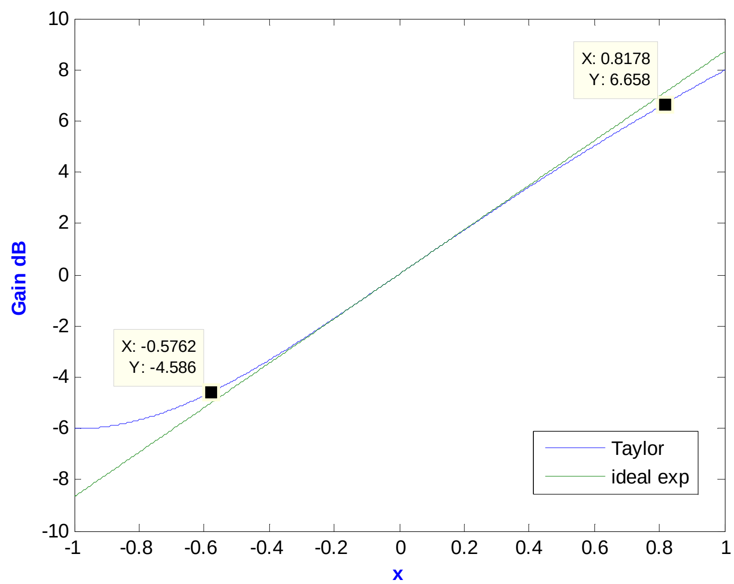


Figure 2.15: The comparison between an ideal exponential function and Taylor series approximation (b/a = 1).

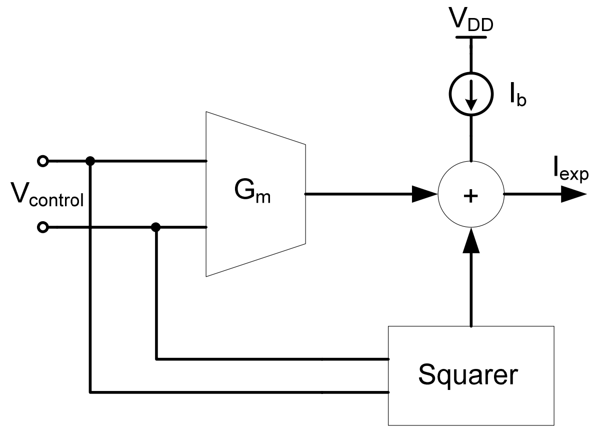


Figure 2.16: The block diagram of the Taylor approximation function circuit [21].

2.2.4 Pseudo exponential approximation

Another function, which is approximated to an ideal exponential function is named as pseudo exponential function. This function also provides to realize an exponential function in CMOS process, when MOSFETs are in saturation or in linear region. The pseudo approximated equation is given in (2.21).

$$e^{nx} \approx \left(\frac{1 + x/2}{1 - x/2}\right)^{n} \; ; \; |x| < 1 \qquad \textbf{(2.21)}$$

The function is drawn with using MATLAB and the error function of pseudo exponential approximation (n = 1) is shown in Figure 2.17.

When the error is between positive and negative five percent, x will be between -0.8 and 0.8 and when x is between -0.8 and 0.8, the pseudo approximated function is also between -7.1dB and 7.43dB which is shown in Figure 2.18.

The error functions of pseudo exponential approximation are shown in Figure A.1, Figure A.2, Figure A.3 and Figure A.4 for the different values of coefficient n (n = 2, 3, 4, 10).

The pseudo exponential approximation functions are shown in Figure A.5, Figure A.6, Figure A.7 and Figure A.8 when the error function is positive and negative five percent.

As it is seen from Figure A.5, Figure A.6, Figure A.7 and Figure A.8, when the value of coefficient n increases, then the value of pseudo exponential approximation function value would be wider, but the x range would be smaller. Therefore, the control signal variability would be difficult.

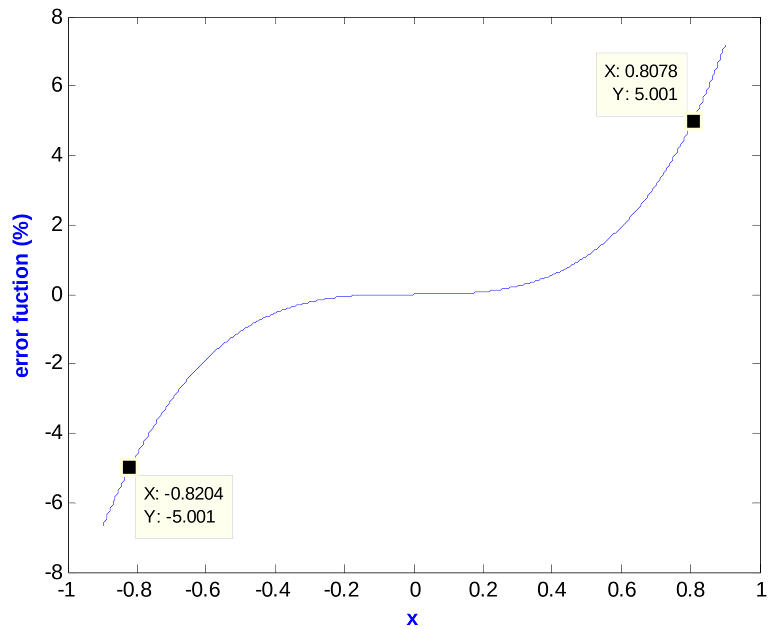


Figure 2.17: The error function of pseudo exponential approximation (n = 1).

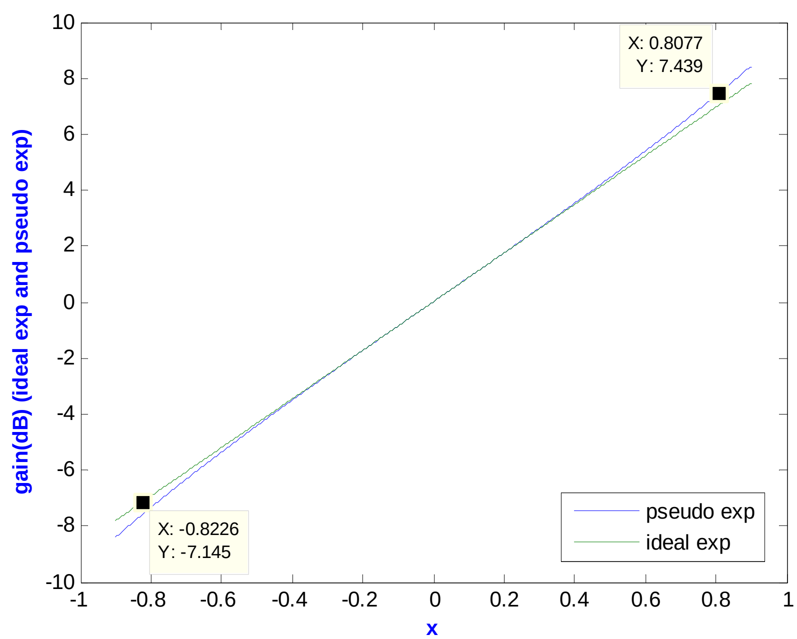


Figure 2.18: Pseudo exponential approximation function (n = 1).

Table 2.1: The comparison of different n values of pseudo exponential function.

N values of Pseudo Exponential Approximation $e^{nx} \approx \left(\frac{1+x/2}{1-x/2}\right)^n$; $\lvert x \rvert < 1$	**x values**	**Gain (dB)**
n = 1	Between -0.8 and 0.8	14
n = 2	Between -0.66 and 0.66	23
n = 3	Between -0.57 and 0.57	30
n = 4	Between -0.51 and 0.51	35
n = 10	Between -0.39 and 0.38	65

The comparison of different n values is given from Table 2.1. As it is also seen from Table 2.1, when the n value is increased, the gain range is increased, but the control range is decreased.

In Figure 2.19, an example of VGA circuit, which gain control block function is the pseudo exponential function, is shown.

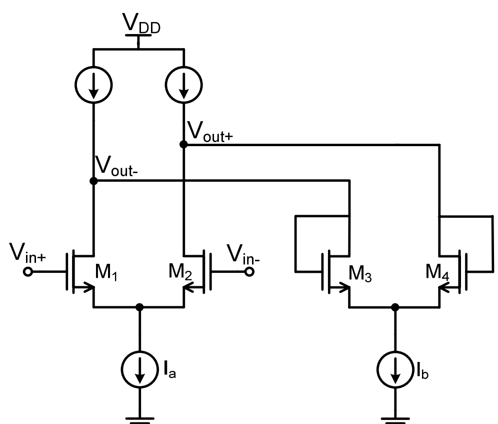


Figure 2.19: A VGA circuit whose gain control block function is the pseudo function with using the MOSFETs in saturation region.

The circuit in Figure 2.19 is composed of a differential input transconductance stage M_1, M_2 and diode connected loads M_3, M_4. The differential gain of VGA is given in equation (2.22).

$$K = g_{m\_M1,2} \times R_{out} \tag{2.22}$$

R_{out} is dependent on the transconductances of M_3 and M_4, it is given in equation (2.23).

$$R_{out} = {}^{1}/_{g_{m\_M3,4}} \tag{2.23}$$

Because of the transconductances of input stage and loads are proportional with bias currents I_a and I_b like in equation (2.24), the gain could be changed with varying the bias currents. If the bias current is varied like in equation (2.25), then the gain is changed exponentially with I_x.

$$K = \frac{g_{m\_M1,2}}{g_{m\_M3,4}} = \sqrt{\frac{2\beta I_a}{2\beta I_b}} \tag{2.24}$$

$$\frac{I_a}{I_b} = \frac{1 + I_x}{1 - I_x} \tag{2.25}$$

Therefore, the exponential gain control of VGA could be done by using pseudo exponential function in CMOS process when the MOSFETs are in saturation region.

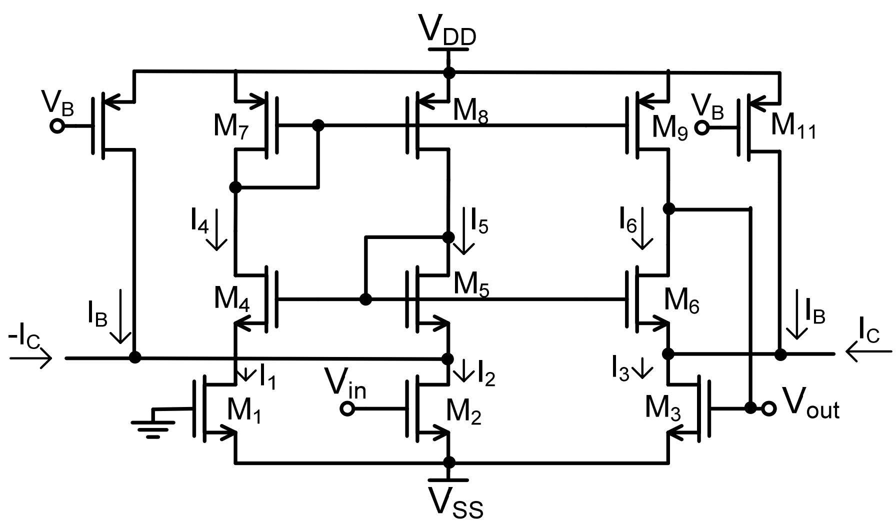


Figure 2.20: A VGA circuit whose gain control function is the pseudo exponential one with using the MOSFETs in linear region.

In Figure 2.20, M_1, M_2 and M_3 are the transistors which operate in linear region. The drain currents of M_1, M_2, M_3 is given in equations (2.26), (2.27) and (2.28).

$$I_1 = \frac{K_{n1}}{2}(2(-V_{SS} - V_{TH})V_{DS1} - V_{DS1}^2) \tag{2.26}$$

$$I_2 = \frac{K_{n2}}{2}(2(V_{in} - V_{SS} - V_{TH})V_{DS2} - V_{DS2}^2) \quad \textbf{(2.27)}$$

$$I_3 = \frac{K_{n3}}{2}(2(V_{out} - V_{SS} - V_{TH})V_{DS3} - V_{DS3}^2) \quad \textbf{(2.28)}$$

Also, the equations (2.29) and (2.30) could be given by Kirchhoff Current Law.

$$I_2 = I_B - I_C + I_5 \quad \textbf{(2.29)}$$

$$I_3 = I_B + I_C + I_6 \quad \textbf{(2.30)}$$

The drain currents of M_7, M_8 and M_9 are same because of using the current mirror (M_7, M_8 and M_9) given by the equation (2.31). Therefore, the drain currents and also V_{GS} voltages of M_4, M_5 and M6 would be the same like in equation (2.32).

$$I_1 = I_4 = I_5 = I_6 \quad \textbf{(2.31)}$$

$$V_{GS4} = V_{GS5} = V_{GS6} = \sqrt{\frac{2I_1}{K_{n4}}} + V_{TH} \quad \textbf{(2.32)}$$

From the equation (2.33), (2.34) can be written.

$$V_{GS4} + V_{DS1} = V_{GS5} + V_{DS2} = V_{GS6} + V_{DS3} \quad \textbf{(2.33)}$$

$$V_{DS1} = V_{DS2} = V_{DS3} \quad \textbf{(2.34)}$$

From the equation (2.31), I_5 and I_6 equals to I_1. Also, when I_1 is subtracted from I_2 or I_3 in the equations (2.29) or (2.30), V_{DS} voltages would be same due to the equation (2.34). Therefore, the equations (2.35) and (2.36) are written.

$$I_B - I_C = K_n V_{in} V_{DS2} \quad \textbf{(2.35)}$$

$$I_B + I_C = K_n V_{out} V_{DS3} \quad \textbf{(2.36)}$$

Finally, the gain equation is given in equations (2.37) and the pseudo approximated equation is given in (2.38) and as it is seen from equation, the gain is varied exponentially.

$$V_{out} = V_{in}\frac{I_B + I_C}{I_B - I_C} = V_{in}\frac{1 + \frac{I_C}{I_B}}{1 - \frac{I_C}{I_B}} \quad \textbf{(2.37)}$$

$$V_{out} = V_{in}e^{2\frac{I_C}{I_B}} \quad \textbf{(2.38)}$$

2.2.4.1 Pseudo exponential function with optimizing the coefficients

In pseudo exponential function, when x approaches to 1 or -1, the function approaches to zero or infinite. As it is seen in Figure 2.17, the error is between positive and negative five percent; x will be between -0.8 and 0.8. In addition, when x is bigger than 0.8, the pseudo exponential function deviates from the ideal exponential function. If the value of the x is increased when the function is zero or infinite, then a better accuracy in representing the exponential relation is expected [44].

An exponential function can be written like equation (2.38) by shortening the Taylor series to the first order function.

$$e^{x} = e^{x+\alpha x-\alpha x} = \frac{1 + \alpha x}{1 - (1 - \alpha)x} \quad \textbf{(2.38)}$$

In this equation, when the value of α is chosen like 0.25 or 0.75, negative or positive range of x will increase as shown in Figure 2.21 and Figure 2.22. When the function is given like in equation (2.39), the x values will be between -0.2 and 2.581, due to the positive and negative five percent values of error function in Figure 2.22. In addition, when the x values are between these values, gain function is between 18.35dB and -1.39dB as shown in Figure 2.21.

$$f(x) = \frac{1 + {}^{3x}\!/_{4}}{1 - {}^{x}\!/_{4}}, x > 0 \quad \textbf{(2.39)}$$

$$f(x) = \frac{1 + {}^{x}\!/_{4}}{1 - {}^{3x}\!/_{4}}, x < 0 \quad \textbf{(2.40)}$$

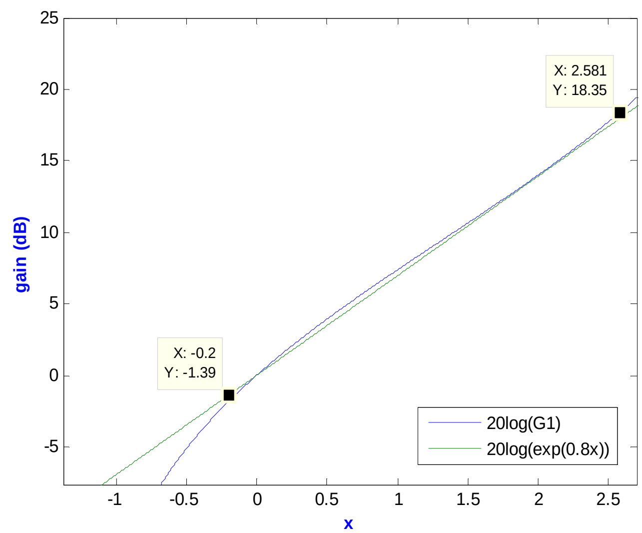


Figure 2.21: Pseudo exponential function by optimizing the coefficients (x > 0).

When the function is given like (2.40), the x values are between -2.6 and 0.19, due to the positive and negative five percent values of the error function in Figure 2.22.

In addition, when the x values are between these values, the gain function ranges between –18.06dB and 1.3dB, as shown in Figure 2.24.

With the equations (2.39) and (2.40), the value of the function varies between -2.6 and 2.58. As a result, the dynamic range of the VGA which uses the equation (2.40) can be wider than the VGA which uses the pseudo exponential function.

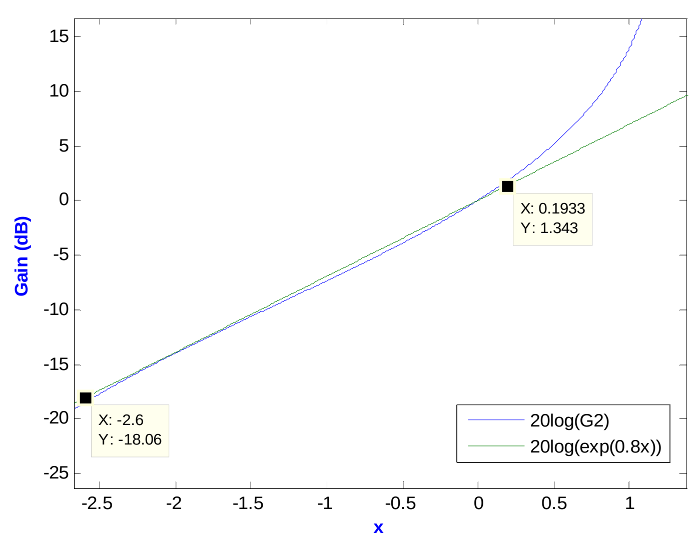


Figure 2.22: Pseudo exponential function with optimizing coefficient (x < 0).

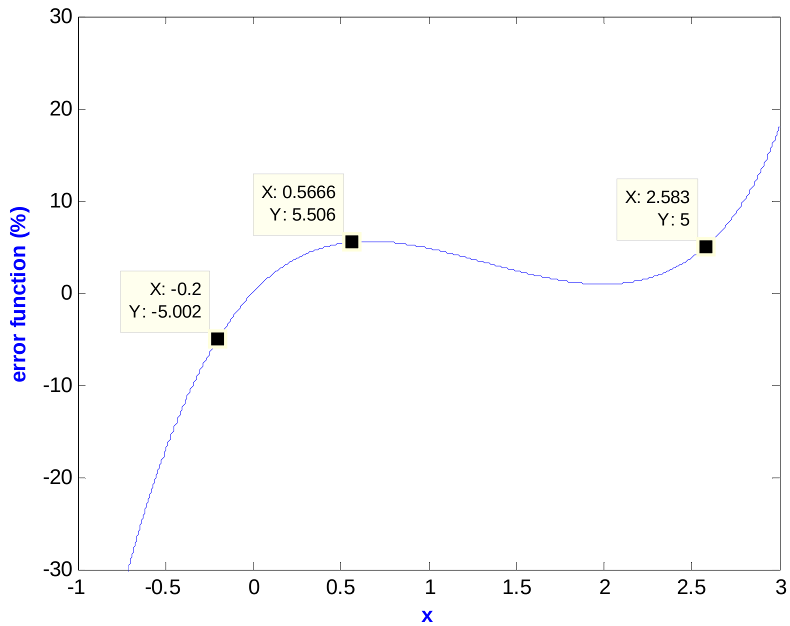


Figure 2.23: The error function of pseudo exponential function with optimizing coefficient (n = 1), (x > 0).

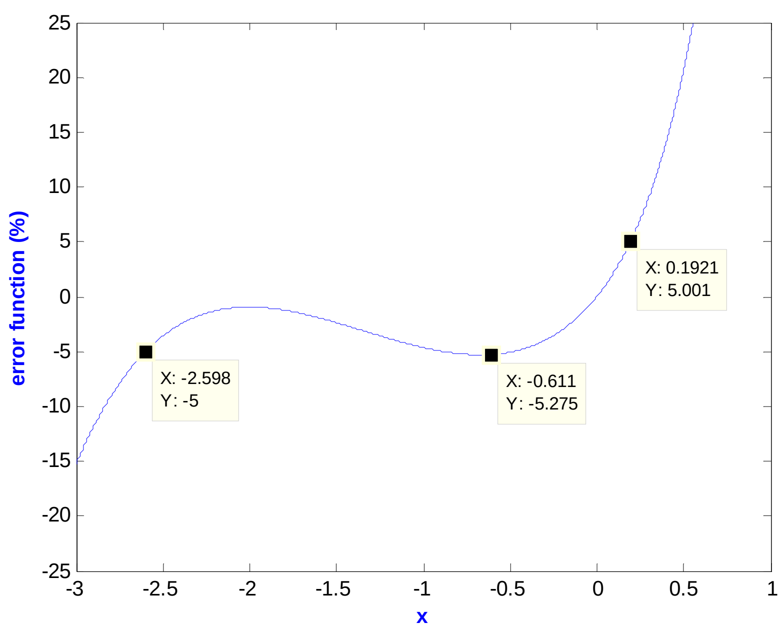


Figure 2.24: The error function of pseudo exponential function by optimizing coefficient (n = 1), (x < 0).

There is an example of VGA shown in Figure 2.25 whose function is composed by pseudo exponential function by optimizing coefficient values [45]. G_1 and G_2 blocks of the block diagram in Figure 2.25 are shown in Figure 2.26 and Figure 2.27.

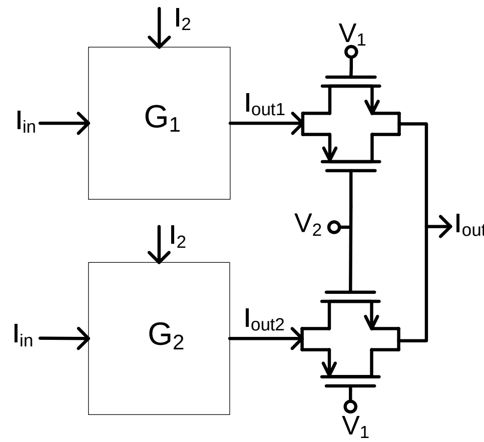


Figure 2.25: The block diagram of VGA given in [45].

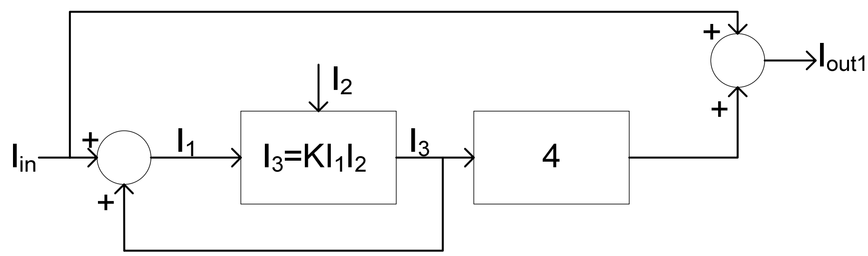


Figure 2.26: Realization of G_1 function.

The equation (2.41) is obtained from the block diagram of G_1 in Figure 2.26. As it is seen from the equation (2.41) when I_2/I_B is chosen as a variable, then it is similar to the equation (2.39).

$$G_1 = \frac{I_{out1}}{I_{in}} = \frac{1+\frac{3I_2}{2I_B}}{1-\frac{I_2}{2I_B}} \qquad \textbf{(2.41)}$$

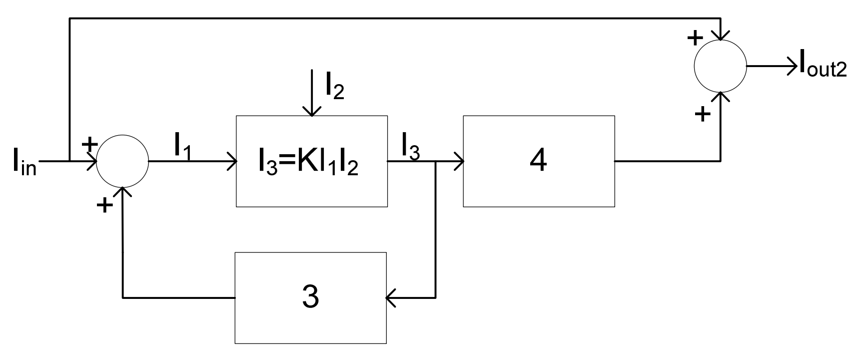


Figure 2.27: The block diagram for the realization of G_2.

The equation (2.42) which is similar to the equation (2.40) is obtained from the block diagram of G_2 given in Figure 2.27.

$$G_2 = \frac{I_{out2}}{I_{in}} = \frac{1 + \frac{I_2}{2I_B}}{1 - \frac{3I_2}{2I_B}} \tag{2.42}$$

In Figure 2.25, if the value of I_2/I_B is bigger then 0, the block G_1 will operate and if the value of I_2/I_B is smaller then 0, the block G_2 will operate. In order to provide these working conditions, circuit in Figure 2.28 is used to generate the control voltages V_1 and V_2.

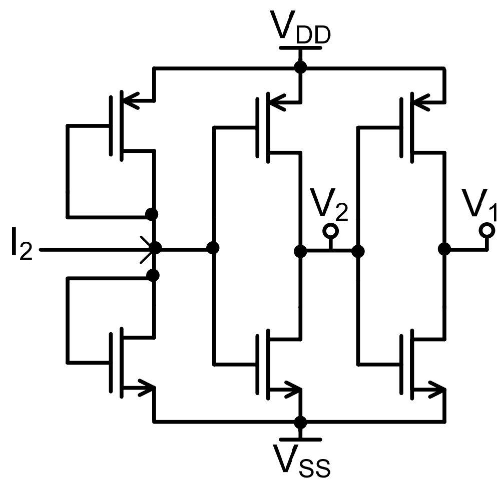


Figure 2.28: Circuit used to generate the control voltages V_1 and V_2 to be used in the block diagram of Figure 2.25.

2.2.4.2 A composition of Taylor and pseudo exponential approximation–1

A composition of Taylor series and pseudo exponential approximation [35], given in equation (2.43), is composed of using the equations (2.44) and (2.45).

$$f(x) = \left[\frac{k + (1 + ax)^2}{k + (1 - ax)^2}\right] \tag{2.43}$$

$$e^{2ax} \cong \frac{1 + ax}{1 - ax} \tag{2.44}$$

$$e^{2ax} \cong 1 + 2ax + \frac{(2a)^2}{2!}x^2 = \frac{1}{2}[1 + (1 + 2ax)^2] \tag{2.45}$$

where k is a constant.

A composition of Taylor series and pseudo exponential approximation with the different k values is plotted in Figure 2.29 by using MATLAB. The function reaches its maximum value when k equals to 0.15.When the x value is between 10 and -10, the value of the error function is between positive and negative five percent as it is seen from Figure 2.30.

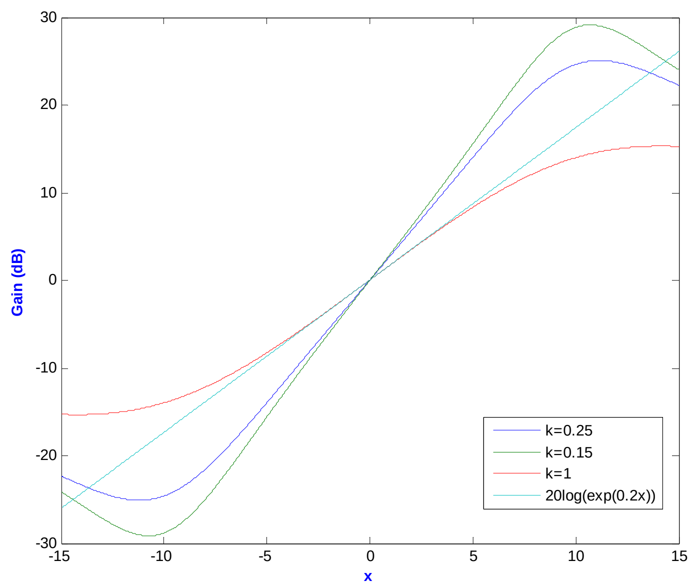


Figure 2.29: A composition of Taylor and pseudo exponential approximation–1 with different k values.

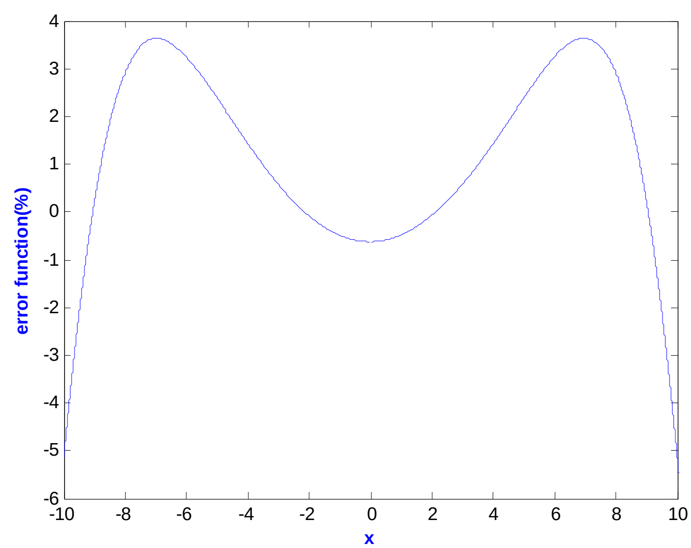


Figure 2.30: The error function (k = 0.15) of the curve given in Figure 2.29.

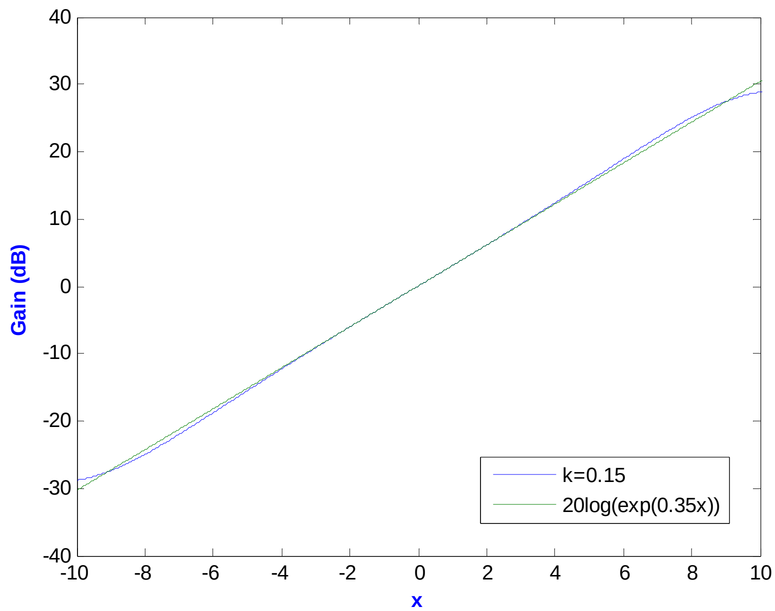


Figure 2.31: Comparison of the ideal exponential function and the composition of Taylor and pseudo approximation–1.

Comparison of the ideal exponential function and the composition of Taylor and pseudo exponential approximation are shown in Figure 2.31 and it is seen that the dynamic range equals to 60dB.

To realize the equation (2.43), the control circuit like Figure 2.32 can be used.

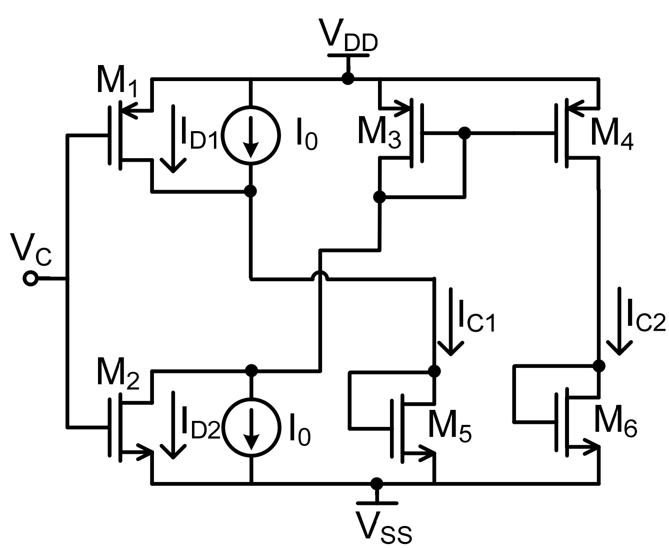


Figure 2.32: Control circuit schematic of a VGA [56].

In Figure 2.32, the drain currents of M_1 and M_2 are given in equations (2.46) and (2.47).

Due to Kirchhoff current law, when I_{C1} equals to the summing of I_{D1} and I_0, which is shown in equation (2.48) and also the equation (2.49)

$$I_{D1} = K_p(V_C - V_{DD} + |V_{THp}|)^2 \tag{2.46}$$

$$I_{D2} = K_n(V_C - V_{SS} + V_{THn})^2 \tag{2.47}$$

$$I_{C1} = K_p(V_{DD} - |V_{THp}|)^2 \left\{ \frac{I_0}{K_p(V_{DD} - |V_{THp}|)^2} + (1 + \frac{V_C}{(V_{DD} - |V_{THp}|)})^2 \right\} \tag{2.48}$$

$$I_{C2} = K_n(V_{SS} - V_{THn})^2 \left\{ \frac{I_0}{K_n(V_{SS} - V_{THn})^2} + (1 + \frac{V_C}{(V_{SS} - V_{THn})})^2 \right\} \tag{2.49}$$

If it is assumed that $K_p = K_n$, $V_{DD} = -V_{SS}$ and $V_{THn} = -V_{THp}$, then from equations (2.48) and (2.49), the ratio of I_{C2}/I_{C1} can be given by equation (2.50). When this equation is compared to (2.44), k equals to $I_0/K(V_{DD}-V_{TH})^2$ and a equals to $1/(V_{DD}-V_{TH})$.

Furthermore, if a function of a gain block includes a current ratio like I_{C2}/I_{C1}, an exponential control like in equation (2.50) can be used and wide dynamic range can be obtained.

$$\frac{I_{C2}}{I_{C1}} = \frac{\frac{I_0}{K(V_{DD}-V_{TH})^2} + (1 + \frac{V_C}{(V_{DD}-V_{TH})})^2}{\frac{I_0}{K(V_{DD}-V_{TH})^2} + (1 + \frac{V_C}{(V_{DD}-V_{TH})})^2} \tag{2.50}$$

2.2.4.3 A composition of Taylor and pseudo exponential approximation–2

Another composition of Taylor series and pseudo exponential approximation, given in (2.51), is composed by using Taylor series approximation [50].

$$f(x) = \frac{1 + ax + k(ax)^2/2}{1 - ax + k(ax)^2/2} \tag{2.51}$$

Hereby, composed Taylor series and pseudo exponential approximation with different k values and an ideal exponential function is shown in Figure 2.33. When k equals to 0.55, the function provides maximum dynamic range. The error function (k = 0.55) of the curve is shown in Figure 2.34.

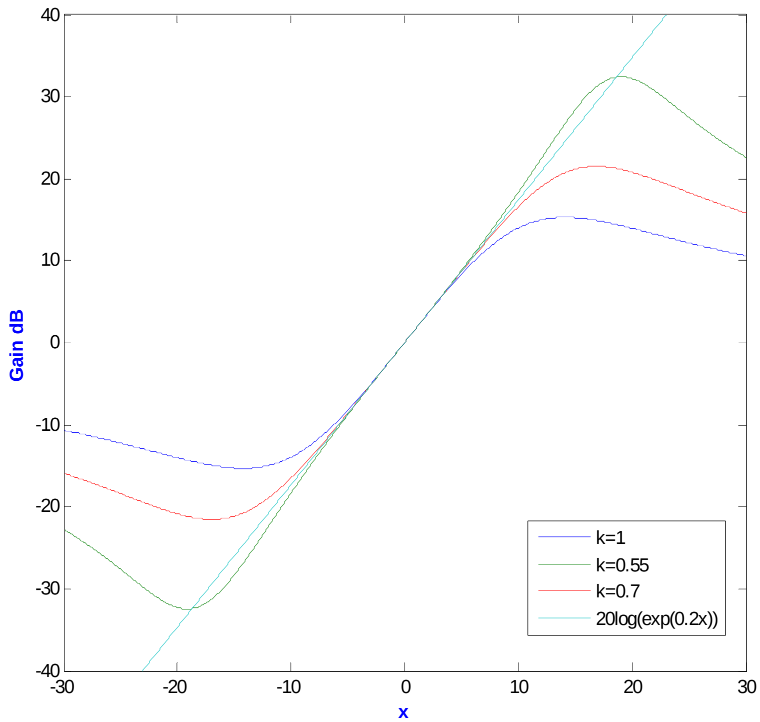


Figure 2.33: A composition of Taylor series and pseudo exponential approximation 2 with different k values and an ideal exponential function.

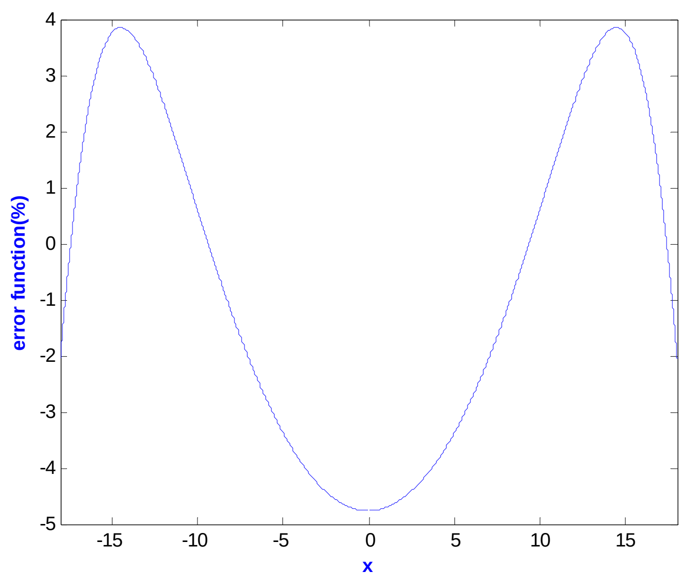


Figure 2.34: The error function (k = 0.55) of the curve which is shown in Figure 2.31.

The error function (k = 0.55) of the curve is shown in Figure 2.34.When the x values are chosen like in Figure 2.34, the comparison of the ideal exponential function and the composed Taylor and pseudo exponential approximation–2 (k = 0.55) can be plotted in Figure 2.35. As it is seen from Figure 2.35, the dynamic range of function is 65 dB.

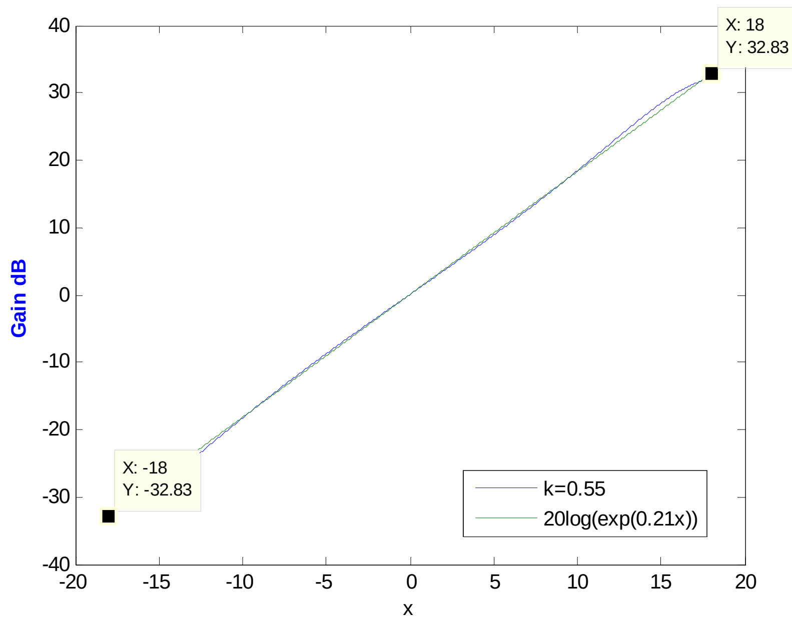


Figure 2.35: Comparison of the ideal exponential function and the composition of Taylor and pseudo approximation–2.

2.2.5 Exponential function with using differential equations

In Figure 2.36, transistor M0 is a PMOS transistor operating in linear region and in common-source configuration.

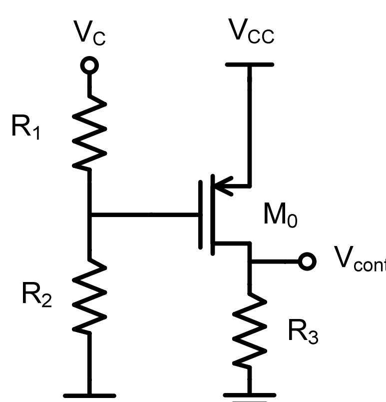


Figure 2.36: Exponential converting circuit [46].

The transconductance of the transistor $g_{m,M0}$ and dV_{cont}/dV_C of M_0 can be expressed by:

$$g_{m,M0} = \beta(V_{CC} - V_{cont}) \quad \textbf{(2.52)}$$

$$\frac{dV_{cont}}{dV_C} = -\frac{R_1}{R_2+R_1} g_{m,M0} R_3 = K_2(V_{CC} - V_{cont}) \quad \textbf{(2.53)}$$

If condition of the equation (2.54) is provided, by using differential equation like in (2.55), then (2.56) and (2.57) can be obtained.

$$K_2 = \frac{R_1 R_3}{R_2+R_1}\beta > 0 \quad \textbf{(2.54)}$$

$$\frac{d(V_{CC} - V_{cont})}{(V_{CC} - V_{cont})} = K_2 dV_C \quad \textbf{(2.55)}$$

$$\frac{d(V_{CC} - V_{cont})}{(V_{CC} - V_{cont})} = K_2 dV_C \quad \textbf{(2.56)}$$

$$\ln(V_{CC} - V_{cont}) = K_2 V_C + C \quad \textbf{(2.57)}$$

$$V_{CC} - V_{cont} = e^{K_2 V_C + C} \quad \textbf{(2.58)}$$

If the gain equation includes V_{CC}-V_{cont}, then this gain could be varied by V_C, as it is seen from equation (2.58).

2.3 Chapter Summary

The gain control block has different control functions in literature. These control functions could be classified into two groups as continuous and discrete functions.

VGA with a continuous control function can also be classified as linear and exponential ones.

In order to provide the exponential control function, DC current voltage characteristic of a bipolar transistor, a MOSFET operating in subthreshold region and some of the approximated equations which are using the linear or saturation region characteristics of the MOSFET can be used. Also, exponential representation using differential equations in a loop are possible.

All of the approximation functions in literature and the corresponding error functions are implemented and compared using MATLAB.

Moreover, the basic circuit examples are given for all of these control functions.

3. BASIC CIRCUIT STRUCTURES OF THE GAIN BLOCK OF THE VGA

The basic structures of the gain block of the VGA can be classified into four circuit structures:

- Variable Feedback Structure
- Variable Biasing Structure
- Cascode Structure
- Current Steering Structure

3.1 Variable Feedback Structure

The gain is varied with using variable gain resistor or switchable capacitor in the feedback structure. In Figure 3.1, an example of a variable gain cell with using variable gain resistor is shown and the MOSFET operating in triode region is used as a variable gain resistor at the variable feedback structure of the common emitter circuit.

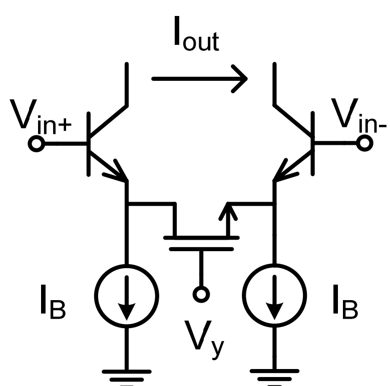


Figure 3.1: A common emitter circuit structure with variable feedback.

Generally, in literature, variable feedback structure is used as a variable resistor in the feedback loop of an amplifier or a common emitter circuit structure with variable feedback resistor.

Firstly, variable feedback resistor in the feedback loop of an amplifier is shown in Figure 3.2 and the variable feedback resistor is used as a floating resistor (R_{float}) [47].

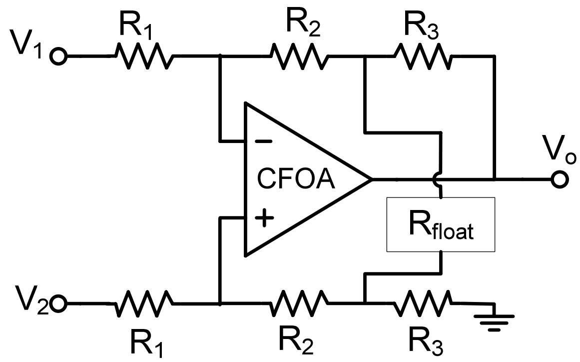


Figure 3.2: Variable gain amplifier using floating resistor [47].

The gain equation of Figure 3.2 is given in equation (3.1).

$$\frac{V_o}{V_2 - V_1} = \frac{R_2}{R_1}\left(1 + \frac{R_3}{R_2} + \frac{2R_3}{R_{float}}\right) \quad \textbf{(3.1)}$$

As it is seen from equation (3.1), gain variation is provided with variable resistor (R_{float}).

Secondly, the MOSFET operating in triode region is used as a variable gain resistor at the variable feedback structure of the common emitter circuit [21, 22, 23, 53, 58, 70, 73] is shown in Figure 3.3.

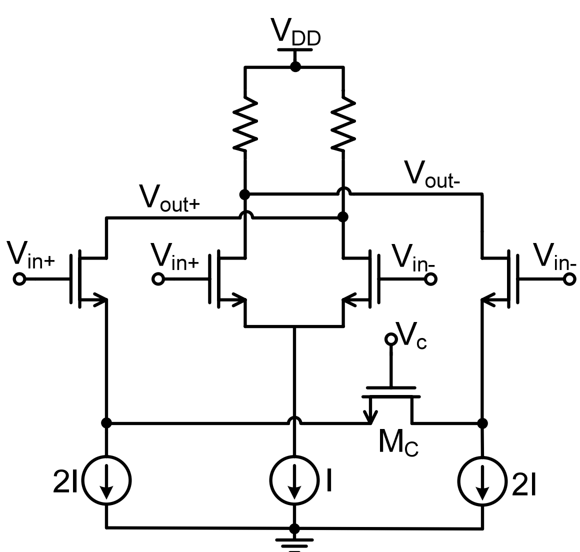


Figure 3.3: The MOSFET operating in triode region is used as a variable gain resistor in the variable feedback structure [8].

To obtain the gain function of Figure 3.3, firstly the circuits in Figure 3.4 and Figure 3.5 are examined.

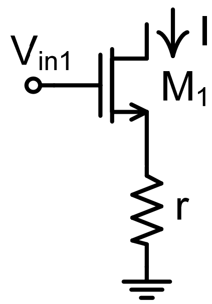


Figure 3.4: A MOSFET with a resistor at the source node.

A MOSFET with a resistor at the source node is shown in Figure 3.4 and the transconductance is given in (3.2).

$$g_m = \frac{1}{r + {}^{1}/_{g_{m1}}} \qquad \textbf{(3.2)}$$

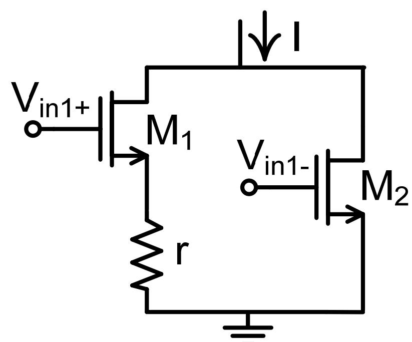


Figure 3.5: A two MOS transconductance circuit.

Also in Figure 3.5, with proper biasing of M_1 and M_2, g_{m1} is chosen as the twice of g_{m2}. With this proper biasing G_m can be shown in equation (3.3).

$$G_m = -\frac{1}{2} g_{m1} \left(\frac{r - {}^{1}/_{g_{m1}}}{r + {}^{1}/_{g_{m1}}} \right) \qquad \textbf{(3.3)}$$

The g_m equation (3.3) also equals to the g_m equation of Figure 3.3.

The comparison of the variable gain cells which are used variable feedback structure is given in Table 3.1.

Furthermore, the high linearity of the variable feedback structure is an advantage, but the stability problem is a disadvantage. Also, because of the unstable conditions of the circuit, the gain control is limited.

Table 3.1: The comparison of the VGAs with using variable feedback structure.

Ref.	Process	Supply Voltage (V)	Gain Range (dB)	f_{-3Db} (MHz) Operating Band	Power Consumption (mW)	NF (dB)
[7]	BiCMOS	3.6	45	250	N/A	5
[8]	0.18μm CMOS	1.8	86.6	1500	25.1	8
[17]	0.18μm CMOS	0.5	49	10	0.025	N/A
[20]	0.35μm CMOS	3	20	10	12	N/A
[47]	N/A	N/A	7	N/A	N/A	N/A
[66]	0.6μm CMOS	3	70	110	18	N/A
[63]	0.35μm CMOS	1.5	20	10	0.9	N/A

3.2 Variable Biasing Structure

Variable biasing structure is formed with varying the biasing current or voltage in the gain cell like in Figure 3.6. The low noise is an advantage of the structure, but the disadvantage of the circuit, linearity of the amplifier depends on the biasing current.

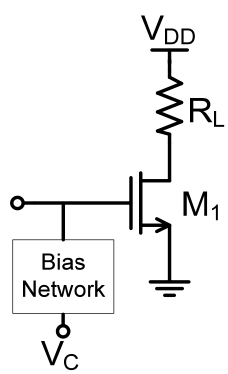


Figure 3.6: Variable biasing structure.

In literature, the example circuits of variable biasing structure are shown in Figure 2.19 [4, 6, 23, 24, 35, 48, 49-53] and Figure 2.20 [19, 12, 78].

In Figure 2.19, the gain cell is biased with currents I_a and I_b. The gain variation is provided by changing these I_a and I_b currents with the MOSFETs in saturation region.

In Figure 2.20, transistors M_2 and M_3 are biased with currents I_B and I_C. The gain variation is provided by changing these currents with the MOSFETs in linear region.

Also, the comparison of the VGAs which are used variable biasing structure is shown in Table 3.2.

Table 3.2: The comparison of the VGAs with using variable biasing structure.

Ref.	Process	Supply Voltage (V)	Gain Stage	Gain (dB)	f_{-3dB} (MHz) Operating Band	Power Consumption (mW)
[4]	0.18μm CMOS	N/A	3	83	37	6.12
[5]	Si bipolar	N/A	1	77	400	16.2
[6]	0.13μm CMOS	N/A	N/A	54	743	8.1
[12]	0.5μmCMOS	2	N/A	50.7	0.134@3.8dB	0.002
[19]	0.5μm CMOS	±1.5	1	30	21.9	0.48
[23]	0.18μm CMOS	N/A	N/A	12	700	3.6
[24]	0.18μm CMOS	1.8	3	73	380	10.8
[35]	0.18μm CMOS	1.8	2	N/A	32	6.5
[48]	0.6μm CMOS	3	2	34	1	21
[49]	0.5μm CMOS	3.3	1	15	20	12.5
[50]	0.18μm CMOS	N/A	N/A	90	50@G_{max}	6.66
[51]	0.35μm CMOS	3.3	N/A	32	46 ÷ 267	4.63
[52]	0.18μm CMOS	N/A	N/A	84	1@G_{max}	6.48
[53]	0.18μm CMOS	1.8	3	60	16	3.6
[78]	0.5μm CMOS	±1.5	N/A	15	N/A	0.4

3.3 Cascode Structure

In Figure 3.7, a simple cascode structure is shown. The cascode structure has a common source device with a common gate load. It provides to increase the output impedance and to decrease the Miller capacitance that appears at the input is much smaller than that of a simple common source amplifier so that we can easily obtain a high frequency response.

With varying V_{CTRL} voltage, the gate voltages of cascode transistors M_3 and $M_4$is changed. Therefore, the operation region of input transistors M_1 and M_2 is changed. This provides to be able to vary the gain.

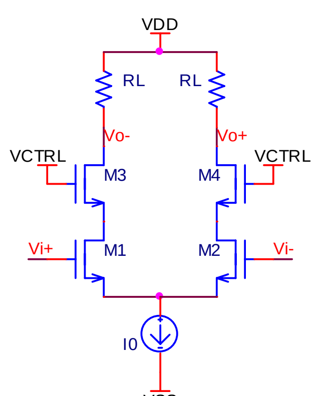


Figure 3.7: Cascode structure.

With changing V_{CTRL}, the operation regions of M_1-M_4 transistors are changed. Four different operations are examined and the gain variation is examined for each operation.

Firstly, when M_1 and M_2 operate in triode region and M_3 and M_4 operate in saturation region, the gain equation (3.4) is written for M_1 from the input (v_i) to the drain of M_1 (v_o'). R_1 equals to $1/g_{m1}$ and g_{m1} is given in (3.9).

$$\frac{v_o'}{v_i} = \frac{1}{2} g_{m1}(R_1 // \frac{1}{g_{m3}}) \tag{3.4}$$

The gain equation (3.5) is written for M_3 from the drain of M_1 (v_o') to the output. Because of the operation region of M_3-M_4, g_{m3} equals to square root of $2\beta I_3$.

$$\frac{v_o}{v_o'} = \frac{R_L}{R_1 + \frac{1}{g_{m3}}} \tag{3.5}$$

The whole gain when M_1 and M_2 operate in triode region and M_3 and M_4 operate in saturation region is given in equation (3.6).

$$\frac{V_o}{V_i} = \frac{1}{2} g_{m1}(R_1 // \frac{1}{g_{m3}}) \frac{R_L}{R_1 + \frac{1}{g_{m3}}} \tag{3.6}$$

If drain current of M_3 transistor is given like in equation (3.7), because of the drain voltage of M_1 equals to source voltage of M_3, the drain voltage of M_1 can be given in equation (3.8).

$$I_3 = \frac{\beta}{2}(V_{CTRL} - V_{S3} - V_{TH})^2 \tag{3.7}$$

$$V_{D1} = V_{CTRL} - (\sqrt{\frac{2I_3}{\beta}} + V_{TH}) \tag{3.8}$$

As it is seen from the equation (3.9), transconductance of M_1 can be varied by V_{CTRL}. Therefore, the gain can be varied by V_{CTRL}.

$$g_{m1} = \beta V_{DS1} = \beta\left[\left(V_{CTRL} - \sqrt{\frac{2I_3}{\beta}} - V_{TH}\right) - V_{S1}\right] \quad \textbf{(3.9)}$$

Also, V_{DS1}can be written like in equation (3.10) [54]. In this equation, A equals to $2I_{DS}/\beta$ and V_X is given in (3.11).

$$\frac{V_{DS1}}{\sqrt{2A}} = V_X + \sqrt{V_X^2 + 1} \quad \textbf{(3.10)}$$

$$V_X = \frac{V_C - V_{TH2} - (V_{in} - V_{TH1})}{\sqrt{2A}} - \frac{1}{\sqrt{2}} \quad \textbf{(3.11)}$$

While $|V_X| \leq 1$, inverse hyper tangent function is given in (3.12). Therefore, transconductance of M_1 has an exponential characteristic because of the inverse hyper tangent function of V_{DS1}.

$$V_X + \sqrt{V_X^2 + 1} \approx e^{V_X} \quad \textbf{(3.12)}$$

Secondly, when M_1-M_2 operate in saturation region, M_3-M_4 operate in triode region, the gain from input to the output is given in equation (3.15) with using (3.13) and (3.14).Here, g_{m1} is given in equation (3.16).

As it is seen from the gain equation (3.15), g_{m1} or R_L does not change, therefore the gain is not varied, when M_1-M_2operate in saturation region, M_3-M_4 operate in triode region.

$$\frac{V_o'}{V_i} = \frac{1}{2} g_{m1}(R_{3,4} + R_L) \quad \textbf{(3.13)}$$

$$\frac{V_o}{V_o'} = \frac{R_L}{R_{3,4} + R_L} \quad \textbf{(3.14)}$$

$$\frac{V_o}{V_i} = \frac{1}{2} g_{m1} R_L \quad \textbf{(3.15)}$$

$$g_{m1} = \sqrt{2\beta I_D} \quad \textbf{(3.16)}$$

Thirdly, when M_1-M_4operate in saturation region, the total gain is given in equation (3.19) with multiplying (3.17) and (3.18).Here, g_{m1} and g_{m3} equal to square root of 2βI. Furthermore, the gain is not varied as it is seen from equation (3.17),

$$\frac{V_o'}{V_i} = -\frac{g_{m1}}{2g_{m3}} \tag{3.17}$$

$$\frac{V_o}{V_o'} = g_{m3}(R_L//g_{m3}r_{o3}r_{o1}) \tag{3.18}$$

$$\frac{V_o}{V_i} = -\frac{1}{2}g_{m1}R_L \tag{3.19}$$

Fourthly, when M_1-M_2 operate in triode and M_3-M_4 operate in subthreshold region. The total gain can be obtained when equations (3.20) and (3.21) are multiplied. Due to the operation region of M_1 and M_3, R_1 and g_{m3} are given equations (3.22) and (3.23).

From the gain equations (3.20) and (3.21), the gain is not varied.

$$\frac{V_o'}{V_i} = \frac{1}{2}g_{m1}(R_1//\frac{1}{g_{m3}}) = \frac{1}{2}g_{m1}R_1 \tag{3.20}$$

$$\frac{V_o}{V_o'} = \frac{R_L}{R_1 + \frac{1}{g_{m3}}} \tag{3.21}$$

$$R_1 = \frac{1}{\beta(V_{GS1}-V_{TH})} \tag{3.22}$$

$$g_{m3} = \frac{I_D}{\zeta V_T} \tag{3.23}$$

Four different operations are examined and it is seen that when M_1 and M_2 operate in triode region and M_3 and M_4 operate in saturation region, the gain variation can be obtained.

In literature, there are many VGAs which have cascode structure in the gain cell. In thesis work, these structures are simulated in 0.35µm CMOS process with using PSPICE.

Firstly, the circuit in Figure 3.8 is simulated and the gain variation, bandwidth and linearity is observed. In the circuit, a variable gain amplifier has cascode structure and active load and also biasing structure M_9-M_{12}. This biasing structure also provides common mode feedback and constant output current. The dimensions of the transistors in the circuit are given in Table 3.3.

The active load of the circuit in Figure 3.8 is given in equation (3.24) and as it is seen from the equation, it acts like an inductive load in the high-frequency region,

$$Z_o = \frac{1}{g_{m13}} + \frac{sc_1}{g_{m13}g_{m15}} \quad \textbf{(3.24)}$$

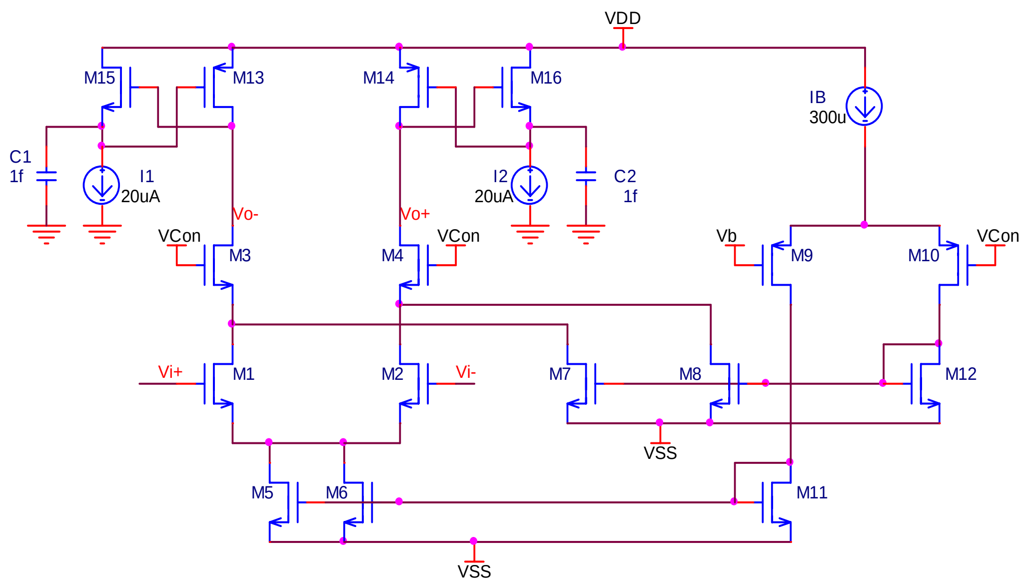


Figure 3.8: A variable gain amplifier with cascode structure and active load [54].

The dynamic range of the circuit in Figure 3.8 is 20.8 dB as it is seen from Figure 3.9. Moreover, in Figure 3.9, bandwidth of the circuit can be observed. When the gain is maximum and equal to 11.4 dB, the bandwidth is 764MHz. Also, when the gain is minimum and equal to -12dB, the bandwidth is 956MHz.

Table 3.3: The dimensions of the transistors in the circuit given in Figure 3.8.

Transistor	W (µm)	L (µm)
M1, M2	10	0.35
M3, M4	30	0.35
M5-M8, M11, M12	50	0.35
M9, M10	30	0.35
M13, M14	3	0.35
M15, M16	100	0.35

While the gain differs from the ideal function ±1.5dB, the total dynamic range is 20.8dB. Also, the power consumption of the circuit in Figure 3.8 is 2.43mW.

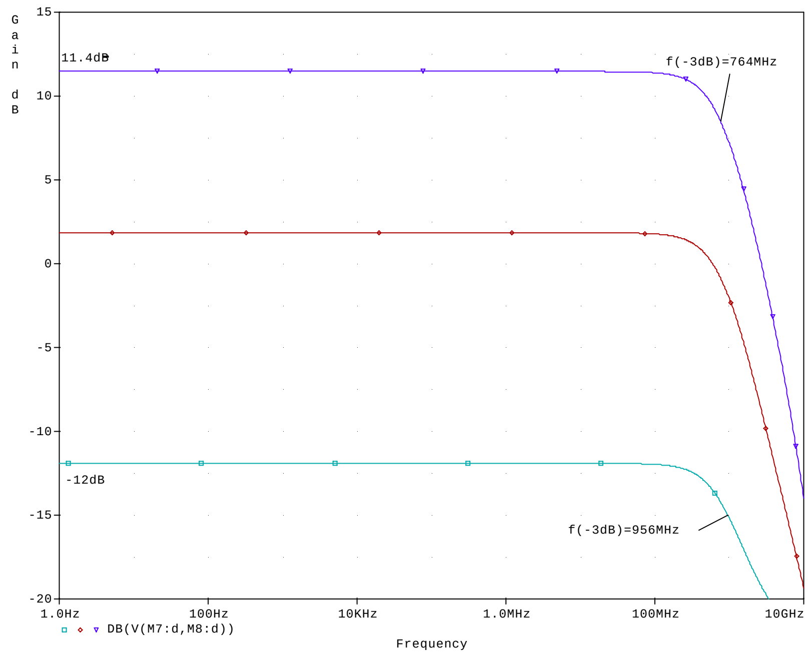


Figure 3.9: The AC characteristic of the circuit in Figure 3.8 while varying V_C.

Furthermore, the comparison of the ideal exponential function and the gain function of the circuit in Figure 3.8 is shown in Figure 3.10.

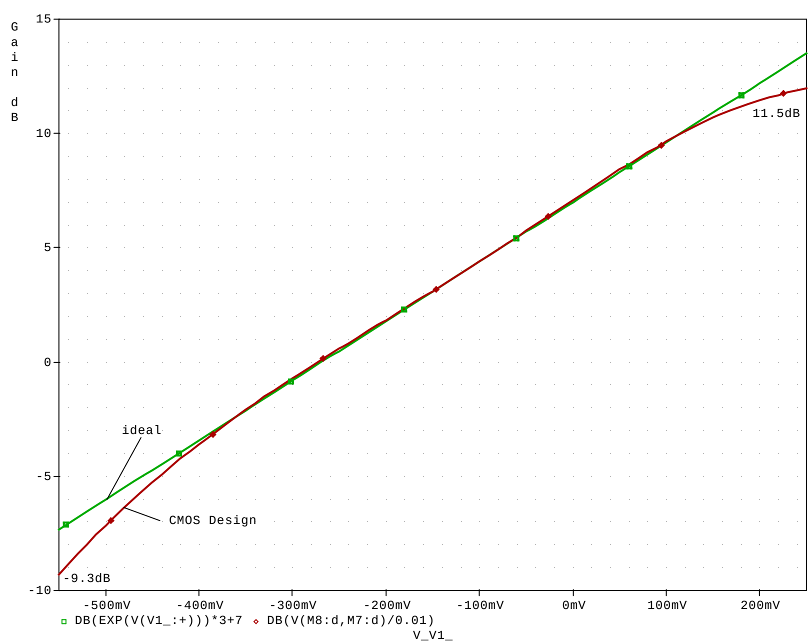


Figure 3.10: The comparison of the ideal exponential function and the gain function of the circuit in Figure 3.8 while varying V_C.

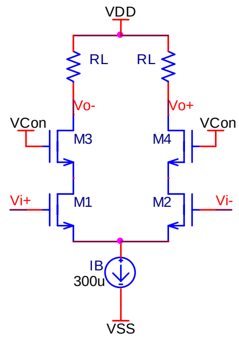


Figure 3.11: A VGA with cascode structure and resistive load [55].

Secondly, a VGA with cascode structure and resistive load is shown in Figure 3.11 and it is simulated and the gain variation, bandwidth and linearity is observed.

The dimensions of the transistors in the circuit are given in Table 3.4.

Table 3.4: The dimensions of the transistors in the circuit given in Figure 3.11.

Transistor	W (µm)	L (µm)
M1, M2	3	0.35
M3, M4	10	0.35

The dynamic range is observed as 19dB from Figure 3.12 and Figure 3.13. In Figure 3.12, the maximum and minimum values of the gain are 0dB and -18dB, and between these gain values, bandwidth of the circuit in Figure 3.11 is between 816MHz and 883MHz. Also, the power consumption of the circuit is 0.9mW.

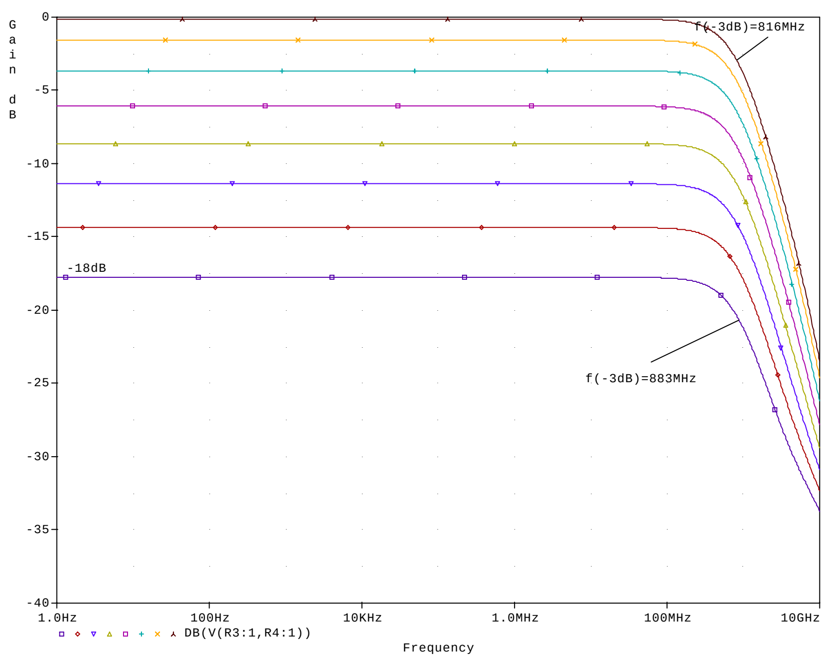


Figure 3.12: The AC characteristic of the circuit in Figure 3.11while varying V_C.

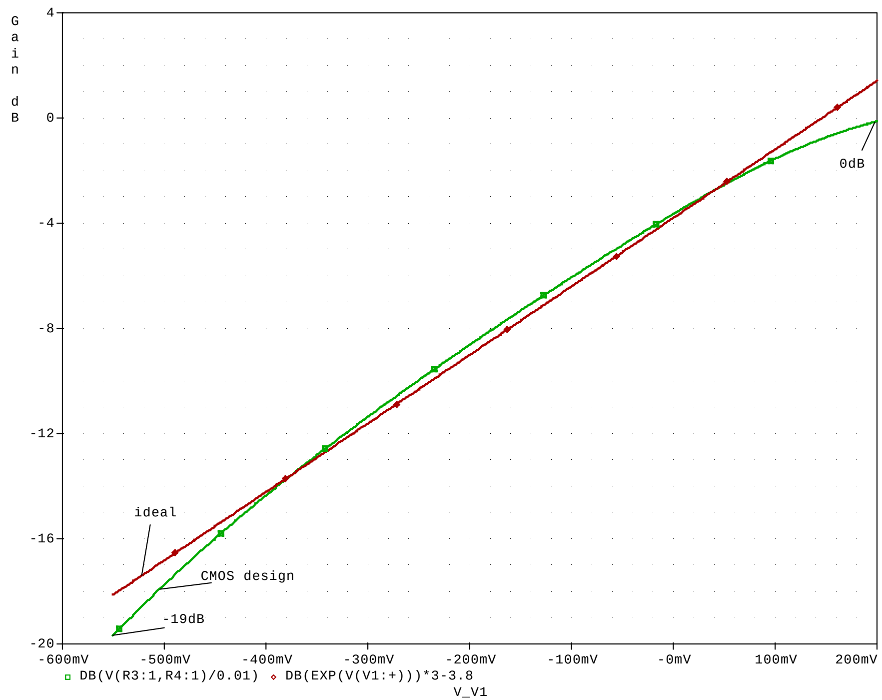


Figure 3.13: The comparison of the ideal exponential function and the gain function of the circuit in Figure 3.11 while varying V_C.

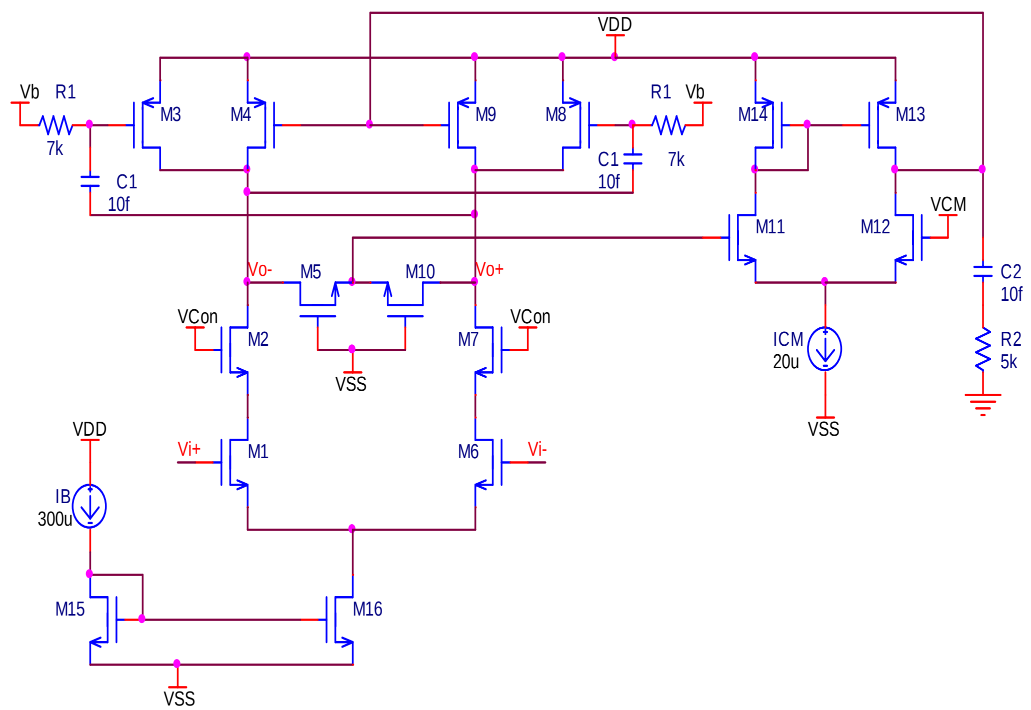


Figure 3.14: A VGA with cascode structure with active load and CMFB [42].

Thirdly, a VGA with cascode structure with active load and CMFB are shown in Figure 3.14. The dimensions of the transistors in the circuit are given in Table 3.5.

Table 3.5: The dimensions of the transistors in the circuit given in Figure 3.14.

Transistor	W (μm)	L (μm)
M1-M12	10	0.35
M13, M14	30	0.35
M15, M16	20	0.7

The simulation results of the circuit are shown in Figure 3.15 and Figure 3.16. As it is shown in Figure 3.15 , the dynamic range of the circuit is 24dB and the bandwidth of the circuit is between 900MHz and 1GHz. The comparison of the ideal exponential function and the gain function is shown in Figure 3.16. Also, the power consumption of the circuit is 1.68mW.

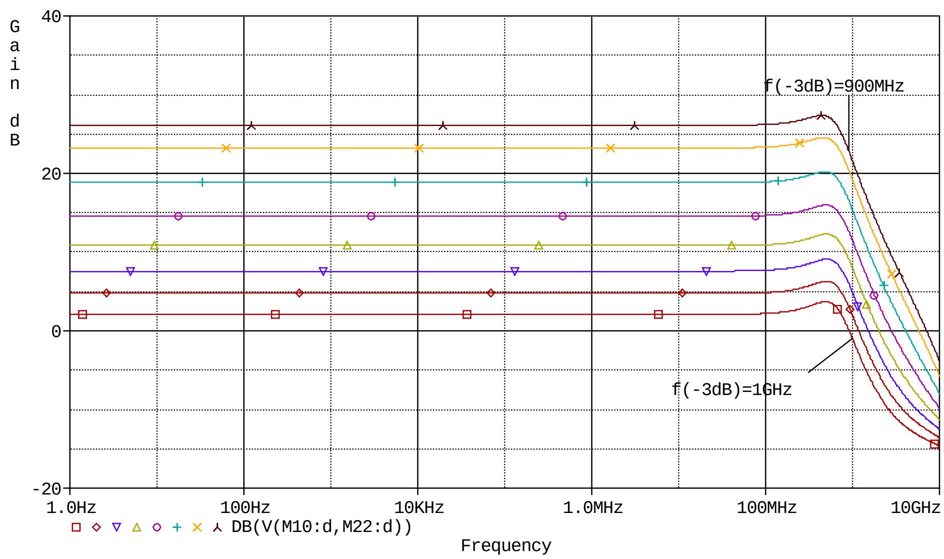


Figure 3.15: The AC characteristic of the circuit in Figure 3.14 while varying V_C.

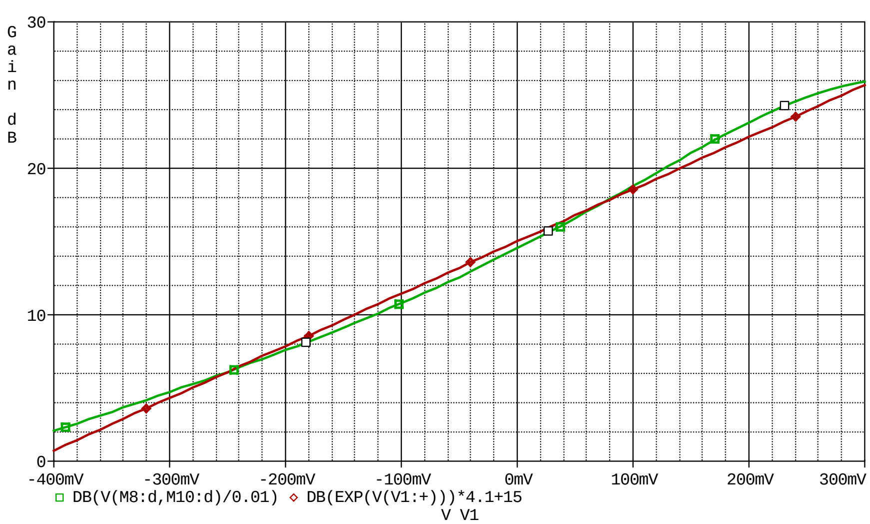


Figure 3.16: The comparison of the ideal exponential function and the gain function of the circuit in Figure 3.14 while varying V_C.

Fourthly, a VGA with active load and with improved input cascode stage is shown in Figure 3.17 and the dimensions of the transistors in the circuit are given in Table 3.6.

Improved input stage provides higher dynamic range than the classic differential cascode stage. In input stage, M_1-M_4 are operated in triode region for better linearity and M_6-M_8 provide variable gain with changing the V_{DS} of the M_1-M_4. When V_{C_int1} is high M_7-M_8 go on and M_5-M_6 go off because of the lower V_{C_int2}, and the gain is increased. On the other hand, when V_{C_int2} is high and V_{C_int1} is low, M_5-M_6 go on and M_7-M_8 go off, and the gain is decreased.

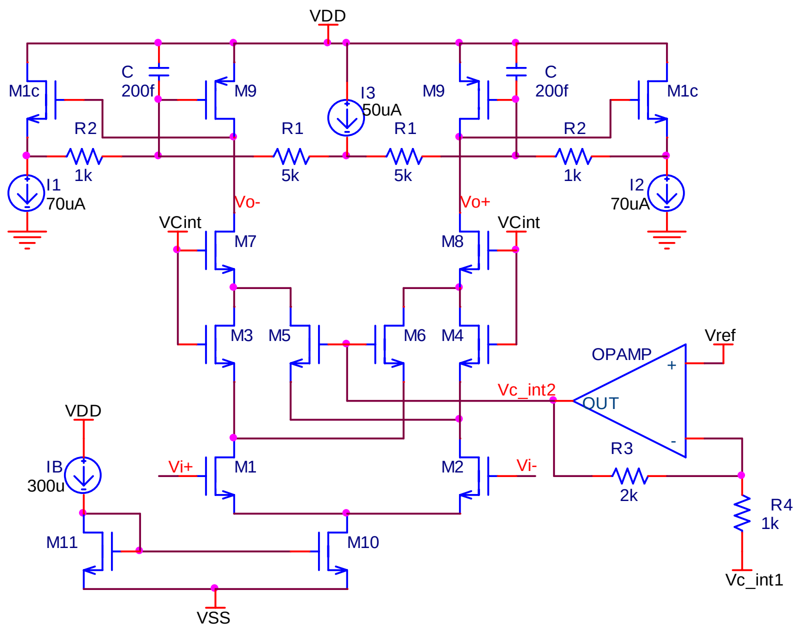


Figure 3.17: A VGA with active load and with improved input cascade stage [56].

Table 3.6: The dimensions of the transistors in the circuit given in Figure 3.17.

Transistor	W (µm)	L (µm)
M1-M4	50	0.35
M5, M6	5	0.35
M7, M8	80	0.35
M9	3	0.7
M1c	70	0.35
M10, M11	60	1

The simulation results of the circuit are shown in Figure 3.18 and Figure 3.19. As it is shown in Figure 3.18, the dynamic range of the circuit is 33dB and the bandwidth of the circuit is between 556MHz and 707MHz.

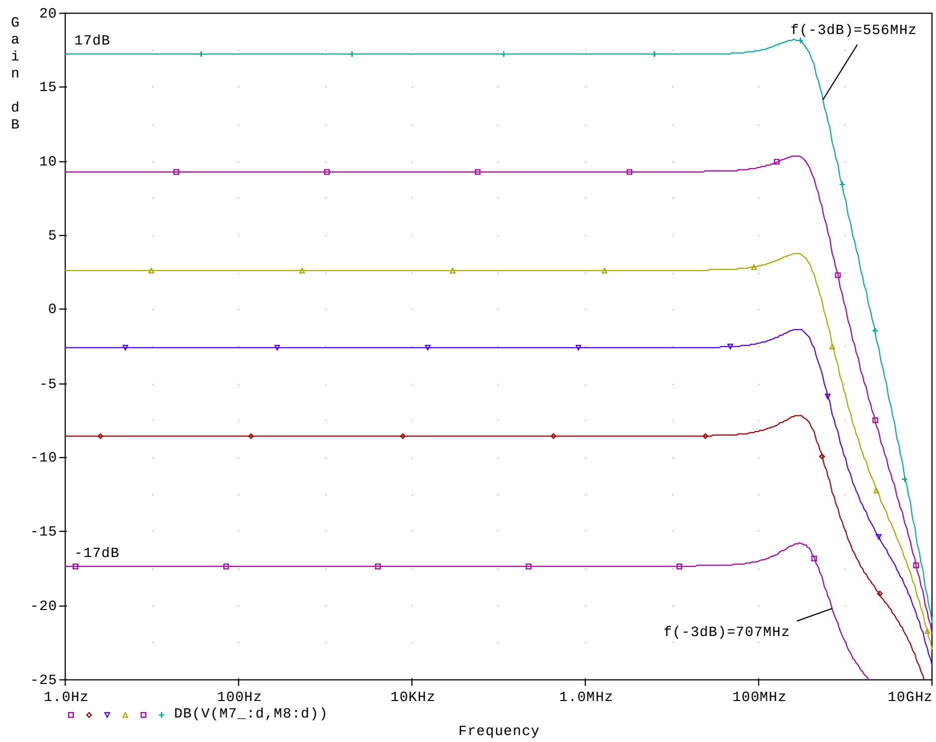


Figure 3.18: The AC characteristic of the circuit in Figure 3.17while varying V_C.

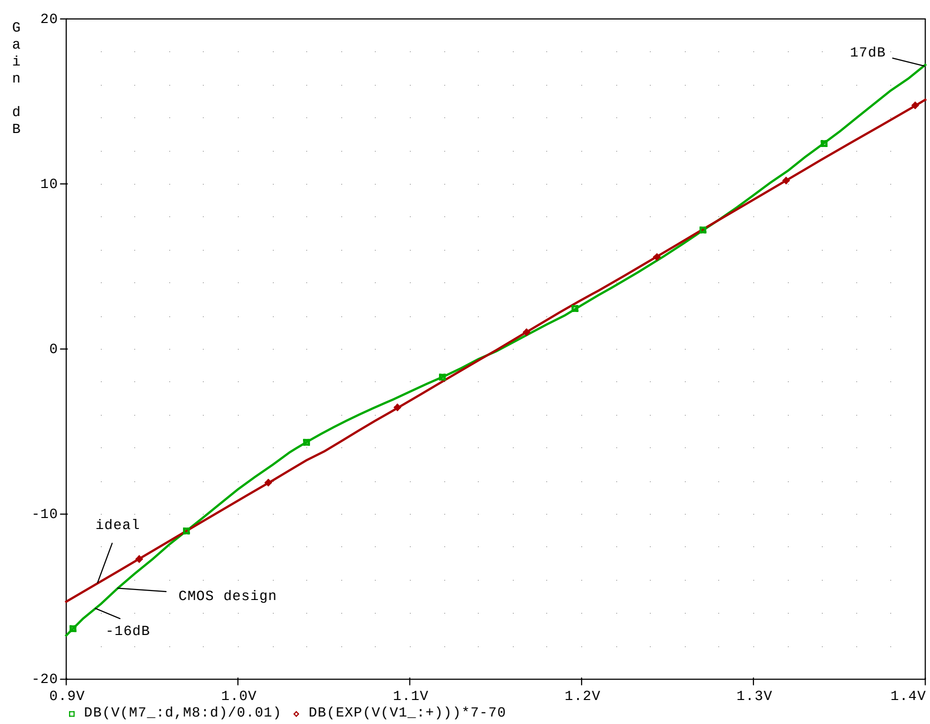


Figure 3.19: The comparison of the ideal exponential function and the gain function of the circuit in Figure 3.17 while varying V_C.

As it is seen from the simulation result, the dynamic range of this circuit is better than the other cascode structures because of the improved dynamic range. The comparison of the ideal exponential function and the gain function is shown in Figure 3.19. The power consumption is 2.61mW.

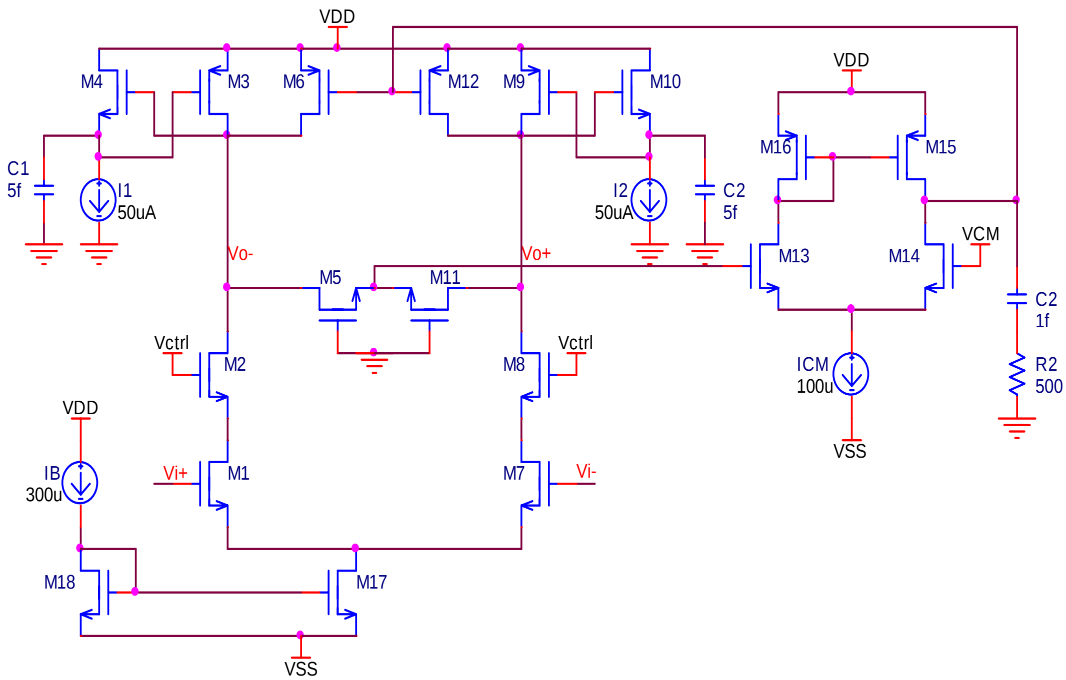


Figure 3.20: A VGA with cascode structure with active load and current bleeding structure [3].

Fifthly, A VGA with cascode structure with active load and current bleeding structure is shown in Figure 3.20. M_6 and M_{12} are formed that current bleeding structure and this structure increase the value of load with decreasing the current of the load.

The dimensions of the transistors in the circuit are given in Table 3.7.

Table 3.7: The dimensions of the transistors in the circuit given in Figure 3.20.

Transistor	W (μm)	L (μm)
M1, M7	2	0.35
M2, M5, M8, M11, M13, M14	10	0.35
M6, M12	40	0.35
M3, M9	4	0.35
M4, M10	75	0.35
M15, M16	20	0.35
M17, M18	20	0.7

The simulation results of the circuit are shown in Figure 3.21 and Figure 3.22. As it is shown in Figure 3.21, the dynamic range of the circuit is 20.2dB and the bandwidth of the circuit is between 1.18GHz and 1.1GHz. The comparison of the ideal exponential function and the gain function is shown in Figure 3.22. The power consumption is 1.59mW.

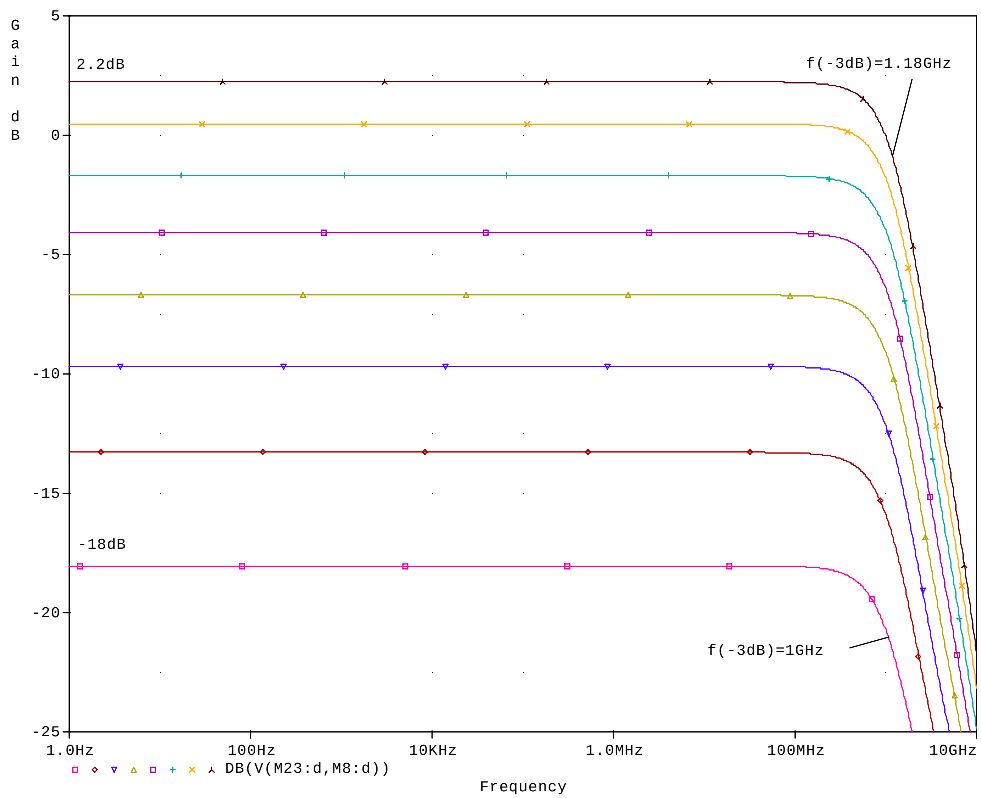


Figure 3.21: The AC characteristic of the circuit in Figure 3.20 while varying V_C.

In Table 3.8, the comparison of simulation results of the cascode structures in [3, 42, 54-56] is shown.

In all cascode references [3, 42, 54-56] differential cascode structure is used. Generally, the differential stage is used for suppressing even harmonics, rejecting common-mode noises and doubling the signal swing and also the cascode structure improves bandwidth with using Miller effect. Moreover, an active load is used in [3, 42, 54, 56] to provide wide bandwidth and improve the signal swing.

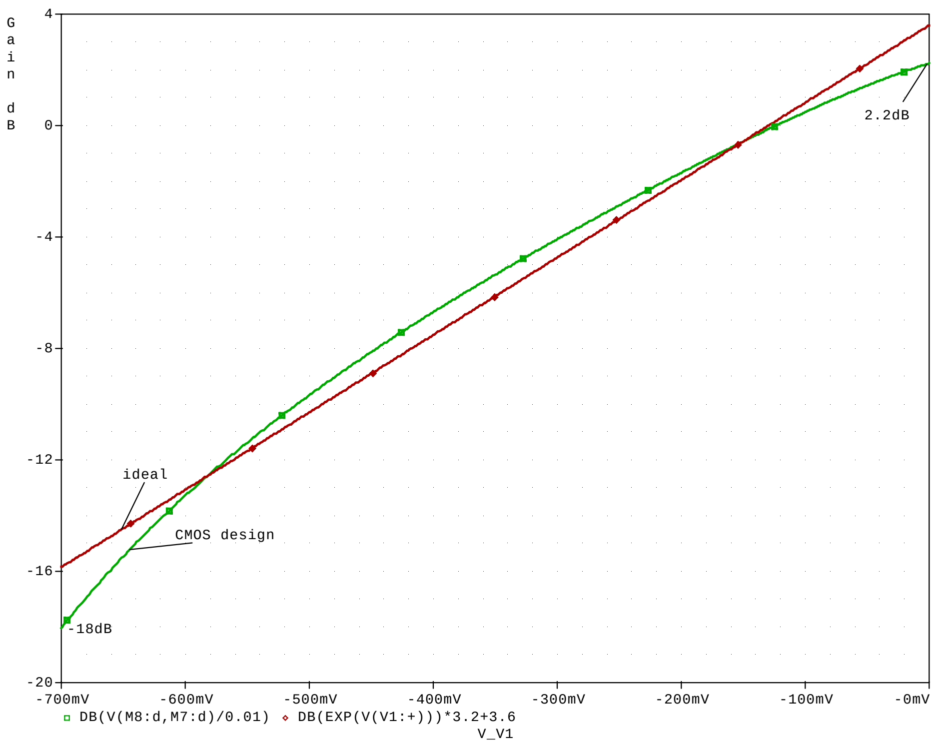


Figure 3.22: The comparison of the ideal exponential function and the gain function of the circuit in Figure 3.20 while varying V_C.

In references [3, 42, 55-56], a constant current bias is used for a good linearity and wideband performance regardless of control voltages. Also, a common mode feedback (CMFB) is used to obtain constant output DC level.

Table 3.8: The comparison of simulation results of the cascade structures.

References	Dynamic Range	Bandwidth	Power Consumption
[54]	20.8dB	764MHz	2.43mW
[55]	19dB	816MHz	0.9mW
[42]	24dB	900MHz	1.68mW
[56]	33dB	556MHz	2.61mW
[3]	20.2dB	1.18GHz	1.59mW

3.4 Current Steering Structure

The circuit in Figure 3.23, cascode transistors are used to steer the current to and from the load. It provides high gain control range but it suffers more from noise than other approaches. Noise analysis of the circuit is given in [41].

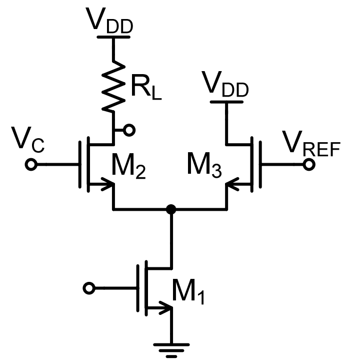


Figure 3.23: A current steering structure [41].

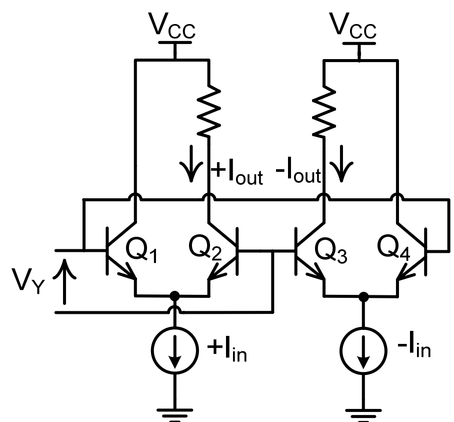


Figure 3.24: Signal summing VGA [11].

A signal summing or current steering VGA in Figure 3.24 is advantageous in terms of low-noise and low-distortion characteristics. Also, it can operate at high frequency, because the gain-control stages operate as common-base transistors. The gain equation of the circuit in Figure 3.24 is given in (3.25).

$$\frac{I_{out+}}{I_{in+}} = \frac{1}{1 + e^{\frac{V_Y}{V_T}}} \qquad \textbf{(3.25)}$$

In literature, to be able to obtain more variable gain range and to have a better linear in dB characteristic, 1 is subtracted from the denominator [11, 57].V_Y is chosen like in equation (3.26), then the 1 can be subtracted from the denominator in the equation (3.25).

$$V_Y = V_T \ln\left(e^x - 1\right) \qquad \textbf{(3.26)}$$

$$\frac{I_{out+}}{I_{in+}} = e^{-x} \tag{3.27}$$

In Figure 3.25, gain cell with current steering structure is shown and its gain equation is given in (3.28).

$$A_V = (2\alpha - 1)g_{m5}R_{out} \tag{3.28}$$

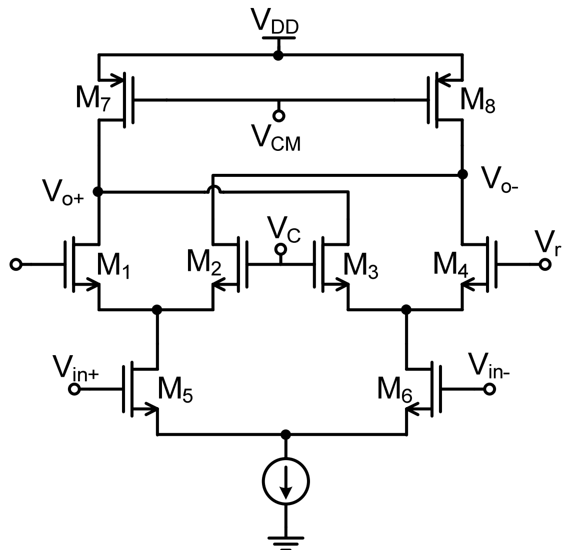


Figure 3.25: Gain cell with current steering structure [58].

α is the current gain and in order to have a linear in dB control gain, 2α-1 should have an exponential characteristic. α is given in equations (3.29), (3.30) and (3.31).

$$2\alpha - 1 = 2\frac{g_{m1}}{g_{m1} + g_{m2}} - 1 \tag{3.29}$$

$$2\alpha - 1 = 2\frac{\sqrt{I_1}}{\sqrt{I_1} + \sqrt{I_2}} - 1 \tag{3.30}$$

$$2\alpha - 1 = \frac{V_{GS1} - V_{GS2}}{V_{GS1} + V_{GS2} - 2V_T} \tag{3.31}$$

If V_{G1} and V_{G2} are chosen as $C+C_1e^t$ and $C-C_1e^t$, then the gain would be in (3.32) and can be exponentially controlled.

$$A_V = \frac{2C_1e^t}{2C - 2V_S - 2V_t}g_{m5}R_{out} \tag{3.32}$$

The comparison of VGAs with using current steering structure is shown in Table 3.9.

Table 3.9: The comparison of VGAs with using current steering structure.

Ref.	Process	Supply Voltage (V)	Gain Range (dB)	f_{-3dB} (MHz) Operating Band	Power Consumption (mW)	NF (dB)	Die Area (mm^2)
[11]	BiCMOS	3	39	50	18	5	1
[58]	0.18µm CMOS	1.8	47	400	6.1	13.8	N/A
[70]	0.25µm CMOS	2.5	27	380	21	11	N/A
[60]	BiCMOS	5	50	100	500	N/A	2.3

3.5 Chapter Summary

The basic circuit structures of the VGA gain block are classified into four which are variable feedback, variable biasing, cascode and current steering implementations.

A comparison is made to show advantages and disadvantages for each approach and example circuit implementations are given.

Moreover, cascade structure is examined deeply. Gain characteristics are examined in the control voltage range where the transistors operate in different regions.

Also, five different cascode structures given in the literature are implemented and simulated by using 0.35µm CMOS process to compare and show their performances.

4. NOVEL VGA STRUCTURES, EXPONENTIAL APPROXIMATION AND A NEW VGA MODEL

Two new VGA structures are designed in 0.35µm CMOS process with using SPICE to provide wide dynamic range and high frequency of operation. Also, a new exponential approximation function is proposed and a control block is realized by using a new approximation function. Moreover, a new model for the variable gain amplifier is constructed with using operational transconductance amplifiers and the proposed model is realized on board to verify the model performance.

4.1 Design of Two New VGA Structures

Two new circuits are proposed and simulated using 0.35µm CMOS process with SPICE and both circuits are linear in dB CMOS VGAs.

4.1.1 61dB dynamic range 1.2GHz linear in dB CMOS VGA

VGAs are generally constructed with three basic blocks, a gain, control and common mode feedback blocks. In this new circuit structure, the gain block has a current steering structure [14] with having wide dynamic range and the control block has pseudo exponential function [24]. Also, output common mode voltage is set a constant voltage by providing unchanged load currents while changing the control voltage or current. Moreover, the unchanged load currents provide the unchanged operation frequency. Also, active loads are used for wideband operation.

The control block of the circuit in Figure 4.2 includes M13, M14, M15, M16 transistors. With varying the gate voltages of M13 and M14, as seen in equations (4.1) and (4.2), the currents of M15 and M16 are varied like in equations (4.3) and (4.4). Because of the current mirrors, M15-M21 and M16-M17-M19, the current of M15 and M21 and the current of M16, M17, M19 would be equal. Moreover, the currents of M3-M4 and M5-M6 would be equal to these control currents.

The gate voltages VG1 and VG4 can be set to equal the current of M11 or M12 to M1 or M2 (I1/2). Therefore, the current of M5 and M6 equals to the control current (the current of M17 and M19).

$$V_{B1} = V_B - V_X \tag{4.1}$$

$$V_{B2} = V_B + V_X \tag{4.2}$$

$$I_{B1} = I_B + I_X \tag{4.3}$$

$$I_{B2} = I_B - I_X \tag{4.4}$$

The gain of the circuit in Figure 4.2 is given in equation (4.5).

$$G = \frac{g_{m1,2}}{g_{m5,6}} g_{m3,4} Z_o \tag{4.5}$$

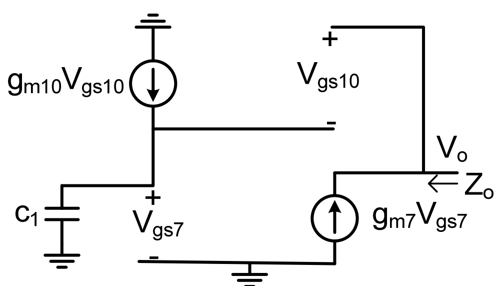


Figure 4.1: The small signal model of active load**.**

The active loads of the circuit in Figure 4.2 include M7- M10 and M8-M9. The small signal equivalent of the load is shown in Figure 4.1. From the loops of small signal circuit, equations (4.6) and (4.7) can be given.

$$V_{gs7} = g_{m10} V_{gs10} \frac{1}{sc_1} \tag{4.6}$$

$$V_{gs10} = V_{gs7} \frac{sc_1}{g_{m7}} \tag{4.7}$$

Then, the active load Z_o is given in equations (4.8) and (4.9).

$$Z_o = \frac{v_o}{i_o} = \frac{V_{gs7}(1 + \frac{sc_1}{g_{m10}})}{g_{m7}V_{gs7}} \qquad \textbf{(4.8)}$$

$$Z_o = \frac{1}{g_{m7}} + \frac{sc_1}{g_{m7}g_{m10}} \qquad \textbf{(4.9)}$$

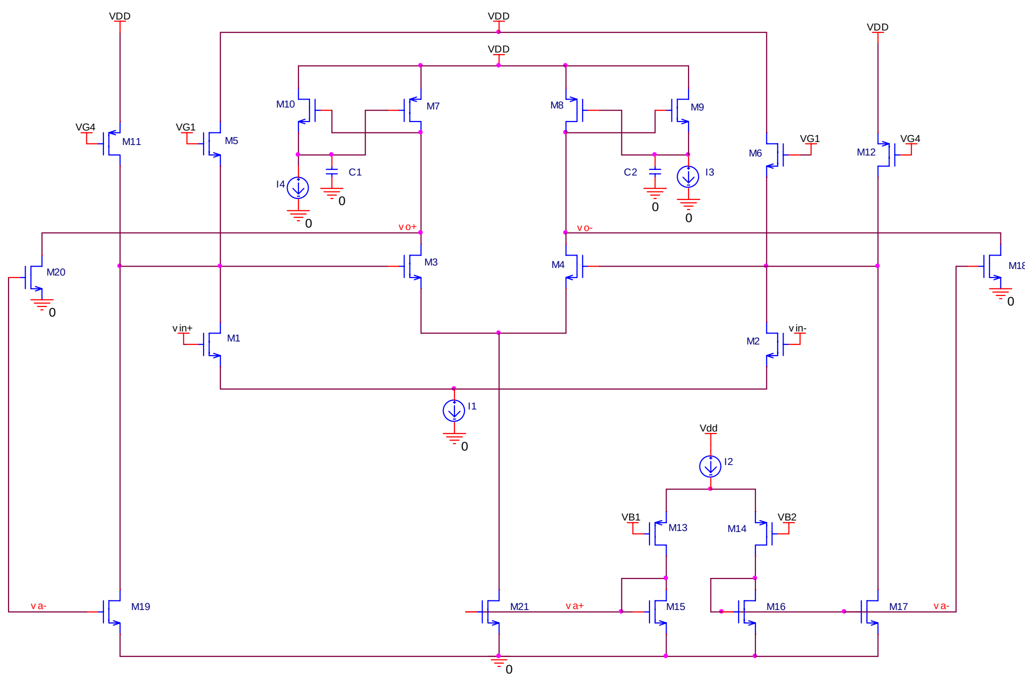


Figure 4.2: The circuit structure of the proposed VGA.

Because the control current equals to the current of the M3 or M4 and M5 or M6, transconductances $g_{m3,4}$ and $g_{m5,6}$ are varied with these control currents. The gain equation can be rewritten like in equation (4.10).

$$G = \frac{g_{m1,2}}{\sqrt{\beta_{5,6}(I_B - I_X)}}\sqrt{\beta_{3,4}(I_B + I_X)}Z_o \qquad \textbf{(4.10)}$$

As it is seen from (4.10), the gain equation includes pseudo approximation function. Therefore, the gain control function would be linear in dB.

Moreover, M18 and M20 do not lead to any common mode change so that common mode feedback block is not needed to be used. When the control voltage is changed and the currents of the M3 and M4 are also changed, M18 and M19 provide the load (Z_o) current to flow same as $2I_B$.

In Figure 4.2, I1 and I2 equal to 300µA, I3 and I4 equal to 10µA and C1 and C2 equal to 10fF. Also, VG1 = 2.8V, VG4 = 1.8V, VB1,2 = 1.5V±V_X, VIN = 1.2V, VDD = 3V. In addition, the dimensions of the transistor are given in Table 4.1.

Table 4.1: The dimensions of the transistors in Figure 4.2.

Transistor	W (µm)	L (µm)
M1, M2, M9-M12	10	0.35
M3, M4, M7, M8	5	0.35
M5, M6	3	0.35
M13, M14	20	0.35
M21	60	2
M16-M20	30	2

4.1.1.1 Simulation results

The AC characteristic of the circuit in Figure 4.2 with changing the V_X control voltage between -0.2V and 0.3V by 0.1V step size is shown in Figure 4.3.The maximum gain is 18.8dB and the minimum gain is -1.4dB, so the dynamic range is 20.2dB. When the gain is the maximum, the cut off frequency is 2.5GHz and when the gain is the minimum, the cut off frequency is 4.4GHz. The average power consumption is 4.15mW.

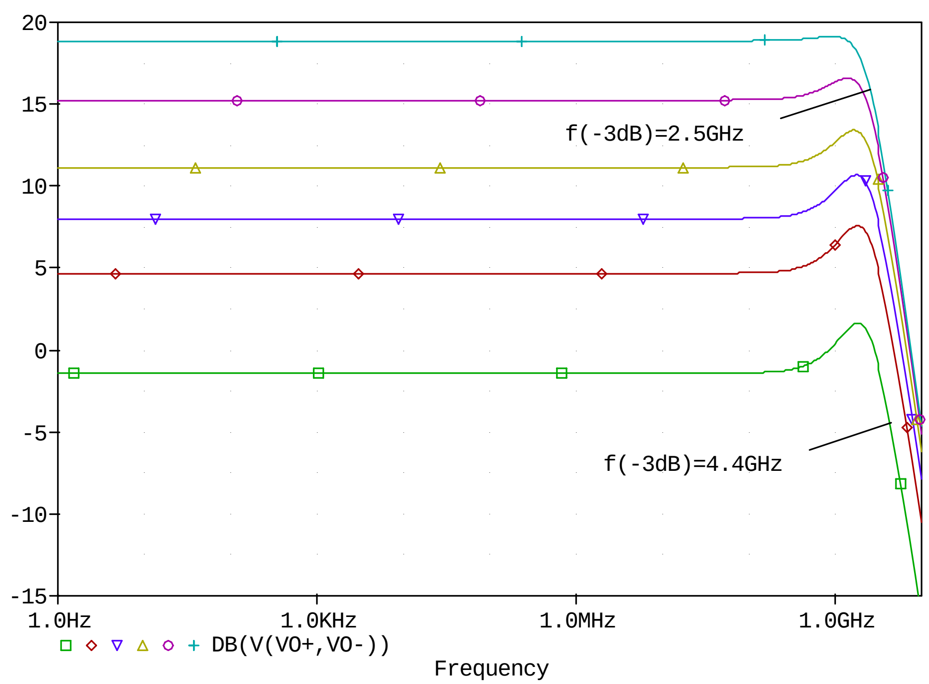


Figure 4.3: The AC characteristic of the circuit in Figure 4.1 with changing the control voltage V_X.

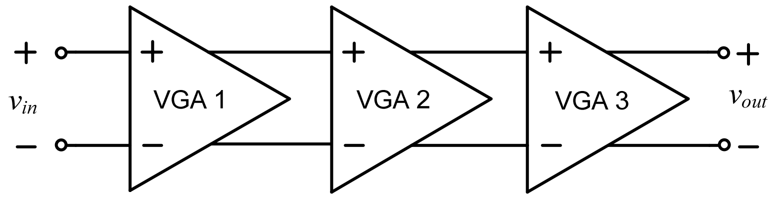


Figure 4.4: The circuit structure of the proposed cascaded three stages VGA.

If the circuit in Figure 4.2 is cascaded like in Figure 4.4, the dynamic range and the bandwidth can be observed in Figure 4.5. This cascaded configuration provides wider dynamic range, but it decreases the cut off frequency. In Figure 4.5, V_X is changed between -0.2V and 0.3V by 0.05V step size.

As it is seen from Figure 4.5, maximum value of the gain is 46.75dB and minimum value of the gain is -14.25dB. Therefore, the dynamic range is 61dB. In addition, when the gain is the maximum, the cut off frequency is 1.23GHz and when the gain is the minimum, the cut off frequency is 2.2GHz. Also, when the control voltage is changed between -0.2V and 0.3V, the average power consumption is 15mW.

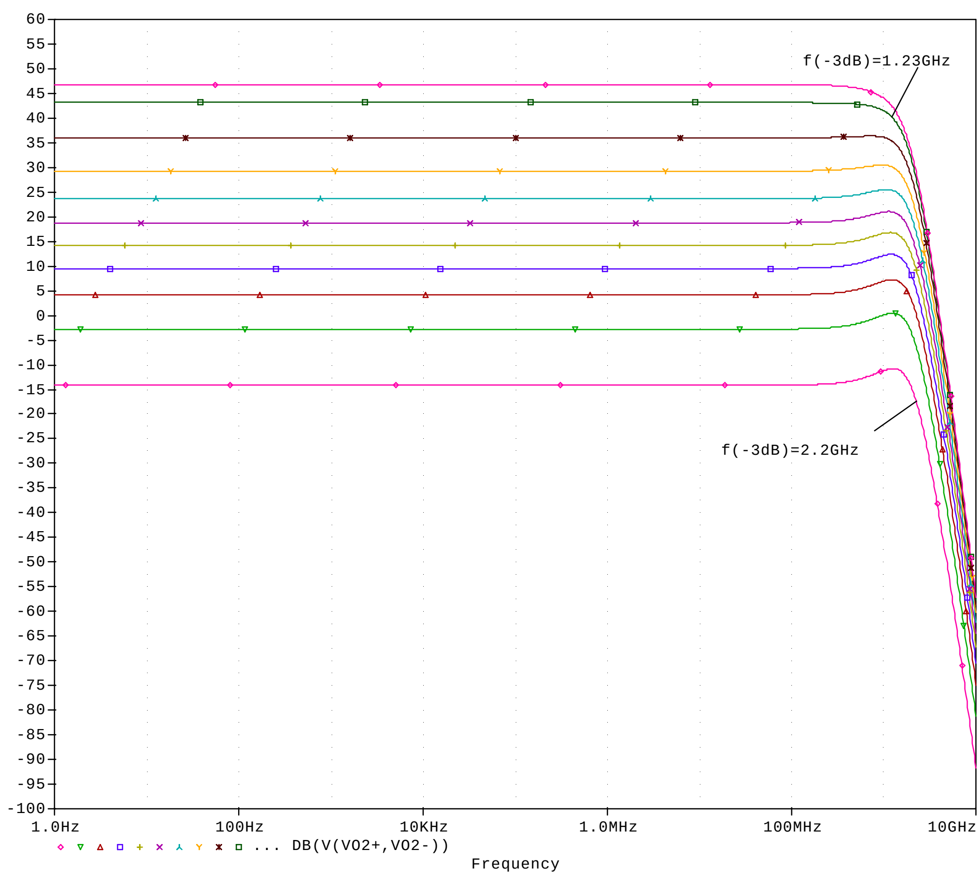


Figure 4.5: The AC characteristic of the circuit in Figure 4.3 with changing the control voltage V_X.

Also, in reference [14] which is shown in Figure 4.6, the gain cell is same as in Figure 4.1. In order to increase bandwidth, the load current is increased with using current mirrors in [14], but in the proposed circuit given in Figure 4.2, active load structure is used in order to increase bandwidth. Also, according to [14], control block includes parasitic bipolar transistor as shown in Figure 4.7, but in the proposed circuit, control block uses only CMOS transistors and therefore the disadvantages of the parasitic BJTs are avoided.

On the other hand, because of the pseudo exponential approximation function used in the control block, the dynamic range is decreased. To achieve the same 60dB dynamic range as the reference one, the proposed circuit is cascaded like given in Figure 4.4. The comparison table for these two circuits is given in Table 4.4.

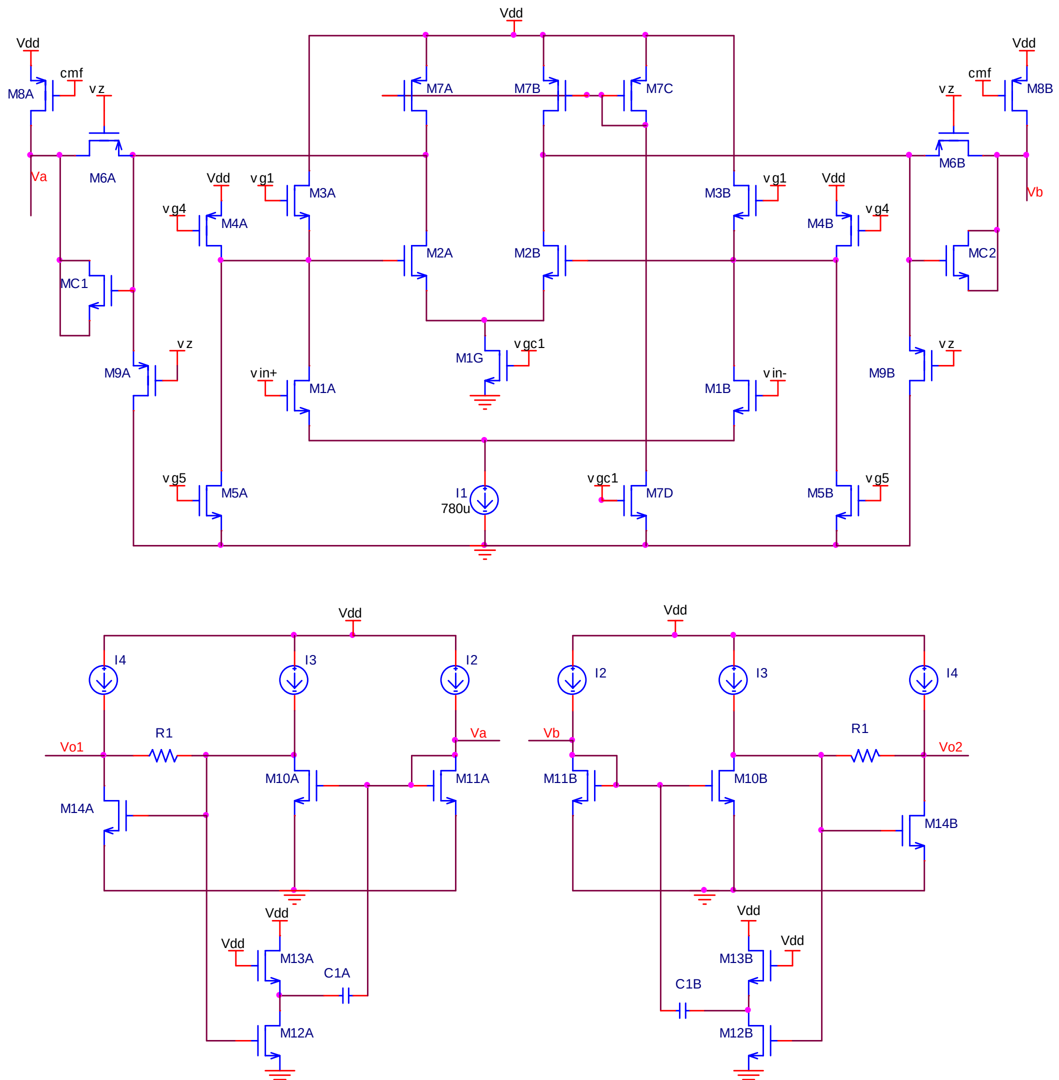


Figure 4.6: The gain cell of the VGA [14].

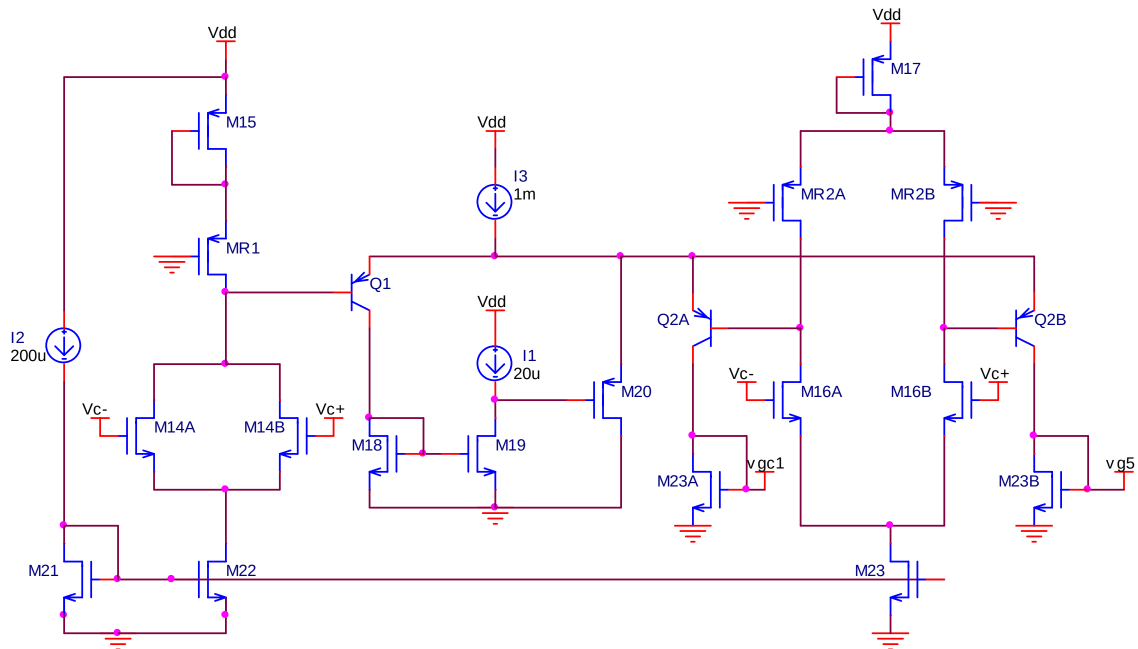


Figure 4.7: The gain control circuit employs lateral bipolar transistors to produce exponentially varying currents with control voltage.

Table 4.2: The dimensions of the transistors in the circuit in Figure 4.5.

Transistor	W (μm)	L (μm)
M1A, M1B	10	0.35
M2A, M2B	100	0.35
M3A, M3B	15	0.35
M4A, M4B	18	0.35
M5A, M5B	10	0.8
M6A, M6B	60	0.35
M7A, M7B	70	2
M7C	50	2
M7D	60	0.8
M8A, M8B	15	1
M9A, M9B	20	0.35
M10A, M10B	20	1
M11A, M11B	50	1
M12A, M12B, M13A, M13B	5	0.35
M14A, M14B	50	0.35

The biasing currents in the circuit are I2 = 500μA, I3 = 80μA, I4 = 1mA.

Transistor dimensions of Figure 4.6 and 4.7 are given in Table 4.2 and 4.3 respectively. The sub blocks given in Figure 4.6 and Figure 4.7 are gathered in together to build up overall VGA circuit [14] and simulated. AC characteristic of the overall VGA circuit with changing the control voltage VX is shown in Figure 4.8.

Table 4.3: The dimensions of the transistors in the circuit in Figure 4.6.

Transistor	W (μm)	L (μm)
MR1	20	0.35
MR2A, MRB, M15, M17	10	0.35
M16A, M16B, M14A, M14B	30	1.5
M18, M19	5	2
M21-M23	10	1
M23A, M23B	10	0.8

As it is seen from Figure 4.8, the dynamic range is 59.5dB. The cut off frequency changes between 86MHz and 764MHz when the gain value is between the maximum and the minimum values. Also, the average power consumption is 26.55mW. Therefore to be able to compare these two circuits in Figure 4.2 and Figure 4.6, the circuit in Figure 4.2 is cascaded like in Figure 4.4. The comparison is shown in Table 4.4.

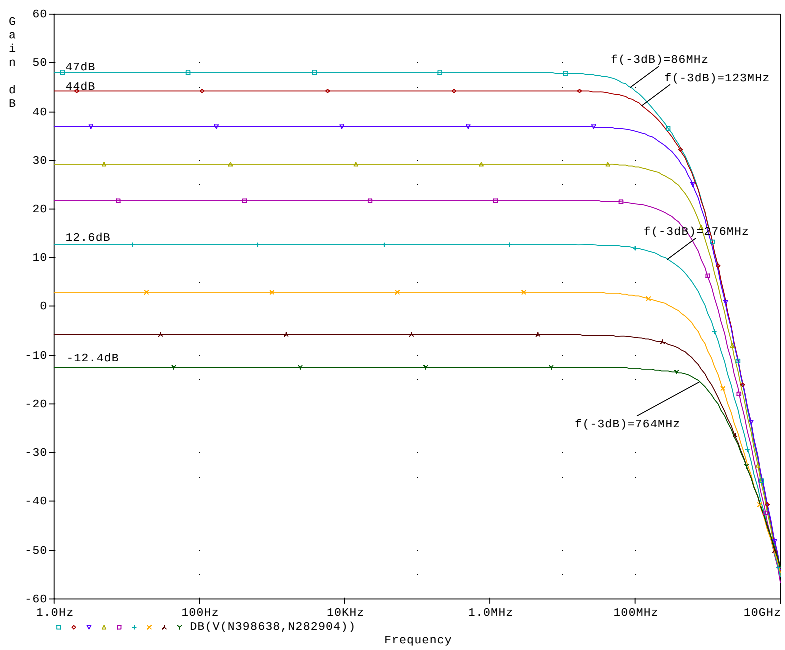


Figure 4.8: The AC characteristic of the circuit in [14] with changing the control voltage V_X.

Table 4.4: The comparison of the performance of the circuits in Figure 4.3 and in [14].

	[14]	**Proposed VGA circuit**
Dynamic range	59.5dB	61dB
The cutoff frequency	86MHz-764MHz	1.2GHz-2.2GHz
The average power consumption	26.55mW	15mW

4.1.2 A 36.7dB dynamic range 716MHz CMOS VGA

In the Figure 4.9, there is a circuit structure with variable bias gain block and control block with using pseudo exponential approximation function with optimizing coefficients. In this circuit the only difference is the control function which is pseudo approximation function with optimizing coefficients. To obtain this function, the control block of reference [24] is modified and used.

The circuit topology of G_1 or G_2 block is shown in Figure 4.10. The dimensions of the transistor in the first and the second block is given in Table 4.5 and Table 4.6. In Table 4.7, the dimensions of the transistors in the function selecting block is also given.

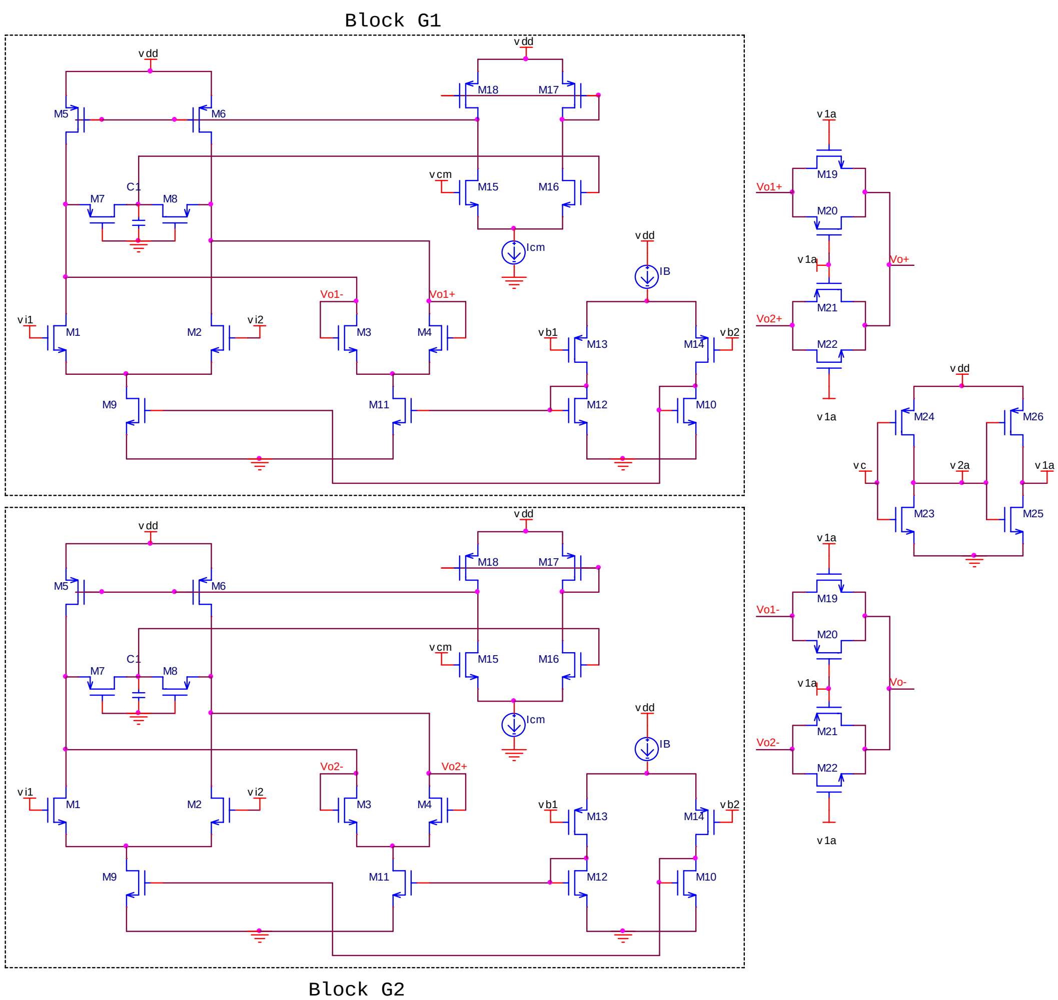


Figure 4.9: The circuit structure of the proposed VGA.

$$V_{B1} = V_B + V_X \tag{4.11}$$

$$V_{B2} = V_B - V_X \tag{4.12}$$

$$I_{B13} = 3I - I_X \tag{4.13}$$

$$I_{B14} = I + I_X \tag{4.14}$$

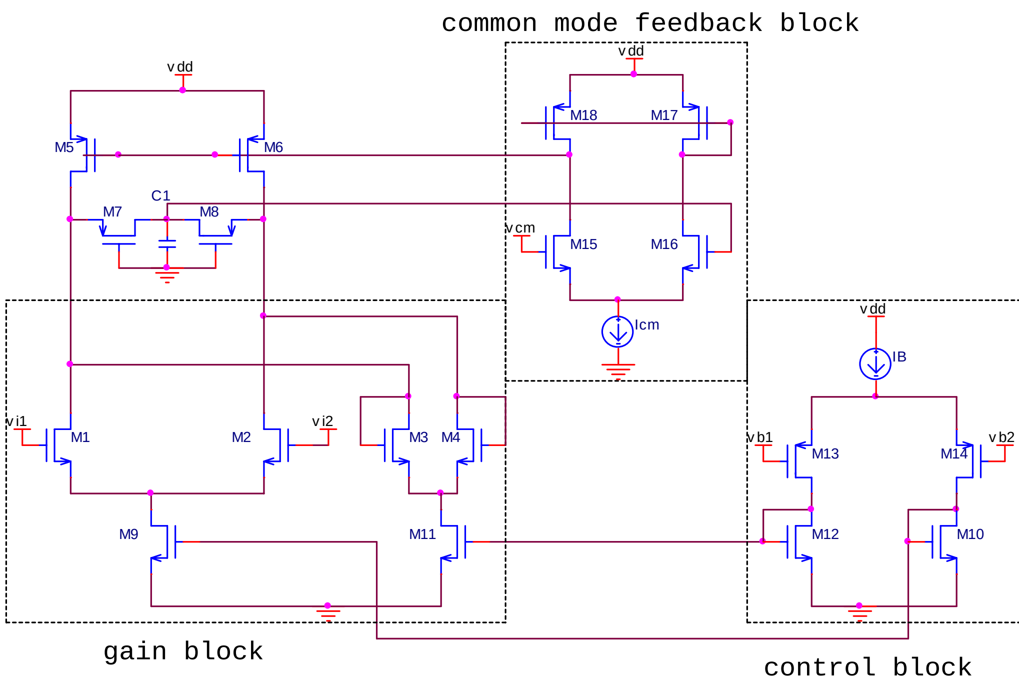


Figure 4.10: The circuit topology of G_1 or G_2 block.

As it is seen from these tables, only the dimensions of transistors of the control block and the current mirrors are different, because of the different coefficients of the control function, which are given in equations (2.39) and (2.40) pseudo approximation function with optimizing coefficients.

In the first control block G_1, while the control voltage is varied like in the equations like (4.11) and (4.12), the current of M13 and M14 are varied like equations (4.13) and (4.14). This block (G_1) operates while x is bigger than 0. Because of the W/L ratio of M13 is three times of W/L ratio of M14, the bias current of M13 is three times of M14 given in equations (4.13) if it is assumed that I_B equals to 4I.

In addition, because the current mirror (M9-M10) ratio is set to 3:1, the current of M9 equals to $3I+3I_X$ and because the current mirror (M11-M12) ratio is set to 1:1, the current of M11 equals to $3I-I_X$. Therefore, the gain of the first block is given like in equation (4.15).

$$G_1 = \frac{g_{m1,2}}{g_{m3,4}} = \frac{\sqrt{\beta_{1,2}(3I + 3I_X)}}{\sqrt{\beta_{3,4}(3I - I_X)}} \qquad \mathbf{(4.15)}$$

The second control block G_2 operates while x is smaller than 0. Because the W/L ratios of M13 is the three times W/L ratios of M14, the bias currents of M13 and M14 are given like in equations (4.16) and (4.17). Because the current mirror (M12-M13) ratio is set to 1:1, the current of M9 equals to $3I+I_X$ and because the current mirror (M14-M15) ratio is set to 3:1, the current of M11 equals to $3I-3I_X$. Therefore, the gain of the second block is given like in equation (4.18).

$$I_{B13} = 3I + I_X \qquad \mathbf{(4.16)}$$

$$I_{B14} = I - I_X \qquad \mathbf{(4.17)}$$

$$G_2 = \frac{g_{m1,2}}{g_{m3,4}} = \frac{\sqrt{\beta_{1,2}(3I + I_X)}}{\sqrt{\beta_{3,4}(3I - 3I_X)}} \qquad \mathbf{(4.18)}$$

Therefore, by modifying the dimensions of the transistors into specific values, the pseudo approximation function with optimizing coefficients is provided as in equations (4.15) and (4.18).

The voltage biases in Figure 4.9, VCM = 2V, VDD = 3V, VB1 = VB2 = $1V \pm V_X$ and VIN = 1.8V. Also, I1 equals to 200µA and I2 equals to 20µA.

Table 4.5: The dimensions of the transistors in first block (G_1) in Figure 4.10.

Transistor	W (µm)	L (µm)
M1, M2, M5,M6, M17, M18	10	0.35
M3,M4	3	0.35
M7,M8	0.35	8
M9	120	0.7
M10-M12	40	0.7
M13	15	0.35
M14	5	0.35

Table 4.6: The dimensions of the transistors in second block (G_2) in Figure 4.10.

Transistor	W (μm)	L (μm)
M1, M2, M5,M6, M17, M18	10	0.35
M3,M4	3	0.35
M7,M8	0.35	8
M11	120	0.7
M9, M10, M12	40	0.7
M13	5	0.35
M14	15	0.35

Table 4.7: The dimensions of the transistors in the selecting block in Figure 4.9.

Transistor	W (μm)	L (μm)
M19, M21	1	0.35
M20,M22	3	0.35
M24, M26	30	0.35
M23,M25	10	0.7

4.1.2.1 Simulation results

The AC characteristic of the circuit in Figure 4.9 with changing the control voltage V_X is shown in Figure 4.11. As it is seen from Figure 4.11, the dynamic range equals 36.7dB, within this dynamic range, the cut off frequency is between 716MHz and 795MHz. Also, the power consumption is 4.8mW.

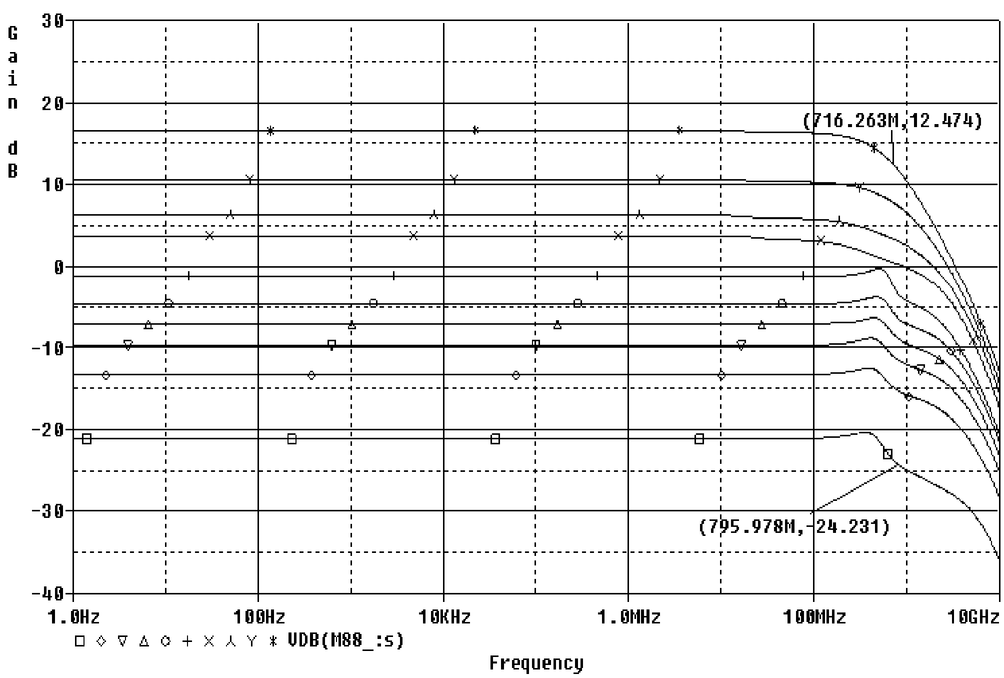


Figure 4.11: The AC characteristic of the circuit in Figure 4.9 with changing the control voltage V_X.

4.2 A Novel Exponential Approximation

The pseudo exponential approximation function with optimizing coefficients is employed by using the first degree of the Taylor approximation function and the coefficients of the functions are appropriately chosen when x is bigger than 0 and when x is smaller than 0.This new exponential approximation is obtained by optimizing the coefficients of the second order Taylor series expansion and the coefficients of the functions are appropriately chosen like in (4.19) and (4.20) when x is bigger than 0 and when x is smaller than 0.If $x > 0$, the function in equation (4.19) and If $x < 0$, the function in equation (4.20).

$$f_1(x) = \frac{1 + 0.417x + 0.154x^2}{1 - 0.1584x + 0.00625x^2} \qquad \textbf{(4.19)}$$

$$f_2(x) = \frac{1 + 0.1584x + 0.00625x^2}{1 - 0.417x + 0.154x^2} \qquad \textbf{(4.20)}$$

Moreover, the comparison of the novel approximation function and the ideal exponential function is given in Figure 4.12. When x is between 10 and -10, the functions would range between 53.86dB and -53.86dB. Therefore, if the proposed function is used, then the dynamic range could be 108dB.

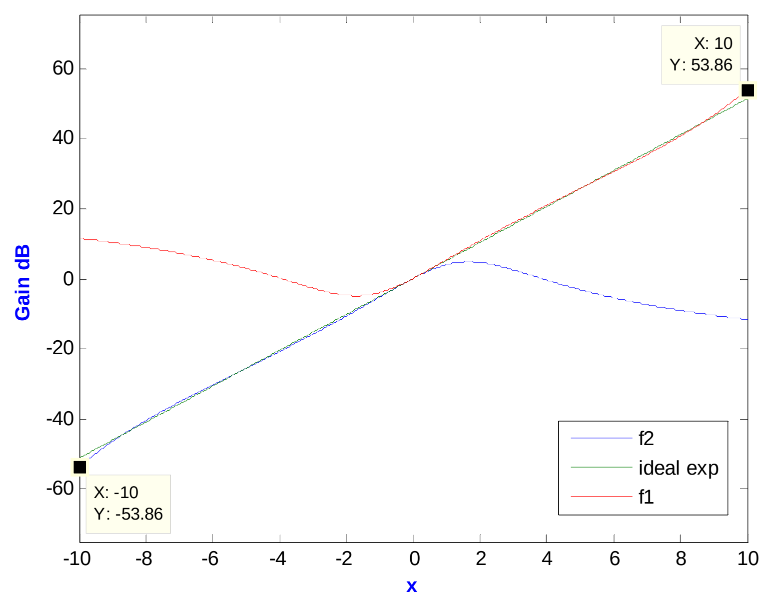


Figure 4.12: The comparison of the novel approximation function and the ideal exponential function.

4.2.1 The comparison of the proposed exponential approximation

The classification of the control block of VGA is studied in section 2 with the different control functions. To compare the performance of the proposed function with the previously proposed methods, a comparison table is given in Table 4.8. According to given data, maximum gain range and widest control range (the x values) can be obtained from the proposed exponential approximation function.

When all these coefficients are normalized to 1, x values are shown in Table 4.8. All the comparison data of the functions in Table 4.8 are obtained from MATLAB.

Table 4.8: The comparison of the control functions for the normalized x values.

Control Functions	**Control Functions**	**x value range** (all functions are normalized to e^x)	**Gain (dB)**
Taylor Series Approximation	$e^{\frac{b}{a}x} \cong 1 + \frac{b}{a}x + \frac{b^2}{2a^2}x^2$	-0.57 < x < 0.81	11
Pseudo exponential approximation	$e^{nx} \approx \left(\frac{1+x/2}{1-x/2}\right)^n$	-0.8 < x < 0.8	14
Pseudo exponential function with optimizing coefficients	$f(x) = \frac{1+0.9375x}{1-0.3125x}, x > 0$ $f(x) = \frac{1+0.3125x}{1-0.9375x}, x < 0$	-2.08 < x < 2.06	36
A composition of Taylor and pseudo exponential approximation – 1	$f(x) = \left[\frac{0.15+(1+0.28x)^2}{0.15+(1-0.28x)^2}\right]$	-3.5 < x < 3.5	58
A composition of Taylor and pseudo exponential approximation – 2	$f(x) = \frac{1+0.476x+0.062x^2}{1-0.476x+0.062x^2}$	-3.93 < x < 3.93	65.4
Proposed exponential approximation	$\mathbf{f(x) = \frac{1+0.417x+0.154x^2}{1-0.1584x+0.00625x^2}, x > 0}$ $\mathbf{f(x) = \frac{1+0.1584x+0.00625x^2}{1-0.417x+0.154x^2}, x < 0}$	**-5.9 < x < 5.9**	**108**

4.2.2 A modified control block for the proposed exponential approximation

In Figure 4.13, the function in equation (4.19) is realized by modifying the circuit in [38]. The first block realizes the nominator of the equation (4.19) and the second block realizes the denominator of the equation (4.19).

In the implementation of the novel approximation function (f_1), the biasing current values of the nominator are given such as I1 = 1.17mA, I2 = -2.3I_x, Io = 37µA, Ic = 2.3I_x and the biasing current values of the denominator I3 = 31.3µA, I4 = 1.2I_x, Io = 37µA, I_c = 1.2I_x. The dimensions of the transistors in the control function f_1 is given in Table 4.9.

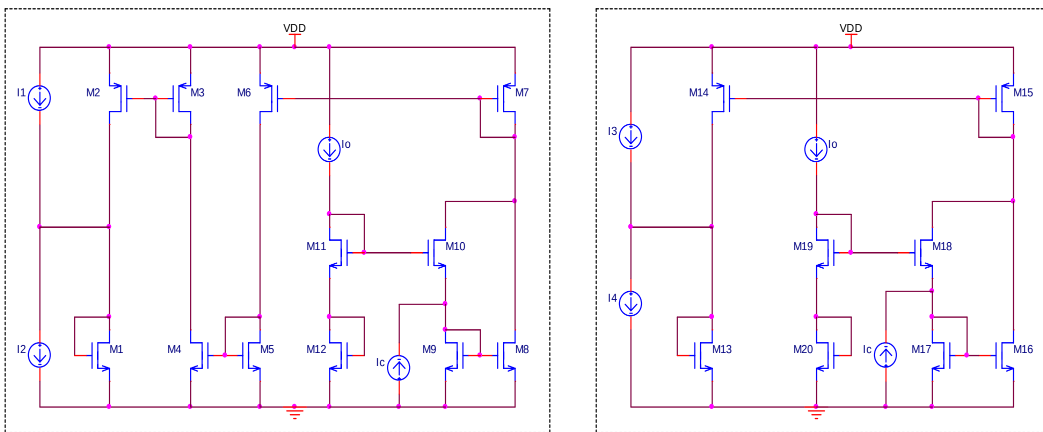
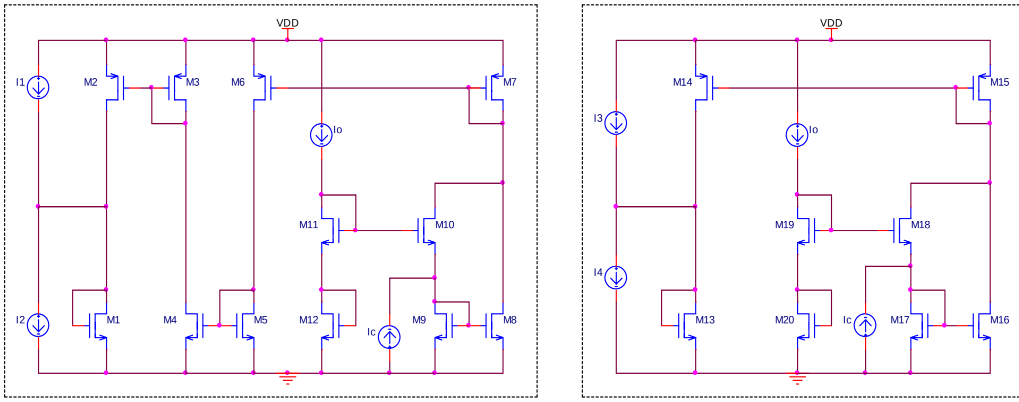


Figure 4.13: The implementation of the novel approximation function (f_1).

Table 4.9: The dimensions of the transistors in realization of the control function f_1 in Figure 4.13.

Transistor	W(µm)	L(µm)
M1, M13	10	0.35
M2	40	2
M3, M15	20	2
M4	40	1
M5, M8, M9, M12, M16, M17, M20	20	1
M6	40	2
M10, M11, M18, M19	15	1
M7	10	2
M14	14	2



denominator (f2) nominator (f2)

Figure 4.14: The implementation of the novel approximation function (f_2).

In the implementation of the novel approximation function (f_2), the biasing current values of the nominator are given such as I1 = 1.17mA, I2 = 2.3I_x, Io = 37μA, Ic = 2.3I_x and the biasing current values of the denominator I3 = 31.3μA, I4 = -1.2I_x, Io = 37μA, Ic = 1.2I_x. The dimensions of the transistors in realization of the control function f_1 is given in Table 4.8.

Table 4.10: The dimensions of the transistors in realization of the control function f_2 in Figure 4.14.

Transistor	W(μm)	L(μm)
M1	10	0.35
M2	40	2
M3, M15	20	2
M4	40	1
M5	20	1
M8, M9, M12, M16, M17, M20	20	1
M6	40	2
M10, M11, M18, M19	10	1
M7	10	2
M14	14	2

4.2.2.1 Simulation results

In Figure 4.15, the simulation result of the circuits in Figure 4.13 and 4.14 is shown. As it is seen from figure, when the control current is varied between -82μA and 85μA, 91dB dynamic range is obtained. The comparison of the realization of the control functions in control circuits is given in Table 4.11 and the new approximation function provides the widest dynamic range.

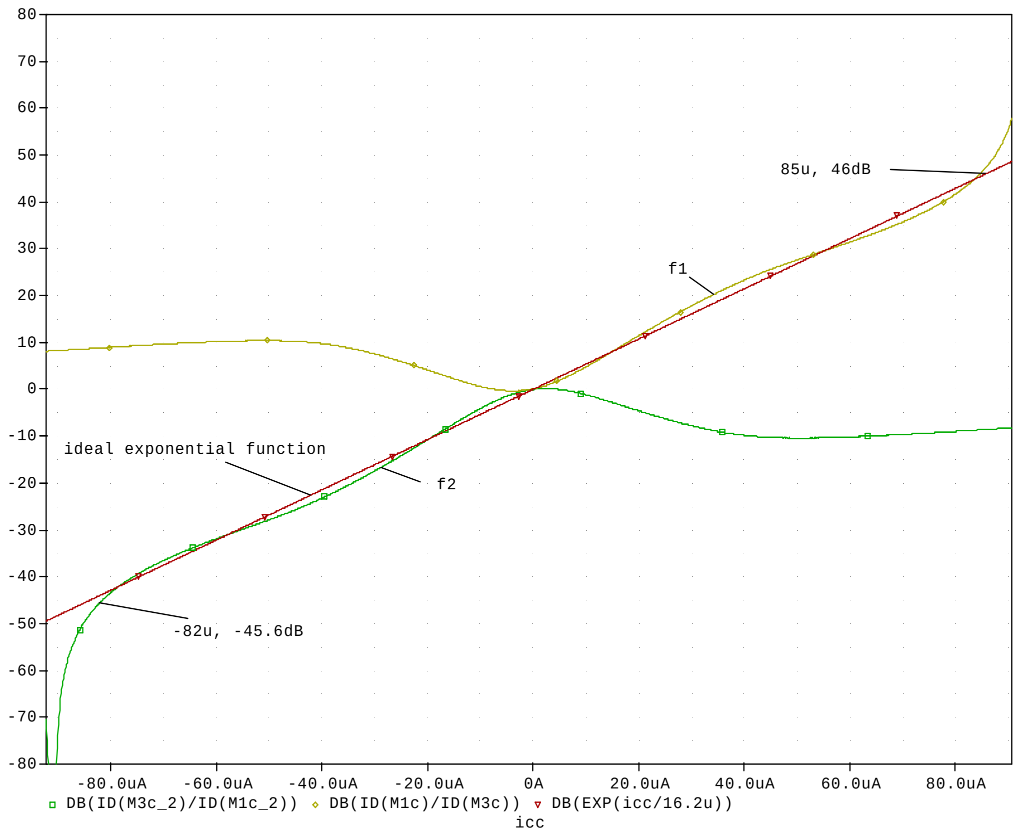


Figure 4.14: The simulation result of the circuits in Figure 4.13 and 4.14.

Table 4.11: The comparison of the realization of the control functions in control circuits

Control Functions	The dynamic range of the realization of the control functions
Taylor series approximation	15dB [28], 20dB [29]
Pseudo exponential approximation	24dB [2]
Pseudo exponential function with optimizing coefficients	50dB[39]
A composition of Taylor and pseudo exponential approximation 1	47.5dB [45]
A composition of Taylor and pseudo exponential approximation 2	45dB [38]
New exponential approximation function	**90dB**

4.3 A Novel VGA Model

A new variable gain amplifier is modelled in order to realize a VGA experimentally. The circuit in Figure 2.19 is modelled by using transconductance amplifiers and given in Figure 4.16. In Figure 2.19, transistors M1 and M2 are modelled as G_{m1} and M3 and M4 are modelled as a resistance which is shown as unity negative feedback transconductance amplifier (G_{m2}). The gain of the circuit model in Figure 4.16 is given in equation (4.21).

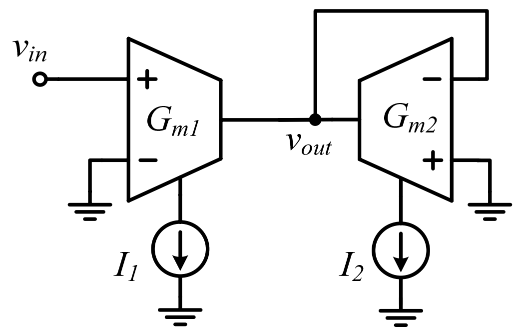


Figure 4.15: A new model of the VGA in Figure 2.19.

$$G = \frac{G_{m1}}{G_{m2}} \tag{4.21}$$

The operational transconductance amplifiers G_{m1} and G_{m2} are varied with their biasing currents I_1 and I_2. If these current are set to form a pseudo exponential approximation function like in equation (4.22) and (4.23), the gain equation would be given as (4.24). Therefore, the gain could change linear in dB with its control current I_A.

$$I_1 = I_B + I_A \tag{4.22}$$

$$I_2 = I_B - I_A \tag{4.23}$$

$$G \propto \frac{I_B + I_A}{I_B - I_A} \tag{4.24}$$

4.3.1 Simulation results

The circuit model in Figure 4.16 is realized with using PSPICE. OTAs in Figure 4.16 are realized by LM13700 like in Figure 4.17.

Also, the implementation of the control block of the new model of the VGA is shown in Figure 4.18 and the transistors are implemented by using CD4007. When V_X and V_Y changes oppositely as given in equations (4.25) and (4.26), also the bias currents of G_{m1} and G_{m2} is varied according to equations (4.22) and (4.23).

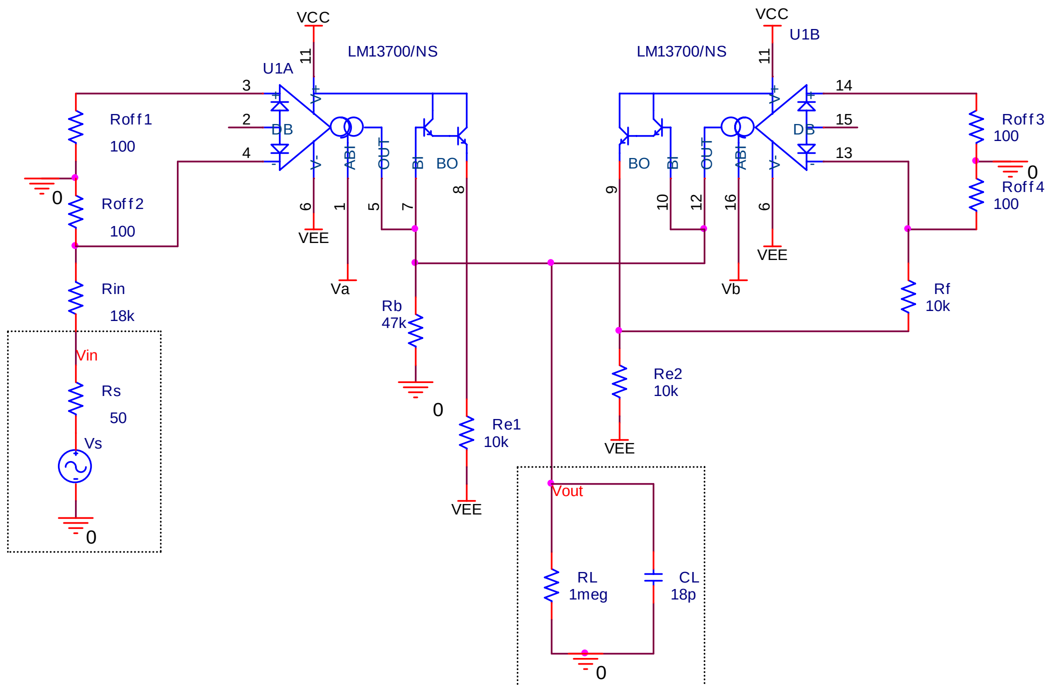


Figure 4.16: The implementation of the gain block of the new model the VGA.

$$V_x = V_B - V_a \qquad \textbf{(4.25)}$$

$$V_y = V_B + V_a \qquad \textbf{(4.26)}$$

Figure 4.19 shows the simulation results of the circuits given in Figures 4.17 and 4.18. It is shown that 25dB dynamic range (10.2dB to -14.5dB) and the cut off frequency of 141kHz to 744kHz could be obtained from the SPICE simulations.

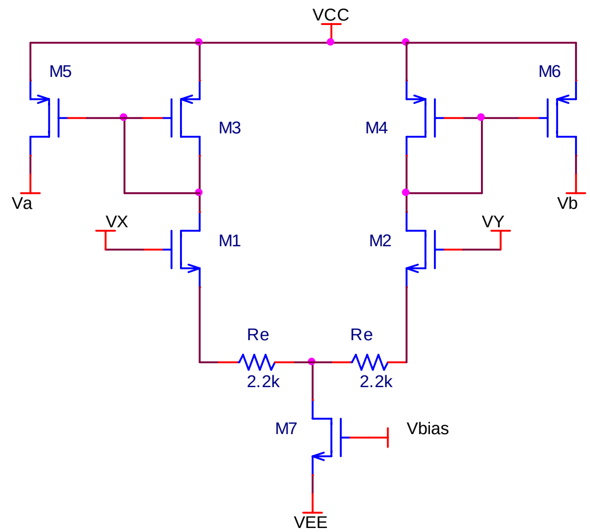


Figure 4.17: The implementation of the control block of the new model the VGA.

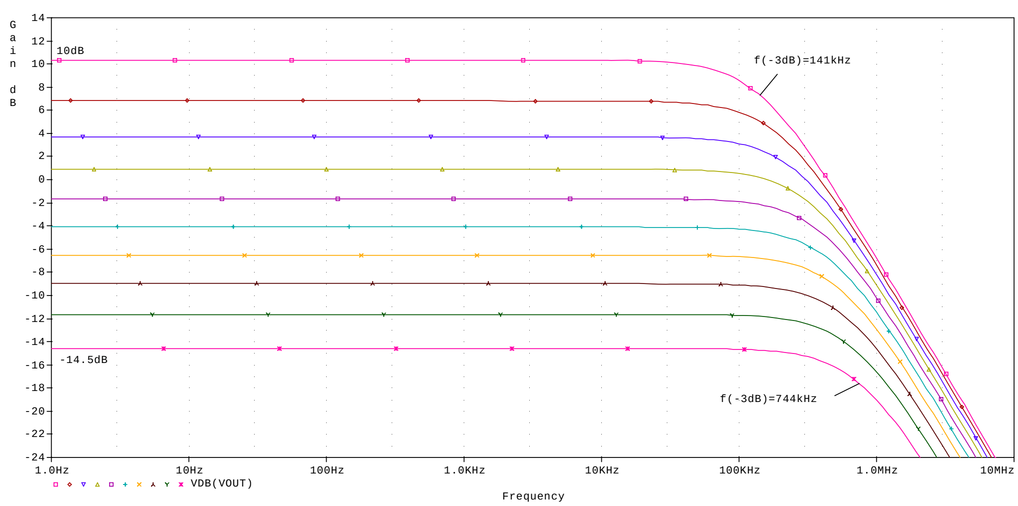


Figure 4.18: The simulation results of the new model the VGA.

4.3.2 Measurement results

The circuit in Figure 4.16 is realized on board by using LM13700 to implement G_m blocks and CD4007 for the control block. When the control voltage is varied between -1V and 0.7V, by applying a sinusoidal voltage at the input and by varying the frequency, then the output voltage could be observed to have AC characteristics of the circuit. Measurement results are given in Figure 4.20.

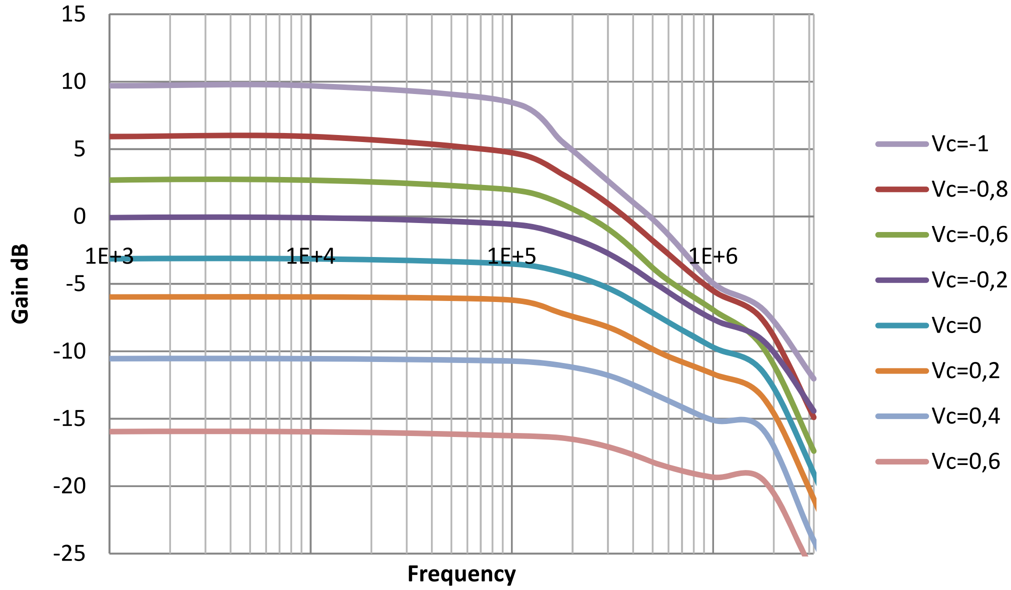


Figure 4.19: The measurement result of the new model the VGA.

4.3.3 Verification of the results

In order to compare the simulation and measurement results, Figure 4.21 and 4.22 are given. The comparison of the gain control function for simulation and measurement result is given in Figure 4.21. Also, the comparison of the AC characteristic of the simulation and measurement result is given in Figure 4.22.

Finally, it can be seen from Figure 4.22 that, when control voltage is varied from -1V to 0.7V, the gain values changes between 10dB and -16dB. Simulation and measurement results are almost in match. The operating bandwidth of the circuit is also appropriate. In the measurements, the cut off frequency changes between 137kHz and 1.93MHz, where LM13700 has an operation bandwidth of 2MHz.

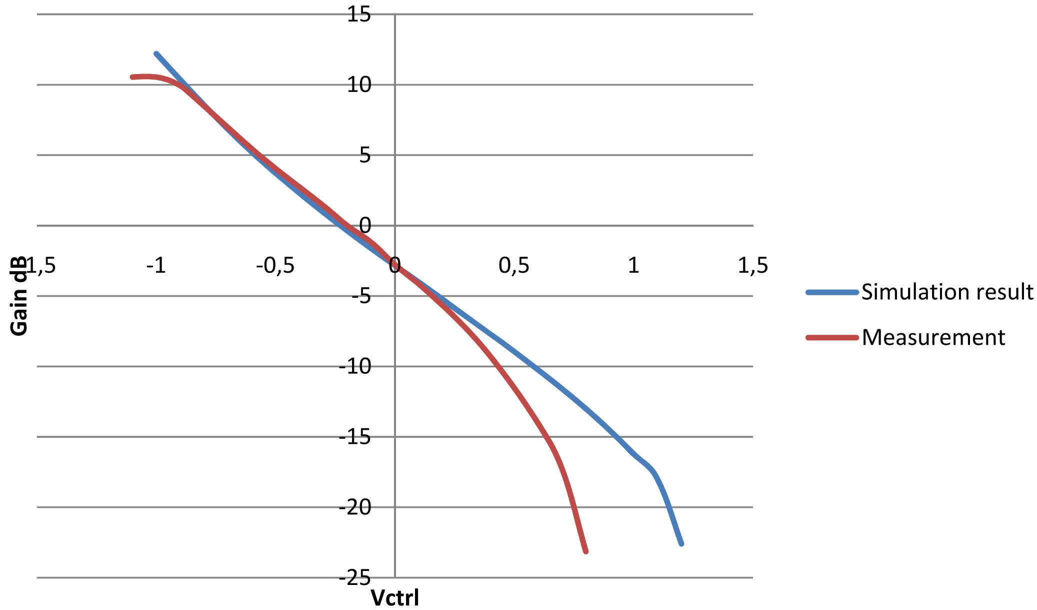


Figure 4.20: The comparison of the gain control function of the simulation and measurement result.

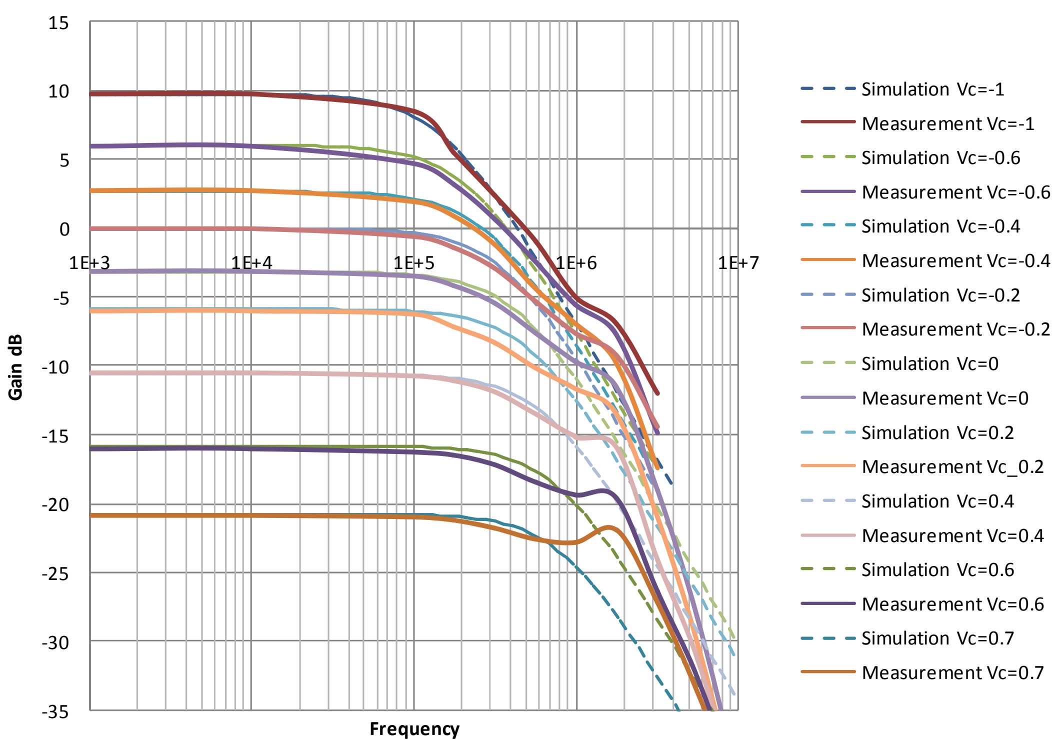


Figure 4.21: The comparison of the AC characteristic of the simulation and measurement result.

4.4 Chapter Summary

In this chapter, two new VGA circuit topologies are proposed and designed in 0.35μm CMOS process. The first proposed VGA consist of a current steering gain structure and a control block employing pseudo exponential function. Also, output common mode voltage is set to a constant voltage by providing unchanged load currents while changing the control voltage or current. Therefore there is no need to implement common mode feedback in this VGA. Also, active loads are used for wideband operation.

The second proposed VGA is composed of one variable gain amplifier block and a control block employing two different pseudo exponential approximation functions for the upper and lower ranges of the control voltage.

Secondly, a new pseudo exponential approximation function is obtained by optimizing the coefficients terms of the second order Taylor series expansion. This function is compared with the other approximated functions given in Chapter 2. Also, a control block is designed with using the new function in 0.35μm CMOS process.

Thirdly, a new variable gain amplifier is modelled in order to realize a VGA experimentally. The new VGA model is constructed with a gain and control block.

5. CONCLUSION AND RECOMMENDATIONS

In this thesis, VGAs are classified in the terms of the operating principles and circuit realizations. Additively, five different cascode structures given in the literature are implemented by using 0.35µm CMOS process to compare and show their performances.

Beyond that, two new circuit topologies and a new variable gain amplifier model are proposed. The first proposed circuit structure is composed of three cascaded variable gain amplifiers and designed in 0.35µm CMOS process. Maximum value of the gain is 46.75dB while the minimum is -14.25dB employing 61dB dynamic range. The cut off frequency is remains in the range of 1.23GHz to 2.2GHz. The second proposed circuit structure is composed of one variable gain amplifier block and two different control functions are realized in the control block for the two different range of the control voltage. The gain could be changed from15.47dB to -21.23dB while the cut off frequency changes 716MHz to 795MHz.

Moreover, a new pseudo exponential approximation function is obtained by optimizing the coefficients of the terms of the second order Taylor series expansion. It is shown that 90dB dynamic range could be obtained with the control circuit by using the new proposed approximation. According to the author's knowledge, this could be the widest dynamic range that a control block can handle. Future works could be the complete VGA circuit implementation of the proposed approach to verify given analysis and simulations.

Consequently, a new variable gain amplifier model is constructed by using operational transconductance amplifiers and the proposed model is realized on board to verify the model performance. LM13700 commercial operational transconductance amplifiers are used to measure performance metrics of the proposed model. SPICE analysis and the measurement results are shown to be in agree within the gain range of 10dB to -16dB where the cut off frequencies are below 2MHz limited by LM13700 bandwidth.

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APPENDICES

APPENDIX A.1 : Pseudo Exponential Approximation Function with Different n values.

APPENDIX A.2 : The comparison of the VGAs in Literature.

APPENDIX A.1

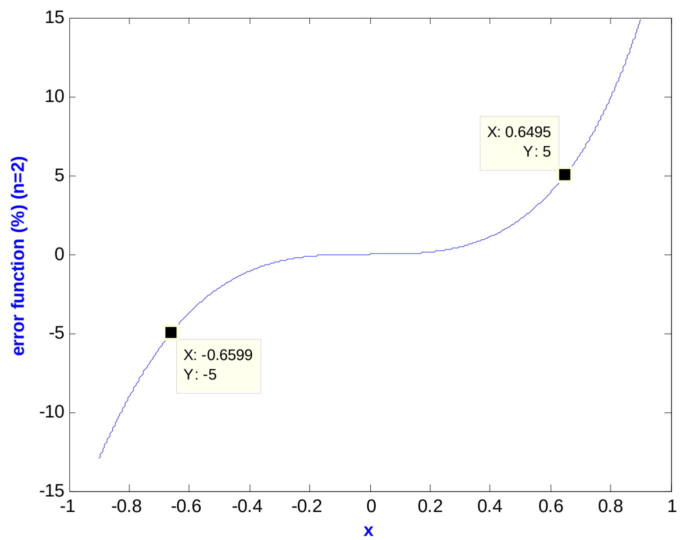


Figure A.1: The error function of pseudo exponential approximation for n = 2.

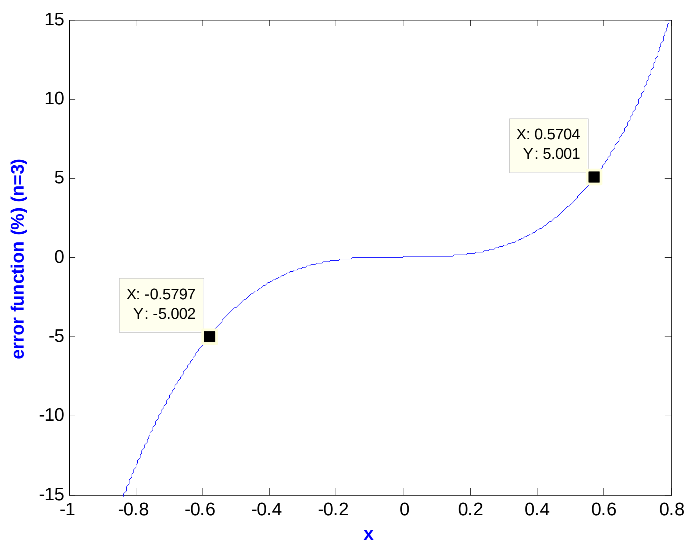


Figure A.2: The error function of pseudo exponential approximation for n = 3.

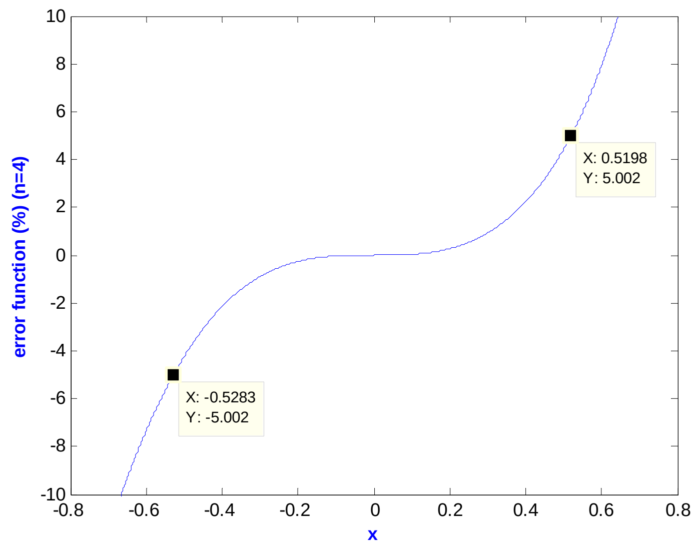


Figure A.3: The error function of pseudo exponential approximation for n = 4.

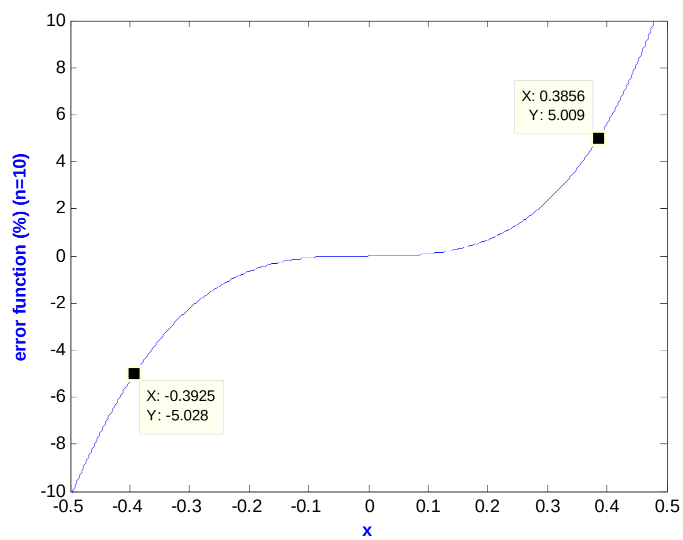


Figure A.4: The error function of pseudo exponential approximation for n = 10.

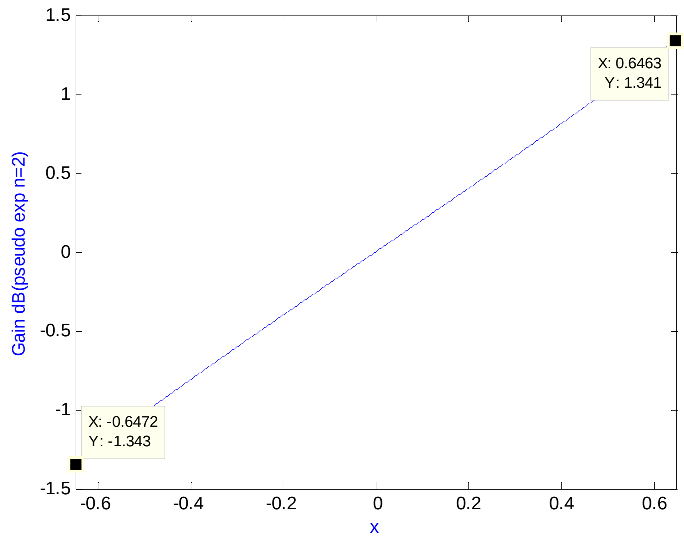


Figure A.5: Pseudo exponential approximation function for n = 2.

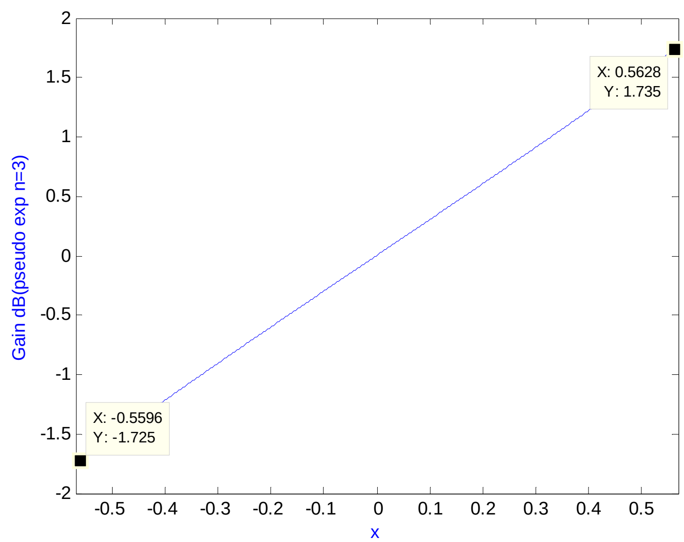


Figure A.6: Pseudo exponential approximation function for n = 3.

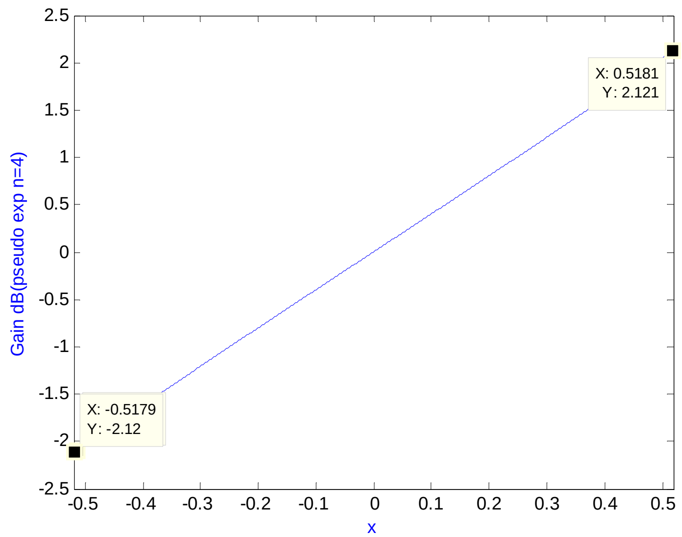


Figure A.7: Pseudo exponential approximation function for n = 4.

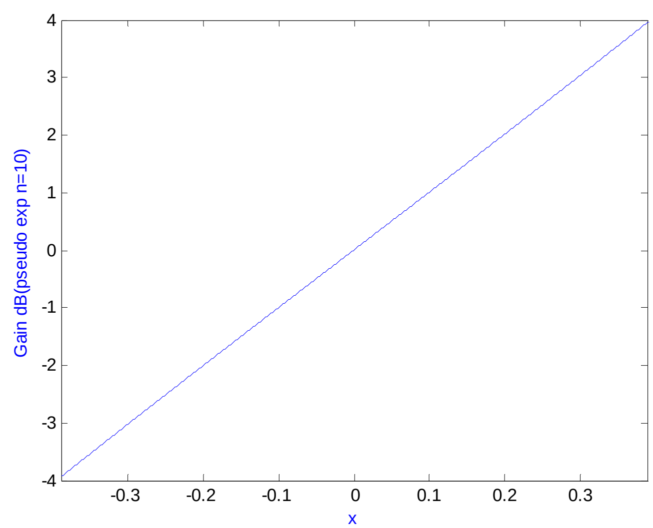


Figure A.8: Pseudo exponential approximation function for n = 10.

APPENDIX A.2

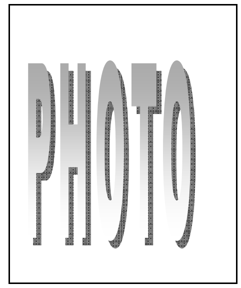
Table A.1: The comparison of the VGAs in literature.

Ref.	Process	Supply Voltage	Method	Gain(dB) /Number of stage	f(MHz)	Power (mW)	NF (dB)	Chip Area (mm^2)
[1]	0.5μm CMOS	3.3V	BJT	70	20	33	N/A	N/A
[3]	0.18μm CMOS	1.8V	Exp.	28.4/1	1200	4.86	N/A	0.04
[4]	0.18μm CMOS	1.8V	Parasitic BJT	83/3	37	6.12	N/A	0.4
[5]	Si bipolar	2.7V	BJT	77/1	400	16.2	N/A	N/A
[6]	0.13μm CMOS	1.8V	Pseudo exp.[2]	54	743	8.1	N/A	N/A
[8]	0.18μm CMOS	1.8V	Pseudo exp.	85/5	950	25.1	7.45	N/A
[10]	BiCMOS	2.8V	BJT	50	900	N/A	N/A	0.1
[11]	BiCMOS	3V	BJT	78/2	50	36	5	1
[12]	0.5μm CMOS	2V	Subthreshold MOS	50.7	0.134	0.002	N/A	N/A
[13]	0.18μm CMOS	1.8V	Exp.	70/3	40	4.7	N/A	34.842
[14]	2μm CMOS	N/A	Parasitic BJT	35/1	50	150	N/A	0.8
[15]	0.35μm CMOS	±1.5V	Pseudo exp.	26/1	21	24.8	N/A	N/A
[17]	0.18μm CMOS	0.5V	Linear	49	10	0.025	N/A	N/A
[18]	2μm MOSIS	3V	Pseudo exp.	30	N/A	2.88	N/A	N/A
[19]	0.5μm CMOS	±1.5V	Pseudo exp.	30/1	21.9	0.48	N/A	N/A
[20]	0.35μm CMOS	N/A	Taylor Appr.	60/3	N/A	35	12	N/A
[22]	0.8μm CMOS	N/A	Pseudo exp.	60	10	80	N/A	0.6
[23]	0.18μm	N/A	Pseudo exp.[1]	12/1	700	N/A	N/A	N/A
[24]	0.18μm CMOS	1.8V	Pseudo exp.	73/3	380	10.8	5	N/A
[25]	AD600	±4.75V	N/A	40/1	35	125	N/A	N/A
[27]	THS7530	N/A	N/A	58	300	N/A	9	N/A
[28]	AD603	±4.75V	N/A	40/1	90	N/A	N/A	N/A
[30]	ADL5330	N/A	N/A	56	10	N/A	N/A	N/A
[35]	0.18μm CMOS	1.8V	Pseudo exp.[2]	95/2	32	6.5	N/A	0.4
[39]	0.5μm CMOS	3.3V	Pseudo exp.	20/1	310	22	N/A	N/A
[40]	HBT IC	5V	Linear	35	750	N/A	6.5	N/A
[41]	0.18μm CMOS	1.8V	Linear	32	1830	8	1.4	N/A
[42]	0.18μm CMOS	1.8V	Pseudo exp.[2]	94.1	4	20.5	N/A	0.42
[43]	0.5μm CMOS	3V	Taylor Appr.	15	N/A	N/A	N/A	N/A
[44]	0.5μm CMOS	±1.5V	Pseudo exp.[1]	50	1.6	1.2	N/A	N/A
[45]	0.5μm CMOS	±1.5V	Pseudo exp.	29.5	3	0.5	N/A	N/A
[46]	0.18μm	1.8V	Differential Eq.	12.8/1	430	16.2	6.2	N/A
[48]	0.6μm CMOS	3V	Pseudo exp.	34/2	1	21	N/A	0.43
[49]	0.5μm CMOS	3.3V	Pseudo exp.	15/1	20	12.5	N/A	0.15
[50]	0.18μm CMOS	1.8V	Pseudo exp.[3]	90/2	50	6.66	N/A	0.34
[51]	0.35μm CMOS	3.3V	Pseudo exp.[2]	32	46	4.63	10	N/A
[52]	0.18μm CMOS	1.8V	Pseudo exp.[2]	84/2	40	6.48	N/A	0.4
[53]	0.18μm CMOS	1.8V	Pseudo exp.[2]	60/2	3	3.6	N/A	N/A
[54]	0.18μm CMOS	1.8V	Pseudo exp.	84/3	350	5.4	N/A	0.18
[55]	0.35μm CMOS	3V	BJT	100/3	200	32.4	N/A	0.38
[56]	0.18μm CMOS	1.8V	Parasitic BJT	75/2	150	N/A	N/A	N/A
[57]	BiCMOS	0.8V	BJT	12	1600	6.4	6.5	N/A
[58]	0.18μm CMOS	1.8V	Parasitic BJT	90	400	22	13.8	0.15
[59]	BiCMOS	N/A	BJT	24	3100	N/A	N/A	N/A
[60]	BiCMOS	2.5V	BJT	31.5		40	2.5	1.6
[61]	0.13μm CMOS	N/A	Linear	40	130	0.05	N/A	N/A
[62]	BiCMOS	2.7V	BJT	70	100	21.6	N/A	N/A
[63]	0.35μm CMOS	1.5V	Linear	40/2	10	0.9	N/A	51000
[64]	0.18μm CMOS	1.8V	Digital	33	470	22	4	0.32
[65]	1.6μm CMOS	5V	Linear	80/6	10	37	N/A	0.72
[66]	Bipolar	5V	Linear	25	35	40	N/A	0.15
[67]	0.25μm CMOS	3.3V	Pseudo exp.	66.5/2	4	72.6	15	0.4
[68]	N/A	N/A	Linear	25/1	80	30	N/A	N/A

Table A.1 (continued): The comparison of the VGAs in literature.

Ref.	Process	Supply Voltage	Method	Gain(dB) /Number of stage	f(MHz)	Power (mW)	NF (dB)	Chip Area (mm^2)
[69]	0.35µm CMOS	2.7V	BJT	94/1	200	16.4	7@Gmax	0.04
[70]	0.25µm CMOS	2.5V	Subthreshold MOS	80	380	63.25	11	N/A
[71]	0.13µm CMOS	2.5V	Pseudo exp.[3]	N/A	800	N/A	N/A	N/A
[72]	0.25µm CMOS	3.3V	Taylor Appr.	50	N/A	N/A	N/A	N/A
[73]	0.5µm CMOS	±0.75V	Pseudo exp.	12	26	0.375	N/A	0.035
[74]	0.6µm CMOS	N/A	Pseudo exp.	30	0.01	10	N/A	N/A
[75]	0.25µm CMOS	2.5V	Subthreshold MOS	80/4	30	27.5	N/A	0.49
[76]	0.25µm CMOS	3V	Linear	15	2100	3.6	N/A	N/A
[77]	1.2µm CMOS	3V	Taylor Appr.	20	N/A	0.9	N/A	N/A
[78]	0.5µm CMOS	±1.5V	Pseudo exp.	15	N/A	0.4	N/A	N/A
[79]	3µm CMOS	5V	Parasitic BJT	50/1	1	N/A	N/A	0.7

[1] Pseudo exponential function with optimizing the coefficients
[2] A composition of Taylor and pseudo exponential approximation – 1
[3] A composition of Taylor and pseudo exponential approximation – 2



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