DETERMINATION OF TRAP LEVELS OF MOS STRUCTURE SEMICONDUCTOR DEVICES AT CRYOGENIC TEMPERATURES

A MASTER'S THESIS

in

Electrical and Electronics Engineering
University of Gaziantep

By
Nuran Doğru
July 1997

Approval of the Graduate School of Natural and Applied Sciences

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ABSTRACT

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DOĞRU, Nuran
M.S. in Electrical and Electronics Eng.
Supervisor: Prof. Dr. Sadettin ÖZYAZICI
July 1997, 105 pages

In this thesis, trap levels which effect the characteristics and efficiency of the semiconductor devices in MOS (metal-oxide-semiconductor) structure solar cells must have been determined at cryogenic temperatures. For this reason MOS solar cells are designed and fabricated in the form of Al- oxide- p type silicon crystals.

In laboratory work, solar cells are produced by creating natural oxide layer and then depositing Aluminum metal contacts by vacuum evaporation technique. Since trap levels in semiconductors can quickly charge and discharge at room temperatures, all measurements must be carried out in a cryostat which uses liquid nitrogen gas (77 K). Using Photocapacitance technique these levels in cells can be determined. Trap levels, I-V, dI/dV,and Capacitance of each solar cell must have been measured by using Monochromator, Capacitance meter and I-V characteristics measurement. But during experimental study, I-V, C-V and C-λ characteristics were not obtained, because cryostat was not run. Therefore, some physical parameters such as quantum efficiency, absorption coefficient, I_p (photocurrent)-λ and V_p (photovoltage)- λ were measured.

To maximize the efficiency of the MOS solar cell open-circuit voltage (V_{oc}), short-circuit photocurrent (I_{sc}), and the fill factor (FF) must be as high as possible.

To determine the effect of insulating layer thickness on cells, solar cells are produced with different oxide thickness. It is known that a thin oxide layer increases the open-circuit voltage without any appreciable decrease in short-circuit current.

Front surface of the silicon is coated with different aluminum thickness to observe the effects of aluminum layer on cell.

The information obtained from trap levels can be used not only for the fabrication of more efficient solar cells, but also for increasing the efficiency of devices which use semiconductor materials.

Key words: MOS solar cells, trap levels, photocurrent, efficiency, cryogenic temperature.

ÖZET

MOS YAPILI YARI İLETKEN DEVRE ELEMANLARININ TUZAK SEVİYELERİNİN DÜŞÜK SICAKLIKLARDA TESBİTİ

DOĞRU, Nuran
Yüksek Lisans Tezi, Elk. Elektr. Müh. Böl.
Tez Yöneticisi: Prof. Dr. Sadettin ÖZYAZICI
Temmuz 1997, 105 sayfa

Bu tezde, MOS yapılı güneş pillerindeki yarı iletken devre elemanlarının karakteristiğini ve verimini etkileyen tuzak seviyelerinin çok düşük sıcaklıkta tesbitinin yapılması gerekiyordu. Bu nedenle Al-oksit-p-tipi silicon kristaller şeklinde MOS yapılı güneş pilleri tasarlanmış ve üretilmiştir.

Laboratuvar çalışmasında, güneş pilleri doğal yöntemle oksit tabakası yaratılarak ve vakuum buharlaştırma yöntemi ile Alüminyum metal kontaklar yaparak elde edilmiştir. Yarı iletken devre elemanlarındaki tuzak seviyelerinin oda sıcaklığında çabucak dolup ve boşalmalarından dolayı bütün ölçümler sıvı azot (77 K) gazı kullanan kriyostat içinde yapılmalıdır. Fotokapasitans tekniği kullanılarak bu tuzak seviyeleri belirlenebilir. Güneş pillerinin, tuzak seviyeleri , I-V, dI/dV ve kapasitansı Işık ayrıştırıcı, Kapasitans metre ve I-V karakteristik ölçüm düzeneği ile ölçülmesi gerekiyordu. Fakat deney süresince, I-V, C-V ve C-λ karakteristikleri elde edilememiştir, çünkü kriyostat çalıştırılamamıştır. Bu nedenle, kuantum verimi, emme katsayısı, I_p (fotoakım)-λ ve V_p (fotovoltaj)- λ gibi bazı fiziksel parametreler ölçülmüştür.

MOS güneş pillerinin veriminin maximum olabilmesi için açık-devre voltajı (V_{oc}), kısa-devre akımı (I_{sc}) ve düzeltme faktörünün (FF) mümkün olduğunca yüksek olması gerekir.

Oksit kalınlığının piller üzerindeki etkisini belirleyebilmek için, oksit kalınlığı farklı piller üretilmiştir. İnce bir oksit tabakasının kısa-devre akımını etkilemeden açık-devre voltajını artırdığı bilinmektedir.

Alüminyum kalınlığının pil üzerindeki etkisini gözlemlemek için, siliconun ön yüzü farklı kalınlıklarda Alüminyum ile kaplanmıştır.

Tuzak seviyeleriyle ilgili elde edilen bilgiler sadece güneş pillerinin verimini artırabilmek için değil yarı iletken malzeme kullanan diğer devre elemanlarının veriminin artırılmasına da yardımcı olabilecektir.

Anahtar Kelimeler: MOS güneş pilleri, tuzak seviyeleri, fotoakım, verim, çok düşük sıcaklık.

ACKNOWLEDGEMENTS

I would like to thank my supervisor Prof. Dr. M. Sadettin Özyazıcı for his help in the preparation of this work.

I wish to express my gratitude to Research Assistant Hayriye Tütüncüler for her great help and I would like to thank also to other assistans of Engineering Physics for the friendship they have shown.

Thanks are for Technician Mehmet Atlar for his help the laboratory.

Finally, special thanks to Research Assistans Serkay Özalıcı, Gölge Öğücü and Lecturer Filiz Bekem for their supports and helps.

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LIST OF SYMBOLS

E_f Fermi level (eV)

E_i Intrinsic fermi level (ev)

E_c Conduction band level

E_v Valance band level

E_g Band gap of semiconductor (ev)

E_t Activation energy of recombination center (ev)

p Hole concentration (cm^{-3})

n Electron concentration (cm^{-3})

n_i Electron concentration in intrinsic semiconductor (cm^{-3})

n_o The equilibrium electron concentration (cm^{-3})

ρ_o The equilibrium hole concentration (cm^{-3})

n_s Surface electron concentration (cm^{-3})

N_t Concentration of recombination center (cm^{-3})

k Boltzmann constant (J/K)

F_{ph} Flux

T Temperature (K)

G_{th} Thermal generation rate (cm^{-3} sec^{-1})

G_L Photo generation rate (cm^{-3} sec^{-1})

U Excess carriers recombination rate (cm^{-3} sec^{-1})

α_r Absorption coefficient (cm^{-1})

τ_p Hole bulk lifetime (sec)

τ_n Electron bulk lifetime (sec)

τ_r Radiative lifetime (sec)

σ_{cn} Electron capture cross section (cm^2)

σ_{cp} Hole capture cross section (cm^2)

V_{th} Thermal velocity (cm/sec)

C_n Electron capture coefficient (cm^3 / s)

C_p Hole capture coefficient (cm^3 /s)

e_p Hole emission coefficient (cm^3 /s)

e_n Electron emission coefficient (cm^3 /s)

ϕ_m Work function of the metal (V)

ϕ_s Work function of the semiconductor (V)

ϕ_B Barrier height (V)

ϕ_{bn} Barrier height for n-type solar cell (V)

ϕ_{bp} Barrier height for p-type solar cell (V)

V_{bi} Built in potential (diffused) (V)

V_{oc} Open circuit voltage (V)

V_G Gate voltage (V)

V_p Photovoltage (V)

Ψ_s Potential drop across the semiconductor

Ψ_{ox} Potential drop across the insulator (V)

Ψ_B Energy difference between actual Fermi and intrinsic fermi level (V)

V_{FB} Flat-band voltage (V)

V_d Drift velocity (cm/s)

V_a Applied voltage (V)

ϕ_o Energy difference between E_c and Fermi level

J current density (A/cm^2)

J_s Saturation current density (A/cm^2)

J_p Photocurrent density (A/cm^2)

I_o Dark saturation current (A)

I_p Photocurrent (A)

I_D Diode current (A)

I_{sc} Short circuit current (A)

P_i Incident solar power density

n Ideality factor

R_L Load resistance (Ω)

R_s Series resistance (Ω)

R_{sh} Shunt resistance (Ω)

q electronic charge C

A Active area of the solar cell (cm^2)

FF Fill factor

η Efficiency of solar cell (conversion energy)

η_q Quantum efficiency of solar cell

c_f correction factor

λ_g Wavelength of photon (m)

C_{ox} Oxide capacitance (F)

x_i insulator affinitiy

T_{ox} Oxide thickness (cm)

Q_M Charge on metal (C)

Q_s Total charge stored in a semiconductor (C)

Q_B Ionized acceptor ions in the depletion charge (Bulk Charge) (C)

Q_n Charge density in the inversion layer (C/cm^2)

ε_s Permitivity of semiconductor

ε_{ox} Permitivity of oxide layer

ε Electric field strength (V/ cm)

w Width of depletion region (cm)

w_{max} Maximum depletion region width (cm)

L_D Deby length

N_c Effective density of states in the conduction band

N_D Donor concentration (cm^{-3})

N_A Acceptor concentration (cm^{-3})

μ_n Electron mobility (cm^{-2}/V-sec)

μ_p Hole mobility (cm^{-2}/V-sec)

D_n Diffusion coefficient for electron

D_p Diffusion coefficient for hole

m^* Effective mass (kg)

R^{**} Effective Richardson constant (A/cm^2-K^2)

L_n Diffusion lengths for electrons

L_p Diffusion lengths for holes

hv Photon energy

q Electron charge (C)

CHAPTER 1

INTRODUCTION

Many societies across the world in which we live have developed a large appetite for electrical energy. This appetite has been stimulated by the relative ease with which electricity can be generated, distributed, and utilized, and by the great variety of its applications. It is arguable whether the consumption of electricity should be allowed to grow unchecked, but the fact that there is an ever-increasing demand for this synthetic energy form. Clearly, if this demand is to be met then the world's electricity generating capacity will have to continue to grow. The prospects for meeting this demand would be improved if alternative energy sources were to be developed. The sun is one such source and conversion of sunlight directly into electricity via the photovoltaic effect is one method of generating solar electricity. The heart of any photovoltaic power system is the solar cell. It is the transducer that converts the sun's radiant energy directly into electricity, and basically a semiconductor diode capable of developing a voltage of 0.5-1 V and a current density of 20-40mA cm^{-2} depending on the material used and the sunlight conditions. The connection of solar cells in series and parallel and incorporation into module provides a higher rated until which can be interconnected with similar modules to comprise an array. The maximum efficiency for the conversion of sunlight to electricity via the photovoltaic effect around 25% for unconcentrated sunlight conditions on earth the maximum solar power intensity is close to $1kWm^{-2}$. Under these conditions the maximum possible electrical output is 250W for every square meter of transducer. Thus an appropriate positioned residential rooftop of area $80m^2$ could in principle, realize a peak electrical power of 20kW whilst, at the central power station level, e.g., a peak rating of 250MW, a transducer area of at least $10km^2$ would be required.

Metal oxide semiconductor (MOS) solar cell have been studied by many workers as a low cost alternative to the p-n junction solar cells and they are significantly simpler to fabricate. They are also formed at low temperature without any appreciable degradation in the bulk properties of the semiconductor.

MOS solar cell has properties which are in general intermediate between those of Schottky barrier (metal-semiconductor contact) and p-n junction. The dark current in the MOS device may be dominated either by majority carriers (as in Schottky barrier) or by minority carriers (as in p-n junction). This creates two classes of MOS cells the so called *Majority Carrier* and *Minority Carrier Cells.* The photocurrent of course, is in both cases due to minority carriers.

The insertion of a very thin insulating layer between the metal and semiconductor of a Schottky contact can make a dramatic difference to its operation. The range of the insulator thickness which has been considered for the Al-SiO_2 -(p- type) Si device is 10-28 A°. If the insulator was thin enough, then

a) the dominant carrier flow for a given semiconductor type can be controlled by selection of the metal work function, and

b) if the contact metal work function and substrate dopant type (p or n) are chosen so that minority-carrier current flow is dominant, the *MIS diode* so formed is electronically equivalent to a conventional *p-n junction diode.* For Si substrates, minority-carrier operation can be obtained if the insulating layer is kept <16 A°, and low work function metals (Al, Ti, Be, Mg) are used with p-type substrates and high work function metals with n-type.

In contrast therefore to Schottky devices, such minority carrier Metal-Insulator-Semiconductor (min MIS) devices possess the same photovoltaic abilities as p-n junction solar cells [38].

If the insulator thickness is further decreased, the tunnel currents increase to the point where they are sufficiently large enough to disturb the

semiconductor from thermal equilibrium. This occurs around 28 A° for Al-SiO_2 -(p-type) Si. Thus in general below some critical value of insulator thickness, " nonequilibrium" tunnel MIS diodes are formed. Over a certain bias range, the MIS tunnel diode operates in this nonequilibrium mode where the diode current is semiconductor limited (due to generation-recombination in the bulk) and the tunnel current merely acts an OHMIC contact. Such nonequilibrium diodes can be further classified as majority carrier, surface state or minority carrier devices depending on whether the dominant tunnel-current flow near zero bias is between the metal and majority-carrier band, the surface states, or the minority carrier band. Which diode is formed depends on whether the semiconductor-insulator interface at zero bias is accumulated, depleted or strong inversion. The contact-metal work function is the most important parameter in determining which of these states exist. For example, minority carrier diodes can be formed on p-type silicon substrates by selecting metals, such as aluminum, have a low value work function ϕ_m.Conversely, a high work value of ϕ_m , such as gold, is needed to form a minority carrier diode on n-type silicon majority-carrier dodes, the converse of the above description applies. Minority-carrier devices, on the other hand, can show I-V characteristics which obey the ideal Shockly diode equation and one suitable for photovoltaic conversion.

If the thickness of the insulator is further decreased to about 10 A° the concept of a tunnel MIS diode apparently becomes invalid (primarily based on experimental evidence). Below 10 A° it appears to be more appropriate to describe such sctructures as Schottky barriers.

Briefly above 28 A° the devices becomes an equilibrium *Tunnel Diode* and below 10 A° it exhibits *Schottky behaviour.*

The thin insulating layer allows control over not only the magnitude of the dark current flowing through the diode but also the dominant type (majority or minority carrier) of current.

A theoretical analysis [39] has provided the motivation for introducing a thin oxyide interfacial layer between the metal and silicon in a Schottky barrier (MIS) for increasing the open circuit voltage.

Recent experimental work [40-47] has shown that the presence of thin interfacial insulating layer of oxide between the metal and semiconductor of a Schottky barrier can considerably increase the photovoltaic conversion efficiency.

The various parameters that influence the performance of MIS-type solar cell are the following; insulator thickness, resistivity of substrate, insulator charge surface, state density, minority carrier lifetime, and crystal orientation.

In the construction of a solar cell it is important to maintain the lifetime at as high a value as possible in order to preserve the optically generated hole and electron pairs. In a solar cell the fundamental conversion of light energy to electrical energy is performed when photons are converted to electron-hole pairs with the semiconductor. Absorption of photons by semiconductor as a function of the frequency of the photons, the nature of the semiconductor and the thickness of the semiconductor. Beyond the cut-off wavelengths which no electron-hole pairs will be produced (the semiconductor is nonabsorbing).

The first aim of this thesis is to design and fabricate MOS structure solar cell. The second aim is to improve the performance and the stability of MOS solar cell and also investigate the deep levels. Parameters which are related to the device efficiency is analyzed by using the I-V and C-V characteristics of MOS solar cell. Effects of the oxide charges and interface states in the Si-SiO_2 interface are investigated. Barrier height modification caused by interfacial layer containing positive charge is demostrated and this effect is seen as possible explanation for the heght barriers recorded.

This study has been arranged as follow ; Chapter 2 gives review about the metal-semiconductor contacts. Chapter 3 includes mechanism of

recombination processes. As an introduction to MOS solar cell theory, some of the basic semiconductor and MOS structure properties and its some important characteristics are explained in Chapter 4. Chapter 5 deals with design and construction of minority carrier MOS solar cell. The theory of experimental sets are explained in this chapter. The experimental results are obtained from fabricated MOS structure solar cells and design criterias are also discussed in this chapter. Finally, overall conclusion and remarks are given last chapter.

CHAPTER 2

METAL-SEMICONDUCTOR JUNCTIONS

2.1 Introduction

When a metal is making intimate contact with a semiconductor, the Fermi levels in the two materials must be coincident at thermal equilibrium. At far left, the metal and semiconductor are not in contact, and the system is not in thermal equilibrium. If a wire is connected between the semiconductor to the metal and thermal equilibrium is established, the Fermi levels on both sides line up. Relative to the Fermi level in the metal the Fermi level in the semiconductor is lowered by an amount equal to the difference between the two work fuctions.

The work function is the energy difference between the vacuum level and the Fermi level. For a semiconductor, it is useful to work with the *electron affinity,* which is defined as the energy needed to take an electron from the bottom of the conduction band E_c to the vacuum level. Work function of a semiconductor varies with the position of the Fermi energy relative to the band edges and hence with the doping level, and is therefore less useful than electron affinity.

Electrical junctions between metals and semiconductors fall into one of two groups, namely ohmic contact, and rectifying contacts. The non-rectifying junction has a low ohmic drop regardless of the polarity of the externally applied voltage and is called the OHMIC CONTACT. All semiconductor devices ohmic contacts to make connection to other devices or circuit elements. The rectifying junction is commonly known as the SCHOTTKY - BARRIER diode.

2.2 Rectifying n-type Semiconductor Contacts

A rectifying barrier may exist at an *n*-type semiconductor contact, if the termionic work function ϕ_m of the metal is greater than the semiconductor work function ϕ_s shown in figure 2.1(a). As before electrons flow from the lower work function material, that is, from the semiconductor, until the Fermi levels align. The resulting energy-band structure after contact is shown in figure 2.1(b). Under equilibrium conditions a potential barrier known as the DIFFUSION POTENTIAL, of ϕ_m-x exists between the two materials, where x is the depth of the conduction band of the semiconductor. There is a region, known as the DEPLETION LAYER, between the two materials in which there is no free charge carrier since electrons in that region have transferred to the metal. The resistivity of this region is therefore much greater than that of the semiconductor itself. Thus current flow can only takes place if the voltage applied to the junction is in the correct direction to overcome the diffusion potential. That is, a rectifying junction is formed which permits current to flow easily in one direction, but not in the reverse direction. A practical application of the metal to *n*-type rectifying contact is to the so called HOT CARRIER DIODE or SCHOTTKY BARRIER DIODE.

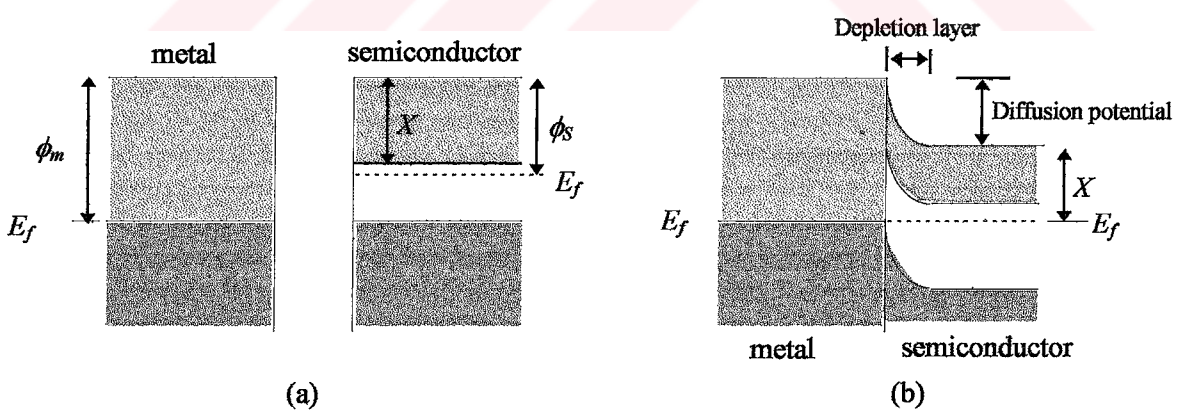


Figure 2.1 Energy-band diagrams for a metal-to-semiconductor rectifying contact (a) before contact and (b) after contact.

Like pn junction, a rectifying contact cannot usually be formed by merely pressing together ordinary specimens of material, an ohmic contact being the usual result of such endeavor. At the very least, a good rectifying contact requires that the surface of the semiconductor specimen be polished

or etched in order to remove imperfections produced in cutting the specimen from the original ingot. Otherwise, the very short minority-carrier lifetime in the surface region of the semiconductor precludes rectifying action. When a rectifying *n*-type contact exists the polarities of the applied voltages for forward and reverse bias, and the actions occuring at the contact are similar to those for a pn junction, the metal of the contact acting somewhat as a junction *p*-region. That is, the contact is forward biased when the metal is positive and reverse biased when it is negative, and the current-voltage characteristic is defined by the diode equation.

2.3 Rectifying p-type Semiconductor Contacts

Figure 2.2 shows an energy-level diagram for a *p*-type semiconductor contacts under equilibrium conditions. As in the energy diagram for the *n*-type contact, ϕ_m is the work function of the metal and ϕ_s is that of the semiconductor, ϕ_s being approximately the vertical distance between the reference level ($E=0$) and the top of the valance band. With the Fermi levels aligned for zero applied voltage, deep in the *p*-region the top of the valance band is just below the Fermi level, but at the contact, it is ϕ_s below the reference level ($E=0$). As a result, a barrier (contact potential) of ($\phi_s - \phi_m$) exists to electron flow from the metal to the *p*-region and to hole flow from the *p*-region to the metal. Unlike the *n*-type contact, no barrier exists to the flow across the contact of metal-region holes and *p*-region electrons. As in the junction, the current I_1 of the metal-region electrons able to surmount the barrier is equal to the current I_2 of *p*-region electrons "falling down" the barrier, and the net electron current is zero. Similarly, current I_3 of metal-region holes falling down the barrier is equal and opposite current I_4 of holes climbing the barrier, and the net contact current is zero.

The effect of making the *p*-type semiconductor negative with respect to the metal is shown by the energy-level diagram of Figure 2.3. Unlike the effect on the *n*-type contact, this polarity of applied voltage increases the barrier to the flow of majority carriers across the contact, and the contact is reverse biased. Figure 2.4 shows the reduction of the barrier to majority -

carrier flow when the *p*-region is positive with respect to the metal, forward-biasing the contact.

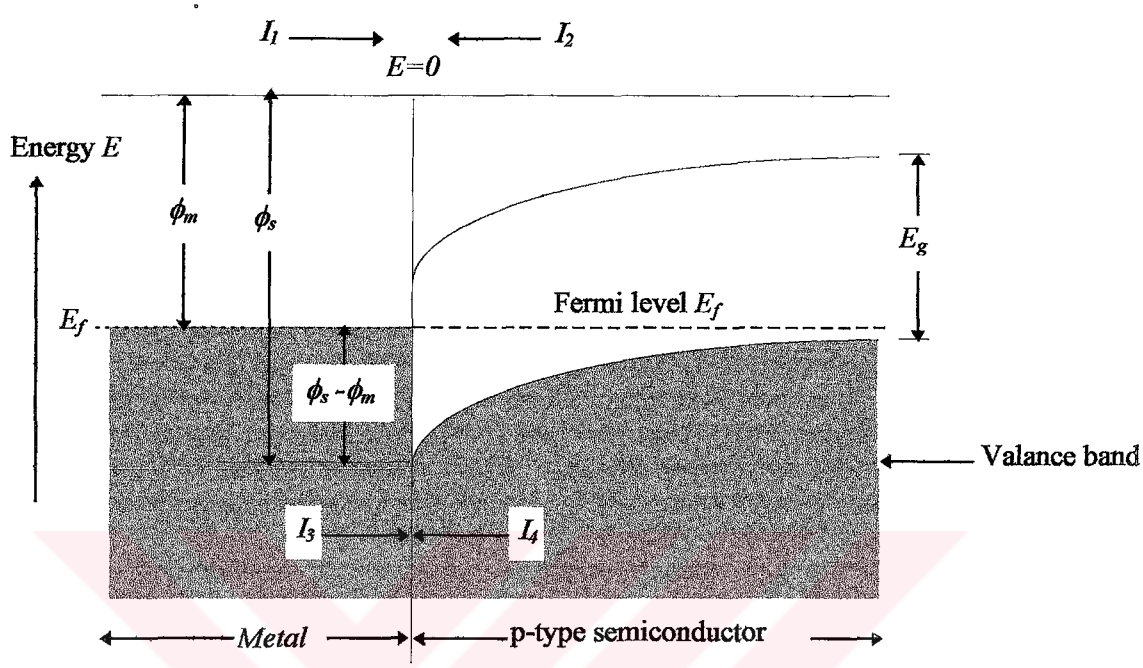


Figure 2.2 Energy-level diagram for a metal-to-*p*-type semiconductor contact under equilibrium conditions (zero bias). A barrier of $(\phi_s-\phi_m)$ exists at the contact for metal-region electrons and *p*-region holes. Majority and minority electron currents I_1 and I_2 are equal and opposite as are minority and majority hole currents I_3 and I_4.

We see that a rectifying barrier may exist at a *p*-type semiconductor contact if the thermionic work function ϕ_s of the semiconductor is greater than the metal work function ϕ_m. It is of interest to note that the polarity of the applied voltage for forward operation of the *p*-type contact is just the opposite to that of the *n*-type contact. This difference was the first indication of the existence of two semiconductor types , and the distinguishing designations, *n* and *p*, as originally used referred to the polarity of the semiconductor for easy flow of current . This serves as a method for determining the type of a semiconductor, but it is not a particularly good one, owing to the difficulty in obtaining a rectifying contact.

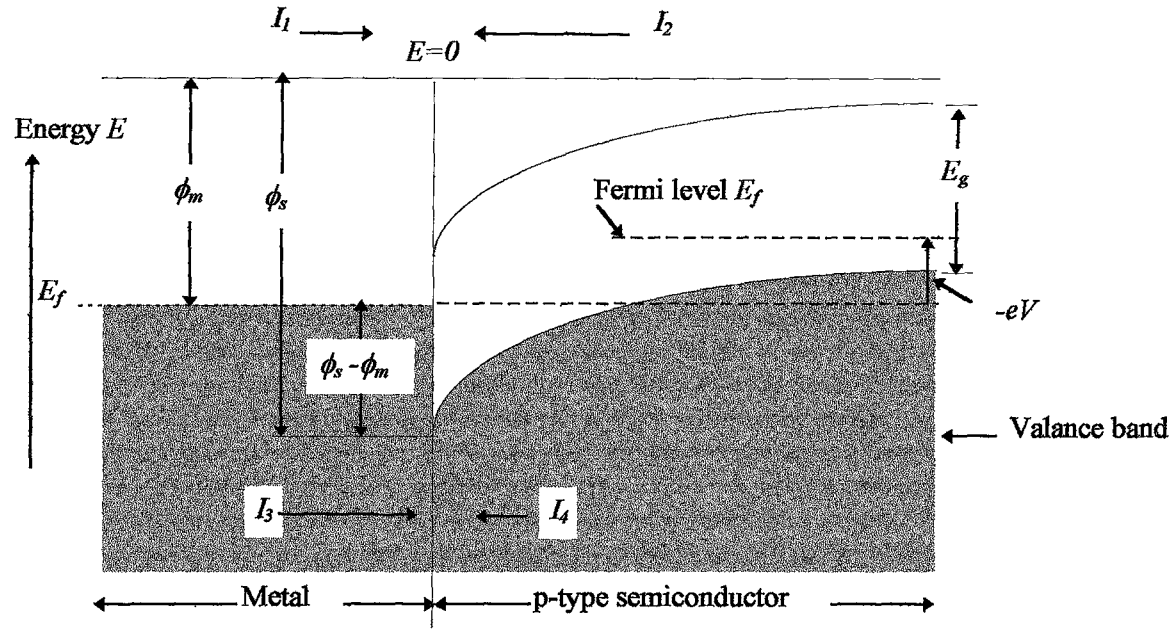


Figure 2.3 Energy-level diagram for a reverse-biased metal-to-*p*-type semiconductor contact. The *p*-region is negative by the voltage V, increasing the barrier to metal-region electrons and to *p*-region holes and reducing majority-electron current I_1 and majority-hole current I_4 below the equilibrium values. Minority-electron current I_2 and minority-hole current I_3 are unaffected by bias.

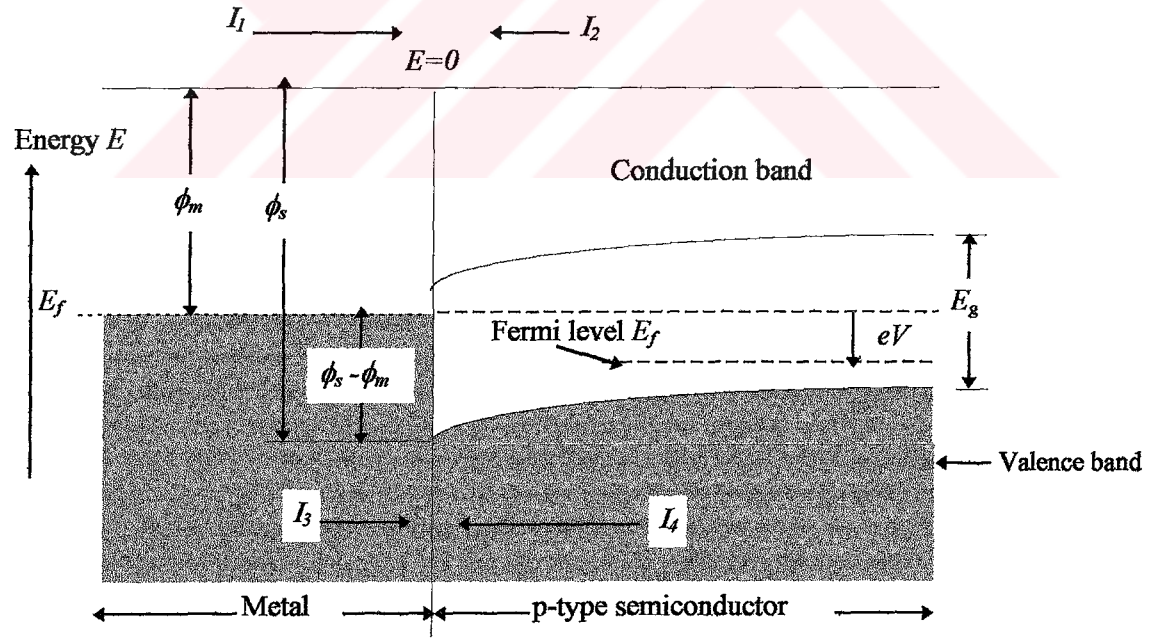


Figure 2.4 Energy-level diagram for a forward-biased metal-to-*p*-type semiconductor contact. The *p*-region is positive by the voltage V, decreasing the barrier to metal-region electrons and to *p*-region holes and increasing majority-electron current I_1 and majority-hole current I_4 above the equilibrium values. Minority-electron current I_2 and minority-hole current I_3 are unaffected by bias.

2.4 Ohmic Contacts

An ohmic contact is one at which rectification or some other non-linear effect does not occur. This definition attributes a certain characteristic to the contact. In practical semiconductor-diode or transistor device fabrication, the term ohmic contact may be used to describe any contact which allows charge carriers to move freely into and out of the device and does not interfere with the operation of the device. Such requirements as low resistance, not injecting minority carriers, and electrical and mechanical stability may be considered. Electrical stability implies mechanical stability. If the ohmic properties of both the semiconductor and contact material remain unchanged up to the contact surface, and if no barriers exist at the contact, the resistance of the material-contact structure will be that of the materials themselves. It is difficult to make a contact which is completely free of barriers at the contact interface. It is, however, readily possible to make contacts which are suitably ohmic in nature so as not to interfere with the operation of the semiconductor device.

The most obvious approach to making a low-resistance contact would be to make the contact area large. This is indeed done when such a technique is applicable. It has been shown that simple barrier-layer theory would indicate that it is possible to make an ohmic contact if one chooses the correct relationship between the contact-material work function and that of the semiconductor. This relationship requires the choice of a contact material of work function smaller than that of the semiconductor for *n*-type semiconductors and one of work function larger than that of the semiconductor for *p*-type. This relationship does not seem to work in practice in all cases. It is found that most metals make rectifying contacts to semiconductors when the semiconductor surfaces are in good condition, while most metals make ohmic contacts if the semiconductor surfaces are damaged. In other words, it is the condition of the surface rather than the choice of materials which largely governs the properties of the contact. Certain useful techniques of polishing, etching, soldering, etc., are known to give the desired results. Some of these techniques will be described briefly,

and a theoretical picture presented which may give an approximately correct idea of the reason that ohmic contacts can be made.

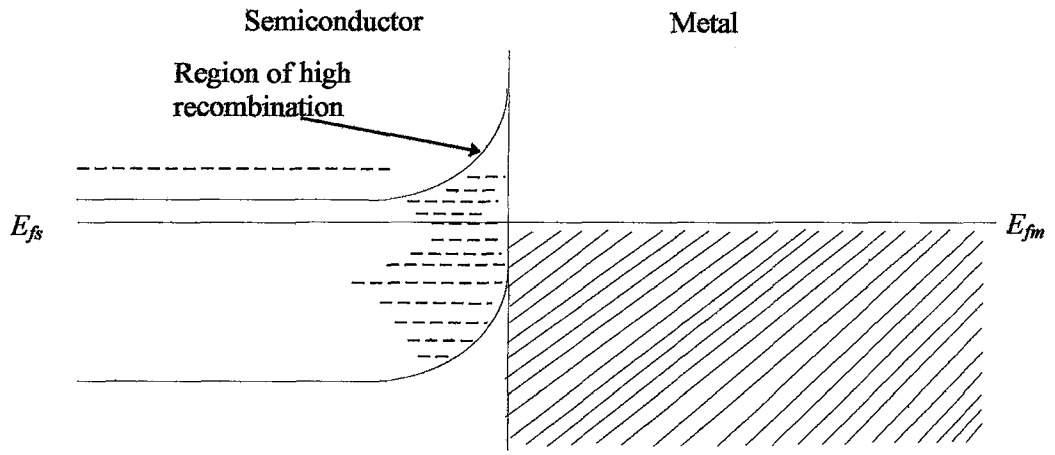


Figure 2.5 A possible picture of an ohmic contact in which the ohmicity is attributed to the high recombination near the contact. The extra allowed states near the contact are due to surface damage to the semiconductor before contact is made.

Most ohmic contacts which are made by damaging the semiconductor surface or disrupting the band structure depend on the resulting very high recombination rate of electrons and holes near such a region to overcome the effects of any barrier which may be present. The band structure at a sandblasted or mechanically ground and polished surface may look something like that in Fig.2.5. We see that both holes and electrons are free to move across the contact region and recombine readily in the damaged layer.

It is found that soldering to a semiconductor surface with a material of the same type as the impurity type of the semiconductor results in a good ohmic contact. It is possible that the soldering process diffuses the impurity into the surface, giving a very highly doped region such as is shown in Fig.2.6. The effect at the contact is to reduce the barrier to electrons greatly by making it so narrow that electrons may tunnel through it.

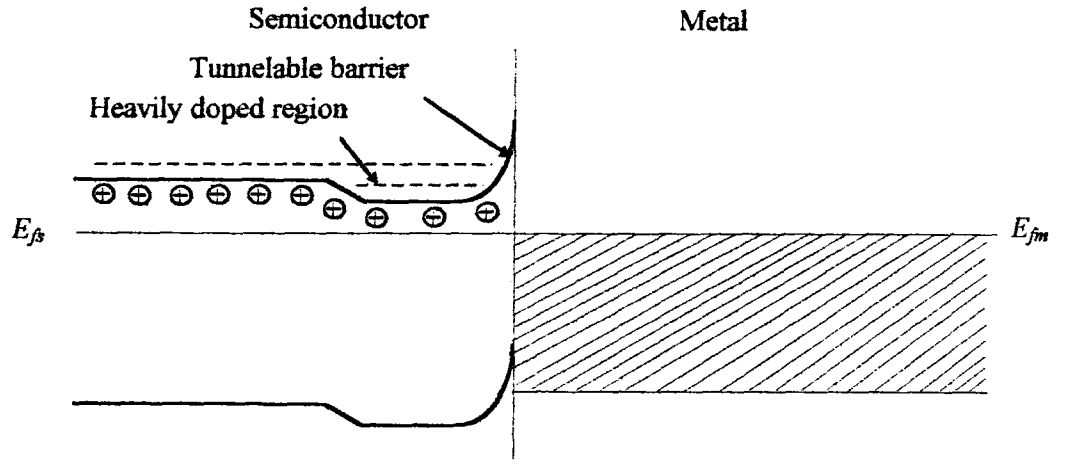


Figure 2.6 An ohmic contact due to very heavy doping of the semiconductor near the contact. This doping may be due to diffusion of solder into the surface of the semiconductor in the case of soldered contacts to the semiconductor surface. The barrier which remains at the contact interface is so thin that the electron can tunnel through it.

Bonding techniques which make use of wires of appropriate types pressed or spot-soldered to the various device layers are numerous. There are also many details, too numerous to go into here, associated with preparation of surfaces and contact areas, choice of contact materials, chemical treatments, etc. Many problems arise in any fabrication process, and many of these problems have been ingeniously solved.

2.5 Ohmic Contacts for p and n-type Semiconductor

Since the presentation of the last two sections was based on the conditions that $\phi_m > \phi_s$ for the *n*-type contact and $\phi_s > \phi_m$ for the *p*-type contact, let us now consider contacts in which these conditions are not met. Figure 2.7 shows an energy-level diagram for the contact between a metal and an *n*-type semiconductor for which $\phi_s > \phi_m$. The diagram is for zero applied voltage and depicts the situation the instant after contact is established. We observe that, near the metal, the lower edge of the semiconductor conduction band lies below the Fermi level, producing the depression A. Electrons immediately flow into this depression, just as a liquid would flow into a depression in its surface, and the depression is obliterated. Thereafter, electrons may flow

unimpeded in either direction in the semiconductor conduction band, and we have a nonrectifying or ohmic contact. Similar reasoning shows the absence of a rectifying barrier at a contact between a metal and a *p*-type semiconductor for which $\phi_s<\phi_m$..

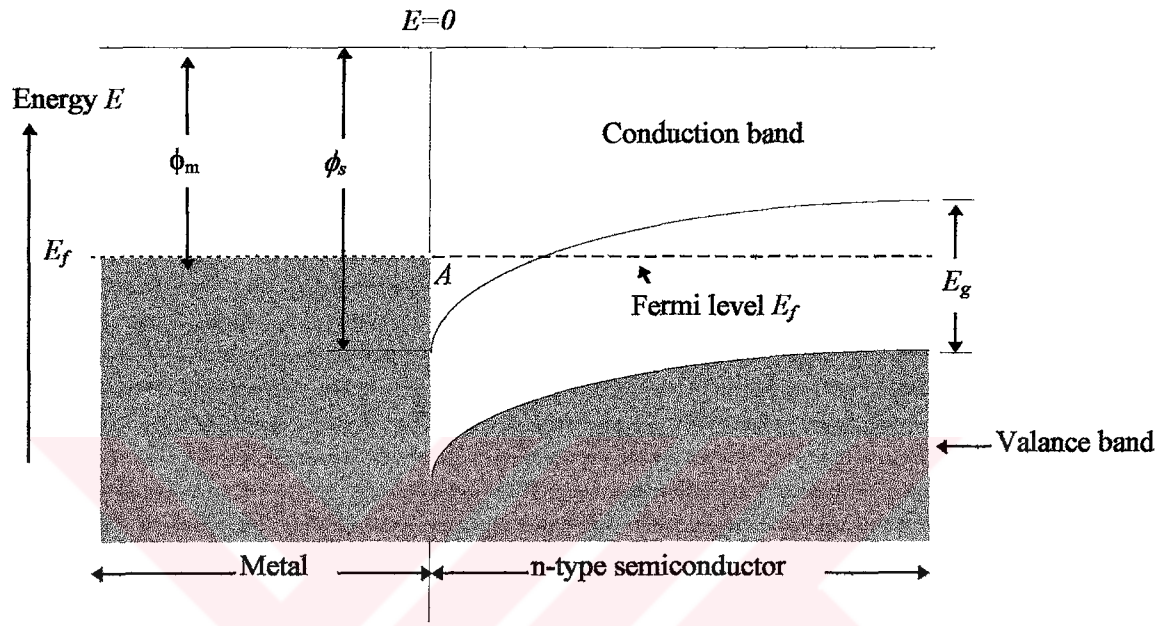


Figure 2.7 Energy-level diagram for a contact between a metal and an *n*-type semiconductor for which $\phi_s > \phi_m$. Conditions are depicted immediately after contact. Depression *A* subsequently fills up with electrons and the contact becomes resistanceless.

Such contacts are ideally resistanceless, the only resistance present being that of the metal and semiconductor specimens and their connections. Thus, we see that an ohmic contact to a semiconductor can be obtained by choosing metals such that $\phi_m<\phi_s$ for *n*-type material and $\phi_m>\phi_s$ for *p*-type material. Ohmic contacts may also exist as a result of semiconductor surface imperfections that reduce the minority-carrier lifetime and, for this reason, the crystalline structure at the surface of a semiconductor may be deliberately damaged, say by sandblasting, when an ohmic contact is to be made. Soldering or welding leads to a semiconductor usually results in a ohmic contact, owing to surface damege. When the minority-carrier diffusion length is short compared to the width of the transition region, almost all carrier recombination takes place in the transition region, and no change occurs in the carrier density on either the *p*-side or the *n*-side of the contact. (That is,

no minority-carrier injection occurs upon the application of a voltage of the polarity that would forward-bias a rectifying contact.) The currents in the metal

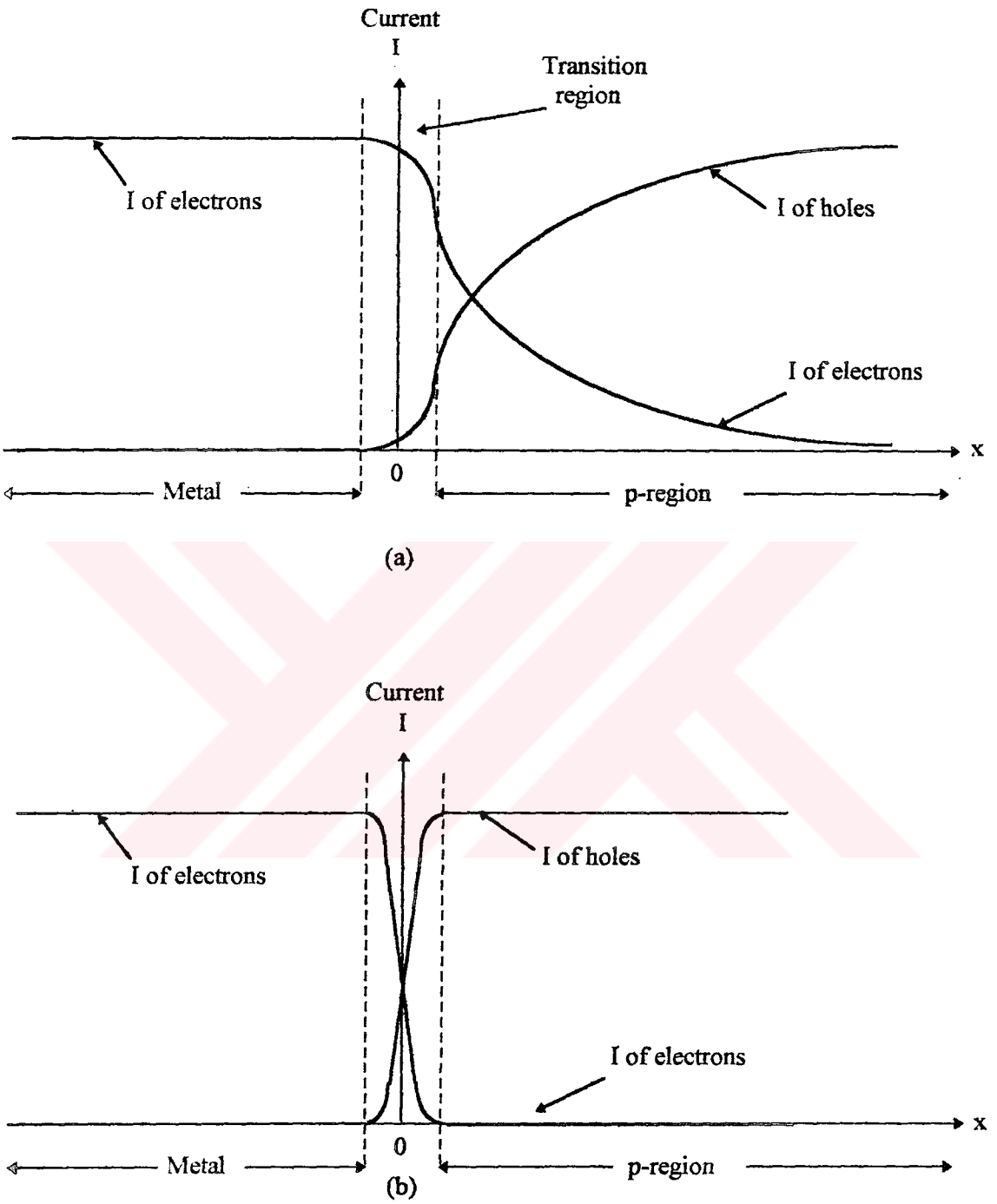


Figure 2.8 Hole and electron currents in the metal-and *p*-region near a forward-biased metal-*p*-type contact. (a) A rectifying contact for which diffusion length >> width of transition region. (b) Ohmic contact for which diffusion length << width of transition region.

and semiconductor regions near a forward-biased contact are shown in Fig. 2.8 (a) for a rectifying contact, in which some recombination occurs in the transition region, and in Fig. 2.8 (b) for an ohmic contact. Because of the high

conductivity of the metal, the hole current in the metal region is represented as being negligible. As pointed out earlier, an ohmic contact is the usualresult of pressing a metal against a semiconductor specimen, or of pressing together specimens of *p*-type and *n*-type material, owing to imperfections in the semiconductor surface.

An ohmic contact can also be thought of as a contact having a very large reverse-saturation current, owing to short minority-carrier difusion length in the semiconductor region. According to the diode eguation,there are negligible differences in the magnitudes of the forward and reverse voltages for forward and reverse currents of equal magnitude, providing the magnitude is small compared to the reverse-saturation current. Therefore, rectifying contacts and pn junctions appear to be ohmic for very small currents and conversely contacts that appear to be ohmic for small currents may show nonohmic characteristics for large current.Therefore rectifying contacts and pn junctions appear to be ohmic for very small currents and conversly contacts that appear to be ohmic for small currents may show nonohmic characteristics for large currents.

2.6 Current Transport Processes

The current transport in metal-semiconductor contacts is mainly due to majority carriers, in contrast to pn junctions, where the minority carriers are responsible. Figure 2.9 shows four basic transport processes under forward bias (the inverse processes occur under reverse bias).

The four processes are

1. Transport of electrons from the semiconductor over the potential barrier into the metal (the dominant processes for Schottky diodes with moderately doped semiconductors (e.g., Si with $N_D \leq 10^{17}$ cm^{-3} operated at moderate temperatures (e.g., 300°K)).

2. Quantum-mechanical tunneling of electrons through the barrier (important for heavily doped semiconductors and responsible for most ohmic contacts).

3. Recombination in the space-charge region (identical to the recombination processes in a pn junction.

4. Hole injection from the metal to the semiconductor (equivalent to recombination in the neutral region).

In addition, we may have edge leakage current due to the high electric field at the contact periphery or interface current due to traps at the metal semiconductor interface. Various method have been used to improve the interface quality, and many device structures have been proposed to reduce or eliminate the edge leakage currents.

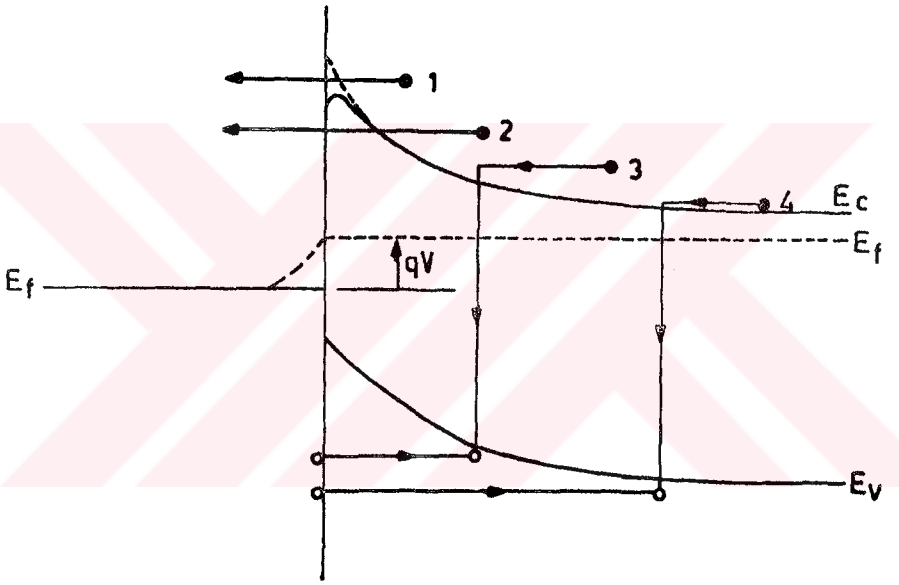


Figure 2.9 Four basic transport process under forward-bias.

The application of an external bias to a metal-semiconductor junction will after the relative position of the Fermi levels, and hence the energy bands in the semiconductor. This is similar to the effect in a pn junction but with one important exception; we saw that in a pn system current transport is dominated by minority carriers, but in a metal- semiconductor system thermionic emission of majority carriers over the potential barrier is the major source of current flow. Consider Figure 2.10. In equilibrium, with no applied bias, there are two drift currents, of equal magnitude but opposite directions, which flow across the junction because of the built-in electric field-this again

is similar to a pn junction. The current densities will be proportional to the electron concentration *n* in the junction region, i.e.

$$J_{sm} = J_{ms} = C_n \tag{2.1}$$

where *C* is a constant. Note that the arrows represent current flow; because we are dealing with electrons, the charge flow is in the opposite direction. At the surface of the semiconductor becomes

$$n = N_c \exp\left(-\frac{e\phi_{bn}}{kT}\right) \tag{2.2}$$

For $V>0$, i.e. the application of a forward bias to the junction, the built in potential V_{bi} is lowered by *V*. However, the barrier height ϕ_{bn} (the difference between the metal work fuction and the electron affinityt of the semiconductor) is unaltered (Fig. 2.10(b)). This has the effect of increasing the electron density at the semiconductor surface, thereby increasing J_{sm}, but J_{ms} remains as before. There is a net current flow across the barrier given by,

$$J = J_{sm} - J_{ms}$$

$$= CN_c \exp\left(-\frac{e(\phi_{bn} - V)}{kT}\right) - CN_c \exp\left(-\frac{e\phi_{bn}}{kT}\right)$$

$$= CN_c \exp\left(-\frac{e\phi_{bn}}{kT}\right)\left[\exp\left(\frac{eV}{kT}\right) - 1\right] \tag{2.3}$$

This can be simplified to

$$J = J_s\left[\exp\left(\frac{eV}{kT}\right) - 1\right] \tag{2.4}$$

where

$$J_s = CN_c \exp\left(-\frac{e\phi_{bn}}{kT}\right) \tag{2.5}$$

CN_c is found to be equal to $R^{**} T^2$, where R^{**} is the effective Richardson constant, and depends on the effective mass m^* of the carriers. It is given by

$$R^{**} = \frac{4\pi m^* ek^2}{h^3} \tag{2.6}$$

For reverse bias, i.e. $V<0$, again J_{ms} is unaltered, but J_{sm} is smaller than in the equilibrium case. The net effect is that (2.4) becomes

$$J = J_s\left[\exp\left(\frac{eV}{kT}\right) - 1\right] \tag{2.7}$$

Equations (2.4) and (2.7) are similar to the I-V characteristics obtained for a pn junction. They can similarly be simplified for large magnitudes of V, and similarly have an ideality factor (usually between 1.0 and 1.3 for a metal-semiconductor junction) introduced into the denominator of the exponential term. The current carrying mechanisms are very different, however, and the constant J_s is derived from totally different physical parameters in either case.

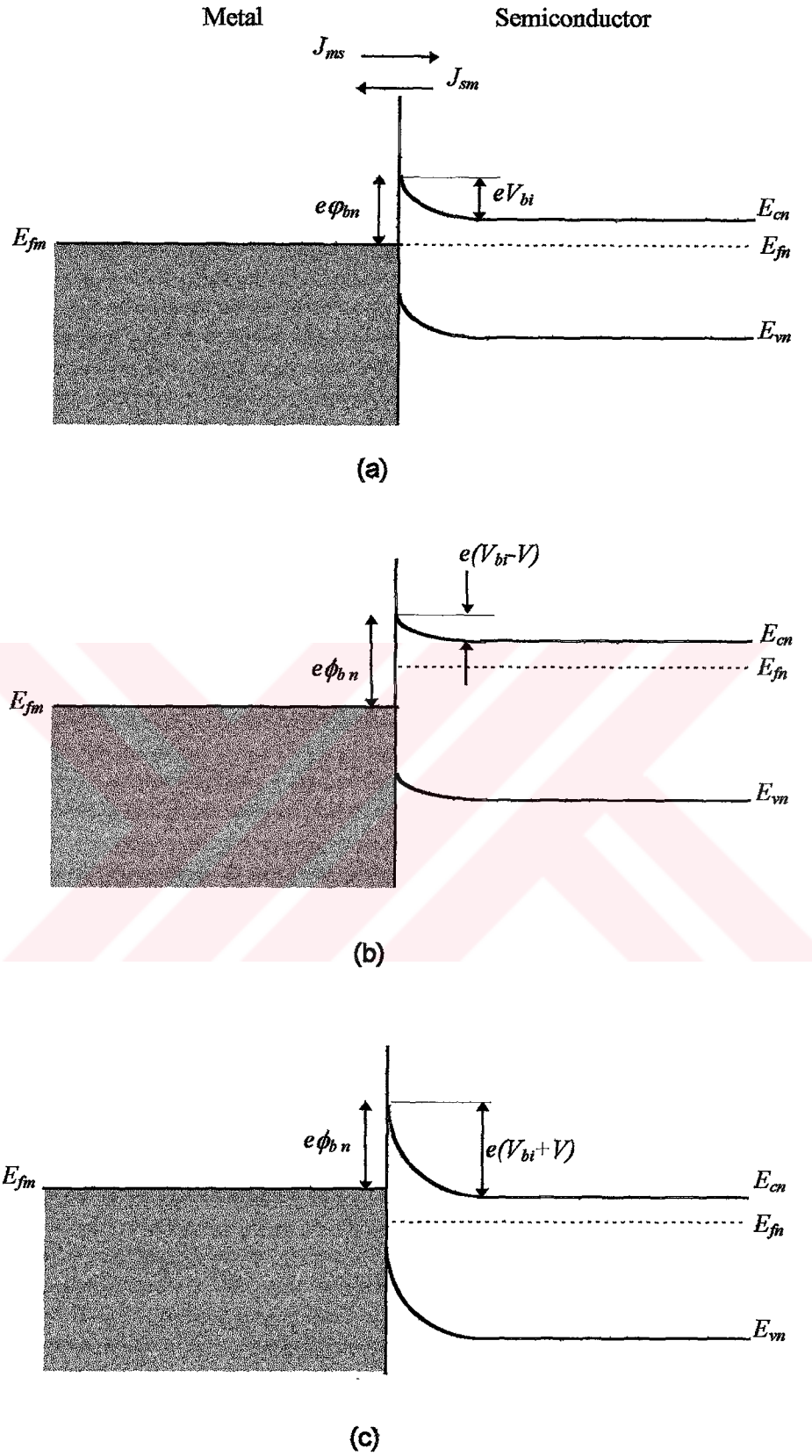


Figure 2.10 Band diagrams for a metal-semiconductor junction with an applied bias (a) $V = 0$, (b) $V > 0$, (c) $V < 0$.

CHAPTER 3

CARRIER RECOMBINATION

3.1 Introduction

Under thermal equilibrium carriers in semiconductors possess an average thermal energy corresponding to the ambient temperature. This thermal energy enables some valance electrons to reach the conduction band. The upward transition of an electron leaves a hole behind so that an electron-hole pair is produced. This process is called CARRIER GENERATION and is represented by G_{th} in Fig 3.1a, When an electron makes a transition from the conduction band to the valance band, an electron-hole pair is annihilated. This reverse process, called RECOMBINATION, is represented by R_{th} in Fig 3.1a. Under thermal equilibrium, the generation rate the recombination rate must be equal so that carrier concentrations remain constant. Thus, the condition $pn=n_i^2$ is maintained.

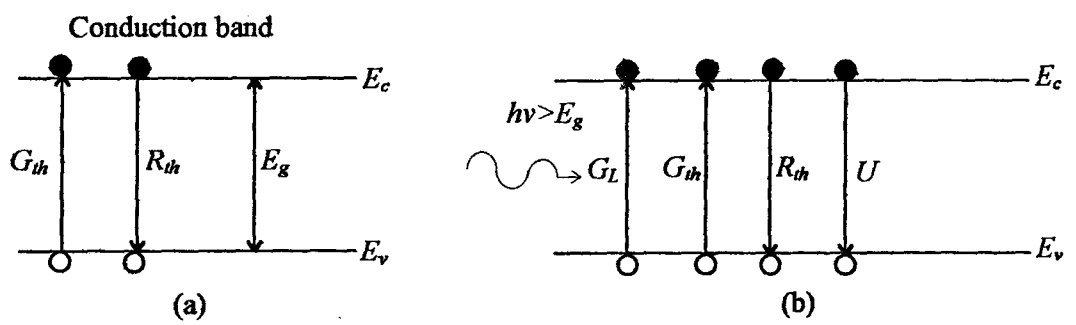


Figure 3.1 Band-to-band generation and recombination of electron-hole pairs. (a) at thermal equilibrium and (b) under optical illustration.

The equilibrium condition may be disturbed by the introduction of free carriers exceeding their thermal equilibrium values. This process, called

CARIER INJECTION, can be accomplished by either optical or electrical means. Optical injection involves an incident light having photon energy equal to or greater than the band-gap energy E_g. The photon energy is given by the product hv, where v is the frequency of the light and h is Planck's constant. When the optical energy is absorbed by an electron in the valance band, the electron is excited to the conduction band and a hole is created in the valance band. The generation rate of electron-hole pairs by light is shown in Fig 3.1b. The injection of carriers increases the electron and hole densities such that $pn > n_i^2$. The additional carriers are called EXCESS CARRIERS. The excess electrons and holes are always in equal number so that space charge neutrality is preserved.

Excess electrons in the conduction band may recombine with holes in the valance band, as represented by U in Fig 3.1b. Thus, the optically generated electron-hole pairs may be annihilated and the thermal equilibrium density may be reestablished. The energy released by the recombination is emitted as a photon or phonons depending on the nature of the recombination mechanism. When a photon is emitted the process is called RADIATIVE RECOMBINATION. On the other hand, the lack of photon emission indicates a NONRADIATIVE RECOMBINATION process, which emits phonons to the lattice in the form of heat dissipation.

3.2 Band-to-Band Recombination

Band to band recombination, also referred to as DIRECT THERMAL RECOMBINATION, is conceptually the simplest of all recombination process under this condition, an electron in the conduction band can simply give up its energy to move down and occupy the empty state (hole) in the valance band without a change in momentum. This is the most efficient way to annihilate an electron hole pair in a direct-band semiconductor. When it happens, the energy given up by the electron will be emitted as a photon, the quantum of light. All available information about the band-to-band radiative recombination has been obtained from the optical absorption coefficient α_f of the

semiconductor. The rate G_r at which electron-hole pairs generated radiatively under thermal equilibrium can be determined by

$$G_r = \alpha_r p_o n_o = \alpha_r n_i^2 \tag{3.1}$$

Then, the excess carrier recombination rate is given as

$$U_r = \frac{G_r}{n_i^2}\left(pn - n_i^2\right) = \frac{G_r}{n_i^2}(n_o + p_o + p_e)p_e \tag{3.2}$$

The radiative lifetime τ_r is now obtained as

$$\tau_r = \frac{n_i^2}{G_r(n_o + p_o + p_e)} \tag{3.3}$$

For a strongly n-type semiconductor having a donor concentration $N_D, n_o \cong N_D, p_o \cong 0$ and neglectin p_e low-level injection lifetime is defined as

$$\tau_r = \frac{n_i^2}{G_r N_D} \tag{3.4}$$

At high-level injection, p_e is large and

$$\tau_r = \frac{n_i^2}{G_r p_e} \tag{3.5}$$

3.3 Auger Recombination

The energy released by the direct recombination is absorbed by a second electron in the conduction band. This second electron after being kicked upward loses its energy to the lattice by scattering events. This is known as AUGER RECOMBINATION. There are different possibilities when traps are involved, and the one shown in the simplest example. Usually Auger recombination is important when the carrier concentration is very high as a result of either high doping or high injection level.

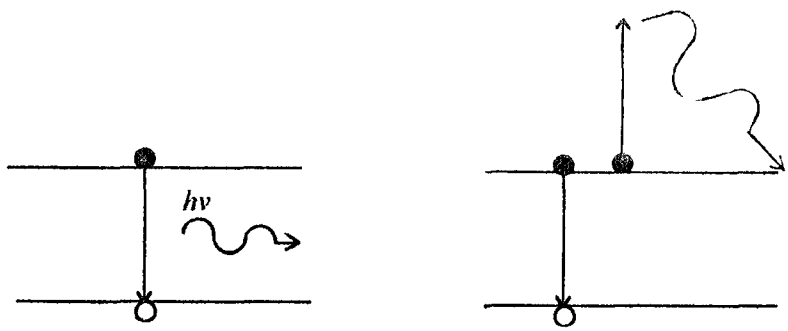


Figure 3.2 (a) Direct and radiative recombination, (b) Auger recombination.

Impurity atoms other than donors and acceptors and some types of crystal defects in semiconductor, introduce localized energy levels deep in the band gap away from the band edges. These levels act as stepping stones for electrons between conduction band and valance band, making a substantial enhancement in the recombination process. Depending on its location in the band gap, a deep level may act as an electron or a hole trap or a recombination center. An electron trap has a high probability of capturing a conduction electron and setting it free after sometime. Same process happens in a hole trap interacting with a hole. At a recombination center the probability of electron and hole captures are nearly equal.

3.4 Intermediate-Level Recombination (Indirect Transitions)

Indirect transitions process is characterized by the transition of an electron from conduction to valance band in steps. For an electron to reach the valance band, it must experience a change of momentum as well as energy to satisfy the conservation principles. The transitions takes place either by means of a single level or of several levels.

3.4.1 Single Level Recombination

There are electronic states deep in the otherwise forbidden gap that are created by defects or impurities. Here, the word DEEP indicates that the

states are away from the band edges and near the center of the forbidden gap. These states are known as RECOMBINATION CENTERS or TRAPS.

Single-level recombination consists of four steps:

1. An electron is captured by an empty center
2. An electron is emitted from an occupied center.
3. An unoccupied center captures a hole, and
4. An empty center emits a hole.

Consider a semiconductor with a density of recombination centers N_t located at an energy E_t. The probability that the center is occupied by an electron is given by

$$f_t^o = \frac{1}{1+e^{(E_t-E_f)/kT}} \tag{3.6}$$

The number of occupied centers is therefore $N_t f_t^o$, and the number of empty centers is $N_t\left(1-f_t^o\right)$. The superscript 'o' specifies the equilibrium condition.

By following the argument used in driving the direct-recombination rate, we find the capture rate of an electron by an empty center to be

$$R_1 = c_n n N_t\left(1-f_t\right) \tag{3.7}$$

where n is the electron density in the conduction band and C_n is the capture coefficient, which has a typical value of 10^{-18}cm^3/s. The electron-capture coefficient is the product of the thermal velocity V_{th} and the electron-*capture cross section* σ_{cn}, where σ_{cn} is a measure of the closeness of an electron to an empty center and has a typical value of 10^{-15}cm^2. A hole-capture cross section is defined in the same manner. The rate of emitting an electron to the conduction band from an occupied center is given by

$$R_2 = e_n N_t f_t \tag{3.8}$$

where e_n is the emission coefficient. By analogy, the capture and emission rates of holes by the centers may be written as

$$R_3 = c_p P N_t f_t \tag{3.9}$$

$$R_4 = e_p N_t (1 - f_t) \tag{3.10}$$

where c_p and e_p are hole capture and emission coefficient, respectively.

Under thermal equilibrium, the number of electrons emitted from the centers must be the same as that of the captured electrons, that is, $R_1 = R_2$. Equating Eqs. (3.7) and (3.8) and using $n = n_i e^{(E_f - E_i)/kT}$ we obtain

$$c_n n_i e^{(E_f - E_i)/kT} N_t (1 - f_t) = e_n N_t f_t \tag{3.11}$$

Furthermore, since

$$\frac{1 - f_t}{f_t} = e^{(E_t - E_f)/kT} \tag{3.12}$$

we have $p = n_i e^{(E_i - E_f)/kT}$

$$e_n = c_n n_i e^{(E_t - E_i)/kT} \tag{3.13}$$

Using the same procedure and $p = n_i e^{(E_i - E_f)/kT}$, we find the hole emission rate

$$e_p = c_p n_i e^{(E_i - E_t)/kT} \tag{3.14}$$

Since the capture and emission probabilities are independent of equilibrium and nonequilibrium conditions. Eqs. (3.13) and (3.14) are valid at nonequilibrium although they have been derived under the thermal-equilibrium condition. However, the probability of occupancy expressed by

Eq. (3.6) is not applicable at nonequilibrium because the Fermi level E_f is meaningful only at equilibrium.

Let us now consider the nonequilibrium case by applying an external source of energy e.g., a light source so that a generation rate G_L exists uniformly throughout the semiconductor. Under steady-state conditions, the electrons entering the leaving the conduction band in Fig 3.3 must be equal. This is called the *principle of detailed balance,* and it yields

$$G_L = R_1 - R_2 \tag{3.15}$$

Similarly, the detailed balance of holes in the valence band leads to

$$G_L = R_3 - R_4 \tag{3.16}$$

Equating Eqs. (3.15) and (3.16), we have

$$R_1 - R_2 = R_3 - R_4 \tag{3.17}$$

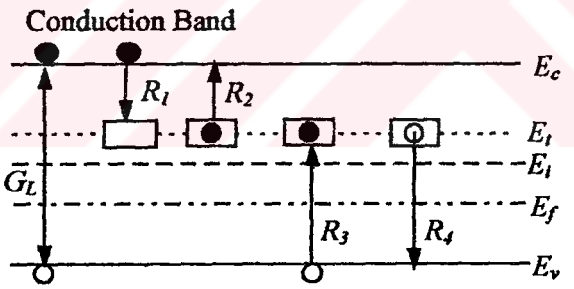


Figure 3.3.Generation and recombination processes under illumination.

We can now substitute Eqs. (3.7) to (3.10) into the foregoing expression to obtain

$$c_n n N_t (1 - f_t) - e_n N_t f_t = c_p p N_t f_t - e_p N_t (1 - f_t) \tag{3.18}$$

By assuming $c_n = c_p = c$ and using Eqs. (3.13) and (3.14), we can derive f_t from Eq. (3.18), yielding

$$f = \frac{n + n_i e^{(E_t - E_i)/kT}}{n + p + 2n_i \cosh\left[(E_t - E_i)/kT\right]} \tag{3.19}$$

Therefore, the net recombination rate is

$$U \equiv R_1 - R_2 = \frac{cN_t(pn - n_i^2)}{n + p + 2n_i \cosh\left[(E_t - E_i)/kT\right]} \tag{3.20}$$

From Eq. (3.20), we find that at equilibrium, that is at $pn = n_i^2$, the net recombination rate is zero. It is also interesting to note that the maximum recombination rate occurs when $E_t = E_i$. In other words, the most efficient recombination centers are located at or near the center of the forbidden gap. Away from the level E_i, the centers would be less effective because it is more probable to capture one type of carrier but less probable to capture the other type.

3.4.2 Multiple-Level Recombination

As shown in Figure 3.4 the basic mechanism is similar to that of single-level recombination differences are observed mainly at high injection level condition (i.e. where $\Delta n = \Delta p \approx$ majority-carrier concentration), where the asymptotic lifetime is an average of the lifetimes associated with all the positively charged, negatively charged, and neutral trapping levels.

At high-level injection,

$$\tau_p = \frac{1}{\sigma_{cp} V_{th} N_t} + \frac{1}{\sigma_{cn} V_{th} N_t} \tag{3.21}$$

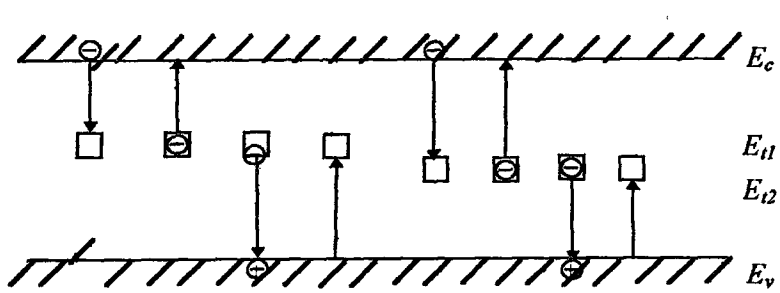


Figure 3.4 Multi -level recombination.

CHAPTER 4

MOS SOLAR CELLS

4.1 Introduction

Optical energy can be absorbed in a semiconductor if the photon energy is greater than the band-gap energy. The absorbed photons generate electron-hole pairs, which produce a photo current in a semiconductor or a pn junction. In the case of a junction, a potential difference is established across the space-charge layer. This process of converting optical energy into electric energy is known as the photovoltaic effect. The converter is known as the SOLAR CELL.

4.2 The Photovoltaic Effect

The photovolatic effect is a process by a which a voltage is produced at the junction of two different materials (e.g., a metal-semiconductor or a pn junction), through an incident photon flux. In a pn junction photons of sufficient energy incident upon the semiconductor produce hole-electron pairs. Some of these holes and electrons diffuse toward the junction and if they are created sufficiently close to it, have a high probability of reaching it before they recombine. At the junction they are separated by the barrier. If they are created at the *p*-side of the junction and diffuse toward the junction, the electrons will be swept across the junction into the *n*-side whereas the holes will be blocked by the barrier if the hole-electron pairs diffuse in from the *n*-side of the junctions, the holes are swept into the *p*-side by the barrier while the electrons are blocked.

The carriers which are swept across the barrier are the minority carriers in the region in which they are generated and their flow through the barrier constitutes reverse current. If there are no exterior connections to the device (open circuit condition) the charge which accumulates on either side of the

junction reduced the barrier height. This reduction causes the forward current to increase. The forward current results from the passage of thermally produced majority carriers across the barrier. An equilibrium condition is quickly established which results in an open circuit voltage intermediate between zero and full barrier voltage.

If the illumination is sufficiently intense to annihilate the barrier, the photovoltage has reached its saturation value.

In order to obtain a high photovoltaic efficiency the following requirements have to be met:

- The energy per photon has to be slightly greater than the band gap energy.
- The impurity concentration has to be high and temperature low.
- The surface reflectivity has to be small.

The product of photovoltage and photocurrent represents the net flow of energy from the solar cell to the external load, energy coming from the sun and converted from photon-energy to the electrical energy with in the solar cell.

4.3 Optical Absorption in a Semiconductor

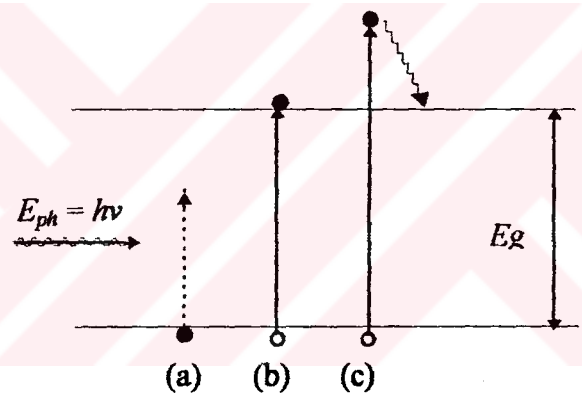
The unit energy of light, called a photon is hv, where v is the light frequency and h is Planck's constant. The wavelength of light λ is related to the frequency by

$$\lambda = \frac{c}{v} = \frac{hc}{E_{ph}} = \frac{1.24}{E_{ph}} \mu m \qquad (4.1)$$

where E_{ph} is the photon energy hv in electron volts and c is speed of light, that is, 3×10^{10} cm/s. When a semiconductor is illuminated, photons may or may not be absorbed, depending on the photon energy and the band-gap energy E_g. Photons with energy smaller than E_g are not readily absorbed by the

semiconductor because there is no energy state available in the forbidden gap to accommodate on electron (Figure 4.1a). Thus light is transmitted through and the material appears transparent. If $E_{ph} = E_g$, photons are absorbed to create electron-hole pairs, as shown in Figure 4.1b. When the photon energy is greater than E_g, an electron-hole pair is generated and, in addition, the excess energy $E_{ph} = E_g$ is dissipated as heat (Figure 4.1c).

Let us consider the nature of absorption for a semiconductor shown in Figure 4.2. The optical source provides monochromatic light with $hv > E_g$ and a flux F_{ph} or F in photons per square centimeter per second. As the light beam penetrates the crystal, the fraction of the photons absorbed is proportional to the intensity of the flux $F(x)$. Therefore, the absorbed photons within Δx are



Figu4.1 Optically generated electron-hole pairs in a semiconductor.

$$\alpha\, F(x)\, \Delta x$$

where α is a proportional constant called the absorption coefficient. From the continuity of light in Figure 4.2, we find

$$F(x+\Delta x) - F(x) = \frac{dF(x)}{dx}\Delta x = -\alpha F(x)\Delta x$$

or

$$-\frac{dF(x)}{dx} = \alpha F(x) \qquad (4.2)$$

The negative sign indicates decreasing intensity of the flux along x due to absorption. With the boundary condition $F = F_{ph}$ at x=0, we obtain the solution of Equation (4.2) as

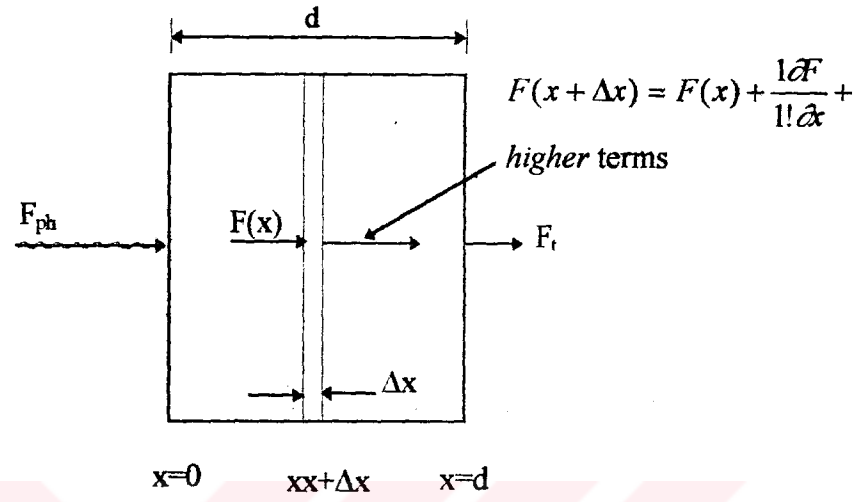


Figure 4.2 Optical absorption in a semiconductor.

$$F(x) = F_{ph}e^{-\alpha x} \tag{4.3}$$

Therefore, the fraction of light transmitted through the semiconductor is

$$F_t = F(d) = F_{ph}e^{-\alpha d} \tag{4.4}$$

where d is the thickness of the semiconductor. Since the absorption is determined by the photon energy, it is conceivable that α is a function of hv. Silicon absorbs photons with $\lambda \leq 1.1\,\mu m$.

4.4 The MOS Diode

The MOS consists of a parallel plate capacitor with one electrode a metallic plate, called the gate and the other electrode the silicon. The two electrodes are separated by a thin insulating layer of SiO_2. Such a structure is shown in Figure 4.3.

MOS diode is also known as the MOS capacitor.

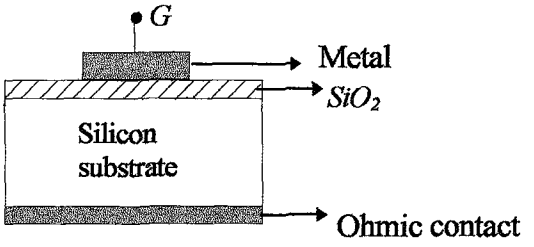


Figure 4.3 Structure of MOS Capacitor.

Consider the depletion condition in Figure 4.4. We have applied a small negative potential to the top metal contact which will put a small negative charge on this contact. The oxide layer prevents current flow but the effect of the negative charge is felt by the electrons in the *n*-type silicon. The negative charge tends to repel the free electrons from a region underneath the top contact, as shown, forming a depletion region. This is exactly the same sort of depletion region as in the pn junction. It is a region depleted of free charge carriers. Look at the MOS structure again. The top metal contact and the oxide layer together look like half of a capacitor structure. The semiconductor with its free charge carriers forms the 'other plate' of the capacitor. That's why the device is called an MOS capacitor.

Using the MOS capacitor for measuring properties of the MOS system the following properties can be obtained.

1. Surface band bending and depletion layer width in the silicon as a function of gate bias.
2. Voltage and field at avalanche breakdown in the silicon.
3. Doping profile in the silicon.
4. Interface trap level density as a function of energy in the band gap.
5. Interface trap capture probability for both electrons and holes as a function of energy in the band gap.
6. Lifetime in the bulk silicon.
7. Surface recombination velocity.
8. Oxide thickness.

9. Oxide breakdown field.
10. Charge configurations in the oxide such as oxide fixed charge and the charge at the interface between SiO_2 and another insulator deposited on top of it.
11. Nonuniformities in the oxide charge distribution and nonuniformities of surface potential caused by the discrete nature of charge in the oxide.
12. Work function differences between silicon and gate.
13. Ionic drift and polarization effects in SiO_2.
14. Band-to-band tunneling in the silicon and tunneling into SiO_2.
15. Diffusion of water into SiO_2.
16. Quantum effects in the inversion layer at low temperatures.
17. Results of thermally activated chemical reactions and electrochemical reactions in SiO_2.
18. Conductivity type of the silicon.
19. Dielectric constant of silicon.
20. Dielectric constant of SiO_2.
21. Properties of electron and holes types in SiO_2.

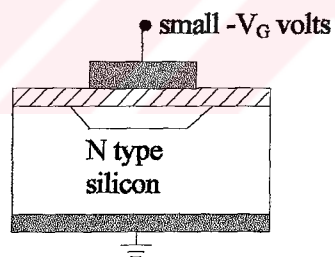


Figure 4.4 The ideal MOS diode for depletion condition.

The MOS capacitor also has been used in determining ways of controlling oxide fixed charge and interface trap level densities, effects of light on interface traps and surface charges, and in studying the effects of ionizing radiation on SiO_2. Internal photo emission measurements using the MOS capacitor have yielded information about the barrier height between the conduction bands of silicon and SiO_2 and about trapping centers distributed in the SiO_2 layer.

4.5 The Effect of Insulating Layer

Silicon has become the principal semiconductor material primarily because SiO_2 is film which be grown on it. Band gap of SiO_2 is 8.2 eV. These oxide films are dense, uniform and stable over wide range of temperatures. This allows to use of this oxide as a barrier to selectively mask against the diffusion or ion implantation of dopants. Furthermore, this oxide film and the Si-SiO_2 interface determine the electrical characteristics of devices built in the silicon substrate.

The insulating layer (SiO_2) has two effects.

1. Because of potential drop in the layer, the zero bias barrier height is higher than it would be in Schottky diode.

2. When a bias is applied, part of the bias dropped across the insulting layer so that the barrier height is a function of bias voltage. The effect of this bias dependence of the barrier height is to change the shape of current-voltage characteristics.

The oxide layer protects the surface from environmental contamination, and acts as a barrier against the diffusion of impurities into the semiconductor underneath, thus improves device performance.

The various charges that may be present in insulating layer are illustrated in Figure 4.5.

1.Fixed Oxide Charge Q_f is fixed and cannot be charged or discharged over a wide variation of ψ_s; it is located within the order of 30A° of the Si-SiO_2 interface; its density is not greatly affected by the oxide thickness or by the type or concentration of impurities in the silicon; it is general positive and depends on oxidation and annealing conditions, and on silicon orientation. They are immobile under applied electric field. This charge cannot be altered by the application of the bias to the gate and so has come to be known as the OXİDE FİXED CHARGE.

The magnitude of Q_f depends on the crystallographic orientation of the silicon and on the silicon and on the ambient (oxidizing or inert) in which the wafer is placed during last high temperature treatment used in processing.

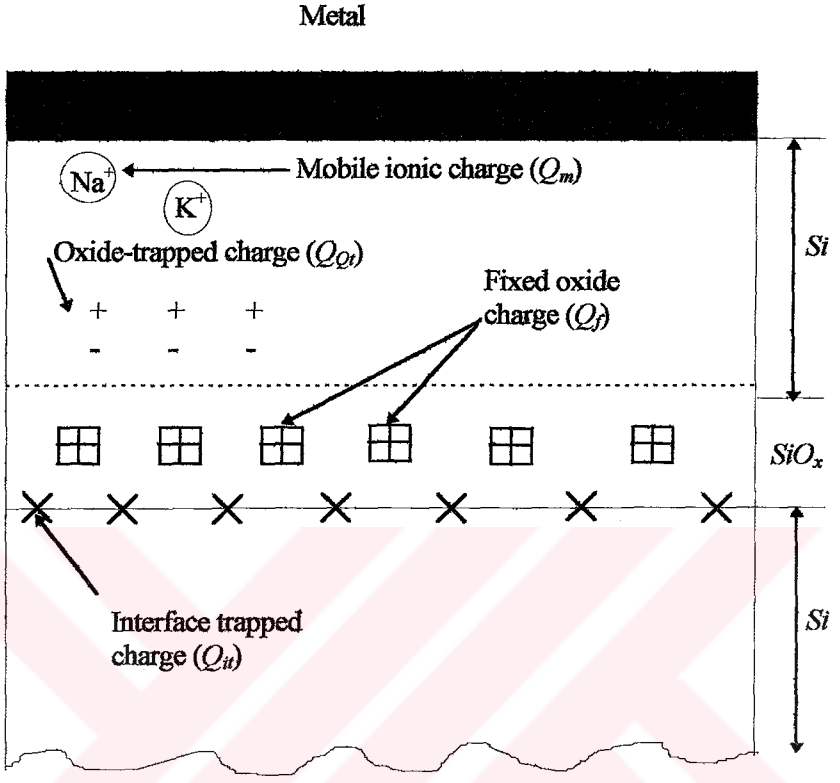


Figure 4.5 Charges associated with thermally oxidized silicon.

Q_f can be minimized by annealing in an inert ambient such as argon at a temperature in excess of 900°C

Even if the work functions of the metal and semiconductor are equal presence of Q_f will give a nonzero flatband voltage, as shown in Figure 4.6. The (+) charge in the SiO_2 attracts electrons to the silicon surface, causing the bands in the silicon to bend. To eliminate this band bending, it is necessary to apply a negative voltage to the gate in order to place a charge equal to Q_f in magnitude but opposite sign on this electrode. In consequence

$$V_{flatband} = V_{FB} = -\frac{Q_f}{Cox} \qquad (4.5)$$

Figure 4.6b shows how to band diagram changes under flatband conditions. It is important to note that the terms "flatband" refers to the bands in the silicon; when charge is present in the oxide, flatband conditions in the silicon can be achieved only when there is a potential drop and hence band bending across the oxide.

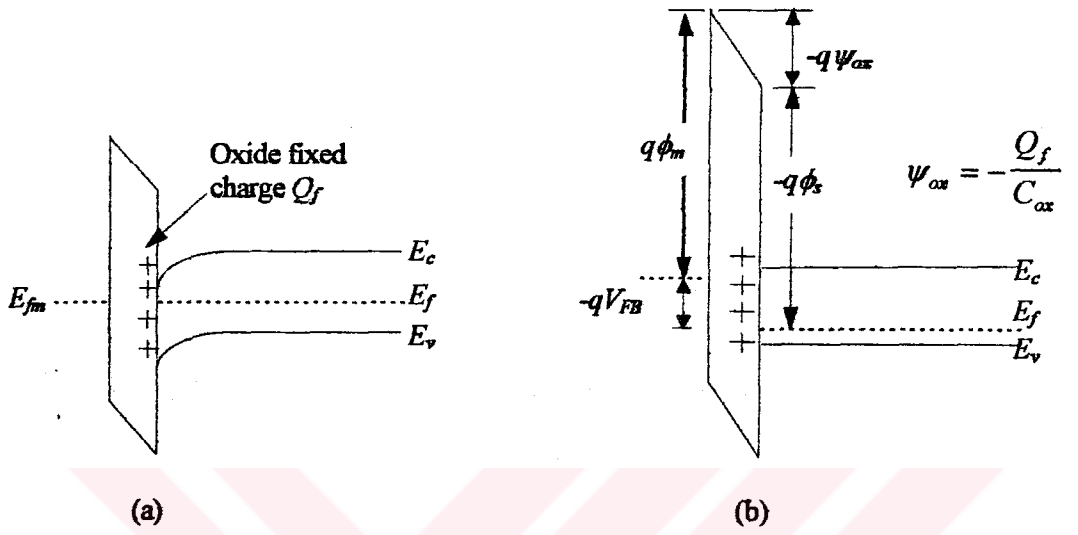


Figure 4.6 Computing V_{FB} when oxide fixed charge Q_f is present: (a) $V_G = 0$; (b) $V_G = V_{FB}$

<u>2.The Mobile Charge Q_m</u> is primelary due to the presence of alkali ions like Na^+, K^+, and Li^+. These ions are present in the cleaning solutions and other reagents as well as in the quartz tube used in oxidation process. These charge can move through the oxide at elevated temperature causing change in the flatband voltage with time.

Extremely low concentrations of Na^+ ions in the oxide were found to give significant instability in V_T (threshold voltage).

Na^+ ions are small and can move freely through the relatively open structure of SiO_2 in response to an applied gate bias. If gate bias positively the ions move toward the Si-SiO_2 interface, where they shift the flat band voltage in the same manner as Q_f. Application of a negative bias to the gate attracts the Na^+ ions toward the gate, reducing their influence on V_{FB} and V_T.

<u>3.The Oxide-Trapped Charge Q_{ot}</u> may be either (-) or (+) due to electrons or holes trapped in the bulk of the oxide. The traps may result from ionizing

radiation from avalanche injection produced by hot electrons or from other similar process.

The band gap of SiO_2 is roughly 8eV. If a photon with energy greater than this is incident on an SiO_2 layer, electron-hole pairs are photogenerated in the layer. Electrons are quite mobile in SiO_2, but holes are relatively immobile and are easily trapped. During etching and thin-film deposition steps required in processing silicon wafers are frequently exposed to "soft" (i.e. low energy) x rays. As a result large quantities of electrons and holes are photogenerated in oxide layers and many of these holes are trapped. The trapped holes constitute a positive charge $Q(x)$, which shifts V_T..

The Q_{ot} can be completely removed by annealing the wafers at temperatures in the range 300 to 400°C after exposure to radiation. Q_{ot} is therefore relatively little importance in complete devices.

4.*Interface Trapped Charge* Q_{it} is mainly due to the breaking of covalent band at the Si-SiO_2 interface. The probable origin of this charge lies in oxidation-induced structural defects; metallic diffusing to the interface, and other defects caused by radiation or similar band breaking process. The charge is in electrical communication with the underlying silicon and has often been referred to as fast surface states or interface states charge.

4.6 The MOS Capacitor with Applied Bias and Band Diagrams

4.6.1 Metal and Semiconductor Work Functions

(a) Work function of a metal:

Conduction electrons can escape from a metal into free space only If they can overcome the thermionic work function of the metal (ϕ_m) which is defined as the energy required to remove an electron from the Fermi level of the metal to the vacuum energy level. The metal work functions is sensitive to surface contamination (shown in Figure 4.7).

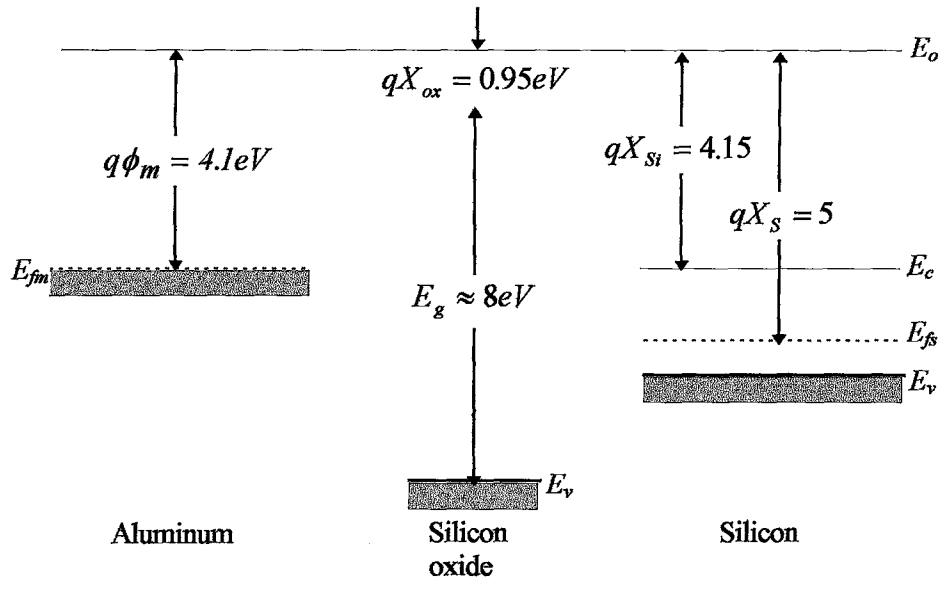


Figure 4.7 Energy levels in three separated components that form an MOS system; aluminum, thermally grown silicon, and *p*-type silicon containing $N_a \sim 2\text{x}10^{15}$ cm^{-3}.

(Although recent measurements indicate E_g in SiO_2 to be ~9 eV, many experimental data appear to be consistent with the 8 eV value that we will use)

(b) Work function of a semiconductor:

The escape of electrons from a semiconductor into free space requires a thermionic work function (ϕ_s) which is defined as the energy required to remove an electron from the Fermi level of the semiconductor to the vacuum energy level (shown in Figure 4.7).

$$\phi_s = x_s + E_g/2q + \phi_F \qquad (4.6)$$

where x_s electron affinity of the semiconductor, i.e., the energy required to remove an electron from the bottom of the conduction band to the vacuum energy level.

ϕ_F = Fermi Potential

$$\phi_F = -(E_F - E_i)/q;$$

for a *n*-type semiconductor $\phi_F < 0$

for a *p*-type semiconductor $\phi_F > 0$

The dependence of ϕ_S upon the impurity concentration of the semiconductor is a result of the concentration dependence of ϕ_F.

(c) Metal-semiconductor work function

The barrier height of a metal-semiconductor system (ϕ_{ms}) can be predicted by two models, depending upon the magnitude of the surface state density.

- **Surface state model:** In this model it is assumed that the surface state density of the semiconductor surface is large. In this case the barrier height is independent of the properties of the metal and of the impurity concentration of the semiconductor. It is;

for an *n*-type semiconductor $\phi_{ms} \approx (2/3)E_g$

for a *p*-type semiconductor $\phi_{ms} \approx (1/3)E_g$

The temperature dependence of ϕ_{ms} is similar to that of the energy gap E_g..

- **Work function difference model:** In this model it is assumed that the surface state density is negligible and that the barrier height is determined by the difference in the work functions of metal (ϕ_m) and semiconductor (ϕ_s).

$$\phi_{ms} = \phi_m - \phi_s \qquad (4.7)$$

In this case the barrier height depends upon the nature of the metal and the impurity concentration of the semiconductor.

This model holds only qualitatively. Deviations of observed values of ϕ_{ms} from this ideal model are due to various effects, as surface states, image forces, contamination, etc. The work function model holds better, on a relative basis, for covalent semiconductors (e.g., Si) than for other semiconductors (e.g., GaAs).

4.6.2 Ideal MOS Diode

The metal-oxide-semiconductor (MOS) structure is shown in Figure 4.8. We have assumed that the energy bands are flat and the work functions are the same for all three parts. As defined in 4.6.1, the work function specifies the work required to bring an electron from the Fermi level to the vacuum level. It should be noted that the band gap is 8 eV for SiO_2 and 1.1 eV for Si so that the vertical dimensions of the figure are not in proportion. But the diagram is correct qualitatively. As three components are brought into contact, the Fermi levels align.

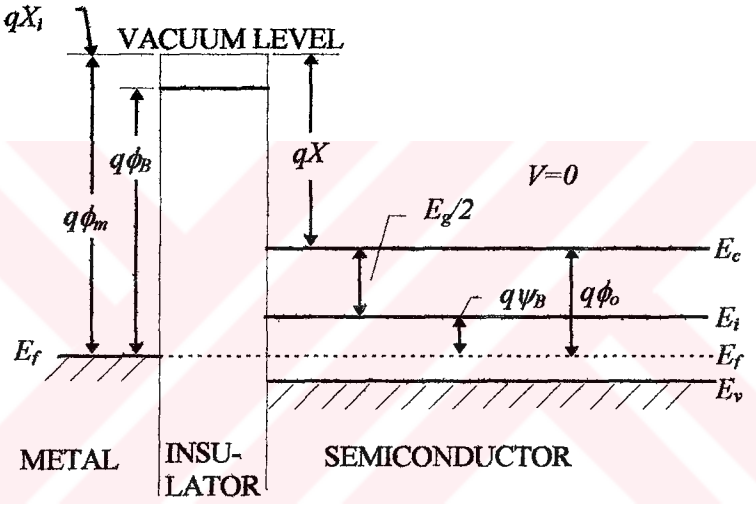


Figure 4.8 Energy-band diagrams of ideal MIS diodes at V=0 for *p*-type semiconductor.

This is an idealized situation, where the energy bands remain flat because the work functions are assumed to be the same so that there is no charge transfer upon contact. We are also assuming that there is no charge located inside the oxide or at the interface between the oxide and the semiconductor. The bands in the semiconductor thermal equilibrium conditions are flat and horizontal. This is known as the flat-band condition. Physically there are no electric fields (or charge distributions) which will bend the bands in this thermal equilibrium case. In reality there may be charges in the oxide which will cause band bending in the semiconductor, even under thermal equilibrium conditions.

The energy-band diagram of an ideal MOS structure for V=0 shown in Figure 4.8. An ideal MOS diode is defined as follow:

(1) At zero applied bias, energy difference between the metal work function ϕ_m and the semiconductor work function is zero, or the work-function difference ϕ_{ms} is zero

$$\phi_{ms} = \phi_m - (x + \frac{E_g}{2q} - \Psi_B) = 0 \qquad \text{for } n\text{-type} \tag{4.8a}$$

$$\phi_{ms} = \phi_m - (x + \frac{E_g}{2q} + \Psi_B) = 0 \qquad \text{for } p\text{-type} \tag{4.8b}$$

where ϕ_m is the metal work function, x the semiconductor electron affinity, x_i the insulator electron affinity, E_g the bandgap ϕ_B the potential barrier between metal and the silicon oxide and ψ_B the potential difference between the Fermi level E_f and the intrinsic Fermi level E_i. In other words, the band is flat (flat-band condition) when there is no applied voltage **(2)** The only charges that can exist in the structure under any biasing conditions are those in semiconductor and these with the equal but opposite sign on the metal surface adjacent to the SiO_2 .**(3)** There is no carrier transport through the insulator under dc biasing conditions, or the resistivity of the insulator is infinity.

It is useful to introduce two parameters related to the doping level in the substrate. The first of these is the energy difference $q\phi_o$ between the conduction band edge and the Fermi level measured deep in the "bulk" substrate well away from the influence of the gate electrode. From $n_o = N_c \exp\left(E_f - E_c\right)/kT$;

$$\phi_o = \frac{kT}{q} \ln \frac{N_c}{n_o} \tag{4.9}$$

where n_o is the equilibrium electron concentration in the substrate.

A second useful parameter is the energy difference $q\psi_B$ between the actual Fermi level E_f and the intrinsic Fermi level E_i. For a p-type substrate with

$$\psi_B = \frac{kT}{q} \ln \frac{N_A}{n_i} \tag{4.10}$$

similarly, for an n-type substrate with donor doping N_D,

$$\psi_B = \frac{kT}{q} ln \frac{n_i}{N_D} \tag{4.11}$$

in this case ψ_B has been defined as a negative quantity.

When a positive bias applied to the gate, holes are repelled from the semiconductor surface, so the bands bend as shown in Fig. 4.9.

As the hole leave the surface, ionized acceptor ions are left behind, forming a surface depletion region. The applied bias V_G can be viewed as splitting up into two parts: a potential drop ψ_s across the semiconductor and a potential drop ψ_{ox} across the insulator. These quantities are defined to be positive when the direction of band bending is that shown in Fig. 4.9.

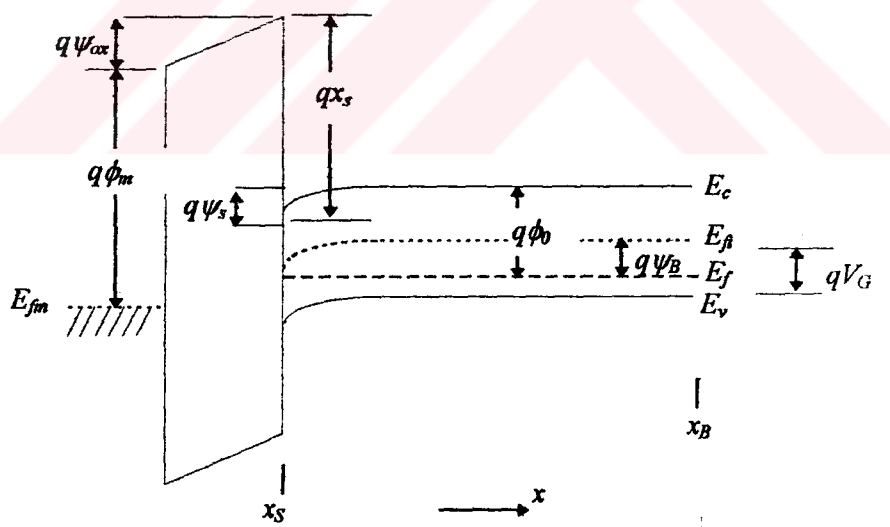


Figure 4.9 MOS capacitor band diagram for positive applied bias V_G.

$$V_G = \psi_s + \psi_{ox} \tag{4.12}$$

The surface potential is the voltage across the semiconductor, using the semiconductor as the reference, ψ_s corresponds to the potential at the silicon

surface, i.e., the silicon-silicon oxide interface. Therefore, It is called the SURFACE POTENTIAL.

The carrier densities under thermal equilibrium are given

$$n = n_i e^{(E_f - E_i)/kT} \tag{4.13a}$$

$$p = n_i e^{(E_i - E_f)/kT} \tag{4.13b}$$

From these equations we find that $n>p$ for $E_f>E_i$ and the semiconductor is n type. Similarly, we have $n<p$ for $E_f< E_i$ in a p-type semiconductor.

It should be noted that the oxide being a good insulator, does not allow current conduction between the metal and semiconductor even under bias. The conduction of zero current corresponds to a constant Fermi level inside bulk semiconductor. Physically, a flat Fermi level is equivalent to the state of thermal equilibrium where we have $n_p=n_i^2$. This condition prevails even under external bias in the MOS structure.

4.6.3 Accumulation, Depletion and Inversion

Depending on the polarity of the applied voltage and its magnitude, it is possible to realize three different surface conditions:

1. Carrier accumulation
2. Carrier depletion
3. Carrier inversion

The case of a MOS capacitor fabricated on a *p*-type substrate is treated here. The characteristics of a similar device fabricated on a *n*-type substrate can be treated in an analogous manner.

Carrier Accumulation:

When the hole density just below the silicon surface is greater than the equilibrium hole density in the bulk, we have the condition of carrier accumulation. This condition is realized by applying a negative voltage at the metal electrode. The resulting negative surface potential ψ_S produces an upward bending of the energy-band diagram, as shown in Figure 4.10(b). The bands near the interface in the semiconductor, now bend upward. There is no current flow through the oxide so the Fermi level in the semiconductor remains constant. Since E_f remains constant, the band bending leads to a larger E_i-E_f near the surface. According to equation (4.13), we have a higher hole density and a lower electron density at the surface compared with that of the bulk consequently, holes are accumulated at the surface, and the surface conductivity is increased. The negative charge on the metal Q_M is balanced by the positive hole charge Q_S (the total charge per ünit area stored in the semiconductor) (Figure 4.10 (c)) in this instance.

The high concentration of holes near the accumulated silicon surface can be through of as forming the second electrode of a parallel-plate capacitor with the gate electrode as shown in Fig. (4.10d). Since the accumulation layer is in direct ohmic contact with the *p*-type substrate, the capacitance of the structure under accumulation conditions must be approximately equal to $\varepsilon_{ox} A/T_{ox}$, where A is the area of the gate electrode, T_{ox} is the oxide thickness.

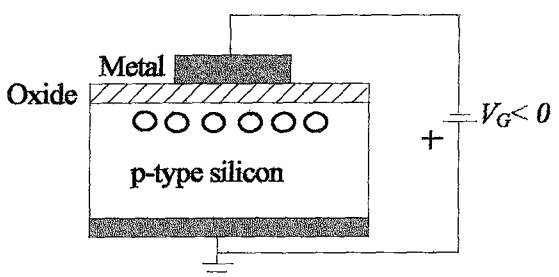
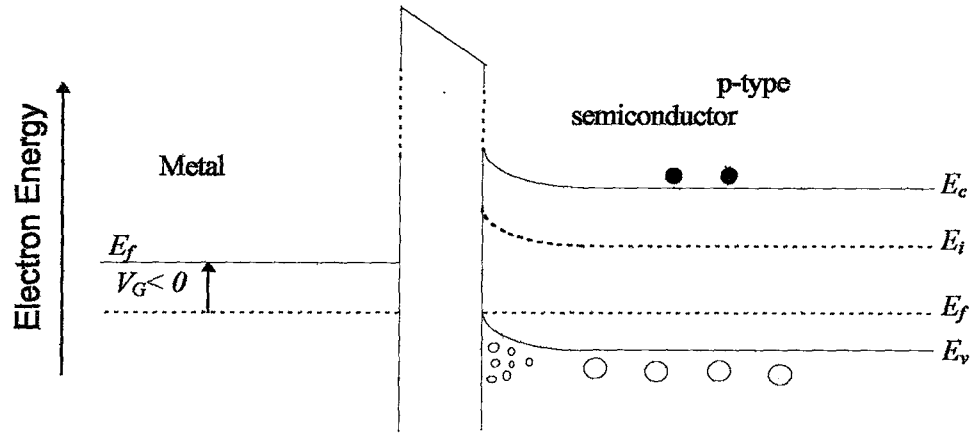
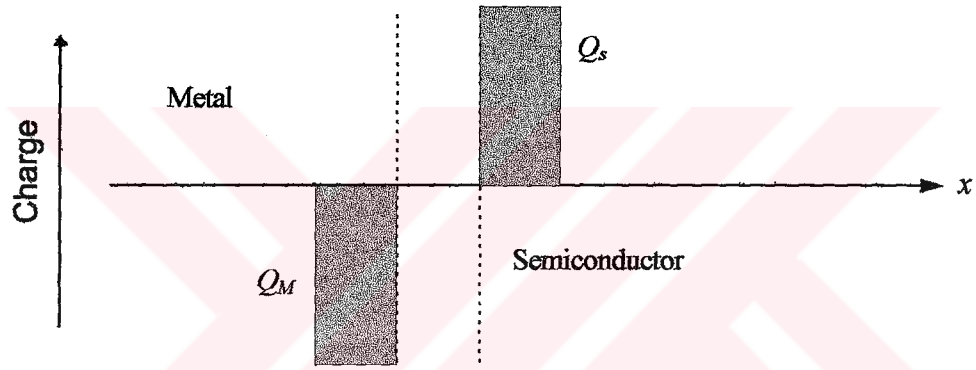


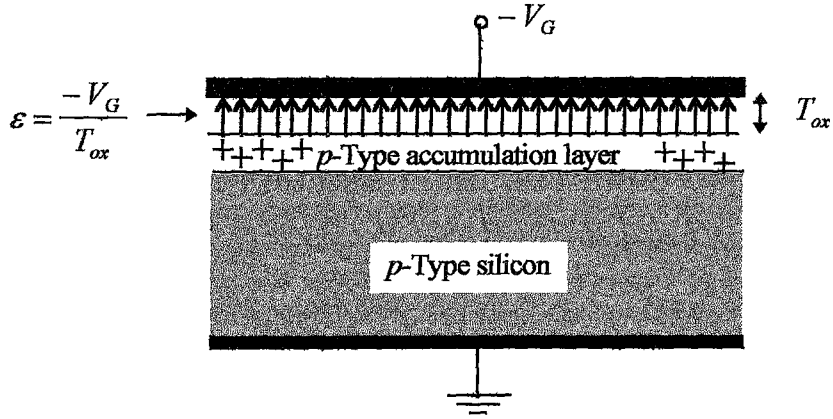
Figure 4.10 (a) Accumulation



(b) Energy band diagram



(c) Charge distribution



(d) Surface accumulation layer

Figure 4.10 Ideal MOS diode in accumulation.

Carrier Depletion

When a small positive V_G is applied the surface potential is positive and the energy bands bend downward, and a depletion of the majority carrier holes at the oxide-semiconductor interface. This is shown in Fig. 4.11a together with the relevant band diagram in Fig .4.11b.

With an applied positive potential the Fermi level in the metal moves downwards from its thermal equilibrium position, as shown. The voltage drop across the oxide is reflected by the slope in the oxide band energy, and the semiconductor bands now bend near the oxide-semiconductor interface. Remembering that holes 'float' and electrons 'sink' under drift conditions it is clear that with the band bending shown, holes will move away from the interface resulting in a depletion region. The charge conditions are shown in Fig. 4.11c. The uncovered (negative) donor charge (per unit area) is $-qN_AW$ and this just balances the positive charge per unit area Q_M on the metal electrode (assuming no other charge source are present). Note that the Fermi level in the semiconductor is flat and horizontal, as expected, since no current can pass through the oxide layer.

The total charge per unit area Q_S is given by

$$Q_S = Q_B = -qN_A\, w \tag{4.14}$$

$$\psi_S = \frac{kT}{q} ln \frac{N_A}{ni} = \psi_B \tag{4.15}$$

where w is the width of the depletion layer. The symbol Q_B *(ionized acceptor ions in the depletion region)* is defined as the *bulk charge* in the semiconductor, and negative sign specifies the polarity of charge. The relationship between ψ_S and w can be obtained by solving Poisson's equation using the depletion approximation. The result is

$$\psi_S = \frac{qN_A w^2}{2\varepsilon_S} \tag{4.16}$$

where ε_S is the permittivity of the semiconductor.

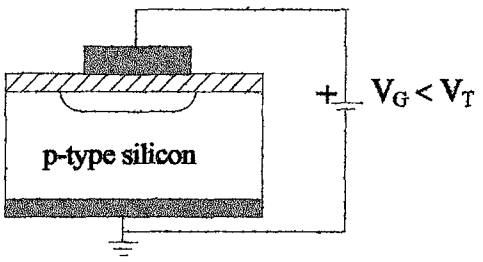
Since the magnitude of the charge density per unit area in the surface depletion region will be equal to the acceptor doping concentration times the electronic charge times the width of the surface depletion region, increasingly positive gate-to-substrate voltage will tend to increase both Q_S and *w*. As the width of the surface depletion region increases the capacitance from gate to substrate associated with the MOS capacitor structure will decrease, because the capacitance associated with the surface depletion region will add in series to the capacitance across the gate insulator as shown in Fig.4.11d. Thus total capacitance per unit area from gate to substrate under depletion conditions is given by

$$C(V_G) = \left(\frac{1}{C_{ox}} + \frac{1}{C_{SD}(V_G)} \right)^{-1} \tag{4.17}$$

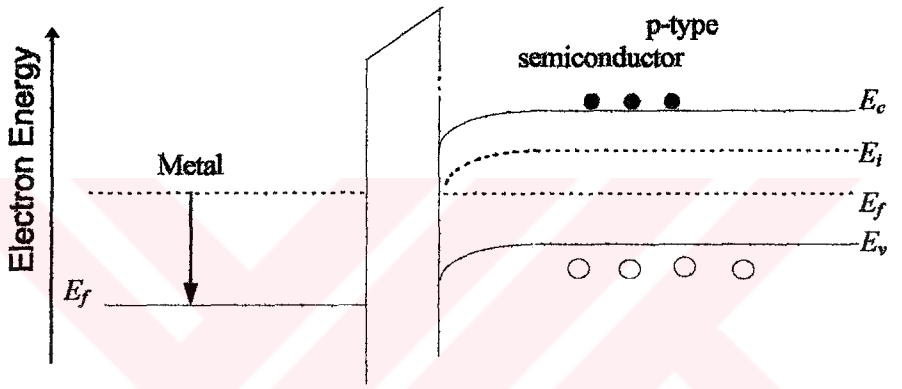
where C_{ox} is the oxide capacitance per unit area, $\varepsilon_{o\,x} / T_{ox}$, and C_{SD} is the capacitance per unit area associated with the surface depletion region. Then C_{SD} can easily be shown to be

$$C_{SD} = \frac{\varepsilon_s}{w} \tag{4.18}$$

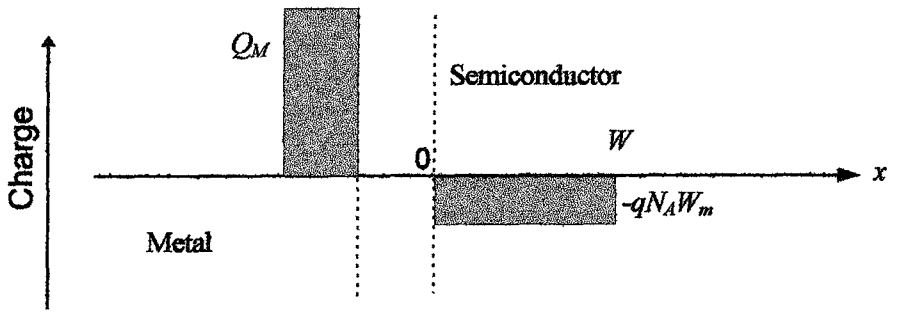
where ε_S is the dielectric constant of silicon and *w* is the width of the surface depletion region, which will be a function of the applied gate voltage. It should be noted that Eqn. (4.16) will be valid only when the amount of charge that might be trapped in surface states at the silicon-silicon dioxide interface is independent at the surface potential.



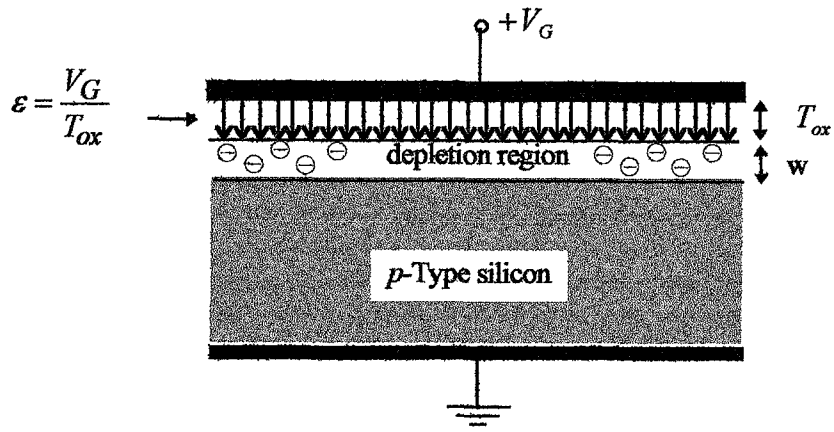
(a) Depletion



(b) Energy band diagram



(c) Charge distribution



(d) Surface depletion layer

Figure 4.11. Ideal MOS diode in depletion.

Carrier Inversion

If now increase the positive potential on the metal electrode to a value above the threshold voltage V_T, the semiconductor surface will invert and an (electron) inversion layer will reside at the interface. Fig. 4.12 illustrates the MOS diode in the inversion condition. With the increased positive potential the Fermi level in the metal is depressed even further. The greater voltage drop across the oxide is reflected in the greater slope in the oxide energy band, and there is even greater band bending in the semiconductor. In fact, the band bending in the semiconductor is so great that the intrinsic Fermi level has crossed the Fermi level. The electron concentration as a function of E_f -E_I is given by equation 4.13a.

$$n = n_i \exp(E_f - E_I) / kT$$

and since

$$E_f - E_I > 0 \qquad (4.19)$$

then

$$n > n_i \qquad (4.20)$$

$$p < n_i \tag{4.21}$$

and the surface of the semiconductor is inverted (there are more electrons than holes, but we're in *p*-type material). The thickness of the inversion layer is very small, typically 1-10nm.

The depletion-layer width w_m in this inversion case, w_m standing for maximum depletion-layer width. The reason for this is once the inversion layer has formed the depletion-layer width reaches a maximum. Any further charge increase appears in the inversion -layer charge only.

Fig.4.12c shows the positive top metal electrode charge Q_M being balanced by the negative inversion-layer and depletion-layer charges, i.e.

$$Q_M = -qN_A W + Q_n \tag{4.22}$$

$$Q_S = Q_B + Q_n = -qN_A W + Q_n \tag{4.23}$$

where Q_n is the charge density per unit area in the inversion layer.

The value of V_G that must be applied to just create a condition of strong inversion at the silicon surface is known as the *threshold voltage* V_T, and is one of the most important parameters describing any MOS capacitor. To obtain strong inversion, we need n_s=N_A so

$$\psi_S = \frac{2kT}{q} \ln \frac{N_A}{n_i} = 2\psi_B \tag{4.24}$$

The depletion region width at threshold is therefore given by

$$W_{\max} = \sqrt{\frac{2\varepsilon_S (2\psi_B)}{qN_A}} \tag{4.25}$$

So the ionized acceptor charge per unit area Q_B stored in the depletion region is given by

$$Q_B = -qN_A W_{max} = -\sqrt{2\varepsilon_S qN_A(2\psi_B)} \tag{4.26}$$

Although at threshold the electron concentration at the silicon surface is equal to the acceptor ion concentration, through most of the depletion region n is negligible compared to N_A. At threshold it is therefore reasonable to assume $Q_S=Q_B$, so

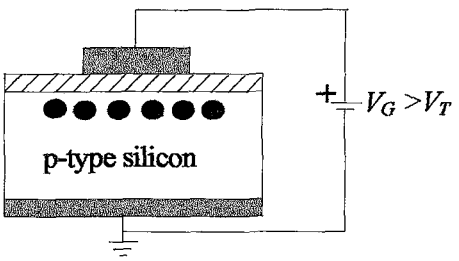
$$V_T = \psi_s + \psi_{ox} = 2\psi_B + \sqrt{\frac{2\varepsilon_s qN_A(2\psi_B)}{C_{ox}}} \tag{4.27}$$

At this point it is worth summarizing the surface condition,

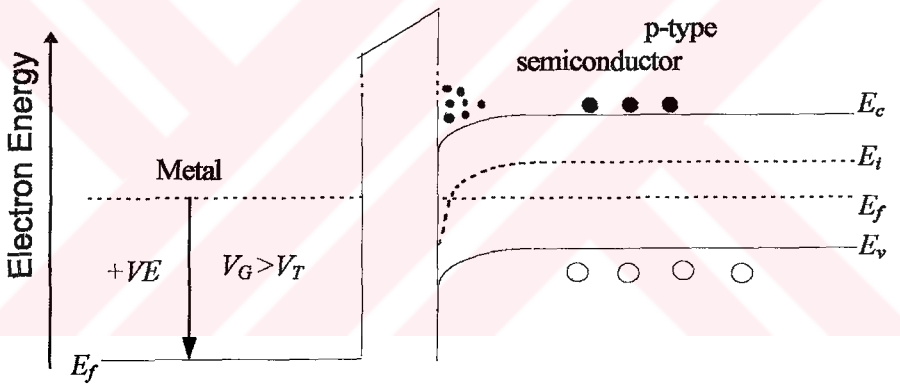
$\psi_S<0$	the surface is accumulation
$\psi_S=0$	flat-band condition.
$0<\psi_S<\psi_B$	the surface is depleted.
$\psi_S=\psi_B$	midgap with $n_s=p_s=n_i$ (intrinsic concentration).
$\psi_S>\psi_B$	the surface becomes inverted
$\psi_B<\psi_S<2\psi_B$	the surface only in weak inversion.
$\psi_S>2\psi_B$	the surface becomes strongly inverted.

As shown in Fig. 4.12d, the width of the surface depletion region for a MOS structure in equilibrium will remain virtually constant after the formation of a surface inversion layer, even if the gate voltage is made more positive. Small variations in the width of the surface depletion region around its maximum value can occur, however, if a nonequilibrium situation exists where the charge density in the inversion layer is unable to follow a high-frequency small-signal ac voltage applied to gate electrode, superimposed on the dc bias. Since the charge density in the inversion layer may or may not be able to follow the ac variation of the applied gate voltage it follows that the capacitance under inversion conditions will be a function of frequency. In general when a surface inversion layer is present, the gate-to-substrate capacitance of the MOS capacitor structure, for low-frequency ac signals, will be equal to the dielectric capacitance $C_{ox}A$. For high-frequency signals, the observed capacitance will be equal to the series combination of the dielectric capacitance and the capacitance associated

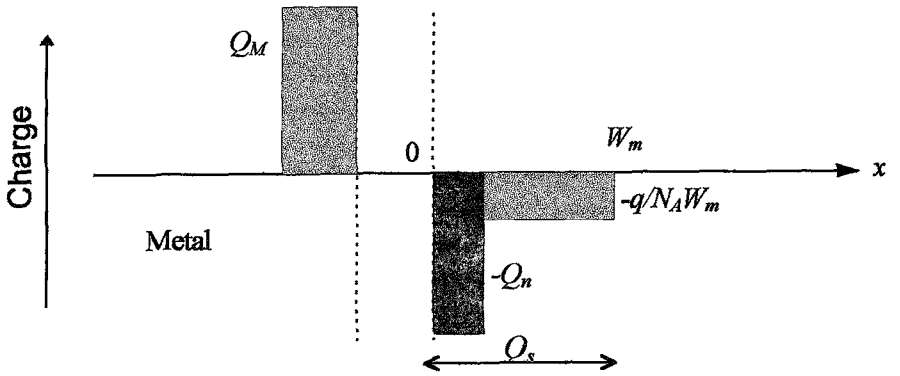
with the surface depletion region at its maximum width. Fig.4.12e shows typical capacitance versus voltage relationships for MOS capacitors fabricated on *p*-type silicon substrate.



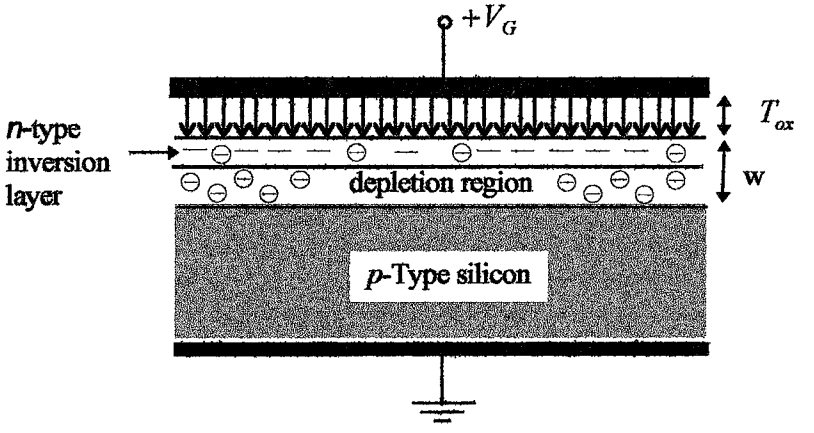
(a) Inversion



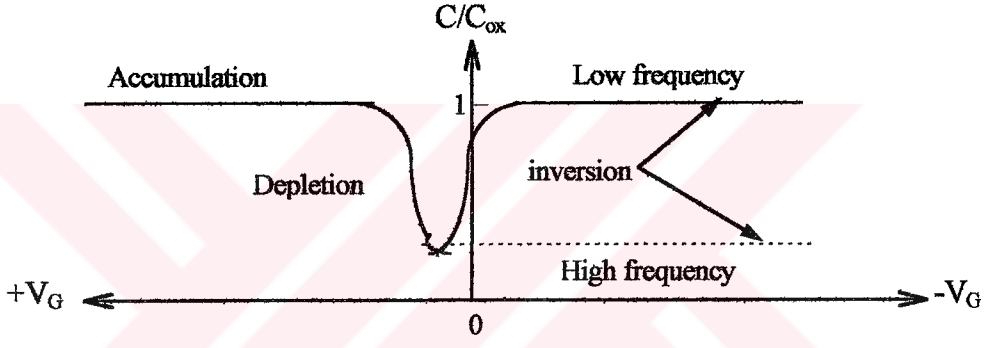
(b) Energy band diagram



(c) Charge distribution



(d) Surface inversion layer



(e) Capacitance- Voltage relationship for a MOS capacitor fabricated on p-type silicon substrate

Figure 4.12 Ideal MOS diode in inversion.

4.7 Solar Cell Equivalent Circuit

By connecting a load across the terminals of a solar cell a current I_L can flow through the load and develop a voltage V_L across it. The values of V_L and I_L, besides depending on the nature of the load, will be related to the photogenerated current I_p and properties of MOS diode. These relationships and properties can be established by reference to the simple equivalent circuit shown in Fig. 4.13, where imperfections in the diode leading the current leakage are represented by shunt resistance R_{sh} and parasitic resistance effects are represented by Rs. From Fig. 4.13, it is seen that

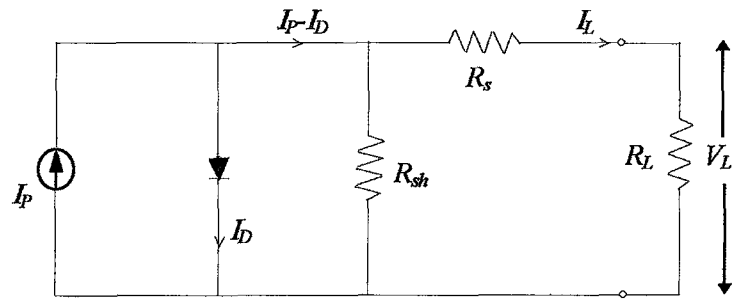


Figure 4.13 Simple equivalent circuit of solar cell.

$$I_L\left(1+\frac{R_s}{R_{sh}}\right)=I_P-I_D-\frac{V_L}{R_{sh}} \tag{4.28}$$

which shows that both diode current and voltage are effected by the presence of R_s and R_{sh}.

It is important for R_s to be small and for R_{sh} to be large. Typical desired values for silicon cells are $R_S<0.5\ \Omega$, $R_{sh}>500\Omega$.

The actual operating point of a given solar cell *I-V* characteristics is determined by the value of the load resistance R_L such that biasing occurs at the maximum power (I_m, V_m) shown in Fig.4.14. The energy conversion efficiency can be described by

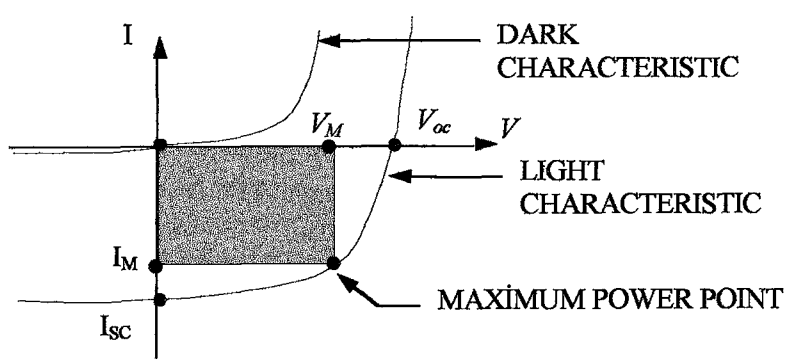


Figure 4.14 Solar cell I-V characteristics.

$$\eta=\frac{I_m V_m}{p_i A} \tag{4.29}$$

where p_i is the incident solar power density and A is the active area of solar cell. Defining the ratio of I_m, V_m to I_{sc}, V_{oc} as the fill factor "FF", a further expression for η can be written as where I_{sc} is the short circuit current, V_{oc} is the open circuit voltage.

$$\eta = \frac{(FF) I_{sc} V_{oc}}{p_i A} \tag{4.30}$$

4.8 Important Material Parameters for Solar Cell Design

To relate the terminal properties of solar cell, designer should examine some parameters for getting high efficiency.

4.8.1 Energy Gap

The energy gap of pure silicon is accurately known. At room temperature, 300 K it is 1.120 eV. In the range near and somewhat above room temperature where solar cells are usually operated the energy gap decreases linearly with temperature as described by

$$E_g = 1.120 - 2.8 * 10^{-4}(T - 300) \tag{4.31}$$

4.8.2 Intrinsic Carrier Concentration

The intrinsic carrier concentration is instrumental in determining the dark saturation current and hence open circuit voltage of a solar cell. Its variation with absolute temperature is given by

$$n_i = 3.87 * 10^{16} T^{3/2} exp(-E_g / kT) \tag{4.32}$$

where E_g=1.120eV and k is Boltzmann's constant. A room temperature this expression gives n_i=1.37*10^{10}. It increases by a factor of 2.23 in the next 10K.

4.8.3 Mobilities and Diffusion Coefficients

At low electric field the drift velocity V_d is proportional to the electric field strength ε, and the proportionality constant is defined as the mobility in cm^2 / V-s or

$$V_d = \mu\varepsilon \tag{4.33}$$

For nonpolar semiconductors, such as Ge and Si, the presence of acoustic phonons and ionized impurities results in carrier scattering which significantly effects the mobility.

The electrons and hole mobilities in pure silicon are given by

$$\mu_n = 1360\left(\frac{T}{300}\right)^{-2.42} \tag{4.34}$$

$$\mu_p = 495\left(\frac{T}{300}\right)^{-2.29} \tag{4.35}$$

in doped silicon these parameters are described by impurity scattering, falling roughly a factor of 10 as the impurity concentration increases from 10^{16} to $10^{19}/cm^3$. At higher donor or acceptor concentrations, the semiconductor behaves "metallic" and mobilities assume nearly constant values, $\mu_n = 90cm^2/V\text{-}s$ and, $\mu_p = 48cm^2/V\text{-}s$.

The carrier diffusion coefficient (D_n for electrons and D_p for holes) is another important parameter associated with mobility. The diffusion cefficient D depends on temperature and impurity concentration. Under low-concentration conditions, D becomes independent of impurity concentrations. (In low concentration conditions, the impurity concentration is less than the intrinsic carrier concentration at the diffusion temperature for example, at 1100 ^{0} C, $n_i = 10^{19}$ cm^{-3} . In a limited temperature range and under low-concentration conditions, the diffusion coefficient can be described by

$$D(T) = D_o \exp(-\Delta E / kT) \qquad (4.36)$$

where D_o is the diffusion coefficient extrapolated to infinite temperature, and ΔE is the activation energy of diffusion.

The output of a solar cell is derived from the diffusive flow of minority carriers to some form of collecting junction so the diffusion coefficient *D* is more direct concern than the mobility. They are connected by Einstein relation $D=\mu kT/q$.

4.8.4 Minority Carrier Lifetime

The minority carrier lifetime, the mean time interval between generation and recombination of change carrier, is a major property that is fundamental in determining the effectiveness of a semiconductor as a photovoltaic candidate. By a recombination process excess electrons and holes in a semiconductor recombine and tend to restore the system to the thermal equilibrium condition given by

$$pn = n_i^2 \qquad (4.37)$$

The lifetime (τ) also depends upon the quality of the starting material and upon many details of the cell fabrication.

The photogenerated carriers in the absorbed semiconductor must be able to move across that region of the junction. Carriers that recombine before arriving at the junction are lost the photovoltaic effect and cannot take part in the generation of photocurrent. Diffusion is mechanism with which the minority carriers move to the depletion region. Therefore, minority carrier diffusion length is a most important material parameter. Electrons and holes have characteristic diffusion lengths (L_n and $L_{p,}$) respectively that are material dependent.

The diffusion lengths can be expresses in terms of basic material parameters and they depend on the impurity concentration, crystallinity, crystal

orientation, defect concentration and stoichiometry. The decrease of minority carrier diffusion length with doping density in silicon is shown Fig. 4.15.

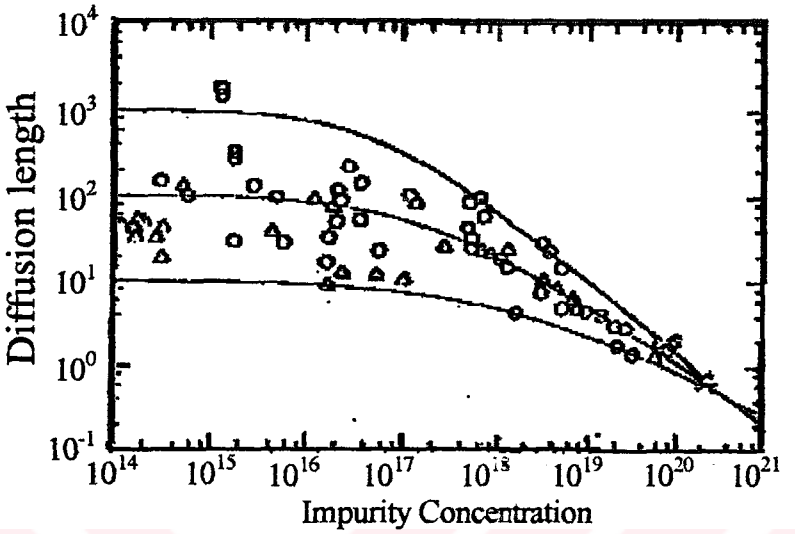


Figure 4.15 Variation of diffusion length with impurity concentration in silisyum. Curves correspond to ranges typical high, average and low lifetime.

The decrease of minority carrier diffusion length with doping density in silicon is shown Fig. 4.15 [3]. Two regions of Fig. 4.15 are of particular interest. The substrate, or base region, typically has a thickness of 100-200 micrometers and doping level in the range 10^{15}-$10^{17}/cm^3$.

Efficient current collection from the base region requires a diffusion length that is greater than the cell thickness.

4.9 Electrical Characteristics of MOS Solar Cell

4.9.1 Current-Voltage Characteristics

The total potential difference V_b between the metal and the semiconductor may be divided into two parts: ψ_{ox} and ψ_s , where ψ_{ox} is the voltage drops across the insulating (oxide) layer and ψ_s is the voltage drops in the space charge layer of semiconductor. This can be written as

$$V_b = \psi_{ox} + \psi_s \tag{4.38}$$

when external voltage V_a is applied across the junction (or when it is developed by the photovoltaic effect) we have

$$V_a = \Delta\psi_{ox} + \Delta\psi_s \tag{4.39}$$

Communication between the surface states, metal, valance and conduction bands of semiconductor may follow six ways:

1. Direct transition of electrons from valance band of semiconductor to the conduction band of semiconductors. The reverse process is radiative recombination that is negligibly small.

2. Holes tunnel through from the valance band of semiconductor to the filled state of metal. In thermal equilibrium, equal current flows from the metal to semiconductor. When light is incident on the semiconductor under the influence of space charge layer photogenerated holes reach the semiconductor oxide interface.

3. An electron current flows the conduction band of the semiconductor to the metal.

4. Current due to tunnelling of electrons flows from the surface states to vacant states in metal. The current is balanced by thermal equilibrium by an equal tunnelling current from metal to surface states.

5. Electrons are captured from conduction band by the surface states. At the same time to maintain an equilibrium, there is reemission of electrons from the filled surface states to the conduction band. At thermal equilibrium both processes balance each other. When external voltage is applied, an electron capture rate exists.

6. In similar process holes in valance band are captured by surface states and reemmitted.

The current through the cell is equal to the algebraic sum of hole and electron current and current by tunnelling at the surface states. A typical energy-band diagram for MOS. solar cell (p-type substrate) is given in Fig. 4.16 in which p-type semiconductor is biased positively with respect to top metal contact by a voltage V_a.

The band gaps of the insulator and semiconductor are represented by E_{gi} and E_{gs}, respectively. The energy difference between oxide and semiconductor conduction band edges is represented by ϕ_{si}. The metal insulator barrier height is represented by ϕ_{mi}.

Under the bias conditions shown in Fig.4.16, there are net current flows J_{ct} and J_{vt}, from conduction and valance band edges of semiconductor to the metal contact due to electron tunnelling transitions between the metal and these bands. Similarly a net current J_{st} flows to metal from the surface states considered localized at the semiconductor oxide interface. The effective current flows due to interchange of the charge between the conduction and valance bands of semiconductor and these states by recombination-generation processes are represented by J_{ci} and J_{vi}, respectively.

When appreciable tunnel starts to flow, if insulator thickness is below about 60 A°, the current is initially of such small magnitude that semiconductor is in thermal equilibrium. If insulator thickness is further decreased, the tunnel current increases to point where they are sufficiently large enough to disturb the semiconductor from thermal equilibrium. This occurs around the 28 A° for Al-SiO_2 (p-type) Si. Thus, in general below some critical value of the oxide thickness nonequilbrium tunnel MOS diode formed.

If oxide thickness is between (15-20 A°) dark I-V characteristic can be taken as

$$I_D = I_o\left[\exp\left(qV_a/nkT\right) - 1\right] \qquad (4.40)$$

where I_o dark saturation current,

$$I_o = AR^{**}T^2 \exp\left(q\phi_{bp}/kT\right) \tag{4.41}$$

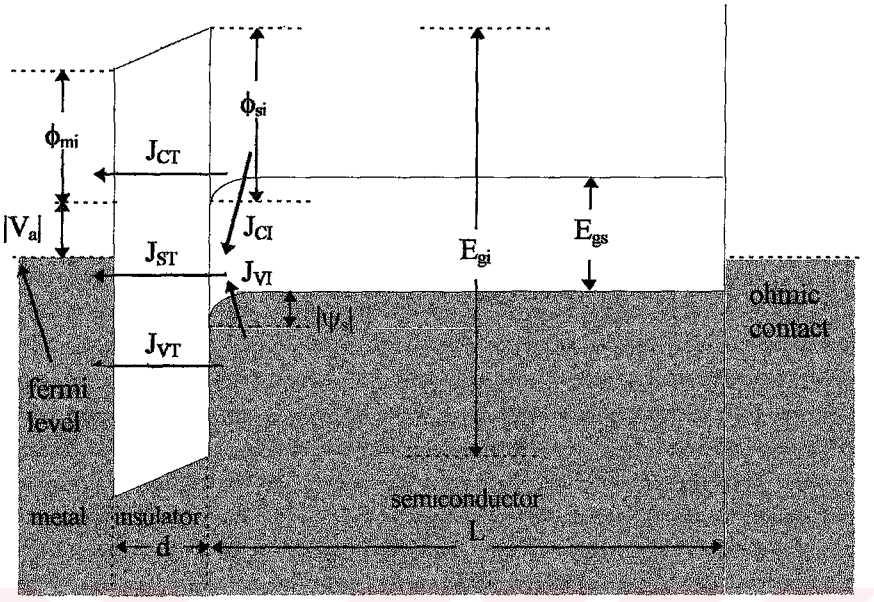


Figure 4.16 Energy band diagram of metal-oxide-p-type silicon solar cell.

The case of tunnel conduction has been treated theoretically by Card and Rhoderick [31] and more recently Green [32]. This theory assumes that, in thin insulator is in tunnel conduction mode with negligible voltage drop across it and that the thermionic emission diffusion theory of Crowell and Sze describes current like in Eqn. (4.40) and (4.41).

4.9.2 Short Circuit Photocurrent

When lights shines on a solar cell the incoming photons generate electron-hole pairs that are collected and become a photocurrent, I_p. The process of collecting the holes and electrons gives rise the photovoltage that is biased as to generate a diode current, I_D, that is in opposing direction to the photocurrent and whose properties given in Eqn. (4.42). The absolute value of photocurrent density generated by incoming light may be written as

$$J_p = qX_1G \tag{4.42}$$

where G is the generation rate that can be written as

$$G = \int_0^{\lambda} \alpha(\lambda) T(\lambda) M(\lambda) \exp[-\alpha(\lambda) x] d\lambda \qquad (4.43)$$

where $T(\lambda)$ is transmittance into the surface layer, $M(\lambda)$ is the incident photon flux and λ_g is the wavelength of photons with the incident energy equal to the band gap energy E_g. This photon or photocurrent, depends strongly on the factor, X_l, that is the collection distance for photogenerated charge carriers.

In MOS solar cells the semiconductor side of the cell is the controlling factor and the metal or oxide portions affect the interface recombination of holes and electrons in the solar cell.

I-V characteristics of MOS solar cell under illumination, is given as

$$I = I_o\left[\left[\exp\left(qV_a/nkT\right) - 1\right] - I_p\right] \qquad (4.44)$$

where I_p is the photocurrent. The short circuit photocurrent of an ideal solar cell is dependent primarily on the intensity of illumination and material parameters. It is given by

$$I_{SC} = \frac{-I_p}{1 + \frac{qR_S I_o}{n}} \qquad (4.45)$$

4.9.3 Open Circuit Photovoltage

If the solar cell is illuminated but the load is disconnected, no net current can flow and to balance the photocurrent component there must be an increase in dark current which flows in the direction opposite to that of photocurrent.

Under open circuit conditions $I=0$, $V_a=V_{oc}$

$$0 = I_o\left[\exp\left(qV_{oc}/nkT\right)\right] - I_{SC} \qquad (4.46)$$

By neglecting the effects of R_s and R_{sh} and assuming largest value of the photocurrent $I_p=I_{sc}$. It follows that

$$V_{oc} = \frac{nkT}{q} \ln\left[\frac{I_p}{I_o} + 1\right] \tag{4.47}$$

since I_o is always very small as compared to I_p, V_{oc} can be written as

$$V_{oc} = \frac{nkT}{q} \ln\frac{I_p}{I_o} \tag{4.48}$$

It is clear from Eqn. (4.48) to obtain high value of open circuit photovoltage for a given photocurrent, the saturation values of dark current components must be rendered small.

The higher V_{oc} values at higher base layer doping densities are a direct consequence of layer dark current. However, this capability of developing high V_{oc} must be weighted against the reduced carrier lifetimes in the base which will reduce I_{sc}. Thus, overall cell conversion efficiency will not increase indefinitely with an increase in base layer doping density. Furthermore voltage reducing effects also serve to reduce V_{oc} at high base layer doping levels. The high short-circuit current are thus seen to be conflicting. However, high open circuit photovoltage are possible in solar cell with high resistively base layers.

4.9.4 Fill Factor and Efficiency

The fill factor, FF, of a solar cell is a measure of the "sharpness of knee" in output current-voltage curve of Fig. 4.17. I-V characteristics of a solar cell under illumination indicating the effects of series and shunt resistances is shown in Fig. 4.17. It is clear that FF will be adversely affected by R_s and R_{sh} but dependence are other properties of the cell may not be obvious.

Consider the I-V characteristics of MOS solar cell under illumination as shown in Fig. 4.13. It is

$$I_L = I_o\left[\exp\left(qV_L/nkT\right) - 1\right] - I_p \tag{4.49}$$

and therefore the output power $P_{out}=I_L.V_L$. Its maximum value

$$P_{max} = I_m V_m \tag{4.50}$$

when dP_{out}/dV_L and equating $V_L=V_m$ we get

$$\left(1+\frac{qV_m}{nkT}\right)exp\left(\frac{qV_m}{nkT}\right) = \frac{I_p}{I_o} + 1 \tag{4.51}$$

Eqn. 4.51 can be solved numerically to find V_m and

$$I_m = \left[I_o exp\left(\frac{qV_m}{nkT} - 1\right) - I_p\right] \tag{4.52}$$

or

$$I_m = \left[I_o\left(\frac{qV_m}{nkT}\right)exp\left(\frac{qV_m}{nkT}\right)\right] \tag{4.53}$$

Maximum power can obtained as

$$P_{max} = \left[I_o\left(\frac{qV_m}{nkT}\right)\exp\left(\frac{qV_m}{nkT}\right)\right]V_m \tag{4.54}$$

The fill factor becomes

$$FF = \frac{I_m V_m}{I_{sc} V_{oc}} \tag{4.55}$$

$$FF = \frac{I_o\left(\frac{qV_m}{nkT}\right)exp\left(\frac{qV_m}{nkT}\right)V_m}{I_{sc}V_{oc}} \tag{4.56}$$

the efficiency of a solar cell is the ratio of electric power which can be abstracted at the maximum power point and input power density.

$$\eta = \frac{P_{max}}{P_i A} \tag{4.57}$$

P_{max} can be written as

$$P_{max} = I_{sc} V_{oc} (FF) \tag{4.58}$$

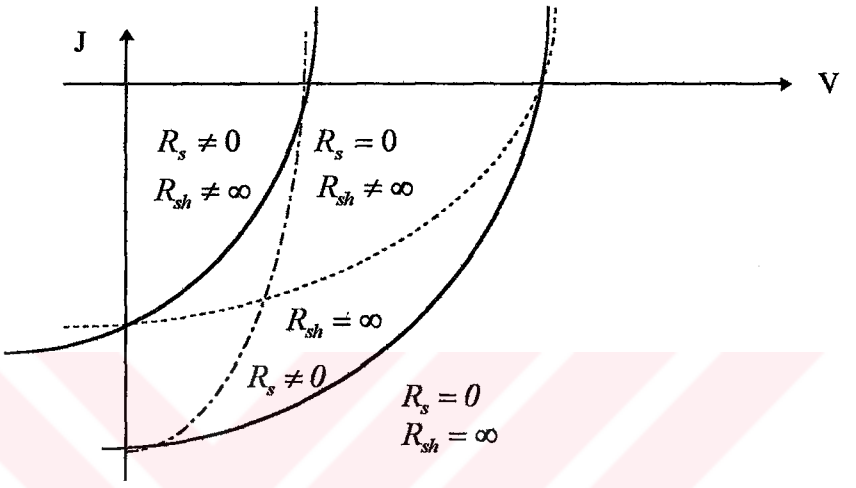


Figure 4.17 J-V characteristics of solar cell indicating the effects of series and shunt resistances.

4.9.5 Capacitance of the MOS System

As with the Schottky barrier and the *pn* junction, analysis of the behavior of the small-signal capacitance measured between the two output electrodes provides very valuable insight into the electrical behavior of the MOS system. In the case of the MOS system, this analysis has been central to research that has resulted in the present well-developed state of understanding of the oxide-silicon system and its technology.

Consider first that the MOS system is biased with steady voltage that causes the silicon surface to be accumulated. For a *p*-type silicon sample such as that of Fig. 410a, this corresponds to a negative applied voltage and would result in a charge configuration like that sketched in Fig.4.10c. The excess holes at the surface are pulled very close to the oxide. If a small ac voltage is superposed on the dc bias, it causes small variations in the charges stored on

the metal gate and at the silicon surface. If the system is now connected to an instrument that measures the capacitance associated with these variations, the capacitance measured will be very close to that of the oxide itself because the spatial extent of the modulated charge in the silicon is small compared to the oxide thickness. The more the surface is accumulated, the thinner will be the accumulated layer (effectively, the Debye length at the surface will be reduced by the added carriers); hence, the capacitance will approach asymptotically the capacitance associated with the pure oxide. Thus, the capacitance per unit area* C' in accumulation approaches

$$C'_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \tag{4.59}$$

where T_{ox} is the oxide thickness. When the gate voltage is changed in the direction of its flat-band value, the surface accumulation decreases to zero and the capacitance decreases as Debye length at the surface increases. To obtain an exact formulation for capacitance in this bias range, it is necessary to solve Poisson's equation under the condition that free electrons, free holes, and dopant atoms all contribute to the total space charge at the surface. This analysis was first carried out by Kingston and Neustadler [33] and their results have been widely applied to obtain various electrical properties of MOS systems. A particular result that is readily calculated from the Kingston and Neustadler theory is the capacitance Per unit area when $V_G=V_{FB}$. If this quantity is called C'_{FB}, it can be expressed [1] by

$$C'_{FB} = \frac{1}{T_{ox}/\varepsilon_{ox} + \left[kT/q^2\varepsilon_s N_a\right]^{1/2}} = \frac{1}{1/C + L_D/\varepsilon_S} \tag{4.60}$$

where L_D, the extrinsic Debye length. The characteristic decay length L_D appearing in the exponential is known as the DEBYE LENGTH.

When the gate voltage becomes more positive than the flat-band voltage, holes are repelled from the surface of the silicon and the system is in the depletion-bias condition. Under this condition, relatively straightforward

electrostatic analysis shows that the overall capacitance corresponds to the capacitance that is obtained by a series connection of the oxide capacitance and the capacitance across the surface depletion region

$$C' = \frac{1}{1/C'_{ox} + w/\varepsilon_s} \tag{4.61}$$

where w is the width of the surface depletion layer, which depends upon gate bias as well as the doping and oxide properties. From Eqn. (4.61) we see that the capacitance of the system decreases as the depletion region widens.

When the gate bias is increased sufficiently to invert the surface, a new feature must be considered to describe the MOS capacitance behavior. We recall that the inversion layer at the MOS surface results from the generation of minority carriers. Hence, the population of the inversion layer can change only as fast as carriers can be generated within the depletion zone near the surface. This limitation causes the measured capacitance to be function of the frequency of the ac signal that is used to measure the small-signal capacitance of the system.

The simplest case arises when both the dc gate-bias voltage and small-signal measuring voltage are changed very slowly so that the silicon can always approach equilibrium. In this case, the signal frequency is low enough so that the inversion-layer population can "follow" it. The capacitance of the MOS system is just that associated with charge storage on either side of the oxide; its value is therefore approximately C'_{ox}. Under this circumstance, a plot of measured capacitance versus gate bias follows the dashed curve marked "low frequency" in Fig.4.18 going from C'_{ox} in the accumulation region of bias through a decreasing region as the surface traverses the depletion region and moving back up to C'_{ox} when the surface becomes inverted.

A characteristic time to form an inversion layer at the surface of an MOS system biased to inversion is of the order of $(2N_a\tau_0/n_i)$ where τ_0 is the minority-carrier lifetime at the surface.*

For typical values of lifetime (1 μs) and dopant concentrations (10^{15} cm^{-3}), this time is roughly 0.2 s. Therefore, the small-signal measuring voltage must be changed very slowly to observe the low-frequency C-V curve (dashed curve of Fig. 4.18).

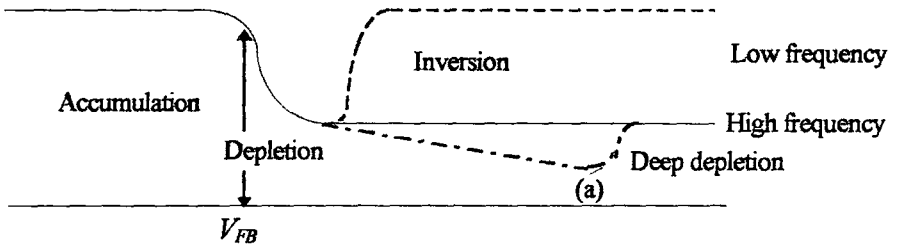


Figure 4.18 Small-signal capacitance of an MOS system with *p*-type silicon.

Low frequency behavior: both the bias voltage and the ac measuring signal vary slowly (less than ~10 Hz.)* High frequency behavior: bias voltage varies slowly, but the ac measuring signal varies rapidly (typical circuits use 1 MHz); deep depletion variation: both the gate bias voltage and the ac measuring signal vary rapidly. The behavior at point (a) is described in the text.

The presence of some means, such as surface illumination, that can stimulate the surface generation and recombination rates will increase the range of the low-frequency behavior. If the inversion layer extends to contact a source for electrons, the low-frequency curve can be observed at frequencies extending into the MHz range. This is the case because the electrons in the inversion layer can then be supplied and withdraw rapidly through the ohmic connection.

When the ac measuring signal is changed rapidly while the dc bias voltage is varied slowly, the inversion layer cannot respond to the measuring signal. The number of charges in the silicon space-charge layer is modulated instead by the movement of holes at the far edge of the depletion region. The capacitance then corresponds to the series combination of the oxide capacitance and the depletion-region capacitance, as was true in depletion-mode bias. Since the depletion region reaches a maximum width W_{max} when the system goes into strong inversion, the measured capacitance approaches a

* Generation from surface states is considered negligible. Note that τ_0 can vary considerably in practice

value corresponding to the series connection of the oxide capacitance and to that associated with the maximum depletion-region width. It remains constant at this value as the bias voltage is increased further. This high-frequency C-V curve is shown by the solid line of Fig. 4.18.

A final capacitance behavior is sketched in Fig.4.18. This is the curve shown dot-dashed and marked *deep depletion.* It corresponds to the experimental situation in which both the gate bias voltage V_G and the small-signal measuring voltage vary at a faster rate than can be accommodated by generation-recombination in the surface depletion region. Since the inversion layer cannot form, the depletion region becomes wider than w_{max} and the name *deep depletion* is properly descriptive. The capacitance in this mode is given by Eqn. (4.61) as was true in the normal depletion mode; here, however, w exceeds the inversion value w_{max} and C' does not reach a minimum. One means of generating a "deep depletion" capacitance curve is to sweep the gate bias V_G with a low-frequency triangular wave upon which is superposed the sinusoidal ac measuring frequency. The generation of carriers increases as the depletion layer is widened, however, and the deep-depletion curve is frequently observed to relax to the high-frequency curve at higher biases. The relaxation is indicated schematically at point *(a)* on the deep-depletion curve of Fig. 4.18.

CHAPTER 5

EXPERIMENTAL PROCEDURE AND RESULTS

5.1 Introduction

There are several important processes which contribute to the eventual production of the monolithic integrated circuit. They include:

(a) Purification and preparation of the silicon wafers.

(b) Epitaxial growth.

(c) Oxidation

(d) Photomasking and etching.

(e) Diffusion

(f) Metal deposition (interconnections)

Semiconductor material prepared for a specific device applications requires careful evaluation to see if its parameters lie within the specification for a particular device structure. There are available today a wide range of material and device evaluation techniques, with which to characterize both the base material and in some cases to evaluate the actual layers within device structures.

For device grade semiconductor layers, the following information is usually required:

(a) Inspection of layer quality, morphology, uniformity, and thickness;

(b) Evaluation of layer resistivity (or conductivity) and mobility;

(c) Measurement of doping profiles.

This chapter explains the laboratory techniques for measuring some basic electrical parameters. The methods used in fabricating MOS solar cells (using *p*-type silicon crystal) and the results of experiments their physical characteristics are given.

5.2 Determination of Conductivity Type

The carriers present in a semiconductor move by one of two processes, drift or diffusion. DRIFT is the motion caused by the presence of an electric field. With no applied field, carriers move about randomly in a semiconductor Fig. 5.1a. Under the influence of an applied field, the carriers acquired a direct component of motion Fig. 5.1b. The sum of the directed components of drift procedure current flow in the sample. DIFFUSION is the migration of particles from regions of high concentration to region of low concentration caused by random motion. The resultant magnitude and direction of both types of carrier motion determines the total current flow in a material.

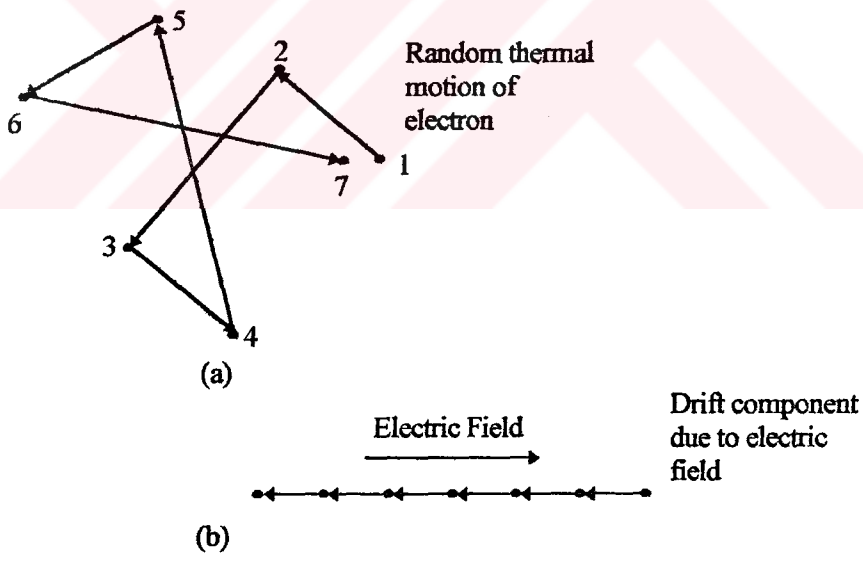


Figure 5.1 Carrier drift under the influence of an electric field.

The diffusion of the mobile carrier (either holes in *p*-type silicon or conduction electrons in *n*-type silicon) from temperature regions to lower temperature regions is used to determine whether a sample of silicon is *n*-type or *p*-type. If an area of silicon wafer is heated locally, as shown in Fig. 5.2, the

majority carriers diffuse away from the heated region. A voltage results which is measured to determine the conductivity of the sample. If the sample is *n*-type, the voltage on the hot probe is positive with respect to a second probe. Similarly, if the sample is *p*-type, the voltage on the hot probe is negative with respect to a second probe. This testing technique is useful on samples unless there is just a thin layer of oppositely doped material on the surface of the wafer.

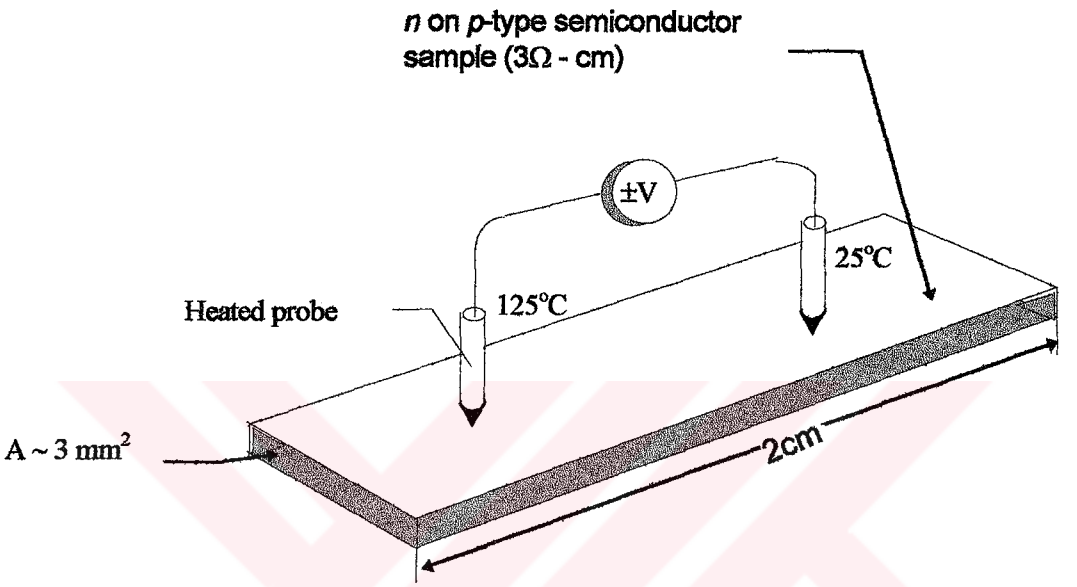


Figure 5.2 Determination of conductivity type using the hot-probe technique.

5.3 Fabrication of Solar Cells

At laboratory MOS solar cells fabricated were from silicon available as 400-560 micron thick, 76.2 diameter slices. The slices were cut from single crystal silicon <111> metallurgical plane. They are slightly *p*-type and according to manufacturers specification, resistivity of wafer is 2-20Ω-cm.

The process involved in the fabricating of the MOS solar cells can be grouped under five headings,

1. Determination of the resistivity
2. Preparation of crystals
3. Oxidation of silicon
4. Preparation of mask

5.3.1 Determination of the Resistivity

The amount of dopant in a wafer, bar or sample of doped silicon is determined by first measuring the sheet resistance R_s of the wafer, bar, or sample in ohms per square ($\Omega/\square$). The probe is a practical and simple way of determining the sheet resistance. Here four equally spaced collinear probes are placed onto the layer surface Fig. (5.3a). A current of I (amperes) is passed through the outer probes and a voltage V (volts) is measured using the two inner probes. Note that these two inner probes do not draw a current and there is, therefore no need to worry about any contact resistances. A valve of current I is chosen such that V and I are linearly interrelated.

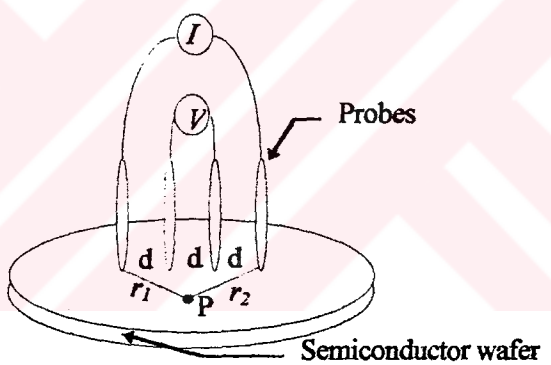


Figure 5.3 (a) The geometry of a four point probe.

For situations where the layer is: *p* on *n* or *n* on *p* or *p*(or *n*) on semi-insulating layer all the current drown passes in the layer being measured. Now for the outer two probes drawing a current I the potential at some arbitrary point P is:

$$V_p = \frac{I}{2\pi} R_s \ln\left(\frac{r_2}{r_1}\right) + A \qquad (5.1)$$

where A is a constant of integration.

Apply this equation to the central electrodes of the four-point probe:

$$V_1 = \frac{IR_s}{2\pi}\ln 2 + A \tag{5.2}$$

$$V_2 = -\frac{IR_s}{2\pi}\ln 2 + A$$

to obtain the potential V between the inner probes

$$V = V_1 - V_2 = \frac{IR_s}{\pi}\ln(2)$$

Rearranging,

$$R_s = \left(\frac{\pi}{\ln(2)}\right)\frac{V}{I} = 4.5324\left(\frac{V}{I}\right) \tag{5.3}$$

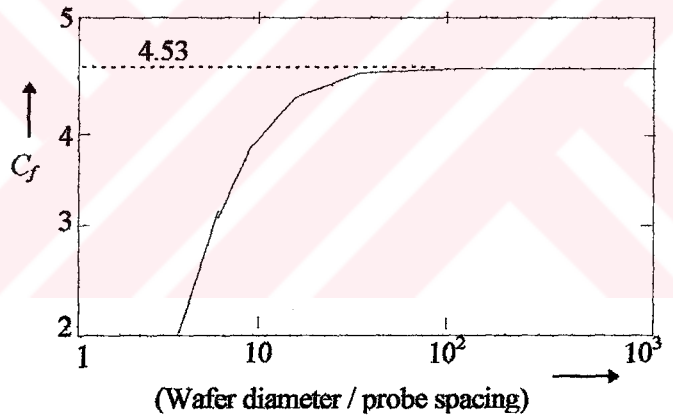


Figure 5.3b The correction factor C_f plotted as a function of the ratio of wafer diameter to probe spacing.

The equation for R_s presented above assumes an infinite wafer. In practice, the use of finite wafers requires a correction factors of where C_f is defined

$$R_s = C_f\left(\frac{V}{I}\right) \tag{5.4}$$

For the simple case of circular wafers with central probes the relationship between the correction factor C_f and the wafer diameters/probe spacing is shown in Fig. (5.3b).

5.3.2 Preparation of Crystals

Numerous methods of cleaning are popular in semiconductor industry, but they all have certain common characteristics. The first step in dealing with wafers with an unknown history is to thoroughly degrease them. A common method is used of a degreasing chemical such as 1,1,1-trichloroethone followed by rinses in acetone and alcohol. This cleaning procedure guarantees that only greases or waxes that might be insoluble in subsequent cleaning steps are removed. (If the history of the wafer is known, this degreasing operation may often be safely omitted.) Wafers are then sent through a series of solutions designed to remove any trace of metals or other potentially harmful materials. A common series of cleaning step is:

STEP	REASONS
Heat in H_2SO_4	Removes any photoresist or other organic material.
Heat in aquareqia	Dissolves gold as well as other metals.
DIP briefly in dilute HF	Top layer of SiO_2 containing any potential contamination is etched away.
Rinse in water	Remove any residual acid.
Dry	Get wafers ready for the next process step.

Cleaning process in our laboratory:

All silicon substrates used in this experimental work have been prepared as follows.

Step 1: Firstly,the silicon substrate is immersed into the trichloroethone and left there for 5 minutes to clean the oily substances on the surface on the substrate using the ultrasonic cleaner (Bransonic 221).

Step 2: The taken substrate in cup is immersed into the asetone and procedure of step 1 is applied.

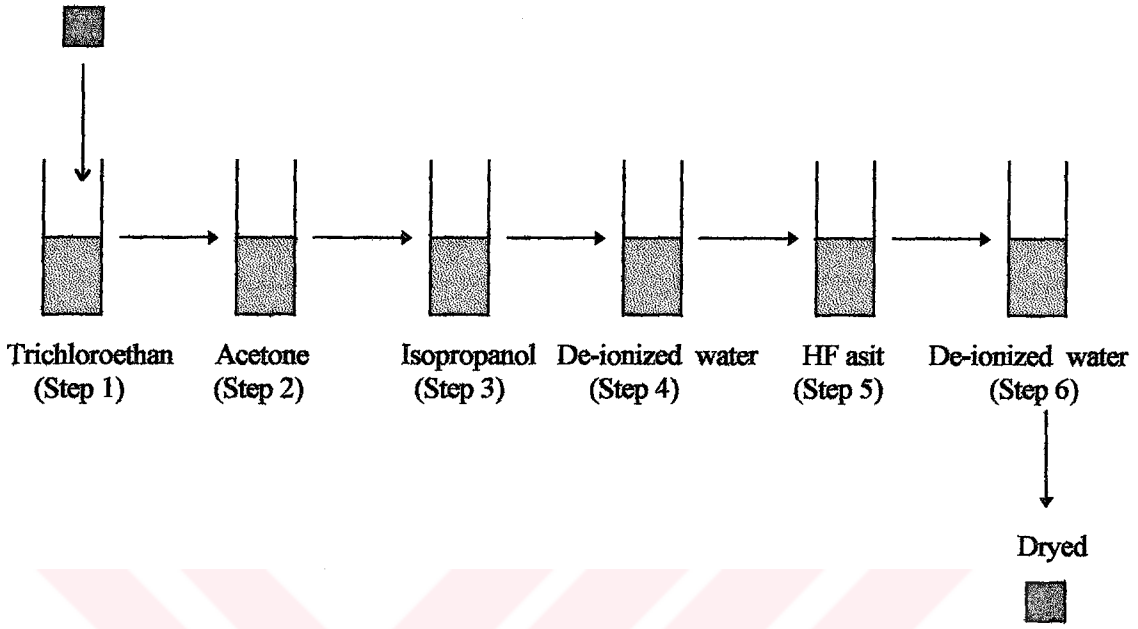


Figure.5.4 Cleaning process of the silicon substrates.

Step 3: The substrate is immersed into the isopropanol and procedure of step 1 is applied.

Step 4: After these steps, sustrate is immersed into the dionized water and rinsed.

Step 5: The cleaned substrate is immersed into the Hydrofluoric acid (40 % pure) for 2 minutes.

Step 6: This step, the substrate is rinsed again and dryed by the vacuum system (solitec).

5.3.3 Oxidation of Silicon

The ability to grow a chemically stable protective layer of silicon dioxide (SiO_2) on a silicon wafer makes silicon the most widely used semiconductor substrate. The silicon dioxide layer is both an insulating layer on the silicon surface and preferential masking layer during the fabrication sequence.

The presence of a very thin layer of SiO_2 does not interfere with the diffusion of oxidizing atoms to the Si- SiO_2 interface. These atoms diffuse to the interface until an excess of them is present. The SiO_2 growth rate is limited by the speed with which the silicon can react with the oxidizing atoms. This case called the reaction-rate-limited case, is shown in Fig. (5.5a). When the oxide layer is sufficiently thick, the oxidizing species cannot diffuse through this layer rapidly enough to keep the reaction going at peak speed. This case the "transport-limited" or "diffusion-limited" case, is shown in Fig. (5.5b).

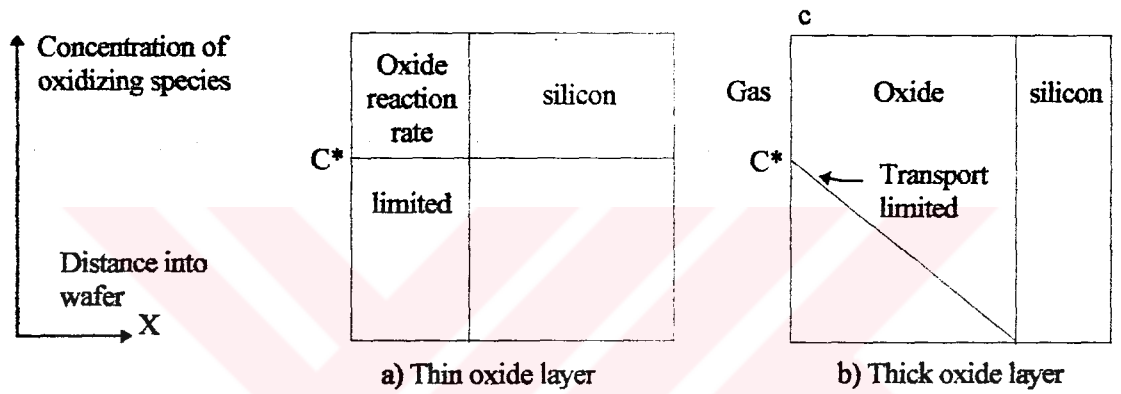


Figure 5.5 Distribution of the oxidizing species in the oxide layer for the two limiting cases of oxidation.

In our experimental work optimum oxide thickness is 10-25 A° [35]. For such thin oxide growth on the polished surface of the wafer, the natural oxide technique that forms at room temperature was used. Fig. (5.6) shows oxidation time versus film thickness for cleaned silicon crystal with a <111> oriented surface as for an etched silicon surface, in air at room temperature [36]. To get optimum oxide thickness silicon slices are hold in air for 24-30 hours at room temperature.

The range of the insulator thickness which has been considered for the Al- SiO_2-(*p*-type) Si device is 10-28 A°. Above 28 A° the device becomes on equilibrium tunnel diode and below 10 A° it exhibits schottky-diode behaviour [37].

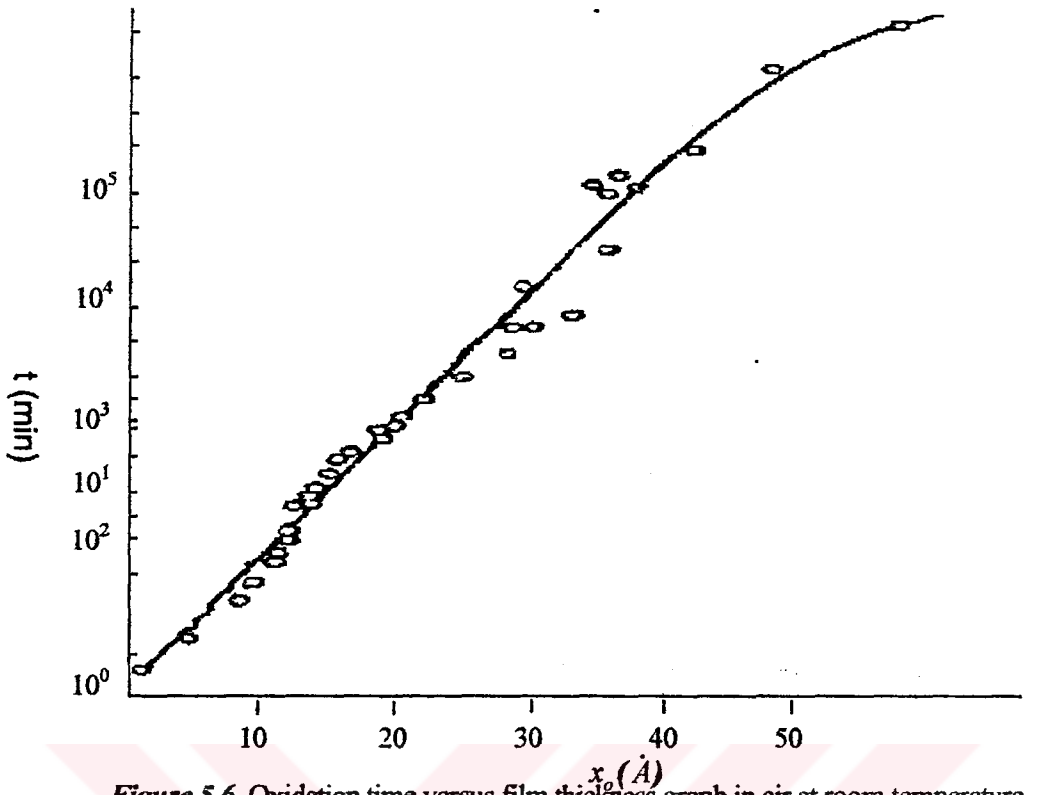


Figure 5.6 Oxidation time versus film thickness graph in air at room temperature.

5.3.4 Preparation of Mask

A mask must be used to determine the active area of the cell and to have electrical connection between the contacts and terminals.

Mask is prepared from copper board whose other face is fiber. Mask is cut into 15x15 mm^2 dimension as in silicon wafers. A circle which has a diameter of 10 mm was drilled from the center of square wafer. The dimension of the circle is also the dimension of the active area. After then, masks are cut like an inclined plane from the end of the circle to get electrical connection between contact and terminals as shown in Fig. (5.7).

Silicon slices which are cleaned were placed between two masks and adhered by Bally. The nail polished was coated on the inclined plane and copper side of the mask to support electrical connection. After this process, they are waited in air at room temperature, for different time durations (10-48 hours) to get thin oxide layer.

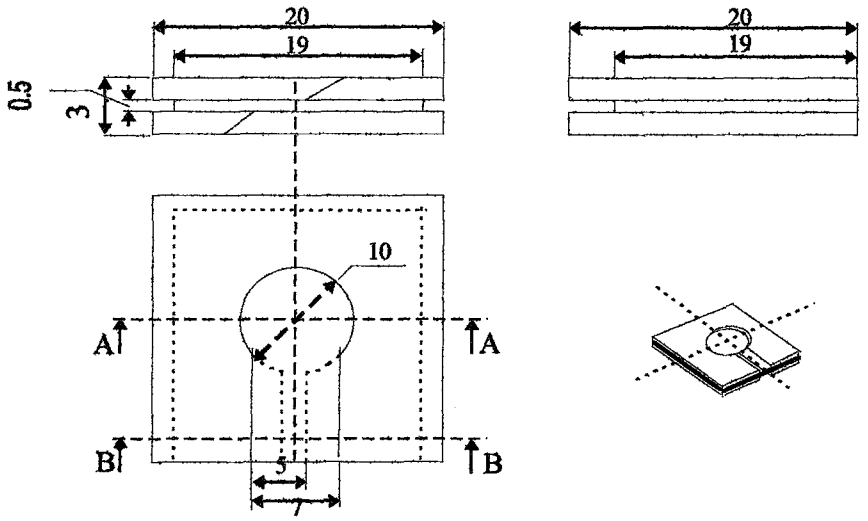


Figure 5.7 Perspective and three dimensional view of MOS solar cell .

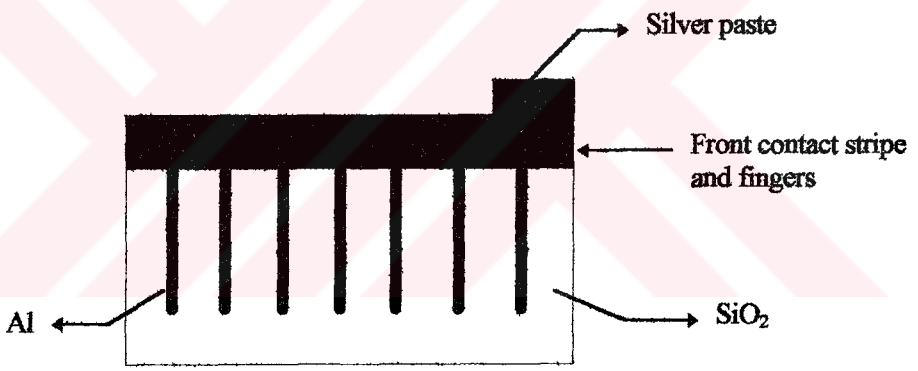


Figure 5.8 Top view of MOS solar cell.

In the other method there is no need copper board. A front ohmic contact stripe and fingers, a back ohmic contact that covers the entire back surface, and an antireflection coating on the front surface. Active region of silicon is coated very thin aluminum layer making a appropriate mask as shown in Fig.5.8 to absorb more light.If we want to take electrical connection, this contact area is coated very thick aluminum layer.Copper wire is bond this area by silver paste (It is a liquid and it has conductance characteristics.).

5.3.5 Application of Ohmic Contact

Ohmic contacts to silicon are made by evaporating aluminum to silicon using Edwards AUTO 306 Vacuum Coater with Diffusion Pumping System. The successful etching of the aluminum on the front side of the wafer to form the device interconnection does not guarantee that a good electrical contact has been formed. A subsequent *alloying* step is usually used to produce a low resistance contact between the aluminum and the silicon. Alloying is performed in a diffusion furnace set at a relatively low temperature.

The aluminum-silicon EUTECTIC TEMPERATURE is 577°C. If an aluminum-silicon mixture is heated to above 557°C, melting will occur, ruining any devices that are present. The upper limit in the alloy temperature is thus 577°C. The lower temperature is set by process concentrations like cleanliness and the aluminum deposition temperature. Most alloying steps are performed at temperature between 450 and 550°C for times of between 10 and 30 minutes.

During alloying or directly following it the wafer are often heated in a gas mixture containing hydrogen (or occasionally another gas). This step is usually called ANNEALING. Annealing is designed to optimize and stabilize device characteristics.

The resistance *R* of the result aluminum-silicon contact depends upon:

1. Contact area
2. Surface doping concentrations
3. Surface cleanness
4. Alloy or sintering conditions

The goal of the aluminum alloy or sintering is to minimize the contact resistance. If alloying is performed at the correct temperature and the surface is property cleaned the dependence of contact resistance can be reduces to; **1.** Contact opening size **2.** Doping concentration

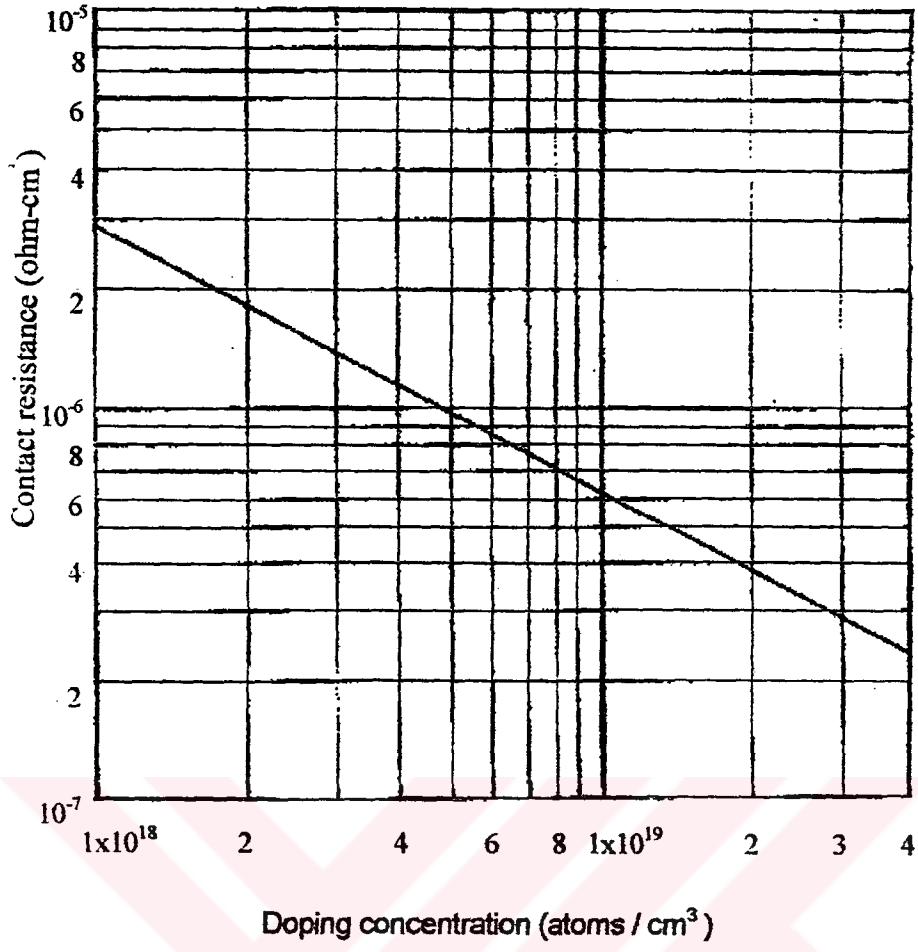


Figure 5.9 Contact resistance of aluminum on *p*-type silicon.

Fig. (5.9) indicate the dependence of contact resistance R_c in Ω-cm^2 upon doping concentration for aluminum on *p*-type.

Once the contact dimensions are known, it is a simple matter to calculate the actual resistance *R* from equation (5.5) for a rectangular contact

$$R = \frac{R_c}{(contact - lenght) * (contact - width)} \qquad (5.5)$$

At our laboratory, before oxidation, a thick aluminum layer (~1000 A°) was evaporated on the back side of cleaned silicon silice providing ohmic contact. Aluminum is evaporated by the resistance heating method in which a tungsten wire wound in the form of a basket (or spiral) is used as heating element. Evaporation temperature of aluminum is 900°C at 10^{-5} Torr and the vapor pressure of Tungsten is very low (10^{-16} Torr). Purity of aluminum is not degraded

by any tungsten vapour. After oxidation, silicon slice is annealed in furnace containing dry N_2 for 1 minutes at 620°C. The top aluminum (70-100 A°) is deposited on the active area through a solid mask using deposition rate of 1-10 A°/sec at $4x10^{-5}$ torr.

5.4 Vacuum Deposition

A metal layer on a wafer is not often obtained using a vacuum deposition system. There are many types of vacuum depositions systems, but they have the same characteristics in common.

In our experimental work, metal coating was made by Edward's (model AUTO 306) Vacuum Coater with Diffusion Pumping System which is shown Fig. (5.10a) and (5.10b). The Auto 306 is micro processor controlled vacuum coater that can be configured to perform a variety of coating tasks. It has the following main elements:

1. Vacuum pumping system (vapor diffusion pump and rotary pump)
2. A microprocessor control system and control panel.
3. Chamber that may be evacuated to provide a sufficient vacuum for the deposition to take place.
4. Water cooled crystal holder to measure the thickness of the coating layer using (model FTM5). Film Thickness Monitor.
5. A baseplate
6. Cabinet

The baseplate of the coater provides an interface between the process chamber and the system. It is manufactured from stainless steel and is machined with a number of holes to enable the mounting of optional vacuum electrodes.

The rotary pump uses a rotor that is sealed against the leakage by a vacuum system, vapor that enters the pump through the inlet port, is compressed, and is ejected to the atmosphere through the exhaust or discharge part.

In the diffusion pump, vapor from a boiler passes through a series of nozzles in a downward direction carrying residual atoms in the chambers with it. Atmospheric pressure can be reduced up to 1.10^{-7} by diffusion pump.

The instrumentation of a vacuum deposition system provide a method of

1. Determining the vacuum level in the chamber.
2. Measuring the status of all valves, etc., in the system.
3. Determining the thickness of any deposited layer.

For vacuum deposition filament evaporation technique is used. In this technique, current flows through a filament. Filament evaporation is the simplest and least expensive deposition method. Evaporation takes place from filament o boat heated by thermal resistance heating. Evaporation is accomplished by gradually increasing the current flowing through the filament (care must be taken to choose a filament compatible with material to be evaporated). Filament evaporation systems are easy to set up and any materials can be evaporated using them. However, the contamination level of the deposited materials is often sufficiently high to interfere with the functioning of the device. Contamination may come from the filament or from poor handling techniques. For this reason filament evaporation of aluminum is not common.

The metal which is used for deposition must meet or exceed all of the requirements:

1. The metal must make a low resistance electrical contact with the silicon.
2. The metal must have a limited reactivity with silicon in order to produce stable contact.
3. The metal must have a high electrical conductivity, so that high current is easily carried without any voltage drops.
4. The metal must adhere well to the underlying silicon, silicon dioxide.
5. The metal coating must not exhibit electromigration (Electromigration is the migration of atoms in the deposition of metal caused by flow of current).
6. The metal coating must not corrode under normal operating conditions.

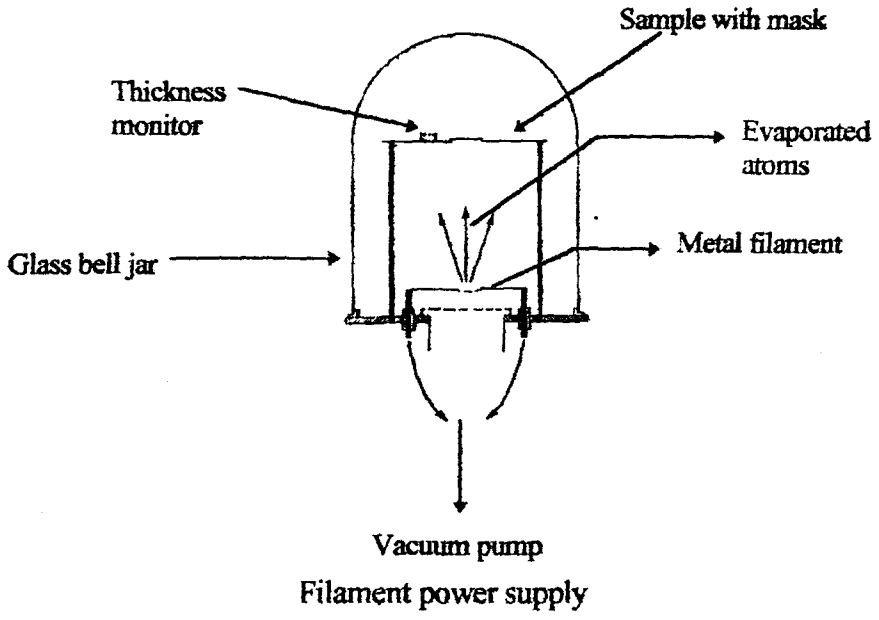


Figure 5.10a Vacuum Evaporator

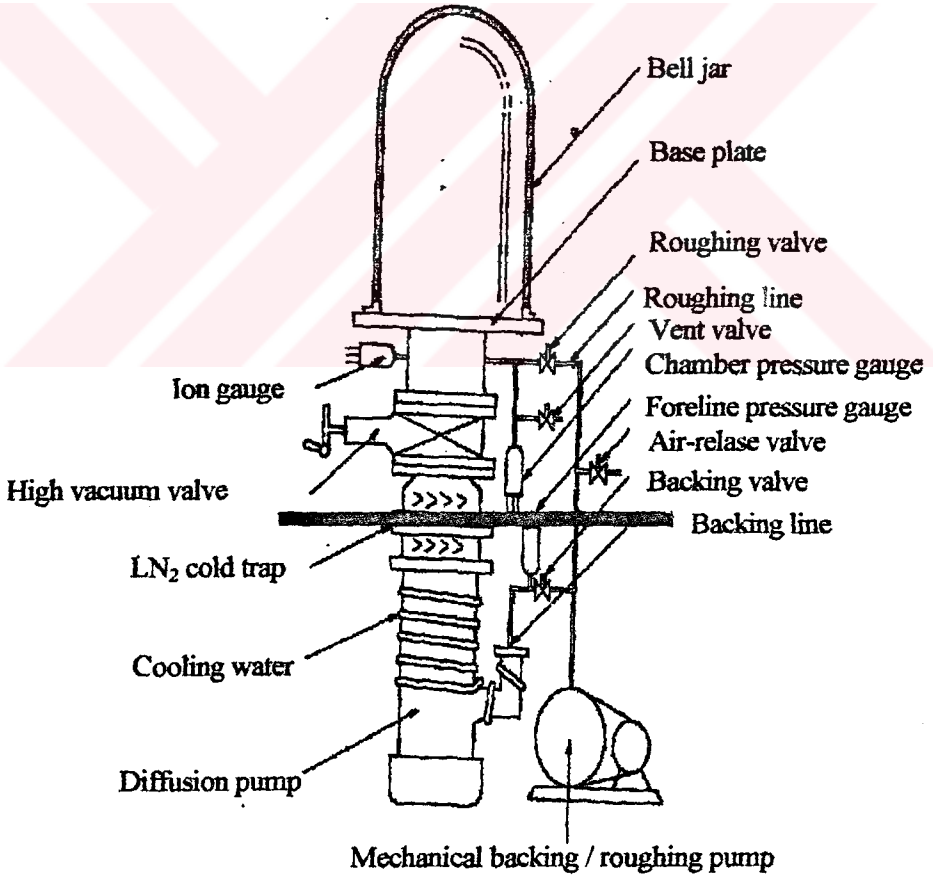


Figure 5.10b Schematic diagram of a typical fast-cycling, high-through-put vacuum coating system.

No metal perfectly meets all of these requirements. However, aluminum does meet all of them satisfactory.

5.5 Determination of Band Gap and Energy Level Values of Trap Levels in the MOS Cells

The values of the band gaps of insulators and semiconductors are measured by using different methods. The band gap energies depend on the temperature, the variation of absorption, photoconductivity excitation, and luminescence excitation as a function of wavelength, or the wavelenght dependence of the emitted luminescence radiation of free electrons and free holes.

Photoconductivity is the increase in electrical conductivity of an insulating crystal caused by radiation incident on the crystal.

Variation of photoconductivity excitation with wavelenght method through the current (or voltage) caused by the free carriers created as the result of absorption.

The values of energy levels of sensitizing centers in the forbidden gap are determined by means of smaller peaks in the photoconductivity excitation .

In this experimental work, we measured the value of the band gap of MOS cell by using the variation of photoconductivity excitation with wavelength method as shown in Figures.5.11,12, and 13.

We know that if the light impinges on the cell, the electrons in the valance band are excited to the conduction band. But if the energy of the light is smaller than the band gap of the cell, the electron can not be excited to the conduction band. The excited electrons return to the valance band see Fig.4.1a. Also, if the energy of the light is larger than the band gap of the cell, in this case the excited electrons go above the higher energy over the conduction band see Fig.4.1c.

The energy value of a light at a fixed wavelength is;

$$E_p = hv = h\frac{c}{\lambda} \tag{5.6}$$

where E_p is the energy value of light, h is the Planck constant, v is the frequency, c is the velocity of light. and λ is the wavelength of light.

If the wavelength of incident light is changed, the energy value of light is changed. And at a certain wavelength the electrons are excited from the valence band to the conduction band. This energy value of light is approximately equal to energy value of band gap ($E_p = E_g$). Thus at this condition a small current or voltage pulse is generated on the cell.

The wavelength of light is changed by using a Spectrophotometer, operating in a wavelength range 200-1100 nm.

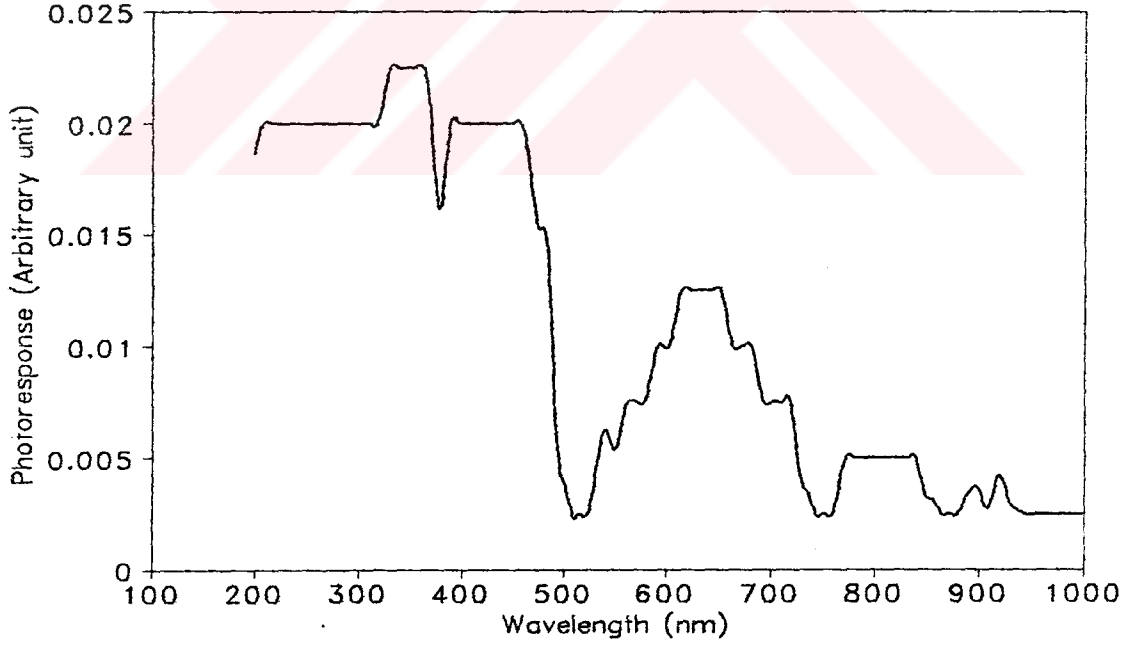


Figure.5.11 Photoresponse excitation as a function of wavelength for sample 14.

The photoresponse at MOS cell is obtained as a function of wavelength as seen in Fig.5.11. As seen from this figure, the maximum peak occurs at 350 nm. This means that the maximum response of this cell to takes place at 350 nm. At this wavelength, the electrons get excited from valence band to the conduction band. By using equation 5.6, the band gap of cell is found 3.5 eV.

The value obtained from these by experimental study is the expected value. The other three peaks which appear at 450 nm, 650 nm and 800 nm are seen in the same figure. Following the same procedure, the values of the photons corresponding to the these wavelenghts at the same time which show the trap energy level in the forbidden energy region are found 2.75 eV, 1.907 eV and 1.55 eV,respectively

Applying the same procedure all of the figures , we can say that, energy gap of cell is changed between 3.5 eV and 4.13 eV.

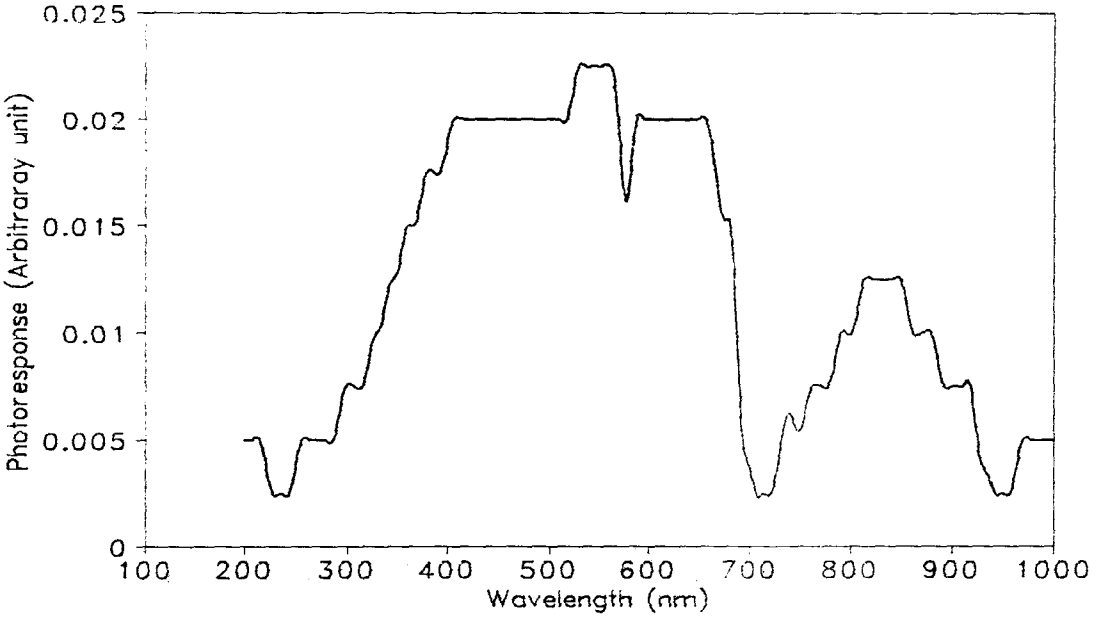


Figure 5.12 Photoresponse excitation as a function of wavelenght for sample 15.

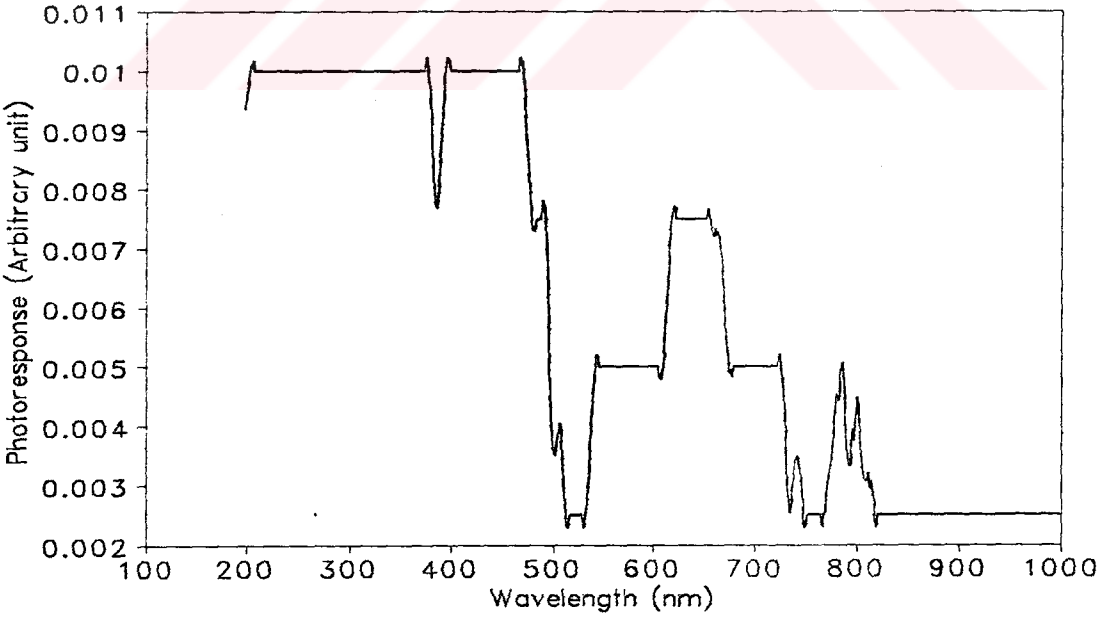


Figure 5.13 Photoresponse excitation as a function of wavelenght for sample 16

5.6 Determination of Absorption Coefficient of Silicon

To determine the absorption coefficient, Spectrophotometer was used for the transmission and absorption measurement. This procedure is carried out as follows;

Firstly, the absorption values corresponding to different wavelengths are found for silicon sample by using the Spectrophotometer. Then, the absorption coefficients α of silicon as shown Fig.5.14 corresponding to different wavelengths are calculated by substituting to thickness of silicon and absorption values, in the equation;

$$\alpha = \frac{Absorption}{d} \tag{5.7}$$

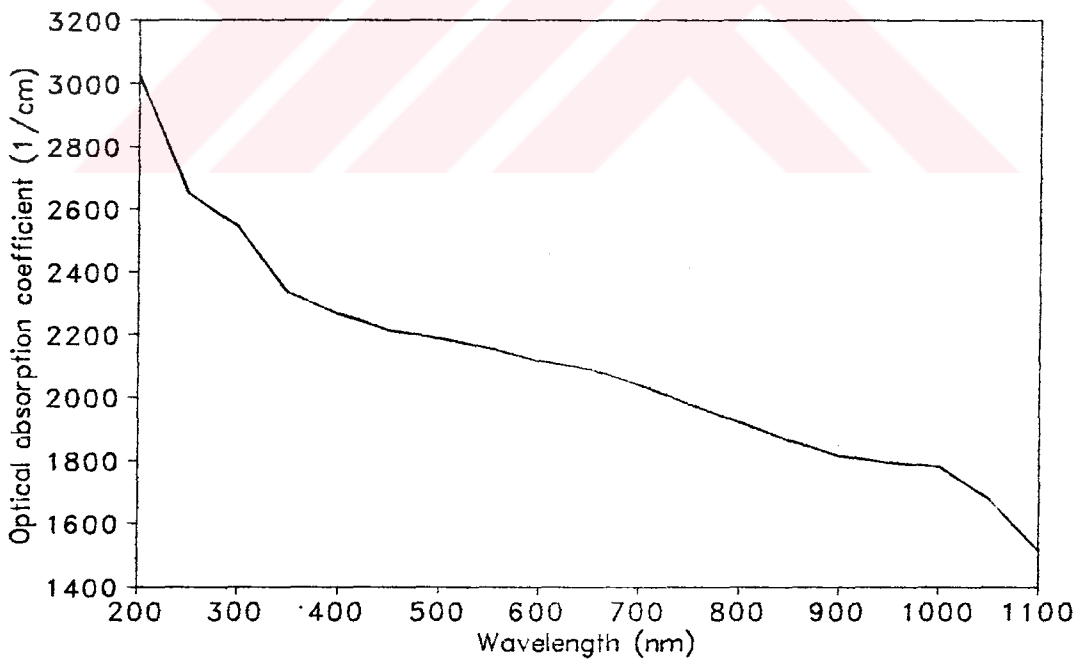


Figure 5.14 Optical absorption coefficient for silicon with different wavelengths.

where d is the optical path length of the sample.

Note that , there is negligible absorption at long wavelengths see Fig.5.15.

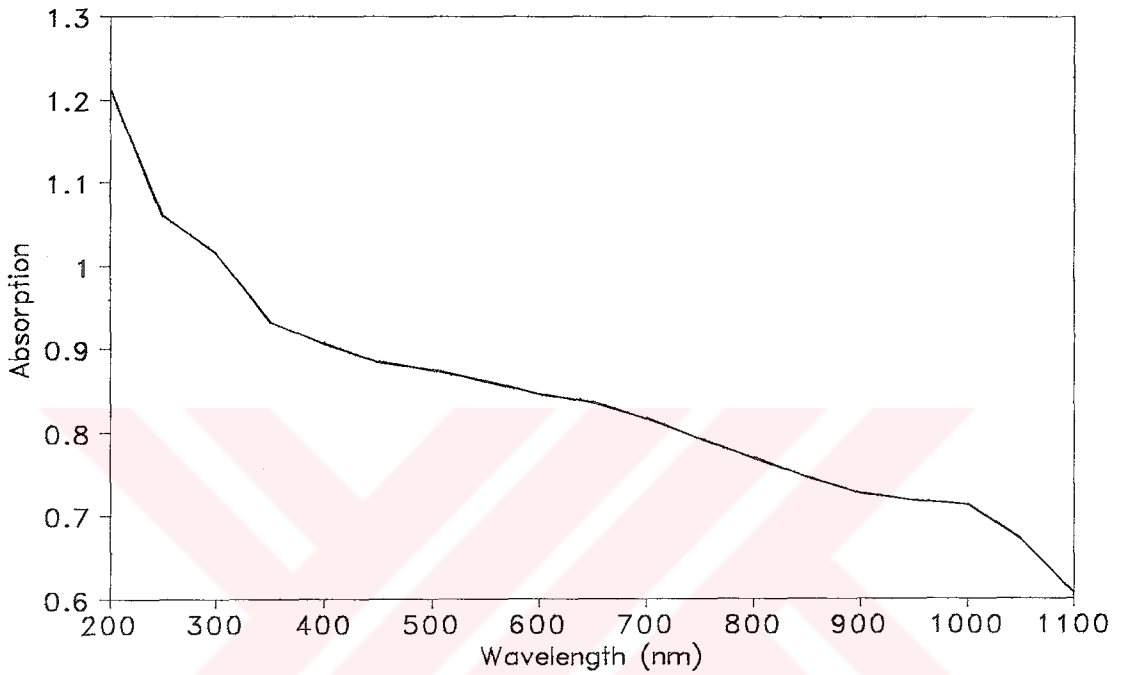


Figure 5.15 Absorption values of silicon for different wavelenghts.

Absorption coefficient α can be also found fom the transmission values. For that reason,the transmission values (F/F_{ph}) corresponding to different wavelengths as shown Fig 5.16 are found for sample by using the Spectrophotometer. Then the absorption coefficients α of sample corresponding to different wavelengths are calculated by substituting the thickness of sample and transmission values (F/F_{ph}), in the equation

$$\alpha = \frac{1}{d}\ln\frac{F_{ph}}{F} \qquad (5.8)$$

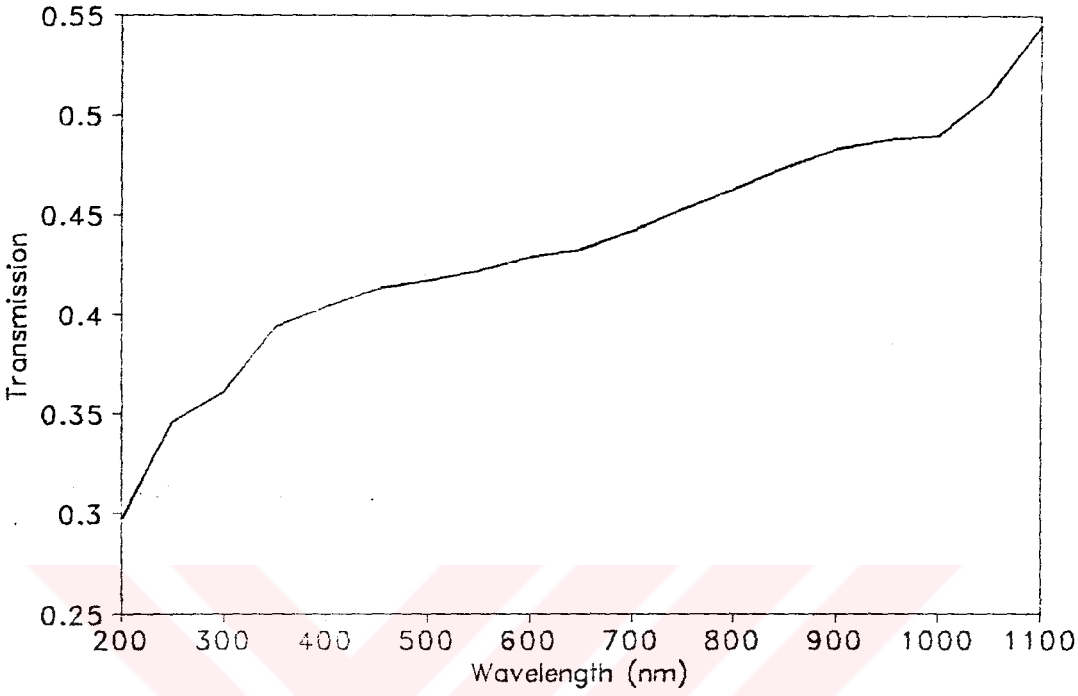


Figure 5.16 Transmission values of silicon for different wavelenghts.

From Fig.5.15 ,it is apperant that a photon with energy $hv > E_g$ can be absorbed in a semiconductor. Since the valence band contains many electrons and conduction band has many empty states into which the electrons may be excited, the probability of the photon absorption is high.

A photon with energy less than E_g is unable to excite an electron from the valence band to the conduction band. Thus in a pure semiconductor, there is negligible absorption of photons with $hv < E_g$. One exception to this rule is that a small amount of absorption can occur within a given band (free carrier absorption); for example, a low-energy photon can excite a conduction band electron temporarily to higher state within the conduction band. No excess carriers are created in this process. This

compenent of absorption is usually negligible compared with band-to-band excitation (intrinsic absorption) by photons of higher energy and most photons with $h\nu < E_g$ are transmitted through the material as seen Fig.5.16. This explains why some materials are transparent in certain wavelength ranges.

5.7 Determination of Quantum Efficiency of MOS Cells

The quantum efficiency η_q of the samples depending on the wavelength of the photons are determined from the measured values of the photocurrent I_p. To measure the potocurrents, an experimental set-up is established as shown in Fig.5.17 .

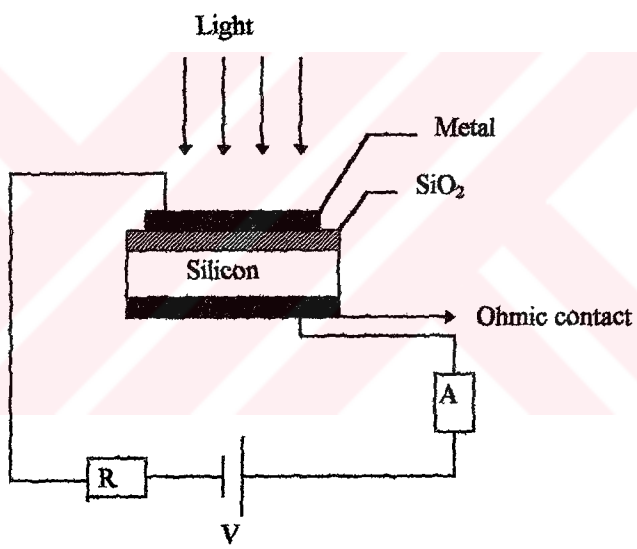


Figure 5.17 Measurement of photocurrent.

A DC power supply is connected in series with a standard resistor R (more high). R was not connected because of the photocurrent and photovoltage of cells are very small. **Measurement procedure as follows**; power supply is adjusted zero and the sample is illuminated with a Spectrophotometer with different wavelengths, at the same time the photocurrents corresponding to these wavelengths are measured. Similar measurements are carried out for the different voltages. But we measured only zero voltage. The quantum efficiency of the sample is determined substituting the measured values of I_p in the following equation;

$$\eta_q = \frac{I_p}{q}\frac{h\nu}{P_{opt}} \tag{5.9}$$

where P_{opt} is the optical power at wavelength λ (corresponding to a photon energy hv) and q is the electron charge.

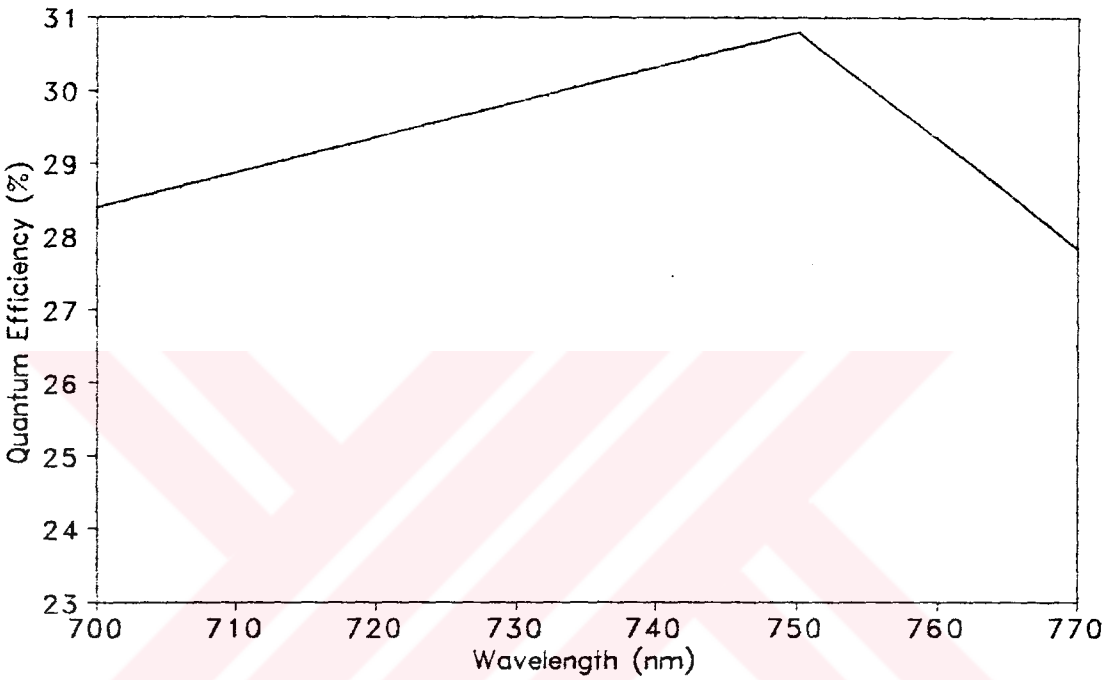


Figure 5.18 Quantum efficiency of MOS cell with different wavelenghts.

The quantum efficiency of sample according to wavelength as seen Fig.5.18 was calculated by substituting the values of the light falling onto sample (P_{opt}) obtained from the equation 5.9. The curve reach a maximum at 750 nm. This is the expected result because a semiconductor absorbs photons with energies equal to the band gap, or larger. It is known that silicon absorbs photons with wavelenght is less than or equal to 1.1μm.

5.8 Determination of Photocurrent and Photovoltage

Potocurrent of sample at the same time the resistance is measured using Fig.5.17 with corresponding wavelengths. Then using equation $V = I_p * R$, photovoltage values are calculated.

Photoresistance as shown Fig.5.19 for longer and lower wavelenghts increases and it is minimum at 650 nm.

Photocurrent and photovoltages are become maximum at the same wavelength as shown Fig.5.20 and Fig.5.21 and also efficiency of the sample is high at this point see Fig.5.18.

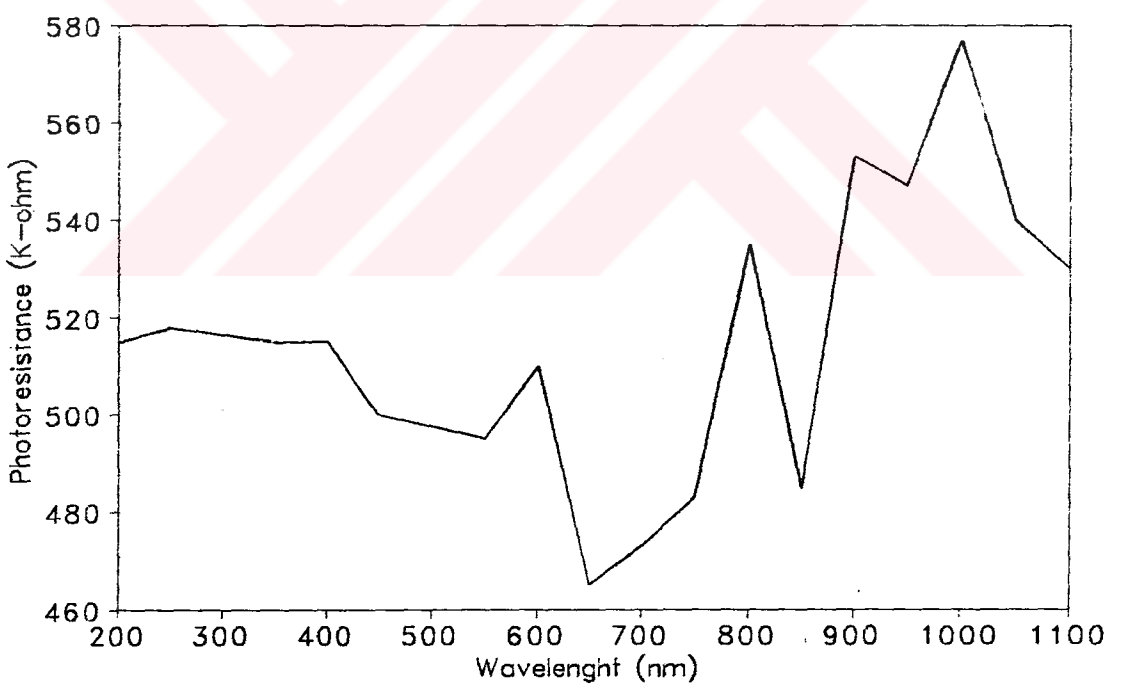


Figure 5.19 Photoresistance of MOS cell with different wavelenghts.

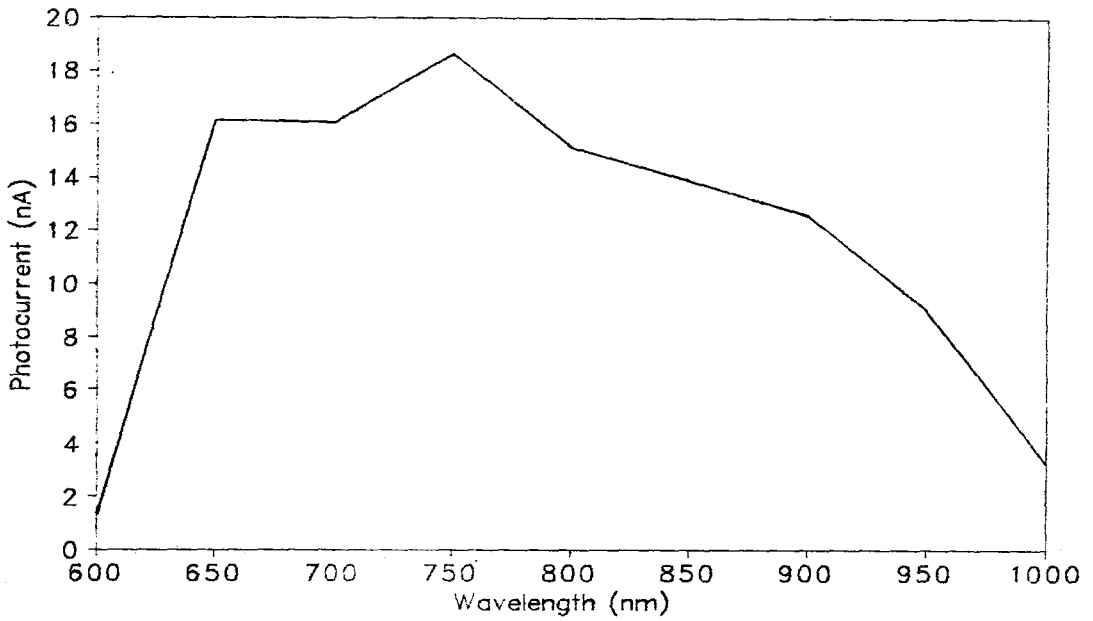


Figure 5.20 Photocurrent of MOS cell with different wavelenghts.

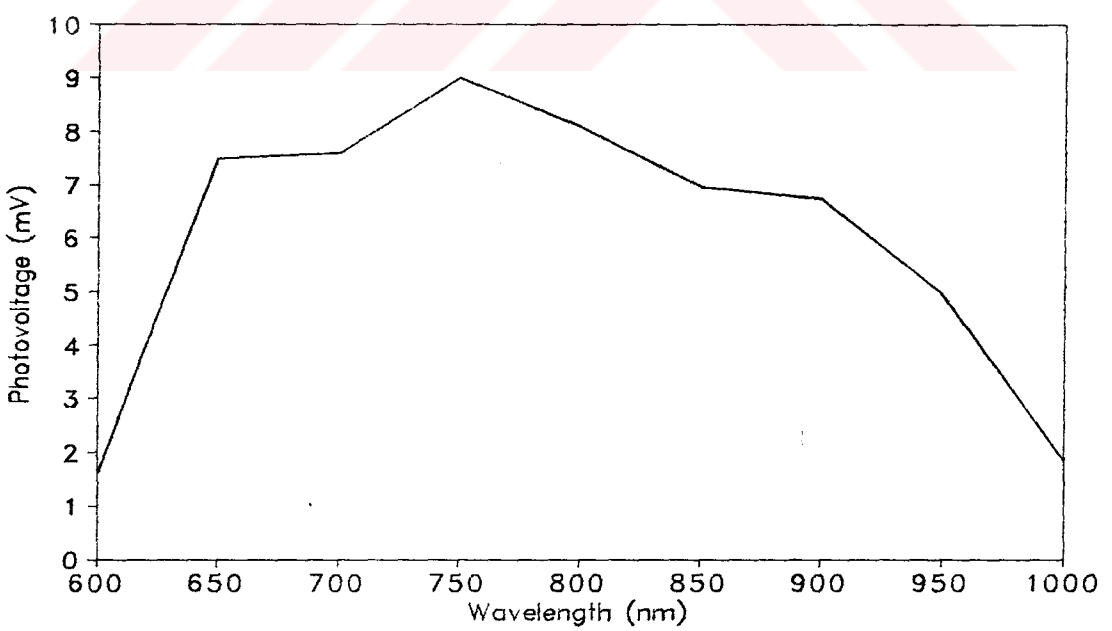


Figure 5.21 Photovoltage of MOS cell with different wavelenghts.

CHAPTER 6

CONCLUSION

Solar cells were produced by creating naturel oxide layer on p-type silicon and depositing Aluminum metal contacts by vacuum evaporation technique.

Minority carrier (Al-SiO_2 - p- Si) solar cell has a inversion or depletion layer at the thermal equilibrium. This is a consequence of the fixed positive charge in the oxide layer associated with the excess Si. These positive charges repel majority carriers (holes) from the surface layer of the semiconductor and attract electrons to the surface and the band center falls below the Fermi level. This accumulation of electrons acts like an n- type surface layer on the p-type substrate and number of minority carriers (electrons) are more than majority carriers in p-type silicon. Briefly, the p-type substrate in the absence of any applied gate voltage normally contains an electron inversion layer.

Positive charges in the oxide layer of Majority carrier (Au-SiO_2- n-Si) attract the majority carriers (electrons) in the n-type silicon and accumulation of electrons exists at the surface of the semiconductor. In this case, depletion layer that forms depends only on the difference between the work functions of the metal and the semiconductor and consequently the barrier height of Majority carrier solar cells is less than the Minority carrier solar cells. This situation reduces the open-circuit voltage of majority carrier solar cells so that p-type silicon is used for MOS cells design.

In theorical analysis, positive charges and surface states enhance the open-circuit voltage and reduce the dark saturation current at zero bias. In addition surface states act as recombination-generation centers and provide additional tunnelling paths between the metal and semiconductor. Thus,

short- circuit current is affected by surface charges and it also depends on the material parameters such as diffusion length, minority carrier life time which are metnioned in section 4.8. These parameters vary with silicon substrate resistivity. Capacitance of solar cell is also affected from surface state charges.

Altough the physical origin of surface states and insulator charge is still not completely understood, surface states occur due to lattice imperfections, absorbed and adsorbed impurity atoms, and oxide layer. The surface states (traps) can have acceptor-type charges or donor-type charges. For Minority carrier MOS solar cell, donor type surface states would be advantageous to improve open-circuit voltage which indicates high barrier height.

Resistivity of the silicon substrate affects the efficiency. Silicon which has low resistivity (high doping density) gives high short-circuit current with increasing efficiency compared to silicon that has high resistivity (fabricated with the same procedure), in this work.

Efficiency of solar cells is affected by many factors which decrease conversion efficiency. These are;

1) Aluminum is well known for its high reflectivity in the optical spectrum. Early works on this subject show that at 100 A° thickness Aluminum layer only 18-20 % transmittance can be expected. Thus for efficient light conversion with these cells, antireflection (AR) coating is used to maximize the transmittance. But in this work AR coating is not used. The evaporated SiO not only acts as an antireflecting coating but also tends to induce an inversion layer in the silicon underneath. This inversion layer improves the efficiency for generated of minority carriers, not only providing a low resistance path for these carriers along the surface but also by ensuring that surface states are heavily occupied by these carriers reducing their effectiveness as recombination centers. Literature on AR coating is extensive but no single technology has emerged as prefable data.

2) Determination of oxide thickness from the graph given in Figure 5.5 without using ellipsometry would not give an accurate thickness of oxide layer. The oxide thickness would be greater than as it is assumed. During oxidation of the silicon surface at room temperature in air, contaminations would be also grow on silicon surface. This also lowers efficiency.

3) Ohmic losses due to preparation methods.

4) Using lamps with very low illumination.

In micro electronic device technology, the working enviroment must be very clean to avoid contaminations that affect the stability of dsevice and photovoltaic response.

we did not take measurement results (I-V, C-V and Q-λ) at cryogenic temperatures, because cryostat was not run. Therefore, we tried to measure some parameters explained in last chapter by Spectrophotometer.

Since Spectrophotometer has a low intensity (10 W), photocurrent and photovoltage of cell showed low values as seen Fig.5.19 and Fig.5.20 during experimental work.

Using these experiment results, we do not find the fill factor (FF), I_m and V_m at a constant wavelength.

Effects of Aluminum and oxide thickness on cells were not observed.

In these experimental works, photons of selected wavelengths are directed at the sample and the relative transmission of the various photons is observed. Photons with energies greater than the band gap energy are absorbed while photons with energies less the than band gap are transmitted.

Quantum efficiency of cells are found very low in these works.

The energy band gap of cell and energy levels of sensitizing centers in the forbidden gap were determined by using spectrophotometer.

REFERENCES

1. Sze, S.M., 1981. " Physics of Semiconductor Devices ", John Wiley and Sons.

2. Richman, P., 1973. " MOS Field-Effect Transistors and Integrated Circui ", John Wiley and Sons.

3. Pulfrey, D.L., 1978. " Photovoltaic Power Generation ", Van Nostrand Reinhold (VNR).

4. Colliver, D.J., " Compound Semiconductor Technology ",Artech House.

5. Pulfrey, D., L. and Tarr, N., G., 1989. " Introduction to Microelectronic Devices", Prentice-Hall.

6. Wolf, H., F., 1971. " Semiconductors", John Wiley and Sons.

7. Muller, R., S., and Kamins, T., I., 1977. " Device Electronics for Integrated Circuits ", John Wiley and Sons.

8. Roberts, G., G., and Morant, M., J., 1979. " Insulating Films on Semiconductors ", Conference series number 50.

9. Gise, P., and Blanchard, R., 1986. " Modern Semiconductor Fabrication Technology ", Prentice- Hall.

10. Morgan, D., V., and Board, K., 1983. " An Introduction to Semiconductor Microtechnology ", John Wiley and Sons.

11. Zemel, N., J., 1979. " Nondestructive Evaluation of Semiconductor Materials and Devices " , Plenum Press.

12. Yang, E., S., 1988. " Microelectronic Devices ", Mcgraw-Hill.

13. Parker, G., 1994. " Introductory Semiconductor Device Physics ", Prentice-Hall.

14. Rouschenbach, H., S., " The Principles and Technology of Photovoltaic Energy Conversion ".

15. Bauza, D., 1994. " Detection of Slow Traps in the Oxide of MOS Transistors by a new current DLTS Technique ", Electronic Letters Vol.30, No.6, pp.484-485.

16. Chopra, K., L. and Das, S., R., " Thin Film Solar Cell " .

17. Wang, K., L., 1979. " A Determination of Interface State Energy During the Capture of electrons and Holes using DLTS ", IEEE Trans. on Electron Devices, Vol.ED.26, No.5, pp. 818-821.

18. Grossman, M., 1976. " Technician's Guide to Solid-State Electronics".

19. Pulfrey, D., L., 1978. " MIS Solar Cells ", IEEE Trans. on Electron Devices ,Vol. ED.25, No.11, pp. 1308-1317.

20. Özdemir, S. and Buket, U., 1987. " Temperature Dependence of Dark and Illuminated Current- Voltage Characteristics of Gating-Type min MIS Silicon Solar Cells ", Solar Cells, Vol.20, pp. 81-89.

21. Shewchun, J., Burk, D., and Spitzer, M., B., 1980. " MIS and SIS Solar Cells ", IEEE. Trans. on Electreon Devices ", Vol.ED.27, no.14, pp. 705-715.

22. Hall, R., N., 1981. " Silicon Photovoltaic Cells ", Solid-State Electronics, Vol.24, pp. 596-616.

23. Tütüncüler, H., 1994. " Desing and Fabrication of MOS Solar Cells ", M.S.Thesis.

24. Soydan, Ü., 1989. " Desing and Construction of Pulse Generation and Signal Processing Unit for Deep Level Transient Spectroscopy Studies ", M.S. Thesis.

25. Kutlar, A., Z., 1994. " Desing of a Computer Controlled Testing System for Semiconductor Devices ", M.S. Thesis.

26. Milnes, A., G., 1973. " Deep Impurities in Semiconductors ", John Wiley and Sons.

27. Ankrum, P., D., " Semiconductor Electronic ".

28. Marfaing, Y., Lascaray, J. and Triboulet, R., 1974. " Study of Deep and Shallow Levels by Photocapacitance in Au-n CdTe Schottky Barriers", Institude of Physisc Conf. , ser. No.22, pp. 201- 209.

29. Glover, G., H., 1972. " Determination of Deep Levels in Semiconductors from C-V measurement ", IEEE Trans. on Electron Devices ,Vol.ED.19, No.2, pp. 138-143.

30. Morris, M., N., 1976. " Semiconductor Devices " .

31. Card, H., C. and Rhoderick, E., H., 1971. " Studies of Tunnel MOS Diodes Interface Effects in Silicon Schottky Diodes ", J. Appl. Phys. , Vol.14, pp. 1589-1601.

32. Green, M., A., King, F., D. and Shewchun, J., 1974. " Minority Carrier MIS Tunnel Diodes and their Application electron and Photovoltaic Energy Conversion ", Sold-State Electron Vol.17, pp. 551-561.

33. Kingston, R., H. and Neustadter, S., F., 1955. J. Appl. Phys. , Vol.26, 718.

34. Schockley, W. and Read, W., T., 1972. Jr. Physç Rev. , Vol.87, 835.

35. King, K. and Card, H., C., 1980. " A comparision of Majority and Minority Carrier Silicon MIS Solar Cells ", IEEE Trans. of Electron Devices , Vol.27, No.4, pp. 716-723.

36. Nicolian, E., H. and Brews, J., R., 1982. " MOS Physics and Technology ", A Wiley-Interscience Publ.

37. Shewchun, J., Singh, R. and Green, M., A., 1977. " Theory of Metal-Insulator- Semiconductor Solar Cells ", J. of Appl. Phys. Vol.48,No.2, pp. 765-770.

38. Green, M., A. and Godfrey, R., B., 1976. " MIS Solar Cell - General theory and new experimental results for silicon ", Appl. Phys. Lettr. , Vol.29, No.9, pp. 610-612.

39. Fonash, S., J., 1975. J. Appl. Pysc. , Vol.46, p.1286.

40. Anderson, W., A., Vemon, S., M., Delahay A., E., Ng, K., K., Mathe, P. and Poon, T., 1975. International Electron Devices, p.217. (Unpublished)

41. Stim, R., J. and Yeh, Y., C., M., 1975. Appl. Phys. Lett. , Vol.27, p.95.

42. Charlson, E., J. and Lien, J., C., 1975. " An Al p-silicon MOS photovoltaic cell ", J. Appl. Phys., Vol.46,No.9.

43. Shevenock, S., Fonash, S. and Geneezko, J.,1975. International Electron Devices Meeting, Washington, D.C. 1975, pp.211. (Unpublished)

44. Peckerar, M., Lin, H., C. and Kocker, 1975. International Electron Devices Meeting ,Washington, D.C.1975, p.213. (Unpublished)

45. Lillington, D., R. and Townsend, W., G., 1976. Appl. Phys. Lett. , Vol.28, p.97.

46. Kipperman, A., H., M. and Omar, M., H., 1976. Appl. Phys. Lett. , Vol.28, p.620.

47. Shewchun, J., Singh, R., Pierre, J., St. and Loferski Proe, J., J.,1976. Nationalworkshop on Low Cost Polycristalline Silicon Solar Cells , SMU, Dallas Texas. (Unpublished)

48. Wood, D., 1994. " Optoelectronic Semiconductor Devices ", Prentice- Hall.

49. Cobbold, R., S., C., 1970. " Theory and Applications of Field - Effect Transistors ", Wiley - Interscience.

50. Muller, R., S. and Kamins, T., I., 1977. "Device Electronics for Integrated Circuits ", John Wiley and Sons.

51. Godfrey, R.B., and Green, M.A.,1978. " A 15 % eficient silicon MIS solar cell ", Appl.Phys. Lettr. ,Vol.33, No.7, pp. 636-639.

52. Godfrey, R.B., and Green, M.A.,1979. " 655 mv open-circuit voltage, 17.6 % efficient silicon MOS solar cell ", Appl.Phys. Lettr. , Vol.34, No.11 , pp.790-793.

53. Fabre, E., 1976. " MIS silicon solar cells ", Appl.Phys. Lettr. ,Vol.29, No.9, pp.607-609.

54. Green, A.M., and Godfrey, R.B., 1976. " MIS solar cell - General theory and new experimental results for silicon ", Appl.Phys.Lettr. Vol.29, No.9, pp.610-612.

55. Hall, R.N., 1981. " Silicon Photovoltaic Cells ", Solid-State Electronics, Vol.24, pp. 595-616.

56 Godfrey, R.B., and Green, A.M., " High-Efficiency Silicon MinMIS Solar Cells-Desing and Experimental Results", IEEE Transactions Electron Devices , Vol.ED.27, No.4, pp. 739-745.

57. Pulfrey, D.L., 1976. " IEEE Transactions on Electron Devices ", pp. 587- 589.

58. Tarr, N.G., and Pulfrey, D.L., 1979. " New experimental evidence for minority -carrier MIS diodes ", Apply. phys. Lettr. ,Vol.34, No.4, pp. 295-297.