DESIGN OF BLOCKS FOR AN ULTRA WIDEBAND TRANSCEIVER

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ABSTRACT

DESIGN OF BLOCKS FOR AN ULTRA WIDEBAND TRANSCEIVER

Ultra wideband (UWB) is one of the strongest technologies for short-range high data rate and longer range low data rate communications. Wireless personal area networks are one example of the first group while wireless sensor networks are considered as one of the second. UWB has not only various advantages and potentials such as low cost circuitry, precise ranging capability, etc. but also has its own challenges. Thus, in the literature, there is a lot of work which uses some of these advantages and tries to find solutions for the challenges and problems with different circuit architectures.

The goal of this dissertation is to design a high data rate UWB transceiver. Designing a high data rate low power transmitter was the main focus of this thesis during this design process while the design of the receiver part was accomplished by project team. Various transceiver structures, modulation techniques, communication approaches, pulse shapes and circuits are reviewed in terms of performances, spectral characteristics, hardware complexities, and data rates. At the end of this review, an energy detection non-coherent impulse radio (IR) UWB system is chosen. Blocks of this system are initially realized using a hardware description language. After simulations of the system two different pulse generator topologies are examined in detail and compared. Consequently, a new one is designed which has a data rate up to 1 Gbps and respectively consumes relatively low power.

Simulations of the transmitter and the receiver are performed simultaneously. Thus, some adjustments can be done on the transmitter according to the simulation results of the receiver or vice versa. Besides, corner simulations are taken into consideration during design period of the pulse generator. In the literature, many of

the studies do not include corner case simulations hence, it can be said that most of the circuits proposed in these papers cannot endure the problems formed as a result of the variations arise during manufacturing process.

In the last phase of the transceiver design process, layouts of all circuits are drawn with UMC’s 130 nm complementary metal oxide semiconductor (CMOS) technology.

ÖZET

ULTRA GENİŞBAND ALICI-VERİCİ BLOK TASARIMLARI

Ultra genişband (UGB) kısa mesafe yüksek veri hızı ve uzun mesafe düşük veri hızı iletişim şekilleri için en güçlü teknolojilerden bir tanesidir. Kablosuz kişisel alan ağları bu ilk gruba dahil edilebilirken kablosuz algılayıcı ağları ise ikinci grup içerisinde bulunur. UGB sadece devreyi ucuza gerçekleştirebilme, hassas mesafe ölçümü, vb. avantajlara ve bunların getirdiği çeşitli potansiyel uygulama alanlarına sahip olmayıp yanında kendine has çeşitli zorluklara da sahiptir. Bu nedenle, literatürde bu avantajların bir kısmını kullanan ve UGB teknolojisinin sorun ve zorluklarına çeşitli devre ve uygulamalarla çözüm bulmaya çalışan birçok makaleye rastlanılabilir.

Bu yüksek lisans tezinin amacı yüksek veri hızlarında çalışabilen bir UGB alıcı-verici devresi tasarlamaktır. Verici kısmı bu tezin ana tasarım amacını oluştururken alıcı kısmı proje takımının ortak çalışması sonucunda tasarlanmıştır. Düşük güç tüketen ve yüksek hızlı veri transferi gerçekleştirebilen bir verici devresinin tasarlanması ise bu tezin üzerinde asıl olarak odaklandığı konudur. Çeşitli alıcı-verici yapıları, kipleme teknikleri, iletişim biçimleri, darbe şekilleri ve devreler performans, spektral karakteristikler, donanım karmaşıklıkları ve veri hızlarına göre incelenmişlerdir. Bu inceleme sonucunda enerji saptamalı bir uyumsuz dürtü radyo UGB sistemi seçilmiştir. Bu sistemin blokları öncelikle bir donanım tanımlama dili ile gerçeklenmiştir. Yapılan benzeşimlerden sonra iki farklı darbe üreteci detaylı olarak incelenip karşılaştırılmıştır. Bu yapılanlar sonucunda veri hızı 1 Gb/s'ye kadar çıkabilen ve nispeten düşük güç tüketen yeni bir darbe üreteci tasarlanmıştır.

Alıcı ve verici blokların benzeşimleri aynı zamanlarda yapılmıştır. Bu sayede, alıcı benzeşim sonuçlarına göre verici kısmında, verici benzeşim sonuçlarına göre ise alıcı kısmında düzeltmeler yapma imkânı olmuştur. Tüm bunlara ek olarak, köşe

durumu benzeşim sonuçları da özellikle darbe üreteci için olmakla birlikte bütün sistemin tasarlanması esnasında dikkate alınmıştır. Literatürde bulunan çalışmaların birçoğu köşe durumu benzeşimlerinin dikkate alındığına dair bilgi içermemektedir. Buradan yola çıkarak bu çalışmalarda verilen devrelerin bir kısmının üretim esnasında devrelerde ortaya çıkan değişimlerin oluşturacağı problemlere karşı koyamayacağı söylenebilir.

Alıcı-verici devresi tasarım sürecinin en son bölümünde ise United Microelectronics firmasının 130 nanometre bütünleyici metal oksit yarıiletken teknolojisi kullanılarak bütün devrelerin serimi çizilmiştir.

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LIST OF SYMBOLS/ABBREVATIONS

CMOS	Complementary Metal-Oxide Semiconductor
DS	Direct Sequence
ED	Energy Detection
EIRP	Equivalent Isotropically Radiated Power
FB	Fractional Bandwidth
FCC	Federal Communication Commission
FF	Fast NMOS-Fast PMOS Corner
FS	Fast NMOS-Slow PMOS Corner
IR	Impulse Radio
NF	Noise Figure
OFDM	Orthogonal Frequency Division Multiplexing
PSD	Power Spectral Density
Q	Quality Factor
SF	Slow NMOS-Fast PMOS Corner
SNR	Signal to Noise Ratio
SS	Slow NMOS-Slow PMOS Corner
TH	Time Hopping
TT	Typical NMOS-Typical PMOS Corner
UMC	United Microelectronics Corporation
UWB	Ultra Wideband
VHDL-AMS	Very High Speed Integrated Circuit Hardware Description Language-Analog Mixed Signal

E	Instantaneous energy of the waveform
f_C	Center of the energy bandwidth
f_H	Higher limit of the energy bandwidth
f_L	Lower limit of the energy bandwidth
f_M	Frequency of the highest emission
σ	Pulse shape parameter

1. INTRODUCTION

The last decade has witnessed a tremendous growth in wireless technologies. The aim of new generation wireless mobile radio systems is to provide a wide variety of applications for as many users as possible with the possibility of flexible data transmission rates (high, medium and low data rates). Nevertheless, these goals must be achieved under the constraint of limited spectrum and power resources. In the future, more and more devices will be added to the wireless world and thus, communication technologies will face spectral crowding. Therefore, coexistence of wireless devices will be a growing and major issue.

According to the modern definition, any wireless communication technology that produces signals with a bandwidth wider than 500 MHz or a fractional bandwidth[1] greater than 0.2 can be considered as ultra wideband (UWB). UWB is an unlicensed system which coexists with other licensed and unlicensed narrowband systems. According to this situation, a few regulatory agencies are set up to control the transmitted power of UWB. It means that an UWB system can only be allowed to coexist with other technologies under very strict power constraints. In spite of all these strict rules, UWB technology offers attractive solutions for wireless personal area networks (WPANs), wireless telemetry and telemedicine and wireless sensor networks. In addition, UWB systems are able to provide much higher capacity than the current short-range narrowband systems.

UWB systems have some application areas such as wireless communications, radar imaging and vehicular radar applications. Material penetration capabilities of its signals allows us to use them for radar imaging systems (including ground penetration radars), wall radar imaging, through wall radar imaging, surveillance systems and medical imaging. Images of the inside of an object or behind of an object can be obtained with high resolution by using UWB. Likewise, accurate ranging capability, due to the excellent time resolution property, can be used for vehicular radars to avoid accidents, parking guide systems, etc. Communication may be the most important application area of UWB and it

[1] The bandwidth of a device divided by its center frequency.

can be said that this is the reason why UWB takes attention of the wireless world which consists of wireless home networking, UWB wireless mouse, keyboard, wireless speakers, wireless sensor networks, wireless telemetry and telemedicine.

Many researchers are trying to develop UWB transceiver systems to decrease hardware complexity, production cost and power consumption while working for increasing data rate. In some papers completely novel structures are proposed to achieve formerly written goals. Some others present modified versions of existing transceivers. These modifications are done by developing one or few of the blocks that form the transceiver.

Aim of this thesis is to design a high data rate UWB transceiver. During the design process, pulse generator is the mainly focused block for increasing data rate of the transmitter. Power budget of the transceiver is also taken into consideration. Structures of the transceiver and pulse generator are chosen as candidates according to a literature survey.

During the dissertation study, firstly, an ideal model of the transceiver was written with a hardware description language and tested to be able to extract some specifications of it. Eventually, two distinct pulse generator topologies were decided for transistor level test phase to form the transmitter. In addition, circuits that form the receiver were determined simultaneously.

In transistor level test phase, advantages and disadvantages of the chosen pulse generator topologies were observed. Problems of these circuits were tried to be corrected nevertheless, results obtained from the simulations were not satisfactory for the transceiver selected. Thus, a new pulse generator was required and designed with the help of simulation results of the former ones.

Layout drawing was the phase that comes after the transistor level design and simulations of circuits. According to some common layout rules, they were drawn separately. Layout simulations were also done to be sure that the circuits are operating as

expected. All circuits were integrated into one chip which covers an area of 2.325 mm^2 at the end of the transceiver design process.

In section 2, brief information about UWB technology and its history is given with regulations, advantages and challenges of it. In section 3, two different approaches used in UWB communication is examined and some details about them are presented. Section 4 includes detailed information about the pulse shapes employed in UWB. Modulation types commonly used in UWB communication approaches are also presented in this section. In section 5, very general information about a hardware description language is given. Also, model blocks of the transmitter and receiver written with that language is presented with the simulation results of these models. Transistor level design of the circuitry, basic definitions and simulation results can be seen in section 6. Section 7 includes detailed information about three distinct pulse generator topologies last of which is a new structure designed during this project. Their advantages and drawbacks are also given in this section with the simulation results obtained. Section 8 gives the layouts of the blocks that form the transceiver and their simulation results while section 9 concludes this thesis.

2. ULTRA-WIDEBAND (UWB)

2.1. History

UWB is an unconventional type of radio. Radio is the process of sending and receiving electromagnetic signals between transmitters and receivers wirelessly. In radio technology, the information is sent through transmitters as electromagnetic signals and which is translated into original information by receivers. Transmitters encode or modulate the given information on some signal with some techniques. Then, receivers recover the information that is sent through transmitters by decoding or demodulating and present it to the user as received information.

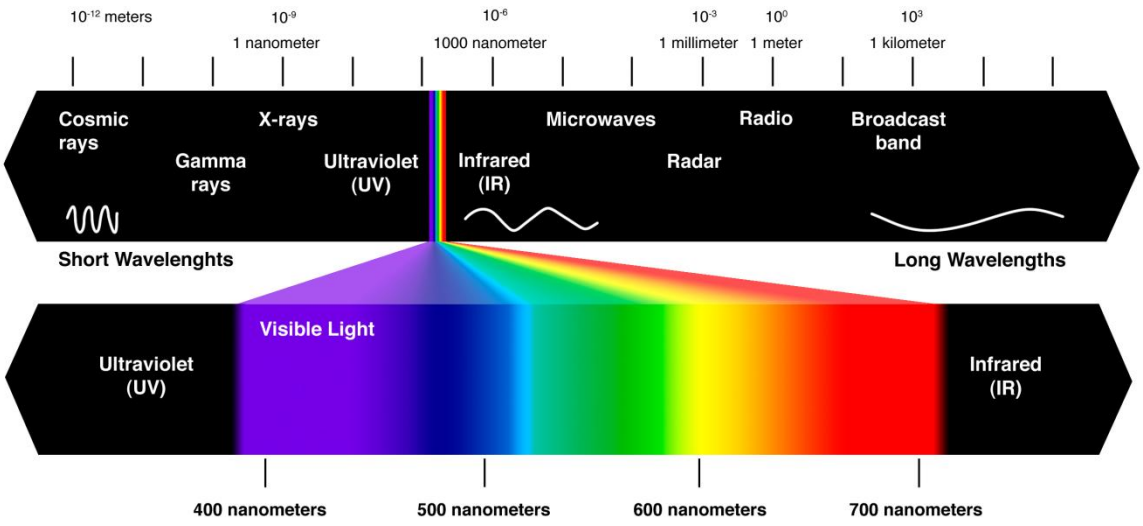


Figure 2.1. Electromagnetic spectrum [1]

Signals, which can be called as electromagnetic energy bearing information, surround people. They have various sources such as; AM (Amplitude Modulation) or FM (Frequency Modulation) band radio stations, television stations, distinct consumer devices, etc. All these signals written above and others share the same transmission medium (the near vacuum of space, the air and the many materials surrounding us) at the same time. In spite of this situation, the desired signal can be chosen among all these signals such as the

radio station we want to listen. In Figure 2.1, all these signal types and their frequency bands in the electromagnetic spectrum can be seen.

Conventional radio signals can be distinguished from each other since different types of signals occupy unique locations in the spectrum. Radio signals share the same limited spectrum by occupying slices of spectrum that are as narrow as possible. A signal without information has zero bandwidth. Modulating information on that signal spreads its bandwidth in proportion to the information bandwidth.

Separation of signals by bands, by channels and by frequencies is not the only way to share the radio spectrum. Information bearing signals can also be separated in time, especially in tiny slices of time. These signals occupy wide bandwidths, ultra-wide bandwidths but short and ultra short slices of time. The tinier the sliver of time, the wider is the bandwidth of the signal in the radio spectrum [2]. Additionally, the entire spectrum can also be used by multiple users. The users are separated in time rather than in frequency. UWB radio tends to separate users in time, while occupying a large segment of the electromagnetic spectrum simultaneously.

In summary, there are two techniques of sharing the spectrum among many users. The spectrum can be divided in frequency and each user is assigned to a small part of the spectrum. On the other hand, many users can occupy the whole spectrum however, each can do it for a short sliver of time.

In the past, Morse code signaling was the base of wireless communication in which the information was coded by hand and decoded by ear. Morse code is composed of combinations of dots and dashes that represents alphabetic characters and coding process was formed by keying a carrier signal on and off in various combinations. With this communication technique, a moderate messaging rate was about 25 words per minute (20 bps in today measure). In short, early wireless signals had relatively small bandwidths, 10’s of Hertz however, the primitive transmitting apparatus of those days emitted very wideband signals, about 100’s of kilohertz wide. As a result of this discrepancy, transmitted signals occupied much more spectrum than the required one. Consequently,

receivers collected lots of background noise with the information that must be received which means the signal-to-noise ratio (SNR) of the receivers was poor. Therefore, they could only hear the strongest signals. All these problems made narrowband signals a requirement for wireless communication.

By 1905, Reginald Fessenden found a new way to change the amplitude of the wireless signal in step with audio amplitude variations and with this technique audio signals could be sent directly on the carrier. As a result, AM was born. However, AM brought us a new problem. Any other natural amplitude variations, such as amplitude noise, static and lightning crashes, would add to the desired amplitude modulated information and be perceived as noise and distortion [2]. Approximately 30 years later, Edwin Armstrong discovered the FM technique. In FM, the frequency of the transmitter carrier was varied in proportion to the amplitude of the signal instead of the amplitude of the transmitter carrier. Additionally, Armstrong realized that FM signal did not need to have a narrow bandwidth. It could vary over a wide range and as a result have a better SNR than AM.

In those days, Federal Communication Commission (FCC[2]) preferred narrowband radios which concentrate all of their power in narrow channels in frequency spectrum. As a result of the increasing demand, the number of available channels became limited. Meanwhile, Claude Shannon offered a new paradigm in 1948 which says that under certain specific conditions, an information signal can be able to hold more information when it is spread in bandwidth like a background noise. Since, a spread signal in frequency band resembles noise to another signal that is similarly spread therefore, both can coexist. Under some specific conditions, signal energy can be detected more efficiently than noise energy. As a result, using a signal that has a low power density over a wide bandwidth during transmission was found as an alternative way to transmitting a signal with a high power density in a narrow band was found. This observation of Shannon's led to *spread-spectrum* modulation in which the signals are using special code families. Special digital codes are

[2] Prior to 1912, radio was largely the domain of amateur experimenters and ship-to-shore communications for naval and commercial operations. Interference was a serious problem. In the United States, the Radio Act of 23 July 1912 stepped in to mitigate the interference issue. The Radio Act of 1927 established the Federal Radio Commission (FRC) and the Communications Act of 1934 established the Federal Communications Commission (FCC) giving regulatory powers in both wire-line and radio-based communications [2].

used for discerning the simultaneous users of the same frequency band. The main advantage of UWB technology can be perceived from Shannon's link capacity formula [3]

$$C = B\log_2(SNR+1). \tag{2.1}$$

The link capacity is linearly proportional to the bandwidth and has a logarithmic relationship with the signal to noise ratio (SNR). So, very little amount of signal power is required to obtain high data rates when the bandwidth used is extremely large. Because of the large bandwidth of UWB applications, it gives the opportunity of giving much higher capacity than the present narrowband systems for short-range applications. With this development, the FCC had allocated a block of spectrum which is shared by multiple users who use overlapping signals across the entire band. This allocation type is used instead of allocating narrow slices of band for every user. This technique makes the use of spectrum much more efficient. Therefore, it can be said that the digital wireless era has begun.

Short-impulse signal transmission between antennas has attracted the attention of a small group of scientists. Impulses are short time signals leading to wider bandwidth and the experiments about impulse signal transmission led us to *impulse radio* which was called UWB radio later. By the late 1960s and 1970s, the benefits of wideband communications were being researched for nongovernment applications. The practicality of modern low-power impulse radio techniques was demonstrated in the late 1970s and 1980s by Fullerton who used a time-coded time-modulated approach. Later, some other scientists used UWB spread-spectrum impulse techniques for proving the benefits of modern low power impulse radio method.

2.1.1. Shannon's Theory

Shannon's capacity equation can be viewed as the best definitive equation of the benefits and possibilities of UWB for today. When the requirement for bit rates increases, capacity becomes more and more important for audio and video applications. As stated before, Shannon's equation is expressed as (2.1), where C is the maximum channel capacity in bps, B is the channel bandwidth in hertz, SNR is the signal to noise ratio. This

famous equation shows us that just three parameters exist to improve the capacity of the channel. A designer can increase the bandwidth, increase the signal power or decrease the noise. Shannon's equation also tells that more bandwidth means more channel capacity. In addition, the capacity can be increased with signal power however, only logarithmically. Moreover, UWB systems can trade off some of the bandwidth for reduced signal power and interference because of the abundance in its bandwidth. Therefore, UWB systems have a huge potential for wireless communications that need high capacity.

2.2. UWB Radio Definition

The radiation of waveforms is the basic part of UWB radio. These waveforms can be categorized by an instantaneous fractional energy bandwidth greater than about 0.20-0.25.

2.2.1. Fractional Bandwidth (FB)[3]

In order to understand the term FB, it is good to define the energy bandwidth of the waveform. For instance, E is assumed to be the instantaneous energy of the waveform, the energy bandwidth is identified by the frequencies f_L and f_H which are, relatively, the lower and upper limit of an interval that includes approximately %90 of E. The width of that interval is called as *energy bandwidth*.

E is indicated as an instantaneous energy that must be computed over an interval which corresponds to the duration of a pulse. If the decision concerning a single bit involves the processing of several pulses, as is usually the case, E refers to the overall energy of all the processed pulses engaged in the decision over one single bit [4]. In this concept, it is important to specify the energy of the group of pulses used in the decision of a single bit as, the effect noise at the receiver must be evaluated with respect to the energy of a well based definition of useful signal energy.

[3] A pulsed transmission scheme is considered during the definition of fractional bandwidth.

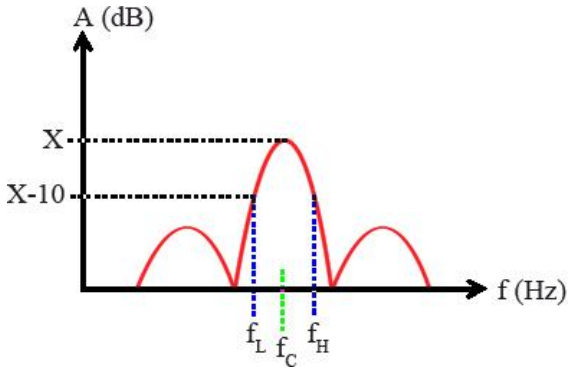


Figure 2.2. Energy bandwidth

The energy bandwidth concept can be seen in Figure 2.2. The center frequency of the spectrum is located at $(f_H + f_L) / 2$. The FB is the ratio of the energy bandwidth and the center frequency. The FB is expressed as:

$$FB = \frac{(f_H - f_L)}{\left(\frac{f_H + f_L}{2}\right)}. \tag{2.2}$$

As it is stated before if the fractional bandwidth is greater than 0.20-0.25, the signal can be called as UWB. From (2.2), it can be noted that the definition of an UWB signal can be given only relatively to the center frequency.

The term *percent bandwidth* which is simply the fractional bandwidth in percent units is also used generally. For instance, a signal with an energy bandwidth of 60 MHz and a center frequency of 80 MHz, it has a percent bandwidth of 75%. It is an UWB signal, since its FB is 0.75 which is higher than the limits. In addition, the term *relative bandwidth* is in use and it is equal to half of the value of the FB.

For the sake of clarity, the limits f_L and f_H shall be defined in less general terms. Distinct ways can be chosen to select these frequencies. However, the preferred way must depend on how stringent the requirement on the bandwidth used. In a recent release of UWB emission masks in the U.S. (FCC, 2002) f_L and f_H are set to the lower and upper bounds of the -10 dB emission points. It means, to assume a signal as an UWB signal, its

bandwidth at -10 dB emission points exceeds 500 MHz, regardless of the FB value. The 500 MHz minimum bandwidth limit sets a threshold at 2.5 GHz [4]. In spite of existing below threshold, a signal can also be called as UWB signal if its fractional bandwidth exceeds 0.20.

2.3. Regulations

After all these works, on 14 February 2002, the FCC set some ground rules in First Report and Order (R&O) for ultra-wideband operations. In short, the FCC gave permission to use a bandwidth of 7500 MHz, which lies between 3.1 and 10.6 GHz, unlicensed spectrum and it is available for commercial communications development in the United States.

The FCC ruling is very protective to sensitive systems like the Global Positioning System (GPS), aviation system and safety-of-life services. It allows UWB technology to exist with existing radio services without causing harmful interference. The *communications and measurement systems* category is of primary interest to commercial UWB radio technology.

Table 2.1. U.S. spectrum allocation for unlicensed use [5]

Unlicensed bands	Frequency of operation	Bandwidth
ISM at 2.4 GHz	2.4000 – 2.4835 GHz	83.5 MHz
U-NII at 5 GHz	5.15 – 5.35 GHz 5.75 – 5.85 GHz	300 MHz
UWB	3.1 – 10.6 GHz	7.5 GHz

UWB operation is defined as a transmission system having UWB transmitter and is defined in terms of the following [2]:

- UWB Bandwidth: the frequency band bounded by the points that are 10 dB below the highest radiated emission, as based on the complete transmission system including the antenna. The upper boundary is designated f_H and the lower boundary is

designated f_L. The frequency at which the highest radiated emission occurs is designated f_M.

- Center frequency:

$$f_C = (f_H + f_L)/2. \tag{2.3}$$

- Fractional bandwidth:

$$BW = 2(f_H - f_L)/(f_H + f_L). \tag{2.4}$$

- UWB transmitter is an intentional radiator that, at any point in time, has a fractional bandwidth FB $\geq$ 0.20 or has a UWB bandwidth $\geq$ 500 MHz, regardless of the fractional bandwidth.
- EIRP: Equivalent isotropically radiated power, that is, the product of the power supplied to the antenna and the antenna gain in a given direction relative to an isotropic antenna.

The first set of FCC key regulations for all UWB systems are as follows [6]:

- No toys and no operation on an aircraft, ship or satellite.
- Emissions from supporting digital circuitry are considered separately from the UWB portion, and are subject to existing regulations, not new UWB rules.
- The frequency of the highest emission, f_M, must be within the UWB bandwidth.
- Other emissions standards apply as cross-referenced in the UWB rules, such as conducted emissions into AC power lines.
- Emissions below 960 MHz are limited to the levels required for unintentional radiators.
- Within a 50 MHz bandwidth centered on f_M, peak emissions are limited to 0dBm EIRP.
- UWB radar, imaging and medical system operation must be coordinated. Dates and areas of operation must be reported, except in the case of emergency. These systems

must also have a manual switch (local or remote) to turn the equipment off within 10 seconds of actuation.

The regulations give permission to UWB systems and handheld devices. Indoor UWB devices must be designed for only indoor operations. The emissions from these devices shall not be used at or directed outside of the building. The bandwidth of UWB indoor devices must be limited between 3.1 and 10.6 GHz. The restrictions can be seen in Figure 2.3.

In Europe, the European Commission's (EC) Radio Spectrum Committee approved the use of UWB in December 2006. Based on the technical studies of European Conference of Postal and Telecommunications Administrations (CEPT) and the standard contributions of European Telecommunications Standards Institute (ETSI), EC finally identified the frequency bands 3.4 - 5 GHz and 6 - 8.5 GHz (with potential extension to 9 GHz) for UWB devices. In the other areas of the world, more and more countries are paving the way for new wireless products incorporating UWB technology [7].

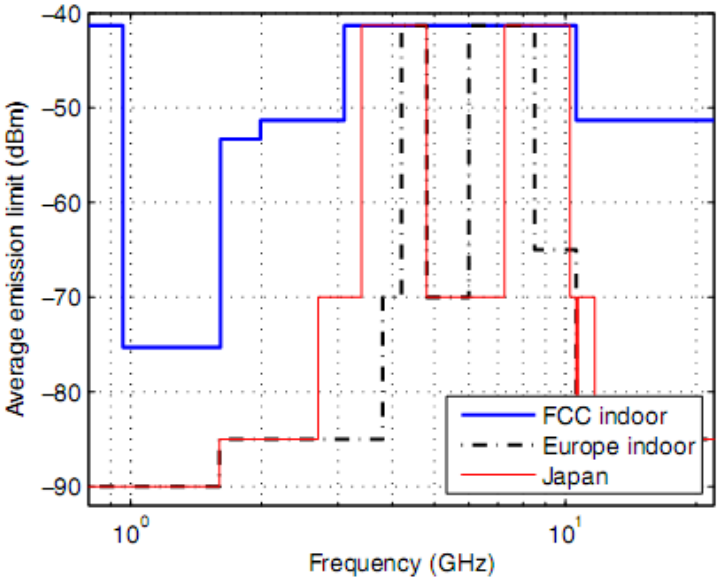


Figure 2.3. Emission limits for indoor operations [7]

2.4. Advantages

UWB systems have lots of useful advantages. First of all, they provide the possibility of using of an extremely wide and unlicensed frequency spectrum. Using UWB systems with other technologies on the same frequency interval greatly increases spectral efficiency. UWB also offers great flexibility of spectrum usage. A variety of parameters that are not only used during the characterization process of the system which gives the flexibility written above but also gives us the chance of designing adaptive transceivers. In addition, these transceivers can be used for optimizing systems performance as a function of the required data rate, range, power, quality of service and user preference. UWB systems are appropriate for applications that require high data rates (on the order of 1 Gbps) however, over very short ranges (less than 1 m). Thanks to the adaptive receiver, the data rate can be easily traded off for increasing the usage range of the application. Likewise, data rate and range can be traded off for low power consumption. Most importantly, adaptive transceivers can be designed according to the needs like providing service for multiple applications without the requirement of additional hardware.

The high temporal resolution of UWB signals results in low fading margins, implying robustness against multipath [8]. UWB signals show relatively low material penetration losses as a result of spanning a very wide frequency range. Excellent time resolution property of UWB systems gives the opportunity of using more accurate ranging applications. Thanks to the extremely short duration pulses that are transmitted, sub-decimeter ranging can be possible. Additionally, due to the specific working principle of the transceiver, which is used in a UWB communication technique, it does not require up/down conversion. Consequently, the designer can reduce the size of the devices.

To sum up, the key benefits of UWB systems can be written as:

- Accurate ranging and high data rate communication at the same time
- Design possibility of low cost and low power transceivers
- Immunity to multipath propagation
- High data rates

- Low interference.

2.5. Challenges

UWB systems have not only advantages but also some challenges like every technology that people have used. Some of these are fundamental and some others are practical. It is good to address them carefully to ensure the success of UWB technology in wireless world. Some issues like; multi-access code design, multiple access interference (MAI) cancellation, narrowband interference (NBI) detection and cancellation, synchronization of the receiver to extremely narrow pulses, accurate modeling of UWB channels, etc. still require research and development. Also, the role of UWB technology in wireless networks is still uncertain.

Among the challenges of UWB, a limited list can be given as follows [8]:

- Coexistence with other services and handling strong narrowband interference;
- Shaping (adapting) spectrum of transmitted signals (multiband, OFDM-based UWB, etc.);
- Practical, simple, and low-power transceiver design;
- Accurate synchronization and channel parameter estimation;
- High sampling rate for digital implementations;
- Powerful processing capabilities for high performance and coherent digital receiver structures;
- Wideband RF component designs (such as antennas, low noise amplifiers, etc.);
- Multiple accessing, multiple access code designs, and multiuser interference;
- Accurate modeling of the ultra wideband channel in various environments;
- Adaptive system design and cross-layer adaptation for UWB;
- UWB tailored network design.

In addition all these challenges, the most obvious one is regulatory problems. As UWB occupies such a wide bandwidth, many users exist whose operating spectrum will be affected. First, they must be convinced about the interference issue which can affect their

existing services. Standards of UWB systems are also a big problem for interoperability of UWB devices. There are currently two camps of UWB supporters each with their own standard of UWB design, and currently there is no compromising ground to resolve this issue [6]. This disagreement may be the biggest obstacle which UWB market must surpass for growth, in the future since, consumers may hesitate to choose which standard to buy.

3. APPROACHES TO UWB COMMUNICATION SYSTEMS

An UWB signal is defined as signal that has fractional bandwidth ratio, which is the ratio of signal bandwidth to center frequency [9], greater than 0.25 or bandwidth of 500 MHz or higher. Two different approaches are used for the implementation of a UWB communication system today. Impulse radio (IR) is one of the variants of UWB technology which modulates data in time rather than in frequency and it sends short duration impulses for communication. The second variant is multiband approach in which the bandwidth is broken into sections and the information is transmitted over several independent narrowband carriers by applying orthogonal frequency-division multiplexing (OFDM).

3.1. Orthogonal Frequency-Division Multiplexing (OFDM)

The parallel transmission of several signals, which are modulated at different carrier frequencies, f_m, forms an OFDM modulated signal. The OFDM approach to UWB meets the 500 MHz bandwidth requirement (the composite signal occupies a 528 MHz bandwidth) by using 128 carriers that are modulated with a Quadrature Phase Shift Keying (QPSK) constellation. All these carriers are equally spaced by Δf in the frequency domain and efficiently generated by using Fast Fourier Transform (FFT) techniques. The input of an OFDM modulator which is a subdivided binary sequence into groups of K bits used to generate blocks of N symbols $\{d_0, \ldots, d_m, \ldots, d_{N-1}\}$ where the generic d_m assumes one of L possible values with

$$K = N \log_2 L. \tag{3.1}$$

To transmit the N symbols of the block in parallel, the signals modulating distinct carriers must be orthogonal in frequency. If T_0 is the time that is used for transmitting each symbol on the corresponding carrier, orthogonality among different transmissions can be achieved by adopting $\Delta f = 1/T_0$. In addition, a guard interval T_G is introduced between transmission of subsequent blocks mainly to prevent Inter-Symbol Interference (ISI) [4].

These requirements lead to the symbol duration of $T = T_0 + T_G$ for OFDM. Thus, the maximum symbol rate appears as:

$$R_S = \frac{N}{T} = \frac{N}{T_0 + T_G}. \tag{3.2}$$

20-30% of the total symbol duration T is composed of the length of the guard interval. Generally, this interval is used for transmitting the *cyclic prefix* which is a copy of the final border section of the OFDM symbol. In addition, guard interval is used to maintain carrier synchronization at the receiver, if time-dispersive channels exist. The duration of the guard interval limits the length of cyclic prefix.

If $c_m=a_m+jb_m$ indicates the point in the constellation associated with symbol d_m, the OFDM signal corresponding to a block of N symbols is given by [4]:

$$x(t) = g_T(t)\sum_{m=0}^{N-1}(a_m \cos(2\pi(f_p + f_m)t + \phi) - b_m \sin(2\pi(f_p + f_m)t + \phi)). \tag{3.3}$$

The OFDM composite signal persists on a channel for the information length of 242.42 ns plus 60.61 ns cyclic prefix time and then switches to another channel within a 9.5 ns guard time [2]. Therefore, the long existence time on a channel is approximately 303 ns and it means that multipath fading can be effectively viewed through a narrowband filter. This OFDM approach uses 528 MHz channels however, it uses at least three at a time like time-frequency hopping manner. For the sake of increasing the total radiated power, consequently, increasing the total occupied bandwidth frequency hopping is used in this OFDM approach. In Table 3.1, system parameters of an OFDM system for three different data rates are shown. Additional 528 MHz wide channels up to 10.6 GHz provide more system capacity, more available power and combinations of power and capacity for improving performance. Actually, the performance of this OFDM approach resembles that of 128 narrowband radios.

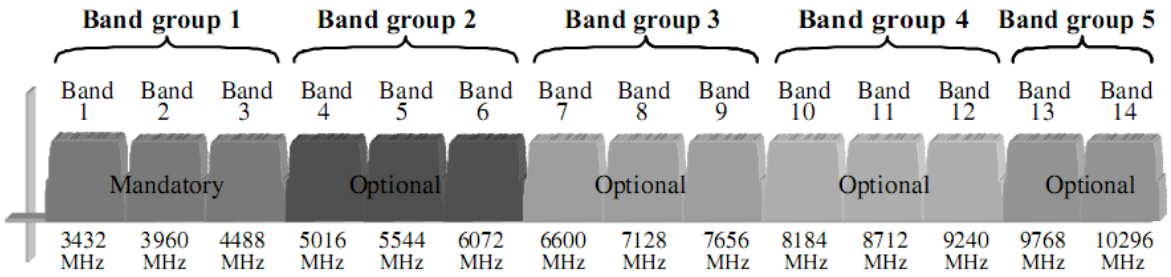


Figure 3.1. Band occupancy of an OFDM-UWB system [7]

Table 3.1. OFDM system parameters for a UWB system [2]

Information data rate	**110 Mbps**	**200 Mbps**	**480 Mbps**
Modulation/constellation	OFDM / QPSK	OFDM / QPSK	OFDM / QPSK
FFT size	128	128	128
Coding rate	11 / 32	5 / 8	3 / 4
Spreading rate	2	2	1
Information tones	50	50	100
Data tones	100	100	100
Information length (ns)	242.42	242.42	242.42
Cyclic prefix (ns)	32 / 528 = 60.61	60.61	60.61
Guard interval (ns)	5 / 528 = 9.47	9.47	9.47
Symbol interval (ns)	312.5	312.5	312.5
Channel bit rate (Mbps)	640	640	640
Symbol period (ns)	937.5	937.5	937.5

Before moving on to the next approach some advantages and disadvantages of OFDM are listed below:

OFDM systems

- Eliminate inter-symbol interference during communication,
- Achieve higher data rates,

while

- Having complex architectures and,
- Consuming more power.

3.2. Impulse Radio (IR)

Impulse radio is a form of ultra-wide bandwidth spread-spectrum signaling and it has properties that make systems a good candidate for short range communications in multipath environments. It is the most common and traditional way to emit an UWB signal which is based on the transmission of low duty cycle signals that are composed of sub nanosecond pulses. The pulse propagates with distortion when it is applied to an appropriate antenna.

The data, in IR, is modulated in time rather than in frequency; therefore, the user can get an enhanced data throughput with low power consumption. IR uses multiple-access techniques such as time hopping (TH), direct sequence (DS) or a combination of both. Thanks to IR, wide-band coherent communication is possible by adopting the Rake receiver for exploiting the inherent diversity of the channel and captures the energy of all paths at the receiver.

Transmitting a reference signal along with the data leads to a signaling scheme referred to as transmitted-reference (TR). Due to its simplicity, there is renewed interest in TR signaling for UWB systems, which can exploit multipath diversity inherent in the environment without the need for channel estimation and stringent acquisition [10]. Differential encoding over consecutive symbols can also be used to alleviate inefficient resource usage as TR signaling allocates a significant part of the symbol energy for transmitting reference pulses.

Spread-spectrum techniques must be used in communications with IR-UWB systems since, they operate in the highly populated interval of the frequency spectrum. Therefore, they must not only insure that they do not interfere with narrowband radio systems operating in the same band but also they must contend with a variety of interfering signals. A simple means for spreading the spectrum of these ultra-wide band low-duty-cycle pulse trains is time hopping, with data modulation accomplished by additional pulse position modulation at the rate of many pulses per data symbol [11]. Due to the significant bandwidth of UWB, an IR based multiple-access system can be used by many users.

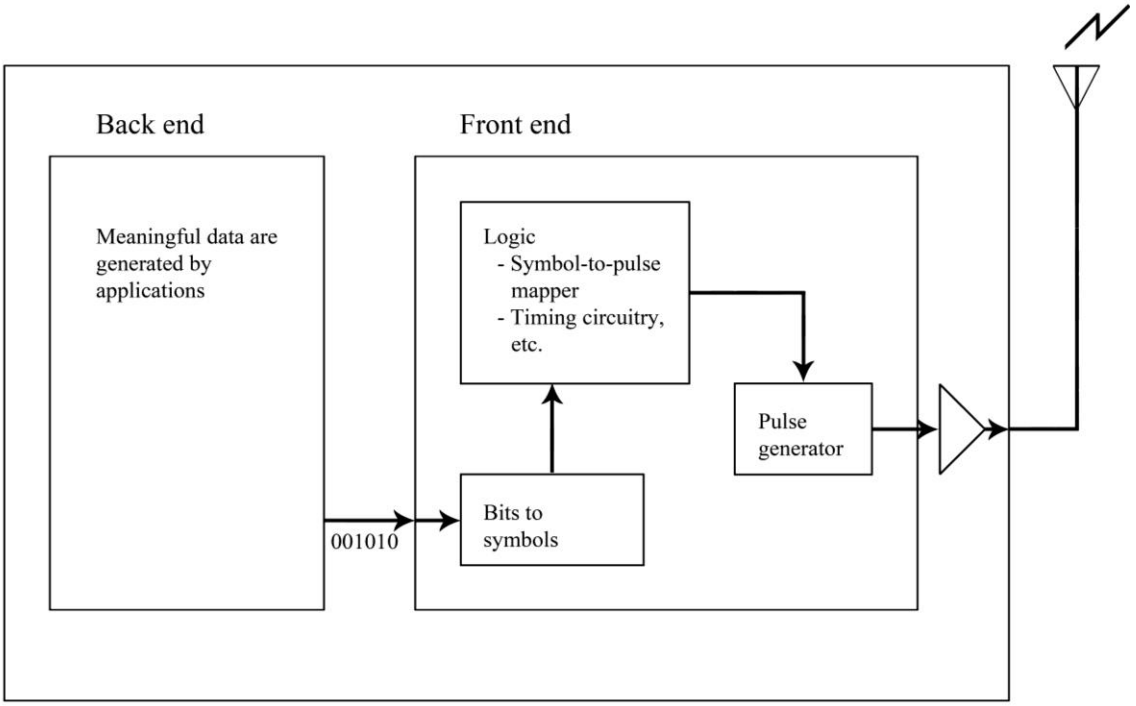


Figure 3.2. A basic block diagram of an UWB transmitter [6]

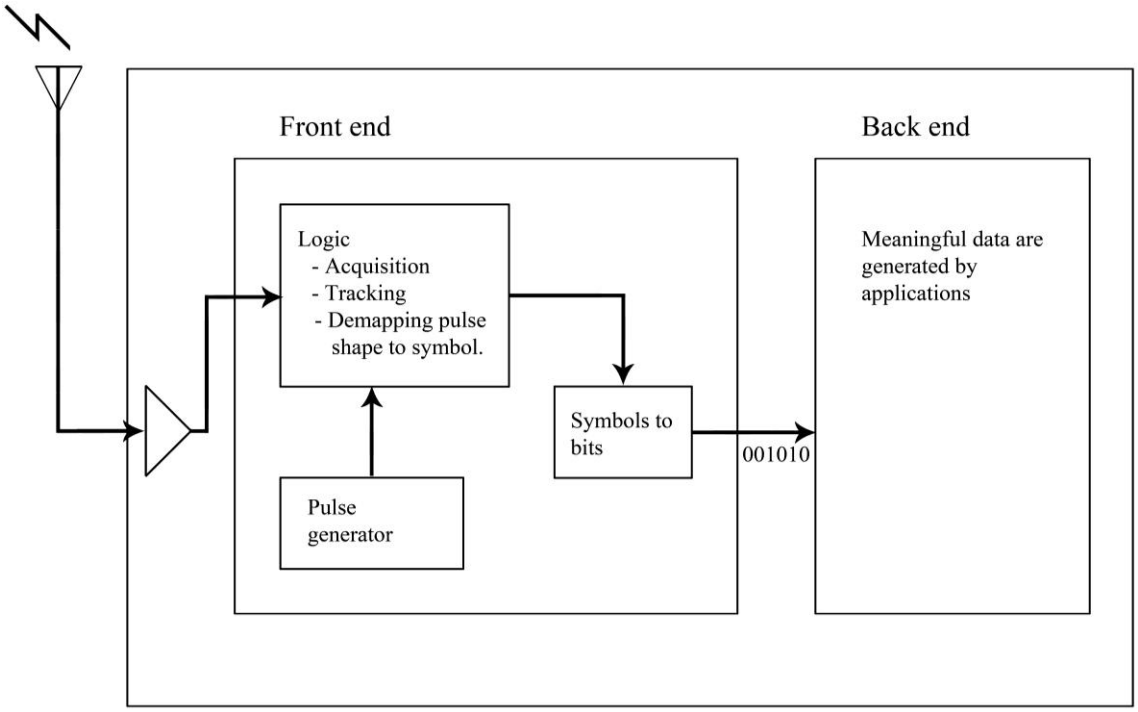


Figure 3.3. A basic block diagram of an UWB receiver [6]

Transmitted pulses of ultra-short duration with very low power spectral density, a wide fractional channel bandwidth and excellent immunity to interference from other radio systems, are typical characteristics of IR-UWB systems [12]. The attractive properties of IR also make the design process of the system challenging. Regulations over such a wide bandwidth limit the radiated power, sync acquisition times are increased as a result of ultra fine time resolution and the system may require additional hardware to capture appropriate signal energy. Also, full mobility of devices that include UWB systems increase power control requirements and the list of the challenges goes on like this.

Before talking about the IR signal types it is good to state that some of the advantages and disadvantages of IR-UWB systems shortly:

IR-UWB systems

- Power consumption of the transmitter can be very small because of the low duty cycle of pulses,
- No need for carrier modulation,
- Simple overall system architecture,
- Robust to multipath fading

while

- It is difficult to generate and send extremely short and low power pulses.

A basic UWB transmitter and receiver block diagram can be seen in Figure 3.2 and Figure 3.3, respectively, which are highly simplified models, just to give a general idea.

3.2.1. Generating the TH-UWB Signals

TH-UWB was found to prevent the collisions in UWB communication systems that have multiple users. This method represents a symbol by a pseudorandom code dedicated to a specific user.

In TH-UWB, a binary sequence, for instance $b = (\ldots, b_0, b_1, \ldots, b_k, b_{k+1}, \ldots)$, that is given to be transmitted and it is generated at a rate of $R_b = 1 / T_b$ bits per second. At the beginning, the system that generates TH-UWB signals repeats each bit N_s times and generates a binary sequence $(\ldots, b_0, b_0, \ldots, b_0, b_1, b_1, \ldots, b_1, \ldots, b_k, b_k, \ldots, b_k, b_{k+1}, b_{k+1}, \ldots, b_{k+1}, \ldots) = (\ldots, a_0, a_1, \ldots, a_j, a_{j+1}, \ldots) = a$ at a rate of $R_{cb} = N_s / T_b = 1 / T_s$ bits per second. This process introduces redundancy and in the classical terminology this is called channel coding. Then, an integer valued code, $c = (\ldots, c_0, c_1, \ldots, c_j, c_{j+1}, \ldots)$, is applied to the binary sequence $a = (\ldots, a_0, a_1, \ldots, a_j, a_{j+1}, \ldots)$ during the transmission coding operation. This operation generates a new sequence *d*. The generic element of the sequence *d* is expressed as follows [4]:

$$d_j = c_j T_c + a_j \varepsilon \tag{3.4}$$

where T_c and ε are constant terms that satisfy the condition $c_j T_c + \varepsilon < T_s$ for all c_j and in general $\varepsilon < T_c$. Here, it is good to state that *d* is a real valued, *a* is a binary and *c* is an integer valued sequence.

According to the most common trends of UWB technology, it is assumed that the integer valued sequence *c* is a pseudorandom code. Two distinct cases exist for *c*. First, the code might be periodic and its period is indicated by N_p. Second case corresponds to the absence of periodicity. In first case $N_p = N_s$ while $N_p \rightarrow \infty$ in the second case. The first one is the most adopted case and the periodicity of the code coincides with the length of the repetition code.

Then, the coded and real valued sequence *d* is modulated with PPM technique which generates a sequence of Dirac pulses, $\delta(t)$, at a rate of $Rp = N_s / T_b = 1 / Ts$ pulses per

second. The generated pulses are located at times $jT_s + d_j$. It means the pulses are shifted in time by d_j, from the nominal positions jT_s. Therefore, it can be seen that the pulses occur at times $jT_s + c_jT_c + a_j\varepsilon$ by substituting d_j with equation (3.4). It is important to note that code c introduces a time hopping shift on the generated signal and because of this reason it is indicated as TH code. In addition, stating the difference between the shift introduced by PPM modulator, $a_j\varepsilon$, and TH code, c_jT_c, might be useful. Tc is called chip time and $a_j\varepsilon < c_jT_c$ except for the condition $c_j = 0$.

The last process our modulated sequence must pass through is pulse shaping. A pulse shaper filter with impulse response $p(t)$ is used. The output of the filter must be a sequence of non-overlapping pulses thus, $p(t)$ must be adjusted very well.

Finally, here is the TH-UWB signal equation after cascading all written operations [4]:

$$s(t) = \sum_{j=-\infty}^{+\infty} p(t - jT_s - c_jT_c - a_j\varepsilon). \tag{3.5}$$

Besides, it is good to note the information that the bit interval, which is the time that is used to transmit one bit, T_b is written as $T_b = N_sT_s$.

If a PPM modulator is used instead of a PAM modulator, equation of the output signal can be rewritten as [4]:

$$s(t) = \sum_{j=-\infty}^{+\infty} p_{a_j}(t - jT_s - c_jT_c). \tag{3.6}$$

3.2.2. Generating the DS-UWB Signals

As mentioned before UWB technology is based on narrow pulses which have very low power thus minimizing interference. If narrow pulses are sent, the spectrum becomes much wider. However, even with this huge bandwidth, higher and higher data rate needs of

the consumer never end. Besides, the width of the spectrum does not have so much importance if a system cannot send enough pulses per second. As a result, the need for higher bit rates led to the development of the DS-UWB approach. This approach also has the ability to mitigate interference, increase system capacity and improve the quality of service (QoS). It allows users to send data in the same bandwidth simultaneously by pre-assigning a pseudorandom noise code which is multiplied to the transmit signal.

In DS-UWB, a binary sequence, for instance $b = (..., b_0, b_1, ..., b_k, b_{k+1}, ...)$, that is given to be transmitted and it is generated at a rate of $R_b = 1 / T_b$ bits per second. At the beginning, the system that generates TH-UWB signals repeats each bit N_s times and generates a binary sequence $(..., b_0, b_0, ..., b_0, b_1, b_1, ..., b_1, ..., b_k, b_k, ..., b_k, b_{k+1}, b_{k+1}, ..., b_{k+1}, ...) = a^*$ at a rate of $R_{cb} = N_s/T_b = 1/T_s$ bits per second. This system resembles the system in TH scheme which introduces redundancy.

Then, with a second operation the a^* sequence is transformed into a positive and negative valued sequence $a = (..., a_0, a_1, ..., a_j, a_{j+1}, ...)$, i.e. $a_j = 2a_j^* - 1$ where $-\infty < j < +\infty$. Later, a binary valued code, $c = (..., c_0, c_1, ..., c_j, c_{j+1}, ...)$ that is composed of ±1's and the period value N_p, which is generally assumed to be N_s, is applied to the sequence $= (..., a_0, a_1, ..., a_j, a_{j+1}, ...)$. Thus, a new sequence $d = a \cdot c$ that is composed of elements $d_j = a_j c_j$. A more common assumption about N_p is taking its value as a multiple of N_s. Meanwhile, it is good to state that d is a ±1's sequence like a and it is generated at a rate of $R_{cb} = N_s / T_b = 1 / T_s$ bits per second.

After these steps, sequence d is modulated with Pulse Amplitude Modulation (PAM) technique which generates a sequence of Dirac pulses, $\delta(t)$, at a rate of $Rp = N_s / T_b = 1 / Ts$ pulses per second. The generated pulses are located at times jT_s.

The last process our modulated sequence must pass through is pulse shaping. A pulse shaper filter with impulse response $p(t)$ is used. The impulse response of the filter is rectangular which has a width of T_s in common DSSS systems.

Finally, the TH-UWB signal equation after cascading all written operations is provided below [4]:

$$s(t) = \sum_{j=-\infty}^{+\infty} d_j \, p(t - jT_s). \tag{3.7}$$

The resulting waveform written in (3.7) is an original PAM waveform and calculation of its Power Spectral Density (PSD[4]) is easier than the PSD calculation of (3.5) because of the lack of time shift that exist in PPM technique. This is due to the fact that the pulses in PAM occur at regular time intervals. Besides, it is good to note the information that the bit interval, which is the time that is used to transmit one bit, T_b is written as $T_b = N_s T_s$, like in the TH-UWB case.

If a PPM modulator is used instead of a PAM modulator, equation of the output signal can be rewritten as [4]:

$$s(t) = \sum_{j=-\infty}^{+\infty} p\left(t - jT_s - \varepsilon \frac{d_j + 1}{2} \right). \tag{3.8}$$

Two different UWB communication approach and most commonly used signal generation techniques in them presented above in detail. Some widely used pulse shapes and modulation methods in UWB communication will be given in the next section.

[4] The PSD is defined as *PSD = P/B*, where *P* is the power transmitted in watts, *B* is the bandwidth of the signal in hertz and the unit of PSD is watts/hertz [6].

4. UWB PULSE WAVEFORMS AND MODULATION METHODS

Any function that satisfies the PSD regulations can be used as an UWB pulse waveform. In theoretical studies, some common pulse shapes (e.g. Gaussian, Rayleigh, Hermitian or Laplacian pulses) are used. However, approximations to a Gaussian pulse shape and its derivatives are common due to their favorable time and frequency response [13]. In practice, it is almost impossible to generate exact pulse shapes because of some reasons, such as matching problems, like in theoretical works. Therefore, only coarse approximations of these pulse shapes can be used.

In this section, Gaussian pulse shapes will be described briefly because the pulse generator that has been used discussed in this thesis generates Gaussian like pulses. Then, some information about modulation techniques used by UWB systems will be given. These pulse shapes can also be used for multiband systems.

4.1. Gaussian Pulse Shapes

The Gauss function, which is being used in many different scientific disciplines, gives its name to this class of pulses. In UWB communication, generally, higher order Gaussian pulses are preferred because of their superior PSD shapes. These types of pulses can be generated by filtering the Gaussian pulse with an appropriate filter. All higher order Gaussian pulses have a different number of zero crossings. The number of zero crossings increases with the increasing order of the derivative. Therefore, higher order Gaussian pulses yield waveforms with lower relative bandwidths and higher center frequencies [14].

4.1.1. The Gaussian Pulse

The Gaussian pulse has smooth transitions everywhere in time domain and it is given by

$$P_{GP}(t) = \frac{1}{\sqrt{2\pi}\sigma} e^{-(1/2)((t-\mu)/\sigma)^2} \tag{4.1}$$

where μ is the center of the pulse and σ describes the width of the pulse. Nevertheless, the Gaussian pulse (Figure 4.1 (a)) includes a DC term (Figure 4.1 (b)) in frequency domain therefore, it is not suitable for wireless systems. While this pulse is impractical, higher order derivatives of it do not contain a DC term and applicable for UWB systems.

4.1.2. Gaussian Monocycle

First derivative of a Gaussian pulse is called a Gaussian monocycle. This pulse shape has a single zero crossing in time domain (Figure 4.1 (a)) and it is given by

$$P_{GM}(t) = \frac{1}{\sqrt{2\pi}\sigma}\left[1-\left(\frac{t-\mu}{\sigma}\right)^2\right] e^{-(1/2)((t-\mu)/\sigma)^2}. \tag{4.2}$$

As it is stated above, the frequency spectrum of a Gaussian monocycle does not contain a DC term (Figure 4.1 (b)).

4.1.3. Gaussian Doublet

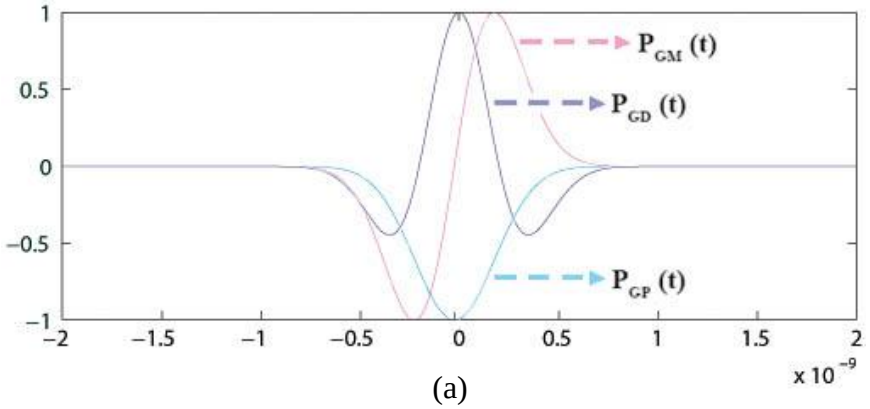
Gaussian doublet is formed by two Gaussian pulses each have reverse amplitude of each other and they have a time gap of T_G between the maximum points of each. Also, the second derivative of a Gaussian pulse is called a Gaussian doublet (Figure 4.1 (a)). Time domain representation is given by

$$P_{GD}(t) = \frac{1}{\sqrt{2\pi}\sigma}\left[e^{-(1/2)((t-\mu)/\sigma)^2} - e^{-(1/2)((t-\mu-T_G)/\sigma)^2}\right]. \tag{4.3}$$

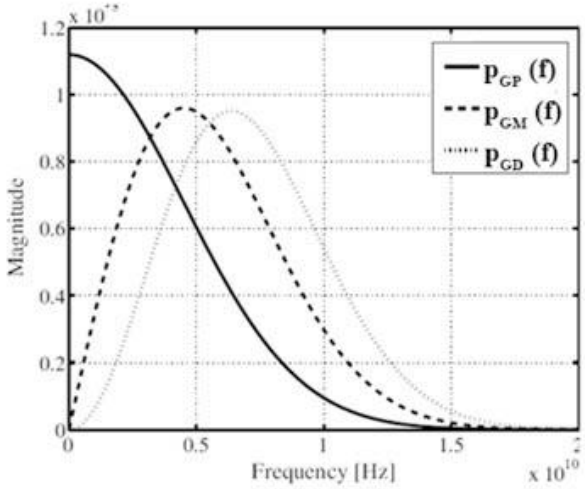
The parameters T_G, σ and μ determine the pulse width.

It is important to note that the bandwidth of the Gaussian doublet (Figure 4.1 (b)) is smaller than that of the Gaussian pulse and Gaussian monocycle [14].

All these waveforms have an asymmetric spectrum around the center frequency.



(a)



(b)

Figure 4.1. A Gaussian pulse, monocycle and doublet in (a) time and (b) frequency domain

4.1.4. Higher Order Derivatives of Gaussian Pulse

Higher order Gaussian pulses can also be used in UWB systems. In some cases, it is much better to use higher order derivatives since, the bandwidth of the pulses decrease with the increasing order of derivatives. This situation is very suitable for applications that are working on a smaller bandwidth, such as the ones work between 3.1 GHz – 5.1 GHz.

In Figure 4.2, PSD of some higher order Gaussian pulses and the change in spectral density according to the order of derivation can be seen.

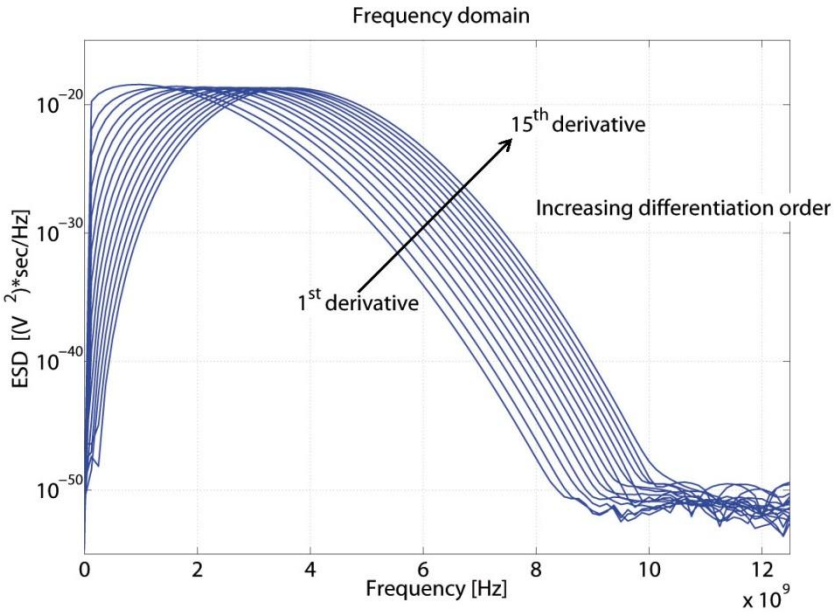


Figure 4.2. Gaussian pulse PSDs with FCC mask

4.2. Modulation Methods

One single UWB signal cannot carry information on itself. Digital information must be added to the pulse which is called *modulation*. A few basic modulation methods are applied to the UWB communication systems and these methods will be examined briefly in this section.

Most common modulation methods used in UWB communication can be separated in to two groups for the sake of clarity. First group is called as *time-based techniques*, which contains pulse position modulation (PPM); and the second one is called as *shape-based techniques* and it contains binary phase shift keying (BPSK), on-off keying (OOK) and pulse amplitude modulation (PAM) [6]. In addition, some well known modulation methods are not applicable to UWB systems. For instance FM, in which each pulse includes lots of frequency elements, is difficult to apply to UWB communication.

4.2.1. Pulse Position Modulation (PPM)

A modulation technique in which the position of each pulse is modulated depending on the transmitted bit while the pulses phase and amplitude remains the same. For instance, an arbitrary pulse train, *g(t)*, is given (Figure 4.3 (a)). The information can be modulated by a delay parameter, τ_i, to create the modulated pulses (Figure 4.3 (b)), g_i, which is given by

$$g_i = g(t - \tau_i) \tag{4.4}$$

where *t* represents time.

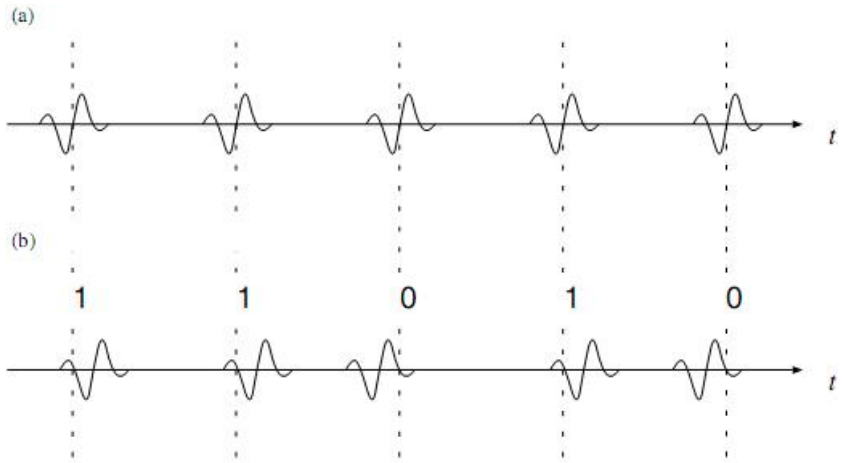


Figure 4.3. (a) An unmodulated pulse train, (b) PPM modulated pulse train

Simplicity of PPM and the extreme controllability of delay time are some advantages of it. Since, it is necessary to modulate pulses with almost picoseconds accuracy. However, it is also a disadvantage because of dealing with sub-nanosecond timing.

4.2.2. Pulse Amplitude Modulation (PAM)

A modulation technique in which the amplitude of each pulse is modulated depending on the transmitted bit while the pulses phase and position remains the same. For

instance, an arbitrary pulse train, *g(t)*, is given (Figure 4.4 (a)). The information can be modulated by a delay parameter, τ_i, to create the modulated pulses (Figure 4.4 (b)), g_i, which is given by

$$g_i = \sigma_i g(t), \qquad \sigma_i > 0 \tag{4.5}$$

where σ is the pulse shape parameter.

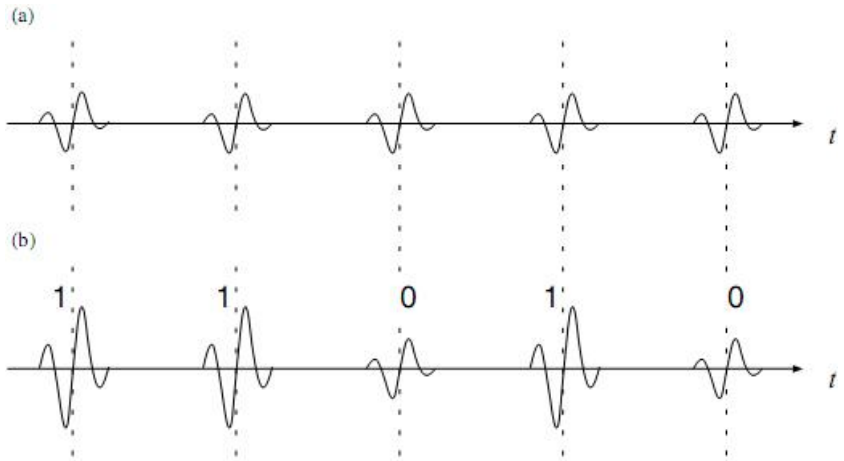


Figure 4.4. (a) An unmodulated pulse train, (b) PAM modulated pulse train

Amplitude modulation is not an advisable modulation technique for most short range communication methods since the pulse that has a smaller amplitude is more vulnerable to noise than its larger amplitude counterpart.

4.2.3. Bi-Phase Modulation (BPM)

A modulation technique in which the phase of each pulse is modulated depending on the transmitted bit while shape and position of the pulse remain the same. For instance, an arbitrary pulse train, *g(t)*, is given (Figure 4.5 (a)). The information can be modulated by a shape parameter, σ_i, to create the modulated pulses (Figure 4.5 (b)), g_i, which is given by

$$g_i = \sigma_i g(t), \qquad \sigma_i = 1, -1. \tag{4.6}$$

BPM has the advantage of the 3-dB gain in power efficiency in comparison with PPM since, PPM delays pulses during transmission. It means that PPM must always waste the time which is very precious for the sake of data rate. For instance, if PPM uses a delay time equal to one pulse width, BPM can send twice the number of pulses which means twice the data rate.

BPM in UWB presents several other benefits such as [6]:

- Because of its power ratio (less than 8 dB), an implementation using bi-phase does not require any external snap-recovery or tunnel diodes or power-amplifier circuitry. Instead, it can be driven directly from a low-voltage high-speed complementary metal-oxide-semiconductor (CMOS) IC.
- A bi-phase system needs only a stable, low-phase-noise clock as the pulses occur on a constant spacing. Synchronization circuits can be narrowband so that they do not add significant jitter. As a result, less power and real estate are needed to implement the required circuits.

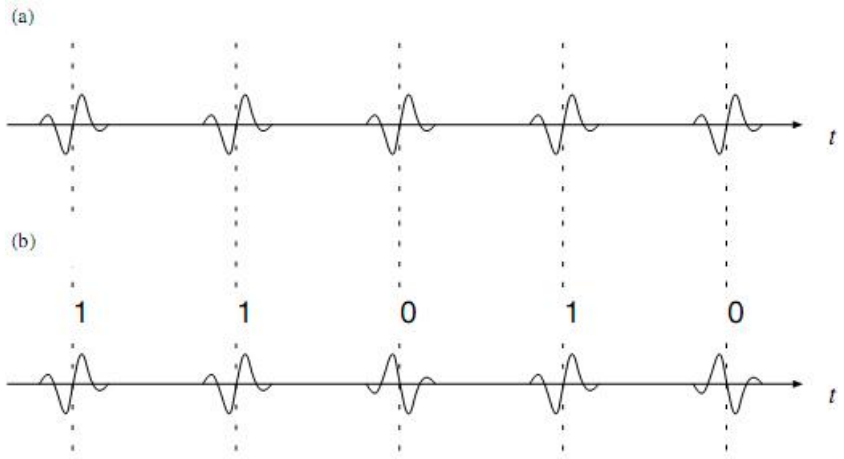


Figure 4.5. (a) An unmodulated pulse train, (b) BPM modulated pulse train

4.2.4. On-Off Keying (OOK)

A modulation technique in which the pulse exists or not depending on the transmitted data is “1” or “0”, respectively. Shape, position, amplitude and phase of the pulse remain the same. For instance, an arbitrary pulse train, *g(t)*, is given (Figure 4.6 (a)). The information can be modulated by a shape parameter, σ_i, to create the modulated pulses (Figure 4.6 (b)), g_i, which is given by

$$g_i = \sigma_i g(t), \qquad \sigma_i = 0,1. \tag{4.7}$$

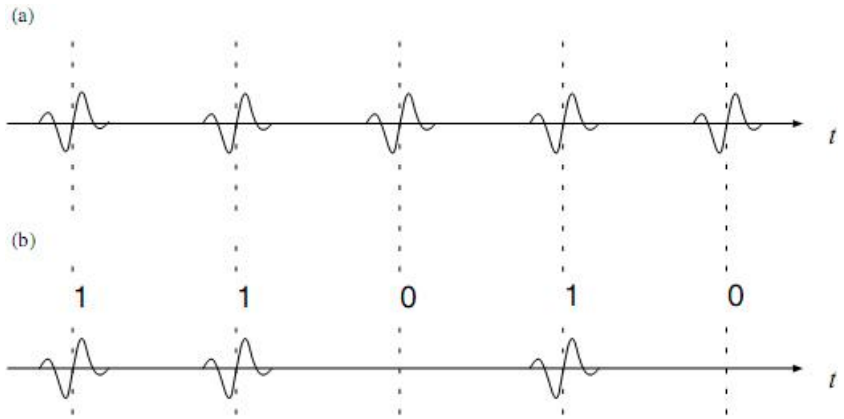


Figure 4.6. (a) An unmodulated pulse train, (b) BPM modulated pulse train

In spite of the ease of OOK, it has a major problem in presence of multipath. Since, echoes of the original transmitted pulses or other pulses make difficult to detect the absence of a pulse.

Below, a table (Table 4.1), that shows the advantages and disadvantages of the modulation methods discussed is provided as a brief summary.

Table 4.1. Advantages and disadvantages of the written modulation methods

Modulation Method	Advantages	Disadvantages
PPM	Simplicity	Requires fine time resolution
PAM	Simplicity	Noise immunity
BPM	Simplicity, efficiency	Binary only
OOK	Simplicity	Binary only, noise immunity

5. VHDL-AMS DESIGN OF THE IR-UWB TRANSCEIVER

VHDL (**V**ery high speed integrated circuit **H**ardware **D**escription **L**anguage) is a commonly used hardware description language to design digital circuits. A sample VHDL model of an OR gate is given in Figure 5.1. Programming in VHDL can be separated in 3 basic parts:

- Entity: Input and output ports of the circuit are described in this part.
- Architecture: Structure of the circuit is described in this part.
- Process: operating principles of the circuit are described in this part and it appears in architecture part.

```
---------- VHDL MODEL OR_unit ----------
library ieee;
use ieee.std_logic_1164.all;
---------- ENTITY DECLARATION OR_unit ----------
entity OR_unit is
    port(x: in std_logic;
         y: in std_logic;
         F: out std_logic
);
end OR_unit;
---------- ARCHITECTURE DECLARATION arch_OR_unit ----------
architecture OR_beh of OR_unit is
    begin
        F <= x or y;
end OR_unit;
---------- END VHDL MODEL OR_unit ----------
```

Figure 5.1. An OR gate written in VHDL

The designed transceiver has a mixed signal structure which means it has not only digital circuits but also it has analog ones. Therefore, VHDL-AMS (**V**ery high speed integrated circuit **H**ardware **D**escription **L**anguage-**A**nalog **M**ixed **S**ignal) is used at the beginning of design process instead of VHDL. Starting the design with a hardware description language gives the advantage of seeing some simulation results about the circuit easily before dealing with transistor level design which is much more difficult to

cope with. In addition, simulation time of a circuit written in VHDL-AMS is shorter than the one which is passed for the circuit designed in transistor level.

Basically, VHDL-AMS is similar to VHDL. However, it includes some extra terms for describing and simulating analog circuits. For instance, one of these differences can be observed in Figure 5.2. The terms *electrical* and *terminal*, which are used to describe input and output ports of the circuit, written under the section entity do not exist in VHDL.

```
---------- VHDLAMS MODEL squaring_unit ----------
LIBRARY ieee;
USE ieee.ALL;
---------- ENTITY DECLARATION squaring_unit ----------
ENTITY  squaring_unit IS
    port ( terminal input: electrical;
        terminal output: electrical;
        terminal ground: electrical);
END ENTITY squaring_unit;
---------- ARCHITECTURE DECLARATION arch_squaring_unit ----------
ARCHITECTURE arch_squaring_unit OF squaring_unit IS
    QUANTITY vin ACROSS input TO ground;
    QUANTITY vout ACROSS i THROUGH output TO ground;
BEGIN
    vout == vin**2.0;
END ARCHITECTURE arch_squaring_unit;
---------- END VHDLAMS MODEL squaring_unit ----------
```

Figure 5.2. A squaring circuit written in VHDL-AMS

5.1. Transmitter

In UWB transmitters, first, meaningful data are generated by applications which can be a web browser on a PDA or an e-mail client on a laptop, etc. this application part of the wireless devices is called “back end”.

The binary data generated by back end is passed to the “front end” in the next step. In some cases, the binary information should be mapped from bits to symbols that actually represent multiple bits. Then, these symbols are sent to pulse generator, via a logic block of

the transmitter, to generate analog pulse shapes. Precise timing circuitry is also required for a meaningful transmission between the transmitter and the receiver.

At the end of the transmitter, before the antenna, analog pulses generated can be amplified according to the situation. Theoretically, to obey the power emission rules, large gain values are not needed. Therefore, power amplification may be ignored at the transmitter side, especially if the pulse generator is able to drive the antenna.

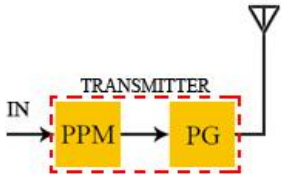


Figure 5.3. UWB transmitter

The designed transmitter is shown in Figure 5.3 which is composed of a *pulse position modulator (PPM)* and a *pulse generator (PG)*.

5.1.1. PPM

PPM block generates square pulses and positions of these are changed according to the data bits at the input. Width of the generated pulses can be adjusted by the designer. For the sake of clarity, operation principle of this block is written below:

- For every bit which is “0”, the block generates a square pulse at a time during the first half of the duration of a data bit.
- For every bit which is “1”, the block generates a square pulse at a time during the second half of the duration of a data bit.

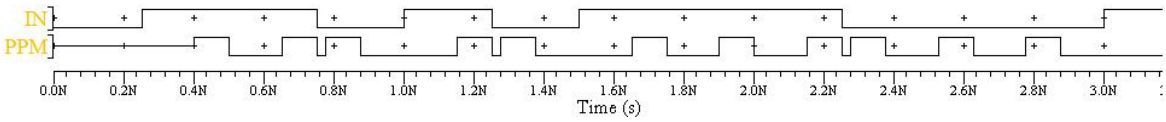


Figure 5.4. Input (IN) and output signals (PPM) of PPM block

Simulation result of the PPM modulator is shown in Figure 5.4.

5.1.2. Pulse Generator (PG)

PG generates 5th order derivative of the Gaussian pulse (Figure 5.5 (a)) when a rising edge comes from the modulator. In simulations, we decided to begin with that type of pulse since its spectral density (Figure 5.5 (b)) completely fits to the emission mask of FCC between 3.1 GHz – 10.6 GHz. In addition, PSD of this pulse has the largest span on frequency domain among the derivatives of the Gaussian pulse which obey the emission rules. For instance, 4th order derivative violates the FCC power regulations while 6th order derivative has a narrower span (Figure 4.2).

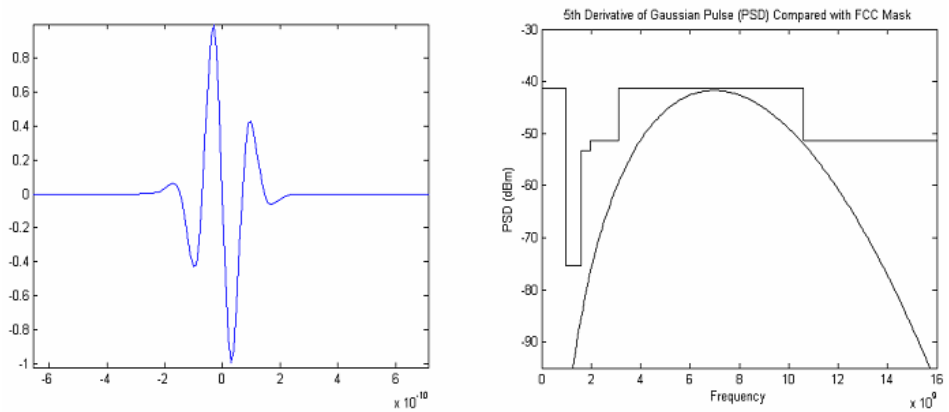


Figure 5.5. (a) 5th order derivative of the Gaussian pulse and its (b) PSD

Pulses generated by the VHDL-AMS model of pulse generator according to the input that comes from the modulator is shown in Figure 5.6. Amplitude and width of the pulse can be adjusted just by changing values of some variables in the equation of 5th order

derivative of the Gaussian pulse. There is no need to calculate currents, widths of transistors, etc. over and over to determine the properties of the required pulse with the help of VHDL-AMS models.

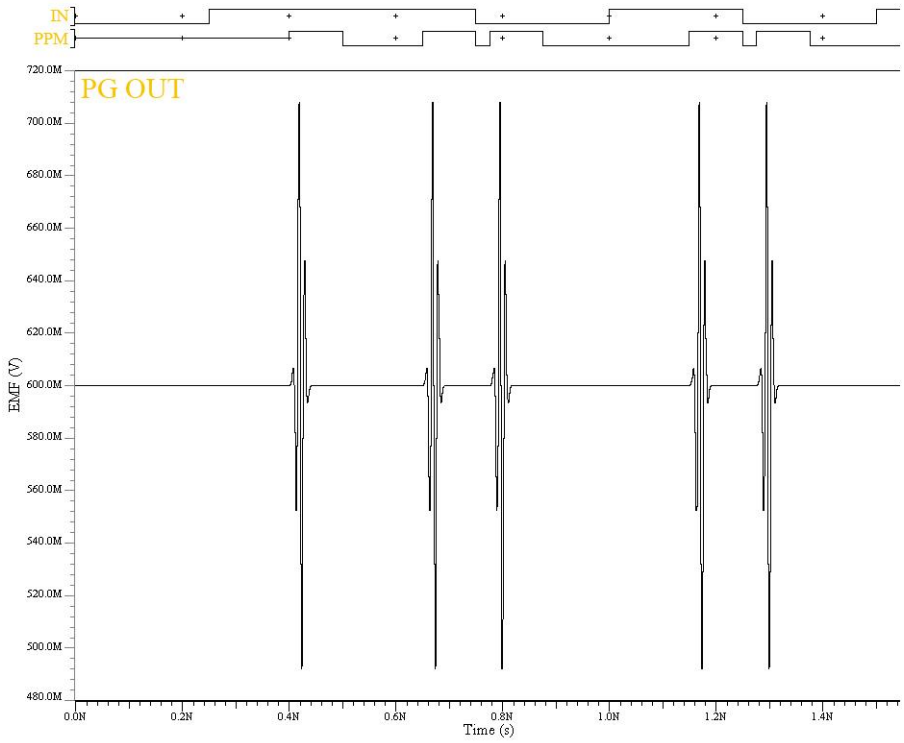


Figure 5.6. Input (PPM) and output signal (PG OUT) of PG

5.2. Receiver

A receiver takes the data coming from the transmitter and recovers it for providing information to a back-end application. The block diagram of the designed receiver is shown in Figure 5.7 which is composed of a *squaring block (SQR)*, *integrate and dump (I&D)*, *sample and hold (S&H)*, *analog-to-digital converter (ADC)* and a *demodulator (DeM)*. Actually, an UWB receiver requires a low-noise amplifier (LNA) to detect weak signals coming from the transmitter however, for the sake of simplicity and to save time, this block is ignored. Instead of writing a VHDL-AMS model of an LNA, the operation of LNA is copied by increasing the values of some constants and variables.

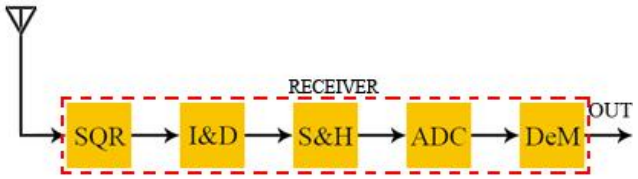


Figure 5.7. UWB receiver

In terms of operating principles, two significant distinctions exist between a transmitter and a receiver. First difference among the two is the requirement of an amplifier to increase the received signal power because of the weak signal property of UWB systems. This is an almost certain requirement for a receiver. The second is the realization of *detection* or *acquisition* functions by the receiver for detecting the transmitted pulses, which carry the original data, among irrelevant signals. Moreover, a receiver should continue to *track* these pulses to compensate the synchronization problems between the clocks of the transmitter and the receiver.

5.2.1. Squaring Block (SQR)

This is the first block of the receiver. It is used for taking square of pulses that are emitted from the transmitter antenna. With squaring operation, a signal that is compatible with energy detection scheme is generated. If the signal at the SQR input is given to the I&D block directly, it cannot take integral of that signal since the average value of the signal at the input of SQR block equals to zero. Additionally, SQR block attenuates noise up to particular levels that comes from air with the original transmitted pulses. Simulation result of the SQR is shown in Figure 5.8. Enable signal of the SQR is “0” at the first 250 ps of the simulation time. Therefore, output signal of the SQR starts after that period.

5.2.2. Integrate & Dump (I&D)

This block integrates the output signal of SQR block to get rid of the noise on the original signal. It operates during the time period defined by the designer to catch the transmitted PPM signal. First time period is at the first half of the duration of a data bit and

the second one is at the second half of the duration of a data bit. Simulation result of I&D is shown in Figure 5.9.

5.2.3. Sample & Hold (S&H)

S&H operates at the end of the integration operation. It samples the value of I&D output signal at the beginning of the sample and hold operation and holds that value for a specified time period. This block holds the desired value by adding the sampled value to the one at the input. With the help of this block, the following ADC can operate much

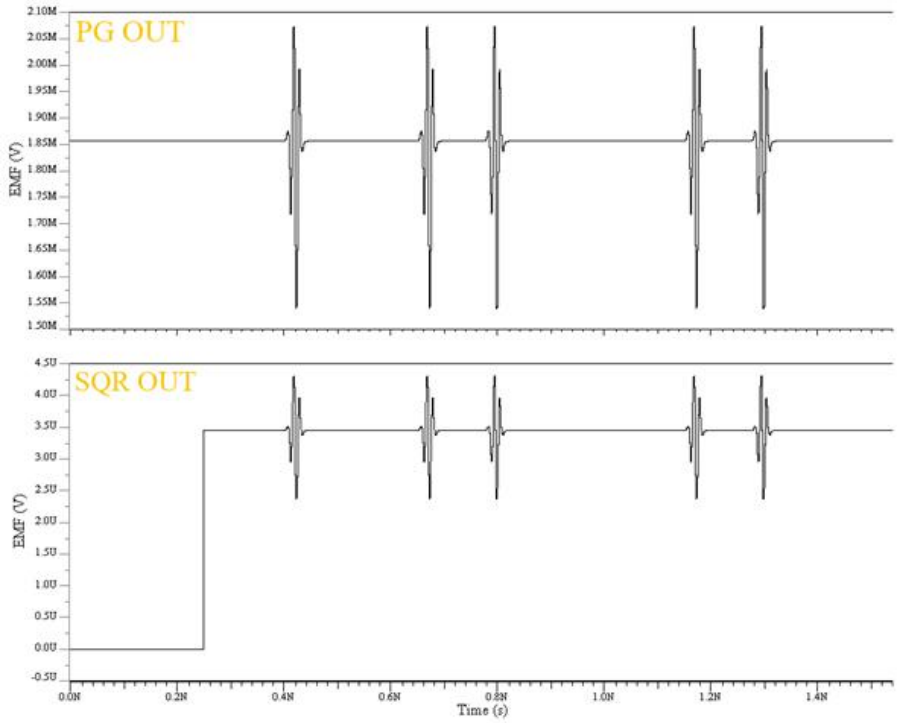


Figure 5.8. Input (PG OUT) and output signal (SQR OUT) of SQR

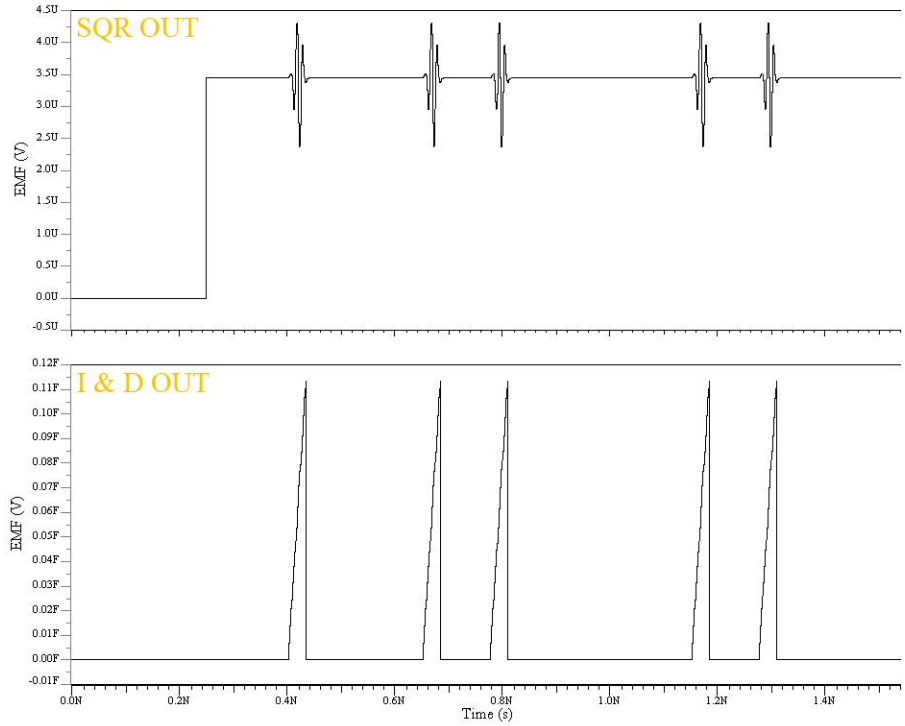


Figure 5.9. Input (SQR OUT) and output signal (I&D OUT) of I&D

slower than needed. In accordance, power consumption can be decreased. Like I&D and PPM blocks, S&H also operates twice during the time period in which one data bit passes. Simulation result of S&H is shown in Figure 5.10.

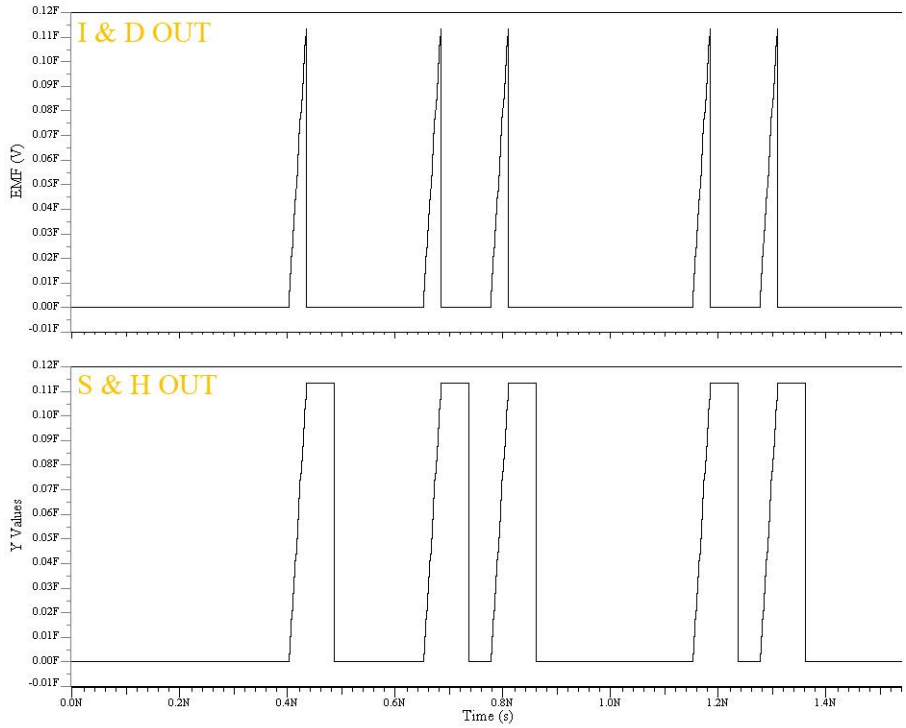


Figure 5.10. Input (I&D OUT) and output signal (S&H OUT) of S&H

5.2.4. Analog-to-Digital Converter (ADC)

ADC continuously controls the signal comes from S&H block and converts the analog value at its input to the digital one. This model generates 5-bit wide output signal. This property of ADC can be adjusted by changing just a few rows of code thanks to VHDL-AMS. It operates like I&D, PPM and S&H blocks which means it controls the signal at the input twice during the time period in which one data bit passes. Simulation result of S&H is shown in Figure 5.11.

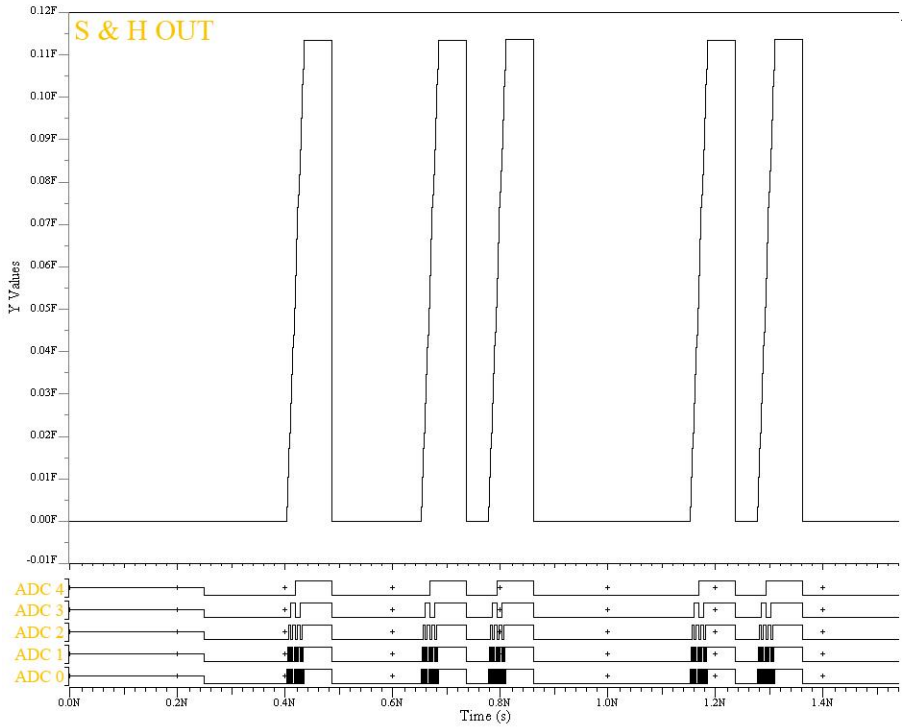


Figure 5.11. Input (S&H OUT) and output signal (ADC 4-0) of ADC

5.2.5. Demodulator (DeM)

DeM generates the original data, which is given at the transmitter side, by comparing the output signal of ADC. While designing this block a threshold value is specified to eliminate the noise from the transmission medium. Voltage levels of the S&H output signal comes to DeM input as a 5-bit word from ADC and this information is converted to an integer value during the operation of DeM and only the integer values greater than the threshold is taken into consideration. After these steps, if the integer value at the first half of the time period in which one data bit passes is larger than the one at the second half DeM generates a “0”. If the integer value at the second half is larger than the one at the first half DeM generates a “1”. As a result of this comparison, some noise levels over the threshold value can also be eliminated. Nevertheless, this operation method introduces a delay to the system which is equal to the duration of a data bit since, DeM has to wait the information that comes from ADC to make a comparison. In Figure 5.12, output of ADC and DeM blocks can be seen. Also, the original data that is given to the transmitter is added to the figure to show the 1 bit delay and to prove that the original data can be

obtained. Note that this is also the output of our ideal receiver model that is completely written in VHDL-AMS.

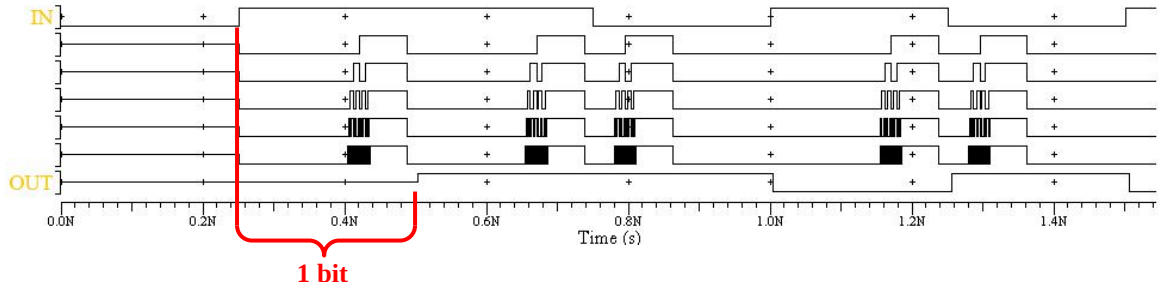


Figure 5.12. Original data (IN), outputs of ADC and output of DeM (OUT)

An ideal and very basic version of our transceiver circuit is generated with VHDL-AMS. This model is used for determining some specifications of our transceiver circuit such as amplitude and width of the pulse generated by the PG. During the simulation period of VHDL-AMS blocks, some of the specs are clarified for the transistor level design of the transceiver.

VHDL-AMS codes of the transceiver blocks are shown in Appendix c.

6. TRANSISTOR LEVEL DESIGN OF IR-UWB TRANSCEIVER

After VHDL-AMS model simulations, some of the specs were identified. According to them, some candidate topologies are selected for the required circuits among existing alternatives in the literature. Then, advantages and disadvantages of the selected structures are evaluated to choose the most appropriate circuitry. At the end, rough block diagrams of the transmitter and the receiver is formed with the help of simulations. These block diagrams and the corresponding blocks can be seen in this section. In addition, some explanations are also given to provide a basic information about the designed transceiver system.

6.1. Transmitter

The designed transmitter is shown in Figure 6.1 which is composed of a *modulator*, a *pulse generator* and a *band-pass filter (BPF).*

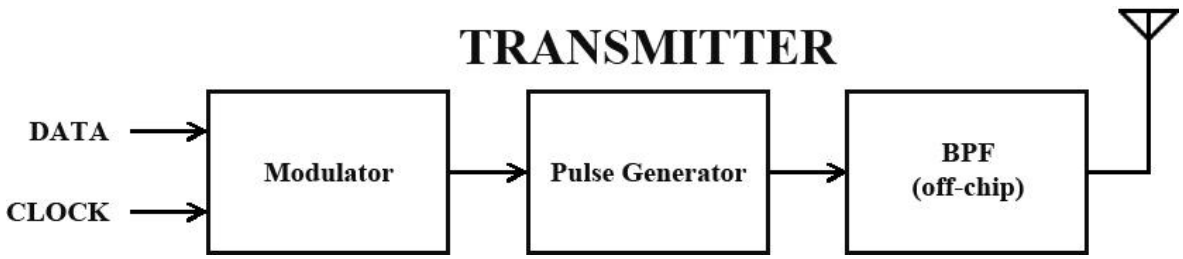


Figure 6.1. Block diagram of the designed transmitter

An AND gate is used as a modulator for simplicity. It takes a clock signal, which obeys the Nyquist sampling theorem, to modulate the data. As can be observed from Figure 6.2, this modulator generates OOK type modulated pulses.

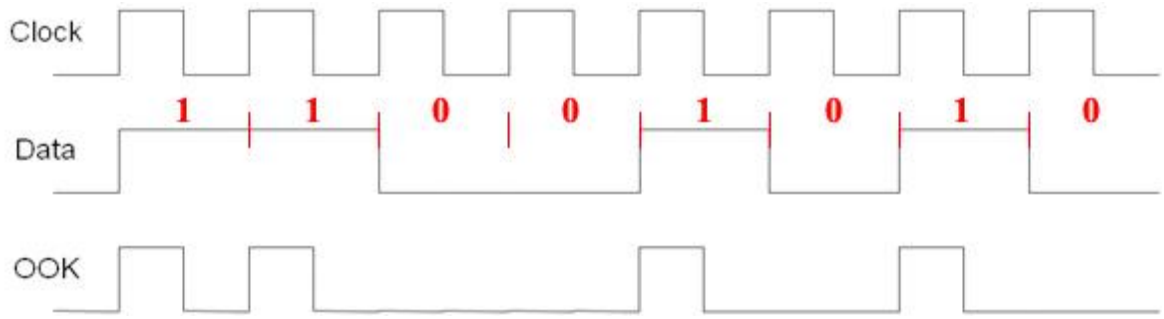


Figure 6.2. OOK modulator inputs (Clock, Data) and output (OOK)

A pulse generator, which will be explained in details in section 7, exists after the OOK modulator.

An off-chip 5th order series Chebyshev BPF (Figure 6.3) is used after the pulse generator, since PSD of the generated pulse cannot fit to the preferred operating frequency of the designed transceiver, which is between 3.1 GHz – 5.1 GHz.

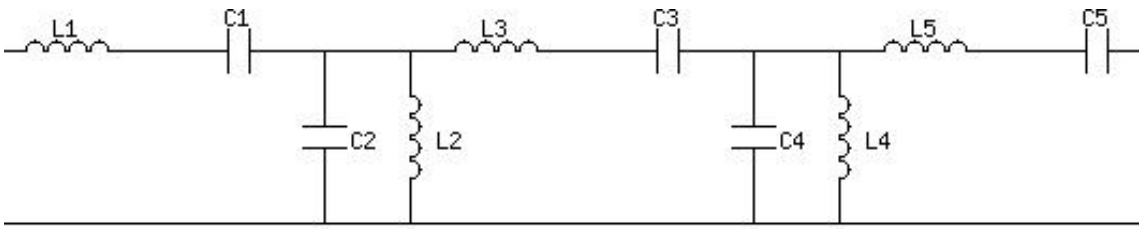


Figure 6.3. 5th order series Chebyshev BPF

6.2. Receiver

The designed receiver is shown in Figure 6.4 which is composed of a *BPF*, *low-noise amplifier (LNA)*, *variable gain amplifier (VGA)*, *multiplier*, *integrator*, *comparator*, *inverter chain* and a *D-type flip flop (DFF)* as a demodulator. The designed receiver is formed as a result of collaborative research of the project team.

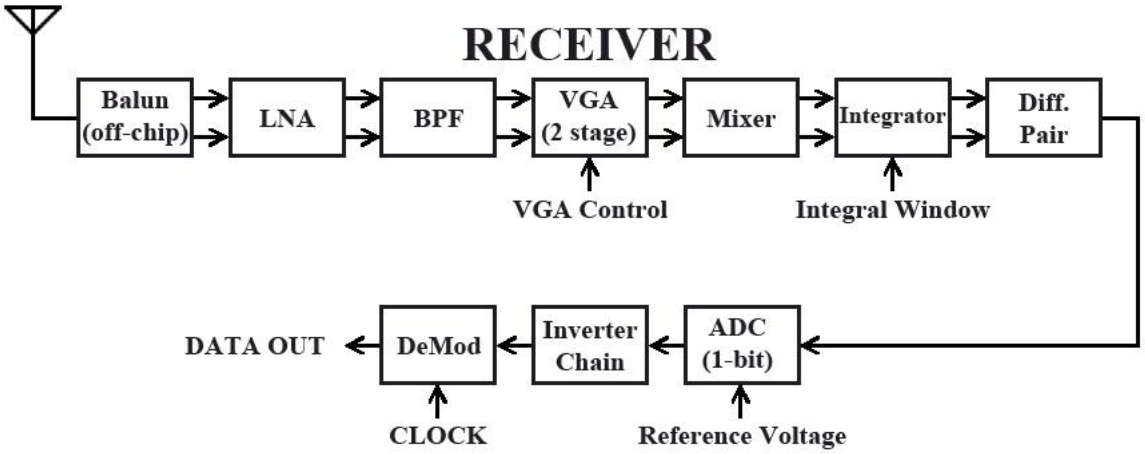


Figure 6.4. Block diagram of the designed receiver

The receiver part starts with an off-chip balun which is actually an electrical transformer type. It can convert single-ended signals to differential ones and vice versa. Operation principle of a balun is based on electromagnetic coupling. However, electromagnetic coupling is not sufficient for wideband operations. It must be combined with magnetic coupling and this class is generally known as *transmission line transformers*. A balun is used for the receiver since, it is needed to make single-ended signals differential. As, the receiver system is in differential structure. The usage of this structure is arisen from the advantage of high common mode rejection property of the differential blocks.

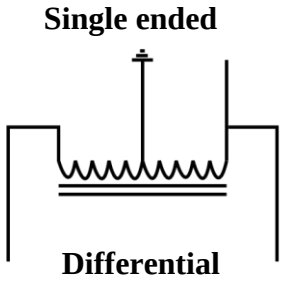


Figure 6.5. A wideband balun

Two 3rd order series Chebyshev BPFs are designed for the differential input of LNA to filter the signal that comes from the receiver antenna. These two filters have a smart design. RF pads, wire bonds from pad to the chip and electrostatic discharge (ESD) diodes,

which have adverse effects on the operation of LNA, are used as building blocks for these two filters in order to decrease or get rid of those effects. RF pads and ESD diodes are used as capacitors while the first inductors of the filters are realized with the wire bonds (Figure 6.6).

BPFs are followed by an LNA (Figure 6.6) which is one of the essential devices that receiver is made up of. Most important role of an LNA is to amplify the level of the signal which comes from input port of the LNA and it must do it without adding significant level of noise and distortion. This block determines the noise and linearity performance of the system since, the level of noise added to the signal by the LNA is increased through the receiver system.

LNA circuits have 5 significant parameters which are: (i) noise figure (NF), (ii) gain, (iii) bandwidth, (iv) impedance matching and (v) power consumption.

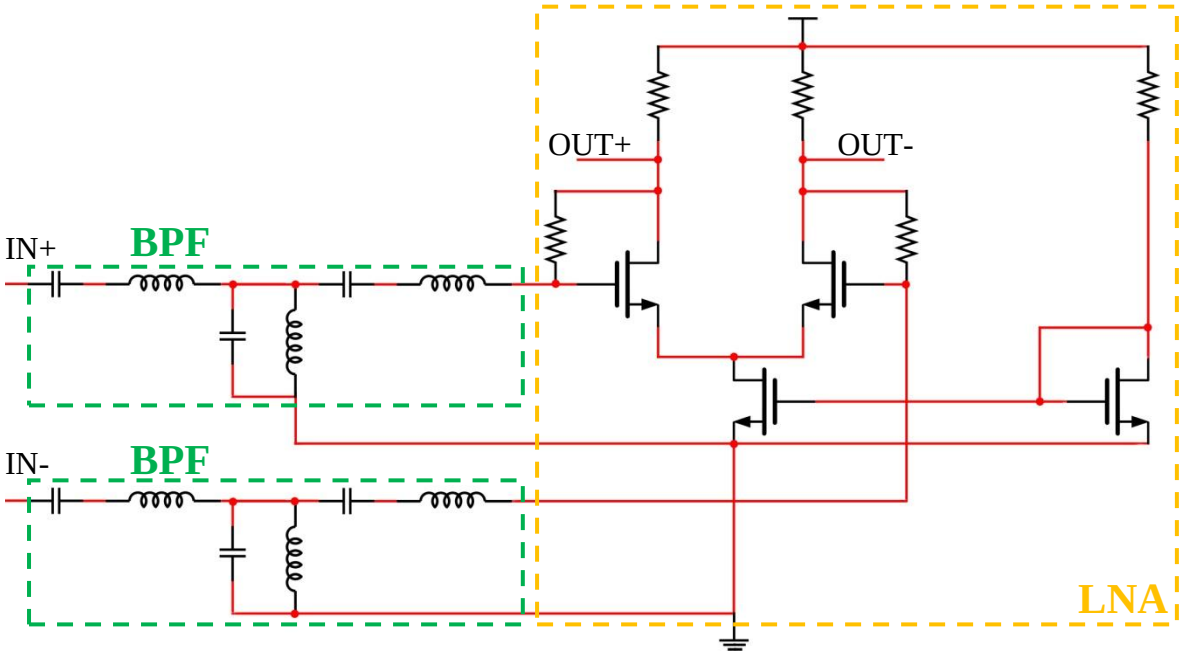


Figure 6.6. Schematic of two BPF at the differential inputs of the LNA

A resistive shunt-feedback-based LNA (Figure 6.6) is preferred for the receiver since this structure does not cover a large area on the chip because of lack of inductors. It provides good wideband matching and flat gain. Nevertheless, LNAs based on this

topology have poor NF in comparison to others and consume high power. NF degradation comes from the requirement of input impedance matching which should be typically 50 ohm. Furthermore, even with a moderate amount of voltage gain, the amplifier requires a rather large amount of current, especially in the CMOS, due to its strong dependence for voltage gain on the transconductance of the amplifying transistor [15].

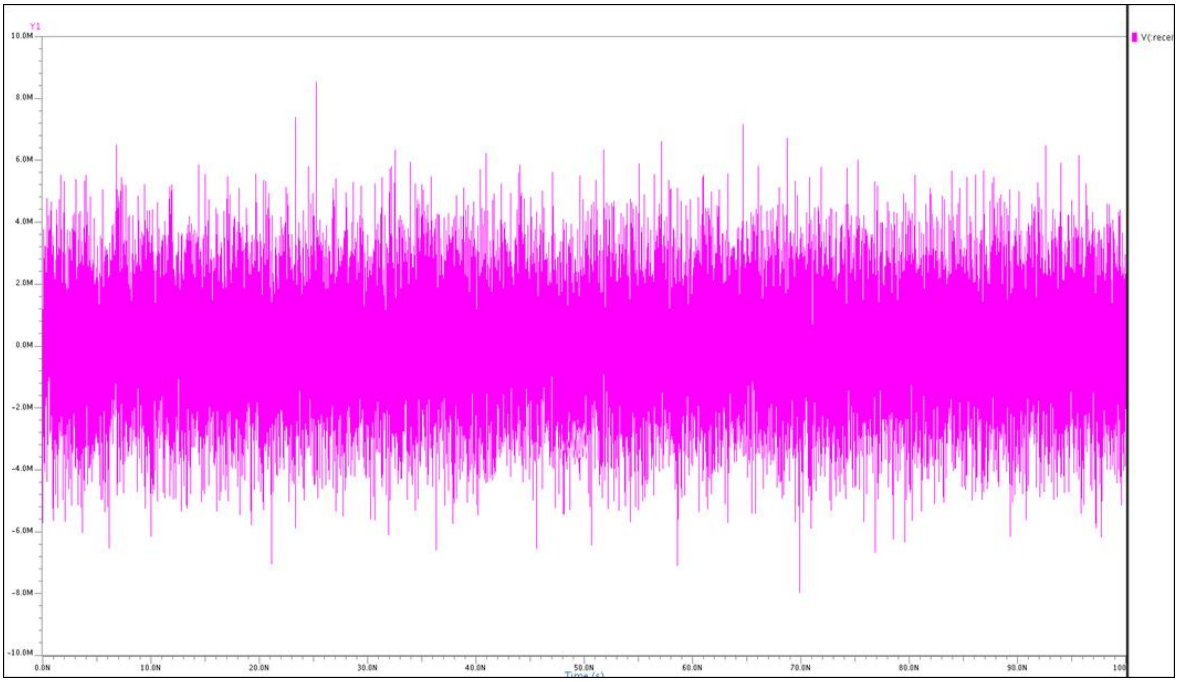


Figure 6.7. Signal at the LNA input

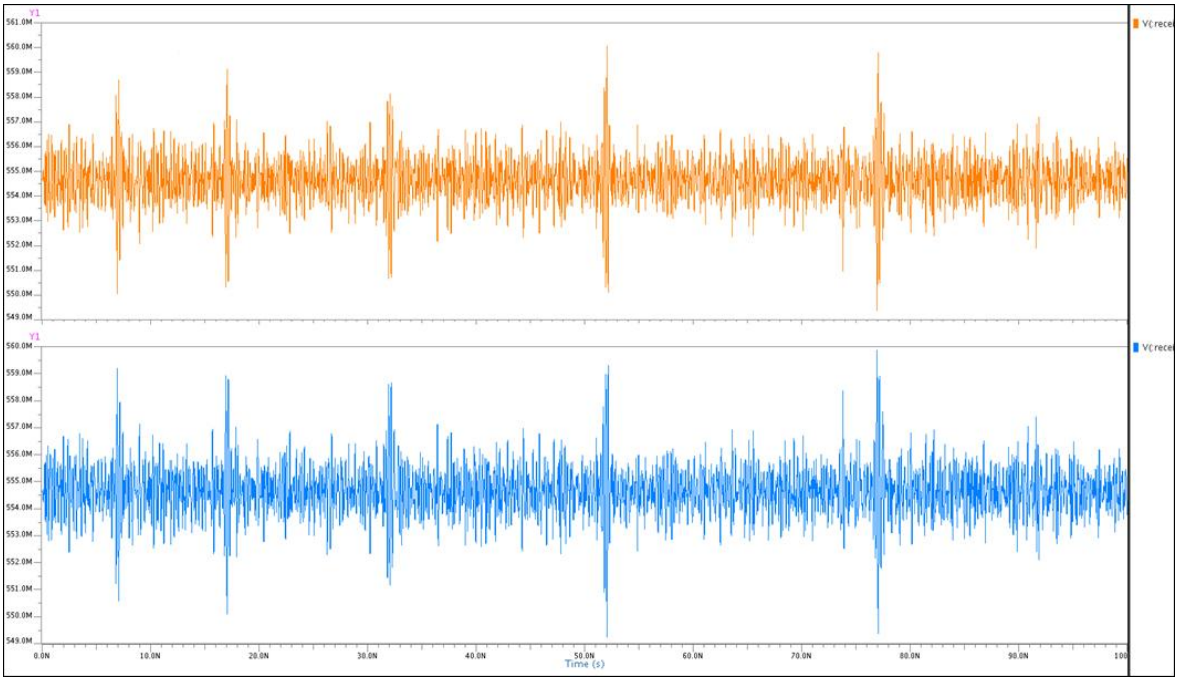


Figure 6.8. Differential output of the LNA

LNA is followed by a VGA. Variable gain amplifiers are used to regulate signal power to an optimum level in the radio communication systems since the transmitted and received signals can have a wide range of amplitude variations depending on the instantaneous signal path and other obstructions [16].

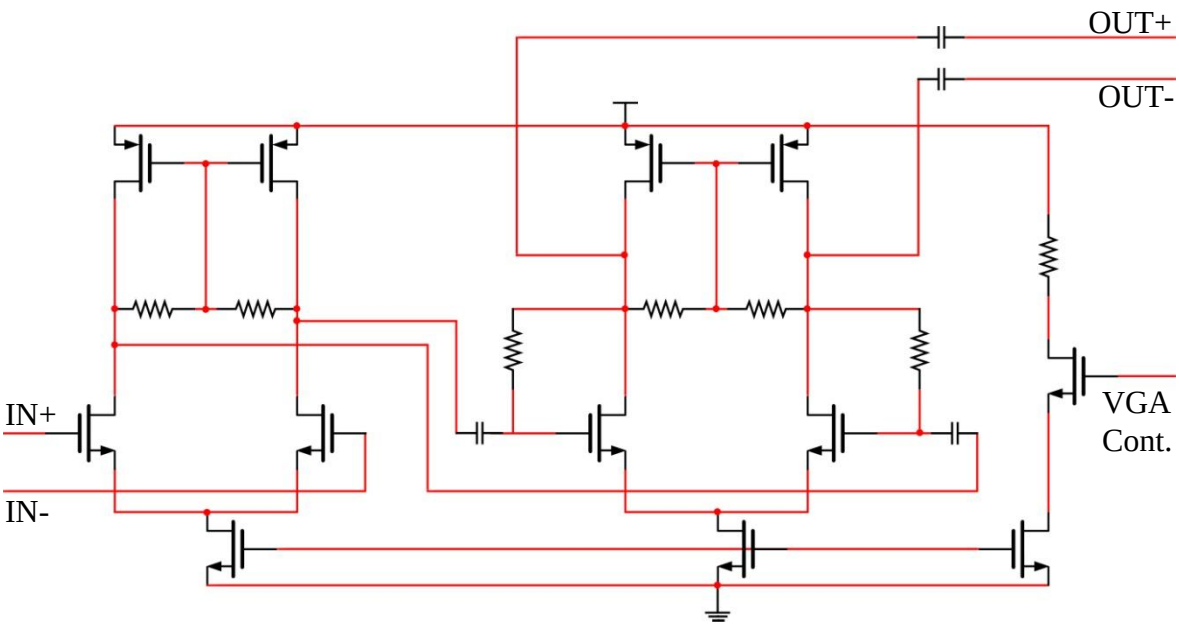


Figure 6.9. Schematic of the VGA

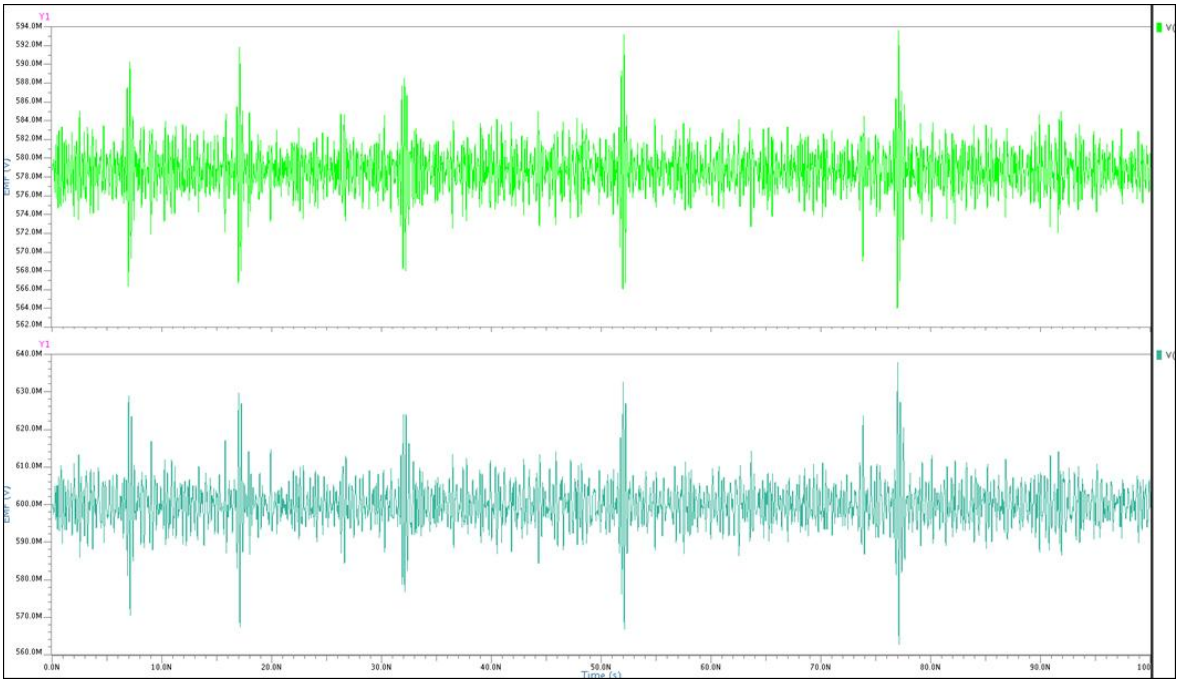


Figure 6.10. Differential output of the VGA

Two Gilbert cell VGA structures are cascaded (Figure 6.9). Gain of the amplifier can be adjusted by changing gate voltage (VGA control signal in Figure 6.4), thereby drain current, of the current source NMOS transistor. VGA must keep amplitude of the signal, which goes from the receiver antenna to the ADC, between acceptable levels since very high or low amplitude signals have adverse effects on the operation of comparator.

VGA is followed by a mixer which is used as a multiplier. An active load double balanced mixer structure (Figure 6.11) is chosen for the receiver. Inherent isolation between all ports, suppression of leakage signals at the output and increased linearity can be counted as some of the advantages of this topology.

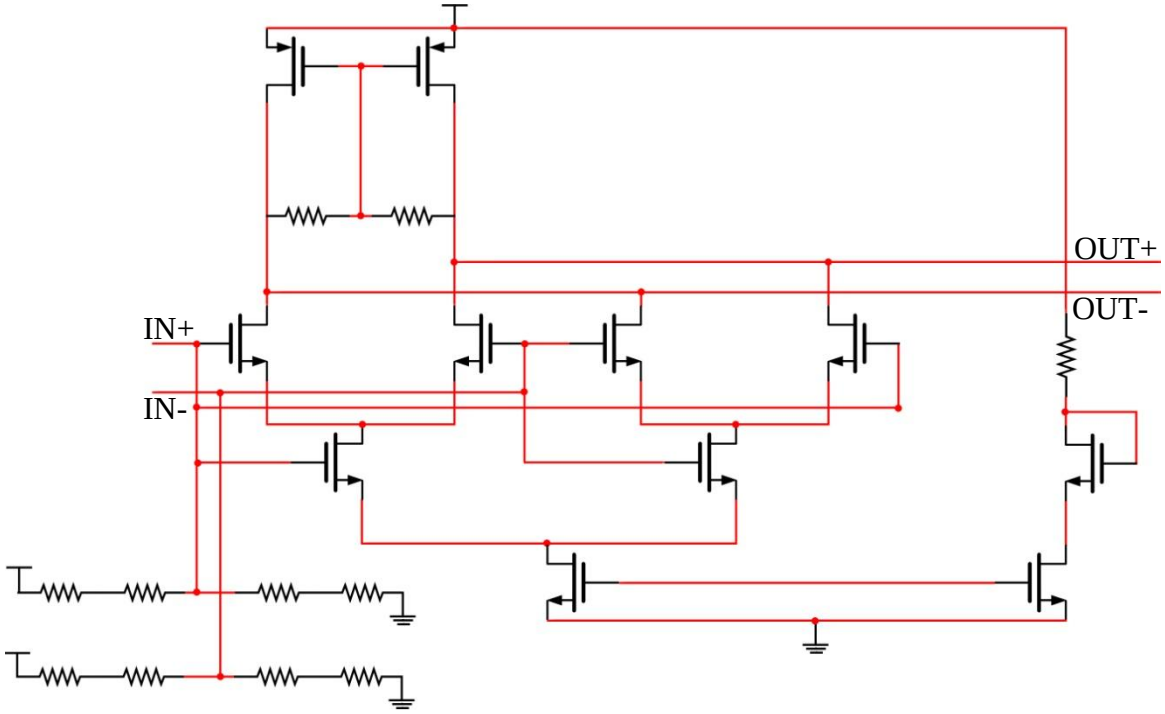


Figure 6.11. Schematic of the mixer

An active load should be used with this topology because of the constant DC voltage level, which should be increased or decreased with the increment or decrement of V_{DD} respectively, at the output.

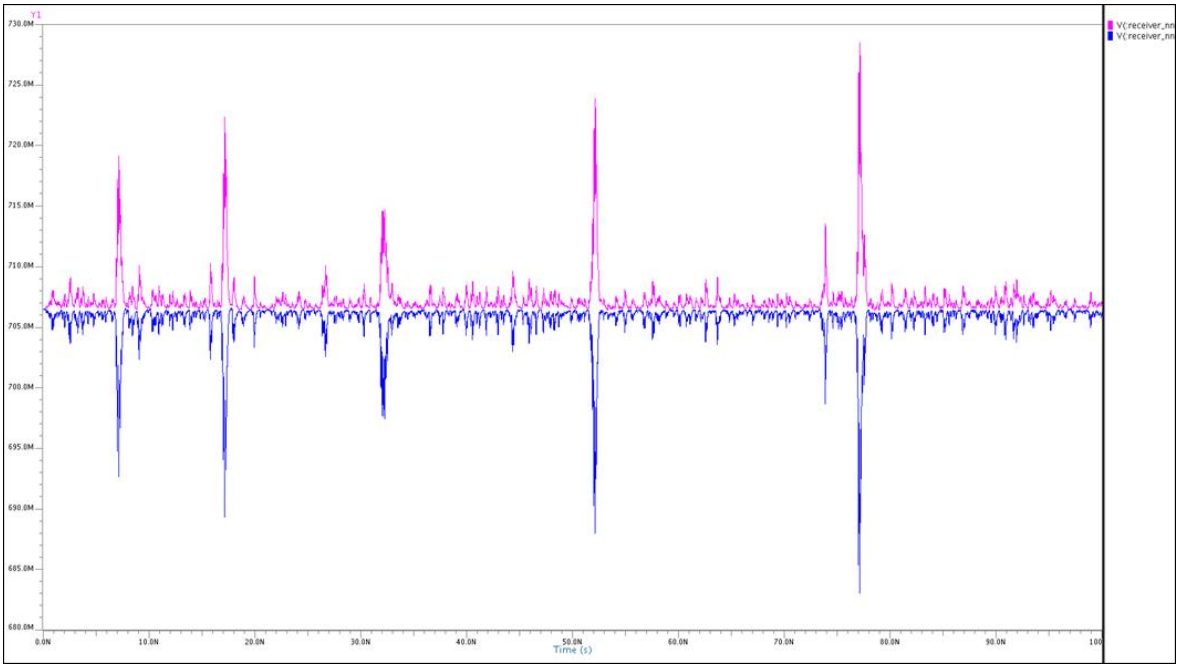


Figure 6.12. Differential output of the mixer

The mixer is followed by an integrator because of the chosen non-coherent energy detection (ED) structure for the receiver. A Gm-C integrator topology (Figure 6.13) is preferred among various different ones as, it is appropriate for ED receivers because of its high frequency response and moderate linearity. However, parasitic device capacitance which adds directly to the integrating capacitor is typically nonlinear leading to harmonic distortion [17]. Additionally, integration time of the circuit can be changed with the help of *integral window* signal which can be seen in Figure 6.4. In short terms, the integrator generates a signal at the output node more suitable for the comparator.

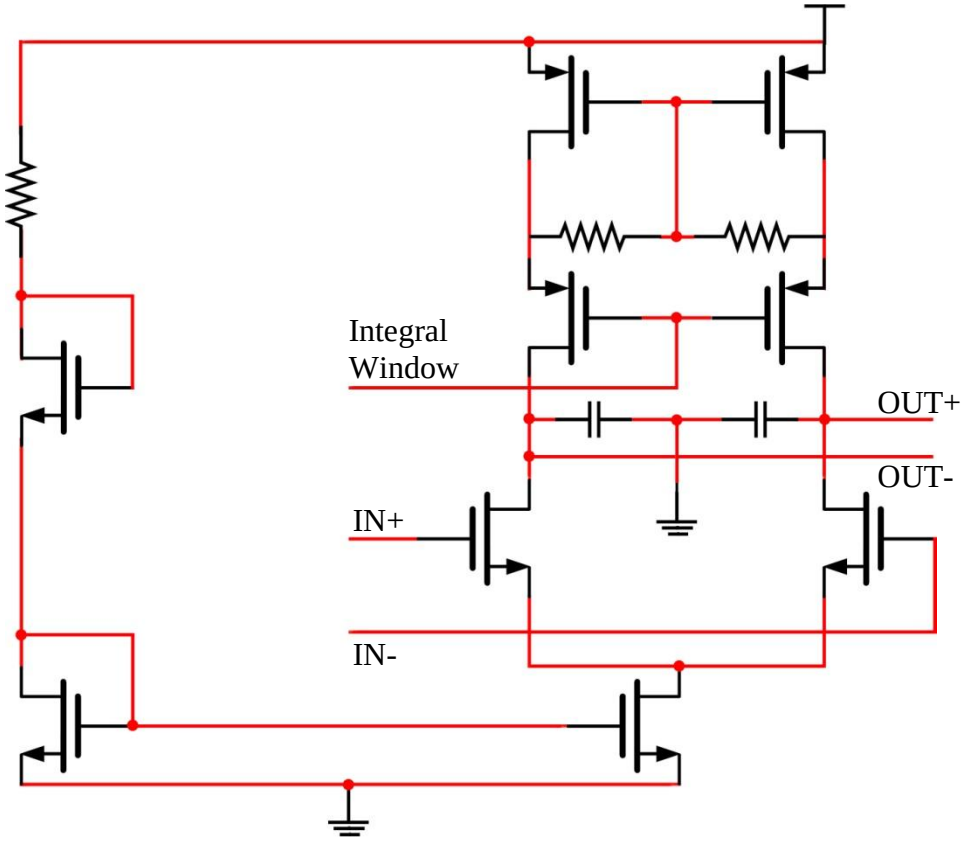


Figure 6.13. Schematic of the integrator

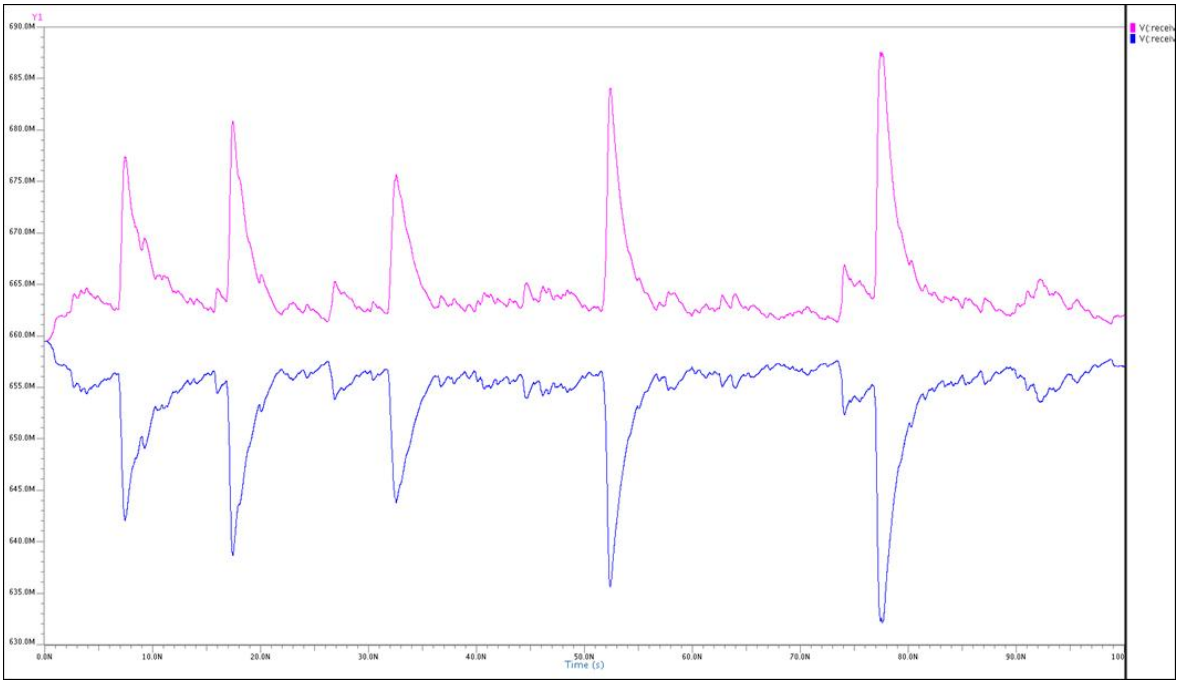


Figure 6.14. Differential output of the integrator

The integrator is followed by a PMOS differential amplifier (Figure 6.15) to convert differential-ended signal to single-ended one. Since, the comparator circuit operates with single-ended signals. PMOS transistors are preferred to realize this topology since, the comparator accepts positive-peaked pulses and PMOS transistors pull voltage level up to V_{DD} more easier than NMOS transistors.

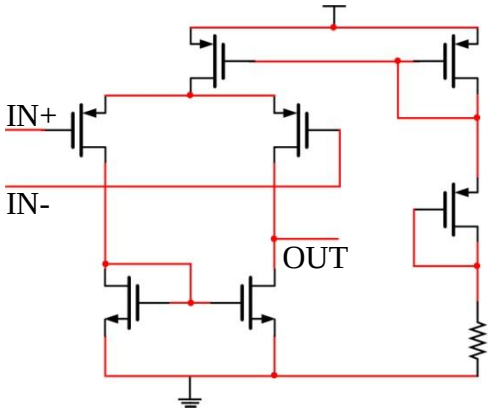


Figure 6.15. Schematic of the PMOS differential amplifier

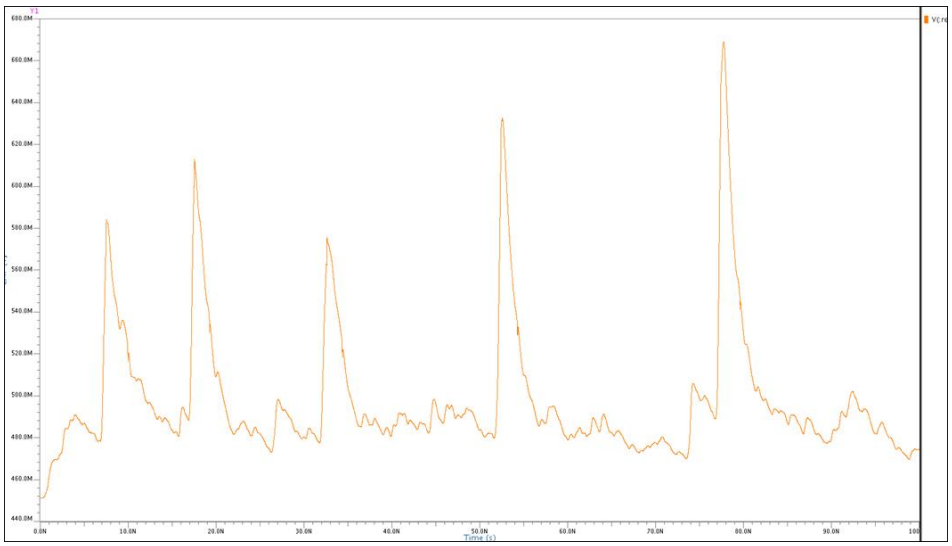


Figure 6.16. Output of the PMOS differential amplifier

PMOS differential amplifier is followed by the comparator which is actually a 1-bit ADC with hysteresis (Figure 6.17). A comparator normally changes its output state when the input voltage crosses through the reference voltage. Because of the noise on the input signal, small voltage fluctuations can cause undesirable rapid changes between the two

output states when the input voltage is close to the reference voltage. To prevent this output oscillation hysteresis property is added to the comparator.

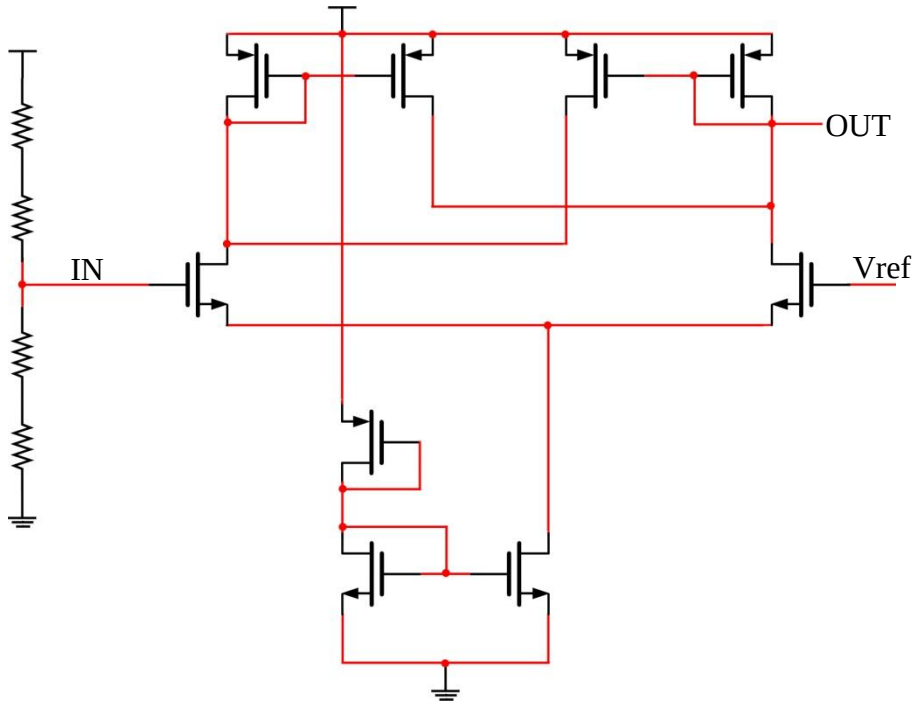


Figure 6.17. Schematic of the comparator

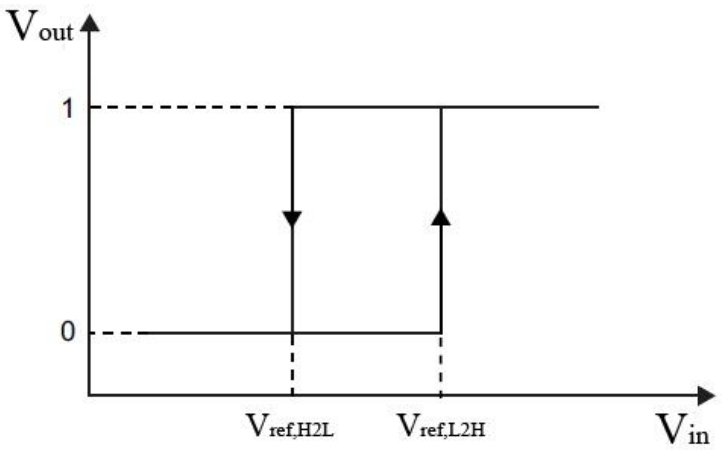


Figure 6.18. Hysteresis

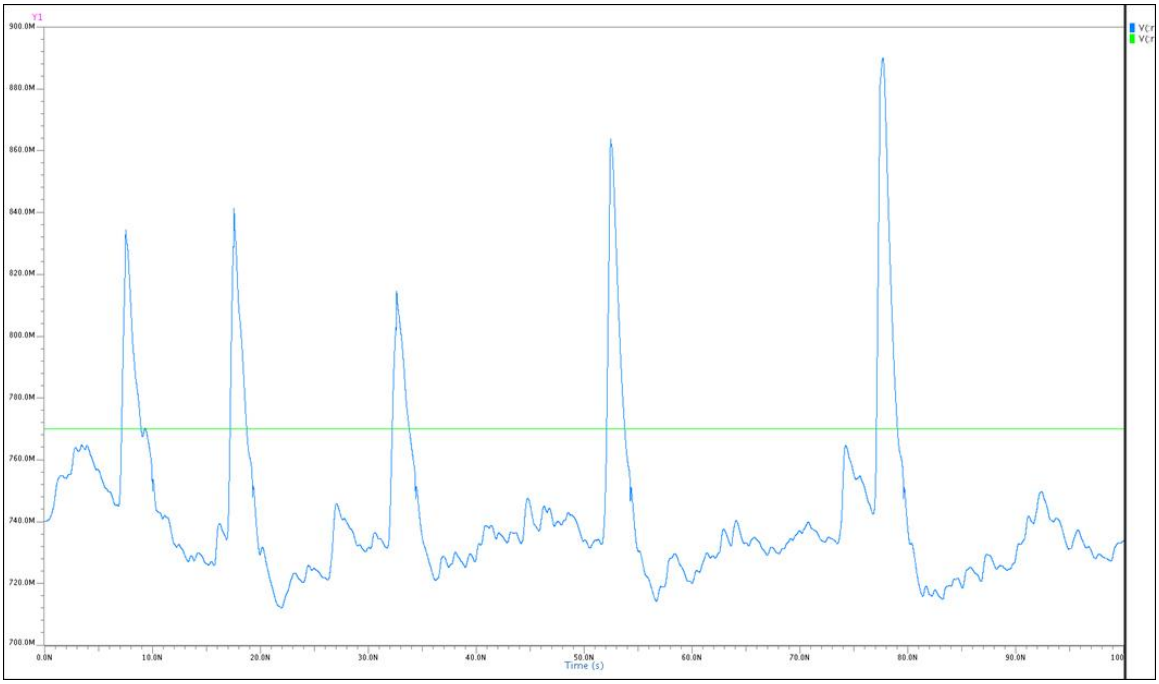


Figure 6.19. Signals at the input of the comparator

It is employed to detect whether its input is larger or smaller than a reference voltage which can be adjusted by *reference voltage* signal (Figure 6.4). At the end of this comparison, the original data sent by the transmitter is generated at the output of the comparator (Figure 6.20 (a)).

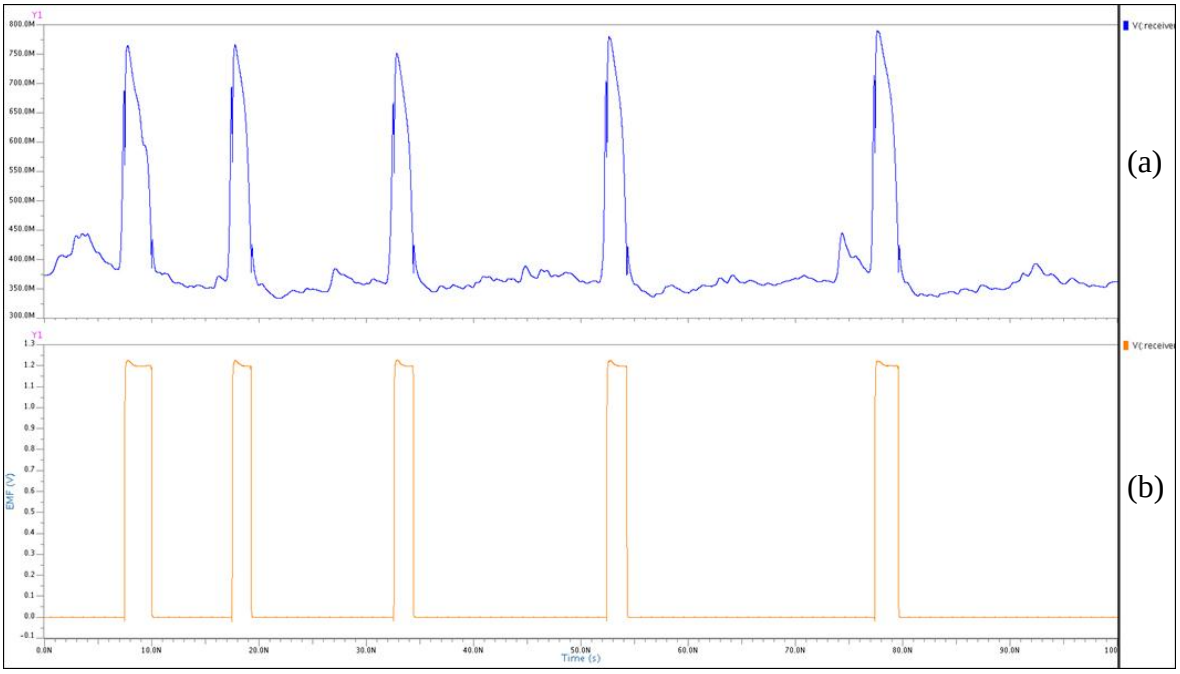


Figure 6.20. (a) Output of the comparator, (b) output signal after two inverters

The comparator is followed by a standard positive edge triggered D-type flip flop structure (Figure 6.21) and it operates as an OOK demodulator.

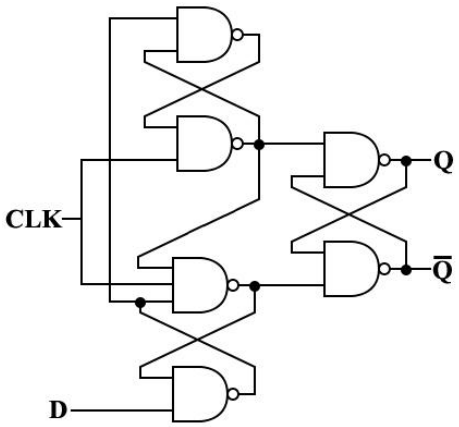


Figure 6.21. Schematic of the demodulator (DFF)

The amplitude of each pulse coming from the integrator is different (Figure 6.14). Therefore, each pulse has distinct widths on the reference voltage of comparator (Figure 6.19). Because of this, positive edge triggered operation principle is adopted. Nevertheless, it brings a disadvantage. For instance, a pulse that has a width smaller than the width of a

clock cycle and it exists between two consecutive positive edge of the clock signal cannot be sampled (Figure 6.22). Thus, one bit of the transmitted data is lost during demodulation.

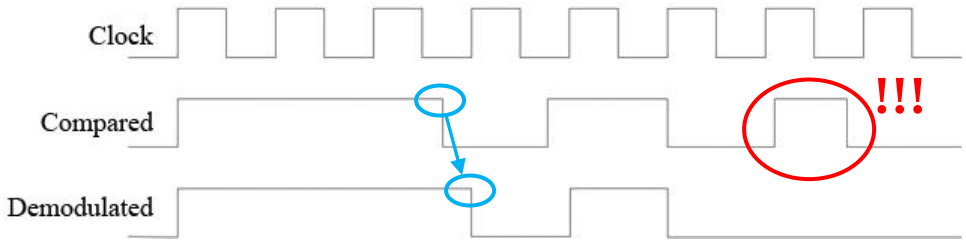


Figure 6.22. Operation principle of the DFF

Simulation result of the demodulator can be seen in Figure 6.23. Also, the signal at the end of the receiver chip measured from an RF pad in a simulation environment and is given in Figure 6.23.

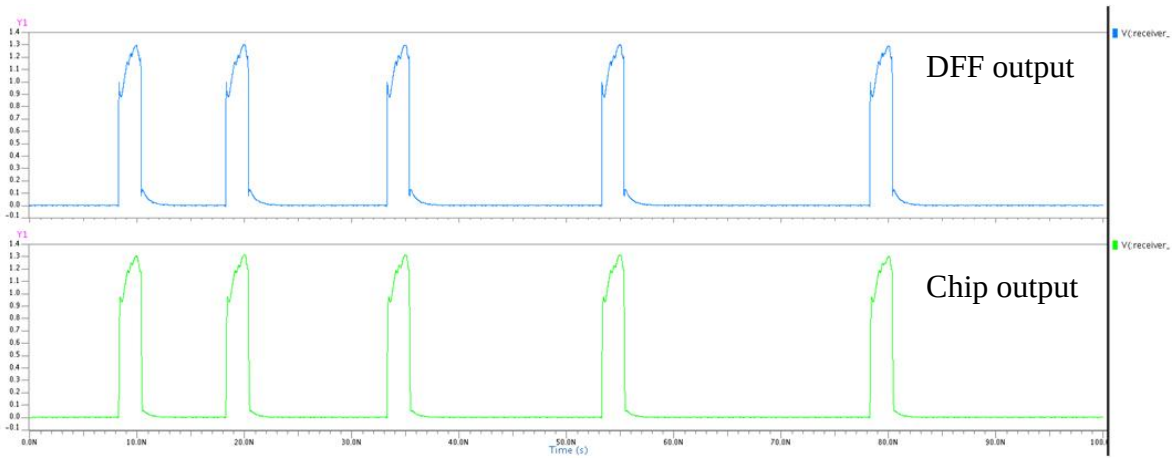


Figure 6.23. DFF and receiver chip output

7. TRANSISTOR LEVEL DESIGN OF PULSE GENERATOR

Pulse generator design is one of the important parts of a transceiver design process since it generates pulses for transmission and PSD of the generated signal is necessary for UWB communication because of the power limits and other regulations presented by FCC. Lots of topologies and pulse generation techniques are examined during the literature search. Two distinct pulse generator topologies and pulse generation techniques, which are presented in [18] and [19], are tested by using UMC's 130 nm CMOS technology in transistor level.

The first pulse generator is a fully integrated one. It accepts positive and negative transition pulses at its inputs and generates the desired pulse by an on-chip filter response. Second one is all-digital and fully integrated. This pulse generator generates UWB compatible pulses by combining four distinct pulses. Thus, it does not require a filter.

After this research period and simulations of various pulse generators, a new one that uses the combination of the former techniques is designed. First, it combines a positive and a negative peaked pulse then generates the desired pulse shape by using the response of an off-chip filter. A topology similar to this one is not presented up to now according to the designer's knowledge.

Aforementioned pulse generator circuits and their simulation results are presented in detail on the following pages.

Table 7.1. Properties of some pulse generators in the literature

	Technology	Power Consumption	V_{DD}	Frequency Range	Pulse Width	Area	Data Rate
[20]	IHP 0.25 µm SiGe:C BiCMOS	55 mW	2.5 V	3.1 - 5.1 GHz	1 ns		
[12]	AMS 0.35 µm CMOS	95 mW	3.3 V		230 ps		
[21]	0.18 µm CMOS	29.7 mW	2.2 V	3.1 - 5.15 GHz	920 ps	0.4 mm^2	10 Mbps
[18]*	ST-Microelectronics 0.13 µm CMOS	20 mW		3.1 - 10.6 GHz	92 ps	0.57 mm^{2+}	
[22]	0.18 µm CMOS	1.35 mW @ 10 MHz	1.8 V	3 - 10 GHz	380 ps - 4 ns		
[23]	0.35 µm CMOS	180 mW	3.3 V		1 ns		100 Mbps
[24]	IBM 0.13 µm CMOS	25 mA @ 1.2 V	1.2 V	4.2 - 9.7 GHz		1.25 mm^{2+}	
[25]	AMI 0.5 µm CMOS	1.88 mW @ 77 MHz	1.8 V	3.1 - 10.6 GHz		0.77 mm^2	
[26]	0.13 µm CMOS	10 mW	1.2 V	3.1 - 5 GHz	800 ps	1.56 mm^2	160 Mbps
[19]*	0.18 µm CMOS	15.4 mW @ 500 MHz	1.8 V	3.1 - 10.3 GHz	380 ps		
D	**UMC 0.13 µm CMOS**	**3.9 mW @ 500 MHz**	**1.2 V**	**3.1 - 5.1 GHz**	**1 ns**	**0.094 mm^2**	**Up to 1 Gbps**

* Tested pulse generators, $^+$ Area with on-chip filter

D: Designed pulse generator in this thesis

7.1. Fully Integrated CMOS UWB Pulse Generator

An UWB pulse generator integrated circuit (IC) structure that operates in the 3.1 GHz – 10.6 GHz band is presented in [18]. The circuit is redesigned in UMC 0.13 μm CMOS technology to test it is appropriate or not for the specs.

First of all, the designer should beware of some topics during design process of a pulse generator such as:

- PSD of the output signal of a pulse generator must obey the FCC regulations to optimize the radiated power.
- To operate on a wide frequency band, complexity of the circuit should as low as possible.
- Integration of digital and analog parts of the circuit can be realized with a low cost technology.

The operation principle of the fully integrated pulse generator is based on the response of an on-chip filter to a given impulse. Because of its being completely integrated, this circuit does not require any off-chip capacitor, inductor, etc. to generate a Gaussian pulse or its derivative. As can be seen in Figure 7.1, the circuit is composed of two main parts one of which is a digital pulse generator and the other one is on-chip band pass filter. The filter seen in Figure 7.1 is a 3^{rd} order Bessel band pass filter. A 3^{rd} order filter is used as, the order of the filter is appropriate for low power rules of FCC. The filter is a necessary part of the circuit since the pulse generation technique consists of applying a square function to the filter input to generate its equivalent Dirac response [18].

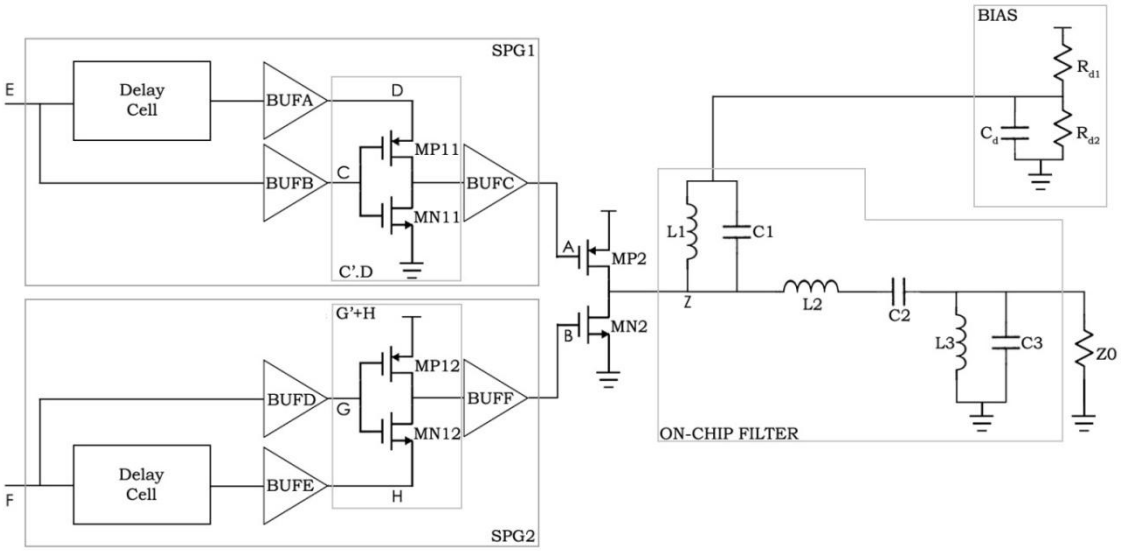


Figure 7.1. Schematic of the redesigned pulse generator

Quality factors (Q) of inductors are the key parameters in the design process of an RF CMOS filter since, in a standard CMOS process, Q highly depends on the inductor value and it has really low values. Nevertheless, Q should have relatively higher values to limit losses.

The most important part in the design of an UWB pulse generator is to generate a pulse which

- Should have a low power consumption,
- Should have a sufficient amplitude on a wide bandwidth (e.g. > 7 GHz) and
- Should have as short as possible rise and fall time.

Two complementary switches, *MP2* and *MN2*, are controlled by two complementary square pulse generators, *SPG1* and *SPG2*, and they generate bipolar pulses.

Table 7.2. Transistor dimensions of complementary switches

	MP2	**MN2**
W / L (µm)	80/0.12	70/0.12

Positive and negative transition (on E and F) is given to SPG1 and SPG2, respectively, to generate a narrower negative and positive pulse on A and B. A delay cell and a digital gate, which achieves the function $\bar{C}.D$ and $\bar{C}+D$, is used to generate these pulses. While $\bar{C}.D$ function is used for SPG1, $\bar{C}+D$ is used for SPG2. According to the simulations, 500 ps width pulses at the input generate 100 ps width pulses at the output.

In this topology, six buffer block (BUFA – BUFF) exist and there are six inverters in each of them.

Table 7.3. Transistor dimensions of buffers

	1st	**2nd**	**3rd**	**4th**	**5th**	**6th**
W_P / L_P (µm)	23.1/0.12	25.7/0.12	30/0.12	36/0.12	42/0.12	48/0.12
W_N / L_N (µm)	9.6/0.12	11.1/0.12	12.9/0.12	15/0.12	17.4/0.12	20.1/0.12

Delay cells used in SPG blocks are composed of two current starved inverters. The topology of delay cells is not given in [18] therefore, at the end of a literature search an appropriate structure (Figure 7.2) is chosen. The circuit has an advantage of delay time control which can be done with *sel_rangeN* and *sel_rangeP* signals. This provides better delay matching between the pulses at the input of BUFA-BUFB and BUFD-BUFE. Also, the glitches on the signal of SPGs can be lowered as much as possible by adjustable delay times.

Table 7.4. Transistor dimensions of delay cell

	M1	**M2**	**M3**	**M4**	**M5**	**M6**	**M7**	**M8**	**M9**
W (µm)	9.6	9.6	6.4	1.6	3.2	3.2	3.2	3.2	3.2
L (µm)	0.12	0.12	0.12	0.12	0.12	0.12	0.12	0.12	0.12

Bias voltage at node Z is set to $V_{DD}/2$ with R_{d1} and R_{d2} through the LC input network (L_{p1} and $C1$) to enable bipolar pulse generation on the output resistor. The value of C_{d1} should be much greater than the one of $C1$ to decrease the bias network influence on the generated pulses.

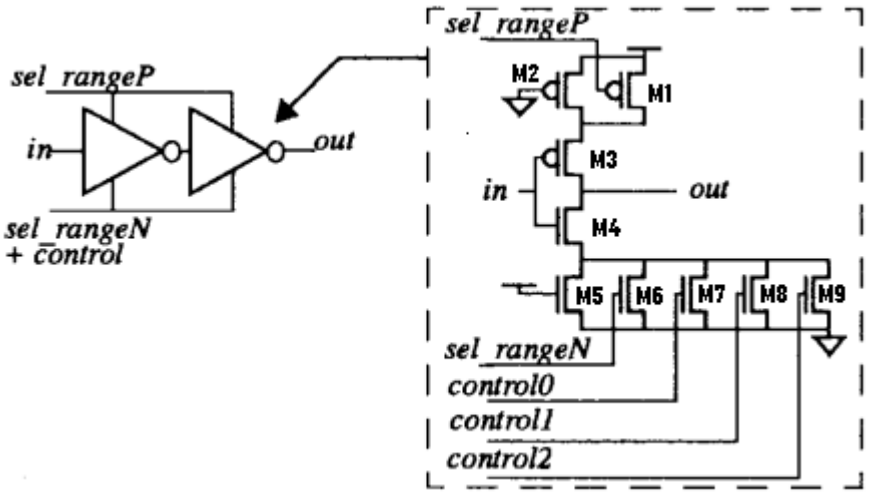


Figure 7.2. Schematic of delay cell

Time domain simulations show that the whole system is capable of generating the desired bipolar pulses (Figure 7.3 (a)). PSD of the generated signal fits to the FCC mask as can be seen from Figure 7.3 (b). The system consumes approximately 14 mW and amplitude of the generated signal has an approximate value of 300 mV.

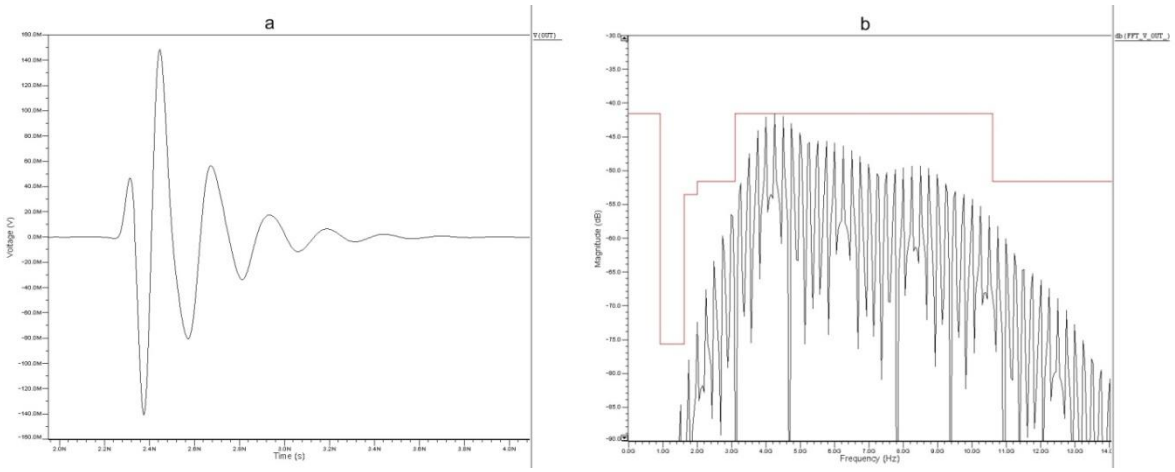


Figure 7.3. (a) Output signal on 50 ohm load resistor and its (b) PSD

7.2. All-Digital Low-Power CMOS Pulse Generator for UWB System

IR technology uses a single pulse as a carrier and it is generally chosen as a Gaussian pulse. Nevertheless, 1st and 2nd order derivatives of a Gaussian pulse must be filtered to

obey the FCC regulation which is given in [27]. Additionally, the current source consumes power constantly to generate pulses and it increases the total power consumption of the system. Nowadays, power consumption can be regarded as the most important parameter in IC design. Therefore, the pulse generated should be designed with a power efficient scheme and it must fit the FCC mask at the same time. As stated before (Figure 4.2), 5th order derivative of a Gaussian pulse has the most effective frequency spectrum under the FCC floor and it can be transmitted without any filtering process [28].

The procedure that generates the 5th order derivative of a Gaussian pulse is very complex and the circuit that realizes it is not suitable for low power transceiver systems. In Figure 7.4 (a), a pulse generator that generates an UWB pulse which obeys the regulations can be seen. It is composed of two main parts and given in [19]. One of these two is a digital triangular pulse generator and the second one is an output stage that drives a 50 ohm load resistor.

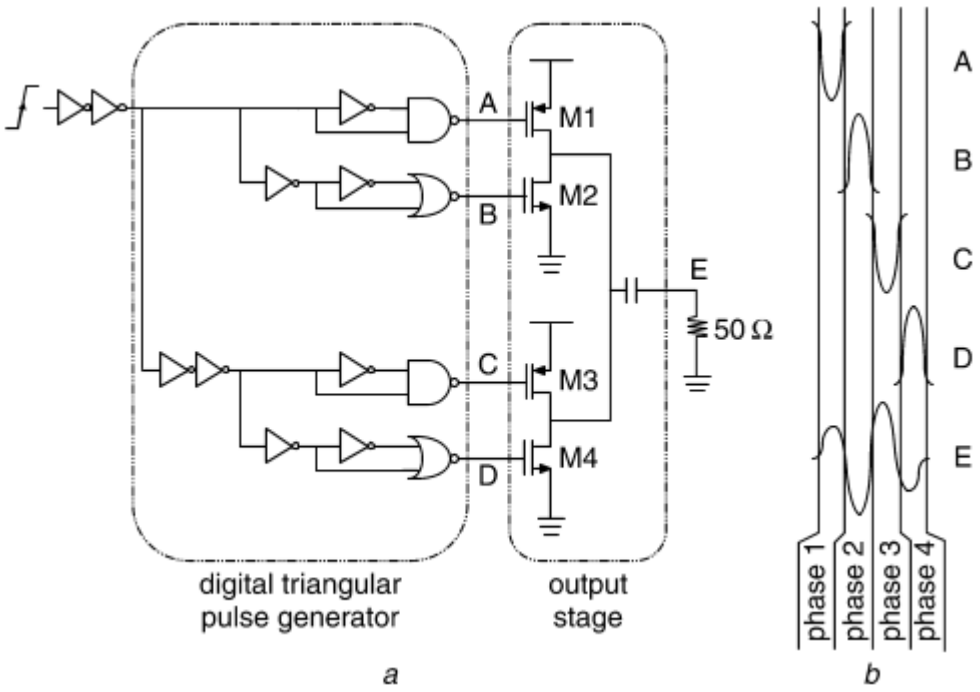


Figure 7.4. (a) Schematic and (b) pulse shapes on nodes A,B,C,D and E [19]

The square pulse at the input and its inverse is given to a NOR and a NAND gate, respectively. Since, a NAND gate generates “0” when both inputs are “1” while, a NOR

gate generates “1” when both inputs are “0”. This gives the desired triangular pulses on nodes A, B, C and D (Figure 7.4 (b)). As a result, a negative-peak triangular pulse (from V_{DD} to the ground) is generated on nodes A and C by NAND gates while, a positive-peak triangular pulse (from the ground to V_{DD}) is generated on nodes B and D by NOR gates. Each triangular pulse should have the same pulse width as much as possible and they can be adjusted by changing the dimensions of M1-M4. The delay of each pulse should also be adjusted very carefully to generate a smooth 5^{th} order derivative of the Gaussian pulse since, it is a sub-nanosecond process and very easy to get an unwanted signal on the load resistor. In this topology, the delay of a pulse can be adjusted with a high sensitivity by changing the number of the inverters and the dimensions of the transistor in them. Four triangular like pulses generated in digital triangular pulse generator are combined at the output stage to get the desired pulse. Additionally, output current value can be adjusted by changing the dimensions of four transistors form the output stage. One of the most important things about this topology is the power requirements. In each phase, only one transistor is on therefore, the circuit consumes low power.

Schematic of the NOR gate is shown in Figure 7.5. It is composed of two parallel p-channel metal-oxide-semiconductors (PMOS), which pull-up the output to V_{DD}, and two parallel n-channel metal-oxide-semiconductors (NMOS), that pull-down the output to the ground. According to this topology, the circuit constantly consumes power apart from the situation that both inputs have “1” or “0”.

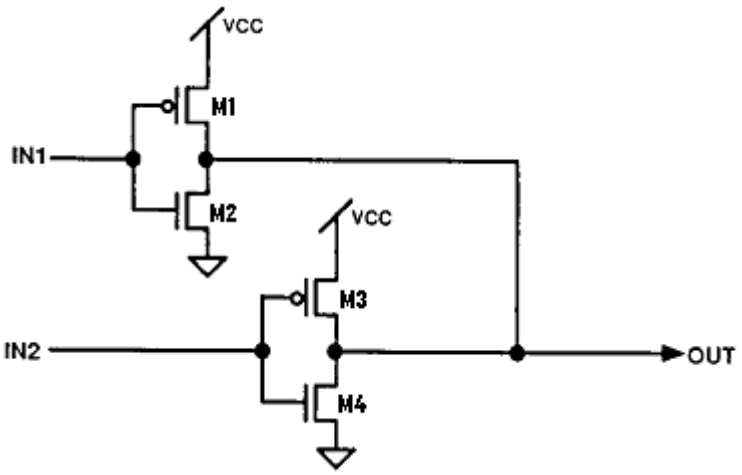


Figure 7.5. Schematic of the NOR gate [29]

An NMOS must drive a PMOS, that loads the output node, and pull-down the output to the ground to generate an acceptable logic "0". Transistor dimensions should be designed according to this operation principle and the designers generally choose the ratio given below:

$$\frac{(W/L)_{PMOS}}{(W/L)_{NMOS}} \leq MAXRATIO. \tag{7.1}$$

MAXRATIO is determined according to the operating conditions and process parameters. Classically, *MAXRATIO* is selected such that the output low level is always smaller than the NMOS threshold voltage [29]. To guarantee that voltage level of the logic "0" at the output is as low as possible, the dimensions of the PMOS transistors are determined by multiplying the ratio of dimensions of the NMOS transistors with *MAXRATIO*.

Table 7.5. Transistor dimensions of NOR gate

	M1	**M2**	**M3**	**M4**
W / L (µm)	15/0.12	21/0.12	15/0.12	21/0.12

A standard NAND gate topology is used for the pulse generator in Figure 7.4 and it is taken from [30]. Dimensions of the transistor used in this gate are determined by observing the simulation results during the design process.

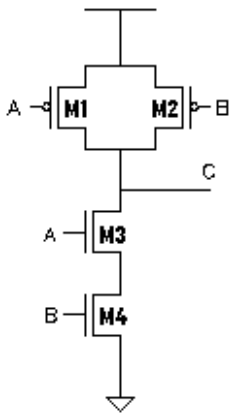


Figure 7.6. Schematic of the NAND gate

Table 7.6. Transistor dimensions of NAND gate

	M1	**M2**	**M3**	**M4**
W / L (µm)	25/0.12	25/0.12	25/0.12	50/0.12

The pulse generator written above is designed by using UMC 0.13 µm CMOS technology. It operates with 1.2 V source voltage and simulated in *Mentor Graphics*. Figure 7.7 (a) shows the pulse shape at the output node and Figure 7.7 (b) shows the power spectral density of that pulse shape with FCC mask. As it can be observed from the figure, between some frequency intervals, PSD violates the FCC mask. The system consumes approximately 5 mW and amplitude of the generated signal has an approximate value of 70 mV.

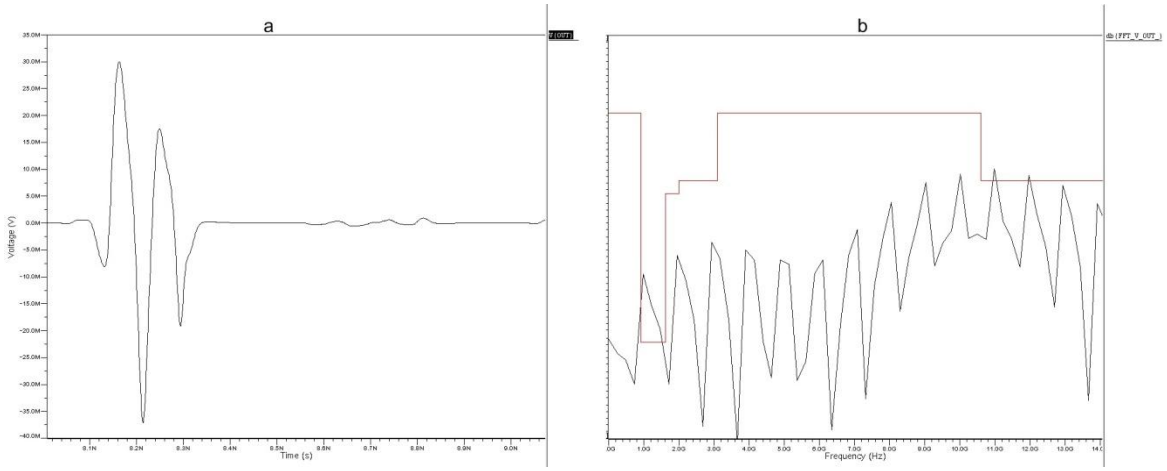


Figure 7.7. (a) Output signal on 50 ohm load resistor and its (b) PSD

This simulated pulse generator is able to generate a pulse which almost fits to the FCC mask over a wide frequency band with narrow violations. For the sake of power efficiency, there is no current source in the circuit [19]. The presented technique with this pulse generator gives the opportunity of decreasing power consumption in accordance with the pulse repetition frequency (PRF).

7.3. Glitch Generator Based Pulse Generator with Filter

Pulse generators written above have high DC power consumption values for the transmitter since modern transceivers require pulse generators that consume low power. This can be done by designing the circuit in a way that it should consume high power when they are generating required pulses and as much as low power when no pulse is being generated. In addition, the pulse generators above also generate some undesired glitches after the required UWB compatible pulse (Figure 7.8). These glitches should not be generated since, they have adverse effects on PSD of the UWB pulse. Besides, glitches may cause FCC mask violation in some conditions. Thus, a new topology is designed for the transmitter.

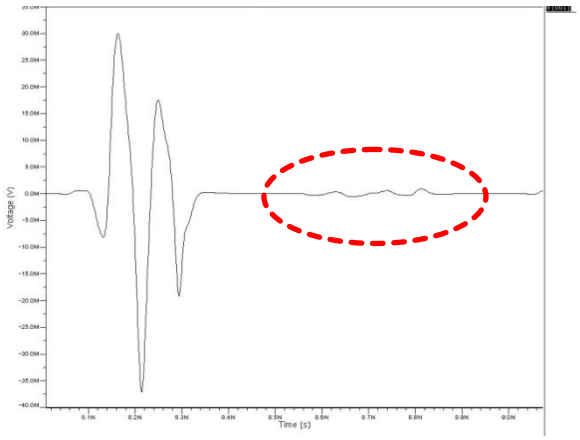


Figure 7.8. Undesired glitches on UWB pulse

This topology does not exist in the literature according to knowledge of the designer. It is based on a glitch generator circuit presented in [30] and designed by combining the techniques that are used in the formerly tested pulse generator circuits. The glitch generator can be seen in Figure 7.10.

A clock signal is given to the input of the glitch generator. On every rising edge of the clock it generates a very narrow pulse. When *PG_IN* = 0, node *NAND_INA* is charged up to V_{DD} (*X6* is off since *GG_OUT* is low). On the rising edge of the clock, there is a short period of time when both inputs of the NAND gate are high, causing *GG_OUT* to go high. This in turn activates *X6*, pulling *NAND_INA* and eventually *GG_OUT* low (Figure 7.9).

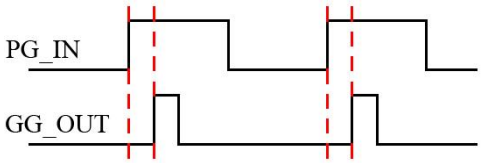


Figure 7.9. Input and output signals of the glitch generator

The length of the pulse is controlled by the delay of the NAND gate and the inverter. Note that there exists also a delay between the rising edges of the input clock (*PG_IN*) and the glitch generator output (*GG_OUT*).

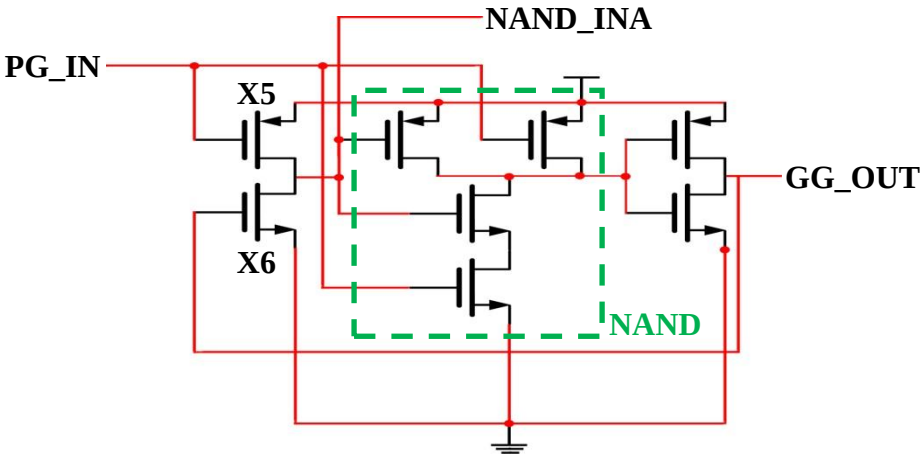


Figure 7.10. Glitch generator

This glitch generator topology (Figure 7.10) has the advantage of generating pulses as narrow as possible without undesired glitches. Besides, it has a very simple structure which requires only 8 transistors. Another advantage of this output stage is low power dissipation. Since, only one transistor is on at a time only when the pulse reaches to the related transistor and this operation principle decreases the DC power consumption of the transmitter.

The glitch generator employed generates one pulse nevertheless, 4 pulses are required to generate a 5^{th} order derivative of the Gaussian pulse and these 4 pulses must be combined at the output port. For this operation, the output stage given in [19] is used (Figure 7.11 (a)). This circuit is chosen because of the simplicity of its structure and operation method. It merges the pulses at the input to generate a UWB compatible pulse at

the output (Figure 7.11 (b)). Two of these pulses are positive peaked and rest of the four is negative peaked. Each of them reached to the output stage at different times.

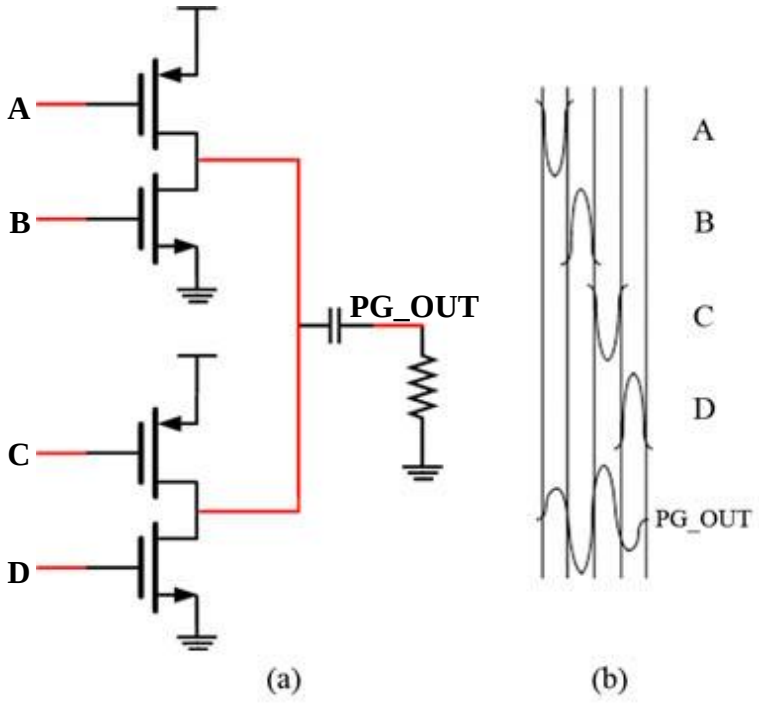


Figure 7.11. (a) Output stage and (b) the desired pulses at the input of it

The resultant bipolar 5th order derivative of the Gaussian pulse is generated on a 50 ohm load resistor by drawing current from (at positive peaked pulses through NMOS transistors) or supplying current to (at negative peaked pulses through PMOS transistors) a capacitor connected to the output of the pulse generator.

When the required pulses are examined, the similarity between them can be seen. The designed glitch generator generates a positive peaked pulse. Therefore, pulses A, B, C and D can be obtained by adding some inverters to the circuit. The inverter chain used to get pulse A and B can be seen in Figure 7.12 and they are also used for generating pulse C and D. Designed pulse generator circuit composed of two glitch generators, each one is for a pair of pulses A,B and C,D. Thus, two distinct branches of inverter chains exist.

Using inverters for obtaining the pulses gives the advantage of adjusting the delay time between each other by changing the number of inverters or the size of transistors.

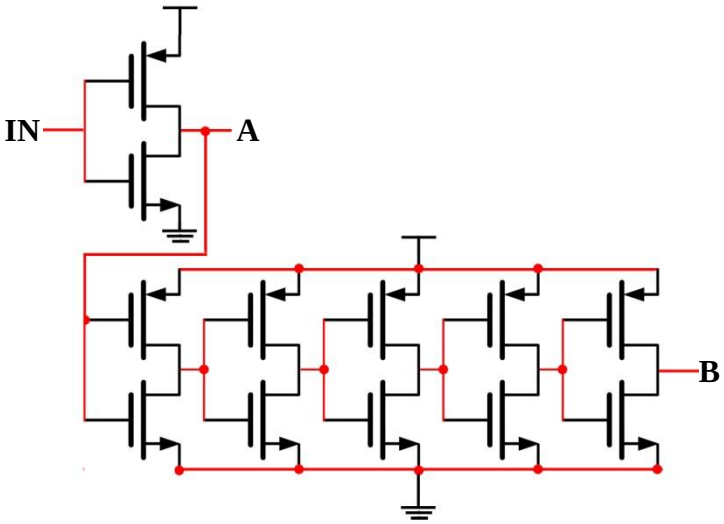


Figure 7.12. Inverter series for pulse A and B

However, delays of the pulses should be adjusted in a very sensitive manner as, they have sub nanosecond widths. For instance, pulse B must start to rise as soon as possible after the pulse A finishes. Delay between pulses is not the only important factor for pulse generation. Pulse width is also important. It can be increased or decreased to some extent since the shape of the resultant pulse can be deteriorated according to the width of one of four pulses. The second advantage of using inverters is the absence of glitches at the pulse generator output.

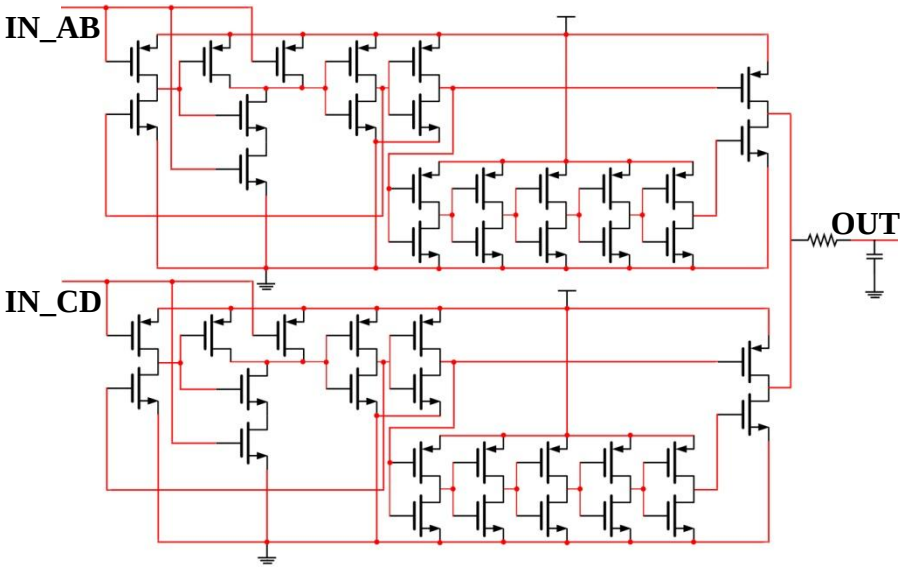


Figure 7.13. 5th order derivative Gaussian pulse generator with two delay paths

At the end of the transient simulations, it is observed that the pulse generator circuit is capable of generating the 5th order derivative of the Gaussian pulse that has a similar shape to the ideal one. The obtained pulse shape is depicted in Figure 7.14. Glitches that come after the actual pulses are not generated. Thus, the signal power that is very important for UWB communication remains on the actual pulse. In addition, as it is written in former paragraphs, DC power consumption is decreased by this topology and the simulator software calculates the dissipated power level around μW.

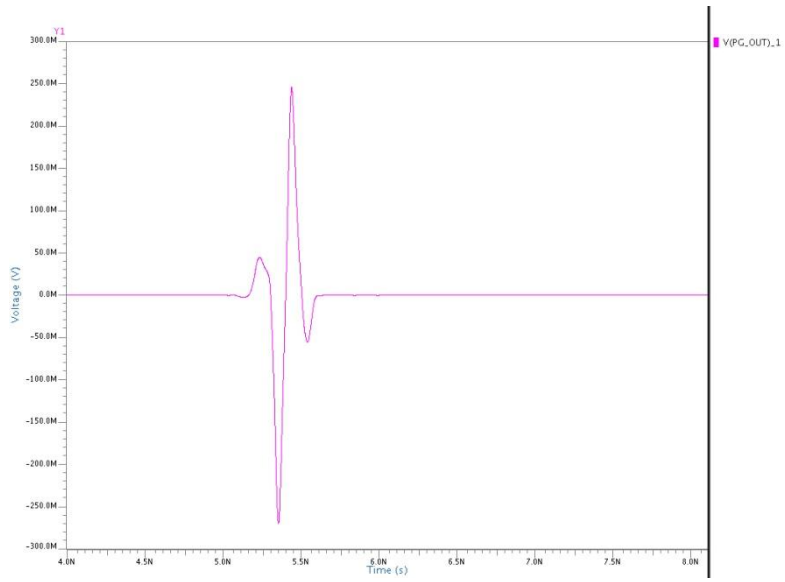


Figure 7.14. Generated 5th order derivative of the Gaussian pulse

After transient simulations, corner case analyses of the circuit are done to see how it responds to process variations. The term corner refers to the variations of technology parameters during manufacturing of transistors in foundry. Corner analysis is a worst-case approach where multiple corners of process can be simulated by using an appropriate parameter file. With the help of these simulations, designers can foresee the problems that may arise during manufacturing process and take precautions by making changes on the design. In the design kit provided by UMC five corner cases exist (Figure 7.15). These are:

- Typical NMOS – Typical PMOS (TT),
- Slow NMOS – Slow PMOS (SS),
- Fast NMOS – Fast PMOS (FF),

- Fast NMOS – Slow PMOS (FS) and
- Slow NMOS – Fast PMOS (SF).

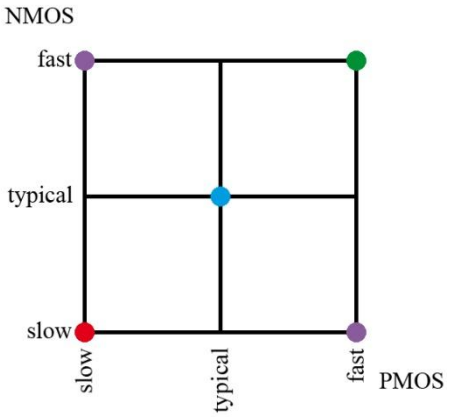


Figure 7.15. Corner cases

These five cases are used during the simulation process of the pulse generator. Simulation results of the cases TT, FS and SF are come up as expected (Figure 7.16) while the remaining corners cause some problems on the pulse shape and consequently on PSD.

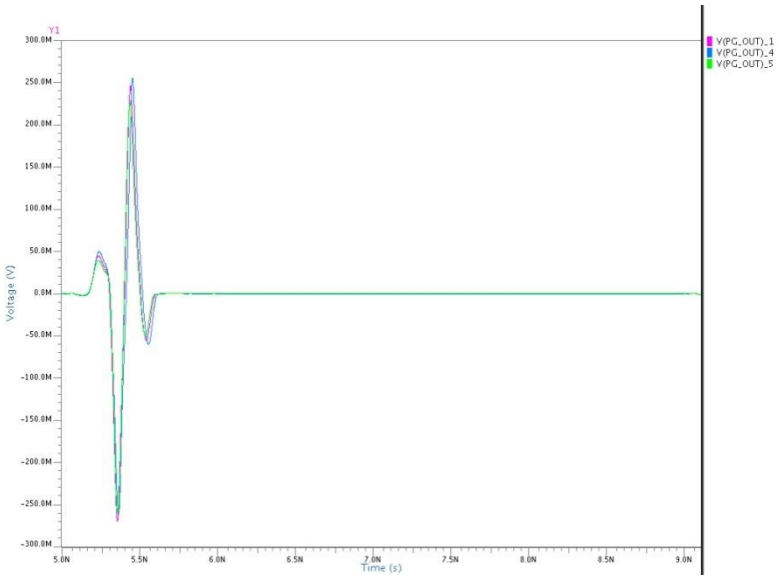


Figure 7.16. TT, FS and SF corner case simulation results

Amplitude and width of the output pulse have small variations for TT, FS and FS corners. As it is known, PSD shape of a pulse is strongly related to its width and amplitude. Small variations on designed pulse do not have massive effects on its PSD. On the other hand, in SS and FF corners, these variations increase on pulse shape at the output (Figure 7.17) and they affect the PSD adversely. Therefore, effects of corner cases should be minimized to be sure to get an FCC mask compatible transceiver after manufacturing process. The sensitivity of pulse generation operation leads to this inconsistency seen between corner cases during simulations since the operation principle of this topology requires accurate timing between four pulses and it is affected excessively when all types of transistors operates in slow or fast mode.

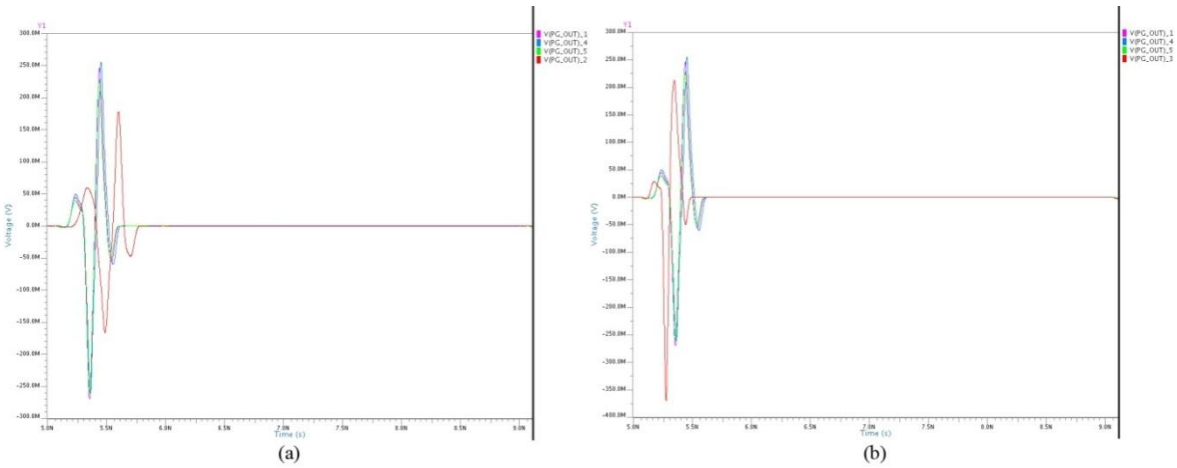


Figure 7.17. (a) SS and (b) FF corners compared with the other ones

As it can be seen from Figure 7.17 (a), width of the pulse obtained in SS corner is wider than the pulses seen in TT, SF and FS corners. On the other hand, pulse amplitude in SS corner is smaller than the amplitudes of pulses in TT, SF and FS cases. Additionally, pulse amplitude in FF corner is larger than the amplitudes of pulses in TT, SF and FS corners while the pulse in FF is wider. In consequence, PSD shape is affected adversely. Differences of some parameters according to various corners are shown in Figure 7.18.

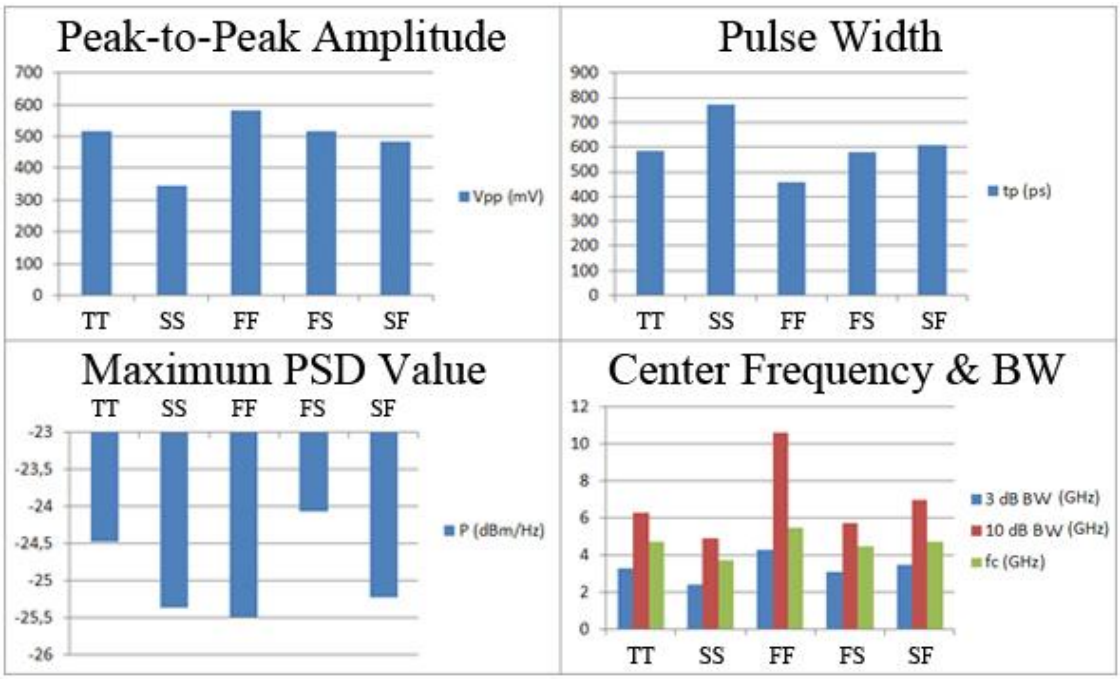


Figure 7.18. Differences of parameters according to 5 corner cases

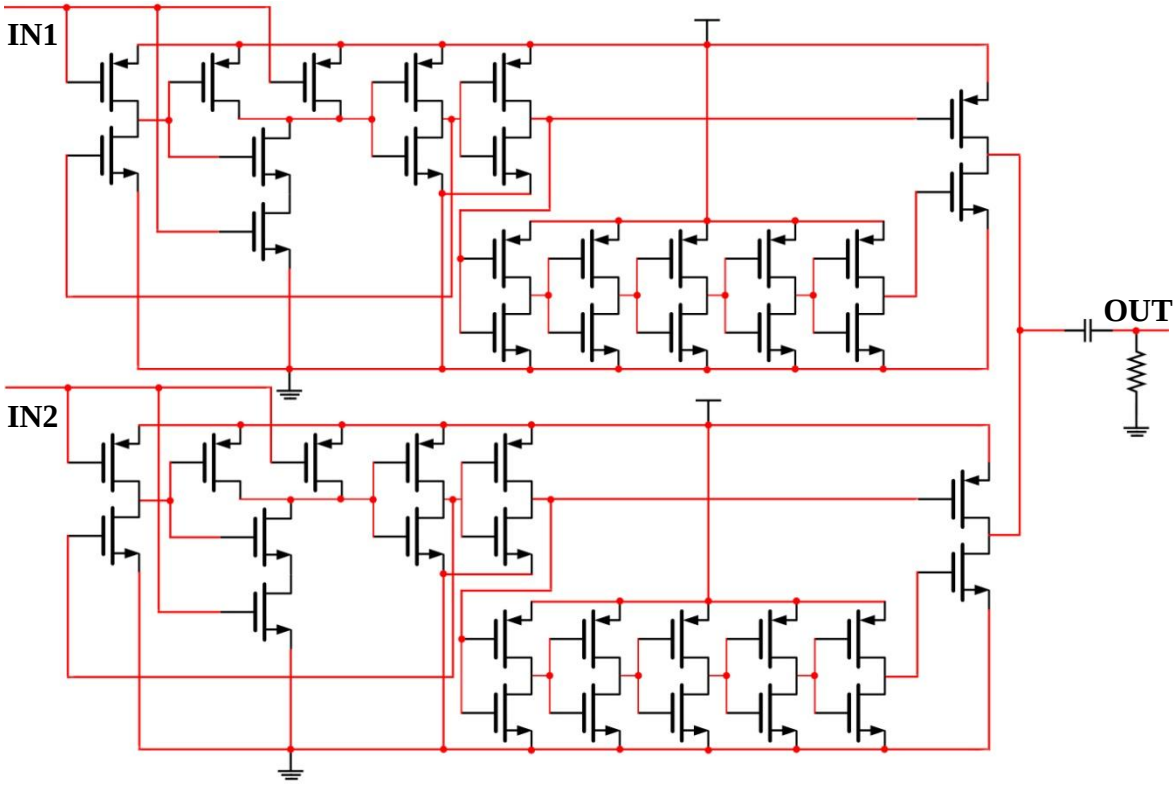


Figure 7.19. 5th order derivative Gaussian pulse generator with one delay path

Due to the discrepancies of some important parameters in various corners, redesigning the circuit became a necessity. The circuit based on glitch generators written above generates four pulses by using two glitch generators for two delay paths. In fact, these four pulses are inverses of each other and they can be generated by using one glitch generator over a single delay path with the help of appropriate number of inverters. As a result, a new circuit comes up which is given in Figure 7.19.

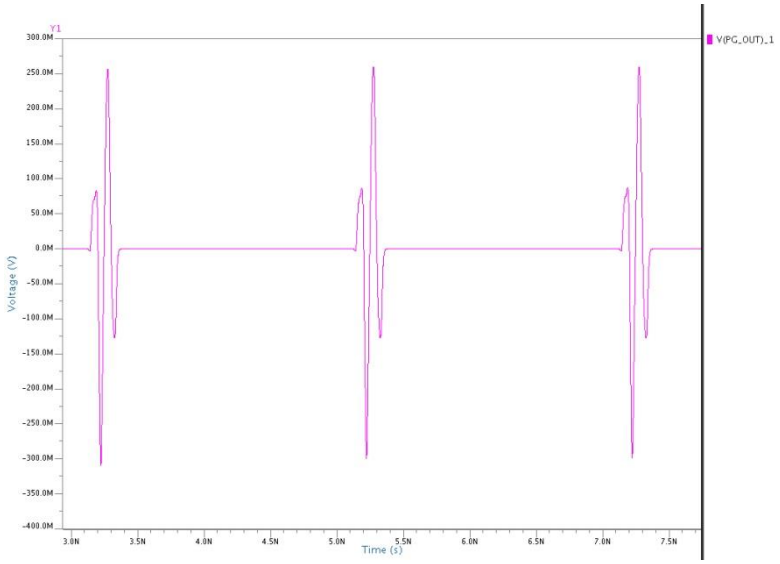


Figure 7.20. Output pulse of the circuit in Figure 7.13

After transient simulations, it is seen that the circuit is operational. In addition, DC power consumption is smaller than the one with two glitch generator as expected. Nevertheless, because of the similar operation principle, PSD shape of the output pulse of this circuit also varies too much in SS and FF corners while the output pulse for remaining corners are acceptable (Figure 7.21). On the other hand, output pulse for SS and FF corners is given in Figure 7.22 to make a comparison with the output pulse for TT case.

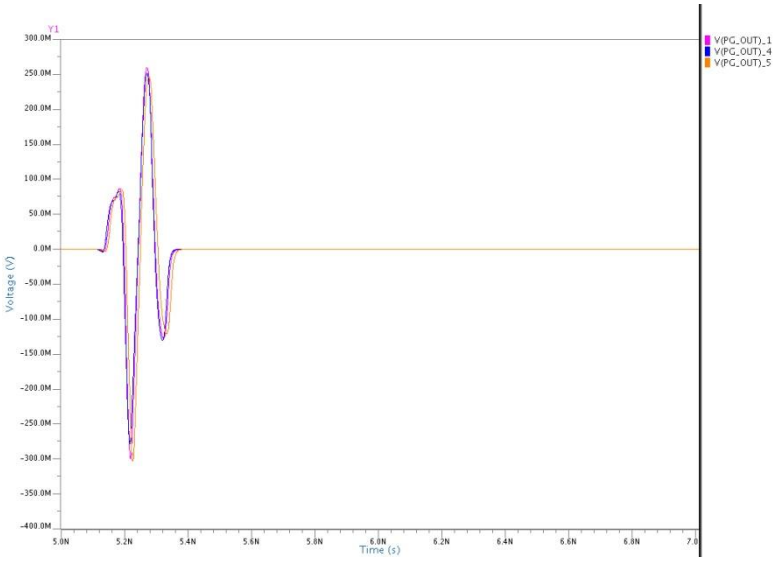


Figure 7.21. Output pulse for TT, SF and FS corners

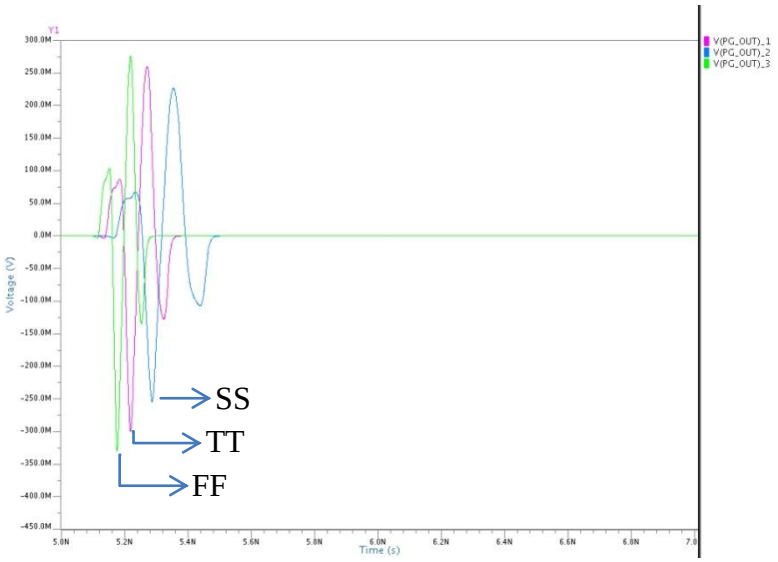


Figure 7.22. Output pulse for SS, TT and FF corners

Differences of some parameters according to various corners are also shown for this circuit in Figure 7.18.

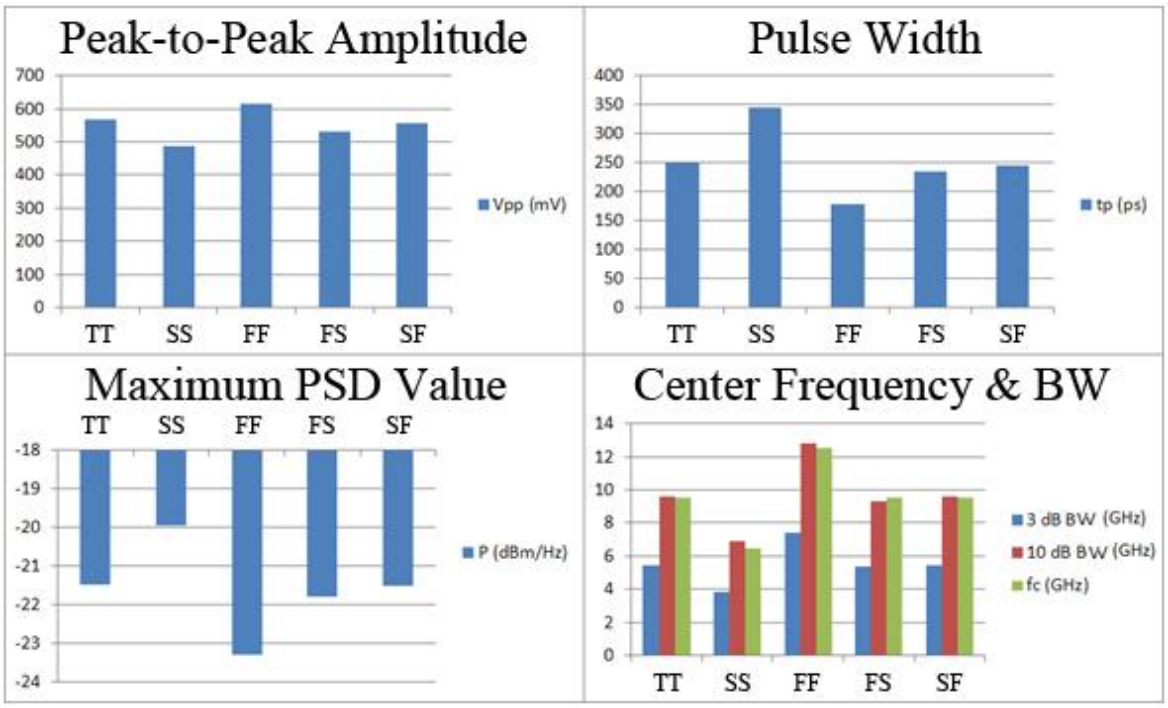


Figure 7.23. Differences of parameters according to 5 corner cases

As it can be observed from Figure 7.18 and Figure 7.23, center frequency, f_c, of PSD shape differs from one corner to another and this situation is not good for UWB communication. Not only f_c but also bandwidth must be as stable as possible for the transmitter designed. Meanwhile, the chosen operation bandwidth (from 3.1 GHz to 10.6 GHz) at the beginning of the project is changed because of the design challenges that may be encountered. For instance, designing an ADC which operates at 10 GHz is very difficult. Therefore, 2 GHz wide new operation band is decided between 3.1 GHz and 5.1 GHz. In consequence, the generated pulse is required to be changed since the frequency spectrum of a 5^{th} order derivative of the Gaussian pulse spans over a wider bandwidth (Figure 5.5 (b)). Various possible solutions exist to fit in a 2 GHz wide bandwidth, one of which is to generate a higher order Gaussian pulse as, the PSD bandwidth decreases with increasing derivative order of the Gaussian pulse. A second solution is to take the derivative of the generated pulses at the output port and the last feasible way is to use an on or off-chip filter.

The first method has some disadvantages. First of all, circuit complexity is increased if the tested two topologies are used. Second, more pulses are needed two generate higher

order derivatives of the Gaussian pulse which means more accurate timing between pulses is required and the number of inverters must be increased. Also, the output stage must be modified according to the desired pulse. Besides, PSD of the signal generated by the last two topologies cannot be controlled under different corners.

Second solution is adding extra derivation circuitries to the output of the pulse generator to get a higher order derivative of the Gaussian pulse. For instance, for getting a 7^{th} order Gaussian pulse, the circuit given in Figure 7.24 should be added to the designed pulse generators. Because of the existence of C and L it takes up lots of real estate which is very precious for an IC. Besides, 7^{th} derivative of a Gaussian pulse has a wider bandwidth on frequency spectrum than the required 2 GHz bandwidth (Figure 4.2).

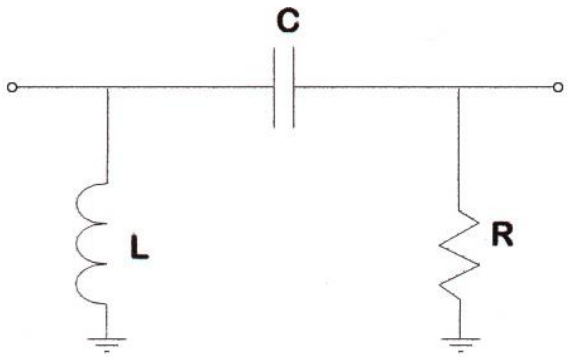


Figure 7.24. Second order derivation circuitry

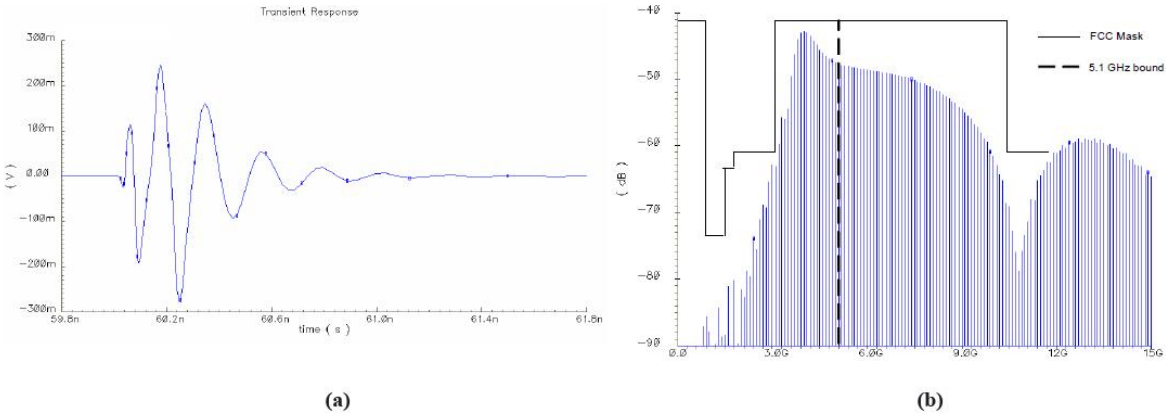
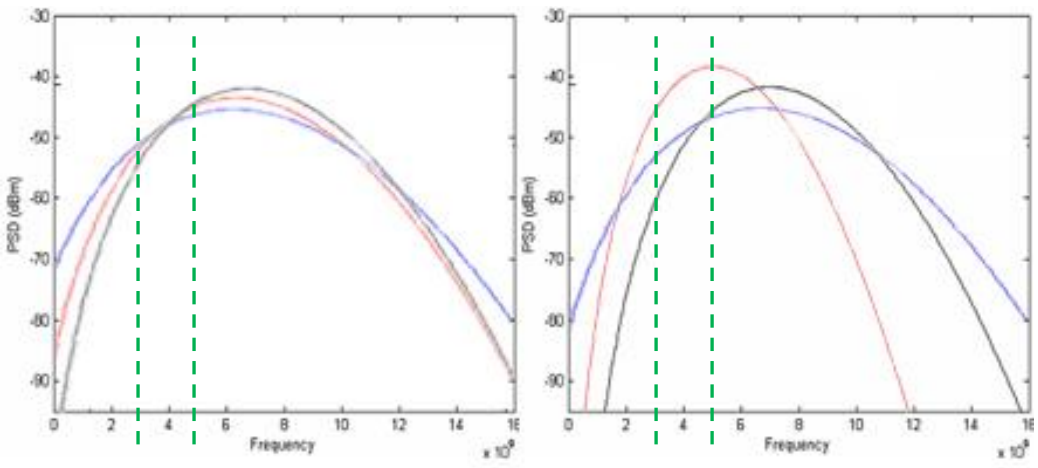


Figure 7.25. (a) 7^{th} order derivative of the Gaussian pulse and its (b) PSD

In fact, the second possible solution is tested before in [31]. In Figure 7.25, generated pulse and its PSD can be seen. Nevertheless, it is risky to use this principle since, only 3 dB-bandwidth fits between 3.1 GHz-5.1 GHz. If 10 dB-bandwidth is considered it fits between a much wider frequency band. Besides, no corner case simulation results are given in [31]. According to our experience, using this circuitry with a pulse generator that uses pulse combination technique is not beneficial in terms of corner case performances while using the same pulse generation principle.

Third and the final solution is using a filter at the end of the pulse generator. However, pulse combination technique is still being used to generate 5th order Gaussian pulse. Thus, PSD shape between 3.1 GHz and 5.1 GHz is still very sensitive to parameter changes. For instance, the center frequency changes from 6 GHz to 12 GHz in two different corner simulations. However, a relatively stable center frequency, which is 4 GHz for the designed transceiver, is required to achieve a successful communication. As it is understood from former simulations 5th order derivative of the Gaussian pulse is not suitable for our communication scheme.



(a) (b)

Figure 7.26. PSD shapes of (a) 2nd and (b) 5th order Gaussian pulse for distinct corners

Then, a pulse which has a wider PSD shape on frequency spectrum is decided to be used. Since, the simulations show that a PSD shape which has a narrower bandwidth varies more than the one with a wider bandwidth according to the corners, in terms of center

frequency, 3 dB and 10 dB bandwidth. It means a lot of information may be filtered out after the transceiver chip is manufactured if 5th derivative of the Gaussian pulse is used with a filter. Lower order derivatives of a Gaussian pulse have much wider bandwidth on frequency spectrum. Therefore, the variations seen on PSD of them at different corners are much less than the ones seen on PSD of the 5th order Gaussian pulse. In accordance, it is decided to generate a 2nd order derivative of the Gaussian pulse with the pulse generator designed. Hence, a more stable PSD shapes can be obtained at the output of the filter as it can be seen in Figure 7.26.

2nd order derivative Gaussian pulse generation is realized with the technique used for the formerly designed pulse generators. In this circuit, two pulses are used to generate the required pulse. An accurate timing is also necessary for the 2nd order Gaussian pulse generator topology. Timing in this circuit is also necessary however, it is not hard as much as the one required by the 5th order derivative Gaussian pulse generator.

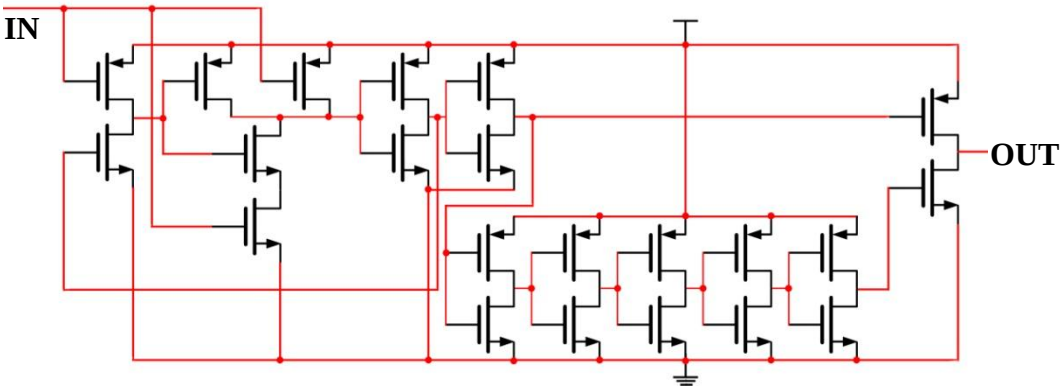


Figure 7.27. 2nd order derivative Gaussian pulse generator

The filter used at the end of the pulse generator is a 5th order series Chebyshev BPF which is decided to be realized as off-chip for the first transceiver chip and given in Figure 6.3. It is not designed as on-chip since, it has 5 inductor and 5 capacitors that can cover too much space on the chip.

Pulse shapes generated at the input and output of the filter is given in Figure 7.28. Pure 2nd order Gaussian pulse shapes cannot be seen at the input port of the filter (Figure

7.28 (a)) since, reflected signal from the filter generates fluctuations at the end of the desired pulse. In spite of these variations at the input, pulse shape at the output of filter is more Gaussian like and it meets the power spectral requirements.

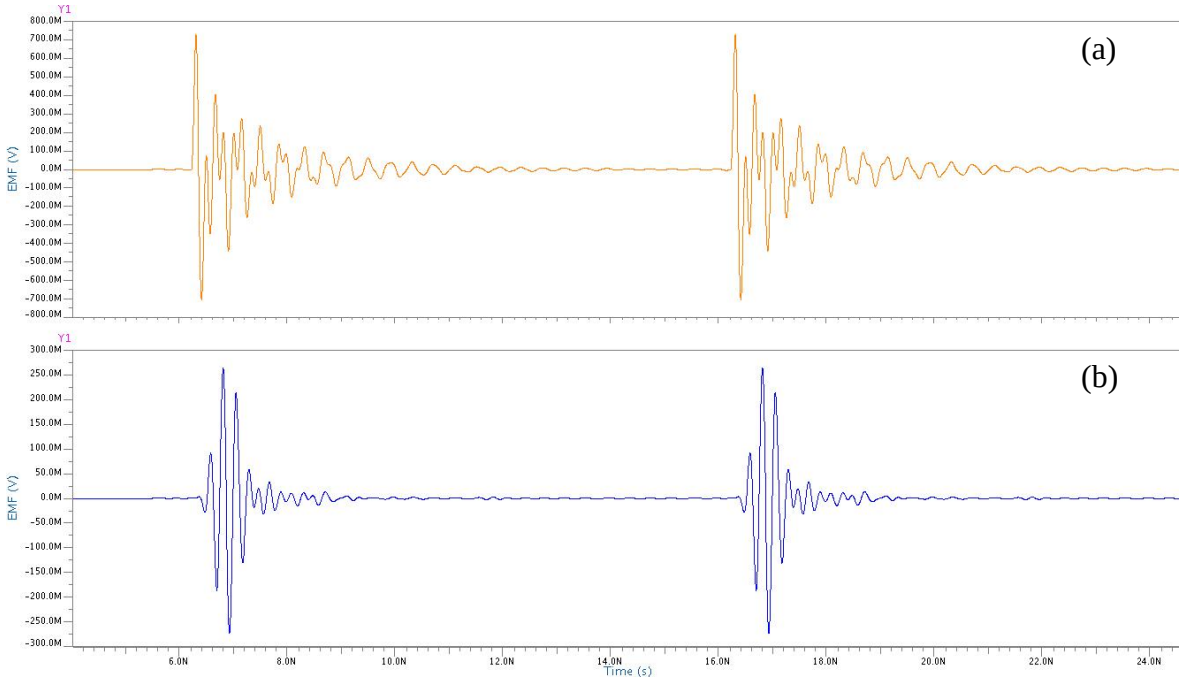


Figure 7.28. Signal at the input and output of the off-chip filter

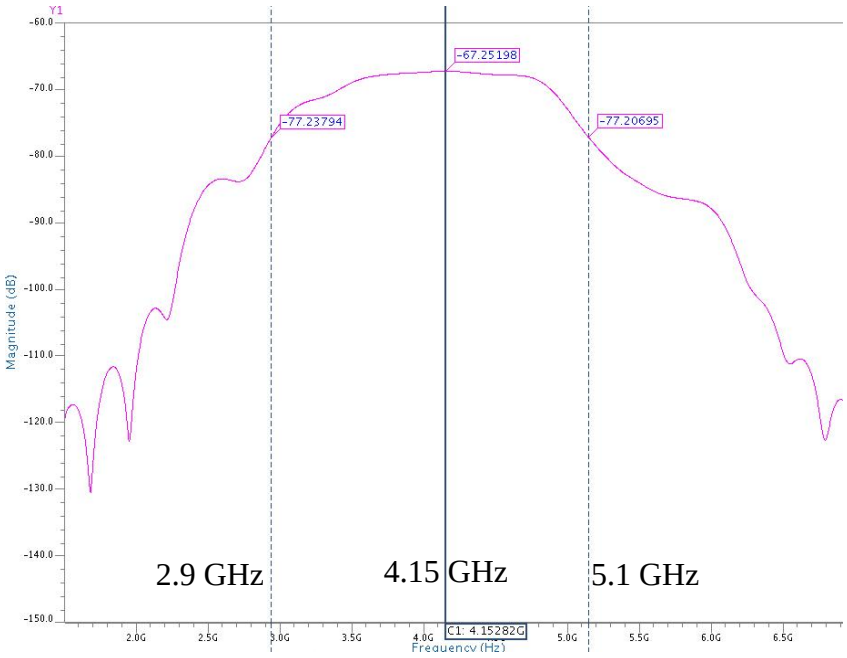


Figure 7.29. PSD shape of the signal at the filter output

Proposed solution confronts the corner case variations on PSD shape as expected. PSD shape of the generated pulse for different corners can be seen in Figure 7.30. Consequently, center frequencies and bandwidths become almost constant with this structure (Figure 7.30).

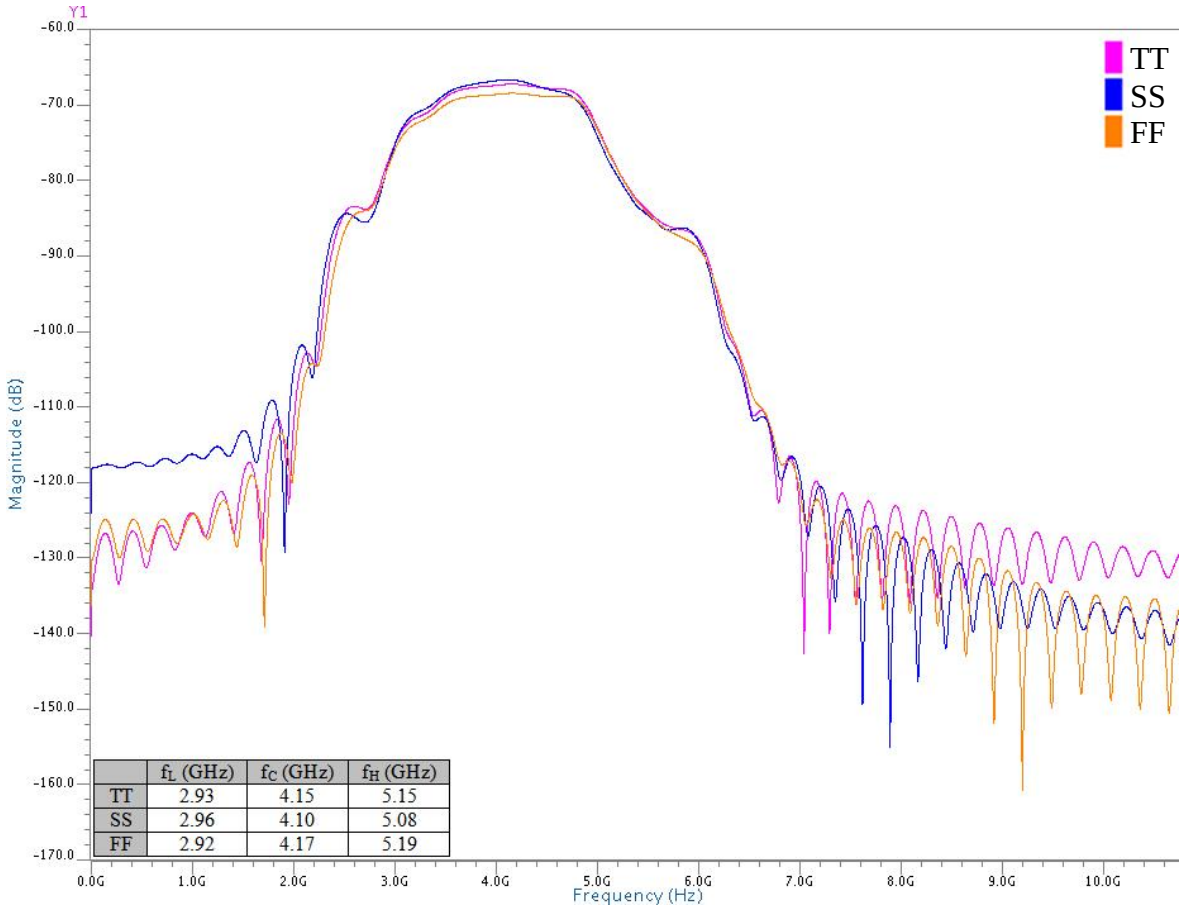


Figure 7.30. PSD shapes of TT, SS and FF corners

Table 7.7. AC power consumption of the pulse generator (simulation result)

	Average Power (W)	
	V_{DD} = 1.2 V	**V_{DD} = 1.8 V**
10 MHz	0.44 m	4.1 m
100 MHz	2.2 m	7.8 m
500 MHz	3.9 m	10.7 m
1000 MHz	20.6 m	49.9 m
V_{pp} (V)	310 m	550 m

Table 7.8. DC power consumption of the pulse generator (simulation result)

	TT	**SS**	**FF**	**SF**	**FS**
DC Power (W)	172.58 µ	11.31 µ	1116 µ	49.37 µ	500.43 µ

Consumed AC and DC power of the last pulse generator is given in Table 7.7 and Table 7.8, respectively. These results are obtained from schematic simulations and as it is stated before standby power consumption of this pulse generator is lower than many of the pulse generator in the literature.

8. IR-UWB TRANSCEIVER LAYOUT

As stated before UMC 130 nm CMOS technology is used for realization since it offers a wide range of devices from high speed to low leakage and employs up to 8 layers of copper interconnects. In addition, RFCMOS/Mixed mode technologies are available. This technology also brings an option which is called *Fusion*. It is a design option that allows both high speed and low leakage transistors to be combined on a single chip.

RFCMOS transistors are preferred because of the operation frequency range of the designed transceiver, high cut-off frequency of RFCMOS transistors and some other high frequency properties. In addition, UMC's 130 nm technology is a low voltage one, which uses 1.2 V, among many other process technologies.

During layout design some criterions and design techniques are taken into account for preventing the performance degradation. Common centroid alignment can be counted as one of the most important techniques among others. This technique is used in order to reduce parasitic mismatch in analog circuits as, parasitic mismatch induced by the layout has adverse effects on the circuit performance significantly. Devices are split into smaller ones and placed around a common center point. For instance, inverters used in the pulse generator have large W values. Therefore, transistors are split into smaller parallel ones and aligned according to a common point. Same types of transistors are arranged among each other.

Second important criterion is symmetric arrangement of transistors especially for the receiver layout since, most of the circuits are differential. To get exactly similar differential pulses, layouts of these circuits must be designed in a symmetric way. If very similar pulses expected at the output port of a differential circuit, very similar parasitic inductance, capacitance and resistance values should be seen on positive and negative signal paths.

Also, the following topics are trying to be implemented to the layout:

- All circuit elements arranged as compact as possible to save real estate.
- Wirings are kept as short as possible in and between the circuits.
- VDD and the ground line are laid on top of each other and they encircle the circuits as thick paths. Since, large fluctuations are observed on VDD signal during simulations. To decrease these oscillations by creating parasitic capacitance between VDD and the ground line this technique is applied during layout design. This is also applied for whole layout of the transceiver chip.
- Layout of each block is designed according to former and latter blocks as much as possible for making input and output ports more closer.

9. CONCLUSION

In this thesis, a literature survey on UWB transceivers and pulse generators is done. Consequently, an energy detection type IR-UWB transceiver is chosen. An ideal model of the selected UWB transceiver system is constructed by using a mixed signal hardware description language, VHDL-AMS, and this model is simulated to obtain specs of the system.

Two different pulse generator topologies are selected and realized in UMC's 130 nm CMOS technology for testing purposes. Then, a new glitch based pulse generator with off-chip bandpass filter is designed which is superior to previous pulse generators in terms of power and area. This pulse generator achieves 10 MHz pulse repetition rate with 440 μW power consumption only in 0.094 mm^2 chip area. It is capable of providing data rates up to 1 Gbps with 20.6 mW power consumption. In addition, this pulse generator generates the required pulse shape at the rising edge of the incoming data. Thus, it can be easily adapted to most transceiver systems that use common modulation techniques.

After the completion of the transistor level designs, layouts of the blocks that form the UWB transceiver are drawn separately in Mentor Graphics by using the Design Architect tool. All blocks are simulated to see if the circuits are still working after the layout design process. Then, all these blocks are merged to form the UWB transceiver chip and submitted for manufacturing with UMC's 130 nm CMOS technology.

All in all, the design goals for the IR-UWB system were met. The transmitter is the main subject of this dissertation which is designed according to the FCC regulations. Thanks to the operation principle of the pulse generator that generates UWB pulses regardless of input modulation scheme, the designed transmitter can be used in many transceiver systems.

APPENDIX A

During layout design process blocks are drawn separately and they are put together at the end of this phase to make the transceiver chip up. In the following pages, layouts of the individually designed blocks and the complete IR-UWB transceiver chip can be seen.

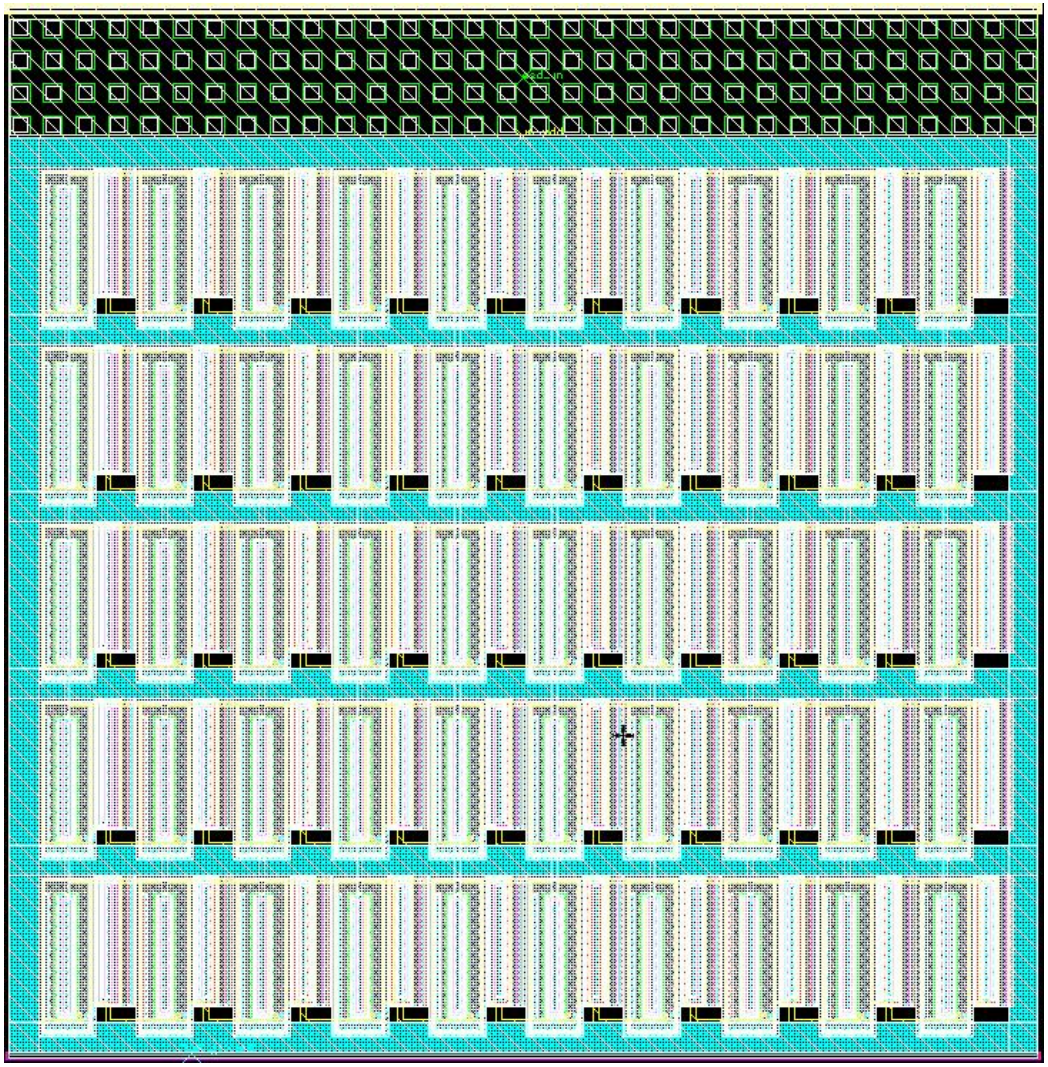


Figure A.1. ESD diodes for pulse generator input

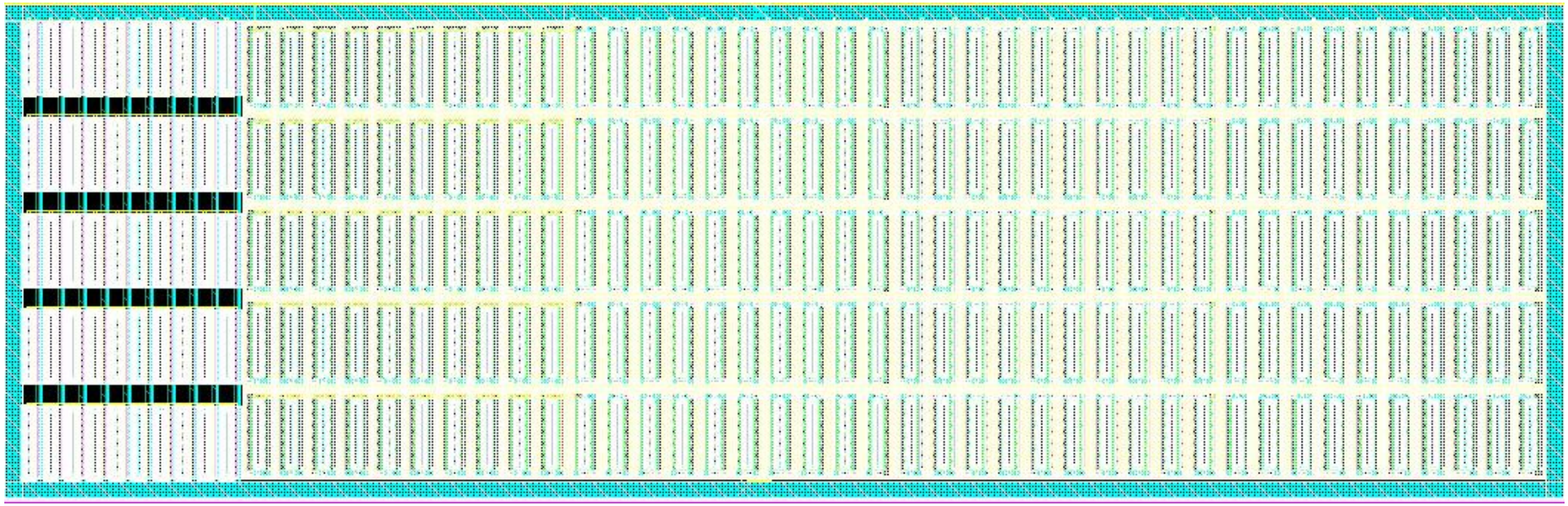


Figure A.2. Clamp for the transmitter

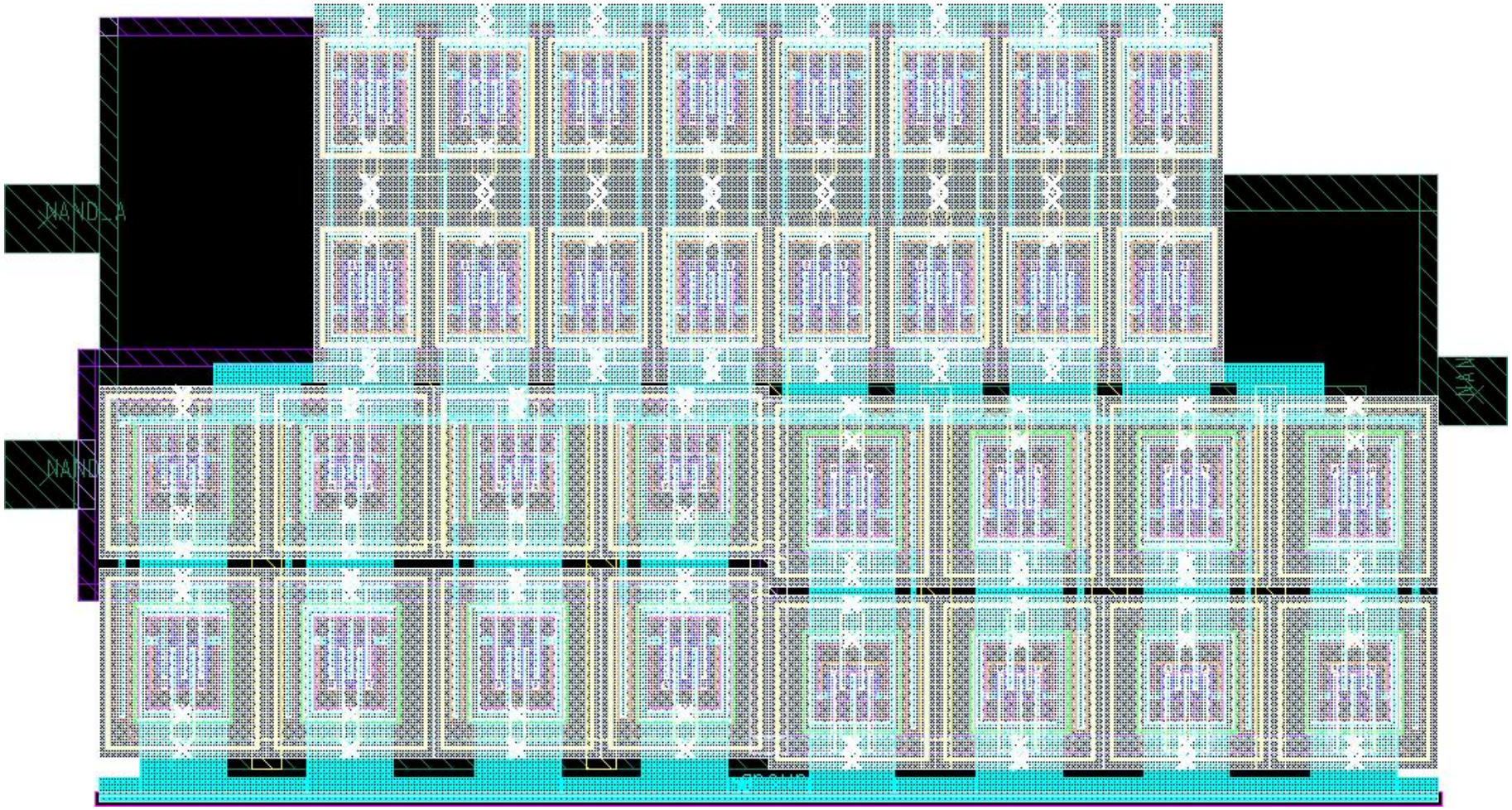


Figure A.3. NAND gate

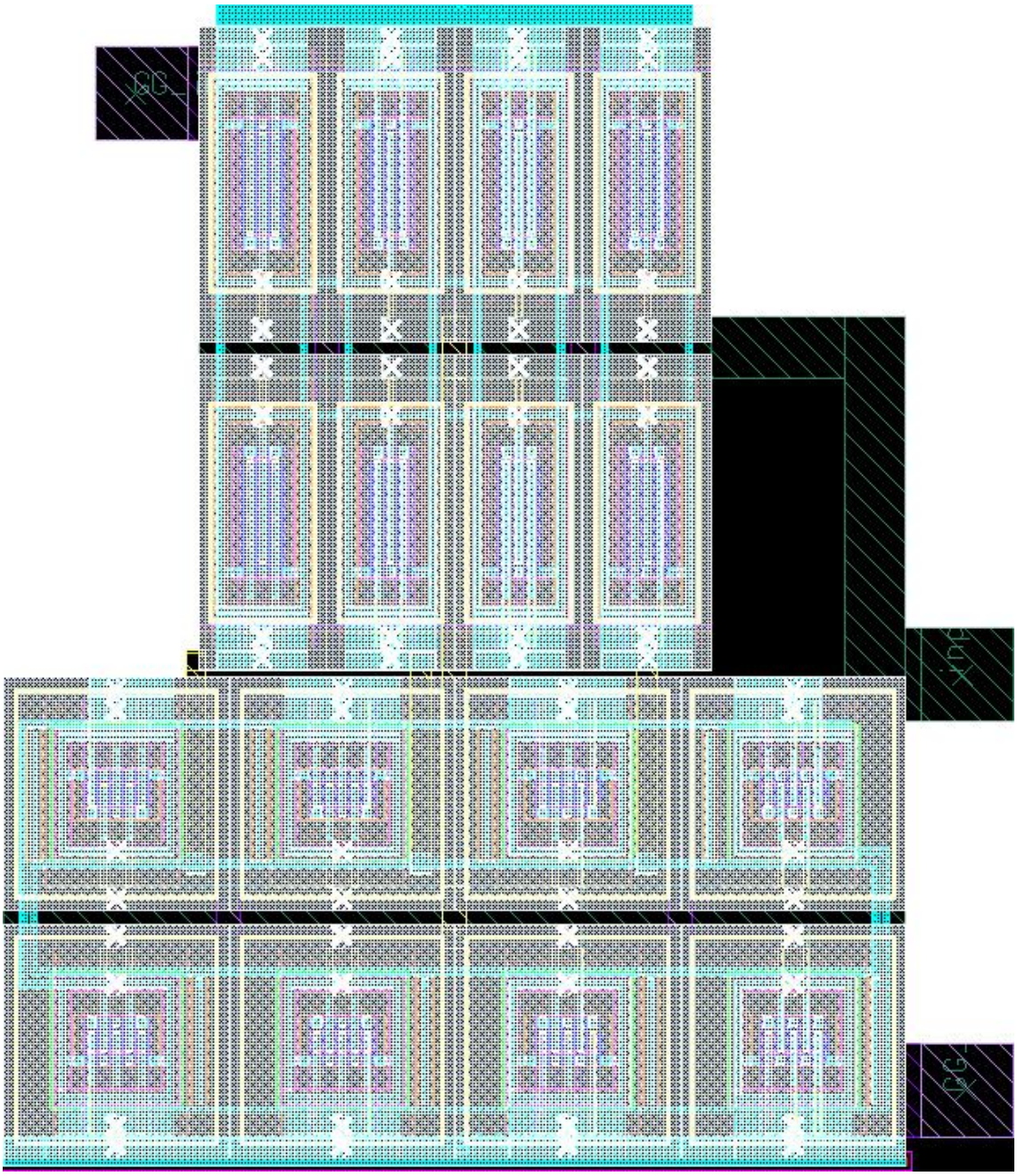


Figure A.4. Glitch generator input stage

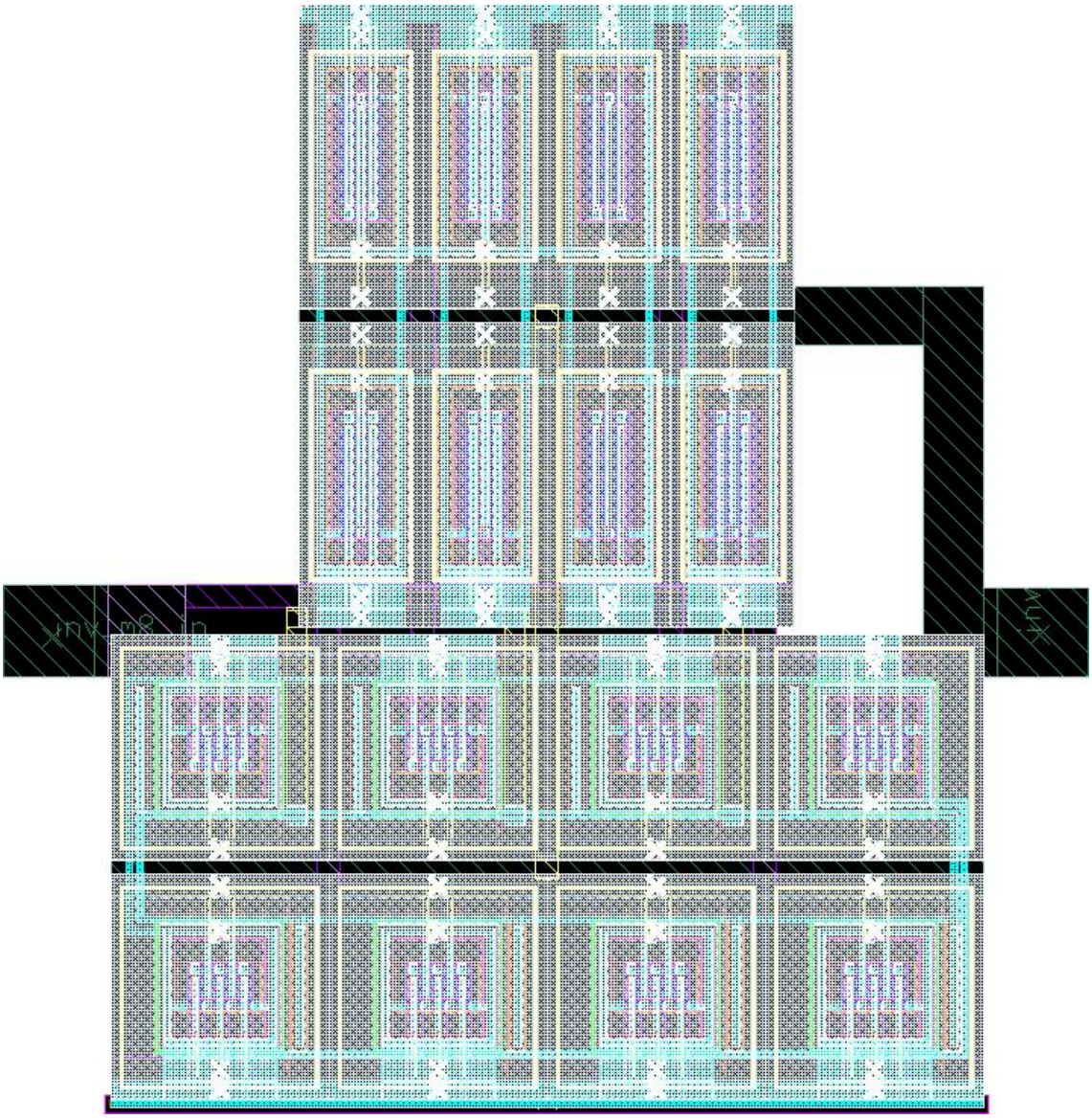


Figure A.5. Inverter with 8 PMOS and NMOS

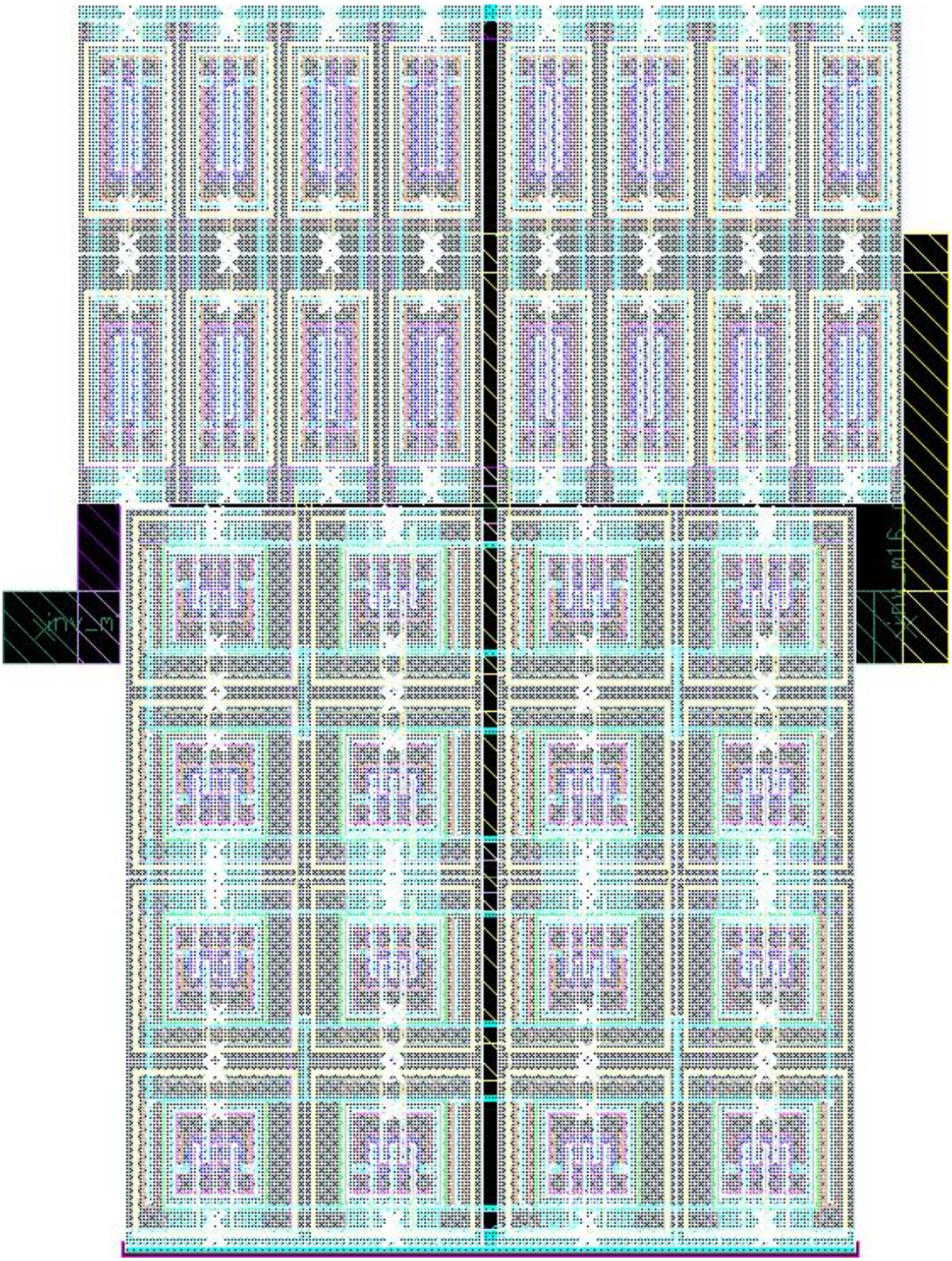


Figure A.6. Inverter with 16 PMOS and NMOS

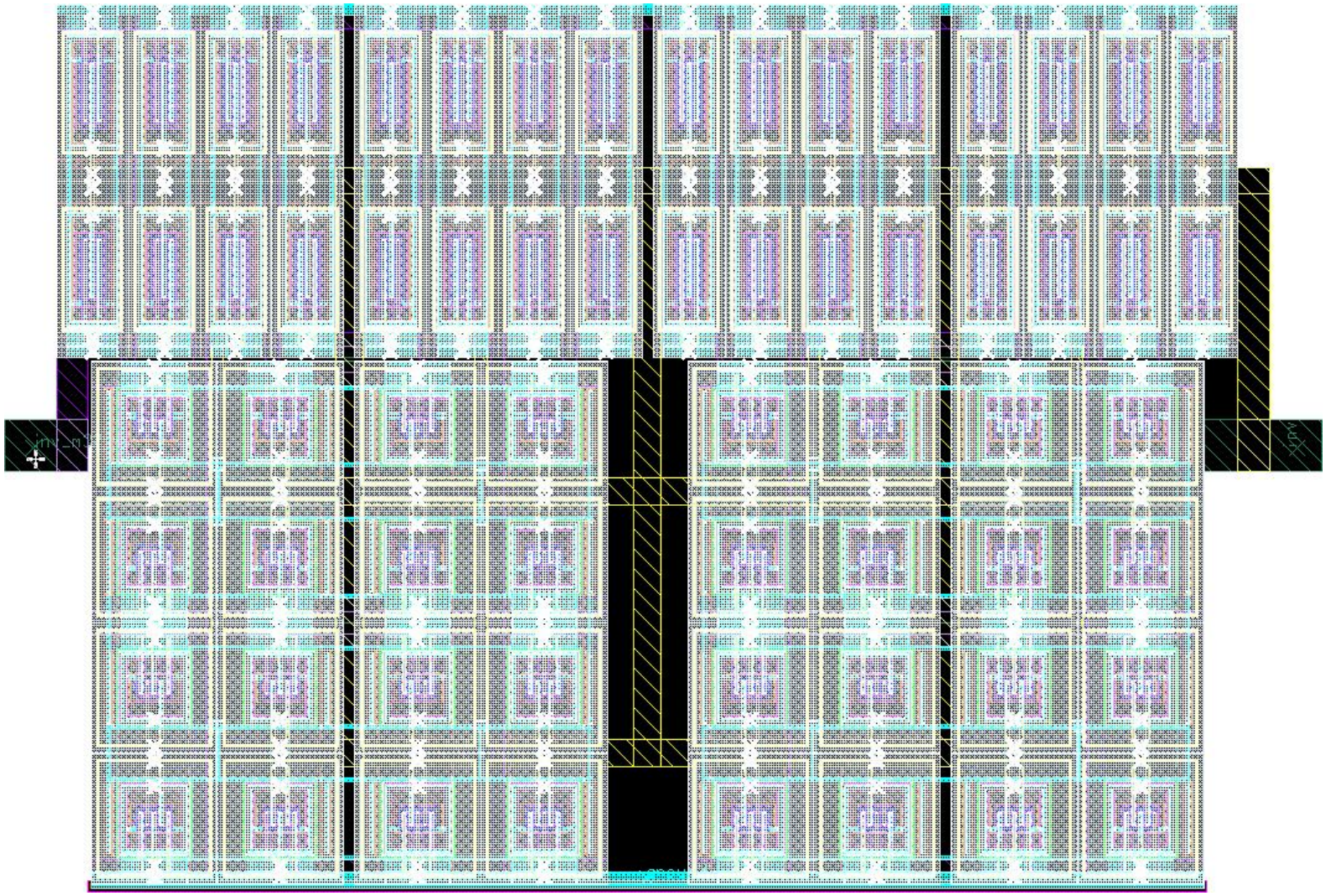


Figure A.7. Inverter with 32 PMOS and NMOS

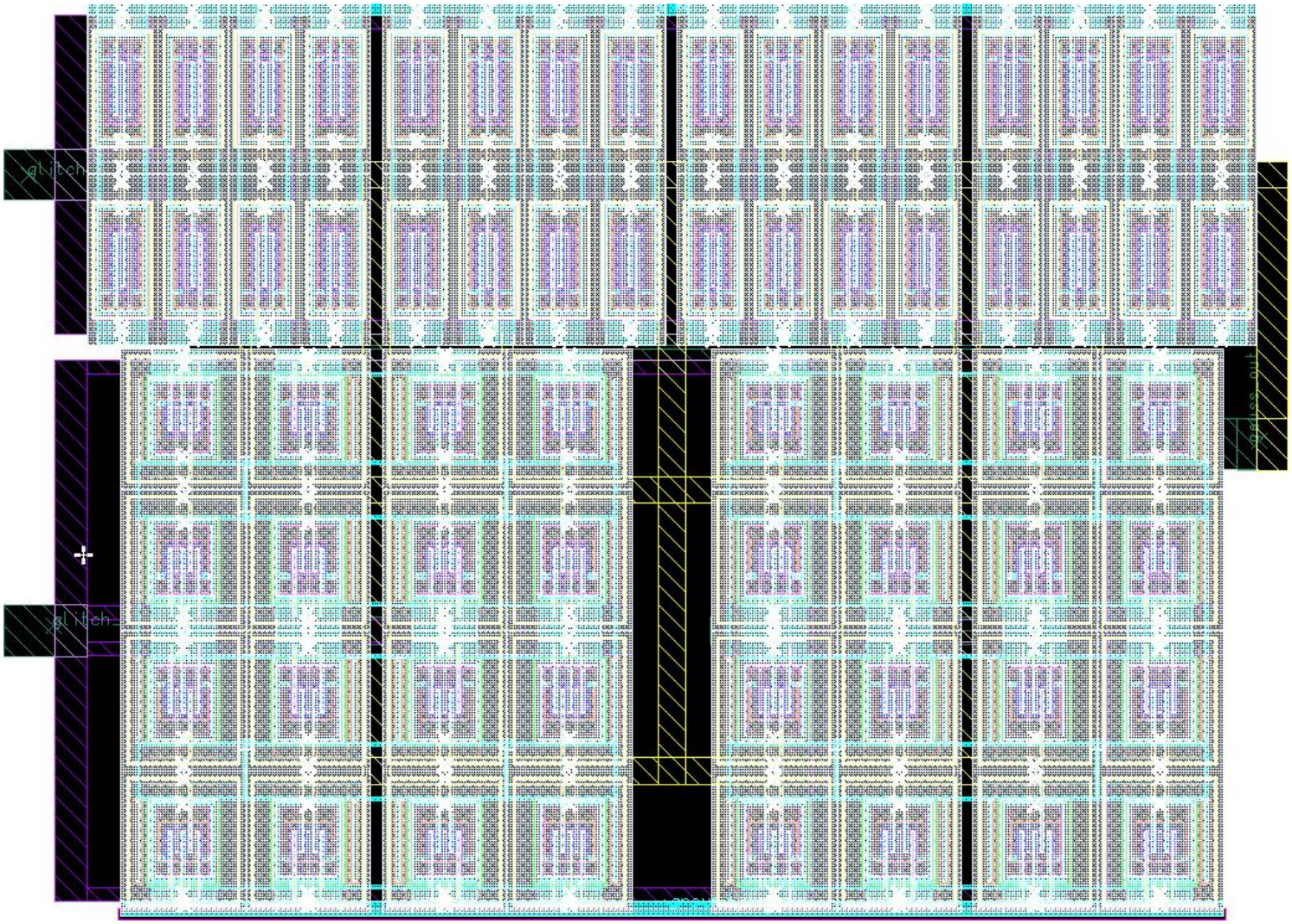


Figure A.8. Pulse generator output stage

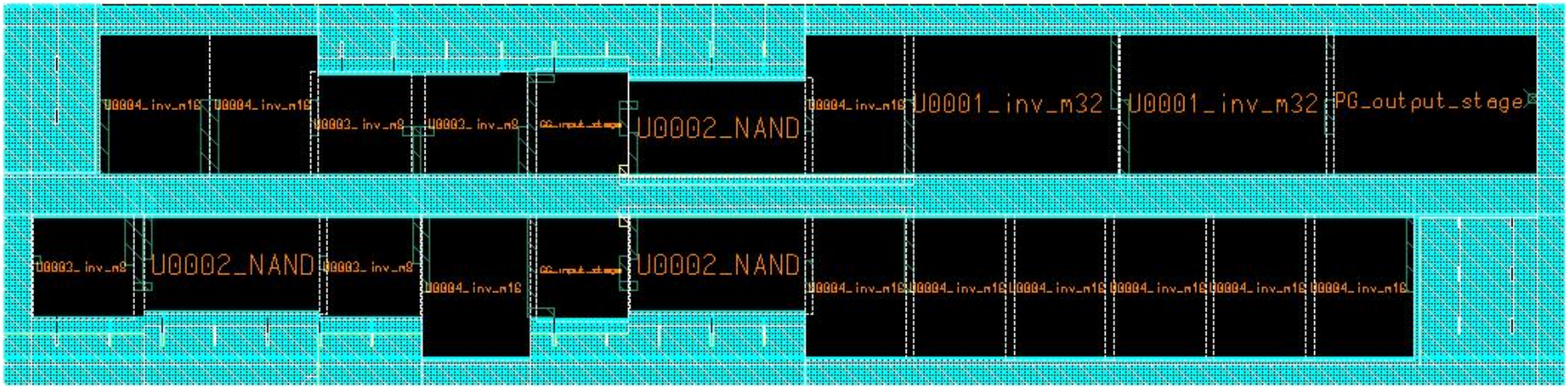


Figure A.9. Pulse generator

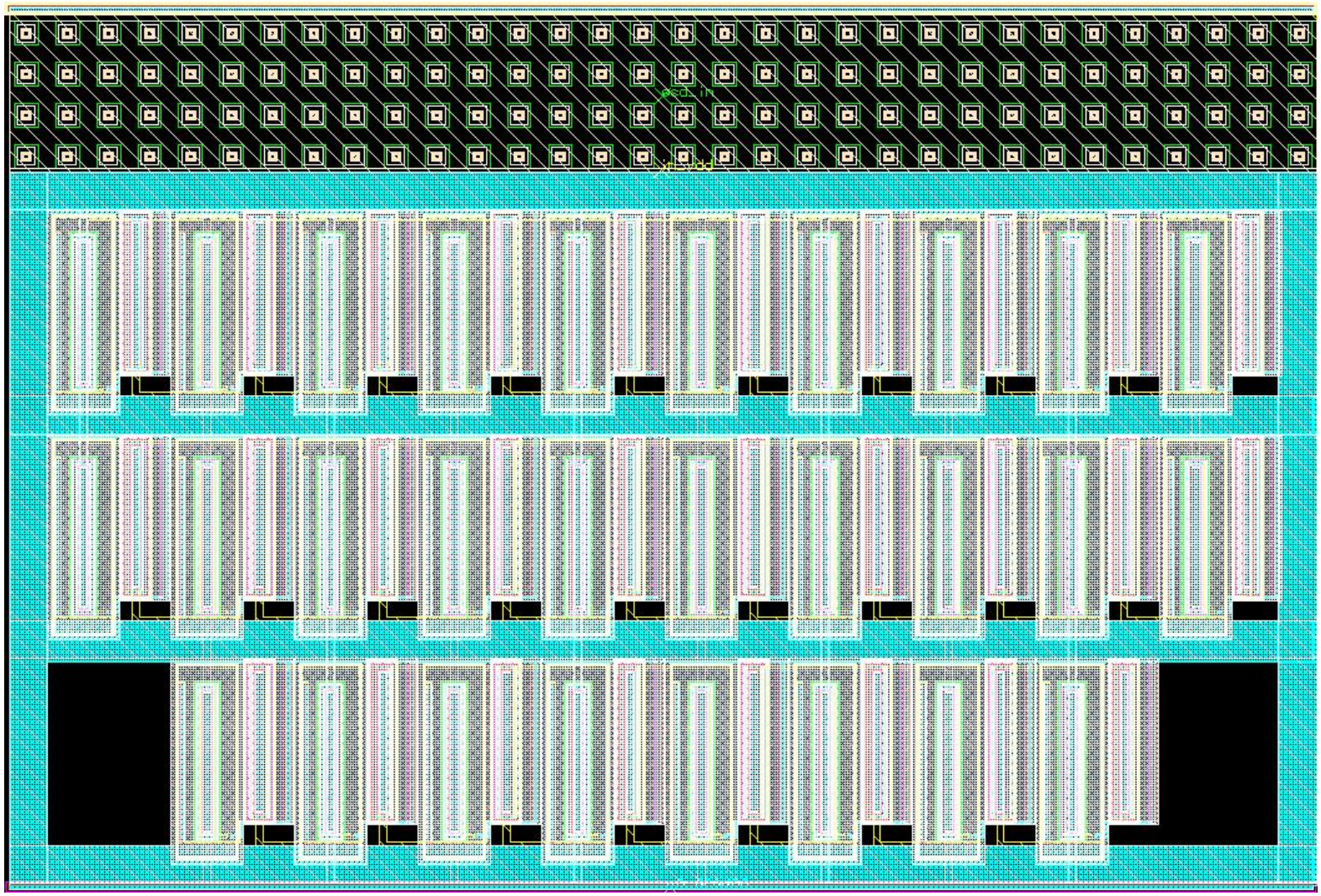


Figure A.10. ESD diodes for LNA

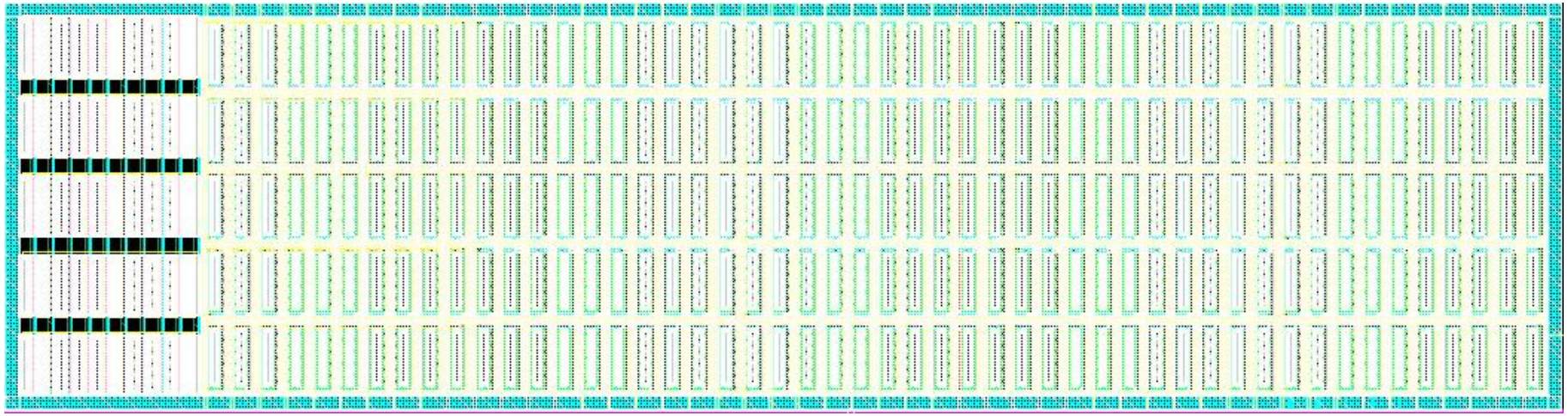


Figure A.11. Clamp for the receiver

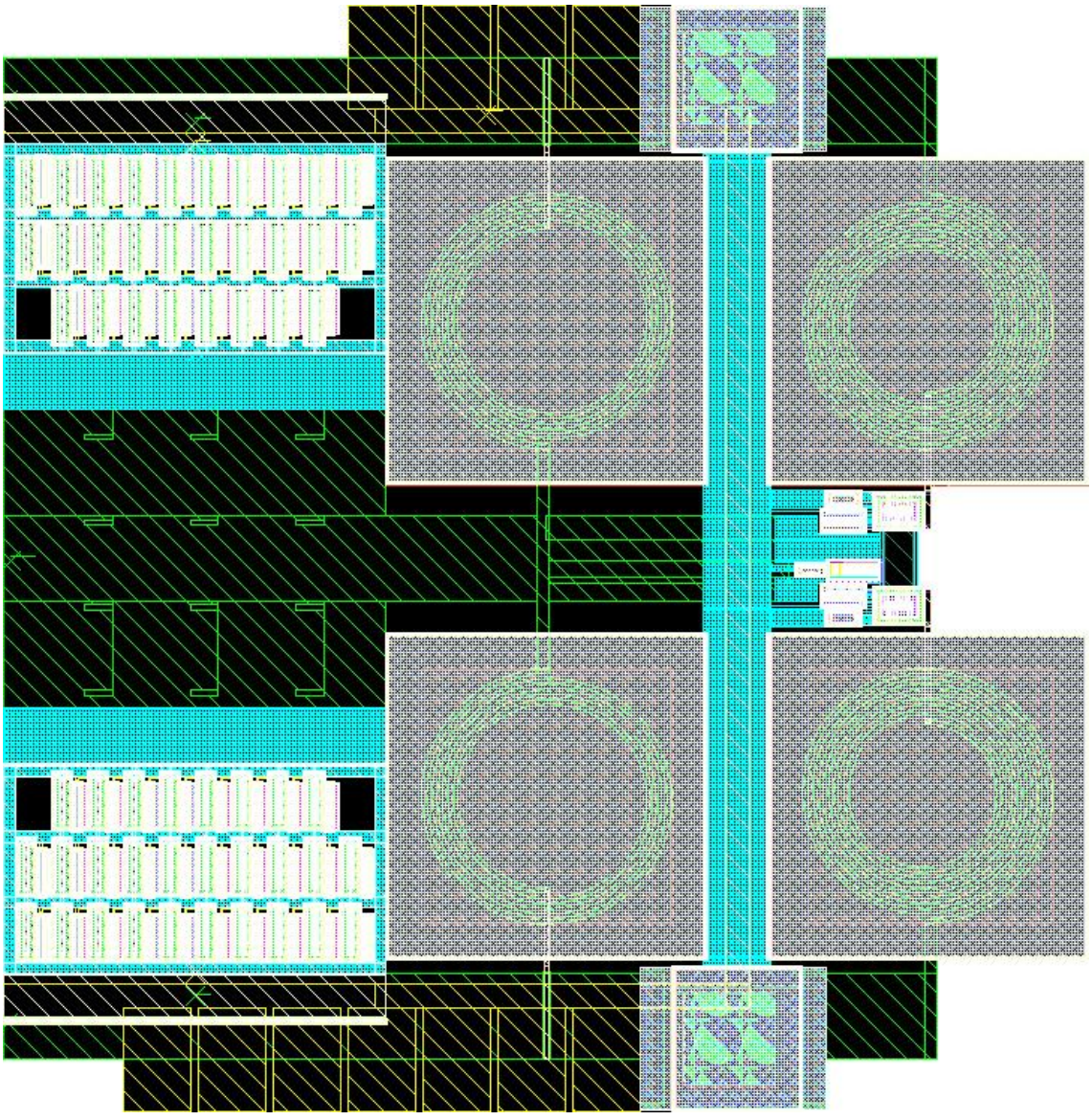


Figure A.12. LNA

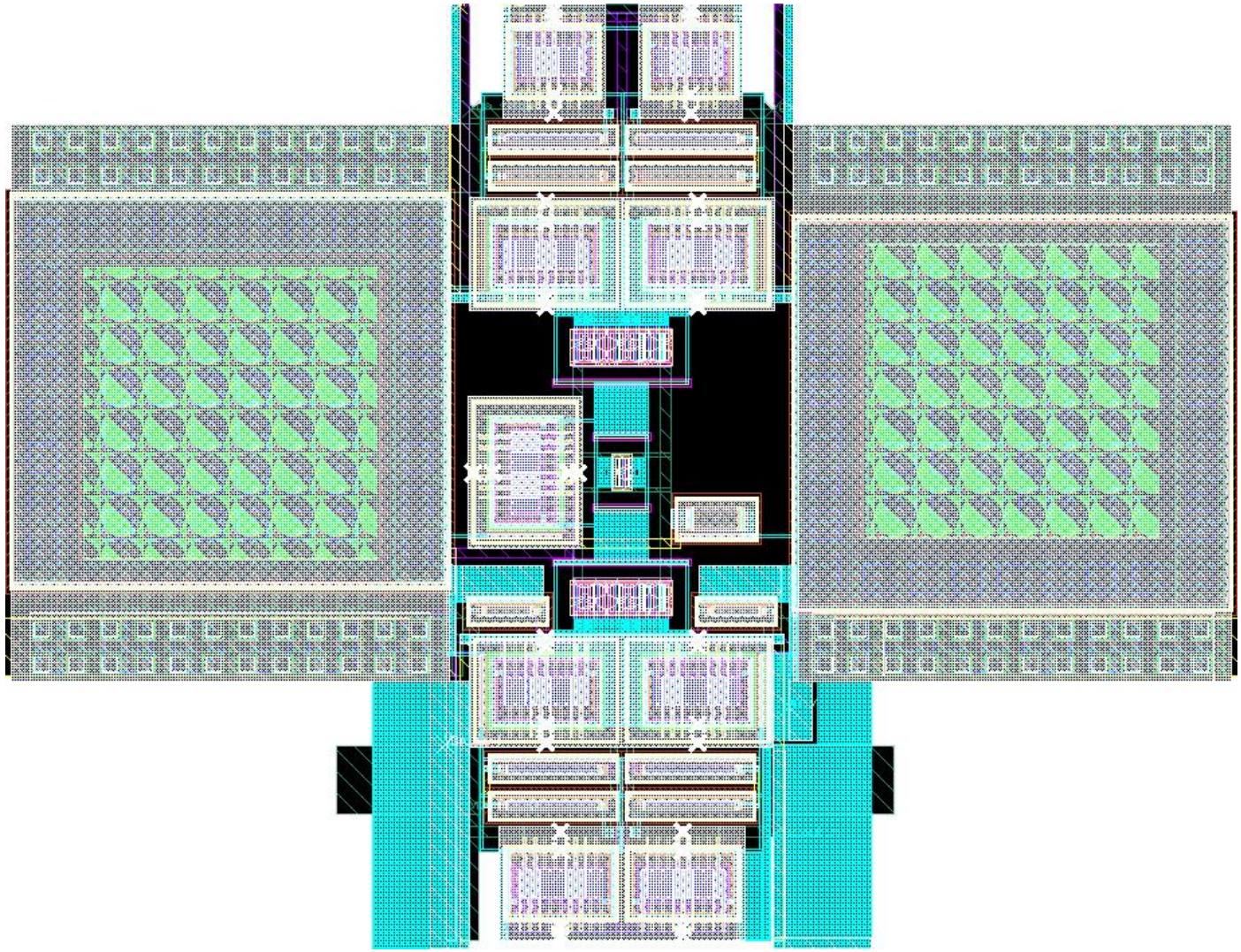


Figure A.13. VGA

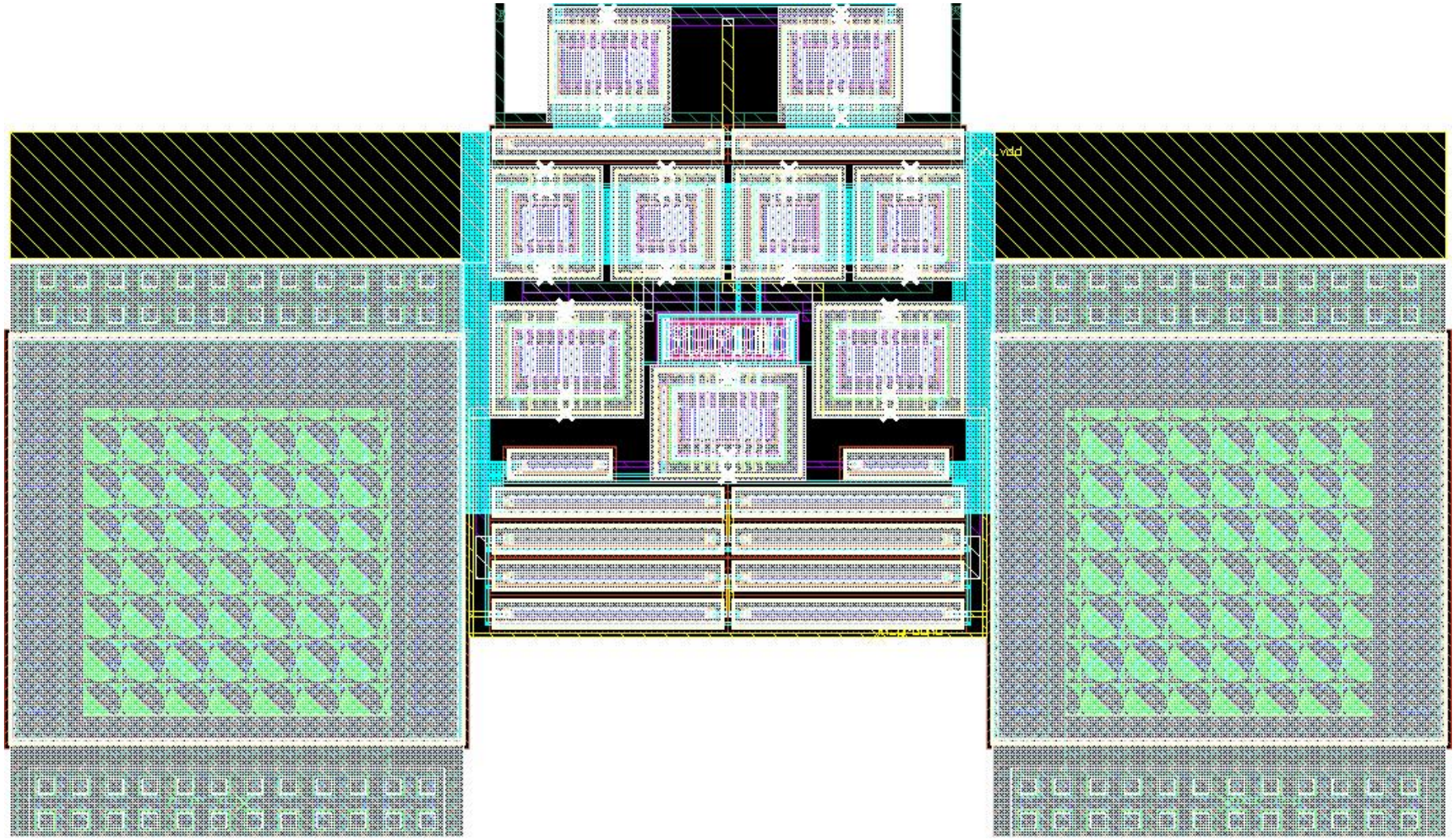


Figure A.14. Mixer

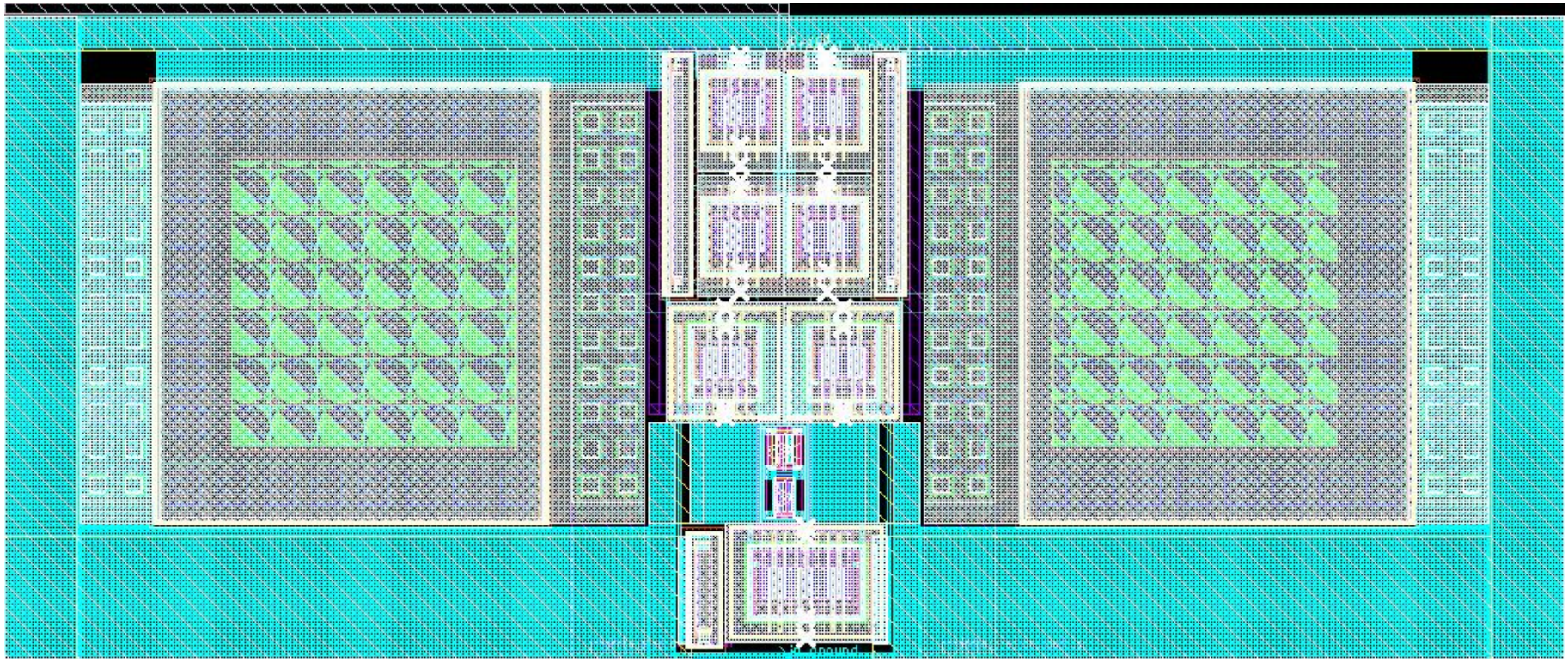


Figure A.15. Integrator

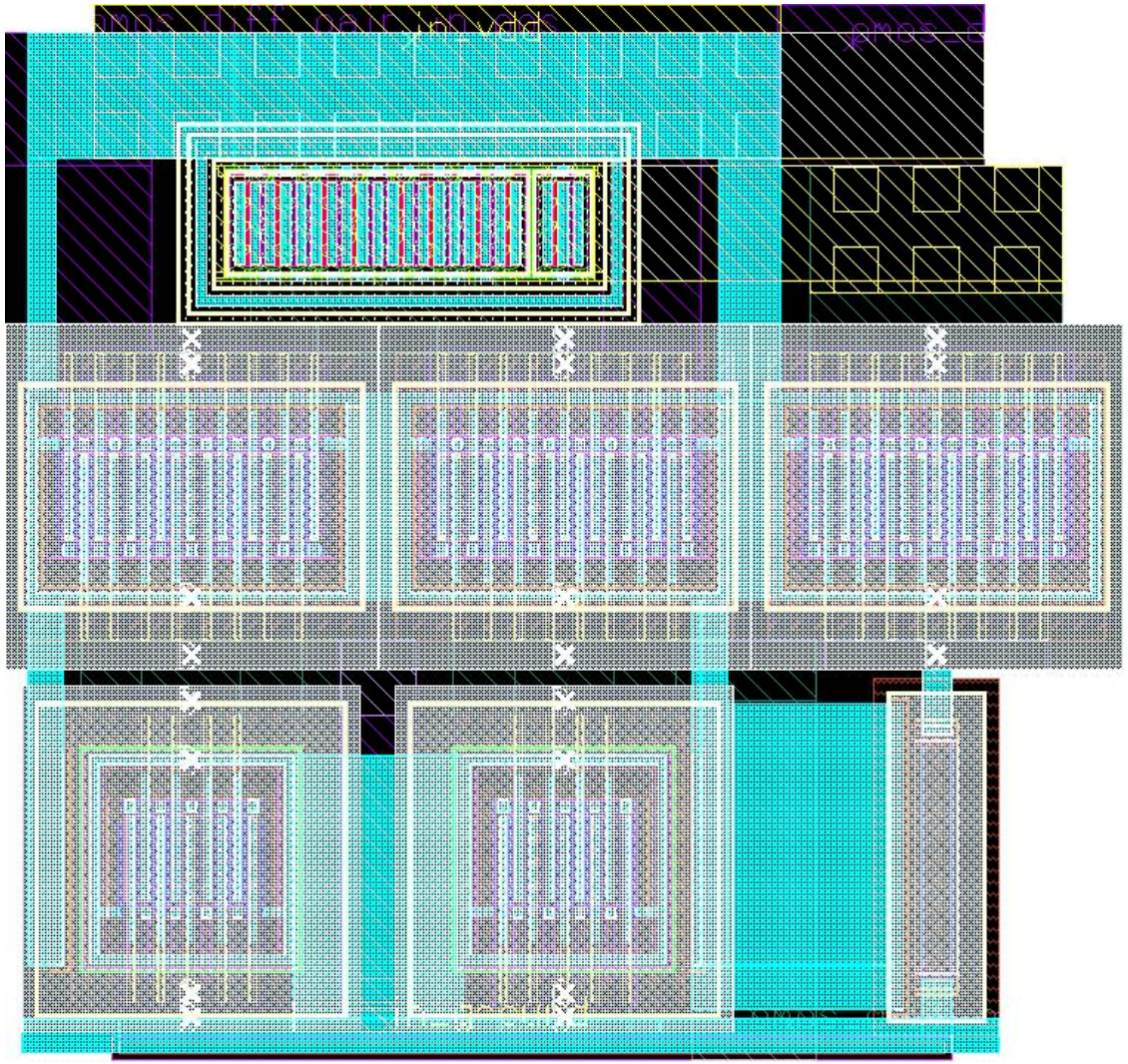


Figure A.16. PMOS differential pair

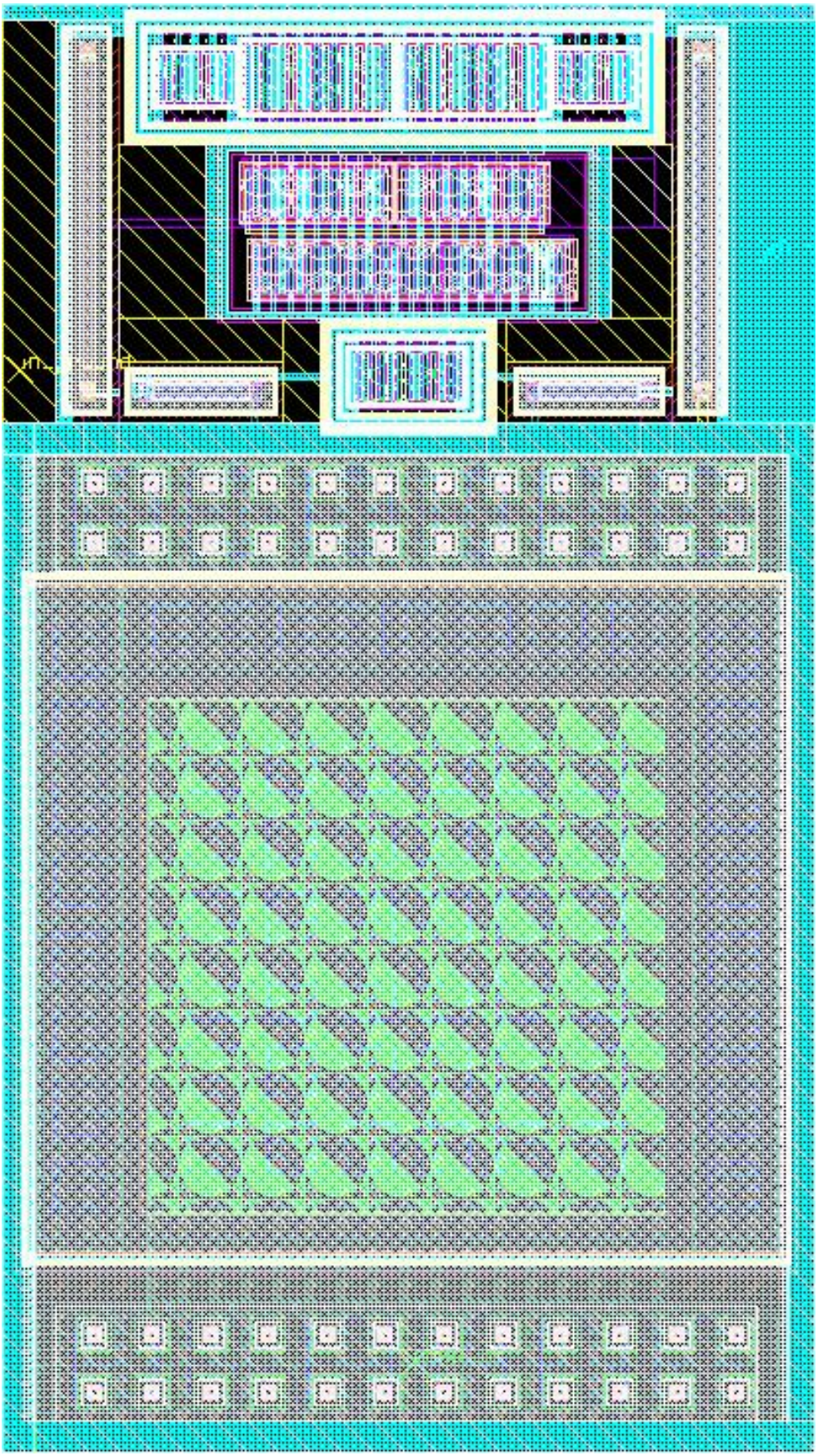


Figure A.17. Comparator

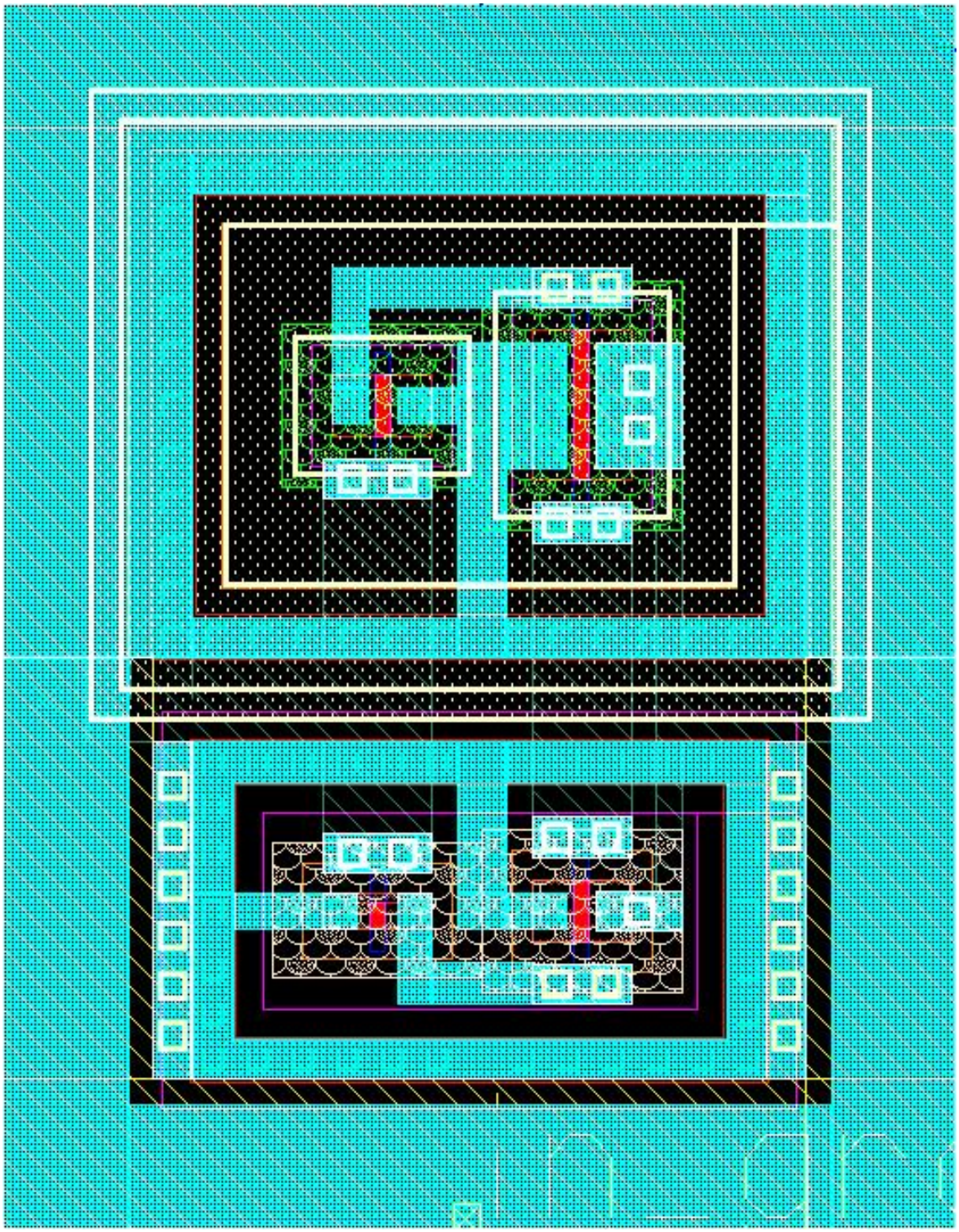


Figure A.18. Inverter stage for comparator-1

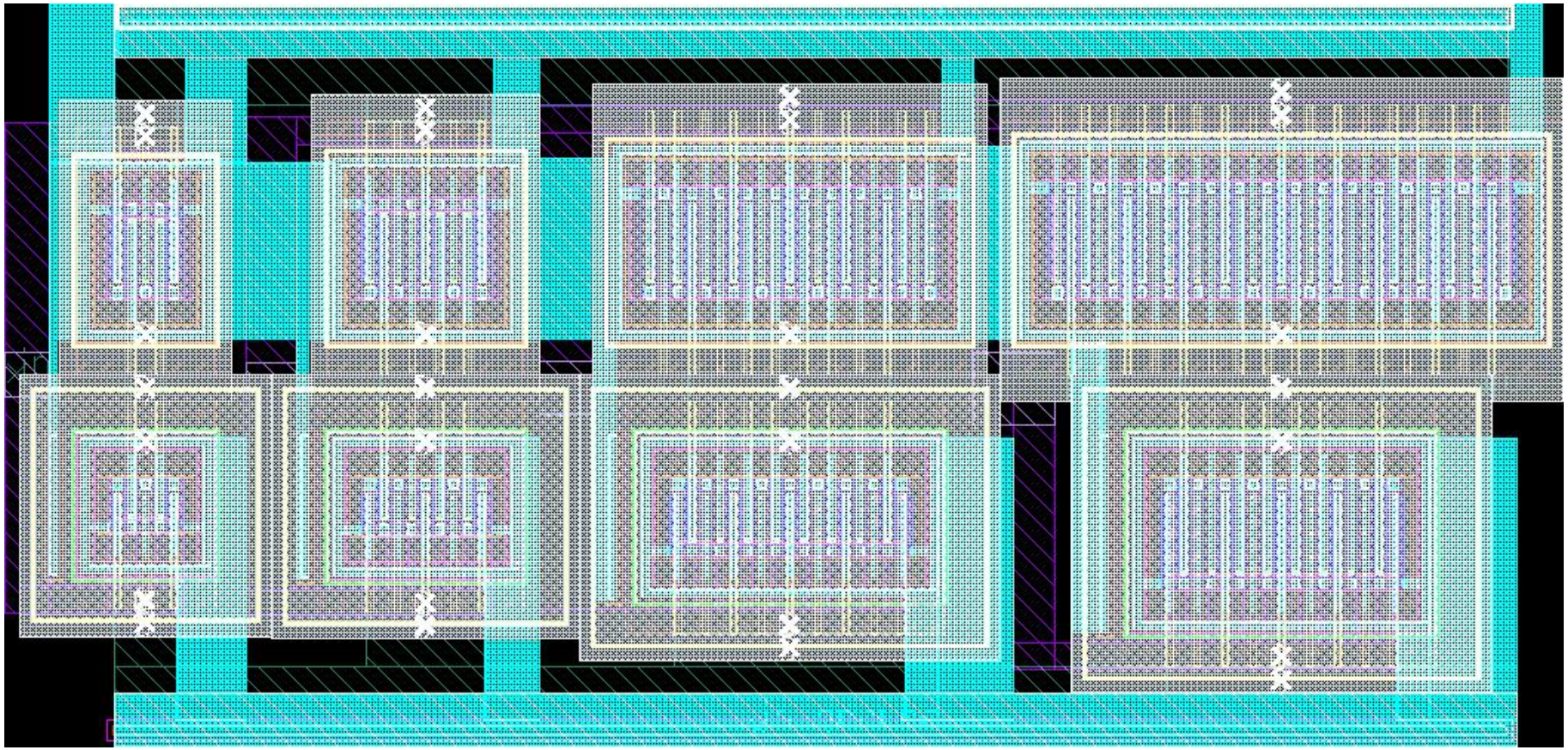


Figure A.19. Inverter stage for comparator-2

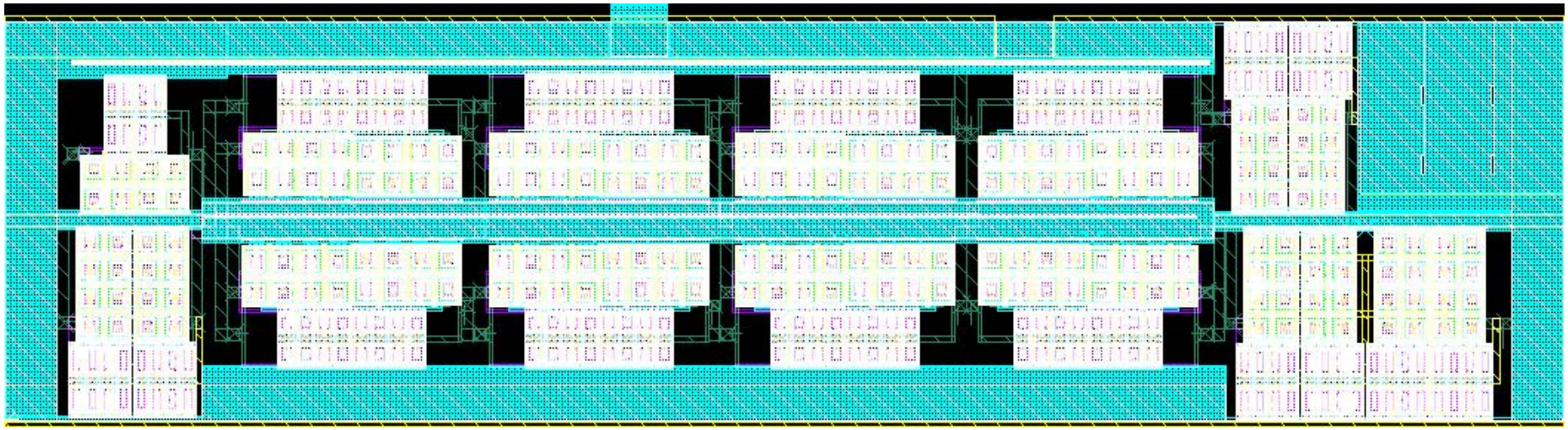


Figure A.20. D-type flip flop

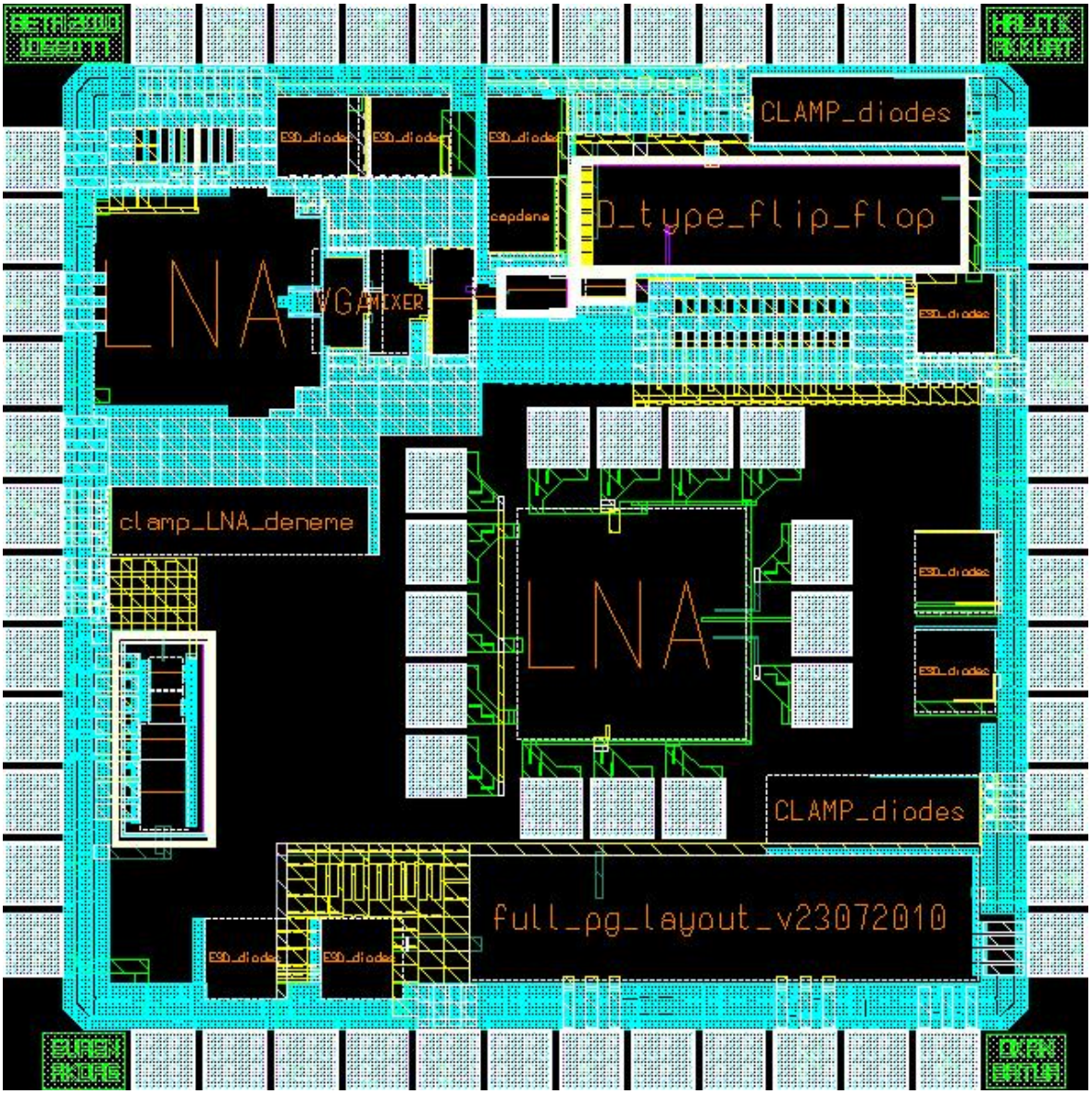


Figure A.21. IR-UWB transceiver chip (1525 µm x 1525 µm)

APPENDIX B

Simulation results of layouts are also given in the following pages to prove that the designed transceiver is successfully working.

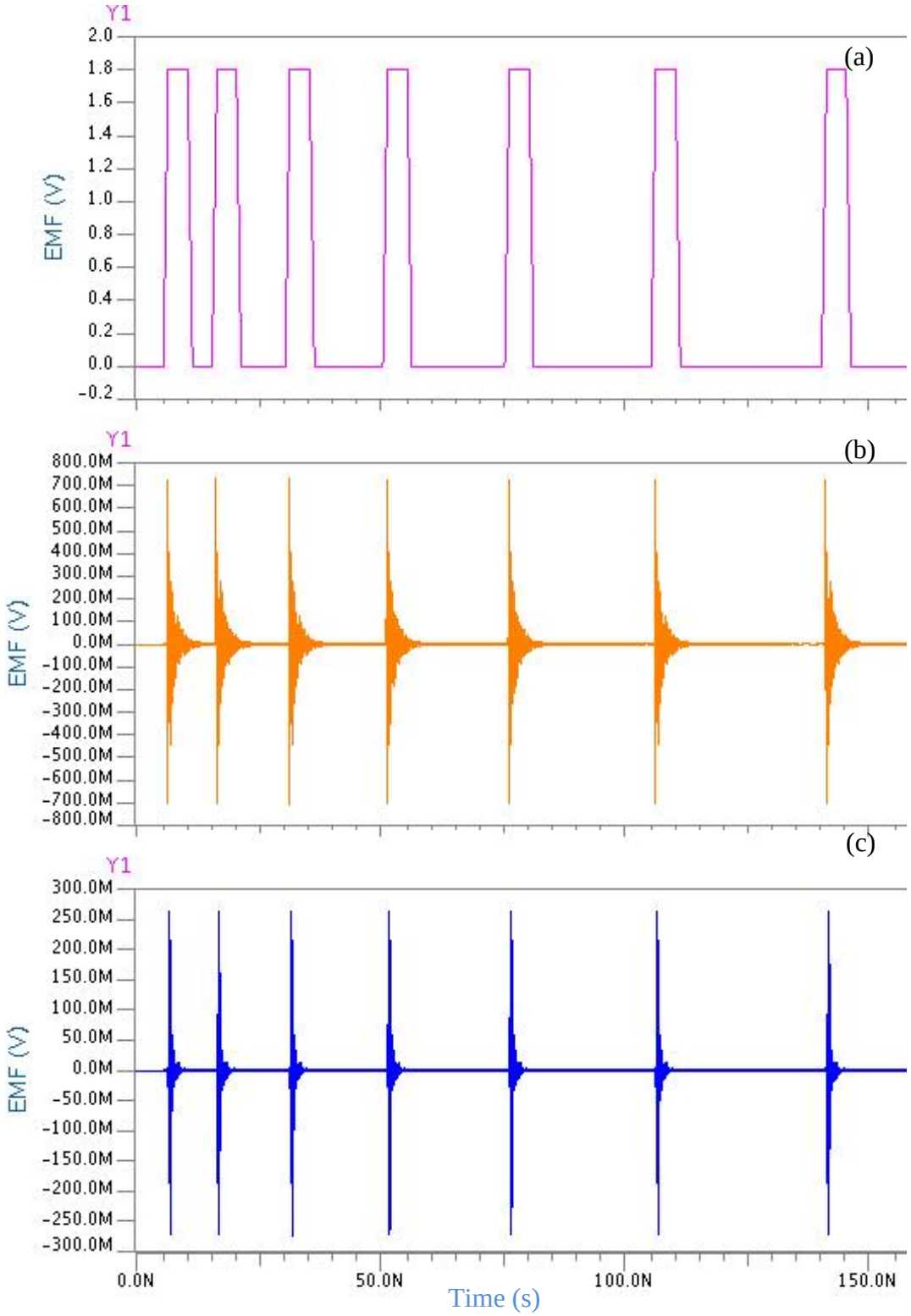


Figure B.1. (a) Data, signal (b) before and (c) after off-chip transmitter filter

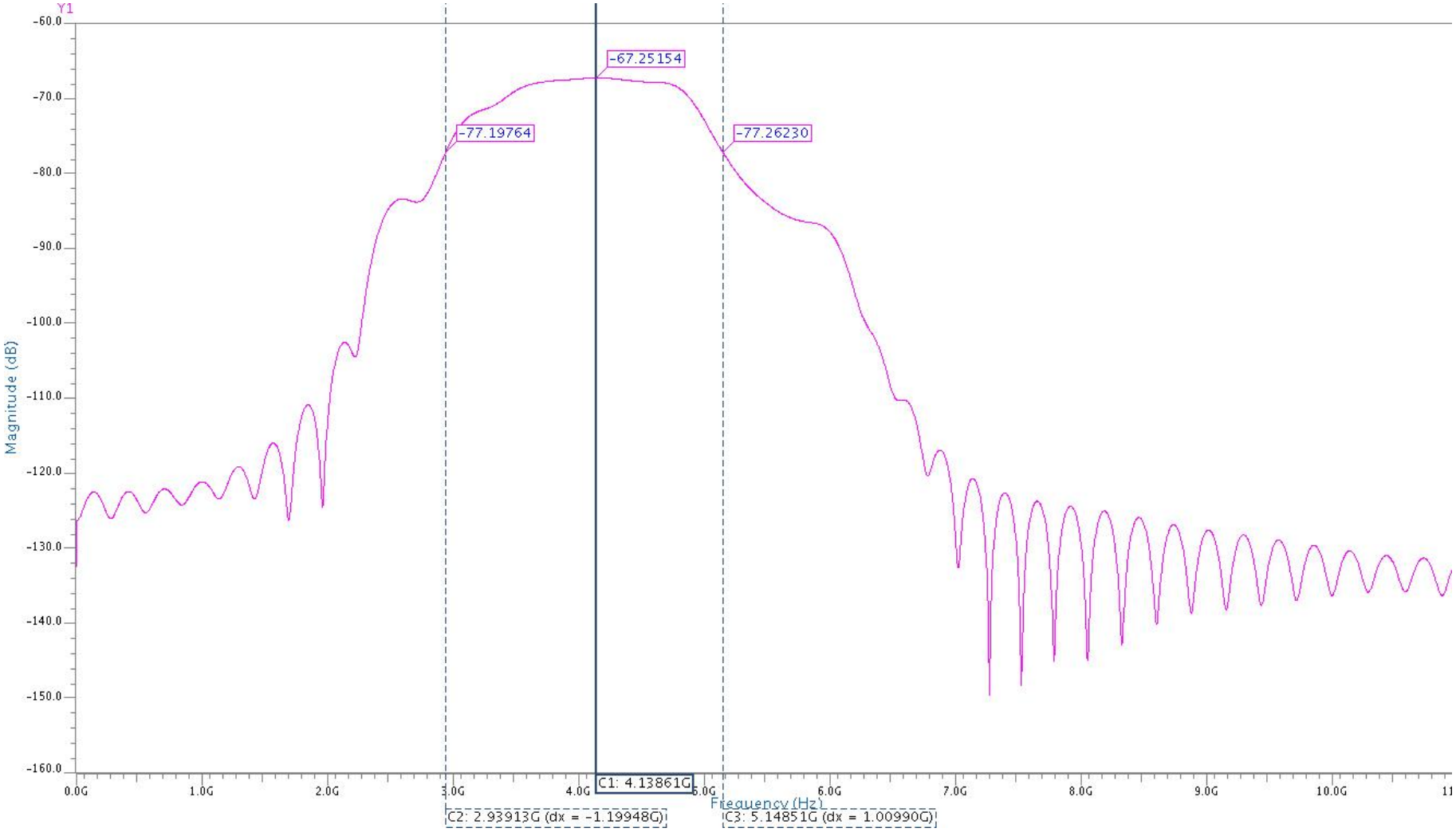


Figure B.2. PSD of output signal of the transmitter

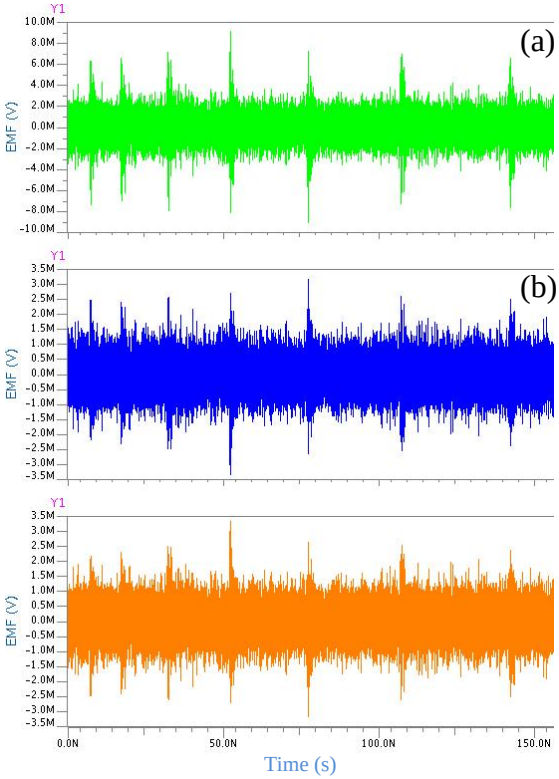


Figure B.3. (a) Input and (b) differential output of balun

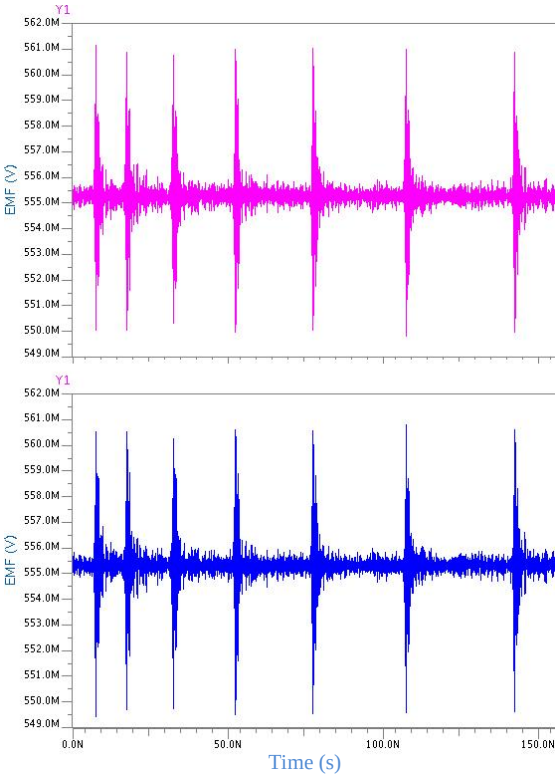


Figure B.4. Differential output of LNA

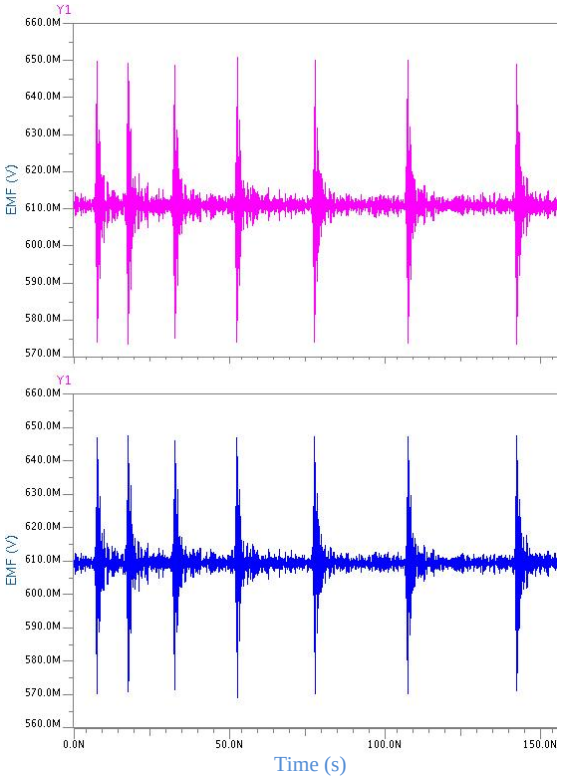


Figure B.5. Differential output of VGA

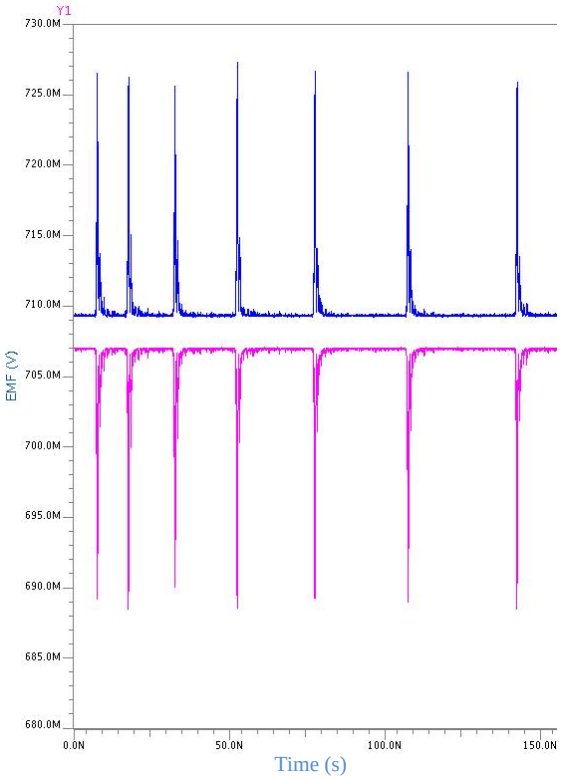


Figure B.6. Differential output of mixer

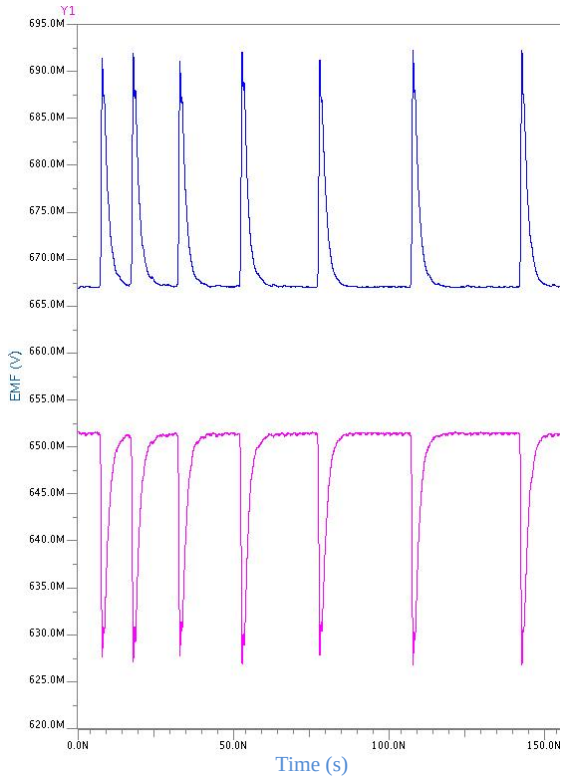


Figure B.7. Differential output of integrator

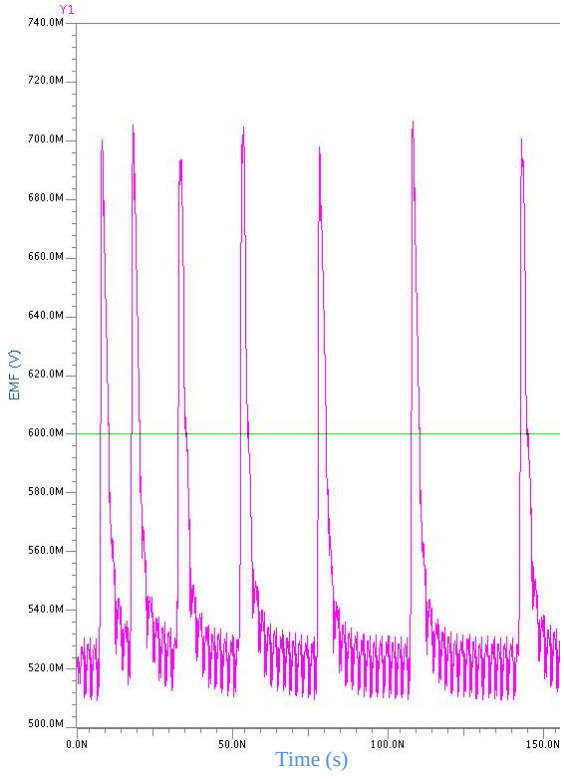


Figure B.8. Output of PMOS differential pair

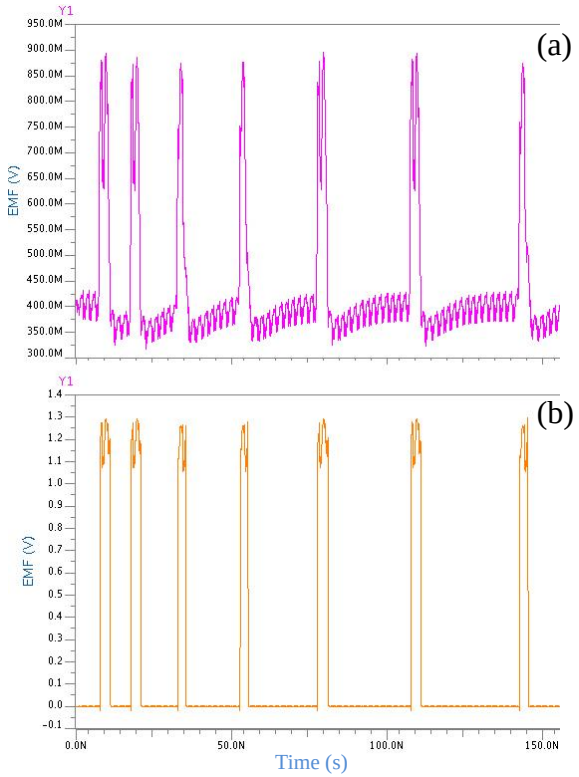


Figure B.9. Output of (a) comparator and (b) inverter at the output of comparator

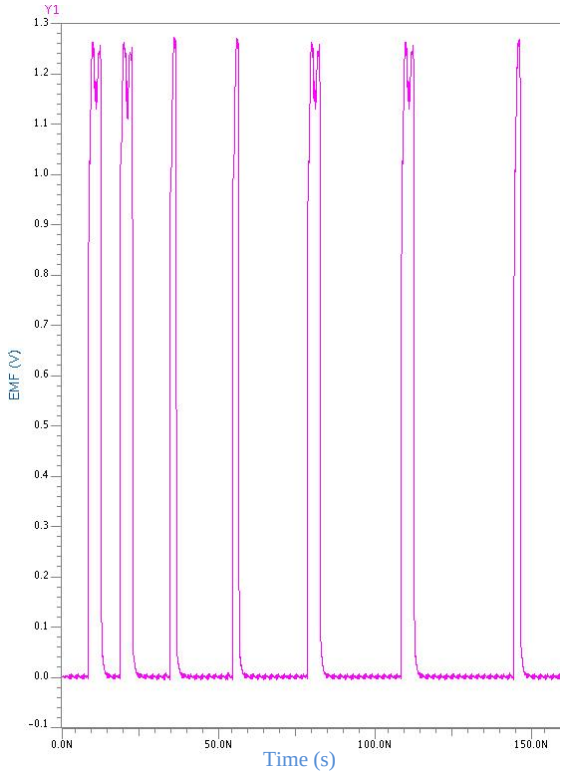


Figure B.10. Output of DFF (the chip output)

APPENDIX C

```
library disciplines;
	use disciplines.electromagnetic_system.all;
library ieee;
	use ieee.electrical_systems.all;
	use ieee.math_real.all;
	use ieee.std_logic_1164.all;
	use ieee.std_logic_arith.all;
entity ppm_with_after_vhdl_ams is
	generic (counter_time: integer := 249);
	port (signal ctrl_clock: in std_logic:= '0';
		signal data_in: in std_logic := '0';
		signal enable: in std_logic := '0';
		signal count_one_out: out integer := 0;
		signal count_zero_out: out integer := 0;
		signal ppm_out: out std_logic := '0');
end ppm_with_after_vhdl_ams;
architecture arch of ppm_with_after_vhdl_ams is
	signal control: std_logic;
	signal ppm_out_temp: std_logic := '0';
	signal count_one : integer := 0;
	signal count_zero : integer := 0;
	signal deneme: std_logic := '0';
begin
ppm: process (data_in, ctrl_clock)
begin
	if enable = '1' then
		if data_in = '1' then
			if ctrl_clock'event then
				count_one <= count_one + 1;
```

```
                    if count_one >= counter_time - 100 then
                        ppm_out <= '1';
                    end if;
                    if count_one >= counter_time then
                        ppm_out <= '0';
                        count_one <= 0;
                    end if;
                end if;
                count_zero <= 0;
            else
                ppm_out <= '0';
                if ctrl_clock'event then
                    count_zero <= count_zero + 1;
                    deneme <= '0';
                    if count_zero >= counter_time/2 then
                        if count_zero <= counter_time then
                            ppm_out <= '0';
                            deneme <= '1';
                        end if;
                    end if;
                    if count_zero >= counter_time/4 - 37 then
                        if deneme = '0' then
                            ppm_out <= '1';
                        end if;
                    end if;
                    if count_zero >= counter_time then
                        count_zero <= 0;
                        deneme <= '0';
                    end if;
                end if;
                count_one <= 0;
            end if;
        else
```

```
                ppm_out <= 'x';
        end if;
end process;
count_one_out <= count_one;
count_zero_out <= count_zero;
end arch;
```

```
library disciplines;
library ieee;
        use disciplines.electromagnetic_system.all;
        use ieee.math_real.all;
        use ieee.std_logic_1164.all;
entity gauss_5th_order is
        generic (sigma: real := 4.0e-12;
                a: real:= 0.2e-69;
                boundary: real := 50.0e-12;
                dc: real := 0.6);
        port (signal ctrl_clock: in std_logic:= '0';
              signal enable: in std_logic:= '0';
              signal pulse_tran: in std_logic;
              terminal output, ground :  electrical);
end entity gauss_5th_order;
architecture arch_gauss_5th_order of gauss_5th_order is
        quantity vout across iout through output to ground;
        signal first: real := 0.0;
        signal second: real := 0.0;
        signal third: real := 0.0;
        signal expo: real := 0.0;
        signal temp2,temp3,temp4: real := 0.0;
        signal clock: std_logic := '0';
        signal t: real := 0.0;
        signal vout_temp: real := 0.0;
begin
```

```
        gauss_source: process(pulse_tran, ctrl_clock, enable
begin
        if enable = '1' then
                if pulse_tran'event then
                        if pulse_tran = '1' then
                                t <= now + 20.0e-12;
                        end if;
                end if;
                first  <= (-1.0*(now-t)**5.0) / (sqrt(2.0*math_pi)*sigma**11.0);
                second <= (10.0*(now-t)**3.0) / (sqrt(2.0*math_pi)*sigma**9.0);
                third  <= (15.0*(now-t)) / (sqrt(2.0*math_pi)*sigma**7.0);
                expo   <= (-1.0*(now-t)**2.0) / (2.0*sigma**2.0);
                vout_temp <= (a*(first+second-third)*exp(expo));
        else
                vout_temp <= 0.0;
        end if;
end process gauss_source;
vout == dc + vout_temp;
end architecture arch_gauss_5th_order;
```

```
library disciplines;
library ieee;
        use disciplines.electromagnetic_system.all;
        use ieee.math_real.all;
        use ieee.std_logic_1164.all;
entity   squaring_unit is
        port (signal enable: in std_logic:= '0';
                terminal input: electrical;
                terminal output: electrical;
                terminal ground: electrical);
end entity squaring_unit;
architecture arch_squaring_unit of squaring_unit is
        quantity vin across input to ground;
```

```
        quantity vout across i through output to ground;
begin
        if enable = '1' use
                vout == vin**2.0;
        else
                vout == 0.0;
end use;
end architecture arch_squaring_unit;
```

```
library disciplines;
        use disciplines.electromagnetic_system.all;
library ieee;
        use ieee.std_logic_1164.all;
entity int_and_dump is
        port (terminal input: electrical;
                terminal output: electrical;
                terminal ground: electrical;
                signal enable: in std_logic:= '0';
                signal ctrl_clock: in std_logic:= '0';
                signal temp_out: out real:= 0.0;
                signal timer_out: out integer;
                signal ctrl_out: out std_logic:= '0';
                signal integrate_out: out std_logic);
end entity int_and_dump;
architecture arch_int_and_dump of int_and_dump is
        quantity vin across input to ground;
        quantity vout across i through output to ground;
        signal integrate_temp : std_ulogic:='0';
        signal ctrl: std_ulogic:='0';
        signal timer: integer:= 0;
        signal temp: real:=0.0;
        signal temp1: real:=0.0;
        signal vtemp: real:=0.0;
```

```
        signal vout_temp: real:=0.0;
        signal eksi: real:= 0.0;
begin
pulse_source:process (ctrl_clock
begin
        if enable = '1' then
                if ctrl_clock'event then
                        timer <= timer + 1;
                        if timer = 25 then
                                eksi <= vin'integ;
                        end if;
                        if timer <= 59 then
                                vtemp <= vin'integ;
                                vout_temp <= vtemp - eksi;
                        else
                                if timer < 124 then
                                        vout_temp <= 0.0;
                                end if;
                                if timer = 124 then
                                        temp <= vin'integ;
                                        timer <= 0;
                                end if;
                        end if;
                end if;
        else
                vout_temp <= 0.0;
        end if;
end process pulse_source;
vout == vout_temp; -- temp;
timer_out <= timer;
temp_out <= temp;
end architecture arch_int_and_dump;
```

```
library ieee;
        use ieee.std_logic_1164.all;
library ieee_proposed;
        use ieee_proposed.electrical_systems.all;
entity sample_and_hold is
        port (signal enable: in std_logic:= '0';
                signal ctrl_clock: in std_logic:= '0';
                sample_out: out real;
                signal vin_hold_out: out real;
                signal sample_timer_out: out integer;
                signal stop_flag_out: out std_logic;
                terminal input:  electrical;
                terminal output:  electrical;
                terminal ground:  electrical);
end entity sample_and_hold;
architecture arch_sample_and_hold of sample_and_hold is
        signal sample: std_ulogic:= '0';
        signal vin_hold: real:=0.0;
        signal v_temp: real:= 0.0;
        signal sample_timer: integer:= 0;
        signal hold_timer: integer:= 0;
        signal ctrl: std_logic:= '0';
        quantity vin across input to ground;
        quantity vout across i through output to ground;
begin
        pulse_source:process (ctrl_clock
begin
        if enable = '1' then
                if ctrl_clock'event then
                        sample_timer <= sample_timer + 1;
                        if sample_timer =  60 then
                                vin_hold <= vin;
                        elsif sample_timer = 110 then
```

```
                        vin_hold <= 0.0;
                    elsif sample_timer = 124 then
                        sample_timer <= 0;
                    end if;
                    v_temp <= (vin + vin_hold);
                end if;
        else
                v_temp <= 0.0;
        end if;
end process pulse_source;
vin_hold_out <= v_temp;
sample_out <= v_temp;
vout == v_temp;
sample_timer_out <= sample_timer;
end architecture arch_sample_and_hold;
```

```
library disciplines;
        use disciplines.electromagnetic_system.all;
library ieee;
        use ieee.std_logic_1164.all;
entity a2d_1 is
        generic (vref_plus_gen: real := 0.18e-15;
                  vref_minus_gen: real := 0.0);
        port (signal enable: in std_logic:= '0';
              signal dout: out std_logic_vector(4 downto 0);
              signal underflow: out std_logic;
              signal overflow: out std_logic;
              signal vin: in real);
end entity a2d_1;
architecture quickstart of a2d_1 is
        signal encode: std_ulogic;
        constant vref_plus: real:= vref_plus_gen;
        constant vref_minus: real:= vref_minus_gen;
```

```
        quantity delta :real; --sensitivity
begin
delta == (vref_plus - vref_minus)/2.0**5;
pulse_source:
begin
loop
        encode <= '0';
        wait for 10 fs;
        encode <= '1';
        wait for 10 fs;
end loop;
end process pulse_source;
p1: process
        variable count: integer := 0;
        variable overflow_tmp, underflow_tmp: std_logic;
        variable dout_tmp: std_logic_vector (4 downto 0);
begin
        wait until encode='1';
        if vin >= vref_plus then
                overflow_tmp  := '1';
                underflow_tmp := '0';
                count := (2**5)-1;
        elsif vin   <= vref_minus then
                overflow_tmp  := '0';
                underflow_tmp := '1';
                count := 0;
        else
                overflow_tmp  := '0';
                underflow_tmp := '0';
                count := integer((vin - vref_minus)/delta);
        end if;
        if enable = '1' then
                l1: for i in 4 downto 0 loop
```

```
                if count >= 2**i then
                        dout_tmp(i) := '1';
                        count := count-2**i;
                else
                        dout_tmp(i) := '0';
                end if;
                dout(i) <= dout_tmp(i);
        end loop l1;
        else
                dout <= "xxxxx";
        end if;
end process p1;
end architecture quickstart;
```

```
library disciplines;
        use disciplines.electromagnetic_system.all;
library ieee;
        use ieee.electrical_systems.all;
        use ieee.math_real.all;
        use ieee.std_logic_1164.all;
        use ieee.std_logic_arith.all;
entity demodulator_vhdl_ams is
        generic (count_time: integer:= 250;
                  threshold: integer:= 9);
        port (signal enable: in std_logic:= '0';
              signal ctrl_clock: in std_logic:= '0';
              signal demod_in: in std_logic_vector (4 downto 0);
              signal demod_out: out std_logic;
              signal first_half_ok: out std_logic:= '0';
              signal second_half_ok: out std_logic:= '0';
              signal first_half_out: out integer:= 0;
              signal second_half_out: out integer:= 0;
              signal timer_out: out integer:= 0);
```

```
end entity demodulator_vhdl_ams;
architecture arch of demodulator_vhdl_ams is
        signal control: std_logic:= '0';
        signal first_half_ok_temp: std_logic:= '0';
        signal second_half_ok_temp: std_logic:= '0';
        signal timer: integer:= 0;
        signal first_half, first_half_temp: integer:= 0;
        signal second_half, second_half_temp: integer:= 0;
begin
demod_arch: process (ctrl_clock)
begin
        if enable = '1' then
                if ctrl_clock'event then
                        timer <= timer + 1;
                        if timer = (count_time/2) - 35 then
                                first_half_ok_temp <= '1';
                        elsif timer = count_time/2 - 34 then
                                first_half_ok_temp <= '0';
                        elsif timer = count_time - 35 then
                                second_half_ok_temp <= '1';
                        elsif timer = count_time - 34 then
                                second_half_ok_temp <= '0';
                end if;
                if timer = count_time then
                        timer <= 0;
                end if;
                if first_half_ok_temp = '1' then
                        first_half <= conv_integer(unsigned(demod_in));
                else
                        first_half <= first_half;
                end if;
                if second_half_ok_temp = '1' then
                        second_half <= conv_integer(unsigned(demod_in));
```

```
                else
                        second_half <= second_half;
                end if;
                if timer = 0 then
                        if first_half < second_half then
                                demod_out <= '1';
                        elsif first_half > second_half then
                                demod_out <= '0';
                        end if;
                end if;
        end if;
else
demod_out <= 'x';
end if;
end process demod_arch;
first_half_ok <= first_half_ok_temp;
second_half_ok <= second_half_ok_temp;
timer_out <= timer;
first_half_out <= first_half;
second_half_out <= second_half;
end arch;
```

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