ADAPTIVE BIAS AND CLASS AB OPERATIONAL AMPLIFIER TOPOLOGIES FOR SIGMA DELTA CONVERTERS

by

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ABSTRACT

ADAPTIVE BIAS AND CLASS AB OPERATIONAL AMPLIFIER TOPOLOGIES FOR SIGMA DELTA CONVERTERS

The technological improvements in digital Very Large Scale Integrated (VLSI) circuits increase the need of analog digital converter with high performance and lower power consumption. Principally, the oversampling techniques such as sigma delta modulation should be chosen instead of Nyquist rate analog digital converters to satisfy this need. Since sigma delta modulation combines oversampling, quantization noise shaping and digital filtering in order to achieve high performance. Also, the power consumption and the speed performance of the operational amplifiers which are utilized in in the modulators should be optimized for low voltage and high speed applications. In this thesis, first of all, basic concepts of oversampling analog digital converters are explained then similar works which had been done before are examined. After that, a new low power operational amplifier designs in Mentor Graphics CAD tool are proposed. To reduce the power consumption of operational amplifiers in integrators as much as possible is the purpose of the research. Moreover, the proposed operational amplifiers are compared to each other in order to illustrate benefits of different topologies. Also an inverter used instead of an operational amplifier. The better topologies are also simulated within second order feedforward sigma delta modulator to find the architecture that consumes the minimum power.

ÖZET

SİGMA DELTA ÇEVİRİCİLER İÇİN UYARLANABİLİR KUTUPLAMALI VE AB SINIFI İŞLEMSEL KUVVETLENDİRİCİ TOPOLOJİLERİ

Sayısal yüksek ölçekli entegre devreler (VLSI) alanında yaşanan teknolojik gelişmeler, yüksek performanslı ve düşük güç tüketimli analog sayısal çeviricilere olan ihtiyacı artırmaktadır. Bu ihtiyacı karşılamaya yönelik yapıacak tasarımlarda öncelikle Nyquist oranlı (Nyquist-rate) analog sayısal çeviriciler yerine yüksek örneklemeli topolojilerden sigma delta modülasyon yöntemi ile tasarım yapmak bu ihtiyacı karşılamak için uygun bir seçimdir. Sigma delta modülasyon tekniği yüksek örnekleme, kuantalama gürültüsü şekillendirme ve sayısal filtreleme yöntemlerini kullanarak yüksek performans ihtiyacını karşılayabilmektedir. Bunun yanında tasarımda kullanılan işlemsel kuvvetlendiricinin güç tüketimi ve hızı da düşük güç tüketimi ve yüksek hız ihtiyacını karşılayacak şekilde yapılmalıdır. Bu tezde öncelikle basit bir şekilde yüksek örneklemeli analog sayısal çeviriciler üzerinde durularak, bu konuda daha önce yapılan tasarımlar incelenecektir. Daha sonra ise Mentor Graphics yazılımı üzerinde yapılan düşük güç tüketimli işlemsel kuvvetlendirici tasarımları sunulacaktır. Bu araştırmanın amacı integral alıcı içerisindeki işlemsel kuvvetlendiricinin güç tüketimini olabildiğince düşürmektir. Bunun yanında önerilen işlemsel kuvvetlendirici tasarımları, farklı tasarımlara ait kazançları ve kayıpları göstermek adına karşılaştırılacaktır. İşlemsel kuvvetlendirici olarak basit bir çevirici dahi kullanılmıştır. Daha öne çıkan tasarımlar ise ikinci derece ileri beslemeli sigma delta modülatör üzerinde test edilerek en az güç tüketimini gerçekleştiren yapı belirlenecektir.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS iii
ABSTRACT iv
ÖZET v
LIST OF FIGURES viii
LIST OF TABLES xiv
LIST OF SYMBOLS xv
LIST OF ACRONYMS/ABBREVIATIONS xvi
1. INTRODUCTION 1
1.1. Background Information and Aim of Thesis 1
1.2. Thesis Outline 7
2. SIGMA - DELTA MODULATORS 9
2.1. Basic Concepts 9
2.1.1. Quantization Noise 9
2.1.2. Oversampling 11
2.1.3. Performance Measures 12
2.1.3.1. SNR 13
2.1.3.2. SINAD 13
2.1.3.3. DR 13
2.1.3.4. ENOB 14
2.2. Sigma Delta Modulators 14
2.2.1. Sigma Delta Modulation 14
2.2.2. Noise Shaping 15
2.2.3. First Order Sigma Delta Modulators 18
2.2.4. Second Order Sigma Delta Modulators 20
3. CIRCUIT DESIGN, ANALYSIS AND RESULTS 24
3.1. Operational Amplifiers 24
3.1.1. Class A Operational Amplifiers 24
3.1.2. Class AB Operational Amplifiers 26
3.1.3. Adaptive Biasing Operational Amplifiers 27

3.2. Implementation of Circuits 28
3.2.1. Class AB/AB Very Low Power Operational Amplifier 28
3.2.2. Class AB Operational Amplifier (without RC Compensation) . 33
3.2.3. Class AB Operational Amplifier 39
3.2.4. Class AB Operational Amplifier with Cascode 43
3.2.5. Inverter used as a Class AB Operational Amplifier 48
3.2.6. Adaptive Biasing CMOS Amplifier 51
4. CONCLUSIONS AND FUTURE WORKS 60
REFERENCES 62

LIST OF FIGURES

Figure 1.1. Conventional (Nyquist rate) Converters [1]. 1

Figure 1.2. Oversampling Converters. 3

Figure 1.3. Conversion Resolution vs. Signal Bandwidth Converted [2]. 4

Figure 1.4. Block Diagram of First Order Sigma Delta Modulator [3]. 5

Figure 1.5. Power Consumption of Parts in SD Modulator. 7

Figure 2.1. Block Diagram of Oversampling SD Modulator [4]. 9

Figure 2.2. Linear Model of Quantizer [5]. 10

Figure 2.3. Oversampling Process [6]. 12

Figure 2.4. Block Diagram of a Delta Modulator [3]. 14

Figure 2.5. Block Diagram of a SD Modulator [3]. 15

Figure 2.6. Noise Shaping [3]. 16

Figure 2.7. Normalized Frequency [7]. 17

Figure 2.8. Block Diagram of First Order Sigma Delta Modulator [3]. 18

Figure 2.9. Linear Model of First Order Sigma Delta Modulator [3]. 19

Figure 2.10. Standard Second Order Sigma Delta Modulator [8]. 21

Figure 2.11. Second Order Sigma Delta Modulator [9]. 21

Figure 2.12. Second Order Sigma Delta Modulator [9]. 22

Figure 2.13. Second Order Sigma Delta Modulator [3]. 22

Figure 2.14. Second Order Sigma Delta Modulator [9]. 22

Figure 3.1. Output Stage of a Class A Operational Amplifier [10]. 24

Figure 3.2. Output Voltage vs. Time Graph of a Class A Operational Amplifier [10]. 25

Figure 3.3. Output Current Characteristics of a Class A Operational Amplifier [11]. 25

Figure 3.4. Typical Output Stage of a Class AB Operational Amplifier [10]. . 26

Figure 3.5. Output Voltage Swing of a Class AB Operational Amplifier [10]. . 27

Figure 3.6. Output Current Characteristics of a Class AB Operational Amplifier [11]. 27

Figure 3.7. Output Current Behavior with Changing Current Factor A [10]. . 28

Figure 3.8. Figure of Class AB/AB Amplifier [12]. 29

Figure 3.9. Schematic of Class AB/AB Opamp with Common Mode Feedback. 30

Figure 3.10. Testbench of Class AB/AB Opamp. 31

Figure 3.11. Transient Simulation Result of Class AB/AB Opamp. 31

Figure 3.12. AC Simulation Result of Class AB/AB Opamp. 32

Figure 3.13. SR Simulation Result of Class AB/AB Opamp for $10mV$ peak to peak Input voltage. 32

Figure 3.14. SR Simulation Result of Class AB/AB Opamp for $1V$ peak to peak Input voltage. 33

Figure 3.15. Figure of Class AB/AB Amplifier without RC Compensation [12]. 34

Figure 3.16. Schematic of Class AB/AB Opamp with Common Mode Feedback without RC Compensation. 34

Figure 3.17. Testbench of Class AB/AB Opamp without RC Compensation. . . 35

Figure 3.18. Transient Simulation Result of Class AB/AB Opamp without RC Compensation. 36

Figure 3.19. AC Simulation Result of Class AB/AB Opamp without RC Compensation. 36

Figure 3.20. SR Simulation Result of Class AB/AB Opamp without RC Compensation for $10mV$ peak to peak Input voltage. 37

Figure 3.21. SR Simulation Result of Class AB/AB Opamp without RC Compensation for $1V$ peak to peak Input voltage. 38

Figure 3.22. Figure of Class AB Amplifier [12]. 39

Figure 3.23. Class AB Opamp with Common Mode Feedback. 40

Figure 3.24. Testbench of Class AB Opamp with Common Mode Feedback. . . 41

Figure 3.25. Transient Simulation Result of Class AB Opamp with Common Mode Feedback. 41

Figure 3.26. AC Simulation Result of Class AB Opamp. 42

Figure 3.27. SR Result of Class AB Opamp for $10mV$ peak to peak input voltage. 42

Figure 3.28. SR Result of Class AB Opamp for $1V$ peak to peak input voltage. 43

Figure 3.29. Class AB Operational Amplifier [13]. 44

Figure 3.30. Schematic of Class AB Opamp with Cascode Stage and Common Mode Feedback. 45

Figure 3.31. Testbench of Class AB Opamp with Cascode Stage. 45

Figure 3.32. Transient Simulation Result of Class AB Opamp with Cascode Stage. 46

Figure 3.33. AC Simulation Result of Class AB Opamp with Cascode Stage. . 47

Figure 3.34. SR Simulation Result of Class AB Opamp with Cascode Stage for $10mV$ peak to peak Input voltage. 47

Figure 3.35. SR Simulation Result of Class AB Opamp with Cascode Stage for $1V$ peak to peak Input voltage. 48

Figure 3.36. Voltage Drops in Differential Input Pairs [14]. 48

Figure 3.37. Voltage Drops in Differential Input Pairs without Tail Current Source [14]. 49

Figure 3.38. CMOS Inverter. 49

Figure 3.39. Characteristics of an Inverter: DC Gain and GB vs. Supply Voltage [15]. 50

Figure 3.40. Transient Simulation Result of Inverter. 51

Figure 3.41. AC Simulation Result of Inverter. 52

Figure 3.42. SR Simulation Result of Inverter with $10mV$ peak to peak Input Voltage. 52

Figure 3.43. SR Simulation Result of Inverter with $1V$ peak to peak Input Voltage. 53

Figure 3.44. Adaptive Biasing Operational Amplifier [16]. 53

Figure 3.45. Current Subtractor Realizing $A.(I_2 - I_1)$. 54

Figure 3.46. Behaviour of I_{out} vs V_{in} for Different Values of A. 55

Figure 3.47. Adaptive Biasing Opamp with Common Mode Feedback. 56

Figure 3.48. Testbench of Adaptive Biasing Opamp. 57

Figure 3.49. Transient Simulation Result of Adaptive Biasing Opamp. 57

Figure 3.50. AC Simulation Result of Adaptive Biasing Opamp. 58

Figure 3.51. SR Result of Adaptive Biasing Opamp for $10mV$ peak to peak input voltage. 59

Figure 3.52. SR Result of Adaptive Biasing Opamp for $1V$ peak to peak input voltage. 59

LIST OF TABLES

Table 3.1. Simulation Results of Class AB/AB Operational Amplifiers. 33

Table 3.2. Simulation Results of Class AB/AB Operational Amplifiers with no Compensation. 38

Table 3.3. Simulation Results of Class AB Operational Amplifiers. 43

Table 3.4. Simulation Results of Class AB Operational Amplifiers with Cascode Stage. 46

Table 3.5. Simulation Results of Inverter Used as Operational Amplifier. . . . 51

Table 3.6. Simulation Results of Adaptive Biasing Operational Amplifiers. . . 58

Table 4.1. Comparison of Specs of Designed Operational Amplifiers. 61

LIST OF SYMBOLS

A	Current factor in Adaptive Biased Opamp
A_V	Voltage Gain
C_c	Compensation Capacitance
C_L	Load Capacitance
I	Current
I_B	Bias Current
I_{max}	Maximum Current
I_{sat}	Saturation Current
I_p	Tail Current of Adaptive Biased Opamp
V_{CAS}	Bias Voltage of Cascode Opamp
V_{diff}	Differential Input Voltage
V_{DD}	Supply Voltage
V_{GS}	Gate to Source Voltage
V_{diff}	Differential Input Voltage
V_{in}	Input Voltage
V_{Th}	Threshold Voltage
V_{Tn}	Threshold Voltage of NMOS Transistor
V_{Tp}	Threshold Voltage of PMOS Transistor
V_{Out}	Output Voltage
R_c	Compensation Resistance
ε_Q	Quantization Noise

LIST OF ACRONYMS/ABBREVIATIONS

ADC	Analog to Digital Converter
BW	Bandwidth
CAD	Computer-aided Design
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital to Analog Converter
dB	Decibel
DC	Direct Current
DNL	Differential Non-linearity Error
ENOB	Effective Number of Bits
ERBW	Effective Resolution Bandwidth
ESD	Electrostatic Discharge
GBW	Gain Bandwidth
HD	Harmonic Distortion
IMD	Intermodulation Distortion
IMD2	Two Tone Intermodulation Distortion
INL	Integral Non-linearity Error
MTPR	Multi Tone Power Ratio
NPR	Noise Power Ratio
NTF	Noise Transfer Function
opamp	Operational Amplifier
OSR	Over-sampling Ratio
OTA	Operational Transconductance Amplifier
PCM	Pulse Code Modulation
PSD	Power Spectral Density
rms	Root-mean-square
SD	Signa Delta
SFDR	Spurious Free Dynamic Range
SINAD or SNDR	Signal-to-noise-and-distortion Ratio

SNR	Signal-to-noise Ratio
SR	Slew Rate
STF	Signal Transfer Function
TSD	Total Spurius Distortion
UMC	United Microelectronics Corporation
VLSI	Very-large-scale-integration

1. INTRODUCTION

1.1. Background Information and Aim of Thesis

Most of the signals present in our daily lives can be classified as analog signals, whereas most of the signals present in computers and other communication devices are composed of $1s$ and $0s$. In other words, they can be classified as digital ones. In order to provide the communication between real world and computer world, it is mandatory to use such converters as analog to digital converters (ADC) and digital to analog converters (DAC). The ease of processing, storing and transmission of data in digital domain leads designers to use digital signal representations with help of ADC circuits.

Converting signals between analog to digital is possible with conventional (Nyquist rate) and over-sampling converters. Conventional converters, which are shown in Figure 1.1, are hard to implement in very large scale integrated (VLSI) circuits due to the need of precise analog components within the filters used in design and also vulnerability of noise and interference. However, the virtue of the conventional method is to use low sampling frequency, mostly the Nyquist rate of the signal that can be calculated as twice the signal bandwidth.

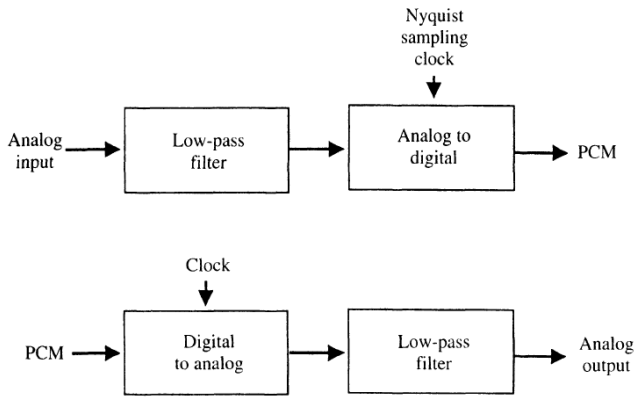

Figure 1.1. Conventional (Nyquist rate) Converters [1].

In order to attenuate undesired high frequency out of band components that alias into the signal while sampling at the Nyquist rate, a low-pass filter is employed at the analog input to the encoder shown in Figure 1.1. Next to the low-pass filter, ADC is used, which can be replaced with flash, successive-approximation or ramp converters in order to achieve fast, moderate or slow conversion operations. At the output of DAC, another low-pass filter is used to smooth sampled outputs at the desired smoothing specification given by the system. There is no doubt that the conventional converter circuits require highly accurate analog circuit components to achieve high overall resolution objective.

However, oversampling converters, shown in Figure 1.2, have higher tolerance to the variations in analog components to achieve high resolution with use of relatively fast and complex digital signal processing circuitry. At this topology, modulation and demodulation take place at such high sampling rate in order to avoid aliasing. Afterwards, smoothing functions are applied by digital filters. The reason of extensive use of digital signal processing in over-sampling converters is due to the fact that fine-line VLSI is capable of designing and implementing relatively fast digital circuits rather than providing precise components of analog circuits. Since sampling rate of over-sampling converters mostly needs to be a few orders of magnitude higher than Nyquist rate, those over-sampling methods are best suited for relatively low-frequency signals.

A notable difference between conventional converters and over-sampling ones can be shown by testing and specifying their performance. In conventional converters, there is a one to one correspondence between input and output sample values. Therefore, it is possible to describe accuracy of the conventional converters by comparing the values of corresponding input and output samples. Conversely, in over-sampling converters there is no such correspondence between input and output values. This is due to the fact that digital low-pass filters inherently affect the overall topology of the circuitry. Thus, each input sample value contributes to a whole branch of output samples. As a result, performance of over-sampling converters can be described with such techniques from communication theory as measuring root-mean-square (rms) noise under various

conditions, distortions introduced into sinusoidal signals and also frequency responses.

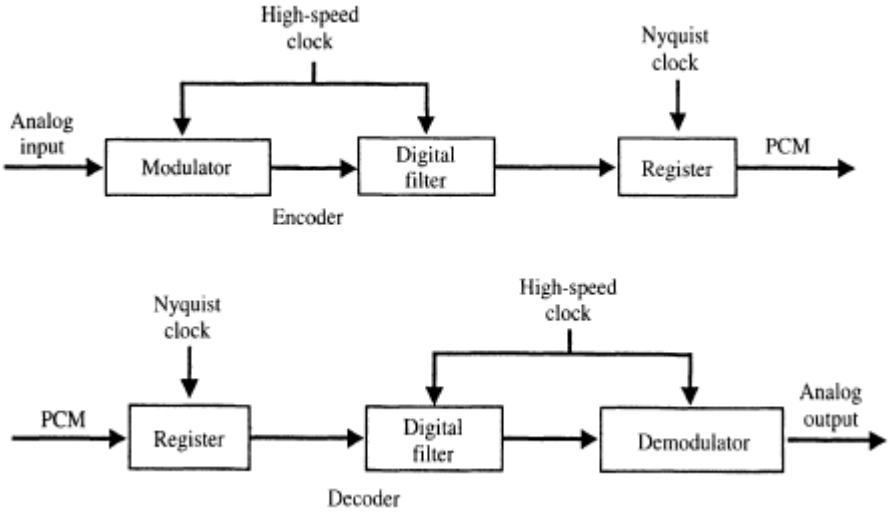

Figure 1.2. Oversampling Converters.

VLSI technology of today provides designers to use fast digital circuits and analog circuits within the same die that results in low cost and low power with relatively high resolution ADC and DAC design. However, implementing analog and digital circuitry on the same die (sharing the same body terminal) results in leakage of injected noise from digital circuitry to the sensitive analog part. Because of injected noise that aliases into the baseband, resolution of the ADC decreases significantly. Furthermore, anti-aliasing filter, sample-and-hold circuitry with good performance and also jitter-free timing are required in order to have a state-of-art design [17].

All the problems which have been mentioned above can be solved with use of over-sampling converters. One of the most popular over-sampling converter architectures can be shown as sigma delta (SD) modulation which includes over-sampling, digital filtering and quantization noise shaping to achieve high performance with relatively less complex analog circuit design.

Moreover, use of SD modulator has many advantages in designing ADCs. One of the most notable advantages of SD modulation can be illustrated as use of only 1-bit

quantization while converting analog signal and use of analog signal processing circuits with an accuracy that is mostly much less than the resolution of overall converter [2]. Therefore, an excellent linearity is present in the converter. Also in applications with relatively low signal bandwidth, such as speech and digital audio applications, highest resolution of conversation can be attained with use of SD topology in analog to digital conversation as shown in Figure 1.3.

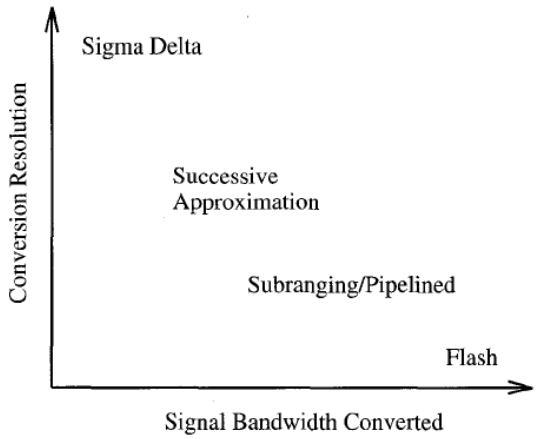

Figure 1.3. Conversion Resolution vs. Signal Bandwidth Converted [2].

Indeed, the bandwidth-resolution relation can be summarized as ADCs based on SD modulations which bring the need for higher sampling rates than Nyquist rate because of their negative feedback. Note that, although digital filtering brings along several advantages in terms of resolution, its delay reduction is a challenging aspect for the same amplitude [8]. Also in decimation filter part, leaked noise from digital circuitry, as a result of sharing the same die with analog part, can be eliminated by designing a proper noise adjustment part in the digital decimation filter. Final advantage of using SD based ADCs is the elimination of sample-and-hold amplifier just before the ADC. This is due to the fact that the design of sample-and-hold amplifiers with an accuracy of more than 10 bits can be problematic because of dielectric absorption in capacitors [17, 18].

An SD modulator is composed of an analog filter and a quantizer enclosed in a feedback loop. Cascaded with the filter, feedback loop plays a key role to decrease

quantization noise at low frequencies whereas boosting the noise components at high frequency. However, the noise amplified at higher frequencies can be removed properly with a digital low pass filter at the output of the SD modulator where the signal is sampled with higher sampling frequency than the Nyquist rate [8].

The simplest SD modulator is a first-order loop wherein the filter contains a single integrator. The structure of this SD modulator is shown in Figure 1.4. However, the quantization noise from first-order modulators is highly correlated and high over-sampling ratio is needed to achieve higher resolution.

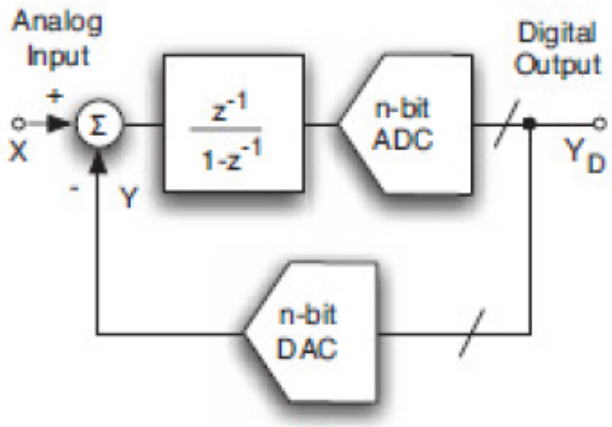

Figure 1.4. Block Diagram of First Order Sigma Delta Modulator [3].

Higher order SD modulators, containing more integrators in the forward path, offer an increased resolution. However, those modulators, which consist of more than two integrators, suffer from potential instability as a result of the accumulation of large signals in the integrators. In order to achieve the performance, which is comparable with higher order modulators and also deals with the stability problem, several first-order modulators can be cascaded. However, in those architectures it is essential to have precise gain matching between each individual first-order sections, which is technically quite hard to achieve such analog to digital conversion because of the parameter tolerances and component mismatches. In order to have high resolution in analog to digital conversation, second-order SD modulators seem to be an attractive approach. The efficiency of second-order SD modulator architectures has been illustrated in some

applications as digital speech processing systems and voice band telecommunications codecs which consist of ADCs based on second order SD modulation [8].

Maintaining the required resolution with sigma delta modulators is not the only goal that is needed to be achieved. Furthermore, design should also meet the requirements of low power consumption. Rapid development in VLSI circuit design also brings smaller and smaller transistor sizes which need lower and lower supply voltage to operate. Apart from the developments originated from technology, improvements in digital circuit design such as decreasing overall number of gates to achieve the same goal and employing adaptive biased operational amplifiers instead of using switched capacitor filters for noise shaping leads to circuit with less power consumption.

Moreover, low voltage and high speed applications require optimizing speed of operational amplifiers and also voltage headroom needs to fulfill the required voltage swing at the output of the operational amplifier. The possible clamp at the output of the operational amplifier may result in loss of feedback control. The reason of loss in control can be explained as the fact that inverting period of the operational amplifier is no longer tightened to the non-inverting period and is free to span up and down causing an incomplete transfer of the input signal. Therefore, the designer should ensure exact dynamic range of operational amplifier used in integrator. Indeed, the first integrator is the most crucial one in terms of dynamic range due to the fact that saturation error of that stage is not shaped by any transfer function. Also, the saturation at the second integrator and quantizer limits the overall performance of modulator. Therefore, it is needed to estimate voltage swings and keep them within the values which do not lead the circuit to saturate. On the other hand, the voltage swings should be large enough not to interfere with noise generated from the system [3].

Hence, analog parts of the circuit can be adjusted to decrease power consumption while keeping the speed and voltage swing regularities present by using specific low power analog blocks. Furthermore, digital part can be optimized in terms of power by optimizing number of logic gates, the supply voltage value and the synthesized technology.

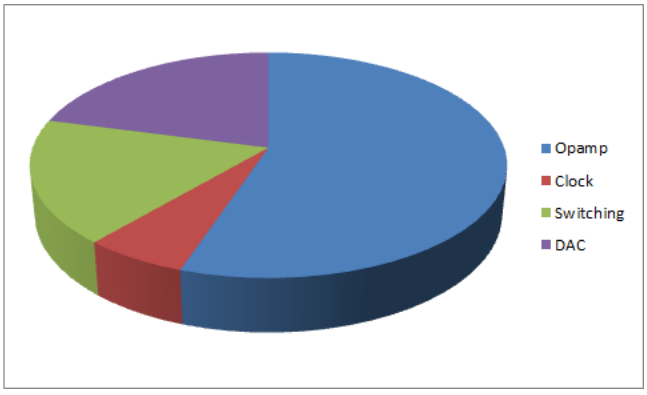

Figure 1.5. Power Consumption of Parts in SD Modulator.

The aim of this thesis is to propose new low power solutions for second-order SD modulators by building different operational amplifiers in Mentor Graphics CAD tool environment in UMC 0.18μm technology. In order to achieve the low power objective, this thesis focuses on the analog point of view and considers designing of different operational amplifiers, which can be classified as the most power hungry analog part of the SD modulator. Given second order SD modulator, different operational amplifier are used to minimize total power consumption of the analog part. As a result of designed building blocks, the performance of these different designs are evaluated and a comprehensive comparison between them is presented in terms of power consumption to reach state-of-art architecture.

1.2. Thesis Outline

The next chapter focuses on oversampling SD modulators and basic concepts as quantization noise, oversampling and some measurements of performance. Simply concept of SD modulators explained, then first and second order SD modulators are examined, then noise shaping concept is clarified. At the end of this chapter, optimum second order SD modulator architecture is selected.

In Chapter 3, the proposed second order SD is briefly explained and in analog point of view the most power hungry part which is operational amplifier options are

discussed. For each operational amplifier design, the performance parameters such as power consumption, signal-to-noise ratio (SNR) of the overall SD modulator expressed. Also circuit design of each operational amplifier is explained in detail.

Finally, Chapter 4 concludes the thesis and possible future work to contribute the same topic is analyzed.

2. SIGMA - DELTA MODULATORS

In this chapter, basic concepts of oversampling SD modulators such as quantization noise, oversampling and performance measurements are expressed. Then, the chapter continues with properties of first-order and the second-order SD modulators. Finally, optimum second-order SD modulator design procedure is illustrated.

An SD converter is composed of filtering, sampling and quantization parts with feedback loop, including a DAC and a decimation filter as a post filter. Analog to digital conversation is done by filtering, sampling and quantization parts with feedback connection through a DAC. Before that loop, an antialiasing filter is used to ensure incoming bandwidth is limited. After the loop, another filter, which is decimation filter, is used to lower the sampling frequency to satisfy Nyquist criteria [10]. The block diagram of oversampling SD ADC is given in Figure 2.1.

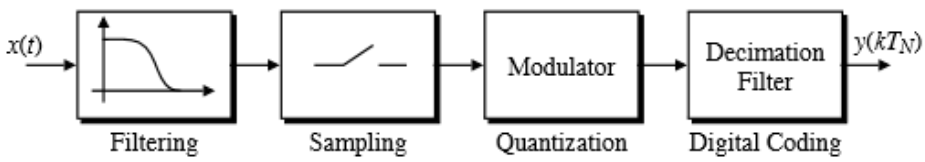

Figure 2.1. Block Diagram of Oversampling SD Modulator [4].

In Figure 2.1, analog input $x(t)$ is the input terminal and at the end of the diagram, $y(kT_N)$, is a high resolution digital output.

2.1. Basic Concepts

2.1.1. Quantization Noise

The heart of a SD modulator and any other ADC can be shown as quantizer, which is a device simply maps real numbers into a finite set of possible representative values [1]. Any analysis of a SD modulator has to consider the behavior of quantizer,

which is an essential part of the system. The process of quantization is linear and introduces errors as a part of this process. Those errors named as quantization errors are simply the difference of output and input of quantizer. Therefore, the output of quantizer can be expressed as sum of input and the quantization error. Mostly, the scale of errors introduced by the quantizer is smaller than the actual signal in terms of amplitude. However, if the signal has small amplitude and the error has the same order of magnitude with the signal, this error will be the larger part of the signal, which is an undesirable outcome. Also, quantization error has components in different frequencies, so that quantization error is also called quantization noise. Quantization noise plays a key role to determine signal-to-noise ratio (SNR). Although quantizer is conceptually simple, it is hard to analyze from the mathematical point of view due to the non-linearity present. Therefore, quantizer is usually linearized by using an input independent additive white noise model as shown in Figure 2.2.

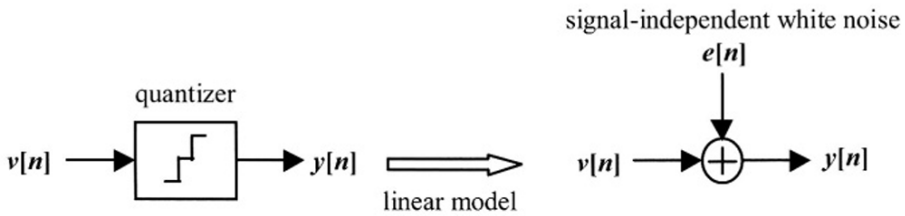

Figure 2.2. Linear Model of Quantizer [5].

With reference to Figure 2.2, quantization representation can be shown as. $y[n] = e[n] + v[n]$, where the output of the quantizer is y and v denotes the input of the quantizer with quantization error being e. Given that the range of the quantizer is $V_{fs} = V_{max} - V_{min}$ and the number of quantization intervals is M, the amplitude of each quantization step is found as: $\Delta = V_{fs}/M$. Therefore, middle point of the nth interval can be defined as $V_{m,n} = (n - \frac{1}{2}).\Delta$. Then output of quantizer can be rewritten as. $y[n] = v[n] + e[n] = (n - \frac{1}{2}).\Delta$, where $n\Delta < v[n] < (n+1)\Delta$.

The linear method used, suggests addition input and error done in order to find output of quantizer. Quantization error is a random function distributed between $-\Delta/2$ to $+\Delta/2$. This means that the value will be zero and power of mean equals to

variance.

$$\sigma_e^2 = \int_{-\Delta/2}^{+\Delta/2} e^2 f_e(e)\, de = \int_{-\Delta/2}^{+\Delta/2} e^2\, de = \frac{\Delta^2}{12} \tag{2.1}$$

Given $e[n]$ values are uncorrelated and identically distributed, and also quantization noise is white and spreads equally through each frequency values from $-fs/2$ to $fs/2$, power spectral density of the quantization noise can be expressed as: $n(f) = \frac{\Delta^2}{12 f_s}$.

2.1.2. Oversampling

Conventional (Nyquist rate) modulators cannot reach high resolutions, so that oversampling converters are handier to achieve that goal. According to Nyquist theory, the minimum sampling frequency is twice the maximum frequency of input signal. Sampling the signal in frequency f_s, which is higher than Nyquist frequency f_N is called oversampling. The ratio of sampling frequency f_s over minimum Nyquist sampling frequency is called oversampling ratio (OSR) that can be shown as:

$$OSR = f_s / f_N \tag{2.2}$$

Usually, the value of OSR is taken to be a power of 2. The result of oversampling technique for R equals to 4 is shown in Figure 2.3.

As can be seen in Figure 2.3, sampled images are not so close to each other after oversampling procedure. Therefore, design procedure of the anti-aliasing filter will be relatively straightforward. Apart from the simpler design of anti-aliasing filter, another advantage of using oversampling is that the decimation process can also be used to provide further resolution [6].

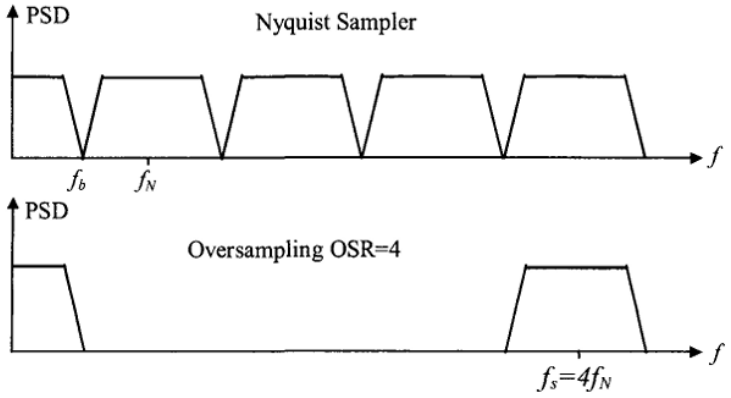

Figure 2.3. Oversampling Process [6].

To sum up, oversampling is a useful tool to increase resolution of SD ADC operation. On the other hand, using large oversampling leads to higher power consumption.

2.1.3. Performance Measures

In order to describe the performance of data converters, there are many specifications for interpreting and understanding the given material from catalogues and facilitating the use and characterization of products. Some specifications can be described in ADC, whereas some others can refer to both ADC and DAC. The specifications are divided into classes as [3].

- General Features: Type of analog signals, resolution, dynamic range, absolute maximum ratings, electrostatic discharge (ESD) notice, pin function descriptions and pin configuration, warm-up time, and drift.
- Static Specifications: Analog resolution, analog input range, offset, zero scale offset, common-mode error, full-scale error, bipolar zero offset, gain error, differential non-linearity error (DNL), monotonicity, hysteresis,missing code, integral non-linearity (INL), power dissipation, temperature ranges, thermal resistance, and lead temperature.
- Dynamic Specifications: Analog input bandwidth, input impedance, load regulation or output impedance, settling-time, cross-talk, aperture uncertainty (Clock

jitter), digital to analog glitch impulse, glitch power, equivalent input referred noise, SNR, signal-to-noise-and-distortion ratio (SINAD or SNDR),dynamic range, effective-number-of-bits (ENOB), harmonic distortion (HD), total spurious distortion (TSD), spurious free dynamic range (SFDR), intermodulation distortion (IMD), two tone intermodulation distortion (IMD2), multi-tone power ratio (MTPR), noise-power ratio (NPR), effective resolution bandwidth (ERBW), and figure of merit (FoM).

- Digital and switching specifications: Logic levels, encode or clock rate, clock timing, clock source, and sleep mode [3].

Some of the most notable specifications can be briefly summarized as:

2.1.3.1. SNR. It can simply defined as the ratio between the power of signal and the total noise derived from not only quantization but also from circuitry. Mathematically it can be defined as:

$$SNRI\ (dB) = 10\log(\frac{P_{signal}}{P_{noise}}), \tag{2.3}$$

where, P_{signal} is power of the signal and P_{noise} is power of generated noise in the circuitry.

2.1.3.2. SINAD. Simply, it can be defined similar to the SNR without nonlinear distortion terms which are generated by and accounted for the input sine wave. In other words, SINAD is defined as the ratio between root-mean-square of the signal and the root-sum-square of the harmonic components plus noise [3].

2.1.3.3. DR. Dynamic range is the value of input signal at which the SNR (or SINAD) is $0dB$. The parameter is helpful for some types of data converters which do not obtain their maximum SNR (or SINAD) at $0dB$ F_s input. This typically happens in SD converters.

2.1.3.4. ENOB. Effective number of bits measures the distortion ratio and the SNR by using bits. SINAD and ENOB are correlated as shown:

$$ENOB = \frac{(SINAD)_{dB} - 1.76}{6.02} \tag{2.4}$$

2.2. Sigma Delta Modulators

2.2.1. Sigma Delta Modulation

Oversampling was used for increasing the effectiveness of a pulse code modulation (PCM) transmission. The key role in this scheme was to use a high sampling rate to transmit the change (Δ) between successive samples apart from actual sample.

In delta modulation, an ADC quantizes the difference between the signal and estimation of the signal. At the same time, a DAC transforms the digital output into analog in the feedback loop and the integration of this signal is the estimation of the input [3]. Block diagram representation of delta modulator is shown in Figure 2.4.

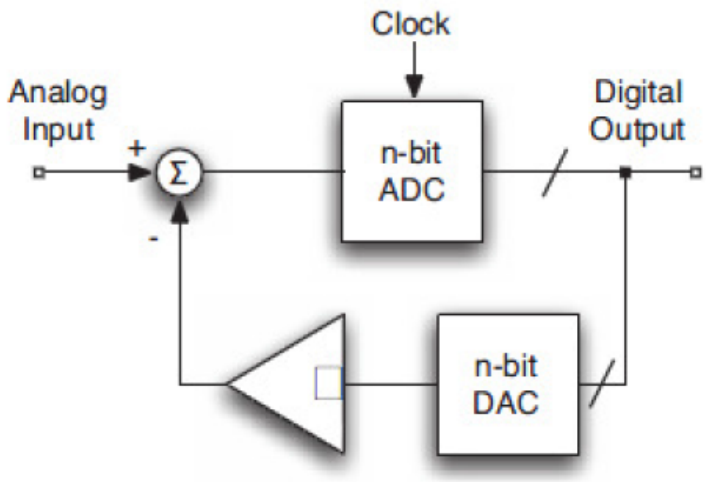

Figure 2.4. Block Diagram of a Delta Modulator [3].

During delta modulation, an ADC quantizes the difference between the signal and

its estimation, while a DAC transforms the digital output into analog through feedback loop and the integration of this signal is the estimation of the input. A modulator with that topology is hard to analyze. However, if an integrator is placed just before the delta modulator, the modulator will encode the integral of the input signal, which will be relatively smoother than input itself. The resulting modulator is called as SD modulator and topology of the SD modulator is shown in Figure 2.5.

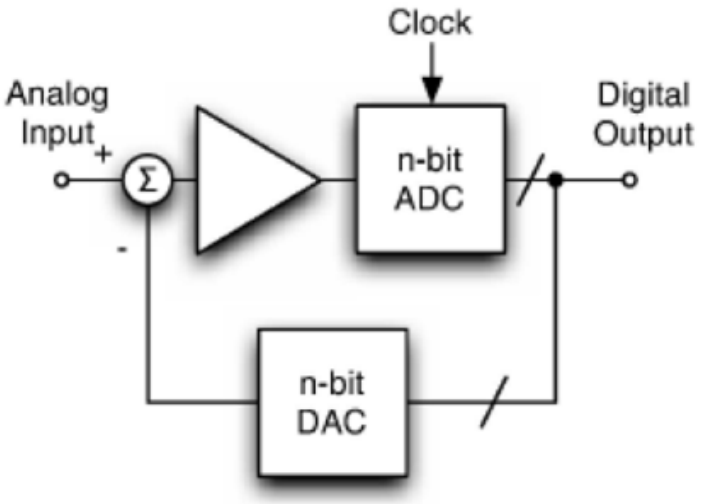

Figure 2.5. Block Diagram of a SD Modulator [3].

With reference to the block diagrams shown in Figure 2.4 and Figure 2.5, the difference between delta modulator and SD modulators is use of an integrator at the input stage. Furthermore, the difference in working principle between delta modulators and SD modulators is that in delta modulators integrator works as estimation of signal, but in SD modulators integrator operates on error difference. Thus, overall modulator behavior is changed from high-pass to low-pass [3].

2.2.2. Noise Shaping

Use of oversampling method becomes more effective if the noise spectrum is lowered in the signal band, possibly at the expenses of an increase in the out-of-band portion, thereby converting the white spectrum of the quantization noise into a shaped

spectrum. Having more noise at higher frequency regions do not lead any problem at all, since a digital filter used after the ADC removes noise present as shown in Figure 2.6.

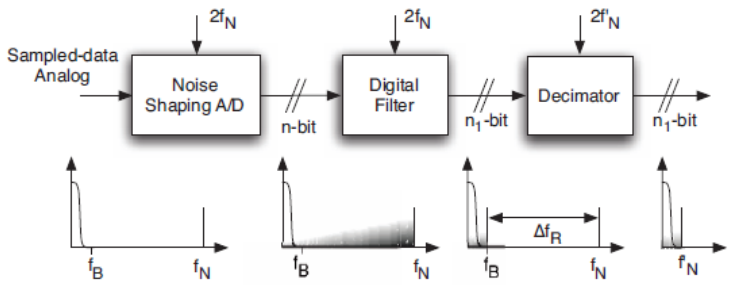

Figure 2.6. Noise Shaping [3].

The spectral shaping of the noise is one of the crucial properties of SD modulation. Noise shaping considerably enhances benefits present in ADCs. Briefly, if the inband quantization noise is attenuated strongly with a loop filter that has a high gain in the signal band, the whole procedure is called as noise shaping [3]. The noise shaping representation given Figure 2.6 is of the form

$$Y(z) = X(z)\frac{H(z)}{H(z)+1} + \frac{E(z)}{H(z)+1}, \tag{2.5}$$

where $Y(z)$, $X(z)$, $H(z)$, and $E(z)$ are the z-transforms of the output, input, transfer function of integrator, and quantization noise, respectively. Also (2.6) indicates that signal and quantization noise pass through two different transfer functions.

$$Y(z) = X(z)STF(z) + e(z)NTF(z), \tag{2.6}$$

named signal transfer function (STF) and noise transfer function (NTF). Mathematical representation of STF and NTF in the z-domain is shown as:

$$STF(z) = \frac{Y(z)}{x(z)}|_{E(z)=0} \quad and \quad NTF(z) = \frac{Y(z)}{E(z)}|_{X(z)=0.} \tag{2.7}$$

A delayless integrator can be defined as.

$$H(z) = \frac{1}{1 - z^{-1}}. \tag{2.8}$$

in the z-domain (2.5) can be simplified, since $STF(z)$ is unity and the $NTF(z)$ equals to $1 - z^{-1}$ as

$$Y(z) = X(z) + E(z)(1 - z^{-1}). \tag{2.9}$$

With reference to the mathematical expressions presented so far, output can be defined as the sum of the input signal and the quantization noise, which is shaped by a first order differentiation. In order to make an approximation to the in-band power of the quantization noise, having square magnitude of NTF in frequency domain will be useful. Given $f_s = 1$ and $f << 1$, frequency response of NTF is shown in Figure 2.7.

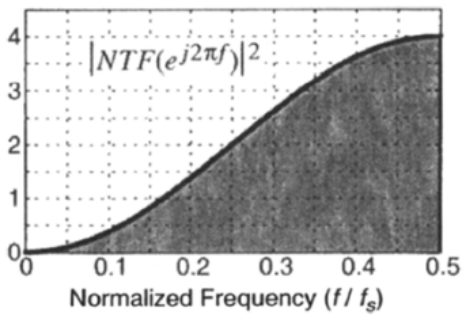

Figure 2.7. Normalized Frequency [7].

As can be seen from Figure 2.7, overall behavior of the frequency response of NTF is clearly a high pass filter behavior which suppresses the quantization noise at zero (near DC). This noise-shaping behavior also has a notable impact in the effectiveness of SD modulation.

2.2.3. First Order Sigma Delta Modulators

First order SD modulator is simply composed of an integrator serially connected to a 1-bit ADC. A 1-bit DAC enclosed in a feedback loop as illustrated in Figure 2.8.

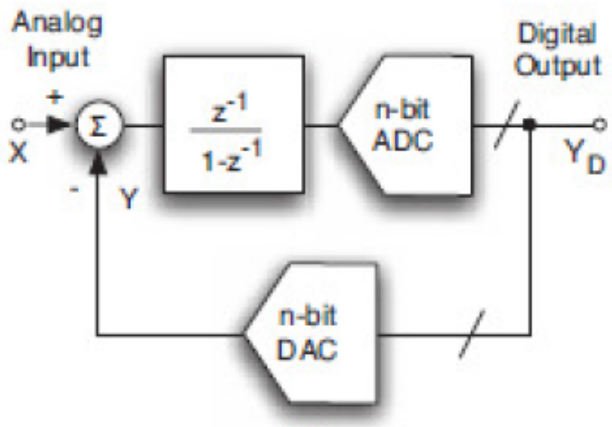

Figure 2.8. Block Diagram of First Order Sigma Delta Modulator [3].

The working principle of the block diagram shown in Figure 2.8 simply can be explained as, integrating the difference between the analog input and the output of DAC to synthesize sampled data input of the ADC. Furthermore, the SD modulator above is an illustration of noise shaping in order to push most of the undesired inband noise to the higher frequencies to remove this noise in decimation part with a low-pass filter. Also, one of the crucial techniques to increase resolution, which is oversampling, is used to spread quantization noise over $[0, fs/2]$ frequency interval [6, 7].

In order to analyze first order SD modulator, the linear system representation shown in Figure 2.9 is used.

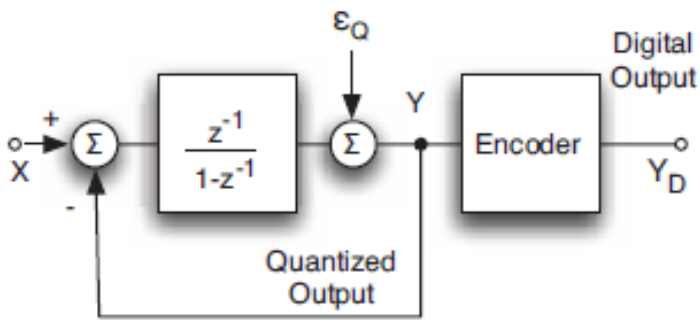

Figure 2.9. Linear Model of First Order Sigma Delta Modulator [3].

In this figure, X is the input, Y_D is the digital output, ε_Q is quantization noise and integrator is represented as $\frac{z^{-1}}{1-z^{-1}}$ in z-domain. Therefore $Y(z)$ can be expressed as

$$Y(z) = (X(z) - Y(z))\frac{z^{-1}}{1 - z^{-1}} + E(z). \tag{2.10}$$

That equation can be simplified as

$$Y(z) = z^{-1}x(z) + (1 - z^{-1})E(z). \tag{2.11}$$

The simplified version of equation indicates that input signal delayed one clock sample and noise passes through $(1 - z^{-1})$. Therefore, it is clear that signal itself and quantization noise are processed differently by the modulator. Using Equation 2.11, STF, and NTF can be found as:

$$STF(z) = z^{-1} \quad and \quad NTF(z) = 1 - z^{-1}. \tag{2.12}$$

According to Equation2.12, STF delayed the signal without any change, whereas NTF

a high-pass response to the quantization noise. Also maximum achievable SNR of first order SD modulator is given by:

$$SNR = \frac{12}{8} k^{2(\frac{3}{\pi^2})} OSR^3, \tag{2.13}$$

where k is the number of thresholds that ADC uses. Detailed analysis of the PSD, in-band noise power and SNR can be found in [3,6,7]. With reference to Equation 2.13, there is an inversely proportional ratio between noise and the third power of OSR.

Consequently, some remarks can be helpful to understand important characteristics of the SD modulators. The first remark is that the output of an integrator is limited, if its input is zero, so that the subtraction between input and output of DAC must have zero average. The second remark is that the quantization noise is zero at DC. Additionally, first order modulator reduces the global noise performance, on the other hand, thanks to the noise shaping, major part of the power generated by noise is pushed to higher frequencies. The last remark is about the linearity and noise specification of ADC and DAC. The digital signal, which is generated by the ADC, is relaxed by the feedback loop. The ADC error should be referred to the input of the integrator and then referred to the input of the modulator. The result of these two operations leads to a division of the error by the transfer function of the integrator. The error is greatly attenuated in the signal band, since the integrator has a very large gain at low frequency. However, the same benefit does not apply to the DAC due to the fact that the error of the DAC affects directly the input of the modulator together with the input signal [3, 19].

2.2.4. Second Order Sigma Delta Modulators

Although first order SD modulators have such advantages as simplicity, stability, and robustness, overall performance in terms of resolution, is inadequate for most applications. Therefore, in order to achieve higher resolution, this subsection focuses on second-order SD modulators.

In order to achieve effective number of bits (ENOB) of 13 with second order SD modulator with oversampling ratio of (OSR) 32 or 64, three different second order SD ADC are compared. The aim is to achieve $0.1pJ/conversion$ with $ENOB = 13$ and less than $40\mu W$ power consumption. The following SD ADC topologies are considered:

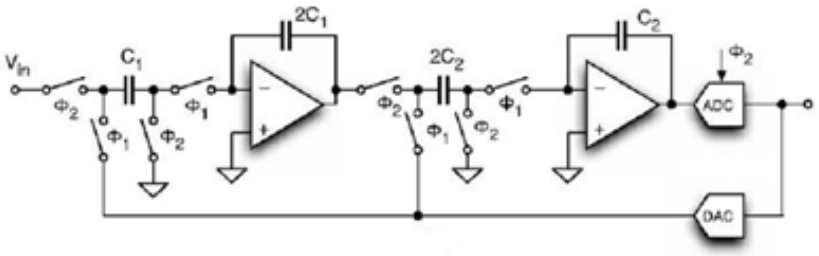

Figure 2.10. Standard Second Order Sigma Delta Modulator [8].

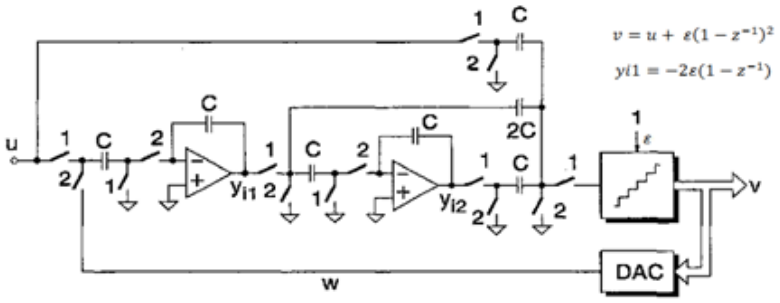

Figure 2.11. Second Order Sigma Delta Modulator [9].

In Figure 2.10, standard second order ADC topology is presented. A standard second-order SD modulator is composed of two integrators and one ADC and one DAC.

In order to analyze the system, it is needed to convert the system to linear system representation as shown in Figure 2.13.

Simulink simulations indicate that change in the integrator outputs of the second topology shown in the Figure 2.11 is less than the standard version. Also, the transfer function of feedforward topologies indicates that the change in the output of integrators is clearly smaller than the other ones. However, in terms of ENOB, there is almost no

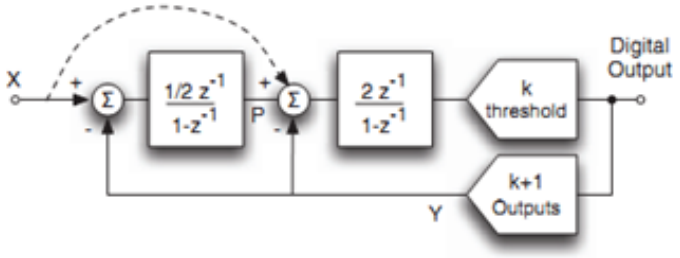

Figure 2.12. Second Order Sigma Delta Modulator [9].

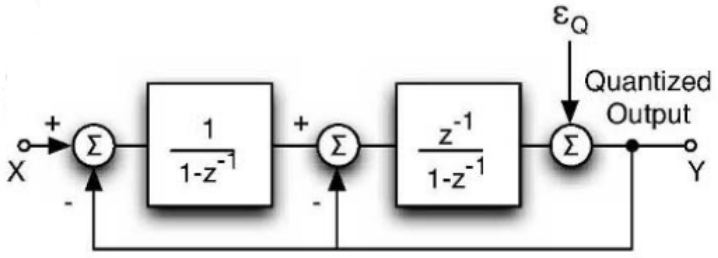

Figure 2.13. Second Order Sigma Delta Modulator [3].

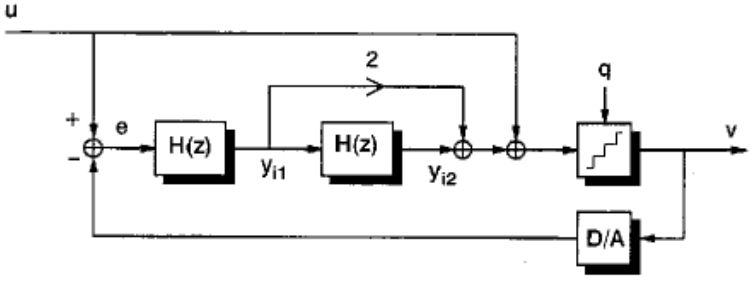

Figure 2.14. Second Order Sigma Delta Modulator [9].

difference between standard second order SD and feedforward SD architecture.

In the architecture shown in Figure 2.12, output of the first integrator is not depend on input itself but, the change in the input terminal. Since only the output of the first integrator is independent from input, this architecture is not as successful as the previous feed forward architecture. However, its performance can be sufficient for this project.

Consequently, due to the results of integrator outputs in different resolution and native success of tolerating analog mismatches, feedforward architecture is selected in this project.

3. CIRCUIT DESIGN, ANALYSIS AND RESULTS

This chapter focuses on the implementation of second order feed forward SD modulator with different operational amplifier designs to achieve low power operation goal. Briefly, those architectures will be explained in more details in next sections.

3.1. Operational Amplifiers

3.1.1. Class A Operational Amplifiers

Class A operational amplifiers (opamps) can be defined as a simple transistor biased with a static current source, which provides quiescent current. Output stage of class A amplifier simply illustrated in Figure 3.1.

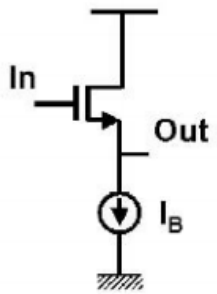

Figure 3.1. Output Stage of a Class A Operational Amplifier [10].

As shown in Figure 3.1, quiescent current is called I_B, which is used to bias the circuit. Also, the highest current that output terminal can supply is smaller than I_B in terms of magnitude. Therefore, the voltage swing at the output port is not available from rail to rail. Output voltage simply equals to $(V_{in} - V_{gs})$, where V_{in} is voltage value at the input terminal and V_{gs} is the voltage from gate to source terminal of a transistor. Moreover, defining output voltage as V_{out}, maximum current that is available at the output terminal as I_{max} and static current source as I_B and time as t, if a sinusoidal signal is applied at the input terminal of a class A operational amplifier, the voltage

swing at the output is shown at Figure 3.2.

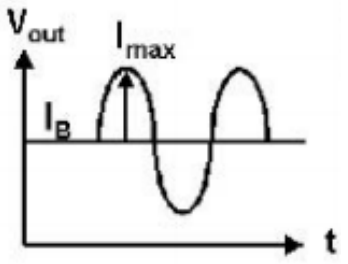

Figure 3.2. Output Voltage vs. Time Graph of a Class A Operational Amplifier [10].

Since the value of I_{max} is smaller than I_B, and in quiescent mode I_B is still present, this architecture is not a favorable choice in terms of power consumption. Also, defining efficiency as the ratio of power consumed in quiescent mode and power consumed in active mode, this topology has quite low efficiency compared to the other presented architectures.

Another classification to avoid any possible confusion, class A operational amplifiers can be defined as having a limited output current and the same current remaining fixed, even when a large differential input voltage is applied [11]. Defining I_{sat} as the maximum output current flowing into or out of the load capacitor, and ΔV_{th} as differential input voltage at which the output current saturates to its maximum value of I_{sat}, Figure 3.3 shows current characteristics of a class-A opamp.

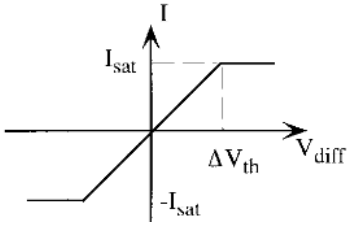

Figure 3.3. Output Current Characteristics of a Class A Operational Amplifier [11].

Consequently, class A operational amplifiers continuously consume biasing current even in quiescent mode. Therefore, the most convenient class A operational am-

plifier topology will be to use a folded cascode with a PMOS tail driven by common mode feedback circuitry. Because since defined topology is having minimum required number of branches to conceptualize differential class A operational amplifier. Detailed analysis of this topology will be given in implementation section.

3.1.2. Class AB Operational Amplifiers

Class AB operational amplifiers can be defined as a version of class B amplifiers, which do not have any crossover distortion with proper biasing that will not cause transistors to operate in cut-off region. Output stage of a class AB operational amplifier is shown in Figure 3.4.

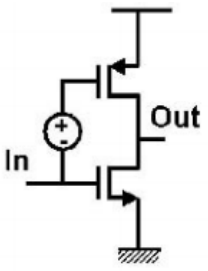

Figure 3.4. Typical Output Stage of a Class AB Operational Amplifier [10].

At the output node, class AB designs guarantee voltage swing from rail to rail (highest potential to lowest potential) at least for capacitive loads. For low resistive loads stability is an important issue to solve [10]. Defining output node as V_{out}, the possible maximum current that can drain in output node as I_{max}, static current source as I_B and time as t, if a sinusoidal signal applied to input terminal, the following current output is presented in Figure 3.5.

In Figure 3.5, I_b static current value is smaller than I_{max} in terms of magnitude and the bigger input signal leads to the larger current drained at the output terminal. In the last years, class AB stages which do not suffer from SR limitation, have demonstrated an efficient performance in terms of power dissipation and speed [20–23].

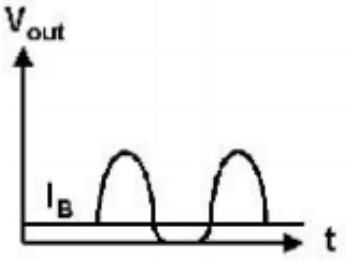

Figure 3.5. Output Voltage Swing of a Class AB Operational Amplifier [10].

Another classification of class AB operational amplifiers can be done by defining a class AB operational amplifier as having an output current, which is not limited (saturated), when a differential large input voltage is applied [11].

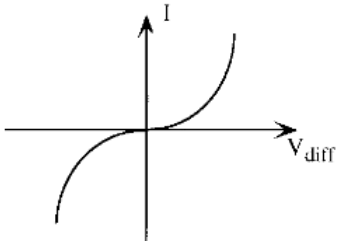

Figure 3.6. Output Current Characteristics of a Class AB Operational Amplifier [11].

3.1.3. Adaptive Biasing Operational Amplifiers

An adaptively biased operational amplifier simply adapts biasing circuitry in order to provide larger output currents depending on the input signal provided [10]. In order to achieve maximum current, biasing current should increase with increasing input values by adapting biasing current to input signal level. Two branches of a differential pair are compared, as a result of that comparison if any difference is present in one of the branches, operational amplifier notices that there is an input signal is applied and therefore biasing current is increased. Also changing ratio of the current mirrors the amount of increase can be adjusted. The increase rate of output current depends on current factor A, which can be seen in Figure 3.7.

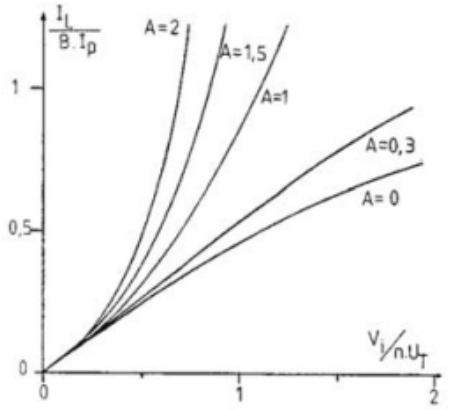

Figure 3.7. Output Current Behavior with Changing Current Factor A [10].

A current factor A, equals to zero, leads to no adaptive biasing to take place. In that case, output current is limited for larger input voltage. However, for an increasing current factor A, the expansion of the output current with input voltage is more and more pronounced, which is similar to a class AB behavior. Also, the factor A cannot be increased more than 10 due to matching issues but, if cascodes are used, the matching between all current sources improves remarkably and higher values of A can be achieved [10].

3.2. Implementation of Circuits

This section focuses on circuit implementations of different operational amplifiers, which are designed for achieving low power feedforward SD modulator design, which are mentioned in previous sections. Different operational amplifier topologies are designed to achieve low power goal.

3.2.1. Class AB/AB Very Low Power Operational Amplifier

The original operational amplifier aimed to build a SD modulator for biomedical applications [12]. In order to achieve a speed limit, slew rate (SR) becomes a notable issue. Since SR becomes a dominant parameter, in class A amplifiers SR imposes a

minimum bias current that leads to consume more power. Therefore, class AB stages which do not suffer from SR limitation can demonstrate such a good performance in terms of speed and power dissipation. In Figure 3.8 topology of class AB/AB circuit is shown:

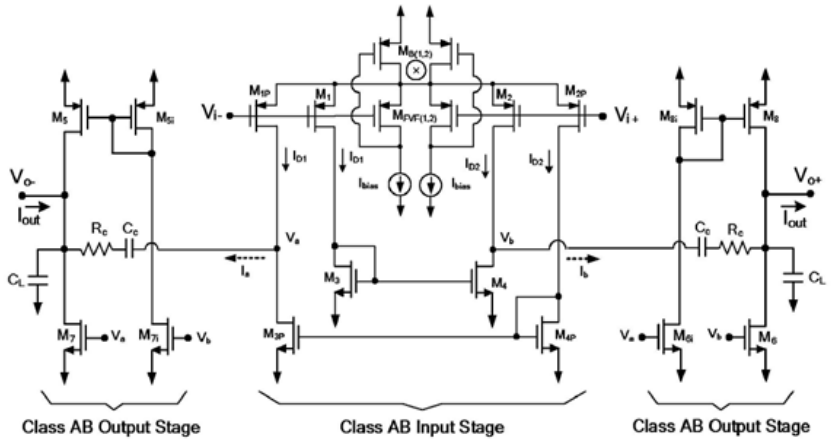

Figure 3.8. Figure of Class AB/AB Amplifier [12].

In this operational amplifier design, a new approach is used which is designing entire amplifier with adopting class AB stages. Therefore, the new topology is denoted as class AB/AB and this topology ensures not only a large SR, but also low static current consumption. Furthermore, biasing of all transistors is done in weak inversion region, which provides convenient low voltage, low frequency and low power solutions. Also for the second stage there is no need to have an extra quiescent current circuitry. The reason of having two stages can be shown as having low supply voltage resulted in reduced dynamic range and therefore use of cascode stage for higher gain will be unpractical. Furthermore, two stage opamps can maintain rail to rail output stage and can drive capacitive and resistive loads.

Due to the slew rate requirement of design which is $20V/\mu sec$ and having load capacitor $C_L = 150fF$ output current is calculated as $I_{out} = 3\mu A$ During the calculations overdrive voltage of transistors are chosen as $V_{ov} = 0.2V$. Also having load capacitance equals to $C_L = 150fF$ results in $GBW = 1.34MHz$ Needed gain of opamp is found as $45dB$ according to Simulink simulations and UMC $0.18\mu m$ technology has Early volt-

age as $V_A = 5V$ length of transistors to achieve needed output resistance $r_o = 140k\Omega$ is found as $L = 0.084\mu m$. Therefore minimum value of L available is chosen. The following schematic is designed with common mode feedback as shown in Figure 3.9. Common mode feedback circuit simply has one fourth of the tail current of input stage

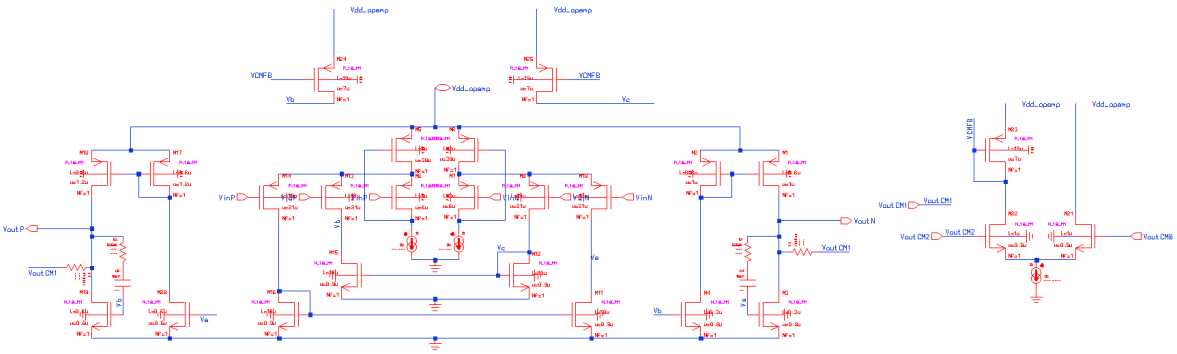

Figure 3.9. Schematic of Class AB/AB Opamp with Common Mode Feedback.

of the opamp. According to the average value of positive and negative outputs of the opamp, the circuit tunes both output nodes to given common mode voltage from ideal DC source by injecting current to the input stage of operational amplifier.

Testbench of the operational amplifier is in Figure 3.10. In this testbench resistor values are set to $10k\Omega$ and in between output terminals of opamp to resistors voltage controlled voltage sources with gain of 1 are used to neglect possible driving strength problems with suggestion of Prof. Devrim Yılmaz Aksın. Also in AC simulations, in order to set DC values of the operational amplifier below another voltage controlled voltage sources with gain of 1 are used to tune the same DC values with previous operational amplifiers.

Transient simulation result of the circuit can be seen in Figure 3.11.

AC simulation result of the circuit can be seen in Figure 3.12.

SR simulation result of the circuit for $10mV$ peak to peak input voltage can be seen in Figure 3.13.

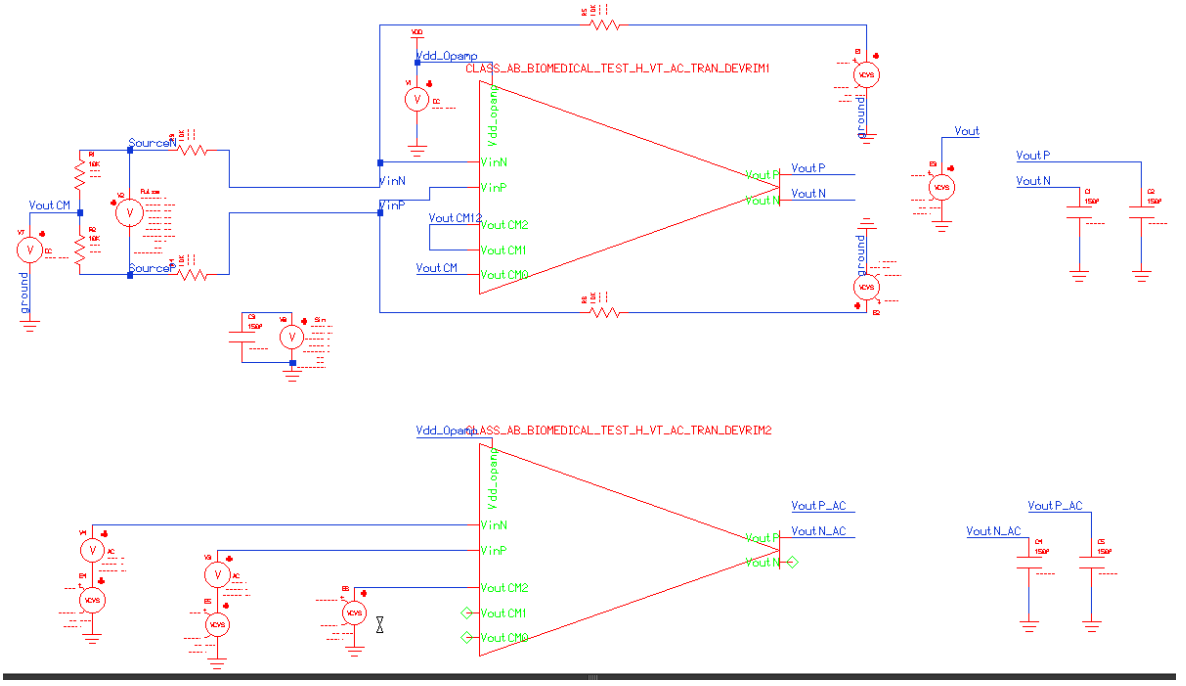

Figure 3.10. Testbench of Class AB/AB Opamp.

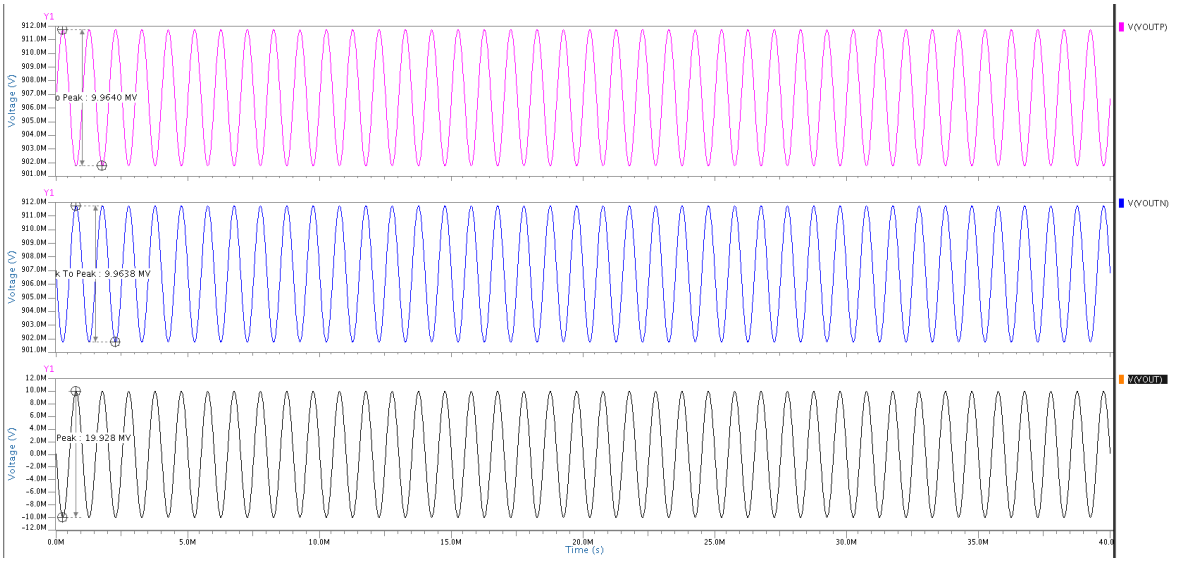

Figure 3.11. Transient Simulation Result of Class AB/AB Opamp.

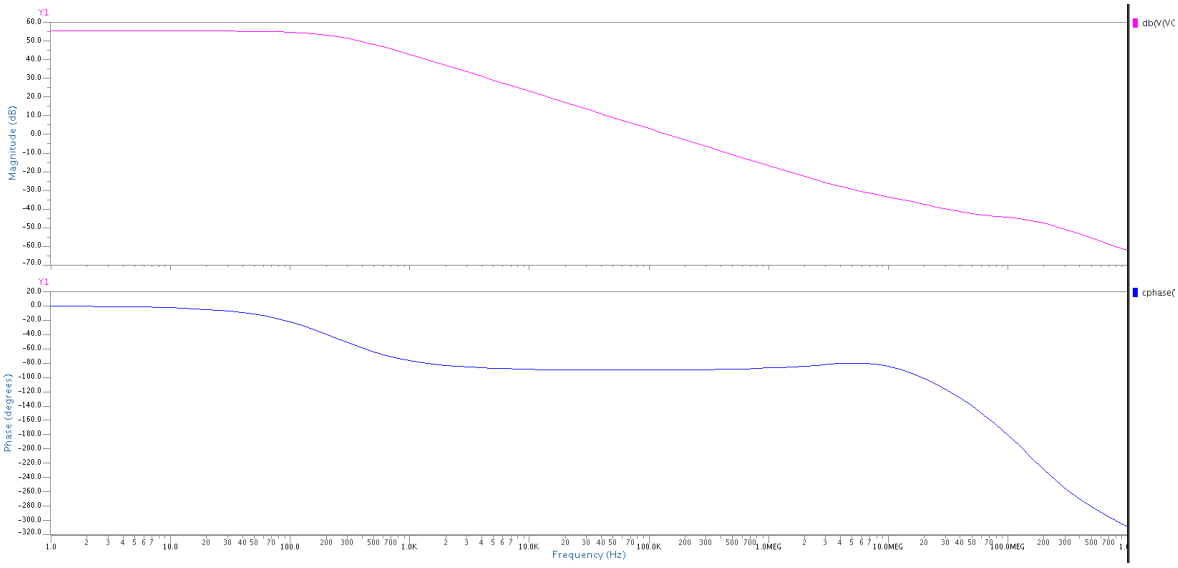

Figure 3.12. AC Simulation Result of Class AB/AB Opamp.

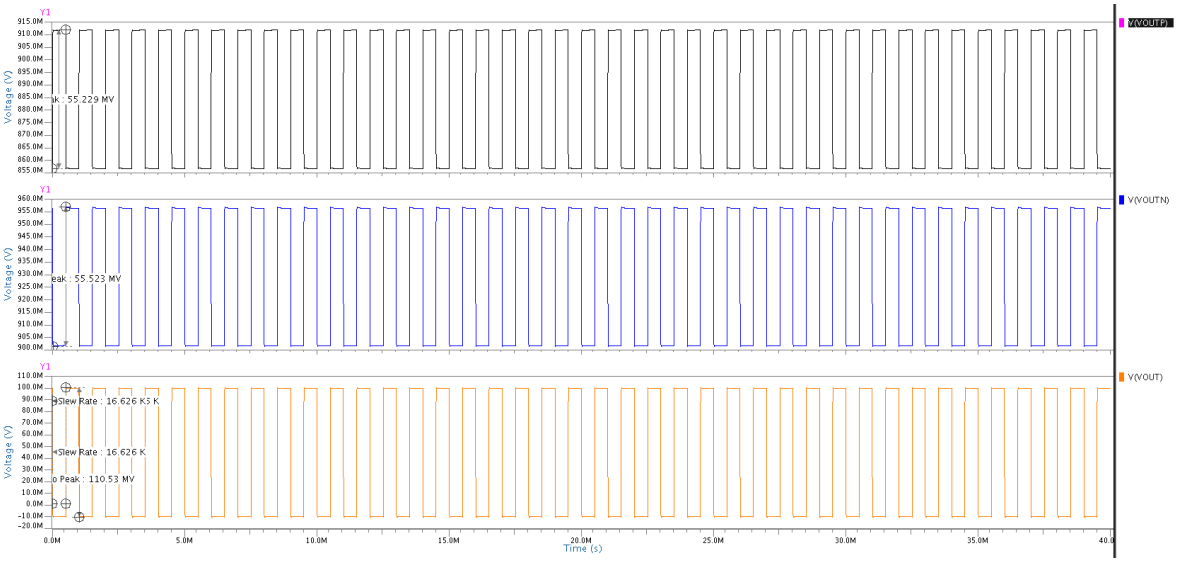

Figure 3.13. SR Simulation Result of Class AB/AB Opamp for $10mV$ peak to peak Input voltage.

SR simulation result of the circuit for $1V$ peak to peak input voltage can be seen in Figure 3.14.

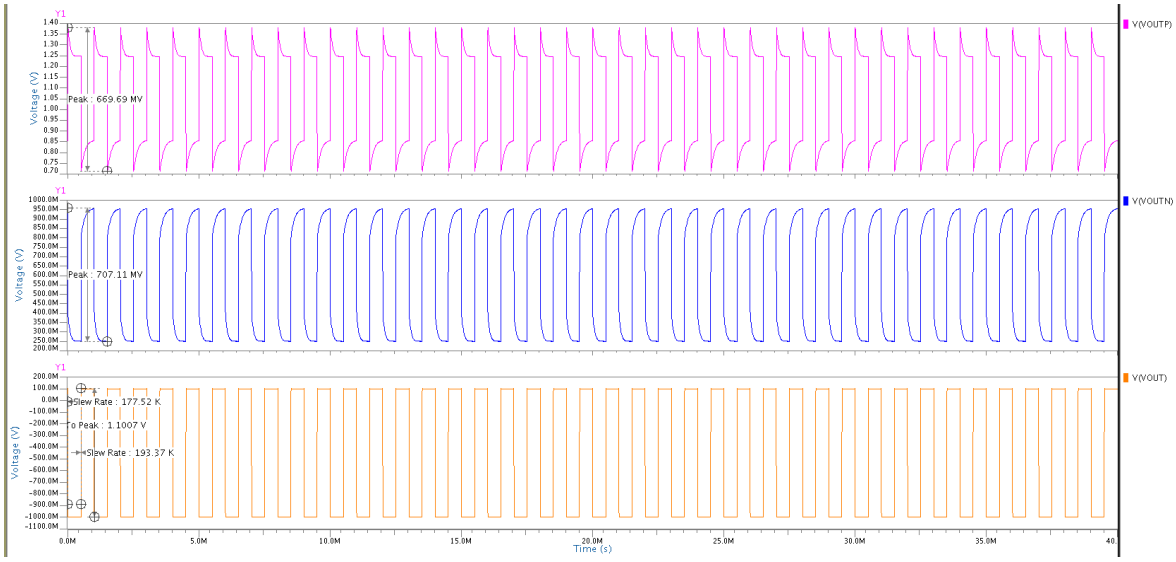

Figure 3.14. SR Simulation Result of Class AB/AB Opamp for $1V$ peak to peak Input voltage.

Table 3.1. Simulation Results of Class AB/AB Operational Amplifiers.

	GBW	A_V	SR $(+-)$	SR $(-+)$	Power	I
ABAB Bio	$143.5M$	$55.2dB$	$16.6k$	$16.6k$	$44.92\mu W$	$24.96\mu A$

3.2.2. Class AB Operational Amplifier (without RC Compensation)

In order to decrease power consumption of class AB/AB amplifier [12], which have been explained in details in previous subsection, resistances and capacitors (R_c and C_c) are simply removed. In that case, overall circuit will not be compensated as much as previous version, however, power consumed in compensation RC pair will be abolished. Figure 3.15 shows class AB/AB operational amplifier without RC compensation.

Due to the slew rate requirement of design which is $20V/\mu sec$ and having load capacitor $C_L = 150fF$ output current is calculated as $I_{out} = 3\mu A$ During the calculations

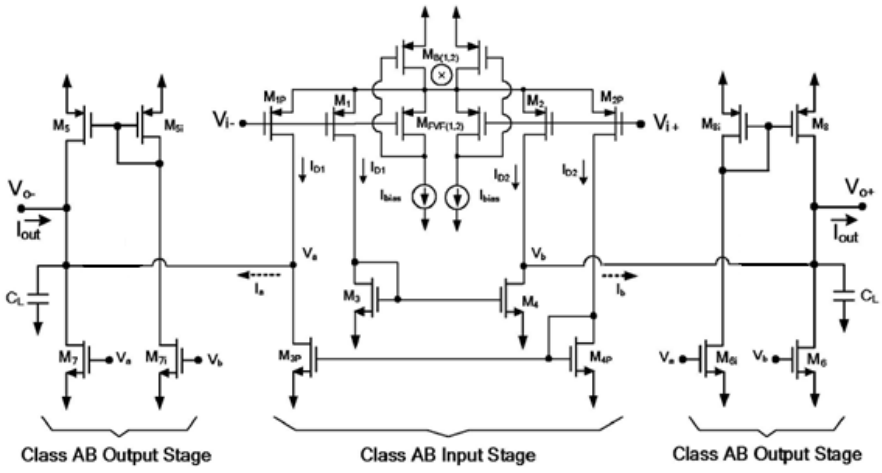

Figure 3.15. Figure of Class AB/AB Amplifier without RC Compensation [12].

overdrive voltage of transistors are chosen as $V_{ov} = 0.2V$. Also having load capacitance equals to $C_L = 150fF$ results in $GBW = 1.34MHz$ Needed gain of opamp is found as $45dB$ according to Simulink simulations and UMC $0.18\mu m$ technology has Early voltage as $V_A = 5V$ length of transistors to achieve needed output resistance $r_o = 140k\Omega$ is found as $L = 0.084\mu m$. Therefore minimum value of L available is chosen.

The following schematic is designed with common mode feedback as shown in Figure 3.16. Common mode feedback circuit simply has one fourth of the tail current

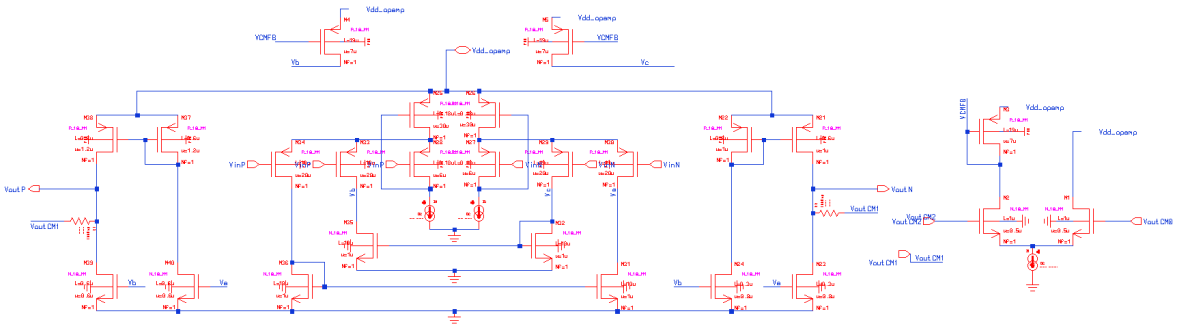

Figure 3.16. Schematic of Class AB/AB Opamp with Common Mode Feedback without RC Compensation.

of input stage of the opamp. According to the average value of positive and negative

outputs of the opamp, the circuit tunes both output nodes to given common mode voltage from ideal DC source by injecting current to the input stage of operational amplifier.

Testbench of the operational amplifier is in Figure 3.17. In this testbench resistor

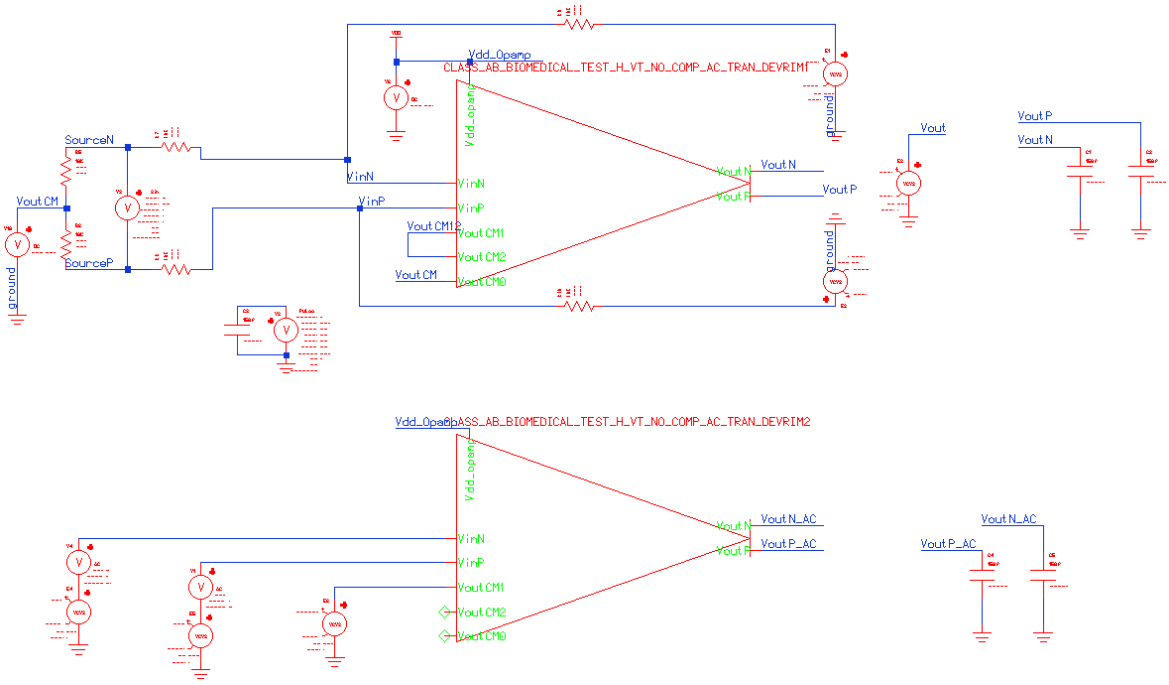

Figure 3.17. Testbench of Class AB/AB Opamp without RC Compensation.

values are set to $10k\Omega$ and in between output terminals of opamp to resistors voltage controlled voltage sources with gain of 1 are used to neglect possible driving strength problems with suggestion of Prof. Devrim Yılmaz Aksın. Also in AC simulations, in order to set DC values of the operational amplifier below another voltage controlled voltage sources with gain of 1 are used to tune the same DC values with previous operational amplifiers.

Transient simulation result of the circuit can be seen in Figure 3.18.

AC simulation result of the circuit can be seen in Figure 3.19.

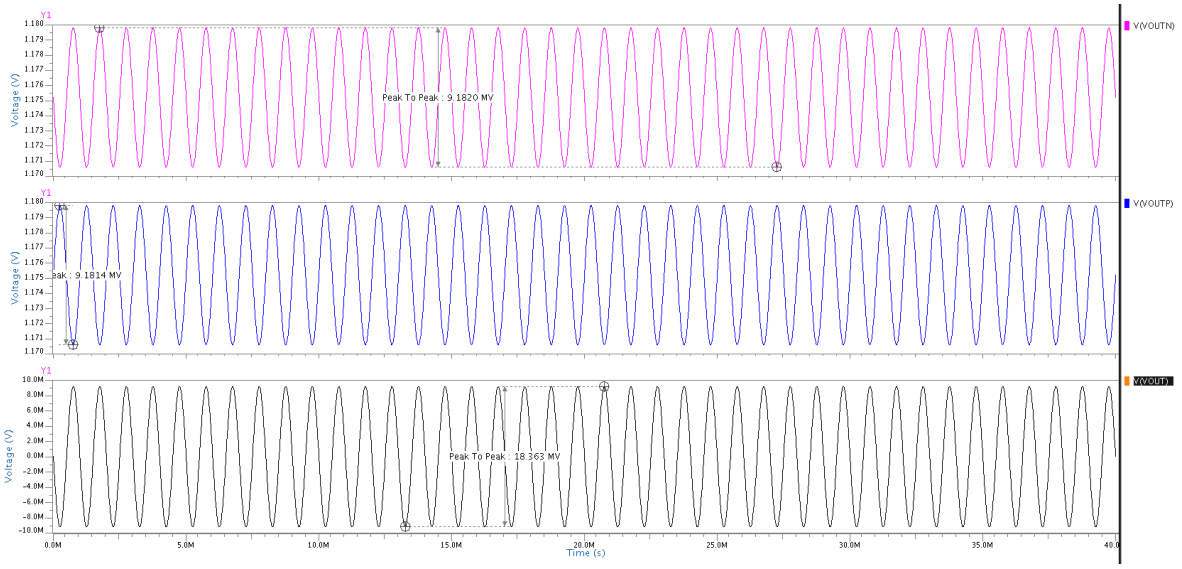

Figure 3.18. Transient Simulation Result of Class AB/AB Opamp without RC Compensation.

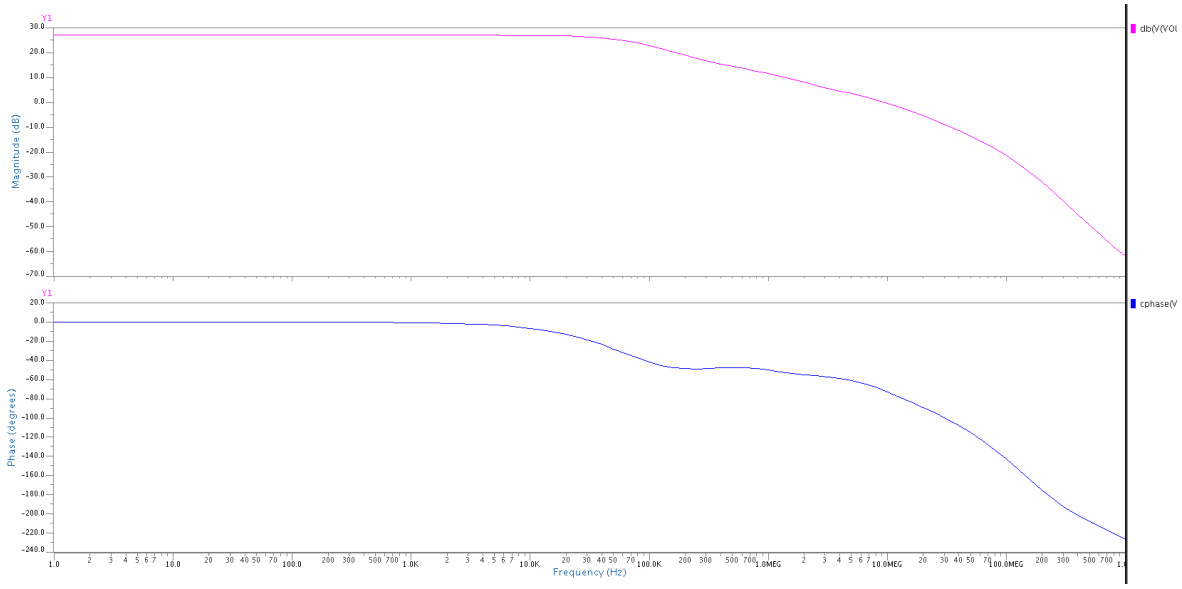

Figure 3.19. AC Simulation Result of Class AB/AB Opamp without RC Compensation.

SR simulation result of the circuit for $10mV$ peak to peak input voltage can be seen in Figure 3.20.

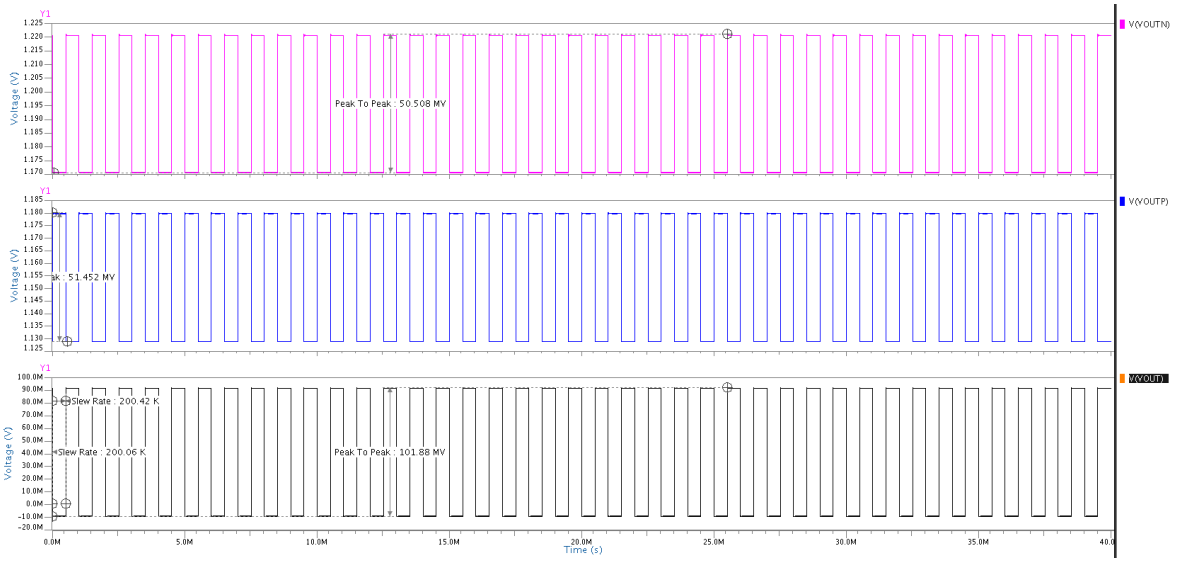

Figure 3.20. SR Simulation Result of Class AB/AB Opamp without RC Compensation for $10mV$ peak to peak Input voltage.

In the testing process, it is advised to measure SR in a repeated manner meaning that the testing was repeated several times to increase the accuracy of the measurements. In order to test the SR of the overall circuit more precisely, another square wave with different peak to peak input voltage values has been applied and different SR values are gathered.

SR simulation result of the circuit for $1V$ peak to peak input voltage can be seen in Figure 3.21.

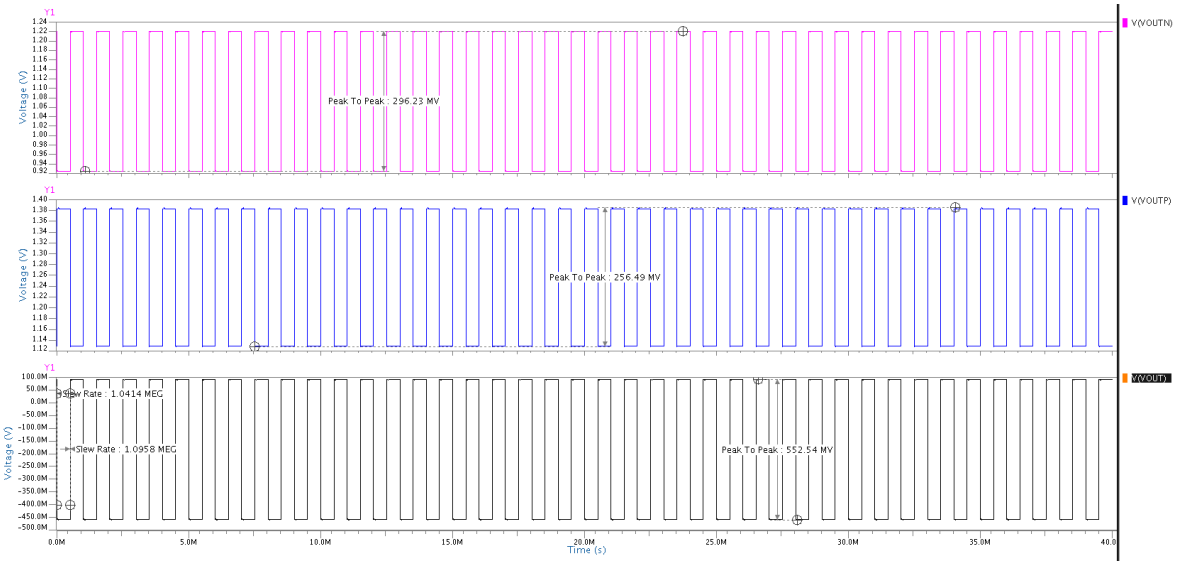

Figure 3.21. SR Simulation Result of Class AB/AB Opamp without RC Compensation for $1V$ peak to peak Input voltage.

After simulations, the following results, listed in Table 3.2, are obtained.

Table 3.2. Simulation Results of Class AB/AB Operational Amplifiers with no Compensation.

	GBW	A_V	SR (+−)	SR (−+)	Power	I
ABAB UC	$11.1M$	$27dB$	$200.4k$	$200.6k$	$27.14\mu W$	$15.08\mu A$

3.2.3. Class AB Operational Amplifier

This amplifier is only class AB input stage of the class AB/AB amplifier shown in Figure 3.8. Since number of branches through class AB/AB topology results in high power consumption and also the gain achieved with whole circuitry is beyond the design goals, only the input part is used as shown Figure 3.22.

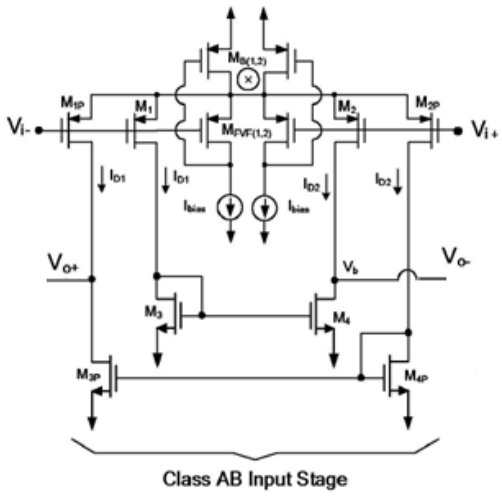

Figure 3.22. Figure of Class AB Amplifier [12].

Due to the slew rate requirement of design which is $20V/\mu sec$ and having load capacitor $C_L = 150fF$ output current is calculated as $I_{out} = 3\mu A$ During the calculations overdrive voltage of transistors are chosen as $V_{ov} = 0.2V$. Also having load capacitance equals to $C_L = 150fF$ results in $GBW = 11.5MHz$ Needed gain of opamp is found as $45dB$ according to Simulink simulations and UMC $0.18\mu m$ technology has Early voltage as $V_A = 5V$ length of transistors to achieve needed output resistance $r_o = 32.6M\Omega$ is found as $L = 19.56\mu m$. Therefore found value of L, W of the transistor can be find by using current equation using technology depended values as $K_N = 97.98\mu$, $K_P = 21.53\mu$ threshold voltages as $V_{Tp} = -535.78mV$ and $V_{Tn} = 335.47mV$. The ratio of NMOS transistors $W/L = 1.53$ and PMOS transistors $W/L = 6.96$ The following circuit with common mode feedback is generated shown in Figure 3.23. Common mode feedback circuit simply has one fourth of the tail current of input stage of the opamp. According to the average value of positive and negative outputs of the opamp,

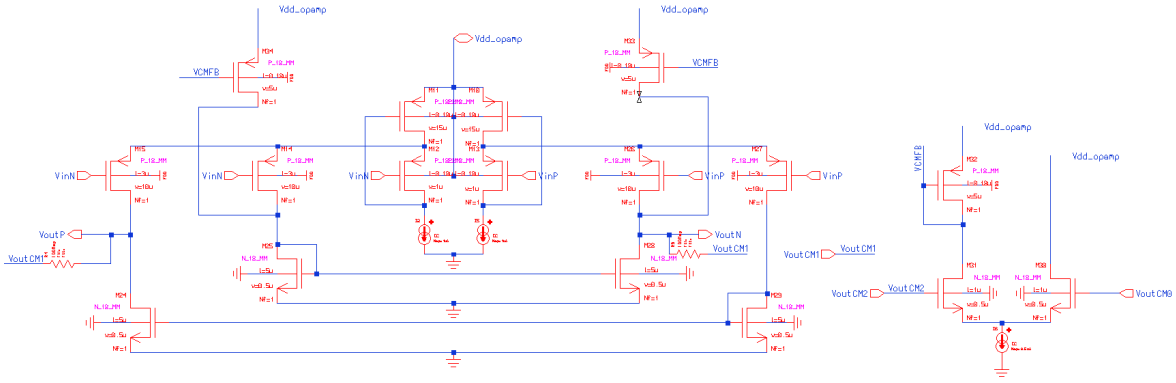

Figure 3.23. Class AB Opamp with Common Mode Feedback.

the circuit tunes both output nodes to given common mode voltage from ideal DC source by injecting current to the input stage of operational amplifier.

The test circuit is shown in Figure 3.24.

In this testbench resistor values are set to $10k\Omega$ and in between output terminals of opamp to resistors voltage controlled voltage sources with gain of 1 are used to neglect possible driving strength problems with suggestion of Prof. Devrim Yılmaz Aksın. Also in AC simulations, in order to set DC values of the operational amplifier below another voltage controlled voltage sources with gain of 1 are used to tune the same DC values with previous operational amplifiers.

Transient simulation result of the circuit is shown in Figure 3.25.

AC simulation result can be seen in Figure 3.26.

Slew Rate results of the circuit for $10mV$ peak to peak input voltage can be seen in Figure 3.27.

Slew Rate results of the circuit for $1V$ peak to peak input voltage can be seen in Figure 3.28.

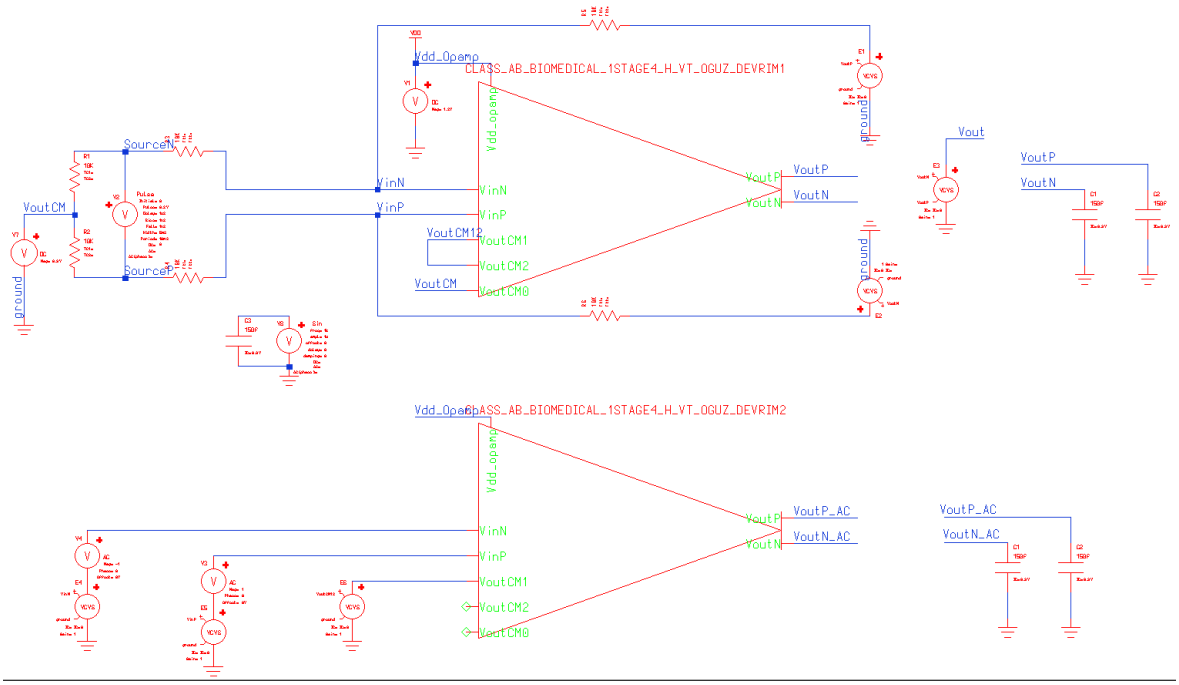

Figure 3.24. Testbench of Class AB Opamp with Common Mode Feedback.

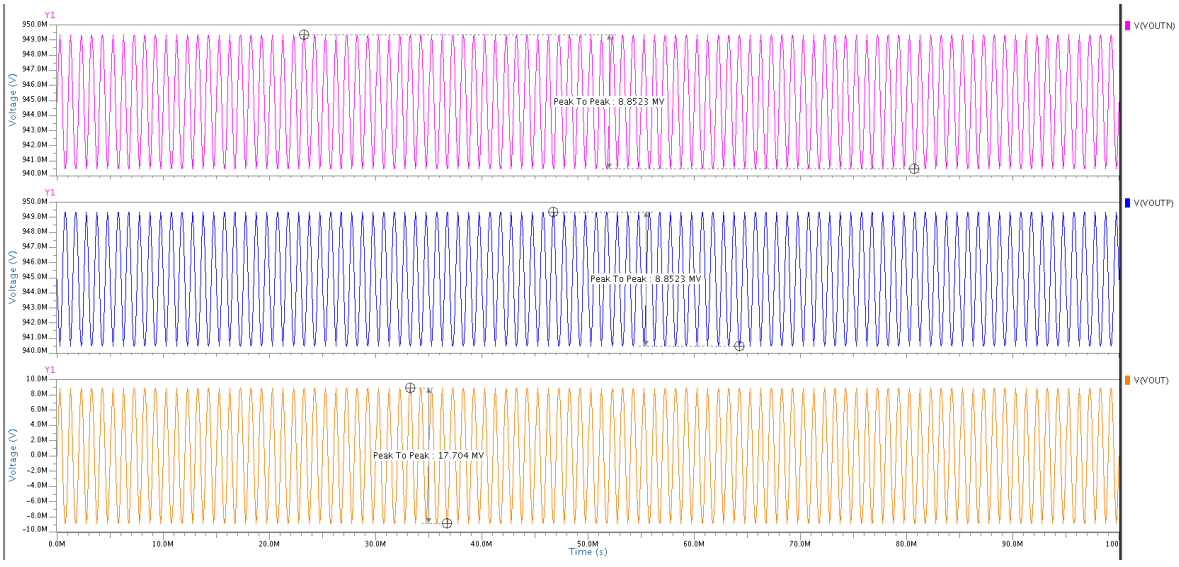

Figure 3.25. Transient Simulation Result of Class AB Opamp with Common Mode Feedback.

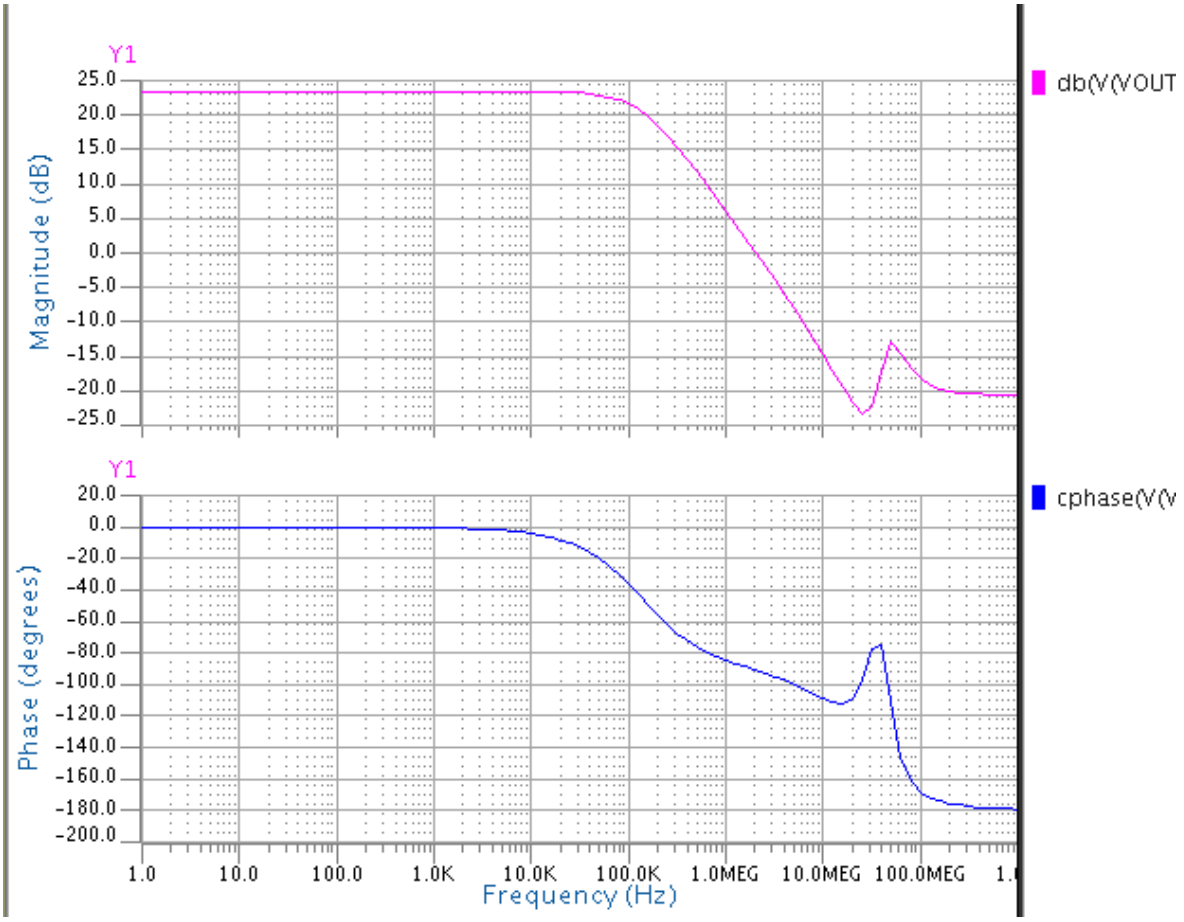

Figure 3.26. AC Simulation Result of Class AB Opamp.

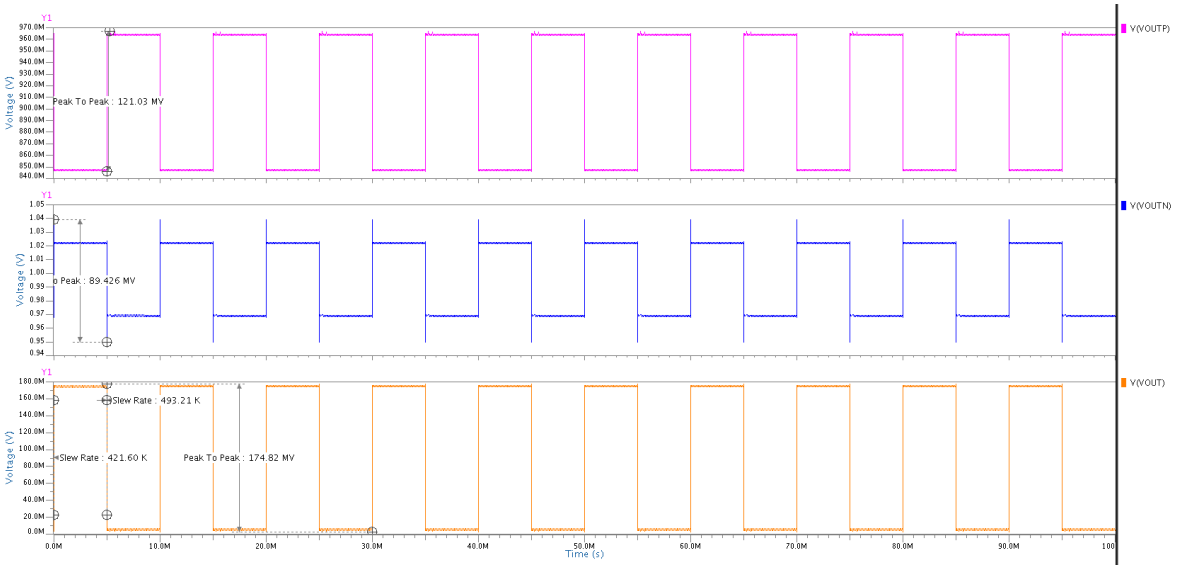

Figure 3.27. SR Result of Class AB Opamp for $10mV$ peak to peak input voltage.

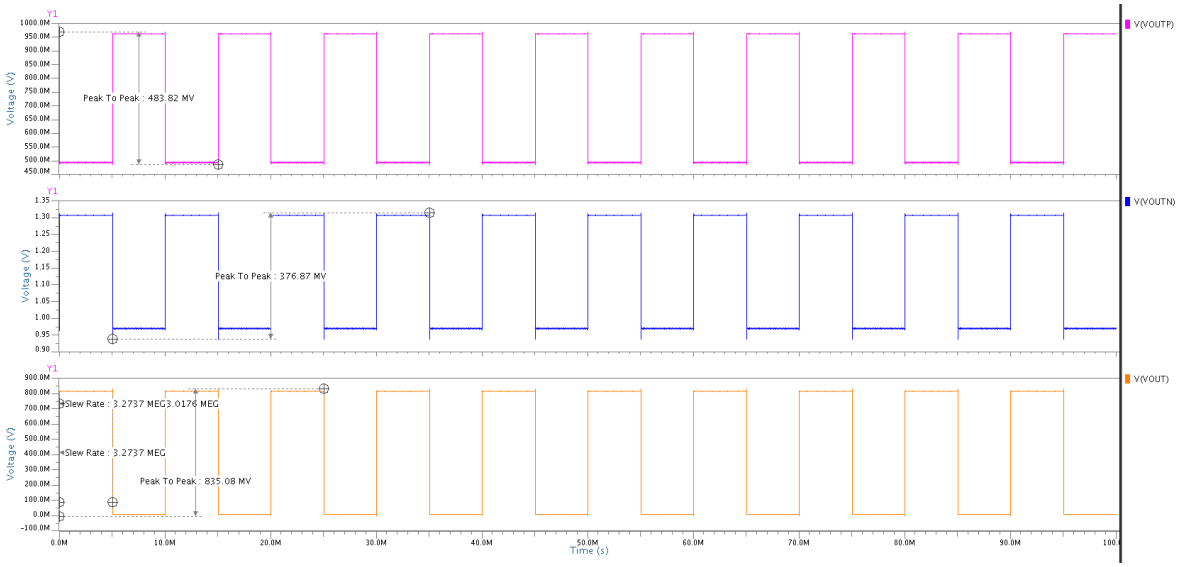

Figure 3.28. SR Result of Class AB Opamp for $1V$ peak to peak input voltage.

After simulations, a significant drop in total power consumption is observed.

Table 3.3. Simulation Results of Class AB Operational Amplifiers.

	GBW	A_V	SR $(+-)$	SR $(-+)$	Power	I
AB Bio	$2.1M$	$24dB$	$493.2k$	$421.6k$	$65.9\mu W$	$36.63\mu A$

3.2.4. Class AB Operational Amplifier with Cascode

This class AB operational amplifier consist of an input stage of a cross-coupled quad and a cascode pair is present at the second stage in order to increase gain. Schematic of the operational amplifier is in Figure 3.29.

While tuning the circuity B_1 value is chosen as 2.8 and B_2 value is chosen as 0.4 The topology is mostly used by having an input differential pair. In that case output current and also SR of the topology is quite limited. However, substitution of the input differential pair by a cross-coupled quad gives an expanding current characteristics. The GBW of the both topologies are the same, but with the cross-coupled quad the SR increases drastically [10].

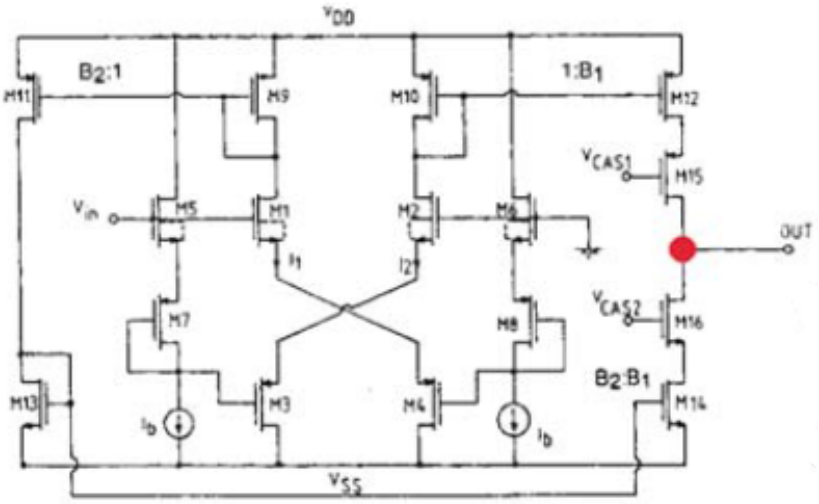

Figure 3.29. Class AB Operational Amplifier [13].

Due to the slew rate requirement of design which is $20V/\mu sec$ and having load capacitor $C_L = 150fF$ output current is calculated as $I_{out} = 3\mu A$ During the calculations overdrive voltage of transistors are chosen as $V_{ov} = 0.2V$. Also having load capacitance equals to $C_L = 150fF$ results in $GBW = 57.1MHz$ Needed gain of opamp is found as $45dB$ according to Simulink simulations and UMC $0.18\mu m$ technology has Early voltage as $V_A = 5V$ length of transistors to achieve needed output resistance $r_o = 296k\Omega$ is found as $L = 0.11\mu m$. Therefore found value of L, W of the transistor can be find by using current equation using technology depended values as $K_N = 97.98\mu$, $K_P = 21.53\mu$ threshold voltages as $V_{Tp} = -535.78mV$ and $V_{Tn} = 335.47mV$.

The following schematic is designed with common mode feedback as shown in Figure 3.30.

Testbench of the operational amplifier is in Figure 3.31. In this testbench resistor values are set to $10k\Omega$ and in between output terminals of opamp to resistors voltage controlled voltage sources with gain of 1 are used to neglect possible driving strength problems with suggestion of Prof. Devrim Yılmaz Aksın. Also in AC simulations, in order to set DC values of the operational amplifier below another voltage controlled voltage sources with gain of 1 are used to tune the same DC values with previous

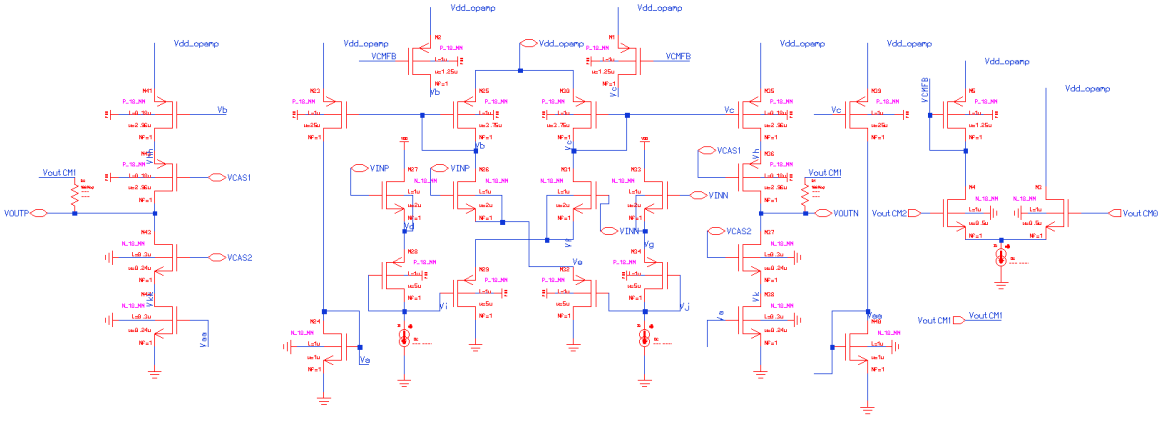

Figure 3.30. Schematic of Class AB Opamp with Cascode Stage and Common Mode Feedback.

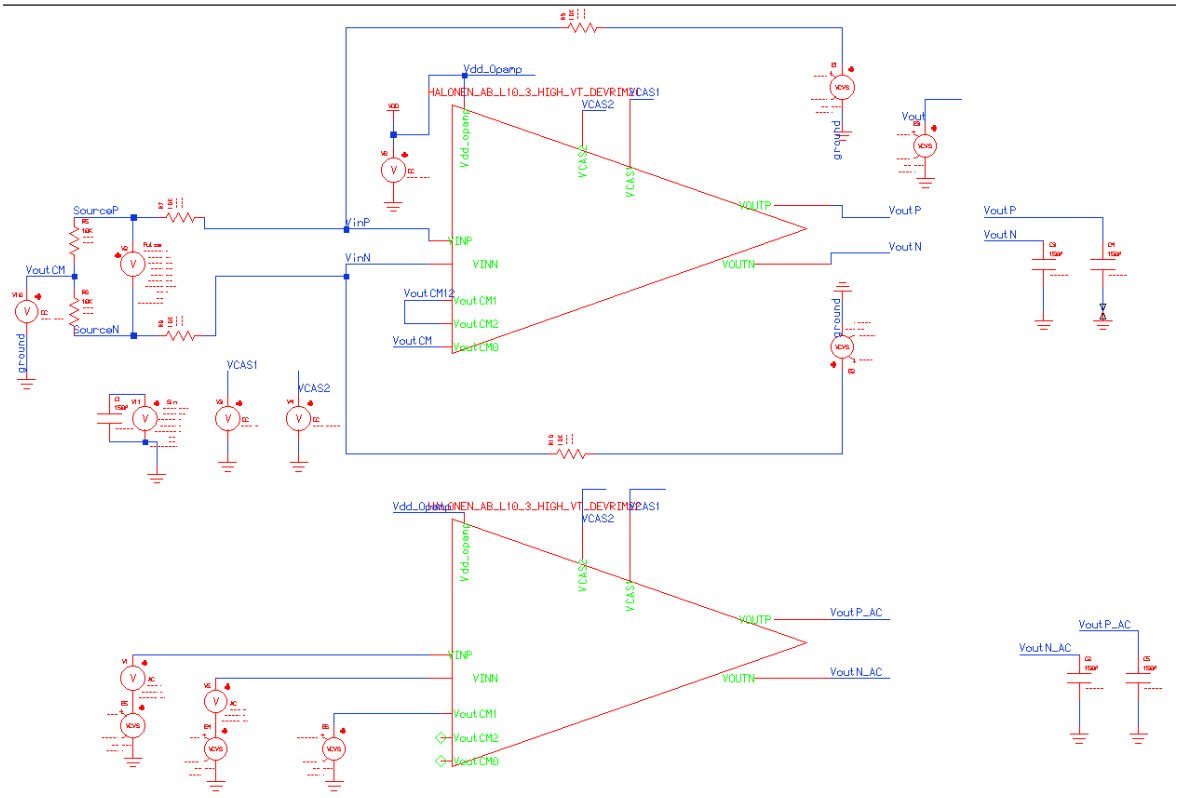

Figure 3.31. Testbench of Class AB Opamp with Cascode Stage.

operational amplifiers.

Transient simulation result of the circuit can be seen in Figure 3.32.

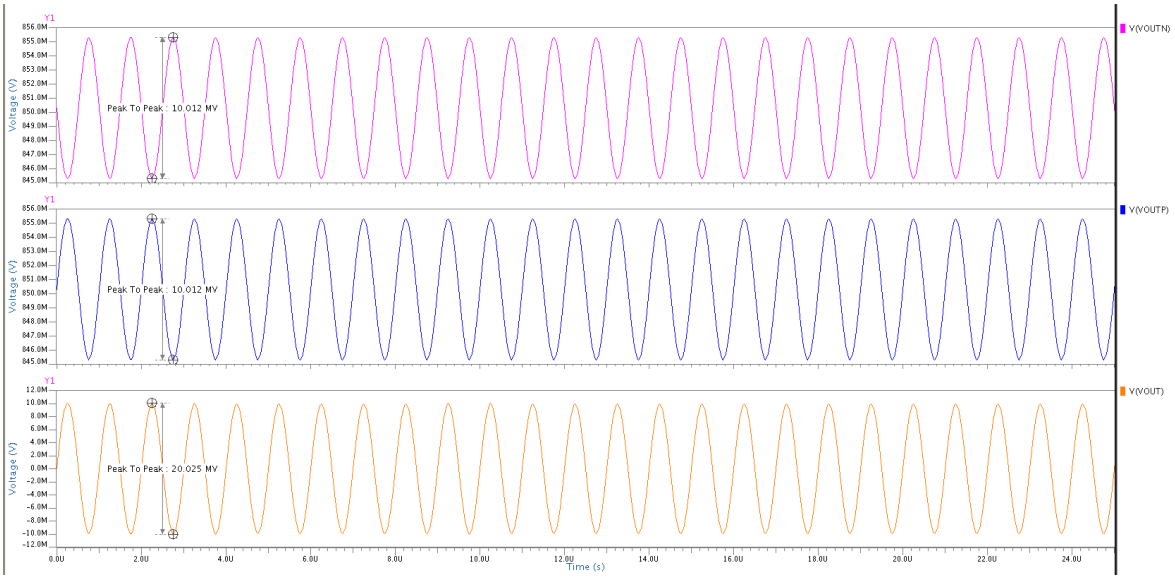

Figure 3.32. Transient Simulation Result of Class AB Opamp with Cascode Stage.

AC simulation result of the circuit can be seen in Figure 3.33.

SR simulation result of the circuit for $10mV$ peak to peak input voltage can be seen in Figure 3.34.

SR simulation result of the circuit for $1V$ peak to peak input voltage can be seen in Figure 3.35.

Table 3.4. Simulation Results of Class AB Operational Amplifiers with Cascode Stage.

	GBW	A_V	SR (+−)	SR (−+)	Power	I
AB Cascode	$30M$	$63dB$	$1.04M$	1.04	$51.48\mu W$	$28.6\mu A$

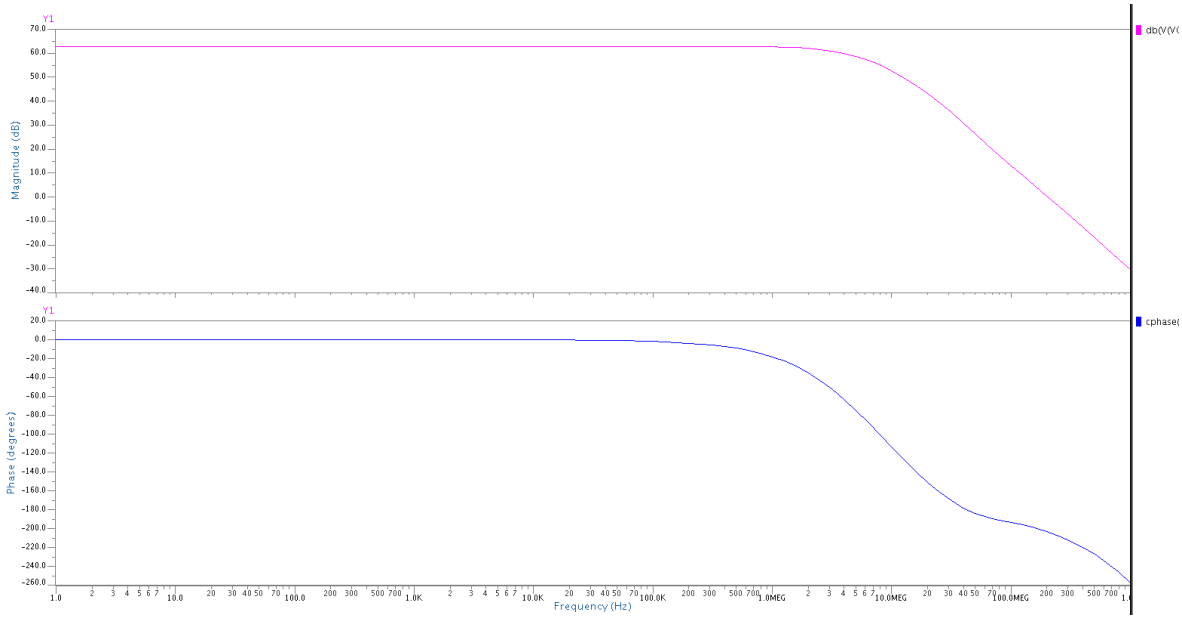

Figure 3.33. AC Simulation Result of Class AB Opamp with Cascode Stage.

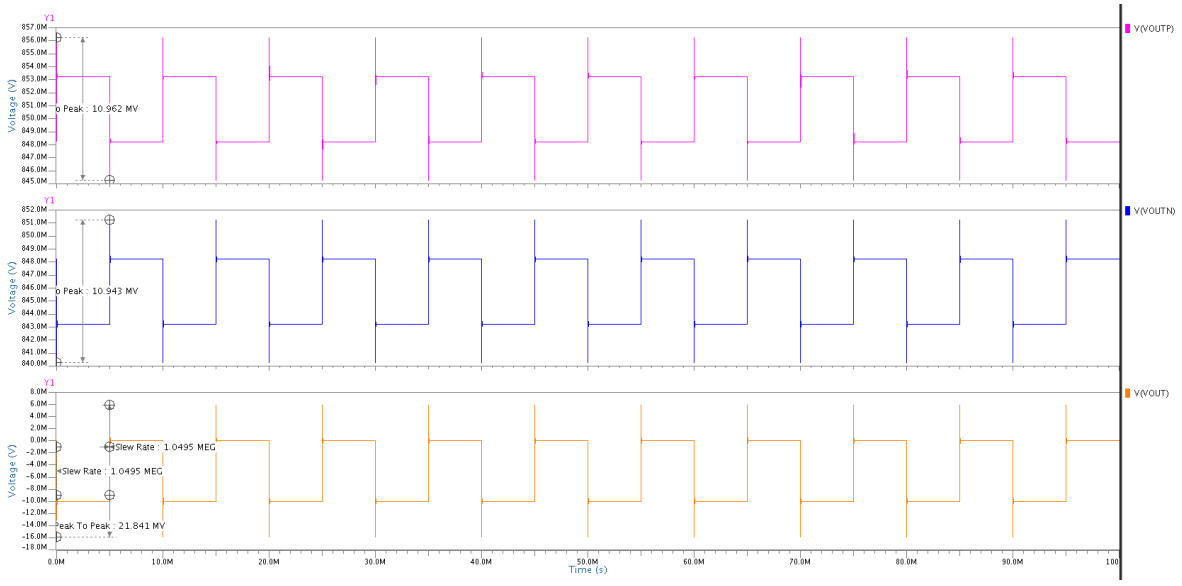

Figure 3.34. SR Simulation Result of Class AB Opamp with Cascode Stage for $10mV$ peak to peak Input voltage.

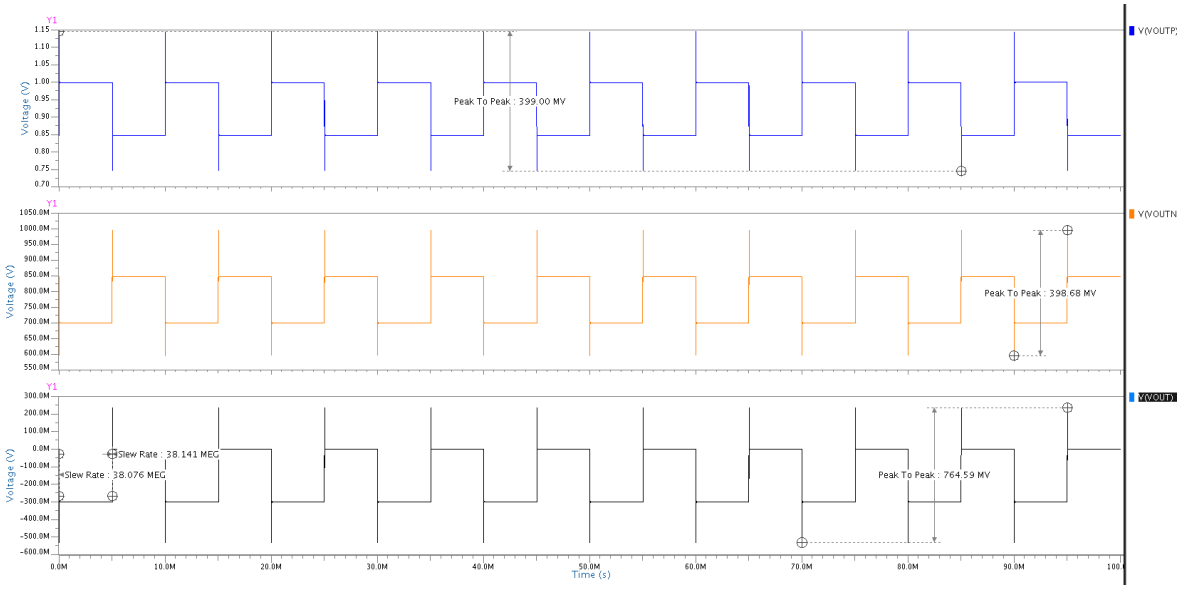

Figure 3.35. SR Simulation Result of Class AB Opamp with Cascode Stage for $1V$ peak to peak Input voltage.

3.2.5. Inverter used as a Class AB Operational Amplifier

Whereas in the past years high-performance circuits were of main interst, a new trend towards extremely low power and ultra-low voltage circuit techniques is emerging [14]. An inevitable part of differential operational amplifiers is to have an input pair as Figure 3.36.

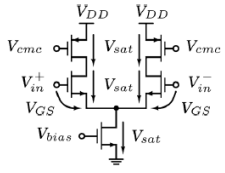

Figure 3.36. Voltage Drops in Differential Input Pairs [14].

There is no doubt that voltage swing of the circuit can be increased by removing tail current source as Figure 3.37.

Therefore remaining part of the operational amplifier is similar to a single CMOS

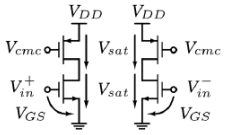

Figure 3.37. Voltage Drops in Differential Input Pairs without Tail Current Source [14].

inverter shown in Figure 3.38 can be used as the simplest class AB operational amplifier by connecting input terminal to a signal source.

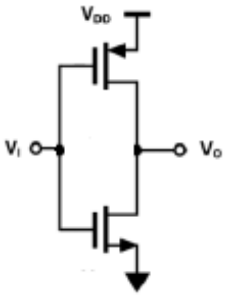

Figure 3.38. CMOS Inverter.

In such switched capacitor circuits as integrator, the open loop DC gain of and amplifier directly determines the accuracy of charge transfer, while the gain-bandwidth product (GBP) of an amplifier determines operation speed of the amplifier [15]. Figure 3.39 illustrates the relation of DC gain, supply voltage and gain-bandwidth.

As shown in Figure 3.39, DC gain and GB of an inverter with respect to supply voltage (V_{dd}). The DC gain of inverter is maximized in the weak inversion region, whereas the GB of an inverter increases with respect to supply voltage and is saturated when the operating region enters strong inversion operation mode. Therefore, in order to obtain both high DC gain and wide GB, inverter should operate at the boundary between the weak inversion and strong inversion modes, which can be realized as having supply voltage (V_{dd}) as equal to nominal summation of the NMOS transistor's threshold V_{tn} and PMOS transistor's threshold. According to supply voltage, push-pull inverters

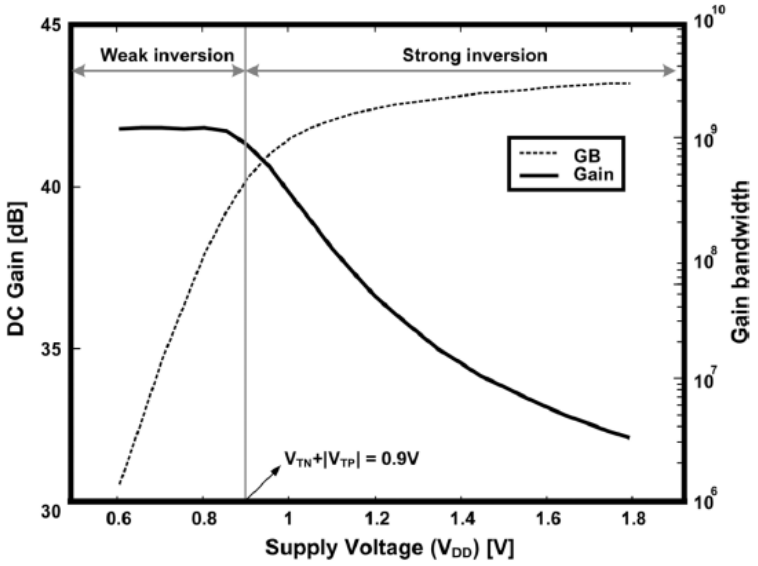

Figure 3.39. Characteristics of an Inverter: DC Gain and GB vs. Supply Voltage [15].

can be classified as class AB or class C [15]. When $V_{tn} + |V_{tp}| < V_{dd}$, the inverter behaves as class AB, and if $V_{dd} \leq V_{tn} + |V_{tp}|$ inverter behaves as a class C amplifier.

With reference to [24], analog circuits will operate in such supply voltages as close to V_{th} in order to achieve low power consumption goal. However, in such low voltage supply, the loss in performance due to non-idealities of analog building blocks is inevitable. Apart from that fact, writer mentions that in SD modulators having a V_{dd} close to V_{th} may force transistors to work in weak inversion, thereby inducing poor accuracy, low operation speed and also limited output swing that will degrade performance of SD modulators [24]. However, use of feedforward topology with reduced sensitivity to integrator nonlinearities may result in fairly enough performance. Therefore, compared to feedback topology, quantization noise transfer function remains the same and signal transfer function as unity, so that non-idealities of analog blocks are less notable in feedforward SD topology [24].

Given $V_{tn} = 352,92mV$ and $V_{tp} = -492,98mV$ and with advice of Professor Dündar, summation of V_{tn} and V_{tp} is multiplied with 1.5 and V_{dd} is found as $1.268V$. Transient simulation result of inverter is shown in Figure 3.40.

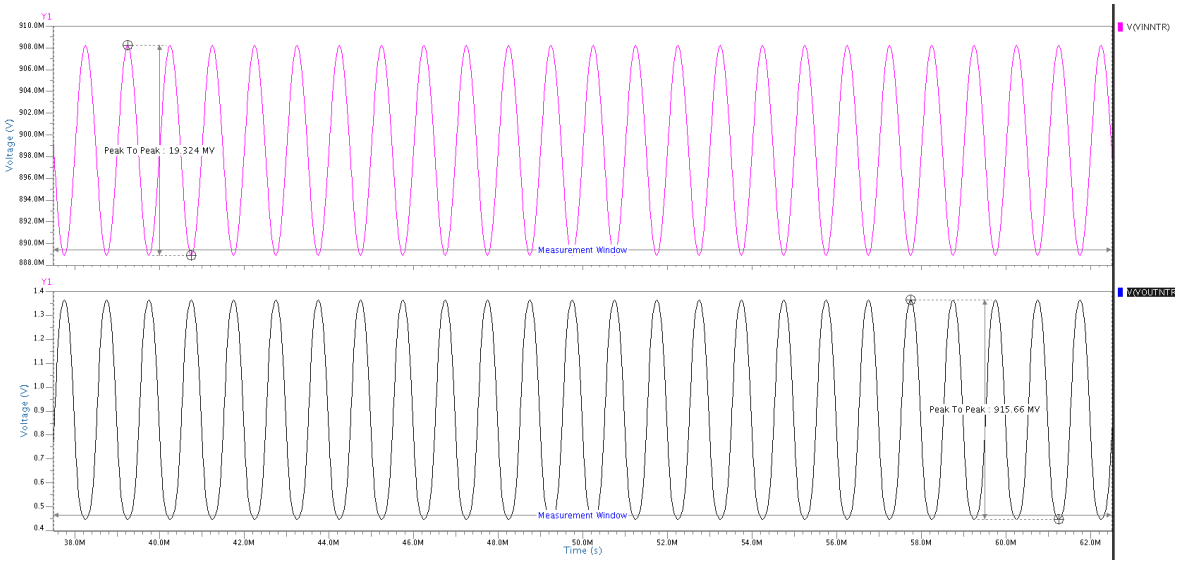

Figure 3.40. Transient Simulation Result of Inverter.

AC simulation result of inverter is shown in Figure 3.41.

SR simulation result of inverter with $10mV$ peak to peak input voltage is shown in Figure 3.42.

SR simulation result of inverter with $1V$ peak to peak input voltage is shown in Figure 3.43.

Table 3.5. Simulation Results of Inverter Used as Operational Amplifier.

	GBW	A_V	SR (+−)	SR (−+)	Power	I
Inverter	$32M$	$36dB$	$32.674M$	$32.672M$	$15.73\mu W$	$8.74\mu A$

3.2.6. Adaptive Biasing CMOS Amplifier

Adaptive biasing amplifiers emerged as a solution of low power dissipation without sacrificing SR characteristics. Adaptive biasing amplifiers based on quite small quiescent current and having a input sense circuitry which enables additional current sources to maintain desired output current for higher SR values. Figure 3.44 shows an architecture of adaptive biasing amplifier [16].

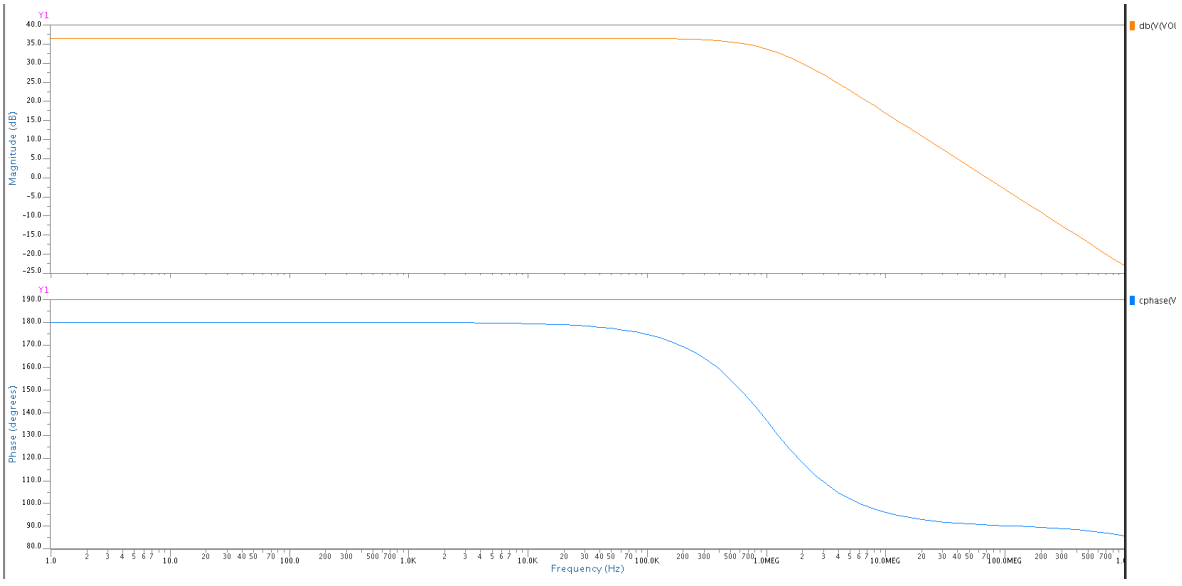

Figure 3.41. AC Simulation Result of Inverter.

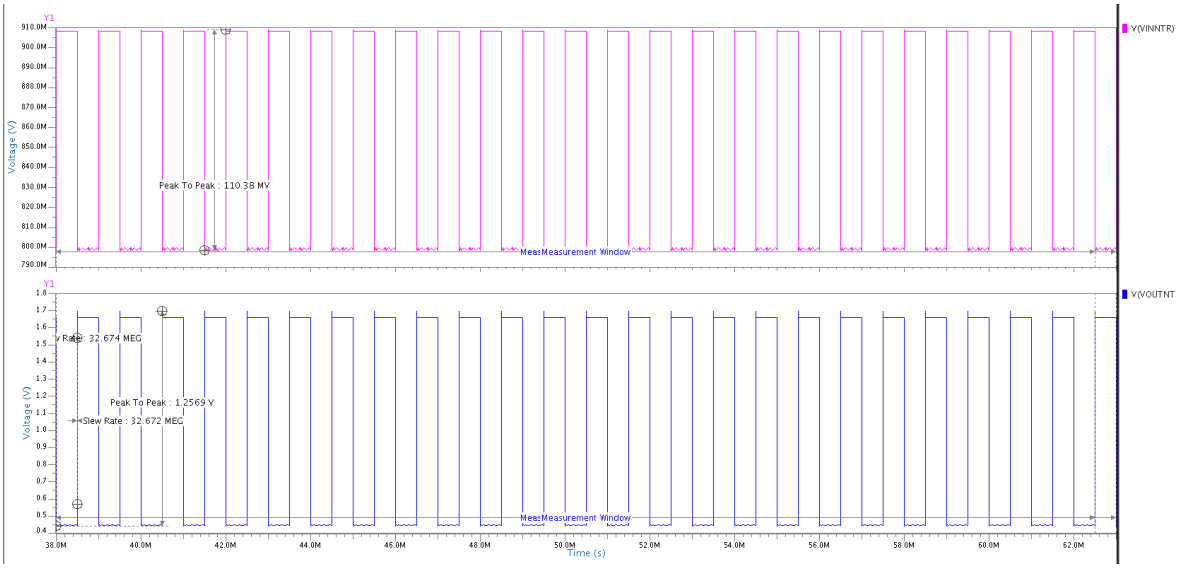

Figure 3.42. SR Simulation Result of Inverter with $10mV$ peak to peak Input Voltage.

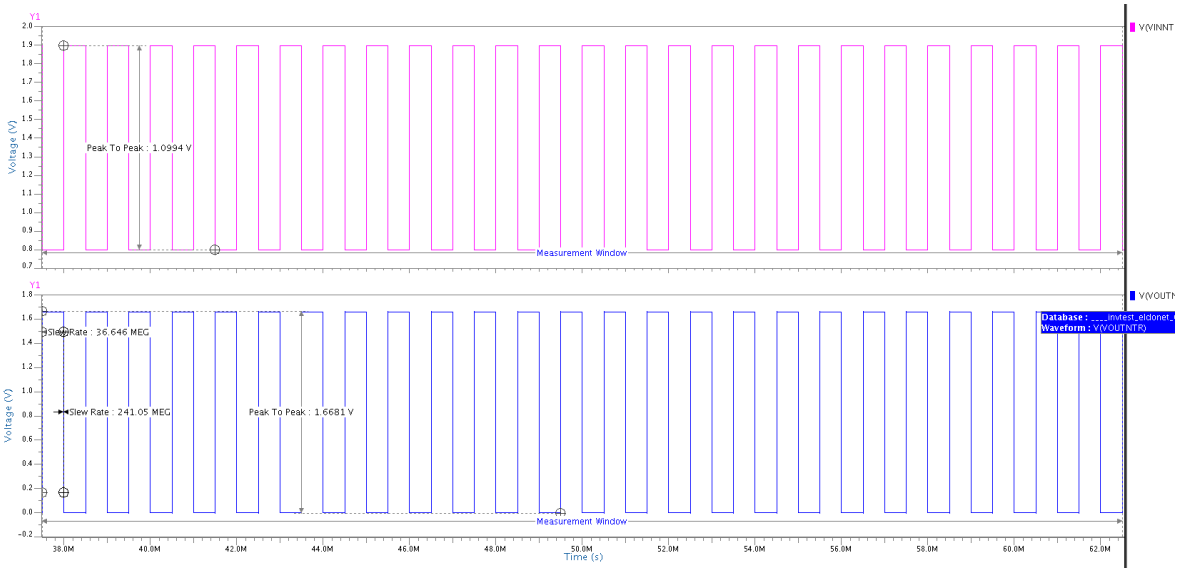

Figure 3.43. SR Simulation Result of Inverter with $1V$ peak to peak Input Voltage.

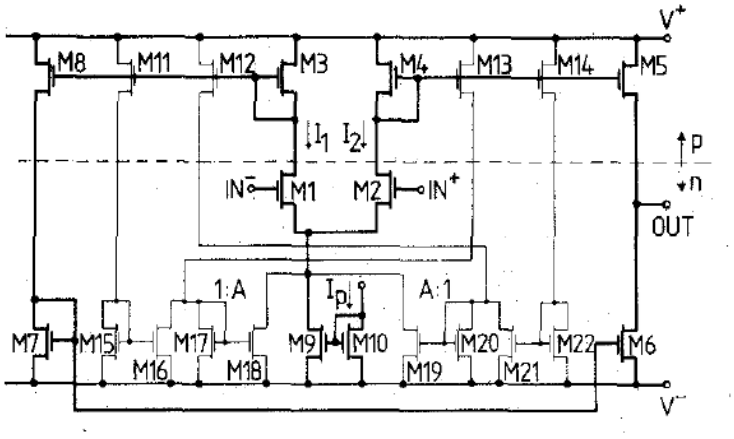

Figure 3.44. Adaptive Biasing Operational Amplifier [16].

Working principle of proposed operational amplifier simply depends on the change in input voltages. When a voltage applied across the inputs of amplifier (IN+ and IN- terminals), the currents I_1 and I_2 become different. The difference of those currents is realized by the circuit shown in Figure 3.45.

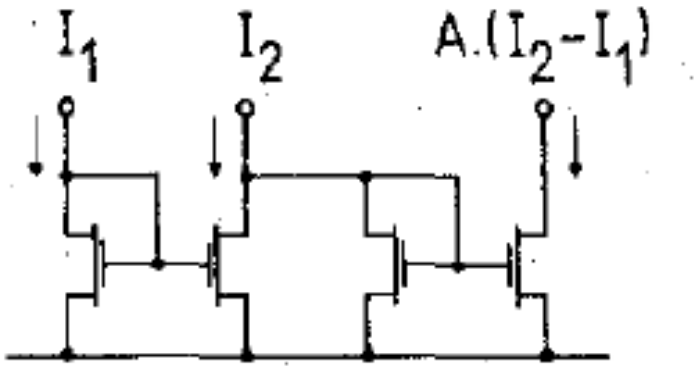

Figure 3.45. Current Subtractor Realizing $A.(I_2 - I_1)$.

In this configuration A is called current feedback factor and the bias current of the amplifier is called I_p. In such cases as I_1 and I_2 are not identical, current subtractor configuration realizes $A.(I_2 - I_1)$ and adds that generated current to main tail current of differential pair. In realization of adaptive biasing operational amplifier circuit, A is chosen as 2 to achieve the following current behavior in Figure 3.46.

The additional current source is realized by two subtractors shown Figure 3.46. Only if I_2 becomes larger than I_1, will the subtractor draw a current which is $A.(I2 - I1)$. Otherwise the subtractor draws zero current since I_1 and I_2 are identical to each other. After that, by putting subtractors in the scheme of the simple OTA where the currents at the inputs of the subtractors are provided by means of current mirror, whole differential feedback amplifier is formed. If there is no disturbance at the virtual ground, the currents I_1 and I_2 are equal and total bias current is thus I_p. Whenever a signal is applied, total bias current will be $I_p + A.|I_1 - I_2|$ In realization of the circuit, in order to have highest transconductance, input transistors are biased in weak inversion region. Therefore I_p is chosen as $1.5\mu A$ The relation between I_1 and I_2 can be expressed

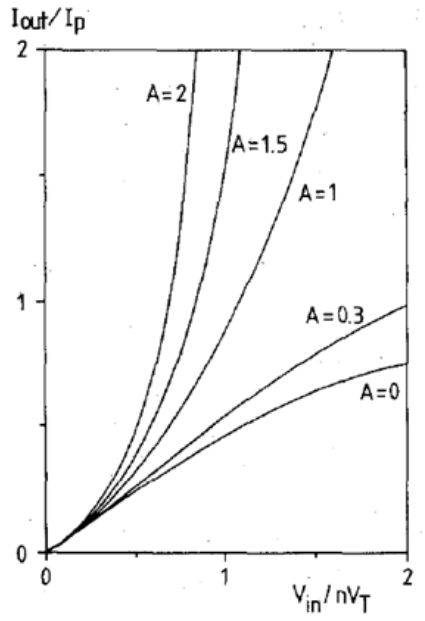

Figure 3.46. Behaviour of I_{out} vs V_{in} for Different Values of A.

with inversion region current formula [25] and Kirchhoff's current law ($V_{in} = V_{in}^{+} - V_{in}^{-}$) .

$$I_1 = I_2.e^{\frac{V_{in}}{n.V_T}} \tag{3.1}$$

Replacing I_2 with I_p

$$I_1 = \frac{I_p.e^{\frac{V_{in}}{n.V_T}}}{(A+1) - (A-1).e^{\frac{V_{in}}{n.V_T}}} \tag{3.2}$$

The current flowing thorough load capacitor I_{out} is b times the difference between I_1 and I_2

$$I_1 = \frac{I_p.(e^{\frac{V_{in}}{n.V_T}} - 1)}{(A+1) - (A-1).e^{\frac{V_{in}}{n.V_T}}}.b. \tag{3.3}$$

Therefore needed current is generated as I_{out} which equals to $3\mu A$ to achieve settling goal

With addition of common mode feedback circuit, final version of adaptive biased operational amplifier is shown in Figure 3.47.

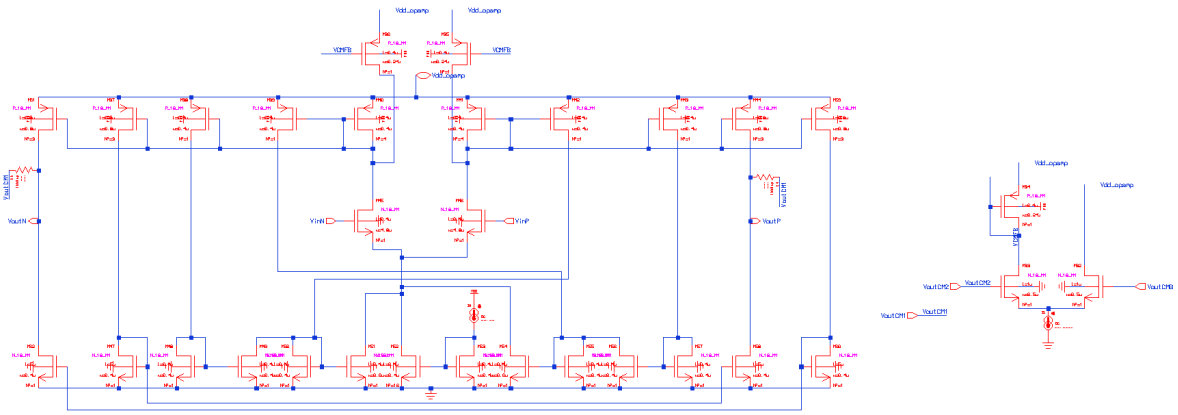

Figure 3.47. Adaptive Biasing Opamp with Common Mode Feedback.

Common mode feedback circuit simply has one fourth of the tail current of input stage of the opamp. According to the average value of positive and negative outputs of the opamp, the circuit tunes both output nodes to given common mode voltage from ideal DC source by injecting current to the input stage of operational amplifier.

The test circuit is shown in Figure 3.48.

In this testbench resistor values are set to $10k\Omega$ and in between output terminals of opamp to resistors voltage controlled voltage sources with gain of 1 are used to neglect possible driving strength problems with suggestion of Prof. Devrim Yılmaz Aksın. Also in AC simulations, in order to set DC values of the operational amplifier below another voltage controlled voltage sources with gain of 1 are used to tune the same DC values with previous operational amplifiers.

Transient simulation result can be seen in Figure 3.49.

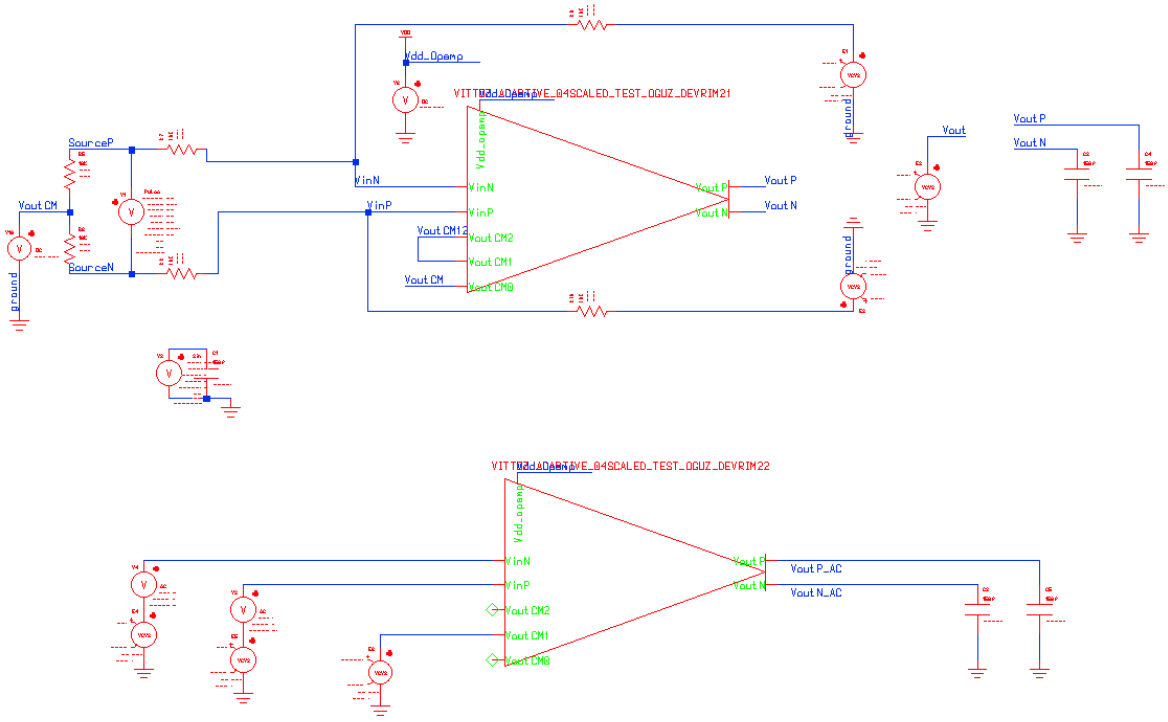

Figure 3.48. Testbench of Adaptive Biasing Opamp.

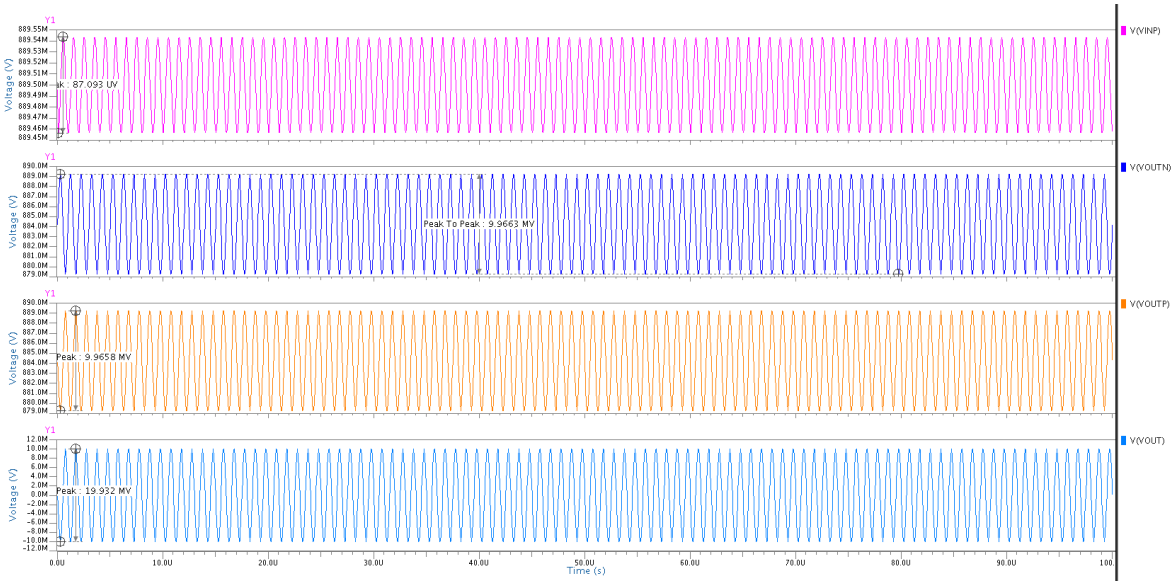

Figure 3.49. Transient Simulation Result of Adaptive Biasing Opamp.

AC simulation result can be seen in Figure 3.50.

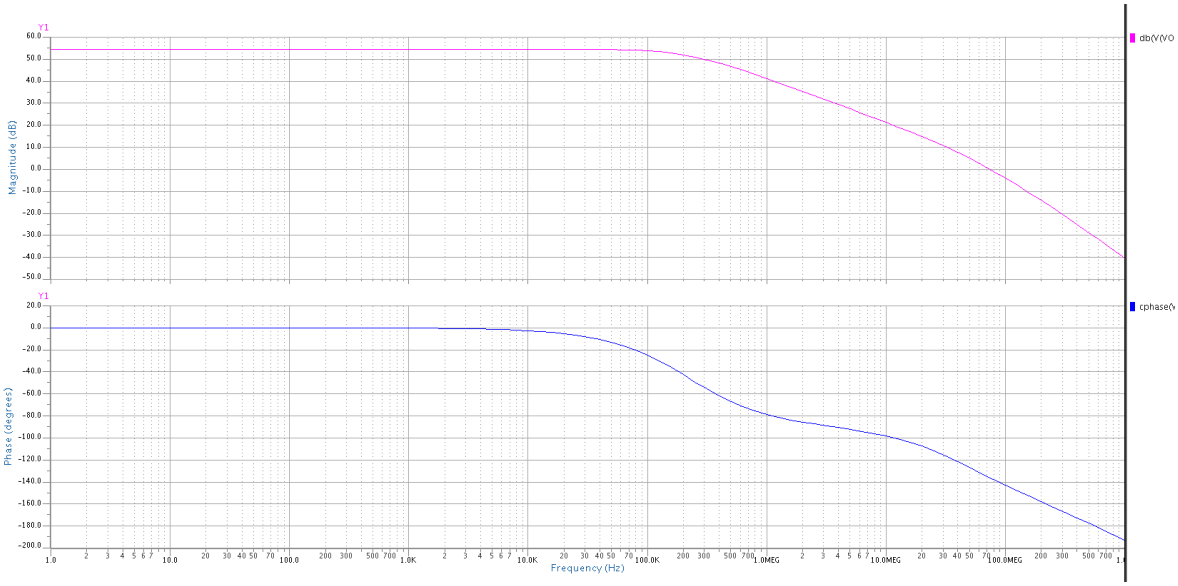

Figure 3.50. AC Simulation Result of Adaptive Biasing Opamp.

Slew Rate results of the circuit for $10mV$ peak to peak input voltage can be seen in Figure 3.51.

Slew Rate results of the circuit for $1V$ peak to peak input voltage can be seen in Figure 3.52.

Table 3.6. Simulation Results of Adaptive Biasing Operational Amplifiers.

	GBW	A_V	SR $(+-)$	SR $(-+)$	Power	I
Adaptive Biased	$50M$	$54dB$	$1.18M$	$1.18M$	$41.7\mu W$	$23.2\mu A$

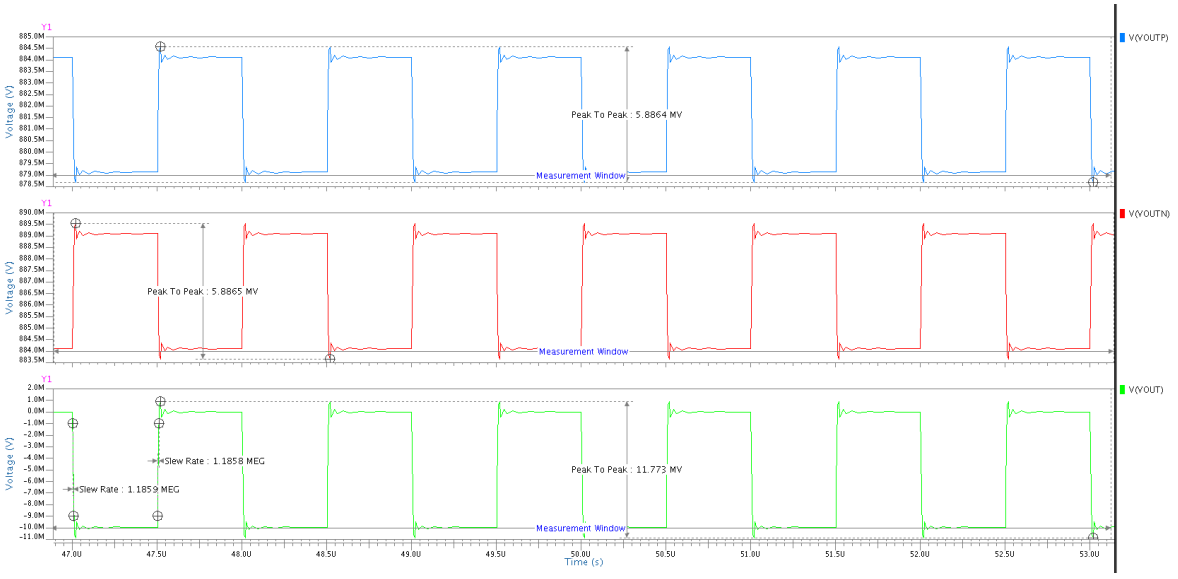

Figure 3.51. SR Result of Adaptive Biasing Opamp for $10mV$ peak to peak input voltage.

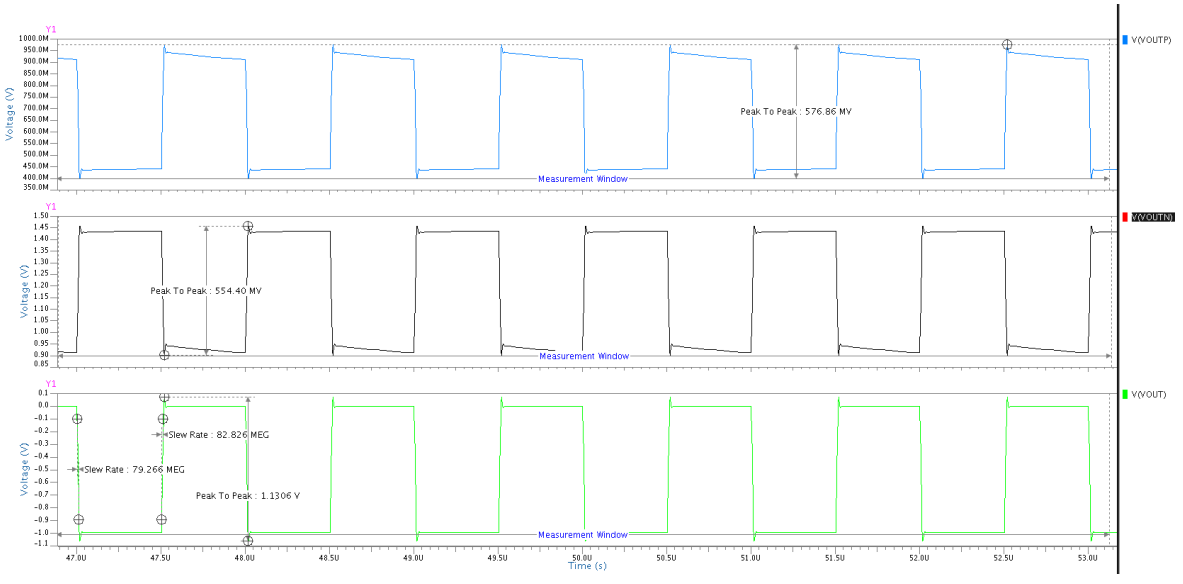

Figure 3.52. SR Result of Adaptive Biasing Opamp for $1V$ peak to peak input voltage.

4. CONCLUSIONS AND FUTURE WORKS

SD modulators have become a common choice of analog to digital conversion due to easier implementation in terms of circuit complexity and also no need of additional sample and hold amplifier design. Also SD modulators are equipped with oversampling, quantization noise shaping and digital filtering, for this reason using SD modulators in low power and high speed applications become very popular. Furthermore, with an optimized operational amplifier design in terms of speed and power consumption, the total power consumption of SD modulators can drastically decreased without any performance loss. Since the most power hungry analog building block is operational amplifiers, there is no doubt that optimizing operational amplifiers for power is key of decreasing total power consumption. In order to achieve better power consumption in operational amplifiers, quiescent current, average current consumption in operation and SR optimization should have done carefully.

In this thesis, different types of operational amplifiers in terms of output stages and working principles are proposed in order to reduce total power consumption of the circuit comparing to similar works done at this field. Since operational amplifier is one of the most critical analog building blocks in terms of power consumption, the aim of the study is to define how to start and modify operational amplifiers for low power SD modulators. Table BELOW shows all results of simulations about designed operational amplifiers. Finally, all the study covered, designing low power operational amplifier is a crucial approach to decrease overall power consumption of SD modulators. Having a well-tuned opamp in a SD modulator will make overall topology efficient in terms of power.

Table 4.1. Comparison of Specs of Designed Operational Amplifiers.

	GBW	A_V	SR $(+-)$	SR $(-+)$	Power	I
ABAB Bio	$143.5M$	$55.2dB$	$16.6k$	$16.6k$	$44.92\mu W$	$24.96\mu A$
ABAB UC	$11.1M$	$27dB$	$200.4k$	$200.6k$	$27.14\mu W$	$15.08\mu A$
AB Bio	$2.1M$	$24dB$	$493.2k$	$421.6k$	$65.9\mu W$	$36.63\mu A$
AB Cascode	$30M$	$63dB$	$1.04M$	1.04	$51.48\mu W$	$28.6\mu A$
Inverter	$32M$	$36dB$	$32.674M$	$32.672M$	$15.73\mu W$	$8.74\mu A$
Adaptive Biased	$50M$	$54dB$	$1.18M$	$1.18M$	$41.7\mu W$	$23.2\mu A$

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