IMPROVING THE EFFICIENCY OF MICROWAVE POWER AMPLIFIERS WITHOUT LINEARITY DEGRADATION USING LOAD AND BIAS TUNING IN A NEW CONFIGURATION

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ABSTRACT

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Advanced digital modulation schemes used in the wireless applications, result in the modulated RF signals with high peak to average power ratio which requires linear amplification. On the other hand, the demand for a longer talk time with less battery volume and weight, especially in hand-held radio units, necessitate more power efficient methods to be utilized in power amplifier design. But improved linearity and efficiency have always been contradicting requirements demanding innovative power amplifier and linearizer design techniques.

Dynamically varying the load impedance and bias point of a transistor according to the varying envelope of the incoming RF signal also known as Dynamic Load Modulation (DLM) and Dynamic Supply Modulation (DSM), respectively, are two separate methods for improving the efficiency in power amplifier design. In this dissertation, a combination of both variable gate bias and tunable load concepts is applied in an amplifier structure consisting of two transistors in parallel.

A novel computer aided design methodology is proposed for careful selection of the load and biasing points of the individual transistors. The method which is based on load-pull analysis performs sweeps on the gate bias voltages of the active devices and input drive level of the amplifier in order to obtain ranges of biases that result in the generation of IMD sweet spots. Following that, the amplifier is designed employing the load line theory and bias switching at the same time in order to enhance the efficiency in reduced drive levels while extending the output 1 dB compression point to higher values at higher drives.

Tunable matching networks are implemented utilizing varactor stacks in a Π configuration at the input

and output of the amplifier. The amplifier starts to operate in the first state where lowest possible bias levels are chosen for both of the transistors and the output matching network is adjusted to provide PAE matching. As approaching towards the higher output powers, the amplifier switches between different consecutive operational states per about 1 dB increment at output power. In this way, the maximum output P_{1dB} can be attained from the amplifier. The operational states are selected among a bunch of possible states obtained from the load-pull analysis, based on providing smaller leaps in transition between states in PAE and gain curves.

In order to validate the proposed design methodology, a 2.4 GHz medium-power amplifier is designed, fabricated and tested which demonstrates the feasibility of the proposed structure and design technique for power amplifier applications.

Keywords: power amplifier, efficiency, linearity, tunable impedance matching network, varactor

ÖZ

MİKRODALGA GÜÇ YÜKSELTEÇLER İÇİN YENİ BİR KONFİGÜRASYONDA YÜK VE BESLEME AYARI İLE DOĞRUSALLIĞI DÜŞÜRMEDEN VERİMLİLİK ARTIRILMASI

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Kablosuz uygulamalarda kullanılan gelişmiş dijital modülasyon teknikleri, doğrusal yükseltme gerektiren, tepe gücü ortalama gücüne göre yüksek olan mödüle olmuş RF sinyallerine neden olur. Öte yandan, özellikle elle taşınır radyo ünitelerinde, daha hafif ve küçük piller ile daha uzun konuşma süresi talebi, güç yükselteç tasarımında daha verimli yöntemlerin kullanılmasını gerektirir. Ancak, yüksek doğrusallık ve yüksek verimlilik isterlerinin birbiri ile çelişmesi, yenilikçi güç yükselteç ve doğrusallaştırıcı tasarım tekniklerini gerektirmektedir.

Sırası ile Dinamik Yük Modülasyonu (DYM) ve Dinamik Besleme Modülasyonu (DBM) olarak bilinen, transistörün yük empedansının veya bias noktasının gelen RF sinyalinin değişken zarfına göre değiştirilmesi, güç yükselteci tasarımında verimliliği artırmak amacı ile uygulanan iki ayrı yöntemdir. Bu tezde, paralel bağlanmış iki transistörden oluşan yükselteç yapısında, hem değişken bias (DBM) hem de ayarlanabilir yük (DYM) kavramları uygulanmıştır.

Her bir transistörün yük ve bias noktalarının dikkatlice seçilmesi için yeni bir bilgisayar destekli tasarım yöntembilimi önerilmiştir. Load-pull analizine dayanmakta olan bu yöntem, IMD sweet spotlarının oluşumuna yol açan bias aralıklarını elde etmek amacıyla, aktif cihazların gate bias gerilimlerinin ve yükselteçin giriş gücünün üzerine tarama yapmaktadır. Ardından load line teorisini ve bias anahtarlamayı aynı anda kullanarak, yüksek sürüşlerde 1 dB çıkış bastırma noktasını yüksek seviyelere taşıyarak düşük sürüş seviyelerinde verimliliği artırmak amacı ile yükselteç tasarlanmıştır.

Yükseltecin giriş ve çıkışına, Π konfigürasyonda olan varaktör kümeleri kullanılarak, ayarlanabilir empedans uyumlama ağları yerleştirilmiştir. Yükselteçte bulunan her iki transistör için mümkün olan en düşük bias seviyesi seçilerek ve güç eklenmiş verimlilik (PAE) uyumu sağlamak amacı ile çıkış

empedans uyumlama ağında ayarlama yapılarak yükselteç birinci durumda çalışmaya başlatılır. Daha yüksek çıkış güçlere yaklaşıldıkça, yükselteç çıkış gücünün 1 dB aralıklar ile artmasına karşılık gelen ardışık çalışma durumları arasında geçiş yapar. Böylece yükselteç yapısından maximum çıkış P_{1dB} elde edilir. Yükselteçin operasyonel durumları, PAE ve kazanç grafiklerinde belirtilen durumlar arasındaki geçişte küçük sıçramalar sağlayan load-pull analizinden elde edilmiş birçok olası durum arasından seçilmektedir.

Önerilen tasarım yöntembilimini doğrulamak için 2.4 GHz'de çalışan orta-güç seviyeli bir yükselteç tasarlanıp, üretilmiş ve testleri yapılmıştır. Böylece güç yükselteç uygulamalarında önerilen yapının ve tasarım tekniğinin yapılabilirliği gösterilmiştir.

Anahtar Kelimeler: Güç Yükselteç, Verimlilik, Doğrusallık, Ayarlanabilir Empedans Uyumlama Ağı, Varaktör

To my beloved parents

and

sister,

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INTRODUCTION

1.1 Linearity and Efficiency in PA Design for Wireless Communications

In modern communication systems like WLAN and CDMA, spectrum is expensive and newer technologies demand transmission of maximum amount of data using the minimum amount of spectrum. Higher spectrum efficiency can be attained by sophisticated non-constant envelope digital modulation schemes such as Quadrature Amplitude Modulation (QAM) and Quadrature Phase Shift Keying (QPSK). In these linear modulation schemes information is transmitted in both the amplitude and phase of the RF signal leading to high Peak to Average Power Ratios (PAPR) [1].

The PAPR of the spectrally efficient modulation formats in use today is about 4-9 dB in CDMA 2000 systems, and can be of the order of 10 dB in IEEE 802.11 d g wireless LAN systems [2]. Table 1.1 lists the characteristics of several popular cellular standards. These standards employ modulation methods that increase the peak to average power of the transmitted signal in proportion to the number of channels being transmitted [3].

Table1.1: Popular cellular phone standards [3].

Communications Standard	Modulation Scheme	PAPR (dB)
CDMA	QPSK/OQPSK	9 to 10
WCDMA	QPSK	8 to 9
TDMA	$\pi/4$ DQPSK	3 to 4
GSM/EDGE	GMSK 8-PSK (in EDGE only)	1 to 2

The large PAPR of these modulation schemes implies the large envelope fluctuations by time which must be preserved in order to save the full information content of the original message signal. Hence the RF power amplifier as the vital part of any wireless transmitter has to be highly linear, to achieve a high bit error rate, and limit spectral regrowth to acceptable levels. Although linear amplification is achievable, it always comes at the expense of efficiency. Since the RF power amplifiers implemented in such systems are 'backed off' from their saturation into their linear operating region or designed to operate in Class A or AB configurations in order to obtain a satisfactory linearity over the transmitter's dynamic range.

This drastically reduces the efficiency of the power amplifier decreasing the battery life of the handset in mobile systems. On the other hand, as the demand for a longer talk time with less battery volume and weight in hand-held radio units increases, more power efficient techniques are clearly needed since a large portion of battery power is dissipated by these amplifiers. A higher efficiency gives a longer battery lifetime and thus a longer talk time of the mobile device [4]. Before any further proceeding, it is necessary to review the definition of 'efficiency' in the PA design. There are two typical definitions for the efficiency in RF PAs [1]: 'output efficiency' and 'power added efficiency'. Output efficiency is defined as the ratio of the RF output power P_{out} to the dc power P_{dc}:

$$\eta = \frac{P_{out}}{P_{dc}} \tag{1.1}$$

However, the above definition does not take into account the input power P_{in} and power gain G , whose effects are significant in RF PAs. This results in the definition of *Power Added Efficiency (PAE)*:

$$\begin{aligned} PAE &= \frac{P_{out} - P_{in}}{P_{dc}} \\ &= \frac{P_{out} - P_{out}/G}{P_{dc}} \\ &= \eta \cdot \left(1 - \frac{1}{G}\right) \end{aligned} \tag{1.2}$$

According to their maximum possible efficiencies as shown in Table 1.2, RF power amplifiers can be classified as Class A, AB, B, C, D, E, and F [1] , [8]. Figure 1.1 relates the different operational classes of power amplifiers to the conduction angle and input signal overdrive [5].

Table1.2: Comparison of peak possible efficiency for different classes of power amplifiers.

Classification	A	AB	B	C	D	E	F
Maximum Efficiency (%)	50	50 ~ 78.5	78.5	100	100	100	100

For small input signals, the PA can operate in class A, AB, B or C, depending on the conduction angle. The conduction angle is determined primarily by the DC gate bias. The efficiency can be improved by reducing the conduction angle and moving in the direction of class C at the expense of lower output power. An alternative is to increase the gate overdrive until the PA operates as a switch, while keeping the same conduction angle. This results in operational classes of D, E and F with the efficiency that ideally approaches to 100%. However, the performance of these high-efficiency amplifiers is often non-linear, resulting in significant out-of-band radiation and interference in adjacent channels [5].

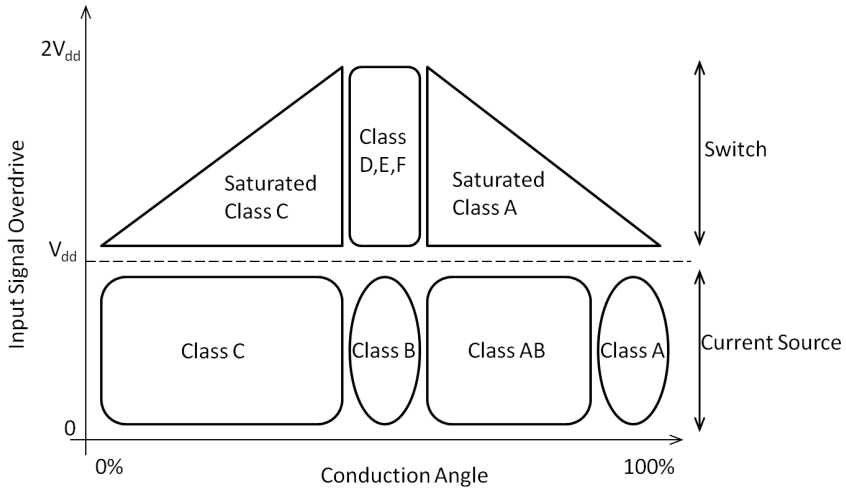


Figure 1.1: Definition of PAs based on conduction angle and signal overdrive.

Further study of different classes of PAs is fully available in the literature and is beyond the scope of this dissertation.

To sum up, improved linearity and efficiency of a communication system have always been conflicting requirements demanding innovative power amplifier design techniques (Figure 1.2). Reported schemes targeted toward improving the efficiency of RF PAs can be broadly classified in two categories, which are: 1) linear PAs with an efficiency-enhancement circuit and 2) non-linear PAs with a linearization circuit.

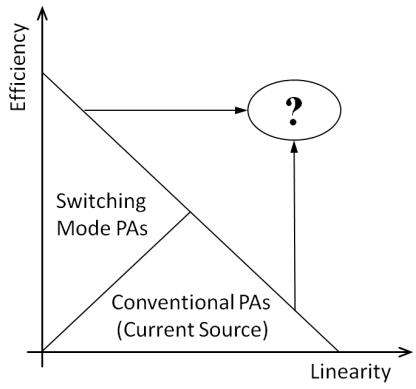


Figure 1.2: Efficiency and linearity trade-off in RF power amplifiers.

Those techniques which improve efficiency without attempting to quantify the impact on linearity or RF power output are of paramount importance in mobile systems, where battery lifetime and thermal management are critical. However, there are other power amplifier applications where efficiency becomes an important, but secondary consideration, in comparison to linearity. Such applications would

typically be single or multichannel base-station transmitters in ground or satellite communications systems [1].

1.2 Linear Power Amplifiers with an Efficiency-Enhancement Circuit

Power amplifiers are the bottleneck of RF power consumption in handsets. A typical Class AB power amplifier consumes more power than a transmitter IC and therefore the power amplifier is the biggest RF dc power consumer in handsets. Since the dc power consumption remains constant at the low power region, the efficiency of the power amplifier is degraded as the RF output power decreases. Furthermore, more than 90 percent of the output power occurs between -15 dBm and +15 dBm, where the efficiency is low. As a result, average power efficiency (over the full range of output powers), instead of peak power efficiency, is the key factor determining the battery life and talk time for portable wireless applications [6].

An implementation of efficiency enhancement technique that results in a very high efficiency in the linear region of operation of the power amplifier proved to be a good solution for the problem of linearity and efficiency contradiction. The techniques to enhance the efficiency of linear power amplifiers assume immense significance in modern wireless systems. Several efficiency enhancement techniques have been suggested to date. Envelope Elimination and Restoration, Envelope Tracking, Outphasing technique known as LInear amplification using Nonlinear Components (LINC), Doherty amplifier and Dynamic Biasing are the most common methods of enhancing the efficiency which are going to be investigated briefly in the following.

1.2.1 Envelope Elimination and Restoration

The Envelope Elimination and Restoration (EER), known as the Kahn technique, is one of the oldest methods originally proposed by Kahn [7] in 1952 as a more efficient alternative to linear Class AB RF power amplification for single sideband (SSB) transmitters. The general principle is to provide a highly efficient and linear power amplification by combining a highly efficient switching-mode amplifier with a linear low-frequency amplifier (modulator). It combines a highly efficient, but nonlinear RF PA with a highly efficient envelope amplifier to implement a high-efficiency linear RF PA [8].

In its classic form as shown in Figure 1.3, the RF input signal is divided by a power splitter and fed into two branches. The signal in the upper branch is detected producing a Base-Band (BB) modulation signal which in turn, modulates the bias voltage of the RF PA.

In the lower branch, a limiter eliminates the envelope and the output signal is now containing only the phase information. Experiencing some delay the constant-amplitude phase modulated carrier is then amplified efficiently by class-C, -D, -E, or -F RF PAs which operate in saturation at all times. The network delay is adjusted to ensure that the group-delay of the BB branch is identical to that of the RF branch, so that the signal is reconstructed properly both in amplitude and phase. The equalization of the time delay between the BB channel and the RF channel is important to be able to amplify signals that contain phase information. Without phase equalization, only the simplest signals can be amplified with low distortion using this scheme. Amplitude modulation of the final RF PA restores the envelope to the phase-modulated carrier creating an amplified replica of the input signal [9]-[10].

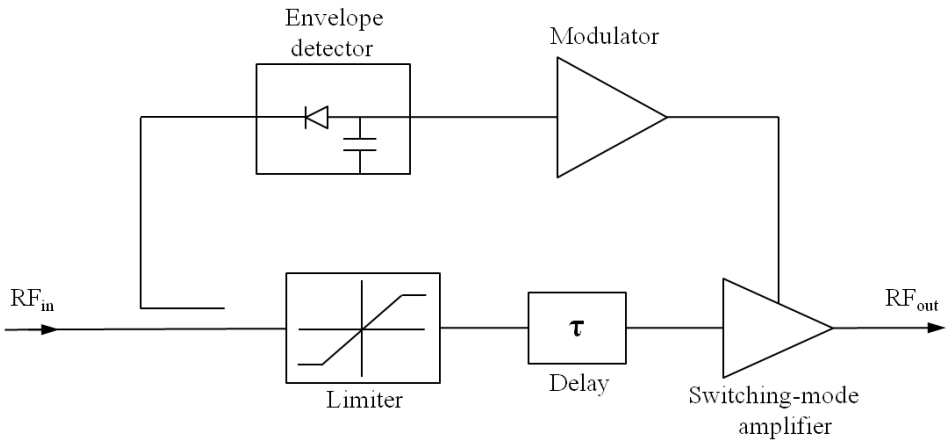


Figure 1.3: Envelope Elimination and Restoration system.

Average efficiencies three to five times those of linear amplifiers have been demonstrated from HF to L-band. Furthermore, transmitters based upon the Kahn technique generally have excellent linearity because linearity depends upon the modulator rather than RF-power transistors. In a modern implementation, both the envelope and phase-modulated carrier are generated by a DSP [11].

However, since the envelope detecting signal path consumes quite an amount of power, the overall efficiency will be degraded considerably. At the same time, since the modulator may have to supply rather large currents if the PA is of high power, the practical bandwidth might be limited to only a few MHz. In fact, even if the bandwidth of the RF branch is much larger than the one of the modulation branch, the extra band cannot be utilized in an instantaneous mode. This is because any additional signal in the RF band introduces modulation frequencies higher than what the BB circuitry can support, which in turn results in strong intermodulation and spectrum asymmetry. Hence an even greater design challenge is posed for wideband applications. Furthermore, a good envelope control circuit is rather complex. These above issues make the EER configuration not well suited for handset power amplifiers [10].

1.2.2 Envelope Tracking

The envelope-tracking (ET) architecture is similar to the EER system. Both of them have an envelope-detecting path and an RF path. However, the RF drive of the RF power amplifier in ET preserves both amplitude and phase information, whereas the RF drive in EER only retains the phase information. The combination of an envelope detector and a DC-DC converter in ET systems, as shown in Figure 1.4, dynamically varies the biasing points of the of the active devices in RF power amplifier. Since the dc power consumption is reduced at low powers, the efficiency is improved.

An ET amplifier relies on modulating the collector (or drain) bias voltage with respect to the instantaneous input envelope signal such that the RF amplifier is in or near gain compression for all envelope signal levels [12]. With the base (or gate) bias control, the operating point moves vertically for a given collector (or drain) voltage on the I-V curve of the transistor; on the other hand, with dynamic control of collector (or drain) bias voltage, the point moves horizontally for a fixed bias current. In the dual bias control scheme, the operating point is designed to move diagonally by controlling both the base

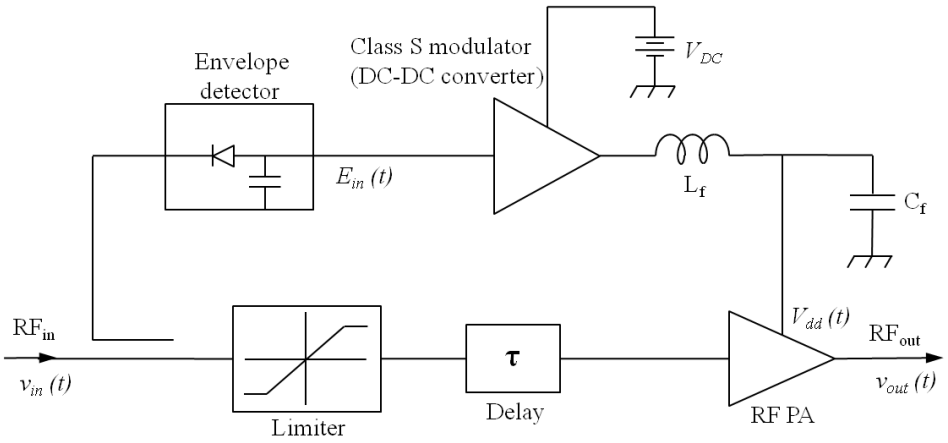


Figure 1.4: Envelope Tracking system block diagram.

(or gate) and collector (or drain) biases to maximize the power efficiency [13].

Operation of the envelope following technique is described by reference to the simplified block diagram of Figure 1.4 where a modulated RF signal ($v_{in}(t)$) is applied to the input of an RF power amplifier. $v_{in}(t)$ is assumed narrow band and therefore can be described in terms of amplitude and phase components taking the form [12]:

$$v_{in}(t) = E_{in}(t)\cos\omega_0 t + \Phi_{in}(t) \tag{1.3}$$

where $E_{in}(t)$ describes envelope properties of the modulation and $\Phi_{in}(t)$ describes phase characteristics of the signal. In addition to the RF signal path, $E_{in}(t)$ is determined via a detector, then amplified by a class-S modulator, and lastly applied as the drain bias voltage $V_{dd}(t)$ to the RF power amplifier. Since the detected envelope signal is time varying, the drain supply bias is also time varying. Class-S modulator is a switching dc-dc converter. A transistor and diode or a pair of transistors act as a two-pole switch to generate a rectangular waveform with a switching frequency several times that of the output signal. The width of pulses is varied in proportion to the instantaneous amplitude of the desired output signal, which is recovered by a low-pass filter. The switching frequency must typically be six times the RF bandwidth. A switching frequency of 500 kHz is readily achieved with discrete components, and 10 MHz is achievable in IC implementations. Due to the need for the Class-S modulator to produce a supply voltage with high current drive, ET technique is difficult to implement for wide bandwidth signals [8].

When the supply voltage tracks the instantaneous envelope modulation signal, it is called Wide Bandwidth ET (WBET) or Envelope Following technique [14] - [17]; when the supply voltage tracks the long-term average of the input envelope power, it is called Average ET (AET) [18] - [19]. The AET can be very effective in situations where the power amplifier functions primarily in deep back-off for extended time periods. varying the supply bias with respect to the RMS magnitude of the input modulated envelope signal occurs on a time scale that is considerably slower than the modulation rate. Under power back-off, bias voltage $V_{dd}(t)$ is lowered to a value less than battery voltage V_{DC} by the class-S modulator. Consequently the efficiency is improved since the power consumed by the amplifier

is significantly less than would be the case if operated at higher supply voltage of V_{DC} [20]. When the supply voltage switches to different step levels according to the input envelope power, it is called Step ET (SET) [21] - [22]. The AET and SET are especially useful for dynamic power control schemes such as the reverse link in CDMA systems where the variation in average power is much greater than 20 dB [23].

A number of efficiency enhancement schemes based on dynamically changing of the supply voltages has been reported in the literature in which designs were carried out with buck (the output voltage is lower than the input voltage) [18], boost (the output voltage is higher than the input voltage) [17] ,[24], adaptive buck-boost [19] and Single-Ended-Primary-Inductance Converters (SEPICs) [25]. In another design [26] an on-chip adaptive bias circuit controlling the quiescent current adaptively to the power level is proposed. The circuit supplies a low quiescent current at the low output power level for high efficiency, and the quiescent current increases adaptively with the input power to supply a higher quiescent current at the high output power level for high linearity. It results in a significant decrease of the module size, as well as decrease in cost, since no dc-dc converters or switches have been utilized in the design.

There are still a number of practical issues during monolithic implementation. First, an off-chip inductor and capacitor are typically used in the DC-DC converter [25], which degrades the integration performance. The monolithic DC-DC converter with on-chip passive components has been implemented [27], but low-Q components considerably reduce the overall efficiency of the ET system. Second, when the bias voltage and current are adjusted dynamically, the power gain of the RF PA varies dramatically [17]. The gain variation degrades the system performance in terms of Error Vector Magnitude (EVM).

1.2.3 Dynamic Bias Switching

Although the efficiency of dynamic power supply schemes can be very high, it is difficult to control the drain bias at high speed because of the narrow bandwidth of the DC-DC converter. Dynamic Bias Switching (DBS) is an attractive way to overcome bandwidth problems because of using a switch instead of a high-speed DC-DC converter.

Unlike the EER or other variations of envelope tracking systems that amplitude modulates the supply voltage, the DBS simply steps up the supply voltage only at moments of signal peaks. As shown in Figure 1.5, such technique is effective for signals with high peak-to-average ratios such as CDMA [21].

DBS is one of the topics which has recently gained a good interest. To mention two of the pioneer designs, in [28] Jeon et al. propose a DBS technique with only one dc power supply is introduced which can reduce power consumption considerably, especially in high peak-to-average power ratio (PAPR) systems and in [29], a DBS system is applied to a class-AB power amplifier for 859 MHz band of WCDMA applications.

1.2.4 Outphasing Technique or LINC

Outphasing operation is a technique with a long history that was first proposed by Henri Chireix in 1935 to improve average efficiency and linearity of AM broadcast transmitters utilizing vacuum tubes with poor linearity [30]. This idea has been revived and applied to various wireless applications since it was reinvented by D. C. Cox, who introduced the term ‘LINC’ (LInear amplification using Nonlinear

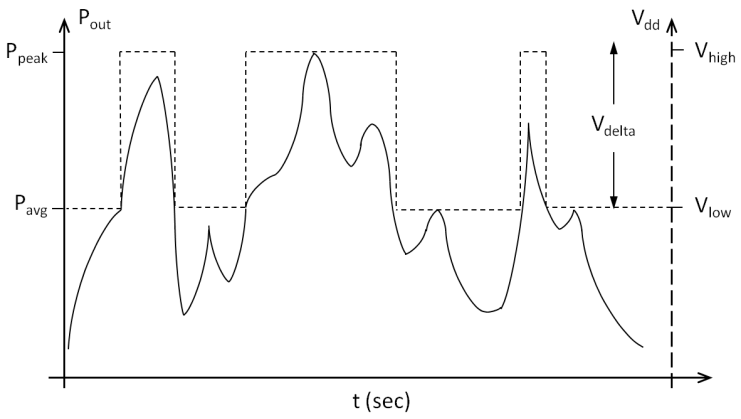


Figure 1.5: Modulated signal waveform in DBS

Components) in 1974. LINC was invented to realize a linear amplifier where the intermediate stages of RF power amplification could employ highly nonlinear devices. An outphasing transmitter produces an amplitude-modulated signal by combining the outputs of two PAs driven with signals of different time-varying phases. The general principle is shown in Figure 1.6.

First, an envelope modulated waveform ($S_{in}(t) = A(t)\cos[\omega t + \phi(t)]$) is decomposed into two outphased constant envelope signals:

$$S_1(t) = \cos[\omega t + \phi(t) + \cos^{-1}(A(t))] \tag{1.4a}$$

$$S_2(t) = \cos[\omega t + \phi(t) - \cos^{-1}(A(t))] \tag{1.4b}$$

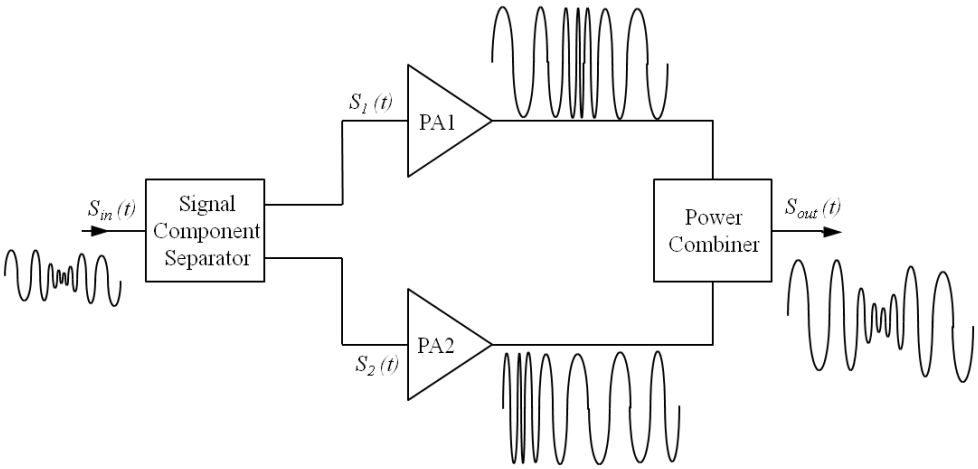


Figure 1.6: Simplified block diagram of an outphasing system.

Subsequently, these two signals are individually applied to highly-nonlinear power amplifiers. The resulting output signals are then recombined through a passive combiner into the final output signal $S_{out}(t)$, where

$$S_{out}(t) = G\,[S_1(t) + S_2(t)] = 2GA(t)\cos(\omega t + \phi(t)) \tag{1.5}$$

The key element in a Chireix's outphasing system is the Signal Component Separator (SCS), which converts the input AM signal into two outphased component PM signals that have constant envelopes. It is exactly such modulation conversion that brings the possibility of highly efficient and highly linear amplification. Because the envelopes of the signals to be amplified are now fixed and the magnitude of the envelopes contains no information (all the amplitude information of the original AM signal is contained in the phase of the component PM signals), we can employ PA cells in the branches which have an extremely high peak efficiency and therefore achieve a overall high efficiency.

Meanwhile, also thanks to the fixed envelope in the branch amplifiers, the nonlinearity of the input-output power characteristic as present in most high-efficiency PA implementation will have very little influence on the overall input-output transfer function of the Chireix's outphasing system. As a result, the total system can be highly linear over a wide range of signal levels, provided the SCS and the power combiner do not introduce nonlinear signal distortion. In practice, for the branch amplifiers, the most high-efficiency PAs or even constant-amplitude phase-locked oscillators can be used to realize linear amplification, which explains the acronym LINC that is typically used for these types of amplifiers.

In summary, theoretically Chireix's outphasing operation provides a clear, simple, and promising solution for simultaneously achieving high efficiency and high linearity in a power amplifier system. However, practical implementation aspects of a Chireix's outphasing amplifier can be complicated. The primary issue is the gain and phase imbalances between the two amplification paths. The typical tolerance for most applications is approximately 0.1~0.5 dB in gain matching or 0.4~2 degrees in phase matching. This is nearly impossible to achieve in most practical situations. Although some advanced calibration algorithms [31], [32] have been proposed to minimize the gain and phase errors, more work in this field must be done before LINC can be readily integrated into handset applications. In a modern implementation, a DSP and synthesizer produce the inverse-sine modulations of the driving signals [8].

1.2.5 Doherty Amplifier

The Doherty technique is one of the most promising efficiency enhancement, or power conservation techniques because of the simplicity of its realization. The Doherty power amplifier was the conception of William H.Doherty of Bell Laboratories, which was originally designed using vacuum tubes in 1936 [33]. One of the interesting aspects of the Doherty configuration is that it uses what would today be termed as an active load-pull technique which is going to be described in the following. The block diagram of a Doherty amplifier is shown in Figure 1.7. It consists of a main amplifier, a peaking amplifier, a phase adjuster (quarter-wave transmission line), and an amplitude attenuator. With phase and amplitude adjustments, output powers from both devices can be combined effectively. The main PA is biased in class B, while the peaking auxiliary PA is biased in class C. When the signal amplitude is half or less (typically 6 dB) than the peak output power (PEP) amplitude, only the main PA is active. Both PAs contribute output power when the signal amplitude is larger than half of the PEP amplitude.

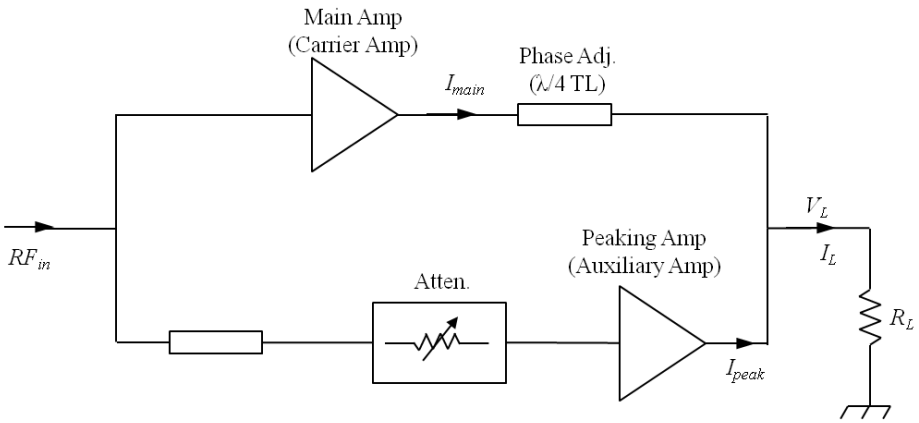


Figure 1.7: Simplified block diagram of Doherty amplifier.

Operation of the Doherty system can be understood by dividing it into low-power, medium-power (load-modulation), and peak-power regions [8]. In the low-power region, the peaking PA remains cut off and appears as an open circuit. The carrier PA, therefore, operates as an ordinary class-B amplifier. The instantaneous efficiency increases linearly with output, reaching the 78.5% of ideal class B at saturation of the main PA at nearly 6 dB from transmitter PEP. As the signal amplitude increases into the medium-power region, the peaking PA becomes active. The additional current I_{peak} sent to the load by the peaking PA causes the apparent load impedance to increase. Transformation through the quarter-wavelength line results in a decrease in the load presented to the carrier PA. This allows to accommodate more current swing (contributed from both devices) while maintaining maximum voltage swing, as shown in Figure 1.8.

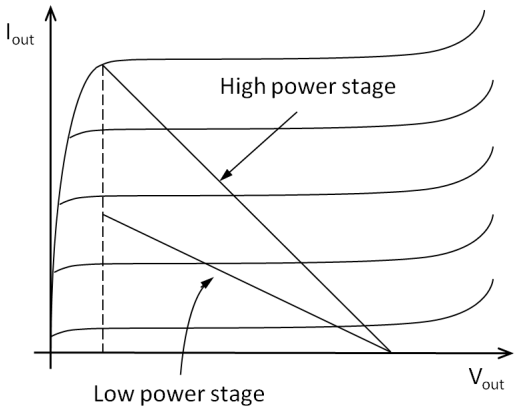


Figure 1.8: Load line diagram of Doherty amplifier operation.

The effective load impedance reduces to $R_L\left(1 + I_{peak}/I_{main}\right)$, where I_{main} and I_{peak} are the currents of the main and peaking devices respectively and they are in anti-phase. This dynamic-load feature is called an active load-pull technique. In the peak-power region, the carrier PA remains in saturation and

acts as a voltage source. It operates at peak efficiency and delivers an increasing amount of power. At PEP output, each PA delivers half of the system output power. It can be shown that under the correct impedance matching conditions, the PEP efficiency in the main device can stay close to maximum efficiency throughout the upper 6 dB of power range.

Note that in active load-pull region, the 'output power' increases in proportion to the 'input voltage' drive level, so that on a linear power scale, a square root characteristic is obtained. Meanwhile, the auxiliary amplifier experiences an upward load-pull effect, so that it generates an output power proportional to the cube of the increasing input voltage amplitude, giving a 'three-halves' power transfer characteristic. These two characteristics combine to give a composite linear power response, as illustrated in Figure 1.9, with close to maximum efficiency being maintained down to the 6 dB back-off point.

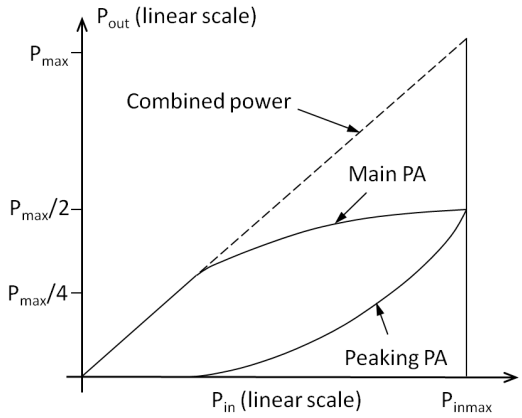


Figure 1.9: Power transfer characteristic of Doherty amplifier.

The efficiency of a two-way Doherty amplifier has been derived by Raab [34], as indicated in 1.6. The detailed derivation is omitted here for simplicity.

$$\eta = \frac{\pi}{2} \frac{\left(\frac{v_{in}}{V_{max}}\right)^2}{3\left(\frac{v_{in}}{V_{max}}\right) - 1} \tag{1.6}$$

where v_{in} is the input voltage and v_{max} is the maximum input voltage. Doherty power amplifiers deliver much better efficiency than Class B power amplifiers. The linearity of the Doherty configuration may be improved by adopting feed-forward or pre-distortion techniques since it is highly nonlinear.

Efforts have been made through the last two decades to enhance the performance of Doherty amplifiers. There is an attempt which has focused on accommodating non-ideal effects (e.g., nonlinearity, loss, phase shift) into a Doherty architecture [35]. Another report shows that it is also possible to use three or more stages to keep the instantaneous efficiency relatively high over a larger dynamic range [36]. The classical power division approximately maximizes the average efficiency for full-carrier AM signals,

as well as modern single-carrier digital signals. The use of other power-division ratios allows the lower efficiency peak to be shifted leftward so that the average efficiency is increased for signals with higher peak-to-average ratios. Doherty transmitters with unequal power division can be implemented by using different PEP load impedances and different supply voltages in the two PAs [37]. In another design [38], a multistage Doherty amplifier, which can be used to achieve higher efficiency at a lower output power level compared to the classical Doherty amplifier, is presented. In modern implementations, DSP can be used to control the drive and bias to the two PAs, resulting in more precise control and higher linearity.

It also has other drawbacks [39] such as gain degradation, intermodulation distortion (IMD), and narrow bandwidth. Gain degradation and IMD are primarily caused by the peaking amplifier. Narrow bandwidth stems from the use of a quarter-wave transmission line as the phase adjuster. Since modern wireless communications utilize a very narrow bandwidth, this is not a serious drawback but some investigations such as [40] are in progress for widening the bandwidth of Doherty PAs.

The gain degradation is caused due to the peaking amplifier. This degradation can be kept low due to the high gain of the carrier amplifier at low power levels. Another major drawback is the intermodulation distortion, which is due to the low biasing of the peaking amplifier. A solution to this issue has been suggested by Iwamoto which involves suitable biasing of the main amplifier leading to the cancellation of the non-linear products [41]. Another well-known issue that can be seen from the configuration of a Doherty system is the resistive load matching. A solution has also been published for this problem where transmission lines with offset have been used to load modulate reactive termination [42].

Finally, considering its complexity and efficiency, the Doherty configuration is typically adopted in base station power amplifiers, not for handset applications. However, more recently some efforts has been put by Bumman Kim's group for applying the Doherty technique for the design of handset devices [43], [44].

1.3 Non-linear Power Amplifiers with a Linearization Circuit

As stated before, there are some PA applications where efficiency becomes a secondary consideration, in comparison to linearity. Back-off is the traditional way of meeting linearity requirements in class A amplifiers. Once the output power is reduced from its maximum value, both the amount of amplitude conversions and distortion products is reduced. Unfortunately, the back-off reduces efficiency, making it an unattractive linearization method for amplifiers. Since efficiency and linearity are opposite requirements in traditional power amplifier design, if the goal is to achieve good linearity with reasonable efficiency, some linearization technique has to be employed. The main goal of linearization is to apply external linearization to a reasonably efficient but nonlinear PA so that the combination of the linearizer and PA satisfy the linearity specification. This is demonstrated in Figure 1.10 [45].

Let us assume the IMD3 specification to be -45 dBc. Without linearization, the amount of back-off that fulfils the IMD3 specification would result in an efficiency of approximately 10%. The lower curve presents the linearized IMD3 value, with a same linearity achieved the power amplifier efficiency is better than 20%. In this example, the power consumption of the power amplifier is reduced by more than a factor of two.

In principle, this may seem simple enough, but several higher order effects seriously limit its effectiveness in practice. As an example the calculation above considers only the power consumption of the

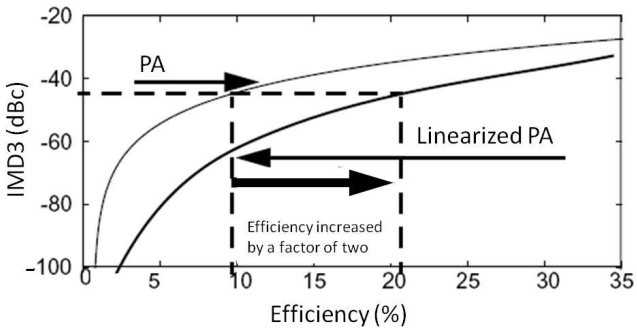


Figure 1.10: Linearity of a PA as a function of efficiency in standalone and linearized configuration.

amplifier, but in reality linearization also consumes a significant amount of power. Let us assume that the output power is compressed by 0.25 dB, which is a typical value for a modern telecommunications amplifier. Now some $10^{0.25/10} - 1 = 6\%$ additional power is needed in the output to restore the power of the fundamental output signal, and an additional 1% is enough for cancelling the approximately -25 dBc IMD3 components. The total additional power needed both to restore the fundamental and to cancel the IMD3 signals is therefore close to 7% of the output power of the PA. Unfortunately, it is large enough so that the efficiency and construction of the linearizer circuitry does matter.

Most PA linearization techniques use the amplitude and phase of the input RF envelope as a template with which to compare the output, and so generate appropriate corrections. It is the way in which the correction is applied which forms the main distinction between different linearization techniques currently in use. A linearizer which applies a corrective signal to the output of the PA will need to generate a significant amount of power to perform its function, but in so doing it will physically increase the peak power capability of the linearized PA. If the correction is applied at the input, it clearly cannot in any way increase the PA peak power. Input correction also poses an additional problem in that the composite input signal will be subjected to the nonlinearities of the PA. This can have some serious consequences, which can significantly reduce the apparent benefits of the linearization process.

The three principal types of linearization techniques are pre-distortion, feedforward and feedback. Predistortion is the generic term given to techniques which seek to linearize a PA by making suitable modifications to the amplitude and phase of the input signal. Feedforward, a technique which has thus far dominated multicarrier PA linearization, applies a corrective signal at the PA output. A feedback loop can also be categorized as a form of input correction. A feedback system, working in a lower signal bandwidth application, seeks to generate a corrective control which is usually applied to the amplifier input signal [1]. On the following, we are going to have a concise review on the three techniques. A brief comparison of the different techniques is presented in Table 1.3.

Table1.3: Comparison of different PA linearization technique.

Linearizarion Technique	Complexity	Performance	Efficiency	Bandwidth	Cost	Comments
Feedback	Moderate	Moderate	High	Narrow	Moderate	stability; reduced gain
Feedforward	High	High	Moderate	Wide	High	not for handset PAs
Analog/RF Predistortion	Low	Low	High	Wide	Low	simplest form; reduced gain
Digital Predistortion	High	Moderate	Moderate	Moderate	Moderate	easy to integrate and control

1.3.1 Predistortion

Predistortion is based on expanding the signal before the power amplifier, so that the predistorter -amplifier pair appears as a linear circuit. In principle, predistortion is a very power efficient and wideband linearization method, although it typically needs a slow feedback to adapt the predistorting function. The basic concept of a predistortion (PD) system (Figure 1.11) involves the insertion of a nonlinear element prior to the RF PA such that the combined transfer characteristic of both is linear.

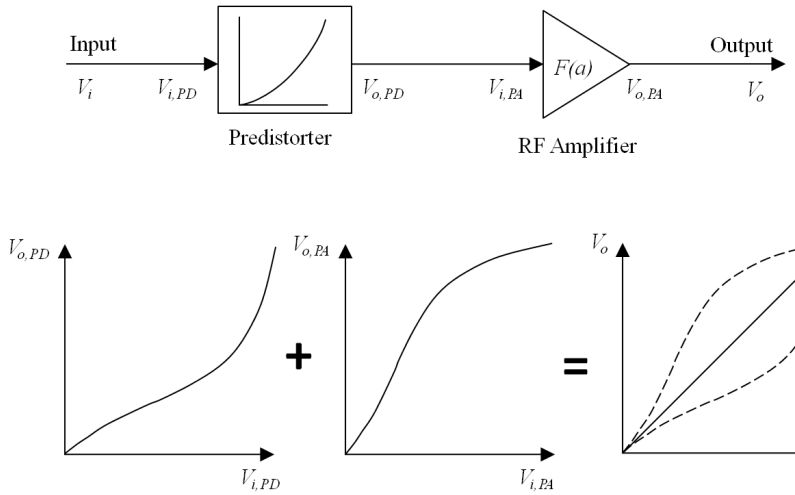


Figure 1.11: Predistortion concept

Predistortion can be accomplished at either RF or baseband [1], [8], [9]. Based on the predistortion frequency, most predistortion systems can be categorized into two groups: analog and digital predistortion. Analog predistortion is typically implemented in the RF/IF frequency, whereas digital predistortion is generally achieved in the baseband domain. An RF predistorter typically creates the expansive predistortion characteristic by subtracting a compressive transfer function (such as that of a diode) from a linear transfer function. Improvements in the Adjacent Channel Power Ratio (ACPR) by

10 dB are typical. The operating bandwidth is limited by the gain and phase flatness of the predistorter itself and of the RF PA. In addition, memory effects in the PA and the predistorter limit the degree of cancellation. Better performance can be achieved with more complex forms of RF predistortion such as Adaptive Parametric Linearization (APL), which is capable of multi-order correction. Most RF-predistortion techniques are capable of broad-band operation [9].

Digital Predistortion (DPD) has become the most active area for PA linearization development and has been made possible mainly through unconnected developments in high speed digital signal processing (DSP) technology. They can operate with analog-baseband, digital-baseband, analog-IF, digital-IF, or analog-RF input signals. Digital baseband and digital-IF processing are most common [8]. Figure 1.12 shows a basic DPD PA system flow chart. Such a system represents the first generation of DPD PA development, and has obvious limitations. It is entirely open loop, and any change in the PA characteristics will rapidly degrade the correction process.

Addition of an adaptation loop in the DPD system enables continuous monitoring of the linearization integrity, and Look-Up Table (LUT) refreshing. It means in effect that the RFPA system has to have its own receiver. For detailed information about analog and digital PD and their algorithms, the reader is referred to [1], [8] and [46].

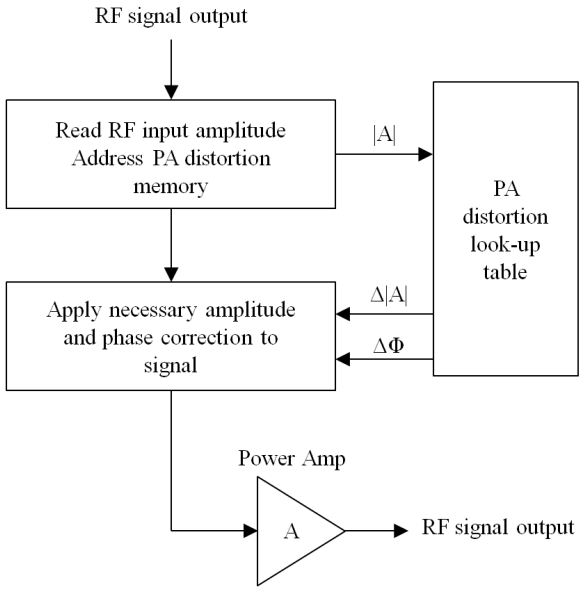


Figure 1.12: Basic digital predistortion system flow chart.

1.3.2 Feedback

The linearity of an RFPA, is defined to be the integrity with which it preserves the amplitude and phase variations of a modulated RF carrier. The negative feedback improves the linearity of the PA by feeding back the sampled output signal to the input and accordingly modifying the amplitude and/or phase of the input signal to the PA.

Judging by the frequency of the signal, feedback can be applied either directly to the RF amplifier (RF feedback) or indirectly to the modulation (envelope, phase, or I and Q components). Broadly speaking, feedback techniques can be broken down into four categories: RF feedback, envelope feedback, polar feedback, and Cartesian feedback. As opposed to the RF feedback, the last three ones are all types of low-frequency feedback. Furthermore, Cartesian and polar modulation feedback are two basic types of the low-frequency feedback and should, more accurately, be referred to as transmitter linearization techniques since each design is a complete transmitter rather than simply a linear amplifier. A brief description of each technique is presented in the following.

1.3.2.1 RF feedback

In RF feedback, a portion of the RF-output signal from the amplifier is fed back to and subtracted from the RF-input signal without detection or down-conversion. The general scheme of RF feedback amplifiers is shown in Figure 1.13. Second order harmonic feedback [47] is one representative example. This technique samples the second-order harmonics at the output of the nonlinear power amplifier and feeds it back to the input of the amplifier.

In principle, the complete cancellation of the IMD3 can be achieved. However, the phase and amplitude adjustment in the feedback path have to be very accurate in order to realize the ideal cancellation. The delays involved must be small to ensure stability, and the loss of gain at RF is a more significant design issue. Besides, the existence of band pass filter in the feedback path limits this technique to narrowband systems. The use of RF feedback in discrete circuits is usually restricted to HF and lower VHF frequencies, but it can be applied within Monolithic Microwave Integrated Circuit (MMIC) devices well into the microwave region [9].

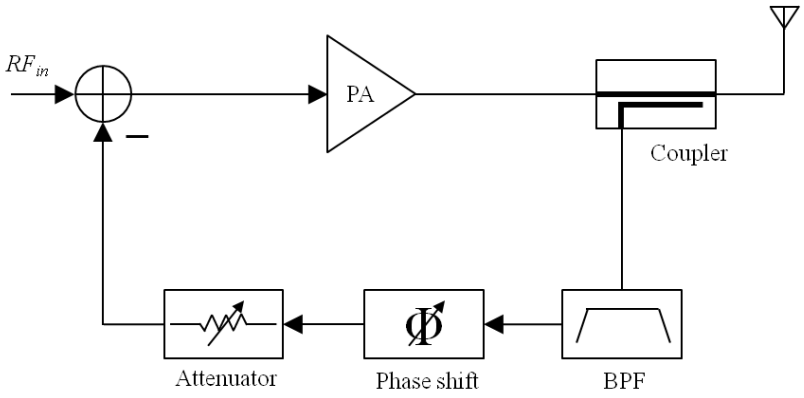


Figure 1.13: Simplified schematic of RF feedback system.

1.3.2.2 Envelope feedback

Envelope feedback reduces distortion associated with amplitude nonlinearity. It can be applied to either a complete transmitter or a single PA. The RF input signal is sampled by a coupler and the envelope of the input sample is detected. The resulting envelope is then fed to one input of a differential

amplifier, which subtracts it from a similarly obtained sample of the RF output. The difference signal, representing the error between the input and output envelopes, is used to drive a modulator in the main RF path. This modulator modifies the envelope of the RF signal, which drives the RF PA. The envelope of the resulting output signal is, therefore, linearized to a degree determined by the loop gain of the feedback process [8].

1.3.2.3 Polar feedback

The polar feedback technique was first proposed by Petrovic [48]. It is in fact a solution for the fundamental inability of envelope feedback to correct for AM-PM distortion by adding a phase-locked loop to the envelope feedback system. Envelope detection and phase comparison generally take place at the IF [8]. The general diagram of a polar feedback system is shown in Figure 1.14.

The sampled output RF signal is down-converted to an Intermediate Frequency (IF) signal by the local oscillator and the mixer. The IF signal is then decomposed into the polar form (phase and amplitude) with a limiter and a demodulator. The same topology is employed to extract the phase and amplitude of the input IF signal. The outputs of two demodulators are fed into an error amplifier to generate the error signal, which controls the amplitude of the RF signal. The phase control path is essentially a simple phase-locked loop (PLL), which includes a phase detector, a loop filter, a loop amplifier, and a voltage-controlled oscillator (VCO). Therefore, both the amplitude and phase of the RF signal can be carefully controlled with independent feedback loops.

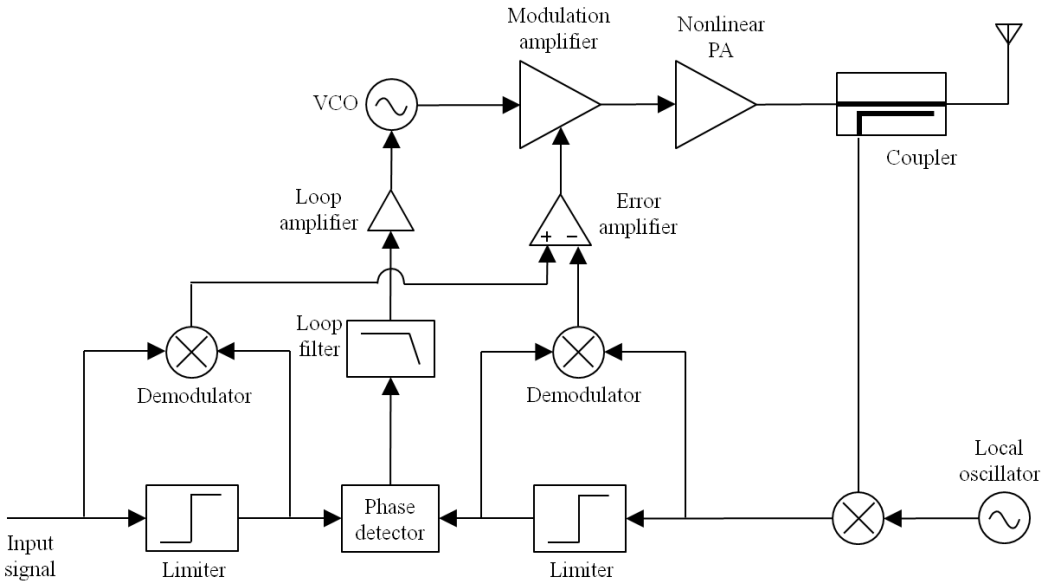


Figure 1.14: Schematic of polar modulation feedback system.

The polar feedback system has a number of advantages. First, the RF path consists of a VCO, a modulation amplifier, and a power amplifier. Since there is no mixer, the issues related to the mixer (such as image-reject filtering) can be avoided. Second, high-efficiency power amplifiers can be employed in the RF path so that the efficiency of the whole system is improved. Several multi-band direct con-

version transmitters in the polar loop topology [49]-[50] have been reported with the RF frequency up to 1900 MHz and spurious emission more than 60dB below the desired RF signal.

On the other hand, several issues limit the application of the polar feedback technique in RF systems. The phase-locked loop may have difficulty in locking at low envelope levels or tracking drastic phase changes. Furthermore, its feedback bandwidth requirement is much higher that of the Cartesian loop to be discussed, considering the phase discontinuity inherent in multi-tone signals in the phase feedback loop [9].

1.3.2.4 Cartesian feedback

The Cartesian modulation feedback technique is a superior form of feedback transmitter which was also first proposed by Petrovic in 1983 [51]. It overcomes the problems associated with the wide bandwidth of the signal phase by applying modulation feedback in I and Q (Cartesian) components. The idea is to I-Q modulate the carrier before power amplification. In this technique, two identical feedback processes operate independently on the I and Q channels. As shown in Figure 1.15, the sampled RF output signal is downconverted into a quadrature (I and Q) feedback signal, which is subtracted from the quadrature input signal to obtain the error signal.

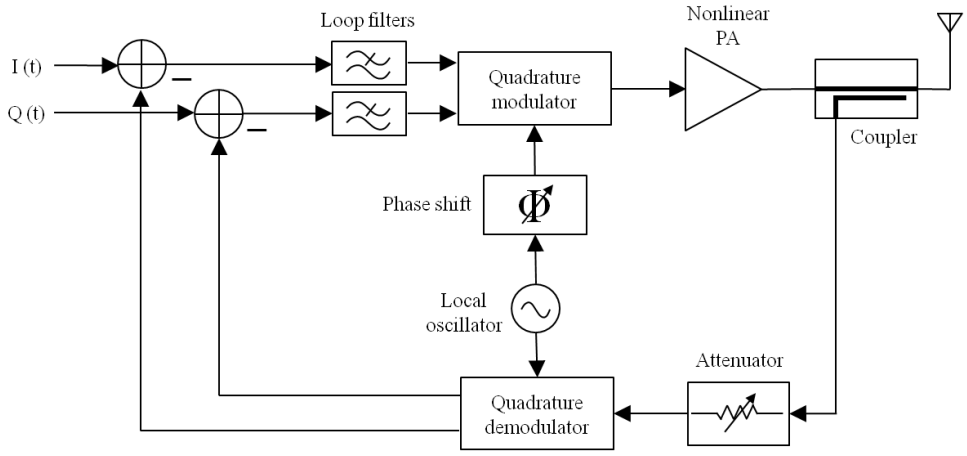


Figure 1.15: Schematic of Cartesian modulation feedback system.

After passing through the loop filters, the error signals are quadrature-up-converted into a complex RF signal to drive the PA. A sample of the output from the PA is attenuated and down-converted in quadrature and synchronously with the up-conversion process. The phase shifter synchronizes the downconversion and upconversion paths and the attenuator is used to adjust the sampled output signal to the proper level suitable for the downconverter. The resulting quadrature feedback signals then form the second inputs to the input differential subtracters (integrators), completing the two feedback loops. In this way, I and Q components can be easily matched unlike polar feedback whose paths are very different making matching difficult. In essence, the Cartesian feedback system is a linearized transmitter rather than a linearized power amplifier. Cartesian transmitter systems [52]-[53] have been reported with more than 20 dB suppression of the IMD3 and up to 500 KHz modulation bandwidth. Since the I and Q components are the natural outputs of a modern DSP, the Cartesian loop is widely

used in mobile radio systems [9]. However, some practical issues need to be addressed in the Cartesian system design. First the synchronization between the upconversion and downconversion paths has been difficult without manual trimming. To solve this historic problem, several automatic phase alignment techniques have been proposed [54]-[55]. However, this further increases the complexity of the whole system.

The loop stability is another issue which is affected by the loop delay [56], as well as by the characteristics of the nonlinear power amplifier [57]. A bigger loop delay will result in a smaller phase margin of the loop transfer function and therefore reduces the loop stability [56]. On the other hand, careful design of circuit components and parameters is critical for stable feedback systems [57].

1.3.3 Feedforward

As with most of the linearization methods, the feedforward technique is not a new idea. It was invented in 1928 by Harold S. Black [58] nine years before the feedback concept [59] in an attempt to linearize telephone repeaters. The concept of feedforward systems is simple, but its hardware implementation is quite costly. Consequently, compared to its feedback counterpart, the feedforward technique is historically less popular. With more awareness of the limitations of conditional stability and loop bandwidth in the feedback systems, the feedforward technique has drawn more attention, especially in the wideband and multi-carrier systems [60]-[61].

Figure 1.16 shows the simplified schematic of feedforward systems. In its basic form, a feedforward amplifier consists of two amplifiers (the main and error amplifiers), directional couplers, delay lines, and some loop control networks. The directional couplers are used for power splitting/combining, and the delay lines ensure operation over a wide bandwidth. Loop-control networks, which consist of amplitude and phase-shifting networks, maintain signal and distortion cancellation within the various feedforward loops [62].

According to the figure, the RF input signal is split through a hybrid splitter into two paths: a main RF path and a signal cancellation path. The distortion generated by the main power amplifier is sampled and fed into a subtracter together with the delayed RF signal. By adjusting the attenuator, the RF signal is completely cancelled out at the output of the subtracter. The residual distortion products are linearly amplified by an error amplifier, and then combined with the distorted RF signal in the main RF path. Ideally, an amplified RF signal without distortion will be generated at the output of the second coupler.

It is actually possible to identify three sub-categories of feedforward PA systems: those which act primarily to linearize the PA at backed-off levels, and usually require the PA to be used below its peak power capability; those which act primarily in a peak power restoration mode; and those which do some of both. The second of these subcategories can be considered to be an efficiency enhancement technique in applications where the signal peak-to-average ratio is very high [1].

There are several practical considerations in the implementation of feedforward systems. The error amplifier [63] must be highly linear, which results in low efficiency topology (e.g. Class A) and limits the total efficiency of the feedforward system [64]. Besides, the phase and amplitude imbalances between the main RF path and the signal cancellation path will dramatically degrade the linearization performance [65]. For instance, a 25 dB distortion suppression requires either an amplitude error of 0.5 dB or less or a phase error of 0.5 degree or less [63]. As a result, extra control must be employed to synchronize both the gain and phase.

It seems that despite the difficulties and challenges, feedforward solutions have thus far dominated the

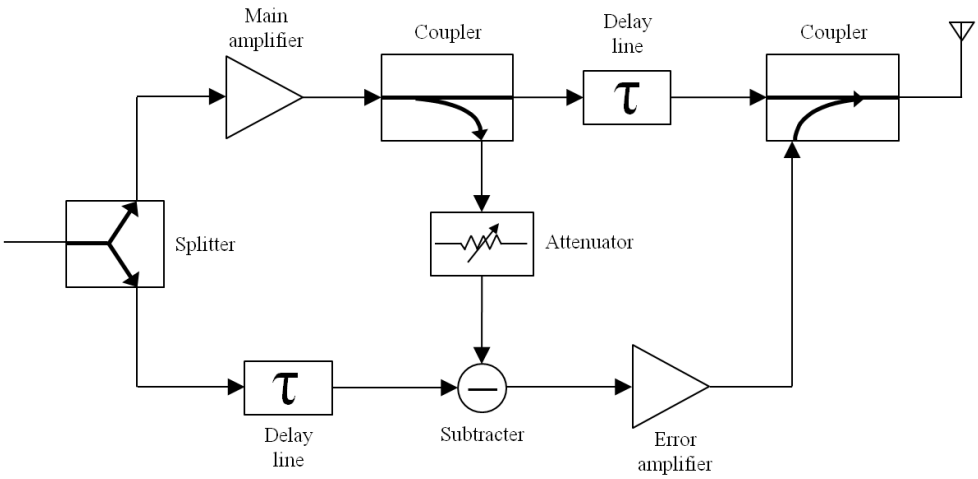


Figure 1.16: Schematic of feedforward system.

mobile communications market. The linearization performance seems to have been such that users have been willing to accept low efficiencies, typically in the 10-15% range for PA applications. With the advancement of digital signal processor (DSP) technology, many digitally controlled feedforward amplifiers have been reported [66]-[67]. However, the implementation of the feedforward technique is so costly that it is employed only in the base-station and satellite systems [68]-[69].

Furthermore, the extra cost of the various couplers, delay lines, and the PA itself all point to a need for an alternative solution capable of higher efficiency and lower cost. Clearly, DPD in principle offers a solution which dispenses with all of these RF components, and only adds about $10 worth of silicon. It would seem that the long reign of the feedforward amplifier may be coming to an end [46].

1.4 Research Objectives and Organization of the Thesis

To increase talk time and battery life, high-efficiency power amplifiers are necessary in handset designs. On the other hand, with the advancement of WCDMA systems, more spectrum efficient techniques need to be applied. This can be attained by complex non-constant envelope digital modulation schemes leading to high peak-to-average ratios that require highly linear amplification. However, the traditional Class AB power amplifiers may not satisfy the stringent requirements for both efficiency and linearity, triggering challenges to devise some methods to improve one parameter without wasting the other. This PhD dissertation also targets this problem.

The major purpose of the thesis is to increase the overall efficiency of a microwave power amplifier by introducing another stage to the structure and change the biases according to the input signal level and based on some key criteria. Moreover, in order to deliver the maximum possible power to the load, the load impedance of the whole amplifier is tuned to the optimum point using tunable matching structure.

Inspired in concept from the Dynamic Bias Switching (DBS) and Dynamic Load Modulation (DLM) techniques as well as Doherty Amplifier, a design methodology is proposed which enhances the efficiency by changing the bias point of an alternate stage as well as tuning the load impedance using a

tunable matching network. The proposed technique can be utilized in mobile communication handsets where linearity and especially efficiency of the amplifiers play an important role in system designs. The key results of the thesis are summarized as follows:

- A new configuration consisting of two FET devices connected in parallel has been proposed. The drains of the transistors are directly connected while the gates are ac-wise connected so that different gate biases can be applied to each device. In this way, we are able to create large-signal IMD sweet-spots by maintaining the gate bias of one of the devices in a specific range determined by two-tone load-pull analysis in the first step of the design.
- A new computer aided design methodology is proposed based on load-pull analysis. First the biasing range of the transistors are found, following by spotting the optimum load impedances where either the amplifier can deliver maximum power or maximum efficiency can be achieved. We have made use of an important fact that the optimum load point moves on the Smith chart according to the input power and gate bias voltages necessitating design of Tunable Matching Network (TMN). In this stage a number of so called *operating states* are chosen among a bunch of options in order to fulfil some specific requirements.
- A varactor-based TMN is designed which not only plays the role of matching network but also is designed to enable the on-board load-pull analysis. This is due to unavailability of external load-tuners. Since efficiency is an important factor in our design, the loss-factor of the TMN is of prime importance which needs to be considered in design of TMN.
- An integrated design of the main amplifier together with its input and output tunable matching networks has been presented and simulated using harmonic balance simulator engine of the Agilent ADS. The circuit was fabricated and the analyses were verified by the experimental results.

This dissertation consists of five chapters which are organized as follows:

As studied earlier, at this introductory chapter, efficiency and linearity requirements of the modern wireless communication systems were discussed and the trade-off between these two contradicting requirements was highlighted. Two main techniques available in the literature for bringing up the two parameters together were studied in §1.2 and §1.3.

Following that in Chapter 2, we will investigate tunable matching techniques in general. First an introduction of the load-line theory and optimum load tuning mechanism for delivering the maximum power to the load in contrast to conjugate matching to provide maximum power gain will be presented. Subsequently in §2.3, a brief description of load-pull analysis and the resulting load-pull contours are demonstrated. Different techniques for providing tunability in matching structures are studied later and among those the varactor-based TMNs are investigated separately in §2.5.

Chapter 3 is dedicated to the detailed description of our design. It begins with the introduction of intermodulation sweet-spots and explains the conditions under which a small-signal or a large-signal sweet-spot may be created in IMD response of an amplifier. It follows in §3.3 by the presentation of our circuit configuration and design methodology based on a two-tone load-pull analysis in order to find the range of the gate bias voltages as well as the optimum load impedances. In the next section, the design of varactor-based load-pull analysing circuit which is also utilized as the tunable output matching network is presented. The chapter ends with the illustration of the harmonic balance simulation results which reveals the final performance of the amplifier in terms of power added efficiency, power gain, VSWRs, bandwidth and intermodulation behavior.

Chapter 4 presents the measured results of the fabricated amplifier with its tunable input and output matching networks. Key design parameters, such as PAE, power gain, and IMD will be presented.

Chapter 5 concludes the dissertation with a summary of this work. Future directions are discussed in the field of high-efficiency and high-linearity power amplifiers for advanced handset applications.

CHAPTER 2

TUNABLE MATCHING TECHNIQUES

2.1 Introduction

As stated in the previous chapter, the PAs suffer from efficiency degradation at reduced drive levels. Various techniques, such as Envelope Tracking, outphasing method and Doherty amplifiers have been proposed to improve PA's efficiency under low power operation or power back-offs. However, envelope tracking approach needs efficient envelope amplification, adding to the overall power consumption. Doherty amplifier implementation requires multiple devices and extra dividing/combining circuits, which adds to the cost, size, and circuit complexity. Another technique that address the efficiency in the back-off mode is dynamic biasing or regulation of the supply voltage of the output stage. But dynamic biasing provides only modest improvements in efficiency, and supply voltage regulation requires an efficient DC-to-DC conversion, again increasing system cost and complexity.

Comparatively, an alternative for improved efficiency is load-line adjustment as a function of output power using an adaptive or reconfigurable output matching network. This method known also as Dynamic Load Modulation (DLM) has been demonstrated as an effective substitution and recently has gained a lot of interest [70]-[75]. It utilizes tunable output matching networks (OMNs) with preferably passive tuning components that consume negligible dc power and can be designed as a part of the OMN. Moreover, the DLM technique has also been proposed at transmitter-level [76], [77], where the Tunable Matching Network (TMN) is controlled by the baseband signal, generated and predistorted by the DSP module.

This chapter will begin with an overview of load-line theory and explain why an improved efficiency can be achieved by tuning the load impedance. Following that, an introduction to load-pull analysis and various load-pulling techniques will be presented. Then, different schemes available in the literature for providing reconfigurability in load values and hence creating a TMN will be discussed. And finally, varactor-based TMNs will be investigated in more detail.

2.2 Load-Line Theory

2.2.1 Gain Match and Power Match

Impedance matching is the most crucial stage in RF power amplifier design because without that no power would be transferred to the load. Generally there are two types of load matching: gain (conjugate) match and power match. In the first type, as the name implies, the goal of matching is

maximizing the power amplifier's gain while in power matching the transfer of maximum power to the load is targeted which does not necessarily lead to the maximum gain, as will be described.

Figure 2.1 shows the power transfer characteristic of a Class A amplifier with two different output matching conditions. The solid line shows the response for an amplifier which has been conjugately matched at much lower drive levels. The two points A and B refer to the maximum linear power and the 1 dB compression power, respectively.

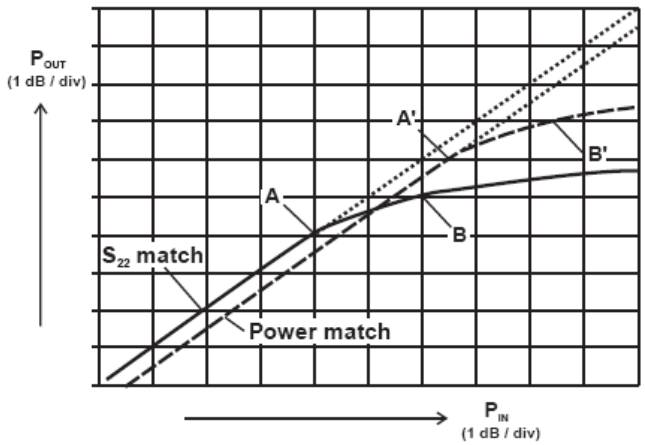


Figure 2.1: Compression characteristics for conjugate match and power match [1].

It has become something of a standard in the RF amplifier community to use the 1 dB compression point as a general reference point for specifying the power capability of an amplifier or an amplifying device (transistor). It also represents a practical limit for linear operation. The 1 dB compression point actually represents a moderate, rather than a weakly nonlinear point. So in linear PA design it is primarily focused on point A, which represents the point at which nonlinear behaviour (gain compression) can initially be detected [1].

In a typical situation, the conjugate match would yield a 1 dB compression power significantly lower than that which can be obtained by the correct power tuning, shown by the dashed line in Figure 2.1. At both points A and B, the device would be delivering 2 dB lower power than the device manufacturers specifications. Unfortunately, power transistors are often the most expensive individual components in a system, and such wastage of performance can be translated directly into unnecessary cost. So the power matched condition has to be taken seriously, despite the fact that the gain at lower signal levels (i.e., the lower left-hand corner of Figure 2.1) may be 1 dB or so less than the conjugate matched condition. The two power sweep measurements of this figure indicate that there is some kind of functional relationship between output power and output match which actually leads us to the load-line theory to be described next.

2.2.2 Optimum Load Matching

As the starting point for this analysis of an RF power amplifier consider a heavily idealized device model, shown in Figure 2.2. This is an ideal nonlinear transconductive device, represented here as a

voltage controlled current source with zero output conductance and zero turn-on voltage. The transconductance is linear except for its strong nonlinearities represented by pinch-off and hard saturation at I_{max}. This is the maximum current the device can handle, and hence will be a limiting factor of the output power. A second limiting factor is the maximum drain bias voltage (V_{DC}). The maximum voltage supplied to the drain might be limited by the available power supply or the breakdown voltage of the transistor itself.

A key feature of this analysis is that the device is never allowed to breach these limits of linear operation; in this sense the analysis is valid up to, but not beyond, the onset of gain compression. An important detail is that although the transistor is being considered as an ideal voltage-controlled current generator, the RF load may have a reactive component, but any output parasitics of the transistor will be considered to be part of the external load.

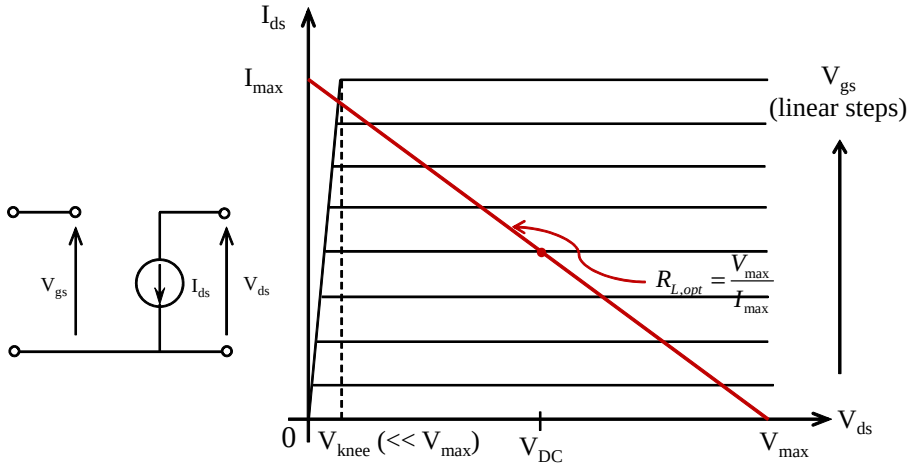


Figure 2.2: Ideal nonlinear device model for optimum load explanation.

Now take, for example, a case where the current generator can supply a maximum limiting current of 1 Amp, and has an output resistance of 100 ohms. Applying the conjugate match theorem, a load of 100 ohms would be selected for maximum power transfer. But the voltage appearing across the generator terminals would be 50 V. Since the current generator is the output of a transistor, this would exceed the voltage rating of the device. As stated before, there is an additional restriction in that the transistor voltage swing is limited by the available DC supply. To an outside observer, only able to observe the power (but not the voltage or current waveforms) in the load resistor, the device would therefore show limiting action at a current considerably lower than its physical maximum of I_{max}. This is clearly an undesirable situation; the transistor is not being used to its full capacity, or efficacy.

To obtain the maximum possible output power, both the voltage and current swing must be used to its full values. The current swing goes from zero to I_{max}, and the voltage swing from zero to $V_{max} = 2V_{DC}$ since the voltage is symmetric about V_{DC}. Hence, in order to utilize the maximum current and voltage swing of the transistor, a lower value of load resistance would need to be selected. This is known as the *load-line theory* which states that the maximum power that a given transistor can deliver is determined by the power supply voltage and the maximum current of the transistor. The optimum value is commonly referred to as the load-line match load, $R_{L,opt}$ and in its simplest form would be the

ratio

$$R_{L,opt} = \frac{V_{max}}{I_{max}} = \frac{2V_{DC}}{I_{max}} \tag{2.1}$$

The available output power at optimum load impedance would be

$$P_{L,opt} = \frac{V_{DC}}{\frac{I_{max}}{2}} = \frac{1}{2} V_{DC} I_{max} \tag{2.2}$$

It is worth noting that the peak RF voltage of $2V_{DC}$ arises primarily from the symmetry of the assumed sinusoidal waveforms. An RF waveform that is symmetrical about its mean level has to rise to a peak voltage of twice the DC supply in order to remain above zero on the downward part of the cycle. It can be shown that when the waveforms become asymmetrical due to harmonic content, the peak voltages can be greater (or less) than $2V_{DC}$. Also for non-ideal transistors, due to the non-zero knee voltage as shown on Figure 2.2 the actual amplitude of the voltage waveform is less than V_{DC}. So In calculations of $R_{L,opt}$ for non ideal transistors V_{DC} may be substituted by $V_{DC} - V_{knee}$ for greater accuracy.

It is also important to note that the optimum load has been derived at the terminals of the transistor current generator or the intrinsic drain of the transistor. Since this is the point where the drain voltage drives a current into the output network and thus, where the power is generated. We need to transform this result to the output soldering tab of the packaged die. The device output capacitance, bond-wire inductance, and the package parasitics have to be taken into account at the outside terminal in order to present an impedance which maps onto the original optimum one. This is the very reason that makes the calculation of the exact location of the optimum load a tedious or even impossible task necessitating the use of circuit simulators or measurements.

2.3 Load-Pull Analysis

Under linear conditions a device characterization performed in terms of scattering parameters is an adequate device representation. Nevertheless, the effectiveness of such a representation fails when describing the circuit behaviour under large signal operating conditions. In the latter case, nonlinear phenomena arise in the active device, generating harmonic distortion, intermodulation, Adjacent Channel Power Ration (ACPR) and many other nonlinear effects. Moreover, device performance strongly depends not only on the bias point but also on the power at the input port (i.e. the level of the driving signal). In this context, the techniques that quantitatively characterize the device performance versus both the source and/or the output loads are referred to as source- and/or load-pull techniques [78].

The load-pull analysis therefore is to vary the load value of an actual transistor or a Device Under Test (DUT) to determine the optimum load which results in peak output power at different input driving stimuli. As the first step in RF PA design, load pull measurement with real transistors or in a simulated environment is a powerful method of finding optimum conditions. The simulated environment has also an advantage hard to realize in reality. This is the possibility to terminate individual harmonics with arbitrary impedances.

The load-pull analysis is performed by measuring delivered power and drain efficiency or PAE at a large number of load impedances represented by points on the smith chart. The results are then usually reported on a Smith chart as the contour level curves for the selected parameter (i.e. constant output power, or efficiency, or IMD, etc.). By inspection of these contours it is possible to find the peak values of output power and efficiency and their respective impedance points. It should be noted that the points of optimum efficiency found by load-pull analysis are only optimum for that particular measurement setup. Changing a parameter such as drive power or biasing conditions will give a new set of optimum points.

Load-pull data gives the designer a well-defined impedance design target, on which to base the strategy for suitable matching network design. It apparently converts an intractable nonlinear problem into one which can be attacked and solved using linear techniques and even linear simulators. The load-pull test seems likely to continue to provide the basic measurements required to derive and fine-tune nonlinear models for RF power devices. The usefulness of the source/load-pull analysis on other typical applications like the mixer design [79],[80], as well as the oscillator characterization and design [81]-[83], is also widely appreciated. Moreover the source pull characterization, even if performed at small signal levels, has important applications in low-noise amplifier design, allowing device noise parameter identification, while applying different source impedance loading conditions [84],[85].

Figure 2.3 presents a typical set of load-pull data. The results show closed *contours*, marking the boundaries of specified output power levels. For most practical purposes, the PA designer is mainly concerned with the 1 dB and 2 dB contours, these representing levels relative to the maximum or optimum power output of the device at the test frequency. The most obvious observation in looking at the data in Figure 2.3 is that the constant power contours, plotted on a Smith chart, are not circles. Unlike noise and linear gain circles, they resolutely refuse to display a circular profile, no matter how carefully the equipment is calibrated. This was assumed to be a manifestation of nonlinear behavior, but note that the contours are still roughly the same shape, even if the criterion for power measurement is shifted to the maximum linear power (i.e., points A, A' in Figure 2.1) [1].

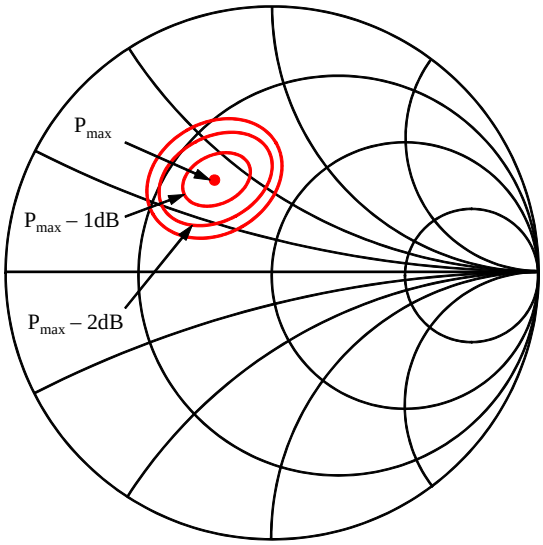


Figure 2.3: Typical load-pull contours.

In its simplest form, a load-pull test setup consists of the device under test with some form of calibrated tuning on its output. The input will probably also be tunable, but this is mainly to boost the power gain of the device, and the input match will typically be fixed close to a good match at each frequency. Some kinds of RF transistor, particularly bipolar transistors, show significant dependency between output power and input load [1].

In terms of categorizing the different load pull strategies, several classifications are possible. There are different approaches to properly change and control the loading conditions to be presented to the active device, which can lead to a first classification in two classes [78]: in the first one, namely *passive* load pull, the impedances are changed by using passive networks having variable passive components, like multiple stubs or slug tuners. In the second one, namely *active* load pull, an auxiliary signal, usually somehow related to the same test source, is used to properly generate a given load (or reflection coefficient).

As a further classification, accounting for the nonlinear behaviour of the active device, and thus the resulting harmonic generation phenomena, the load pull can be carried out at the fundamental frequency only (i.e. controlling the loading conditions at the carrier frequency only), or at the carrier and harmonic frequencies (harmonic load pull), i.e. controlling the loading conditions also at one or more harmonic frequencies of the carrier. To complete such a very rapid classification, a further feature (normally used in order to identify the methodology to be adopted when measuring the required figures) is based on the use of scalar or vectorial techniques and measuring instruments. In the first case, in fact, power meters (PM) and/or spectrum analysers (SA) are usually adopted, while in the latter, a network vector analyser (VNA) or a fast sampling scope is mandatory. Clearly also the calibration techniques to be adopted in the two cases are different, together with the resulting accuracy for the two set of strategies (higher for the vectorial approach) [78].

Detailed investigation of different load-pull techniques can separately be a new subject for a research which is totally beyond the scope of this dissertation. In the next chapter, our own load-pull measurement setup developed just for our PA design purposes will be presented. The interested reader can be referred to [1] and [78] for further information about different load-pulling methods.

2.4 Providing Tunability in Reconfigurable Matching Networks

As stated in the previous section, using load-line theory maximum power efficiency in PA design can be achieved over the input drive variation if the load resistance presented to the transistor is adjusted to the optimal value according to the input power level. This finding leads us directly towards the ways of devising the mechanisms for providing tunability in the implementation of matching networks. This so called power-adaptive tunable output matching network, which presents different load impedances at different power levels, can therefore be used to enhance the overall PA efficiency. Historically, tunable matching networks have been extensively introduced and utilized in RF circuits nearly from the beginning of 21st century.

Different configurations were proposed in the literature using a variety of tunable components in different technologies. In the following, some of the common techniques and their advantages and drawbacks are presented. In a hybrid technology, such as lumped surface-mounted and distributed components mounted on a low-loss dielectric substrate, tunability is obtained by PIN diode switches [86], [87], or by continuously varied semiconductor varactors [72]-[74] and [88]-[95]. The advantages of this technology are its practical and economical aspects. The main drawback is the frequency limitation due to packaging constraints, whereas hybrid devices can be designed to work from 100 MHz

to 10 GHz. Furthermore, a compromise has to be found between frequency and maximum power: in [92], an impedance tuner could operate at a maximum power of 16 dBm up to 5 GHz, whereas in [86], the maximum power was 40 dBm at 400 MHz.

Semiconductor devices have small tuning delays depending primarily on electron mobility. Minimum circuit dimensions are determined by the sizes of the surface-mounted components. Thus, even if distributed components are replaced by lumped ones, the dimensions are still of the order of 1 cm. Integrated circuit (IC) technology can drastically reduce the size of lumped components to the order of 1 mm [84], [96]. The tunability is obtained as in hybrid technology with the additional ability of using switching transistors. Distributed components are usually inconvenient for RF networks, not only because of their size, but also because losses can be excessive, particularly if not fabricated on low-loss substrates such as float-zone silicon or silicon-on-insulator. In such cases, insertion loss can exceed 10 dB [84].

In classical CMOS technology, transmission-line quality factors are very low (approximately 5-10) because of metal and dielectric losses. Impedance matching networks have been demonstrated at frequencies from 1 GHz [96] to 20 GHz [84]. Higher frequency networks are hard to design because of dielectric and metal losses. The main advantage of this technology is fabrication by a standard CMOS process. In addition, research advances can be easily and rapidly transferred to industry.

Micro-Electro-Mechanical System (MEMS) devices have been used in applications from 5 to 110 GHz. With MEMS, the tunability is obtained by adjusting a varactor [97]-[99], or switching [100]-[104]. With a relatively low loss and low nonlinearity, MEMS are especially suitable for moderate and high power devices. They are also useful in low-loss applications, and work at higher frequencies than components in other technologies. However, disadvantages of MEMS include limited life because of mechanical wear, high control voltages (typically 20-40 V), and large delays of the order of microseconds. This technology is also relatively expensive and packaging remains a challenge.

There are some papers about implementing tunable matching networks using tunable transmission lines [105], [106]. Ferroelectric varactors have also been investigated by several groups [107]-[110]. A variation of the static electrical field causes a variation of the permittivity, and thus, of the capacitance. A maximum input power of 33 dBm at 1.95 GHz is claimed in [108]. The output power of the third-order intermodulation (IMD3) intercept point reaches 52.8 dBm for 1 MHz of offset between the two inputs at 1.95 GHz. However, the insertion loss of 1 dB is significant. The main disadvantage is that the bias voltage has to be of the order of tens of volts, such as 30 V in [110] and 100 V in [108]. In [107], [108], and [110], ferroelectric varactors were reported on RF substrates, respectively, FR4, RT Duroid 6002 and RO3003. Consequently, the size of the complete network is near that of a hybrid semiconductor version.

Considering the practicality and ease of implementation of tunable matching networks using variable capacitors or varactors, we are also going to design the TMN of our amplifier utilizing varactors. Hence, I found it useful to dedicate a separate section for describing varactor-based TMNs in more detail.

2.5 Varactor-Based Tunable Matching Networks

A varactor diode is a P-N junction diode that changes its capacitance and the series resistance as the bias applied to the diode is varied. The property of capacitance change is utilized to achieve a change in the frequency or the phase or in our case the impedance of an electrical circuit. Since the varactors

are normally implemented by reversely biased diodes with no need for significant driving power and varactor control signal is essentially a baseband voltage signal, no significant driving power is required for the tunable matching network. The baseband control signal to the varactors can, therefore, be very wideband without any efficiency degradations due to the driving circuitry. This inherent wideband potential of the varactor-based DLM makes it very promising in transmitter architecture for modern communication signals such as multi-carrier WCMDA which has not only a high PAR but also a wide bandwidth.

In 1997, Sinsky and Westgate studied a tunable matching network consisting of varactors and a quarter-wavelength impedance transformer [89]. But varactor-based TMN as the main building block of the more general subject of Dynamic Load Modulation, proposed by Raab for linear and efficient power amplification of signals with high envelope variations [70], [71]. In this technique, the load impedance of the RF power transistor is varied dynamically according to the signal amplitude.

However, design of varactor-based matching networks for load modulation of high PAs at high frequencies requires special design considerations, which are rarely presented in any previous publications. Nemati et al. for the first time in [74] discuss these high power design issues and present a high efficiency load modulation architecture for peak output power levels and frequencies more than 5 W and 0.9 GHz, respectively.

According to [74], feasibility of a varactor-based tunable matching network for high power high frequency applications is dependent on varactor technology and circuit design considerations. Within the general family of tuning varactors, there are several major categories, each designed for particular consideration of application and cost. The most important requirements for the varactor technology are low series resistance, large capacitance tuning range, linearity, and high breakdown voltage [91].

Moreover, the classical problem related to varactor diodes is their distortion when a modulated signal is applied to their terminals, disqualifying them for linear applications. In [111], however, it was demonstrated that by stacking diodes in anti-series, one can obtain an almost ‘distortion-free’ tunable capacitor. In [72], custom-made silicon-on-glass varactors with a uniform doping profile are proposed in an anti-series configuration to address the linearity requirement for load modulation applications. The breakdown voltage of these varactors is 12 V, which limits their application to low-power handset applications.

Generally, the key electrical parameters guiding the selection and usage of a varactor diode can be considered as:

- Reverse breakdown voltage and reverse leakage current
- Capacitance value and the capacitance-voltage change behavior
- Quality factor Q

Circuit tuning requirements will define the appropriate device capacitance versus voltage curve and specific material doping gradients. The two semiconductor materials generally used are Silicon and Gallium Arsenide. Based on the various material gradients varactors can be categorized in three main groups: Abrupt junction, Hyper-abrupt junction and frequency linear tuning varactors [112]. Since the device of our choice is an abrupt junction diode, it would be helpful in our later design stage to present a brief introduction of these devices.

Abrupt junction varactors are presently the most commonly used products. Thanks to advanced processing techniques it became possible to obtain uniformly doped profiles, which resulted in inverse square root dependence in these diodes. Junction capacitance of these devices can be best described by

$$C_j(V_r) = \frac{C_{j0}}{\left(1 + \frac{V_r}{\Phi}\right)^{\gamma}} \tag{2.3}$$

where V_r is the applied reverse voltage, C_{j0} is the junction capacitance for zero voltage applied, Φ is the built-in or junction potential which is 0.7 V for silicon diodes and γ is the exponent or grading parameter. Considering the package parasitics, a simple equivalent circuit of Figure 2.4 can be utilized at the design stage in which L_s and C_p are parasitic components introduced by packaging and R_s is due partly to packaging but mostly to the limited Q of the junction diode itself. Series inductance, L_s and parallel capacitance C_p are considered constant and are given by the manufacturer for a specific package. Series resistance, R_s, is a function of applied voltage and operating frequency and may be also considered constant. The value used should be taken from the specified maximum value or derived from its Q specification. The Q factor, also known as the figure of merit and the quality factor, is an important parameter for a varactor diode since it determines the frequency limit applicability and loss of the diode.

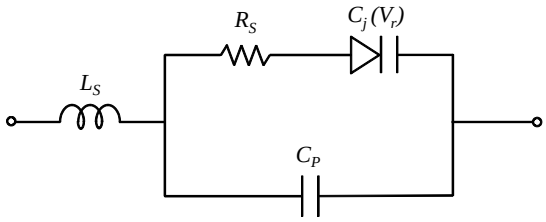


Figure 2.4: Simplified equivalent circuit of the packaged varactor.

The classical definition of the Q of any device or circuit is [113]

$$\mathrm{Q} = \frac{\text{Energy Stored}}{\text{Energy Dissipated}} \tag{2.4}$$

For a series combination of a capacitance and a resistance as for the case of Figure 2.4, the quality factor is defined as

$$\mathrm{Q} = \frac{1}{2\pi f R_S C_j(V_r)} \tag{2.5}$$

where f is the operating frequency. From the above equation it follows that Q is a sensitive function of the applied reverse bias. As this bias is increased, depletion layer expands, reducing the junction capacitance as well as the undepleted resistance. Both of these changes translate into an increase in Q. Also important to note is the dependence of Q on the operating frequency. Historically, the tuning varactor business developed the habit of specifying Q at 50 MHz, in spite of the fact that Q values of microwave diodes are so high that it is impossible to measure them accurately at 50 MHz. However, due to linear relationship, one may extrapolate Q to a different frequency simply by using the reciprocal relationship:

$$Q(f_1) = Q(f_2) \cdot \frac{f_2}{f_1} \tag{2.6}$$

In addition to C_{j0}, Φ and γ which are the main parameters of $C_j(V_r)$ defined by Equation (2.3), some other parameters are also included in the SPICE model of the chip varactor to provide a more trustful nonlinear model for high power applications. As an example in Figure 2.5, typical SPICE parameters of the nonlinear model of a varactor diode used by Agilent ADS together with definitions of some of the parameters are shown.

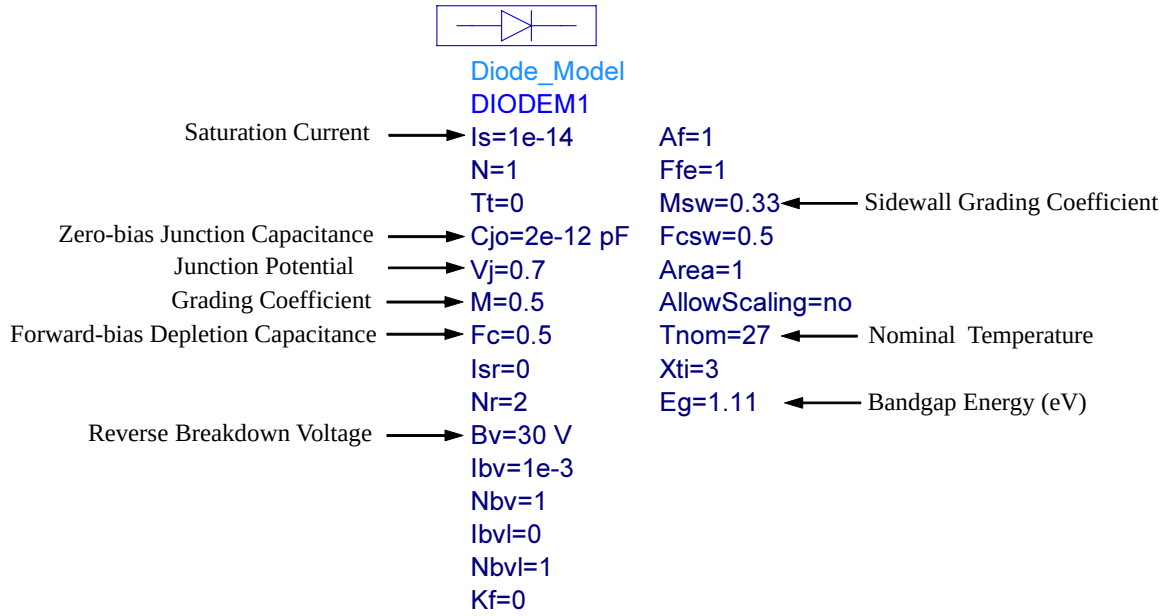
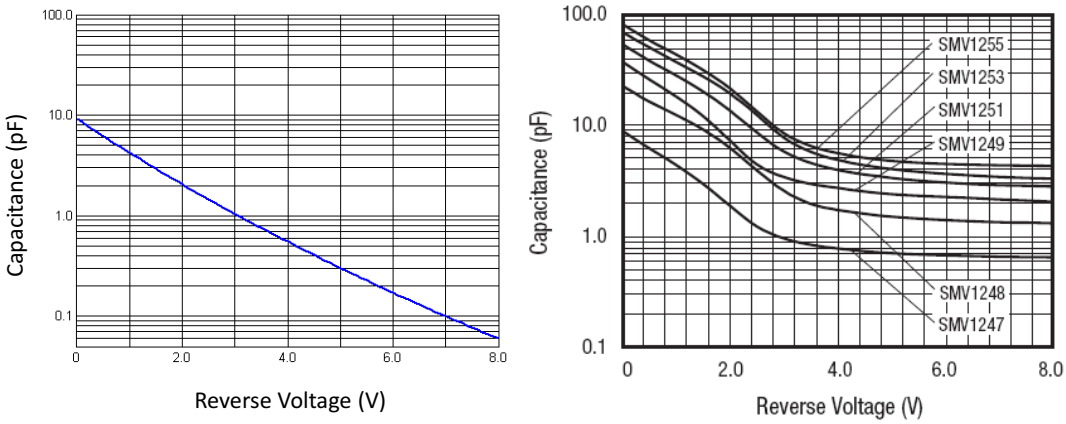


Figure 2.5: SPICE model parameters of a typical varactor diode provide by Agilent ADS.

It is important to note that although the variation of the capacitance with applied reverse voltage is described with Equation (2.3), the real curve of the capacitance versus voltage would deviate from that of the equation due to intrinsic and package parasitics. To give an example, consider SMV1247 which is an hyperabrupt junction tuning varactor from 'Skyworks' with $C_{j0} = 9.22\,pF$, $\Phi = 13\,V$ and $\gamma = 10.5$. The graph of the capacitance as described by Equation (2.3) and the measured results given

in the data-sheet are shown in 2.6. The difference between two graphs is obvious especially at higher voltages where the capacitance-voltage sensitivity decreases more in the actual case.



(a) (b)

Figure 2.6: Capacitance of SMV1247 varactor as a function of applied reverse voltage: (a) equation based characteristic, (b) measured characteristic given by the data-sheet

The varactor model of Figure 2.4 with the parameters of Figure 2.5 is useful for RF VCO and tunable matching applications although it neglects some parasitic components often needed for higher frequency microwave applications, such as the distributed line package model and some capacitance due to ground proximity. For most RF applications, to about 2.5 GHz, these parasitic components would not be important unless higher harmonics generated by the varactor have a considerable effect on the performance of the circuit. In this case, a more detailed equivalent circuit model is needed. The technique used should be based on the varactor model extraction procedure from S-parameter data.

When it comes to the rectifying effect of the varactor diode during a positive voltage swing, most of the times, it is ignored. Because for most RF applications, the lowest practical DC control voltage value is 0.5 V and the magnitude of RF voltage rarely exceeds a peak of 0.2 V. Therefore, the varactor is maintained in its reverse bias state. However, with a large signal application just as for the case of our amplifier it is necessary to consider the rectifying properties of the diode as well. To do that, the turn-on and breakdown of the varactor should be avoided in order to proper behavior and survival of the varactor. In order to avoid the breakdown, the following relation should always hold:

$$V_{RFmax} + V_{BIAS} < V_B \tag{2.7}$$

This increases the minimum achievable capacitance value and consequently, reduces the network tunability. But fortunately since this limitation takes place at the higher voltages where due to exponential relationship, the sensitivity of the capacitance to the variations of the applied voltage is minimum, the reduction in the tunability is negligible. On the other hand, in order to avoid the turn-on and keep the diode always in reverse bias, we have:

$$V_{BIAS} - V_{RFmax} > 0 \tag{2.8}$$

This condition limits the maximum achievable capacitance but unlike the other extreme, this time it has a very severe effect on the tunability because it affects at lower applied voltages where the sensitivity is maximum.

One of the best solutions proposed in the literature for relieving this problem is using two varactors face to face in a structure called *anti-series* configuration as shown in Figure 2.7. With the assumption that the RF voltage is divided equally between two diodes, in the new configuration the limiting constraints of (2.7) and (2.8) would respectively modified to (2.9) and (2.10). This makes a significant difference at the high sensitivity region and solves the problem of lower tunability range of the single varactor which would be present otherwise.

$$\frac{V_{RFmax}}{2} + V_{BIAS} < V_B \tag{2.9}$$

$$V_{BIAS} - \frac{V_{RFmax}}{2} > 0 \tag{2.10}$$

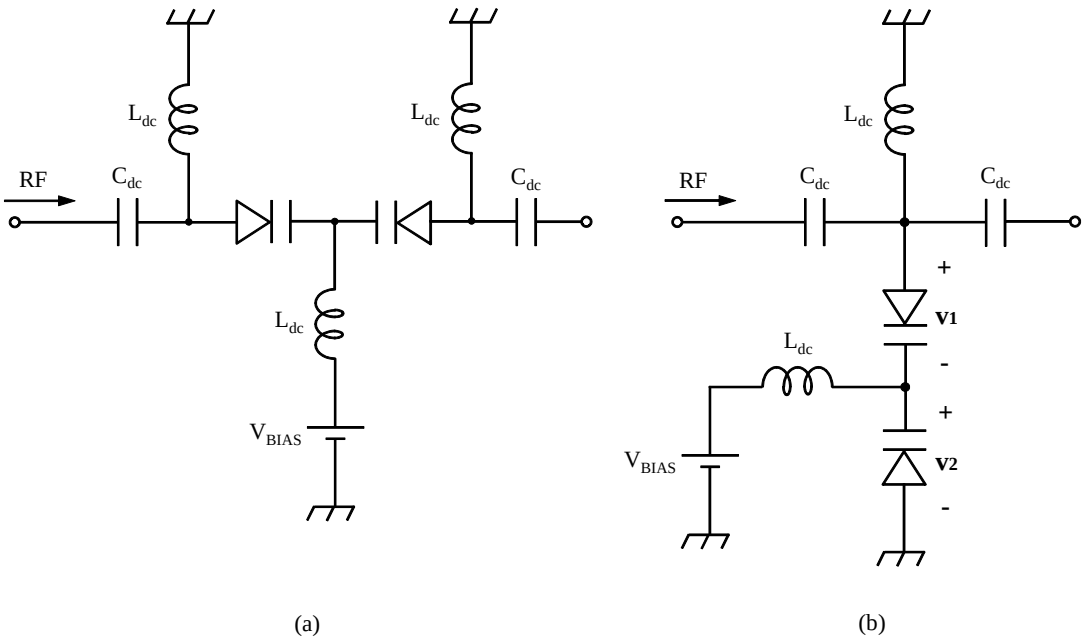


Figure 2.7: Anti-series varactor diode configuration. Varactors can be in (a) series or (b) parallel with the RF path.

In terms of linearity, the anti-series configuration provides an advantage as well. The variation of the varactor capacitor with the 'RF swing' is an undesirable effect, causing nonlinearities and distortion in the signal. According to [114], using the abrupt-junction varactors in anti-series structure would improve the linearity as well as the tunability range. In order to show that, the Taylor or power series expansion of the varactor capacitance described by (2.3) is used as follows [114].

If V_Q is the bias voltage and v is a small fluctuation, by replacing $V_r = V_Q + v$, Equation (2.3) can be expressed as

$$C_j(v) = \frac{C_{j0}}{(\Phi + V_Q)^\gamma} \left(1 + \frac{v}{\Phi + V_Q}\right)^{-\gamma} \tag{2.11}$$

which can be expanded as

$$C(v) = C_0 + C_1 v + C_2 v^2 + \cdots \tag{2.12}$$

where

$$C_0 = \frac{C_{j0}}{(\Phi + V_Q)^\gamma} \tag{2.13a}$$

$$C_1 = -C_0 \frac{\gamma}{\Phi + V_Q} \tag{2.13b}$$

$$C_2 = C_0 \frac{\gamma(\gamma + 1)}{2(\Phi + V_Q)^2} \tag{2.13c}$$

The analysis of the anti-series configuration of Figure 2.7 can again be approached by deriving an equivalent power series for the capacitance of the whole connection. Consider the circuit of Figure 2.7 (b). For each device the power series can be written as

$$C_1(v_1) = K_0 + K_1 v_1 + K_2 v_1^2 + \cdots \tag{2.14}$$

$$C_2(v_2) = L_0 - L_1 v_2 + L_2 v_2^2 + \cdots \tag{2.15}$$

Let v be the total incremental voltage where $v = v_1 + v_2$. It is shown in [114] that the resultant capacitance of the composite common cathode or anti-series connection is

$$C(v) = \frac{1}{P_0} - \frac{2P_1}{P_0^3} v + \frac{3}{P_0^5}\left(2P_1^2 - P_0 P_2\right) v^2 + \cdots \tag{2.16}$$

where

$$P_0 = \frac{1}{K_0} + \frac{1}{L_0} \tag{2.17a}$$

$$P_1 = -\frac{K_1}{2K_0^3} + \frac{L_1}{2L_0^3} \tag{2.17b}$$

$$P_2 = \frac{K_1^2/2 - K_0K_2/3}{K_0^5} + \frac{L_1^2/2 - L_0L_2/3}{L_0^5} \tag{2.17c}$$

For matched diodes (2.16) is written as

$$C = \frac{K_0}{2} + \frac{K_2}{8}\left(1 - \frac{1.5K_1^2}{K_0K_2}\right)v^2 + \cdots \tag{2.18}$$

Equation (2.18) shows that the second-order distortion is ideally zero. The coefficient of v^2 which causes third-order distortion implies two significant effects. First, the factor of $\frac{1}{8}$ arises from the fact that each diode has approximately half the RF voltage across it and thus IMD3 is reduced by $\left(\frac{1}{2}\right)^3$. Secondly, the coefficient has the possibility to be zero if

$$\frac{1.5K_1^2}{K_0K_2} = 1 \tag{2.19}$$

Replacing K_0, K_1 and K_2 using (2.13) results in the value of $\gamma = 0.5$. It means that, in the anti-series connection of varactors if γ is exactly equal to 0.5 (corresponding to an abrupt doping profile), then IMD3 will be theoretically zero.

There is also a conceptual explanation about the reason of reduction of the third order non-linearity in anti-series configuration of varactor diodes. According to Figure 2.7 (b), although both of the varactors are DC biased at the point of their common cathode, the instantaneous RF voltage swing on two diodes are in the reverse direction as shown in Figure 2.8. It means that while the instantaneous capacitance value is increasing due to decrease in biasing voltage of one device, the capacitance of the other device is decreasing due to increase in its biasing voltage. This changing of the capacitances on the opposite direction has the effect of reducing the non-linearity and hence the third order intermodulation terms introduced by the varactors.

However, the story does not end here. Connecting two capacitors in series on the other hand, if not halve but decreases the total capacitance seen from the input. At first sight, it seems that this problem can be easily solved by choosing a varactor with a C_{j0} value higher than the initial one. But according to the data-sheet of the varactors, with increasing the C_{j0} of the diodes, the quality factor decreases which results in raising the value of series resistance R_S. This is definitely unfavorable because even an increase of 0.1 Ω in R_S value leads to a considerable amount of reduction in total efficiency of the amplifier.

This problem can be solved by using smaller C_{j0} and hence higher Q but paralleling as much varactors as needed to provide the required capacitance [74], [95]. In this way, a 2×N series-parallel varactor stack can be formed. An example of 2×3 varactor stack is shown in Figure 2.9. Such a stack is

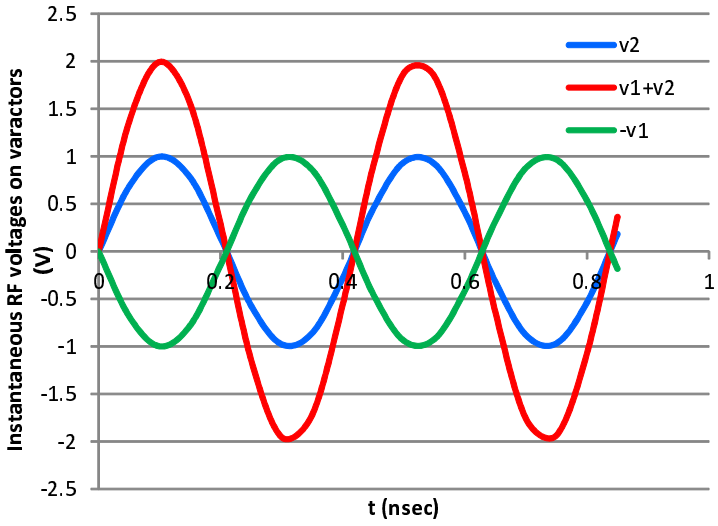


Figure 2.8: Instantaneous RF voltages on the varactors in the anti-series configuration.

equivalent to a single varactor, but with a higher achievable tuning range and increased equivalent breakdown voltage. However, in practice, the implementation of such a stack adds extra parasitics such as connection inductances and should be carefully considered. Monolithic Microwave Integrated Circuit (MMIC) or in-package integration could be a good option to reduce or control the parasitic effects.

The last parameter that should be investigated before finishing this chapter is the loss factor. One of the most important aspects of tuner design is to maximize the power gain or minimizing the loss. The general definition of this gain known as operating power gain (which for the matching network is actually loss rather than gain, just like in mixers) is

$$\begin{aligned} L_P &= \frac{P_L}{P_{in}} = \frac{\text{power delivered to the load}}{\text{power input to the network}} \\ &= \frac{1}{1-|\Gamma_{in}|^2}\,|S_{21}|^2\,\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \end{aligned} \tag{2.20}$$

where Γ_{in} is defined by

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \tag{2.21}$$

For $Z_L = 50\ \Omega$, we have $\Gamma_L = 0$ and from (2.21), $\Gamma_L = S_{11}$. Hence the power loss equation of (2.20) reduces to

$$L_P = \frac{|S_{21}|^2}{1-|S_{11}|^2} \tag{2.22}$$

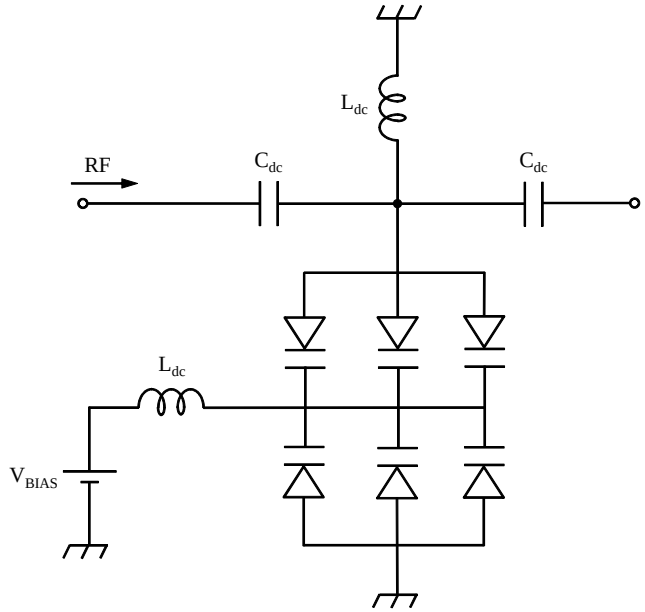


Figure 2.9: A 2×3 varactor stack in parallel with the RF path.

The losses of the tunable matching networks are caused by the limited Q of the inductors and varactors, transmission line losses and the parasitic resistances of the discrete components. In a lossless network, loss factor or L_P is equal to unity and falls below the unity for the lossy networks. Depending on the application, the loss factor is generally preferred to be over -1 dB.

The selection of the TMN configuration and the specific varactor to fulfill the requirements of our design would be based on the material presented in this chapter and is one of the main parts of the next chapter.

CHAPTER 3

EFFICIENCY ENHANCEMENT WITHOUT DEGRADED LINEARITY IN A NEW TOPOLOGY

3.1 Introduction

The design of a power amplifier (PA), as that of any other electronic circuit, is typically partitioned in a series of systematic steps, from the identification of PA requirements up to the final measurements and characterization of the realized circuit, to verify fulfilment of design specifications. The typical design steps are listed in the flow chart of Figure 3.1. Starting from the PA requirements and electrical specifications, the first pass resides in the selection of the technology to be adopted for the design and the subsequent choice of the active device type. The latter is selected according to the targeted application and the required operating frequency. For instance, for low RF frequency and base-station applications, typically LDMOS device are preferable, while for space applications PHEMT GaAs devices are selected for microwave or millimetre wavebands [78].

Referring to the technology, the PA can be realized in hybrid (MIC, Microwave Integrated Circuit) or in monolithic (MMIC, Monolithic Microwave Integrated Circuit) form, depending again on the application, fabrication capabilities and budgetary issues. After proper active device selection, the subsequent step resides in the identification of the preliminary PA architecture required to fulfil the electrical specifications. For moderate to large bandwidths, proper power amplifier design strategies based on load-line concepts are implemented. These strategies are based on the full exploitation of the active device output I-V characteristics, and its nonlinear large signal operating conditions.

The identification of a proper architecture depends on the electrical requirements to be fulfilled as well as the purpose and application of the PA. For example, if the selected device in a single stage structure is not able to provide the required output power and gain level, then a multi-stage solution is sought.

The subsequent step is the identification of the active device bias conditions and matching networks. For this purpose, two possibilities are available, depending on the availability of the nonlinear device model, or the physical availability of the device itself together with characterization setups. In fact, when the device and test-benches are physically available, the best solution is clearly to characterize the actual device through nonlinear measurements. In this case in fact load/source pull techniques are usually adopted to infer the real input and output matching conditions to fulfil the design requirements and trade-offs under large signal operating regimes. Otherwise, the identification of proper loading conditions has to be inferred by using the information available from the adopted active device data-sheet or the nonlinear model provided by the manufacturer. In this phase, several nonlinear analysis tools are commercially available.

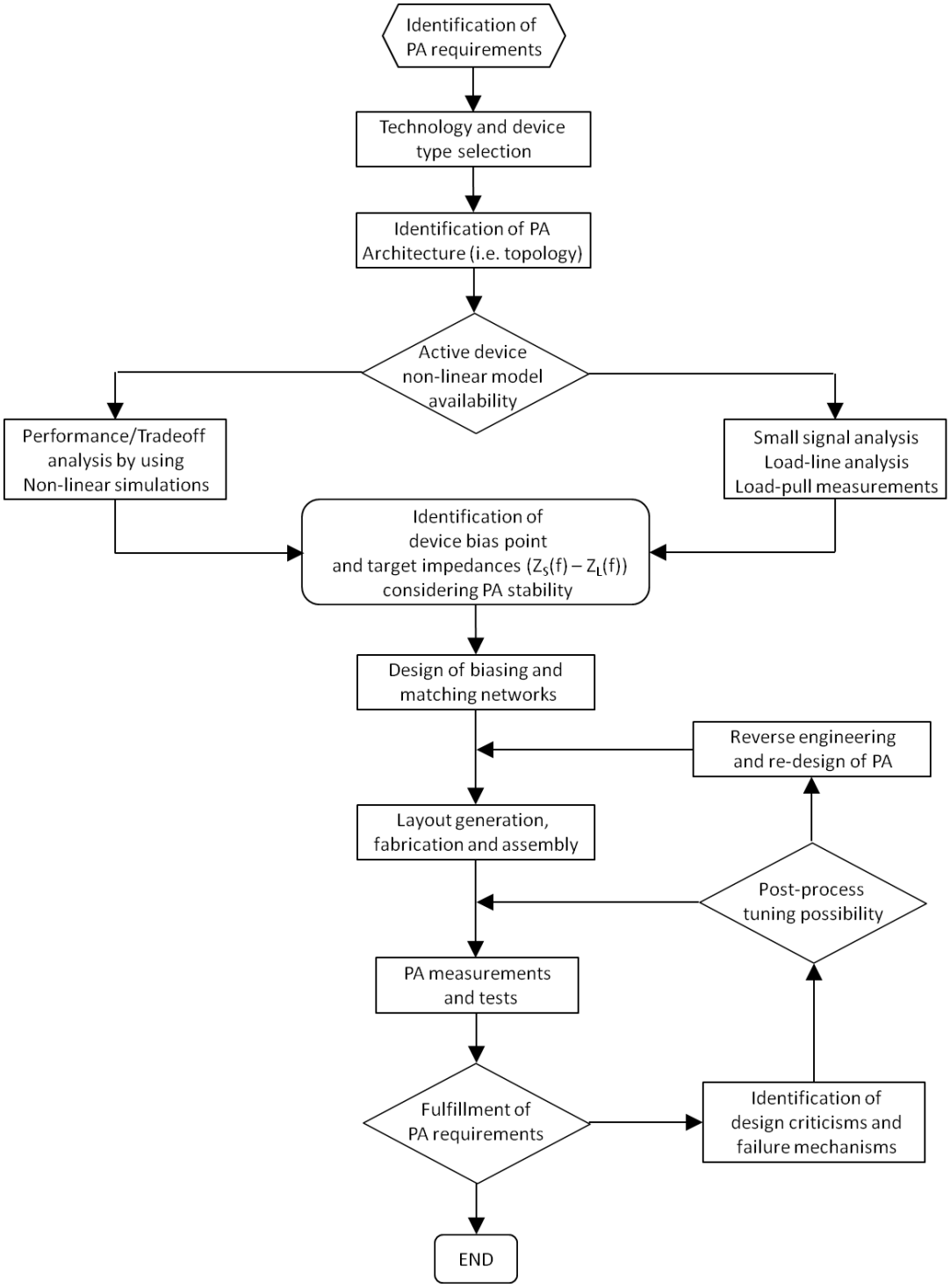


Figure 3.1: Typical design steps for the realization of a PA.

After the identification of the device loading condition, both at the input (Z_S) and output (Z_L) device ports, and their frequency behaviour (including harmonics), providing the fulfilment of stability conditions. From a practical point of view, usually the linear stability conditions only are checked, while the large signal, and thus nonlinear stability conditions, are usually not verified, for the sake of simplicity. The next step is definitely to design the loading networks to implement such impedance values. For the design of the matching networks, both lumped or distributed solutions can be adopted, depending on the available technology and operating frequency. In this step, the preliminary ideal elements (that are chosen to be passive and lossless, e.g. inductances, capacitances and transmission lines) must be replaced by accurate models of their physical implementations. Within simulators they are represented by equivalent circuits, i.e. sub-circuits made up of several lumped/distributed elements.

By replacing the ideal elements with their equivalent-circuit models, one at a time, the designer can accomplish some important practicalities. Moreover, an optimization step can be performed on the remaining ideal elements in order to bring the circuit back within design specifications. At the end of this procedure, a more accurate and realistic circuit schematic is obtained, which has to be transformed into a layout for realization.

Then, electrical tests on the realized amplifier are performed to verify its performance. If the results are not satisfactory, a reverse engineering is adopted to understand the eventual failure mechanism or any design critical point. Therefore, a second run becomes mandatory, consisting in re-designing the matching networks accounting for the information inferred from the tests performed on the first realization [78].

This chapter begins with the introduction of *Sweet Spots* and their role in our power amplifier design. Then a new topology and bias controlling technique for an efficiency enhanced PA design, based on sweet spots will be presented. Following that, a load-pull analysis setup along with the tunable matching network structure to be used in our final amplifier will be introduced. Eventually, the detailed schematic of the designed PA together with the simulation results will be presented and discussed.

3.2 Intermodulation Sweet Spots

Sweet Spots are local minimums in the intermodulation distortion (IMD) curves which occur in the linear region and/or near the compression point of the power amplifiers. Depending on the region of appearance, these minimums or so-called nulls are called small-signal or large-signal sweet spots and each one can exist for a different reason.

One of the best tools introduced in the literature for investigating the behavior of the nonlinearities of power amplifiers is the two-dimensional Taylor series expansion of nonlinear drain-source current (for the FET case) which can be extended to Volterra series in case of the systems with memory effects [115]. Although this kind of behavioral modelling is not the subject of the thesis, just for later referring the two-dimensional Taylor series expansion of the drain-source current is given in (3.1)

$$\begin{aligned} i_{ds}\left(v_{gs}, v_{ds}\right) &= G_m v_{gs} + G_{ds} v_{ds} \\ &+ \frac{1}{2} G_{m2} v_{gs}^2 + G_{md} v_{gs} v_{ds} + \frac{1}{2} G_{d2} v_{ds}^2 \\ &+ \frac{1}{6} G_{m3} v_{gs}^3 + \frac{1}{2} G_{m2d} v_{gs}^2 v_{ds} + \frac{1}{2} G_{md2} v_{gs} v_{ds}^2 + \frac{1}{6} G_{d3} v_{ds}^3 \end{aligned} \tag{3.1}$$

In [116] and [117], Qu and Parker give quantitative expressions for intermodulation in terms of load and the coefficients of the two-dimensional Taylor series expansion the drain-source current. The contribution of the second-order terms in the Taylor series expansion to the third-order intermodulation as well as the contribution of cross-terms to overall intermodulation products are included and investigated. The inclusion of these terms is proven to be significant, especially when the model is used to predict regions of intermodulation reduction that occurs at certain biases and loads. But it should be noted that the given analysis is applicable to weakly nonlinear applications with low-level signals or simply at the small-signal region. Once the device is characterized in terms of its Taylor series coefficients, the bias point and load impedance can be selected to maximize IM performance in the small signal regime.

The second situation is more relevant under large-signal operation, where the first terms of the Taylor expansion are no longer capable of representing $i_o(v_i(t))$ with enough accuracy. This situation is observed for a certain excitation level v_{i0} where the PA large-signal gain versus P_{in} characteristic presents a minimum (or as is more commonly observed, a maximum), and the P_{IMD} (P_{in}) curve shows a sudden minimum. These critical points, usually observed in the PA onset of saturation, provide high signal-to-distortion ratios at high output power and PAE, being therefore very attractive as a linear PA design tool. To distinguish them from the small-signal IMD sweet-spots, obtained at certain bias points and independent of small-signal level, they were called in the literature "*large-signal IMD sweet-spots*". A typical sample of this kind of sweet spot in the IMD3 curve of a power amplifier together with the fundamental output power as a function of the input power is shown in Figure 3.2.

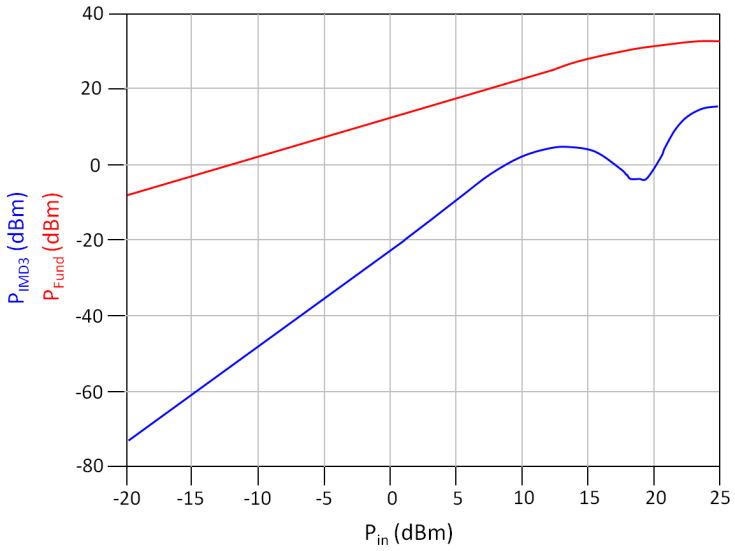


Figure 3.2: A sample of generation of a large-signal IMD3 sweet-spot.

The large-signal sweet-spot phenomena is extensively investigated by N. B. de Carvalho and J. C. Pedro in [118]. In their paper for the first time, they made use of two sinusoidal input describing function (TSIDF) as a tool to describe how large-signal IMD sweet-spots can be created. They separated the i_{out}

equation terms at in-band harmonic frequencies into small- and large-signal contributions and showed that the large-signal sweet spots are generated every time the small- and large-signal IMD components interact with opposite signal phases.

It is found that the optimum bias point for the generation of an IMD sweet spot is one where the small-signal IMD is in phase with the fundamental component. Since, for a large signal, compression mechanisms impose an IMD whose phase tends to oppose that of the fundamental, a large-signal IMD sweet spot will appear in the boundary between these two zones of excitation level. Therefore, as large-signal IMD presents a 180 phase, a distortion sweet spot can be produced by the careful selection of a quiescent point that has an associated 0 phase small-signal IMD. On the other hand, if the bias point selection results on a 180 small-signal IMD, the IMD versus drive pattern will not present any null, but a rapid increase on distortion, close to the 1-dB compression point.

Later on, in another paper [119], de Carvalho et al. showed that provided the device is properly biased, every intrinsic resistive load impedance generates a large-signal IMD minimum. Only the input-power value for which it will be visible will change. The base-band and 2nd harmonic impedances should also be kept under control, if a maximization of the carrier-to-intermodulation- distortion ratio is sought. This is in fact the point that we will benefit from in our tunable output matching network design.

Although it is not practical to make the circuit to operate exactly in the IMD nulling condition due to the sensitivity of nulling phenomena, these results provide guidelines for circuit designers to select the bias and load to position operation in regions of reduced distortion. For any further information about small- and large- signal sweet-spots the interested reader is referred to [120].

3.3 Power Amplifier Design

Ideally, at the terminal of the transistor current source, the optimum load impedance is purely real. However, at the external terminal, the desired load trajectory deviates from the real axis due to the drain-to-source capacitance, bond-wire inductance, and package parasitic effects which become more pronounced as frequency increases. Hence when a transistor package with an accurate model and parasitics is to be used in a design, we have to deal with a lot of feedback elements. These components ultimately encumber the de-embedding process and finding the closed form expressions for the load impedances which delivers the maximum power to the load becomes a tedious task or even impossible, demanding inevitably a Computer Aided Design (CAD) method. Our main goal in this thesis is to present a method to improve the efficiency and linearity performance of a power amplifier by changing the gate bias points of individual transistors of the PA while providing the optimum load at all times using tunable matching network and we are going to do all of this based on a CAD method.

Since the objective of the thesis is to introduce a new configuration and design methodology and investigate its applicability, advantages and drawbacks, rather than designing a commercial power amplifier, our design steps may not sometimes comply exactly with the procedure depicted in flowchart of 3.1. But as we are proceeding, the coverage of nearly all of the steps will be verified.

Considering the fact that our design will be a hybrid circuit with discrete components, the important criterion for the selection of the active device to fulfill our design purposes, was to find a commercially available medium-power transistor for which a large-signal nonlinear model is given by the manufacturer. A second point that I considered is that the transistor should preferably be an enhancement mode FET so that there should be no need for negative bias voltages. That is because the amplifier was intended to have variable bias voltages according to the input power and providing negative variable

biases may complicate the design.

The transistor that we finally chose is ATF-50189 from Avago Technologies [121]. This device is a medium power, low noise Enhancement mode Pseudomorphic HEMT (E-pHEMT), packaged in a low cost surface mount SOT-89 package. Its operating frequency range is from 400 MHz to 3.9 GHz which makes it an ideal choice for general purpose transceiver applications of Wireless Local Area Network (WLAN) and cellular communications. Our design frequency is 2.4 GHz which is one of the operating frequencies of WLAN systems.

3.3.1 Circuit Configuration

For the power amplifiers with tunable matching networks, two main design methods are reported in the literature. One is the separate design [74], [76] which consists of a static PA and a TMN. The PA and TMN are designed and implemented independently as shown in Figure 3.3. This method enables measurement-based characterizations of the PA and tunable matching network, leading to a better design accuracy. However, this independently designed PA-TMN contains more elements than a stand-alone PA, resulting in additional insertion loss and mismatch, as well as an efficiency decrease. Furthermore, the bandwidth is limited to < 5 MHz, due to the interconnecting 50 Ω transmission line between the PA and TMN. Thus, this independent design methodology is not optimal for implementing a broadband PA-TMN.

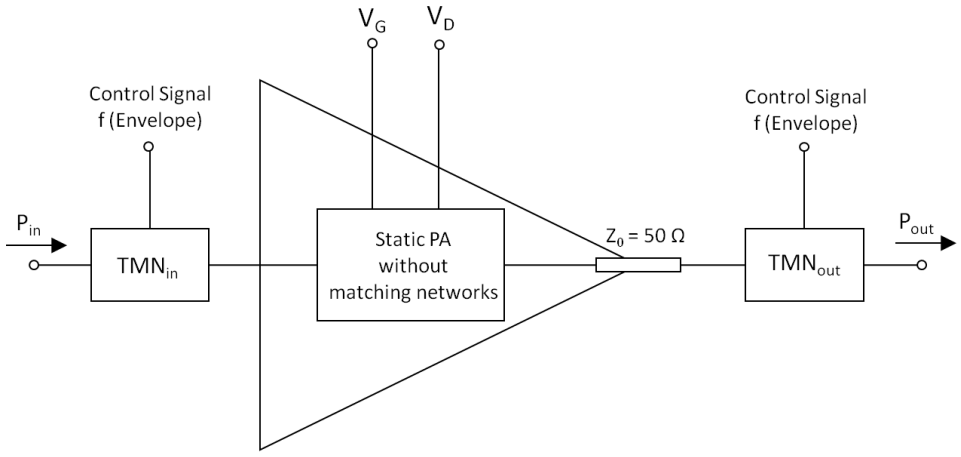


Figure 3.3: Schematic of separate design method of PA-TMN.

Alternatively, as shown in Figure 3.4, the design of PA matching networks and TMN is integrated, achieving a reduced circuit complexity and potential for broadband application. PA designs of [72], [77] and [95] are all examples of integrated structures. In order to minimize the adverse effects of the additional components and transmission lines and hence improving the efficiency, our design approach will also be an integrated one.

For the amplifier part of our design, we initially started with a multi-stage design idea in which more than one transistor were connected in parallel with some kind of switching mechanism at the gates so that with increase of the input drive, successive transistors were pushed into the circuit by switching

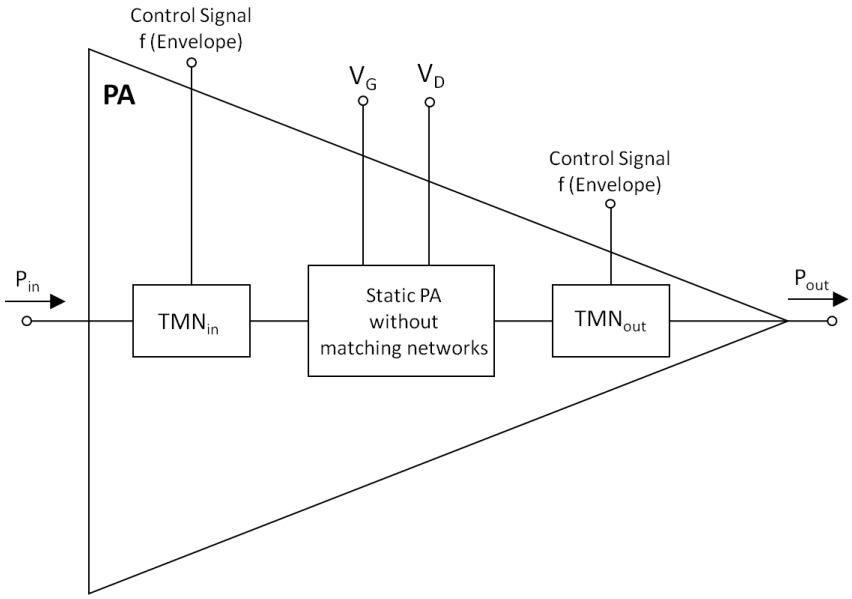


Figure 3.4: Schematic of co-design (integrated) method of PA-TMN.

and hence contributed to the output power. But after trying a lot of configurations including structures with more than two transistors, with and without switches, different kinds of switches and even switches at various points of the circuit, we were finally convinced that the best configuration for fulfilling our objectives is simply a binary structure in which two active devices are connected in parallel without any switches in any part of the circuit.

That is because the addition of any components including a third transistor or any switches would results in a reduction of the overall efficiency of the PA due to non-idealities of the switches at ON and OFF states as well as adverse feedback effects of the extra transistors. A simplified schematic of the designed amplifier is presented in Figure 3.5.

Two main points are worth to highlight about the design. First, according to the figure, while ac-wise connected, two gates of the transistors can be biased independently due to presence of the capacitance C_C. Second point is that, four transmission line segments connected to the gates and drains play a crucial role in maximizing the gain at different bias points while TL $_{D1}$ and TL $_{D2}$ also affect the optimum load impedance presented to the drain ports of the transistors. Their respective values are determined by simulation at the initial steps of the design as will be shown later.

Before going through the design steps, it should be mentioned that in this thesis we are introducing a CAD technique for the power amplifier which depends primarily on the availability of the nonlinear model of the transistor. Our simulation environment is Agilent Advanced Design System (ADS) and the large-signal model of our chosen transistor (ATF-50189) is provided by the manufacturer for ADS environment.

Figure 3.6 illustrates the equivalent model of the transistor as given by Avago Technologies. For the intrinsic device a Curtice 2 model has been selected and the SOT package parasitic components have been added to the die model as depicted in the upper image.

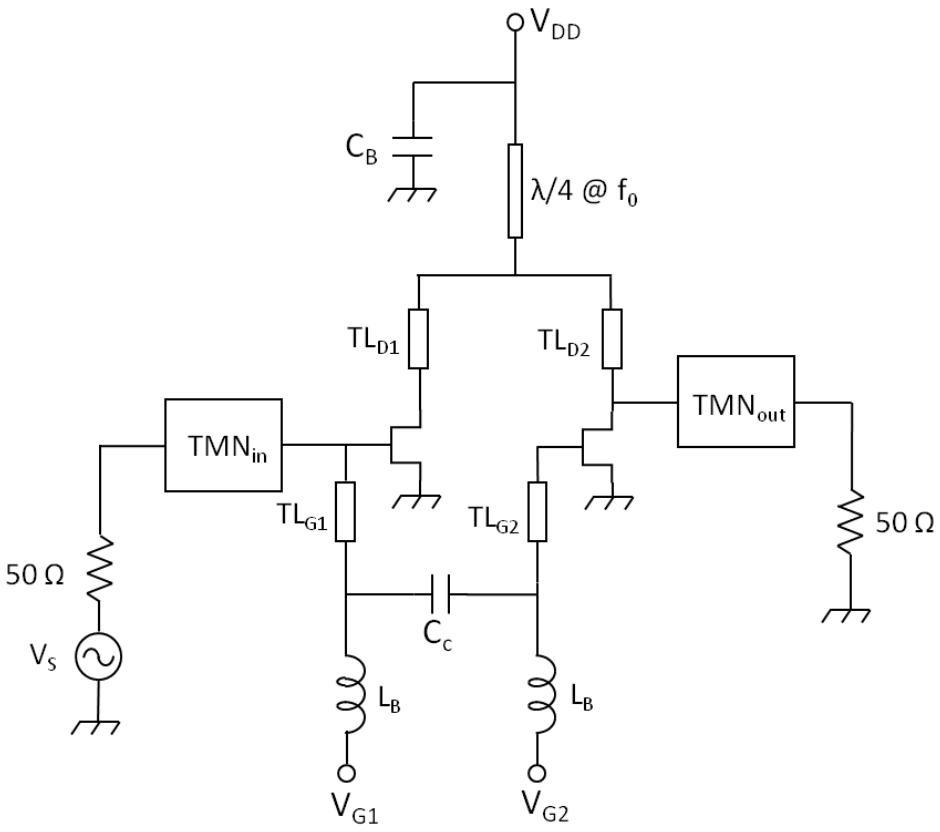


Figure 3.5: Schematic of the proposed PA.

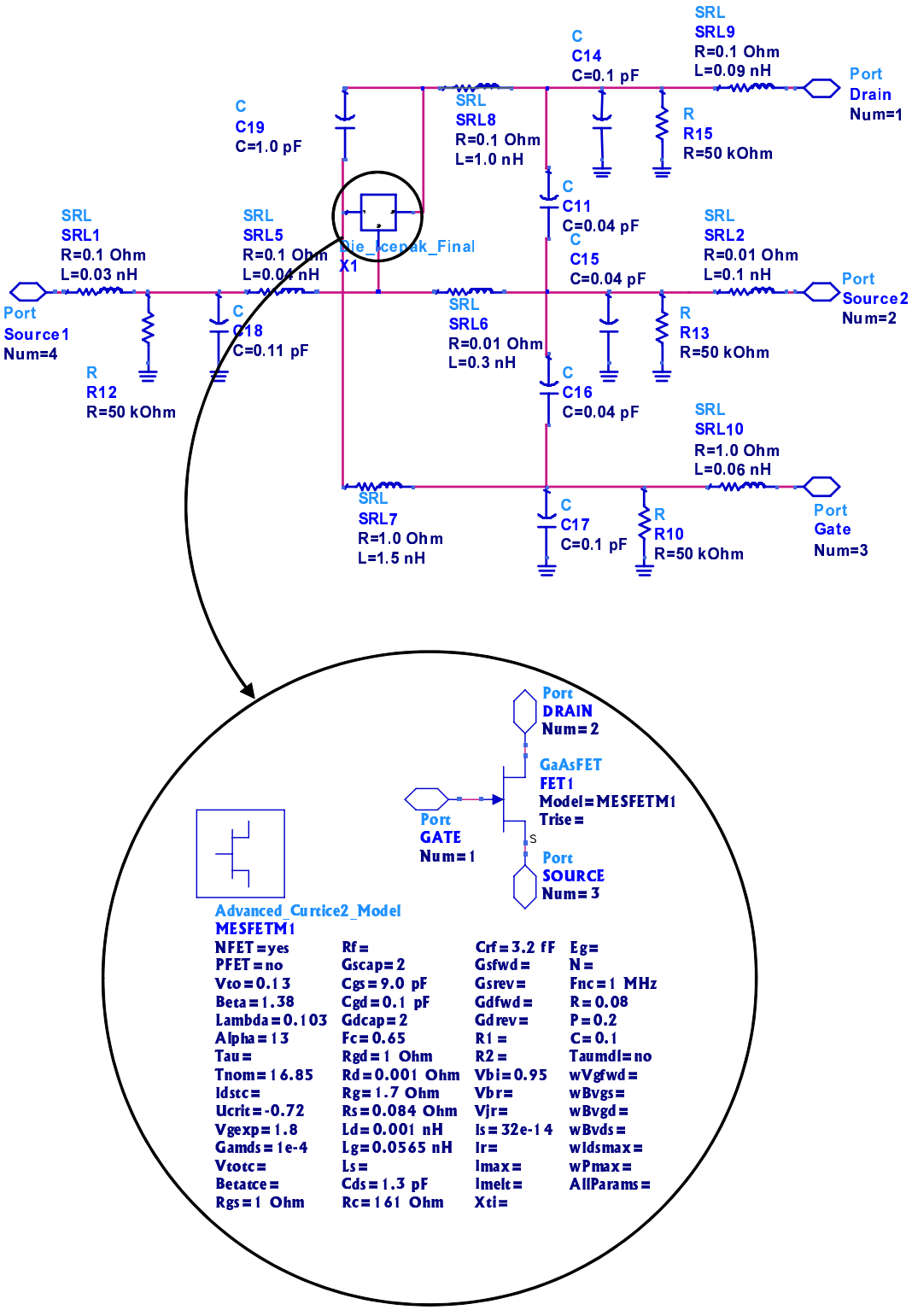


Figure 3.6: Nonlinear model of ATF-50189 provided by Avago Tech for ADS users.

3.3.2 Design Methodology

The design procedure consists of 3 main steps:

1. Optimization of the lengths of TL_{G1}, TL_{G2}, TL_{D1} and TL_{D2} in order to obtain maximum gain at different bias points without loosing stability.
2. Two-tone load-pull analysis of the amplifier in order to determine the gate bias points and the load values which will ultimately result in large-signal sweet-spot in IMD responses.
3. One-tone harmonic analysis of the completed circuit with input and output marching networks at different bias and load conditions and choosing the best options according to the efficiency and gain curves.

The amplifier and matching network are going to be realized on a Rogers' 32 mil substrate (RO4003C) with a dielectric constant of 3.38 and loss tangent of about 0.0025. It has a superior high frequency performance which makes it an ideal choice for wireless applications. In the following, we are going to describe the 3 design steps in more detail.

3.3.2.1 Design step 1

Stability is one of first conditions in any RF amplifier design that should be guaranteed before proceeding. Unfortunately, due to the large signal operating conditions in PAs, the stability issue becomes a nonlinear problem, whose treatment is complex and with difficult solution. Therefore the amplifier stability is typically verified and ensured at small signal conditions, by using small signal simulations based on the Rollet (or Linville) stability factor K.

On the other hand, since in our design the gate biases of two transistors are variable, we should first try to obtain the maximum possible power gain at different biases as well as maintaining this gain at a nearly constant level with acceptable tolerances. This is done by changing the lengths of the four key transmission line pieces shown by TL_{G1}, TL_{G2}, TL_{D1} and TL_{D2} in Figure 3.5. These TL segments as the additional components to the PA structure also influence the stability and hence should be taken care of throughout the optimization process.

The input and output of the amplifier were terminated with 50Ω source and load impedances. For stability analysis, there exist two pre-defined criteria among the built-in functions of ADS which are geometrically derived stability factors based on [122]. On the figures, these two factors are shown as *mu_ load* and *mu_ source*. If either of them is greater than 1, the circuit is unconditionally stable. We set up an S-PARAMETERS simulation together with an OPTIM engine and performed the optimization at various bias points. The drain bias voltage was chosen to be a smaller value of 3.5 V in order to protect the transistors at higher output powers where the drains experience substantial peak voltage levels.

The lengths of the TLs derived after performing several optimizations at different bias point sets are given below. The widths of the all lines are 1.8 mm which results in 50 Ω characteristic impedance on RO4003C substrate.

$$TL_{G1} = 3 \text{ mm} \qquad TL_{D1} = 5 \text{ mm}$$
$$TL_{G2} = 18 \text{ mm} \qquad TL_{D2} = 25 \text{ mm}$$

Figure 3.7 depicts the mu_source and mu_load curves at two extreme bias point sets after replacing the transmission lines of the lengths given above. According to this figure, one of the apparent problems is that the circuit is not stable at lower frequencies due to high power gains. This is the case in most of the RF amplifier designs which will be solved by including resistors in the gate bias circuitry. The inherent losses of the input matching circuit also play an important role in decreasing the gain and stabilize the amplifier at low frequencies.

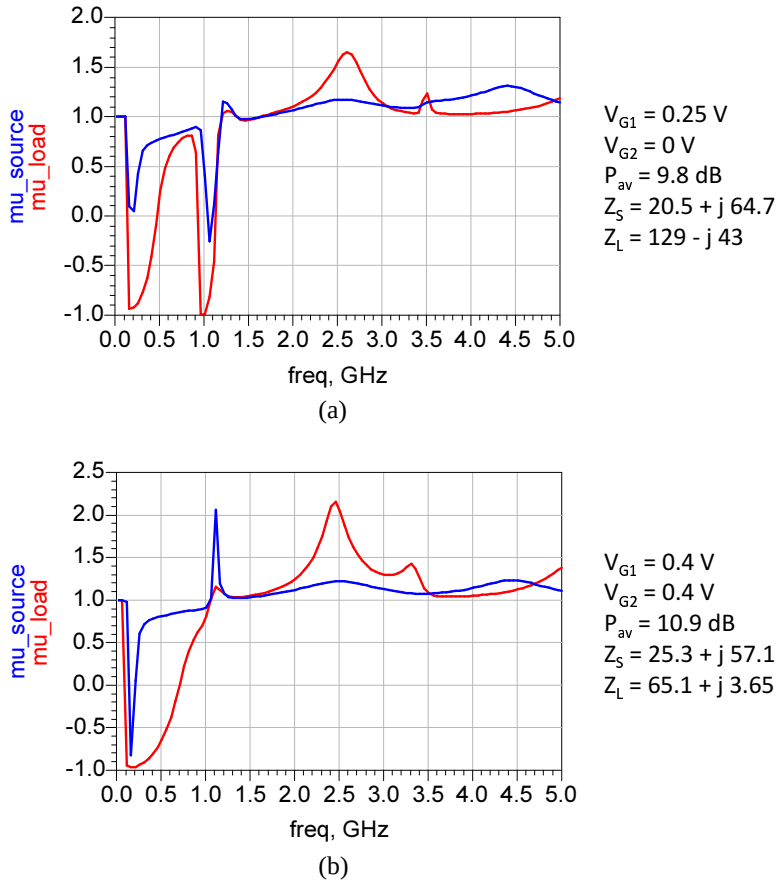


Figure 3.7: Samples of stability factor curves as a function of frequency for two bias point sets of (a) V_{G1} = 0.25 V, V_{G2} = 0 V and (b) V_{G1} = 0.4 V, V_{G2} = 0.4 V.

At the right side of the curves in Figure 3.7, the maximum available power gain as well as the simultaneous match source and load impedances to produce that gain are given. Although there is a slight difference in the gains, but as will be shown later, the higher gain stems from biasing both of the transistors in class A which will be the last *state* of operation in our design and the gain drops slightly at this *state*.

Another point to mention is that the conjugate matching load impedance has changed from 129 - j43 in the first case to about 65 + j3.6 for the second one. So there is a considerable difference between the load impedance values for simultaneously conjugate matching. Unlike the load, the difference is negligible for the source impedances of two cases. This is implying the fact that with changing the gate bias voltages of the two transistors, the optimum load impedance value will also change. We will

actually make use of this fact later in our design.

After finding the lengths of the required key TL segments, the next design step is the two-tone load-pull analysis with the aim of determining the proper gate bias voltages.

3.3.2.2 Design step 2

As the second design step, the main objective of two-tone load-pull analysis is to vary three main parameters, namely, V_{G1}, V_{G2} and the input power P_{in}, and meanwhile monitor the behavior of the third and fifth order intermodulation products. This is done in order to predict the bias points which will result in the creation of large-signal sweet-spots so that we can make use of those points in our design.

The problem that I encountered at this stage was inability of the computer to handle the large amount of data produced by this simulation and display results on the output window. That is because first of all, the simulation is a Harmonic Balance (HB) analysis which involves handling complex non-sparse matrices. Moreover, since there is a two-tone excitation, a two dimensional discrete Fourier transform (FFT) will be included in the process which makes in even more complicated. On the other hand, by counting the real and imaginary parts of the load impedances covering by the load-pull analysis setup, we are trying to perform five sweeps inside one another. Even with large sweeping steps, the created data from the simulation is too huge to be processed and displayed by both my laptop and PC processors.

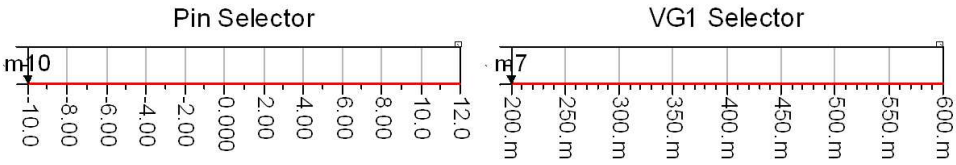
That is why I decided to sweep one of the gate voltages (V_{G2}) manually and left the other two (V_{G1} and P_{in}) to be swept by the simulation. Although in this way the simulation time was still quite long (from nearly one hour to several hours depending on the sweeping steps), the results were at least capable of popping up on the screen after the simulation finished.

As the starting point, V_{G2} is fixed at 0 V while V_{G1} is swept from 0.2 V to 0.6 V. Then V_{G2} is manually incremented up to 0.6 V with 0.2 V steps. According to the I-V characteristics of the transistor, at V_G = 0.2 V, the drain current is 17 mA. The small-signal simulation results of the previous step showed that if the gate voltages of both of the devices fall below 0.2 V, the power gain drops significantly. That is why the sweeping of V_{G1} is started from 0.2 V up to maximum value of 0.6 V in which the I_{DS} reaches its maximum value of about 550 mA.

On the display window of this simulation, I placed two selectors for the two sweeping parameters of V_{G1} and P_{in} together with an Smith chart on which delivered power contours and the optimum load value are demonstrated. After finishing the simulation for each value of manually selected V_{G2}, we can move the markers on the selectors and choose a V_{G1} and P_{in} value and monitor the location of the optimum load on the Smith chart. When putting a marker on the desired load, a group of 3rd order IMD curves appear on another rectangular plot as a function of P_{in} and V_{G1}. Figures 3.8 and 3.9 are demonstrating the result window for V_{G2} = 0 V and V_{G2} = 0.6, respectively.

In order to decrease the amount of data and hence the simulation time, the power sweep range is divided into lower power range starting from -10 dBm to 12 dBm and higher powers starting from 13 dBm up to 19 dBm. With further increasing the input power, no convergence can be achieved and simulation stops.

In Figure 3.8 (a), the selectors are adjusted on V_{G1} = 0.2 V and P_{in} = -10 dBm by the m7 and m10 markers, respectively. The delivered power contours together with the location of the optimum load to

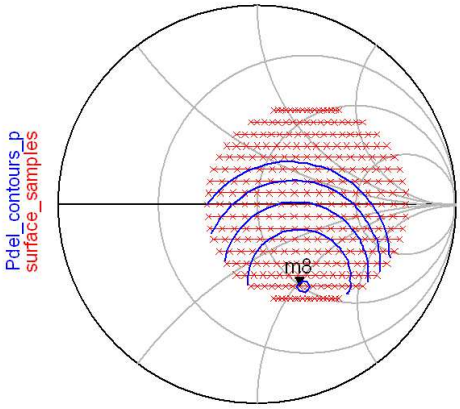


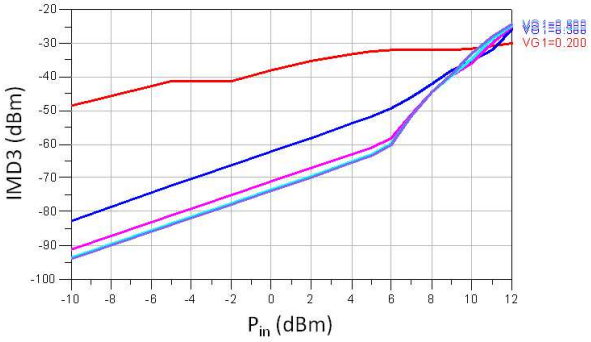
Impedance at marker m8

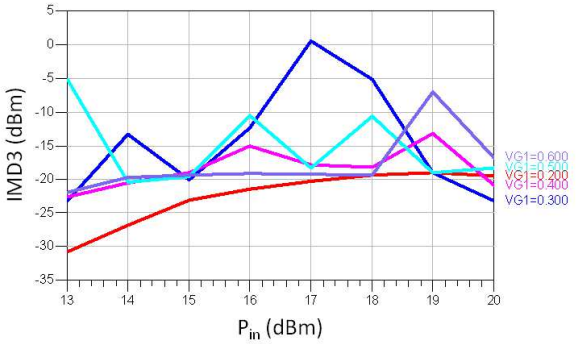
49.85 – j55.70

Input Impedance

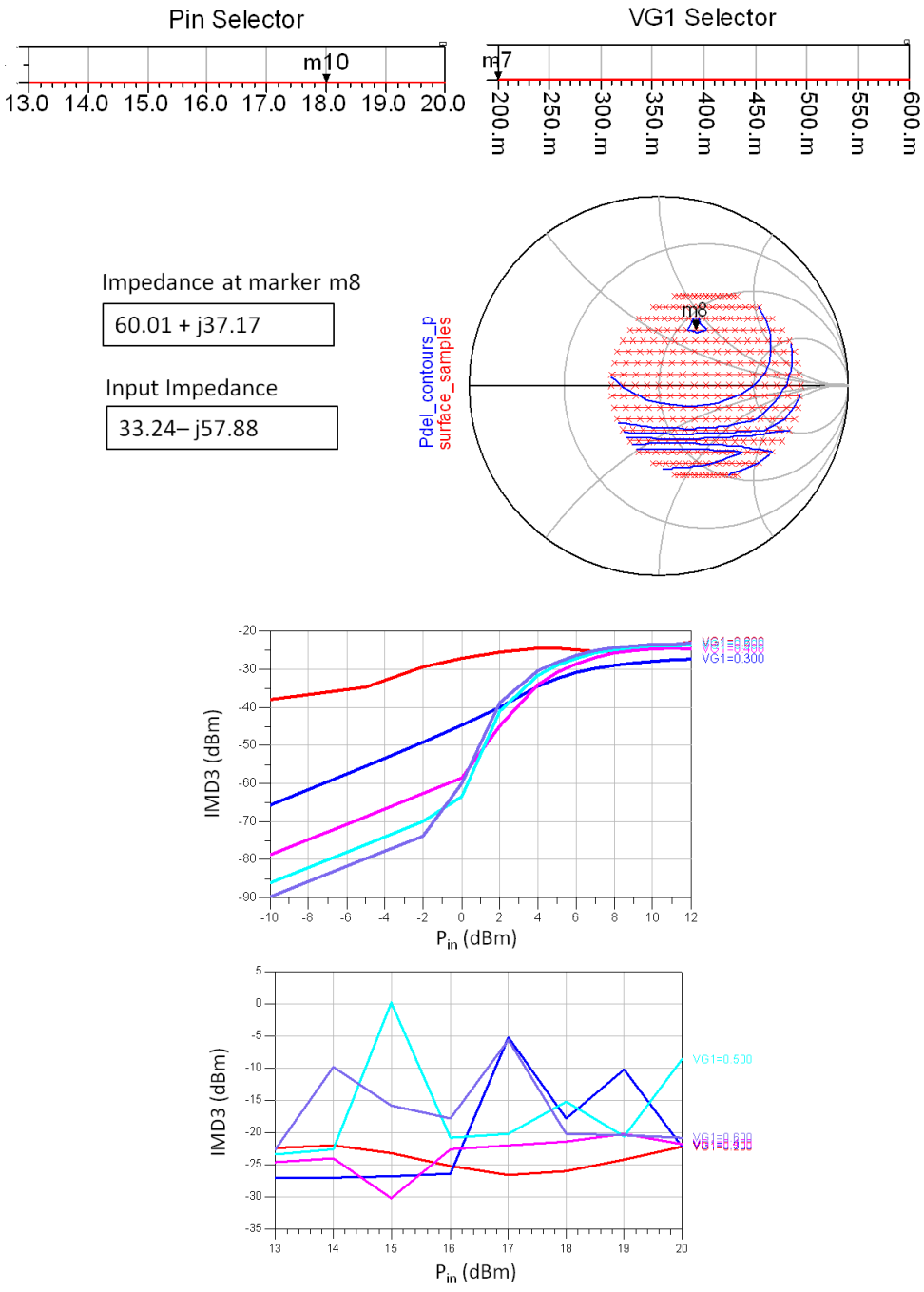
24.42 – j63.12





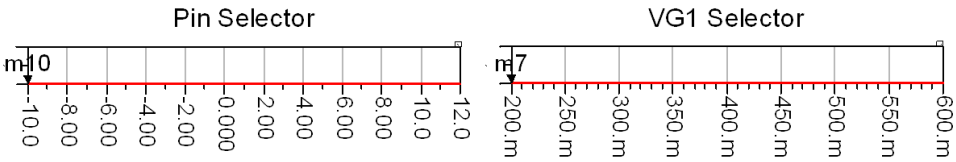


(a)



(b)

Figure 3.8: Sample results of the two-tone load-pull simulation for V_{G2} = 0 V at two optimum load values for (a) low and (b) high input power regions.

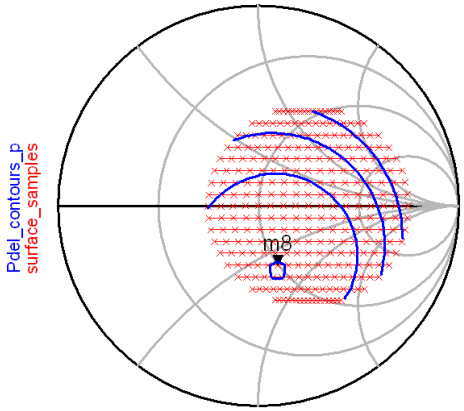


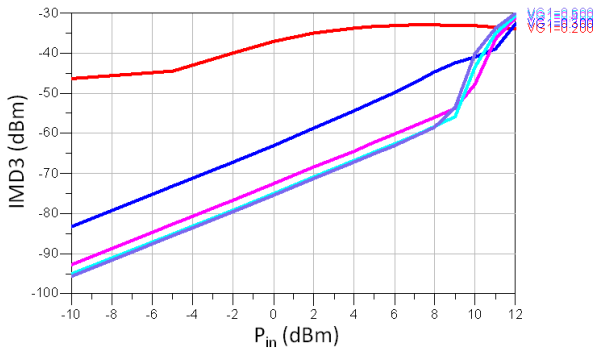
Impedance at marker m8

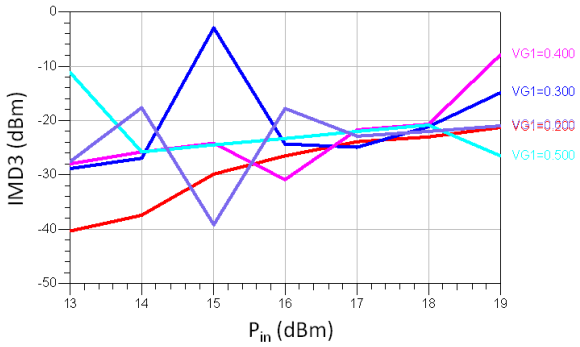
50.20 – j32.81

Input Impedance

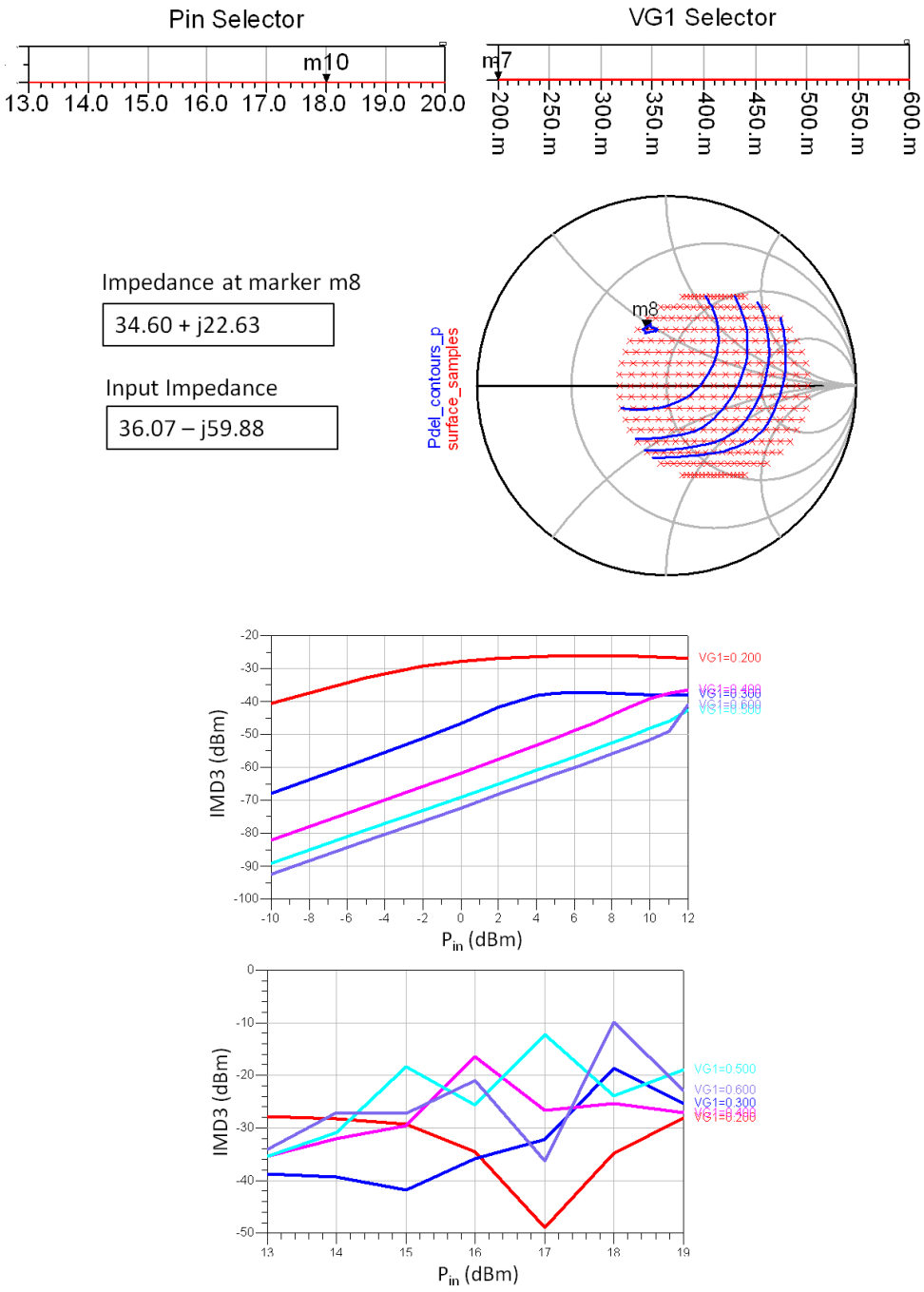
27.40 – j60.41







(a)



(b)

Figure 3.9: Sample results of the two-tone load-pull simulation for V_{G2} = 0.6 V at two optimum load values for (a) low and (b) high input power regions.

deliver the maximum power are sketched on the Smith chart. Putting the marker (m8) on the optimum load gives the value of P_{Lopt} = 49.85 - j55.7 and the input impedance value seen from the input of the amplifier when the output is terminated with P_{Lopt}. Below the Smith chart, the IMD3 curve is plotted but in two separate graphs for low and high input power ranges, as discussed earlier. Note that, as we move the marker m8 on the Smith chart, the IMD3 curves update automatically which means that the curves of Figure 3.8 and 3.9 are valid only for the specific load value that is presented above them on the Smith chart. By examining these graphs we can make sure that a sweet-spot is going to appear for a particular bias set of (V_{G1},V_{G2}) and the chosen load value.

For instance, according to Figure 3.8 (a), for the bias set of V_{G1} = 0.2 V and V_{G2} = 0 V, if matching is done for the optimum load at low drive levels, a nearly flat region appears in IMD3 curve. Note that the graph of our interest in this case is the red one. Although there is no sign of a sweet-spot here, the intermodulation level becomes less than what would be expected if the curve followed the small-signal slope. So this bias and load values can be one of the candidates for our design.

On the other hand, Figure 3.8 (b) shows that by performing the matching at the optimum load of higher input powers, the creation of an IMD3 minimum after about 14 dBm can be clearly observed on the bottom graph of high power ranges. Hence this load value is also a candidate of one of our final operating *states*.

Figure 3.9 (a) and (b) contain the similar graphs of the previous figure except with V_{G2} = 0.6 V. Again, by inspecting the red curves of V_{G1} = 0.2 V, we can find out that this time the sweet-spot will be present for both of the matching conditions. We ran the simulation for other values of V_{G2} and monitored carefully the corresponding intermodulation curves by adjusting the markers on V_{G1} and P_{in} selectors for each simulation. The conclusion can be summed up as follows:

As far as V_{G1} is kept under 0.4 V, for any value of V_{G2} from 0 V to 0.6 V, there exists a favorable behavior in third order intermodulation curve in terms of either the creation of sweet-spot or a flat region for some range of driving signal (P_{in}) which both of them are the signs of linearity improvement of the amplifier. The important point to notice is that the location of the sweet-spot or the flat region along the P_{in} axis is a function of the load impedance. Hence with performing the matching for the optimum loads at different input drives, we are actually able to adjust the location of IMD sweet-spots providing that the gate bias voltage of the first transistor is kept under 0.4 V for the case of this transistor.

This is the fact that we are going to benefit from in the amplifier design to prevent the linearity degradation at higher drive levels near the 1-dB compression point of the amplifier while enhancing the efficiency at small-signal region. In the best case of the simulation environment, we are able to improve the efficiency for more than 35% at 15 dB back-off from the 1-dB compression point which has not been reported in any other work, but definitely in practice a lower performance is expected.

3.3.2.3 Design step 3

So far, we have the gate bias pairs (V_{G1},V_{G2}) and corresponding optimum load impedances that will lead to IMD3 sweet-spots. For convenience in the rest of the thesis, each combination of the three parameters namely, (V_{G1},V_{G2},Z_{Lopt}) will be called one '*state*' of the amplifier. As the last step of the design, we are going to provide the desired impedances by connecting the matching networks to the amplifier at the input and output and then perform one-tone and two-tone harmonic balance analysis of the completed circuit for every *state* and monitor the fundamental output power, 1-dB compression

point, gain and intermodulation terms. In this way, we can choose the proper *states* for the amplifier to switch in between, according to a criteria which is going to be explained.

Before proceeding to the simulation results, there is an important observation which is worth to be mentioned here. Among the results that we can obtain through the load-pull analysis, in addition to the delivered power contour are the efficiency contours as well. It means that we are able to specify the optimum load impedance at which the efficiency becomes maximum. I noticed during the analysis that the optimum load for maximizing the output power and efficiency overlap with each other at small-signal region. But as the input power increases these two points begin to separate and divert from each other following two independent paths on the Smith chart.

Figure 3.10 illustrates the power (blue) and PAE (red) contours at different input powers shown on the chart which are obtained after the load-pull analysis at V_{G1} = 0.25 V and V_{G2} = 0 V.

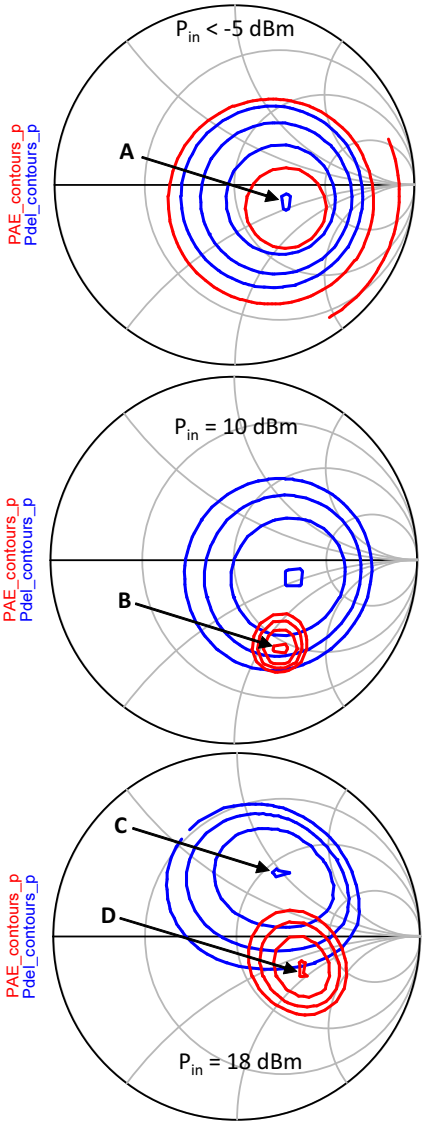


Figure 3.10: Power and PAE contours after the load-pull analysis at different input powers.

As stated above, in low drive levels from the noise margin to a definite value, the optimum power and optimum PAE loads are on the same location which corresponds to point **A** on the first chart of Figure 3.10. As the power increases up to about 10 dBm, while still there is no movement of the optimum power point, the PAE optimum load slides downwards reaching point **B** at the input power of 10 dBm. Rising P_{in} beyond that level, both of the power and PAE optimum loads begin to move upwards reaching points **C** and **D**, respectively, at the input drive level of 18 dBm. It was observed that by performing the matching at point **B**, the PAE can be improved significantly at lower input drives making this point the best candidate for being the first *state* of operation in our amplifier. Points **A**, **C** and **D** can be potential load impedances for the next *states*. The strategy for choosing the proper first *state* of operation and later on switching to the higher states is going to be described in the following.

Since our primary goal is to enhance the efficiency at power back-offs, the first *state* is the ternary of (V_{G1},V_{G2},Z_{Lopt}) that results in the maximum possible efficiency at reduced drive levels. For attaining the maximum efficiency the gate bias of the transistors should be kept as low as possible which gives the only option of V_{G1} = 0.25 V and V_{G2} = 0 V. This leaves us with choosing the last parameter which is Z_{Lopt}.

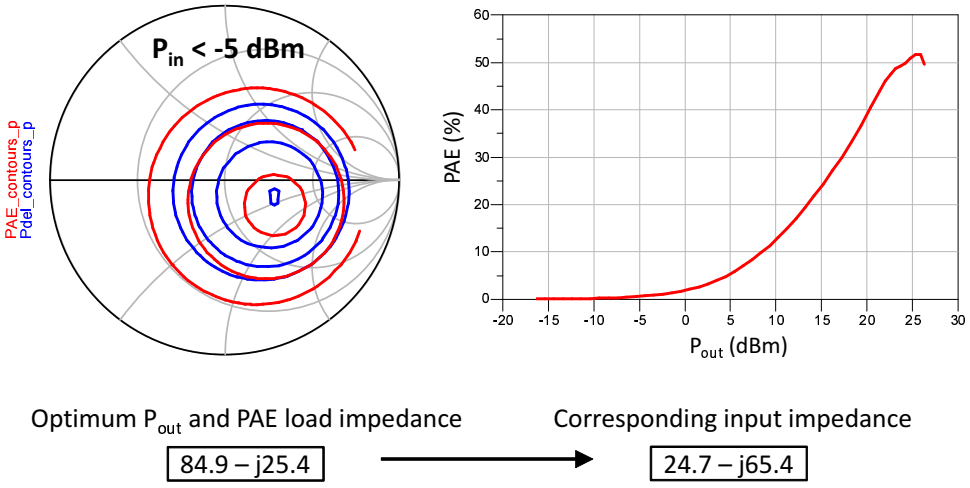
In order to decide on that point, we find the optimum output power and PAE points at a couple of different input powers using load-pull analysis and perform a one-tone HB simulation by providing the matching at those impedance points. By monitoring the PAE curves as a function of input or output power, we can finally choose the option with the best efficiency performance. Figure 3.11 (a) through (f) demonstrates the chosen matching points and resulting PAE curves for V_{G1} = 0.25 V and V_{G2} = 0 V while the input power increased from P_{in} < -5 dBm in (a) to the maximum value of P_{in} = 27 dBm in (d) after which the harmonic balance simulation fails to converge due to excessive non-linearity level. The input impedances shown on the figure are the conjugate matching impedances for maximizing the power gain of the amplifier.

Note that for the case (a), matching is performed at the optimum load for maximum PAE. Following that for the case (b) optimum load for maximum PAE and P_{out} is a common point on the chart. For the rest of the cases from (c) to (f) matching is done at the optimum load for maximum output power. In order to easily compare the PAE plots of these 6 sample states, all curves are plotted on common axes as shown in Figure 3.12. All the other possible matching cases create PAE curves in between these 6 sample cases. According to this Figure, the best option for being the first *state* of operation is the red curve which corresponds to matching for optimum PAE load at the input power of 10 dBm. This makes the first *state* ternary as (V_{G1},V_{G2},Z_{Lopt}) = (0.25V , 0V , 44.1-j61.3 Ω).

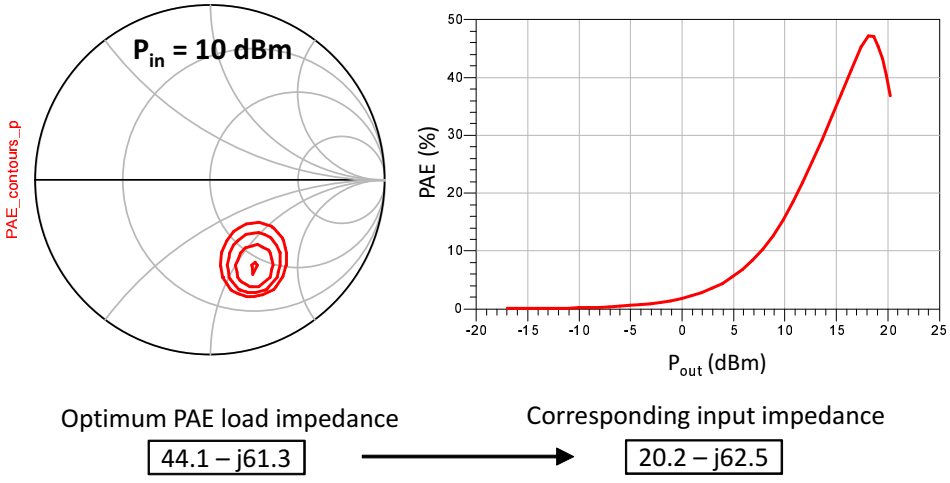
For verifying the presence of a sweet-spot along the IMD3 curve of the first *state*, we made a two-tone harmonic balance of the amplifier with 1 MHz frequency spacing between two tones. Figure 3.13 presents the IMD3 and IMD5 terms that fall at the right side of two fundamental tones, namely at 2401.5 MHz and 2402.5 MHz, respectively. These IMD terms are known in the literature as ‘upper’ IMD terms as opposed to the other two terms at the left side of the fundamentals known as ‘lower’ IMD terms. No considerable difference can be seen between the upper and lower IMD behaviors in the simulations.

According to Figure 3.13, a sweet-spot appears in IMD3 plot as predicted earlier due to correct biasing. There is some kind of an anomalous behavior in IMD5 curve as well which resembles to a shallow sweet-spot at lower powers than the IMD3’s.

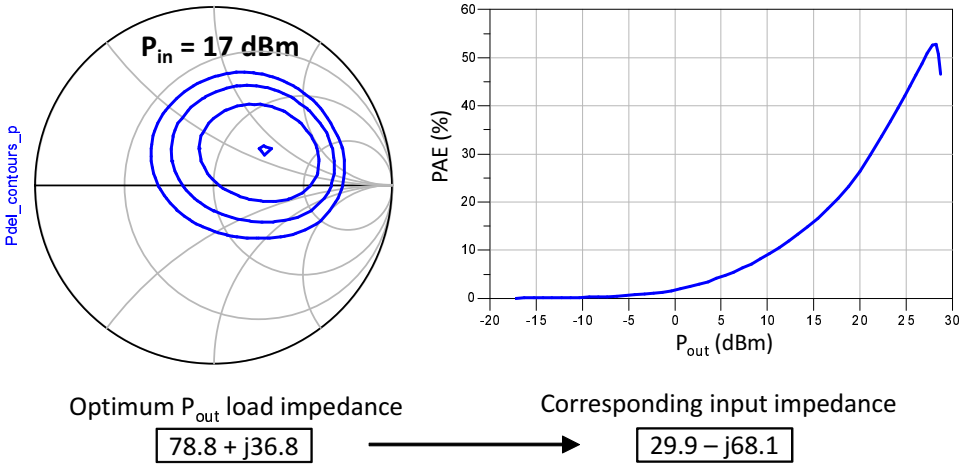
After having chosen the first *state*, it is now time to find the higher *states* to switch as the input power increases. First we should define a criterion for leaving the present *state* and switch to a higher state. This criterion is definitely the linearity which can be assessed in terms of 1-dB compression point,


P_in < -5 dBm
PAE_contours_p
Pdel_contours_p
PAE (%)
P_out (dBm)
Optimum P_out and PAE load impedance
84.9 – j25.4
Corresponding input impedance
24.7 – j65.4

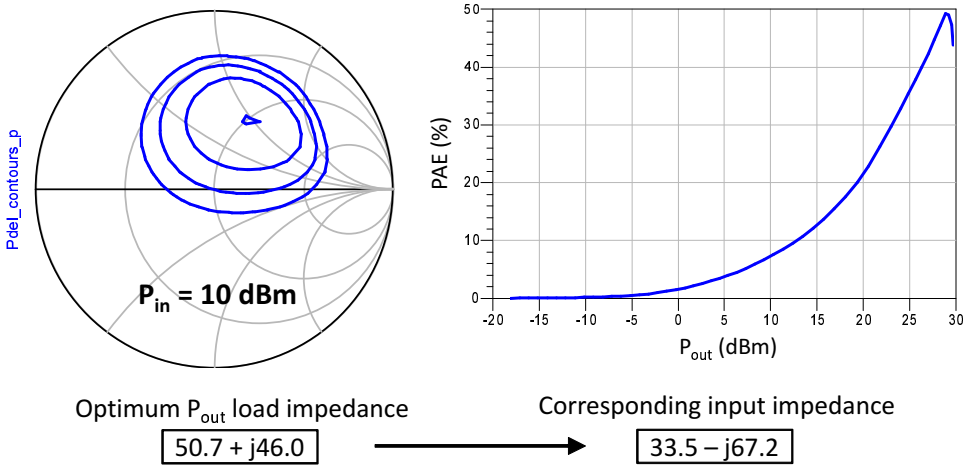
(a)


P_in = 10 dBm
PAE_contours_p
PAE (%)
P_out (dBm)
Optimum PAE load impedance
44.1 – j61.3
Corresponding input impedance
20.2 – j62.5

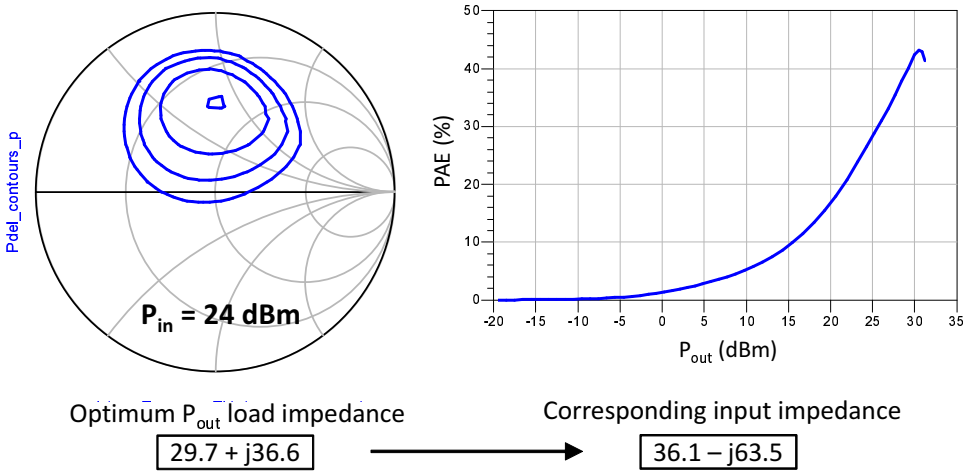
(b)


P_{in} = 17 dBm
Pdel_contours_p
PAE (%)
P_{out} (dBm)
Optimum P_{out} load impedance
78.8 + j36.8
Corresponding input impedance
29.9 – j68.1

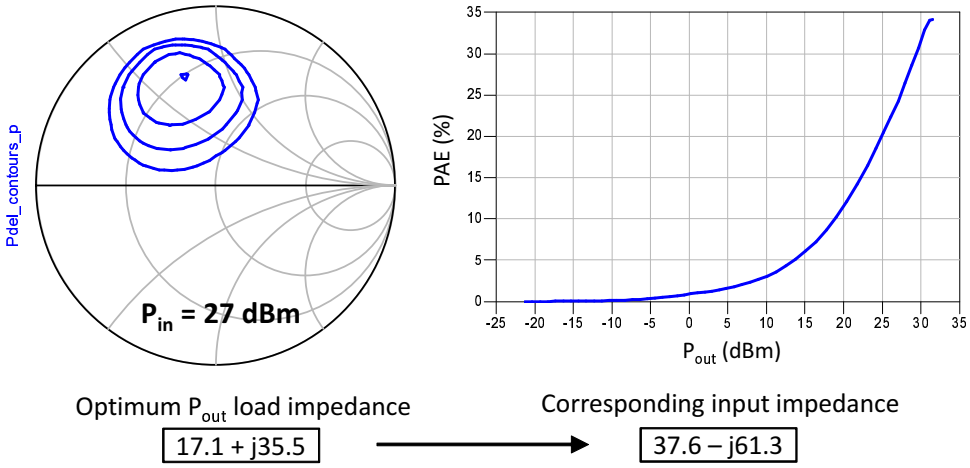
(c)


P_{in} = 10 dBm
Pdel_contours_p
PAE (%)
P_{out} (dBm)
Optimum P_{out} load impedance
50.7 + j46.0
Corresponding input impedance
33.5 – j67.2

(d)



(e)



(f)

Figure 3.11: Optimum load impedances and resulting PAE curves while input power in which the optimum load is derived increased from less than -5 dBm in (a) to 27 dBm in (f).

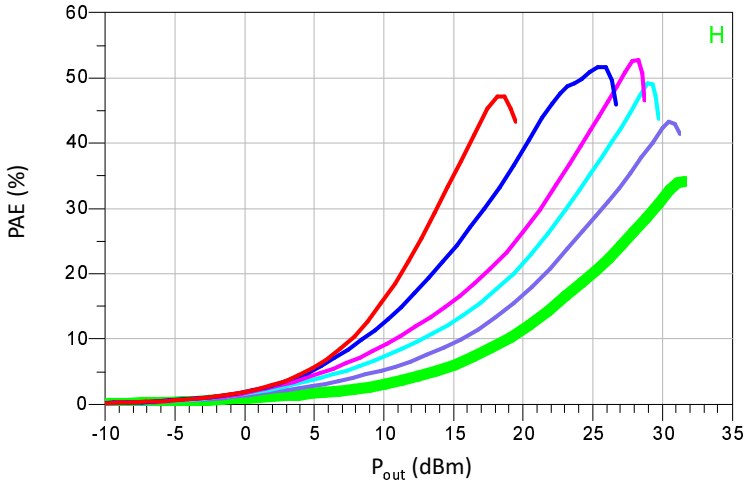


Figure 3.12: PAE curves of the load points of Figure 3.11 drawn on a common axis for comparison purposes.

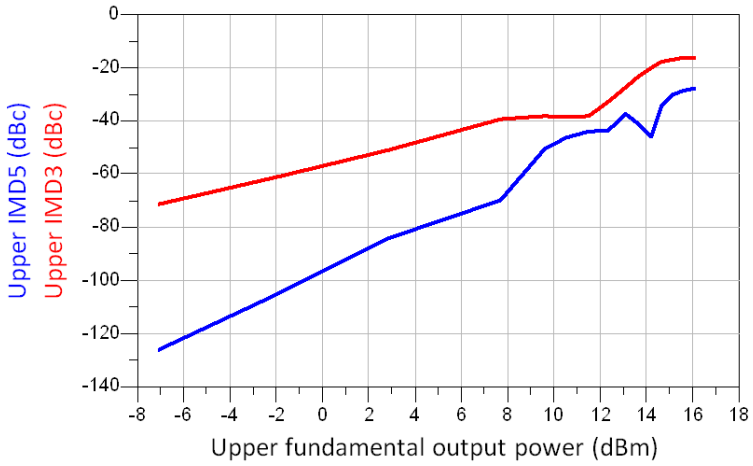


Figure 3.13: Upper third and fifth order IMD of the first operational *state* of the amplifier.

third order intercept point and/or intermodulation terms particularly the level of IMD3. We base our decision making upon the 1-dB compression point first and later on we will also include the IMD3 level. From the harmonic balance simulation of the first *state*, output 1-dB compression point of the amplifier came out to be 18.4 dBm. It means that if the amplifier is targeted to perform always below the P_{1dB}, as soon as the output power begins to exceed 18.4 dBm, we should switch to a new *state* with higher P_{1dB}.

But according to the simulations, there are two mechanisms by which the 1-dB compression point of the amplifier can be increased. First, by performing the matching for the optimum load impedance of the output power at higher drive levels, P_{1dB} is also improved. This can be observed for the Figure 3.11 where we experience a rising trend from P_{1dB} = 22.7 dBm in (a), 26.5 dBm in (c) up to around

35 dBm in (f). Meanwhile from the Figure 3.12 it can be seen that by increasing the P_{1dB} from the leftmost curve to the right, the peak efficiency level also shifts to the right giving lower PAE at lower input drives.

The second mechanism of rising the P_{1dB} is by increasing the gate bias voltage of V_{G2} while keeping V_{G1} constant at 0.25 V for guaranteeing the creation of sweet-spot. By increasing V_{G2} we actually push the second transistor to operate in class-A which naturally results in a better linearity performance and hence increase the P_{1dB}. Note that since the drain current also grows, like the previous case, by increasing V_{G2} the efficiency curves shift to higher power levels. For instance, consider the case V_{G1} = 0.25 V and V_{G2} = 0.3 V. The input power is swept from 0 dBm to 28 dBm in order to find the location of the optimum power loads as shown on the Smith chart of Figure 3.14.

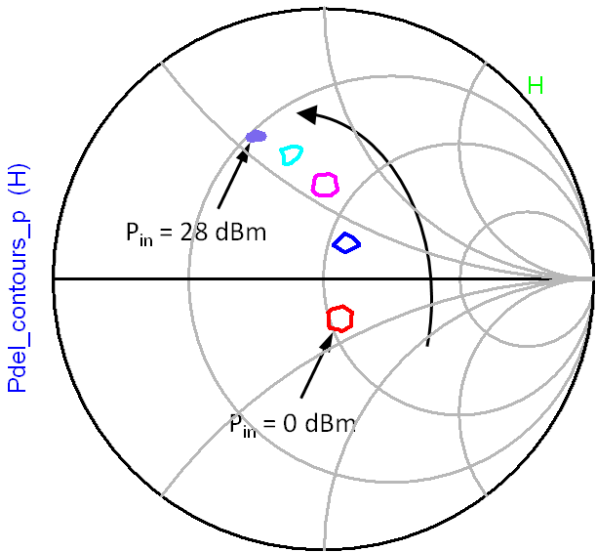


Figure 3.14: Optimum load impedance and its movement as the driving power increases.

Table 3.1 summarizes 5 sample P_{out} optimum load values of Figure 3.14 and their corresponding conjugate match input impedances together with the level of the input powers where the impedances are obtained and finally the output 1-dB compression points.

The efficiency curves of these 5 sample operational states are shown in Figure 3.15. As stated earlier, by performing the matching at higher drive levels, the PAE plots shift to the right and 1-dB compression point also rises to higher values.

Making use of both of these mechanisms to increase the P_{1dB}, a large number of (V_{G1},V_{G2},Z_{Lopt}) ternaries would be created. The main issue here which is the most important part of the design step 3, is to wisely choose those *states* that allows a continuous rise of the output P_{1dB} with increasing the input power attaining a nearly constant (with acceptable ripples) power added efficiency in the back-off region. To make selections between the possible options, two parameters should be monitored. First, the PAE curves and second, the power gain curves. The later is because by changing the optimum load impedance of Z_{Lopt}, a considerable change is observed in the gain behavior in terms of the small-signal gain change as well as creation of an expansion or over-shooting region just before reaching the P_{1dB} compression point.

Table3.1: Summary of 5 sample operational states for V_{G1} = 0.25 V and V_{G2} = 0.3 V

P_{in} (dBm)	Z_{Lopt} (Ω)	Z_S (Ω)	Output P_{1dB} (dBm)
0	56.1 – j18.1	26.8 – j59.6	24.5
16	56.6 + 14.5	30.7 – j63.0	27.2
20	37.3 + j28.2	35.2 – j62.4	29.9
24	25.5 + j31.9	37.6 – j61.2	31.2
27	16.3 + j30.7	37.8 – j58.7	32.2

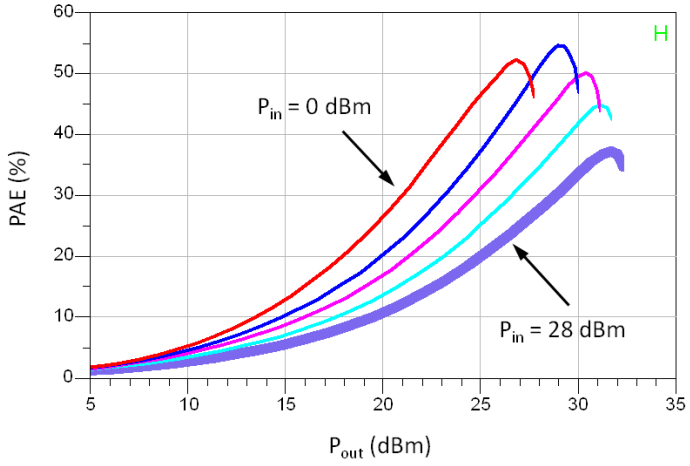
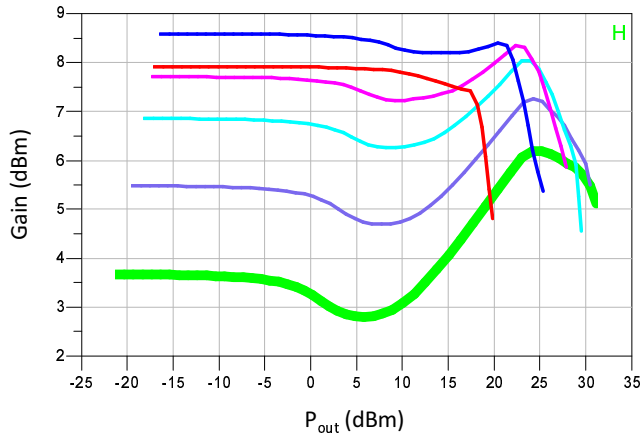


Figure 3.15: Efficiency plots of the 5 sample operational states for the gate bias points of V_{G1} = 0.25 V and V_{G2} = 0.3 V.

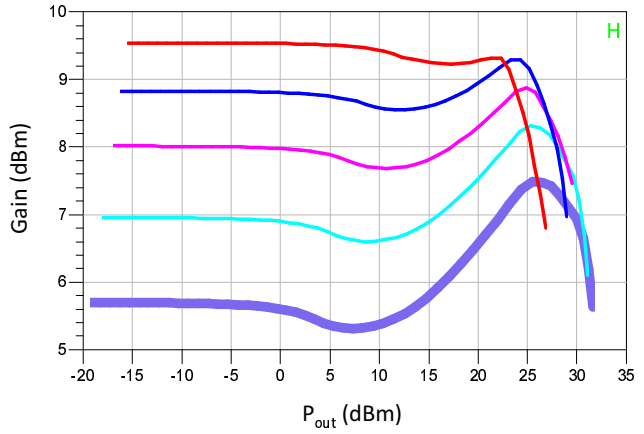
Figure 3.16 (a) and (b) illustrate the gain plots of the two different V_{G2} values whose PAE curves have been presented in Figures 3.12 and 3.15, respectively. The colors are consistent with those of the PAE graphs.

In order to choose the proper *state* according to the gain curves, we should specify a definite small-signal gain and an acceptable amount of ripple, say 1 dB. It means that in either case of the compression or its following expansion, the gain must not vary beyond 1 dB from its small-signal value. Applying this condition on the Figure 3.16, we can keep just the first three curves (red, blue and pink) of case (a) and first two curves (red and blue) of case (b) and eliminate the others.

By performing the same kind of simulation at all the possible bias points and by checking the different load impedances with small increments in the input power and finally, applying the gain and efficiency criteria mentioned above, we were eventually able to determine the final operational *states* of the amplifier. Table 3.2 summarizes the 11 finally chosen operational *states* of the amplifier. The second column of the table denoted as P_{in}, is the input power which has been applied during the load-pull



(a)



(b)

Figure 3.16: Gain plots of the two cases studied before: (a) 6 states of V_{G1} = 0.25 V and V_{G2} = 0 V and, (b) 5 states of V_{G1} = 0.25 V and V_{G2} = 0.3 V.

analysis and that particular optimum impedance point has been derived. The last column of the table on the right represents the output power where the PAE curve reaches its maximum.

It is included in the table to verify the fact that along with the increase of the output P_{1dB} compression point in each *state*, the PAE curve also shifts to the right compared to its preceding *state*. These 11 *states* are selected from among more than 40 candidates, according to the criteria discussed earlier.

In order to visualize the optimum loads of the 11 *states*, the impedances are depicted on the Smith chart of Figure 3.17. An important point to be mentioned here is that the optimum load values of the first 4 states of the Table 3.2 happened to be the loads in which the PAE is maximum at the specific given input power during the load-pull analysis. This is while the remaining 7 *states* are those optimum loads in which the amplifier can deliver the maximum power. According to the table as well as the Smith chart, an interesting observation about these two groups can be stated as follows:

Table3.2: Summary of final 11 operational states of the amplifier

State	P_{in} (dBm)	V_{G1} (V)	I_{D1} (mA)	V_{G2} (V)	I_{D2} (mA)	Z_{Lopt} (Ω)	Output P_{1dB} (dBm)	P_{out} @ Peak PAE (dBm)
1	10	0.25	40	0	0	39.9 – j64.2	18.4	18.2
2	17	0.25	40	0	0	62.6 – j63.8	20.5	21.0
3	18	0.25	40	0	0	83.6 – j58.6	21.3	22.0
4	19	0.25	40	0	0	100 – j42.5	22.1	24.3
5	0	0.25	40	0.15	2	82.1 – j22	23.6	25.8
6	10	0.25	40	0.2	17	70 – j10.8	25.7	26.7
7	16	0.25	40	0.3	80	57.3 + j8.7	27.0	28.6
8	20	0.25	40	0.4	190	41 + j24.4	29.4	30.1
9	21	0.25	40	0.5	345	29.6 + j26.4	30.6	31.0
10	23	0.27	55	0.6	540	22.3 + j27.1	31.1	31.7
11	25	0.27	55	0.6	540	17 + j27.5	31.8	31.9

The resistive part of the first group of impedances increases as the input power is growing from state 1 to 4, while for the second group there exists an inverse trend.

Although the trajectory of the loads may be different based on the active device, the trend of the second group was actually expected, because it is a known phenomena which is also reported in the other works like [72] and [73]. On the other hand, the inverse behavior of the first group (PAE matched) is observed only in this work and to my knowledge, it is not reported anywhere else.

The design procedure comes to an end after determining the final operational *states* of the amplifier. Before proceeding to the simulation results, we are going in the next section to investigate in detail the practical way of finding the optimum load impedances which will be followed by designing the tunable matching network to realize those impedances.

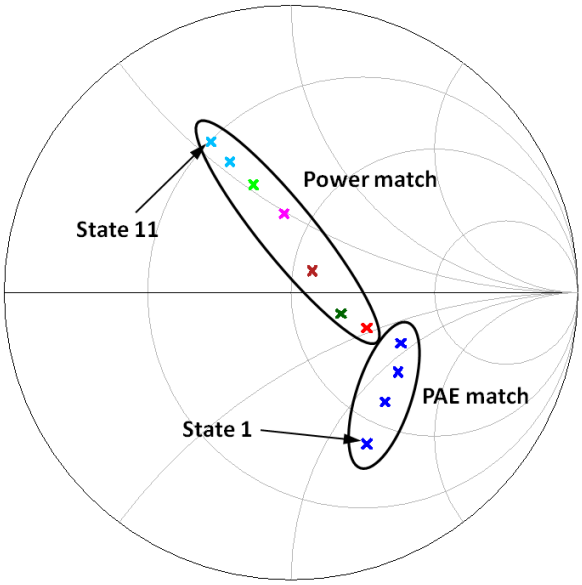


Figure 3.17: Optimum load impedance points at 11 operational states of the amplifier.

3.4 Load-Pull Analysis Setup and TMN Design

As mentioned before, our approach in PA and TMN design is an integrated method as shown in Figure 3.4. That is because efficiency is an important factor in our amplifier and any parasitics introduced by additional components severely influence the efficiency. According to the design methodology described in the previous section, load-pull analysis is the key step of our design which requires a well established load-pull setup. But since this kind of setup is not available in our laboratory, I decided to try another way which can be suitable only for the case my design.

That is to design a common circuit which can serve for both load-pulling purposes and the final tunable matching network. In this way, we are able to minimize the adverse effects of additional parasitics as well as possible minor errors which could be introduced during the de-embedding process if a separate load tuner of a standard load-pull setup were to be used.

3.4.1 Choosing the Configuration

First of all we have to choose the topology of the TMN. The most important criteria at this stage is that the matching network should have the potential to transform the load termination to any position within the Smith chart. Secondly, it should have a simple structure with the less parasitics. Among the simple topologies that fulfil the first criteria are T-type, Π-type and two-stage ladder networks. Our choice would be the two-stage ladder network as shown in Figure 3.18. The advantage of this network over the other two is that, for higher impedance transformation ratios, the Q of the two-stage network is significantly lower. Note that high Q conditions in the matching network give rise to increased losses and higher voltage swings, limiting the power handling capabilities [72].

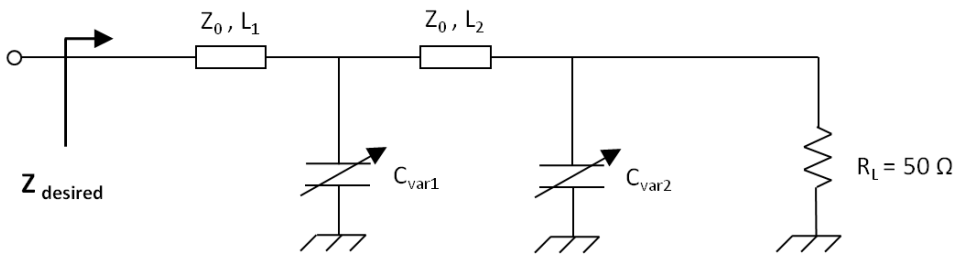


Figure 3.18: Simplified two-stage network topology for TMN implementation.

Moreover, we are going to implement the variable capacitors by commercially available varactor diodes and the varactor biasing circuitry in this structure is simpler to implement and the voltages across the varactors can be checked easily from simple output power measurements. Note that the transmission line segments are used instead of inductors. That is also because of its simplicity of realization and lower parasitic effects compared to discreet inductors or bond-wire realization as in [72].

The area of the Smith chart that can be covered by this network topology is a function of varactor sweeping ranges as well as the width and lengths of the two transmission line segments. As an example, Figure 3.19 presents the covered area for the specific parameter values shown on the figure.

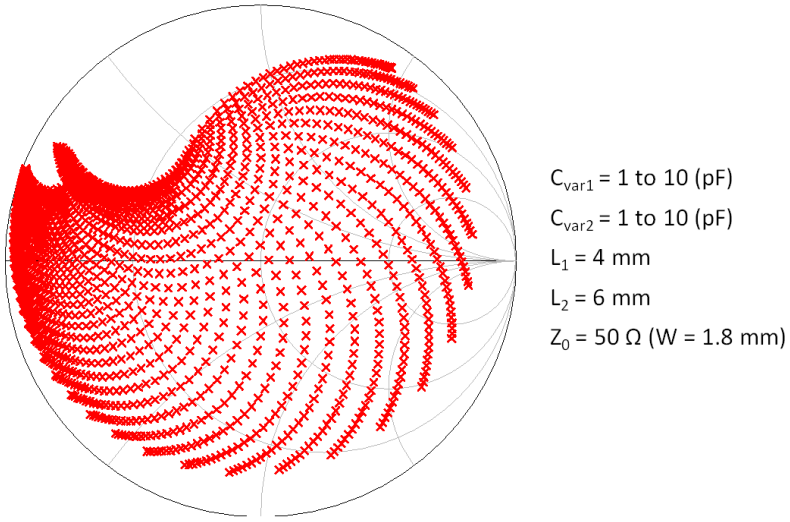


Figure 3.19: Impedance coverage of the simple two-stage ladder matching network.

By simply changing the length of the first transmission line at the input, the red area would rotate around the center of the chart enabling us to cover any desired load impedance trajectory obtained from amplifier design stage. We have chosen the characteristic impedance of the lines to be 50 Ω for simplicity in connecting to other stages and measurement equipments but according to the design requirements other values can be selected.

3.4.2 Choosing the Varactor Device

After choosing the configuration, the second step is to find a varactor diode that fits our purposes. Since in our design the varactors are going to be a part of the output matching network of a power amplifier, the subjects of power handling, linearity, rectifying effects and loss which was studied in section (2.5) should be precisely taken into consideration in selecting the device.

Aeroflex/Metelics as a part of the larger corporation of Aeroflex, is a leading supplier of Schottky diodes, PIN diodes, Tunnel diodes and Varactors. It is one of the few manufacturers of varactor diodes with high breakdown voltages to be used in RF power applications. MTV 4030, MTV 4045, MTV 4060 and MTV 4090 are four main series of low resistance, high Q, high breakdown voltage abrupt junction varactor devices provided by Aeroflex/Metelics. The two digits of the number in the name of the devices represent the breakdown voltage of the series. It is interesting to note that, due to their proper exponent parameter value ($\gamma = 0.45$), the varactors of these series have already a desirable characteristic in terms of linearity. It means that using the anti-series structure would improve the linearity as well as discussed in section (2.5) and [111].

In selecting the proper device for our application between these four groups, we should consider the fact that by increasing the breakdown voltage the quality factor of the varactor decreases. After inspecting all of these series and considering the power and voltage issues of our amplifier, **MTV 4045** came to be the best choice for our design. Figure 3.20 gives the plot of all the variable capacitances of this group as a function of the applied reverse voltage.

While deciding on which varactor of these series should be used, I logically opted for the first device namely, MTV 4045-01, due to its highest Q factor among the all. As discussed in section (2.5), I was intending to form a 2×N varactor stack by connecting as many of them in parallel as needed to provide the desired capacitance. But I found out that this would be the best option if the varactors were to be implemented in the integrated form rather than hybrid components. That is because during the simulations when I took into account the additive loss factors and the parasitic effects that soldering of individual varactors in parallel might bring about, I noticed their negative influence on the efficiency. Since the efficiency is of prime importance in our design, we would try to avoid the extra components of any kind and their resulting loss that may finally lead to the degradation in efficiency of the amplifier. Hence, by increasing the number of the high quality factor devices connected in parallel, the degradation of efficiency due to the additional loss that parallel connecting brings about, is inevitable. This means that a compromise should be made between the device type and the number of devices in parallel.

Considering these facts, I should have found a high Q varactor that by paralleling just a few number of them we could provide enough capacitance range to cover the area of interest on the Smith chart. Our ultimate choice finally came out to be **MTV 4045-05** with two ones in parallel. The important point to mention is that, as will be shown in the following, this choice can fulfil our impedance coverage requirement, provided that some additional components be introduced to the network of Figure 3.18.

Note that the anti-series configuration is necessary due to its positive effects on increasing the tunability range and the linearity as discussed in section (2.5). According to the corresponding curve of MTV 4045-05 in the Figure of 3.20, a single varactor of this type has a capacitance tunability range of about 2 pF in zero applied voltage down to 0.5 pF in 30 V of applied reverse voltage. The intrinsic parameters and CS-19 package parasitic components of this device is summarized in Table 3.3. The CS-19 package was ordered due to its low parasitics, according to the manufacturer. The notations of the table is consistent with those of the Figure 2.4 and Equation 2.3.

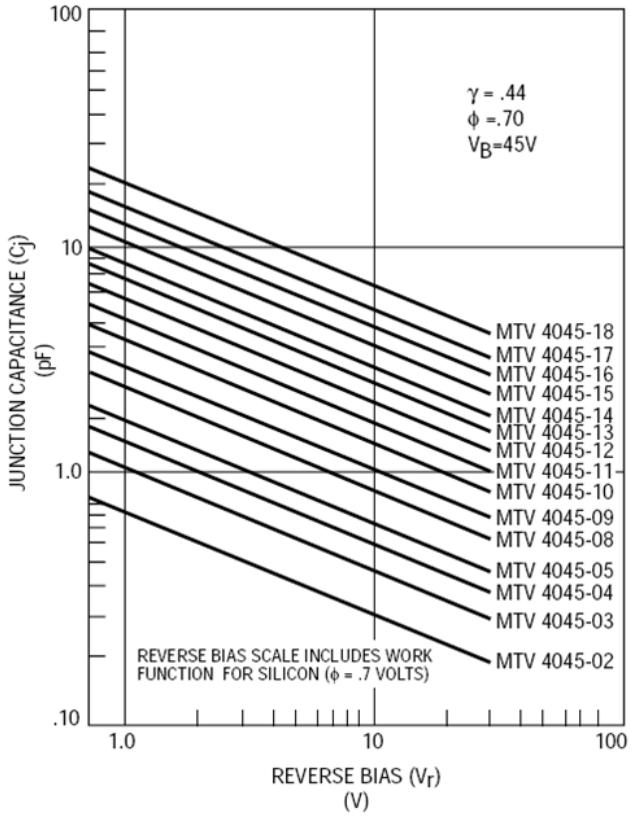


Figure 3.20: Typical performance of MTV 4045 series varactor diodes [123].

Table3.3: Intrinsic and CS-19 package parameters of MTV 4045-05

Parameter	Value
C_{j0}	2.77 pF
Φ	0.7 V
γ	0.45
V_B	45 V
L_S	0.5 nH
C_P	0.1 pF
R_S	1.1 Ω

To evaluate the capacitance tunability range of this device in anti-series configuration, we should specify the maximum RF swing at the output of the amplifier. With the reference to Table 3.2 the maximum attainable peak output power of the amplifier will be about 32 dBm (≈ 1.6 W) which, while delivered to a 50 Ω load, will result in a peak RF voltage of about 12.6 V. Hence according to Equations 2.9 and

2.10 for the anti-series configuration, we have:

$$\frac{12.6}{2} + V_{BIAS} < 45\ \text{V} \quad \Rightarrow \quad V_{BIAS} < 38.7\ \text{V} \tag{3.2}$$

$$V_{BIAS} - \frac{12.6}{2} > 0 \quad \Rightarrow \quad V_{BIAS} > 6.3\ \text{V} \tag{3.3}$$

3.4.3 Applying Additional Modifications

With the reference to the characteristic curve of MTV 4045-05 in Figure 3.20 and Equations (3.2) and (3.3), the tunability range is from maximum capacitance of 0.95 pF at 6.3 V to minimum of about 0.4 pF at 38.7 V. It is due to this small tunability range that we will have to introduce additional components to the matching network, as stated before. To make it clear, consider the circuit of Figure 3.21 in which the capacitors of Figure 3.18 are replaced by anti-series varactors. The length of the transmission lines are kept the same. The DC-feeding inductors are added for biasing purposes of the varactors and the intervening capacitors are the DC-blocking capacitors.

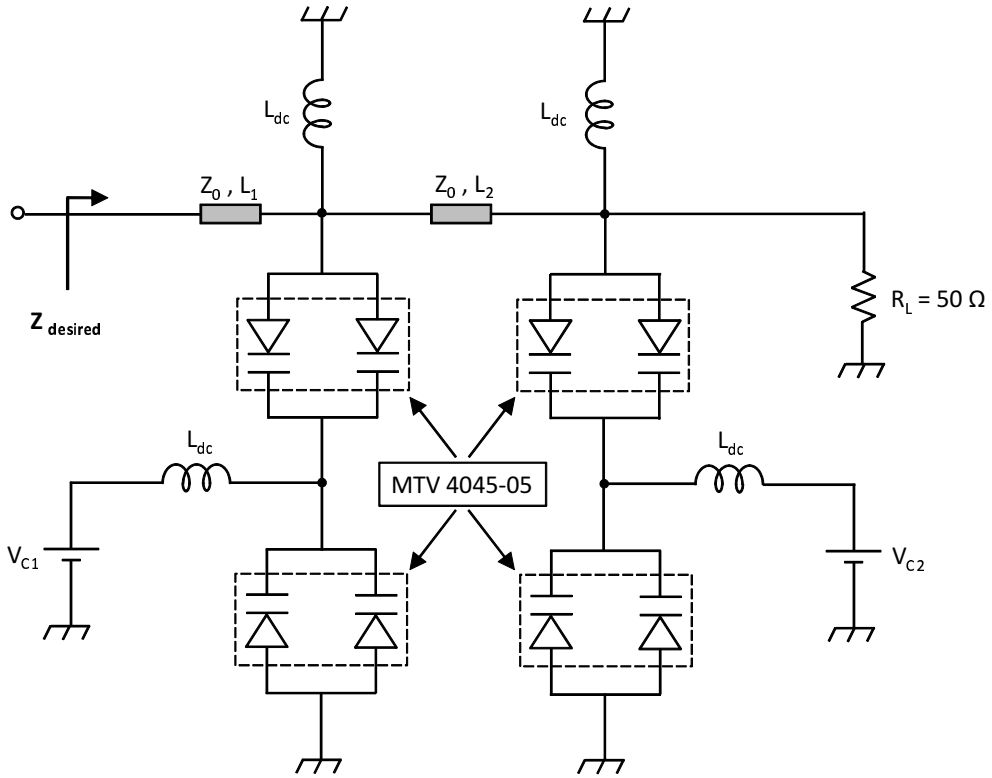


Figure 3.21: Two-stage ladder TMN with anti-series varactors replaced the capacitors in Figure 3.18.

The impedance area covered by this network is presented in Figure 3.22. As can be seen, when replacing the ideal capacitors by real varactor model, the impedance coverage region of the network

shrank substantially such that it seems to be totally useless for our purposes. While searching for some solutions, I decided to add two pieces of transmission lines in the two parallel branches before the varactors. I was actually planing to transform the reactance range covered by each anti-series varactor branch to other values using the impedance transformation properties of the transmission line and it perfectly worked.

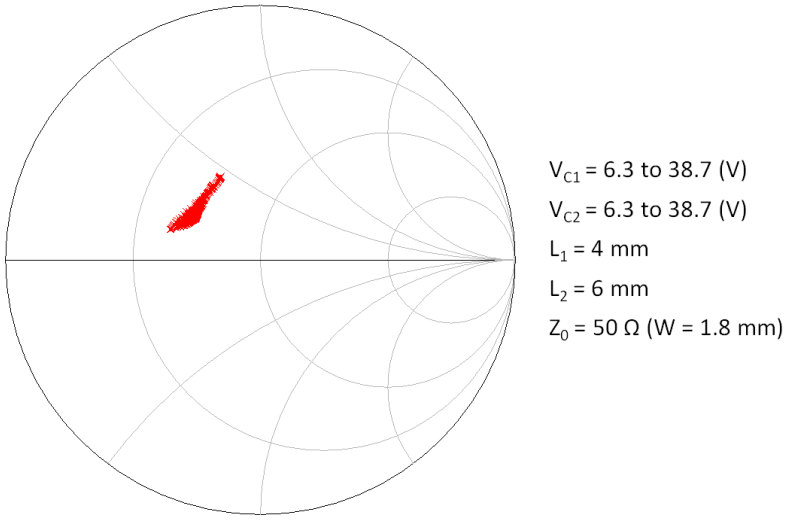


Figure 3.22: Impedance coverage of the network of Figure 3.21.

As is known, the impedance seen from the input of a transmission line terminated by the load Z_L, is written as

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan\beta L}{Z_0 + jZ_L \tan\beta L} \tag{3.4}$$

While replacing Z_L with the impedance of a capacitor we obtain

$$Z_{in} = Z_0 \frac{\frac{1}{jC\omega} + jZ_0 \tan\beta L}{Z_0 + j\frac{1}{jC\omega}\tan\beta L} = jZ_0 \frac{Z_0 C\omega \tan\beta L - 1}{Z_0 C\omega + \tan\beta L} \tag{3.5}$$

Equation (3.5) shows that while the capacitance varies from 0.4 pF at $V_C = 38.7$ V to 0.95 pF at $V_C = 6.3$ V, it can be translated into totally different values using transmission lines before the varactors. By choosing a proper value for the length of the lines, we can provide the desired impedance coverage. By adding these components the network of Figure 3.21 can be re-sketched as shown in Figure 3.23.

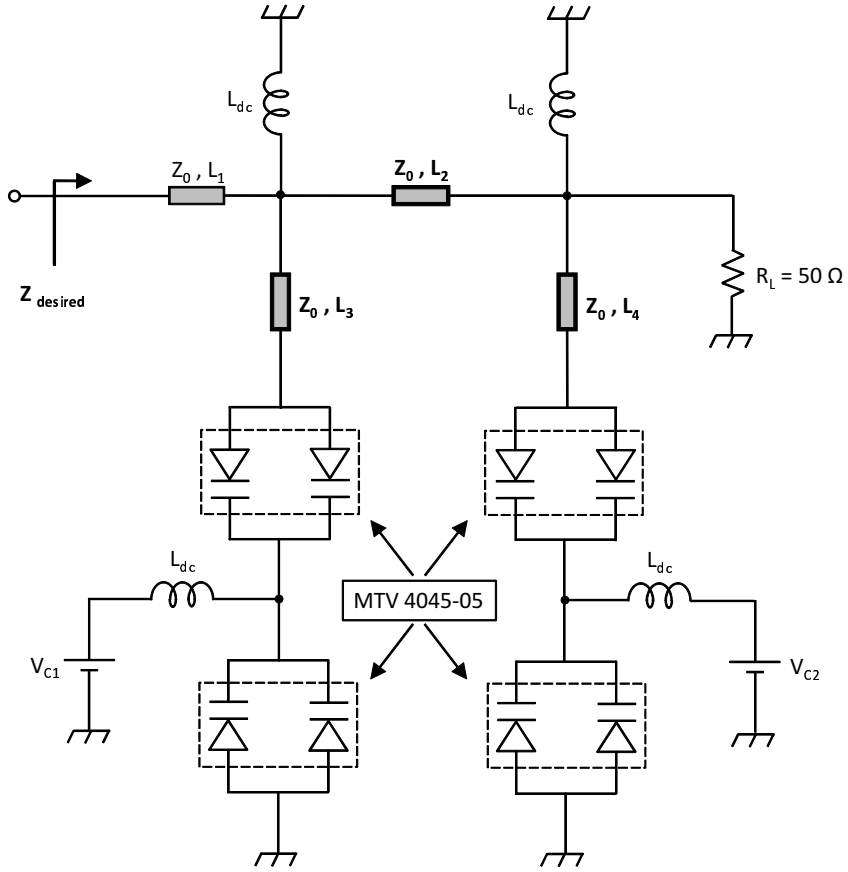


Figure 3.23: Two-stage ladder TMN with anti-series varactors and added transmission lines.

In this way, we have been able to expand the impedance coverage region to a larger area which is illustrated in Figure 3.24. This area has been obtained by setting the lengths as L_3 = 7 mm and L_4 = 10 mm. By modifying these lengths together with L_1 and L_2, we can change the shape and location of the covered area on the Smith chart and hence provide the desired matching.

3.4.4 Loss Factor

Although everything seems to be alright, the story does not end here. When I tried to perform the matching using this network for the first operating *state*, I noticed a considerable reduction in the final efficiency of the amplifier, even though the matching had been performed precisely at the optimum point.

The only explanation for this observation could be the inability of the matching network to transmit the power from its input to the 50 Ω load. This lead me to the fact that since the matching network is no more a lossless network, during the design process we should not only adjust the elements of the matching network to provide the desired impedance, but also the loss factor of Equation (2.22) should carefully watched and tried to minimized.

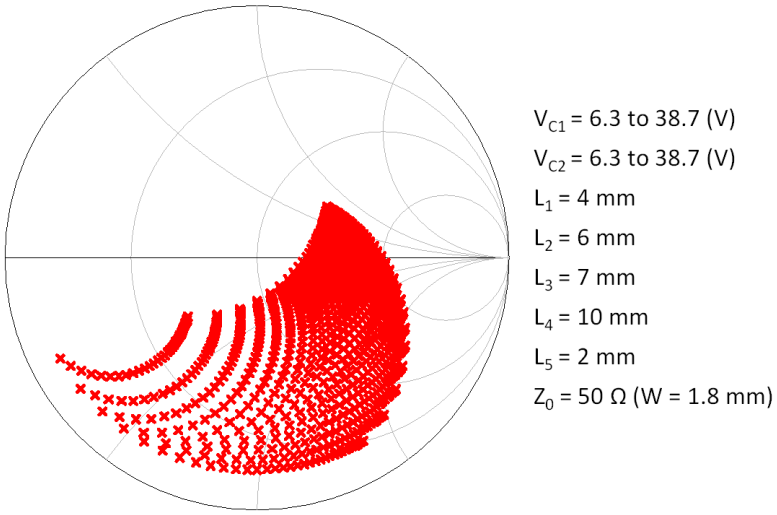


Figure 3.24: Impedance coverage of the network of Figure 3.23.

As an example, for the network of Figure 3.23, if the loss factor is calculated as a function of two control voltages of the varactors, the graphs of the Figure 3.25 is obtained. Note that the loss factor is larger than -1 dB for the control voltages above around 12 V and since the sensitivity of the capacitance to the applied voltage in the varactors reduces as the voltage increase, this applies a serious constraint on the impedance coverage of the matching network.

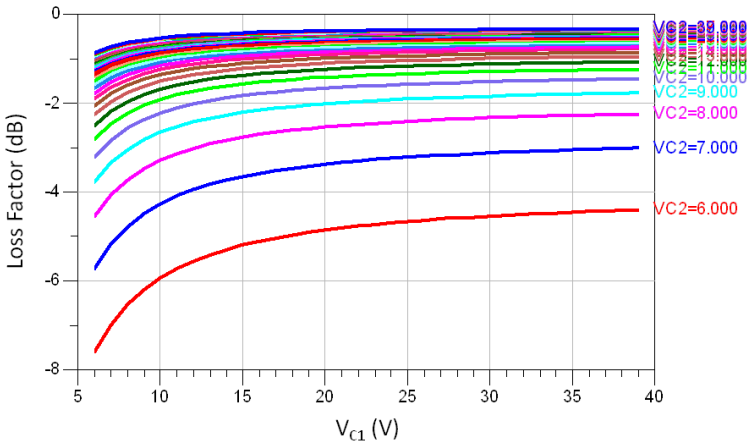


Figure 3.25: Loss factor of the matching network of Figure 3.23 for small input powers.

Figure 3.26 demonstrates the impedance coverage area exactly the same as Figure 3.24 but with two different colors which distinguish those points with loss factor smaller than -1 dB (red) and those with loss factor larger than -1 dB (blue) which are in fact our desired points. It has been found that the more we try to utilize the points with smaller loss, the more the coverage area shrinks.

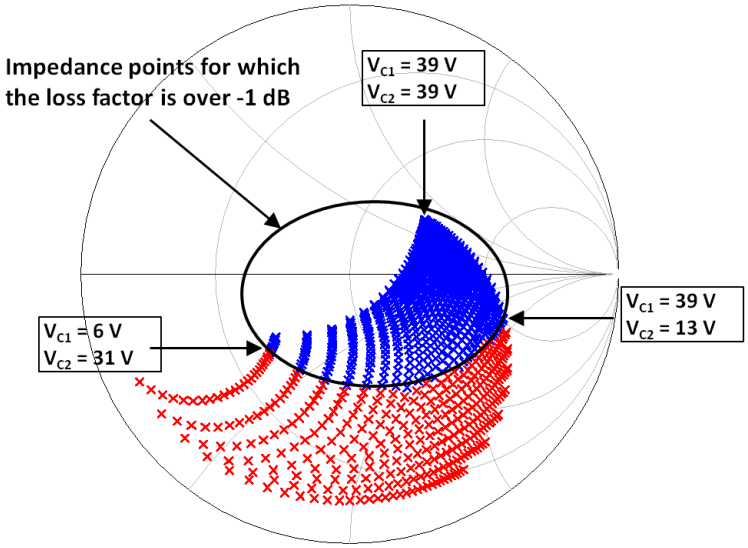


Figure 3.26: Impedance coverage of the network of Figure 3.23 for small input powers distinguishing the low-loss and high-loss regions.

3.4.5 Large-signal Effects

Last but not least is investigating the behavior of the matching network at higher input powers. Note that the impedance coverage areas presented so far are all under small-signal conditions. It was observed that when the input power of the matching network which is actually the output power of the amplifier increases two changes take place.

First, a significant reduction of the loss factor occurs for low and high values of the two biasing voltages which in turn decreases the tunability range and makes the coverage region of interest shrink even more to a small area. This effect can be easily seen on Figures 3.27 and 3.28 while respectively compared with Figures 3.25 and 3.26.

Second, the coverage area on the smith chart deforms from its initial shape for the small-signal inputs, due to the appearance of the non-linear effects in the varactors. The main consequence of this phenomena is that there is no more a one by one mapping between the control voltages and the impedance points. It means that there might be two different sets of (V_{C1},V_{C2}) that result in common impedance point on the Smith chart.

This effect can be noticed from Figure 3.28 in which some blue and red points are nearly overlapping with each other. Definitely, in these cases, those biasing sets that result in the minimum loss should be chosen.

3.4.6 Final Design of the Load-Tuner

By considering all of the design issues presented above, we are now in the position to design the load-tuner for the load-pull analysis which in turn will also play the role of the tunable matching network to span the optimum load trajectory of Figure 3.17. For the case of the load-tuner, the loss-factor is

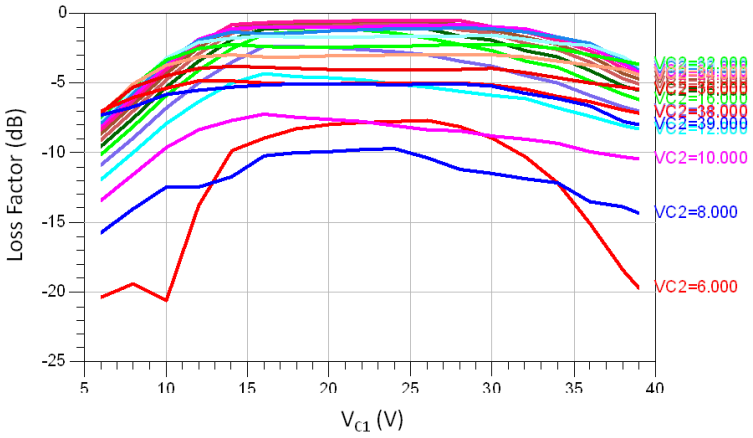


Figure 3.27: Loss factor of the matching network of Figure 3.23 for the input power of 30 dBm.

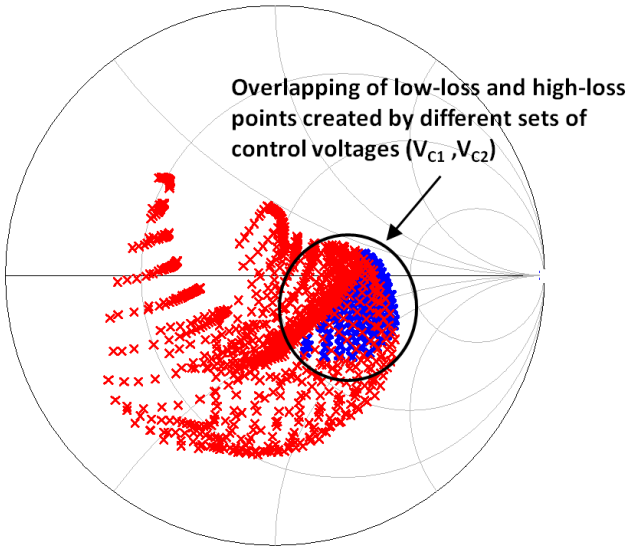


Figure 3.28: Impedance coverage of the network of Figure 3.23 for the input power of 30 dBm distinguishing the low-loss and high-loss regions.

not as much critical as for the case of the final TMN. That is because during the load-pull analysis, the goal is to find the load impedance in which maximum power can be delivered or maximum efficiency can be achieved rather than to provide the maximum power or efficiency. On the other hand, the TMN to be used in the amplifier should be able to transfer the maximum power from the transistor part to the load and hence its loss must be minimized. Since our designed network is going to be used for both purposes, on one hand we will try to expand the area of the Smith chart being covered in order to obtain reliable load-pull results and in the other hand, the loss factor of (2.22) will be tried to be maximized.

An important point that was found during the optimizations for attaining minimum loss is that, by replacing the four DC-feed inductors that DC-wise ground the anodes of the varactor stacks, by $\lambda/4$

transmission lines which are ac-wise shorted in one end, a significant improvement in the loss factor can be obtained. That is because due to parasitic components, the RF-chokes used in practice can not provide as good open-circuit as a $\lambda/4$ line terminated by short-circuit can, at the design frequency. So despite its negative effect on the bandwidth, we preferred to utilize transmission lines instead of the inductors as depicted in Figure 3.29. Note that since there exists no DC source for the varactor stacks on the top, there is also no need for biasing capacitors. In order to provide a better open circuit for the signal, a higher characteristic impedance ($Z_0 = 69\,\Omega$) for the $\lambda/4$ lines has been chosen.

After performing the optimizations and fine tuning the parameters composed of the lengths of the five key transmission lines and the input capacitance value, the impedance coverage region of Figure 3.30 is obtained. Parameter values and sweeping ranges of the control voltages are shown at the right side of the Smith-chart. The small black circles on the chart are the chosen optimum points of Figure 3.17 which were obtained by ideal built-in load-tuner of the ADS during simulations. Like the previous figures, the impedances denoted by blue crosses are those for which the loss factor rises over -1 dB (loss is below 1 dB). Nearly all of the eleven points have been fallen within the low loss region.

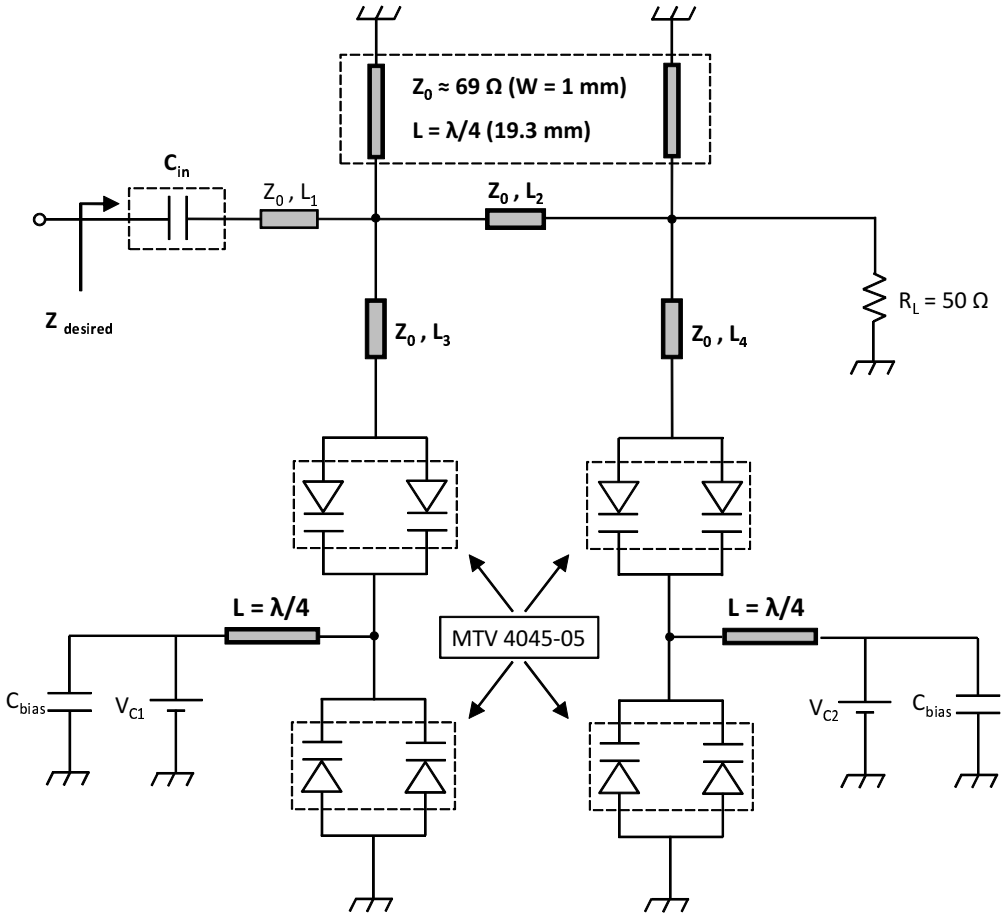


Figure 3.29: Final view of the two-stage ladder TMN with anti-series varactors, added transmission lines and $\lambda/4$ transmission lines for biasing purposes.

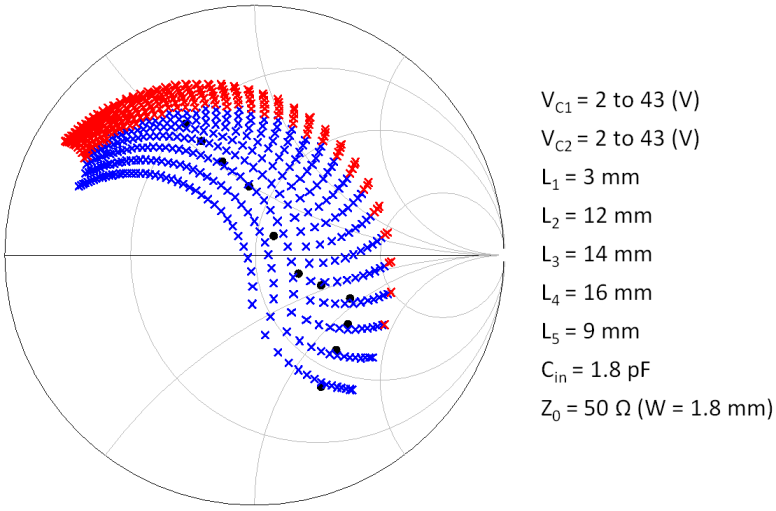


Figure 3.30: Impedance coverage of the network of Figure 3.29 for small input powers with the given ranges of control voltages and parameter values.

The important point to mention is that the graph of Figure 3.30 shows the coverage area under small-signal conditions. That is why the sweeping range of the varactor voltages are beyond the limits specified by Equations (3.2) and (3.3). Since with increasing the input power of the load-tuner, the covered area undergoes some kind of deformation and shrinkage, in designing the load-tuner, we should also take into account the large-signal coverage area which makes the tuning process even harder.

The parameter values shown in Figure 3.30, are all found considering this fact. That is why the small-signal coverage region starts at the edge of the impedance point of the first state but extends well beyond the impedance of the last state.

Figure 3.31 presents the coverage area for the extreme input power of 31 dBm. As can be seen, in spite of limiting the control voltages and deformation of the covered area, the optimum points are still located inside the covered area designated by blue crosses.

The loss-factor for the case of small input powers and the highest value of 31 dBm are depicted in Figures 3.32 and 3.33, respectively. It is clear from the second figure that with increasing the input power of the load-tuner, the tuning range of the varactor control voltages are limited even more due to the sharp decrease of the loss-factor such that, for the extreme case of 31 dBm, only a small window is left to choose V_{C1} and V_{C2}. According to the figure except the last point, all the others are still embedded in this small blue area.

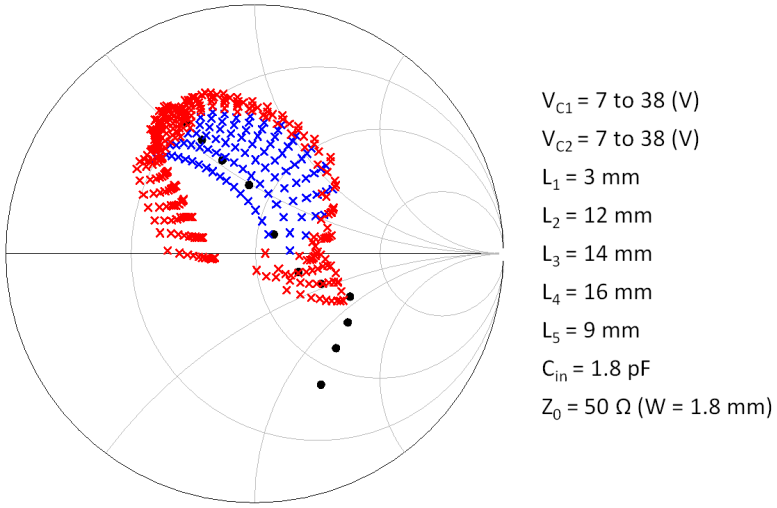


Figure 3.31: Impedance coverage of the network of Figure 3.29 for the input power of 31 dBm with the given ranges of control voltages and parameter values.

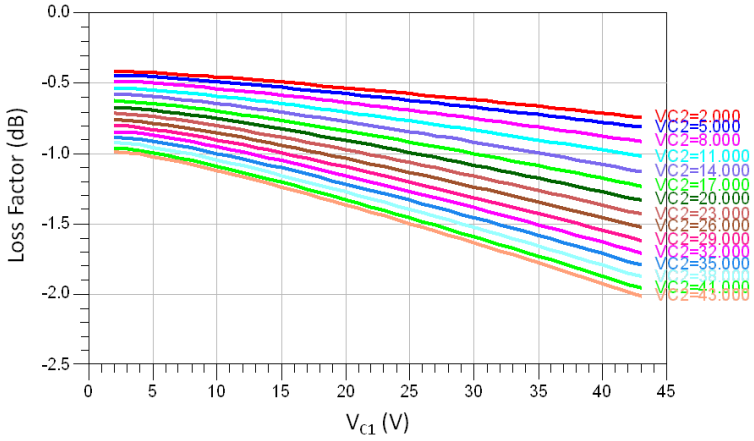


Figure 3.32: Loss factor of the matching network of Figure 3.29 for small input powers.

3.4.7 Load-Pull Analysis Using Varactor-Based Load-Tuner

In order to verify the function of the designed load-tuner, we are going to perform the load-pull analysis once again in order to spot the 11 optimum points which have already found using the built-in ideal load-tuner of the ADS. Table 3.4 compares the optimum load points obtained by the varactor-based load-tuner with those of the ideal one at 11 operational *states* of the amplifier. The input powers in which the impedance points are derived and bias conditions of the transistors are all the same as the Table 3.2. As explained earlier for the first four *states* the optimum load for maximum PAE are being considered while for the rest, maximum delivered power is intended. The control voltages of the varactor stacks which produce the corresponding impedance points is listed in Table 3.5.

Note that along with performing the load-pull analysis to find the optimum load points, due to finding

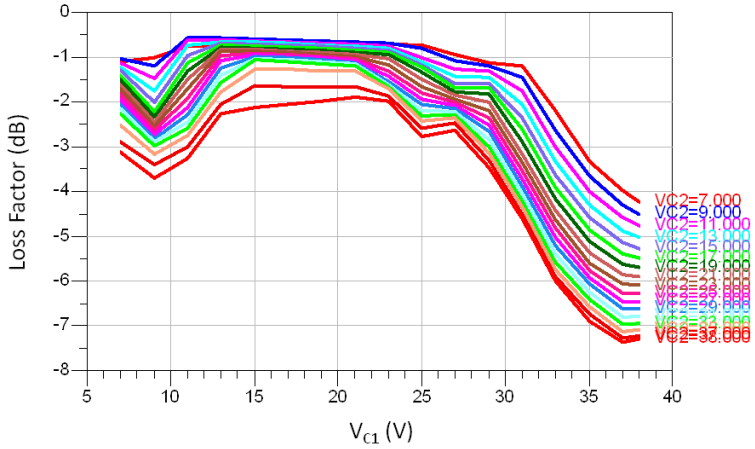


Figure 3.33: Loss factor of the matching network of Figure 3.29 for the highest input power of 31 dBm.

the control voltages of the varactors, we have actually designed the tunable matching network as well. Because it is now known that at each operational *state* of the amplifier which voltages should be applied to the two varactors stacks. A visual comparison has been made between two sets of impedances in Figure 3.34. The black dots represent those points previously found using the ideal load-tuner and the colored points are the new set found using the practical varactor-based load-tuner. The close agreement between two sets verifies the applicability of the designed load-tuner to perform the practical load-pull analysis of the amplifier.

Table3.4: Comparison of the 11 optimum load points obtained by varactor-based load-tuner with those of the ideal load-tuner.

State	P_{in} (dBm)	V_{G1} (V)	V_{G2} (V)	Z_{Lopt} (Ω) (Ideal load-tuner)	Z_{Lopt} (Ω) (Varactor-based load-tuner)
1	10	0.25	0	39.9 – j64.2	40.4 – j56.2
2	17	0.25	0	62.6 – j63.8	63.9 – j61.4
3	18	0.25	0	83.6 – j58.6	73.7 – j50.8
4	19	0.25	0	100 – j42.5	88.4 – j30.5
5	0	0.25	0.15	82.1 – j22	79.8 – j20.3
6	10	0.25	0.2	70 – j10.8	71.6 – j14.0
7	16	0.25	0.3	57.3 + j8.7	58.8 + j9.7
8	20	0.25	0.4	41 + j24.4	40.6 + j25.9
9	21	0.25	0.5	29.6 + j26.4	33.3 + j27.2
10	23	0.27	0.6	22.3 + j27.1	24.5 + j25.7
11	25	0.27	0.6	17 + j27.5	19.1 + j28.3

Table3.5: Control voltages of the varactors corresponding to the 11 operational states.

State	V_{C1} (V)	V_{C2} (V)	Z_{Lopt} (Ω) (Varactor-based load-tuner)	Z_S (Ω) (Varactor-based load-tuner)
1	2	19	40.4 – j56.2	20.5 – j61.6
2	4	16	63.9 – j61.4	22.6 – j63.6
3	5	12	73.7 – j50.8	24.4 – j63.8
4	7	19	88.4 – j30.5	25.1 – j66.2
5	6	11	79.8 – j20.3	25.3 – j63.4
6	7	7	71.6 – j14.0	27.7 – j62.6
7	9	6	58.8 + j9.7	29.8 – j62.0
8	16	6	40.6 + j25.9	35.3 – j60.4
9	20	7	33.3 + j27.2	37.7 – j58.6
10	27	11	24.5 + j25.7	38.3 – j56.5
11	28	35	19.1 + j28.3	39.1 – j55.3

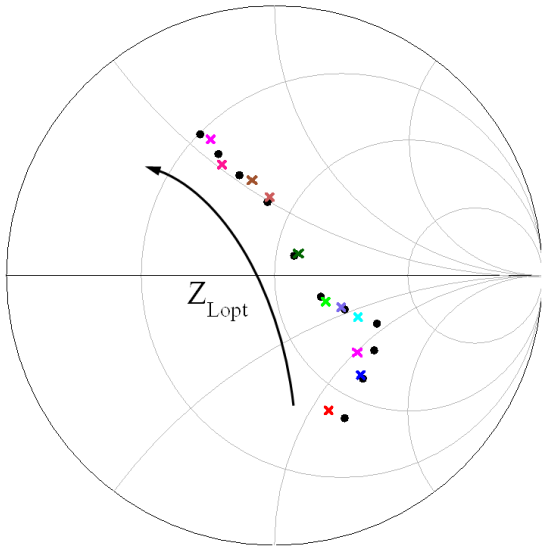


Figure 3.34: Optimum load impedance points at 11 operational states of the amplifier obtained by varactor-based (colored) and ideal (black) load-tuners.

3.4.8 Tunable Input Matching Network

Finishing the design of the output matching network, it is now turn for the input matching. The last column of Table 3.5 is dedicated to the input impedances of the amplifier when the output is terminated at the corresponding optimum load. In order to maximize the gain, we intend to perform a conjugate matching at the input. Therefore the input impedance to be matched at each state is the complex conjugate of the values shown in Table 3.5.

However, as the numbers imply, the variation of the input impedance throughout the entire power and bias ranges is quite smaller than the load impedance. In this condition, a rather less complex tunable matching structure with a higher loss-factor can be chosen to cover the area. One such a network is shown in Figure 3.35. Again the parameter values are all obtained by optimizations and tunings. The complex conjugate of the required input impedances together with the covering area of the tunable input matching network are shown in Figure 3.36. Note that, this time since the power levels are small at the input, there is no need to investigate the high power effects of the TMN.

By designing the input and output tunable matching networks the design of the amplifier comes to an end. In the next section we are going to present the one-tone and two-tone harmonic balance simulation results of the completed amplifier.

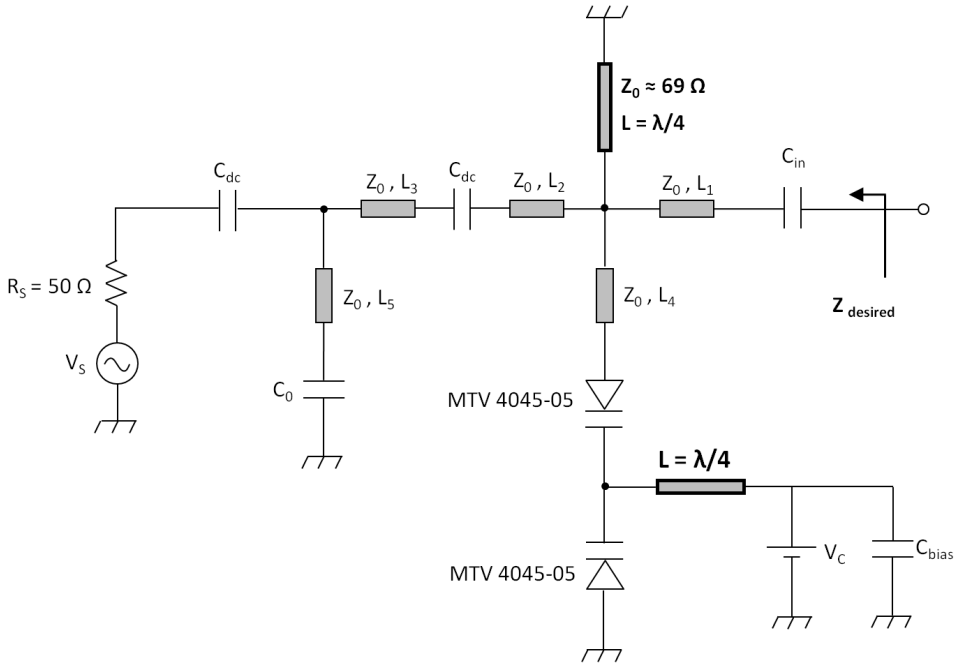


Figure 3.35: Input tunable matching network.

3.5 Simulation Results

In this section, we are going to present the simulation results of the amplifier with the tunable matching networks connected at the input and output. Totally four simulations have been done separately at the 11 operational states of the amplifier.

3.5.1 One-Tone Harmonic Balance Simulation

The first simulation is the one-tone harmonic balance in which a single sinusoidal signal is applied at 2.4 GHz. The input power is swept from -20 dBm to 25 dBm. From this simulation two important

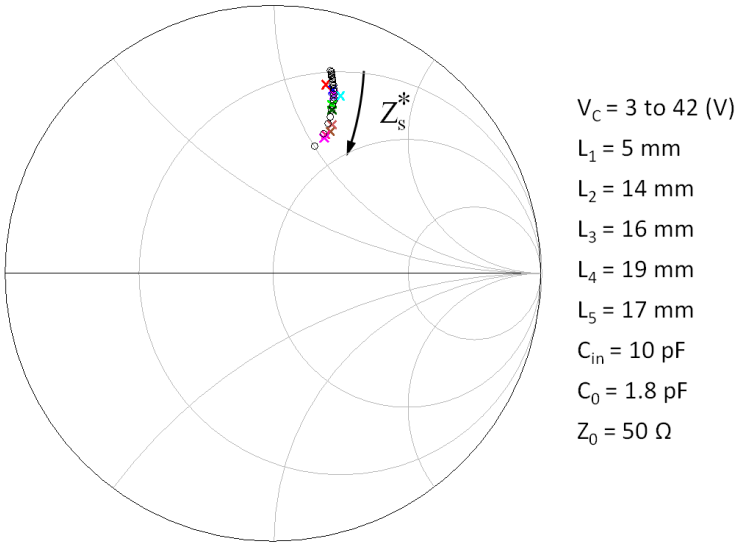


Figure 3.36: Complex conjugates of the input impedances at 11 operational states of the amplifier together with the coverage area of the input matching network.

graphs of power added efficiency and power gain are obtained. Due to the importance of output power in the power amplifier concepts, it is more common in the literature to draw all of the curves as a function of the output power rather than the input power.

The first graph to be presented is the P_{in}-P_{out} curve which is shown in Figure 3.37. It is clear from the figure that by switching between the states from the input power of about 10 dBm to 25 dBm, we have tried to avoid the compression and keep the amplifier in the linear region as will be more discussed in the following. Figures 3.38 and 3.39 illustrate the resulting PAE and gain of the amplifier at its 11 operational states, starting from the leftmost red curve up to the thicker rightmost pink curve.

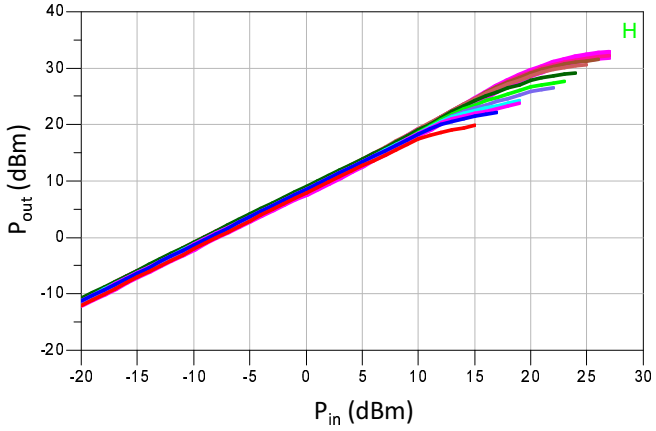
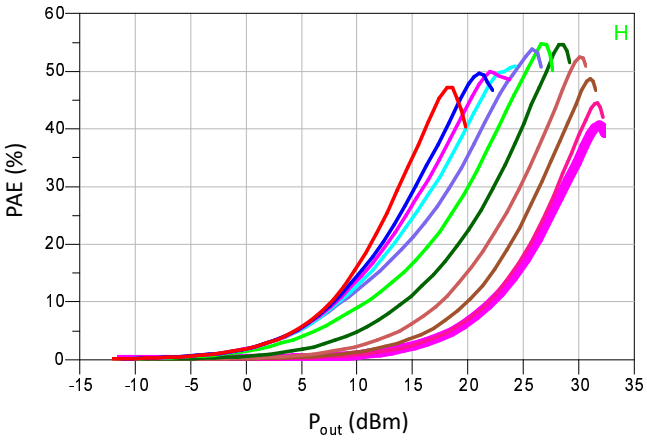
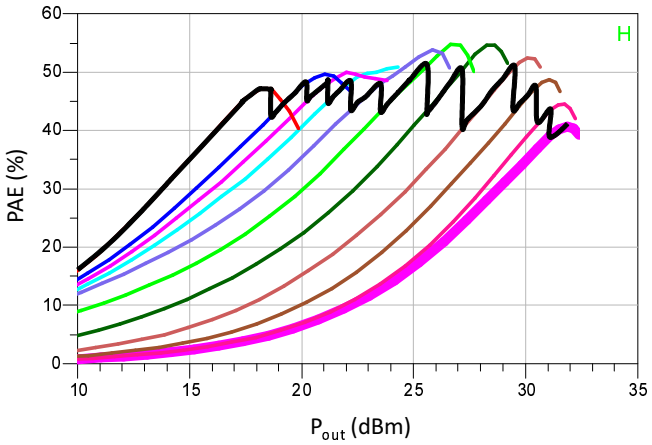


Figure 3.37: P_{in}-P_{out} characteristic curves of the amplifier at the 11 operational states.

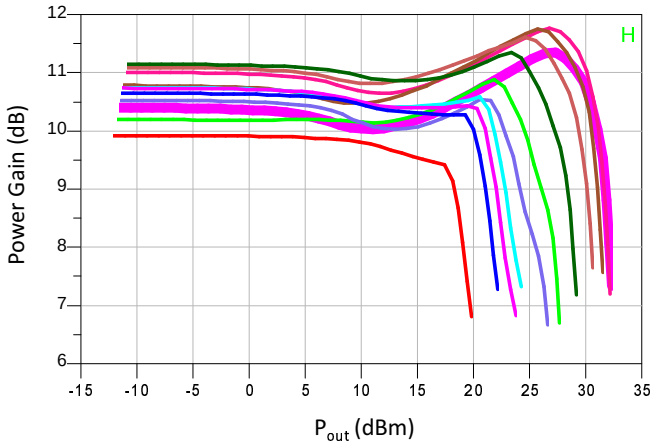


(a)

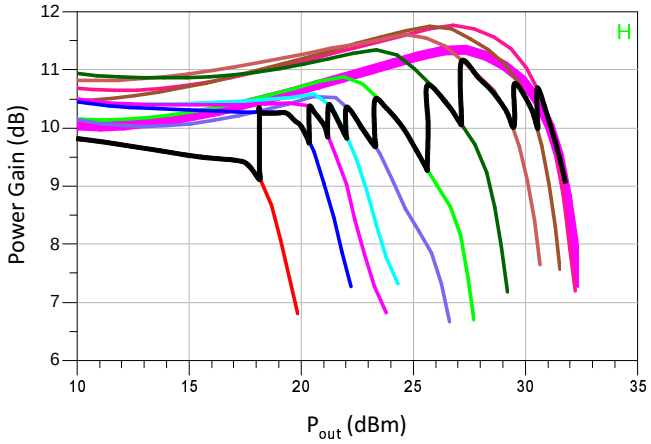


(b)

Figure 3.38: (a) Power added efficiency as a function of the output power at 11 operational states of the amplifier, (b) zoomed view of the PAE where transitions between states at 1 dB compression points are highlighted.



(a)



(b)

Figure 3.39: (a) Power gain as a function of the output power at 11 operational states of the amplifier, (b) zoomed view of the gain where transitions between states at 1 dB compression points are highlighted.

In the lower part of each figure, a zoomed view of the transition region between the states is shown where the final results are highlighted by black curves drawn on the corresponding segments of the different states. Note that here we have chosen the 1 dB compression points as the criteria for switching between states. One can also prefer the levels of 3rd order IMD for switching as will be demonstrated later after the two-tone analysis results.

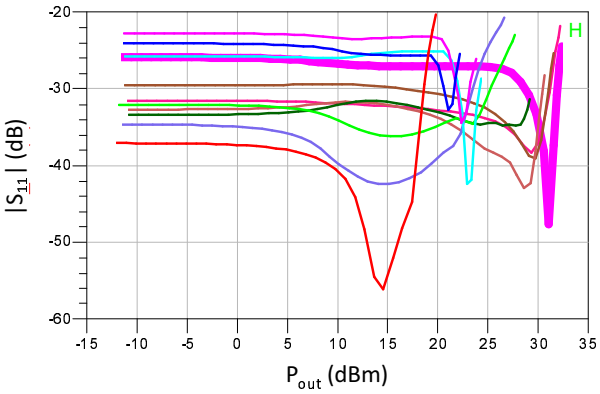
According to the figure of the PAE, from output power of about 16 dBm, we have reached the PAE value of over 40% and been able to maintain the PAE at the average value of around 45% up to the 1 dB compression point of the last state which 31.8 dB. This means that, using our design methodology we have been able to keep the efficiency nearly constant from the 15.8 dB back-off, while preventing the linearity degradation at higher output power levels. In other words, if we were to operate the amplifier only in the last state in order to achieve the maximum P_{1dB}, we would loose the efficiency significantly at reduced drive levels such that at the output power of 16 dBm the PAE level would drop to 3%. On the other hand, if we intended to operate the amplifier only in its first state in order to achieve maximum efficiency at lower input powers, then we had to accept the very low output P_{1dB} of 18.4 dBm. However, using our new topology and switched biasing together with the tunable matching network, we can now fulfil both of the requirements at the same time.

Now consider the gain curves of Figure 3.39. Due to power match rather than the conjugate match at the output, we have lost from the gain of our amplifier which is assumed to be compensated by a pre-amplifier. The small-signal power gain of the first state is about 10 dB. Before the gain drops to 9 dB switching to the second state should be taken place and this process continues until the gain drops to 9 dB at the output P_{1dB} of the last state. In state selection, we have tried to keep the gain variations in state transitions, around the initial 10 dB value. It means not to drop below 9.5 dB and not to exceed over 10.5 dB, so that we can maintain the average value of 10 dB in the back-off region. Except for one case of switching from state 7 to 8 which gain has reached over 11 dB at the point of switching, in the other cases it is kept below that level. By more precise selection of the consecutive states we can avoid these sort of discrepancies in the design.

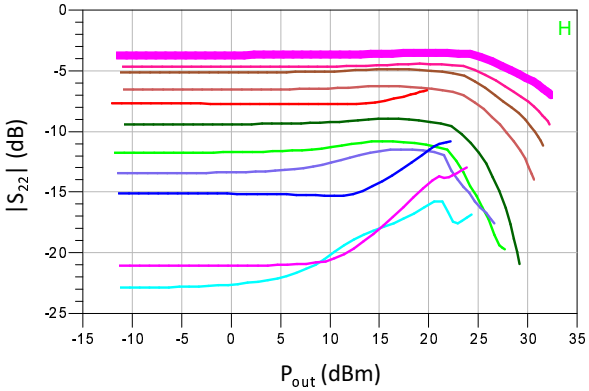
3.5.2 Large-signal S Parameters Simulation

Our second simulation is called Large Signal S Parameter simulation known as LSSP in ADS. In fact, it is also a harmonic balance simulator which gives the S parameters of a network as a function of power, rather than the frequency. From the important results that can be obtained using this simulation are the magnitudes of S_{11} and S_{22} which is useful in calculating the input and output return loss or VSWR of the amplifier. Figure 3.40 (a) to (c) present the magnitude in dB of S_{11}, S_{22} and S_{12}, respectively.

According to the figure, due to conjugate matching with a low loss network, the magnitude of S_{11} at all of the operating states is well below -20 dB which is a perfect result. On the other hand, again due to efficiency or power match at the output rather than conjugate matching, a considerable reduction in S_{22} performance can be seen, as expected. At the small-signal region of the first state, we have a $|S_{22}|$ of about -7.8 dB. This is while at the worst case of state 11, considering the fact that the state would be active after the output power of 31 dBm, the magnitude of S_{22} is below -6 dB. The magnitude of S_{12} is well below -18 dBm which is also very favorable.



(a)



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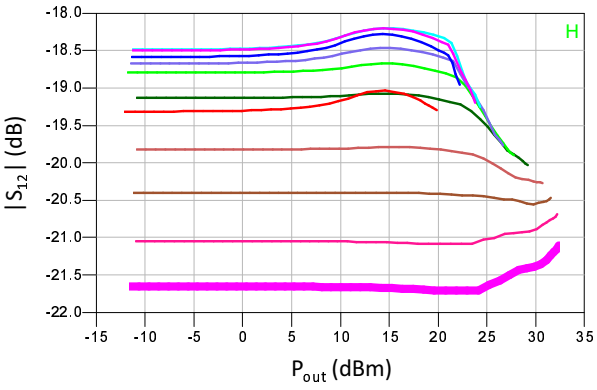


(c)

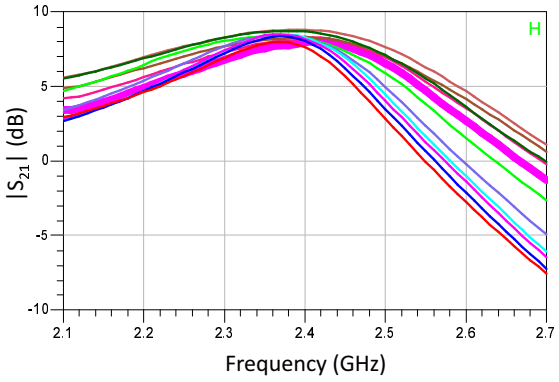
Figure 3.40: Magnitude in dB of (a) S_{11}, (b) S_{22} and (c) S_{12} as a function of output power.

3.5.3 Bandwidth Simulation

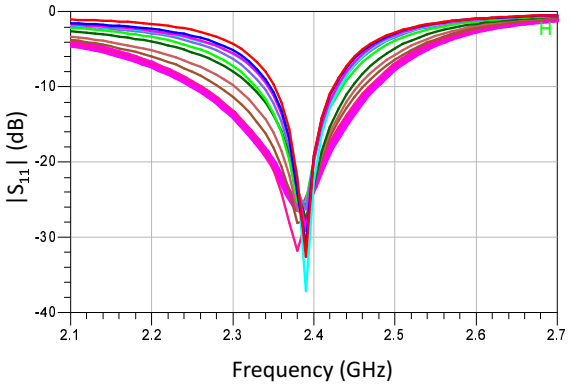
The third simulation is performed to determine the frequency bandwidth of the amplifier over which we had no monitoring throughout the design procedure and hence we expect narrowband results. For this purpose, we again set up a LSSP simulation engine, but this time the frequency is set to be the sweeping parameter and as the input driving power, we specify a single P_{in} value for each individual state which is in the middle of the operational power range of that state. Figure 3.41 (a) to (c) respectively present the magnitude in dB of S_{21}, S_{11} and S_{22} as a function of frequency.

As the graph of the gain or $|S_{21}|$ suggests, there is an increasing trend in the bandwidth of the amplifier from the first state up to the 8th state after which it starts to shrink again. Therefore we have the narrowest bandwidth for the first state.

If the bandwidth is defined according to the points where the gain drops 1 dB below its maximum value, then the bandwidth for the first state would be 118 MHz with the exact center frequency of 2379 MHz. This value extends up to 243 MHz at the center frequency of 2393 MHz for the 8th state. The perfect match at the input and the degraded output VSWR due to power and efficiency matching rather than conjugate matching, can again be readily seen from the $|S_{11}|$ and $|S_{22}|$, respectively.



(a)



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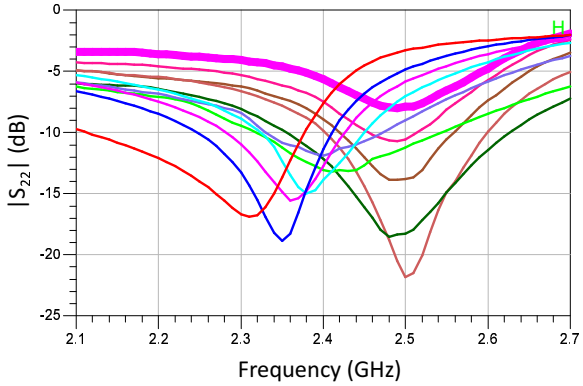


(c)

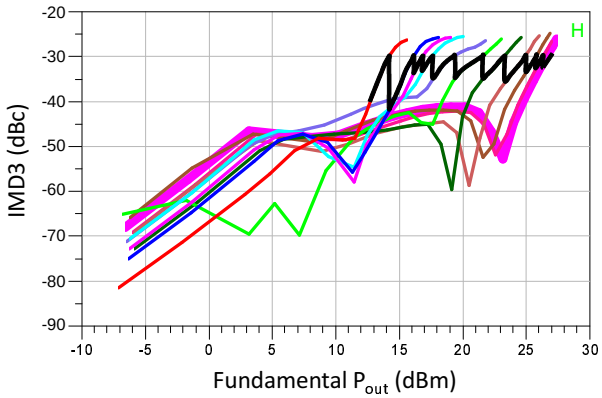
Figure 3.41: Magnitude in dB of (a) S_{21}, (b) S_{11} and (c) S_{22} as a function of frequency.

3.5.4 Two-Tone Harmonic Balance Simulation

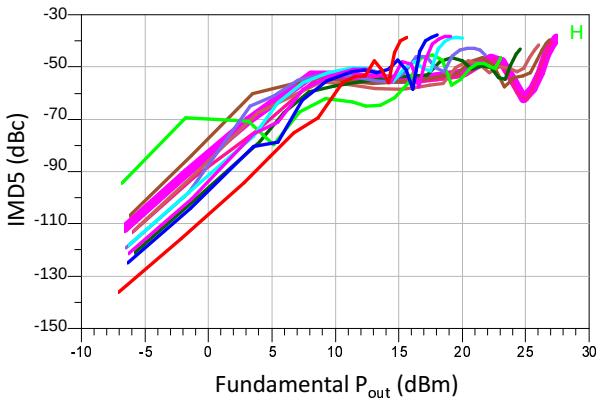
The last but not the least is the two-tone harmonic balance simulation of the amplifier. At this stage, two sinusoidal input signal with a tone separation of 1 MHz, were applied to the amplifier. The mixing order was set to be 7 in order to obtain more accurate results. In this way, in calculation of the IMD3 not only the direct term of $2f_2$-f_1, but also two higher order terms that contribute to the IMD3 level namely, f_2+f_2+f_1-f_1-f_1 and f_2+f_2+f_2-f_2+f_1-f_1-f_1 will be considered. Resulting IMD3 and IMD5 curves as a function of fundamental output power are shown in Figure 3.42. It is common to express the IMD levels in dB per carrier (dBc) which means that it is the ratio of the power of the intermodulation product and fundamental tone or carrier.

The first point that is evident from the graphs is the presence of the large-signal sweet-spots in all of the 11 states due to wisely selecting the biasing points at the first stages of the design. In most of the higher order states not only is there a sweet-spot, but also both IMD3 and IMD5 curves deviate from their normal behavior and present a nearly flat region at high output powers just before reaching the sweet-spot. This anomalous behavior also play a major role in reducing the intermodulation level.

As already stated, we could set the state transition criteria not by 1 dB compression point but using IMD3 or Adjacent Channel Power Ratio (ACPR) in case of a modulated input power. Like the PAE and gain curves, a black path is also drawn on the IMD3 curves of the Figure 3.42 which represent the level of IMD3 within the state transition region. The criteria for switching to higher states is chosen to be exceeding the -30 dBc level. The amplifier operates in the first state until the carrier power reaches to about 14 dBm where transition to second state takes place and reduce the IMD3 level. By continuing this process we are able to keep the IMD3 level at the average value of -33 dBc throughout the back-off region from the output carrier power of 13 dBm up to about 27 dBm.



(a)



(b)

Figure 3.42: (a) Third and (b) fifth order intermodulation products as a function of fundamental output power.

CHAPTER 4

EXPERIMENTAL RESULTS

4.1 Introduction

For RF and microwave engineers, while on one hand the design stage of a circuit may offer special challenges, on the other hand, the practical implementation of the circuit and getting the desired results has its own difficulties demanding not only the knowledge but rather experience. That is because as the frequency increases, the number of parasitics and second order effects that are not or can not be taken into account during the design and simulation stage also increases, giving rise to inconsistent experimental results.

In my design also at first I was not able to obtain any gain from even a single transistor and encountered a perfect oscillator when I connected the two transistors as in the simulations. For the case of the load-tuner, the desired region of the Smith chart was not covered and the loss of the network was extremely high, rendering it totally useless. So I decided to investigate in a component level and proceed step by step while troubleshooting at each stage. This chapter is dedicated for all of these intermediate steps that finally lead to the desired results and meanwhile made me attain a lot of practical experiences, making my PhD research period even more worthwhile.

In the next two sections of this chapter, the implementation process and measurement results of the amplifier and load-tuner are going to be discussed, respectively. Later on, the load-pull measurement results are presented and in the final section, the measurement results of the completed design containing the amplifier and input/output tunable matching networks are displayed. As was told in Chapter 3, the substrate of our choice for realizing the circuits is 32 mil Rogers' RO4003C.

4.2 Implementation and Measurements of the Amplifier

For the first time when I realized the amplifier of Figure 3.5 as it was simulated in the ADS environment, no gain could be obtained from the amplifier. Moreover, there were current flows from the gate ports of the both transistors which should definitely not be the case for an HEMT device like ATF-50189. The first thing that must be found out was to check whether the transistors are working properly or they are burned out.

For that I sketched a small board on which a single transistor could be mounted for testing. The fixture is shown in Figure 4.1. The gate and drain biases are applied using external Bias-Tees as shown on the figure. For checking the transistor, it is biased to a point where the S-parameters are given in the datasheet for that point and then compared with the measured ones. As an example for one of the

working transistors the two S-parameter sets are presented in Figure 4.2 for biasing conditions of V_{DS} = 4.5 V and I_{DS} = 280 mA[1].

Being able to properly bias the transistor to a given point and obtaining the S-parameters similar to the datasheet, implies that the active device is behaving properly and can be mounted on the amplifier board. After testing both of the transistors as described, I made sure that the cause of the problem was something else rather than the transistors. In order to find it, I prepared another board for a single transistor with on board gate and drain biasing lines. The schematic and fabricated circuit are shown in Figure 4.3.

Figure 4.1: Fixture for testing the transistors before mounting on the main board.

After testing the transistor, it was mounted on the board with the biasing components as shown in Figure 4.3 (a). The value of the biasing inductor was chosen such that while it provides a high impedance for the RF signal, its Series Resonance Frequency (SRF) is well over 2400 MHz. Not surprisingly, the same problem appeared again. The power gain was nearly zero and the power supply of the gate was showing a current flow and there was a serious instability problem. This gave me the notion that there must be something wrong with biasing circuitry and grounding, because there was no problem in the test board of Figure 4.1 while using standard Bias-Tees.

In the next testing board, I performed two modifications. First, I designed a radial stub structure using ADS momentum in order to provide a better open circuit for the RF signal in the biasing line of the drain port. The schematic of the stub and its Momentum layout are shown in Figure 4.4 (a) and (b), respectively. The lengths shown in the figure are obtained after optimization in Momentum environment and the resulting input reflection coefficient is depicted on the Smith chart of Figure 4.4 (c). A very high input impedance of 8745-j8578 Ω ($|Z_{in}|$ = 12.25 kΩ) could be achieved using this structure.

The second modification was to create a couple of vias in the board and fill them with solder as well as soldering the entire bottom edge in order to connect the top and bottom sides of the board and provide a better grounding. The fabricated circuit is illustrated in Figure 4.5. This time the gate current decreased considerably but the gain was still lower than what was reported in the datasheet. After studying some papers and application notes related to the transistor of our choice and trying a couple of testing boards with single and double transistors, I was finally able to obtain a proper behavior in terms of gain and stability from the circuit of our original two-transistor amplifier.

[1] For smoothing the measured data in the data display window of ADS, some redundant data are inserted at the two extreme measurement frequencies below 0.5 GHz and over 4.5 GHz which describes why the measured curves deviate from their normal trend

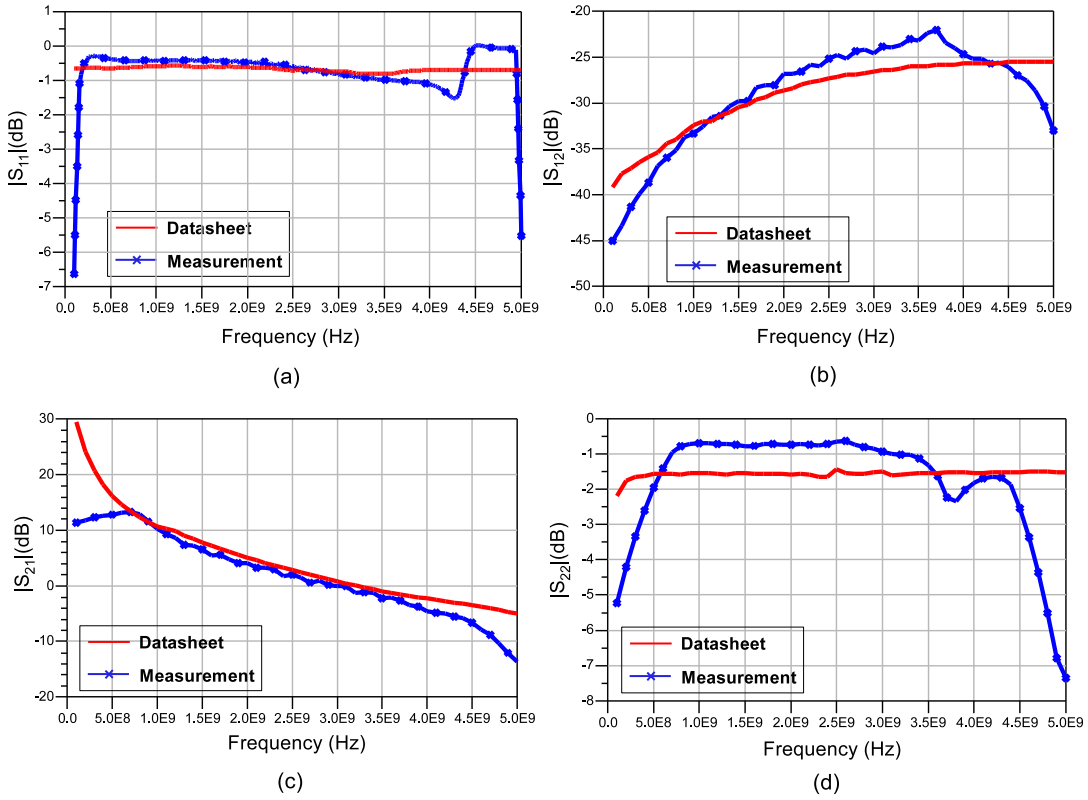


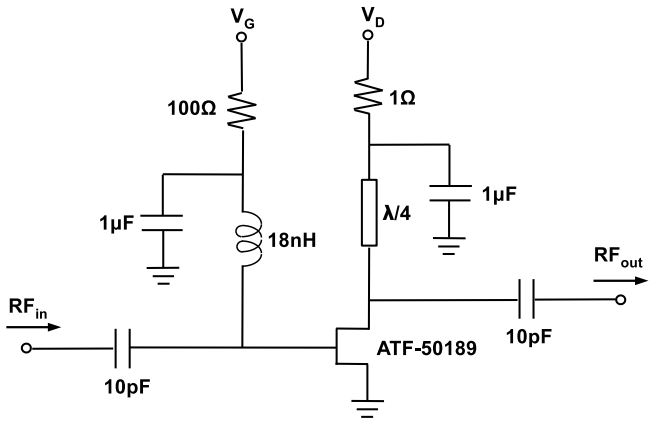
Figure 4.2: Comparing the measured and datasheet S-parameters of a single ATF-50189 transistor under the biasing condition of V_{DS} = 4.5 V and I_{DS} = 280 mA.

In the final board, a lot of random via holes have been created and the drain bias has been realized using three stages of inductors, capacitors and a resistor. The schematic and fabricated circuit are shown in Figure 4.6, (a) and (b). In general, to get the best results the vias holes should have been completely metallized using the LPKF equipment, but due to some problems concerning the chemicals of the equipment, I was not able to perform the metallization process and hence manually filled a couple of random holes with solder until I could get a proper result.

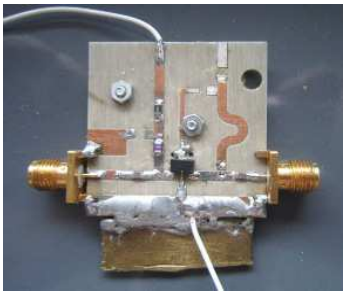
Since the lengths of the transmission lines connecting the gates and drains of two transistors are critical parameters affecting the performance of the whole amplifier, a fine tuning was applied on them using the full wave analysis results of the Momentum embedded in the schematic simulation. Figure 4.7 illustrates the transmission line structure between the transistors analysed in ADS momentum. By defining internal ports in the connection points of the layout, we are able to import the whole structure in the schematic window.

In this way, the full wave analysis of the layout block is performed in Momentum environment and the results are imported into the schematic environment where the measured S-parameters of the active devices together with the S-parameters of the passive components provided by the manufacturers are all integrated in a single circuit of the schematic window as shown in Figure 4.8.

By tuning the lengths of the transmission lines in the schematic window, their respective values are exported as variables to the layout window where the Momentum analysis runs and sends the intermediate results back to the schematic environment and the final S-parameters of the whole structure



(a)



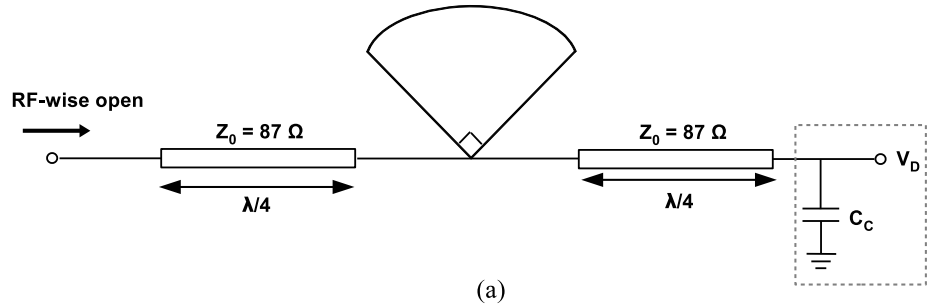
(b)

Figure 4.3: (a) Schematic and (b) fabricated testing board of a single transistor with gate and drain biasing lines.

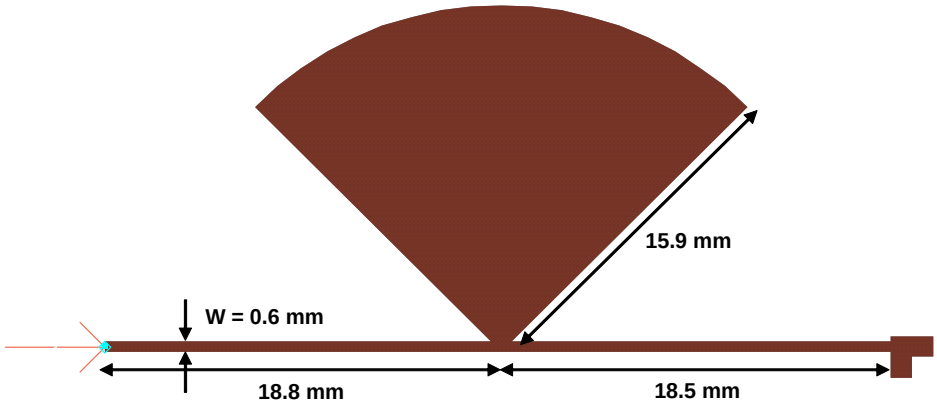
can then be viewed on the display window. In the tuning process, it was tried to get the best results in terms of gain and stability at different biasing points. The lengths of the lines obtained after the final tuning are those shown in Figure 4.6 (a). The measured S-parameters of the fabricated circuit at three sample biasing points are presented in Figure 4.9 The drain biasing voltage is fixed at 4.5 V in all of the experiments.

It can be seen that even without the input and output matching networks connected, due to proper adjusting the lengths of the transmission lines, an approximate matching conditions prevails such that the gains are over 9 dB for all biasing points and the input and output return losses are quite satisfactory. This condition actually simplifies the design of the matching networks to be discussed in the next section.

Another important point that was revealed during the S-parameter measurement was that the amplifier is not unconditionally stable for the gate biasing voltages of $V_{G1} < 0.36$ V and $V_{G2} < 0.3$ V. As an example, the stability factor for the biasing conditions of $V_{G1} = 0.3$ V and $V_{G2} = 0.25$ V is calculated using the measured S-parameters and sketched in Figure 4.10 (a) which shows the stability factor has a value under 1 for the frequency of interest. Also for this biasing point, the output power spectrum is shown in Figure 4.10 (b) while a 0 dBm single-tone signal is applied at the input. Dropping of the



(a)



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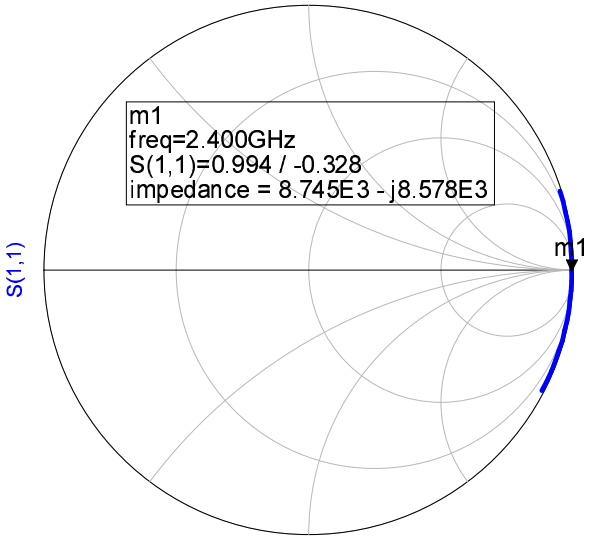


(c)

Figure 4.4: (a) Schematic, (b) ADS Momentum layout and (c) input reflection coefficient of the radial stub biasing structure for the drain.

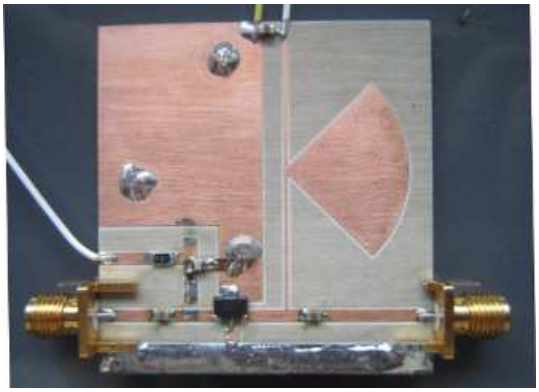


Figure 4.5: Fabricated circuit of the single transistor amplifier with radial stub drain biasing and three solder-filled via holes.

gain and emerging of other spectral components are also signs of instability.

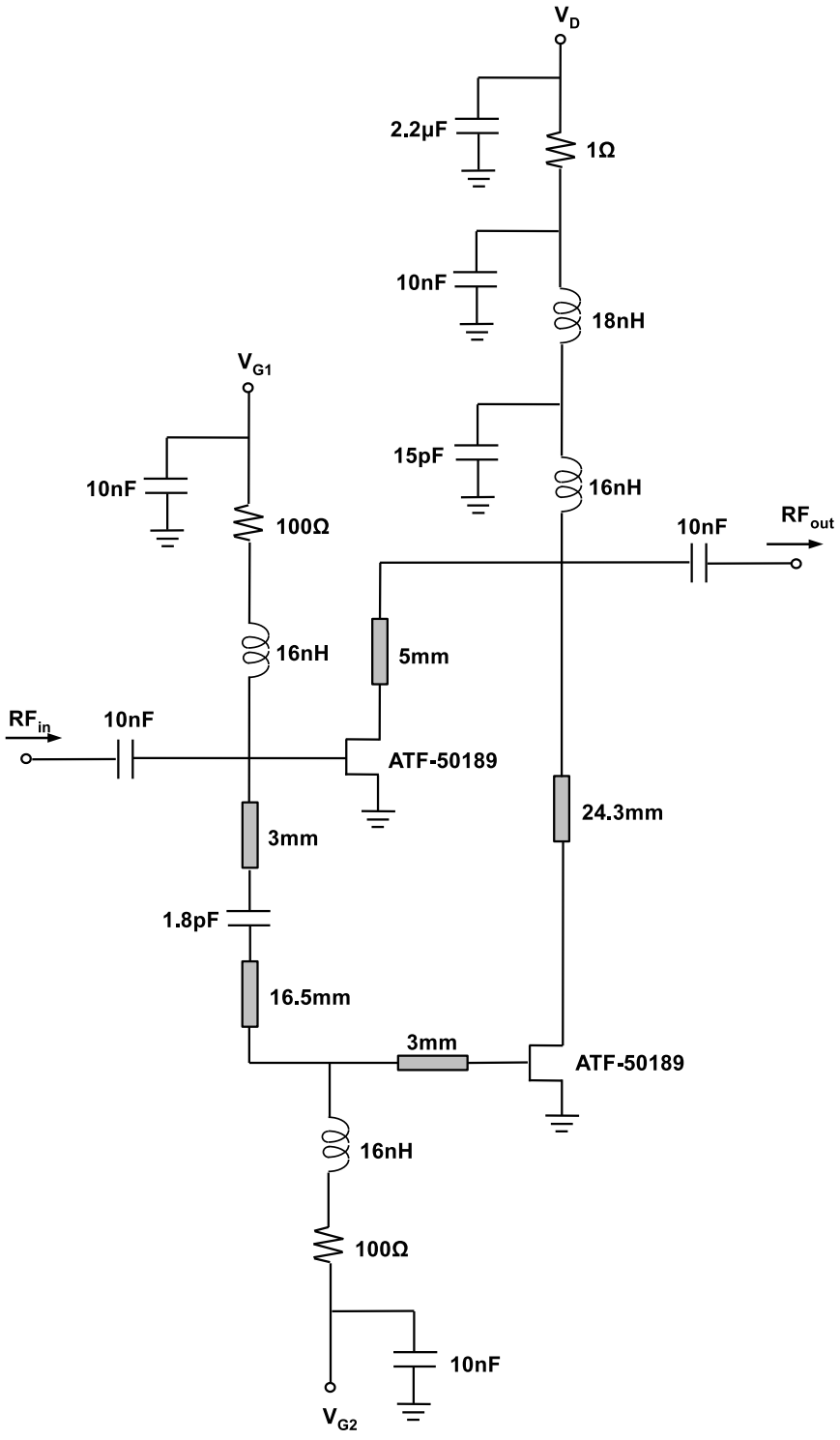
4.3 Implementation and Measurements of the Tunable Matching Networks

Designing the tunable matching network such that it can provide an accurate matching conditions was in fact a challenging task in practice. When I first fabricated the load-tuner based on the varactor model and the parameter values used within simulations, the result was totally unacceptable and disappointing. The loss of the network was pretty high and the covered area of the Smith chart was a tiny region. That is why I had to start the design from the scratch using the real components. The first step was to precisely characterize the varactor structure which in our design it should be considered as a stack of 2×2 varactors in anti-series configuration. After finding an accurate measurement-based characteristics from the stack, the transmission line lengths should be tuned such that we can achieve the desired coverage and loss. The following subsections are dedicated respectively to these two steps of TMN implementation.

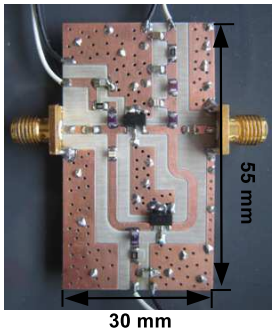
4.3.1 Characterization of 2×2 Varactor Stack

Since in the matching network of our design the varactor stacks are placed in parallel branches where one end of them is directly connected to the ground, the whole stack can be treated as a one port network. For measuring the S-parameters of this network, a simple board was prepared on which the varactor stack consisting of four MTV4045-05 components grounded in one end, together with the biasing inductors, are connecting using a short piece of transmission line to the output connector. The schematic and fabricated board are shown in Figure 4.11. As can be seen, it is a one port network whose S-parameters can be measured using a network analyser with a 1-port calibration.

The important point to mention is that the measured S-parameters of this structure can not be directly used in the design of the matching network. That is because as already mentioned in the previous chapter, the lengths of the transmission lines connecting the varactor stack to the main line are very critical in determining the loss and covering area of the TMN.


V_D
2.2µF
1Ω
10nF
18nH
V_G1
15pF
16nH
10nF
RF_out
10nF
100Ω
16nH
5mm
RF_in
10nF
ATF-50189
24.3mm
3mm
1.8pF
16.5mm
3mm
ATF-50189
16nH
100Ω
10nF
V_G2

(a)



(b)

Figure 4.6: (a) Schematic and (b) fabricated circuit of the two-transistor amplifier proposed in this thesis.

Figure 4.7: Momentum layout view of transmission lines connected to the gates and drains of the two transistors.

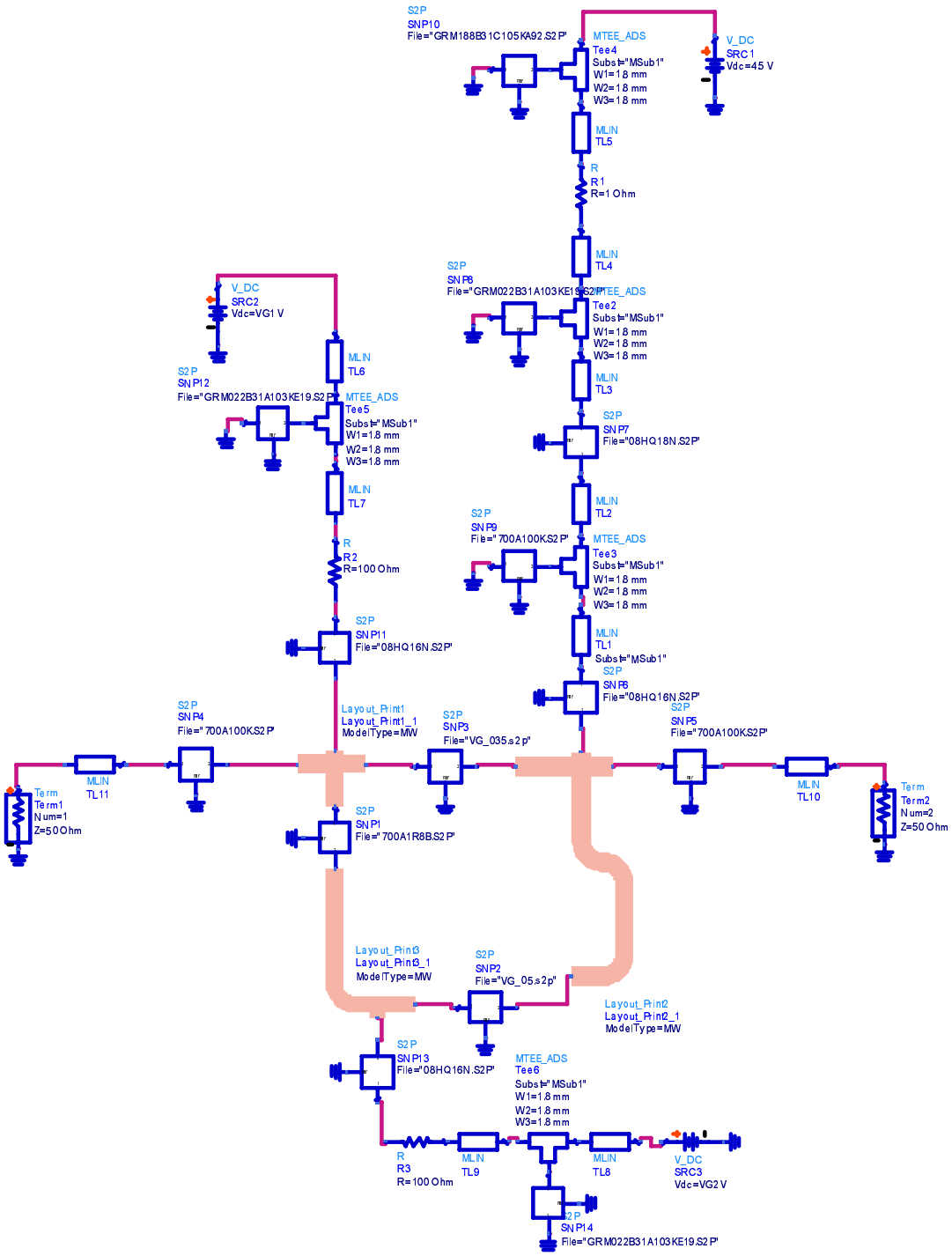


Figure 4.8: Simulated amplifier circuit in the schematic window of ADS where the critical transmission lines connecting the two transistors are analysed in Momentum.

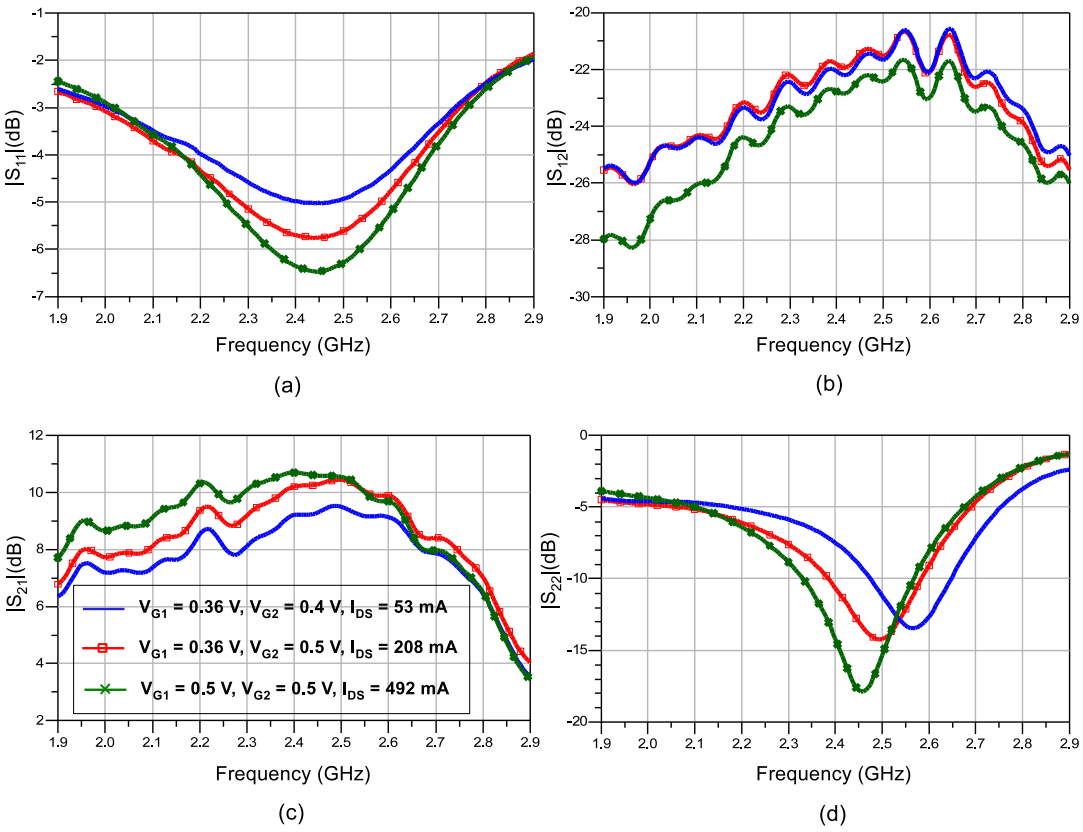
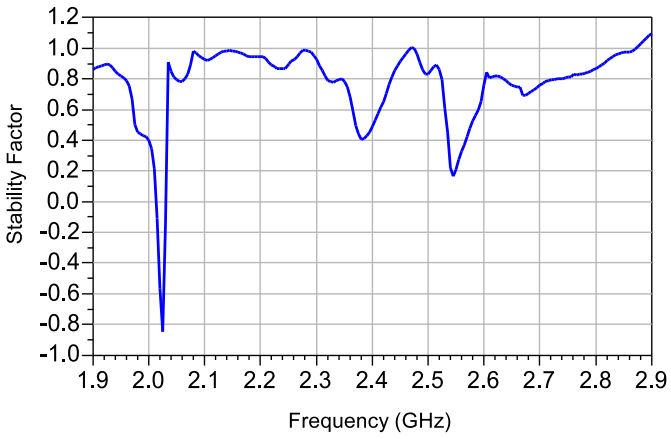
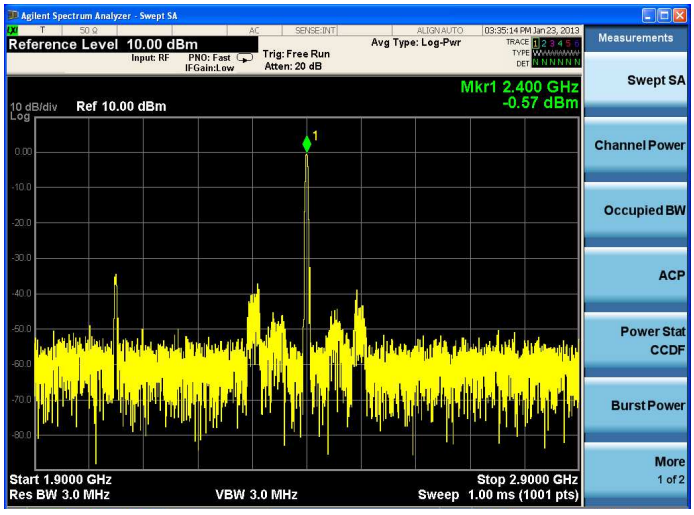


Figure 4.9: Measured S-parameters of the amplifier of Figure 4.6 at three different bias points.



(a)



(b)

Figure 4.10: (a) Stability factor and (b) output power spectrum of the amplifier for V_{G1} = 0.3 V and V_{G2} = 0.25 V.

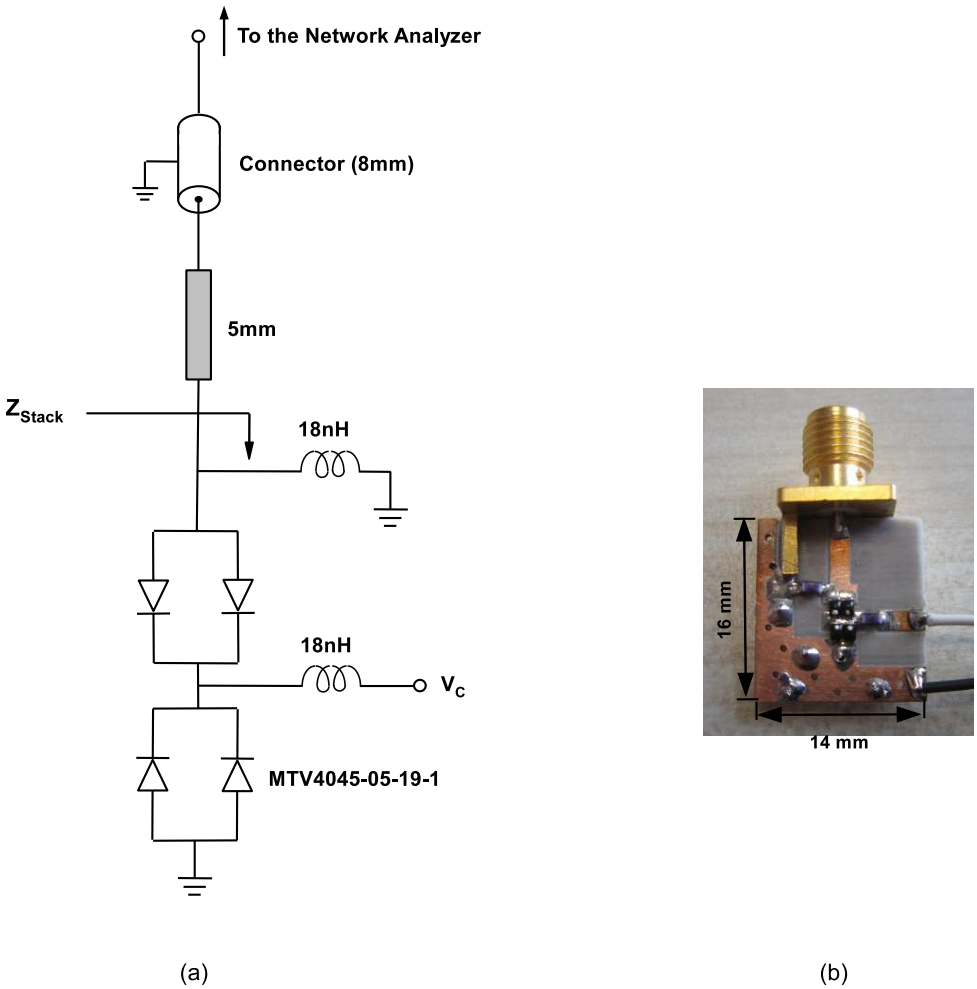


Figure 4.11: (a) Schematic and (b) fabricated board of the varactor stack characterization module.

This necessitate that the effects of the connecting transmission line and the connector itself should be removed so that the impedance of the varactor stack alone, depicted as Z_{Stack} on the figure of 4.11 can be extracted. Although the lengths of these input components are quite smaller than the wavelength, due to their impedance transforming property, they influence the results considerably. In order to de-embed the extra input elements we need to do some maths. First consider the S-parameter description of a standard 2-port network:

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{4.1a}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{4.1b}$$

a_2 and b_2 can be expressed in terms of a_1 and b_1 by finding a_2 from (4.1a) and replacing it in (4.1b),

which results in the following two equations:

$$a_2 = \frac{b_1 - S_{11}a_1}{S_{12}} = \frac{1}{S_{12}}b_1 - \frac{S_{11}}{S_{12}}a_1 \tag{4.2a}$$

$$b_2 = S_{21}a_1 + S_{22}\left(\frac{b_1 - S_{11}a_1}{S_{12}}\right) = \frac{S_{22}}{S_{12}}b_1 + \left(S_{21} - \frac{S_{22}S_{11}}{S_{12}}\right)a_1 \tag{4.2b}$$

Now consider two networks connected in series and terminated with ground (short circuit) in one end as shown in Figure 4.12. This is actually the structure we are dealing with in our varactor stack characterization board of Figure 4.11.

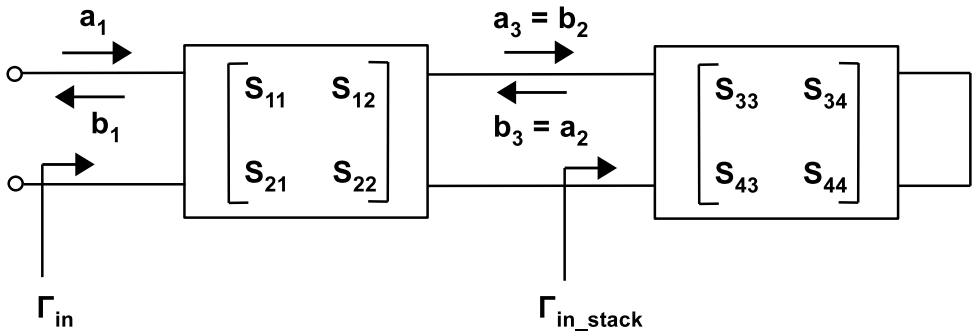


Figure 4.12: Series connection of two networks terminated with short circuit representing the characterization board of varactor stack.

What is known for us in this system is the input reflection coefficient (Γ_{in}) which has been found through 1-port S-parameter measurement. But what we are looking for is the reflection coefficient of the varactor stack (Γ_{in_Stack}) which can be calculated as follows:

$$\Gamma_{in\_Stack} = \frac{b_3}{a_3} = \frac{a_2}{b_2} \tag{4.3}$$

By replacing a_2 and b_2 from (4.2a) and (4.2b) we have

$$\begin{aligned}
\Gamma_{in_Stack} &= \frac{\frac{1}{S_{12}}b_1 - \frac{S_{11}}{S_{12}}a_1}{\frac{S_{22}}{S_{12}}b_1 + \left(S_{21} - \frac{S_{22}S_{11}}{S_{12}}\right)a_1} \\
&= \frac{(b_1/a_1) - S_{11}}{S_{12}S_{21} + S_{22}\left[(b_1/a_1) - S_{11}\right]} \\
&= \frac{\Gamma_{in} - S_{11}}{S_{12}S_{21} + S_{22}\left[\Gamma_{in} - S_{11}\right]}
\end{aligned} \tag{4.4}$$

According to (4.4), if the S-parameters of the first network, which in our case is the series connection of transmission line and the connector are known, de-embedding of that network can be readily done using Equation 4.4. The required S-parameters can be obtain by simulation using the model of transmission line and connector, provided that their respective lengths can be set as accurately as possible. With reference to my past experiences in measuring the previously implemented matching networks and performing some tuning, I adjusted the lengths and other parameters of the connector and transmission line. The final values and definition of the parameters are shown in the ADS schematic window of Figure 4.13.

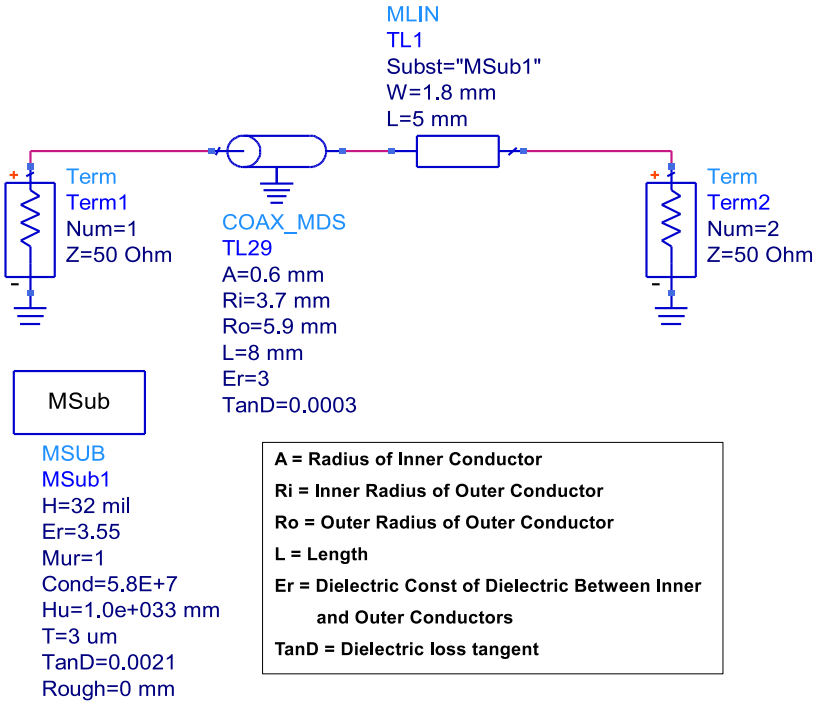


Figure 4.13: Simulated two port network consisting of the connector and transmission line to be de-embedded from the measured S-parameters of network shown in Figure 4.11.

Figure 4.14 illustrates the measured reflection coefficients and the extracted ones after the de-embedding process. The biasing voltage of the varactor stack is swept from 1 V to 40 V. As can be seen clearly on the Smith chart, a substantial rotation of the impedances has been taken place by de-embedding the extra components. Now that we have found the impedance of the varactor stack at different biasing points, we can proceed to the design of the load-tuner based on these data.

4.3.2 Tuning of the Transmission Line Segments

The transmission line segments that need to be tuned in order to get the desired impedance coverage with a low level of loss, are L_{mid}, L_{br1} and L_{br2} as depicted in Figure 4.15. Since the input line length has the sheer effect of rotating the impedance points, it is not initially included in the tuning process.

At this point, I encountered the problem of importing the one-port S-parameters of the varactor stack at different biasing points which were derived in the previous section after the de-embedding stage. I had

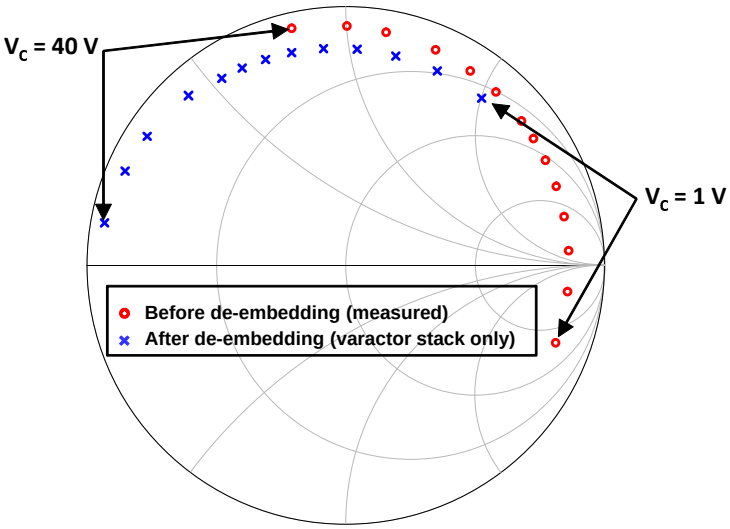


Figure 4.14: Input impedance points before and after de-embedding the effect of input line and connector.

to find a way to make the ADS automatically read several 1-port touchstone files (.s1p) at the same time for the two branches of the load-tuner and display the resulting input impedance on the Smith chart. Unlike the simulation using the model of the varactor where the applied biases could be swept by the simulator, this time the sweeping should be done between different files.

After carefully inspecting the Data Access Components (DAC) of the ADS environment, I could find a way to overcome the problem using an item called Multi-Dimensional 2-Port S-parameter File (S2PMDIF) which is located in the Data Items palette at the schematic window of ADS. One of the file types that this item can interpret is Measurement Data Format files with the extension of .mdf. The content and structure of an mdf file is similar to a s2p file with the major difference that in an mdf file several s2p data can be inserted and a variable is defined within the file which serves as a counter for the s2p data to be read by the S2PMDIF module in the schematic window. The same variable should also be defined in the schematic environment. Figure 4.16 presents an example of how this data component can be utilized in ADS. The variable “CNTR” is the one defined inside the “varactor.mdf” which is the file being read by S2PMDIF component. The variable “cntr” which is defined on the schematic and swept by the ParamSweep component is actually the value of the variable “CNTR”. A truncated version of a sample mdf file can be found in the Appendix.

The only problem left is that the S2PMDIF component can read the mdf files inside which the data are organized in the form of s2p file rather than s1p file which is the case in our design. Since there is not such a component as S1PMDIF, to solve the problem I converted the s1p files into s2p files by just adding zeros for the missing values of S_{12}, S_{21} and S_{22} and then inserted the resulting s2p data into the mdf file. But in order to get the correct results in the simulation, the second ports of the S2PMDIF components should be terminated with 50 Ω loads as shown in Figure 4.17.

As previously described in the amplifier case, for obtaining more accurate results in this simulation as well, the three main transmission lines to be tuned, are prepared as a single layout component rather than schematic models. In this way, the full wave analysis of the ADS Momentum can be performed on them and the results then imported to the schematic.

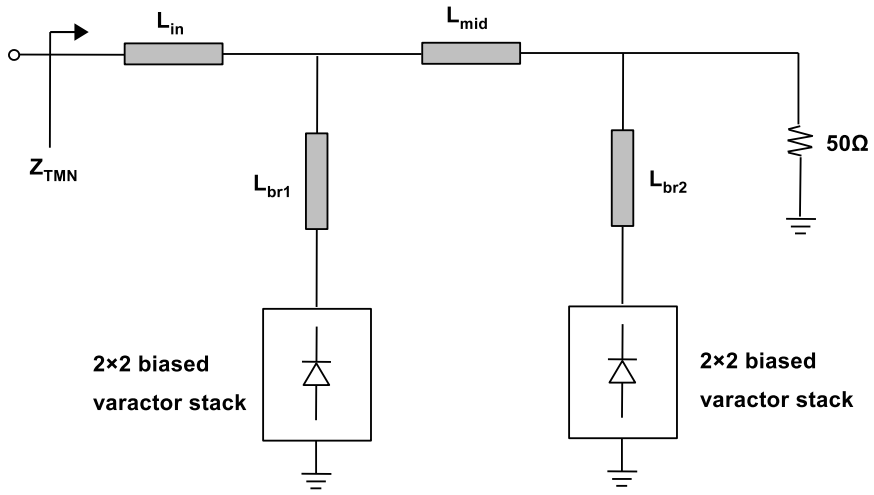


Figure 4.15: Schematic of the load-tuner showing the critical transmission line segments to be tuned.

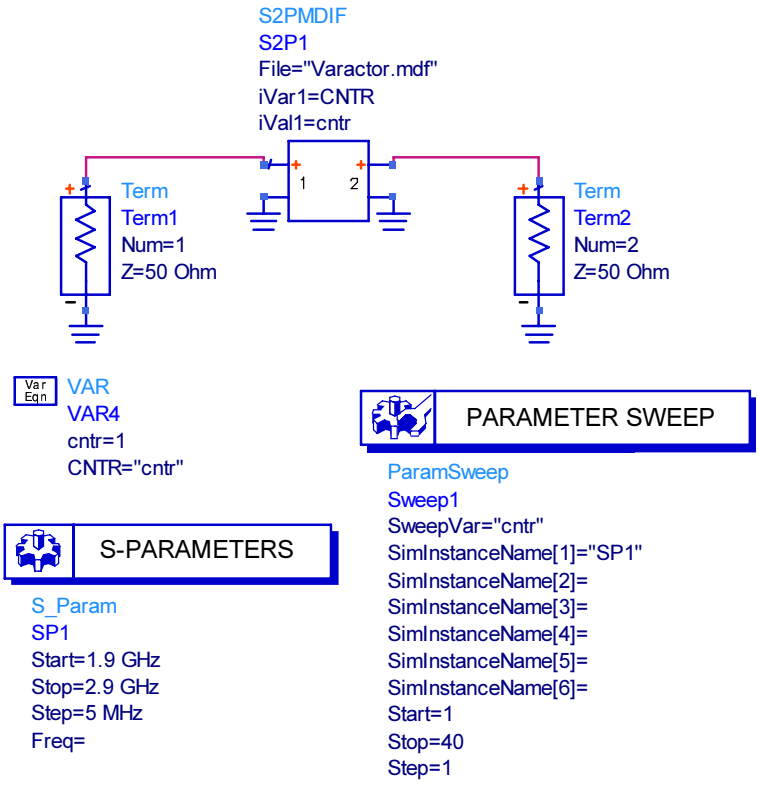


Figure 4.16: Sample ADS schematic showing how to employ an S2PMDIF data item in order to sweep between several s2p data.

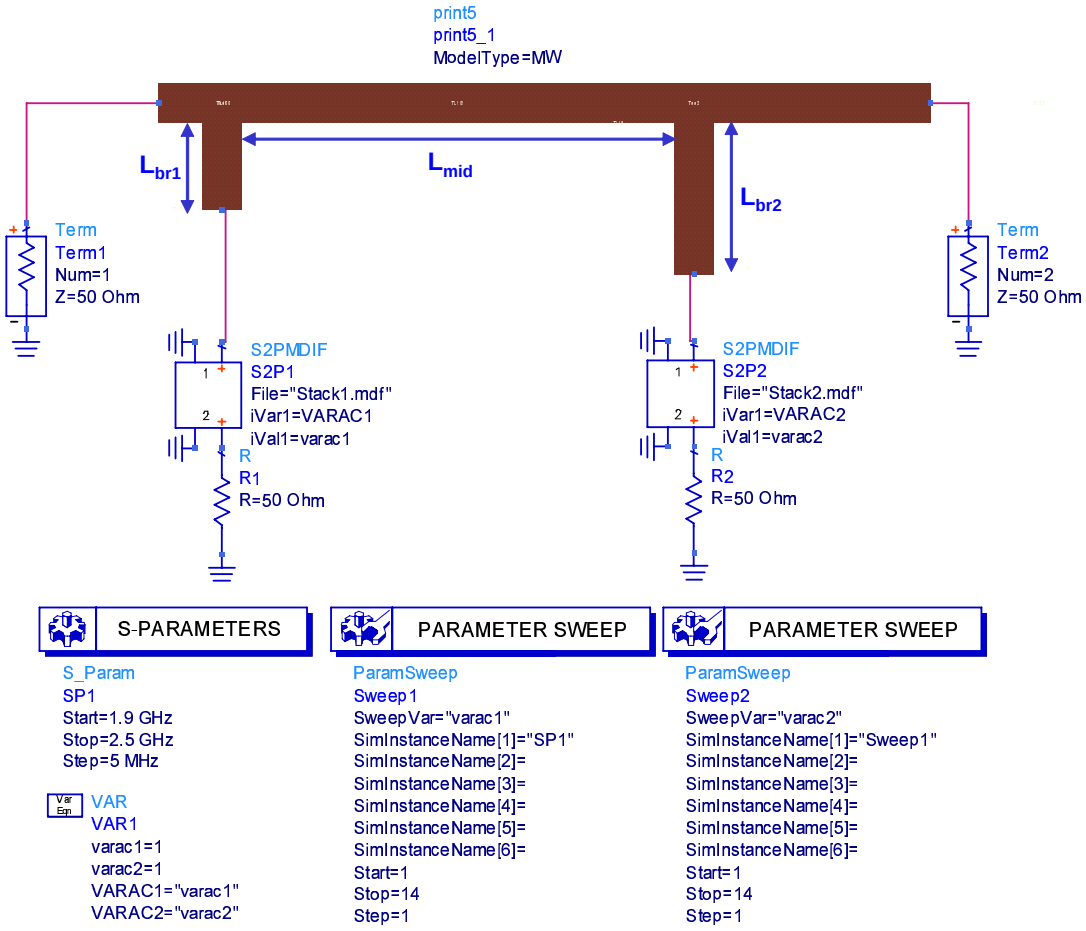
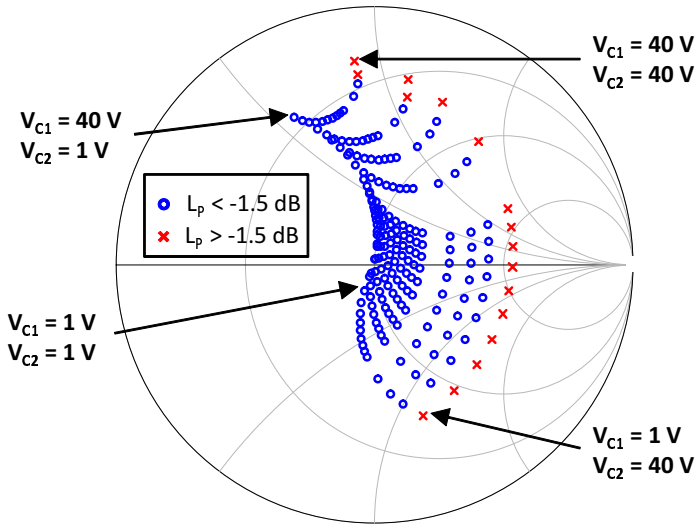


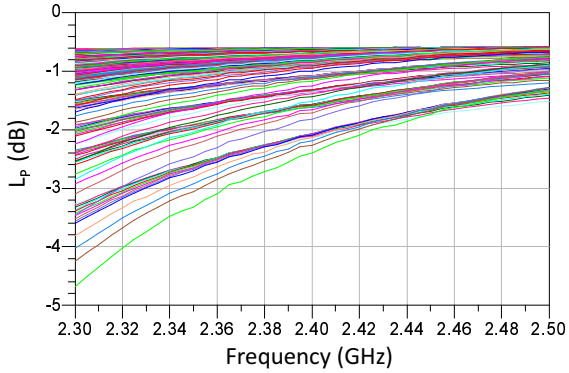
Figure 4.17: Load-tuner simulation setup in ADS showing S2PMDIF components for each varactor stack and the imported layout of the intervening transmission lines.

Through the optimizations, two criteria were taken into account. First the load-tuner should be able to cover the area of Smith chart containing the points of the Figure 3.17 and their surrounding region. Secondly, the loss value to achieve as defined by Equation (2.22), should set to be over -1.5 dB. For limits under this value the loss becomes too large and for limits over -1.5 dB the covering area shrinks to small regions, both of which degrades the performance of the matching network.

The final covered area after the optimizations and corresponding loss values are demonstrated in Figure 4.18 (a) and (b), respectively. For comparison purposes the same graphs are also shown for different sets of line lengths in Figure 4.19. For the case of Figure 4.19 (a) and (b) the covered area is quite expanded while very high loss values are present. On the other hand, in Figure 4.19 (c) and (d), the loss value is reduced well below -1.5 dB but this time the covering capability of the network has been reduced. Note that on the Smith charts of Figures 4.18 and 4.19, the impedance points depicted by blue circles are the points with L_P over -1.5 dB which are considered as points with acceptable level of loss. The fabricated circuit of the load-tuner is shown in Figure 4.20. Having the amplifier and the load-tuner, the impedance seen from the input of the amplifier at different bias points and load values can now be measured in order to design the input matching network which is going to be explained in the next section.

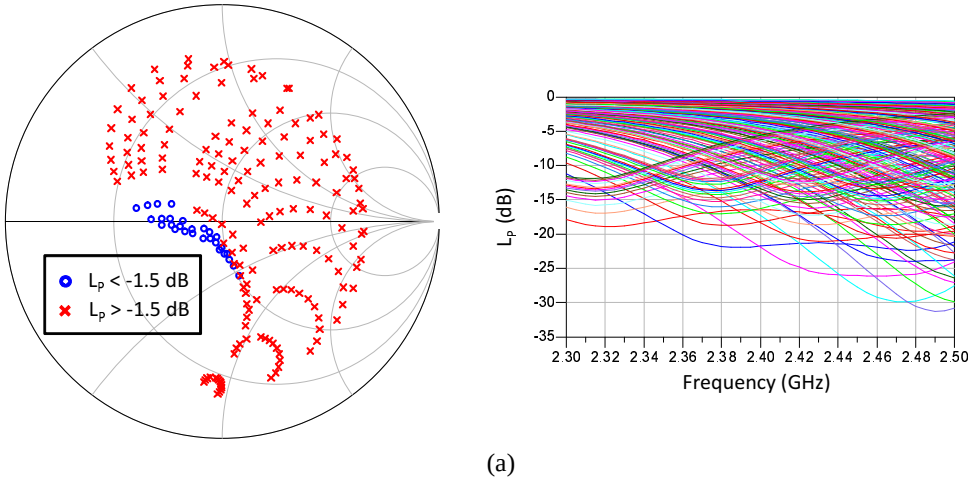


(a)

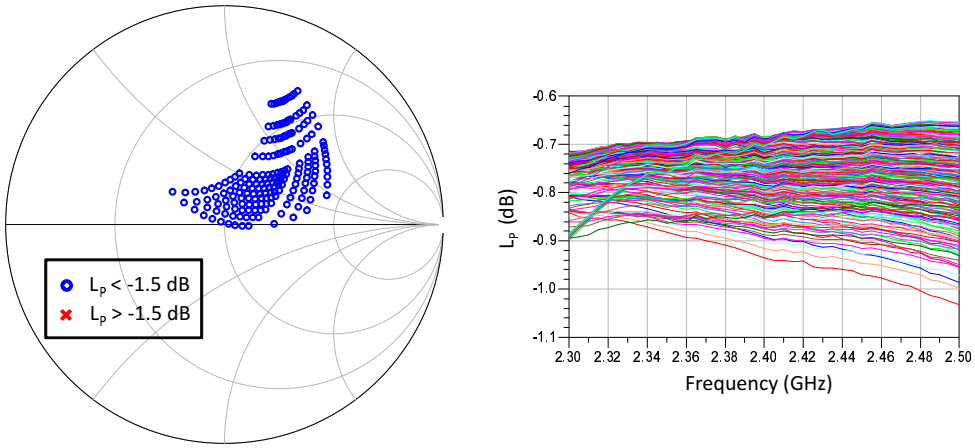


(b)

Figure 4.18: (a) Covered area and (b) loss of the load-tuner for transmission line lengths of L_{in} = 32 mm, L_{mid} = 16 mm, L_{br1} = 7 mm, L_{br2} = 6 mm.



(a)



(b)

Figure 4.19: (a) Covered area and loss of the load-tuner for transmission line lengths of L_{in} = 30 mm, L_{mid} = 12 mm, L_{br1} = 20 mm, L_{br2} = 25 mm; (b) Covered area and loss of the load-tuner for transmission line lengths of L_{in} = 10 mm, L_{mid} = 32 mm, L_{br1} =8 mm, L_{br2} = 7 mm.

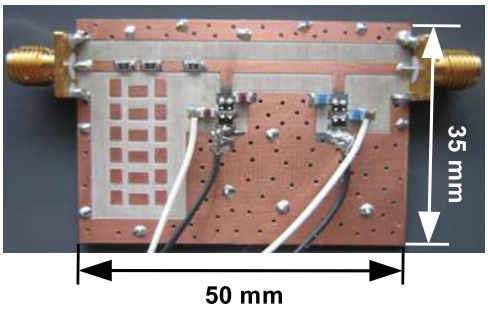


Figure 4.20: Fabricated circuit of the load-tuner or output matching network as a separate module from the amplifier.

According to Figure 4.19, it is observed that the loss vary from very small values of about 0.8 dB to well over 20 dB. The main reason of obtaining such wide range of loss values which primarily depends on L_{br1} and L_{br2} lengths, can be revealed with reference to the impedance points of the varactor stack shown in Figure 4.14. As far as the lengths of L_{br1} and L_{br2} are in the approximate range of 6 mm to 10 mm, due to the impedance transformation property, they transform the impedance of the varactor stack to high values around the open circuit point on the Smith chart which means the decrease of the insertion loss. On the contrary, for the ranges of about 20 mm to 30 mm for L_{br1} and L_{br2}, the impedance of the varactor stacks are transformed to low values around the short circuit point on the Smith chart which means the increase of the insertion loss.

There can also be an explanation in terms of the quality factor. Considering the fact that the quality factor is described by $Q = 1/RC\omega$, by addition of the transmission lines to the varactor stack the overall capacitance value seen at the end of the TL also changes which introduces a loaded Q which can be less or more than the Q of the varactor stack only. When L_p reaches very small levels for L_{br1} and L_{br2} values around 20 mm to 30 mm, it means than the loaded Q has been decreased significantly which results in the increase of the loss.

4.3.3 Implementation of the Input Matching Network

In order to find the exact covered area of the impedance points seen from the input of the amplifier, the load-tuner was connected to the amplifier using an external male-to-male transition while taking into account the extra length that the transition adds to the L_{in} of the load-tuner. Then the S-parameters of the whole module was measured by network analyzer as demonstrated in Figure 4.21.

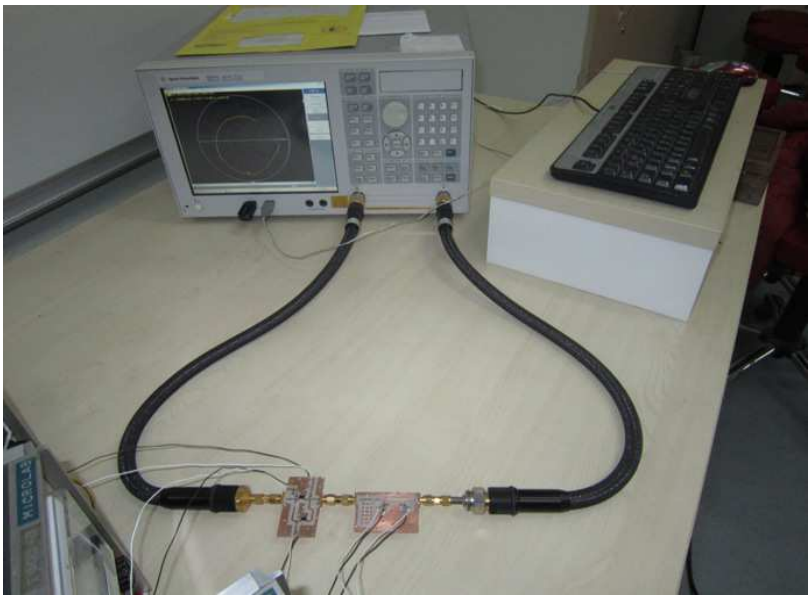


Figure 4.21: Measurement of the S-parameters of the amplifier with load-tuner connected.

By changing the gate bias voltages and load values, different input impedances were obtained. Some chosen samples of the measured impedances depicting the boundaries of the occupied region and some points within the region are shown on the Smith chart of Figure 4.22.

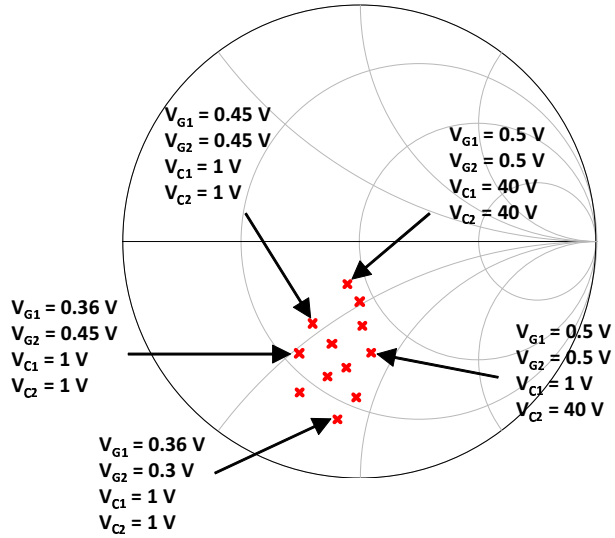
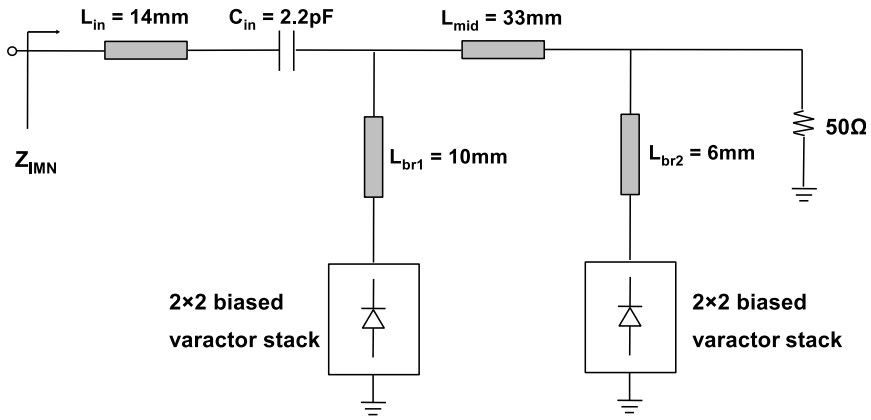


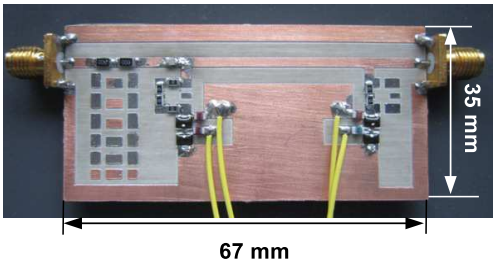
Figure 4.22: Covered area of the impedances seen from the input of the amplifier at different bias and load values.

According to this figure, although the variation of the input impedance does not cover a large area, it is not small enough to enable us to utilize the simpler structure consisting of just one parallel branch for the input matching network as it was discussed in section 3.4.8. Hence, for the input port also, we are going to use the ladder network of Figure 4.15.3

The input matching network should be able to provide the complex conjugate of the impedance points shown in Figure 4.22. After tuning of the transmission line lengths as described in Figure 4.17, I had to add an extra capacitance of 2.2 pF in order to cover the desired area of the Smith chart. The schematic and fabricated circuit of the input tunable matching network are shown in Figure 4.23. The covered area of this network together with the complex conjugate of the measured input impedance points are demonstrated on the Smith chart of Figure 4.24 (a). The loss curves are sketched in Figure 4.24 (b).

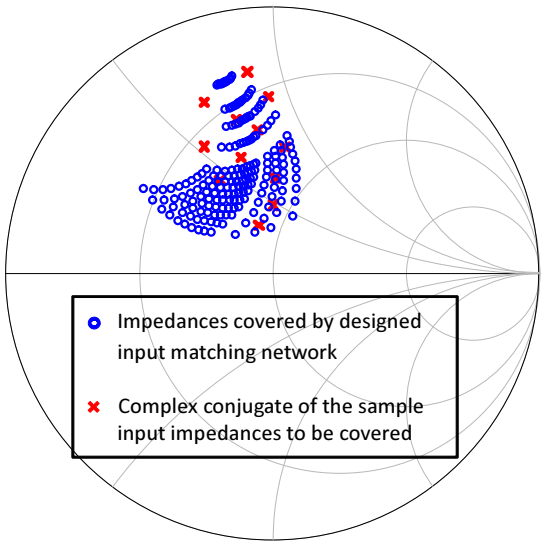


(a)

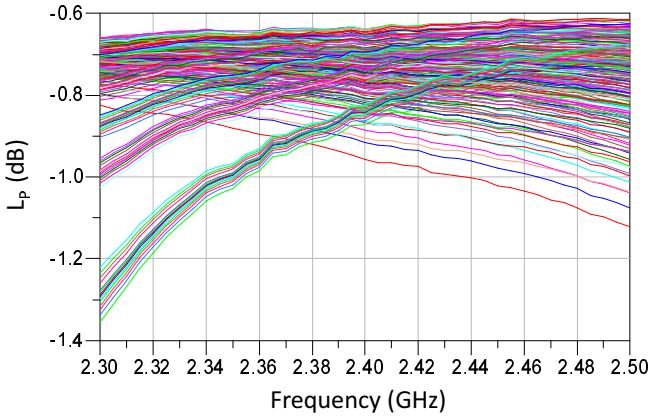


(b)

Figure 4.23: (a) Schematic and (b) fabricated circuit of the input tunable matching network.



(a)



(b)

Figure 4.24: (a) Covered area and (b) loss of the input tunable matching network.

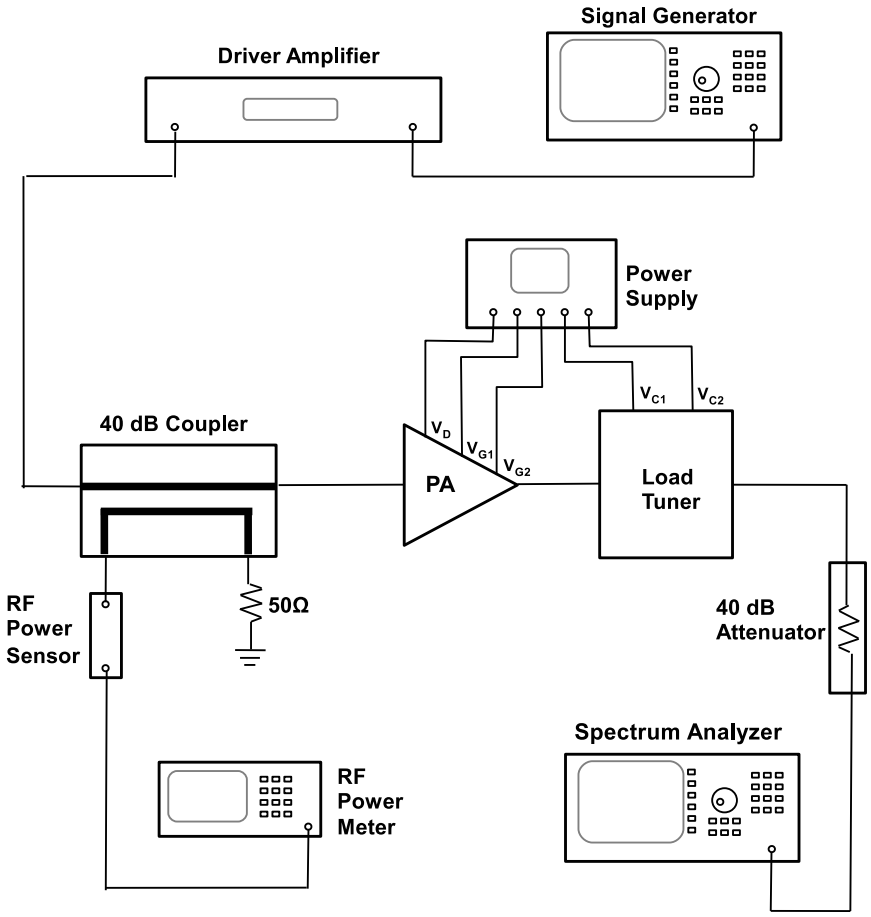
4.4 Load-Pull Measurements

For the load-pull analysis, the amplifier and load-tuner are connected using an external male-to-male transition while taking into account the extension of the L_{in} of the load-tuner. Load-pulling should be performed at different input power levels beginning from the completely linear operating region up to the starting of the gain compression. This means that the signal generator should be able to generate the maximum RF power of 23 dBm. But the maximum output power of the equipment available in the microwave lab is 18 dBm at the most demanding a driver amplifier. The driver amplifier was available in ASELSAN where I was admitted to perform the measurements. The setup is demonstrated in Figure 4.25.

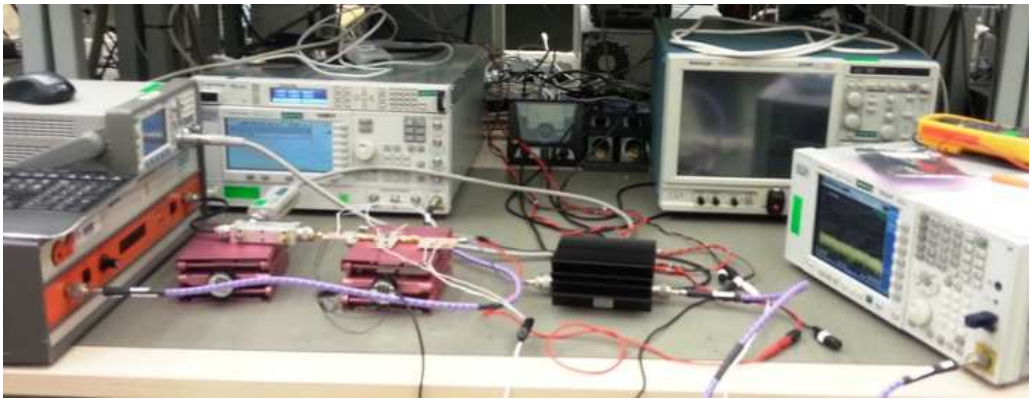
As mentioned earlier, since stability problems arise for gate bias values of $V_{G1} < 0.36$ V and $V_{G2} < 0.3$ V, I started the measurements from $V_{G1} = 0.36$ V and $V_{G2} = 0.3$ V and incremented V_{G1} by 0.05 V until 0.55 V. I also added a last case of $V_{G1} = 0.55$ V and $V_{G2} = 0.55$ V in order to push the amplifier to its maximum gain performance. Table 4.1 summarizes the load-pull measurement results.

P_{in} in the table is the input power to the power amplifier in which the load-pulling is performed. As shown in the table, for each biasing point, load-pulling has been done at 5 different input powers starting from -10 dBm up to 22 dBm with smaller steps at higher powers where the amplifier begins to enter the non-linear region. I_D is the total drain current read from the power supply display connected to the common drain of the transistors when the input RF power is not yet been applied.

An important point observed during the measurements was the unusual drain current of 70 mA for the $V_{G1} = 0.36$ V and $V_{G2} = 0.3$ V case and then decrease of current by increasing the gate voltage of the second transistor. This could be again a sign of oscillation in some frequencies. That is why I did not continue the load-pull measurements for that case and started from $V_{G2} = 0.35$ V.



(a)



(b)

Figure 4.25: (a) Schematic and (b) on-site photograph of the load-pull measurement setup in ASELSAN.

Table4.1: Summary of the load-pull measurement results.

V_{G1} (V)	V_{G2} (V)	I_D (mA)	P_{in} (dBm)	Power Match		PAE Match	
				V_{C1} (V)	V_{C2} (V)	V_{C1} (V)	V_{C2} (V)
0.36	0.3	70 !	NA	NA	NA	NA	NA
0.36	0.35	36	-10	7	20	7	20
			0	7	20	7	20
			15	7	20	6	20
			20	10	15	5	15
			22	18	9	5	18
0.36	0.4	53	-10	8	15	NA	NA
			0	8	15		
			15	10	11		
			20	15	9		
			22	25	10		
0.36	0.45	107	-10	9	12	NA	NA
			0	9	12		
			15	10	11		
			20	15	7		
			22	25	5		
0.36	0.5	211	-10	8	10	NA	NA
			0	8	10		
			15	11	9		
			20	17	6		
			22	30	5		
0.36	0.55	355	-10	10	7	NA	NA
			0	10	7		
			15	13	6		
			20	22	3		
			22	37	2		
0.55	0.55	718	-10	15	4	NA	NA
			0	15	4		
			15	15	4		
			20	20	3		
			22	40	1		

As shown in the table, for the first biasing point only, the optimum loads for both maximum delivered power and maximum PAE indicated as Power Match and PAE Match, respectively, are obtained. That is for determining the first operational state of the amplifier which provides the best efficiency for low drive levels. In order to specify the PAE Match loads, first the output powers at different loads were found and then the PAE was calculated. Consequently, the load value or varactor voltages in which the PAE is maximum would be determined. For the other biasing points in the table, the optimum loads for maximum delivered power at different input powers are derived. Note that the optimum loads are represented by their respective varactor bias voltages of V_{C1} and V_{C2} in the table.

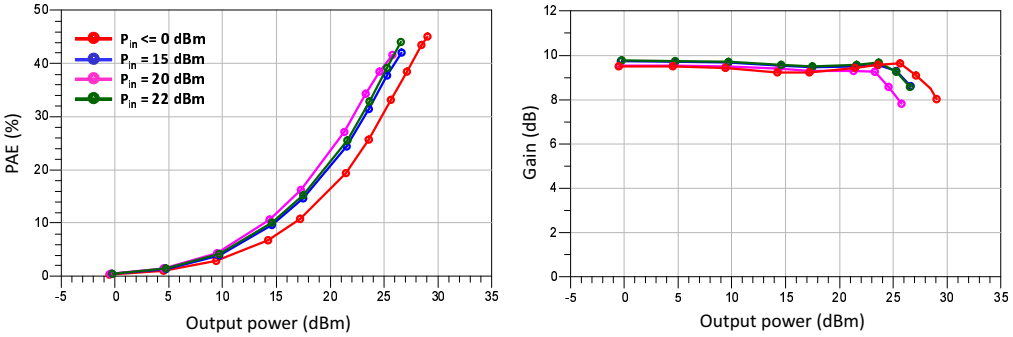
4.5 State Selection

As summarized in Table 4.1, the load-pulling data are available for 35 different combination of biasing and matching conditions which results in 25 operational states. To select the desired states, the output power is measured after connecting the input matching network and tuning it for each state in order to obtain the maximum gain. Then the PAE and gain curves are sketched as a function of output power and ultimately the best operational states can be selected according to the criteria discussed in section 3.3.2.3.

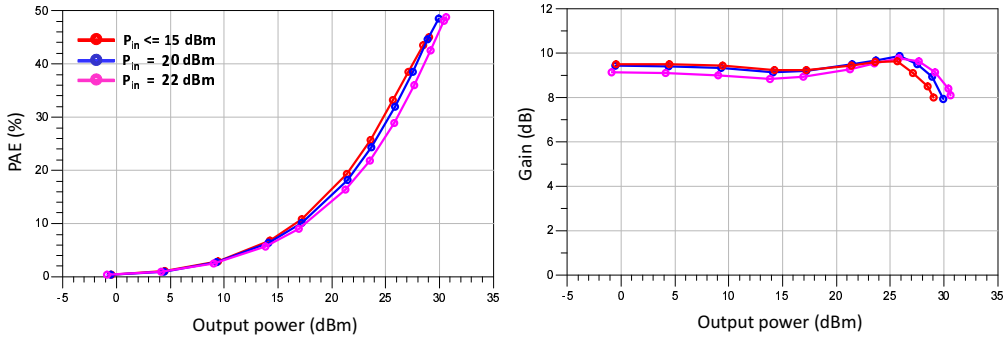
Table 4.2 summarizes the input and output varactor stack biasing voltages for 25 different states and corresponding output 1 dB compression point. Figure 4.26 (a) to (g) present the PAE and power gain curves for the bias and matching conditions of Table 4.2. Based on the compression points as well as the efficiency curves of Figure 4.26, I was able to select 7 optimum operational states, as highlighted on the table.

Table4.2: 1 dB compression points of the amplifier at 25 different biasing and matching conditions.

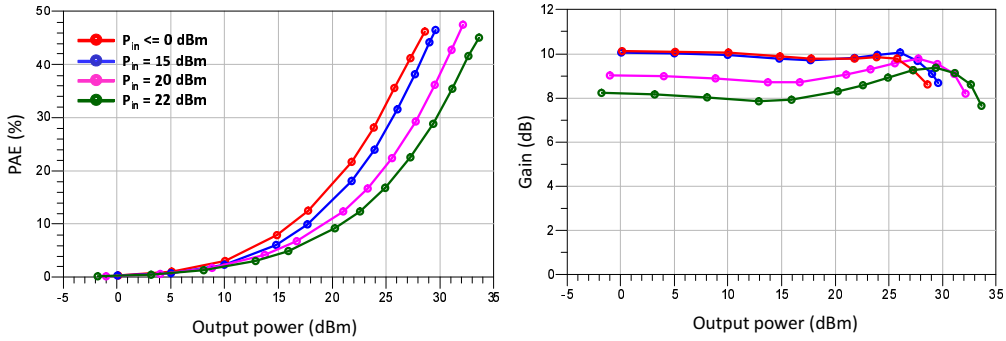
V_{G1} (V)	V_{G2} (V)	V_{Ci1} (V)	V_{Ci2} (V)	V_{Co1} (V)	V_{Co2} (V)	Output P_{1dB} (dBm)	
0.36	0.35	25	20	7	20	**28.5**	
		25	25	6	20	**25.5**	← **2nd state**
		40	40	5	15	**24.5**	← **1st state**
		40	40	5	18	**26**	
		20	17	10	15	**30**	
		15	13	18	9	**30.5**	
0.36	0.4	40	17	8	15	**27.5**	← **3rd state**
		20	17	10	11	**29**	← **4th state**
		12	12	15	9	**32.5**	
		9	10	25	10	**33.5**	
0.36	0.45	25	10	9	12	**28.5**	
		15	5	10	11	**30**	
		10	3	15	7	**31**	← **5th state**
		10	2	25	5	**31.5**	
0.36	0.5	20	8	8	10	**29.5**	
		12	4	11	9	**30.5**	
		8	3	17	6	**31.5**	
		7	3	30	5	**32**	← **6th state**
0.36	0.55	20	8	10	7	**30.5**	
		12	6	13	6	**31.5**	
		7	3	22	3	**32**	
		7	3	37	2	**33**	← **7th state**
0.55	0.55	15	5	15	4	**31**	
		10	4	20	3	**31**	
		10	4	40	1	**31**	


P_in <= 0 dBm
P_in = 15 dBm
P_in = 20 dBm
P_in = 22 dBm
PAE (%)
Gain (dB)
Output power (dBm)
Output power (dBm)

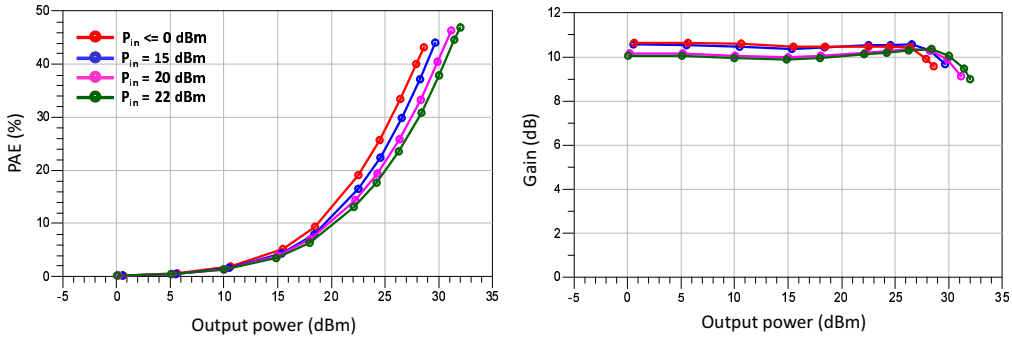
(a)


P_in <= 15 dBm
P_in = 20 dBm
P_in = 22 dBm
PAE (%)
Gain (dB)
Output power (dBm)
Output power (dBm)

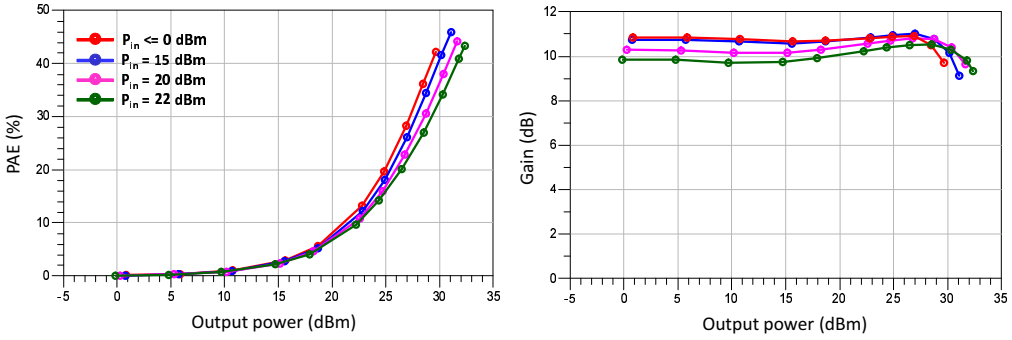
(b)


P_in <= 0 dBm
P_in = 15 dBm
P_in = 20 dBm
P_in = 22 dBm
PAE (%)
Gain (dB)
Output power (dBm)
Output power (dBm)

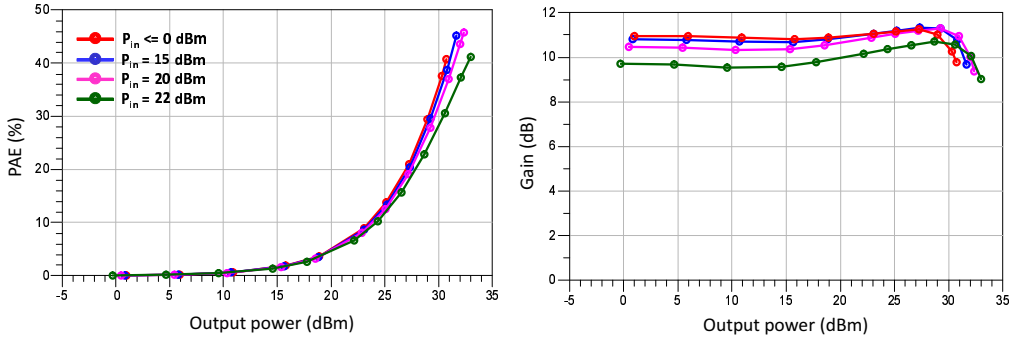
(c)


P_in <= 0 dBm
P_in = 15 dBm
P_in = 20 dBm
P_in = 22 dBm
PAE (%)
Output power (dBm)
Gain (dB)
Output power (dBm)

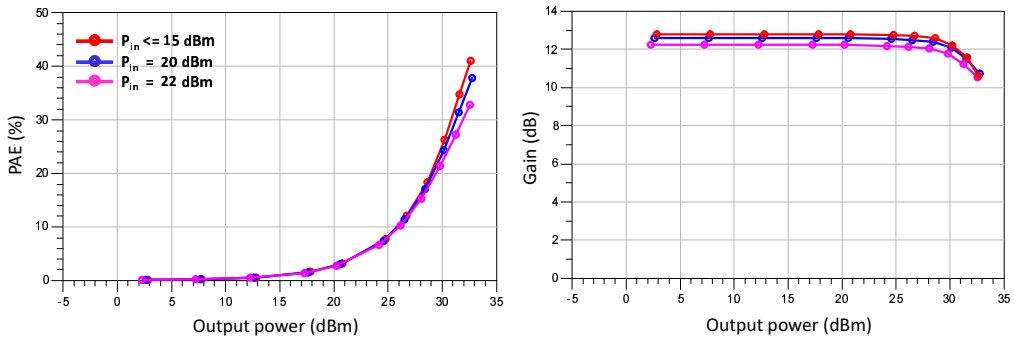
(d)


P_in <= 0 dBm
P_in = 15 dBm
P_in = 20 dBm
P_in = 22 dBm
PAE (%)
Output power (dBm)
Gain (dB)
Output power (dBm)

(e)


P_in <= 0 dBm
P_in = 15 dBm
P_in = 20 dBm
P_in = 22 dBm
PAE (%)
Output power (dBm)
Gain (dB)
Output power (dBm)

(f)



(g)

Figure 4.26: Measured PAE and Gain curves for (a) PAE matching with V_{G1} = 0.36 V and V_{G2} = 0.35 V, and Power Matching with (b) V_{G1} = 0.36 V and V_{G2} = 0.35 V, (c) V_{G1} = 0.36 V and V_{G2} = 0.4 V, (d) V_{G1} = 0.36 V and V_{G2} = 0.45 V, (e) V_{G1} = 0.36 V and V_{G2} = 0.5 V, (f) V_{G1} = 0.36 V and V_{G2} = 0.55 V, (g) V_{G1} = 0.55 V and V_{G2} = 0.55 V.

4.6 Final Results

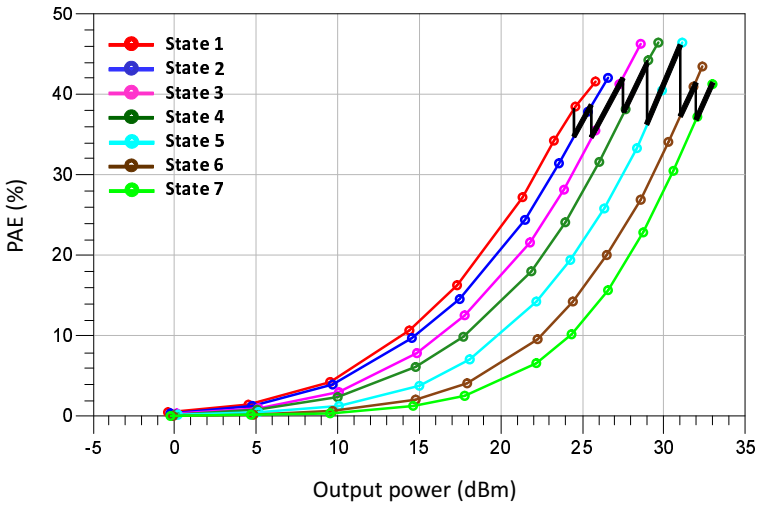
4.6.1 PAE and Gain

The power added efficiency and gain plots of the 7 selected states are sketched on common axis shown in Figure 4.27 (a) and (b). As stated before, we have chosen the 1 dB compression points as the criteria for switching between states. The transition region is between the compression point of the first state (24.5 dBm) to the last one (33 dBm) which is highlighted on the figures by bold black lines drawn over the respective curves.

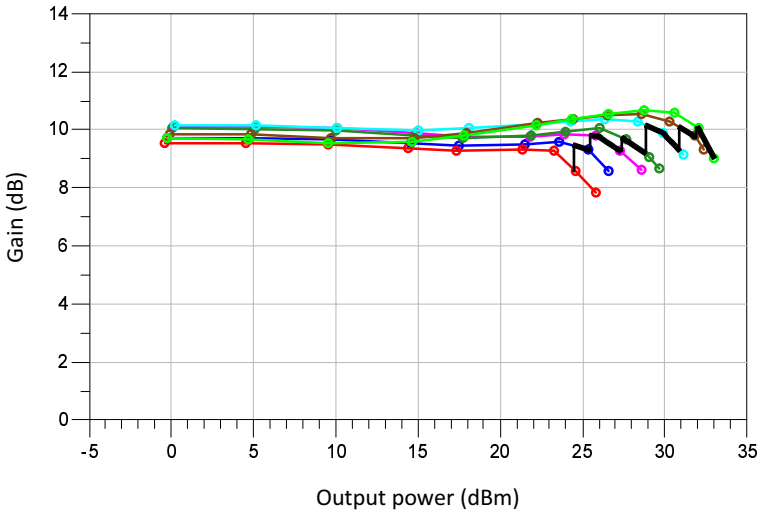
According to Figure 4.27 (a), the PAE has reached to the value of about 39% at the 1 dB compression point of the first state which 24.5 dBm after which we are able to maintain the PAE at the average value of around 40% up to the 1 dB compression point of the last state which 33 dB. This means that in practice, using our design methodology, we are able to keep the efficiency nearly constant from 8 dB back-off, while preventing the linearity degradation at higher output power levels.

In other words, if we were to operate the amplifier only in the last state in order to achieve the maximum P_{1dB}, we would loose the efficiency significantly at reduced drive levels such that at the output power of 24.5 dBm the PAE level would drop to 12%. So we have improved the efficiency from 12% to 40% at 8 dB back-off. On the other hand, if we intended to operate the amplifier only in its first state in order to achieve maximum efficiency at lower input powers, then we had to accept the very low output P_{1dB} of 24.5 dBm. However, using our new topology and tunable matching network and switched biasing, we can now fulfil both of the requirements at the same time.

Now consider the gain curves of Figure 4.27 (b). The small-signal power gain of the first state is about 9.5 dB. Before the gain drops to 8.5 dB, switching to the second state should be taken place and this process continues until the gain drops to 8.5 dB at the output P_{1dB} of the last state. This means that the gain is maintained at the average value of 9.5 dB in back-off region.



(a)



(b)

Figure 4.27: Measured (a) PAE and (b) power gain of the amplifier at 7 selected operational states.

4.6.2 Third Order Intermodulation

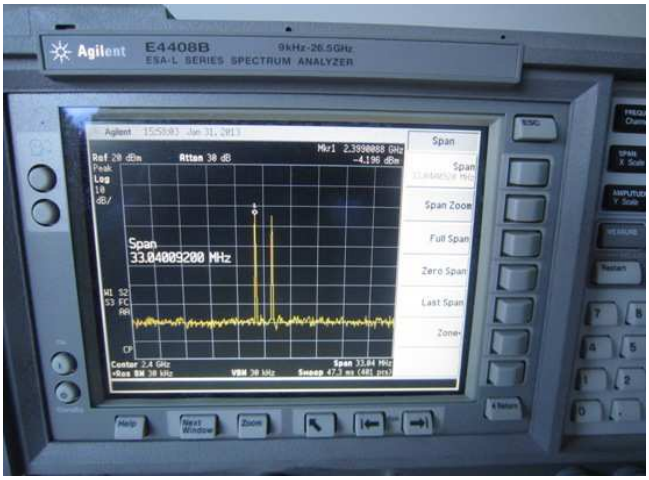
For examining the intermodulation response of the amplifier, a two-tone signal was required. But none of the available signal generators were able to suppress the carrier from the produced signals and create a clear two-tone signal. Therefore, it was decided to utilize two separate signal generators to produce each tone separately. The two tones should normally be combined using a power combiner before being applied to the amplifier.

Using a power combiner is necessary to prevent the leakage of the signal from each generator to the other as well as minimizing the return loss at the output of the generators. Leakage of the signal to the generators results in the contribution of the non-linearities produced by the output stage of the signal generators to the two-tone signal applied to the amplifier. But there was no power combiner available at the design frequency. Moreover, we only intend to check the presence of the sweet-spots and their locations are well below the 1 dB compression point. Hence the level of the applied signals are low enough to make using a Tee junction possible instead of a power combiner. This was already verified before the amplifier measurements. The configuration is shown in Figure 4.28.

Third order IMD measurement results for the 7 operational states are demonstrated in Figure 4.29. The presence of sweet-spots can be observed for all of the states which is a sign of linearity enhancement.

(a)

(b)



(c)

Figure 4.28: Producing two-tone signal using two separate signal generators; (a) connection of the two devices using coaxial T junction, (b) adjusting the signal generators to create two signals at 2399 MHz and 2401 MHz, (c) spectrum analyzer view of the created two-tone signal.

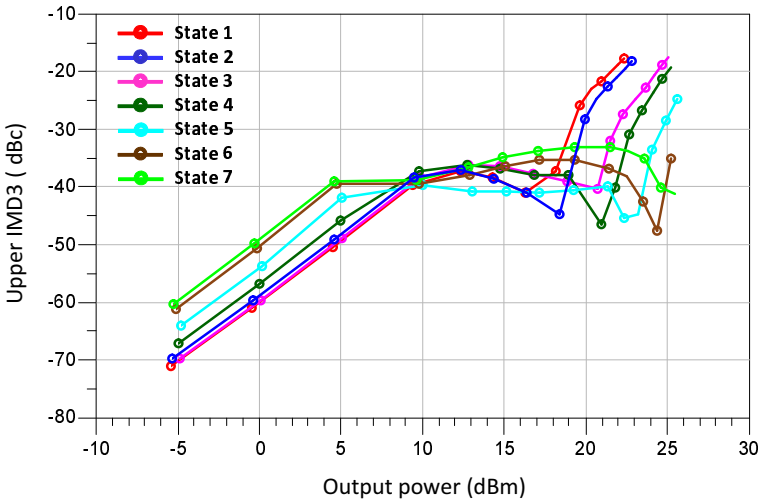
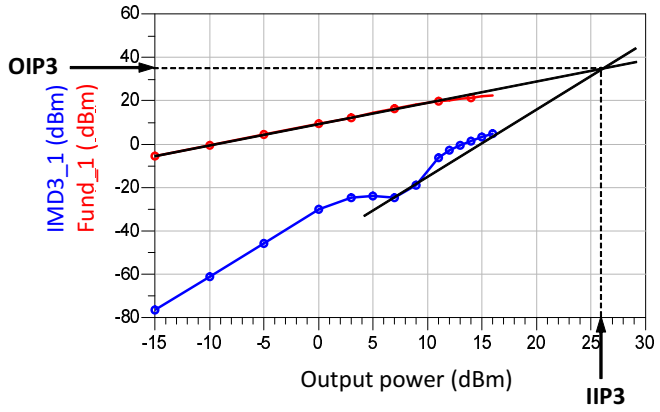


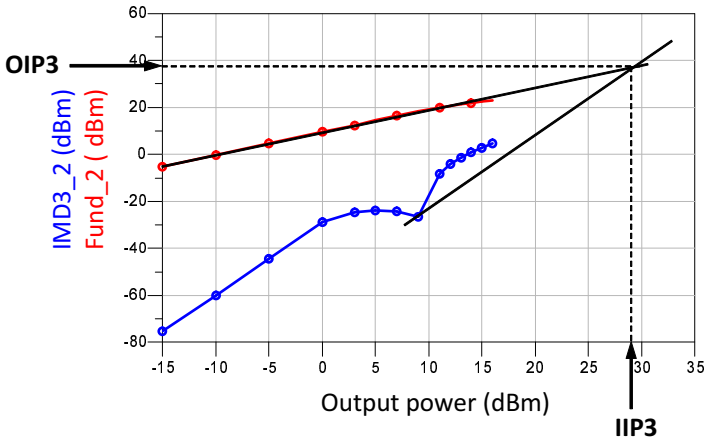
Figure 4.29: Measurement results of the upper 3rd order intermodulation distortion of the amplifier at 7 selected operational states.

4.6.3 Third Order Intercept Point

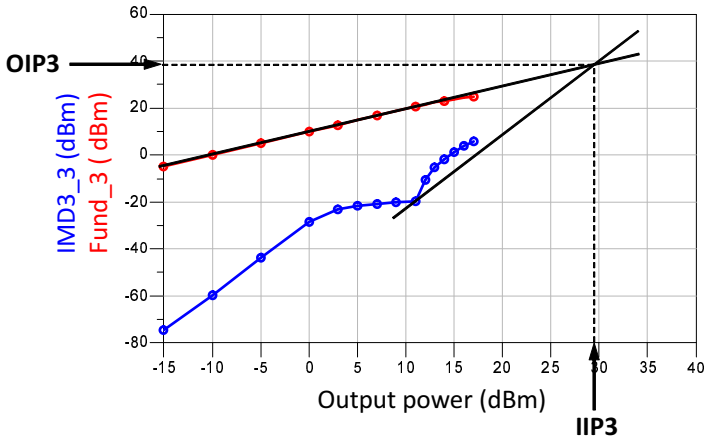
As the last parameter that can be checked at the different operational states of the amplifier is the Third Order Intercept Point (IP3). It can be obtained graphically by plotting the fundamental output power and the IMD3 product versus the input power in on logarithmic scales. Both curves are extended with straight lines of slope 1 and 3. The point where the curves intersect is the intercept point. It can be read from the input or output power axis, leading to the input or output intercept point, respectively (IIP3/OIP3). Figure 4.30 (a) to (f) present the intercept points at 6 operational states of the amplifier. Note that in our case, the intersecting points are obtained by extending the slope 3 lines from the point of the sweet-spot which is usually the case in the literature.



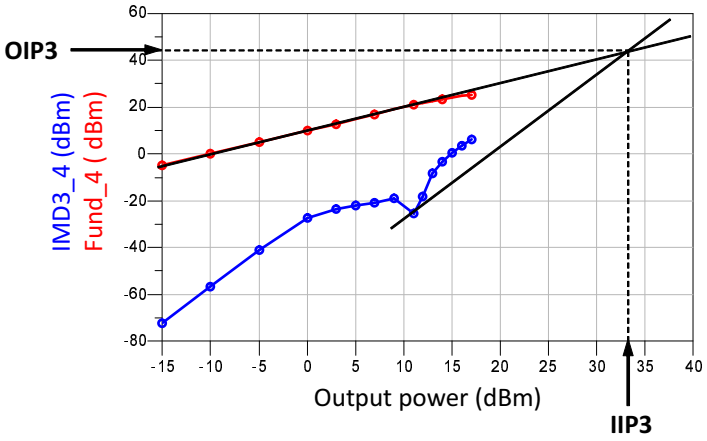
(a)



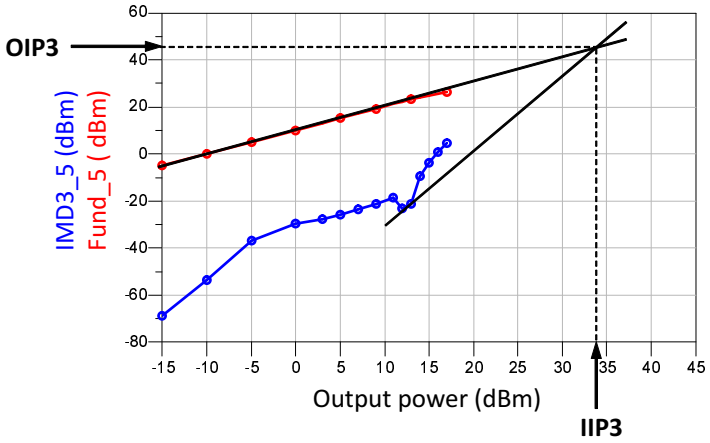
(b)


OIP3
IMD3_3 (dBm)
Fund_3 (dBm)
Output power (dBm)
IIP3

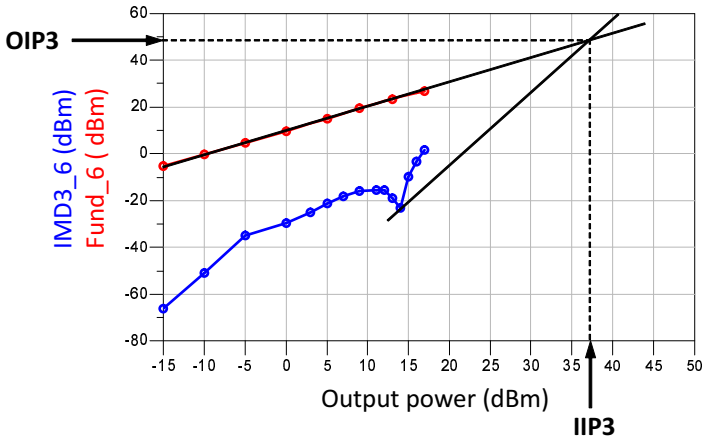
(c)


OIP3
IMD3_4 (dBm)
Fund_4 (dBm)
Output power (dBm)
IIP3

(d)


OIP3
IMD3_5 (dBm)
Fund_5 (dBm)
Output power (dBm)
IIP3

(e)



(f)

Figure 4.30: Fundamental and IMD3 curves plotted as functions of the input power for finding the third order intercept points from the locations of the sweet spots at (a) state 1 up to (f) state 6.

Table 4.3 summarized the input and output IP3 values at 6 operational states of the amplifier. It can be seen that there is an increasing trend in intercept points starting from OIP3 = 35.5 dBm at the first state, up to the maximum value of the OIP3 = 49 dBm at the 6th state. It is worthwhile to mention that the OIP3 value of the transistor as reported in its datasheet is 45 dBm. This means that there is an improvement of about 4 dBm in the OIP3 value in our design which is the direct consequence of the generation of sweet-spot.

Table4.3: Summary of the input and output third order intercept points at 6 operational states of the amplifier.

State	IIP3 (dBm)	OIP3 (dBm)
1	26	35.5
2	29	38.5
3	29.5	39
4	33.5	43.5
5	34	45.5
6	37	49

4.7 Fabrication of the Completed Circuit on a Common Board

As the finishing work of the thesis, the amplifier and matching networks were integrated on a common board in order to benefit from the advantages of the integrated design method. The fabricated circuit is shown in Figure 4.31.

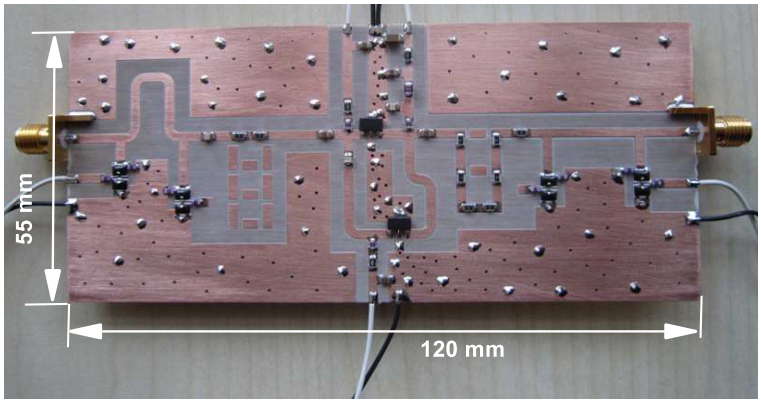


Figure 4.31: Fabricated amplifier with tunable input and output matching networks integrated on a common board.

Due to the sensitivity of the impedances provided by the matching networks to the lengths of their respective input transmission lines, a degradation in gain and PAE responses was observed in the integrated case for the previously chosen 7 states. It is expected that by first integrating the amplifier and load-tuner and performing the load-pull analysis again and finally adding the input matching network with precisely adjusting the line lengths, better results can be obtained.

CHAPTER 5

CONCLUSION AND FUTURE WORK

Achieving high power efficiency and improved linearity at the same time is one of the main goals in power amplifier design for wireless applications. This thesis presents a new method of designing power amplifier in a configuration consisting of two transistors connected in parallel. The method is heavily based on load-pull analysis at different gate bias voltages and input powers. The creation of large-signal sweet-spots are also monitored throughout the load-pulling. A set of bias voltages and load impedances are determined so that the efficiency is improved at reduced driving powers while the output 1 dB compression point is shifted to higher values at higher drives. The design procedure can be divided into two parts of amplifier design and tunable matching network design. In the amplifier design two transistors are connected with a common drain but separate gate biasing lines in order to independently change the bias of each individual device. In the design of the tunable matching network, the main issue is to cover the interested load impedances while providing minimum possible loss. The tunability is provided by high Q, high breakdown voltage abrupt junction silicon varactors.

This chapter summarizes the key research results achieved in this thesis and provides some suggestions for future studies.

5.1 Summary and Conclusions

Within the framework of the research conducted in this thesis, following conclusions can be drawn:

- Using the introduced amplifier structure and design methodology, the power added efficiency of a sample 2.4 GHz amplifier can be maintained nearly at its peak value of 41% from 8 dB back-off (15.8 dB in simulations) up to the total 1 dB compression point of the amplifier which is 32.5 dBm. This means that in one hand the efficiency is enhanced at lower input drives where normally the amplifier operation is perfectly linear but the efficiency is quite low. And in the other hand, with maintaining the same level of efficiency we have shifted the gain compression point to higher values which means prevention of the linearity degradation at higher output power levels.

- The length of the transmission lines connecting the drains and gates of the two devices are found to be crucial design parameters where the former (drain line) changes the region of the optimum load impedances on the Smith chart and the latter influences the gain of the amplifier. So in the design process the lengths of these lines are tuned to transfer the optimum load points to a region

capable to be easily matched with lower loss level as well as providing maximum possible power gain.

- A couple of practical issues were encountered during the fabrication of the amplifier. These problems which were identified to be a result of improper grounding and biasing, suggest that for the amplifier to be stable and produce reasonable power gain, firstly, metallized via holes should be created in the substrate to provide better grounding and secondly, the drain biasing line should be grounded using capacitors of different values in the range of 10 pF up to 2.2 μF.

- One of the main points revealed in this research during the amplifier design is that the highest efficiency at low input powers which corresponds to the first state of our design is achieved by matching the amplifier to its optimum PAE impedance point at a higher input power level just before entering the non-linear operation region. For the case of our sample amplifier the input power in which the matching should be performed is found to be 17 dBm.

- It is a known fact that by increasing the input RF power to an amplifier, the position of the optimum load impedance moves towards low resistive values and this has the effect of shifting the 1 dB compression point to higher levels. This effect is more pronounced if the amplifier is biased in class-B or class-AB. But as this shift takes place, the gain of the amplifier also drops which actually neutralize the advantage of improved linearity. In this work, by introducing another transistor and connecting it in parallel with its companion while separating the gate biasing lines, we are able to compensate the gain drop by increasing the gate bias voltage of one of the devices accordingly but still keeping another device to be biased in class-AB. That is why, our design can be considered as a combination of dynamic load and bias switching.

- Employing two transistors and keeping the gate bias of one of the devices at a small level (class-AB), the creation of IMD3 large-signal sweet-spot can be guaranteed. This is another advantage of using two transistor configuration of our design. But it should be noted that in the creation of sweet-spots, not only the biasing point but also the behavior of the transconductance and output conductance of the transistor and their derivatives with respect to the gate-source and gate-drain voltages, play a crucial role and should be examined beforehand.

- To implement the load-tuner and input matching network, two sets of 2×2 varactor stacks in anti-series configuration is used for the first time in this work. The two sets are connected using a 50 Ω transmission line creating a low-pass Π network. The inherent low-pass filtering behavior of this structure has also the effect of reducing the second and the third harmonics at the output. Moreover, the high-linearity anti-series topology of varactors leads to an insignificant contribution to the harmonic generation.

- In the load-tuner or output tunable matching network design part, one of the main challenges is being able to cover a large area of the Smith chart while keeping the loss in a minimum level so that the gain and efficiency of the amplifier are not degraded significantly. The trade-off between loss and covering area of the load-tuner is another key issue that is investigated in more detail in this work for the case of the Π topology utilizing varactors in parallel branches. The effect of the lengths of the transmission lines connecting the varactor stacks to the middle line as well as the length of the middle line itself, on the loss and covering area are monitored and optimized to get the desired results.

5.2 Directions for Future Work

The accomplishments in this thesis can be further extended by the following investigations as the future work:

- Due to heavily depending of our design method on finding and then matching the amplifier to the optimum load points, in the process integrating the input and output matching networks with the amplifier on a single board, the lengths of the transmission lines should be precisely adjusted in order to obtain the proper results. Otherwise a significant degradation in the performance of the amplifier is expected. On-board directional couplers can be designed at the input of the load-tuner in order to carefully measure the reflected power and modify the circuit accordingly in the future steps. Before achieving the best performance in terms of gain and efficiency, a number of intermediate boards may be required to be fabricated and tested.

- The efficiency degradation of the tunable or adaptive PAs is mainly owing to the lossy varactors. The performance of the matching networks can be further improved by utilizing varactors with higher quality factor or by designing with MEMS varactors, ferroelectric or LDMOS transistors.

- After determining the varactor biasing voltages at different operational states, in order to complete the design, a control circuitry for the varactors should be designed and integrated with the PA part. This circuitry should demodulate or detect the envelope of the incoming RF signal and use it to adjust the bias voltages of the individual varactor stacks. Since the control voltages of each varactor stack is different, this system should be able to generate more than one set of voltages as functions of input envelope for each stack.

- The design methodology and proposed PA structure can be applied on GaN devices for higher output powers. In fact I initiated a design using CGH40010 which is a 10 W GaN device from CREE. The design was carried out using the large signal model provided by the manufacturer. The results of the simulations confirmed the feasibility of applying my design procedure on GaN devices at higher power levels, but the improvement in the efficiency was rather smaller. It was found that for the case of this transistor there exists small movements in the location of the optimum load impedance. Finding the reason for this behavior and conducting a general research about the GaN devices can be a subject of future studies.

- Since no Large Signal Network Analyzer (LSNA) was available, we were not able to study the large signal behavior of the varactor-based matching networks. As stated in the simulations, the behavior of the varactors change when higher powers are applied which ultimately degrades the performance of the amplifier at higher drive levels even more. This effect was not studied in this thesis and can be considered an extension to this work.

- The amplifier topology can be further generalized by incorporating more than two transistors in parallel and investigate their mutual effects at different load and biasing levels and possible improvements that can be achieved using several stages of transistors.

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APPENDIX A

TRUNCATED .MDF FILE SAMPLE

REM Biasing voltage = 1 V
VAR VARAC=1
BEGIN ACDATA
Hz S DB R 50

% F	N11X	N11Y	N21X	N21Y	N12X	N12Y	N22X	N22Y
1.90	22.93	80.37	-0.44	13.44	-0.42	13.58	-21.97	86.25
.								
.								
.								
2.40	-10.60	146.78	-1.01	1.88	-1.07	2.32	-9.80	151.35
.								
.								
.								
2.90	-5.46	134.84	-2.48	-8.32	-2.52	-7.91	-4.89	130.74

END ACDATA

REM Biasing voltage = 2 V
VAR VARAC=2
BEGIN ACDATA
GHz S DB R 50

% F	N11X	N11Y	N21X	N21Y	N12X	N12Y	N22X	N22Y
1.90	22.93	80.37	-0.44	13.44	-0.42	13.58	-21.97	86.25
.								
.								
.								
2.40	-10.60	146.78	-1.01	1.88	-1.07	2.32	-9.80	151.35
.								
.								
.								
2.90	-5.46	134.84	-2.48	-8.32	-2.52	-7.91	-4.89	130.74

END ACDATA
.
.
.

REM Biasing voltage = 40 V
VAR VARAC=40
BEGIN ACDATA
Hz S DB R 50

% F	N11X	N11Y	N21X	N21Y	N12X	N12Y	N22X	N22Y
1.90	22.93	80.37	-0.44	13.44	-0.42	13.58	-21.97	86.25
.								
.								
.								
2.40	-10.60	146.78	-1.01	1.88	-1.07	2.32	-9.80	151.35
.								
.								
.								
2.90	-5.46	134.84	-2.48	-8.32	-2.52	-7.91	-4.89	130.74

END ACDATA

CURRICULUM VITAE

PERSONAL INFORMATION

Surname, Name: Ronaghzadeh, Amin
Nationality: Iranian
Date and Place of Birth: 21 March 1981, Tabriz
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EDUCATION

Degree	Institution	Year of Graduation
Ph.D.	METU, Dept. of Electrical and Electronics Engineering	2013 (CGPA: 3.94/4)
M.S.	Uni. of Tabriz, Dept. of Electrical and Electronics Engineering	2006 (CGPA: 19.25/20)
B.S.	Uni. of Tabriz, Dept. of Electrical and Electronics Engineering	2003 (CGPA: 18.5/20)
High School	Meshkat High School, Ankara	1999 (CGPA: 19.85/20)

PROFESSIONAL EXPERIENCE

Year	Place	Enrollment
2004 - 2005	Uni. of Tabriz	Research and Teaching Assistant
Summer 2002	Science and Technology Park, Tabriz	Intern (Summer practice)

FOREIGN LANGUAGES

English (Fluent), Turkish (Fluent), French (Intermediate)

PUBLICATIONS

International Conference Publications

[1] A. Ronaghzadeh and S. Nikmehr, “Full-Wave Analysis of Microstrip Discontinuities Using Multiwavelet-Based Method of Moments,” *14th Iranian Conference on Electrical Engineering, (ICEE 2006)*, May 2006, Tehran, Iran.

[2] A. Ronaghzadeh and S. Nikmehr, “Rigorous Analysis of Noise in Multistage MESFET Amplifiers,” *3rd International Conference on Electrical and Electronics Engineering (ICEEE 2006)*, Sep. 2006, Veracruz Mexico.

[3] A. Ronaghzadeh and S. Nikmehr, “Noise Considerations in Cascaded Single-Stage Distributed Amplifiers,” *4th International Conference on Electrical & Computer Engineering (ICECE 2006)*, Dec. 2006, Dhaka, Bangladesh.

[4] A. Ronaghzadeh and S. Nikmehr, “A Novel DC to 30GHz High-Gain and Low-Noise GaAs HEMT MMIC Amplifier Module,” *4th International Conference on Electrical & Computer Engineering (ICECE 2006)*, Dec. 2006, Dhaka, Bangladesh.

[5] A. Ronaghzadeh and Ş. Demir, “Efficiency Improvement of Power Amplifiers without Degraded Linearity Using a New Topology and Control Method,” *30th General Assembly and Scientific Symposium of International Union of Radio Science (URSI GASS 2011)*, August 2011, Istanbul, Turkey.

National and International Journal Publications

[1] A. Kalteh, A. Ronaghzadeh and S. Nikmehr, “A Miniaturized Wideband Fractal Patch Antenna for PCS Applications (1850-1990 MHz),” *Journal of Faculty of Engineering*, University of Tabriz, Issue 15, pp. 31-37, June 2007.

[2] A. Ronaghzadeh and Ş. Demir, “Highly Efficient Power Amplifier Design without Degraded Linearity by Tuning Load and Bias in a New Topology,” *Submitted to the IEEE Trans. Microwave Theory & Tech*, Feb. 2013.