DESIGN OF A PROGRAMMABLE LOW-NOISE AND LOW-POWER READOUT CHANNEL FOR SOLID-STATE DETECTORS

by
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ABSTRACT

DESIGN OF A PROGRAMMABLE LOW-NOISE AND LOW-POWER READOUT CHANNEL FOR SOLID-STATE DETECTORS

MILAD DIBA

Electronics Engineering M.Sc. Thesis, August 2021

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Keywords: X-ray detection, Solid-State Detectors, ASIC, Gamma-Ray, Medical Imaging, Low-Power, Low-Noise.

Current medical X- and Gamma-ray imaging applications benefit from the usage of semiconductor detectors that sum up the incident flux over time. Although these systems have shown promising results, they expose a large radiation dose to the patient, and they do not have sufficient contrast resolution to discriminate between some tissue types. Significant improvements in patient dose, image quality, and ability to perform tissue discrimination can be achieved by utilizing new technologies and readout methods if requirements for high count rates, good efficiency, and reasonable energy resolution can be met. Photon-counting detectors for energy and timing measurements have been developed for applications such as Positron Emission Tomography (PET) and X-ray diffraction imaging offering better energy resolution and prominent detection efficiency. Hence, to meet the requirements, there is a demand for customized fast, low-noise, and low-power Application-Specific Integrated Circuits (ASICs) [1, 2, 3].

In this work, A programmable low-power, low-noise readout circuit for Cadmium Zinc Telluride (CdZnTe or CZT) detectors is presented. CdZnTe detectors encompass a wide range of applications such as medical imaging and astrophysics. The front-end comprises a charge-sensitive amplifier (CSA), a programmable reset network with dark current compensation capability, a fifth-order semi-Gaussian filter

with pole-zero cancellation, a comparator, and serial interface to communicate with external microcontroller. Utilizing the programmablity of the resetnetwork, the CSA can provide 256 different discharge timeconstants, ranging from 60n to 600 μ seconds , making the readout suitable for a wide range of event-rates. The application-specific integrated circuit (ASIC) is designed and simulated in a 0.35-μm 3.3V C35 CMOS process of Austria Micro-Systems. The ASIC has a power consumption of less than 2 mW per channel and the CSA only consumes 260 μW, stable with a feedback capacitance of 60 fF which contributes to a conversion gain of 135 mV/fC. Equivalent Noise Charge (ENC) is 98 erms @ 0 pF detector capacitance.

ÖZET

DESIGN OF A PROGRAMMABLE LOW-NOISE AND LOW-POWER READOUT CHANNEL FOR SOLID-STATE DETECTORS

MILAD DIBA

ELEKTRONIK MUHENDISLIGI YÜKSEK LİSANS TEZİ, Ağustos 2021

Tez Danışmanı: Doc. Prof. Dr. Ayhan Bozkurt

Anahtar Kelimeler: X-ışını, ASIC, Gamma-ışını, düşük güç, düşük gürültü, Solid State dedektörleri, tıbbi Görüntüleme

Günümüzün X-ışını ve gamma ışını tabanlı tıbbi görüntüleme uygulamaları, yarı-iletken algılayıcıların gelen ışınları zaman içinde toplayarak kaydetmesi temeline dayanır. Her ne kadar bu sistemler ümit verici sonuçlar verse de, hastaların yüksek dozda radyasyon almalarına sebep verirler. Ayrıca bu sistemler bazı doku türleri arasında ayrım yapabilmek için yeterli kontrast çözünürlüğüne sahip değiller. Algılayıcılarda , yeni teknoloji imkanları kullanılarak, yüksek sayım oranı, yeteri miktarda enerji çözünürlüğü ve verimlilik gibi özellikler elde edildiği takdirde, hastaya verilen doz miktarı, görüntü kalitesi ve doku türlerin ayırt edilebilmesi konularında oldukça önemli gelişmeler kaydedilebilir.

Daha iyi enerji çözünürlüğü ve algılama verimliliği vaddeden, pozitron emisyon tomografisi (PET) ve X-ışını kırınımı ile görüntüleme (X-ray diffraction imaging) gibi uygulamalar için bir çok foton-sayıcı algılayıcı sistemleri geliştirilmiştir. Dolayısıyla, daha verimli algılayıcıların ihtiyaçlarını karşılamak için özelleştirilmiş, hızlı, düşük gürültülü ve düşük enerji tüketimine sahip Uygulamaya Özel Tümleşik Devre (Application Specific Integrated Circuit - ASIC) sistemlerine ihtiyaç duyulmaktadır.

Bu çalışmada, Cadmium Zinc Telluride (CdZnTe or CZT) yarı-iletken algılayıcıları için tasarlanmış programlanabilir, düşün enerji tüketimine sahip, düşük gürültülü okuma devresi sunulmaktadır. CdZnTe algılayıcıları tıbbi görüntüleme, astrofizik gibi oldukça geniş uygulama alanlarına sahiptir. Ön-uç elektroniği, yüke duyarlı yükseltici (charge sensitive amplifier – CSA), programlanabilir ve kara akım telafi edici

özelliğe sahip bir ağ sıfırlama(reset network), 5-dereceli, pole-zero geçersiz kılma özellikli bir yarı-Gauss filtresi, bir karşılaştırıcı (comparator) ve harici mikrokontrol ile iletişim için kullanılan bir seri arayüze sahiptir. Ağ sıfırlayıcının programlama özelliğini kullanmak için, CSA 256 farklı deşarj zaman sabiti sunmaktadır. Bu zaman sabitleri 60 nano saniyeden 60 mikro saniyeye kadar değişerek okuma elektroniği için geniş olay oranı (event-rate) aralıklarına imkan vermektedir. Geliştirdiğimiz ASIC, her bir kanal için 2mW değerinden daha az güç tüketimine sahiptir. Ayrıca CSA sadece 260 micro W enerji harcamaktadır. Eşdeğer gürültü yükü (Equivalent Noise Charge – ENC), 0 pF algılayıcı kapasitansında 98 erms değerini vermektedir.

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Finally, I also take this opportunity to thank my family for their love and motivation among my graduate studies.

LIST OF ABBREVIATIONS

CSA **C**harge **S**ensitive **A**mplifier
ASIC **A**pplication **S**pecific **I**ntegrated **C**ircuit
SSD **S**olid **S**tate **D**etector
S-G **S**emi **G**aussian
PZC **P**ole **Z**ero **C**ancellation
CCD **C**harge **C**oupled **D**evices
CdZnTe **C**admium **Z**inc **T**elluride
ENC **E**quivalent **N**oise **C**harge
DAC **D**igital to **A**nalog **C**onverter

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1. Literature Overview

1.1 Introduction to Solid-State Detector Readout Systems

Since the discovery of X-rays in 1805 and later its diagnostic applications in health-care, many efforts have been made in world of front-end electronics. Radiation interaction with detector material which plays a key role for any photon-counting system whether is due to photo-electric or compton effect. Modern readout electronics of solid-state detectors trend in astrophysics, consumer electronics, and medical imaging applications are prone to smaller, higher density readouts to achieve the highest position resolution. The fundamental limitations in the accuracy and cost of the readout system are determined by the noise and consumed power of the electronic channels connected to the detector/sensor [1]-[3].
Gamma and x-ray solid-state detectors have obtained significant attention in the past decade. Cadmium Zinc Telluride (CdZnTe or CZT) material has become an optimum detector choice in X- and Gamma-ray readout electronics due to their high atomic number (Cd: 48, Zn: 30, and Te: 52), promising charge transport properties, a high density (5.8g/cm3) and a tunable bandgap of 1.5 to 2.2 eV [1]. Medical application purposes of CdZnTe detectors focus on thick CdZnTe crystals. Prior studies in fabrication and development of CdZnTe detectors have resulted in production of these detectors with reasonable thickness and good performance. The presented front-end circuits in this work are more optimized for a CdZnTe detector used to obtain the energy spectrum of incident electrons ranging from 10 keV to 1 MeV.

In this work, we present the design of a low-noise and low-power front-end with prgrammable reset network time-constant for solid-state radiation detectors (to be specific, CdZnTe detectors). All blocks of the readout are simulated using

Austria Micro-Systems C35B4M3 process and post-layout results are also presented.

1.1.1 Signal formation in Radiation Detectors

Various types of radiation detectors have been fabricated and introduced over years: vacuum tube photomultipliers, avalanche photodiodes, silicon strips, pixels and drift detectors, charge coupled devices (CCDs) provide a long, but not a full-scale list. A detailed design analysis and fabrication methods of these devices is beyond the scope of this thesis, and the reader is referenced to [2,3,4]

Figure 1.1 shows the working principle of the solid-state detector which is formed by enclosing a material between two electrodes. The enclosed material is considered as sensing element for radiation detection. Moreover, the electrodes are kept at distinct potentials, in order to generate an electric field inside the detecting volume. For many years, only gasses have been used as the detecting medium; However, starting from the sixties of the last century, semiconductors became popular thanks to their high atomic number, availability, and decent charge transport properties [4].

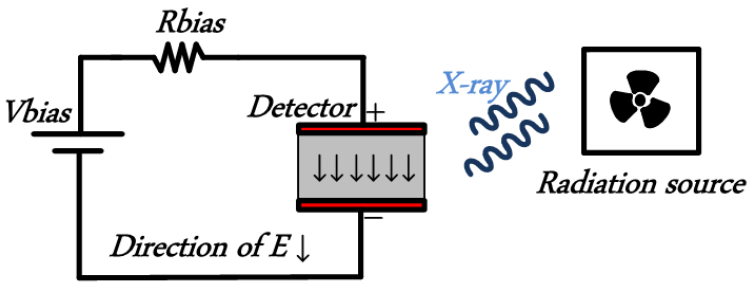

Figure 1.1 Working principle of a Solid-State Detector.

As depicted in Figure 1.1, charged particle crossing or photon (here X-rays) hitting the sensor/detector interacts with its atoms, creating ion-electron pairs in a gas and hole-electron pairs in a semiconductor. In case of many semiconductor detectors, once a photon hits the detector, based on the detector material, it generates a number of electron-hole pairs. Regarding the bias topology of the detector which provides the electric field, the generated electron-hole pairs drift to electrodes of the detector [1,2,3,4]. This drift of electron-hole pairs induces a small current which has

to be amplified by the charge-sensitive amplifier before any other signal processing. In other devices, like gaseous detectors, the primary charge is too small to be efficiently detected and it is thus first transported into a region of higher electric field, where the carriers gain enough energy to create secondary ionization.
It is worthwhile to discuss signal formation parameters such as rise time of accumulated charge in solid-state detectors since they can determine electronic system's requirements in terms of speed and bandwidth [5]. For a planar detector, crystal carrier speed is expressed as:

$$v = \mu E \tag{1.1}$$

where μ is the electron mobility and is about 1000 $cm^2/(V.s)$. E represents the applied electric field and differs based on the application. For CdZnTe detectors, usually $100V/mm$ ($1000V/cm$) is applied to form an electric field between electrodes of the detector. Using Equation (1.1) and recalling the relationship between time, distance, and speed from basic physics, rise time of the accumulated charge at the output of a planar detector can be expressed as:

$$t_{risetime}(s) = \frac{d}{v} \tag{1.2}$$

where d is planar detector's thickness [5]. Using equations (1.1) and (1.2) accumulated charge's rise time is calculated to be $100ns$ for a CdZnTe planar detector with thickness of $1mm$. Ignoring the variations in carrier mobility, one can assume a linear function for the charge collection rise time in CdZnTe planar detectors. Hence, if we have a $3mm$ planar detector, the rise time will be $300ns$. However, for pixel, strip, coplanar detectors, the rise time will change due to behavior of weighting potential distributions. It will be much sharper for a pixel detector and the rise time and perhaps will be close to $100ns$ even for $4-5mm$ thickness. The transient current generated by the detector can be derived by:

$$I_{detector} = \frac{Q_{total}}{t_{risetime}} \tag{1.3}$$

where Q_{total} is the total accumulated charge generated by the detector.
The band-gap of CdZnTe X-ray detectors is typically 1.5-1.6 eV however it turns out that photon energy/band gap is not exactly equal to expected number of electron hole pairs due to statistical effects and other factors. The quoted number is around 4-5 eV to produce one e-h pair. The Fano factor reduces the statistical noise. Nevertheless a rough estimate for 100 keV photon would result in generation of 20,000 - 25,000 e-h pairs. For planar detectors, the calculation is straightforward. According to the bandgap of CdZnTe material, an energy of 100 keV leads to generation of

approximately 25'000 e-h pairs, which is equal to 1.5 fC. From equation (1.3) and having a rise time of $300ns$ for a $3mm$ thick CdZnTe detector, one can write:

$$I_{detector} = \frac{Q_{total}}{t_{risetime}} = \frac{1.5fC}{300ns} = 5nA \tag{1.4}$$

This is the peak value of the transient current generated by a CdZnTe planar detector with a thickness of $3mm$ while it is exposed to 100 keV of energy.

1.1.2 Electrical Modeling of a Radiation Detector

Design of a front-end circuit is not feasible without a realistic model of the detector. From a signal processing view, solid-state detectors can be modeled as linear networks consisting primary elements such as independent current sources resembling transient events or dark currents, capacitors inductors and resistors for parasitics and detector physical properties [4]. Generally, the circuit shown in Figure 1.2. is adequate. The model consists of a current source, $I_{detector}$, representing the detector signal as a function of time. Connected in parallel to the source, C_d models the capacitive load the sensor presents to the front-end electronics. The DC source I_{dark} takes into account the device dark current, while R_d models the resistive component of the detector output impedance (negligible) or physical resistors that may be used in the detector High-Voltage bias. Inductor L_t and resistor R_t describe respectively the parasitic inductance and resistance of the connections. In many circumstances these can be omitted but care must be taken to properly handle them in high speed and very low noise applications. The direction of the current source must be chosen to properly reflect the signal polarity.

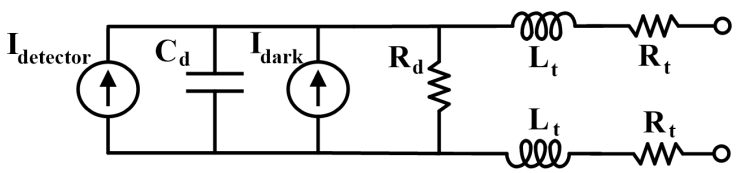

Figure 1.2 Simplified Model of a Solid-State Detector.

1.1.3 Detector Front-End

Energy measurement is of great importance in medical and security application. As discussed earlier in section 1.1.1, the deposited energy in a semiconductor detector is proportional to the total charge rather than the current. Charge is the integral of current so the detector is attached to a charge-sensitive amplifier (CSA), which generates an output pulse with a voltage step directly proportional to the time integral of the current. The CSA output is then sent to a shaping amplifier, which shapes the pulse to facilitate accurate measurements under realistic environment, amplifies them, and filters out the excess noise to minimize Equivalent Noise Charge (ENC). The shaped and amplified pulse, a voltage pulse with peak amplitude proportional to the absorbed energy, is then fed to a multi-channel analyzer, that measures the peak amplitude of these pulses, plotting a histogram showing the number of pulses with amplitude measured within the range of each channel. This is the output spectrum [2,3,4,5]. Figure 1.3 shows system level configuration of a solid-state detector front-end.

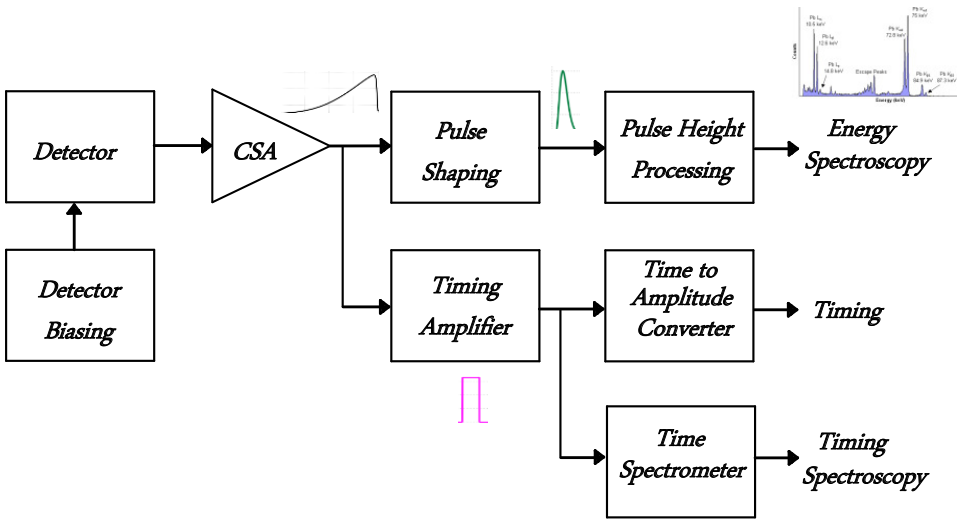

Figure 1.3 General view of a Solid-State Detector Readout System.

Figure 1.4 describes a simplified readout channel consisting of primary circuit blocks once a semiconductor diode, CdZnTe, CdTe or Ge detector is utilized for X- and Gamma-ray detection. The detector can be modeled as described in Figure 1.2 as a capacitive device with high impedance, parasitic or coupling capacitance and some other elements modeling the real-time performance of the detector when exposed to radiation . In this type of front-end system an operational amplifier

based integrator with a feedback capacitance is often used and its output is fed to a shaper to meet the necessary signal conditioning [4].

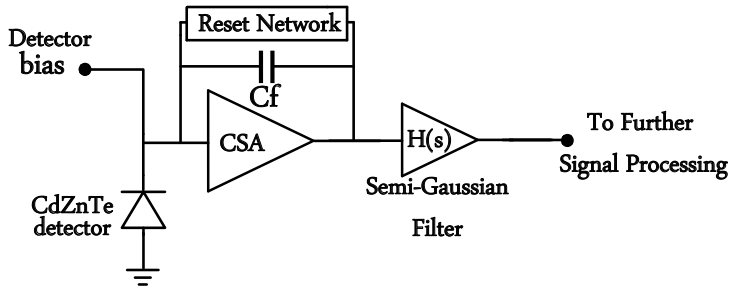

Figure 1.4 Simplified Block Diagram of a Radiation Detector Readout System.

1.2 Motivation

This work relies on the design of an analog programmable front-end channel as readout of a type of radiation detectors named CdZnTe detectors, utilizing X- and Gamma-ray photon counting. The scope of the work is focused on the programmable reset-network of CSA, low-power operation and pulse-shaping of the CSA output signal. The CMOS technology of 0.35um Austria Microsystems is selected due to its prosperous experience in space and radiation hardened applications. A front-end channel realizing the design requirements in terms of noise, power consumption and area with known detector capacitance and peaking time is discussed in this work. Programmability of the system will be investigated to meet count-rate and stability requirements. Since restrictions on size and performance of available passive resistors in CMOS technology enhances the challenges in using large value passive resistors required in high count-rate applications, design and analysis of a new CMOS-based resistor can be advantageous.

The most crucial block out of a detector readout electronics is the Charge Sensitive Amplifier (CSA). Careful investigations in Transistor-level Architecture, circuit techniques, and CMOS device characteristics is required to fulfill the performance requirements for the CSA and the rest of the blocks in the readout channel.

1.3 Contributions of This Work

In this thesis, we provide a detailed analysis and design of solid-state detector readout circuits. We begin by introducing a procedure for device parameter extraction and technology limits to fully understand noise and power constraints in front-end circuits. We provide all essential steps of the procedure, consisting of investigating the specifications, designing the analog blocks, noise evaluation, low-power consumption and layout considerations. We discuss transistor-level design of each block of the front-end channel, compare the proposed design with previous work, and challenge the pros and cons of each system. Furthermore, we present a comprehensive analysis and design of a programmable reset-network for solid-state detectors. The analysis in this work is based on the BSIM 3v3 model of SPICE for MOS transistors which is a valid model for all operating regions of a transistor. Where there is a need for new parameters for a better understanding of the device behaviour, BSIM parameters were used to define the new parameters . Moreover, we provide analysis and design of a programmable low-noise and low-power charge-sensitive amplifier together with a signal processing chain including a Pole-Zero Cancellation (PZC) and a semi-Gaussian filter. Furthermore, design and analysis for a resistor-less nano ampere current source are studied together with its dependency on Process-Voltage-Temperature (PVT) variations. The proposed circuit blocks are simulated in 0.35um deep bulk CMOS process of Austria Micro-Systems (AMS). A brief review of the contributions are listed in the following subsections.

1.3.1 A Low-Power and Low-noise Charge-Sensitive Amplifier

The proposed CSA in this work is intended for capacitive sensor readout circuits, in particular, interface circuits for solid-state detectors utilizing applications in X- and Gamma-ray spectroscopy.

From a signal conditioning point of view, the CSA is an integrator built by a high gain operational amplifier and a capacitor in the feedback loop. Integration of the generated charge pulses by the detector and converting them into voltage pulses is

the main characteristic of the CSA. The generated charge Q_d by the by detector is integrated by the feedback capacitor C_f. Basic circuit theory tells us that charge injection on a circuit node, will reduce the voltage potential difference at that node with respect to the common ground. This means a fall/rise in transient voltage signal at the input of the amplifier (CSA), and thereby due to presence of negative feedback, the CSA sees an amplified transient signal with reverse polarity at its output. Since the CSA has a very large open-loop gain, negative feedback forces the input voltage of the CSA instantaneously zero. Now, one can conclude that all the input charge Q_d is integrated on C_f and we have:

$$v_{ocsa} = \frac{Q_d}{C_f} \tag{1.5}$$

This voltage pulse needs to be discharged with a proper time constant of $\tau_f = R_f C_f$ in order to return the output transient signal of the CSA to the DC baseline, preparing the CSA to integrate the charges of the next coming event. Some useful characteristics of a CSA are listed below in order of importance:

- ENC (Equivalent Noise Charge) :
  ENC determines the minimum detectable charge by the system with the presence of intrinsic noise of the readout.

- Low-power consumption:
  Due to high number of readout channels required for high-resolution systems, power consumption of each channel must be kept as low as possible. On the other hand in some cases, capacitive matching of the detector and input device of the CSA requires large values of bias current. This complicates the low-power design criteria in designing a CSA and requires careful attention in optimizing device sizes and bias conditions.

- High Sensitivity (Gain):
  Charge gain in terms of $mV/fcoulombs$.

- Temperature stability:
  Temperature dependency of circuits is an inevitable issue in analog circuit design. This problem can be optimized by the utilizing circuit design techniques and topologies with less temperature dependency.

1.3.2 Pulse Processing

The signal at the output of CSA is then fed to to a Semi-Gaussian (S-G) filter. The S-G filter's main functions are to increase the Signal to Noise ratio (SNR) and further amplication of the CSA output meanwhile modifying the pulse width for the desired peaking time. From a mathematical point of view, and assuming that the S-G filter has one RC differentiator and n integrators (n also represents shaper's order), one can write transfer function of the S-G filter as:

$$H(s) = [\frac{s\tau_0}{1+s\tau_0}][\frac{A}{1+s\tau_0}]^n \tag{1.6}$$

where τ_0 is the time-constant established by the differentiator (high-pass filter) and integrator (low-pass filter) and A is the DC gain of the integrators.

Peaking-time as an important factor in definition of Full Width at Half Maximum (FWHM) and resolution of the acquired signal is optimized by the time constant of the shaper as below:

$$\tau_s = n\tau_0 \tag{1.7}$$

1.3.3 A Modified Reset-Network

As discussed in previous sections, the generated charge from the detector (Q_d) is integrated on the feedback capacitor (C_f). Once the charge integration is done, the voltage across the C_f must be discharged in order to prepare the readout circuit for the next event. Discharging the C_f either continuously or discretely is realized by a reset network. Attention must be paid in designing the reset-network since it directly contributes to the noise of the front-end. It would be a brilliant idea to adjust the feedback time-constant (τ_f) based on the application and event-rate of incoming energy photons. This can easily result in a better quality for the output pulse due to a smoother fall time of CSA's output signal and removal of unnecessary undershoots. On the other hand, (τ_f) must be significantly longer

than the shaping time (τ_s) and also short enough to prevent pulse pile-ups. In most applications, aforementioned conditions result in a high value feedback resistance (R_f). Implementing such a resistor challenges the limits of fabrication and area together with process and temperature variation dependency and noise contribution. In our work, we propose a new programmable reset-network capable of dark current compensation up to $10nA$ and 256 selections for the value of R_f. Depending on the target application, a broad list of reset-networks can be found in the literature. Some of the most common structures are shown in Figure 1.5. Advantages and disadvantages of each reset-network are listed in Table 1.1.

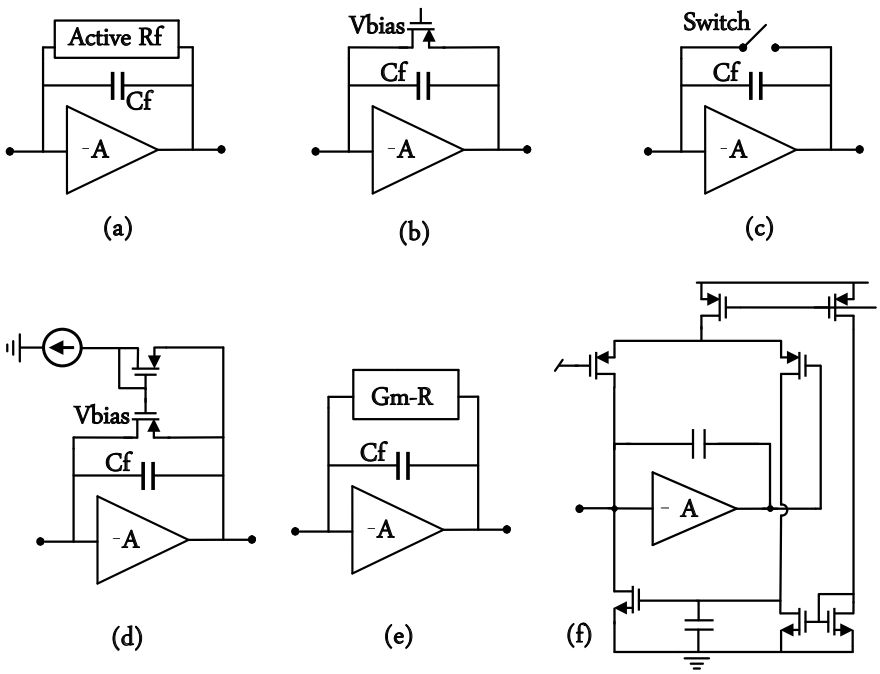

Figure 1.5 Some of the most common structures for reset-networks used in solid-state detector readout front-ends. (a) Reset-network using passive R_f [6], (b) MOSFET in triode region [7], (c) Switched based reset [8], (d) Current mirror based reset [9], (e) Transconductor-R based resistor [10], (f) Krummenacher low-frequency feedback loop [11].

1.4 Design parameters of Readout System for Solid-State Detectors

Table 1.1 Advantages and disadvantages of each reset-network in Figure 1.5.

	Pros	Cons
(a)	simple	small R_f
(b)	simple	non-linear
(c)	simple	Charge injection
(d)	simple	DC shift at V_{out}
(e)	Highly linear	BiCMOS process used, fixed R_f
(f)	Fixed Baseline, I_{dark} Compensation	Noise, fixed R_f, undershoot

In this section, we will discuss about some useful parameters and performance metrics of a front-end system for solid-state detectors.

1.4.1 Equivalent Noise Charge (ENC)

Figure 1.6 shows a common output signal of a readout circuit for solid-state detectors when the same input stimuli is repetitively applied. (This is obtained using multiple-run feature of simulation software such as Cadence or SPICE). In this case, an input charge of 1 and 1.2 fC is the input charge coming from the detector and the readout system described in Figure 1.5 has a gain of 135mV/fC and 5 μs peaking time. As observed here, the different output signals do not overlap, however they lay within a band. This is due to the noise in the system. The term 'noise' represents unfavored signals and disturbances produced with the detector and front-end circuit. This noise is intrinsic to the system and shielding the system can not eliminate it.

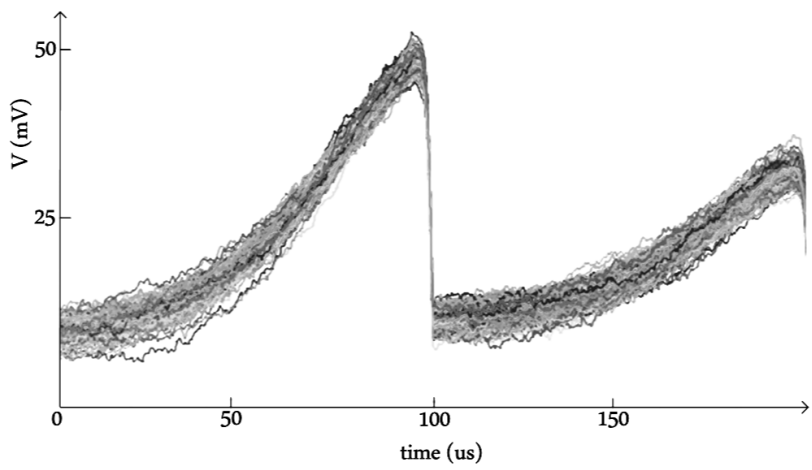

Figure 1.6 Output of the front-end CSA including intrinsic noise effect.

Origins of noise stems from the fact that the charge carriers in electronic circuits are in finite numbers and move at finite speed. Any variation in the speed or number of charge carriers lead to voltage or current fluctuations inside the circuit. In the jargon of front-end electronics and sensor interface design, noise is usually defined as Equivalent Noise Charge (ENC) referred to the amplifier input. Quoting the noise in terms of ENC paves the way for a quick comparison between noise-floor and the desired output signal. To have a better understanding from the ENC and its effect in acquiring high resolution output signal, if the first peak value of waveform in Figure 1.6 is sampled, it can be observed that the signal fluctuates about 8-10 mV from its average value of 50 mv. Since the front-end offers a sensitivity of 135 mV/ fC, one can calculate the ENC as following:

$$\frac{8mV}{135mV/fC} = 0.059fC \tag{1.8}$$

which corresponds to a charge of 369 electrons. This number for ENC may vary from less than ten electrons in high resolution spectroscopy to thousands of electrons in large capacitive detectors with high charge generation capability such as Silicon Photomultipliers.

In general, noise sources in the front-end are transistor-level devices in the readout electronics, detector dark current and bias network of the detector. In noise analysis of a front-end circuit, noise sources are expressed in terms of voltage or current contributions. Voltage and current noise sources are connected in series and parallel with the amplifier input to utilize the concept of equivalent noise sources, which states that the noise of a given device is referred to the system input.

Thermal and flicker noise are the most common noise sources in every electronic circuit. Fluctuations in speed of the charge carriers due to thermal agitation generate the thermal noise. Thermal noise is also known as “white noise” .On the other hand, even with the absence of net current flowing in a circuit, charge carriers still move randomly due to the kinetic energy associated to the temperature and this results in noise generation (colored noise) . Flicker noise is a known colored noise source in semiconductors [12],

$$v_{n,f}^{2} = \frac{K_f}{f} \tag{1.9}$$

where K_f (Flicker noise coefficient) is a fitting parameter, constant for a given device and f is frequency.

On the other hand, thermal noise can be approximated by the equation below:

$$v_{n_w}^2 = \frac{4K_B T \lambda n}{g_m} \tag{1.10}$$

where K_B is the Boltzmann constant, T in temperature in $Kelvins$, λ is a device parameter whose value is ranging 2/3 to 1 from sub-threshold to strong inversion and n is sub-threshold slope factor. Noise is also generated by the detector and its associated bias network. For instance, in CdZnTe detectors, irradiation produces a current known as "dark / leakage" current which can be modeled as a DC current source in parallel to the front-end input.

$$i_n^2 = 2qI_{dark} \tag{1.11}$$

Figure 1.7 shows a fairly accurate model of a front-end with input-referred parallel and series noise sources [12]. It is worthwhile to mention that parallel noise is all noise sources modeled as a current contribution and series noise denotes voltage contribution of a noise source.

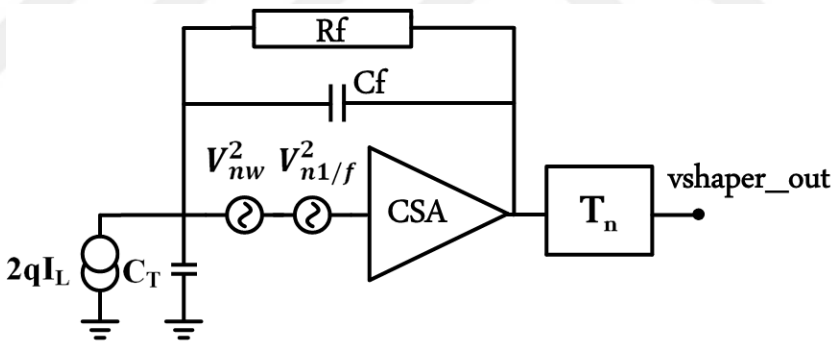

Figure 1.7 Front-end amplifier with input-referred parallel and series noise sources.

1.4.2 Noise Minimization of Detector and the Front-End

According to [12], ENC can be written as Equation (1.7).

$$ENC^2 = \frac{1}{q^2}[ENC_f^2 + ENC_w^2 + ENC_i^2] \tag{1.12}$$

where each term can be analyzed separately as below:

$$ENC_f^2 = \frac{K_f}{WLC_{ox}} N_f C_T^2 \tag{1.13}$$

$$ENC_w^2 = \frac{4K_B T \lambda n}{g_m} \frac{C_T^2}{T_p} N_w \tag{1.14}$$

$$ENC_i^2 = 2qI_{dark} N_i T_p \tag{1.15}$$

In Equations (1.13)-(1.15), C_T N_w, N_i and N_f are coefficients introduced by the shaper. T_p is the peaking time. C_T is the total capacitance which is the sum of detector capacitance and all the capacitance that is seen at the gate of the input transistor [4, 12]. The goal is to minimize total ENC in expression (1.12). We will analyze flicker, thermal and parallel noise contributions separately. Investigating the Equations (1.13)-(1.15), it is observed that large value of WL and low values of γ/g_m correspond to minimization of flicker and thermal noises; respectively. This is interesting since in case of a fixed current for the MOS, if we increase W by keeping L constant, we are pushing the transistor into weak inversion with corresponds to high values of γ/g_m. This means that for a fixed current there is an optimum W where flicker and thermal noise contributions are equal. In order to determine the optimum W, a SPICE simulation was performed implementing the above expressions directly into the SPICE netlist.
Taking the square root of (1.12) we obtain the equivalent noise charge in electron rms. A few critical points must be noted about (1.12):

- The effect of series noise (both thermal and 1/f) is directly proportional to C_T, hence detectors modeled by a small capacitance are more preferable for low-noise measurements.
- The thermal series noise and the parallel noise contribute to ENC in opposite ways by the T_p. Long peaking times decrease the contribution of series noise and enhance the one of parallel noise, and vice-versa.
- Flicker noise is not affected by T_p.

1.4.3 Peaking Time

The time required for the signal to arise from the baseline to its peak value is called the peaking time. Note that the peaking time is measured from the baseline to the peak, so from 0% to 100% of the signal, while the rise time is calculated from the 10% and 90% points. Peaking time is a critical parameter in front-end circuit design, since it determines both the speed and the noise of the system. Its value may range from a few nanoseconds (fast systems used in timing measurements) to several micro seconds common of front-end for high-resolution spectroscopy. An output signal with large T_p will be similar to an ideal Gaussian pulse. Optimization of T_p is advantageous for providing a better energy resolution of the readout system. Peaking time is defined by Equation (1.7) in section 1.3.2. Moreover, together with the order of the used shaper, peaking time can be related to total ENC and noise minimization. An optimum value for peaking time is given in [12]:

$$\tau_s = C_T \left(\frac{8.K_B.T.n^2}{6.g_m.q.I_{bias}.(2n-1)} \right)^{\frac{1}{2}} \tag{1.16}$$

where C_T is the total capacitance seen from the input of the front-end, K_B is Boltzmann's constant, T is temperature, n, g_m and I_{bias} are input transistor parameters for subthreshold slope factor, transconductance and bias current, respectively. In Equation (1.16), we are considering that the intrinsic noise of the front-end amplifier is dominated by the input transistor and in this case a Metal-Oxide Field Effect Transistor (MOSFET) available in CMOS technology. Please note that, in definition of peaking time, it is assumed that the input stimuli to the front-end is a Dirac-delta, i.e the impulse response. If the peaking time is much longer than the sensor signal collection time, the impulse response describes with good approximation also the front-end response to the actual detector signal. If this is not the case, the output is obtained from the convolution between the detector signal and the front-end impulse response and, for the same total charge, exhibits a smaller peak than the one observed with a Dirac-delta input. This amplitude loss is called ballistic deficit [4, 12].

1.4.4 Gain and Sensitivity

The gain of a front-end is considered as the ratio between the peak of the output voltage and the input charge. In Figure 1.4, we have assumed a system with a charge of 1-1.2 fC, obtaining an output peak value of 35mV and 50 mV, thereby the sensitivity is 35-50 mV/fC. In some other cases, the sensitivity is expressed in Volt per electron, although this terminology is less frequent in the solid-state detector jargon. In a linear system, the sensitivity shall be chosen so that the maximum signal of interest brings the amplifier to its maximum possible headroom. For instance, the output stage of an amplifier working with 3.3 V power-supply may saturate if the output signal is below 0.5 V or above 2.6 V, resulting in a maximum linear output range of 2.1 V. The ratio between the maximum output voltage for which the front-end amplifier still keeps the proportionality between the input and the output signal and also the rms noise-level at the output is named the output linear dynamic range and, divided by the sensitivity, leads to the input linear dynamic range. In our example the amplifier was designed for a sensitivity of 50 mV/fC. In case the front-end output stage has a linear range of 2.1 V, the maximum signal that can be handled by the circuit without meeting its saturation limits is 42 fC. Thereby, it is of great significance to design a front-end which has a higher sensitivity and larger linear range.

In this work, we have designed a front-end circuit which provides a sensitivity of 135 mV/fC in a circuit with 3.3 V power-supply. Applying the same method used in our previous example, the maximum signal that our circuit can handle without saturation is 15 fC. This is well beyond the enough value for hard X-ray spectroscopy and medical imaging purposes.

1.5 Performance comparison of related work

In this section a performance comparison in terms of the key design parameters will be discussed briefly, however before we move on with a listing the key parameters, an overview of the current trends in CMOS readout front-end systems will be summarized. High Integration density, fabrication cost, and CMOS Technology

scaling are the rising challenges for engineers and companies working on radiation detection front-ends. These challenges encompass low-power consumption, low-noise performance, high-speed and high-precision of a front-end channel.

Efforts have been made towards scaling submicron CMOS technologies in terms of integration, analysis, and radiation tolerance [16]. Such works have investigated deep submicron technologies for readout front-end systems above 100 nm minimum feature size to below 100 nm like 90 nm and 65 nm.. However, further investigations are required to confirm the reliability of new submicron CMOS technologies below 100 nm. The study suggests that submicron CMOS technologies like $0.25\mu m, 0.18\mu m$, and $0.13\mu m$ using minimum feature size are still reliable choices for low-noise design of front-end electronics since they have offered good radiation tolerance in harsh environments [16, 17].

The overview of the related studies in terms of key design parameters discussed in previous sections has led to some interesting conclusions. Starting with the peaking time (T_p), some of the recent work have reported a peaking time above 1 μs [13, 15] whereas some others [12, 14], has confirmed well below or equal to 1 μs peaking time. On the other hand, the detector capacitance (C_{det}) together with an optimized peaking time is used to the meet performance requirements. Moreover, another significant performance achievement is being made in terms of ENC and power consumption in [18] and is due to the small value of detector capacitance , which otherwise could not be feasible. Hence the input capacitance and the peaking time are significant factors in determining the ENC and power consumption.

The summary in Table 1.2 includes a quality factor introduced by Christer Svensson [19]. All key parameters of a solid-state detector front-end readout except area have been taken into consideration by this formula. This quality factor suggests that high-performance readout front-ends should have a quality factor as low as possible and it can be calculated as following:

$$QF = \frac{ENC^2 P \tau_P}{C_g^2} 10^{-18} \tag{1.17}$$

Where, P is the power consumption of a single channel, τ_P is the peaking time and C_g is the detector and total input capacitance at the input node. provided that the

Table 1.2 Performance comparison of some single photon counting front-end systems.

No	Ref. work	$\mathbf{C_{dw}}$[**pF**]	Peaking time [ns]	ENC [e-rms]	P[mW]	QF
1	Sansen [12]	40	1000	600	10	2.25
2	Beikahmadi [13]	0.25	1140	66	1	1.2
3	Geronimo [14]	2	1000	92	18	39
4	Noulis [15]	5	1810	487	1	17.2

power consumption of digital part of the readout channel is negligible compared to analog circuit blocks and will not affect the quality factor value.

1.6 Requirements of this work

In this work a very precise pre-defined specifications in terms of performance parameters are to be achieved. A T_p of $5\mu s$ is to be obtained for a wide range of count-rates. The front-end noise should not exceed 50-150 ENC with an overall power consumption to be within 3-4 mW from a supply voltage of 3.3V available in C35b4m3 CMOS precess of Austria Micro-Systems (AMS). The detector capacitance is 10pF and can sum with parasitic capacitance to form a total capacitance of 11-12 pF, approximately. These requirements are presented in the Table 1.3 with the calculated QF.
Besides the requirements listed in Table 1.3, other specifications are:

- **Input**:
  X-ray intensity is determined to be 100-250 kHz per pixel and a corresponding photon approximately generates a maximum of 20000-25000 electrons in case of a CdZnTe detector in Hard X-ray spectroscopy.

- **Programmability**
  The proposed readout electronics system should be programmable for diffirent count-rates.This will be obtained through selection of Digital to Analog Converter (DAC) bits which lead to implementing multiple time-constants for the reset network.

- **Temperature Range**
  -20 to $+70°C$.

Table 1.3 Requirements of this work.

Ref. work	$\mathbf{C_{dw}}$[**pF**]	Peaking time [ns]	ENC [e-rms]	P[mW]	QF
This work	2-12	4-5	50-150	2-4	1.8-12

Please note that while calculating the QF for the designs listed in Table 1.4, one has to assume a value for the C_{det} within the written range. In generic, high value of C_{det} results in an increase in ENC value. However, since nominator and denominator of Equation (1.17) includes C_{det}, one can conclude that QF is independent of C_{det} value. And thereby, QF can be considered a significant performance comparison factor.

1.7 Front-end Architecture of this work

In this section, we present a brief introduction to the readout electronics architecture used in this work. System-level architecture of the front-end system is depicted in Figure 1.8. Detailed analysis of each individual block is discussed in the following chapters. The reset-network of the CSA is implemented utilizing a modified topology of low-frequency feedback (Krummenacher reset-network) which offers multiple values for the reset-network's active resistance [11]; Making the overall front-end suitable for various event-rates and applications. This architecture also incorporates a pole-zero cancellation block (PZC) [14, 24]. The PZC is required to eliminate the drawbacks of the pole introduced by the feedback time-constant (τ_f) at higher event-rates [25]. Some of these drawbacks are:

- Undershoots at the output of the shaper.
- Pulse pile-ups at the output of CSA.

The undershoot caused by the reset network is cancelled once the following condition is met by the Pole Zero Cancellation (PZC) circuit:

$$R_f C_f = R_{M_{pz}} C_{pz} \tag{1.18}$$

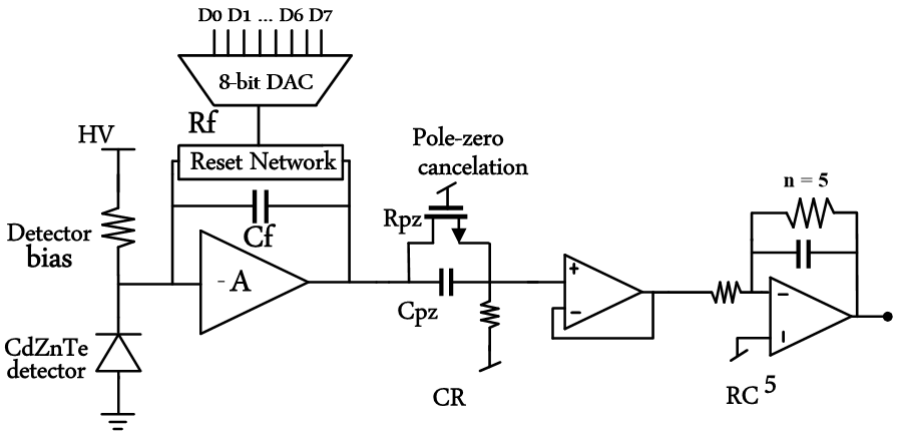

Figure 1.8 System Architecture of the this work.

Hence, use of a configurable R_{pz} can modify the elimination of undershoot even if R_f is changed. In this work we have implemented R_{pz} as a MOSFET in triode region that is configured externally by applying a DC voltage in range of 0-3.3V to its gate.

After the PZC circuit handles the potential undershoot, the obtained signal is fed to a Semi-Gaussian filter which is formed by a high-pass filter followed by a voltage buffer and 5 replicas of a low-pass filter, resulting in a $5^th-order$ S-G filter.

1.8 CMOS Process Technology Parameters

In this work, we have used $0.35\mu m$ C35b4m3 CMOS process technology of Austria Micro-Systems (AMS). It is of great significance to have a deep understanding of the technology device models and their parameters definition and values. The CMOS device noise model parameters are inevitable factors in low-noise design and noise-matching of the analog interface to the detector. The C35b4m3 process technology of AMS is utilizing BSIM3V3 device models for the purposes of simulation, and its noise model is based on noise model 2 equations of general BSIM3v3 which are very trustworthy for noise estimation particularly for flicker noise approximation. The parameters necessary for our design are approximated using extraction and noise parameters from [26, 27]. These parameters are listed as following:

- Oxide thickness $t_{ox} = 7.754nm$

- Threshold voltage V_{th}:
  - PMOS $V_{th} = -0.72V$
  - NMOS $V_{th} = 0.52V$
- Process Transconductance μC_{ox}:
  - PMOS $\mu_p C_{ox} = 58\mu A/V^2$
  - NMOS $\mu_n C_{ox} = 205\mu A/V^2$
- Flicker Noise Coefficient K_f :
  - PMOS $K_{fP} = 1.191 \times 10^{-26}$
  - NMOS $K_{fN} = 2.170 \times 10^{-26}$

The device models in AMS $0.35\mu m$ utilize the following thermal noise equations based on the BSIM3v3 model. Detailed information can be found in [26].

$$i_{nd}^2 = \frac{4K_B T \mu_0}{L^2 + \mu_0 \mid Q_{inv} \mid R_{ds}} \mid Q_{inv} \mid \tag{1.19}$$

Where for Q_{inv} we have:

$$Q_{inv} = -WLC_{ox}V_{gseff}(1 - \frac{A_{bulk}.V_{ds}}{2(V_{gseff} + 2V_{tm})}) \tag{1.20}$$

On the other hand for the flicker noise the following equations are provide:

$$i_f^2 = \frac{V_{tm} q^2 I_{ds} \mu_0}{(f_f^E) L^2 C_{ox} 10^8}[P_N] + \frac{V_{tm} I_{ds}^2 \Delta L_c lm}{f_f^E L^2 W.10^8} \frac{N_{oia} + N_{oib} N_l + N_{oic} N_l^2}{(N_l + N_{oid})^2} \tag{1.21}$$

where $[\mathrm{P}_N] is:$

$$[P_N] = [N_{oia} log(\frac{N_0 + (2.10^{14})}{N_l + (2.10^{14})}) + N_{oib}(N_o - N_i) + \frac{1}{2} N_{oic}(N_o^2 - N_l^2)] \tag{1.22}$$

All the parameters used in Equations (1.15)-(1.18) can be found in BSIM model technology file which is provided by the foundry [28] except N_o and N_l which can

be derived from equations below:

$$N_0 = \frac{C_{ox}(V_{gs} - V_t h)}{q} \tag{1.23}$$

And for N_l:

$$N_l = \frac{C_{ox} V_{gseff}(1 - \frac{A_{bulk} V_{dseff}}{V_{gseff} + 2V_{th}})}{q} \tag{1.24}$$

2. Input Transistor Optimization and Analysis

This chapter includes the design and analysis of the Input Stage in readout front-end system. It is dedicated to an overview of input transistor sizing and optimization for a given capacitive detector specifications. Dependence of front-end performance on the input device and its contribution to noise, power dissipation, and input capacitance, Moreover input transistor type and sizing is presented based on the analysis, EKV modeling and simulation results. Then, noise analysis and capacitance-matching will be discussed based on simulation results for device optimization. It is worthwhile to notify that all the simulation results throughout this work is based on utilizing AMS models of the MOSFETs for SPICE and Cadence Design Systems (CDS) and we rely on these models in our proceedings [28]. Figure 2.1 demonstrates an overall view of design principle.

2.1 Input Transistor Optimization and Sizing

The first unit in the the signal processing chain of SSDs is the input transistor of CSA in the readout channel. Input transistor design is of great importance in the front-end design and consist of optimization related to the detector input capacitance and noise contribution. Subsequently, optimization process relies on equations related to modeling, and other factors that can be effectively bounded to CMOS process technology [29].

Efforts have been made regarding input transistor analysis, optimization and its relation to key parameters of SSD readout front-end and detailed low-noise design techniques have been provided in [30, 31]. The design constraint is not that straightforward and strongly depends on simulation analysis regarding noise optimization in a chosen CMOS process technology, where technology noise parameters such as

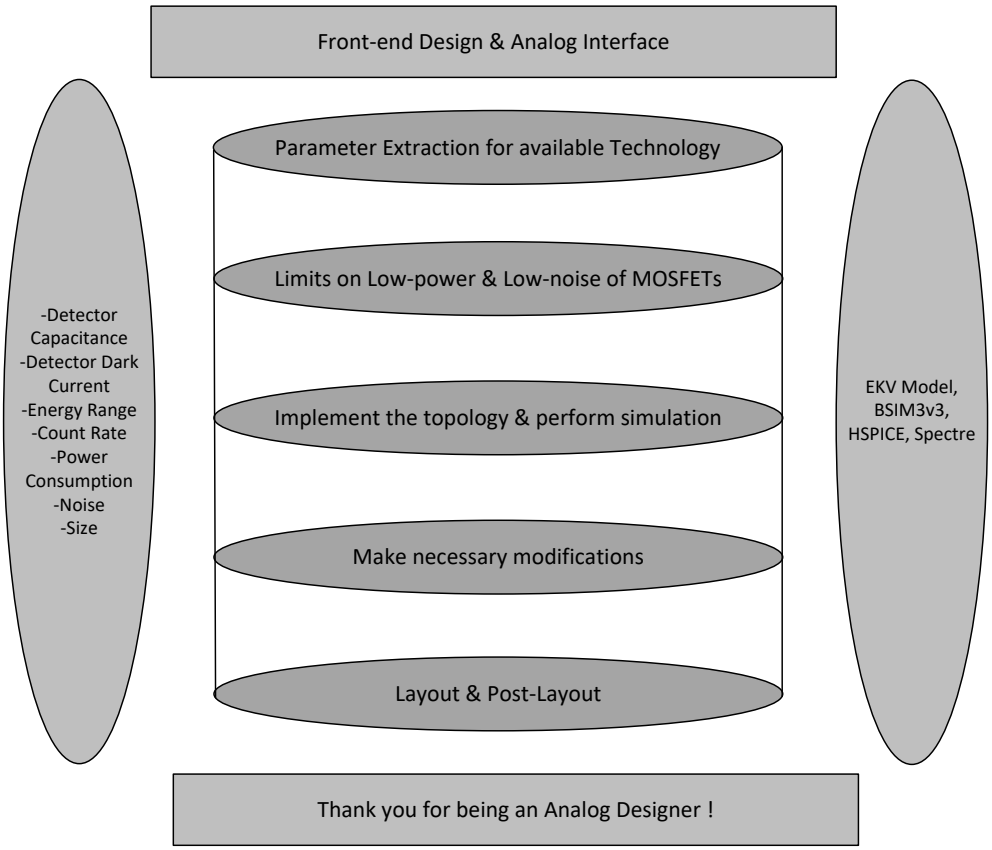

Figure 2.1 General view of the required work in front-end design for solid-state detectors.

fitting parameters and noise coefficients are gaining more importance and their approximate modeling is complex. In [32] a detailed analysis is provided considering secondary effects to derive an analytical model for noise. Generally, In steps of optimizing the noise, the front-end designer has to pay attention to the simulation which utilizes device models for noise particularly for flicker or $1/f$ noise. It is worthwhile to mention that BSIM3v3 models provide one of the most reliable approximations for noise specially the flicker noise and have proven to be valid compared to measurement results in [33, 34].

2.1.1 Significant parameters for input transistor sizing

Literature found in [2-41], following parameters are classified to be the most significant parameters in the hierarchy of necessary steps for input transistor sizing:

- **CMOS Process Technology:**
  Noise performance of the input MOSEFT relies on the CMOS process technology parameters related to the noise model, starting with flicker noise coefficient as a fitting parameter, to subthreshold slope factor and oxide capacitance, varying over device scaling. Noise performance of different CMOS technologies is published in [35, 36]. Subsequently, another fact of the scaled device technologies specially in deep submicron technologies is their radiation tolerance/hardness [35].

- **Fabrication Company:**
  Noise parameters might vary for an specific CMOS technology. The study in [36] reports the values and focuses on the differences between noise parameters of a particular technology. The oxide thickness can differ among fabrication foundries and its value is directly related to the noise parameters.

- **Detector Capacitance:**
  Noise performance can be affected directly by the detector capacitance (C_{det}). Regarding the biasing condition of the MOSFET , its gate capacitance of can be related to the detector capacitance which sums up to the total input capacitance introducing the most significant factor in peaking time and target ENC optimization. Further information about sizing and capacitance-matching is provided in [35].

- **CMOS Input Device Type:**
  Choice of the CMOS device to be P-type Metal Oxide Field Effect Transistor or N-type Metal Oxide Field Effect Transistor (MOSFET) is significant for noise behaviour. The K_f parameter of flicker noise differs for PMOS and NMOS devices due to charge carrier type and its mobility.

- **Input Device Operation Region:**
  Power consumption is of great significance due to implementation of multichannel readout systems in SSD's readouts and is directly related to the operation region of transistors used in readout circuitry since it determine a certain value of transconductance g_m and thereby the biasing condition.

- **Peaking Time:**
  Peaking time known as the most critical parameter in optimization process and pulse processing chain, determines resolution and FWHM together with bandwidth and frequency-domain analysis.

2.1.2 Noise

Intrinsic noise sources of a MOSFET and its equivalent model named as input-referred or gate-referred noise are presented in Figure 2.2 [4].

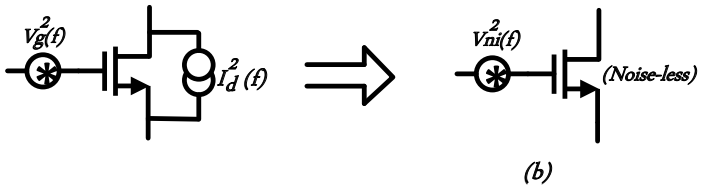

Figure 2.2 MOSFET thermal and flicker noise sources (a) and its equivalent gate-referred model (b) .

The thermal noise of the MOSEFT is dependent on the region of operation. In strong inversion region the input referred or gate-referred noise voltage spectral density is given as:

$$V_{g\,thermal}^2 = \frac{4K_BT\gamma}{g_m} \tag{2.1}$$

Where K_B, T, and g_m are Boltzmann constant, temperature, and transconductance, respectively. γ coefficient value varies from 2/3 for long channel and between 3/2 to 2 for submicron (short-channel) devices. However, the Equation 2.1 is no longer valid for a MOSFET operating in weak inversion. Equation 2.2 defines gate-referred thermal noise of a MOSFET operating in weak inversion.

$$V_{g\,thermal}^2 = \frac{2qnV_T}{g_m} \tag{2.2}$$

where n , q , and V_T are subthreshold slope factor, charge of one electron, and threshold voltage, respectively.
Nevertheless, no explicit equation for quick calculations has been defined for a MOSFET operating in moderate inversion region. Although, boundary condition expressions in weak and strong inversion regions are still valid in this region, but use of Computer Aided Design tools and performing simulations based on models such as BSIM or Spectre are more preferred by circuit designers.

On the other hand for the Flicker (1/f) noise, we have [35]:

$$V_{g\,flicker}^2 = \frac{K_f}{WLC_{ox}^2 f} \tag{2.3}$$

2.1.3 MOSFET Gate Capacitance and Size

In strong inversion region g_m is a function of input gate capacitance (C_g) through device geometry as given in following expression:

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{nL}I_{ds}} \tag{2.4}$$

Since in strong inversion we have $C_g = WLC_{ox}$ Equation 2.3 can be simplified in terms of C_g as below:

$$g_m = \sqrt{\frac{2\mu I_{ds}}{nL^2}}\sqrt{C_g} \tag{2.5}$$

The optimum value of $C_{tot} = C_g + C_d$ for thermal noise minimization is achieved in strong inversion region using the expression derived in [12] as:

$$C_g = \frac{C_d}{3} \tag{2.6}$$

However, since in moderate inversion, no explicit expression is defined for quick calculations, Equation 2.5 can not be derived easily for the moderate inversion. And only simulations based on numerical methods can lead to an approximate optimum value of C_g for thermal noise minimization. Figure 2.3 shows gate capacitance and drain current of a PMOS4 model of $0.35\mu m$ AMS versus V_{gs} variations. In this work and generally in jargon of detector readout fron-end, C_g is the input capacitance of the MOSFET which is the summation of gate-bulk and gate-source capacitances. From EKV model C_g depends on Inversion Coefficient (I_C). I_C is discussed in section 2.4. Conventional modeling of MOS input capacitance assumes high values of I_C (strong inversion) and lead to the famous formula of $C_g = \frac{2}{3}WLC_{ox}$. However, based on EKV model the generic expression for C_g is defined as [4]:

$$C_g = C(x)WLC_{ox} \tag{2.7}$$

Where $C(x)$ is:

$$C(x) = \frac{n - \frac{1+x}{3}}{n} \tag{2.8}$$

And for x, we have:

$$x = \frac{(\sqrt{I_C + 0.25} + 0.5) + 1}{(\sqrt{I_C + 0.25} + 0.5)^2} \tag{2.9}$$

Equations (2.6) - (2.8) indicate that gate - capacitance of a MOSFET only depends on size and Inversion Coefficient (I_C) if variations in subthreshold slope factor n is negligible. This facilitates the design procedure for capacitive matching and noise minimization of the front-end circuit for required power consumption assuming that the input MOSFET is the dominant noise source of the CSA. Investigating Equations (2.1) - (2.8), it is observed that Large values of WL and small values of γ/g_m correspond to minimization of Flicker and thermal noises, respectively. This is interesting since in case of a Fixed current for the input MOSFET, if we increase W by holding L constant, we are pushing the transistor into weak inversion which corresponds to high values of γ/g_m. This means that for a fixed current there is an optimum W where Flicker and Thermal noise contributions are equal. Our goal is to determine that optimum W.

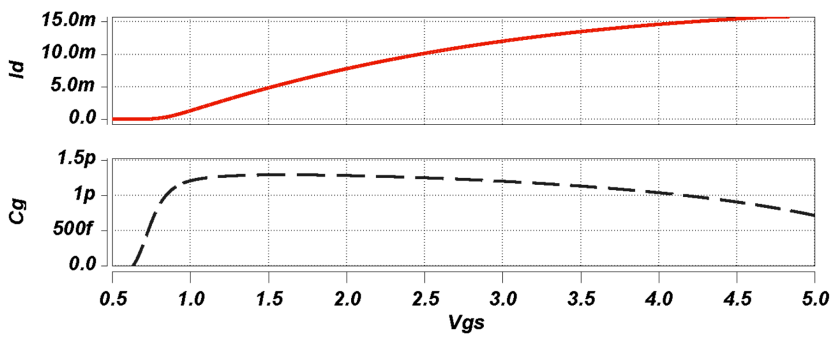

Figure 2.3 I_d vs. V_{gs} and C_g vs. V_{gs} graphs of a PMOS4 transistor of $0.35\mu m$ of AMS with $\frac{W}{L} = \frac{700\mu}{0.8\mu}$.

2.2 Input Transistor Design and Polarity

2.2.1 Fundamentals of MOSFET and Operating Regions

Analog CMOS design is extensively complicated by the further degrees of design freedom, trade-offs, inversion level and device size. These factors make CMOS design more difficult compared to designing circuits based on Bipolar Junction Transistor. MOSFET inversion level are discussed in this chapter utilizing a factor named as Inversion Coefficient (I_C) to give a deep understanding of MOSFET operation for the reader. I_C is a numerical measurement factor of MOSFET inversion which defines the operating regions as following [37]:
If $I_C < 0.1 \Rightarrow$ MOSFET is in Weak Inversion and it can be modeled similar to a BJT. For Moderate Inversion we should have $0.1 < I_C < 10$ and if $I_C > 10$, MOSFET is operating in Strong Inversion. Figure 2.4 summarizes how inversion coefficient (IC) is related to operating regions.

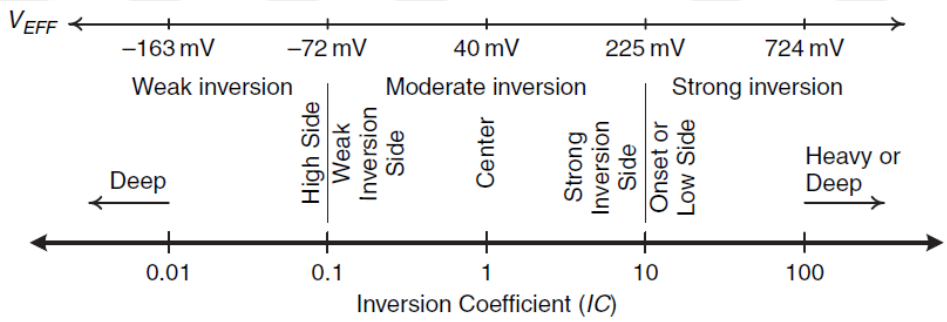

Figure 2.4 The inversion coefficient presented as a number-line demonstrating the regions of MOSFET inversion with the related effective gate–source voltage, $V_{eff} = V_{gs} - V_{th}$ for room - temperature T = 300K and an average subthreshold slope factor of n = 1.21 [37].

The regions of inversion are discussed below in terms of IC and the associated V_{eff}. Furthermore, a brief summary about MOSFET g_m/I_D (transconductance efficiency), V_{eff}, V_{DSsat} (drain–source saturation voltage), intrinsic voltage gain, and intrinsic bandwidth are presented.

- **Deep weak inversion.** $I_C < 0.01$, $V_{eff} < -163mV$
  Large device size ratio, channel width, and the required area by the MOSFET result in high values for gate capacitance, very low band-width (recall from

basic frequency response of a single stage amplifier, $BandWidth \simeq g_m/C_g$), and high DC-leakage in terms of gate leakage-current of MOSFET, operation of MOSFET in this region is not preferred. There is an slight increase in gm/I_D or decrease in V_{DSsat} value in this region compared to the deeper side of weak inversion. This region of Operation may be used for ultra low drain currents.

- **High side of weak inversion** I_C =0.1 , $V_{eff} = -72mV$.
  This point is the boundary of weak and moderate inversion. Operation here provides approximately the maximum value of g_m/I_D of deep weak inversion, small values for V_{eff} and V_{DSsat}, high gain, and better frequency performance compared to deep weak inversion.

- **Weak-inversion side of moderate inversion.** $0.1 < I_C < 1$, 72mV $< V_{eff}$ $<$ 40mV.
  This sub-region determines the boundary of weak inversion and the center of moderate inversion, with $I_C = 0.3$ corresponding to the geometric center between weak and moderate inversion. Operation here provides high gm/ID, low V_{eff} and V_{DSsat}, high gain, and improved bandwidth compared to the prior inversion sub-regions.

- **Center of moderate inversion.** $I_C = 1$, $V_{eff} = 40mV$
  Operation in the center of moderate inversion provides low V_{eff}, V_{DSsat}, and appropriate value for gm/I_D and gain with modest bandwidth.

- **Strong-inversion side of moderate inversion.** $1 < I_C < 10$, 40mV $<$ $V_{eff} <$ 225mV
  This sub-region corresponds to the center of moderate inversion and the boundary or onset of strong inversion, with $I_C = 3$ representing the geometric center between moderate and strong inversion. Operation in this sub-region results in modest gm/I_D, increasing V_{eff} and V_{DSsat}, good gain, and adequate bandwidth for most of the applications.

- **Onset of strong inversion.** $I_C = 10$, $V_{eff} =$ 225mV.
  This sub-region of strong inversion provides low g_m/I_D, high values of V_{eff} and V_{DSsat}, low gain, and high bandwidth.

- **Low side of strong inversion:** $10 < I_C < 100, 225mV < V_{eff} < 724mV$
  Operation in this sub-region provides declining values for g_m/I_D, high and increasing V_{eff} and V_{DSsat}, low and declining gain, and outstanding bandwidth. Since high values of V_{eff} and V_{DSsat} are dominant, operation of this sub-region might not be suitable for low-voltage designs. Moreover, important

velocity-saturation reduction in g_m/I_D and increment's in V_{eff} are mostly for short-channel nMOS devices which could also lead to poor frequency response by saturation or level- off of bandwidth.

- **Deep strong inversion:** $I_C > 100, V_{eff} > 724mV$.
  Keeping a device in deep or heavy strong inversion is difficult due to small W/L ratio and the required channel width. Thereby, this sub-region of operation is not as advantageous as previous regions in low-voltage designs due to high value of V_{eff} and V_{DSsat}. Transconductance-Efficiency (g_m/I_D) and voltage -to - voltage gain is very low.

Throughout this work, moderate inversion region is considered for sizing transistors and capacitive matching to the solid-state detector. And since moderate inversion requires low values of V_{eff} and V_{DSsat} it is superior to other operating regions in terms of low-voltage operation. Furthermore, g_m/I_D and voltage gain are relevantly high, bandwidth is adequate for most of the applications, and velocity saturation mitigation in g_m/I_D and increments in V_{eff} are negligible, even for short-channel devices [37].
The inversion coefficient is used throughout this work to provide analytical expressions for the rest of the CMOS transistor parameters and can be calculated easily by [4, 37]:

$$I_C = \frac{I_D}{I_0(\frac{W}{L})} \tag{2.10}$$

where I_0 is called technology current and I_C represents the inversion coefficient. The technology current is the drain current of a MOSFET with size ration of unity at which device is operating in the center of moderate inversion and can be calculated by equating transconductances in weak and strong inversion regions:

$$g_m(W.I) = g_m(S.I) \tag{2.11}$$

From equations (2.4) and (2.5), we have:

$$\frac{I_d}{nV_T} = \sqrt{2\mu C_{ox}\frac{W}{nL}I_d} \tag{2.12}$$

Solving for the I_d (M.I.) = I_d (W.I.) gives:

$$I_d = 2n\mu C_{ox} V_T^2 (\frac{W}{L}) \tag{2.13}$$

Normalizing it by division to the device size, I_0 is obtained as:

$$I_0 = 2n\mu C_{ox} V_T^2 \tag{2.14}$$

This is the drain current for a device with $W/L = 1$, operating in the center of moderate inversion where the estimated g_m of weak- and strong-inversion regions are equal.
In Equation 2.14 , n is the factor which decreases slightly (starting from weak inversion) with the increasing V_{gs} which is associated with increasing I_C (deriving the device into strong inversion) Figure 2.5. However, one can ignore the variations of n in a particular region of operation. For instance, in case the designer is decisive about the operation of device near the center of moderate inversion, assuming a fixed value for n can be a reliable choice.

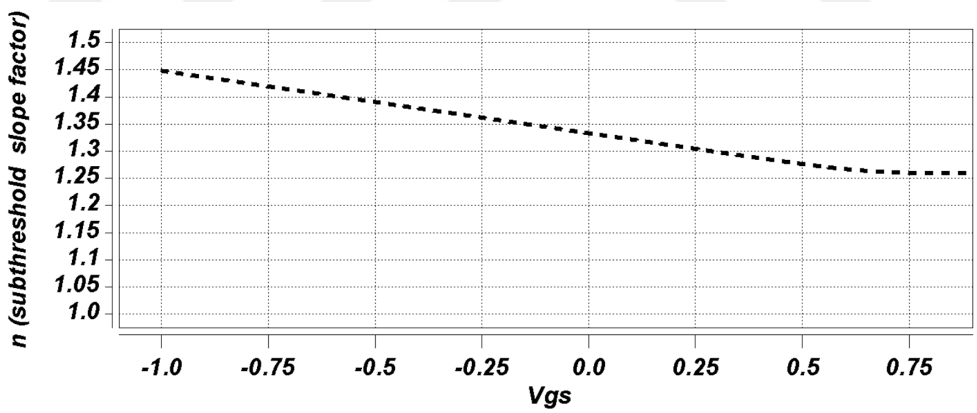

Figure 2.5 Extracted subthreshold slope factor, n, versus gate–source voltage for a PMOS4 CMOS transistor with W/L = 700u/0.8u.

We have already discussed the relation between g_m and I_d for strong inversion region in Equation (2.4). In weak inversion region, operation of MOSFET is similar to a Bipolar Junction Transistor (BJT), hence one can relate g_m to I_d as following [4, 37]:

$$g_m = \frac{I_d}{nV_T} \tag{2.15}$$

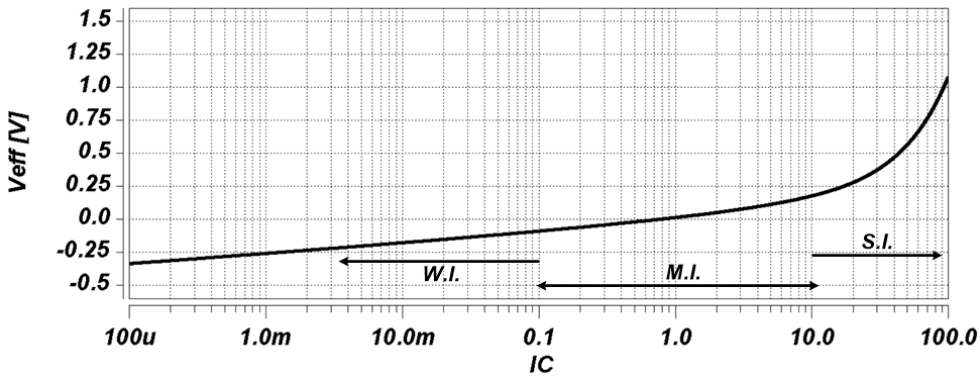

Figure 2.6 Extracted V_{eff} vs. I_C

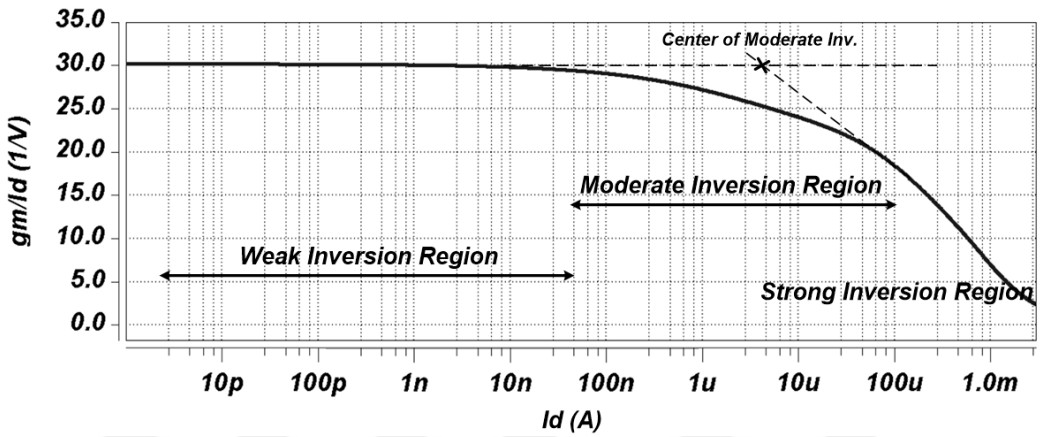

Figure 2.7 g_m/I_d vs. I_d graph. Demonstrating the operation regions of a MOSFET.

2.2.2 Input transistor sizing

In the detector front-end design, the noise performance of a readout system is usually expressed as the equivalent noise charge (ENC). The equivalent noise charge ENC is defined as the ratio of the total integrated root-mean-square (rms) noise at the output of the pulse shaper to the signal amplitude due to one electron charge q. Obviously, the ENC depends on the characteristics of both the charge sensitive amplifier and the pulse shaper. It has been concluded that the optimum choice of pulse shaper depends strongly on applications, and for a given application one must assess the trade-offs among different design parameters [12].

In principle, either the time-domain or frequency domain approach can be used to calculate the ENC of a detector readout system [38, 39, 40]. While the analysis in the frequency domain is much more easier and common to most engineers, the time-domain approach is more helpful for comparison of the signal-to-noise ratio performances between different pulse processing units [14]. Nevertheless, the time-domain approach has thus far been limited to the treatment of the thermal and shot noise. The flicker noise can not be dealt with by this time domain analysis.

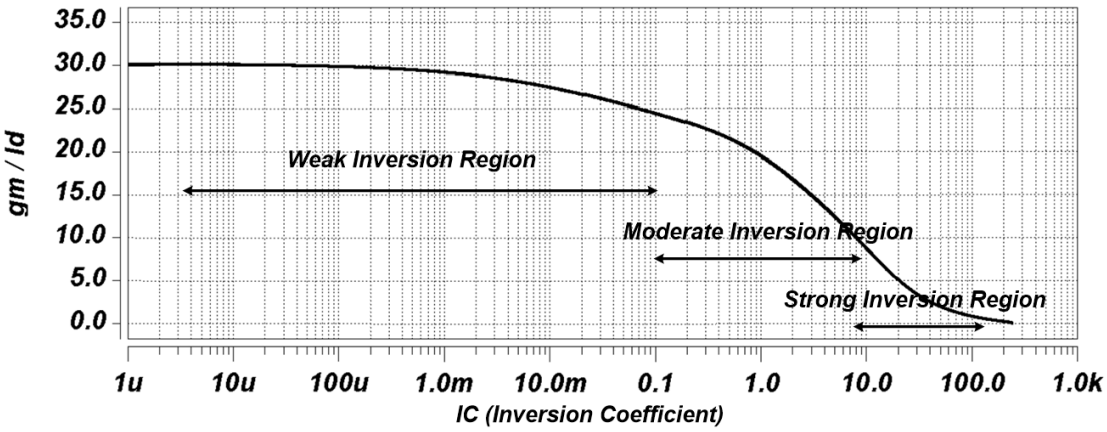

Figure 2.8 g_m/I_d vs. I_C graph. Demonstrating the operation regions of a MOSFET.

As CMOS technologies have inherently much higher l/f noise, the frequency domain analysis must be utilized in order to study the effect of l/f noise.

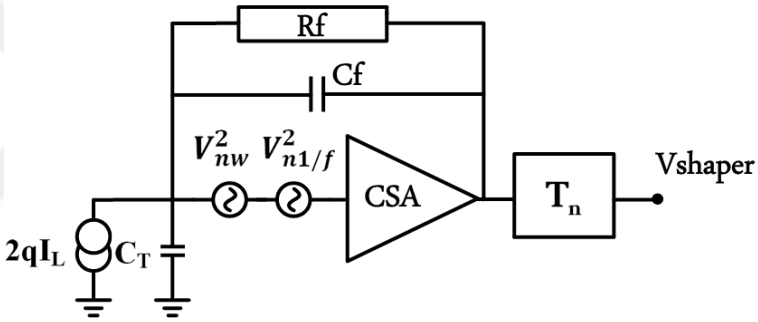

Figure 2.9 Simplified noise sources in detector front-end system.

The noise of a detector readout front end can always be represented by an equivalent input voltage noise generator and an equivalent input current noise generator, as shown in Fig, 2.9, C_T represents the total capacitance at the input of the readout system. With the generally accepted assumption that the total system noise is dominated by the input device of the CSA, the two equivalent input noise sources are given by:

$$v_{eq}^2 = v_{nw}^2 + v_{n1/f}^2 \tag{2.16}$$

where v_{nw}^2 is the gate-referred voltage thermal noise and $v_{n1/f}^2$ corresponds to gate-referred voltage flicker (1/f) noise. Substituting these terms from Equations (2.1)

and (2.3), we have:

$$v_{eq}^2 = \frac{4K_BT\gamma}{g_m} + \frac{K_f}{WLC_{ox}^2 f^{EF}} \tag{2.17}$$

In addition to the amplifier noise, the detector leakage current and its associated bias network give rise to another noise component, which is the shot noise due to detector dark or leakage current. It is generally expressed as:

$$i_{shot}^2 = 2qI_L \tag{2.18}$$

From the expressions (2.18), (2.19), and (2.20), the total noise power spectrum at the output of the charge sensitive amplifier is calculated to be:

$$v_o^2(s) = [\frac{C_g + C_{fb}}{C_{fb}}^2]v_{eq}^2 + [\frac{1}{sC_{fb}}]^2 i_{shot}^2 \tag{2.19}$$

The first term is due to the amplifier noise and the second is the contribution of the detector leakage current and its associated bias network. In order to calculate the ENC the total integrated rms noise at the output of the pulse shaper must be calculated. The transfer function of a semi-Gaussian pulse shaper consisting of one RC differentiator and n integrators (see Figure 2.9) is given by:

$$T_n = [\frac{s\tau_s}{1+s\tau_s}][\frac{A}{1+s\tau_s}]^n \tag{2.20}$$

where τ_0, is the time constant of the differentiator (High Pass Filter) and integrators (Low Pass Filter), and A is the dc gain of the integrators. The number n corresponds to the order of the S-G filter.
The total integrated rms noise in frequency domain can be written as:

$$v_{t\,ot}^2 = \int_0^\infty [v_o(2\pi jf)]^2 [T_n(2\pi jf)]^2 \, df \tag{2.21}$$

Now, since the frequency response of the overall system is determined, one can simply calculate the ENC. And for that, signal amplitude at the S-G filter's output due to one electron charge must be calculated as well. Further discussion on how signal amplitude can be calculated can be found in [14].
As the total noise power spectrum , includes three independent noise terms, which are the channel thermal noise, l/f noise, and the shot noise, it is more convenient to analyze each individual term, separately.

- **ENC due to Thermal Noise:**

$$ENC_{th}^2 = \frac{4K_BTn\gamma}{g_m}\frac{(C_g+C_{det})^2B_i}{4\pi\tau_s q^2} \tag{2.22}$$

where B_i is S-G filter coefficient and will be discussed in the chapter 4 together with shaper characteristics.

- **ENC due to Flicker Noise:**

$$ENC_f^2 = \frac{K_f}{WLC_{ox}^2}\frac{(C_g+C_{det})^2}{q^2}A_i \tag{2.23}$$

where A_i is S-G filter coefficient.

- **ENC due to Shot Noise:**

$$ENC_{shot}^2 = 2qI_{dark}\frac{\tau_s B_j}{4\pi q^2} \tag{2.24}$$

where B_j is S-G filter coefficient.

The total equivalent noise charge ENC, is simply given by the sum of the ENC's due to three individual noise sources given in Equations (2.22-2.24) as:

$$ENC_{tot} = \sqrt{ENC_{th}^2 + ENC_f^2 + ENC_{shot}^2} \tag{2.25}$$

Combining equation (2.5) with the expression (2.22) for the ENC, due to the channel thermal noise, one can understand that in order to minimize the ENC,, the minimal transistor gate length L and the maximal dc bias level, must be chosen. The transistor gate width W has a more severe effect. On the one hand, the increase in the gate width reduces the transistor channel thermal noise due to the increase in the transistor transconductance g_m. On the other hand, the increase in the gate width impairs the signal-to-noise ratio performance due to the increment in the input capacitance. As a result, an optimal gate width must exist for which the ENC, is minimal. It is calculated by solving the equation of the derivative of equation (2.22) with respect to the gate width W. It is given by:

$$W_{opt} = \frac{C_{det}+C_{fb}}{2\alpha C_{ox}L} \tag{2.26}$$

where α is defined as $\alpha L = L + 3L_D$, which is very close to unity for long channel devices. In order to minimize this value, a transistor with a minimal channel L must

be chosen and a high DC bias current must be used. Also, the parasitic capacitances and feedback capacitance should be kept at minimum, in spite of the fact that they are noiseless components.
On the other hand, for flicker noise minimization we should have:

$$(WL)_{opt} = \frac{3(C_{det} + C_{fb})}{2\alpha C_{ox}} \tag{2.27}$$

The existence of the optimal gate area rather than gate width stems from the fact that the l/f noise source depends on WL and is independent of W / L ratio [12], [13]. It means that as far as ENC, is concerned, either W or L may be chosen freely to meet the noise matching condition in Equation (2.27). However, taking into account the ENC_{th} due to the channel thermal noise and requirements related to the Gain Bandwidth Product (GBP) and the response speed, etc., a minimal transistor gate length should be chosen.
In the scope of this work, we will analyze flicker, thermal and parallel noise contributions separately as expressed in Equations (2.22-2.24). Investigating these expressions, it is observed that large value of WL and low values of γ/g_m correspond to minimization of flicker and thermal noises; respectively. This is interesting since in case of a fixed current for the MOS, if we increase W by keeping L constant, we are pushing the transistor into weak inversion with corresponds to high values of γ/g_m. This means that for a fixed current there is an optimum W where flicker and thermal noise contributions are equal. In order to determine the optimum W, a SPICE simulation was performed implementing the above expressions directly into the SPICE netlist. This simulation was based on BSIM3v3 model of Austria-MicroSystems CMOS library in HSpice software of Synopsys. Figure 2.10 shows the simulation results in determining the optimum peaking time for a bias current of 20μA, I_{dark} = 10nA, C_{det} = 12pF and ENC constraint of less than 250 $erms$. As this was assumed to be the worst condition for the available detector.
Table 2.1 lists the input transistor size and characteristics. Note that we have not used the device minimum feature size although it sis suggested by the theoretical analysis. This is to avoid short-channel effects such as velocity saturation or significant variations in mobility of the MOSFET.

Table 2.1 Characteristics of the Input Device

Device	Width: Length ($\mu m : \mu m$)	$I_{DS}(\mu A)$	$V_{DSsat}(V)$
PMOS	615:0.8	20	0.2

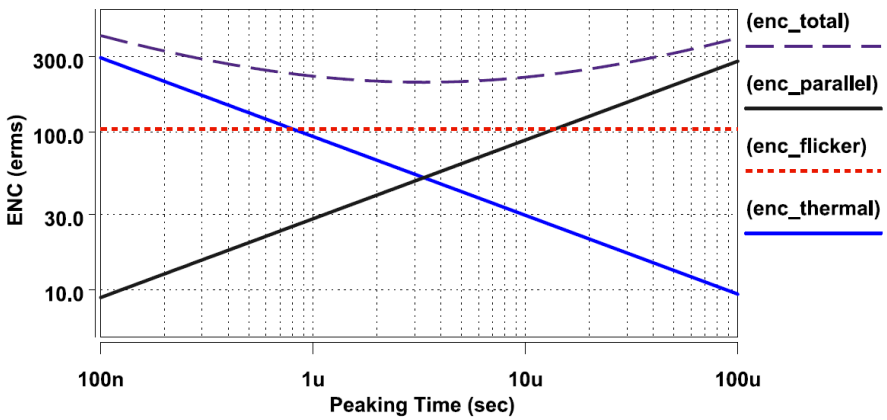

Figure 2.10 Effect of peaking time resulting in noise minimization in 3.8μsec..

3. Design of Charge Sensitive Amplifier (CSA)

CSA is one of the most significant blocks of a SSD readout front-end electronics. Throughout this chapter, design, analysis and simulation results of the proposed CSA of this work will be discussed in detail. We begin with CSA's critical role in a front-end system, then CSA operation principle and its transistor-level device sizing are presented. In general, designers are interested in the noise minimization of a CSA toghter with its high voltage-to-voltage gain, since it is the first block of the front-end system which concentrates on amplifying a very small input signal with the lowest possible baseline noise. Requirements for proper operation of the front-end system in terms of frequency-response i.e. bandwidth, stable DC biasing, power consumption, and low-noise performance must be met by the architecture of the CSA. Modern CSA designs focus on low-power and low-noise principles which is obtained at the beginning, by the optimization and proper sizing of the input transistor and afterwards other remaining transistors together with the bias network. Recently, challenges in CMOS readout front-end systems has been updated with implementation of large feedback resistors required in the reset-network. Finally, performance of the CSA is provided at the end of this chapter.
Charge integration of the transient signals coming from the detector is one the main purposes of the CSA in the readout chain. These charge pulses from the SSD are converted to voltage pulses at the output of the CSA. Which is done by integrating the charge over a feedback capacitor of the CSA, and after that other signal-conditioning operations such as filtering, and amplification are applied. In addition to integration of charge by the CSA, proper CSA design can easily lead to noise suppression of the overall readout circuit since CSA operates as the first block of the readout electronics to the outside environment.

In Chapter 1, the output of the SSD was discussed to be a weak charge pulse with a short pulse width that is in most applications of hard x-ray spectroscopy within the range of $50-300ns$ for CdZnTe detectors. The CSA is designed to have a high input impedance to match the detector's output impedance. On the other hand,

since output of the CSA provides a voltage type signal, it is preferred to have a low impedance in order to fulfill impedance-matching with the following stages of the front-end chain.

Optimization of the CSA and device sizing is required for the required specifications of the system. The optimization constraint might differ significantly referring to the requirements. References [7, 8, 10, 12, 13], focus on the optimization of CSA for low-nise performance. Both frequency and time domain approaches are extensively discussed.

3.1 Principles of CSA in a Readout Front-End System

Figure 3.1 demonstrates the fundamentals of CSA operation. The radiation detector is hit by the incoming photons, this results in generation of eh pairs and due to the electric field bulit up by the detector biasing, the generated charges form signal charges at the output of the detector whose amplitude is proportional to the particle energy. Due to the inverting configuration of the CSA internal circuitry, once the input node of the amplifier decreases, a voltage with opposite polarity is generated at the output of the CSA. Since the amplifier possesses a very high open-loop gain, the output node potential through feedback loop pushes the input node to be zero [4]. All of the charge pulses are integrated on the feedback capacitor with output as a step voltage pulses.

v_{out} has to be reset-ed and restored to the baseline to prepare the system for the next coming event. In case, the CSA is not reset-ed, just like the first event, the next event will produce voltage at the output of the CSa similar to the previous one. However, since the system is not prepared to host another event, this signal will be superimposed on the previous one and eventually cause the CSA to reach its extreme of its headroom value, taking the CSA into saturation. Hence, a device showing resistive behaviour is necessary to discharge the feedback capacitor and preapre the system for the next event. This is done with the feedback resistance . Due to the feedback resistance connected in parallel to the feedback capacitance , the output voltage pulse slowly discharge with time constant $\tau = R_f C_f$. The

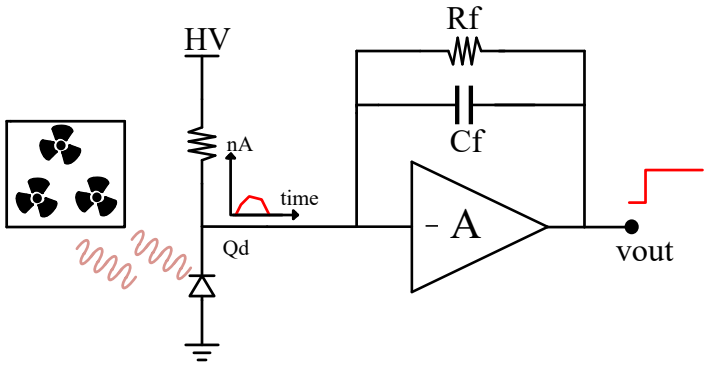

Figure 3.1 Simplified block diagram of a CSA interface to the Radiation Detector.

generated charge signal is given by the following equation using Laplace transform over a time interval $t = 0$ to t_0.

$$Q_d(s) = Q_d\left(\frac{1}{s} - \frac{e^{-st0}}{s}\right) \tag{3.1}$$

The transfer function can be written as:

$$T(s) = -\frac{1}{C_f}\frac{\tau}{1+s\tau} \tag{3.2}$$

Thereby, the output voltage can be expressed as:

$$V_{out}(S) = -\frac{Q_d}{C_f}\left(\frac{1}{s} - \frac{e^{-st_0}}{s}\right)\frac{\tau}{1+s\tau} \tag{3.3}$$

Analyzing Equation (3.3) in time domain, results in output voltage equation as below:

$$v_{out}(t) = -\frac{Q_d}{C_f}\frac{1-e^{-\frac{t}{\tau}}}{\frac{t_0}{\tau}} \tag{3.4}$$

Investigation Equation (3.4), one can conclude that, if $t_0 << \tau$ Equation (3.4) can be approximated by:

$$v_{out}(t) = -\frac{Q_d}{C_f}e^{-\frac{t}{\tau}} \tag{3.5}$$

Thereby, throughout the CSA block, the signal charge pulses Q_d are converted to damping voltage pulses with a peak value of $-\frac{Q_d}{C_f}$ and a time-constant of $\tau = R_f C_f$ for the damping.

3.1.1 Open-loop Gain of a CSA

Open-loop gain of the CSa is discussed in this section. It is worthwhile to mention that an ideal case of a CSa would have infinite gain and bandwidth. However, in practice one can refer Figure 3.2. as equivalent circuit of a CSA, being connected to the detector. The input impedance can be written as:

$$Z_{in} = \frac{\frac{1}{sC_f}}{1 + A_o} \tag{3.6}$$

where A_o is the open-loop gain of the internal amplifier in Figure 3.2. For a given charge of Q_d as the input to the CSA, v_{in} can be written as:

$$v_{in} = \frac{Q_d}{(1 + A_o)sC_f + sC_{det}} \tag{3.7}$$

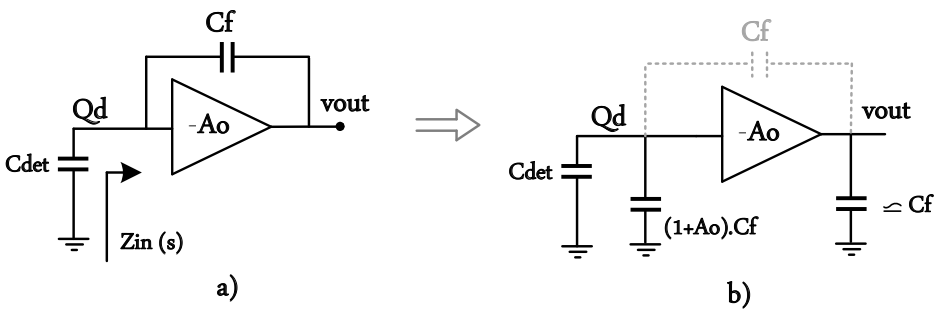

Figure 3.2 a) CSA electrical model with its feedback capacitor when connected to a solid-state detector. b) Application of Miller theorem to the feedback capacitor.

Note that Equation (3.7) is obtained by assuming that:

$$Q = C.V \tag{3.8}$$

And from Equation (3.8), we have:

$$v_{in} = \frac{Q_d}{C_{tot}} \tag{3.9}$$

Where C_{tot} is the total capacitance (Impedance) at the input node and is equal to:

$$C_{tot} = C_d + (1+A)C_f \tag{3.10}$$

The latter term in Equation (3.10) is achieved by using the well-known Miller convention from basic circuit theory.

The output voltage which is equal to $v_{out} = A.v_{in}$ can be expressed as below:

$$v_{out} = \frac{A.Q_d}{sC_d + (1+A)sC_f} \tag{3.11}$$

Since Gain (Sensitivity) is equal to:

$$Sensitivity = \frac{v_{out}}{Q_d} \tag{3.12}$$

From Equations (3.11) and (3.12) and by taking a factor of C_f in the denominator, we have:

$$Sensitivity = \frac{1}{C_f} \cdot \frac{1}{1 + \frac{C_{det}+C_f}{AC_f}} \tag{3.13}$$

From Equation (3.13), one can simply conclude that the ideal case for the sensitivity of a CSA, is achieved once $AC_f >> C_{det} + C_f$. Which means that open-loop gain of the CSA must be as high as possible considering the bandwidth constraint and leads to the well-known formula of:

$$Sensitivity = \frac{1}{C_f} \tag{3.14}$$

3.1.2 Folded-Cascode Amplifier Architecture

Figure 3.3 shows transistor-level schematics of the CSA used in this work. As discussed in Chapter 2, a PMOS device (M_1) is selected as input device due to its low flicker noise coefficient (K_f) compared to an NMOS device in $0.35\mu m$ CMOS technology of AMS.

The core amplifier consists of transistors M_1, M_2, and M_{15}. The first transistors together with their associated current sources build the folded-cascode architecture. M_{15} is used as a voltage-buffer to reduce the loading-effect of the next stages and

also provide adequate headroom for the output voltage swing [41, 42].
Multiple current mirror and current source structures were implemented to meet the design constraints in terms of noise, power consumption and dynamic range (voltage swing headroom). Transistors $M_7 - M_{13}$, $M_3 - M_6$ and $M_{16} - M_{20}$ provide biasing for the folded-cascode transistors (M_1,M_2) and the buffer (M_{15}).
M3 being a non-input device contributes low drain-referred noise since it is source degenerated by M5 (in triode). The CSA block only consumes 260 μwatts of power and has dual supply operation where V_{DD} and V_{SS} are $3.3V$ and $0.0V$, respectively. Moreover, due to direct-coupling (DC) to the detector, a common-mode voltage is required to bias the first input device (M_1) such that its DC gate voltage stands on *zero* volts (DC). TABLE 3.1 lists the aspect-ratios of the critical transistors.

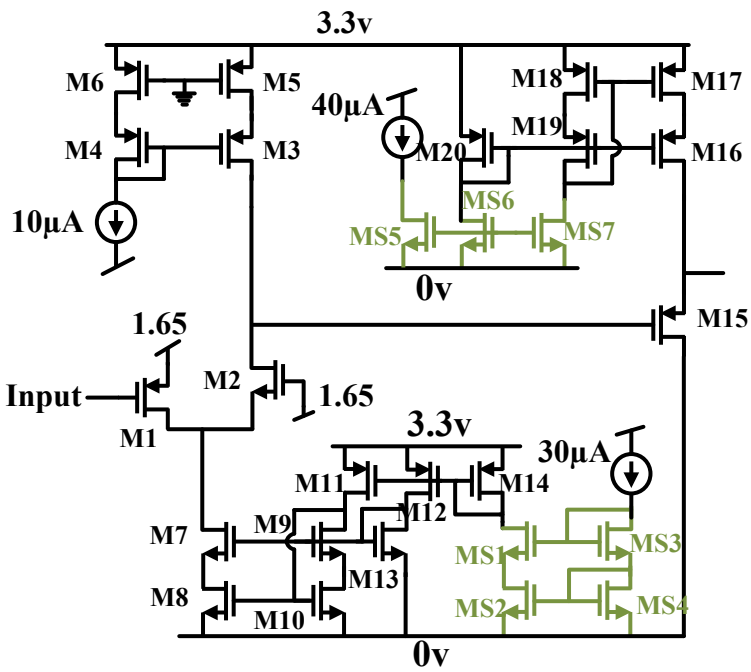

Figure 3.3 Transistor-level circuit schematics of the CSA.

Table 3.1 DEVICE SIZES OF THE CSA

M1	700:0.8
M2	405:1.3
M3-M4	21:2
M5-M6	2:0.5
M7-M8	130:10
M9	456:0.7

All the dimensions are in μm .

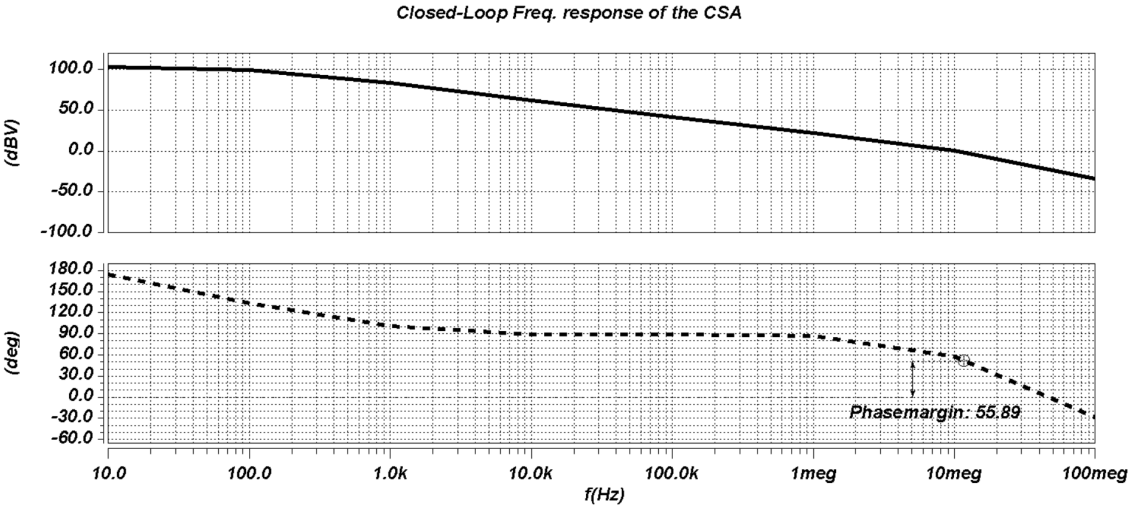

Figure 3.4 Closed-Loop frequency response of the CSA.

Figure 3.4 shows the frequency-response of the CSA with the presence of capacitive feedback. The achieved phase-margin is approximately 55 degrees, which is suitable for most of the general purpose spectroscopy and medical imaging applications.

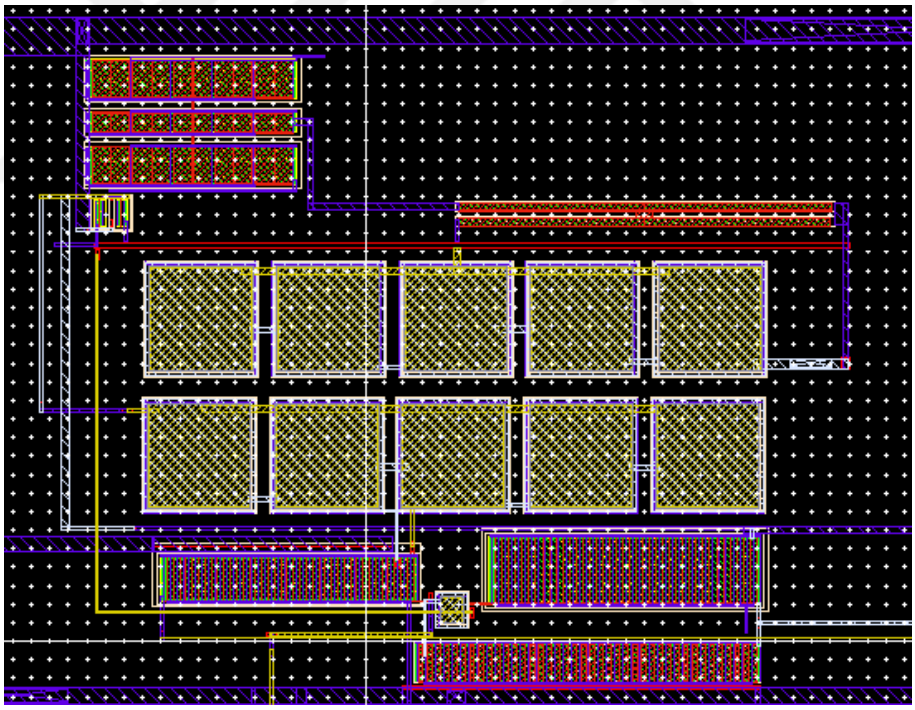

Figure 3.5 Layout of the proposed CSA.

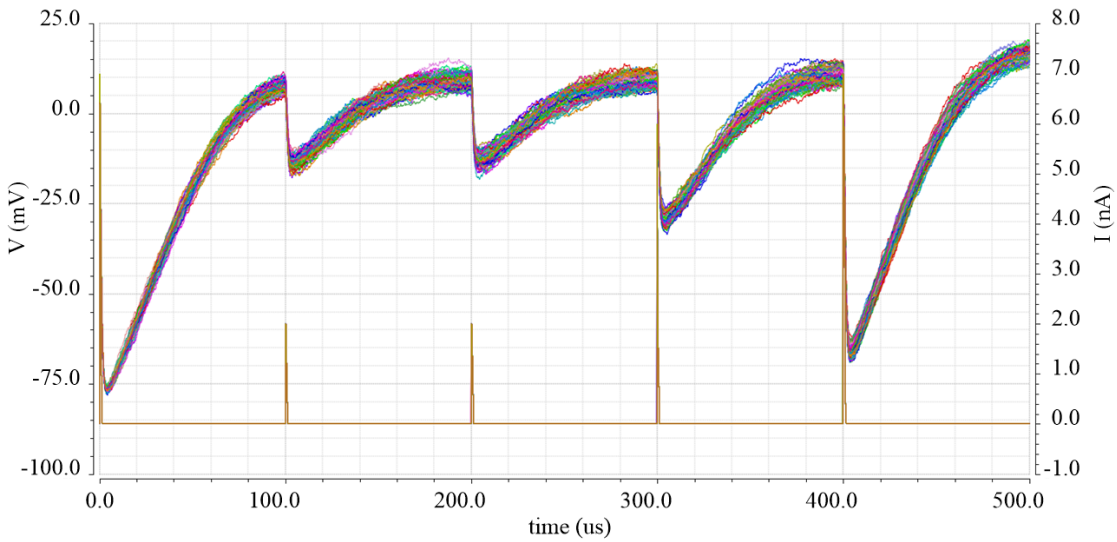

Figure 3.6 100 runs of transient noise simulation for CSA. Input is a summation of multiple current pulses with a minimum arrival time of 100 μs.

4. Design of Programmable Reset-Network and Semi-Gaussian Shaper

4.1 Overview of the conventional low-frequency feedback Reset-Network

Figure 4.1 shows the circuit topology of the well-known low-frequency feedback reset network introduced in 1980s [11]. The circuit allows to compensate for the dark current already in the CSA configuration and thereby no additional block such as a Base Line Holder (BLH) is required.
To understand the operation of the circuit, consider the circuit at equilibrium, where M_{1k}, M_{2k} and M_{3k} all are biased with a current of $I_{krum}/2$. Now, assume a DC current is being injected to v_{in} node. This flow of current into the amplifier input (-A) leads to an amplified voltage but in reverse polarity compared to the input. (Note that the amplifier causes a -180 degree phase shift from input to the output). As v_{out} decreases, gate of transistor M_{2k} decreases and thereby v_{sg} of M_{2k} increases which results in drawing more current from I_{krum} current source and in jargon of electronics, the differential pair made by M_{1k} and M_{2k} is switched such that all of I_{krum} current flows into M_{2k} and M_{1k} enters to cut-off region of operation. Due to the presence of $I_{krum}/2$ source at the bottom, the excess current flows into the C_k capacitor and starts charging it. As C_k charges, it rises v_{sg} of M_{3k} and this transistor starts sinking current from the input node. Thereby, the injected current at the input does not flow into the feedback network and the circuit does not meet saturation or base-line shift due to the dark current. This loop must be slow enough, so that only DC current which represents the Dark current is compensated. Otherwise, there will be a significant baseline shift at the output of the CSA. This mode of operation is known as inductive behaviour of the feedback and the virtual inductor's value can be calculated as:

$$L_f = \frac{2C_k}{g_{m1k,2k} g_{m3k}} \tag{4.1}$$

On fast transient signals, like the transient pulses generated by the radiation detector, the reset network does not react to the variations. Meaning that, the differential pair made by M_{2k} and M_{1k} does not switch and looking from input and output of the CSA, a constant impedance is seen. As evident,C_f is discharged through the drain resistances of M_{2k} and M_{1k} which can be written as:

$$R_f = \frac{2}{g_{m1k,2k}} \tag{4.2}$$

According to [43], one condition must be met to ensure the stability of the feedback loop which is :

$$\frac{C_k}{g_{m3k}} >> 2\frac{C_f}{g_{m1k,2k}} \tag{4.3}$$

Further discussion on Krammenacher low-frequency feedback such as locations of poles and zeros and frequency response can be found in [11, 43].

4.2 Design of Reset-Network

Figure 4.2 shows the proposed reset-network used in this work which is a modified version of reset-network circuit in Figure 4.1. The novelty of the work is based on a programmable current which biases the transistors in the loop i.e. M_{1k}, M_{2k} and M_{3k}. In other words, changing the I_{krum} current results in different values for the R_f and thereby the reset time-constant (τ_f) is changed, making the overall front-end suitable for different count-rates.

The challenge in the design of the proposed reset-network is the required bias current for I_{krum}. Since, as discussed in chapters 1-3, we have chosen

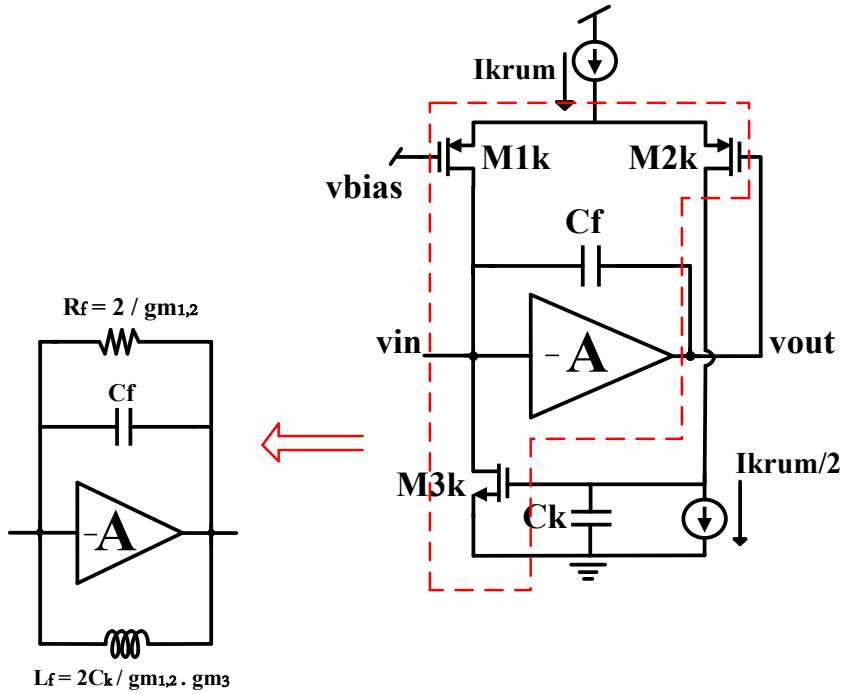

Figure 4.1 Conventional Krummenacher low-frequency feedback and its equivalent small-signal circuit.

$C_f = 60fF$, a proper value of R_f results in resistances in ranges of $0.5 - 10G\Omega$. According to Equation (4.2), $g_{m1k,2k}$ must be as small as possible to establish such a big resistance. Thereby, biasing M_{1k} and M_{2k} with low currents (pico ampere) in weak-inversion results in high values of R_f. Further discussion on the generating such a low current is presented in chapter 5. Table 4.1 lists the device sizes and values used in Figure 4.2.

Table 4.1 DEVICE SIZES OF THE RESET NETWORK

M1k	7:0.7
M2k	7:0.7
M3k	200:0.7
M4k	100:10
M4	2:100
M5	2:100
M6	50:10
M7	50:10
Ck	5 [pF]

All the dimensions of MOSFETs are in um .

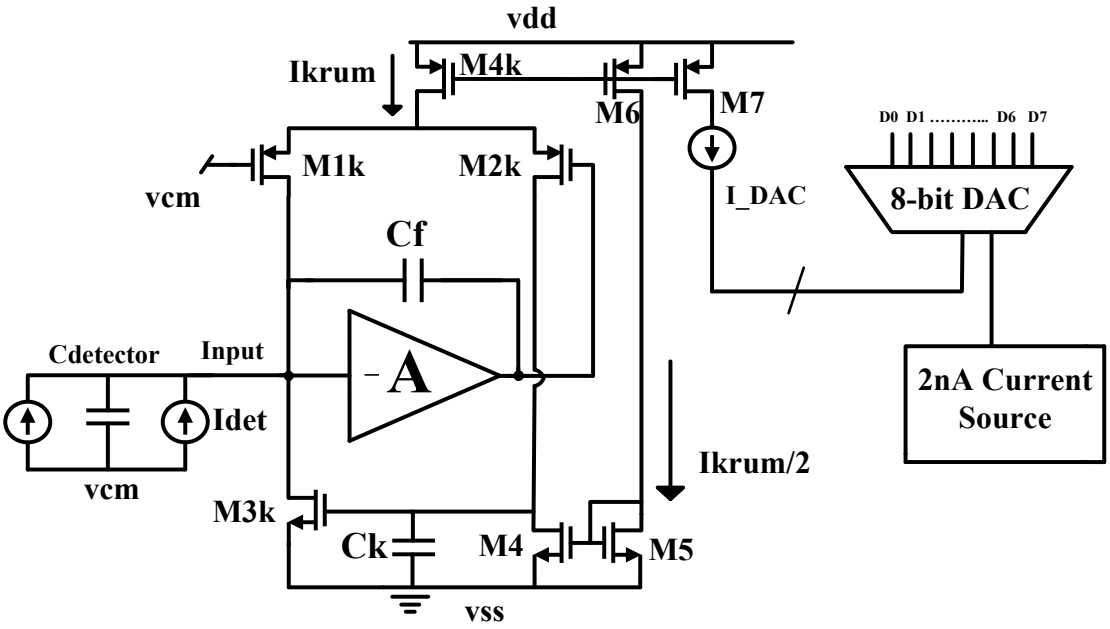

Figure 4.2 Proposed New Reset-Network.

4.3 Design of an 8-bit Digital to Analog Converter (DAC)

Optimization of the proposed readout focuses on this section. An ultra-low power DAC is designed using MOSFET-Only Current Division Technique [44, 45, 46] and the on-chip $2nA$ current source which will be discussed in chapter 5. By proper selection of D0-D7 bits, I_{Krum} is modified to establish the high-value resistance in the feedback loop. All 256 selections of the DAC are feasible using a simple serial-interface to a commercial micro-controller. Lowering the cost of ASIC by eliminating the need for on-chip Analog to Digital Converters.

4.3.1 Current division principle in DAC

Figure 4.3 depicts one slice of a classical resistor-based, R - 2R like ladder which is the fundamental of current division in Digital to Analog Converters [45, 46]. The same functionality can be obtained in a MOSFET-Only implementation as shown in Figure 4.4.

The R part of the classical R-2R ladder is realized by transistor M_2. Trnasistors M_1 and M_3 (or M_4) operates as the $2R$ portion of the resistive counterpart. In case W/L ratio of all transistors are identical, the current I_{in} is divided equally such that one of the currents exits the ladder as I_{thru}, and the other one is switched as I_{out} or I_{dump}. Transistors M_3 and M_4 act as switches (Differential switches), and are not part of the division ladder. Further discussion on the theory and analytical expressions can be found in [44,45].

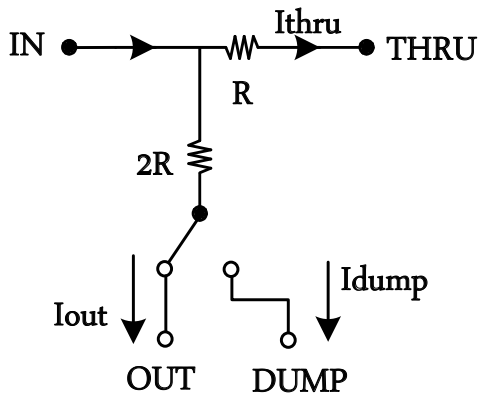

Figure 4.3 R-2R ladder.

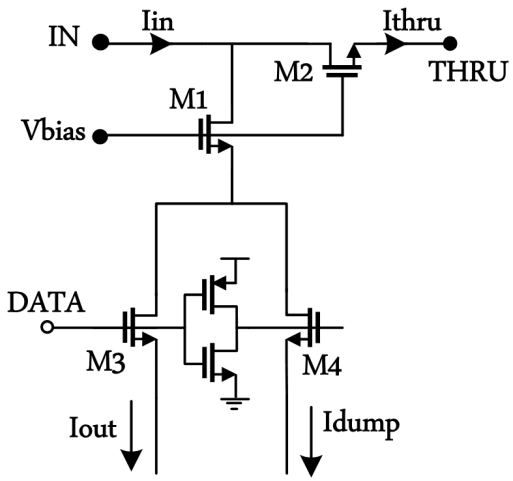

Figure 4.4 MOSFET-Only ladder.

It should be noted that, although the configuration of the MOSFET-Only ladder is similar to the R-2R ladder, the function is not identical in terms of small-signal parameters such as resistances seen between drain and source terminals of the MOSFETs. Especially in our design case, where the $8-bit$ DAC provides the I_{DAC}

current, careful attention must be paid in sizing the transistors in the ladder to avoid loading effects because of the feedback network.

4.3.2 8-bit DAC used in this work

In this work, we have designed an $8-bit$ DAC based on the MOSFET-Only ladder discussed in previous section. The contribution of this DAC to the proposed readout front-end is providing different values for the bias current (I_{DAC}) of the low-frequency feedback network introduced in Section 4.2. Table 4.2 lists the device sizes of the $8-bit$ DAC used in this work and Figure 4.5- 4.6 depict the overall circuit topology and layout of the DAC, respectively.

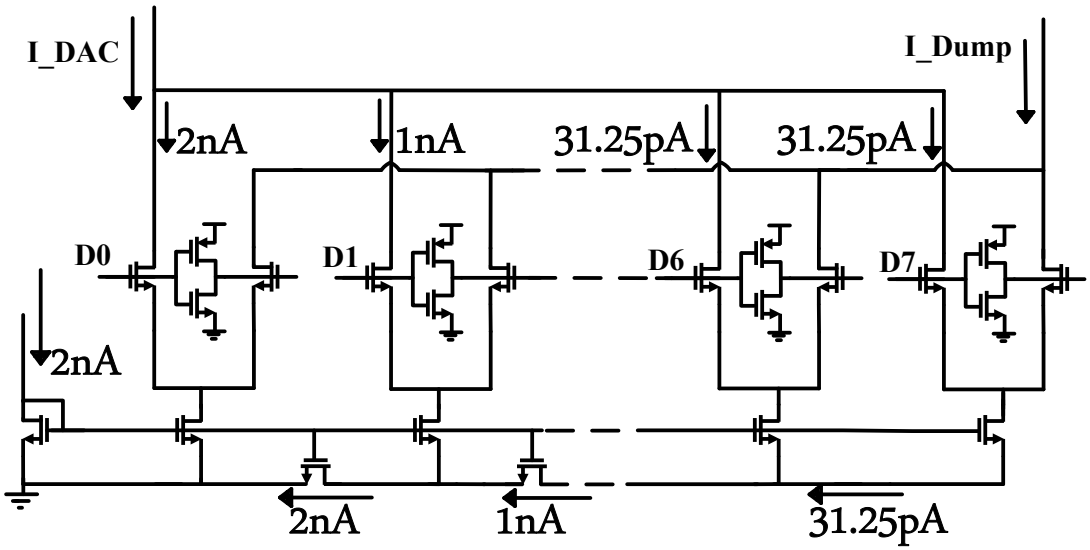

Figure 4.5 Schematics of the 8-bit DAC used in this work.

Figure 4.7-4.8 show the advantage of a programmable reset network. As depicted in Figure 4.7, due to the high count-rate of the incoming signals from the radiation detector, the feedback capacitor (C_f) is not fully discharged after each incoming event.Meaning that, the reset time-constant (τ_f) is big compared to time of arrival of the next event. Hence, CSA's baseline is not restored and once a new event is arrived, CSA's output voltage starts to rise from an initial value. This results in generation of a phenomenon called $PulsePile-up$. The pulse pile-up leads to

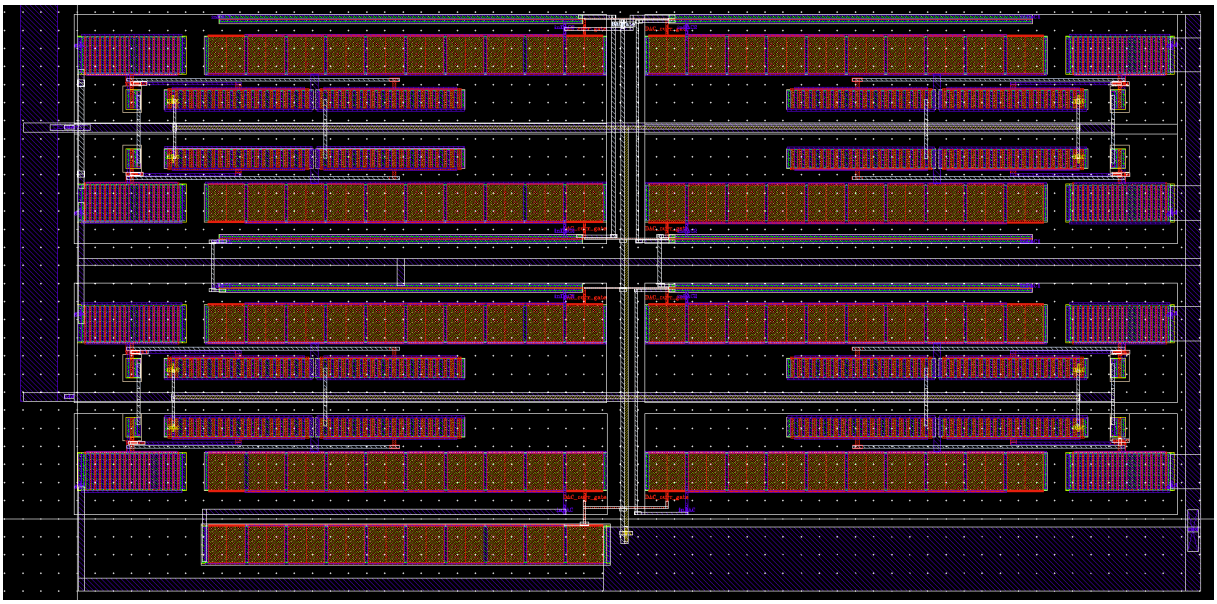

Figure 4.6 Layout of the 8-bit DAC used in this work.

loss of the captured data and dead-time in the readout front-end. Thanks to the programmable reset-network used in this work, once a pile-up happens a new reset time-constant can be established by selecting other bit(s) of the $8-bitDAC$ which results in feeding more current to I_{DAC} and thereby a larger value of $g_{m1k,2k}$ or smaller value of R_f is generated. In other words, reset time-constant can be decreased(increased) by enabling(disabling) $D_0....D_7$ bits of the DAC. Figure 4.8 shows an example of selecting additional DAC bits and eliminating pulse pile-ups for the undesired output shown in Figure 4.7.

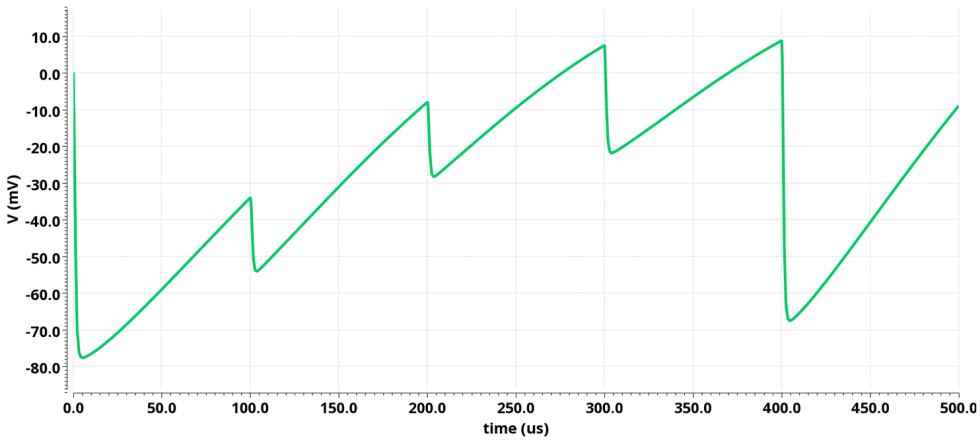

Figure 4.7 Pile-up due to large time-constant of reset network.

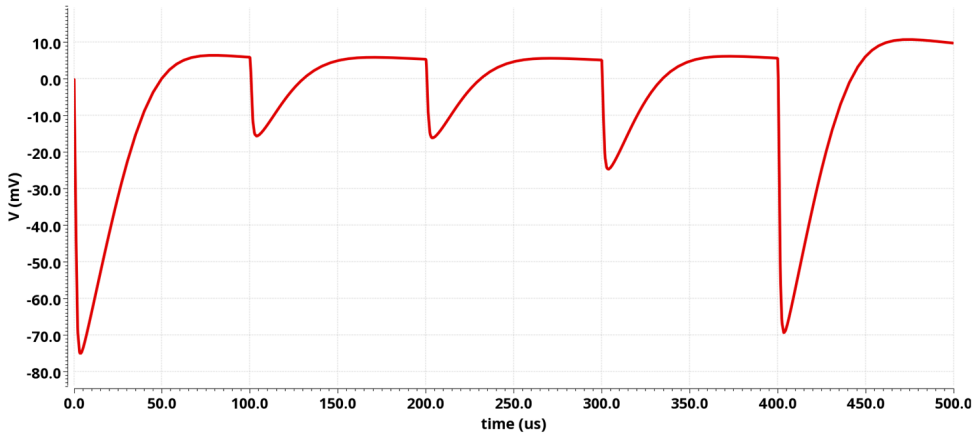

Figure 4.8 Elimination of pile-ups by a proper selection of DAC bits to establish a shorter time-constant.

4.4 Design of Pulse Processing Unit

Semi-Gaussian filters are well-known pulse processing blocks for many readout front-end circuits. They offer a good signal-to-noise ratio and eliminate the excess noise coming from the CSA. In addition to this, these filters prepare the obtained signal for energy measurements and digital signal processing [13, 47]. In this work a fifth-order semi-gaussian filter is designed and simulated for a peaking time of 5μ secs. Value of this optimized peaking time is achieved by optimization method already discussed in chapter 2.

The pulse shaper in this work, consists of a differentiator (High pass filter) followed by five integrators (Low pass filters). Due to possible undershoots generated by the reset time-constant of the CSA, we have chosen an adjustable circuit block consisting of a Pole-Zero Cancellation (PZC) and a CR circuit as the differentiator represeing the first block of the pulse processing unit. On the other hand, five simple active low-pass filters were cascaded to realize the low-pass block of the S-G shaper. Figure 4.9 shows the simplified block diagram of the pulse processing unit used in this work. And device sizes of the pulse processing unit are listed in Table 4.2.

A two-stage amplifier know as Miller compensation opamp is utilized to realize the gain blocks of the active RC filters. The amplifier architecture is shown in Figure 4.10 and is unity gain stable. Table 4.3 lists device sizes of the opamp.Block diagram of gain-stage of the filter used in this work is a simple Miller-compensation opamp. We have implemented a Fifth-order semi-Gaussian filter which is built by cascading five active low-pass filters.

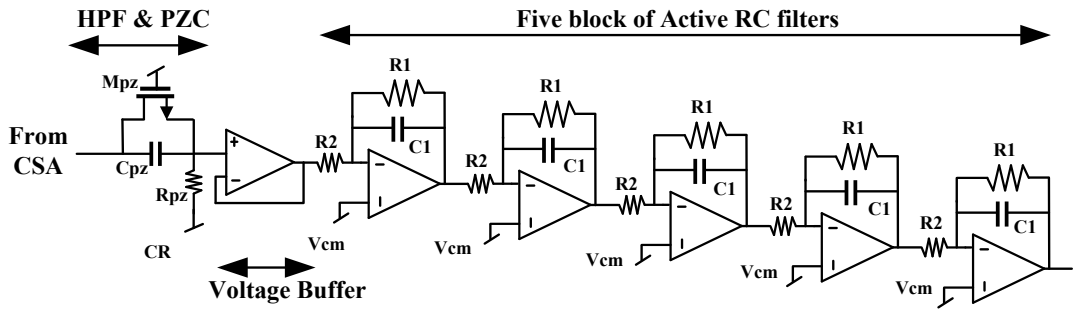

Figure 4.9 Block diagram of the Pulse Processing Unit.

Table 4.2 DEVICE SIZES OF THE PULSE PROCESSING UNIT

M_{pz}	$60\mu m : 1\mu m$
C_{pz}	$20\ pF$
R_{pz}	$50\ K\Omega$
R_1	$200\ K\Omega$
R_2	$100\ K\Omega$
C1	$5\ pF$

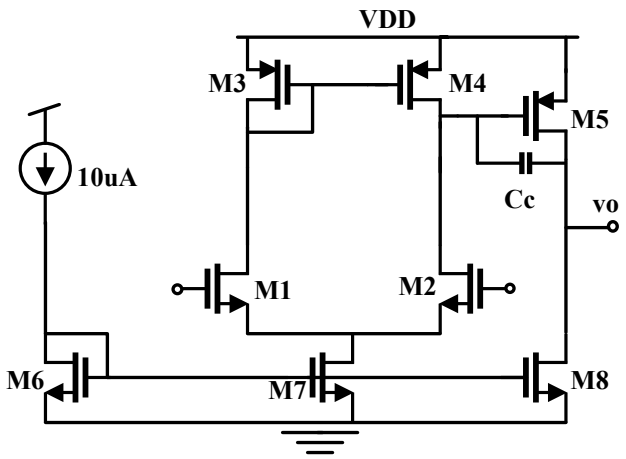

Figure 4.10 Circuit Schematics of the Miller Compensation OpAmp used in Active RC filter.

Output-noise spectral density is depicted in Figure 4.11. Regarding the bandwidth of this application, ENC is calculated to be 98 $erms$.

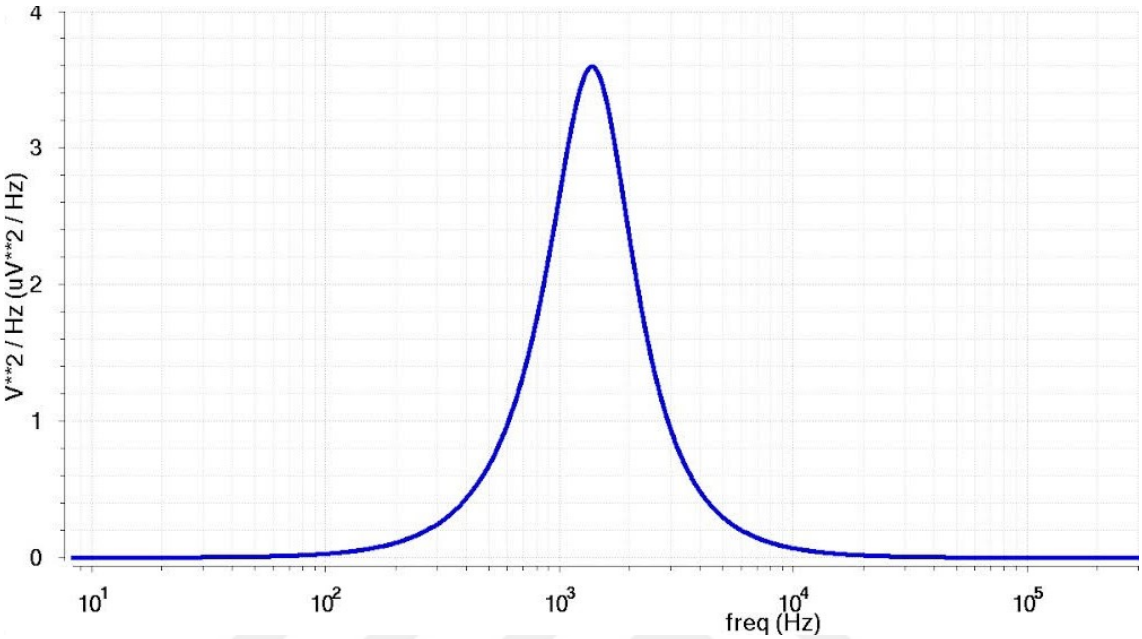

Figure 4.11 Simulated output-noise spectral density .

Table 4.3 DEVICE SIZES OF THE MILLER COMPENSATION OPAMP

M6	20:1
M7	100:1
M8	500:1
M1,2	30:3
M3,4	45:2
M5	430:2
C_c	1 [pF]

All the dimensions of MOSFETs are in um .

4.4.1 Pole-Zero Cancellation Circuit

In signal processing chain for SSDs, decay time of the CSA's output usually introduces an undershoot in the S-G filters output signal. In case another event arrives while the output signal of S-G filter is recovering, the incoming new event will be superimposed on the undershoot and a pile-up would be added to the output. To overcome such a problem, a Pole-Zero Cancellation (PZC) is added to the pulse

processing unit between the CSA and the S-G filter. The following condition must be met for the PZC circuit to properly cancel the pole associated with the decay of the CSA reset network:

$$R_{M_{pz}} C_{pz} = R_f C_f \tag{4.4}$$

Device sizes of PZC circuit are provided in Table 4.3 and Figure 4.12 shows the performance of PZC circuit for different values of V_{pz} which results in optimization of $R_{M_{pz}}$ values to eliminate the undershoot.

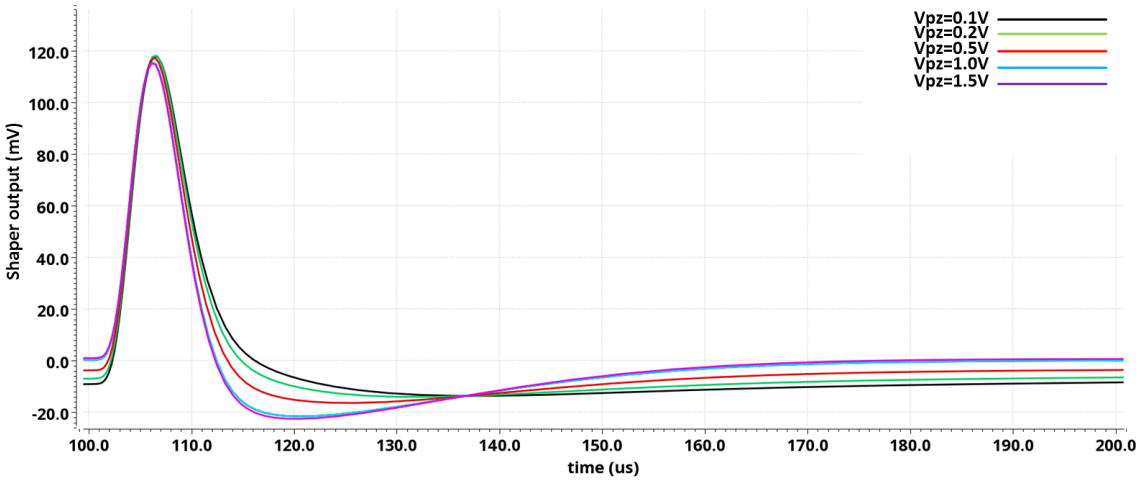

Figure 4.12 Effect of V_{pz} (Control voltage) on Shaper's output.

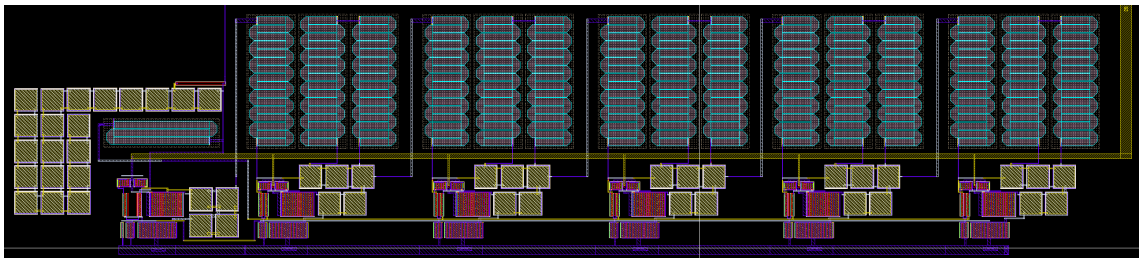

Figure 4.13 Layout of Pulse Processing Unit .

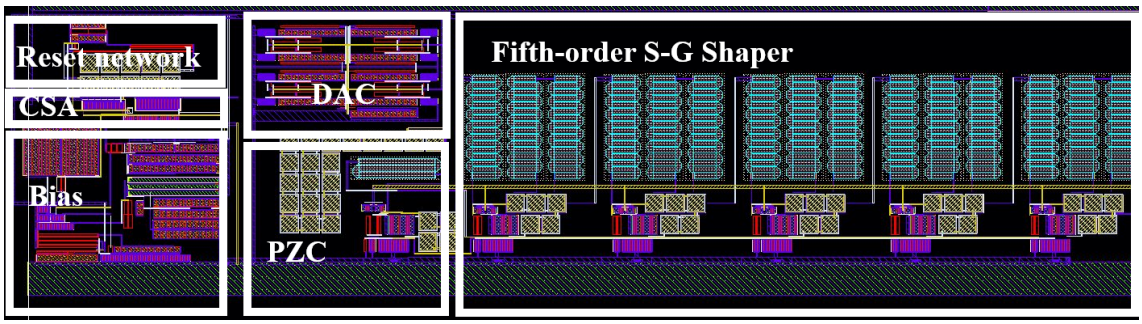

Figure 4.14 Layout of entire ASIC .

4.4.2 Simulation Results

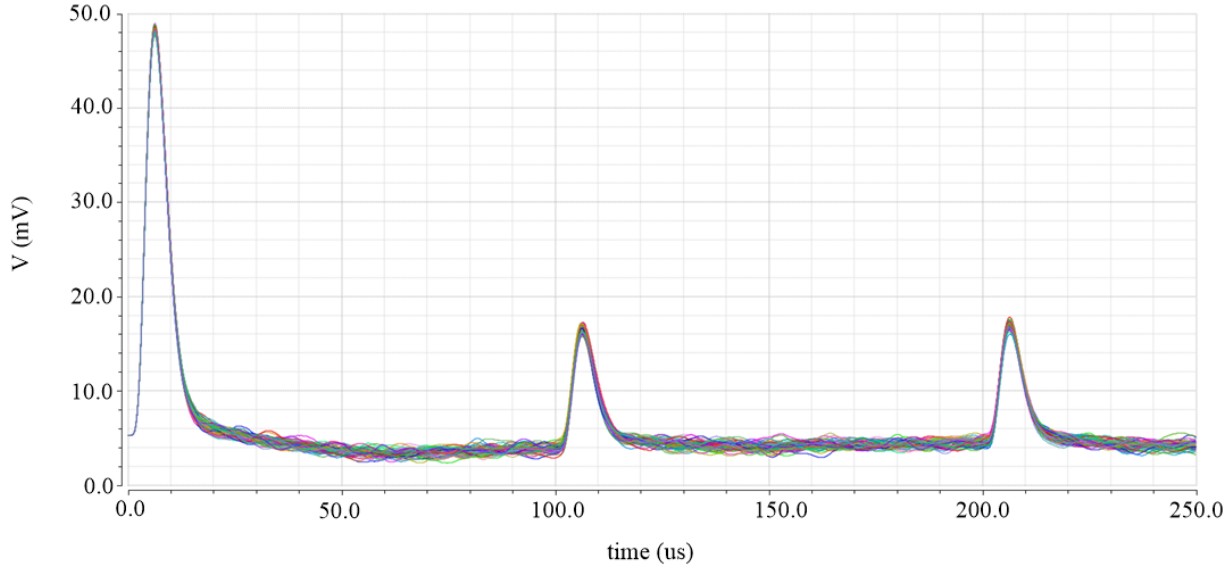

Figure 4.15 Transient-Noise simulation of shaper's output for charge-injections of 1.2 fC and 1.5 fC with an event count-rate of 200'000 counts per second .

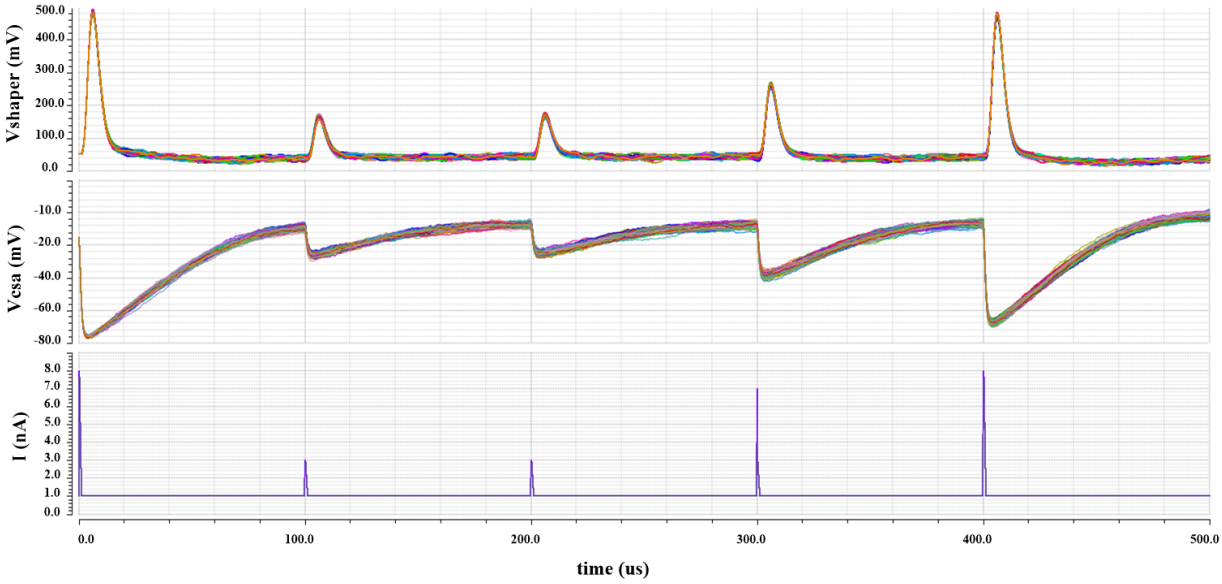

Figure 4.16 input and outputs .

5. Design of nano-ampere resistor-less current source

As discussed in previous chapters, optimization of the proposed readout focuses on design of an ultra-low power DAC powered by an on-chip $2nA$ current source. The current source utilizes β-Multiplier architecture and a self-cascode (SC) pair to establish the necessary current [48, 49, 50]. By proper selection of DAC bits, I_{Krum} is modified to establish the high-value resistance in the feedback loop. 256 selections of the DAC result in feedback resistor values ranging from 600 M to 3 G Ωs, lowering the cost of ASIC by eliminating the need for on-chip Analog to Digital Converters. Reference current ($2nA$) is discussed in this chapter and process corner analysis in four regions in addition to voltage and temperature variations are provided.

5.1 Basics of nano-ampere current source

The basic idea behind nano-ampere current sources is to establish a very large resistor in the core current generator. Figure 5.1 shows the popular configuration of a β -Multiplier for establishing low currents in range of μAs. This circuit is no longer capable of generating ultra-low currents in range of *nano* and *pico* amperes due to the passive element (R) used to establish v_{gs} difference between core transistors [50]. Thereby, designers have been trying to find an alternative solution in realizing the needs for a large value resistor using active elements. Self-Cascode configuration offers a relatively high resistance by deriving M_9 and M_{10} to weak and moderate inversion. This establishes the required V_x value and the required voltage difference between M_1 and M_2, gate-source voltages [49].
Figure 5.2 shows the circuit realization of the nano-ampere current source used in

this work. According to the literature, β -Multiplier circuit has two operating points. One at zero current and the other one at the current of interest. Every circuit offering two operating points, needs a start-up circuit in order to push the loop to start its operation from a point rather than zero. Transistors M_6, M_7 and M_8 form the start-up circuit for this current source. Device sizes of the presented current source are listed in Table 5.1.

In our work, the current source is designed to generate a supply and voltage independent current of $2nA$. Figure 5.3 shows the performance of the presented current source. As evident, there are only a slight variation in current which is due to sizing of transistors and the mismatch between calculations and BSIM 3v3 model.

Additionally, the presented current source is simulated in all of four process corners to ensure the stability of the circuit at worst conditions. Besides, we have run the process corner simulations at multiple V_{DD} values to deeply investigate circuit's behaviour. Figure 5.4-5.7 represent process corner simulation results.

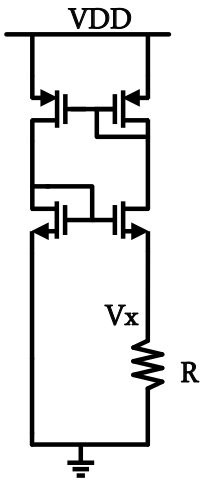

Figure 5.1 Conventional Beta-Multiplier circuit with a passive resistor to generate μ ampere currents .

Table 5.1 DEVICE SIZES OF THE CURRENT REFERENCE

M1	1:100
M2	10:100
M3-M4-M5	2:100
M9	1:9.5
M10	1:50

All the dimensions are in um .

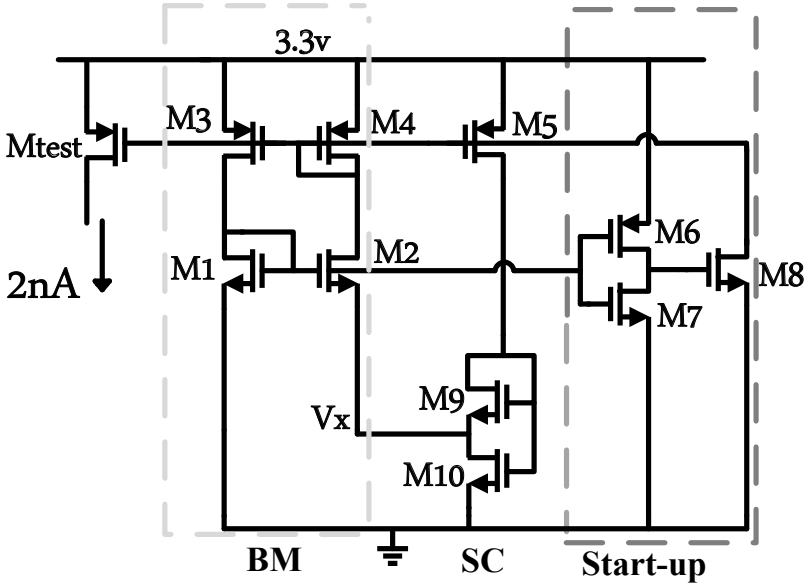

Figure 5.2 Nano-Ampere current source circuit schematics .

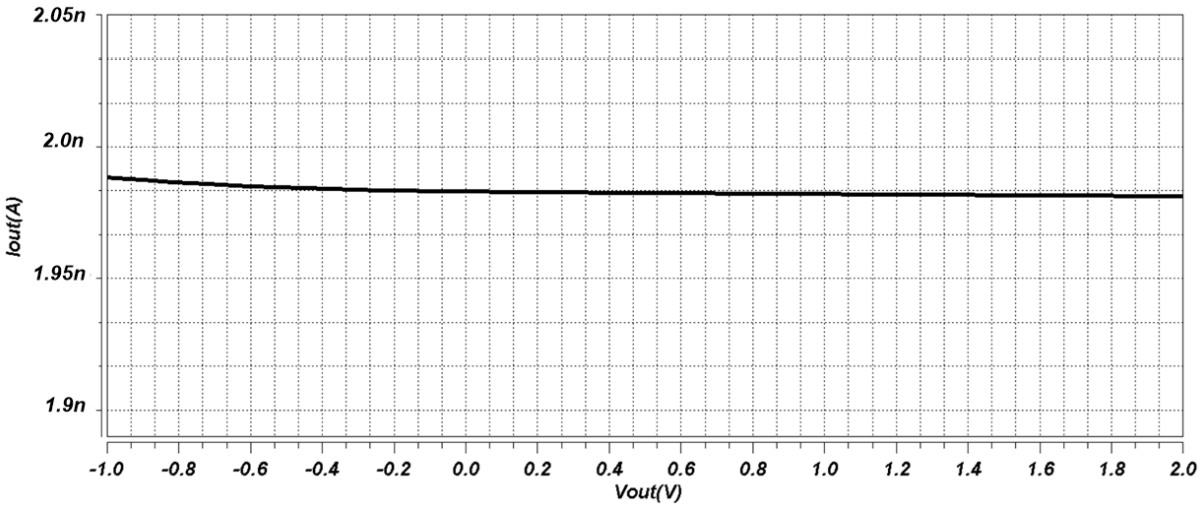

Figure 5.3 Simulated I_{out} current vs. V_{out} variations.

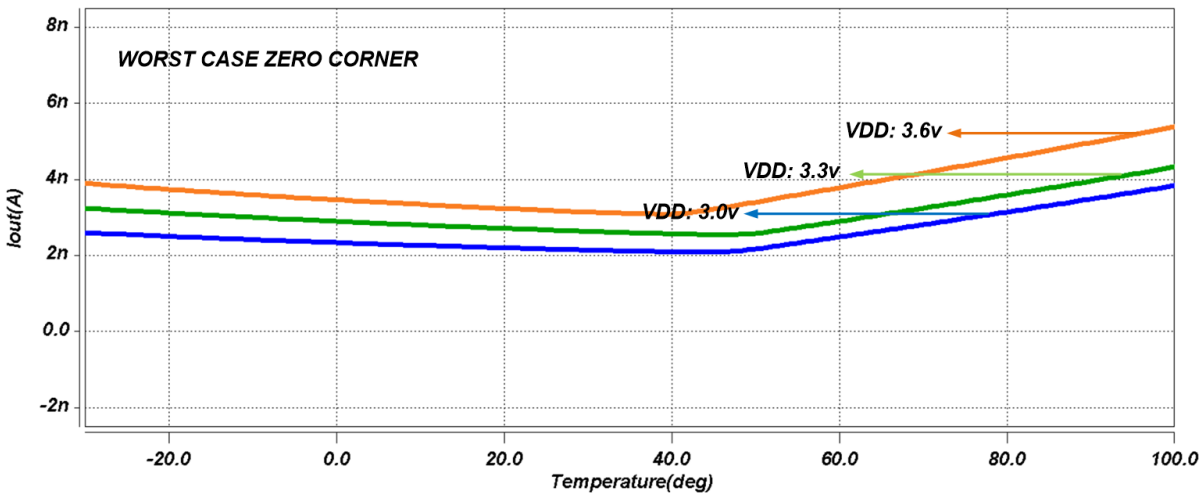

Figure 5.4 Worst Case Zero (WZ): Slow NMOS and Fast PMOS .

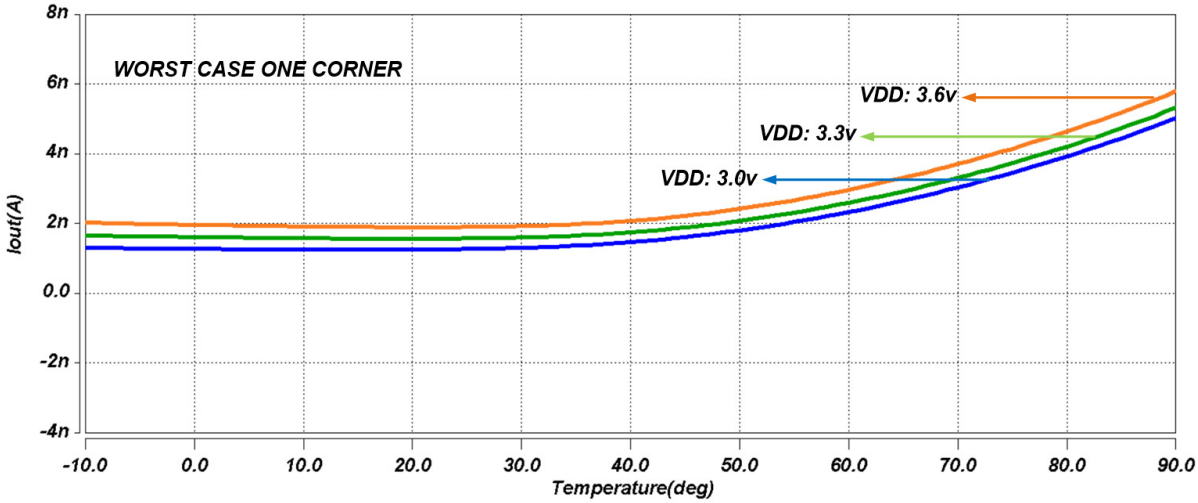

Figure 5.5 Worst Case One (WO): Fast NMOS and Slow PMOS .

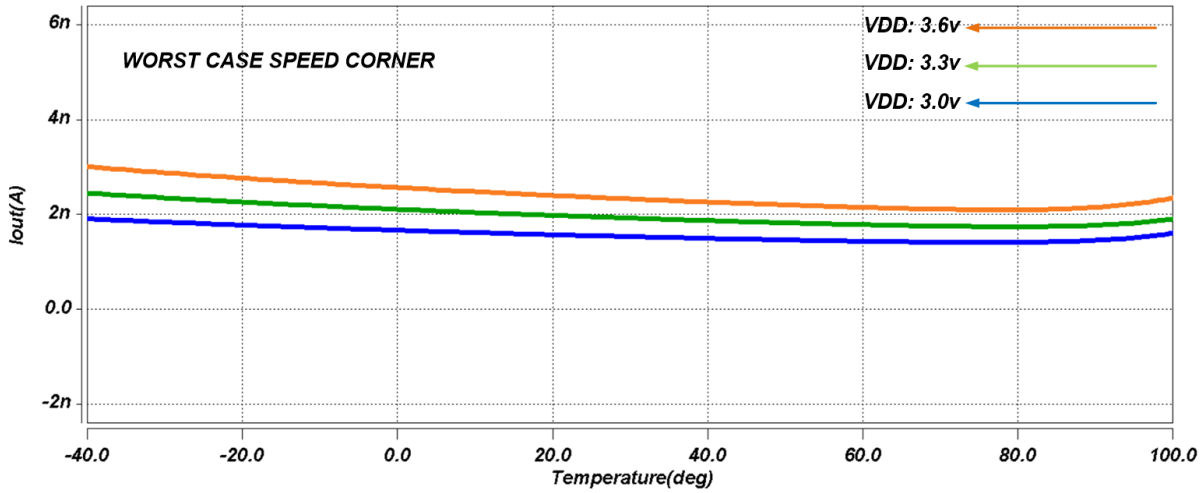

Figure 5.6 Worst Case Speed (WS): Slow NMOS and Slow PMOS .

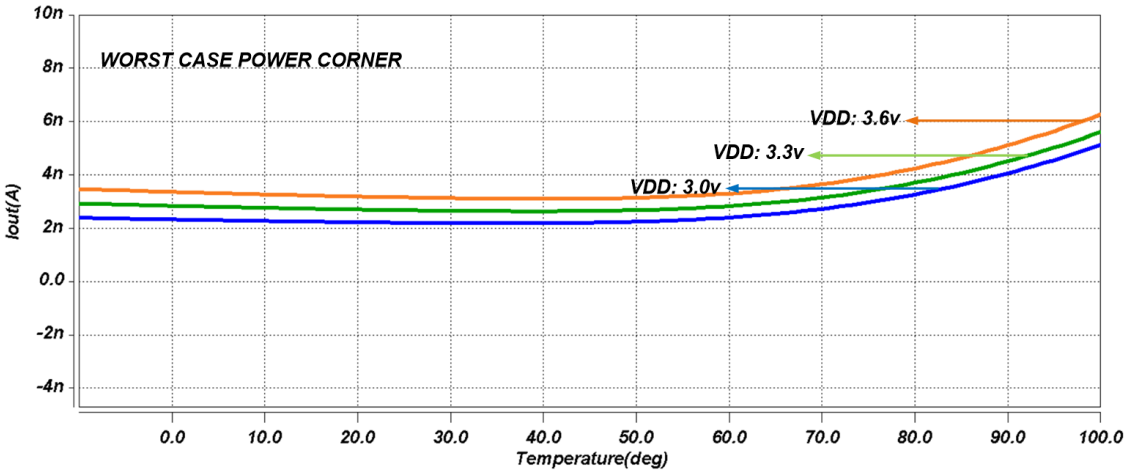

Figure 5.7 Worst Case Power (WP): Fast NMOS and Fast PMOS .

6. Conclusions

6.1 Comparison to previous work

The proposed readout channel is compared to the previous work done in $0.35\mu m$, in terms of power consumption, quality factor, ENC, Sensitivity and peaking time CMOS technology. The proposed readout offers better performance especially in terms of sensitivity, ENC and input capacitor range. As seen in Table 6.1 quality factor of this work is superior to similar work done in $0.35\mu m$ CMOS process technology.

Table 6.1 Performance comparison of this work.

Specification	This work	[20]	[22]	[21]	[23]
Process	0.35μm	0.35μm	0.35μm	0.35μm	0.35μm
C_{det}[pF]	0-12	0-35	6	–	0-5
Peaking time [μs]	5	0.4	1	8	1.5,3,5
Power cons. [mW/channel]	2	2.8	7.8	3	2.8
Sensitivity [mV/fC]	135	55	100	100-300	12.1
ENC [erms]*	98*	2278*	70*	89*	133
QF	1.02	4.7	1.062	–	2.9

*with C_{det} of 0pF .

6.2 Research Summary

This work was focused on the design and analysis of an Application Specific Integrated Circuit for Solid State Detectors. The main aspects of designing a high performance readout system is discussed together with system and device-level requirements and trade-offs between them. Available active reset-networks were briefly overviewed and a modified reset network was introduced.In order to achieve a proper level of performance based on our application, we presented a state-of-art designs of each individual block of the readout. We compared the proposed front-end with previous work in the same process technology and highlighted the drawbacks and advantages of our design.

This thesis presented an optimized low-power, low-noise front-end for CdZnTe detectors. Using the new reset-network mechanism, the readout circuit offers higher sensitivity, lower noise performance and less design complexity. The main advantage of a programmable reset-network was to prevent pulse pile-ups and thereby presenting a readout suitable for a wide range of applications in x-ray spectroscopy and medical imaging.

The ASIC is designed in 0.35- μm CMOS. The CSA block has a power consumption of only 260 μwatts and a chip area less than $0.15mm^2$ and $1.2mm^2$ for the CSA and overall ASIC, respectively. Equivalent Noise Charge (ENC) is calculated to be 98 erms with a detector capacitor of $0pF$ and a feedback capacitor of 60 fF. The readout circuit consumes about 2 mW of power.

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