UNIVERSITY OF CALIFORNIA

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A LOW NOISE ANALOG RADIO BASEBAND WITH NOVEL NOISE SHAPING CIRCUIT TECHNIQUES

A dissertation submitted in partial satisfaction
of the requirements for the degree of

DOCTOR OF PHILOSOPHY

in

ELECTRICAL ENGINEERING

by

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September 2008

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Contents

List of Figures

List of Tables

Abstract

A LOW NOISE ANALOG RADIO BASEBAND WITH NOVEL NOISE SHAPING CIRCUIT TECHNIQUES

by

Ahmet Tekin

This thesis describes the design and realization of an integrated analog baseband receiver for direct conversion radio applications that is flexibly reconfigurable, low noise and requires a small area. Novel aspects of the receiver chain include use of a noise shaped filter based on frequency dependent negative resistors (FDNRs) to reduce blockers, a new configuration of FDNRs to realize a differential filter combined with a dB-linear variable gain amplifier and on chip calibration of both filter frequency characteristics and DC offset cancellation. The novel circuit concepts introduced in this work have been verified by the design and measurement of a 65-nm CMOS test chip. The final baseband chain combining these circuit techniques has resulted in a high performance universal radio baseband operating off of a 1.2 V supply that can be used for multiple applications with signal bandwidths in the range 700 KHz up to 5.2 MHz.

The introduction of digital data communication combined with compression techniques and digital signal processing has fueled the development of numerous wireless standards and applications ranging from cellular, cordless phones and mobile TV to short range Home RF, Wireless LAN and Bluetooth technologies. The high

density of spectral use implied by these standards and frequency allocations implies that very strong interferers must be tolerated while the desired signal in the channel of interest might be very weak. As a result, the classical noise-linearity-power-area tradeoff becomes an even more pronounced challenge in wireless receiver design. Area and power are becoming particularly important in this tradeoff as receivers are desired that are mobile, compact, have long battery life and can support multiple standards.

As CMOS supply voltages decrease, lower noise levels are needed to maintain a comparable dynamic range (DR). Design of low-noise circuits using classical topologies to filter out interferers involves use of large area on-chip capacitors and often are no longer realizable using deep-submicron low-voltage CMOS technologies. To reduce this area when using high cost deep-sub-micron CMOS processes we propose new circuit topologies for various sub-blocks that include innovative noise shaping circuit techniques to enable the transition to a lower supply voltage without incurring the cost of extra area. Here results for a complete baseband receiver and its sub-circuits are compared with and shown to exceed performance previously reported for these circuits based on a number of figures of merit.

Acknowledgements

First, I praise and thank Allah the all mighty who provided me with patience and provisions to complete my PH.D. successfully. I would like to thank all my family members for their tolerance, support, encouragement and patience. It is my honor to acknowledge the support of my advisor Dr. Kenneth Pedrotti. His suggestions and constructive comments proved invaluable. I would like to thank Dr. Holger Schmidt and Dr. Claire Gu for serving in my thesis committee, Dr. Wentai Liu for supporting me in his research lab and all other faculty members at the school of engineering helping me to build my knowledge in the field. Special thanks to Hassan Elwan for all the useful ideas, discussions and help that he provided. I would also like to thank all of school of engineering staff who helped us in all of our daily school issues. Special thanks to Ms. Mullane in this regard.

Finally, I would like to thank my fellow graduate students at UCSC and my colleagues at Newport Media, Inc., for keeping me company during my graduate studies. I appreciate their cooperation, support and suggestions for my work.

To my family

1 Introduction

1.1 A New Life Style: Wireless

Various wireless standards have emerged in recent years as a result of strong consumer demand for wireless applications [1-2]. The introduction of digital data communication with digital signal processing has fueled the development of numerous wireless standards and applications ranging from cellular, cordless phones and mobile TV to short range Home RF, Wireless LAN and Bluetooth technologies.

While abundance of these wireless applications drives the technology to its limits to catch-up with the demand, the crowding of the spectrum poses additional challenges for the designers. These emerging wireless standards have to be compatible with the existing standards. Hence, very strong interferers can coexist in the nearby channels whereas the desired signal in the channel of interest might be very weak. As a result, the classical noise-linearity-power-area tradeoff becomes an even more pronounced challenge in wireless receiver design. Moreover, because of the trend to integrate multiple applications into a single wireless device, the battery life becomes even more significant concern. Hence, any design solution for portable devices should offer low-power operation. Since device size is also of greater concern in such portable devices, the designs should be reconfigurable for different frequency bands and applications to minimize the component count in the final design.

1.2 A Closer Look at the Rapidly Spreading TV Standards

Mobile TV involves bringing TV services to the mobile phones. It combines the services of a mobile phone with television content and represents a logical step both for consumers and operators and content providers. Mobile TV over cellular networks allows viewers to enjoy personalized, interactive TV with content specifically adapted to the mobile medium. The services and viewing experience of mobile TV over cellular networks differs in a variety of ways from traditional TV viewing. In addition to mobility, mobile TV delivers a variety of services including video-on-demand.

Mobile TV is one of the most challenging wireless applications in terms of design requirements and specs for the actual hardware designers. Once more, spread of numerous incompatible mobile TV standards across the globe could not be prevented, as was also the case with 2G and 3G mobile systems. These include digital video broadcasting-handheld (DVB-H), digital multimedia broadcasting (DMB), TDtv (based on TD-CDMA technology), 1seg (based on Japan's integrated services digital broadcasting-terrestrial (ISDB-T)), digital audio broadcasting DAB, and MediaFLO. None is ideal as all have drawbacks of one kind or another: spectral frequencies used or needed, signal strength required, new antennas and towers, network capacity. The main challenge now is the design of a low-cost, low-power universal multi-standard receiver that can work over all the standards mentioned above. It is not only the variety of standards with different signal bandwidths and carrier frequencies that makes the design difficult to achieve but also, the frequency band that every individual standard needs to cover. The frequency allocation for DVB-T/H system for example is shown in Figure 1-1. The DVB-H/T channels in the upper UHF band suffer from very strong close-by transmit-path GSM interferers residing at 880 MHz - 915 MHz band. Due to strong antenna-to-antenna coupling in the devices accommodating the both standards the linearity requirement on the mobile TV receiver is very demanding due to the intermodulation (IM) products of the GSM interferers. Moreover, the DVB-T/H channels reside throughout most of UHF band and part of VHF band. Other analog and digital standards will continue to broadcast in these bands, hence, after the down-conversion, these adjacent blocker signals have to be filtered out with a sharp filter. The effect of intermodulation products is illustrated in Figure 1-2. The presence of strong adjacent channel blockers along with the desired signal at the baseband requires the design of a filter with high linearity and dynamic range. The filter must be able to process large signals with little intermodulation distortion. Harmonics of the signal will remain in the filter stop-band where they are automatically attenuated. However, it is very possible that 3^{rd} order intermodulation between particular combinations of two tones in the stop-band generates significant products in the pass-band as shown in Figure 1-2 (a).

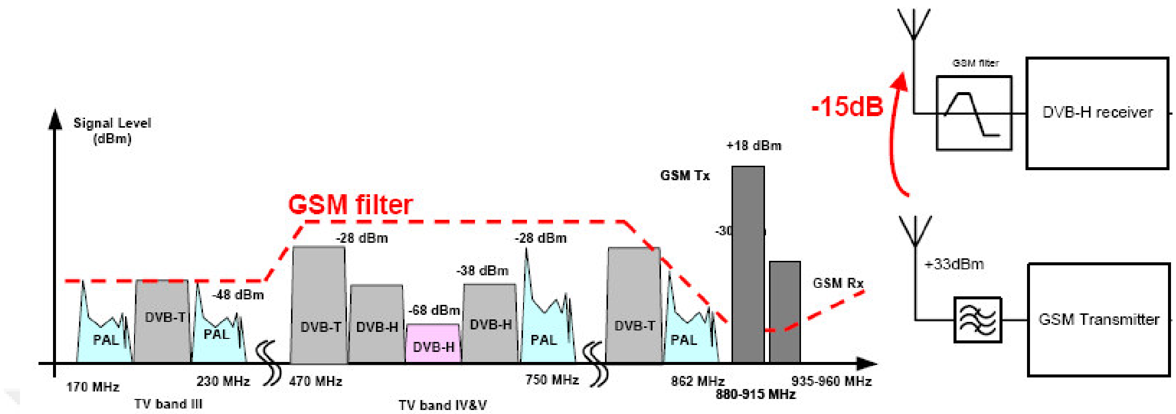


Figure 1-1 Frequency allocation plot for DVB-T/H

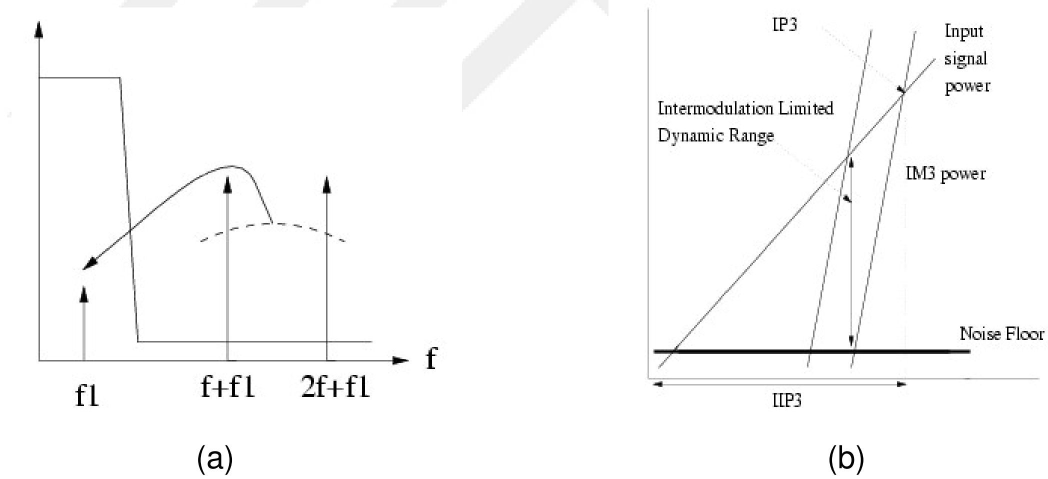


Figure 1-2 Intermodulation (a) IM mixing due to nonlinearity (b) implications of intermodulation on dynamic range

A mobile-TV receiver design for any of the mentioned standards must take the interferers into account. As a concrete example, ISDB-T, channel 7 in VHF band overlaps with the National Television System Committee (NTSC) channel 8. Figure

1-3 illustrates this particular case. For the 3-Seg standard, the adjacent NTSC analog blocker channel can start as close as 300 KHz from the desired ISDB-T channel. Once more, the adjacent channel filtering requirement is stringent. As a result, the receiver system design for mobile TV applications must consider not only power consumption and device size, but also multiple interferers that do exist in the same UHF and VHF bands. Moreover, mobility-dictated impairments, such as doppler and multi-path interference, set additional constraints for mobile TV receiver designers. Hence, new circuit architectures must be investigated to find a low-cost, low-power, high performance receiver solutions for mobile TV technology.

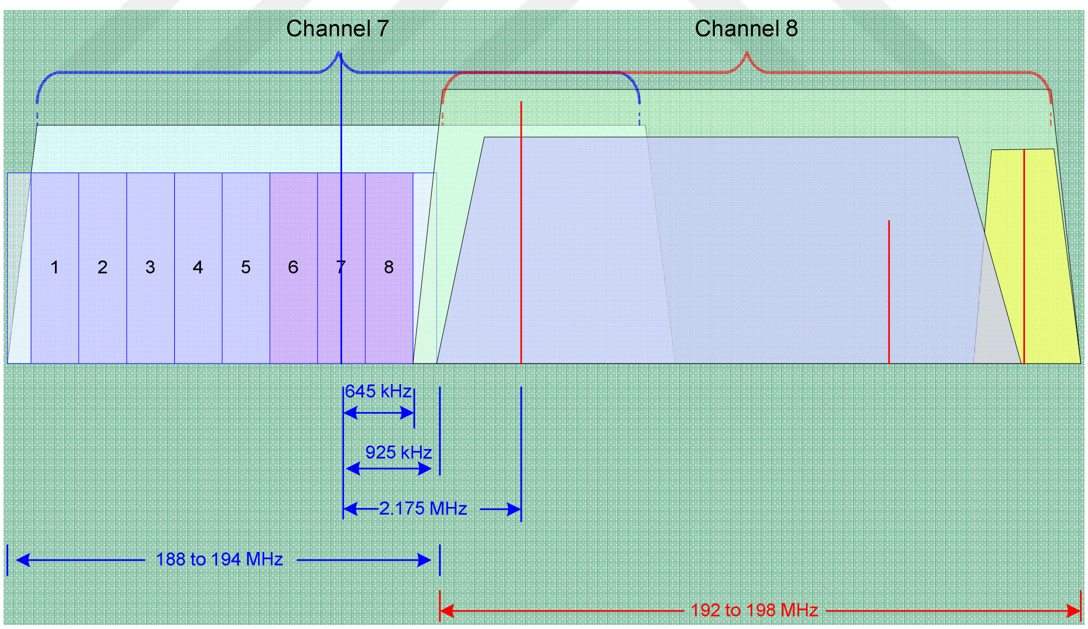


Figure 1-3 Channel allocation in 3-Seg (ISDB-T)

1.3 Receiver Architectures

The emerging wireless standards have various constraints and challenges, a common one being full integration. This led to the development of highly integrated wireless receivers such as direct-conversion (homodyne) and wide-band IF double conversion architectures [3]. The conventional superheterodyne receiver architecture is shown in Figure 1-4.

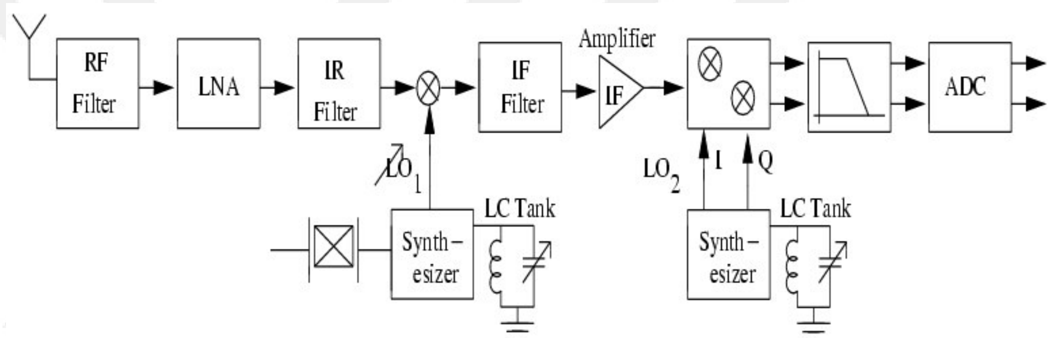


Figure 1-4 Conventional superheterodyne receiver

Its implementation requires the use of discrete-component filters and often expensive technologies like gallium arsenide and silicon bipolar in addition to CMOS. At the front end, a radio frequency (RF) filter is used to remove the out-of-band energy. Additionally, it partially rejects the image-band signals which are further attenuated by an image rejection (IR) filter. The desired band is shifted to a fixed intermediate frequency (IF) by mixing it with a variable frequency synthesizer. Then, an IF filter is used to attenuate alternate channel energy. Finally, the desired band is downconverted to baseband using a second mixer. This mixer performs the conversion twice with sine and cosine. This is called quadrature downconversion which helps in eliminating the image signal. However, these high frequency filters should be associated with very high quality factors (Q) in order to achieve the desired selectivity and sensitivity performance. But such high Q filters are impractical for integration.

On the other hand, in direct conversion receivers the desired signal is downconverted to the baseband using a single mixer stage eliminating the off-chip IF stage and the IR filtering as shown in Figure 1-5. However, there are two major issues with this architecture. First, the presence of a time-varying offset at the mixer output reduces the receiver dynamic range and in the worst case it can saturate the baseband chain, particularly at high gain settings. The DC offset is caused by coupling of the local oscillator (LO) signal back to the LNA input, or even to the antenna. Self-mixing of this LO signal can result in substantial DC offset at the baseband input. Second, the integration of a high frequency, low phase-noise, channel select frequency synthesizer is a difficult task.

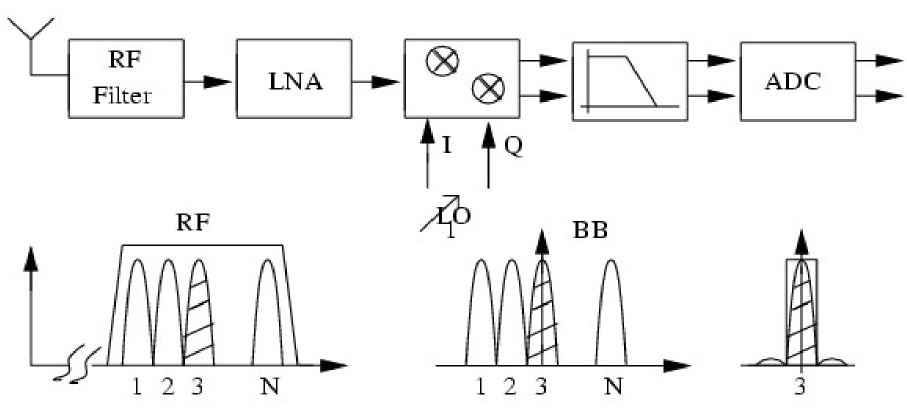


Figure 1-5 Direct conversion receiver

The wide-band IF with double conversion architecture shown in Figure 1-6 circumvents the problem of frequency synthesizer integration. Unlike the superheterodyne receiver, this receiver translates the desired RF band to IF using a mixer with a fix frequency LO which can be implemented with low-Q on-chip components.

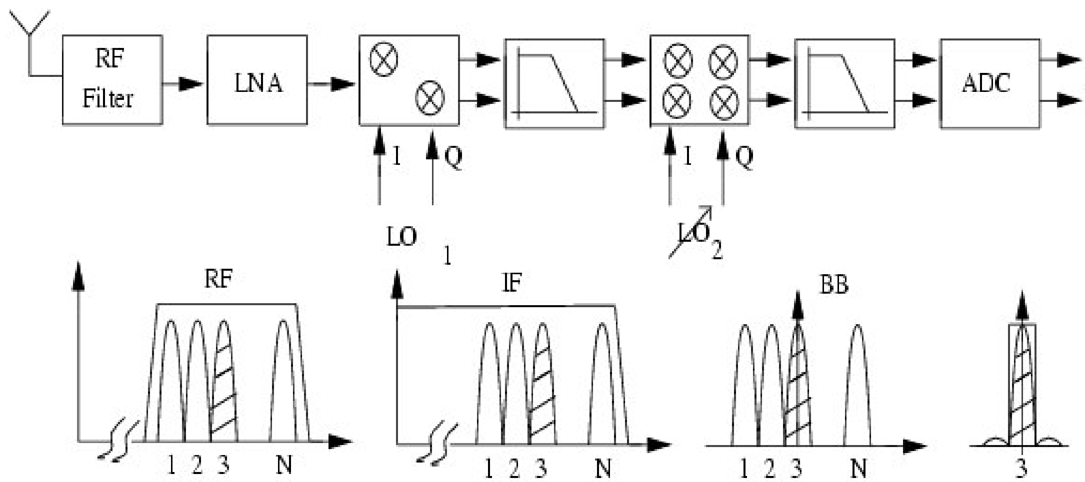


Figure 1-6 Wide-band IF with double downconversion receiver

Upconverted frequency signals are eliminated using a simple IF low pass filter. A second mixer downconverts the IF channels to baseband selecting the desired channel using a tunable frequency synthesizer. In summary, most of the integrated receiver architectures perform channel filtering and final amplification at baseband.

1.4 Baseband Blocks

As discussed earlier, integrated receivers perform channel filtering and variable gain amplification at baseband. This enables the implementation of a programmable integrated channel select filter for multi-standard applications. However, baseband channel filtering is often subjected to strong adjacent channel blockers along with the desired signal requiring the design of filters with high linearity and dynamic range. Because of noise-linearity-power trade-offs, different RF filters and mixers are used for each standard. However, a programmable/reconfigurable baseband chain with filter and amplifier sections that can be shared by different wireless standards results in a simplified, low power and cost-effective design solution. Thus, this baseband chain will have the most significant contribution to the hardware saving of the entire receiver. However, the design of a programmable, large dynamic range baseband represents a major challenge, particularly at low supply voltages dictated by the modern deep-sub-micron CMOS processes.

For optimum performance the filtering operation should be accompanied by signal amplification. The combined filtering/gain operation ensures that the out-of-band signals are attenuated while the desired in-band signal is amplified. This simultaneously improves the overall noise figure of the receiver and relaxes the dynamic range requirement of the analog to digital converter used. The baseband analog blocks required in an integrated wireless receiver are: (1) Highly linear filter section for out-of band blockers attenuation, (2) Tunable filter section for channel selection and (3) Variable gain amplifiers for providing programmable gain settings. The role of the baseband VGA and filters is illustrated in Figure 1-7. Clearly the required goal is to convert the received signal to the digital domain with minimum power consumption. The filter bandlimits the signal and removes unnecessary channels thus enabling an ADC with lower resolution and sampling frequency to be used. Variable gain amplifiers (VGAs) in the baseband chain compensate for gain variation in the RF front-end and reduce the dynamic range of the ADC.

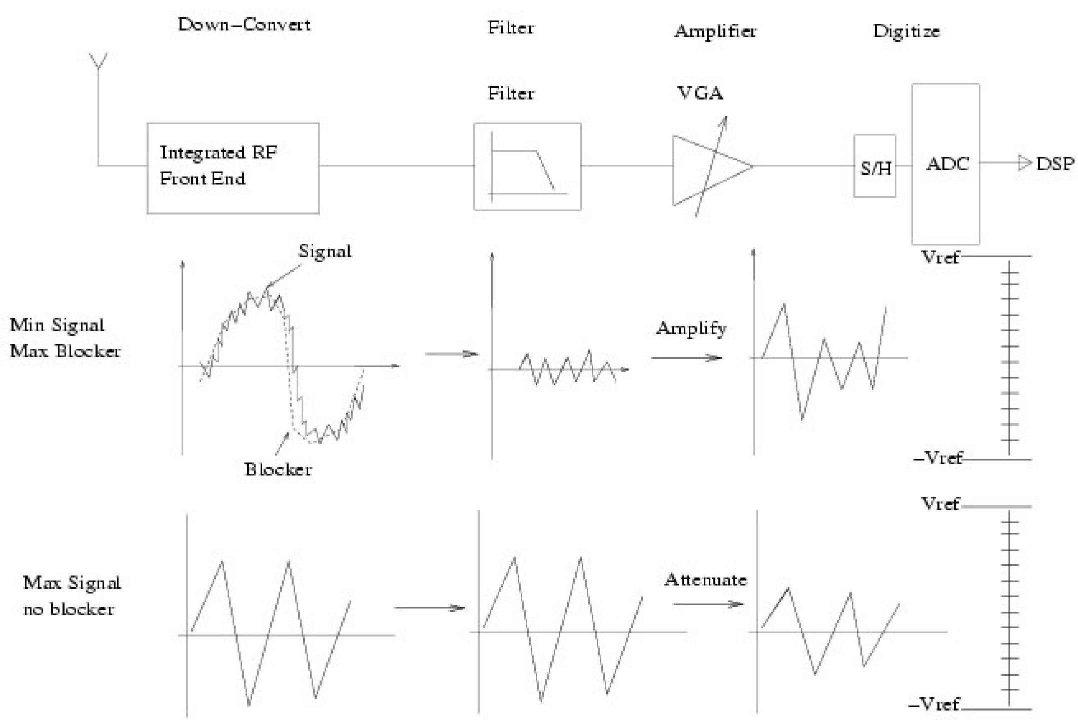


Figure 1-7 Baseband signal processing

Since the signal level at the baseband section can vary depending on the strength of the received signal the ADC must be designed to handle the minimum and maximum expected signal levels. The VGA is used to reduce the variation of the signal by providing an adjustable gain. In case of a weak signal reception the VGA amplifies the signal at the ADC input and thus an ADC of lower resolution can be used. Similarly in case of a large signal reception the VGA gain is reduced appropriately to prevent the signal from saturating the baseband blocks and the ADC. The tradeoff in baseband chain design is thus in the choice of a higher filter order and a wider gain control in the VGA sections on the expense of a relaxed ADC specification (sampling frequency and resolution).

1.5 Research Goals and Thesis Organization

Recently, many high performance receiver circuits have been reported [4-10]. Most of these designs tailor the technology and the classical circuit techniques to achieve good performance for a given application. As the supply voltages decrease however, this approach does not remain competitive. Lower supply voltage requires lower noise levels to be able to maintain a comparable DR performance. As discussed in the previous section, in most of the integrated receivers a channel select filter is employed to attenuate the nearby blockers and hence relax the dynamic range requirement of the ADC. Design of a low noise classical filter circuit involves use of large on-chip capacitors, which translates into a large die area. Hence, in order to alleviate the area tradeoff in a high cost deep-sub-micron process, new circuit topologies must be investigated. The work presented in this thesis introduces some innovative noise shaping circuit techniques to enable the transition to a lower supply voltage without the extra cost of die area. The novel circuit concepts introduced in this work have been supported with the measurement results of a 65-nm CMOS test chip. The final baseband chain combining these unique circuit techniques has proven to be a high performance universal radio baseband that can be used for any application with signal bandwidths in the range 700 KHz up to 5.2 MHz. The characterization of the final design has been performed for two demanding mobile TV applications, Integrated Services Digital Broadcasting-Terrestrial ISDB-T (3-Segment f_c=700 KHz) and Digital Video Broadcasting-Terrestrial/Handheld (DVB-T/H f_c=3.8 MHz). Low noise, low power, highly linear operation with fine programmability as well as very small die size in a low-cost process makes the proposed architecture an attractive solution for new generation multi-standard wireless devices.

The thesis is organized as follows: in Chapter 2, frequency dependent negative resistance based novel post-mixer third-order elliptic filtering stage is introduced. Thanks to unique noise shaping characteristics of the circuit, a high order blocker filtering is achieved at as early as the mixer outputs. Such a technique improves the sensitivity of the receiver chain significantly, particularly with regard to the existence of large adjacent interferers. The detailed noise, stability, and linearity analysis of the proposed technique are presented along with the measurement results from the 65-nm CMOS test chip.

Another noise shaping circuit concept is introduced in Chapter 3. The Asymmetric Floating Frequency Dependent Negative Resistance (AFFDNR) circuit in the feedback of an amplifier is introduced as a unique solution for providing gain in the signal band while simultaneously implementing a third-order low-pass elliptic response for the blocker signals. This blocker aware post-mixer amplifier provides up to 20 dB of programmable gain ahead of the following baseband blocks, reducing their overall noise contributions.

A differential-ramp based Variable Gain Amplifier (VGA) technique is introduced Chapter 4. Using the proposed technique, digitally programmable gain amplifiers (PGAs) can be converted to analog controlled, dB-linear VGAs with minimum impact on noise and linearity. This provides an efficient way of realizing an analog controlled VGA for OFDM based applications. The technique is illustrated by converting an opamp based high-linearity, low-noise PGA to a dB-linear VGA.

Chapter 5 presents a novel universal receiver baseband architecture using the low-noise circuit blocks presented in the preceding chapters. The chain includes a post-mixer noise shaping blocker pre-filter, a programmable-gain post mixer amplifier (PMA) with blocker suppression, a differential ramp-based novel linear-in-dB variable gain amplifier and a Sallen-Key output buffer. The 1.2-V chain is implemented in a 65-nm CMOS process, occupying a die area of 0.45 mm^2. The total power consumption of the baseband chain is 11.5 mW. While the device can be tuned across a bandwidth of 700-KHz to 5.2-MHz with 20 KHz (80 KHz at the high end of the band) resolution, it is tested for the mentioned mobile TV applications, ISDB-T and DVB-T/H.

2 Noise Shaping Blocker Filtering Technique for Low Noise Integrated Receivers

2.1 Introduction

In today's wireless communication systems, very strong interferers can coexist in the nearby channels whereas the desired signal in the channel of interest might be very weak. This is particularly the case for mobile-TV applications, where very strong interferers can exist in the vicinity of the desired channel [11]. Amplification of the signal in the desired channel should be accompanied with the high-order filtering of the strong blockers in the nearby channels to increase the dynamic range of the overall system. For handheld and portable devices, the solution must offer a small device area with low-power and low-noise operation.

Common amplifier-filter topologies can be used as in the case of existing radio receivers [5-6], [9-10], [12]. However, there are severe trade-offs in terms of noise, area, and power in existing solutions. A typical Direct Conversion Receiver (DCR) block diagram with corresponding signal and noise profiles is shown in Figure 2-1. The point immediately after RF down-conversion (A) is generally a critical point and determines the required circuitry down the chain depending on the signal and blocker profiles in the band of interest. A topology with a gain stage followed by filtering can yield better sensitivity, as long as the blocker levels in the adjacent channels are limited and noise is the main factor to consider (Figure 2-2 (a)). In the case of strong blockers however, such architecture may not be optimum, due to the resulting stringent linearity requirement of the amplifier.

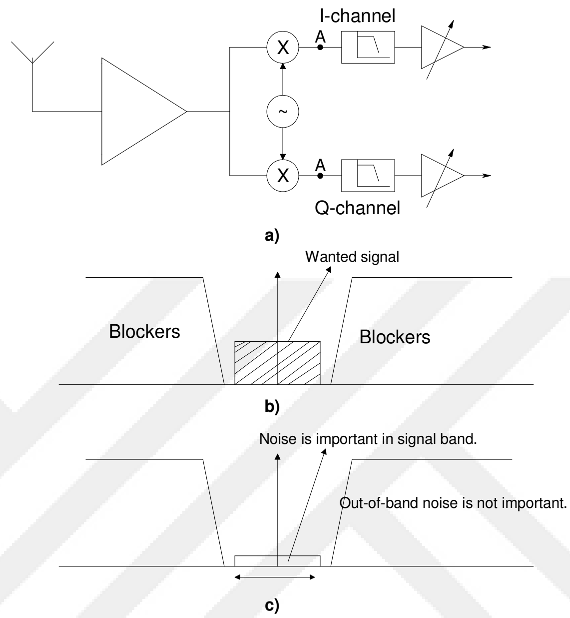


Figure 2-1 Typical DCR receiver front-end; (a) Block diagram (b) Signal profile around the desired channel c) Noise profile around the desired channel

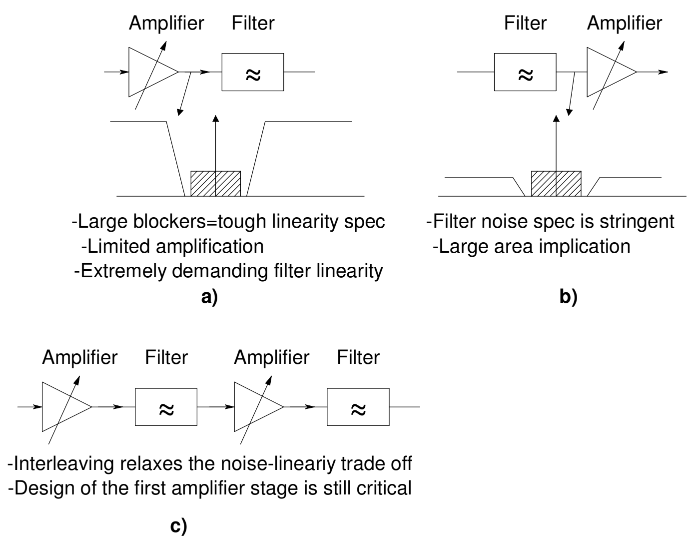


Figure 2-2 Noise-linearity trade off in different architectures; (a) Gain-filtering topology (b) Filtering-gain topology (c) Interleaved gain-filtering topology

In the case of a gain-filtering interleaved architecture as shown in Figure 2-2 (c), the design of the first amplifier stage can be demanding. Thus, a filtering block might be required ahead of the gain stage as shown in Figure 2-2 (b). The filter noise should be minimal for such a topology so as not to degrade the sensitivity due to noise. This can be satisfied with an additional cost of area and power in the filter if classical filter circuit topologies are to be employed [13-21].

The proposed FDNR (Frequency Dependent Negative Resistance) based filtering technique that is described in detail in Section 2.2, offers unique advantages in terms of noise with its noise shaping characteristics [22-25]. Moreover, the circuit provides this high order filtering at the mixer output protecting this node against blockers, a feature that traditional filter topologies can not offer. Filtering at this critical node relaxes the mixer linearity spec and allows the mixer to have a higher gain. Input noise spec of post-mixer blocks can thus be further relaxed. Hence, employing the technique in the receive chain of a radio can enhance the overall performance of the radio, an improvement that can not be achieved using classical gain-filtering techniques unless area is sacrificed. The proposed technique, however, needs to be analyzed and the trade-offs should be clarified in terms of noise, linearity, power, area, and most importantly stability. Coexistence of multiple interdependent feedback paths dictates a careful analysis of the stability of the proposed circuit. To prove the clear benefits of the concept, detailed noise, linearity and stability analysis are carried on in Section 2.3, Section 2.4 and Section 2.5, respectively. The details the class-AB opamp and the bandwidth calibration circuit are presented in Section 2.6. Section 2.7

presents the measurement results of a 65-nm CMOS proof-of-concept test-chip. Higher order implementation techniques are introduced in Section 2.8 as possible future work and in Section 2.9 we present our conclusion.

2.2 An FDNR Based Third Order Elliptic Response Circuit

In early 70's, following their invention, FDNRs were used extensively to realize high order filter functions [26-32]. However, some known drawbacks encountered in the filter implementations have limited their use as a filter section. In most of the target low-pass implementations, for example, there is a DC response associated with the series capacitor in the signal path [30]. The FDNR circuit satisfies the negative resistance function only in reference to the circuit ground. Moreover, the number of opamps employed in an FDNR based filter is greater than that of an integrator based implementation of the same transfer function. Considering these disadvantages, these FDNR based topologies have long been abandoned. The circuit of the proposed third-order section shown in Figure 2-3, however, offers some unique features that can be utilized to design a very low noise, blocker-immune radio base-band. Moreover, it can be extended to higher order structures with no additional resistance or capacitance in the signal path (Section 2.8).

The main advantage of the proposed third order configuration of Figure 2-3 is that it uses only one resistor in the signal path, the load resistor of the preceding stage R_f, to realize the desired filter transfer function. Hence the load resistance of a mixer or of a gm stage can be reutilized as a part of the filter transfer function which is not the case for classical filter topologies. The noise contribution of this particular resistor is already accounted for in the mixer noise budget and the noise of the FDNR resistors R_1, R_2, R_3, is shaped (Section 2.3). Since the opamps are not in the signal path, their flicker noise contributions are also shaped and hence have less contribution to the overall filter noise.

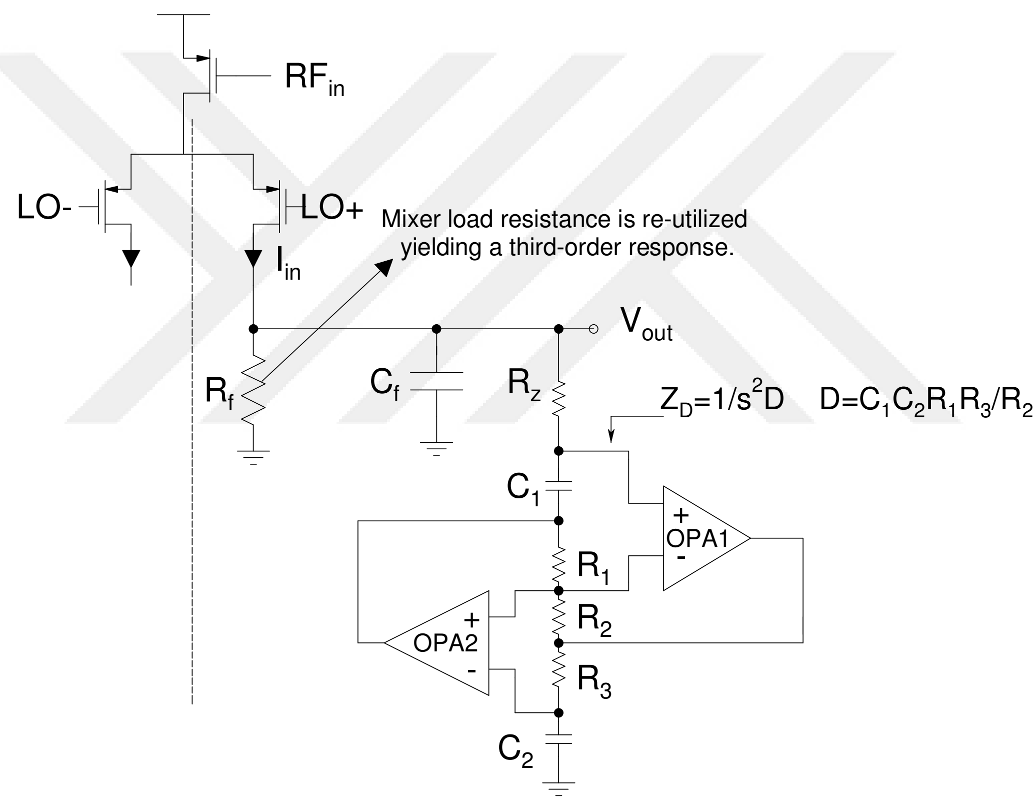


Figure 2-3 Simplified single-ended schematic of the proposed third-order elliptic circuit at the mixer output

Moreover, as opposed to classic filter topologies, the opamps of the proposed third-order section are not in the signal path and hence do not contribute any IQ mismatch or DC offset, which is a much desired property in a receiver chain. The signal transfer function of this circuit from input to output can be written down as follows:

$$\frac{V_{out}(s)}{I_{in}(s)} = \frac{R_f\,(s^2 DR_z + 1)}{s^3 DR_z R_f C_f + s^2\left(DR_z + DR_f\right) + s\left(R_f C_f\right) + 1} \tag{2.1}$$

$$D = {C_1 C_2 R_1 R_3}/{R_2}\,. \tag{2.2}$$

This signal transfer function provides a notch at a frequency, $\omega_{notch} = 1/\sqrt{DR_z}$ and the notch frequency depends on the value of D and R_z. As a result, a large variety of component values can be used to realize the desired cut off and notch frequencies. Linearity, stability and area trade-offs associated with proposed circuit will be investigated to narrow down to an optimum component value combination for the target application.

2.3 Noise Analysis

The schematic including the noise sources in an FDNR is shown in Figure 2-4. In the proposed circuit, the noise of all passive and active components in the FDNR section, namely of R_z, R_1, R_2, R_3, OPA_1 and OPA_2, is shaped, hence the only substantial noise contributor is R_f whose noise contribution is accounted for in the amplifier or mixer noise budget.

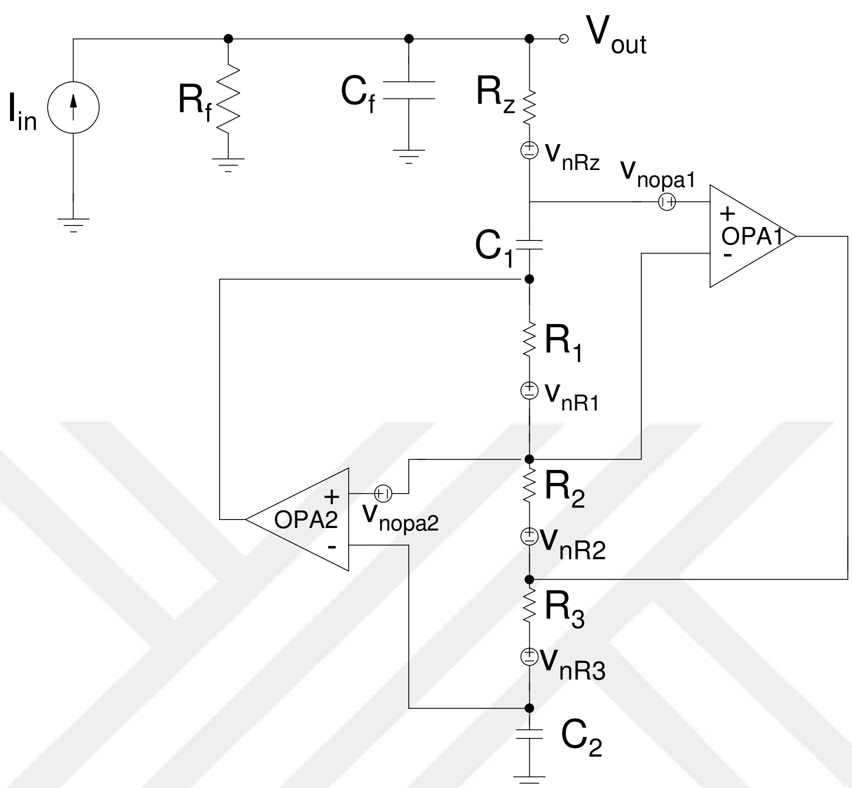


Figure 2-4 Schematic including the noise sources in the circuit

In order to clarify the noise shaping concept of the proposed circuit, the noise transfer functions from each of these contributors have been calculated and presented as follows:

OPA_1 noise transfer function:

$$\frac{V_{out}(s)}{Vn_{OPA1}(s)} = \frac{sC_1R_f\left(1 - s\,R_1R_3C_2/R_2\right)}{s^3DR_zR_fC_f + s^2\left(DR_z + DR_f\right) + s\left(R_fC_f\right) + 1} \tag{2.3}$$

OPA_2 noise transfer function:

$$\frac{V_{out}(s)}{Vn_{OPA2}(s)} = \frac{sC_1R_fR_1\left(sR_3C_2 + 1\right)}{R_2(s^3DR_zR_fC_f + s^2\left(DR_z + DR_f\right) + s\left(R_fC_f\right) + 1)} \tag{2.4}$$

R_z noise transfer function:

$$\frac{V_{out}(s)}{Vn_{Rz}(s)} = \frac{s^2 DR_f}{s^3 DR_z R_f C_f + s^2(DR_z + DR_f) + s(R_f C_f) + 1} \tag{2.5}$$

R_1 noise transfer function:

$$\frac{V_{out}(s)}{Vn_{R1}(s)} = \frac{sR_f C_1}{s^3 DR_z R_f C_f + s^2(DR_z + DR_f) + s(R_f C_f) + 1} \tag{2.6}$$

R_2 noise transfer function:

$$\frac{V_{out}(s)}{Vn_{R2}(s)} = \frac{sR_1 R_f C_1}{R_2 (s^3 DR_z R_f C_f + s^2(DR_z + DR_f) + s(R_f C_f) + 1)} \tag{2.7}$$

R_3 noise transfer function:

$$\frac{V_{out}(s)}{Vn_{R3}(s)} = \frac{sR_1 R_f C_1}{R_2 (s^3 DR_z R_f C_f + s^2(DR_z + DR_f) + s(R_f C_f) + 1)} \tag{2.8}$$

Figure 2-5 shows the plots for the magnitude of these noise transfer functions as well as the signal transfer function. Since the noise generated by the FDNR resistors is shaped, the designer can use larger resistors (noisier) and hence can reduce the capacitor size. This results in a significant area saving. As a mean of comparison, the total amount of capacitor required versus the desired noise level in a bandwidth of 1-MHz is plotted in Figure 2-6 for various third order filter topologies (Figure 2-7) as well as the FDNR based filter topology described in this work. It should be noted that the single opamp topologies (Sallen-Key and Multiple-Feedback) can not achieve an elliptic response; hence their overall figure of merit may not be as high for applications requiring large attenuation in the nearby channels.

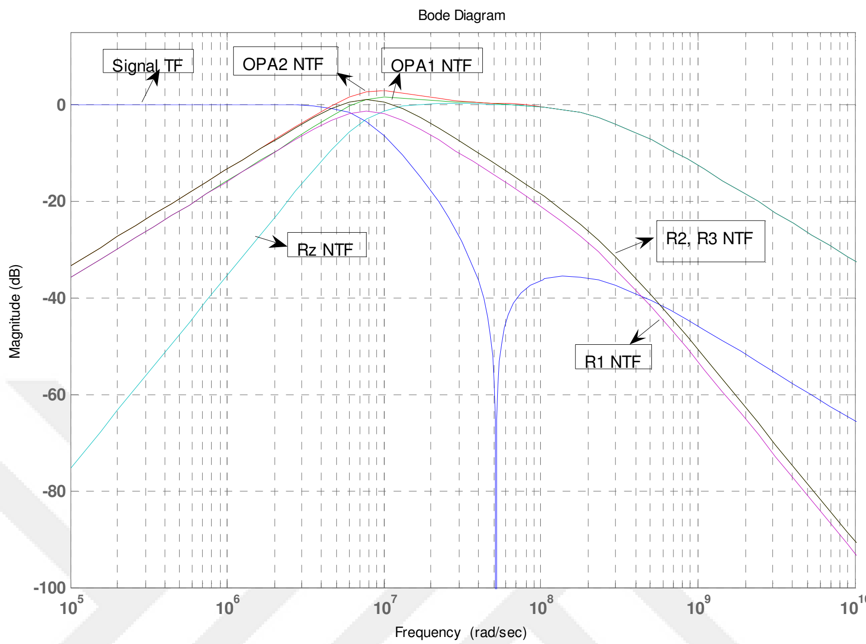


Figure 2-5 Signal and noise transfer functions of the proposed circuit

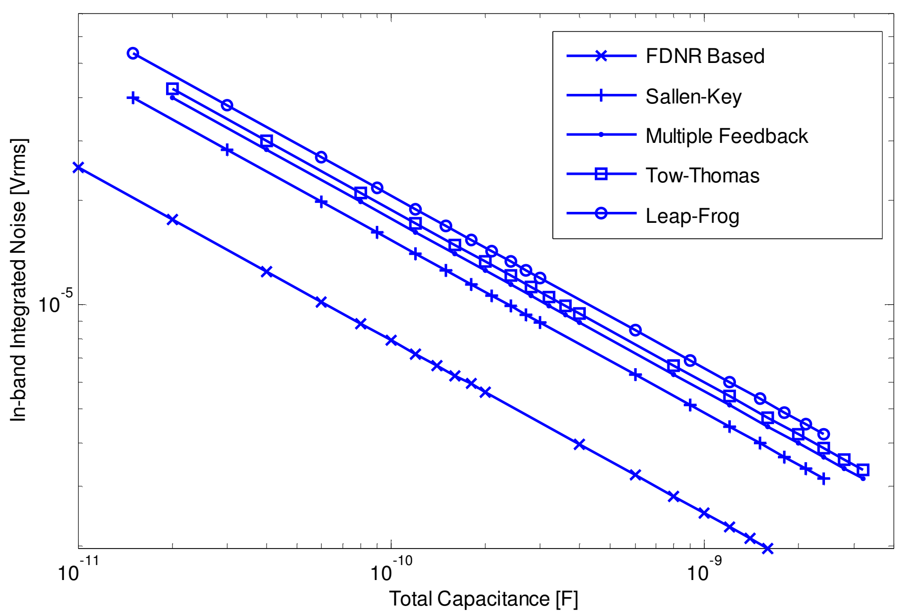


Figure 2-6 Total integrated in-band noise vs. required capacitance for the various third order filter topologies shown in Figure 2-7

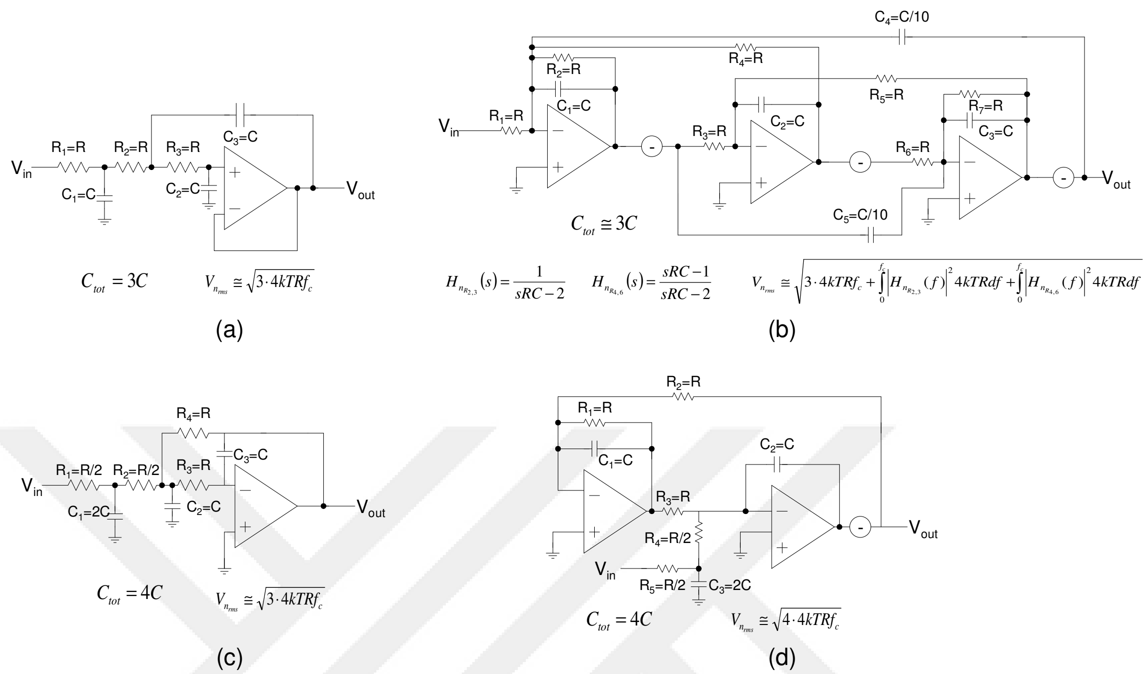


Figure 2-7 integrated in-band noise for various third-order filter topologies: (a) Sallen-Key. (b) Leap-frog (ladder). (c) Multiple-feedback. (d) Tow-Thomas.

For the sake of simplicity, the plots shown in Figure 2-6 reflect the noise only due to the resistors in the circuits and do not include the noise contributions of the opamps used in these circuits. Since the noise of the opamps is also shaped in an FDNR based topology, the advantage of this topology becomes even more pronounced once the opamp noise contributions are also included in the analysis.

2.4 Linearity Analysis

There are two important cases that need to be addressed regarding the linearity of the circuit. First, the response of the circuit to two strong tones at the blocker frequencies. The IM3 product of these tones is minimized by providing a very large gain in the opamps at these blocker frequencies. The other case is the nonlinearity experienced by the in-band signal. Depending on the ratio of notch frequency to cut-off frequency, the overall filter response can display some peaking around the cut-off frequency. The peaking in the signal transfer function might result in larger peaking at the internal FDNR nodes, particularly at the opamp outputs of the proposed circuit. Thus, a full swing in-band signal might cause the FDNR opamps outputs to have even a larger swing degrading the overall linearity of the circuit. Hence, the signal transfer function should be optimized taking the peaking at the internal FDNR nodes into account.

The transfer function from input to Opamp2 output can be written down as follows:

$$\frac{V_{opa2}(s)}{V_{in}(s)} = \frac{(s\ D/C_1 + 1)}{s^3 DR_z R_f C_f + s^2\left(DR_z + DR_f\right) + s\left(R_f C_f\right) + 1} \tag{2.9}$$

The magnitudes of this transfer function as well as the signal transfer function are shown in Figure 2-8 (b) and Figure 2-8 (a), respectively, for a range filter characteristics corresponding to the same cut-off and notch frequencies. As can be observed from the plots, more rapidly decreasing filter response with more stop-band attenuation results in more peaking at the internal nodes. We can approximate the magnitude of the transfer function given in (2.9) around the cut-off frequency as follows:

$$\left|H_{opa2}(s)\right|_{f=f_c} \cong \sqrt{1 + \frac{{\omega_c}^2 D^2}{{C_1}^2}} \Big/ \sqrt{2} \tag{2.10}$$

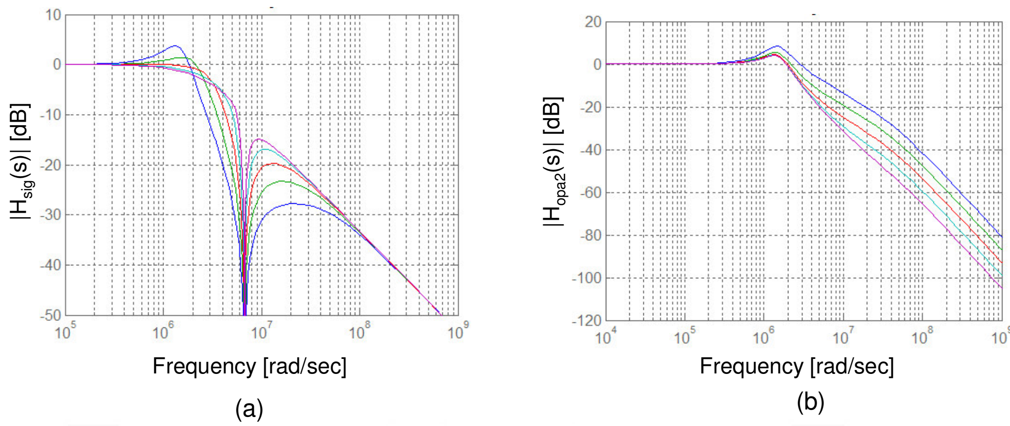


Figure 2-8 (a) The filter response for various peaking levels (b) Corresponding peaking levels at the FDNR internal node

(2.10) suggests that the only way to obtain higher attenuation for fixed cut-off and notch frequencies without introducing extra peaking is to increase the value of capacitor, C_1. The amount of peaking that is allowed at the opamp output sets the minimum value for this capacitor as shown in Figure 2-9.

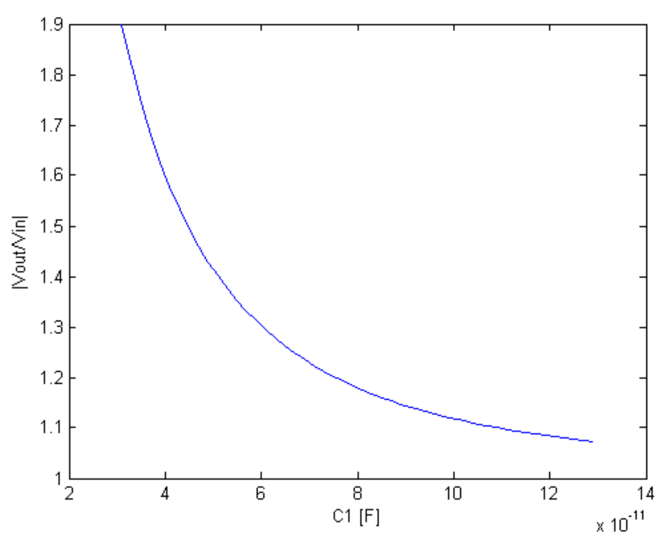


Figure 2-9 Minimum C_1 capacitance values corresponding to various peaking levels at the opamp outputs

2.5 Stability Analysis

The stability of the system should also be taken into account while optimizing the design for the desired filter response. There are multiple feedback networks that require attention. A simplified stability analysis of system is useful since it has implications on unity gain bandwidth, DC gain and compensation scheme of the opamps used in the design. In order to simplify the analysis, one of the opamps is considered to be ideal while the other one is analyzed with the network around it. If each of these independent cases provides the required margin for stability, the initial assumption for each individual case is not violated, and hence the system can be expected to be stable.

Figure 2-10 (a) shows the loop around Opa1. In order to simplify the analysis, the same capacitor and resistor values are used for all of the components in the circuit. Switching to the actual design parameters would only move the poles and zeros around the ones corresponding to this simplified configuration. The loop transfer function around this opamp can be written as follows:

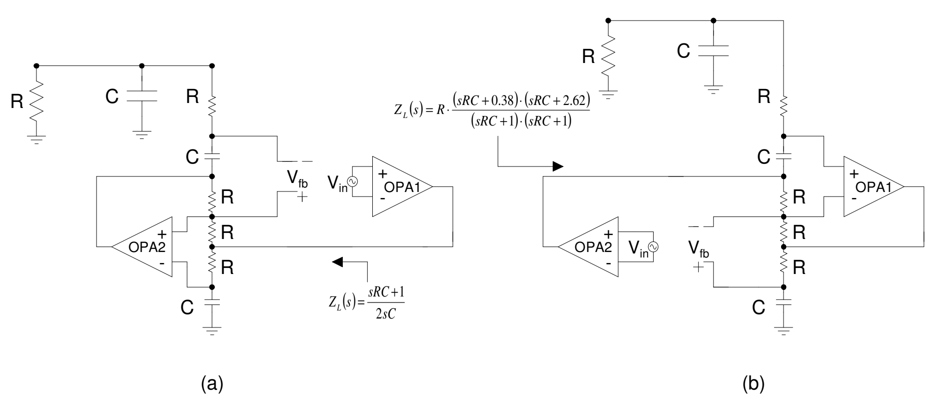


Figure 2-10 (a) Stability case for OPA1, where OPA2 is assumed to be ideal (b) Stability case for OPA2, where OPA1 is assumed to be ideal

$$L(s) = A(s) \cdot \frac{(sRC+1)(sRC+0.12+j0.8)(sRC+0.12-j0.8)}{(sRC+1)(sRC+0.38)(sRC+2.62)} \tag{2.11}$$

where, A(s) is the opamp transfer function when loaded with an impedance $Z_L = \frac{(1+sRC)}{2sC}$. This loading corresponds to a pole and a zero in the opamp transfer function including the output impedance of the driver devices in the opamp. All poles and zeros are in the vicinity of the filter cut-off and notch frequency and all cancel out including the ones resulting from the opamp loading. However, two of the zeros in the loop transfer function are complex conjugate and cause a notch in both the amplitude and phase response. If the gain of the amplifier around this notch frequency is not large enough to absorb the phase and amplitude notch with margin, system stability can be threatened. The loop transfer function is the same for the Opa2 case shown in Figure 2-10 (b). However, this time the load seen by the opamp is $Z_L = R \cdot \frac{(sRC+0.38)(sRC+2.62)}{(sRC+1)(sRC+1)}$ and has two poles two zeros. Again the second opamp, Opa2, needs to be able to provide sufficient gain around the cut-off frequency.

In conclusion, the opamps in the proposed design should not only target high unity gain bandwidth, but also should provide a large gain around the desired notch frequency. This is generally the case for most of the opamps used in filter applications, but, for this particular FDNR application this requirement has an impact on the stability of the system.

2.6 Opamp and Bandwidth Calibration Circuit

The schematic of the opamp used in the design is shown in Figure 2-11 (a). This folded-cascode opamp achieves a unity gain bandwidth greater than 200-MHz, consuming 380 μA from a 1.2 V supply with a phase margin of 61°. The input devices M_1 and M_2 are native (zero-Vt) devices to allow a rail-to-rail input swing. The PMOS and NMOS cascode devices are biased with a Vt-multiplier bias stage shown in Figure 2-11(a). Hence, the cascode bias points track the process variations adjusting the headroom in these devices accordingly. The output is a class-AB stage with cascode devices biasing the floating current sources. This way, high impedance is maintained at the first stage output. Higher impedance at this node results in a higher unity gain bandwidth since the total amount of compensation capacitor needed drops with higher impedance at this node.

The bandwidth calibration circuit used in the design is shown in Figure 2-11 (b). During the initial calibration a 7-bit bandwidth calibration code sets the resistive DAC targeting the desired filter bandwidth for a given crystal clock frequency. The trim range of this resistor is large enough to cover whole filter bandwidth as well as any crystal frequency in the range of 10 MHz to 40 MHz that is used as a reference. Following this, successive approximation logic computes a calibration code with the help of a comparator as illustrated in Figure 2-11 (b). Note that, since the resistor in this configuration is used as a trim element determining the bandwidth and crystal frequency, the capacitor is used as the calibration element with 6-bit resolution. In the filter side, in addition to corresponding 6-bit resolution capacitor bank, there is a resistor trim to switch between the high-end and the low-end of the band. Tuning resolution at the low-band mode is around 20 KHz.

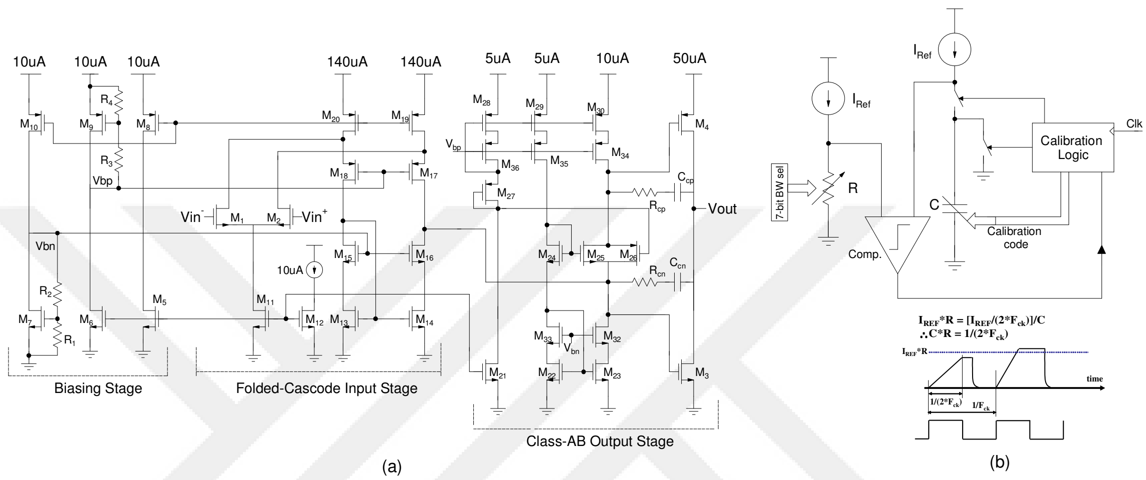


Figure 2-11 (a) The native input, folded-cascode, class-AB opamp schematic (b) Bandwidth calibration circuit

2.7 Measurements

A design covering a tuning range from 700-KHz to 5.2-MHz is fabricated in a 65-nm CMOS process and tested. The cut-off, notch and stop-band characteristics can independently be set to satisfy the blocker and noise requirements of various applications across the band with a 7-bit control word corresponding to a tuning resolution of 20-KHz. Figure 2-12 (a) shows various filter transfer function curves corresponding to different trim codes across the band. The testing and characterization is done for two distinct applications, Integrated Services Digital

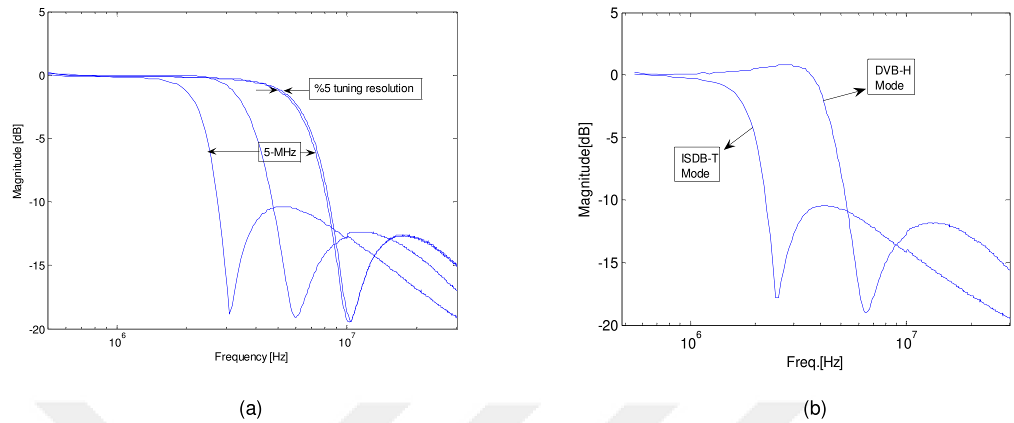


Figure 2-12 (a) Measured filter response for various bandwidth settings across the band. (b) Filter responses corresponding to target ISDB-T and DVB-H applications

Broadcasting-Terrestrial (ISDB-T) and Digital Video Broadcasting – Handheld (DVB-H), with signal bandwidths being 750-KHz and 3.8-MHz, respectively. The filter can be tuned to provide optimum response for in-band and blocker signals corresponding to these two example applications (Figure 2-12 (b)). In ISDBT mode, the signal cut-off is around 750-KHz whereas the N+1 blocker starts at 2.5-MHz. In DVBH mode, the signal bandwidth is around 3.8-MHz whereas the N+1 blocker power can occur in the next 8–MHz bandwidth. The optimum case for the DVBH has a slight peaking in the filter response, since the notch frequency is set to be relatively close to filter cut-off.

The noise characteristics of the filter for these target bands are shown in Figure 2-13. Figure 2-13 (a) shows the noise in ISDB-T mode whereas Figure 2-13 (b) shows the noise in DVB-H mode. The expected noise shaping can clearly be observed

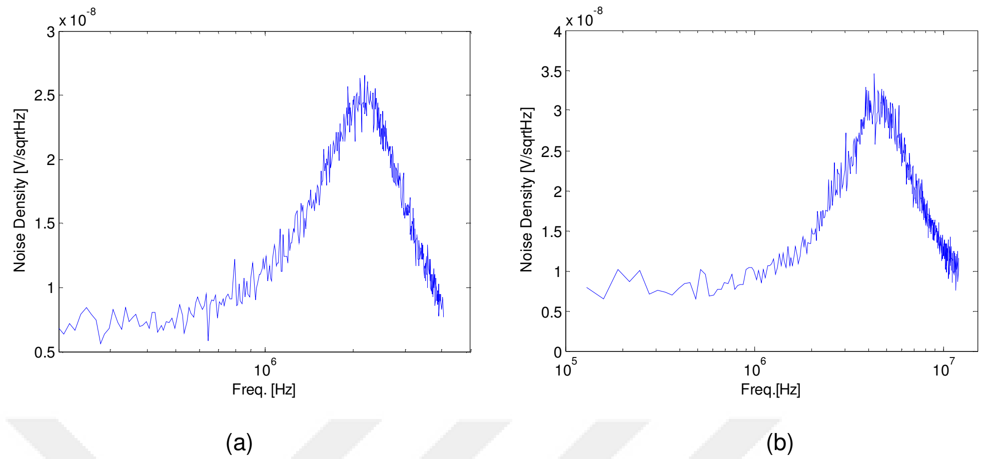


Figure 2-13 (a) Filter noise in ISDB-T mode. (b) Filter noise in DVB-H mode

for the both cases. The noise density in the signal band is around 7.5 nV/sqrtHz, which is mainly due to the 2-kΩ output resistance (R_f) of the driving stage. The 20-dB/decade in-band noise roll-off stops once the noise level of this resistor is reached. This resistor is the load resistance of the mixer or the driving stage and its noise contribution is already accounted for. It is important to note that this load resistor can not be utilized in other active filter topologies and hence additional resistors are required in the filter to achieve the desired filter characteristic. This is a unique advantage of the proposed FDNR based topology. As regard to linearity, HD tests and two-tone IM3 tests were conducted for the both target modes. Figure 2-14 (a) shows that a 250-KHz 420-mVpp differential tone in ISDB-T mode results in -57-dB HD2. A 1.2-MHz 420-mVpp differential tone in DVB-H mode yields -59 dB HD2 (Figure 2-14 (b)).

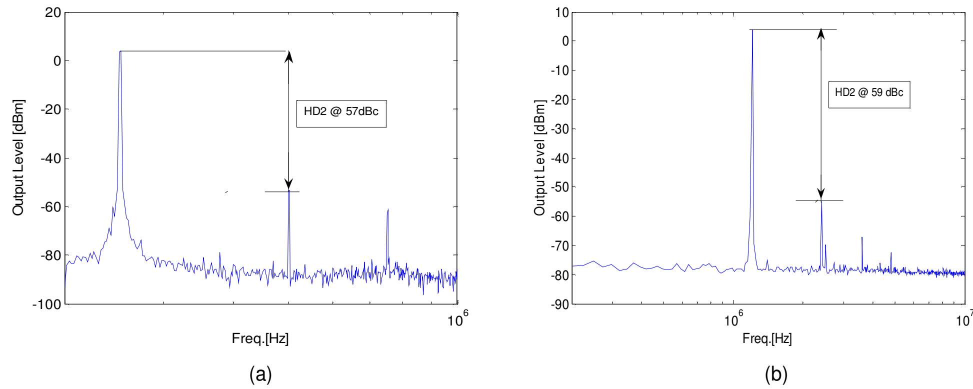


Figure 2-14 (a) In-band HD in ISDB-T mode (b) In-band HD in DVB-H mode

In ISDB-T mode, 2.4-MHz and 4.4-MHz blockers (420-mVpp differential each) result in -80.4-dBc IM3 which corresponds to an out-of-band IIP3 of 36.5 dBm (Figure 2-15 (a)). In-band IIP3 for this case is 22.5 dBm. In DVB-H mode, 5-MHz and 8-MHz blockers (420-mVpp differential each) result in -69.8-dBc IM3 which corresponds to an out-of-band IIP3 of 31.5 dBm (Figure 2-15 (b)). In-band IIP3 for this case is 20 dBm. For the both cases, the tones are swept in-band and out-of-band recording the IIP3 for each of these cases. The plots showing IIP3 with varying average two-tone frequency are shown in Figure 2-16**.** The design occupies a die area of 0.16 mm^2 in the mentioned 65-nm CMOS process. Total power consumption is in the range of 2-mA to 3.2-mA from a 1.2-V supply depending on the received signal strength.

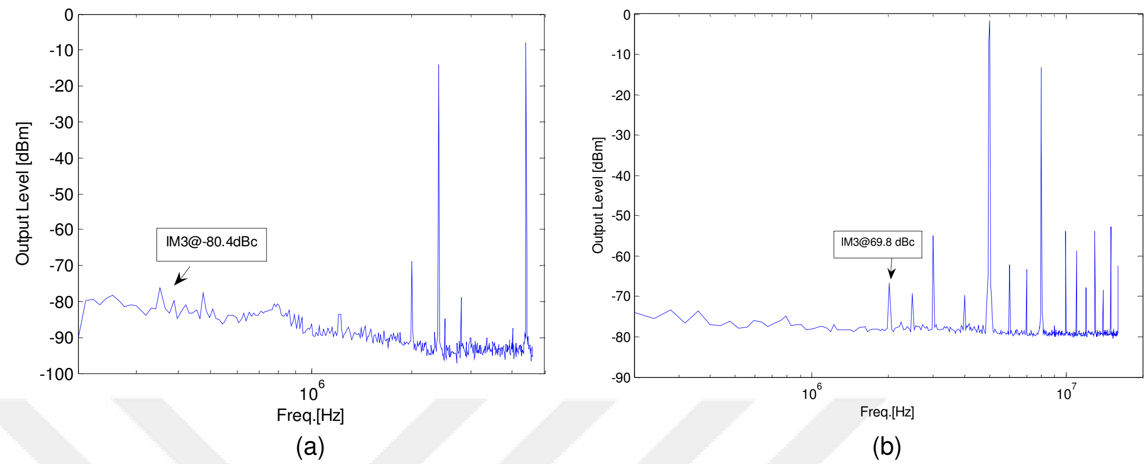


Figure 2-15 (a) Two-tone test in ISDB-T mode (b) Two-tone test in DVB-H mode

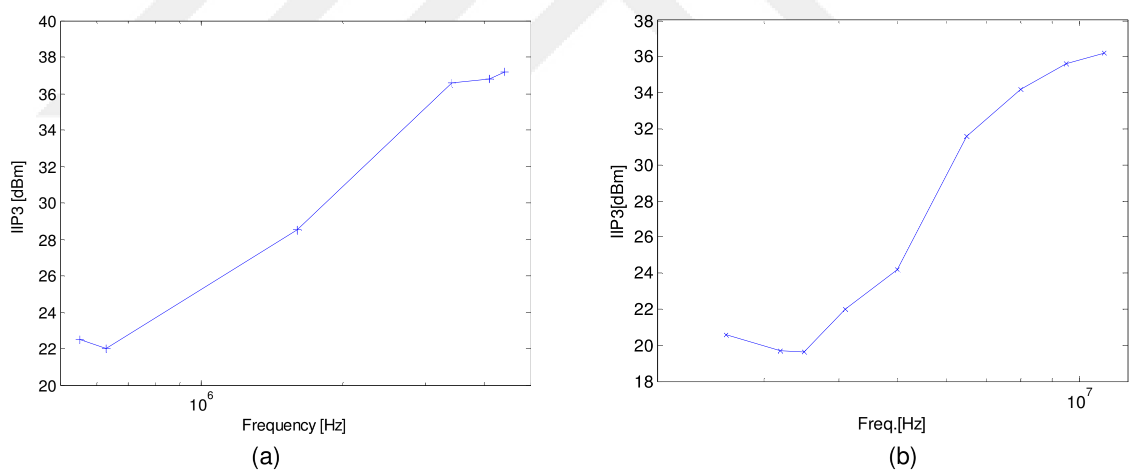
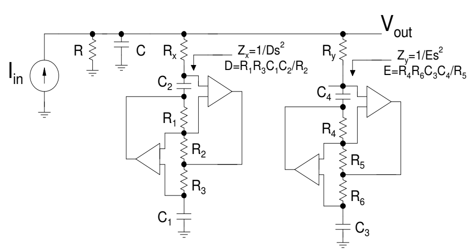


Figure 2-16 (a) IIP3 vs Freq. sweep in ISDB-T mode (b) IIP3 vs Freq. sweep in DVB-H mode

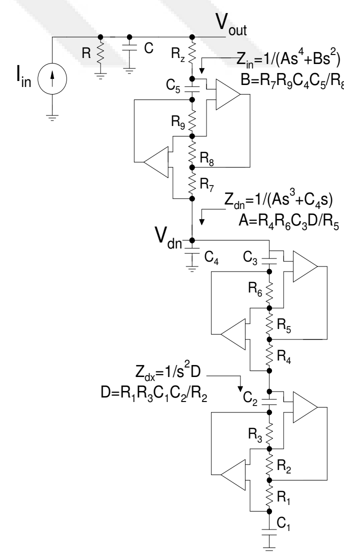
2.8 Higher Order Topologies

Figure 2-17 shows two unique FDNR based double-notch higher order architectures that can be constructed based on the basic third-order idea discussed above. In the four-opamp structure shown in Figure 2-17 (a), there are two FDNR sections placed in parallel each corresponding to a notch in the transfer function. The linearity spec on the one providing the high frequency second notch is relaxed and hence the area for this second FNDR can be scaled down. Six-opamp series architecture (Figure 2-17 (b)) is another interesting architecture where three FDNRs are placed in series configuration resulting in a similar double-notch filter transfer function. The noise from the lowest and the middle FDNRs experience second order and third order noise shaping, respectively, and hence the area penalty for those additional FDNRs is not as severe. The detailed noise and linearity analysis of these structures is left as future work.



$$H(s)=\frac{V_{out}}{I_{in}}(s)=\frac{R(DR_xs^2+1)(ER_ys^2+1)}{DER_xR_yRCs^5+DE(R(R_x+R_y)+R_xR_y)s^4+(DR_x+ER_y)RCs^3+(D+E)(R_x+R_y)s^2+sRC+1}$$

(a)



$$H(s)=\frac{V_{out}}{I_{in}}(s)=\frac{R(AR_zs^4+BR_zs^2+1)}{AR_zRCs^5+A(R_z+R)s^4+BR_zRCs^3+B(R_z+R)s^2+sRC+1}$$

(b)

Figure 2-17 Higher order FDNR architectures: (a) Four-opamp parallel structure (b) Six-opamp series structure

2.9 Conclusion

A noise shaping filtering technique is introduced along with the noise, linearity and stability analysis to bring forward the design trade-offs. The proposed circuit employs an FDNR circuit following the down-conversion mixer in a unique configuration such that strong blockers in the nearby channels are notched down with minimal area and noise cost. The noise of the passive and active filter components are shaped out of the desired band. The technique enhances the sensitivity of a receiver chain significantly, particularly in an environment where strong blockers can coexist. Performance metrics of a 65-nm CMOS test-chip are summarized in Table 2-1. Comparison of the literature in terms of noise and required capacitance per pole is shown in Figure 2-18. It can be seen that the approach proposed in this work results in lower noise for a given amount of capacitance relative to published work to date. The die photo of the design is shown in Figure 2-19.

Technology		65-nm CMOS
Die area		0.24 mm^2
Power supply		1.2 V
Current consumption	max	3.2 mA
	min	2 mA
DC-gain		0 dB
f_c	ISDB-T mode	750 KHz
	DVB-H mode	3.8 MHz
Out-of-band IIP2	ISDB-T mode	57 dBm
	DVB-H mode	50.5 dBm
Tuning range		700 KHz–5.2 MHz
Tuning resolution		%3
Noise density		7.5 nV/sqrtHz
SFDR	ISDB-T mode	84 dB
	DVB-H mode	76.6 dB
DR (@HD3=40dB)	ISDB-T mode	92.7 dB
	DVB-H mode	85.5 dB
In-band IIP3	ISDB-T f_1=500KHz,f_2=600KHz	22.5 dBm
	DVB-H f_1=2.4MHz,f_2=2.8MHz	20 dBm
Out-of-band IIP3	ISDB-T f_1=2.4MHz,f_2=4.4MHz	36.5 dBm
	DVB-H f_1=5MHz,f_2=8MHz	31.5 dBm
In-band HD2 (420mVpp diff.)	ISDB-T(f=500KHz)	-57 dB
	DVB-H(f=1.2MHz)	-59 dB

Table 2-1 Performance summary of the proposed baseband pre-filter

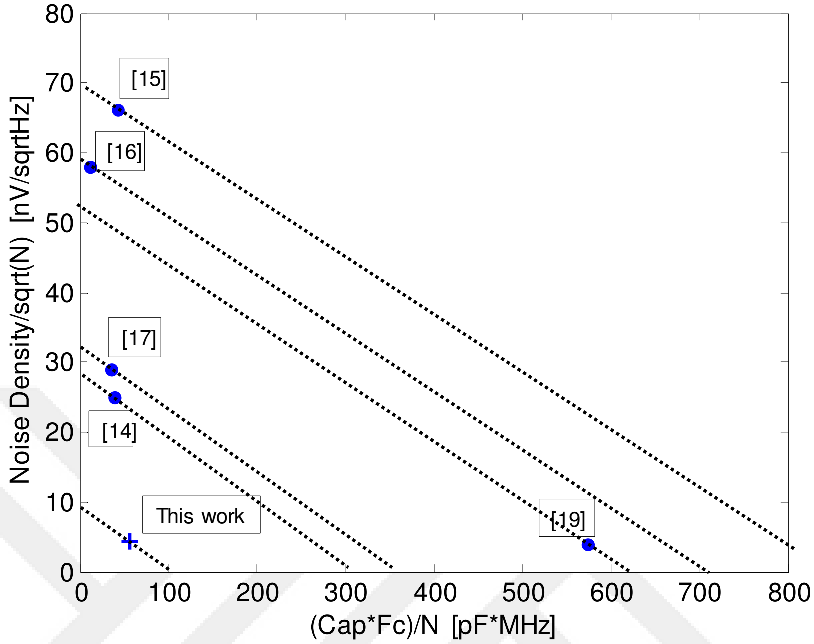


Figure 2-18 Literature comparison in terms of noise and required capacitance per pole

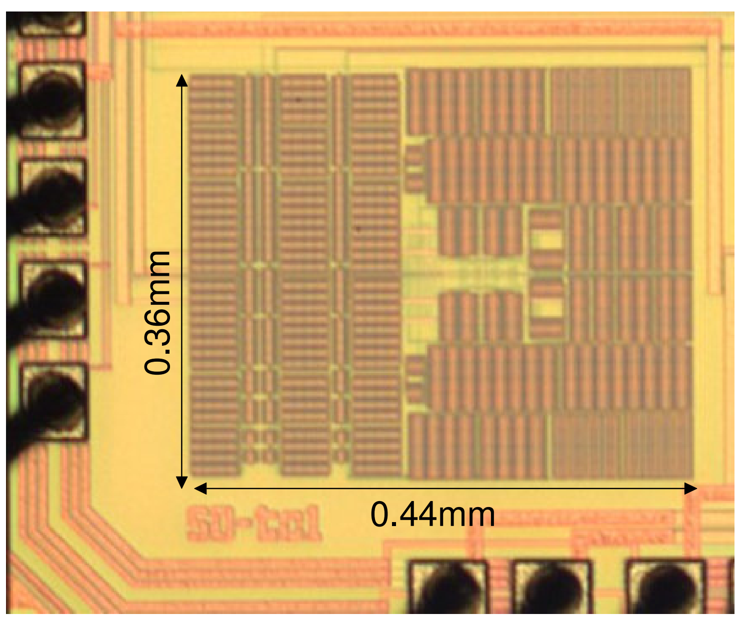


Figure 2-19 Die microphotograph of the design

3 A Low Noise Gain Stage with Noise Shaping Blocker Suppression

3.1 Introduction

In this chapter, a blocker aware gain stage is presented. The Asymmetric Floating Frequency Dependent Negative Resistance (AFFDNR) circuit in the feedback of an amplifier is introduced as a unique solution for providing gain in the signal band while simultaneously implementing a third-order low-pass elliptic response for the blocker signals [33]. Due to its noise shaping characteristics, the noise contribution due to the filtering action is insignificant.

In the design of a receiver chain, gain-filtering allocation along the chain is a significant task. The tradeoffs in terms of noise, area, and power are very sensitive to the choice of architecture. Some of the commonly used gain-filtering topologies, as well as the proposed approach are illustrated in Figure 3-1. A topology with a gain stage followed by a filtering can be more preferable choice for a better sensitivity, if the blocker levels in the adjacent channels are limited and noise is the main factor to consider (Figure 3-1 (a)). In the case of strong blockers however, such architecture may not be optimum, considering the linearity requirement of the amplifier. Even in the case of an interleaving architecture as shown in Figure 3-1 (c), the design of the first amplifier stage can be demanding. Thus, a filtering block might be required ahead of the gain stage as shown in Figure 3-1 (b). The filter noise should be kept minimal for such a topology, not to degrade the sensitivity from the noise point of view. The technique proposed in this chapter offers a solution with simultaneous gain and noise shaping filtering (Figure 3-1 (d)), namely amplification only in the band of interest. Low-noise amplification of only the desired signal is proposed against the classical approach of amplifying everything including the blockers and, then, trying to filter-out the blockers in the subsequent filtering stage. Avoiding the amplification of the blockers not only relaxes the linearity spec of the amplifier, but also relieves the filtering requirements of the following filtering stage.

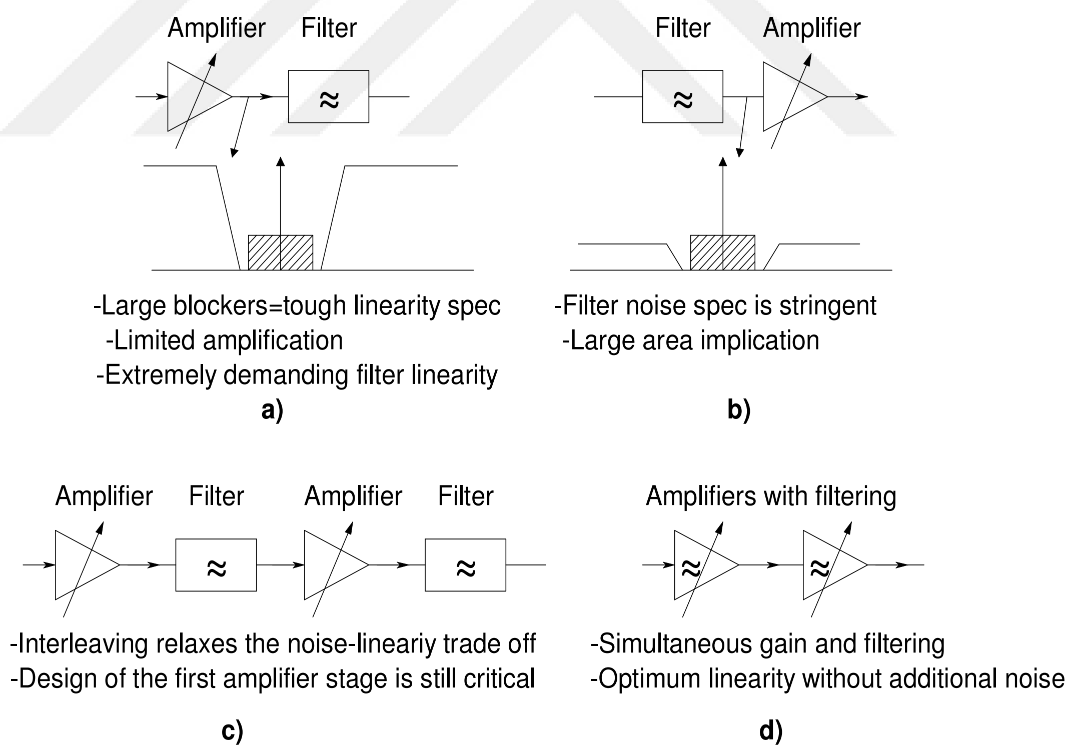


Figure 3-1 Various gain-filtering architectures: (a) Gain block ahead of filtering (b) Filtering before the gain stage (c) Interleaved gain and filtering (d) Simultaneous gain and filtering

The unique attribute of the proposed technique is that, noise of the AFFDNR circuit elements in the feedback path is shaped, and hence the desired third-order elliptic filtering obtained without any significant noise degradation. Employing the technique in the receive chain of a radio can enhance the overall performance of the radio, an improvement that can not be achieved using classical gain-filtering techniques unless area is sacrificed. Although it can be used for any application with a signal bandwidth in the range 700 KHz to 5 MHz, the 65 nm CMOS implementation targets the two mobile-TV applications mentioned in the previous chapter; Integrated Services Digital Broadcasting-Terrestrial (ISDB-T) and Digital Video Broadcasting – Handheld (DVB-H). The chapter is organized as follows: Section 3.2 introduces the AFFDNR concept in the feedback of an amplifier along with the resulting signal transfer function. As to prove the advantages of the concept, detailed noise analysis is carried on in Section 3.3. The class-AB opamp and the bandwidth calibration circuit are presented in Section 3.4. Some other circuit configurations utilizing the technique are presented in section 3.5. Section 3.6 presents the measurement results of a 65-nm CMOS proof-of-concept test-chip and Section 3.7 is Conclusion.

3.2 An AFFDNR Based Gain Stage

A new circuit topology based on the previously mentioned FDNR structure, the AFFDNR used in the feedback of a programmable gain amplifier (PGA), is shown in Figure 3-2. Figure 3-2 (a) shows an instrumentation topology with high input impedance, while Figure 3-2 (b) shows a fully differential implementation with finite input impedance. Two single-ended opamps are used in instrumentation topology, whereas, one fully-differential opamp with common mode feedback is used in the fully differential case.

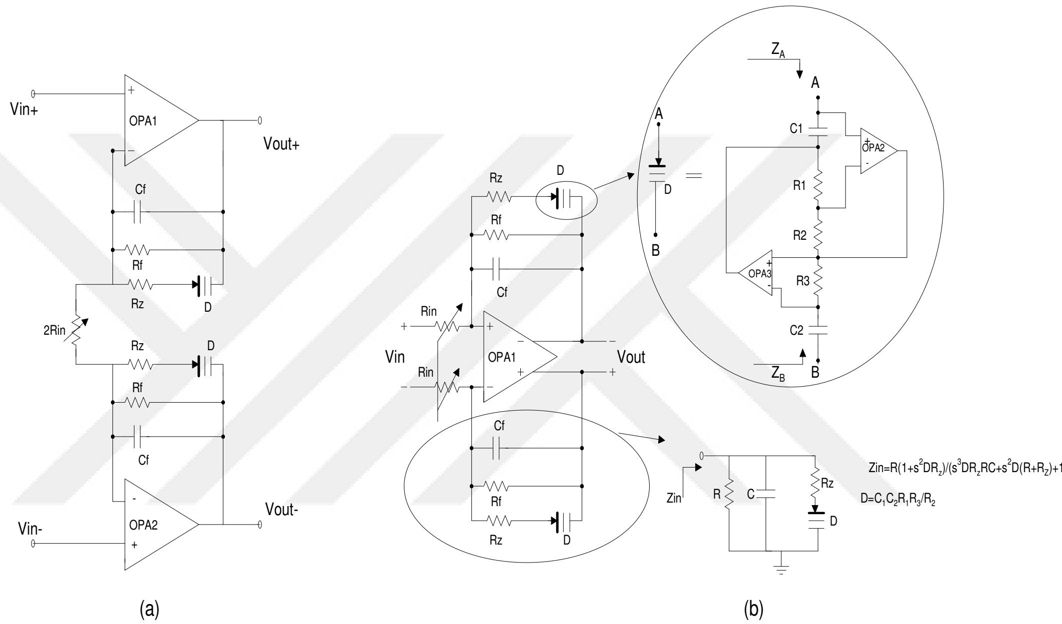


Figure 3-2 Amplifiers with AFFDNR feedback: (a) Instrumentation topology (b) Fully differential implementation

The PGA opamp input stage should be able to handle signal swing in the instrumentation topology, while in the fully differential case, the opamp inputs are at virtual ground and do not experience any voltage swing. The circuits are composed of the main PGA opamps that realize the gain with the use of the feedback resistance R_f and input resistance R_{in}. Although, linearity of such a system is relaxed, allowing larger gain in the amplifier, certain applications still require gain variability depending on the received signal strength. Input resistor Rin can be trimmed for PGA operation if gain variation is desired. The filtering stage is placed in the feedback path in parallel with R_f. R_f is incorporated into the filter transfer function and hence serves a dual function, providing gain and adding filtering. When the signal is applied to the input terminal, the feedback path with AFFDNR presents an impedance of R_f for the in-band signal whereas the blocker sees a short to the output. The blocker signals do not experience any gain in the signal path. Thus, the linearity spec of the amplifier is relaxed since the output can not see a large blocker voltage swing. More precisely, the signal in the desired channel of interest is amplified with third-order elliptic filter characteristic due to the proposed frequency selective feedback. It should be noted that the proposed AFFDNR is not a reciprocal circuit and the mentioned filtering action can only be obtained provided that the polarity is as shown in Figure 3-2 (b). Namely, the impedance looking into the node A, Z_A, is desired negative resistance whereas, the impedance looking into the node B, Z_B, is inductive when the opposing port is grounded for each of the cases. In this topology, the AFFDNR filter amplifiers are not in the signal path, so no additional DC offset or IQ imbalance is introduced as opposed to common amplifier-filter topologies.

Using KVL and KCL, the equation defining the relation between the input and output of this AFFDNR feedback circuit can be driven as:

$$\frac{V_{in}(s)\cdot R_f}{R_{in}} = \frac{(V_{out}(s)-V_{in}(s))\cdot(s^3 DR_z RC + s^2(DR_z + DR) + sRC + 1)}{s^2 DR_z + 1} = \left(V_{out}(s)-V_{in}(s)\right)\cdot F(s) \quad (3.1)$$

where, F(s) is the transmission function and

$$D = {C_1 C_2 R_1 R_3} / {R_2} . \tag{3.2}$$

Looking into the relation between input and output provided in (3.1), for the low frequency in-band signals, F(s) is unity and hence an in-band signal experiences expected non-inverting gain of $A_V = 1 + R_f / R_{in}$. The input-output relation around the notch frequency however yields an interesting case. One would expect a minimum gain of unity from this amplifier topology, worst case being the zero feedback impedance. Looking into the response of the amplifier around the notch frequency however, we can even observe some attenuation (Figure 3-5). The reason for this becomes clear once the F(s) in (3.1) is analyzed. Figure 3-3 shows the bode plot of the function F(s). The phase response reaches 180° very quickly, while the amplitude response is in the ramp-up and still has a relatively finite value. Such a finite magnitude with a negative sign corresponds to attenuation in the overall signal transfer function given in (3.1).

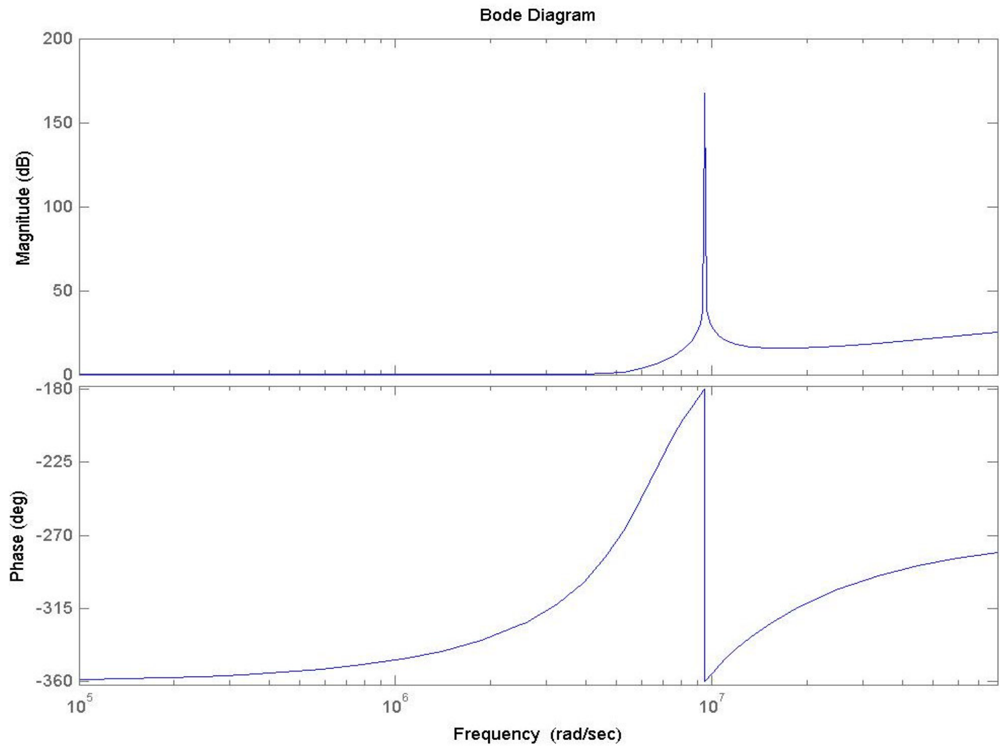


Figure 3-3 Bode plot for the function F(s) given in (3.1)

3.3 Noise Analysis

The detailed schematic of the simplified single-ended design including the noise sources is shown in Figure 3-4. The noise of the amplifier elements, the input resistance R_{in} and the feedback gain resistor R_f, remains the same and sets the noise floor for this topology. The noise of the AFFDNR filtering section elements (R_z, R_1, R_2, R_3, OPA1 and OPA2) is however shaped and does not contribute to the overall noise figure significantly. Thus, one can obtain a relative high order filtering without extra noise penalty. To explicitly demonstrate the noise shaping concept of the proposed circuit, the noise transfer functions from each of these contributors to the

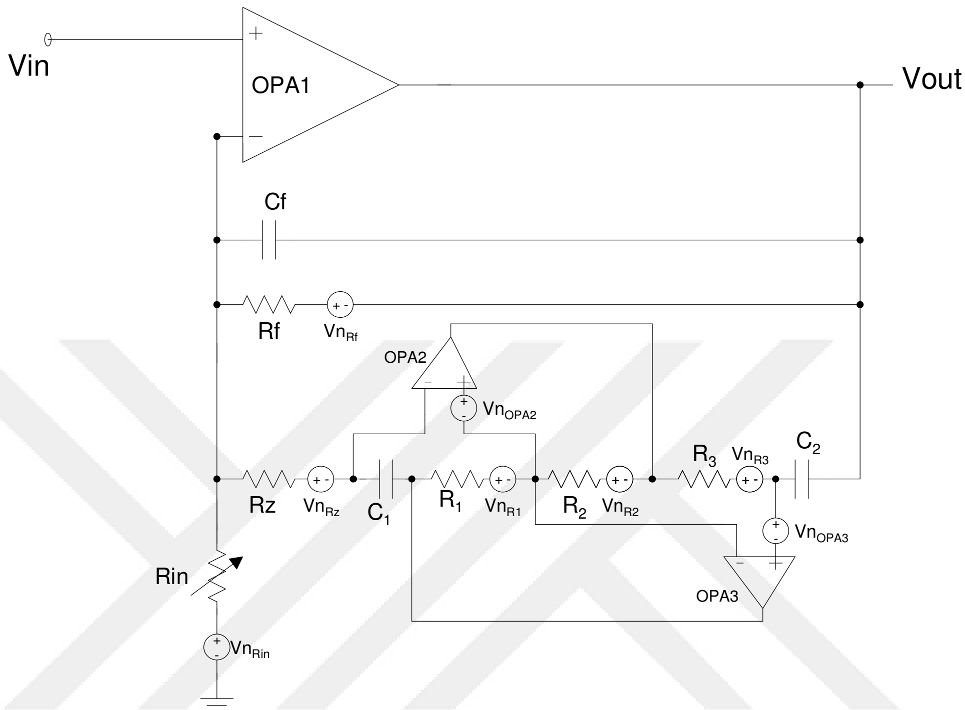


Figure 3-4 Schematic of a simplified single-ended circuit including the noise sources

output have been calculated and are as follows:

OPA2 noise transfer function:

$$\frac{V_{out}(s)}{Vn_{OPA2}(s)} = \frac{sC_1 R_f \left(1 - s\,R_1 R_3 C_2 / R_2\right)}{s^3 DR_z R_f C_f + s^2 \left(DR_z + DR_f\right) + s\left(R_f C_f\right) + 1} \tag{3.3}$$

OPA3 noise transfer function:

$$\frac{V_{out}(s)}{Vn_{OPA3}(s)} = \frac{sC_1 R_f R_1 \left(sR_3 C_2 + 1\right)}{R_2 (s^3 DR_z R_f C_f + s^2 \left(DR_z + DR_f\right) + s\left(R_f C_f\right) + 1)} \tag{3.4}$$

R_z noise transfer function:

$$\frac{V_{out}(s)}{Vn_{Rz}(s)} = \frac{s^2 DR_f}{s^3 DR_z R_f C_f + s^2 (DR_z + DR_f) + s(R_f C_f) + 1} \tag{3.5}$$

R_1 noise transfer function:

$$\frac{V_{out}(s)}{Vn_{R1}(s)} = \frac{sR_f C_1}{s^3 DR_z R_f C_f + s^2 (DR_z + DR_f) + s(R_f C_f) + 1} \tag{3.6}$$

R_2 noise transfer function:

$$\frac{V_{out}(s)}{Vn_{R2}(s)} = \frac{sR_1 R_f C_1}{R_2 (s^3 DR_z R_f C_f + s^2 (DR_z + DR_f) + s(R_f C_f) + 1)} \tag{3.7}$$

R_3 noise transfer function:

$$\frac{V_{out}(s)}{Vn_{R3}(s)} = \frac{sR_1 R_f C_1}{R_2 (s^3 DR_z R_f C_f + s^2 (DR_z + DR_f) + s(R_f C_f) + 1)} \tag{3.8}$$

Signal transfer function from input to output can be written down as follows:

$$\frac{V_{out}(s)}{V_{in}(s)} = 1 + \frac{R_f (s^2 DR_z + 1)}{R_{in} (s^3 DR_z R_f C_f + s^2 (DR_z + DR_f) + s(R_f C_f) + 1)} \tag{3.9}$$

Figure 3-5 shows the plots for the magnitude of these noise transfer functions as well as the signal transfer function.

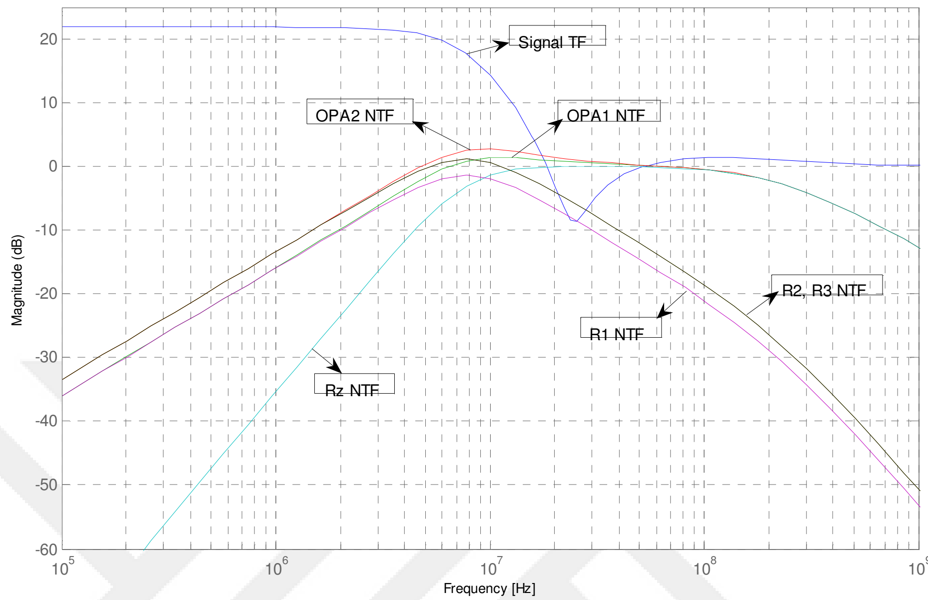


Figure 3-5 Signal and noise transfer functions showing the noise shaping

It is also possible to use the noise shaping characteristic of the proposed technique to reduce overall chip area. Since the noise generated by the AFFDNR resistors is shaped, this enables the designer to use larger resistors (noisier) and hence reduce the capacitor size. This approach can result in significant area saving for a particular noise level. As a mean of comparison, the total amount of capacitor required versus the desired in-band input referred noise level is plotted in Figure 3-6 for various third order filter topologies as well as the circuit topology described in this work.

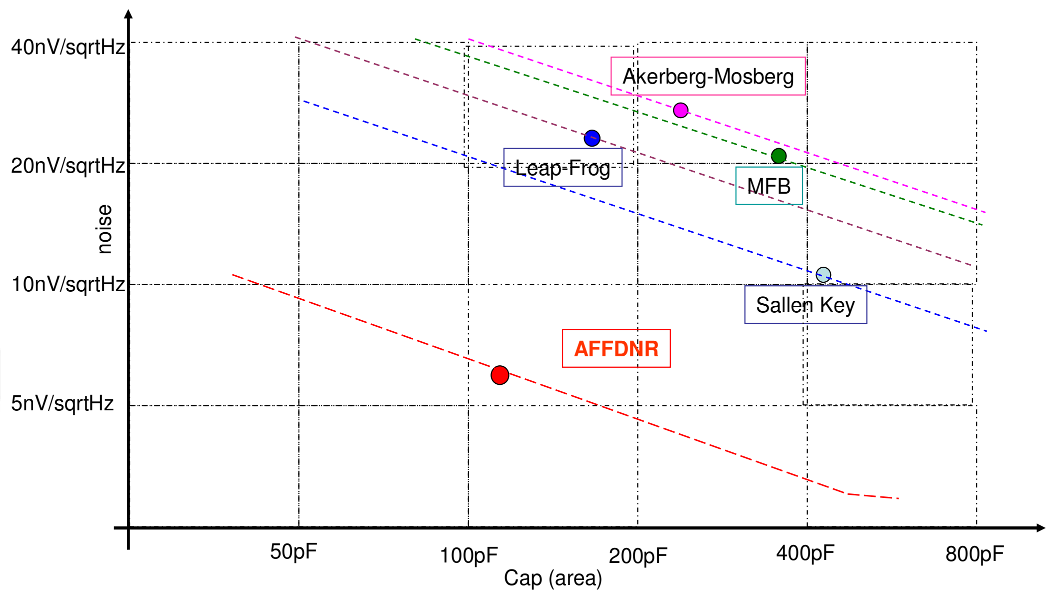


Figure 3-6 Desired noise level vs. required capacitor value for a range of filter topologies targeting the same cut-off frequency of around 3.5 MHz

3.4 Opamp and Bandwidth Calibration Circuit

The class-AB opamp and bandwidth calibration circuit that are presented in Chapter 2 were reused modifying the compensation network depending on the load requirement of this particular configuration. The OPA2 has the most demanding spec in terms of and hence the required compensation yields the worst unity-gain-bandwidth for this opamp. This worst case opamp achieves a unity-gain-bandwidth greater than 160-MHz, consuming 500 µA from a 1.2 V supply with a phase margin of 53°.

3.5 Other AFFDNR Circuit Topologies

The basic feedback AFFDNR idea can also be applied to other feedback circuits. Figure 3-8 shows some of the unique configurations that can be obtained. A fully differential topology shown in Figure 3-7 (a) takes advantage of the input resistance of the amplifier, Rin, and an AFFDNR to realize a high order cascade system. In this topology, the blockers are pre-filtered even before reaching the feedback path in the amplifier. Thus, such a system can handle even larger blockers without additional noisy element. Figure 3-7 (b) shows a cascade instrumentation topology using the load resistance of the proceeding stage, R_{Lpre}, again requiring no additional noisy elements.

The cascade topologies provide a unique advantage regarding to the blocker performance. In the case of a cascade instrumentation topology for example, not only the linearity of the gain stage, but also the linearity of the driving stage is relaxed, allowing more gain in the driver stage. More gain in the preceding stage implies less noise contribution from the following stages. Thus, power and area specs are also relaxed for the gain stage.

3.6 Measurement Results

A differential instrumentation stage covering a frequency range from 700-KHz to 4.2-MHz is fabricated in a 65-nm CMOS process and tested. The cut-off, notch and stop-band characteristics can independently be set to satisfy the blocker and noise requirements of various applications across the band with a 7-bit control word corresponding to a tuning resolution of 20-KHz. The design consumes a die area of 0.12 mm^2 and the total power consumption is in the range of 3-mA to 4.8-mA from a 1.2-V supply depending on the received signal strength. Figure 3-8 (a) shows various amplifier transfer function curves corresponding to different trim codes across the band.

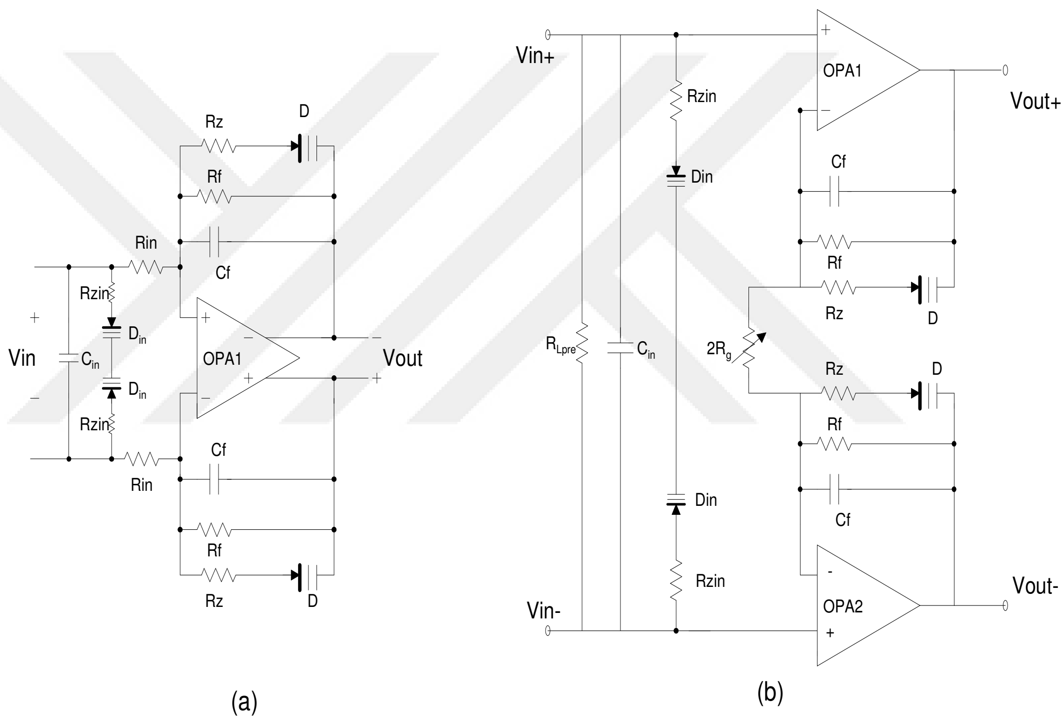


Figure 3-7 (a) Fully differential cascade topology (b) Cascade instrumentation topology

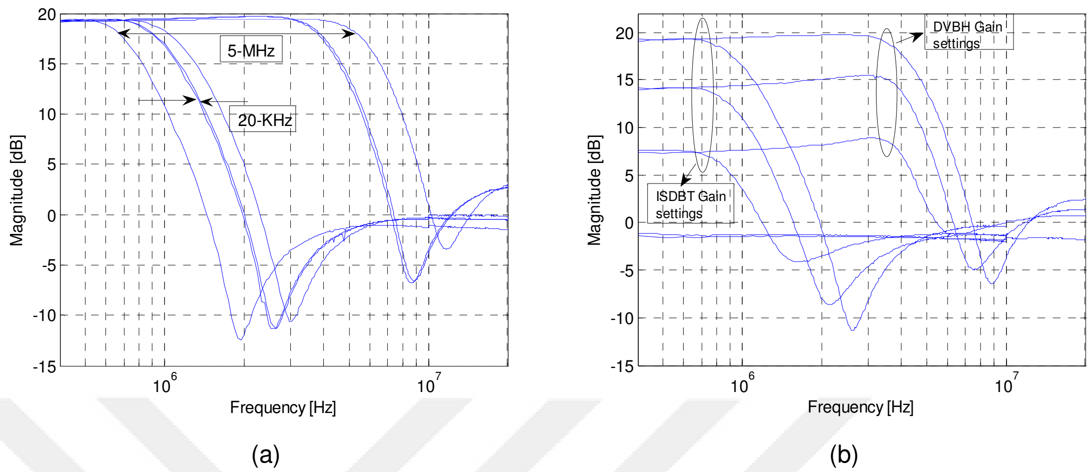
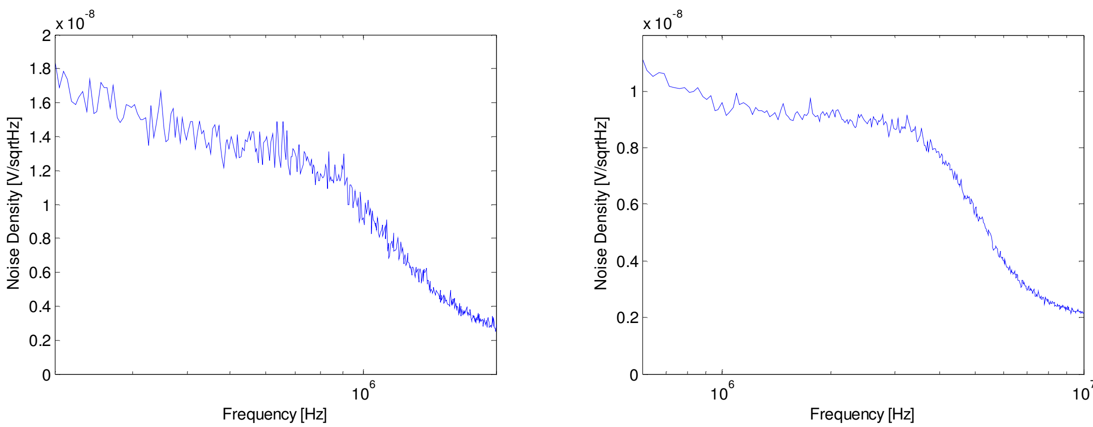


Figure 3-8 (a) Measured amplifier bandwidth characteristics across the band (b) Amplifier response for various gain settings in ISDB-T and DVB-H modes

The testing and characterization is done for ISDB-T and DVB-H, with signal bandwidths being 750-KHz and 3.8-MHz, respectively. The radio chain employing the circuit requires that IM3 levels resulting from -3.5 dBm N+1 blockers are below -70 dBc and -60 dBc for ISDB-T and DVB-H modes, respectively. The input referred noise requirements are 12 nV/sqrtHz and 9 nV/sqrtHz for ISDB-T and DVB-H modes, respectively. The transfer characteristics with various gain steps corresponding to these target applications are shown in Figure 3-8 (b). In ISDBT mode, the signal cut-off is around 750-KHz whereas the N+1 blocker is centered around 2.5-MHz. In DVBH mode, the signal bandwidth is around 3.8-MHz whereas the N+1 blocker power can occur in the next 8–MHz bandwidth. The optimum case for the DVBH has a slight peaking in the filter response, since the notch frequency is set to be relatively close to filter cut-off.

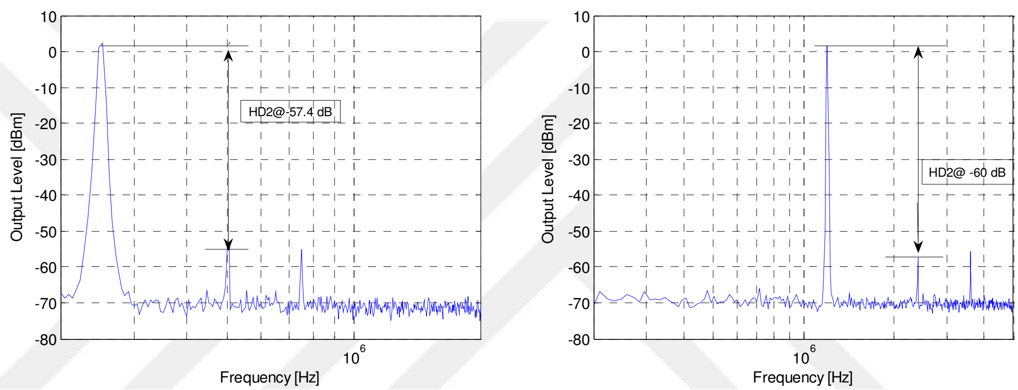
Regarding the noise budget allocation, setting the noise contribution of the AFFDNR and of the gain amplifier is not the optimum choice since the power is more of a concern in the amplifier design. An optimum design strategy for the target design was to allocate most of the in-band noise budget to the amplifier to reduce its power consumption and limiting the FDNR contributions. The noise characteristics of the filter for these target bands are shown in Figure 3-9. Figure 3-9 (a) shows the noise in ISDB-T mode whereas Figure 3-9 (b) shows the noise in DVB-H mode. It can be observed from these plots that the shaped AFFDNR contribution becomes dominant only at the edge of the band. The measured noise density in the signal band is around 9.5 nV/sqrtHz in DVBH mode and 14 nV/sqrtHz in the ISDBT mode. Total capacitance required in the design corresponding to these noise levels was 120 pF.



(a) (b)

Figure 3-9 (a) Total input referred noise measured: (a) In ISDB-T mode (b) In DVB-H mode

As regard to linearity, HD tests and two-tone IM3 tests were conducted for the both target modes. Figure 3-10 (a) shows that a 250-KHz 750-mVpp differential tone at the output in ISDB-T mode results in -57.4-dB HD2 and -58.9-dB HD3. In DVB-H mode A 1.2-MHz 750-mVpp differential tone at the output yields -60-dB HD2 and -57-dB HD3 (Figure 3-10 (b)).



(a) (b)

Figure 3-10 In-band distortion levels measured: (a) In ISDB-T mode (b) In DVB-H mode

In ISDB-T mode, 2.25-MHz and 3.75-MHz blockers (420-mVpp differential each) result in -78-dBm IM3 at the output which corresponds to an out-of-band IIP3 of 37dBm (Figure 3-11 (a)). In DVB-H mode, 7-MHz and 11-MHz blockers (420-mVpp differential each) result in -65.6-dBm IM3 at the output which corresponds to an out-of-band IIP3 of 29.7 dBm (Figure 3-11 (b)). In Figure 3-12, measured IIP3 interpolation plots are presented for the both target bands. Moreover, the tones are swept across the blocker band recording the IIP3 for each of these cases. The plots showing IIP3 with varying average two-tone frequency are shown in Figure 3-13.

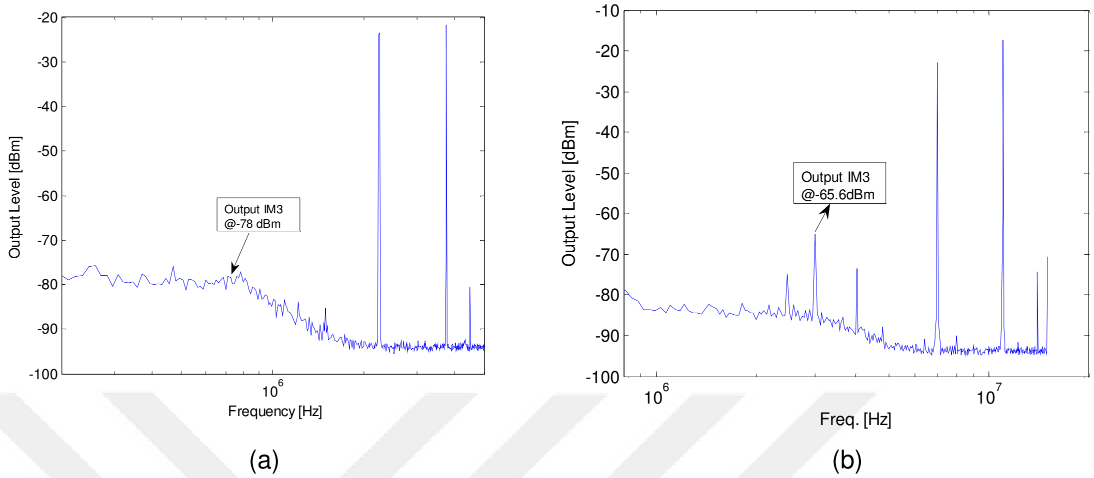


Figure 3-11 Two-tone tests: (a) Output spectrum for 240-mVpp diff. each, 2.25-MHz and 3.75-MHz input blockers in ISDB-T mode (b) Output spectrum for 240-mVpp diff. each, 7-MHz and 11-MHz input blockers in DVB-H mode

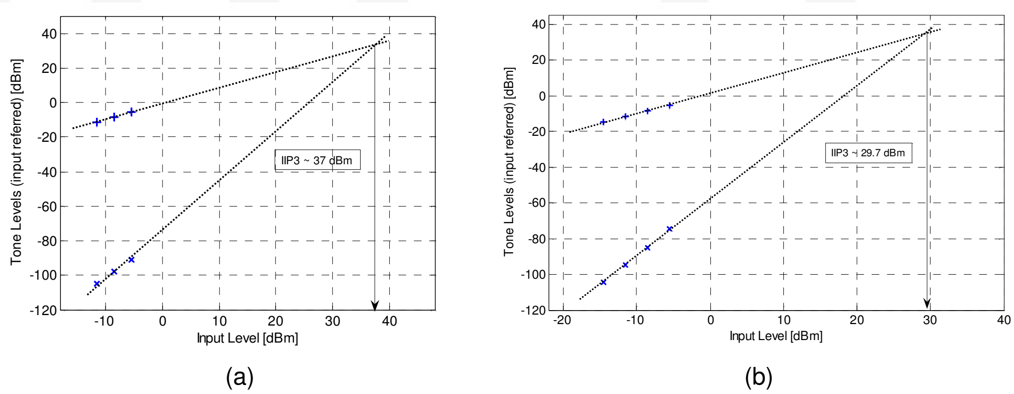


Figure 3-12 Measured IIP3: (a) in ISDB-T mode (b) in DVB-H mode

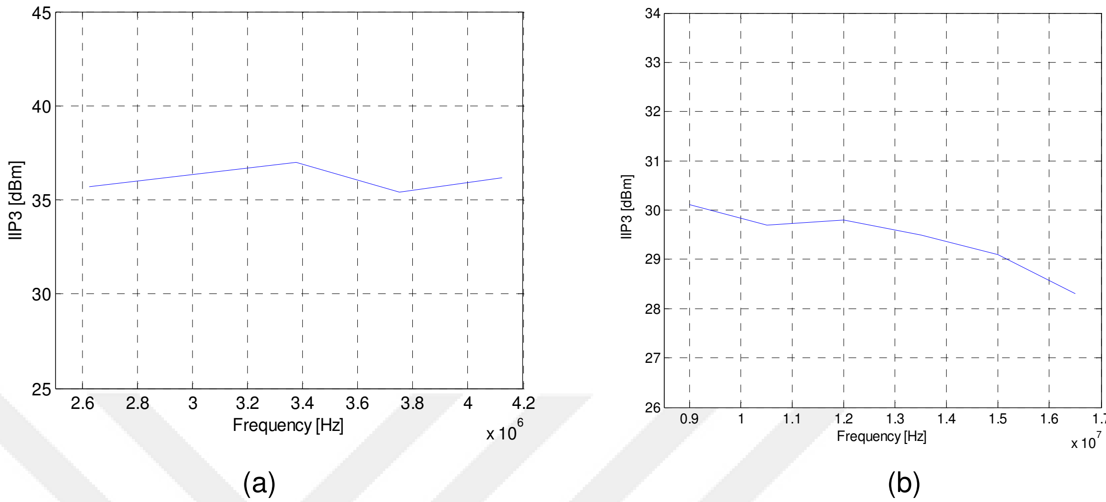


Figure 3-13 IIP3 across the blocker band: (a) in ISDB-T mode (b) in DVB-H mode

3.7 Conclusion

A gain block with high order noise shaping filtering is introduced. The feedback AFFDNR topology described can provide a relative third-order elliptic transfer function with a minimal noise and area penalty. Hence, such a technique, providing gain only in the band of interest, can enhance the sensitivity of a receiver chain significantly, particularly in an environment where strong blockers can coexist. A proof-of-concept test chip with a differential instrumentation topology was fabricated and tested in a 65-nm CMOS process. Performance metrics of this test circuit are summarized in Table 1. The die picture is shown in Figure 3-14.

Technology		65-nm CMOS
Die area		0.13 mm^2
Power supply		1.2 V
Current consumption	max	4.8 mA
	min	3 mA
Gain settings		20-15-8-0 dB
f_c	ISDB-T mode	750 KHz
	DVB-H mode	3.8 MHz
Out-of-band IIP2	ISDB-T mode	75 dB
	DVB-H mode	65.5 Db
Tuning range		700 KHz–4.2 MHz
Tuning resolution		%3
Noise density	ISDB-T mode	14nV/sqrtHz
	DVB-H mode	9.5nV/sqrtHz
DR (@HD3=40dB)	ISDB-T mode	87.6dB
	DVB-H mode	83.3 dB
Out-of-band IIP3	ISDB-T f_1=2.25MHz,f_2=3.75MHz	37 dBm
	DVB-H f_1=7MHz,f_2=11MHz	29.7 dBm
HD2 (750mVpp diff.)	ISDB-T(f=500KHz)	-57.4 dB
	DVB-H(f=1.2MHz)	-60.5 dB
Total cap size		120 pF

Table 3-1 Performance summary of the proposed baseband PMA

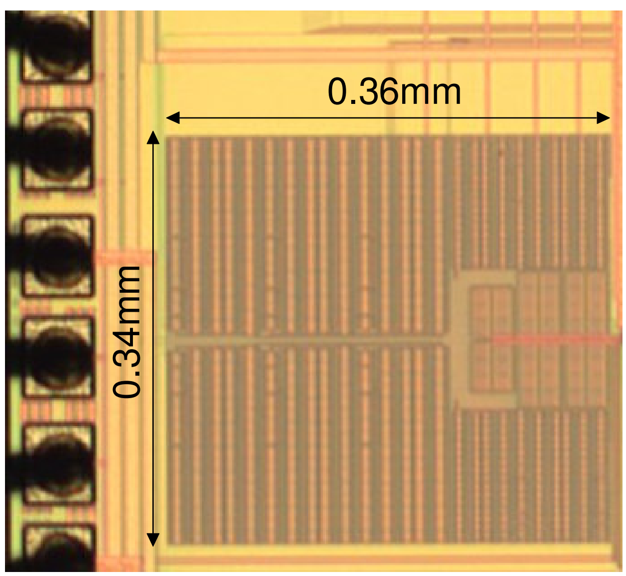


Figure 3-14 Die microphotograph of the PMA

4 A Differential Ramp Based 65 dB-Linear VGA technique

4.1 Introduction

In this chapter, a differential-ramp based Variable Gain Amplifier (VGA) technique is introduced. Using the proposed technique, digitally programmable gain amplifiers (PGAs) can be converted to analog controlled, dB-linear VGAs with minimum impact on noise and linearity. This provides an efficient way of realizing an analog controlled VGA for OFDM based applications. The technique is illustrated by converting an opamp based high-linearity, low-noise PGA to a dB-linear VGA for CMOS mobile TV applications. The design including the cascade of a two-stage continuous 65-dB-linear VGA and a third-order Sallen-Key buffer stage is fabricated in a 65-nm CMOS process.

VGAs are critical building blocks of wireless receivers. Since the received signal strength can vary significantly at the receiver input, the system response has to provide fine gain variation in order to maximize the dynamic range of the receiver [34]. The VGA gain curve should not deviate from the nominal case significantly with process variations. PGAs with fine programmable gain steps have proven to be a good solution in terms of noise and linearity in CMOS processes [35-36]. In most of such PGAs, the gain is determined by a resistor ratio and a dB-linear characteristic is simply obtained by switching in corresponding amount of resistance. Most of the

OFDM-based applications however, demand accurate continuous gain control without any glitches [37-38]. In most of such receiver systems, in order to maintain constant settling time in the Automatic Gain Control (AGC) block, a dB-linear VGA gain characteristic is required. Large input signal handling capability is another important criterion in VGA design. Designs need to maintain good linearity across the whole gain range and DC offset cancellation needs to be addressed, particularly at the high gain settings.

The block diagram of the universal CMOS integrated direct conversion radio baseband requiring a 65-dB gain range dB-linear VGA is shown in Figure 4-1. The main application for this receiver IC is in mobile-TV tuners, specifically Integrated Services Digital Broadcasting-Terrestrial (ISDB-T) and Digital Video Broadcasting – Handheld (DVB-H) standards with signal bandwidth requirements of 750-KHz and 3.8-MHz, respectively. The 20-dB programmable gain (PGA) ahead of VGA relaxes the noise budget of the VGA to 13 nV/sqrtHz. The target VGA needs to be able to provide 48-dB flat gain up to 5-MHz signal bandwidth to satisfy the requirements of the applications. The OIP3 spec is 22 dBm for the highest gain setting and additional filtering is desirable in the VGA to relax the anti-aliasing requirements of the following data converter block. Moreover, the VGA has to be able to handle the full-swing input signal of 2-Vpp differential.

In order to clarify the trade-offs, and be able to propose an optimum circuit technique for the target VGA, classical VGA techniques are briefly discussed in Section 4.2. A new differential-ramp based VGA technique is introduced in Section

4.3. Detailed circuits of the proposed VGA as well as the following third-order Class-AB Sallen-Key buffer are presented in Section 4.4. The measurement results of a 65-nm CMOS test-chip are presented in Section 4.5. The conclusions are presented in Section 4.6.

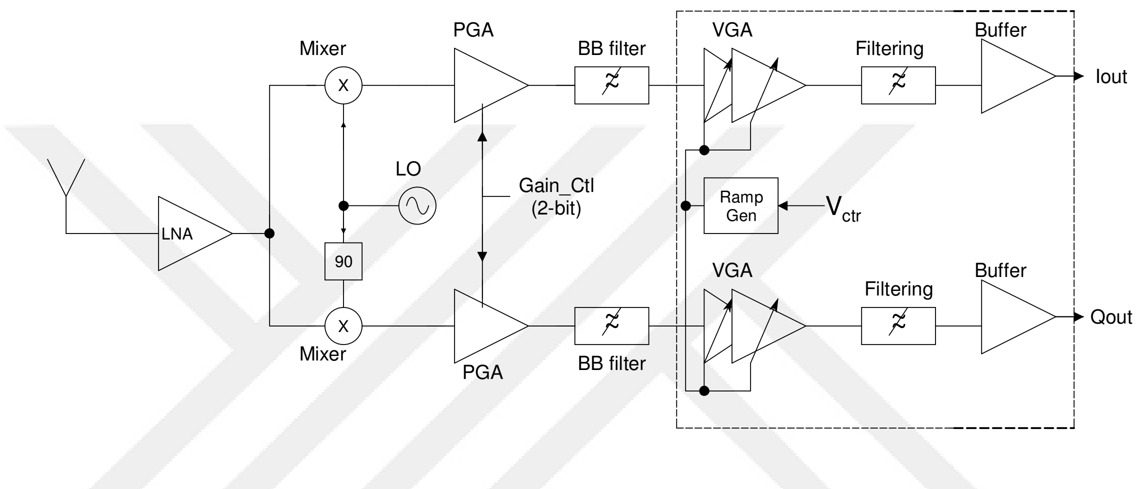


Figure 4-1 A universal DCR for mobile-TV applications showing the proposed VGA in the baseband chain

4.2 Classical VGA Techniques

There is a large variety of dB-linear VGA techniques reported in the literature [39-45]. A basic transconductance-based VGA technique is depicted in Figure 4-2 (a). A MOS device used in triode region controls the transconductance of the differential pair. Applying an exponentially-scaled control voltage to the control node results in dB-linear VGA operation. Although very simple to implement, the technique has many disadvantages. First, the control voltage range is very limited, particularly in the case where there is a large signal swing at the input. Moreover, the circuit suffers from poor linearity which becomes even more pronounced with mismatch of the differential pair devices.

Current steering type VGAs with an exponential control voltage circuit comprise another popular VGA technique [39]. This technique is illustrated in Figure 4-2 (b) and Figure 4-2 (c). Because of the square law MOS device characteristics, again an exponential control voltage conversion is required. The disadvantages of this technique

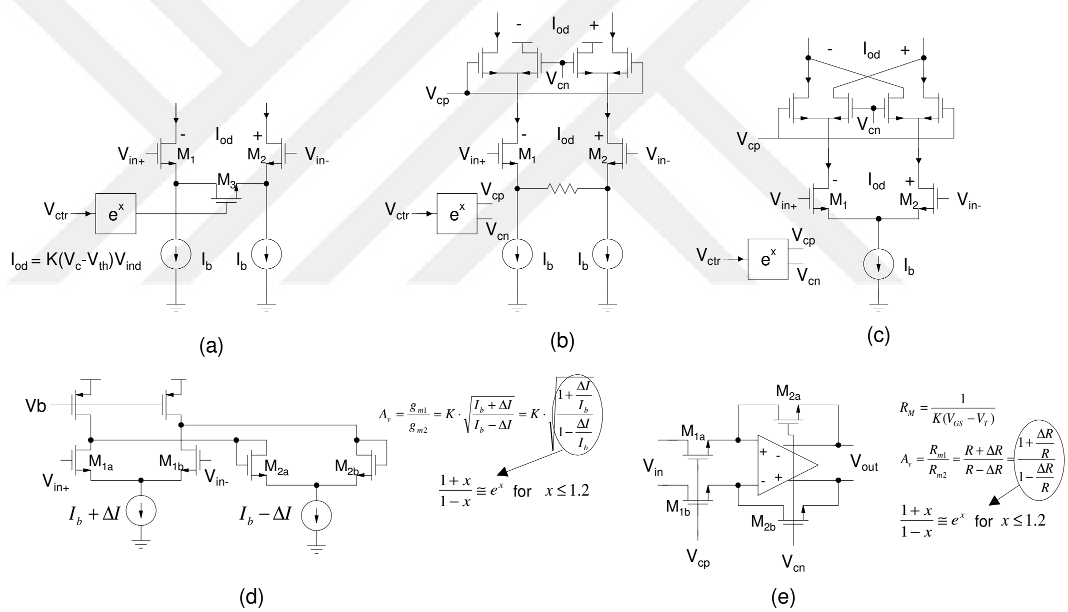


Figure 4-2 Various VGA topologies: (a) Transconductance tuning (b) Current steering (c) Differential current steering (d) Transconductance ratio (e) Feedback tuning

are linearity degradation due to large input signal swing and excess variation of DC offsets for various gain settings. Moreover, any noise on the control voltage creates an amplified noise current flowing to the output node.

Operating the MOS devices in sub-threshold region yields exponential characteristics and eliminates the need for exponential converter circuit [40-41]. However, the noise contribution of these devices may become prohibitively large in low noise applications.

References [42-45] propose a pseudo-exponential model for approximating the exponential gain control mechanism. The basic concept for one of these approximation techniques is illustrated in Figure 4-2 (d). Here, the resultant gain is given by the transconductance ratio and can be controlled by varying the currents of the transconductance stages. It should be noted that the exponential approximation term is under the square root and hence the resultant exponential gain range over which the approximation useful is limited to 12 dB per stage. Thus, in order to obtain a gain range of 60 dB, a VGA based on this technique would require 5 cascaded gain stages. This may not be an issue for very high speed applications where cascading is required to achieve the needed bandwidth, but, may not be an acceptable approach for DCR baseband applications. The linearity demand for the g_m stages in large signal conditions is another drawback of this technique. Moreover, since the output impedance is dominated by $1/g_{m2}$, the amplifier bandwidth does not stay constant as the gain of the stage is increased.

Another topology shown in Figure 4-2 (e) eliminates the linearity degradation caused by large signal swing at the inputs of the diff-pair which is the critical case for most of the topologies that are discussed above. Employing a high gain amplifier in a differential feedback network leaves the amplifier inputs in virtual ground configuration and hence improves the non-linearity of the amplifier itself. However, using MOS devices in triode region in the feedback network is itself a significant source of nonlinearity. Regarding the exponential gain characteristic, again the input MOS resistance R_{m1} and the output resistance R_{m2} can be varied in opposite directions to approximate an exponential dependence on the control voltage. The gain per stage that can be obtained without exceeding the approximation boundary this time is ~24 dB. Another disadvantage of the technique is that, this gain range corresponds to a very limited control voltage range. Hence, the two drawbacks of the technique remain as a limited control range and the non-linearity of the MOS resistors.

4.3 Voltage-Ramp Based VGA Technique

The technique proposed in this work realizes a unique solution to the drawbacks of the last technique (feedback tuning) discussed above, making it an attractive choice for the target 1.2-V receiver baseband application. This is done by introducing a multiple-ramp controlled, gradually changing feedback network [46]. The cost is additional voltage-ramp circuitry which leads to a slight increase in area and power.

Figure 4-3 (a) shows a unit segment that is used to construct the target structure. Here, if we choose R_1 and R_2 such that $R_2 >> R_1$ and $R_1 >> R_M$ then, the non-linearity introduced by the switch becomes insignificant when the switch is fully on. The only nonlinear region of the switch is when the switch is not fully on or fully off. By shrinking the range Δ (Figure 4-3 (b)), we can further reduce this nonlinear range.

Combining many of these small range unit elements in parallel, we can construct a highly-linear wide-range trim mechanism as shown in Figure 4-4.

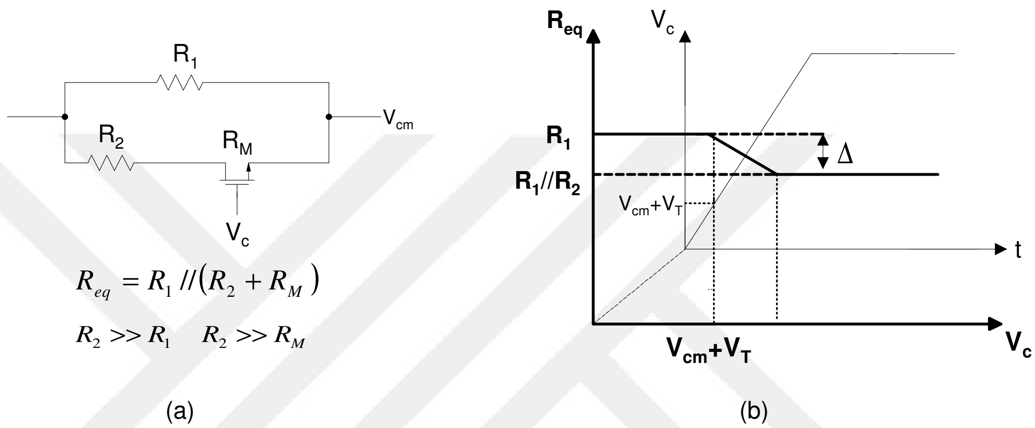


Figure 4-3 (a) Unit element for the proposed technique (b) Variation of the equivalent resistance with the control ramp voltage

The question then becomes how many unit elements can suffice to achieve the desired linearity level. For this reason, the basic tradeoffs in dividing the total range into such small pieces are pointed out in Figure 4-5. Once the number of ramps to be used is set, the resistor values can be computed to fit the exponential approximation range (~25 dB per stage). The schematic of a fully differential stage with complementary control ramps is shown in Figure 4-6.

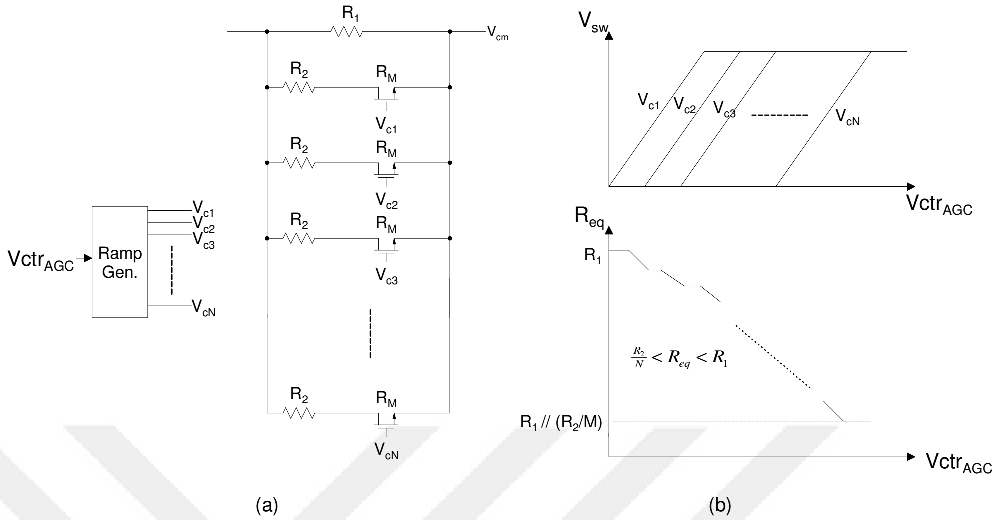


Figure 4-4 (a) Multiple unit elements combined in parallel (b) Variation of the equivalent resistance with the AGC control voltage

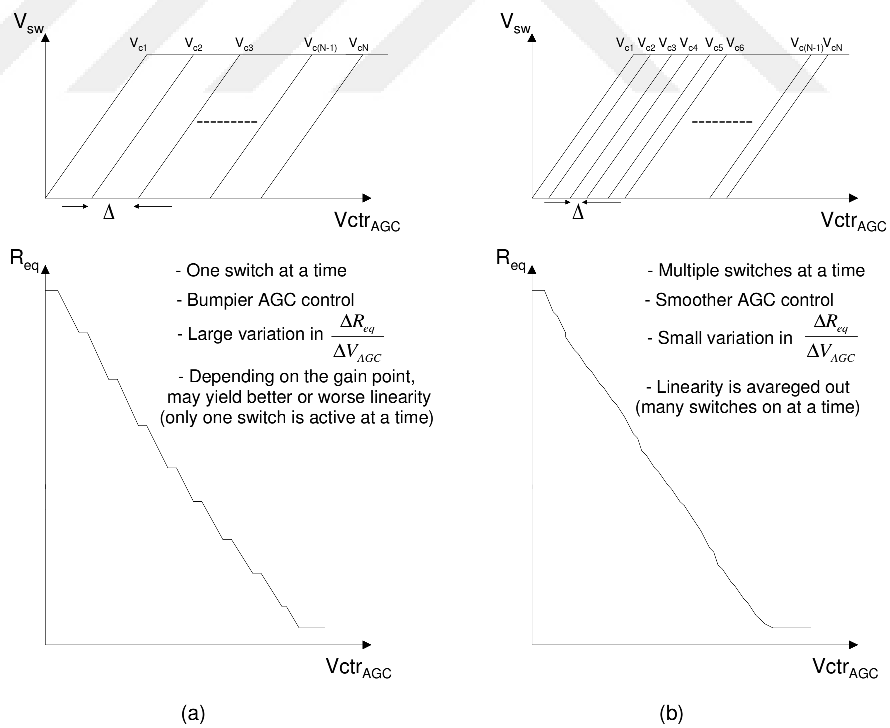


Figure 4-5 (a) The case with single switch "ON" at a time (b) The case with multiple switches "ON" at a time

It is important to mention that in order to obtain exponential characteristic, we needed differential ramp operation. Thus, with increasing AGC control voltage, the control voltages of the input resistors ramp up, while the control voltages on the feedback resistors ramp down, increasing the closed loop amplifier gain exponentially. Using the technique, a two stage 65-dB linear-in-dB VGA with continuous analog tuning was designed with a comparable linearity and noise performance relative to the PGA implementation of the same circuit. The noise and linearity metrics for these two cases are shown in Table 4-1.

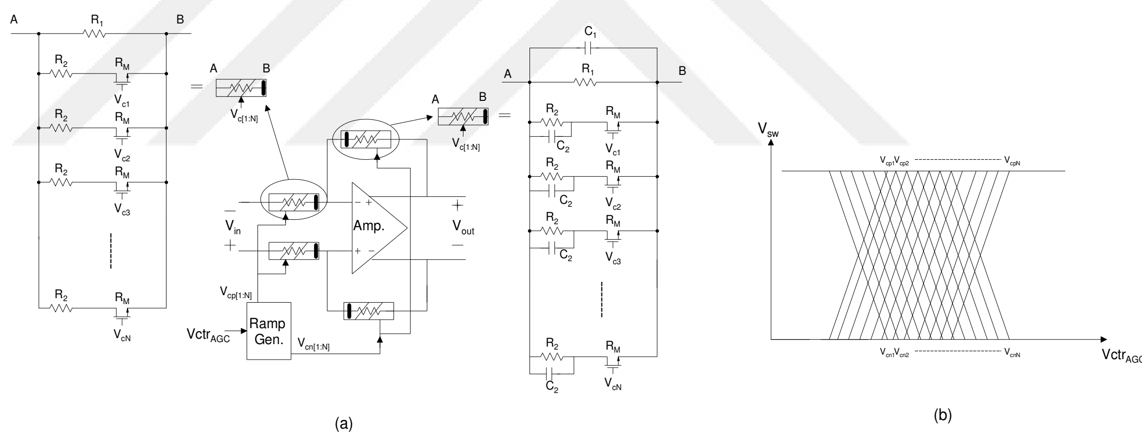


Figure 4-6 (a) Schematic of the proposed fully differential ramp-based VGA stage (b) Differential ramp control voltages vs. AGC control voltage

Feature	PGA (Simulated)	VGA (Simulated)	VGA (Measured)
Noise [nV/sqrtHz]	9.6	9.68	11
OIP_3 [dBm]	25.1	25	22
Gain Step [dB]	1 dB	Cont.	Cont.
Gain Range [dB]	-18 to 48	-18 to 48	-18 to 47
Power [mW]	1.8	2.3	2.23

Table 4-1 Performance comparison of the PGA and the proposed VGA implementation of it

4.4 Circuit Design

The circuit schematic of the chain including the two-stage VGA and the third-order Sallen-Key buffer is shown in Figure 4-7. The gain of each VGA stage is in the range –9 dB to 24 dB. Thus, the total target gain of this two-stage VGA varies from -18 dB to 48 dB. Each stage has a passive pole to provide additional filtering. These two poles as well as the following three poles in the Sallen-Key output buffer can be tuned from 700 KHz to 5 MHz to cover multiple applications. In order to keep the bandwidth constant while the resistor networks are switched a corresponding amount of capacitance is also switched by the ramp control voltages (Figure 4-6 (a)). The same gain control ramps can also be used for continuous adjustment of the compensation network of the amplifier. Thus, unity gain bandwidth of the amplifier is accurately adjusted tracking the desired gain level without sacrificing any phase margin.

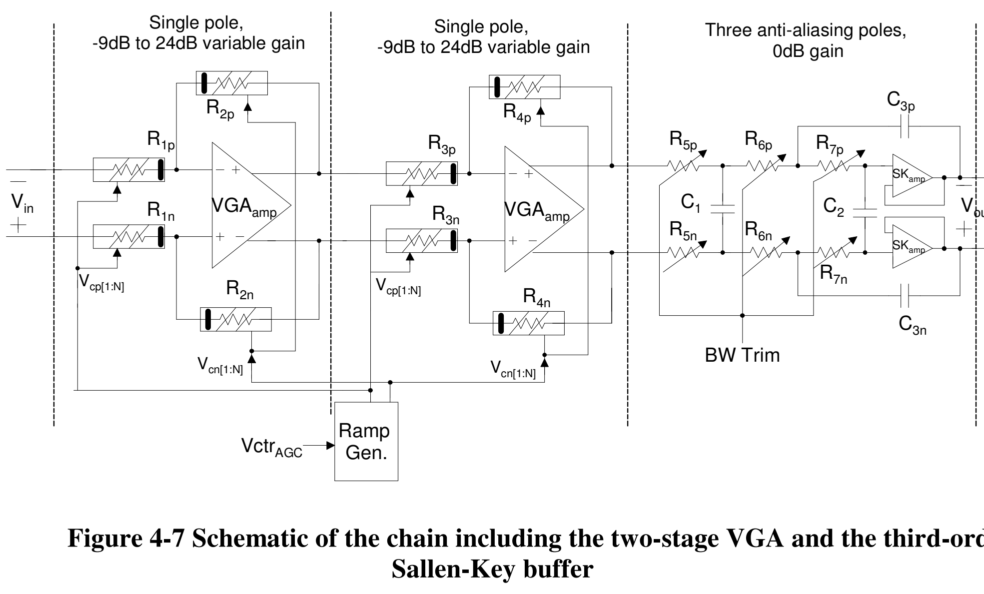


Figure 4-7 Schematic of the chain including the two-stage VGA and the third-order Sallen-Key buffer

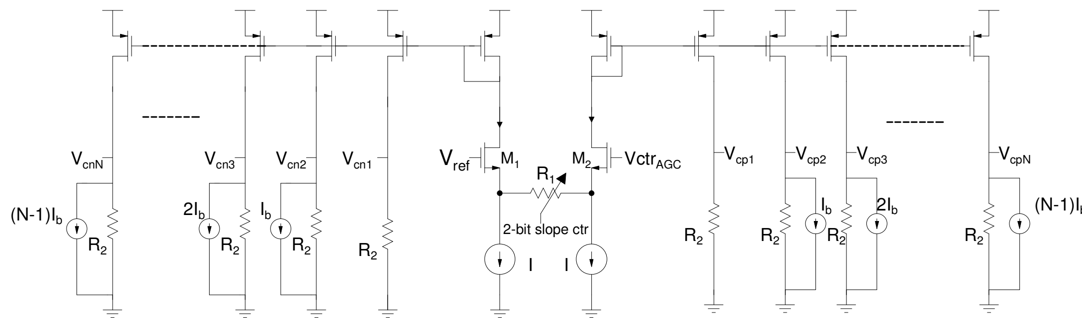


Figure 4-8 Schematic of the differential ramp voltage circuit

The differential ramp voltage generation circuit is shown in Figure 4-8. The input AGC control voltage is compared with a reference voltage Vref and the difference current running through R_1 causes the current in one of the diode connected devices increase while the current through the other one decreases. By mirroring this current into a resistor, a control voltage proportional to the input voltage difference can be obtained. Multiple control voltages with desired amount of offset can be obtained by simply pulling fixed amount of offset current from each of these mirrored branches. The ramp voltage V_{cpN}, for example, can be written down as follows:

$$V_{cpN} = \left(Vctr_{AGC} - V_{ref}\right)\frac{R_2}{R_1} - \left((N-1)I_b\right)\cdot R_2 \,. \tag{4.1}$$

The resistor ratio in the first term, (R_2 /R_1), defines the slope of the characteristics, whereas the second term is the fixed offset. In order to have flexibility in the design, R_1 is trimmable with a two–bit slope control word enabling us to adjust the slope of the control ramps and hence the VGA characteristics. Figure 4-9 shows the VGA gain characteristics obtained by dividing control voltage range over 5, 10 and 20 control ramps. The case of 20 control ramps results in a very accurate and smooth gain curve. The simulated gain curves for the worst process corners for this case are shown in Figure 4-10. The number of ramps for the target mobile TV application however, was chosen to be 10 since the improvements obtained by moving to 20 ramps are not substantial to justify the area cost. For a 10-ramp design the current consumption of the ramp generation circuit is 200 μA from a 2.5-V supply. This circuit works from 2.5-V providing the control voltages for the switches (thick-oxide devices). The switches with 2.5-V gate drive can allow larger signal swing without significant linearity degradation.

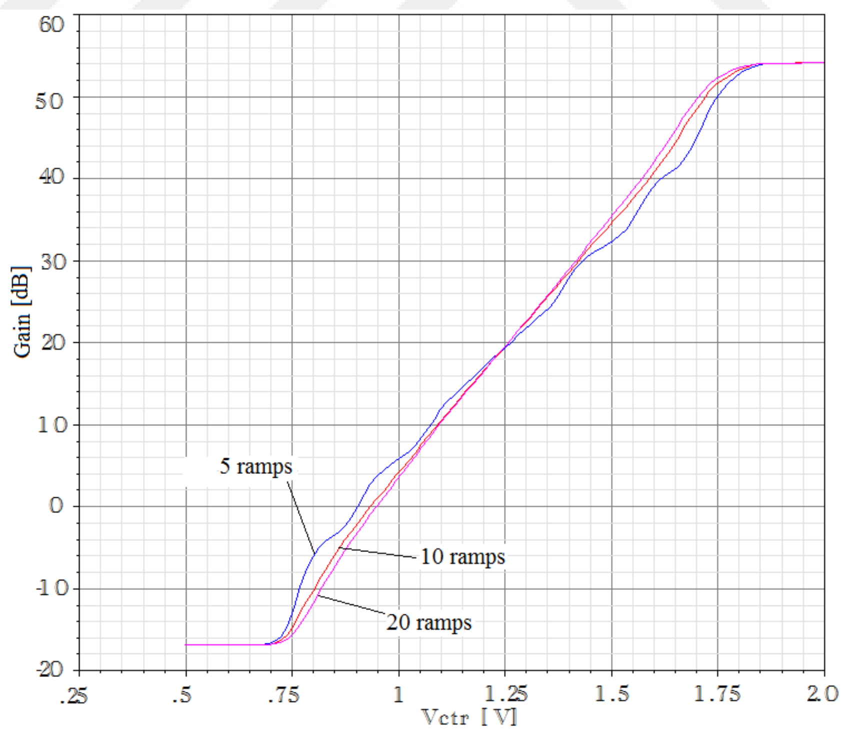


Figure 4-9 VGA gain for various ramp counts

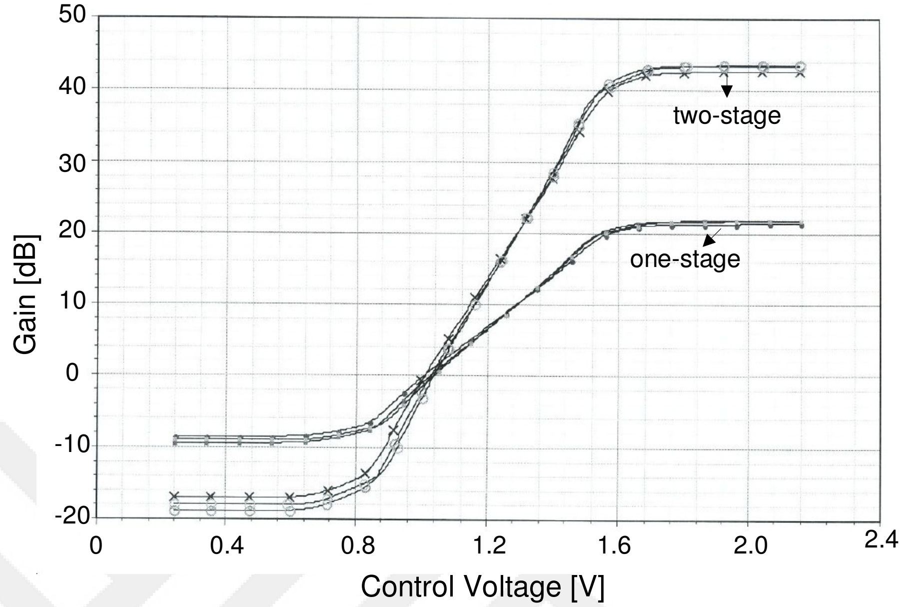
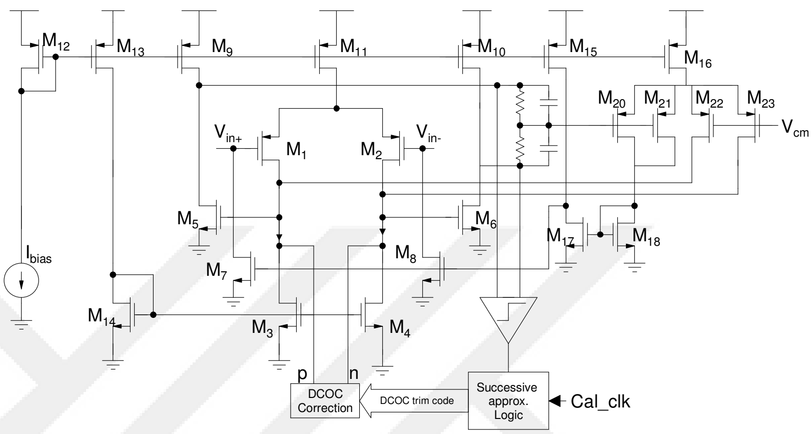
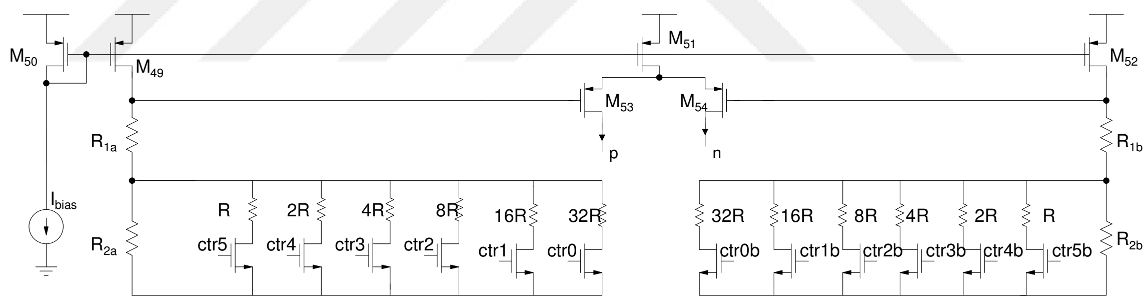


Figure 4-10 Simulated 20-ramp VGA characteristics across the process corners

The fully differential class-A VGA amplifier with DC offset calibration (DCOC) is shown in Figure 4-11. Since the direct conversion mixer outputs in the overall system implementation are AC coupled to the baseband, the DC offsets in every stage are small and can be estimated accurately. Thus, instead of area consuming servo loops around every block a simple internal calibration circuit is employed inside every individual block. Since the design calibrates out the offset inherent in each amplifier, the cancellation is gain independent to first order. When the chip is powered up, inputs of the first gain stage in the baseband chain are shorted and the offset of the first stage is removed, each following gain stage is subsequently calibrated when set at its highest gain settings resulting in the propagation of only a small residue of DC offset along the chain. Once the calibration of all the blocks is complete, the design switches into the normal mode of operation.



(a)



(b)

Figure 4-11 (a) Schematic of the Class-A VGA amplifier with DCOC (b) DCOC correction circuit

The VGA amplifier is a two stage, fully differential Miller-compensated opamp with a unity gain bandwidth greater than 250-MHz. A phase margin of 70 deg is allocated for both common-mode and differential-mode loops. The PMOS devices, M_{22} and M_{23} in Figure 4-11 (a) compare the common-mode level with desired reference level and inject proper amount of common-mode currents into the differential output nodes of the first stage. During the start-up, to eliminate the possibility of inputs and outputs of the amplifier latching-up, a small bleed current is applied through M_{15}, causing the very weak NMOS devices M_7 and M_8 to turn-on and pull down the amplifier inputs. After the amplifier turns on and common mode levels are reached, these devices are tuned-off. The DCOC circuits are also included in the amplifier schematic, Figure 4-11 (a). During the calibration sequence, a comparator detects any DC offset at the differential outputs. Depending of the polarity of the offset, a successive approximation engine updates the six-bit trim code reducing the amount of offset error in every cycle. At the end of six cycles, the resultant six-bit trim code is latched in and calibration done signal is flagged. The DCOC correction circuit is shown in Figure 4-11 (b). Depending on the polarity of the offset, the circuit injects a differential current into the output nodes of the first stage, balancing the offset. The input referred offset correction range is 20 mV per VGA stage. The maximum offset is limited by the comparator accuracy.

The output buffer driving the off-chip load is a Class-AB amplifier in third-order Sallen-Key configuration. This buffer configuration is preferred for two reasons. First, the additional third-order filtering serves as the anti-aliasing filter for the following data converter stage and prevents SNR degradation due to aliasing. Second, because of the two-path feedback, the compensation requirement of this buffer is relaxed providing a wider bandwidth without extra power. Slight peaking is allowed in this stage, compensating for the droop caused by the passive VGA poles. The circuit schematic of this native-input, folded-cascode Class-AB amplifier is shown in Figure 4-12. The amplifier achieves a unity gain bandwidth greater than 160-MHz, with a phase margin of 53°. The input devices M_1 and M_2 are native devices to allow a rail-to-rail input swing. The PMOS and NMOS cascode devices are biased with a Vt-multiplier bias stage.

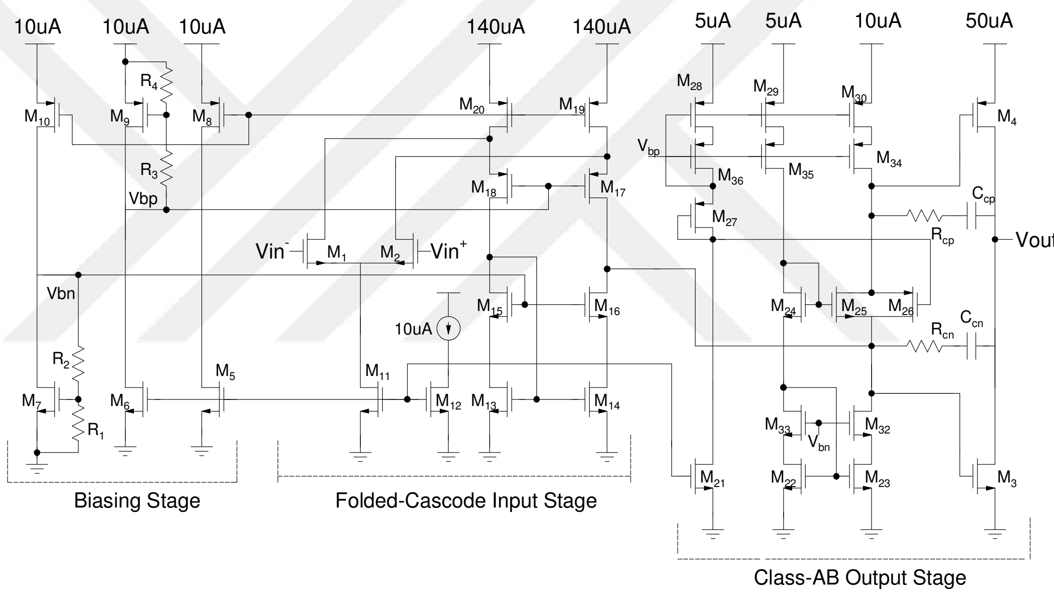


Figure 4-12 Schematic of the Class-AB output buffer

Hence, the cascode bias points track the process variations adjusting the headroom in these devices accordingly. The output stage is a class-AB stage with cascode devices biasing the floating current sources. This way, high impedance is maintained at the first stage output. Higher impedance at this node indirectly implies a higher unity gain bandwidth because of the smaller compensation capacitor required to maintain stability. The total current consumption of this buffer stage is 1.2 mA from a 1.2-V supply driving an off-chip load of 5-KΩ // 10-pF when providing a 2 Vpp differential signal swing.

4.5 Measurements

The design has been implemented and tested in a 65-nm CMOS process. The design occupies a die area of 0.17 mm^2. The whole chain consumes 2.65 mA of current from a 1.2-V supply with an additional 200 µA switch control ramp current from a 2.5-V supply. The characterization of the design is done targeting two distinct applications; ISDB-T and DVB-H. In ISDB-T mode, the signal cut-off is around 750-KHz whereas in DVB-H mode, the signal bandwidth is around 3.8-MHz. The measured VGA gain characteristics for various slope settings are shown in Figure 4-13. The nominal gain curve and the gain error curve corresponding to this particular setting are shown in Figure 4-14.

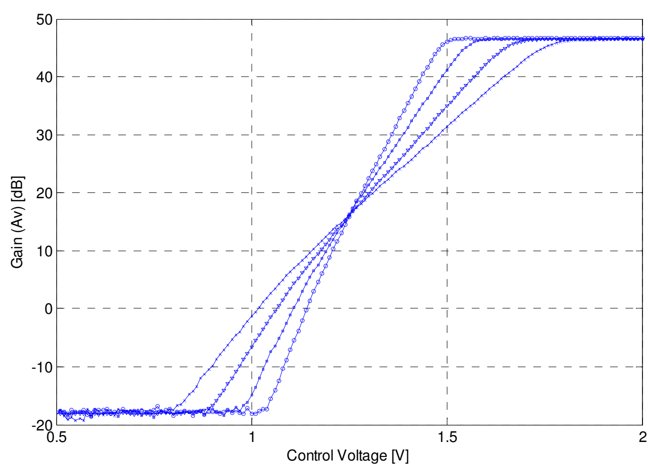


Figure 4-13 The measured VGA gain characteristics

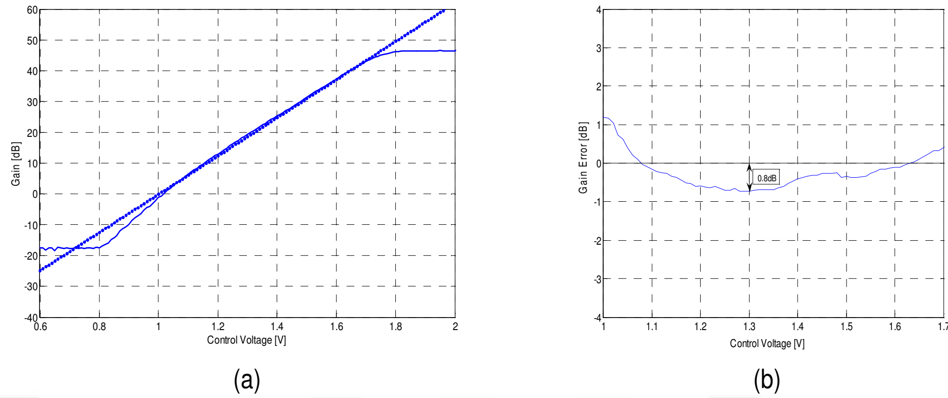
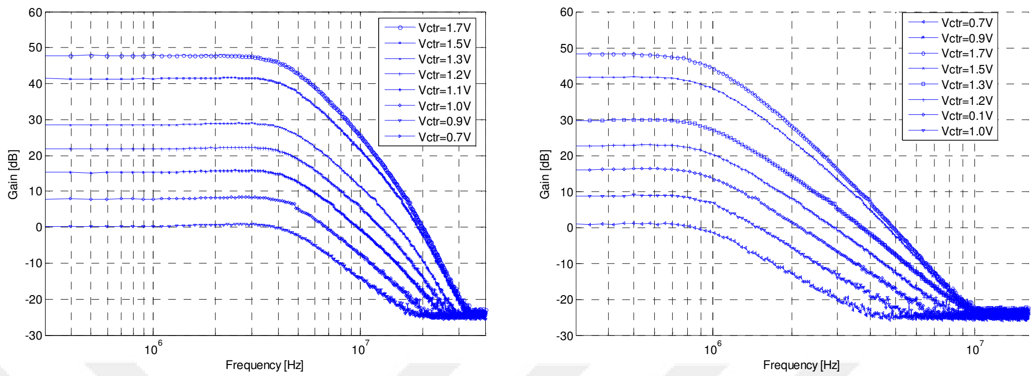


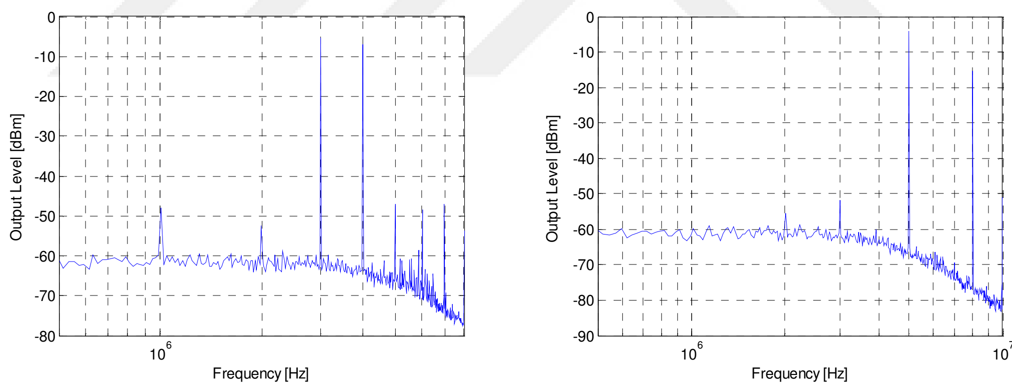
Figure 4-14 (a) The measured gain characteristics for the nominal slope setting (b) The gain error curve for the same nominal slope setting

The frequency response of the chain for various control voltages in ISDB-T and DVB-H modes is shown in Figure 4-15. The in-band and the out-of-band two-tone tests were conducted at the highest gain setting of 47 dB in high bandwidth mode (Figure 4-16). The in-band OIP3 corresponding to 3-MHz and 4-MHz -48 dBm input tones is 22 dBm, whereas, 5-MHz and 8-MHz N+1 blockers at -50 dBm input level results in a 34 dBm OIP3. The in-band HD plot is shown in Figure 17. The design achieves HD3 of -42 dB and HD2 of -44 dB for 0 dBm swing at the output. Figure 4-18 (a) shows the in-band IIP3 interpolation plot. IIP3 vs. Frequency plot is shown in Figure 4-18 (b).



(a) (b)

Figure 4-15 (a) The measured frequency response in DVB-H mode (b) The response in ISDB-T mode



(a) (b)

Figure 4-16 (a) In-band two-tone linearity test in DVB-H mode (b) Blocker two-tone linearity test in DVB-H mode

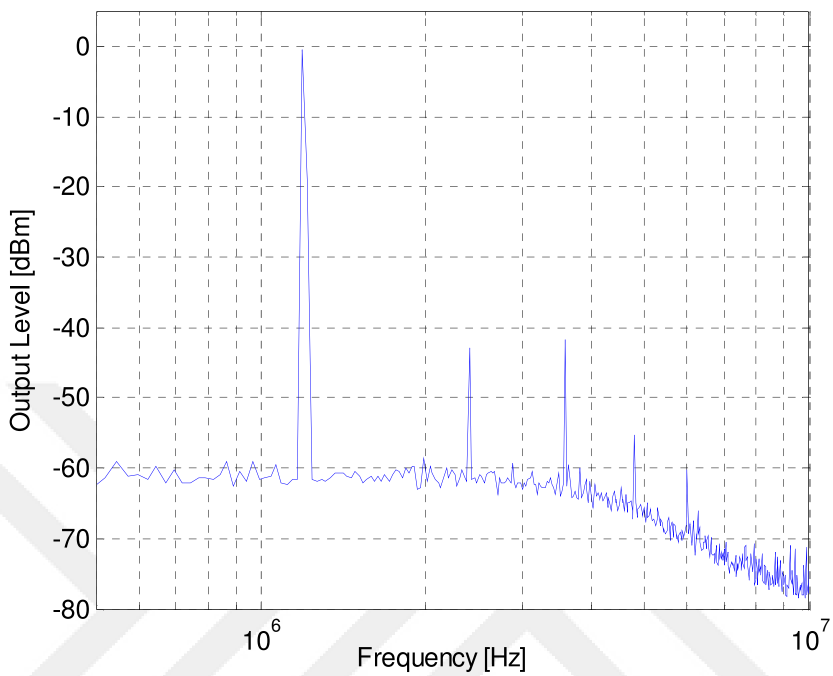


Figure 4-17 Measured in-band HD performance in DVB-H mode

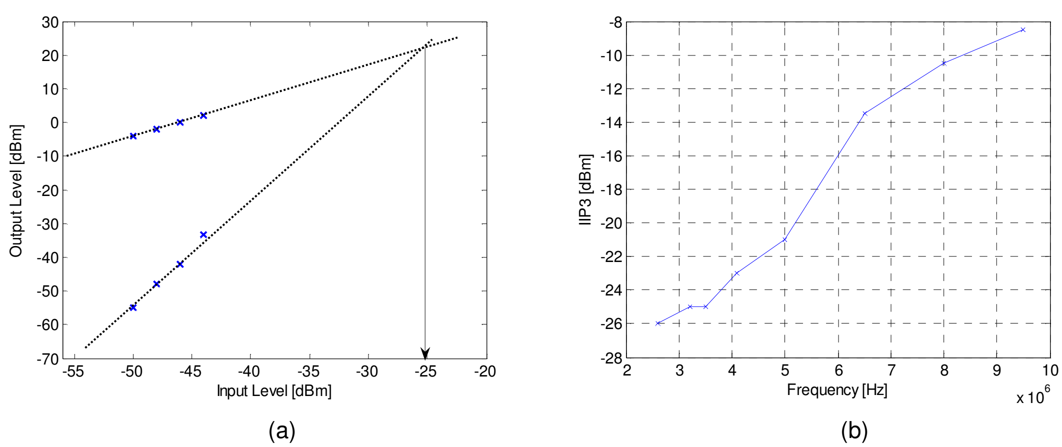


Figure 4-18 (a) Measured IIP3 in DVB-H mode (b) IIP3 vs. frequency in DVB-H mode

The noise measurements for the maximum gain setting in the DVB-H and ISDB-T modes are shown in Figure 4-19 (a) and Figure 4-19 (b), respectively. The input referred in-band noise density is 11 nV/sqrtHz. The input referred noise levels across the gain range are shown in Figure 20. The performance metrics of a 65-nm test-chip as well as of the previous works in the literature are summarized in Table 4-2. A die picture of the design is shown in Figure 4-21.

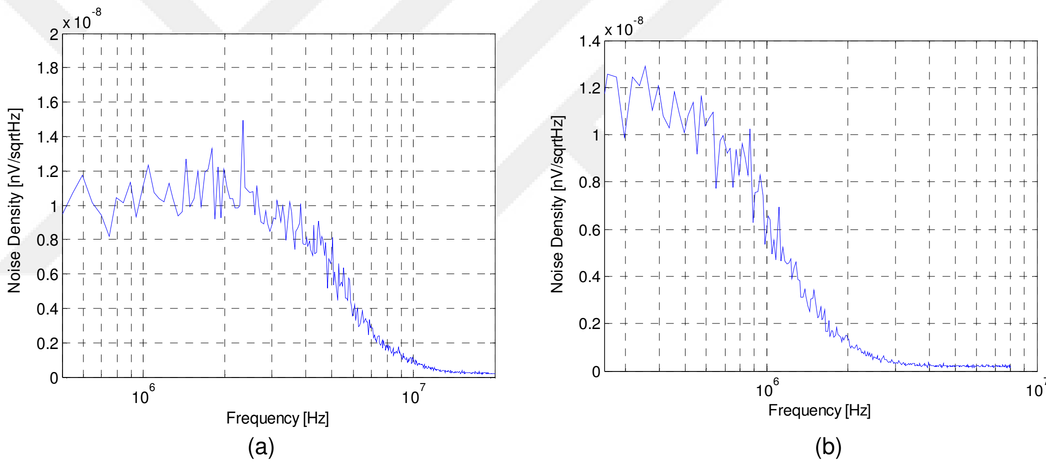


Figure 4-19 (a) Measured input referred noise in DVB-H mode (b) Measured input referred noise in ISDB-T mode

Features	[47]	[48]	[49]	[50]	[36]	**[51]**	**[52]**	**[This Work]**
Bandwidth[MHz]	20	125	15	4	3	**6**	**20**	**3.8**
Tech. [CMOS]	0.18μm	0.35μm	0.8μm	2.0μm	0.13μm	**2.0μm**	**0.5μm**	**0.065μm**
Supply [V]	1.8	3.3	5	3	2.5	**3**	**3.3**	**1.2**
Power [mW]	2.43	21	25	2.7	16	**2.64**	**33**	**2.23**
Gain Range [dB]	-10 to 20	0 to 19	-2 to 12	-6 to 24	-10 to 36	**-0.4 to 29.6**	**0 to 70**	**-18 to 47**
Gain Step [dB]	1	2	2	1	11	**Cont.**	**Cont.**	**Cont.**
Constant BW	Yes	Yes	No	No	Yes	**Yes**	**Yes**	**Yes**
OIP3 [dBm]	29.2	31	42	30	26	**28**	**33**	**22***
IRN [nV/sqrtHz]	11.2	8.6	20	16.5	4.2	**308**	**9**	**11**

*Reported value is for the maximum gain setting of 47 dB.

Table 4-2 Performance summary and comparison

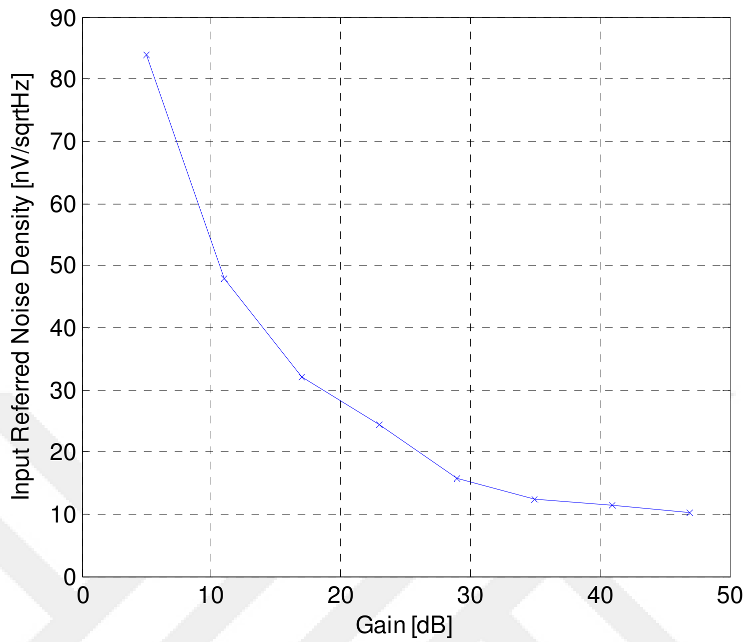


Figure 4-20 Input referred noise levels for various gain settings

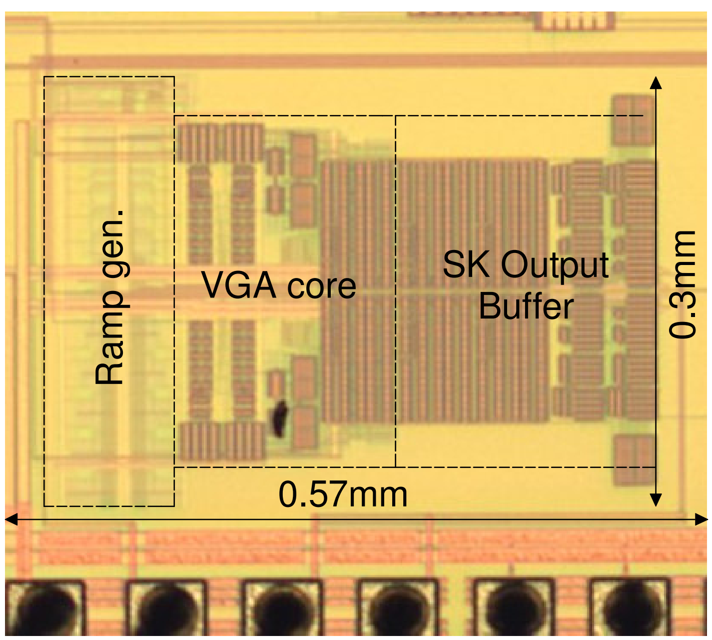


Figure 4-21 Die microphotograph of the proposed VGA design

4.6 Conclusion

In this paper a new continuous linear-in-dB VGA approach is introduced which reduces the linearity and noise problems associated with MOS-switch-based continuous tuning. Using the proposed technique, a rail-to-rail input and output swing and highly linear VGA operation is obtained from a 1.2-V supply. Moreover, a simple DCOC technique introduced provides a gain and temperature independent offset cancellation. One time DCOC at power-on provides a 3 mV output offset error. With this calibration setting, the maximum output offset level observed is 25 mV across 120 °C temperature and 65 dB gain range.

5 A Universal Low Noise Analog Receiver Baseband with Noise Shaping Blocker Filtering

5.1 Introduction

Many new wireless standards have emerged in recent years as a result of strong consumer demand in wireless applications. While the abundance of these wireless applications drives the technology to its limits to catch-up with the demand, the crowding of the spectrum poses additional challenges for the designers. These emerging wireless standards have to be backward compatible with the existing standards. Hence, very strong interferers can coexist in the nearby channels whereas the desired signal in the channel of interest might be very weak. This is particularly the case for mobile-TV applications, where 46-dB stronger analog interferers can exist in the close vicinity of the desired channel [11]. As a result, the classical noise-linearity-power-area tradeoff becomes an even more pronounced challenge in wireless receiver design. Because of the additional battery life concerns, the solution for portable devices must allow a low-power operation. Since area is also of relatively greater concern in such portable devices, designs should be reconfigurable for different frequency bands and applications.

Recently many high performance DCR and Low-IF receiver circuits have been reported [3-10]. Most of these designs tailor the technology and the classical circuit techniques to achieve good performance for a given application. As the supply voltages decrease, this approach does not remain competitive. Lower supply voltage requires lower noise levels to be able to maintain a comparable DR performance. In most of the integrated receivers a channel select filter is employed to attenuate the near by blockers and hence relax the DR range requirement of the ADC. Design of a low noise classical filter circuit involves use of large on-chip capacitors, which translates into a large die area. Hence, in order to alleviate the area tradeoff in a high cost deep-sub-micron process, new circuit topologies should be investigated. The work in this paper introduces noise shaping circuit techniques to enable the transition to a lower supply voltage without incurring the cost of extra area. The noise shaping blocker filtering baseband architecture is described in Section 5.2. Detailed circuit designs of various blocks are discussed in Section 5.3. Experimental results from a 65-nm CMOS test-chip are presented in Section 5.4 and we present our conclusions in Section 5.5.

5.2 Baseband Architecture

The block diagram of the wide-band direct conversion receiver including the proposed baseband architecture is shown in Figure 5-1. In most of radio front-ends, the mixers are followed by a highly linear low-noise post-mixer amplifier (PMA) [4-6]. The main reason for choosing such architecture is that the desired signal level after the mixers can still be low and hence a noise of an on-chip filter circuit with a reasonable die area is not acceptable from sensitivity point of view. The cost related to this choice however is high. First, the mixer and the preceding low-noise amplifier

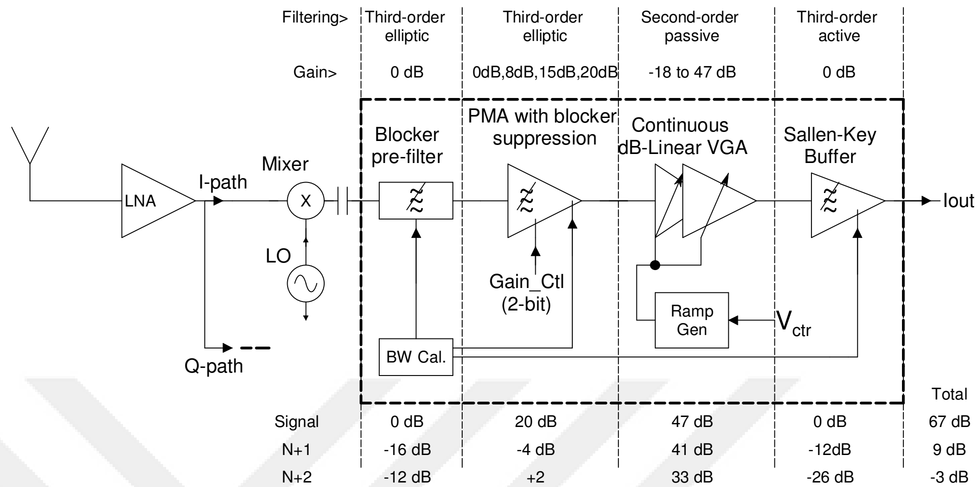


Figure 5-1 The receiver chain including the proposed baseband architecture

gains have to be lower to relax the linearity required in the PMA. This also means that the noise of the baseband circuitry should be kept even lower since it experiences a lower gain ahead of it (implying more area and power in the baseband). Second, the design of the PMA in the presence of unfiltered strong blockers poses a challenge regarding the linearity requirement of this amplifier (more power). Thus, if one can somehow introduce a small area low-noise blocker filtering following the mixers, one can obtain two-fold benefit; a relaxed baseband noise specification, requiring less power and area, and a relaxed PMA linearity specification, also leading to less power. If this filtering somehow can protect the mixer outputs from large blockers, then the benefit becomes even more substantial by allowing more gain in the front-end and reducing the noise spec of the following PMA and the other baseband circuits even further. In the proposed baseband architecture, we use the unique post-mixer noise-shaping high-order blocker pre-filter introduced in Chapter 2 to achieve the benefits mentioned above. As opposed to existing filter topologies, the proposed circuit achieves filtering at the mixer outputs and helps the mixer linearity.

The same basic noise-shaping high-order filtering idea is also utilized in the following PMA stage. This time, an instrumentation type PMA stage, which is introduced in Chapter 3, is used providing gain only in the band of interest and at the same time a relative third-order elliptic filtering for the out-of-band signals. The approach here is to amplify only the signal of interest rather than amplifying the blockers as well and then trying to filter them out in subsequent filtering stages. Eliminating such redundancies in the system results in substantial power and area savings. Moreover, because of the noise shaping characteristics of the proposed technique, the mentioned relative third-order filtering is obtained without any significant noise penalty. Gain of this stage is programmable for gains of 20-dB, 15-dB, 8-dB, or 0-dB.

The PMA is followed by a two-stage voltage-ramp-based rail-to-rail input and output swing variable gain amplifier of Chapter 4 with linear-in-dB gain characteristics. Many CMOS VGA designs proposed in the literature report very linear operation by controlling the VGA gain in steps. The gain switching however may not be acceptable for orthogonal frequency-division multiplexing (OFDM) based systems, such as Mobile-TV. There is however linearity and noise degradation associated with continuous gain control, since now gain-tuning MOS switches may not be fully on. The novel VGA circuit of the baseband chain achieves a continuous highly linear 65-dB gain range with two additional passive poles (a pole per stage). A voltage-ramp circuit generates 10 differential ramp control voltages that controls the VGA stages in both the I and Q branches. AC coupling after the mixers eliminates any signal dependent DC offset resulting from the front-end amplification and mixing. Because the DC offsets from the PMA and the VGA stages can be estimated accurately, a simple DC offset calibration circuit is employed inside each of the VGA stages rather than area consuming servo loops. Since the design intends to eliminate the offset inherent to the amplifier, the cancellation is gain and temperature independent to first order.

The output buffer driving the off-chip load is Class-AB amplifier in a third-order Sallen-Key configuration. This buffer configuration is preferred for two main reasons. First, the additional third-order filtering serves as the anti-aliasing filter for the following data converter stage, and prevents the SNR degradation due to aliasing. Second, because of the two-path feedback used in that stage, the compensation requirement is relaxed providing a wider bandwidth without extra power. Slight peaking is allowed in this stage, compensating for the droop caused by the passive VGA poles. A bandwidth calibration circuit calculates a 6-bit calibration code during the power-up calibration sequence for the filtering blocks. This circuit can be clocked from any crystal reference frequency in the range 10 MHz to 40 MHz. A 7-bit resistor

DAC in this block is used to choose the crystal frequency and the desired bandwidth in the range 700-KHz to 5.2 MHz.

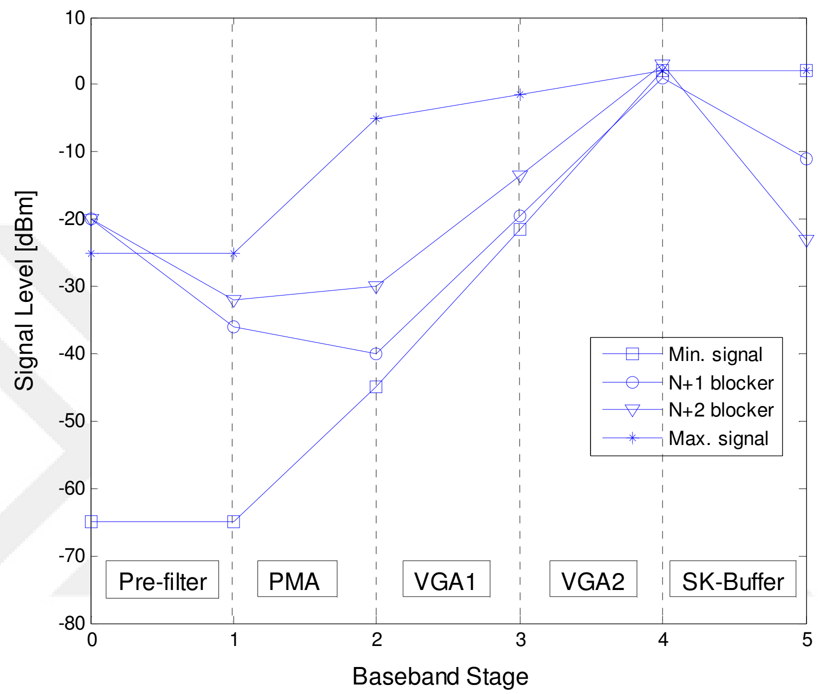


Figure 5-2 The signal and blocker profiles along the baseband chain

The signal and blocker profiles along the baseband chain are shown in Figure 5-2 for a DVB-H channel. Interleaving the gain and third-order noise shaping filtering along the chain eliminate the need for a stand alone high order filter. Most of the filtering elements mentioned serve a dual purpose, gain and filtering. This approach results in significant power and area savings.

5.3 Circuit Design

5.3.1 Pre-filter and PMA with Blocker Suppression

The schematic of the post-mixer blocker pre-filter and a PMA is shown in Figure 5-3. The pre-filter section is a frequency dependent negative resistance (FDNR) based circuit that reutilizes the mixer load resistor R_f, to create a third-order elliptic response at the mixer output and PMA input. Such a configuration is unique in the sense that it does not allow blocker voltage swing at the mixer outputs and hence relaxes the mixer linearity specification resulting in a low power mixer design. Moreover, since the mixer gain can now be increased, the following PMA and the baseband chain can be noisier: another opportunity for power saving. In order to quantify the saving only in the following PMA stage, a simple noise-power tradeoff in this stage is presented. The total opamp noise contribution in the PMA stage shown in Figure 5-3 can be approximated as follows:

$$V_{n_{OPA}}{}^{2} \cong \frac{16kT\gamma}{g_m} \tag{5.1}$$

where g_m is the transconductance of input differential pair devices. The resistor noise contributions are:

$$V_{n_R}{}^{2} = 8kTR_{in}. \tag{5.2}$$

Assuming γ of unity and combining (5.1) and (5.2), the total PMA noise is approximated as:

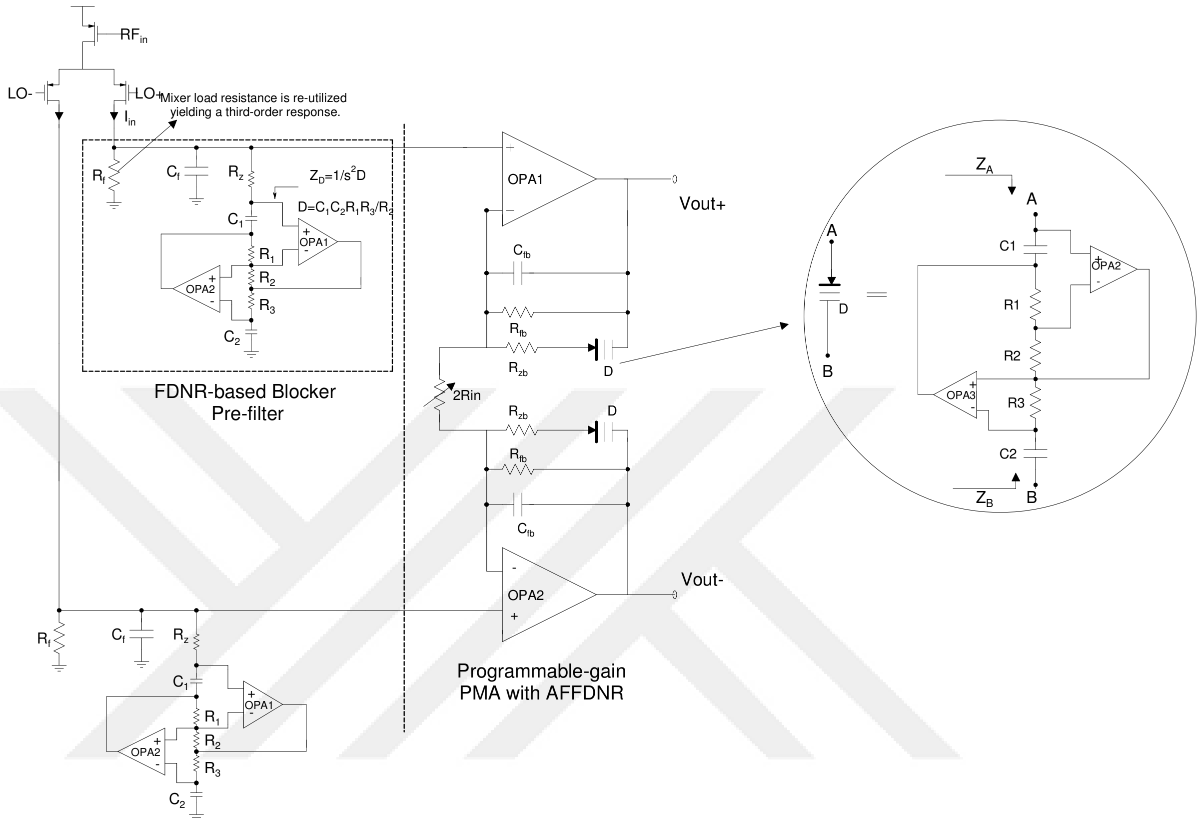


Figure 5-3 Noise shaping pre-filter and blocker-reject PMA schematic

$$V_{n_T}^{\;2} = 2 \cdot \left[4kTR_{in} + 4kTR_{eq}\right] \tag{5.3}$$

where, $R_{eq} = 2/g_m$. In order not to be dominated by the resistor noise contribution, we choose $R_{in} = R_{eq}/2 = 1/g_m$. The noise equation in (5.3) can now be rewritten as:

$$V_{n_T}^{\;2} = 6 \cdot 4kTR_{in} \; . \tag{5.4}$$

The current level that the opamp output stage needs to be able to deliver can be written in terms of input resistance as follows:

$$I_{out} = \frac{nV_{in\,p}}{R_{in}} \tag{5.5}$$

where n is the extra current margin factor at the output devices and can be chosen to be 1.5 in a conservative design. Using (5.4) and (5.5), the output current can be summarized in terms of noise voltage and the peak input voltage swing as follows:

$$I_{out} = \frac{36 \cdot V_{inp}^{\ 2}}{V_{n_T}^{\ 2}}. \tag{5.6}$$

Input differential-pair device transconductance is written down in terms of tail current as:

$$g_m = \sqrt{2KI_{tail}/2} = \sqrt{KI_{tail}}. \tag{5.7}$$

Since $R_{in} = R_{eq}/2 = 1/g_m$ was the design choice, using (5.4) the minimum tail current using the maximum K value K_{max}, can be written down in terms of noise voltage as

$$I_{tail} = \frac{576(kT)^2}{K_{max}V_{n_T}^{\ 4}} \tag{5.8}$$

Combining (5.6) and (5.8), the total current consumption for a desired noise voltage level can be approximated as:

$$I_{total} = I_{out} + I_{tail} = \frac{36V_{inp}^{\ 2}}{V_{n_T}^{\ 2}} + \frac{576(kT)^2}{K_{max}V_{n_T}^{\ 4}}. \tag{5.9}$$

Based on (5.9), a plot of the current consumption corresponding to various noise levels in the PMA is shown in Figure 4. This allows us to quantify the effect of a

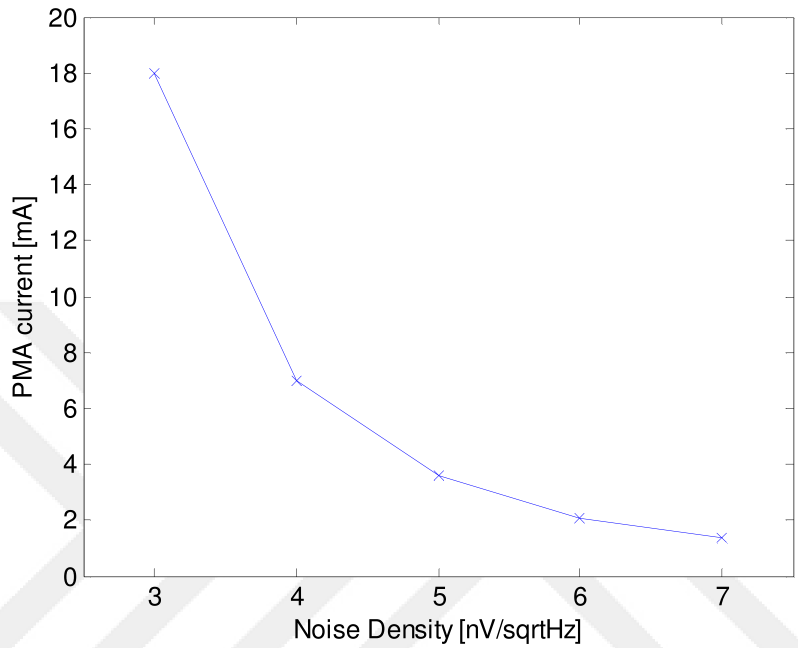


Figure 5-4 PMA noise density vs. required current consumption

reduced noise requirement on the overall power and so manage this tradeoff. Reducing the noise requirement of the PMA by employing such a pre-filtering can result in substantial power saving in this baseband stage. A more interesting property of this pre-filtering circuit is its noise shaping characteristic which is discussed in Chapter 2. It uses only one noisy resistor in the signal path, the load resistor of the mixer (R_f), to realize the desired filter transfer function. The noise contribution of this particular resistor is already accounted for in the mixer noise budget and the noise of all the FDNR resistors R_1, R_2, R_3, and R_z is shaped.

This noise shaping filtering idea is also utilized in the following high input impedance instrumentation type PMA stage (Figure 5-3). This time the feedback gain resistor R_{fb} is reutilized, and the noise of the AFFDNR circuit elements in the feedback path is shaped, and hence, once more, the desired third-order elliptic filtering is obtained without any significant noise degradation.

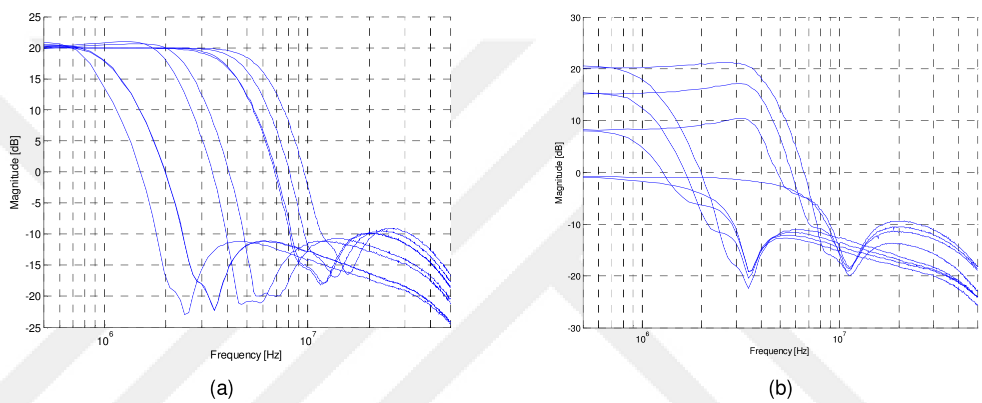


Figure 5-5 (a) Prefilter-PMA response across the range of possible filter settings. (b) Response in ISDB-T and DVB-T/H modes for all PMA gain settings

The measured response of this 6^{th} order pre-filter and PMA section is shown in Figure 5-5. Figure 5-5 (a) shows the response across the band while Figure 5-5 (b) shows the response of the circuit for various PMA gain settings in ISDB-T and DVB-H modes. The measured input referred noise density of the section is 10 nV/sqrtHz and 14 nV/sqrtHz in DVB-H and ISDB-T modes respectively. This section consumes a die area of 0.28 mm^2. In ISDB-T full-gain mode, 2.4-MHz and 4.4-MHz blockers (3.5 dBm each) result in -59.6-dBm IM3 product which corresponds to an out-of-band IIP3 of 44.5 dBm. In-band IIP3 for this case is 18 dBm. In DVB-H mode, 5-

MHz and 8-MHz blockers (3.5 dBm each) result in -55-dBm IM3 which corresponds to an out-of-band IIP3 of 42.6 dBm. In-band IIP3 for DVB-H case is 15.5 dBm. The pre-filter consumes 2.6 mA from a 1.2-V supply, while the PMA needs 3.9 mA in full-gain mode from the same 1.2-V supply.

A simple figure of merit (FOM) is defined to compare the performance of this pre-filter-PMA section with the other filter works in the literature. The FOM proposed in this work is as follows:

$$FOM = \frac{\frac{DR \cdot BW}{V_{DD}}}{\left(\frac{BW \cdot C_{tot}}{N}\right) \cdot \left(\frac{Pwr}{N \cdot BW}\right)} \tag{5.10}$$

where, *DR* is dynamic range, *BW* is the filter bandwidth, C_{tot} is the total amount of capacitance used, *Pwr* is the current consumption and *N* is the number of poles. This FOM includes dynamic range as well as the required power consumption and total capacitance scaling them with respect to the filter bandwidth and number of poles. The plot in Figure 5-6 compares various filters reported in the literature based on the FOM defined. The performance metrics from which the FOM are calculated are summarized in Table 5-1.

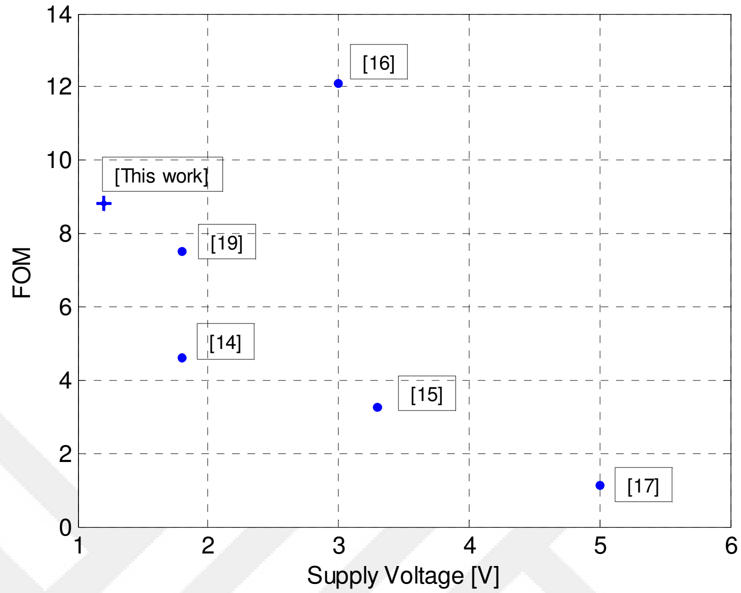


Figure 5-6 Figure of merit comparison of various filters reported in the literature

	BW [MHz]	Cap [pF]	Noise Den. [nV/sqrtHz]	poles [N]	DR [dB]	I_D [mA]	V_{DD} [V]	FOM
[19]	10	230	7.5	4	79	2.25	1.8	7.5
[14]	2	100	56	5	-	2.7	1.8	4.6
[15]	5.5	24	114	3	62	3.6	3.3	3.4
[16]	4	16	130	5	57.6	3.3	3	12.1
[17]	4	28	50	3	70	3.2	5	1.2
This work	4	170	10	6	83	5.5	1.2	8.7

Table 5-1 Performance summary for various filters in the literature

5.3.2 Continuous Linear-in-dB VGA and Sallen-Key Output Buffer

The differential ramp based continuous dB-linear VGA, which is described in Chapter 4, is used as the final gain stage. Following this stage is a third-order Sallen-

Key output buffer. Since the technique is described in detail in Chapter 4, only measurement results will be summarized in this session.

In maximum gain configuration, the measured in-band OIP3 corresponding to 3-MHz and 4-MHz -48 dBm input tones is 22 dBm, whereas, 5-MHz and 8-MHz N+1 blockers at -50 dBm input level results in 34 dBm OIP3. The input referred in-band noise density is 11 nV/sqrtHz for the VGA-SK combination. The total die area of this section is 0.17 mm^2. The block consumes 2.65 mA of current from a 1.2-V supply and 200 µA current from a 2.5-V supply for the switch control ramp circuit.

5.3.3 Reconfigurable Bandwidth Calibration Circuit

The bandwidth calibration circuit and its timing diagram are shown in Figure 5-7. During the initial calibration a 7-bit bandwidth calibration code sets the resistive DAC targeting the desired filter bandwidth for a given crystal clock frequency. The trim range of this resistor is large enough to cover whole filter bandwidth as well as any crystal frequency in the range of 10 MHz to 40 MHz that is used as a reference. Following this, successive approximation logic computes a calibration code with the help of a comparator as illustrated in Figure 5-7. Note that, since the resistor in this configuration is used as a trim element determining the bandwidth and crystal frequency, the capacitor is used as the calibration element with 6-bit resolution.

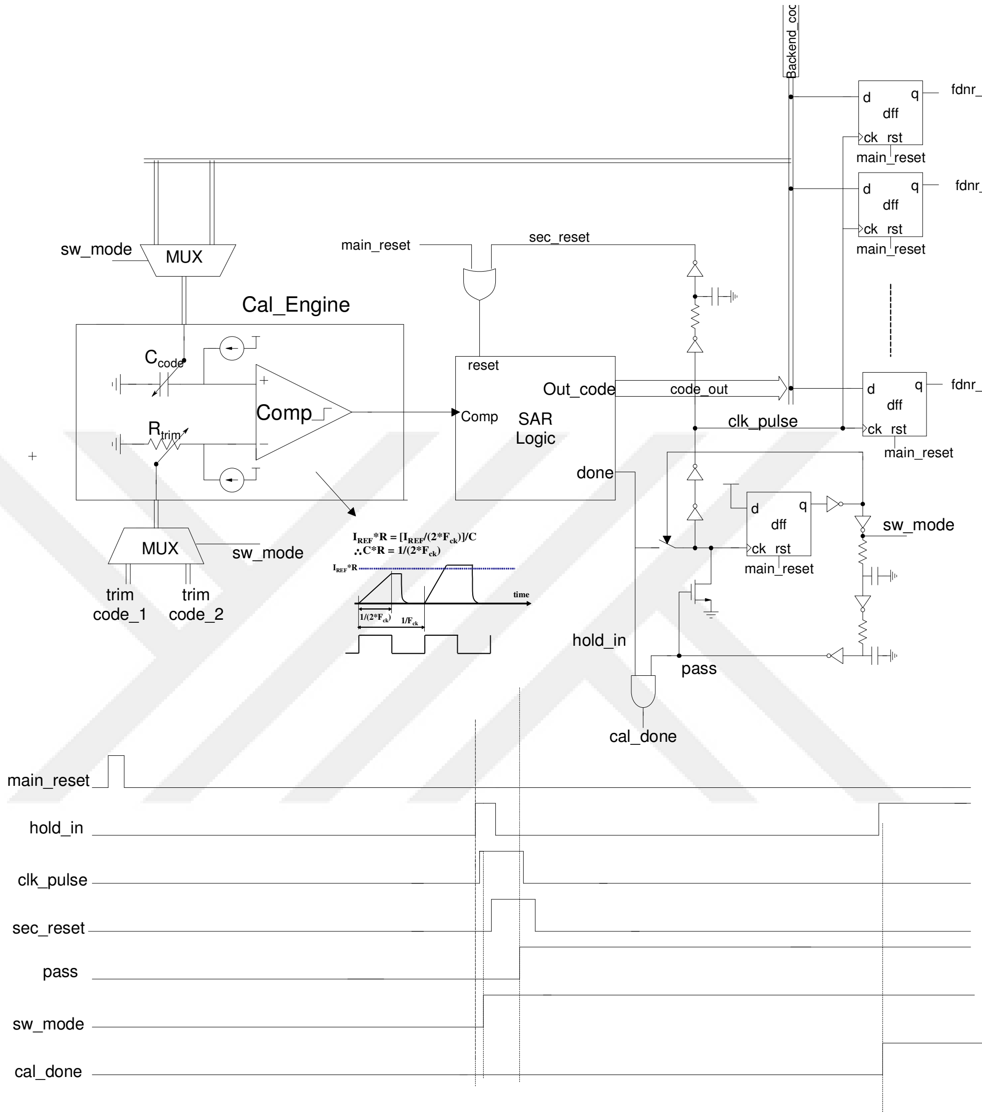


Figure 5-7 The bandwidth calibration circuit and its timing diagram

The first baseband stages (FDNR pre-filter and PMA) require a different calibration code than the backend circuits. There are multiple ways to generate the two sets of codes corresponding to different trim element ratios in different circuit blocks. One solution is to use two different calibration circuits. Because of the extra die area required, this solution is not an attractive one. A second solution is to generate a code for one of the blocks and then use a digital fractional multiplier to scale this code to generate the trim codes required by the other block. Although, the area penalty in this solution is much less, it still adds to the total die area. Another solution, which is used in this design, eliminates the area penalty completely. The idea is to run the calibration sequence twice. After the first sequence the first calibration code is latched into a register (FDNR code). Following this, the capacitor ratios in the calibration engine are reconfigured to generate another set of calibration code for the backend blocks. A new set of resistor trim code is also switched in to be able to set the poles of the backend blocks independently. In this way, the overall cut-off, notch and stop-band response of the whole chain can be adjusted independently, offering a universal widely tunable solution.

On the filter side, in addition to corresponding 6-bit resolution capacitor bank, there is a resistor trim to switch between the high-end and the low-end of the bands. The tuning resolution at the low-band mode is around 20 KHz while it is 80 KHz in the high-band mode.

5.4 Experimental Results

The proposed baseband architecture was implemented in a 65-nm CMOS process and tested. The die and the test board photos are shown in Figure 5-8 and Figure 5-9, respectively.

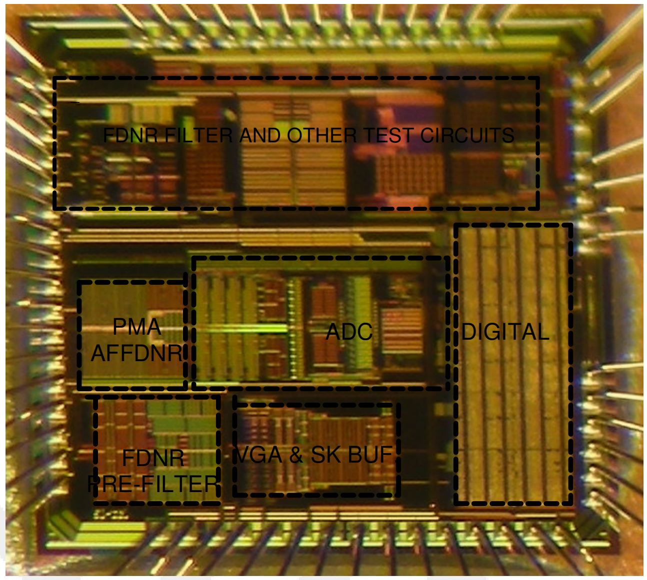


Figure 5-8 Die photo of the complete receiver baseband

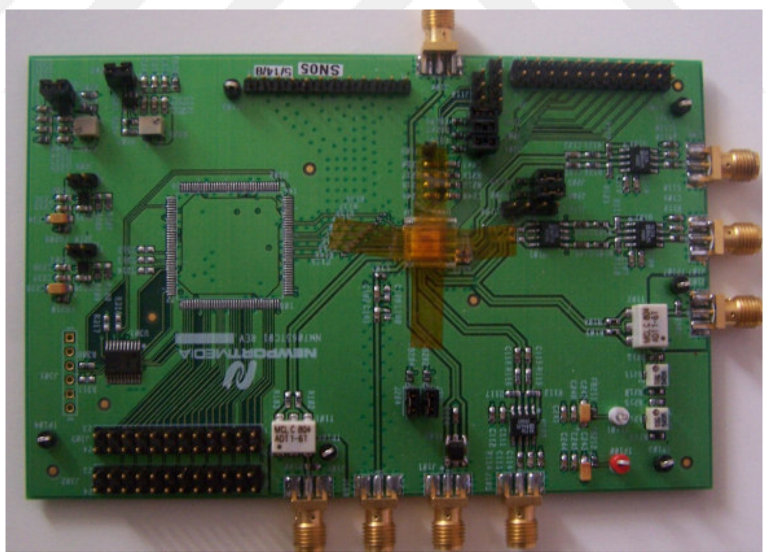


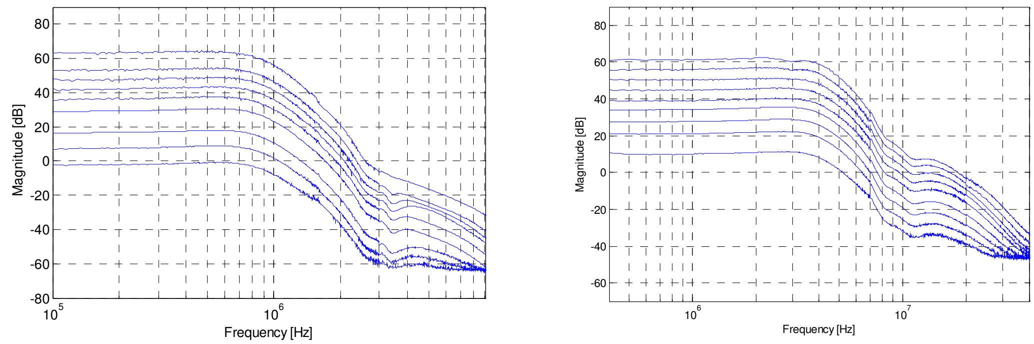
Figure 5-9 Test board of the receiver baseband

The inputs and outputs of various sub-blocks were connected to pins to enable measurement of each section separately. For noise measurements, AD8079 and AD9631 very low noise buffer amplifiers were used on the test board to drive Agilent

E4408B spectrum analyzer. The parameters of various sections used in the design are useful in illustrating the limitations of each block. Table 5-2 summarizes the performance parameters of the individual blocks and the whole baseband chain. The frequency response of the analog baseband chain in ISDB-T and DVB-T/H modes is shown in Figure 5-10. 85-dB blocker-aware continuous gain range combined with low-noise operation results in 87.2 dB and 82.5 dB dynamic range in ISDB-T and DVB-T/H modes, respectively. The two-tone linearity measurements for N+1 blockers are conducted at a gain of 56 dB. In ISDB-T mode, 2.4-MHz and 4.4-MHz blockers (-10 dBm each at the output) result in -22-dBm IM3 which corresponds to an out-of-band IIP3 of 24.2 dBm (Figure 5-11 (a)). In DVB-H mode, 7-MHz and 12-MHz blockers (-15 dBm each at the output) result in -38-dBm IM3 which corresponds to an out-of-band IIP3 of 24 dBm (Figure 5-11 (b)). Figure 5-12 shows the measured IIP3 interpolation data for the target bands. The chain achieves input referred noise levels of 10.5 nV/sqrtHz and 14.5 nV/sqrtHz for the DVB-H and ISDB-T modes, respectively. The measured input referred noise plots are shown in Figure 5-13. The entire receiver baseband occupies a total die area of 0.45 mm^2. The design consumes total of 9 mA current from a 1.2-V supply, as well as, an additional 0.2 mA VGA ramp-control current from a 2.5-V supply. The total power consumption is 11.5 mW.

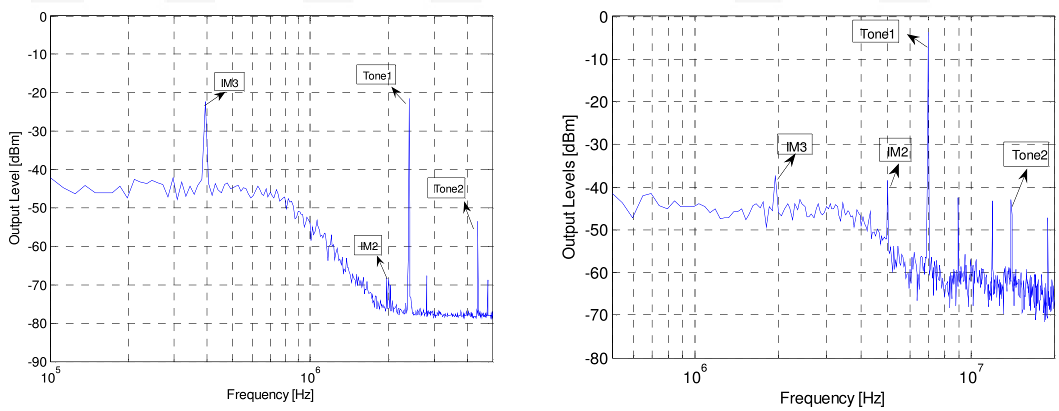
Block	Parameter	Measurement	
		ISDB-T(700KHz)	DVB-H(3.8MHz)
Pre-filter	Die area	0.16 mm^2	
	In-band IIP3	22.5dBm	20.6dBm
	N+1 blocker IIP3	36.5dBm	31.5dBm
	HD2(@-1dBm input)	-57dB	-59dB
	Input referred noise	7.5nV/sqrtHz	7 nV/sqrtHz
	Stop-band attenuation	12dB	13dB
	Notch attenuation	18dB	19dB
	Tuning range	700KHz to 5.2MHz	
	Tuning resolution	20KHz	80KHz
	Current consumption	2.6 mA from 1.2 V	
PMA	Die Area	0.12 mm^2	
	Max. gain	20-dB	
	Min. gain	0-dB	
	Gain steps	5-dB	
	HD2(@2dBm output)	-57.4dB	-60.5dB
	N+1 blocker IIP3	37dBm	29.7dBm
	Input referred noise	9.5 nV/sqrtHz	14 nV/sqrtHz
	Stop-band attenuation	18dB	17dB
	Notch attenuation	31dB	26dB
	Tuning range	700KHz to 4.2MHz	
	Tuning resolution	20KHz	80KHz
	Current consumption	3.9 mA from 1.2 V	
VGA-SK Buffer	Die Area	0.17 mm^2	
	Max. gain	47dB	
	Min. gain	-18dB	
	Gain steps	Continuous	
	In-band IIP3	-25dBm(@max gain)	
	N+1 blocker IIP3	-13dBm(@max gain)	
	HD2 (@0dBm output)	-44dB(@max gain)	
	HD3 (@0dBm output)	-42dB(@max gain)	
	Input referred noise	11 nV/sqrtHz	
	Stop-band attenuation	26dB(@2.5MHz)	16dB(@8MHz)
	Tuning range	700KHz to 5MHz	
	Tuning resolution	20KHz	80KHz
	Current consumption	2.44 mA from 1.2 V	
		0.2 mA from 2.5 V	
Analog Baseband	Die Area	0.45 mm^2	
	Max. gain	67dB	
	Min. gain	-18dB	
	Gain steps	Continuous	
	N+1 blocker IIP3	24dBm	24.2dBm
	Input referred noise	10.5 nV/sqrtHz	14.5 nV/sqrtHz
	Stop-band attenuation	64dB(@2.5MHz)	42dB(@8MHz)
	Notch attenuation	78dB	55dB
	Tuning range	700KHz to 5.2MHz	
	Tuning resolution	20KHz	80KHz
	DR (@HD3=40dB)	87.2 dB	82 dB
	Current consumption	9mA from 1.2 V & 0.2mA from 2.5 V	

Table 5-2 Performance summary of various baseband blocks



(a) (b)

Figure 5-10 The measured baseband frequency response in; (a) ISDB-T Mode (b) DVB-H Mode



(a) (b)

Figure 5-11 (a) Two-tone test in ISDB-T mode (b) Two-tone test in DVB-H mode

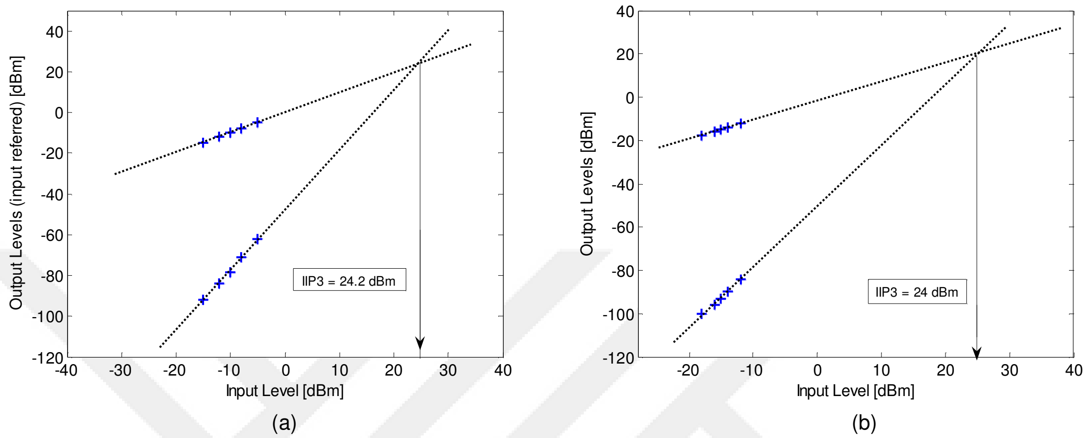


Figure 5-12 Measured IIP3: (a) in ISDB-T mode (b) in DVB-H mode

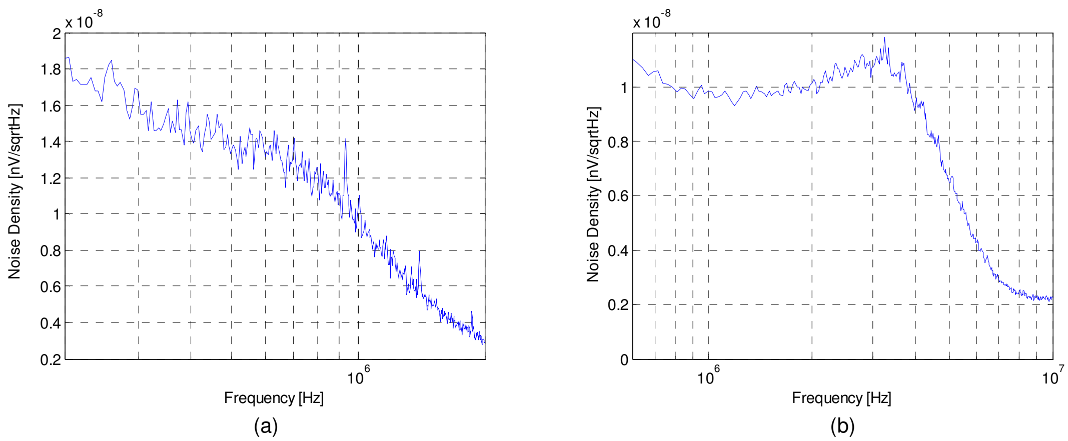


Figure 5-13 Total input referred noise: (a) In ISDB-T mode (b) In DVB-H mode

5.5 Conclusion

A unique analog baseband chain approach is introduced to mitigate disadvantages of the supply voltage scaling in a deep-sub-micron process. This approach provides a comparable, even better performance for certain metrics than its high voltage counterparts without sacrificing extra capacitor area. The new techniques introduced, noise-shaped blocker filtering and linear VGA operation with continuous gain tuning, maximized the dynamic range of the radio. The proposed circuit is placed at the mixer output, allowing a higher front-end gain, and hence relaxing the noise requirement of the baseband. Although the measurements have been conducted for two mobile-TV applications, ISDB-T and DVB-T/H, the solution can be tuned to any application in a frequency band from 700 KHz to 5.2 MHz. The frequency response can be configured for the blocker profile appropriate for the desired application. The multiple calibration sequences during the power-up provide multiple trim codes for various blocks along the chain. Thus, independent band characteristics along the chain can be combined to yield the best response for the desired application.

6 Conclusion

The expanding growth of wireless communications has led to proliferation of different standards. The highly competitive market demands low cost, low power and small form factor devices. Although, technology scaling allows denser device integration, the resulting supply voltage reduction counteracts this benefit by requiring larger device area to maintain the desired system dynamic range. The area cost in the deep-sub-micron processes is too high to justify the use of classical circuit techniques in the design of a receiver chain. Thus, new circuit techniques need to be explored to relax the area and hence the cost tradeoff.

In this thesis work, some unique noise shaping circuit techniques are introduced to alleviate the mentioned noise-area-power tradeoff in a wireless receiver design. In Chapter 2, a noise shaping blocker filtering technique was introduced. The detailed noise, linearity and stability analysis are carried on to reveal the basic design tradeoffs. The validity of the noise shaping filtering concept is verified with the measurement results of a 65-nm low noise, low power, and small form factor design. The technique is not limited by the basic third-order elliptic implementation. Building upon the same FDNR noise shaping idea, some higher order circuit topologies are also explored and presented at the end of the chapter.

In Chapter 3, a blocker-reject amplifier concept was introduced. The proposed AFFDNR feedback amplifier topology provides gain in the signal band while simultaneously implements a third-order low-pass elliptic response for the blocker signals. Thanks to the noise shaping characteristic of the technique, the additional high-order filtering feature is attained without incurring any significant amount of noise in the circuit. In addition to verifying the mentioned gain-filtering idea with the measurement results of a 65-nm test-chip, some cascade circuit topologies were also presented.

In Chapter 4, a differential-ramp based continuous dB-Linear VGA technique was introduced. Using the proposed technique, digitally programmable gain amplifiers (PGAs) can be converted to analog controlled, dB-linear VGAs with minimum impact on noise and linearity. This provides an efficient way of realizing an analog controlled VGA for OFDM based applications. Although the technique is illustrated by converting an opamp based high-linearity, low-noise PGA to a dB-linear VGA for CMOS mobile TV applications, it can easily be applied to other applications. The measurement results of a successful 65-nm test-chip are presented along with the performance parameters of some of the other VGA works in the literature.

In Chapter 5, all of the techniques mentioned in the previous chapters are combined to build a low-noise, low-power analog radio baseband in a 65-nm CMOS process. The measurement results of this test-chip have proven a comparable and even better performance than the existing high voltage state of the art designs. The performance summary of this work as well as the mentioned works is presented in Table 6-1.

Features	[7]	[8]	[4]	[This Work]
Bandwidth[MHz]	1	1	2.2	3.8
Technology [CMOS]	1.2µm	0.18µm	130nm	65nm
Supply [V]	3.0	1.8	2.5	1.2
Power [mW]	7.1	4.86	20.5	11.5
Gain Range [dB]	12 to 30	12 to 55	-6 to 68	-18 to 67
Gain Step [dB]	6	2	10	Continuous
DR [dB] @-40dB HD3	60.1 (SFDR)	73.5 (SFDR)*	82 (11MHz BW)	82.5
IIP3 [dBm]	12.2	30	21	24
IRN [nV/sqrtHz]	43.2	32	5	10.5
Die Area [mm^2]	2.89	1.5	1.65	0.45

*Simulation only.

Table 6-1 Performance comparison of various receiver basebands in the literature

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