ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

STABILITY ANALYSIS OF ADAPTIVELY BIASED LOW DROPOUT REGULATORS

M.Sc. THESIS

Türker UNUTMAZ

Department of Electronics and Communication Engineering

Electronics Engineering Programme

JUNE 2017

ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

STABILITY ANALYSIS OF ADAPTIVELY BIASED LOW DROPOUT REGULATORS

M.Sc. THESIS

Türker UNUTMAZ
504141223

Department of Electronics and Communication Engineering

Electronics Engineering Programme

Thesis Advisor : Assoc. Prof. Dr. Metin YAZGI

JUNE 2017

İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

ADAPTİF KUTUPLAMALI ALÇAK GERİLİM DÜŞÜMLÜ REGÜLATÖRLERİN KARARLILIK ANALİZİ

YÜKSEK LİSANS TEZİ

Türker UNUTMAZ
504141223

Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

Elektronik Mühendisliği Programı

Tez Danışmanı : Doç. Dr. Metin YAZGI

HAZİRAN 2017

Türker Unutmaz, a M.Sc. student of ITU Graduate School of Science Engineering and Technology, student ID 504141223, successfully defended the thesis entitled "Stability Analysis of Adaptively Biased Low Dropout Regulators", which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

Thesis Advisor :	**Assoc. Prof. Dr. Metin YAZGI** Istanbul Technical University	……...
Jury Members :	**Assist. Prof. Dr. Mustafa Berke Yelten** Istanbul Technical University	……...
	Assist. Prof. Dr. Okan Zafer Batur Istanbul Bilgi University	**.....**

Date of Submission : 04 May 2017
Date of Defense : 09 June 2017

To the memory of my father,

FOREWORD

Firstly, I would like to thank my beloved wife, Merve for her big support. She helped me to overcome all the painful times on this study. Many thanks to my parents for being with me all the time and for all their supports.

I also would like to thank my thesis advisor Assoc. Prof. Dr. Metin YAZGI, and my colleague, advisor Kemal OZANOGLU for their valuable support on this thesis and thanks to Assist. Prof. Dr. Mustafa Berke Yelten and Assist. Prof. Dr. Okan Zafer Batur for having accepted to assess my thesis.

May 2017 Türker Unutmaz

TABLE OF CONTENTS

Page

ABBREVIATIONS

AB : Adaptive bias
AC : Alternating current
CPU : Central processing unit
DC : Direct current
ESR : Equivalent series resistance
GPS : Global positioning system
GPU : Graphics processing unit
IC : Integrated circuit
IL : Inner loop
LDO : Low dropout
ML : Main loop
NMOS : Negative-channel metal oxide semiconductor
PMIC : Power management integrated circuit
PMOS : Positive-channel metal oxide semiconductor
RF : Radio frequency

LIST OF TABLES

Page

LIST OF FIGURES

Page

STABILITY ANALYSIS OF ADAPTIVELY BIASED LOW DROPOUT REGULATORS

SUMMARY

Portable mobile devices have become an essential part of our lives. With the improvements in the technology, more functionalities are implemented on the cellular phones and tablets. Increasing functionality of the portable battery powered devices lead to spectacular improvements in the power management and the efficiency topics. The industry is pushing towards the power management integrated circuits (ICs) with high power efficiency and low quiescent currents.

Since the functional blocks in a portable device requires different voltage levels, multiple voltage sources like buck converters, linear regulators or low dropout regulators (LDOs) are needed in the power management ICs. Even though switching converters exhibit higher efficiency, linear regulators are also used to supply noise sensitive analog and radio frequency (RF) circuits because of their cleaner output voltage.

LDOs have better efficiency compared to standard linear regulators. LDO design is an active research area and many publications are present in the literature about stability, low quiescent current and the transient response improvement of the LDOs. The recent papers on LDOs mainly focus on the low quiescent current and transient improvements. Adaptive biasing and dynamic biasing are the most common techniques to achieve a low quiescent current and good transient performance. This thesis focuses on the stability analysis of the adaptively biased LDOs and provides a guide for achieving stable LDOs.

In the first chapter, organization and purpose of the thesis are given. In the second chapter, some common terms related to LDOs like load transient, line transient, load regulation, etc. are defined and nonstatic biasing techniques, transient response improvements, techniques to achieve low quiescent current in the recent LDO publications are explained. In the third chapter, the main feedback loop and the inner loop in the adaptively biased LDO circuits are analyzed and the effect of the adaptive bias loop on the poles and zeros are shown. Stability criteria are obtained to overcome the stability issues caused by the adaptive biasing. The analysis results are verified by the simulation results.

ADAPTİF KUTUPLAMALI ALÇAK GERİLİM DÜŞÜMLÜ REGÜLATÖRLERİN KARARLILIK ANALİZİ

ÖZET

Teknolojinin gelişmesi ile taşınabilir cihazlar gündelik hayatımızda büyük yer kaplamaya başlamıştır. Tümdevrelerin yıldan yıla daha küçük teknolojilerde üretilebilmesi ile birlikte taşınabilir cihazlar daha çok işlem yapabilme özelliği kazanmıştır. İşlem kapasitesinin artmasıyla birlikte batarya ömrü ve verimlilik önem kazanmıştır ve bu cihazlarda kullanılan devrelerin daha düşük güçte ve yüksek verim ile çalışması için yapılan çalışmalar hız kazanmıştır. Ayrıca aynı alanda daha çok enerji depolamak için batarya teknolojileri de gelişmektedir.

Güç yönetimi tümdevreleri günümüzde kullandığımız bütün elektronik cihazlarda bulunmaktadır. Sistemde bulunan elemanların veya diğer tümdevrelerin farklı gerilim ve akım gereksinimleri bataryadan direkt sağlanamayacağından, güç yönetimi tümdevreleri sistemdeki farklı gerilim ve akım ihtiyaçlarını sisteme iletmektedir. Bir güç yönetimi tümdevresinde batarya gerilimini daha düşük gerilimlere dönüştüren gerilim azaltan dönüştürücü ve batarya geriliminden daha yüksek gerilimlere ihtiyaç duyan elemanlar için gerilim artıran dönüştürücüler bulunabilir. Gerilim dönüştürücüler anahtarlamalı ve lineer regülatörler olarak ikiye ayrılabilir. Anahtarlamalı regülatörler bir güç anahtarının açılıp kapanmasıyla çalışırlar ve çıkış geriliminde dalgalanmalara neden olabilirler fakat verimleri oldukça yüksektir. Yüksek akım gereksinimi olan blokların beslenmesinde anahtarlamalı regülatörler sıklıkla kullanılırlar. Lineer regülatörler ise güç anahtarına ihtiyaç duymazlar ve anahtarlamalı regülatörlere kıyasla daha temiz bir çıkış gerilimi üretirler ancak verimleri anahtarlamalı regülatörlere oranla daha düşüktür. Bir güç yönetimi tümdevresi ihtiyaca göre her iki tür regülatörü de içerebilir. Gürültüye duyarlı analog ve radyo frekans devreleri beslemek için lineer regülatörler kullanılırken, verimin ön plana çıktığı yerlerde anahtarlamalı regülatörler kullanılabilir.

Lineer regülatörler kullanılan geçiş transistörünün tipine göre standart lineer regülatörler veya alçak gerilim düşümlü regülatörler olarak isimlendirilirler. Alçak gerilim düşümlü regülatörler P katkılı geçiş transistörü kullanırken, standart regülatörlerde ise N katkılı geçiş transistörü kullanılır. Alçak gerilim düşümlü regülatörün verimi standart lineer regülatöre kıyasla daha yüksektir ve bu nedenle yaygın olarak kullanılmaktadırlar. Ancak alçak gerilim düşümlü regülatörlerde P katkılı geçiş transistörü kullanıldığından tümdevrede kapladığı alan standart regülatörlere kıyasla daha büyüktür ve alçak gerilim düşümlü regülatörlerin frekans kompanzasyonu standart lineer regülatörlere kıyasla daha zordur.

Düşük çalışma akımı ve yüksek verimlilik yanında regülatörlerin yük akımı değişimlerine hızlı cevap vermeleri ve çıkış gerilimlerini istenen gerilim değerinde tutmaları istenir. Son yıllarda yapılan çalışmalarda özellikle düşük çalışma akımı ve iyileştirilmiş geçici hal cevabı konularına odaklanıldığı görülmektedir. Bu iki özelliği aynı anda gerçekleştirebilmek için regülatörün kutuplama akımı sabit bir akım ve değişken bir akımın birlikte kullanıldığı yapılarla sağlanmaktadır. Bu kutuplama teknikleri adaptif ve dinamik olarak ikiye ayrılabilir. Regülatörün akımının yük akımıyla orantılı olduğu kutuplama adaptif kutuplama olarak adlandırılmaktadır. Regülatörün kutuplama akımının sadece yük akımının yükselen ve düşen kenarlarında artırılması ise dinamik kutuplama olarak adlandırılmaktadır.

Regülatörün kutuplama akımının yük akımının değerine göre adaptif olarak değiştirilmesi düşük çalışma akımını sağlamakla beraber yüksek yük akımlarında geçici hal cevabını iyileştirmektedir. Fakat adaptif kutuplama akımının belirli bir limit değerinden fazla olması halinde sisteme eklenen sıfır ve kutuplar regülatörün kararlılığını etkilemektedir. Literatürde yer alan adaptif kutuplamalı regülatörlerde adaptif kutuplama devresinin oluşturduğu çevrimin sisteme etkileri ve sonuç olarak sisteme eklenen veya değişen kutuplar ve sıfırların analizi detaylı olarak verilmemiştir. Adaptif kutuplama çevrimi minimum yük akımında dahi sistemdeki çevrimleri etkilemekte ve kararlı çalışan bir regülatörü kararsız hale getirebilmektedir. Lineer regülatörlerde adaptif kutuplama akımının sabit kutuplama akımına oranının artması düşük yük akımlarında regülatörün verimini artırmasına rağmen kararlılığı kötü yönde etkilemektedir.

Bu tezin amacı, adaptif kutuplamanın alçak gerilim düşümlü regülatörlerin çevrim kazancını nasıl etkilediğini göstermek ve adaptif kutuplamayla sisteme eklenen veya değiştirilen kutup ve sıfırların analitik olarak elde edilmesi ve kararlı bir çalışma için kararlılık kriterlerinin elde edilmesidir.

Tezin giriş bölümünden sonra ikinci bölümde yük regülasyonu, hat regülasyonu gibi lineer regülatörlerin karakteristikleriyle ilgili bazı tanımlamalar verilmiştir. Literatürde yer alan alçak gerilim düşümlü regülatörlerin frekans kompanzasyonu teknikleri, adaptif ve dinamik kutuplama ve gerilim izleyici kullanılarak yapılan alçak gerilim düşümlü regülatörler anlatılmıştır. Yük akımının değişiminin kapasitif kuplaj ile algılanarak çıkış geriliminin hızlı bir şekilde istenen gerilime gelmesine yardımcı ek devreler gösterilmiştir.

Tezin üçüncü bölümünde adaptif kutuplamalı alçak gerilim düşümlü regülatörlerin çevrim kazancı analizi yapılmıştır. Öncelikle emetör bağlamalı kuvvetlendiricinin adaptif kutuplama sağlayan transistörden gelen küçük işaret kazancının transistörlerdeki dengesizlik ile nasıl değiştiği gösterilmiş ve farksal giriş kazancı ile birlikte adaptif kutuplama transistöründen gelen küçük işaret kazancının birlikte verildiği bir model oluşturulmuştur. Bu model kullanılarak 2 katlı, NMOS transistörlerden oluşturulmuş giriş katlı bir LDO regülatörün iki farklı noktadan çevrim kazançları hesaplanmıştır. Hesap sonucu elde edilen sıfır ve kutupların transistörlerdeki dengesizlik ile nasıl değişeceği anlatılmış ve simülasyon sonuçlarıyla desteklenmiştir. Aynı şekilde 4 katlı ve PMOS transistörlerle oluşturulmuş giriş katlı bir LDO regülatörün miller kompanzasyonlu ve kompanzasyonsuz çevrim kazancı hesaplanıp sıfır ve kutupları elde edilmiştir. Yapılan hesaplar Monte Carlo simulasyonundan elde edilen sonuçlarla doğrulanmıştır. Her bir yapı için kararlı çalışma için gereken kararlılık kriteri verilmiştir. Miller kompanzasyonsuz LDO regülatörlerde adaptif kutuplama sonucunda sisteme eklenen sıfırların sadece frekanslarının kontrol edilebildiği

gösterilmiştir. Miller kompanzasyonlu LDO regülatörlerde ise adaptif kutuplamanın neden olduğu sıfırların hem frekans hem de hangi yarı düzlemde olacaklarının kontrol edilebildiği gösterilmiştir. Sistem kararlılığını bozmayan maksimum adaptif kutuplama oranının hangi adımlarla hesaplanacağı verilmiştir.

Tezin son bölümünde sonuçlar ve gelecek çalışmalar anlatılmıştır. Elde edilen sonuçlar özetlenmiştir ve adaptif kutuplama devrelerinde yapılabilecek iyiliştirmelerden kısaca bahsedilmiştir.

1. INTRODUCTION

In the past years, mobile devices entered our lives and became important day after day. Nowadays mobile devices have all the features such as playing and recording videos, running customized applications, including lots of wireless communication standards, connecting internet and more than this. These features require different circuits and systems like RF chip, GPS chip, CPU, GPU, memory and so on which require different voltage levels and currents. To create different supply voltages for the other circuits, power management integrated circuits (PMICs) are used in almost every mobile device and PMICs gained importance with the developments of the new technologies. As the trend is including more functionalities and increasing battery life of the portable systems, efficiency and low power consumption became the key parameters for the circuits. Because of that, also the circuits in the PMICs should be efficient while supplying the other blocks. The most important circuits in a PMIC are the voltage converters. These blocks create different voltage levels with different load current driving capabilities using the battery voltage. Voltage converters can be implemented in different structures such as switching DC-DC converters and linear regulators. Since the efficiency is the critical parameter switching converters are mostly used in the power management ICs. However their switching operation creates noise on the output. Noise on the supply line of the sensitive analog and RF blocks can create issues and linear regulators are the best choice for a clean supply for sensitive blocks. The efficiency of the linear regulators are not good as the switching converters but PMICs include linear regulators because of the aformentioned property. Also they occupy smaller area and their structure is relatively simple when compared to a switching converter. In addition to that in most of the applications linear regulators are connected to the output of a switching DC-DC converter to obtain a clean supply voltage from high voltage levels while maintaining an efficient operation.

In order to increase the efficiency of the linear regulators, the pass device of the linear regulators is implemented with a P type transistor and this type of linear

regulators are called low dropout regulators (LDOs). LDOs offer low dropout voltages compared to standard linear regulators but their frequency compensation is difficult and they occupy larger area compared to standard linear regulator because of the pass device type. The most important parameters for the LDOs are the low quiescent current and good load transient response and the recent studies on the LDOs in the literature mainly focus on the low power and the transient response improvements topics. Decreasing the quiescent current of the LDO for low power operation slows down the loop response of the LDO and increases the voltage drop at the output at load transients. Thus, it is a challenge to obtain good transient response with low quiescent current.

There are several methods to improve the transient response of the LDO while maintaining a low quiescent current. The common point of the methods is using non-static biasing current for the LDO to enhance the bandwidth of the loop and slew rate of gate capacitance of the pass device. Dynamic biasing is one of the methods and the idea is increasing LDO biasing current at the load transient edges. Another method is called adaptive biasing and the bias current is increased proportionally to the load current. The thesis focus on adaptively biased LDOs and the effect of adaptive biasing on the LDOs' loop gains.

1.1 Organisation of Thesis

The thesis is organized as below:

In Chapter 2, the common terms related to the LDOs are explained and standard linear regulator and low dropout regulator comparison is given. The recent studies in the literature related the frequency compensation techniques, dynamic biasing, adaptive biasing, and LDO structures formed by flipped voltage follower and class-AB input stage are briefly covered.

In Chapter 3, the analysis of adaptively biased differential pair and the analysis of adaptively biased LDOs is given for different topologies. The effect of the adaptive bias loop on the overall system's loop gain is given with the calculations. With the aid of the calculations, design criteria are obtained to achieve stable operation and calculation of optimum adaptive biasing ratio is given while maintaining the stability. Monte Carlo simulations results for different topologies and verification of

the derived design criteria are given.

In Chapter 4, the overall study is summarized and the future works are briefly covered.

1.2 Motivation

The purpose of this thesis is to show that adaptive biasing might create stability issues while improving transient response. In the literature, adaptive biasing is widely utilised on the LDOs but detailed analysis of the loop gains, zeros and the poles of the system are not given. Although advantages of the adaptive biasing is obvious in terms of DC behaviour, adaptive biasing circuit forms an additional loop in the system and affects the overall system stability. In addition to that, the mismath on the transistors in the input stage creates a huge variation on the phase margin and same LDO design might show stability problems for some parts while some parts work as expected. The reason of the stability issues and the effect of the mismatch in the first stage are analyzed. After the analysis of the adaptive bias loop on LDOs, obtaining design criteria for stability for different topologies is aimed. As adaptive biasing ratio affects the overall system stability, for a fixed bandwidth at high load currents, the tradeoff between stability and current efficiency is explained. Stability criteria have been derived. The given criteria to achieve stable operation can be used while designing a LDO. With this study, the effect of adaptive biasing on the loop gain is shown and same approach can be used for analysis of other multi loop LDO topologies.

2. LDO CONCEPTS

2.1 Definitions of Common Terms

2.1.1 Dropout voltage

Dropout voltage is the voltage difference between the input and the output of the LDO where the regulation is no longer available [1]. In this region pass device is working in triode region and acts like a resistor. The dropout voltage is given in the equation 2.1 in terms of the load current and R_{DSon} which is the resistance of the pass device.

$$V_{dropout} = I_L R_{DSon} \tag{2.1}$$

As seen in the Figure 2.1, the pass device can be modeled with a resistance and the value of the resistance is controlled by the amplifier output voltage. Since the gain of the loop is decreased because of the triode working region of pass device, the output voltage accuracy decreases in the dropout region.

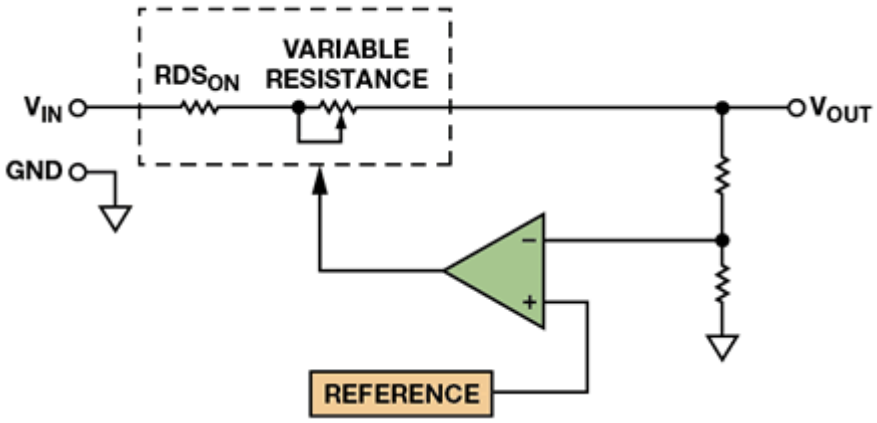

Figure 2.1 : Schematic of a LDO operating in dropout region [1].

Input/output characteristics of a commercial LDO is shown in Figure 2.2. In dropout region the LDO cannot operate functionally and output voltage decreases. In order to maximize the regulator efficiency, low dropout voltage is necessary.

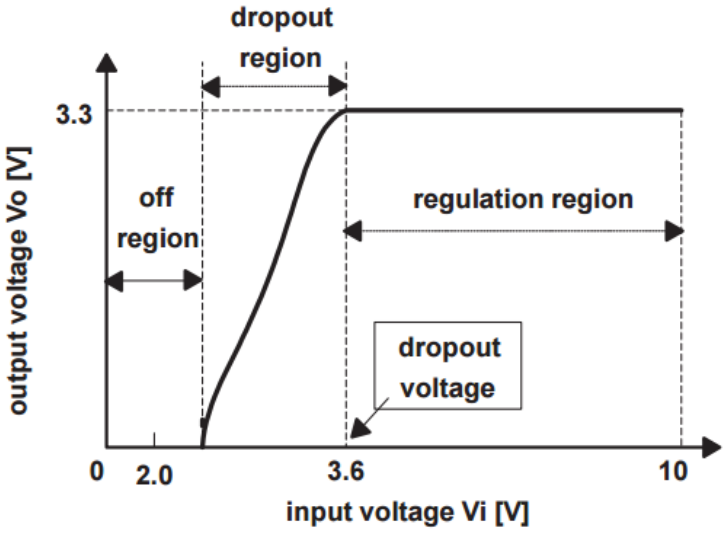

Figure 2.2 : Input/output characteristics of a commercial LDO [2].

2.1.2 Quiescent current

Quiescent current is the current difference between input and output currents. Quiescent current is consumed by the LDO in order to operate and consists of bias current of the error amplifier, 2nd and 3rd stage's bias currents and currents consumed on resistor divider and other auxilary circuts. For maximum efficiency, quiescent current of the LDO should be low. Figure 2.3 shows the quiescent current of the LDO.

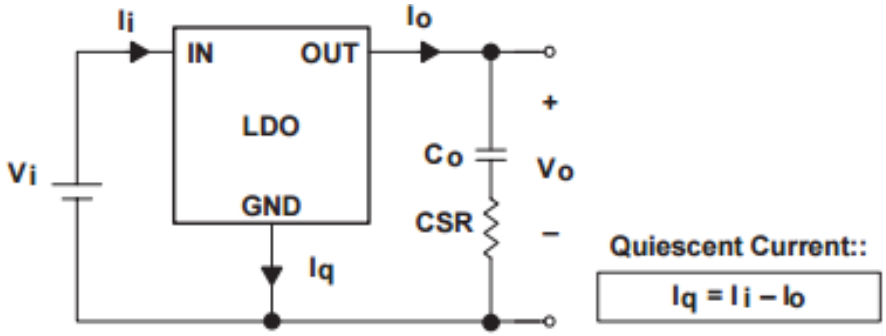

Figure 2.3 : Quiescent Current of a LDO [2].

2.1.3 Efficiency

The quiescent current and the voltage difference between input and output limits the efficiency as given in the equation 2.2 [2].

$$Efficiency = \frac{I_o V_o}{(I_o + I_q)V_i} * 100 \tag{2.2}$$

To have maximum efficiency, dropout voltage and quiescent current should be minimum and LDO should operate at the dropout voltage.

2.1.4 Load and line regulation

Load regulation reflects the ability of the LDO to keep the output voltage in the specified range under different load conditions [2]. Load regulation is a steady state metric and definition is given in the equation 2.3.

$$Load\ regulation = \frac{\Delta V_o}{\Delta I_o} \tag{2.3}$$

In Figure 2.4, in steady state output voltage varies by ΔV_2 when load current is increased by ΔI and this value is determined by the load regulation metric and load current.

Similiarly, line regulation is a metric that defines LDO's ability to maintain the output voltage in specified range under varying input voltage [2]. Line regulation is also a steady state metric and defined in the equation 2.4.

$$Line\ regulation = \frac{\Delta V_o}{\Delta V_i} \tag{2.4}$$

LDO's overall loop gain affects load and line regulation. If loop gain increases load and line regulations are improved.

2.1.5 Load and line transient response

The load transient response is the output voltage change for a load current step change. Output capacitor value, the capacitor's equivalent series resistance (ESR), the bandwidth of the LDO, slew rate of the pass device and load current profile determine the load transient response of the regulator [1]. A typical load transient response can be seen in Figure 2.4. ΔV_1 is the variation of the output voltage during load transient for a ΔI load current change.

The line transient response is the output voltage change for an input voltage step change. Slew rate and amplitude of input voltage change and the bandwidth of the LDO affect the line transient response [1].

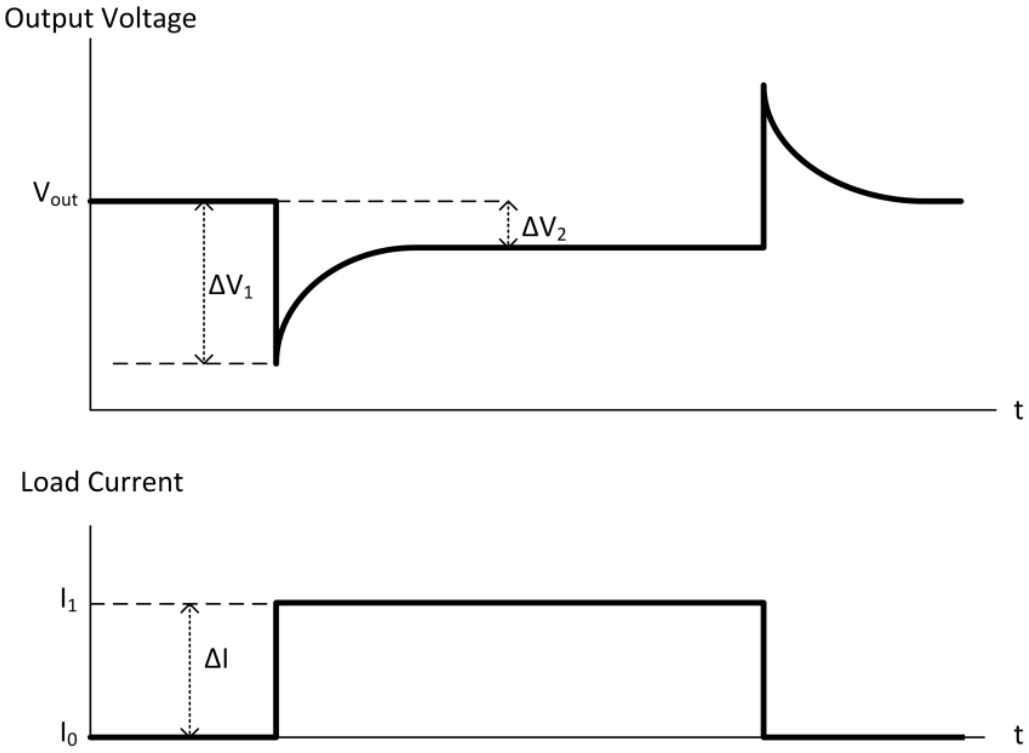

Figure 2.4 : A typical load transient response of a LDO.

2.2 Standard Linear Regulator and LDO Regulator

Linear regulator is a system that provides steady and clean supply voltage to the other circuits. It regulates the output voltage with pass device and voltage drop across pass device creates the output voltage. Scaled output voltage is sensed and compared with a reference voltage by error amplifier and gate of the pass device is driven such that error amplifier's input voltages become equal with the effect of negative feedback. Assuming error amplifier has high gain, the output voltage is given in the equation 2.5 where V_{out} and V_{ref} denote the output voltage and reference voltage, respectively. Resistor divider formed by R_1 and R_2 is used to adjust output voltage to desired value.

$$V_{out} = V_{ref}\left(1 + \frac{R_1}{R_2}\right) \tag{2.5}$$

In order to have good load transient response and maintain stability, a capacitor is generally placed at the output, but capless LDO architectures also exist where a small cap is implemented on chip and the need for an off chip capacitor is eliminated to save the PCB area.

Linear regulators are named according to the type of the pass device. Linear regulator with NMOS pass device is called standard linear regulator and linear regulator with PMOS pass device is called LDO since the dropout voltage is low compared to standard linear regulator. Due to pass device type, standard linear regulators have higher dropout voltages compared to LDOs. For a standard linear regulator, error amplifier output voltage is limited by the input voltage level and NMOS transistor has gate to source voltage. Thus, dropout voltage of standard regulator is V_{GS} of NMOS pass device. At high load condition V_{GS} voltage of NMOS pass device increases and dropout voltage also increases significantly. For a LDO, dropout voltage is defined by source to drain voltage and it has lower value compared to standard linear regulator. Although LDOs are more efficient since they have lower dropout voltages, their sizes are larger for same current drive capability because of the pass device type. Figure 2.5 shows the simple implementations of a standard linear regulator and a LDO regulator.

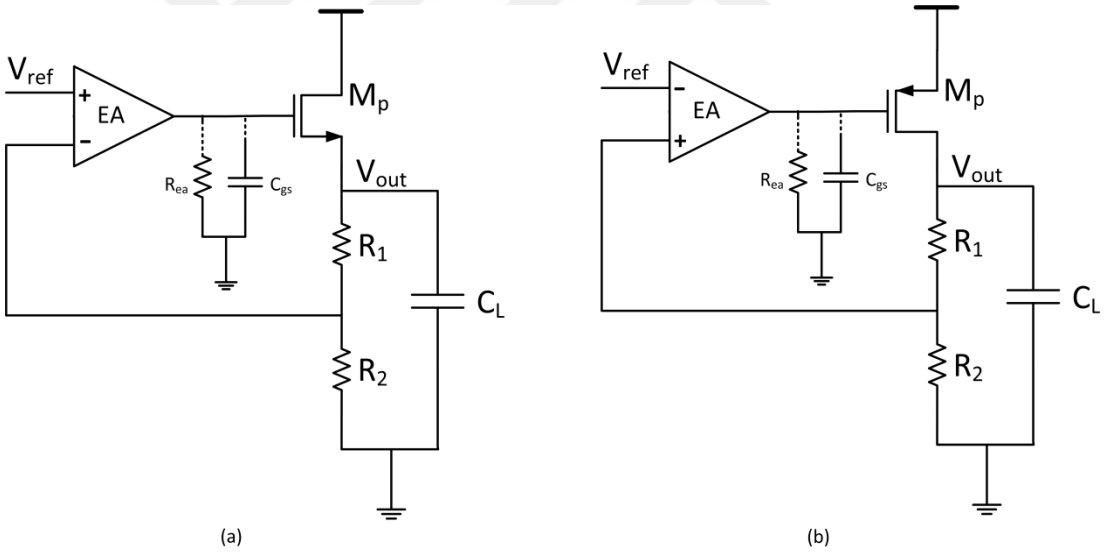

Figure 2.5 : Standard linear regulator (a) and LDO regulator (b).

When LDOs and standard linear regulators are compared in terms of the stability, frequency compensation of the LDOs is more challenging since the output pole occurs at low frequency. In standard linear regulator, the impedance seen at the output is the source of the NMOS device which is relatively low and the pole at the output occurs at relatively higher frequency.

2.3 Literature Review

Low power LDO design requires low quiescent current which creates challanges to obtain fast regulation loop. A load capacitor is used to stabilize the LDO and achieving tolerable voltage drop at the output during load transients. The voltage drop at the output can be expressed by [3]

$$\Delta V_o \approx \frac{\Delta I_o}{C_o}\left(\frac{1}{2\pi w_{ugf}} + \frac{C_g \Delta V_g}{I_{slew}}\right) \tag{2.6}$$

where C_o is the capacitor at the output, w_{ugf} is the bandwith of the loop and ΔV_g is the voltage change on the gate capacitance C_g of the pass device for a ΔI_o load change with a slewing current I_{slew}. In order to improve the transient performance of the LDO to achieve low voltage drop at the output during load transients, w_{ugf} and I_{slew} should be increased which increases the quiescent current of the LDO. If low quiescent current is targeted, constant biasing limits w_{ugf} and I_{slew}.

Nonstatic biasing is used to achieve good transient performance while maintaining low quiescent current. Recent studies in the literature show the advantage of the nonstatic biasing. Adaptive and dynamic biasing for increasing the biasing current of the LDO during load transients, as demonstrated in Figure 2.6, provide extra bias current for bandwidth extension and slew rate improvement [4].

Figure 2.6 : Adaptive biasing (a) and dynamic biasing (b) of the LDO [4].

As given in the Figure 2.6, in the adaptive biasing, bias current of the LDO is increased proportional to the load current increase. As a result both I_{slew} and w_{ugf} can

be increased. In the dynamic biasing, bias current of the LDO is increased on the load transient edges only and I_{slew} is enhanced while w_{ugf} remains same. Different biasing properties are summarized in the Table 2.1.

Table 2.1 : Comparison of different biasing schemes [3].

	Constant Biasing	Dynamic Biasing	Adaptive Biasing
w_{ugf} expansion	No	No	Yes (High)
I_{slew} enhancement	No	Yes (High)	Yes (Moderate)
Dynamic response	Slow	Moderate	Fast

In the literature LDOs utilizing adaptive biasing, dynamic biasing or adaptive and dynamic biasing are reported. High slew rate LDO regulators with class-AB error amplifier are reported in [5-8]. Figure 2.7 shows the conceptual schematic of a class-AB LDO. The current used for discharging or charging the gate capacitance of the pass device is not limited even if low I_B is used for low quiescent currents. When V_{out} voltage becomes smaller than V_{ref} or vice versa, the current supplied from the G_m cells charge or discharge the gate capacitance quickly and slew rate is improved [5]. The increasing bias current at load transient edges settles its defined value I_B in steady state. Class-AB structure can be viewed as a dynamic biasing mechanism.

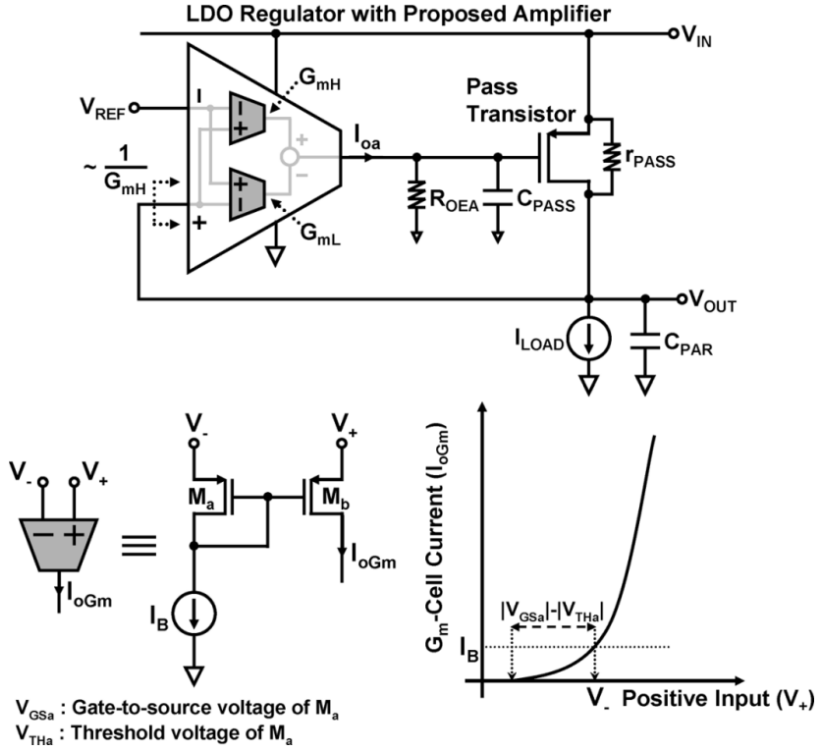

Figure 2.7 : Conceptual schematic of class-AB LDO with low Iq [5].

When the LDO load is high, pass device can be operating in the linear region in order to save the chip area. In the linear region more V_{gs} voltage variation is needed to support same current compared to operation in the saturation region. For a high speed response at the high loads, higher bandwidth and larger slew rate are required.

In [6], an adaptively biased class-AB LDO is reported. The G_m structure given in Figure 2.8 utilize adaptive biasing and dynamic biasing at the same time. I_{AB} current which is proportional to the load current is used with fixed bias current I_B to increase the bandwidth of the LDO at high loads. Moreover, to decrease the response time, a dynamic charging technique is employed since adaptive biasing is activated when the gate voltage of the pass device is decreased. When V_{out} voltage changes because of load transient, the dynamic change is coupled to the gate of the M_8 and the output current of the G_m cell is adjusted quickly to discharge or charge the gate capacitance.

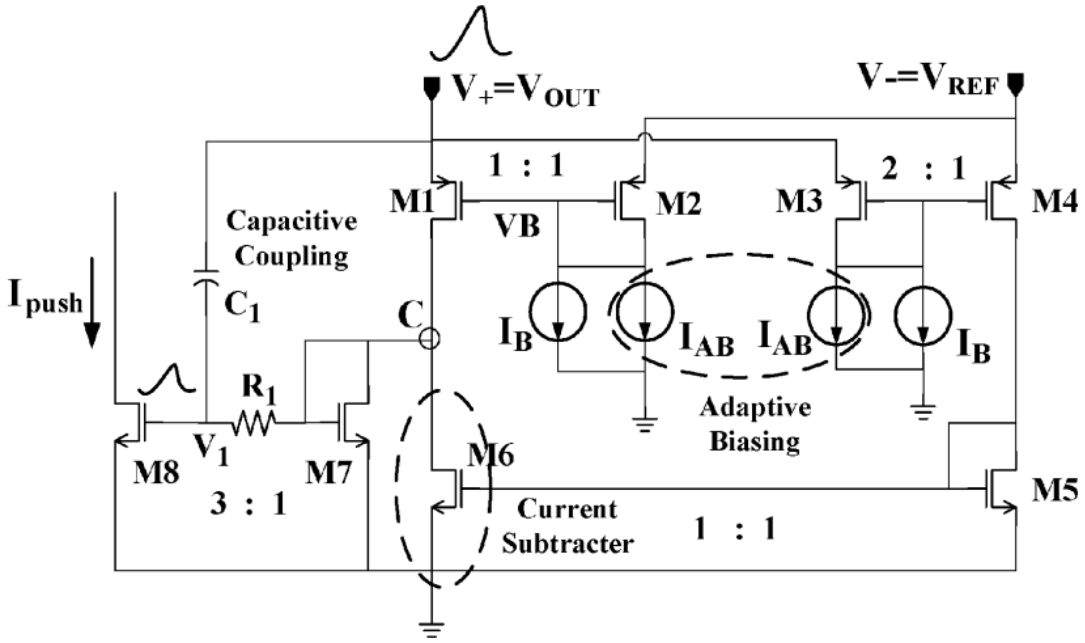

Figure 2.8 : Schematic of high bandwidth transconductance amplifier [6].

Maximum speed response of the amplifier in Figure 2.8 is mainly determined by the transconductance of the M_1 and in order to increase the g_{m1}, the biasing current is applied according to the load. The loop gain comparison of the LDOs reported in [5] and [6] are given in the Figure 2.9. At heavy loads, adaptive biasing in the [6] enlarges the bandwidth.

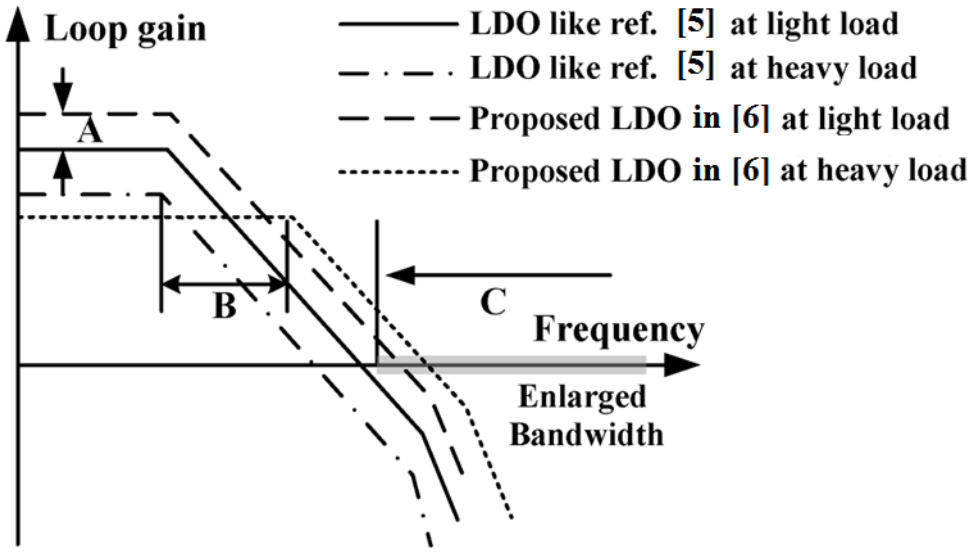

Figure 2.9 : Comparison of the loop gains for the LDOs [6].

In [9], an enhanced current mirror (ECM) buffer is used to improve the bandwidth at low load condition. Since the impedance at node Vg is ($r_{o,54} \parallel r_{o,51} \parallel 1/g_{m,50}$), at low load condition it is dominated by ($r_{o,54} \parallel r_{o,51}$) and the bandwidth is expanded relative to the ordinary current mirror (OCM) buffer. Also adaptive bias improves the transient response by increasing the slew rate at high load conditions. OCM buffer and LDO with ECM buffer are shown in Figure 2.10.

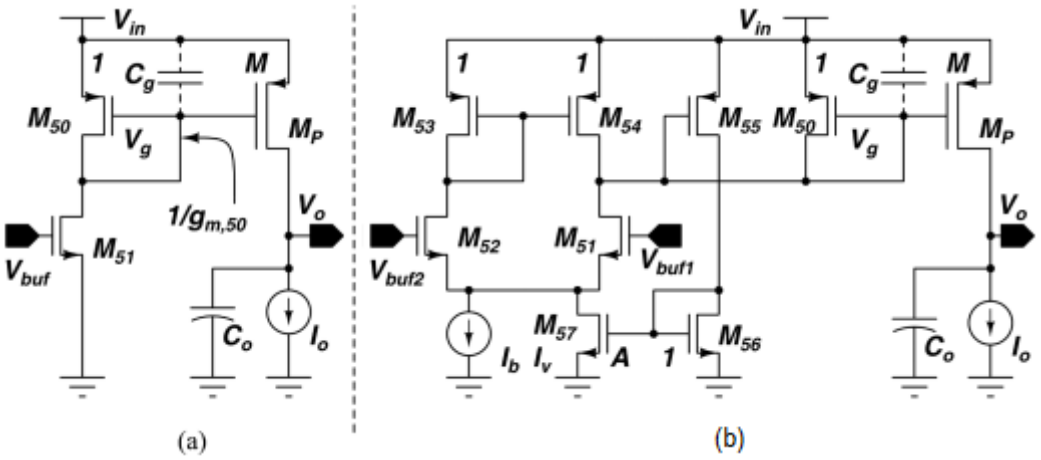

Figure 2.10 : OCM buffer (a) and Adaptively biased LDO with ECM buffer (b) [9].

Dynamic biased LDOs are reported in [10,11] where bias current is increased momentarily to increase the slew rate of the gate capacitance of the pass device. Dynamic biasing is achieved by capacitive coupling from internal node in [10] and in [11] capacitive coupling from the output node is used for sensing the output voltage drop. Dynamic biased LDO in [10] is given in Figure 2.11. In order to push the pole

at the gate of the pass device to higher frequencies for stability a buffer is used in the LDO. Overshoot and undershoot is detected by the error amplifier and amplified voltage by M_{vb1} is coupled by C_{C1} and C_{C2} to M_{vb2} and M_{vb3} to improve the slew rate of the gate voltage.

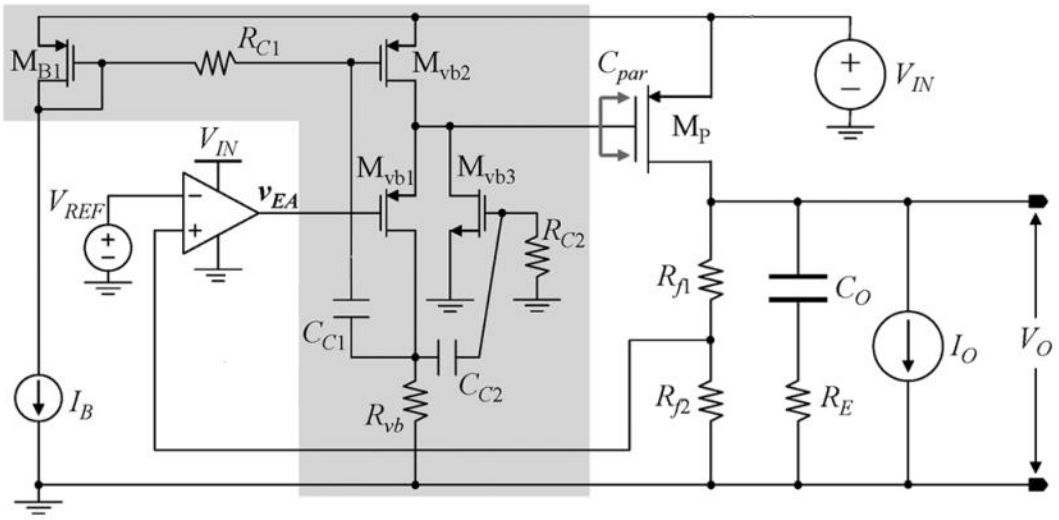

Figure 2.11 : Dynamic biased LDO with voltage buffer [10]

LDOs based on flipped voltage follower (FVF) are reported in [12-16]. The FVF LDO in [12] uses a single transistor for controlling the output voltage. Figure 2.12(a) shows the single transistor control LDO. When V_{out} is decreased, the current flowing on control transistor M_c decreases by ΔI and M_2 discharges the gate capacitance of M_{PT} by ΔI since a fixed voltage is applied to the gate of M_2. But loop gain is low since there is no additional amplifier stage. In [13], another FVF LDO is reported which is formed by the structure in [12]. Figure 2.12(b) shows the full schematic of the regulator. In order to extend the bandwidth, a load tracking impedance circuit created by the diode connected M_{07} is used. Also loop gain boosted by M_{05} and M_{06} for better load regulation.

Dynamic biased LDOs based on flipped voltage follower are reported in [14-15]. A voltage spike detection circuit based on capacitive coupling from the output node is used to increase bias current momentarily. Additional gain stages are implemented to improve load transient performance.

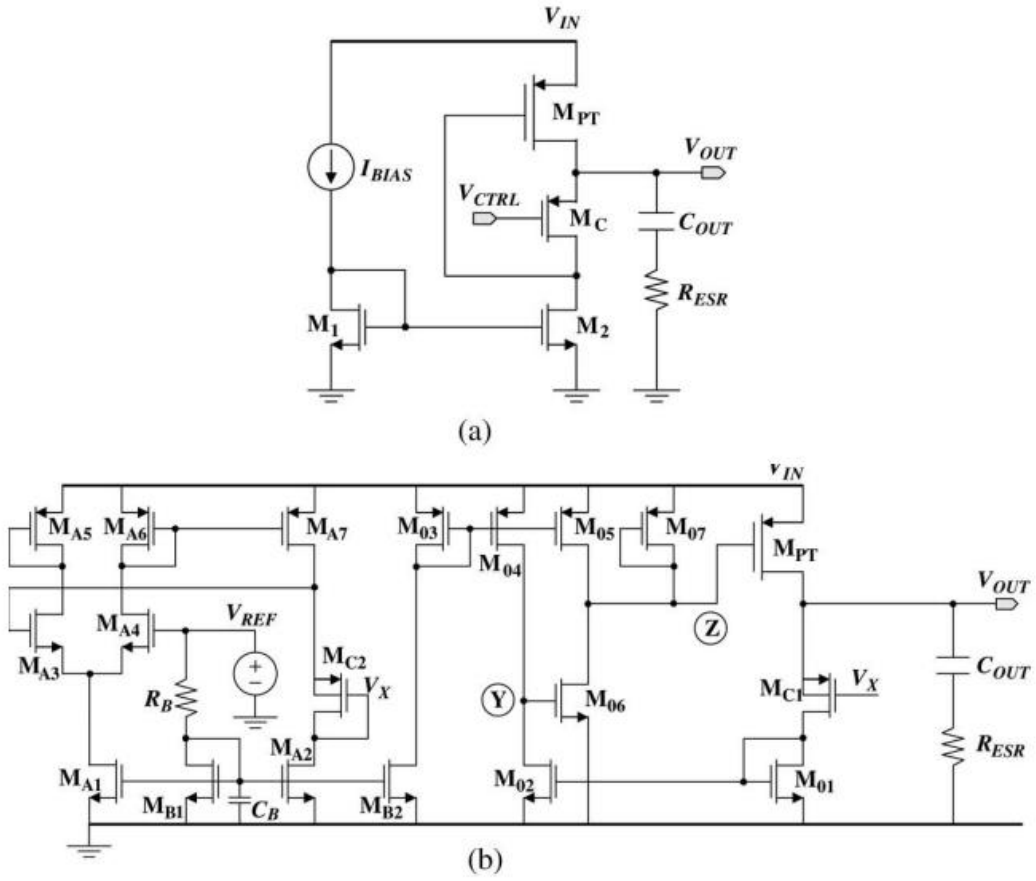

Figure 2.12 : Single transistor control LDO [12] (a) and a FVF LDO [13] (b).

In [17], a buffer is used with adaptively biased shunt feedback to decrease the output resistance and push the pole at the pass device gate beyond the unity gain frequency for different load conditions. Adaptively biased buffer with shunt feedback can be seen in Figure 2.13 and the LDO topology is illustrated in Figure 2.14.

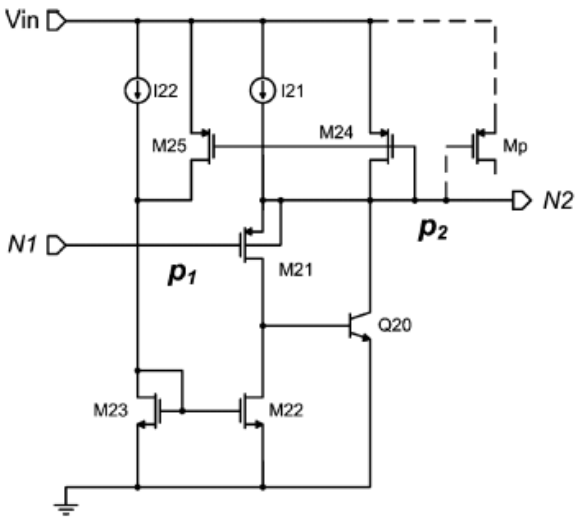

Figure 2.13 : Adaptively biased buffer with shunt feedback [17]

Negative feedback formed by the npn transistor reduces the output resistance by the current gain and adaptive biasing implemented by M_{24} and M_{25} decreases the output resistance further according to the load current. When the load current is increased, gate voltages of M_{24} and M_{25} decrease and more current flow through them. Increased bias current of M_{21} boosts the value of g_{m21} and the output resistance decreases with increasing load current. Thus, the pole at P_2 is pushed beyond the unity gain frequency for the entire load current range and bandwidth is enhanced. In order to split the poles, current buffer compensation scheme is implemented by Miller capacitor C_c.

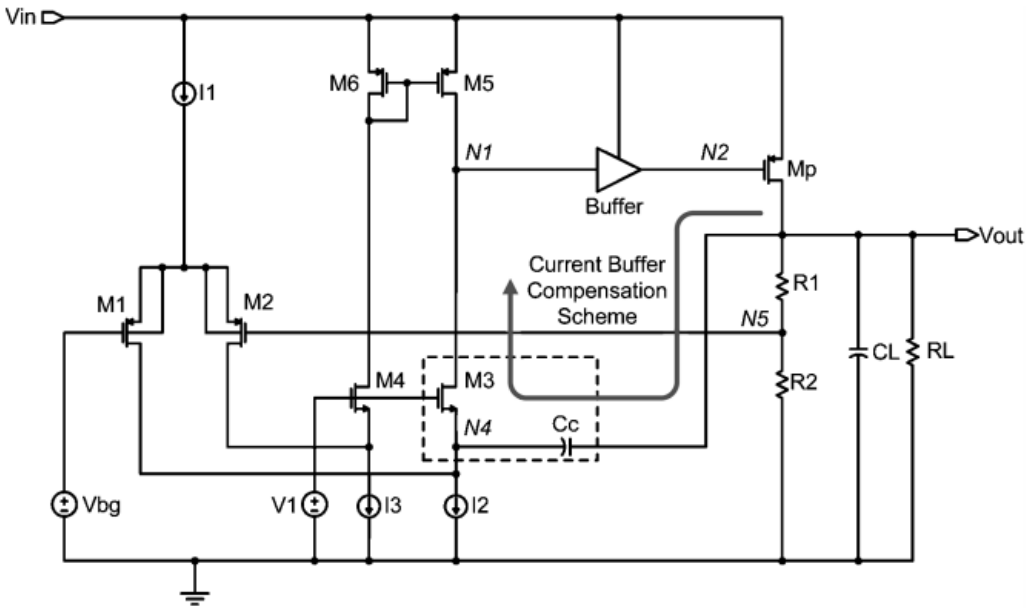

Figure 2.14 : Overall LDO schematic [17]

In [18,19], a zero is internally generated for frequency compensation and ESR zero is eliminated. The LDO regulator topology is depicted in Figure 2.15. Voltage controlled current source is implemented by a transconductance gain enhanced structure which is given in Figure 2.16. An auxiliary OTA is used to lower the impedance seen from the source of M_x to push the parasitic pole of the structure beyond the unity gain frequency. The current mirror increases the value of the effective capacitance and the zero is pushed to lower frequencies with higher mirror ratio. Although this frequency compensation technique eliminates the ESR zero and improves voltage drop at load transients, it adds more complexity to the regulator circuitry.

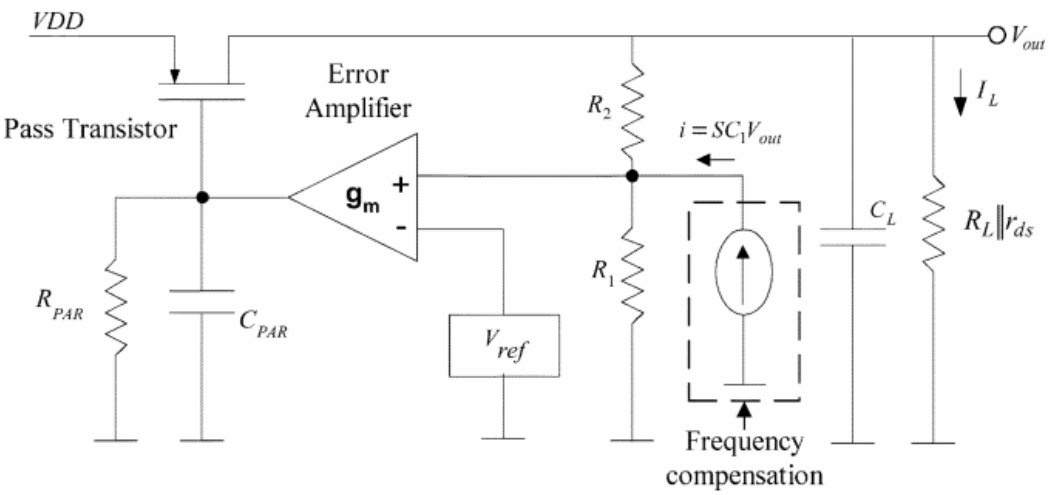

Figure 2.15 : Frequency compensation with internally generated zero [18]

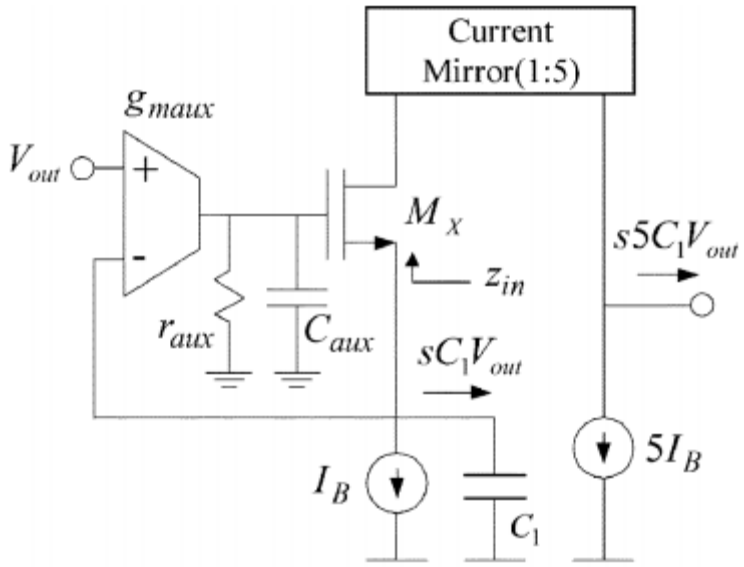

Figure 2.16 : Frequency dependent voltage controlled current source [18]

Miller compensated multistage LDOs have nondominant complex poles at low load conditions and if these poles locate near unity gain frequency, LDO becomes unstable. High Q factor of the complex poles cause sharp phase change at angular corner frequency and for a stable operation frequency of the complex poles should be pushed beyond the unity gain frequency. Q peaking can be prevented by increasing minimum load current spec or increasing Miller compensation capacitor for lowering the unity gain frequency [20]. A Q reduction circuit is reported in [20] and compensation capacitor value is reduced. The same Q reduction circuit is also used in [21,22] to reduce the minimum load current requirement.

In [21,22], error amplifier is adaptively biased to increase the bandwidth at high loads. The schematic of the adaptively biased LDO in [22] is given in Figure 2.17.

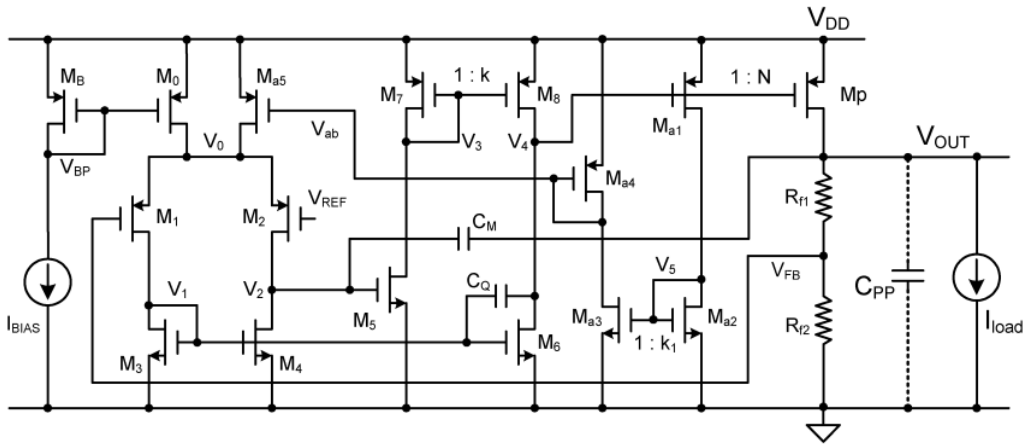

Figure 2.17 : Adaptively biased LDO reported in [22].

Main loop frequency responses of the LDO in [22] for different load currents are depicted in Figure 2.18. The UGF is given by bg_{m1}/C_M where b and g_{m1} denote the feedback ratio controlled by the resistor divider at the output and transconductance of M_1, respectively. With adaptive biasing, g_{m1} is increased when the load current is high and the UGF of the loop is enhanced while the current efficiency is still maintained high at low loads.

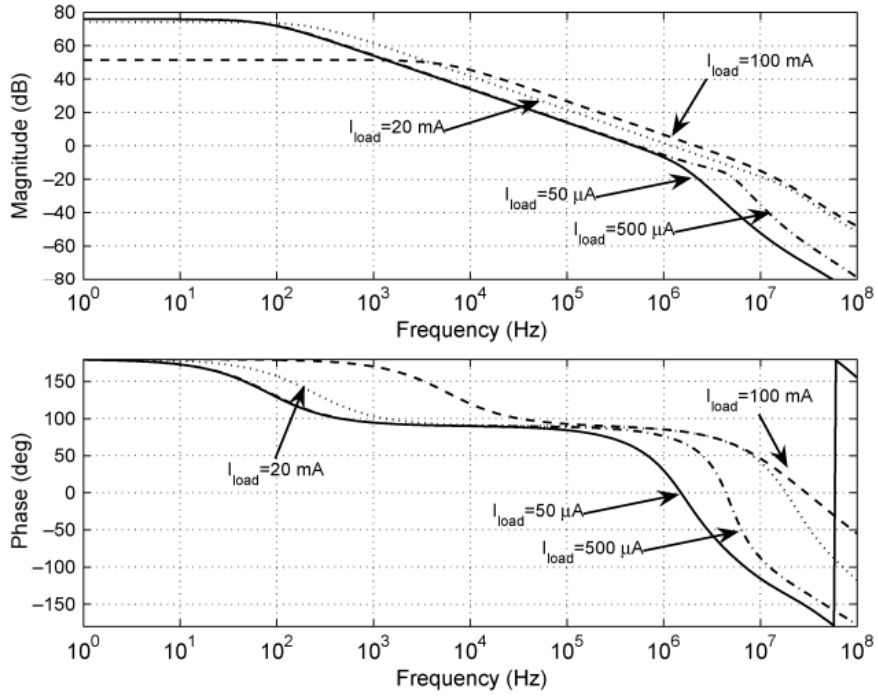

Figure 2.18 : Main loop frequency response of the LDO in [22] at different loads.

A LDO using an adaptive power transistors technique is presented in [23]. The regulator switches to a 2 stage structure when the load current is less than a defined threshold current. Thus, stability is achieved without requiring a minimum load current. Regulator transforms to a 3 stage structure when high currents are drawn and load regulation is improved. With this structure, Q peaking of the complex poles near UGF is prevented.

In [24], a linear regulator topology that emulates a replica biased source follower to achieve a fast load regulation is presented. Block diagram of the LDO is given in Figure 2.19 and the schematic of the P stage is depicted in Figure 2.20. V_{OUT0} tracks the reference voltage with the feedback loop via amplifier A_0 and since output buffers are matched, V_{OUT} is equal to V_{OUT0} at zero load current. Load regulation is achieved by a fast feedback loop within the P stage buffer whose aim is to preserve V_{OUT} at the same voltage irrespective of the load current. Voltage positioning concept is implemented for the optimum drop response since dc and ac voltage drops at the output are equal.

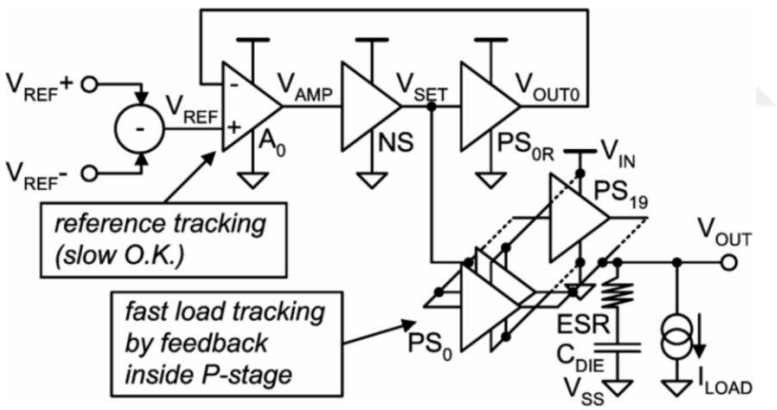

Figure 2.19 : Block diagram of the LDO [24]

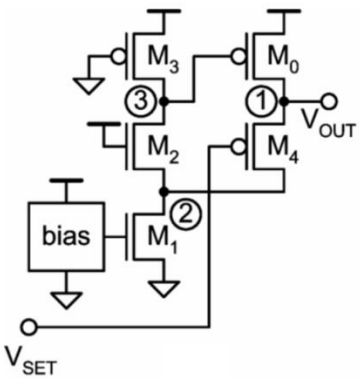

Figure 2.20 : Schematic of the P stage [24]

Capacitor-less LDOs reported in [25-28] do not require off chip capacitor and reduce the PCB layout space. Since the dominant pole is located inside the LDO, active feedback compensation technique is implemented in [26] and damping factor control frequency compensation is used in [27] for a stable operation for entire load range. Since the capacitor used at the output is small, a fast loop is needed to recover the output voltage quickly.

3. ANALYSIS OF AB LOOP

As given in Figure 2.18, adaptive biasing improves the bandwidth of the LDO by increasing the tranconductance of the first stage. When the load current is increased, additional current is used for the tail current of the first stage and the currents flowing through input transistors are increased. But adaptive biasing circuit forms a closed cloop in the system and the effects of it should be investigated in order to prevent stability problems. The adaptive bias loop is formed from the pass device gate to the output of the differential pair over the adaptive biasing transistor.

In order to analyze the loop gain of the overall system, the small signal equiavelent circuit should be obtained for the LDO. The key block in the adaptively biased LDO is the block whose bias current changes proportional to the load current. In this study LDOs that use differential pair for the first stage are analyzed and first, an adaptively biased differential pair is analyzed. A small signal model is obtained for the adaptively biased differential pair and with the aid of this model a 2 stage LDO with NMOS input stage and 4 stage LDOs with PMOS input stage are investigated in terms of stability.

3.1 Analysis of Adaptively Biased Differential Pair

Figure 3.1 shows the input stage of an adaptively biased LDO circuit. M_0 is biased by a fixed voltage V_{bp} and M_{ab} is controlled by V_{ab} which can vary with the load applied to the LDO. In order to analyze the LDO with the adaptive bias loop, the transfer function from V_f to V_{o1} should be obtained for the input stage when the AC differential input is 0. As a simple analysis, if V_f changes by ΔV, it introduces a change of ΔI for the input transistors and these currents flow in the same direction. Since I_{D1} is changed by ΔI, I_{D3} also changes by ΔI and this current is copied to I_{D4}. As a result, the additional ΔI current created by M_2 is canceled by M_4 and V_{o1} does not change which shows that V_{o1} / V_f is equal to 0.

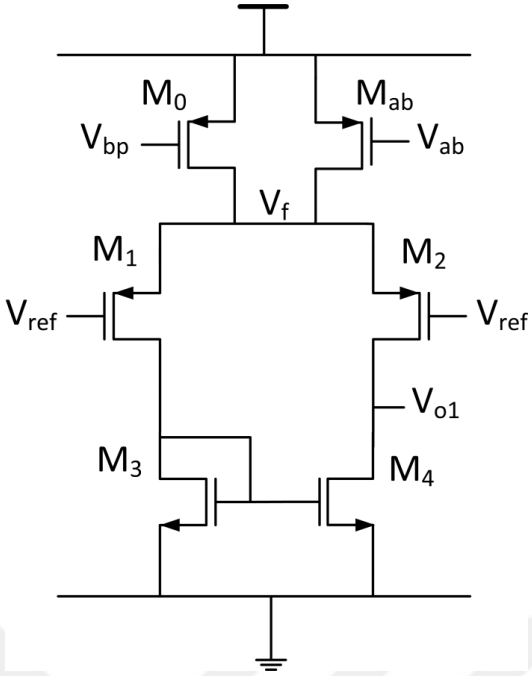

Figure 3.1 : Differential pair with adaptive bias

The detailed analysis of Figure 3.1 shows that V_{o1} / V_f is not 0 even for perfectly matched devices since the load impedance seen by M_1 is $(1/g_{m3})//r_{o3}$ and r_{o4} for M_2 and the impedance difference is generally neglected in most cases.

Small signal equivalent circuit of the differential pair in Figure 3.1 can be seen in Figure 3.2. The transconductance and the output resistance of the transistors are denoted by g_{mi}, r_{oi} (for i=1..4), respectively. C_x and C_{o1} denotes the total capacitance at V_x and V_{o1} to ground, respectively.

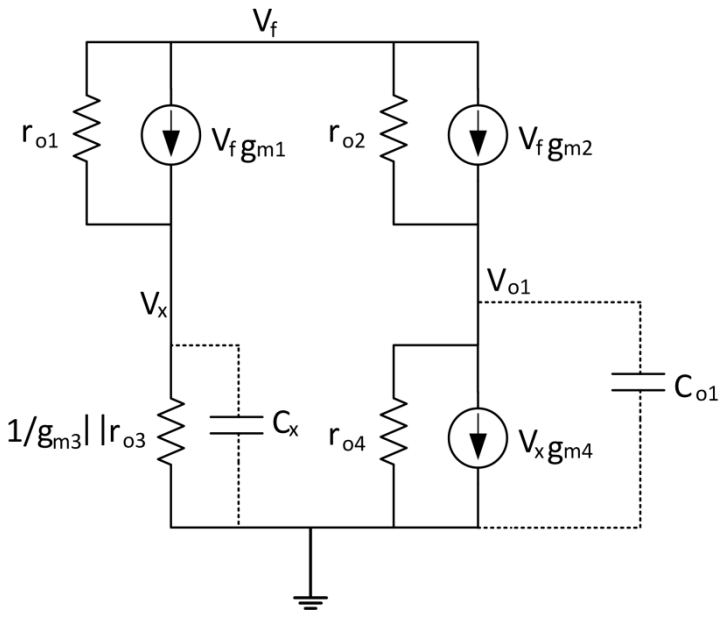

Figure 3.2 : Small signal equivalent circuit for differential pair

From the small signal equivalent circuit, V_x is obtained as

$$V_x = \left(r_{o3} \| \frac{1}{g_{m3}} \| \frac{1}{sC_x} \right) \left(g_{m1} V_f + \frac{V_f - V_x}{r_{o1}} \right) \tag{3.1}$$

and the transfer function V_x / V_f can be calculated as

$$\frac{V_x}{V_f} = \frac{\left(r_{o3} \| \frac{1}{g_{m3}} \| \frac{1}{sC_x} \right) \left(g_{m1} + \frac{1}{r_{o1}} \right)}{1 + \frac{1}{r_{o1}} \left(r_{o3} \| \frac{1}{g_{m3}} \| \frac{1}{sC_x} \right)}. \tag{3.2}$$

V_{o1} is given by

$$V_{o1} = \left(\frac{V_f - V_{o1}}{r_{o2}} + g_{m2} V_f - g_{m4} V_x \right) \left(r_{o4} \| \frac{1}{sC_{o1}} \right) \tag{3.3}$$

Substituting for V_x from equation 3.2, the overall transfer function, $A_f = V_{o1} / V_f$ obtained as

$$A_f = \frac{\left(g_{m2} + \frac{1}{r_{o2}} \right) \left(1 + r_{o1} \left(sC_x + g_{m3} + \frac{1}{r_{o3}} \right) \right) - (1 + g_{m1} r_{o1}) g_{m4}}{\left(\frac{1}{r_{o4}} + \frac{1}{r_{o2}} + sC_{o1} \right) \left(1 + r_{o1} \left(sC_x + g_{m3} + \frac{1}{r_{o3}} \right) \right)}. \tag{3.4}$$

Low frequency gain of the transfer function A_f is given in equation 3.6.

$$A_f = \frac{V_{o1}}{V_f} = A_f |_{DC} \frac{\left(1 + \frac{s}{w_{z1}} \right)}{\left(1 + \frac{s}{w_{p1}} \right) \left(1 + \frac{s}{w_{p2}} \right)} \tag{3.5}$$

$$A_f |_{DC} = \frac{\left(g_{m2} + \frac{1}{r_{o2}} \right) \left(1 + r_{o1} \left(g_{m3} + \frac{1}{r_{o3}} \right) \right) - (1 + g_{m1} r_{o1}) g_{m4}}{\left(\frac{1}{r_{o4}} + \frac{1}{r_{o2}} \right) \left(1 + r_{o1} \left(g_{m3} + \frac{1}{r_{o3}} \right) \right)} \tag{3.6}$$

The pole and zero locations of the transfer function A_f are given in equations 3.7, 3.8 and 3.9, respectively.

$$w_{p1} = \frac{1}{(r_{o4} \| r_{o2}) C_{o1}} \tag{3.7}$$

$$w_{p2} = \frac{1}{\left(r_{o1} \| \frac{1}{g_{m3}} \| r_{o3} \right) C_x} \tag{3.8}$$

$$w_{z1} = -\frac{(1 + g_{m1} r_{o1})\, g_{m4} - \left(g_{m2} + \frac{1}{r_{o2}} \right) \left(1 + r_{o1} \left(g_{m3} + \frac{1}{r_{o3}} \right) \right)}{\left(g_{m2} + \frac{1}{r_{o2}} \right) r_{o1} C_x} \tag{3.9}$$

If $g_m r_o >> 1$, then the zero can be expressed as given in 3.10.

$$w_{z1} \approx -\frac{g_{m1}\, g_{m4} - \left(g_{m2} + \frac{1}{r_{o2}} \right) \left(g_{m3} + \frac{1}{r_{o3}} \right)}{\left(g_{m2} + \frac{1}{r_{o2}} \right) C_x} \tag{3.10}$$

From equation 3.10, it can be seen that w_{z1} location depends on the mismatch of the transistors and its location is at the relatively low frequencies.

Equations 3.6 and 3.9 show that the numerator of the $A_f|_{DC}$ has the same sign of the numerator of w_{z1} which reveals that if $A_f|_{DC}$ is positive, the transfer function has a left half plane (LHP) zero otherwise it has a right half plane (RHP) zero. Another result obtained from the equation 3.6 is for perfectly matched input transistors $A_f|_{DC}$ will be positive and w_{z1} will be a LHP zero. The bode plots of the transfer function V_{o1} / V_f of the circuit in Figure 3.1 with perfectly matched transistors are given in Figure 3.3. In this simulation the size of M_1-M_2 and M_3-M_4 are selected as W/L=30u/5u and W/L=5u/10u, respectively and a fixed bias current of 250nA is used. 1pF cap is used at the output of the differential pair. DC gain, w_{p1} and w_{z1} are measured as 2.45dB, 395Hz and 2.4kHz, respectively. The zero is located between the first and the second pole and it is at relatively low frequency.

Figure 3.4 shows the Monte Carlo simulation results of the same circuit for 200 points. The bode plots are drawn for A_f transfer function. The gain changes between +16dB and -43dB and the locations of w_{p1} and w_{z1} also vary. For the points where the phase starts from 180°, the transfer function shows a negative gain and as a result w_{z1} is located in RHP. -90° phase shift is introduced by the pole w_{p1} and another -90° phase shift is introduced by the RHP zero w_{z1} which create a total phase change of -180°. For the points where the phase starts from 0°, the pole w_{p1} and the LHP zero w_{z1} introduce a total phase change of 0°. All Monte Carlo points reach almost 0°

before the second pole $w_{p2.}$

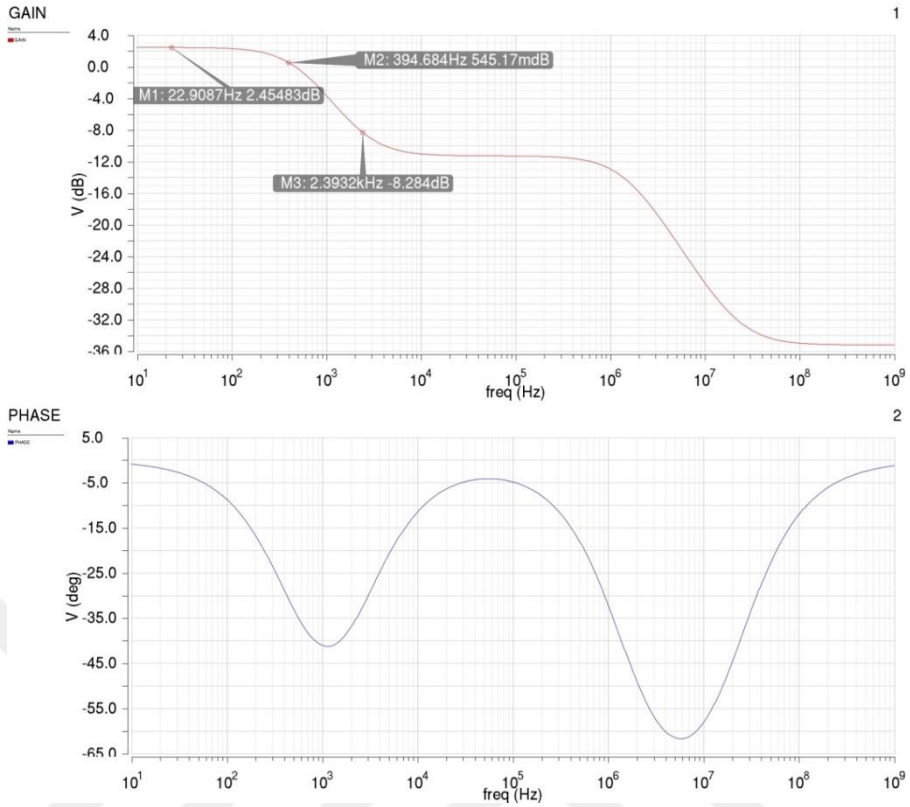

Figure 3.3 : Bode plots of the transfer function A_f for perfectly matched transistors.

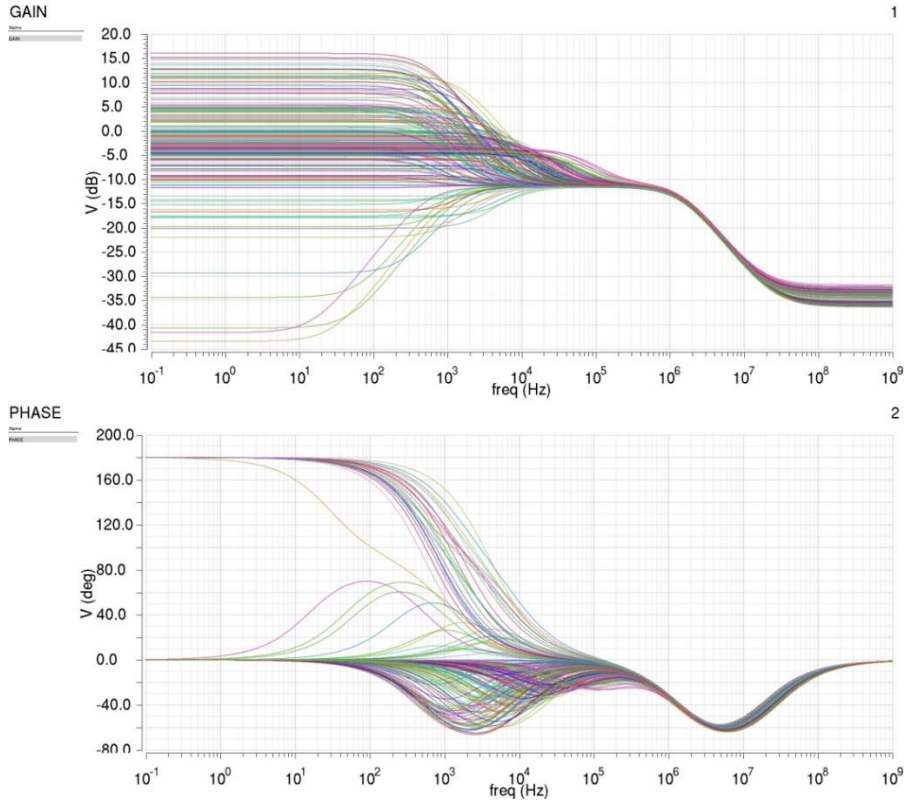

Figure 3.4 : Bode plots of the transfer function A_f for 200 Monte Carlo points.

Transfer function from differential inputs to the output, $A_d = V_{o1} / V_{in}$, where V_{in} is the differential input voltage is given in equation 3.11. $A_d|_{DC}$ presents the DC gain of A_d which is $g_{m1,2}(r_{o4} \parallel r_{o2})$ and the poles and the zero locations are given in equation 3.12, 3.13 and 3.14, respectively [29].

$$A_d = \frac{V_{o1}}{V_{in}} = \quad A_d|_{DC} \frac{\left(1 + \frac{s}{w_{z1}}\right)}{\left(1 + \frac{s}{w_{p1}}\right)\left(1 + \frac{s}{w_{p2}}\right)} \tag{3.11}$$

$$w_{p1} \approx \frac{1}{(r_{o4||}\, r_{o2})\, C_{o1}} \tag{3.12}$$

$$w_{p2} \approx \frac{g_{m3}}{C_x} \tag{3.13}$$

$$w_{z1} = 2w_{p2} \tag{3.14}$$

If the poles and the zeros of the transfer functions A_d and A_f are compared it can be seen that A_d and A_f have same poles but the zeros are different. The zero associated with the A_d is located at higher frequencies compared to the zero of the A_f. In order to combine the transfer functions, DC gains of A_d and A_f can be expressed by transconductances multiplied by the output resistance of the differential pair which is same for both of them and given by $r_{o4} \parallel r_{o2}$.

$$A_d|_{DC} = G_{m1} R_{o1} \tag{3.15}$$

$$A_f|_{DC} = G_{m1f} R_{o1} \tag{3.16}$$

The output resistance of the differential pair, $R_{o1,}$ and w_{p1} are common for the transfer functions A_d and A_f, so using the superposition property of the linear systems, $V_{in}G_{m1}$ and $V_f G_{m1f}\left(1 + \frac{s}{w_{z1}}\right)$ currents can be summed, where w_{z1} denotes the zero of the A_f. G_{m1} and G_{m1f} are the transconductances given in equation 3.17 and 3.18, respectively. The circuit that can be used to model an adaptively biased differential pair can be seen in Figure 3.5. In this circuit, non-dominant poles of the transfer functions and the zero of A_d are neglected since they are located at higher frequencies.

$$G_{m1} = g_{m1,2} \tag{3.17}$$

$$G_{m1f} = \frac{\left(g_{m2} + \frac{1}{r_{o2}}\right)\left(1 + r_{o1}\left(g_{m3} + \frac{1}{r_{o3}}\right)\right) - (1 + g_{m1}r_{o1})g_{m4}}{\left(1 + r_{o1}\left(g_{m3} + \frac{1}{r_{o3}}\right)\right)} \tag{3.18}$$

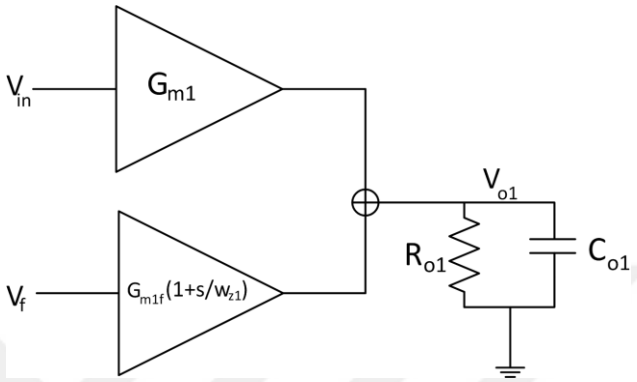

Figure 3.5 : Equivalent circuit for an adaptively biased differential pair

3.2 Analysis of Adaptively Biased 2 Stage LDO with NMOS Input Stage

Figure 3.6 shows an adaptively biased 2 stage LDO. Input stage consists of a differential pair with active load.

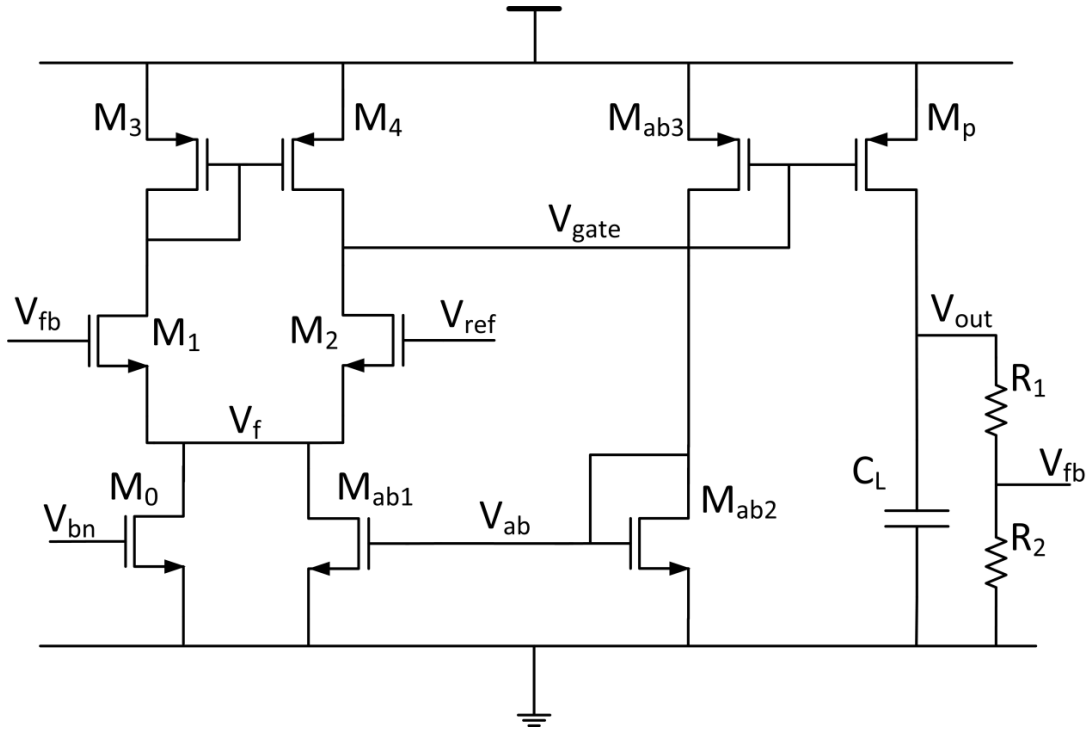

Figure 3.6 : Schematic of an adaptively biased 2 stage LDO with NMOS input stage

The second stage includes the pass device. Since the gate of M_{ab3} is connected to V_{gate} which is the gate voltage of the pass device, a current proportional to the load current is mirrored by M_{ab2} and M_{ab1}. This current is used as the tail current of the differential pair in addition to the fixed bias current by created by M_0.

Voltage divider is used to adjust the output voltage according to expression below:

$$V_{out} = V_{ref}\left(1 + \frac{R_1}{R_2}\right) \tag{3.19}$$

This LDO includes 2 separate loops; one is from the output of the voltage divider V_{fb} to the input of the differential pair and the other is from V_{gate} to V_f node of the differential pair over the transistors M_{ab1}, M_{ab2}, M_{ab3}. Equivalent small signal circuit is given in the Figure 3.7. g_{m1}, r_{o1}, c_{o1} present the transconductance of the first stage, output resistance of the first stage and the total capacitance at node V_{gate} to the ground, respectively. g_{mp} is the transconductance of the pass device and R_L and C_L are the output resistance and the load capacitance of the regulator. g_{mab} denotes the transconductance of the adaptive bias circuit, which is given as below:

$$g_{mab} = \frac{g_{mab3}}{g_{mab2}}\, g_{mab1} \tag{3.20}$$

The input stage is modeled by the circuit given in Figure 3.5. r_{in1} shows the input resistance at node V_f. Current created by g_{mab} is multiplied by r_{in1} and creates the voltage V_f.

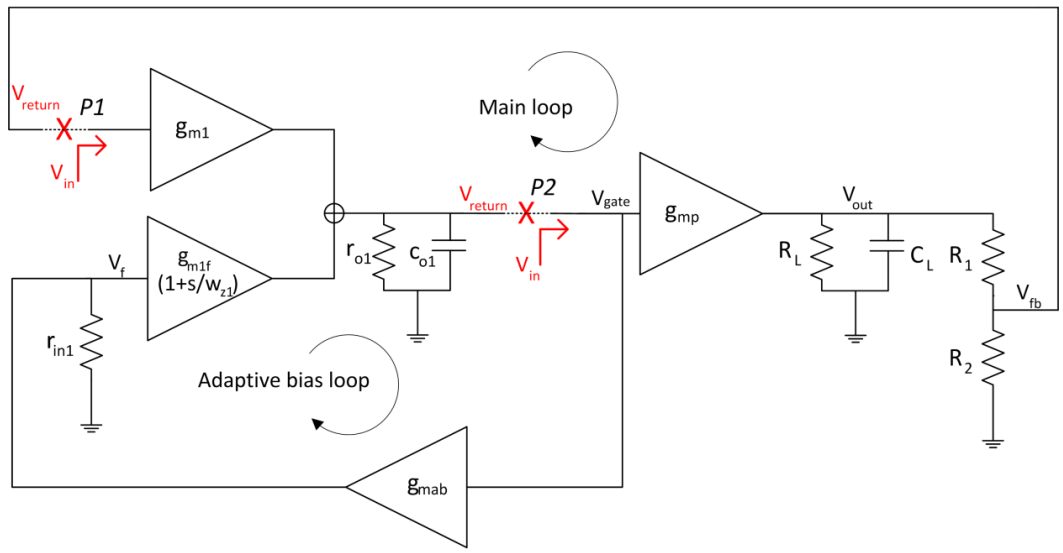

Figure 3.7 : Small signal equivalent of the circuit in Figure 3.6

Loop gain can be calculated by breaking the feedback loops at the points P1 and P2. As can be seen from Figure 3.7, point P2 is the intersection point of the main loop and the adaptive bias loop.

In order to find the loop gain by breaking the loop at P1, if the currents summed up at V_{gate} node;

$$V_{in}g_{m1} + V_{gate}g_{mab}r_{in1}g_{m1f}\left(1 + \frac{s}{w_{z1}}\right) - \frac{V_{gate}}{r_{o1}} - V_{gate}\, sc_{o1} = 0 \tag{3.21}$$

obtaining

$$\left[V_{in}g_{m1} + V_{gate}g_{mab}r_{in1}g_{m1f}\left(1 + \frac{s}{w_{z1}}\right)\right]\frac{r_{o1}}{1 + \frac{s}{w_{p1}}} = V_{gate}\,. \tag{3.22}$$

In equation 3.22, w_{p1} is the pole at the node V_{gate}, given as $1/r_{o1}c_{o1}$. Similarly when the currents summed up at the node V_{out};

$$V_{gate}g_{mp} - \frac{V_{out}}{R_{Leq}} - V_{out}\, sC_L = 0\,, \tag{3.23}$$

obtaining

$$\frac{V_{gate}g_{mp}R_{Leq}}{1 + \frac{s}{w_{p2}}} = V_{out} \tag{3.24}$$

where R_{Leq} is the equivalent resistance R_L // (R_1+R_2) at the output and w_{p2} is the pole at the output, $1/R_{Leq}C_L$.

Substituting for V_{gate} from the equation 3.24, the equation 3.22 gives:

$$\frac{V_{return}}{V_{in}}\Big|_{ML} = \frac{\beta V_{out}}{V_{in}} = \frac{\beta g_{m1}r_{o1}g_{mp}R_{Leq}}{\left(1 + \frac{s}{w_{p2}}\right)\left(1 - A_{ab}|_{DC} + s\left(\frac{1}{w_{p1}} - \frac{A_{ab}|_{DC}}{w_{z1}}\right)\right)} \tag{3.25}$$

$$A_{ML} = \frac{V_{return}}{V_{in}}\Big|_{ML} = \frac{\frac{\beta g_{m1}r_{o1}g_{mp}R_{Leq}}{1 - A_{ab}|_{DC}}}{\left(1 + \frac{s}{w_{p2}}\right)\left(1 + \frac{s}{w_{p1ab}}\right)} \tag{3.26}$$

$A_{ab}|_{DC}$ is the adaptive bias loop gain at low frequencies given by $g_{mab}r_{in1}g_{m1f}r_{o1}$. β

is the feedback ratio of the resistor divider at the output. The loop gain has 2 poles with the magnitudes of w_{p2} and w_{p1ab}. When the adaptive bias loop is added to the two stage LDO, the pole at the output node remains same but the pole magnitude associated with the V_{gate} node changes to w_{p1ab}:

$$w_{p1ab} = \frac{1 - A_{ab}|_{DC}}{\frac{1}{w_{p1}} - \frac{A_{ab}|_{DC}}{w_{z1}}} \tag{3.27}$$

If $1/w_{p1} >> A_{ab}|_{DC} / w_{z1}$, w_{p1ab} can be expressed as,

$$w_{p1ab} = w_{p1}(1 - A_{ab}|_{DC}) \tag{3.28}$$

This result can be obtained by using the series-shunt feedback properties. Adaptive bias loop divides the output resistance of the first stage by (1-$A_{ab}|_{DC}$) and multiplies the bandwidth by (1-$A_{ab}|_{DC}$).

Since $A_{ab}|_{DC}$ is varying with the mismatch on the first stage transistors, w_{p1ab} also varies depending on the gain of the adaptive bias loop. To see this effect two separate Monte Carlo simulations are run for 200 points where the external load current is 0mA and only a small current flows through the pass device for resistor divider. 50nA fixed bias current is used and adaptive bias ratio is selected as 1/800. In the first simulation the adaptive bias loop is broken by blocking the AC signal propagation in the adaptive bias loop, so that the DC bias conditions are not changed. The second simulation is done with the adaptive bias loop. Figure 3.8 shows the gain and phase of the main loop where adaptive bias loop is broken. Maximum and minimum DC gains are measured as 86.6dB and 83.4dB, respectively. The location of the w_{p1} also changes between 60Hz and 119Hz. Minimum and maximum value of the phase margin are measured as 62.2° and 77.3°. Figure 3.9 shows the second simulation with the adaptive bias loop. The maximum and the minimum values of DC gain and w_{p1ab} are 107.3dB, 151.2Hz and 80.2dB, 6.6Hz, respectively. Since $A_{ab}|_{DC}$ is smaller than 1 in most of the points, the main loop gain increases compared to the one where adaptive bias loop is broken. Minimum and maximum values of the phase margin are 7.4° and 83.5°. Since the adaptive bias loop changes the pole at the output of the first stage, phase margin is affected significantly.

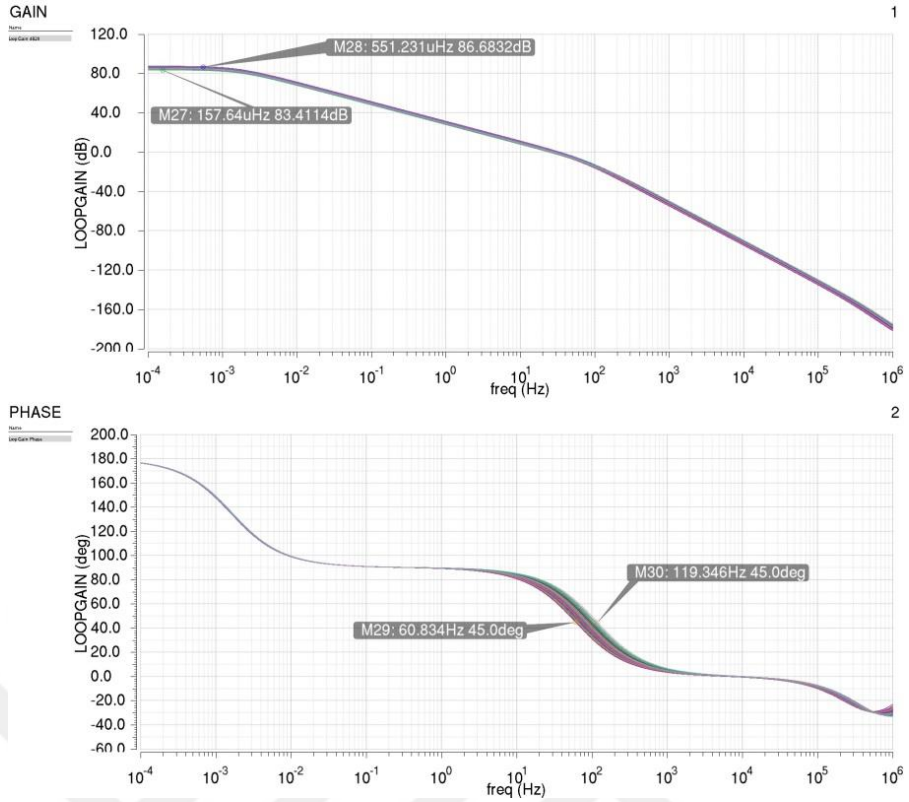

Figure 3.8 : Bode plots of A_{ML} of LDO with NMOS input stage for 200 MC points w/o AB

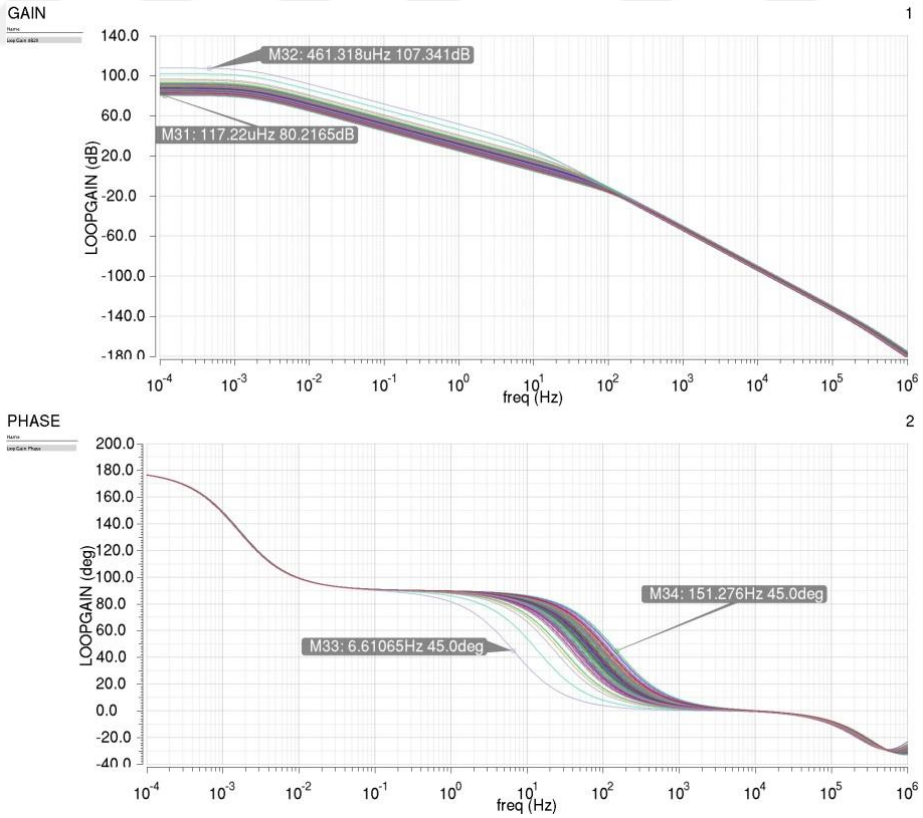

Figure 3.9 : Bode plots of A_{ML} of LDO with NMOS input stage for 200 MC points w/ 1/800 AB ratio

If the circuit is stable before placing an adaptive bias loop and if w_{p1} movement is not desired 1-$A_{ab}|_{DC}$ should be close to 1, that is, $A_{ab}|_{DC} << 1$.

Since $A_{ab}|_{DC}$ is $g_{mab}r_{in1}g_{m1f}r_{o1}$ and r_{in1} is the input resistance seen from V_f node of the differential pair, r_{in1} can be expressed by $(\frac{1}{g_{m1}} || \frac{1}{g_{m2}})$ which is $\frac{1}{2g_{m1}}$ and equation 3.29 is obtained.

$$A_{ab}|_{DC} = \frac{g_{mab}g_{m1f}r_{o1}}{2g_{m1}} \ll 1 \tag{3.29}$$

$A_{ab}|_{DC}$ can be controlled by g_{mab} which is proportional to the I_{ab}. The tail current of the input stage can be expressed by I_{ab}+I_{fb}, where I_{ab} is adaptive bias current and I_{fb} is fixed bias current. At the maximum load condition, the tail current has its maximum value and it increases the slew rate of the gate capacitance of pass device. For a specific slew rate, tail current has a corresponding value and at maximum load condition if I_{ab} is limited for stability, I_{fb} should be increased in order to have same tail current. Thus, increasing the fixed bias current while decreasing the adaptive bias current (for a fixed tail current and fix g_{m1}) limits the pole movement at the output of the first stage according to equation 3.29.

When the adaptive bias ratio is set to 1/7200 to decrease g_{mab}, and limit w_{p1ab} variation, phase margin is improved. Figure 3.10 shows the bode plots of A_{ML} for 200 MC points and phase margin is measured between 59.4° and 77.9°.

In order to find the inner loop gain, the feedback loop is broken at P2. With the aid of the Figure 3.7, starting from V_{gate}, the return voltage, $V_{return,}$ is given below:

$$\left(V_{in}g_{mp}R_L \frac{1}{\left(1+\frac{s}{w_{p2}}\right)} \beta g_{m1} + V_{in}g_{mab}r_{in1}g_{m1f}\left(1+\frac{s}{w_{z1}}\right) \right) r_{o1} \frac{1}{\left(1+\frac{s}{w_{p1}}\right)} \tag{3.30}$$

and hence inner loop gain $A_{IL} = \frac{V_{return}}{V_{in}}|_{IL}$,

$$A_{IL} = \frac{g_{mp}R_L\beta g_{m1}r_{o1} + g_{mab}r_{in1}g_{m1f}r_{o1}\left(1+\frac{s}{w_{z1}}\right)\left(1+\frac{s}{w_{p2}}\right)}{\left(1+\frac{s}{w_{p1}}\right)\left(1+\frac{s}{w_{p2}}\right)} \tag{3.31}$$

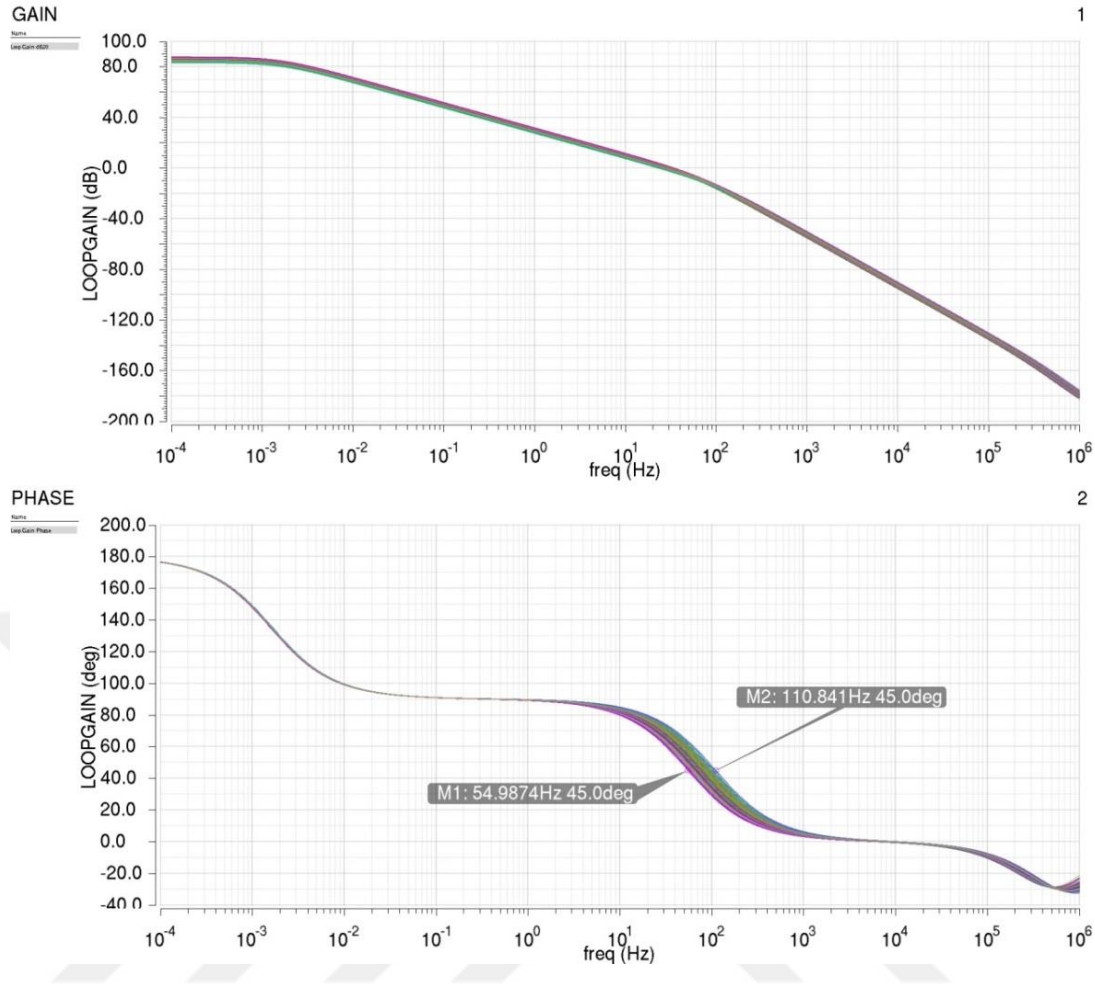

Figure 3.10 : Bode plots of A_{ML} of LDO with NMOS input stage for 200 MC points w/ 1/7200 AB ratio

The DC loop gain of the inner loop has an extra term $g_{mab}r_{in1}g_{m1f}r_{o1}$, which is $A_{ab}|_{DC}$. As can be seen from the 3.31, the transfer function includes 2 zeros. When the numerator of the loop gain is set to 0, it follows that

$$s^2 + s(w_{z1} + w_{p2}) + w_{z1}w_{p2}\left(1 + \frac{g_{mp}R_L\beta g_{m1}r_{o1}}{g_{mab}r_{in1}g_{m1f}r_{o1}}\right) = 0\,. \tag{3.32}$$

Substituting for w_{z1} and g_{m1f} from 3.9 and 3.18 and using $r_{in1}=1/2g_{m1}$, if $\frac{g_{mp}R_L\beta g_{m1}r_{o1}}{g_{mab}r_{in1}g_{m1f}r_{o1}} >> 1$, then equation 3.33 is obtained.

$$s^2 + s(w_{z1} + w_{p2}) + \frac{2\beta g_{m3}g_{m1}^2 g_{mp}}{C_L C_x g_{m2} g_{mab}} = 0\,. \tag{3.33}$$

Since the output pole is the dominant pole for this LDO and it is at the relatively lower frequencies, $w_{p2} << w_{z1}$, yielding

$$s^2 + sw_{z1} + \frac{2\beta g_{m3} g_{m1}^2 g_{mp}}{C_L C_x g_{m2} g_{mab}} = 0\,. \tag{3.34}$$

As a result the analysis by breaking the inner loop shows that the adaptive bias loop adds 2 zeros to the system and the poles do not change compared to the system where adaptive bias loop is not present. It is important to note that since sign of g_{mp} is negative, the last term in the equation 3.34 is negative. Thus, the inner loop gain has one RHP and one LHP zeros. The sign of the w_{z1} defines which zero has the lower value. Figure 3.11 shows the Monte Carlo simulation results of the inner loop gain and phase for the same circuit in Figure 3.6. As shown before in Figure 3.8, w_{p1} value is around 100Hz which shifts the phase by -90°. The inner loop gain curve is getting flat shape after 10kHz since 2 zeros are present. The phase goes down to -78° for some points with the effect of RHP zero and w_{p1} and then starts to rise up to 0° with the effect of LHP zero. For some points LHP zero has a lower value compared to RHP zero and for these points phase goes up to 108° with the effect of LHP zero and w_{p1} and goes to 0° with the effect of RHP zero.

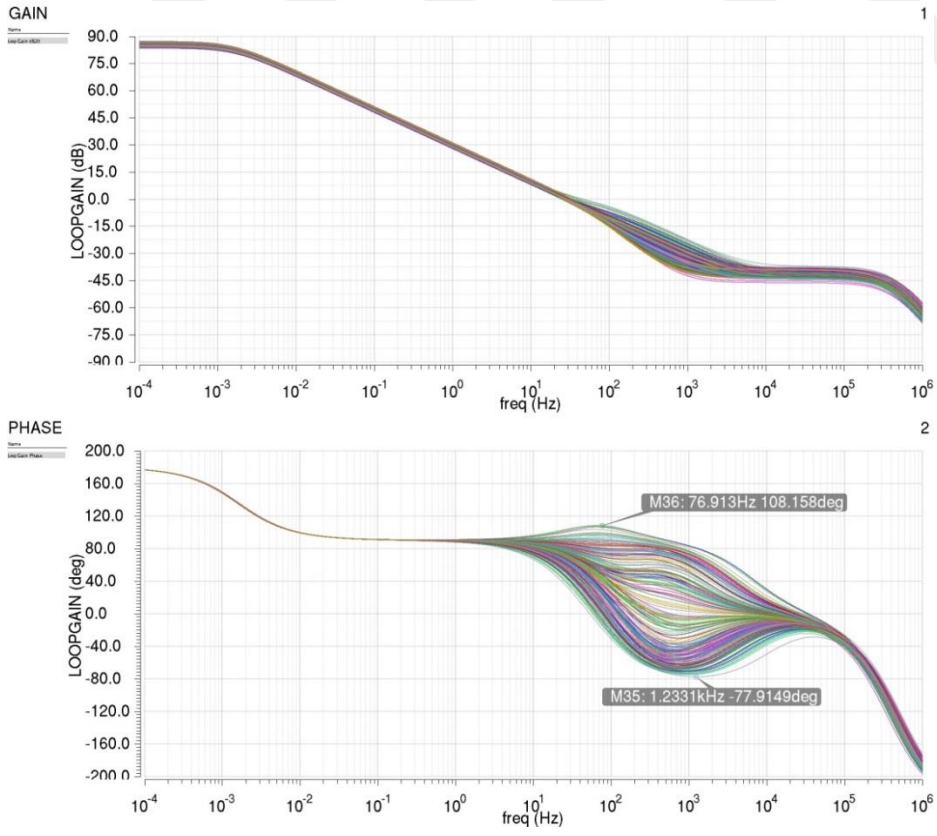

Figure 3.11 : Bode plots of A_{IL} of LDO with NMOS input stage for 200 MC points w/ 1/800 AB ratio

The location of the zeros also change the phase margin of the inner loop. Minimum and maximum values of the phase margin are measured as 7.3° and 106.1°.

Since the phase behavior depends on the sign of the w_{z1}, for some points it increases the phase margin but for some points it decreases the phase margin. The equation 3.34 can be rewritten as below:

$$s^2 + 2\alpha\omega_n s + \omega_n^2 \tag{3.35}$$

where ω_n is the natural frequency of the zeros and α is the damping factor of the zeros.

In order to prevent phase margin variation, the zeros should be pushed beyond w_{ugf} which is the unity gain frequency. The equation is given in 3.36. Increasing ω_n will push the zeros to higher frequencies and this can be done by increasing g_{m1} or decreasing g_{mab} which gives the same result found from the analysis of the main loop. For a fixed current, g_{m1} will be fixed and ω_n can be pushed to higher frequencies by decreasing g_{mab} which can be achieved by decreasing the adaptive bias ratio. Decreasing C_L also moves the zeros to higher frequencies but it affects the load transient response and stability.

$$\omega_n^2 = \frac{2\beta g_{m3} g_{m1}^2 g_{mp}}{C_L C_x g_{m2} g_{mab}} \gg w_{ugf}^2 \tag{3.36}$$

For a one pole system, w_{ugf} is given by g_{m1}/C_L and 3.36 can be rewritten as;

$$\omega_n^2 = \frac{C_L 2\beta g_{m3} g_{mp}}{C_x g_{m2} g_{mab}} \gg 1 \tag{3.37}$$

Thus, for a stable operation the adaptive bias current is limited by the equations 3.29 and 3.36, which states that for a fixed total tail current and fixed output capacitor value, g_{mab} is limited, so the current supplied by the adaptive bias circuit is limited.

To see the effect of the adaptive bias ratio on the inner loop gain, adaptive bias ratio is decreased to 1/7200 and the zeros are pushed to higher frequencies. As can be seen in Figure 3.12, zeros are placed beyond the unity gain frequency and phase margin of the inner loop is increased. Minimum and maximum values of the phase margin are measured as 59° and 80.4°.

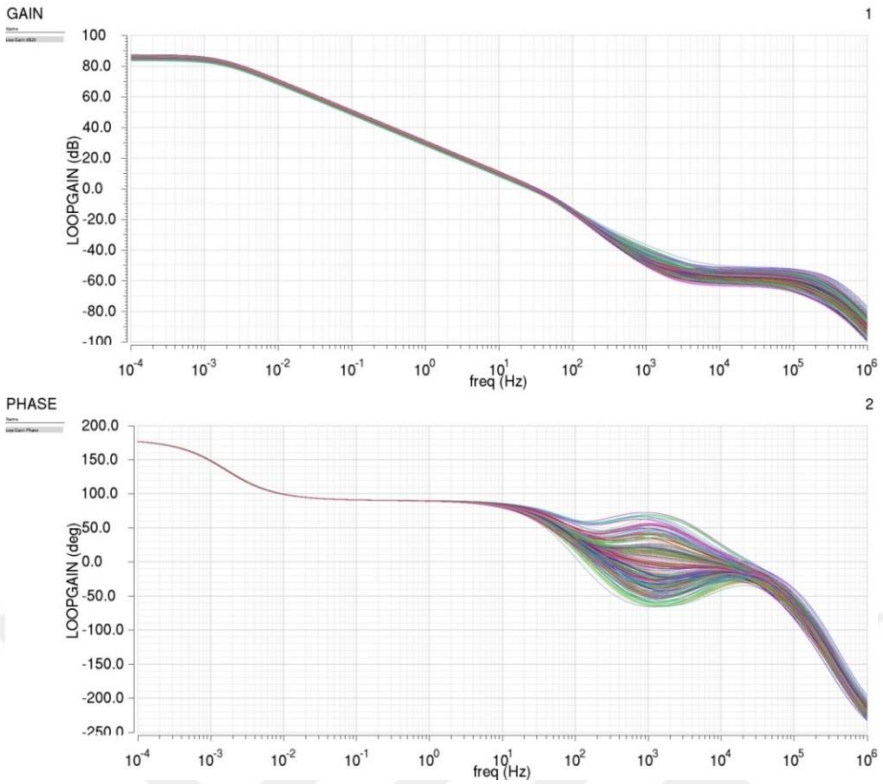

Figure 3.12 : Bode plots of A_{IL} of LDO with NMOS input stage for 200 MC points w/ 1/7200 AB ratio

The stability criteria for main loop and inner loop show that g_{mab} should be low enough to prevent variation of the pole at the output of the input stage for the main loop stability and to push the zeros created by AB loop beyond the unity gain frequency for inner loop stability. In order to decrease the quiescent current of the LDO for low loads, the fixed bias current should be low and for high bandwidth at high loads tail current of input stage should be increased which is done by increasing the adaptive bias ratio, thus g_{mab} is increased. For 1/800 adaptive bias ratio, quiescent current of the LDO at zero load is 2uA and for 1/7200 adaptive bias ratio, quiescent current is increased to 11.1uA to achieve same bandwidth at high loads. As a result, there is a tradeoff between the stability and the quiescent current at low load condition of the LDO. More adaptive bias current and low fixed bias current provide better efficiency but might create stability issues for the LDO.

3.3 Analysis of Adaptively Biased 4 Stage LDO with PMOS Input Stage

A LDO with PMOS input stage is given in Figure 3.13. The second stage is used to increase the gain and the third stage is used to lower the resistance at V_{gate} node to push the pole at this node to higher frequency. This is done by the low output

resistance of the diode connected PMOS which is $1/g_m$ [9]. The adaptive bias current is supplied by M_{ab} whose gate is connected to the pass device gate.

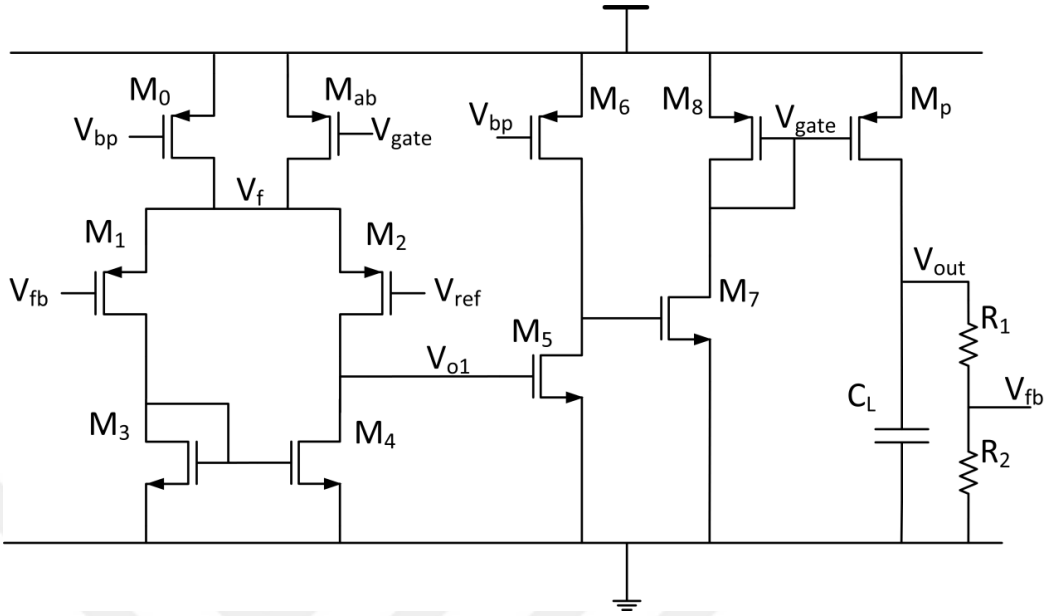

Figure 3.13 : Schematic of an adaptively biased 4 stage LDO with PMOS input stage

The additional stages add 2 poles to the inner loop gain but they are located beyond the unity gain frequency. 2 zeros as analyzed before for the LDO with NMOS input stage are also present in this LDO. The inner loop gain and phase plots of the LDO with adaptive bias loop broken and not broken are given in the Figure 3.14 and Figure 3.15. No load is applied externally and only a small current consumed by the resistor divider flows through the pass device. 50nA fixed bias current and 1/800 adaptive bias ratio are used in the simulations. As it can be seen in Figure 3.15, the zeros are in the same half plane and creates +180° or -180° phase shift depending on their location. The reason of this can be observed with the aid of the equation 3.34. Since the signs of both g_{mp} and g_{mab} are negative, the last term which is ω_n^2 is positive. As this term is multiplication of the zero values, the signs of the zeros should be same, thus they are in the same half plane. And if

$$w_{z1}^2 - 4\frac{2\beta g_{m3} g_{m1}^2 g_{mp}}{C_L C_x g_{m2} g_{mab}} < 0, \tag{3.38}$$

the zeros are complex conjugate pairs. Depending on the sign of the w_{z1}, the zeros can be both located in RHP or LHP. Also the magnitude of the w_{z1} defines the damping factor of the zeros, so the sharpness of the phase change.

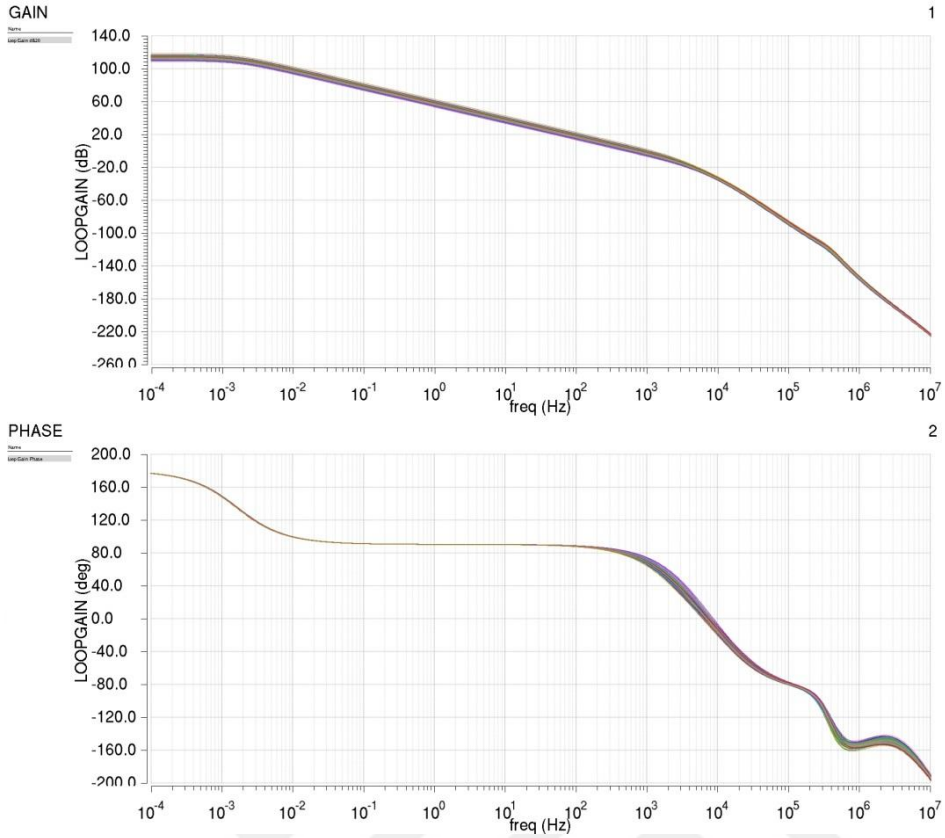

Figure 3.14 : Bode plots of A_{IL} of LDO with PMOS input stage for 200 MC points w/o AB

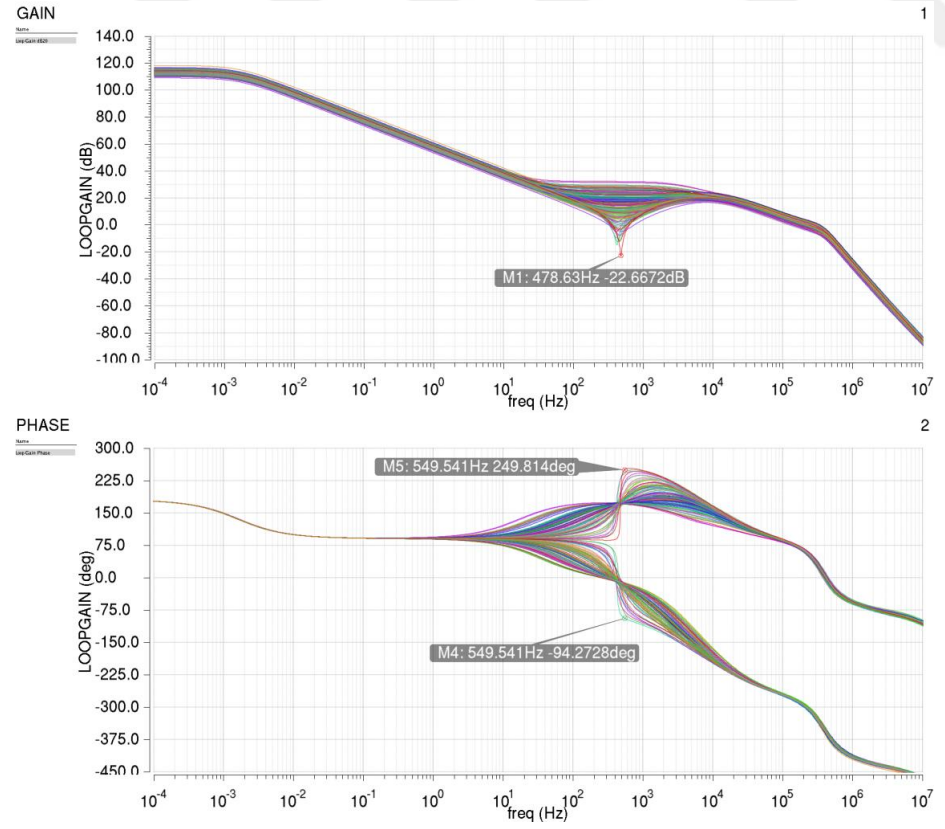

Figure 3.15 : Bode plots of A_{IL} of LDO with PMOS input stage for 200 MC points w/ 1/800 AB ratio

Decreasing g_{mab} shifts the zeros to higher frequencies as given by the equation 3.36 and this can be done by decreasing the adaptive bias ratio. As an example, the adaptive bias ratio is decreased to 1/8000 by decreasing the width of M_{ab} by 10 times. Monte Carlo simulation results are given in Figure 3.16 for this condition. As can be seen from the figure, frequency of the complex conjugate zeros is increased by ~3 times. The frequency of the zeros is measured as ~1.6kHz for 1/8000 adaptive bias ratio in Figure 3.16 and it is measured ~500Hz for 1/800 adaptive bias ratio in Figure 3.15. The quiescent current at zero load is 4.5uA for 1/800 AB ratio while it is 9uA for 1/8000 AB ratio to achieve same bandwidth at maximum load condition.

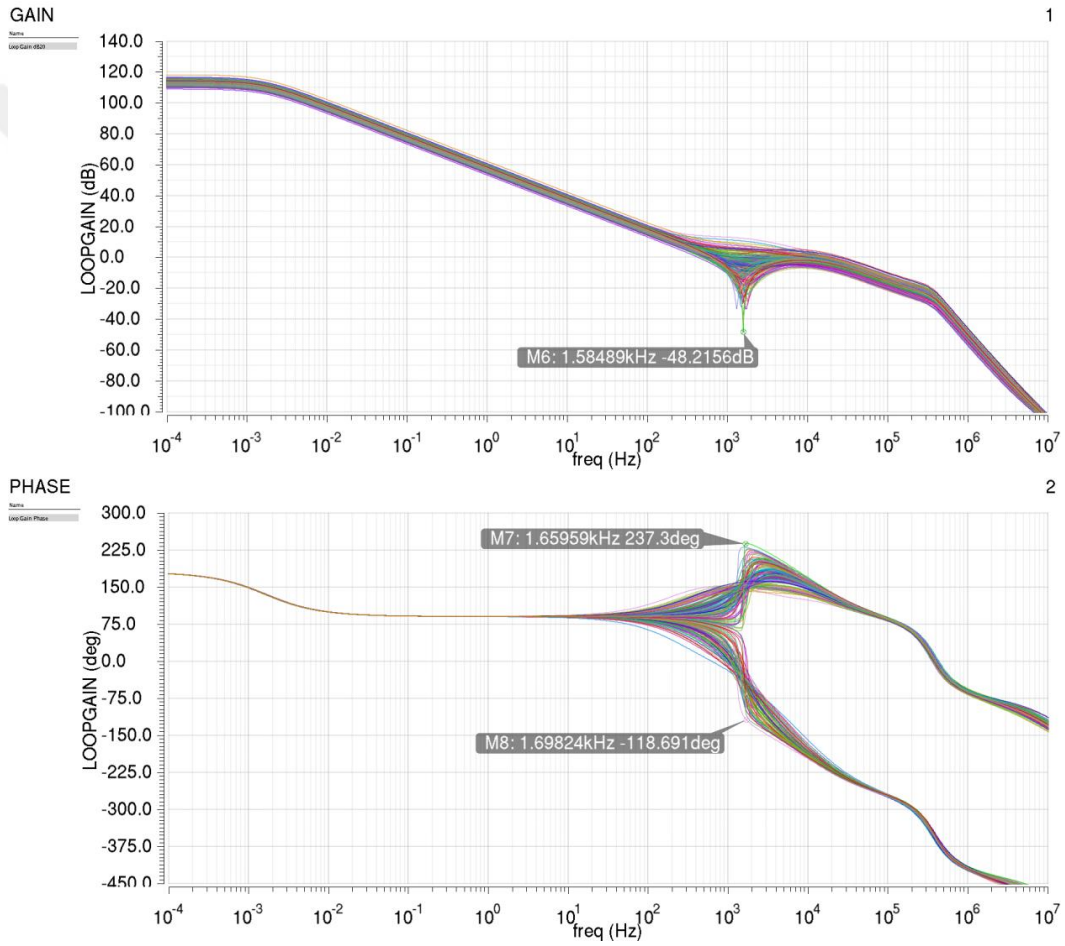

Figure 3.16 : Bode plots of A_{IL} of LDO with PMOS input stage for 200 MC points w/ 1/8000 AB ratio

The simulation results satisfy the correlation between the adaptive bias ratio and the natural frequency of the zeros as given in the equation 3.36. When compared to the LDO with NMOS input stage, adaptive biasing adds 2 zeros to the inner loop gain where the zeros are located in same half plane. The analysis for this topology is done to show the behavior of the zeros as a case study.

The gain of the LDO in Figure 3.13 is higher than 100dB and in order to compensate the LDO in the full load range the output capacitor should be relatively high to reach 0dB with -20dB/dec before the non-dominant pole. Using huge capacitors are not practical always and miller compensation can be used in this circuit to create the dominant pole inside the circuit.

3.4 Analysis of Adaptively Biased Miller Compensated 4 Stage LDO with PMOS Input Stage

A miller compensated 4 stage LDO with PMOS input stage is given in Figure 3.17. Since the gain is high from V_{o1} to V_{out} , miller compensation capacitor C_c is placed between these nodes and the pole at V_{o1} becomes dominant. With this configuration the output pole is pushed to higher frequencies because of pole splitting [29].

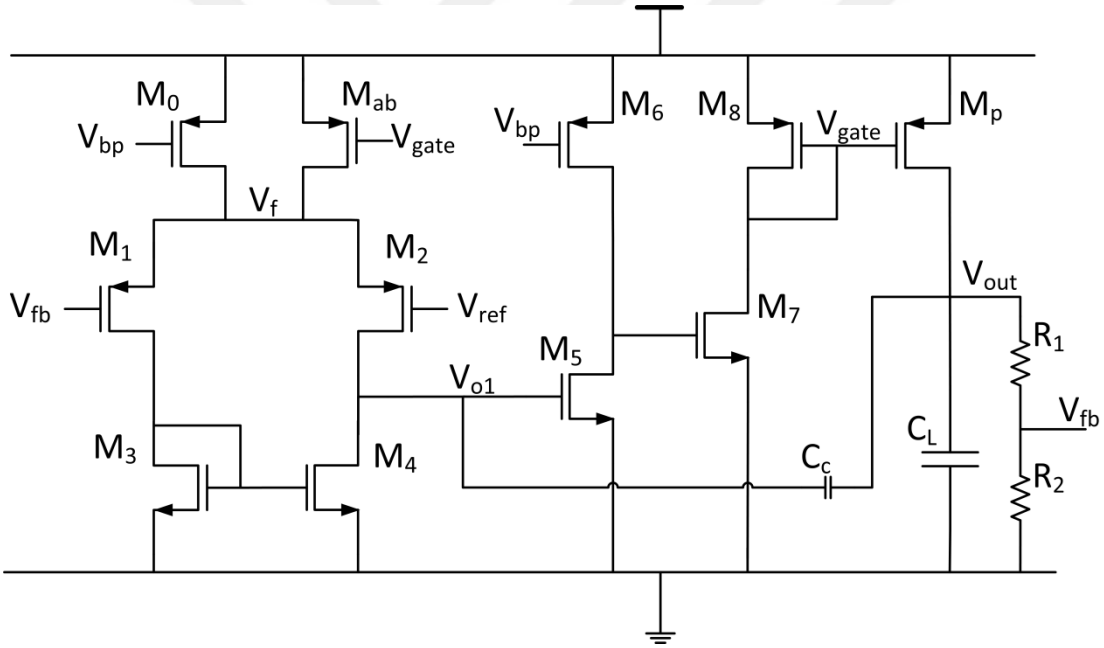

Figure 3.17 : Schematic of an adaptively biased miller compensated 4 stage LDO with PMOS input stage

The small signal equivalent circuit is given in Figure 3.18. The second and third stage gains are combined in g_{m2} and the pole associated with the second stage output is neglected since it is at relatively higher frequencies. The point where all the loops intersect and broken is shown with P2 and P1 is the point where only the main loop is broken.

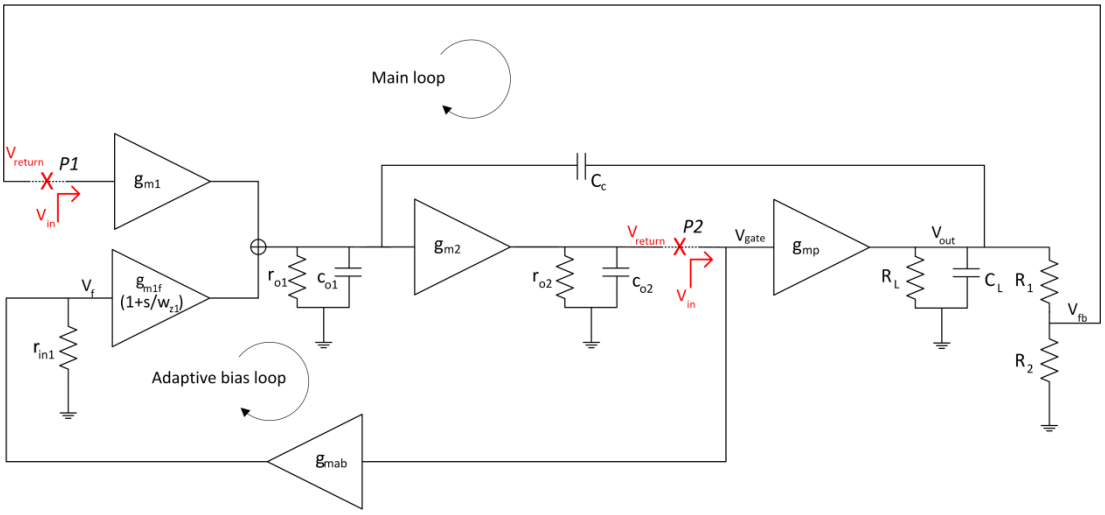

Figure 3.18 : Small signal equivalent of the circuit in Figure 3.17

In order to find the inner loop gain, the feedback loop is broken at P2. Using the small signal equivalent circuit, V_{o1} can be calculated as below:

$$V_{o1} = \left(V_{out}\beta g_{m1} + V_{in}g_{mab}r_{in1}g_{m1f}\left(1+\frac{s}{w_{z1}}\right) + sC_c(V_{out} - V_{o1})\right)\frac{r_{o1}}{\left(1+\frac{s}{w_{p1}}\right)} \quad (3.39)$$

w_{p1} is the pole at the output of the first stage given by $1/r_{o1}c_{o1}$. V_{out} and V_{return} are calculated similarly:

$$V_{out} = \left(V_{in}g_{mp} - sC_c(V_{out} - V_{o1})\right)\frac{R_{Leq}}{\left(1+\frac{s}{w_{p3}}\right)} \quad (3.40)$$

$$V_{return} = V_{o1}\frac{g_{m2}r_{o2}}{\left(1+\frac{s}{w_{p2}}\right)} \quad (3.41)$$

w_{p2} and w_{p3} are the poles at the V_{gate} and V_{out} nodes given by $1/r_{o2}c_{o2}$ and $1/R_{Leq}C_L$, respectively. Substituting for V_{o1} from equation 3.41, equation 3.40 gives

$$V_{out}\left(\frac{\left(1+\frac{s}{w_{p3}}\right)}{R_{Leq}} + sC_c\right) = V_{in}g_{mp} + sC_c\frac{V_{return}\left(1+\frac{s}{w_{p2}}\right)}{g_{m2}r_{o2}} \quad (3.42)$$

Similarly, substituting for V_{o1} from 3.41, equation 3.39 gives

$$V_{return}\frac{\left(1+\frac{s}{w_{p2}}\right)}{g_{m2}r_{o2}}\left(\frac{\left(1+\frac{s}{w_{p1}}\right)}{r_{o1}}+sC_c\right)=V_{out}(sC_c+\beta g_{m1})+V_{in}G_{ab}\left(1+\frac{s}{w_{z1}}\right) \quad (3.43)$$

where G_{ab} is $g_{mab}r_{in1}g_{m1f}$.Thus, using the equation 3.42 and 3.43 the inner loop gain $\frac{V_{return}}{V_{in}}|_{IL}$ obtained as

$$\frac{r_{o1}g_{m2}r_{o2}\left(g_{mp}R_{Leq}(\beta g_{m1}+sC_c)+G_{ab}\left(1+\frac{s}{w_{z1}}\right)\left(1+\frac{s}{w_{p3}}+sC_cR_{Leq}\right)\right)}{\left(1+\frac{s}{w_{p2}}\right)\left[\left(1+\frac{s}{w_{p3}}+sC_cR_{Leq}\right)\left(1+\frac{s}{w_{p1}}+sC_cr_{o1}\right)-sC_CR_{Leq}r_{o1}(\beta g_{m1}+sC_c)\right]} \quad (3.44)$$

Equation 3.44 reveals that adaptive bias loop adds one more zero to the inner loop gain and does not affect the pole locations. If the numerator of 3.44 is set to 0 and if $1/w_{p3} >> R_{Leq}C_c$, the second order function for the zeros is obtained as below:

$$s^2+s\left(w_{z1}+w_{p3}\left(\frac{g_{mp}R_{Leq}C_cw_{z1}}{g_{mab}r_{in1}g_{m1f}}+1\right)\right)+w_{z1}w_{p3}\left(\frac{g_{mp}R_{Leq}\beta g_{m1}}{g_{mab}r_{in1}g_{m1f}}+1\right) \quad (3.45)$$

Substituting for w_{z1} and g_{m1f} from the equations 3.9 and 3.18, using $r_{in1}=1/2g_{m1}$, if $C_L >> C_c$ and $\frac{g_{mp}R_{Leq}\beta g_{m1}}{g_{mab}r_{in1}g_{m1f}} >> 1$, then equation 3.46 is obtained.

$$s^2+s\left(w_{z1}+w_{p3}\left(\frac{g_{mp}R_{Leq}C_cw_{z1}}{g_{mab}r_{in1}g_{m1f}}+1\right)\right)+\frac{2\beta g_{m3}g_{m1}^2g_{mp}}{C_LC_xg_{m2}g_{mab}} \quad (3.46)$$

When the equations 3.33 and 3.46 are compared it can be seen that Miller compensation adds $w_{p3}\frac{g_{mp}R_{Leq}C_cw_{z1}}{g_{mab}r_{in1}g_{m1f}}$ to the coefficient of *s*. Thus, under some conditions the coefficient of *s* can be made positive irrespective of the w_{z1} sign and 2 LHP zeros can be guaranteed for the inner loop gain. In order to make the coefficient of *s* positive, the condition below should be satisfied:

$$w_{z1}\left(\frac{g_{mp}R_{Leq}C_cw_{p3}}{g_{mab}r_{in1}g_{m1f}}+1\right)+w_{p3}>0 \quad (3.47)$$

If the sign of w_{z1} is positive which shows that w_{z1} is a LHP zero, g_{m1f} also has a positive sign then this condition is satisfied and the zeros of the inner loop are in LHP. If the sign of w_{z1} is negative which shows that w_{z1} is a RHP zero, g_{m1f} also has

a negative sign and 3.47 can be rewritten as 3.48 for this condition.

$$-|w_{z1}|\left(-\frac{g_{mp}R_{Leq}C_c w_{p3}}{g_{mab}r_{in1}|g_{m1f}|}+1\right)+w_{p3}>0 \tag{3.48}$$

In order to satisfy the inequality in 3.48, assuming w_{p3} is negligible, the term inside the brackets should be negative which yields

$$\frac{g_{mp}R_{Leq}C_c w_{p3}}{g_{mab}r_{in1}|g_{m1f}|}>1 \tag{3.49}$$

Replacing w_{p3} by $1/R_{Leq}C_L$ gives

$$\lambda=\frac{C_c g_{mp}}{C_L g_{mab}r_{in1}|g_{m1f}|}>1 \tag{3.50}$$

If the condition given in the equation 3.50 is satisfied for every possible DC operating points, then it is guaranteed that inner loop zeros are in the left half plane. If the equation 3.46 is rewritten in the format below

$$s^2+\frac{\omega_n}{Q}s+\omega_n^2 \tag{3.51}$$

Quality factor of the zeros can be found in 3.52:

$$Q=\frac{\sqrt{\frac{2\beta g_{m3}g_{m1}^2 g_{mp}}{C_L C_x g_{m2}g_{mab}}}}{w_{z1}\left(\frac{g_{mp}R_{Leq}C_c w_{p3}}{g_{mab}r_{in1}g_{m1f}}+1\right)+w_{p3}} \tag{3.52}$$

For the zeros with a low quality factor the denominator of the equation 3.52 should be increased, that is

$$\lambda=\frac{C_c g_{mp}}{C_L g_{mab}r_{in1}|g_{m1f}|}>>1 \tag{3.53}$$

Equation 3.53 reveals that although first stage introduces a RHP zero, the inner loop gain has LHP zeros if the condition is met. This can be done by decreasing C_L or increasing C_c. These modifications might not be practical. Decreasing C_L affects load transient performance and makes voltage drop worse. Increasing C_c results in larger

silicon area and lower bandwidth. Since the main idea of the adaptive biasing is improvement of the transient response, increasing λ by C_c or C_L modifications is not desired. Increasing g_{mp} by increasing pass device current results in a minimum load current requirement. Decreasing g_{mab} by lowering adaptive bias ratio increases λ but affects the efficiency of the LDO at low load condition as explained before. Thus, the tradeoff between adaptive bias ratio and stability is obtained from equation 3.53.

In order to see the effects of the adaptive bias loop implemented in a Miller compensated LDO, two set of Monte Carlo simulations are run where the adaptive bias loop is broken and not broken. Simulations are done for no load case and adaptive bias ratio is set to 1/1800. Figure 3.19 shows the bode plots of the inner loop gain of the miller compensated LDO for 200 points. In this simulation adaptive bias loop is broken and phase margin varies between 32° and 43°. Phase of the inner loop gain reaches almost 0° with the effect of 2 poles and a LHP zero created by the miller capacitor shifts the phase by +90° and increases phase margin. It is important to note that in a system if the phase of loop gain crosses 0° an even number of times while magnitude of the loop gain greater than 0dB, the system is stable [29]. Detailed nyquist and bode plots of such system is given in Figure A.1.

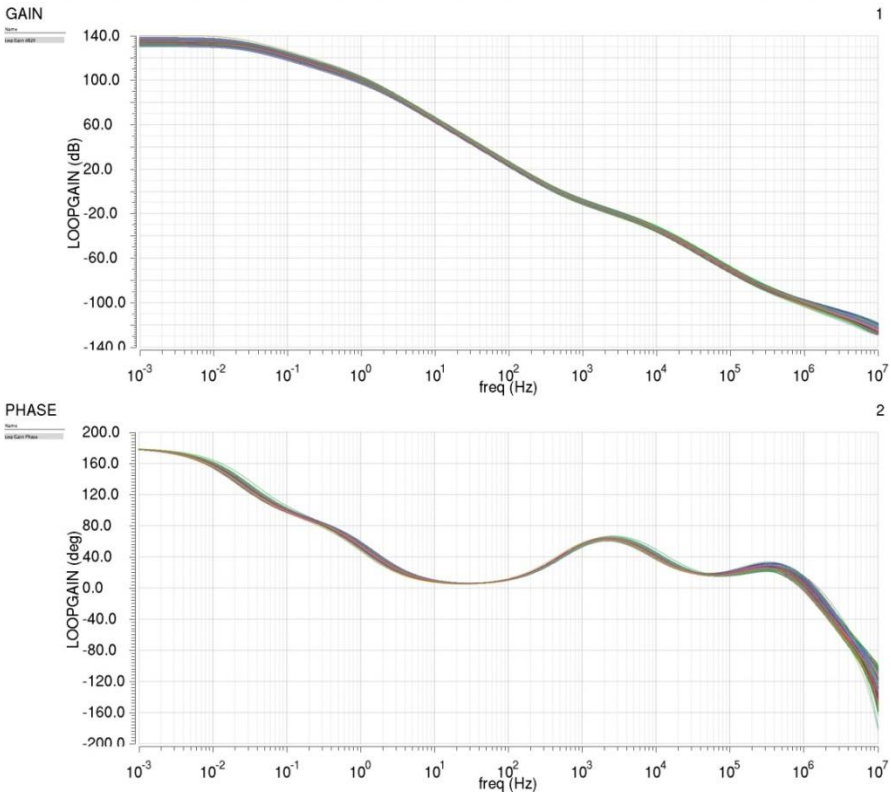

Figure 3.19 : Bode plots of A_{IL} of Miller compensated LDO for 200 MC points w/o AB

When adaptive bias loop is not broken, bode plots show the effects of the two zeros in Figure 3.20. Adaptive bias loop adds one more zero to the system and 2 zeros can be both in RHP or LHP. The inner loop is unstable if two zeros are in RHP which creates -180° phase shift. For the points where the zeros are in LHP but have high Q, the system is also unstable because the phase remains around 0° when gain crosses 0dB. As a result the zeros cannot improve the phase margin and they shift the phase by +180° after the unity gain frequency with very sharp slope. If the inner loop has 2 LHP zeros with low quality factor, phase margin is improved and for these points LDO is stable. Phase margin histogram for the Figure 3.20 is given in Figure 3.21 where the standard deviation is 34.3° and phase margin has a huge variation. Maximum, minimum and mean values of the phase margin are 130°, -40° and 56°, respectively.

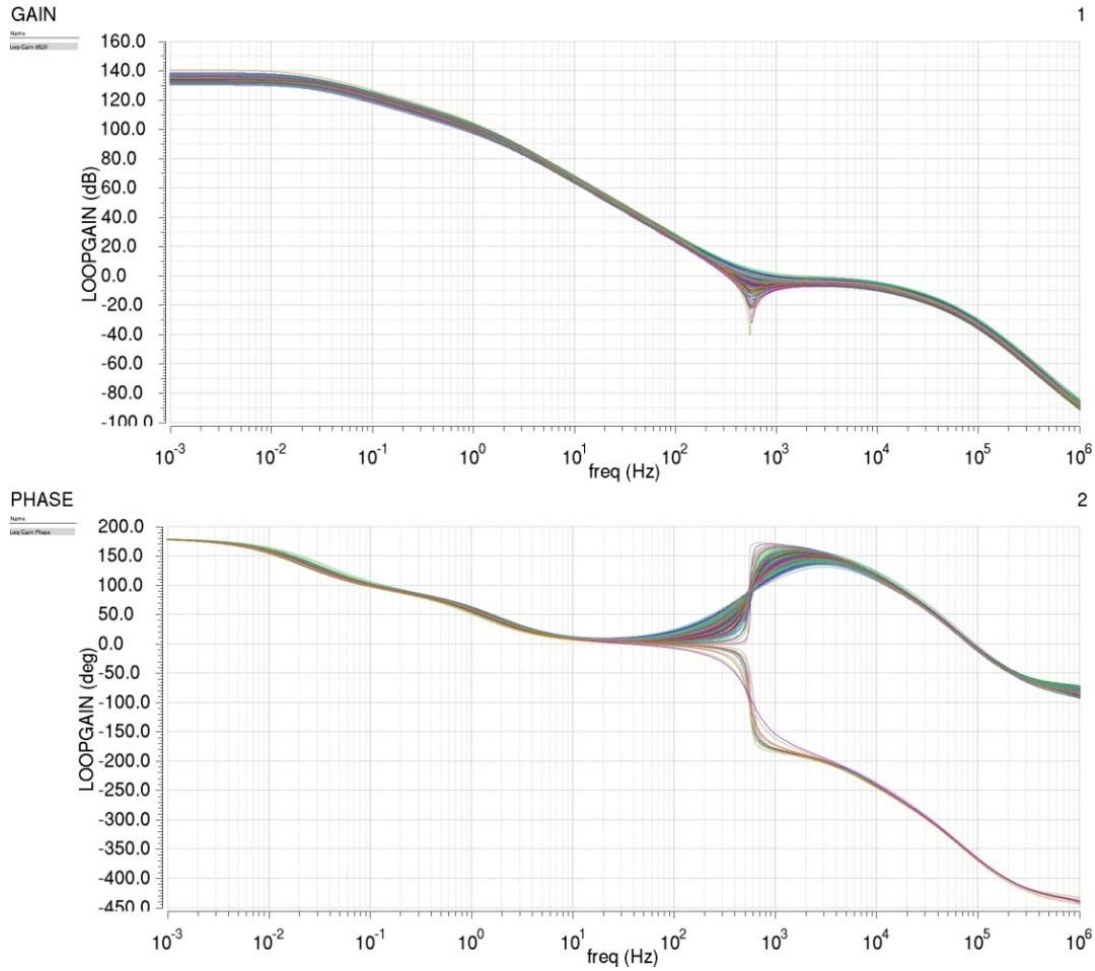

Figure 3.20 : Bode plots of A_{IL} of Miller compensated LDO for 200 MC points w/ 1/1800 AB ratio

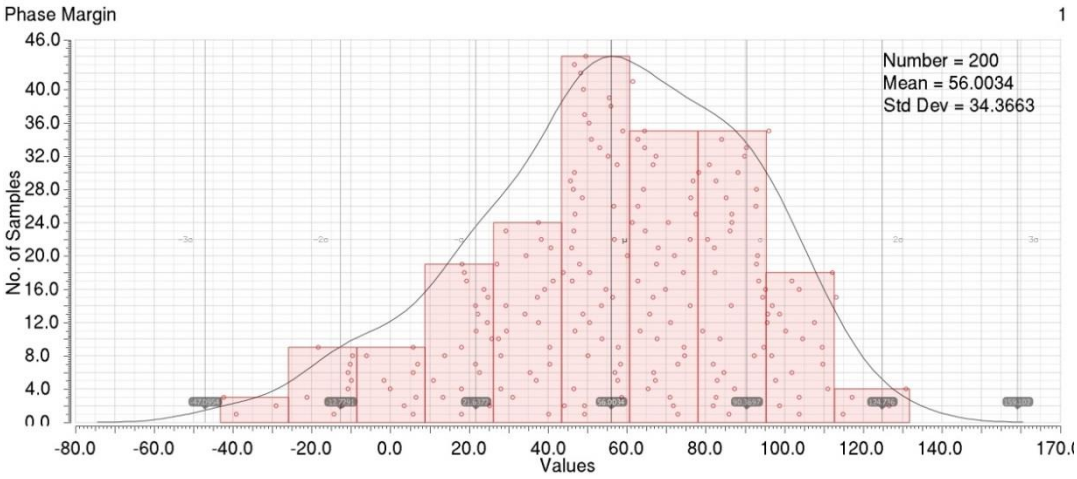

Figure 3.21 : Phase margin histogram of A_{IL} of Miller compensated LDO for 200 MC points w/ 1/1800 AB ratio

As given in the equation 3.50, for 2 LHP zero in the inner loop, λ should be greater than 1 if the input stage exhibits a RHP zero. Figure 3.22 shows the phase behavior and λ values of the same simulation where the input stage has a RHP zero and λ is less than 1.

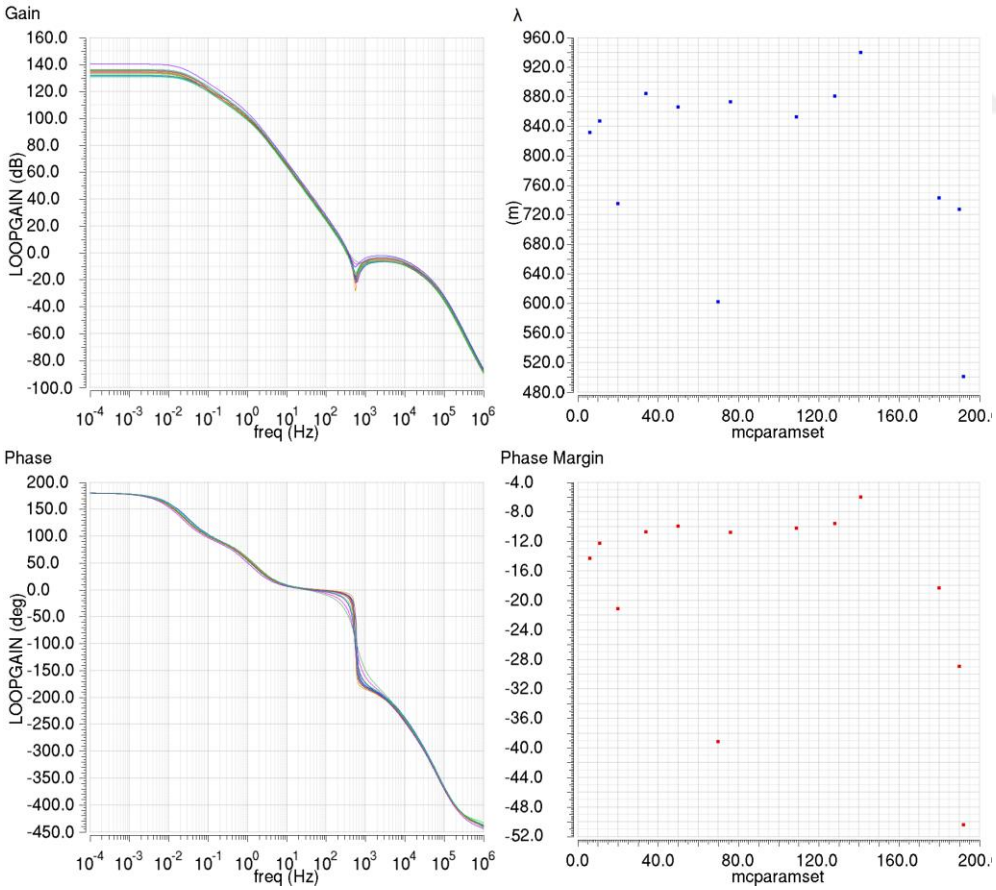

Figure 3.22 : Bode plots of the inner loop with RHP zero in the input stage and λ < 1 w/ 1/1800 AB ratio

It is observed from Figure 3.22 that 2 RHP zeros are present since λ is less than 1. Phase change has a high slope if λ is close to 1 which creates high Q factor as given in the equation 3.52. In the same simulation, MC points with a RHP zero in the input stage and λ greater than 1 are given in the Figure 3.23. Although input stage has a RHP zero, since λ is greater than 1, the inner loop shows 2 LHP zeros. If λ is close to 1, zeros with high Q factor shift the phase by +180° but phase margin is not improved as can be seen in Figure 3.23.

The stability problem of the LDO can also be shown in transient simulations with increasing V_{ref} voltage by 1mV in 1us. In Figure 3.24 the ringing can be seen for the unstable Monte Carlo points. No ringing is observed for the points where the phase margin is high.

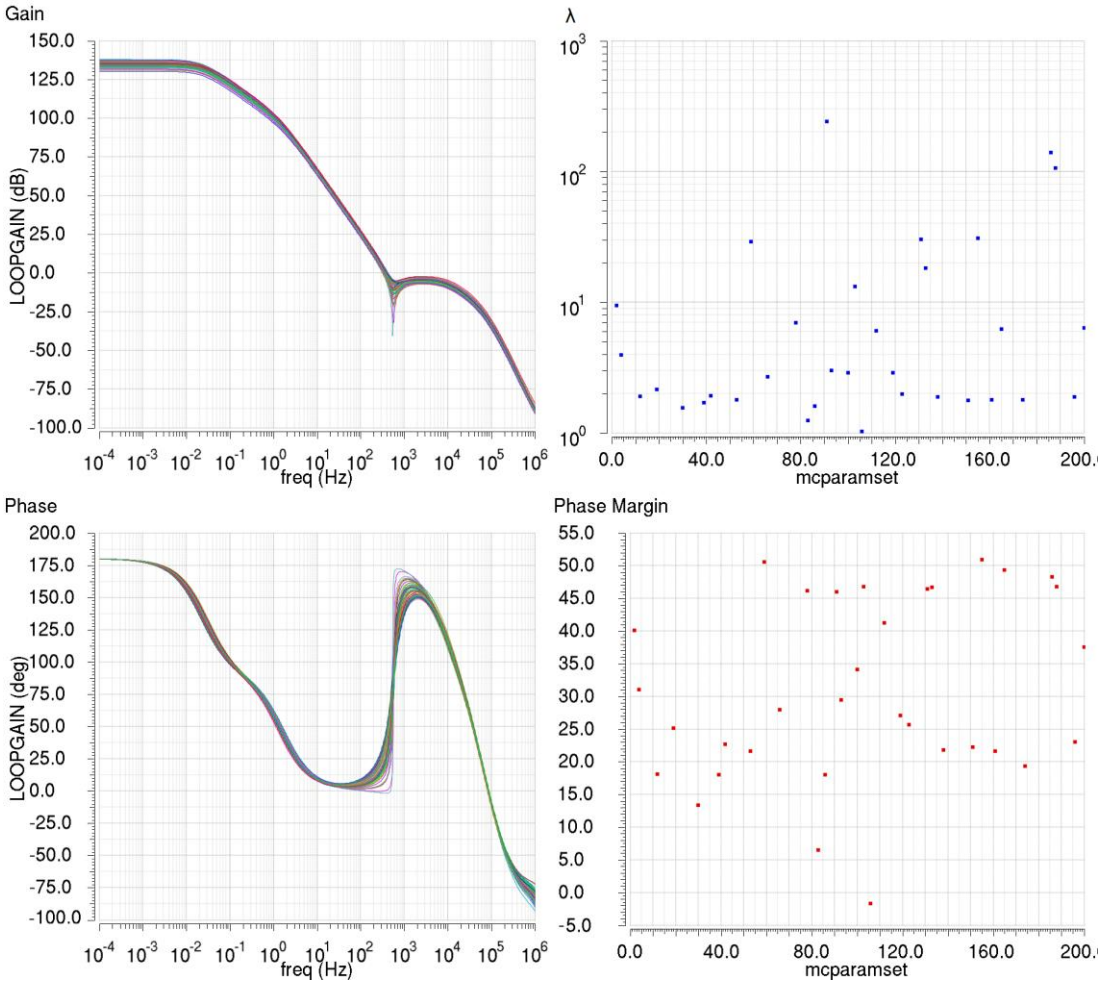

Figure 3.23 : Bode plots of the inner loop with RHP zero in the input stage and λ > 1 w/ 1/1800 AB ratio

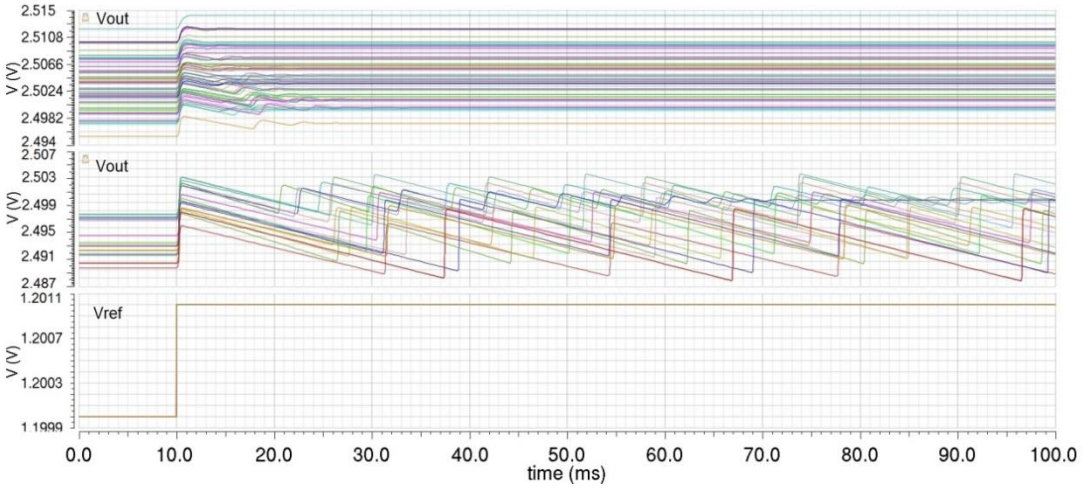

Figure 3.24 : Transient simulation of Miller compensated LDO for 200 MC points w/ 1/1800 AB ratio

If the width of M_{ab} in the Figure 3.17 is decreased, adaptive bias ratio and g_{mab} also decrease by the same factor, so that the condition given in 3.53 can be satisfied and the all zeros can be moved to LHP. As an example, when adaptive bias ratio is decreased to 1/18000, the inner loop has LHP zeros only which can be seen in Figure 3.25. The zeros have low Q factor and phase change is not sharp. λ values are given in the Figure 3.26 for the points where input stage has a RHP zero.

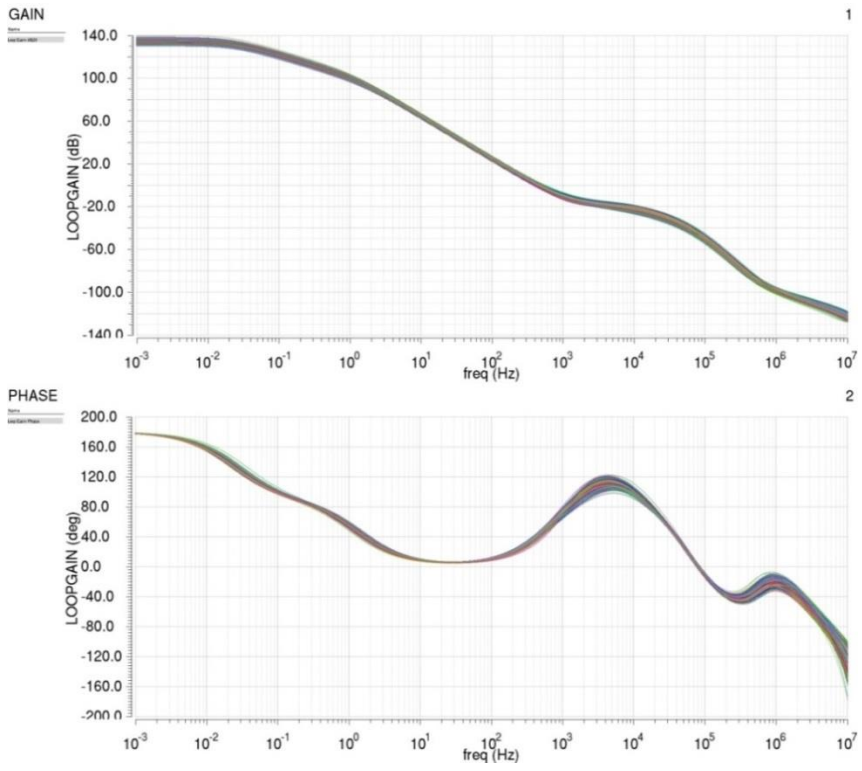

Figure 3.25 : Bode plots of A_{IL} of Miller compensated LDO for 200 MC points w/ 1/18000 AB ratio

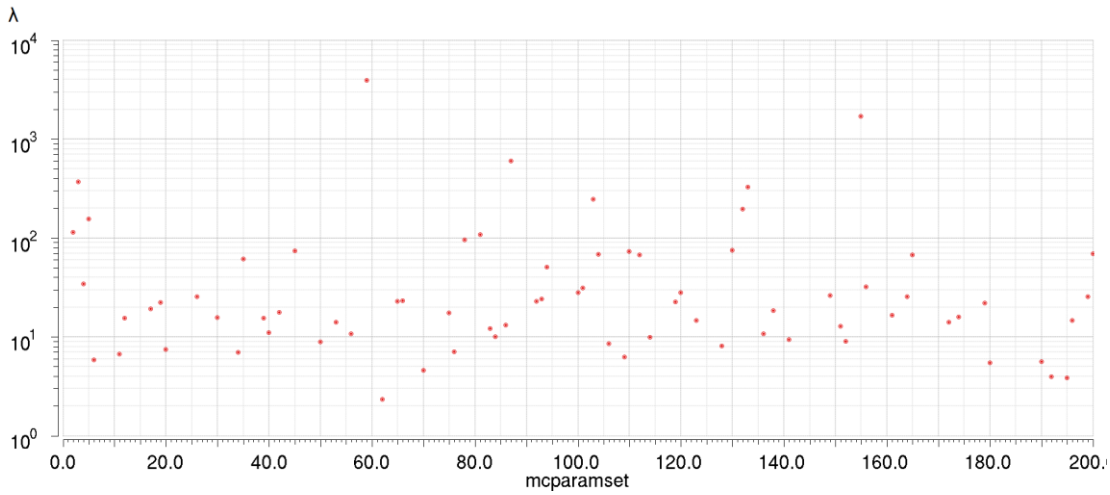

Figure 3.26 : λ values for the points with RHP zero in the input stage w/ 1/18000 AB ratio

Since λ values are far above 1, all points show 2 LHP zeros and phase margin is improved.

The phase margin histogram is given in Figure 3.27. Standard deviation is 4° in this simulation and phase margin variation is less when compared to Figure 3.21. Maximum, minimum and mean values of the phase margin are 52°, 28° and 40°, respectively.

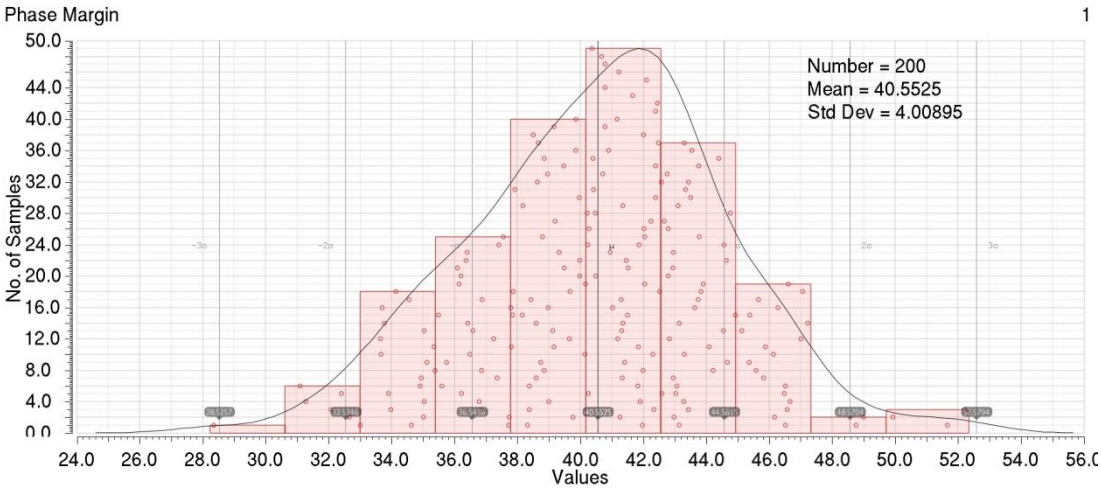

Figure 3.27 : Phase margin histogram of A_{IL} of Miller compensated LDO for 200 MC points w/ 1/18000 AB ratio

A transient simulation is also rerun with decreased adaptive bias ratio and when V_{ref} voltage is increased by 1mV in 1us, all the points settles their final value and no oscillation is observed. Transient simulation results can be seen in Figure 3.28. Thus, LDO is stable for all MC points.

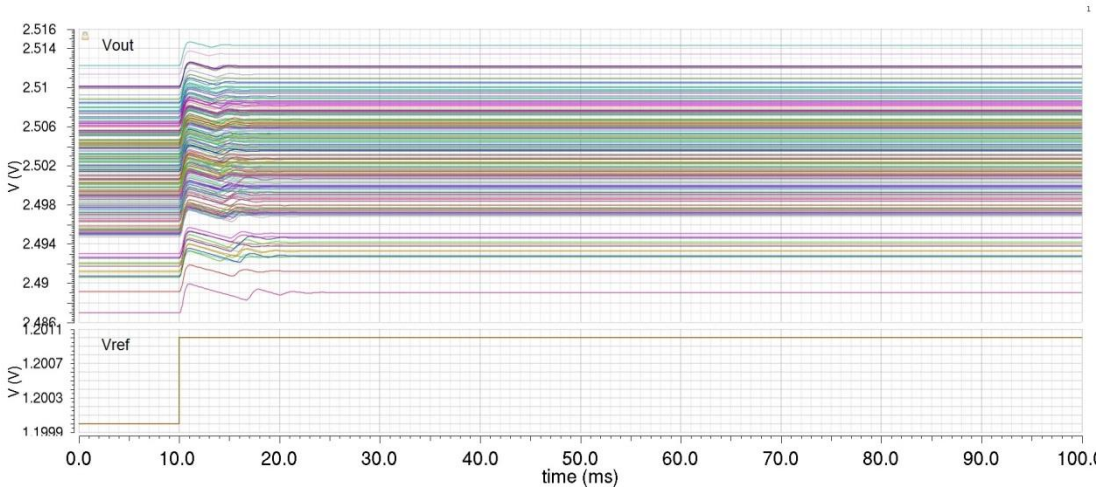

Figure 3.28 : Transient simulation of Miller compensated LDO for 200 MC points w/ 1/18000 AB ratio

As can be seen from the simulation results, when adaptive biasing ratio is decreased by 10 times, all MC points show stable operation, but at the maximum load condition tail current of the differential pair is decreased because of low adaptive bias ratio. To achieve the same bandwidth at the maximum load, the current loss is compensated by the fixed bias current and it is increased by 5uA. For 1/1800 adaptive bias ratio, quiescent current of the LDO at zero load is 5.3uA but LDO shows stability issues for some MC points. For 1/18000 adaptive bias ratio, quiescent current at zero load is 10.3uA and all MC points are stable. Thus, the quiescent current of the LDO is increased to 10.3uA from 5.3uA to achieve same bandwidth at the maximum load. Tradeoff between the efficiency at low loads and stability is obtained from the results.

In order to increase λ, output capacitor value can be decreased. As explained before decreasing C_L is not desired since it affects the load transient response and make it worse but in order to verify the criterion given by the equation 3.53, C_L is decreased and adaptive bias ratio is set to higher value again. Monte Carlo simulations are run with C_L decreased by 10 times and AB ratio is set to 1/1800. As given in the Figure 3.29 the zeros are in LHP and minimum and maximum phase margin are measured as 85° and 103°, respectively. Figure 3.30 shows the λ values for the points with RHP zero in the input stage. All λ values are far above 1, so no sharp phase change is observed in the Figure 3.29.

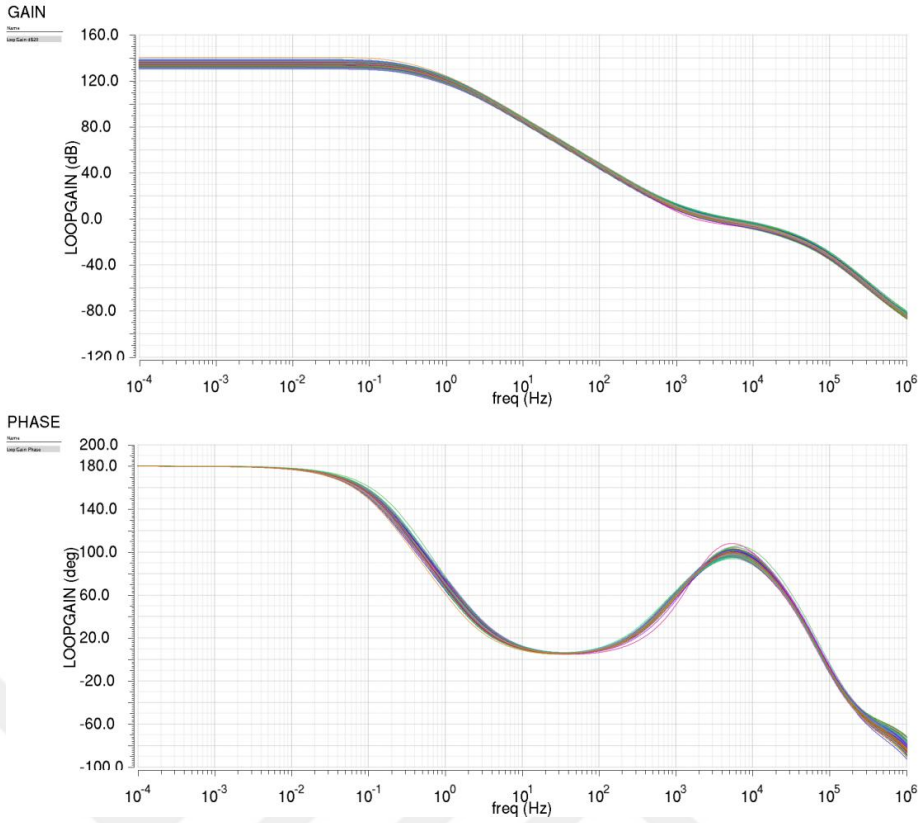

Figure 3.29 : Bode plots of A_{IL} of Miller compensated LDO for 200 MC points w/ 1/1800 AB ratio and C_L decreased by 10 times

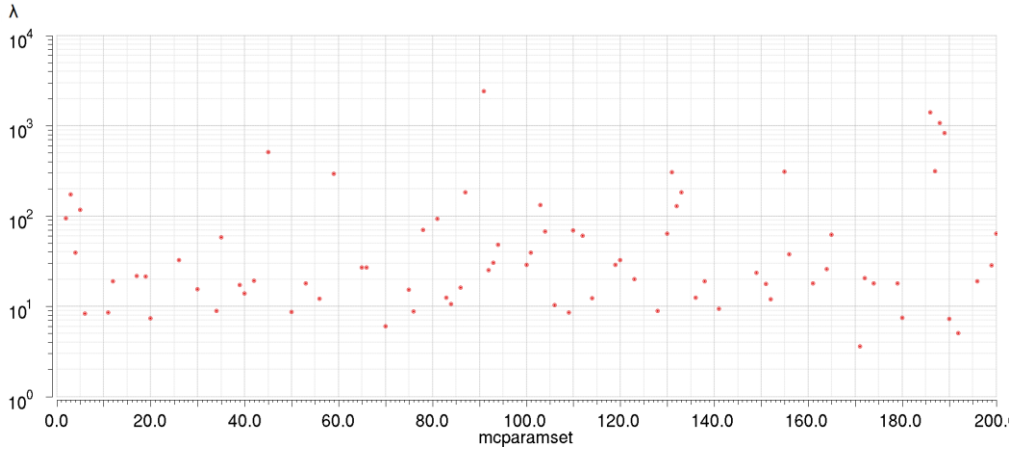

Figure 3.30 : λ values for the points with RHP zero in the input stage w/ 1/1800 AB ratio and C_L decreased by 10 times

The Monte Carlo simulation results verify the conditions for stability given in the equations 3.50 and 3.53. This criterion can be used while designing a Miller compensated LDO in order to prevent stability issues. This topology has the same tradeoff between the adaptive bias ratio and stability that explained before for the 2 stage LDOs. Using more adaptive bias current and low fixed bias current increases the efficiency at low loads but stability of the LDO is not guaranteed as the mismatch

on the first stage transistors has a significant effect on the loop stability. Thus, adaptive bias ratio should be limited by the proposed criterion.

3.5 Calculation of Optimum Adaptive Biasing Ratio for Stable LDOs

In order to find the optimum adaptive biasing ratio, the steps below can be followed. Since the current supplied by the adaptive biasing is negligible when no load current is applied, the tail current of the differential pair, I_{tail}, consists of only the fixed bias current, I_{fb}.

$$I_{tail}|_{min} = I_{fb} \tag{3.54}$$

At maximum load current, the bias current of the differential pair is increased by I_{ab} which is the current supplied by adaptive biasing as given below;

$$I_{tail}|_{max} = I_{fb} + I_{ab} = I_{fb} + \frac{I_{Lmax}}{N} \tag{3.55}$$

where I_{Lmax} denotes the maximum load current and adaptive biasing ratio is represented by 1/N.

For the ldo given in section 3.2, increasing the tail current of the differential pair improves the slew rate of the gate capacitance of the pass device as given in 3.56.

$$Slew\ rate = \frac{I_{tail}}{C_{gate}} \tag{3.56}$$

To achieve higher slew rate at the maximum load condition for obtaining better transient response, more adaptive bias current can be used. Maximum tail current, $I_{tail}|_{max}$, is calculated for a given slew rate by equation 3.56 and adaptive biasing ratio is obtained from the equation 3.55. Since g_{mab} is limited as given in section 3.2, adaptive biasing ratio is limited by the equation 3.57.

$$\omega_n^2 = \frac{2\beta g_{m3} g_{m1}^2 g_{mp}}{C_L C_x g_{m2} g_{mab}} \gg w_{ugf}^2 \tag{3.57}$$

If the maximum adaptive bias ratio calculated with the equation 3.57 is lower than the adaptive bias ratio calculated with the equation 3.55, adaptive biasing is limited for a stable operation. In this case I_{fb} can be increased to meet $I_{tail}|_{max}$ requirement for

a specific slew rate value at the maximum load condition. Increasing I_{fb} also shifts the nondominant pole located at the output of the differential pair to higher frequencies but the efficiency is degraded.

For a miller compensated ldo as given in section 3.4, increasing tail current of the differential pair increases the bandwidth at high loads. As the load current is increased, the pole at the output moves to higher frequencies and bandwidth can be boosted by increasing the transconductance of the first stage as given in the equation 3.58, where g_{m1} and C_c denote the transconductance of the first stage and the miller capacitor, respectively.

$$BW = \frac{g_{m1}}{C_c} \quad (g_{m1} \propto I_{tail}) \tag{3.58}$$

Maximum value of g_{m1} can be calculated at maximum load for a given BW. Since g_{m1} is proportional to I_{tail}, $I_{tail}|_{max}$ can be obtained from $g_{m1,max}$ value. If the quiescent current requirement at no load condition is also given, I_{fb} is fixed and adaptive biasing ratio, 1/N, is calculated from the equation 3.55. As given in section 3.4 adaptive bias ratio is limited for stability with the equation below:

$$\lambda = \frac{C_c g_{mp}}{C_L g_{mab} r_{in1} |g_{m1f}|} >> 1 \tag{3.59}$$

If the maximum adaptive bias ratio calculated from the stability criterion in 3.59 is smaller than the required adaptive bias ratio to meet the bandwidth requirement as calculated from 3.55, I_{fb} can be increased. More fixed bias current decreases the efficiency at low loads and phase margin should be also investigated carefully since the dominant pole will move to higher frequencies at low load currents which means that dominant pole might locate close to the pole at the output at low loads.

Another case is where any change for I_{fb} is not allowed. If the quiescent current at low load is not allowed to be increased or if increasing I_{fb} make phase margin worse at low loads, in these situations, intended value of $I_{tail}|_{max}$ cannot be achieved since adaptive biasing is limited for stability and BW requirement at maximum load is not obtainable. Thus, transient response is affected.

In short, to achieve the BW requirement at high loads adaptive biasing is a solution but for stability reasons maximum adaptive biasing ratio might not be sufficient and

fixed bias current should be increased for BW requirement. In this case, efficiency is degraded at low loads. If the fixed bias current cannot be changed, maximum adaptive biasing ratio for a stable operation might limit the achievable BW.

4. CONCLUSION AND FUTURE WORKS

In this thesis, loop gains of the LDO regulators with adaptive bias are analyzed. The effect of the adaptive bias loop on the LDO stability is investigated. The additional poles and zeros caused by the adaptive bias loop are calculated and for stable operation stability criteria are obtained for two stage LDOs and four stage LDOs with Miller compensation. The calculations are verified with the Monte Carlo simulations. It is shown that for the LDOs without Miller compensation the additional zeros created by the adaptive bias loop should be placed after the unity gain frequency to achieve stable operation. For the LDOs using Miller compensation, the zeros created by the adaptive bias loop can be controlled in terms of their half plane locations and with the given criterion they can be placed on the left half plane for a stable operation. With the outcomes of the analysis the tradeoff between the stability and the low quiescent current is explained.

Another outcome of the derived criteria is, differential pair transistors can be sized such that always left half plane zero can be guaranteed in the transfer function of the differential pair and for a Miller compensated LDO the overall loop gain always show LHP zeros and the huge variation of the phase margin can be prevented.

An improvement for the adaptive biasing can be using a current limit circuit for the adaptive biasing transistor. With this configuration bias current of the first stage can be increased but the effect of the adaptive bias loop in terms of AC behavior will be broken because of the current limiting transistor for high load currents. Since the loop gain is divided by $1\text{-}A_{ab}$, with this configuration loop gain will be increased since adaptive bias loop gain will be negligible because of the current limit transistor.

A journal paper is being planned for this topic. The methodology defined in this work can also be applied to other multi-loop linear circuit applications.

REFERENCES

[1] **Morita, G.** (2014). Understand Low-Dropout Regulator (LDO) Concepts to Achieve Optimal Designs. AnalogDialogue. Retrieved April 11, 2017, from http://www.analog.com/en/analog-dialogue/articles/understand-ldo-concepts.html

[2] **Lee, B. S.** (1999). Understanding the Terms and Definitions of LDO Voltage Regulators. Texas Instruments. Retrieved April 11, 2017, from http://www.ti.com/lit/an/slva079/slva079.pdf

[3] **Maity, A., and Patra, A.** (2015). Dynamic slew enhancement technique for improving transient response in an adaptively biased low-dropout regulator, *IEEE Trans. Circuits Syst. II Exp. Briefs*, **62**, 626-630.

[4] **Ho, M., and Leung, K. N.** (2011). Dynamic bias-current boosting technique for ultralow-power low-dropout regulator in biomedical applications, *IEEE Trans. Circuits Syst. II Exp. Briefs*, **58**, 174-178.

[5] **Man, T. Y., Mok, P., and Chan, M.** (2007). A high slew-rate push-pull output amplifier for low-quiescent current low-dropout regulators with transient-response improvement, *IEEE Trans. Circuits Syst. II Exp. Briefs*, **54**, 755-759.

[6] **Ming, X., Li, Q., Zhou, Z., and Zhang, B.** (2012). An ultrafast adaptively biased capacitorless ldo with dynamic charging control, *IEEE Trans. Circuits Syst. II Exp. Briefs*, **59**, 40-44.

[7] **Qu, X., Zhou, Z., Zhang, B., and Li, Z.** (2013). An ultralow-power fast-transient capacitor-free low-dropout regulator with assistant push-pull output stage, *IEEE Trans. Circuits Syst. II Exp. Briefs*, **60**, 96-100.

[8] **Kim, Y., and Lee, S.** (2013). A capacitorless ldo regulator with fast feedback technique and low-quiescent current error amplifier, *IEEE Trans. Circuits Syst. II Exp. Briefs*, **60**, 326-330.

[9] **Maity, A., and Patra, A.** (2016). Design and analysis of an adaptively biased low dropout regulator using enhanced current mirror buffer, *IEEE Trans. Power Electron.*, **31**, 2324-2336.

[10] **Leung, K. N., and Ng, Y. S.** (2010). A cmos low-dropout regulator with a momentarily current-boosting voltage buffer, *IEEE Trans. Circuits Syst. I Reg. Papers*, **57**, 2312-2319.

[11] **Zheng, C., and Ma, D.** (2011). Design of monolithic cmos ldo regulator with d^2 coupling and adaptive transmission control for adaptive wireless powered bio--implants, *IEEE Trans. Circuits Syst. I Reg. Papers*, **58**, 2377-2387.

[12] **Man, T. Y., Leung, K. N., Leung, C. Y., Mok, P., and Chan, M.** (2008). Development of single-transistor-control ldo based on flipped voltage

follower for soc, *IEEE Trans. Circuits Syst. I Reg. Papers,* **55**, 1392-1401.

[13] **Or, P. Y., and Leung, K. N.** (2010). A fast-transient low-dropout regulator with load-tracking impedance adjustment and loop-gain boosting technique, *IEEE Trans. Circuits Syst. II Exp. Briefs,* **57**, 757-761.

[14] **Or, P. Y., and Leung, K. N.** (2010). An output-capacitorless low-dropout regulator with direct voltage-spike detection, *IEEE J. Solid-State Circuits,* **45**, 458-466.

[15] **Guo, J., and Leung, K. N.** (2010). A 6-μw chip-area-efficient output-capacitorless ldo in 90-nm cmos technology, *IEEE J. Solid-State Circuits,* **45**, 1896-1905.

[16] **Tan, X. L., Koay, K. C., Chong, S. S., and Chan, P. K.** (2014). A fvf ldo regulator with dual-summed miller frequency compensation for wide load capacitance range applications, *IEEE Trans. Circuits Syst. I Reg. Papers,* **61**, 1304-1312.

[17] **Al-Shyoukh , M., Lee, H., and Perez, R.** (2007). A transient-enhanced low-quiescent current low-dropout regulator with buffer impedance attenuation, *IEEE J. Solid-State Circuits,* **42**, 1732-1742.

[18] **Chava, C. K., and Silva-Martinez, J.** (2004). A frequency compensation scheme for ldo voltage regulators, *IEEE Trans. Circuits Syst. I Reg. Papers,* **51**, 1041-1050.

[19] **Lin, H. C., Wu H. H., and Chang, T. Y.** (2008). An active-frequency compensation scheme for cmos low-dropout regulators with transient-response improvement, *IEEE Trans. Circuits Syst. II Exp. Briefs,* **55**, 853-857.

[20] **Lau, S. K., Mok P., and Leung, K. N.** (2007). A low-dropout regulator for soc with q-reduction, *IEEE J. Solid-State Circuits,* **42**, 658-664.

[21] **Zhan, C., and Ki, W. H.** (2012). An output-capacitor-free adaptively biased low-dropout regulator with subthreshold undershoot-reduction for soc, *IEEE Trans. Circuits Syst. I Reg. Papers,* **59**, 1119-1131.

[22] **Zhan, C., and Ki, W. H.** (2010). Output-capacitor-free adaptively biased low-dropout regulator for system-on-chips, *IEEE Trans. Circuits Syst. I Reg. Papers,* **57**, 1017-1028.

[23] **Chong, S. S., and Chan, P. K.** (2013). A 0.9-μA quiescent current output-capacitorless ldo regulator with adaptive power transistors in 65-nm cmos, *IEEE Trans. Circuits Syst. I Reg. Papers,* **60**, 1072-1081.

[24] **Hazucha, P., Karnik, T., Bloechel, B. A., Parsons, C., Finan, D., and Borkar, S.** (2005). Area-efficient linear regulator with ultra-fast load regulation, *IEEE J. Solid-State Circuits,* **40**, 933-940.

[25] **Milliken, R. J., Silva-Martinez, J., and Sanchez-Sinencio, E.** (2007). Full on-chip cmos low-dropout voltage regulator, *IEEE Trans. Circuits Syst. I Reg. Papers,* **54**, 1879-1890.

[26] **Ho, E., and Mok, P.** (2010). A capacitor-less cmos active feedback low-dropout regulator with slew-rate enhancement for portable on-chip

application, *IEEE Trans. Circuits Syst. II Exp. Briefs*, **57**, 80-84.

[27] **Leung, K. N., and Mok, P.** (2003). A capacitor-free cmos low-dropout regulator with damping-factor-control frequency compensation, *IEEE J. Solid-State Circuits*, **38**, 1691-1702.

[28] **Hong, S. W., and Cho, G. H.** (2016). High-gain wide-bandwidth capacitor-less low-dropout regulator (ldo) for mobile applications utilizing frequency response of multiple feedback loops, *IEEE Trans. Circuits Syst. I Reg. Papers*, **63**, 46-57.

[29] **Razavi, B.** (2016). *Design of Analog CMOS Integrated Circuits 2nd ed.* New York : McGraw-Hill.

APPENDICES

APPENDIX A: Nyquist and bode plots

APPENDIX A

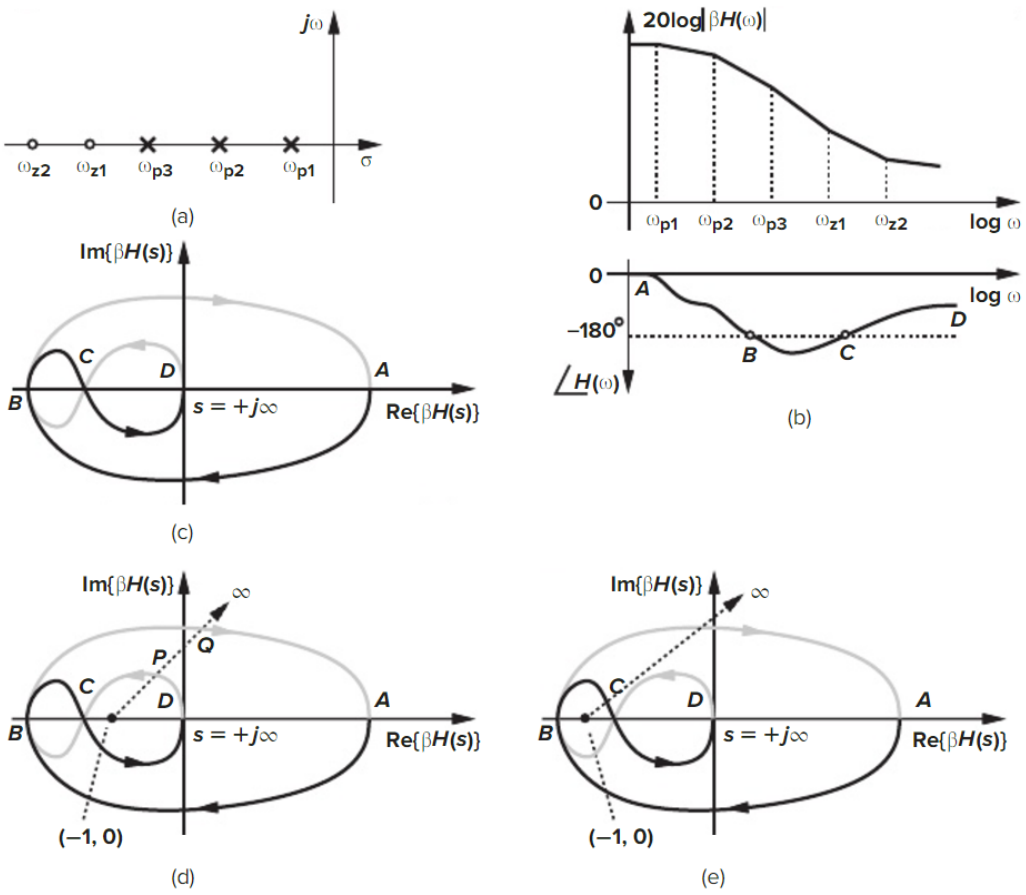

Figure A.1 : (a) System with three poles and two zeros, (b) Bode plots, (c) βH contour, (d) case where C is to the left of (-1,0), and (e) case where C is to the right of (-1,0) [29].

CURRICULUM VITAE

Name Surname : Türker Unutmaz

Place and Date of Birth : Istanbul, 1991

E-mail : trkrntmz@gmail.com

B.Sc. : 2014, ITU, Electronics Engineering

Professional Experience :

- AMS Design and Verification Engineer, Dialog Semiconductor AS., Istanbul
  Dec 2016 - present
- Analog Design Engineer, Dialog Semiconductor AS., Istanbul
  Apr 2016 - Nov 2016
- Junior Analog Design Engineer, Dialog Semiconductor AS., Istanbul
  Oct 2014 - Mar 2016