DESIGN, FABRICATION AND CHARACTERIZATION OF INTERDIGITATED BACK CONTACT SILICON SOLAR CELLS

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ABSTRACT

DESIGN, FABRICATION AND CHARACTERIZATION OF INTERDIGITATED BACK CONTACT SILICON SOLAR CELLS

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The design and development of high-efficiency interdigitated back contact (IBC) solar cells have been studied within the scope of this thesis. Developing a totally industry-compatible, lithography-free, high-throughput process flow for the fabrication of IBC cells was the main motivation of the thesis. For this, a detailed simulation study was conducted using Quokka 2 software to optimize the rear side cell geometry and understand the effect of bulk and layer properties on the device performance. After determining three different cell geometries with varying pitch values of 750, 1250, and 1700 μm, a totally screen-printing-based process flow was designed and applied to fabricate IBC cells. For selective diffusion, thick SiN_x layers with optimized layer compositions were used as the diffusion barriers during the high-temperature boron and phosphorus diffusion process. The patterning of the barrier layers was done using a screen-printable ink with enhanced chemical resistance in acidic solutions. Following the optimization of the diffusion barrier properties and corresponding patterning step, diffusion and corresponding passivation properties were optimized. BCl_3 and $POCl_3$ diffusion recipes were studied in detail not only for the rear emitter and back surface field (BSF) regions but also for the front non-contacted junctions. Industrial fire-through (FT) metals

pastes were used for the metallization of rear junctions whose corresponding optimization was done with the help of detailed contact resistivity analysis. Combining all optimized process parameters for the cell fabrication resulted in maximum efficiency of 19.3% (FF:71.2%, V_{oc}:642 mV, J_{sc}:37 mA/cm^2) for FFE-IBC cell structure which was 19.2% (FF:70.3%, V_{oc}:637 mV, J_{sc}:39 mA/cm^2) for FSF-IBC structure.

In addition to IBC studies, polySi passivating contact cells were also focused on in this thesis. In addition to their passivating properties, ex-situ doped polySi layers of varying thicknesses were studied also for their contacting properties. Excellent passivation properties were obtained for the case of n-polySi layers with the corresponding total recombination parameters (J_0) of 1.6 and 7.4 fA/cm^2 on textured and polished wafers, respectively. For the case of p-polySi layers, 16.3 and 70.2 fA/cm^2 were obtained on the polished and textured wafers. Regarding the contacting properties, a novel methodology to extract the contact recombination parameter ($J_{0,contact}$) was developed. The extracted $J_{0,contact}$ values were lying within the range of 300-400 fA/cm^2 for relatively thicker n-polySi and p-polySi layers which increased to 1000 and 700 fA/cm^2 for their thinner counterparts. Obtained $J_{0,contact}$ values were then correlated to high-resolution SEM images to better understand the contact formation and paste-polySi interaction.

Keywords: Interdigitated back contact solar cells, passivating contact solar cells, recombination parameter.

ÖZ

ARKA KONTAK ARKA EKLEMLİ SİLİSYUM GÜNEŞ GÖZELERİNİN TASARIM, ÜRETİM VE KARAKTERİZASYONU

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Bu tez kapsamında yüksek verimli iç içe geçmiş arkadan bağlantılı (IBC) tipi güneş hücrelerinin tasarım ve geliştirilmesi çalışılmıştır. Tezin ana motivasyonu tamamen endüstriye uyarlanabilir, litografi gerektirmeyen, yüksek üretim çıktılı bir IBC üretim yöntemi geliştirmektir. Bu amaçla, Quokka 2 yazılımı kullanılarak arka yüzey geometrisinin optimize edilip, silisyum alttaş ve üzerindeki tabakaların özelliklerinin aygıt performansı üzerindeki etkisi simüle edilmiştir. Simülasyon çalışmalarının ardından 750, 1250 ve 1700 µm hücre açıklığına üç farklı yapı seçilmiş ve önerilen tamamen serigrafi tabanlı IBC üretim yöntemi bu üç farklı hücre geometrisi için kullanılmıştır. Hücre aşamasında seçici difüzyon için kompozisyonu optimize edilmiş kalın SiN_x tabakaları yüksek sıcaklık bor ve fosfor katkılama işlemleri sırasında bariyer olarak kullanılmıştır. Bariyer tabakalarının desenleme işlemi serigrafi ile serilen, asidik solüsyonlarda kimyasal dayanımı yüksek olan özel bir mürekkep kullanarak yapılmıştır. Difüzyon bariyeri özellikleri ve ilgili desenleme işlemlerinin optimizasyonun ardından, katkılama ve yüzey pasivasyonu çalışmaları devam etmiştir. Hem arka yüzey emiter ve arka yüzey alanı (BSF) hem de ön yüzey kontak atılmamış eklem bölgeleri için BCl_3 ve $POCl_3$ difüzyon reçeteleri detaylı bir şekilde çalışılıp, optimize edilmiştir. Metalizasyon

için endüstriyel metal pastalar kullanılmış, kontak direnci çalışmaları yardımıyla gerekli optimizasyonlar tamamlanmıştır. Optimize edilmiş tüm proses parametreleri kullanılarak üretimi tamamlanan FFE-IBC hücrelerde en yüksek verim değeri %19.3 (FF:%71.2, V_{oc}:642 mV, J_{sc}:37 mA/cm^2) seviyelerine ulaşırken, FSF-IBC hücreler için bu değer %19.2 (FF:%70.3, V_{oc}:637 mV, J_{sc}:39 mA/cm^2) seviyesine çıkmıştır.

IBC çalışmalarına ek olarak, çoklu kristal silisyum (polySi) ile pasive edilmiş hücreler de bu tez kapsamında incelenmiştir. Pasivasyon özelliklerinin yanı sıra haricen katkılanmış polySi katmanlarının kontak özellikleri de farklı tabaka kalınlıkları için incelenmiştir. N-tipi polySi tabaka için parlak yüzeylerde 1,6 ve piramitli yüzeyde 7,4 fA/cm^2 gibi oldukça düşük seviyelerde toplam rekombinasyon parametrelerine (J0) ulaşılmıştır. P-tipi polySi tabakalar için toplam J0 değerleri parlak yüzey için 16,3 ve piramitli yüzey için 70,2 fA/cm^2 seviyelerine kadar düşürülmüştür. Kontak özellikleri düşünüldüğünde ise, kontak rekombinasyon kayıp parametresi ($J_{0,contact}$) hesaplaması için özgün bir yöntem geliştirilmiştir. Bu yöntem kullanılarak elde edilen $J_{0,contact}$ değerleri kalın olan n-tipi ve p-tipi polySi tabakaları için 300-400 fA/cm^2 seviyelerinde kalırken, daha ince olan n-tipi ve p-tipi polySi tabakaları için bu değer sırasıyla 1000 ve 700 fA/cm^2 kadar yükselmiştir. Elden edilen $J_{0,contact}$ değerleri sonrasında yüksek çözünürlüklü taramalı elektron mikroskobu (HR-SEM) görüntüleriyle ilişkilendirilip kontak oluşum mekanizması ve metal pasta-polySi tabakası etkileşimi daha iyi anlaşılmıştır.

Anahtar Kelimeler: İç içe geçmiş arkadan bağlantılı güneş hücreleri, pasive olmuş kontaklı güneş hücreleri, rekombinasyon.

To my family, dearest friends, and my cat Tarçın

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TABLE OF CONTENTS

LIST OF TABLES

TABLES

LIST OF FIGURES

FIGURES

LIST OF ABBREVIATIONS

ABBREVIATIONS

4PP Four Point Probe

AM Air Mass

APCVD Atmospheric Pressure Chemical Vapour Deposition

ARC Anti-Reflective Coating

BSF Back Surface Field

BSG Boron Silicate Glass

CVD Chemical Vapour Deposition

ECV Electrochemical Capacitance-Voltage

EQE External Quantum Efficiency

EWT Emitter Wrap Through

FFE Front Floating Emitter

FSF Front Surface Field

FT Fire-Through

HIT Heterojunction with Intrinsic Thin layer

IBC Interdigitated Back Contact

IPA Isopropyl Alcohol

J-V Current Density-Voltage

LPCVD Low-Pressure Chemical Vapour Deposition

MWT Metal Wrap Through

PECVD Plasma Enhanced Chemical Vapour Deposition

PERC Passivated Emitter and Rear Contact/Cell

PERL Passivated Emitter and Rear Locally diffused

PERT Passivated Emitter and Rear Totally diffused

PL Photoluminescence

PSG Phosphorous Silicate Glass

RCA Radio Corporation of America

SDE Saw-Damage Etched

SEM Scanning Electron Microscopy

LIST OF SYMBOLS

SYMBOLS

FF Fill Factor

iV_{oc} Implied Open-Circuit Voltage

J Current

J_{sc} Short-Circuit Current Density

J_0 Recombination Current Density

$J_{0,co}$ Recombination Current Density Under Metal Contacts

n Number of Free Electrons in the Conduction Band

R Resistance

ρ_{co} Contact Resistivity

R_{series} Series Resistance

R_{shunt} Shunt Resistance

T Absolute Temperature

V_{oc} Open-Circuit Voltage

λ Wavelength

μ Mobility

σ Conductivity

CHAPTER 1

INTRODUCTION

In 2020, the world's annual energy demand was 25000 TWh and fossil energy was still the most used form of energy which is based on limited sources and harmful emissions. As shown in Figure 1.1, the total ratio of fossil energy in 2020 was 60.96% including coal, gas, and oil which means quite a significant amount of CO_2 emission.

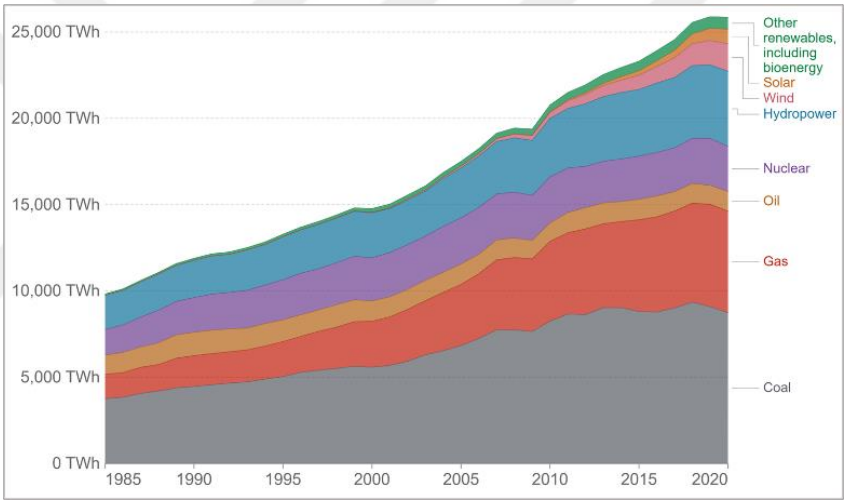


Figure 1.1. World's energy source distribution [1].

The remaining 39.04% of the energy was provided by carbon-free energy sources whose 2.85% was from solar, 6.28% was from wind, and 2.74% was from other renewables including biomass, geothermal, waste, wave, and tidal. Still, 10.12% of the energy was provided by nuclear while 17.05% was from hydropower [1]. However, considering the total global CO_2 emission, shown in Figure 1.2, and its effect on atmospheric temperatures, it is crucial to reduce the usage of fossil fuels [1]–[3]. According to Intergovernmental Panel on Climate Change (IPCC), the temperature increase since the middle of the 20th century was mainly due to the

increasing greenhouse gases concentrations in the atmosphere caused by fossil fuel burning and deforestation [4].

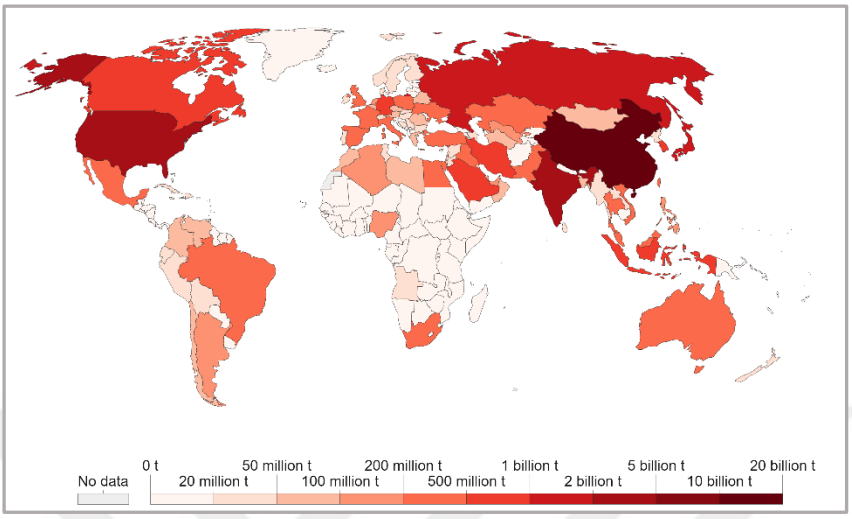


Figure 1.2. Annual CO_2 emissions from the burning of fossil fuels for energy and cement production in 2020. Land-use change is not included [1].

The Earth receives average solar irradiation of 1367 W/m^2 outside the atmosphere and such a large amount of received energy is enough to supply the energy need of the whole planet [5], [6]. The solar irradiation can be directly converted into electricity by photovoltaic cells through a noise and emission-free operation.

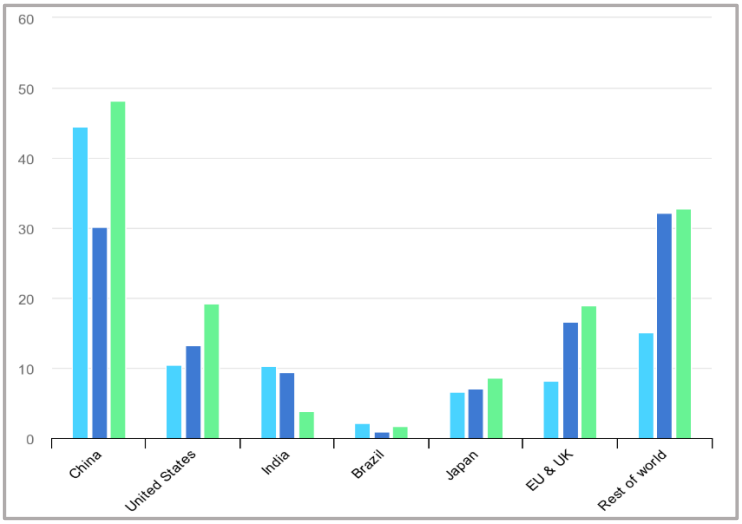


Figure 1.3. Net solar PV capacity additions 2018-2020 [7].

Thus, photovoltaics is a promising technology to provide environmentally friendly and sustainable energy. The production and total installation of solar cells is increasing rapidly. As seen in Figure 1.3, the installed photovoltaic capacity has been rapidly increasing. In 2020, solar PV generation reached 821 TWh by a record increase of 156 TWh (23%) [7].

However, according to Net Zero Scenario, the global energy-related carbon dioxide emission would be brought to net zero to limit the global temperature rise below 2°C preferentially 1.5°C [8]. For this, an annual generation growth of 24% between 2020 and 2030 is required which corresponds to 630 GW of net capacity additions in 2030. To achieve such great dissemination successfully done, further reduction of the manufacturing costs of the PV systems is required together with proper regulations for system installations.

Improving cell efficiency has a high impact on reducing manufacturing costs. Progressing technology has already enabled the manufacturing of 26.30% efficient cells in mass production [9], [10]. Amongst the other cell structures, interdigitated back contact solar cells have the highest efficiency potential with their zero shading losses. While Kaneka is the record holder company on silicon heterojunction-IBC cells with their 26.63% efficiency on 180 cm^2, SunPower is the other company producing IBC cells with the highest efficiency of 25.2% [11], [12]. Zebra-IBC cell is a young member of the industrial IBC family with their large area efficiencies exceeding 24% [13]. Despite their high-efficiency potential, fabrication of interdigitated back contact solar cells is challenging and requires multiple masking steps. Although many different research centers demonstrated small area cell results, corresponding fabrication sequences were mostly relying on photolithography and thermal evaporation. Thus, there is still a gap to develop a cost-effective manufacturing technology.

Due to the potential of reaching high efficiencies with cost-effective manufacturing technology, the present thesis focuses on the design of interdigitated back contact solar cells and the development of a cost-effective fabrication sequence of the

designed cell structure. With the help of additional simulations and detailed characterization, further increase of the device efficiency is also possible.

1.1 Interdigitated Back Contact Solar Cells and Advantages

Interdigitated back contact solar cells exhibit both emitter and base junctions and corresponding metal electrodes at the rear side of the cells. By this, IBC solar cells have several advantages over the conventional front and back contacted solar cells. These advantages can be listed as in the following:

- Metal shading losses are eliminated which results in increased short circuit current density (J_{sc}).
- In the absence of metal contacts at the front side, front side diffusion concentration and passivation layer properties can be optimized for optimum light trapping and passivation properties without any concern for metallization.
- Since all metals are placed at the rear side, the metal finger width would not be limited by the shading concerns. Thus, the series resistance will be reduced.
- Co-planar interconnection increases the packing density of the IBC cells during the module assembly process. Therefore, cell-to-module (C2M) losses are less compared to the modules of front and back contacted cells.
- Homogenous front side appearance makes IBC cells and modules more attractive for building integrated photovoltaic (BIPV) applications.

Despite all the above-mentioned advantages, there are also some risks and challenges related to the interdigitated back contact cell structures. These risks and challenges are:

- Due to the complicated structure of IBC cells, processing requires additional steps which makes the fabrication of IBC cells more complicated and challenging
- High position accuracy is required in the masking steps to avoid fatal shunting between n^+ doped and p^+ doped electrodes.
- Since all junctions are placed at the rear side of the cells, base material is required to be high quality and more stable during successive high temperature process steps.

While the risks and challenges about the complicated processing technology and requirement of a high-quality base material increases the manufacturing cost, the increased cell efficiency would balance that increment in the cost. Within the scope of this thesis, a less complicated, industry-compatible fabrication method could have successfully been developed and applied.

1.2 Motivation of the Thesis

The main motivation of this thesis is to develop a novel IBC cell fabrication method which is not available in literature with following properties:

i. Lithography-free process sequence.
ii. Utilize the tools already available in n-Si and p-Si industrial production lines.
iii. Suitable for batch process.

1.3 Aims of the Thesis

In this thesis, the following goals are tried to be reached at:

i. Design an IBC cell structure with an optimized gap, BSF and emitter width for 4x4 cm^2 small area cells on 156.75x156.75 mm^2 Cz-Si wafers.

ii. Observe the effect of different doping profiles (i.e., depth, peak concentration) of emitter and BSF on device performance.
iii. See the effect of base material, i.e., either p-type or n-type Si.
iv. See the effect of front surface doping profile and understand the effect of FFE and FSF on device performance.
v. Optimize the passivation layer for front side and rear side independently using test structures.
vi. Develop a novel fabrication method using only industry compatible systems, i.e., diffusion furnaces ($POCl_3$ and BCl_3), PECVD, screen printer and firing furnace.
vii. Optimize peak firing temperature for fire-through (FT) AgAl and FT-Ag paste on boron doped and phosphorus doped regions respectively.
viii. Optimize the required metal fraction with high FF but with as low $J_{0,contact}$ as possible.
ix. Carry out electrical and optical characterization on the fabricated small cells.

1.4 Thesis Plan

1.4.1 Simulation

i. Effect of emitter fraction for a constant pitch on the cell performance for ideal contacts (contact resistivity: $1x10^{-4}$ $\Omega.cm^2$) for various bulk lifetime (low, moderate, high) and bulk resistivity values will be examined. The influence of FFE and FSF on carrier transport is also aimed to be understood.
ii. Effect of emitter and BSF regions' sheet resistances will be verified for varying emitter/BSF ratios. Bulk lifetime will be fixed based on the results of previous section while base resistivity will again be swept.

Moreover, unit cell size will also be varied from smaller to larger unit cell sizes.

iii. The best performing cell parameters of the previous section will be utilized. Emitter and BSF sheet resistances will be set to a certain point to that the effect of varying gap fraction, passivating quality of the gap and wafer thickness will be examined.

1.4.2 Fabrication & Characterization

i. Optimization of etch resist
   - Printing parameters
   - Alignment control using optical microscope
   - Curing temperature and time
   - Patterning (chemical resistance of the printed etch resist during dielectric patterning)
   - Stripping and post cleaning

ii. Optimization of diffusion barrier thickness and composition for BCl_3 and $POCl_3$ diffusions

iii. Optimization of boron (BCl_3) and Phosphorus ($POCl_3$) diffusion both for front and rear side
   - Sheet resistance and electrochemical capacitance voltage (ECV) measurements
   - Photoluminescence (PL) measurements

iv. Optimization of SiO_2/SiN_x and Al_2O_3/SiN_x stack as passivation layer for BSF, gap, emitter, FFE and FSF regions on test structures (before and after firing).
   - Photoluminescence (PL) measurements
   - Sinton PCD measurements

v. Optimization of metallization
   - Peak firing condition

- Conveyor belt speed
    - Transfer length measurements (TLM) for contact resistivity analysis on bifacial cells

vi. Small area cell fabrication using optimized recipes
    - Sheet resistance measurements (after each process step)
    - Sinton PCD and PL measurements on test structures and half fabricated cell structures
    - Solar simulator (I-V) measurements following the metallization
    - External quantum efficiency (EQE) measurements on the final device

1.5 Thesis Outline

Chapter 2: Thesis starts with a literature survey on the back contact solar cells including metal wrap through (MWT), emitter wrap through (EWT) and interdigitated back contact (IBC) solar cells. The current efficiency values together with the process details of the cells from different research centers and companies are covered in this chapter.

Chapter 3: In this chapter, a detailed simulation study conducted using Quokka2 software. By the end of this chapter, the effect of bulk properties, front side diffusion, emitter and BSF diffusions, and the cell geometry will be realized.

Chapter 4: A novel fabrication process flow will be suggested and applied for the first time. Composition and thickness of SiN_x layer will be optimized to be used as the diffusion barrier. Patterning of the barrier layers will be done using screen-printable etch resist followed by dilute acidic etching. The first IBC cells will be fabricated using the suggested fabrication sequence.

Chapter 5: Boron and phosphorus diffusion processes will be studied in detail for this chapter. Various BCl_3 and $POCl_3$ recipes were applied on symmetrical

test samples. SiO_2/SiN_x and Al_2O_3/SiN_x stacks are utilized to passivate the doped surfaces while corresponding lifetime measurements were done for before and after diffusion conditions. Moreover, contacting properties of the samples were checked for fire metallization pastes.

Chapter 6: In this chapter, process parameters and recipes optimized in the previous chapter were used to fabricate FFE and FSF-IBS cells. The resulting cells were analyzed as a function of front surface doping, cell pitch, and applied peak firing temperatures.

Chapter 7: In this chapter, polySi passivating contact studies conducted at ECN, Netherlands will be covered. Passivating and contacting properties of doped polySi layers are analyzed for varying polySi layer thicknesses. A novel method was developed to extract contact recombination current density ($J_{0,contact}$) and compared with the results of other methods. As the final task of this chapter, all poly passivated contact cells were fabricated and characterized.

CHAPTER 2

BACK CONTACT SOLAR CELLS

In this chapter, background information about back contact (BC) solar cells will be given together with the best efficiency values. Interdigitated back contact (IBC) solar cells, as being the main topic of this thesis, will be analyzed in detail.

2.1 Introduction

In recent years, n-type solar cells have received growing attention from many cell manufacturers and research centers due to their high-efficiency potential. Unlike p-type silicon (Si), the lack of boron (B)-oxygen (O) complexes increases minority carrier lifetime and makes n-type Si more resistant to light-induced degradation (LID) [14]. More advanced cell architectures utilizing n-type Si like hetero-junction (HJT), passivating contact and back contact-back junction (BC-BJ) are capable of reaching efficiency values above 20% at the industrial level [15]. However, all these advanced technologies require high-quality base materials and more complicated process steps. According to ITRPV-2020 report; despite these requirements, both HJT and Interdigitated back contact (IBC) technologies are expected to increase their market share while that of back surface field (BSF) will shrink and even end by 2025 [16].

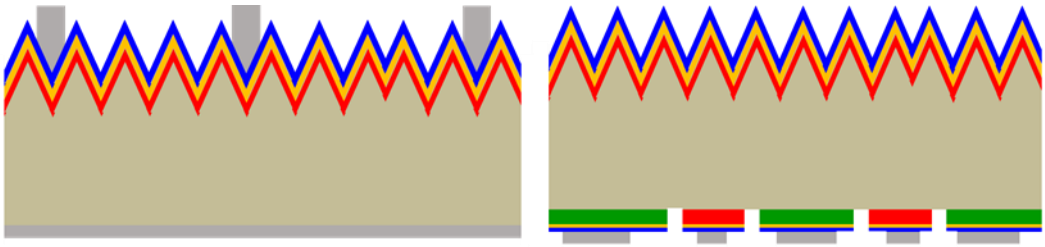


Figure 2.1. Cross-sectional view of a standard Al-BSF (left) and an IBC (right) cell.

The Cross-sectional view of an Al-BSF and IBC cell is given in Figure 2.1. BC solar cells offer various advantages over the cells with front metallization pattern. Firstly, front metal is completely or partially moved to the rear side of the cell as in the case of emitter wrap through (EWT) and interdigitated back contact (IBC) or metal wrap through (MWT) respectively. Thus, optical shading is either partially reduced or eliminated. Secondly, back contact solar cells require less gap between neighboring cells during module fabrication. Thus, a higher packing fraction is reached. As a result, cell to module losses is minimized and a more aesthetic appearance is obtained with BC-BJ modules which is demanded for BIPV applications. Despite all these advantages of back contact solar cells, their market share is still low due to the fact that their fabrication is more complicated and requires multiple patterning and alignment steps [17].

IBC structure where all metallization is moved to the rear side of the wafer as an interdigitated pattern has the highest efficiency potential amongst the other BC-BJ cells [18]. Although various fabrication methods have been offered by different research centers, most of them rely on lithographical patterning steps. This makes the processes more time consuming, more expensive and less industry compatible. Design, optimization and development of an industry-compatible fabrication method of IBC cells will be studied in detail within the scope of this thesis.

2.2 Classification of Back Contact (BC) Solar Cells

2.2.1 Emitter Wrap Through (EWT) Solar Cells

Emitter wrap through (EWT) is the BC structure where all metallization pattern is moved to the rear side of the c-Si wafer as in the case of IBC structure. In the IBC case, however, both junction polarities are placed at the rear side and a high-quality absorber is needed to collect the generated carriers at the corresponding contacts. On the contrary, EWT structure was developed to circumvent this high quality absorber demand [19].

In EWT design with cross-sectional view shown in Figure 2.2, the cell is equipped with a front and a rear emitter region electrically connected by means of small holes, so called "*vias*" drilled through the base wafer. Then, the generated carriers travel to the rear side of the c-Si through those conductive pathways. Hence, low cost materials with lower minority diffusion lengths could be utilized as absorber[19].

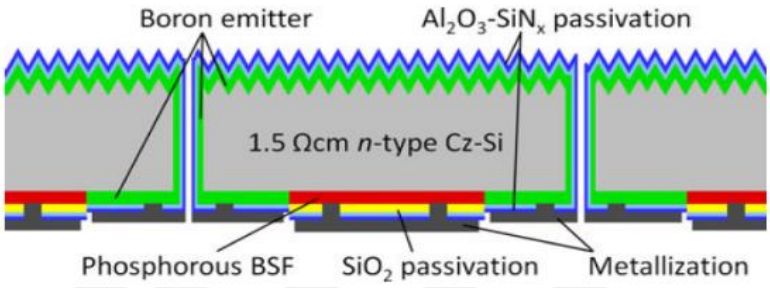


Figure 2.2. Cross-sectional view of an EWT solar cell [7].

Moreover, unlike IBC cells EWT cells are more robust against front passivation quality and bulk lifetime due to the existence of highly doped front emitter [20]. Considering the process flow of an EWT cell with n-type absorber in Figure 2.3, additional drilling and laser induced damage removal steps are required [20].

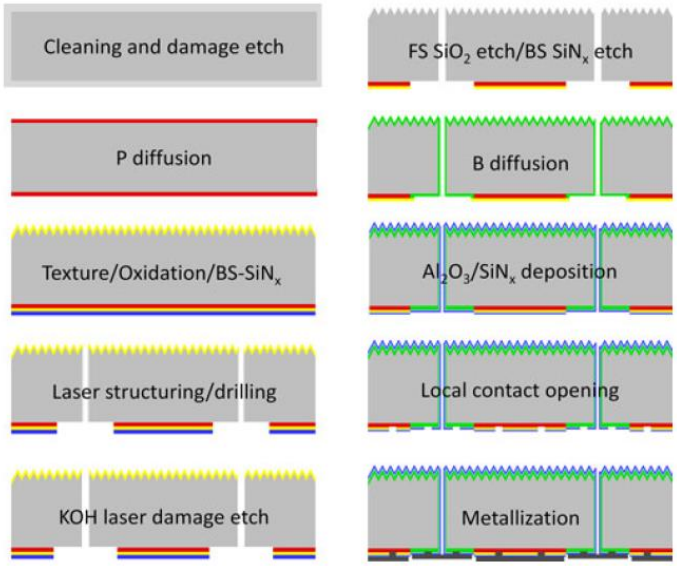


Figure 2.3. Process sequence of an EWT solar cell [7].

The basic issue prevented EWT architecture becoming an industrial technology is the time-consuming laser drilling step and resulting stress induced on the substrate. Per each wafer approximately 15,000-20,000 via holes are drilled by laser [19]. Putting thousands of holes on a wafer makes it brittle against the following process steps like high temperature diffusion, cleaning or screen printing. Although 21.6% efficiency was obtained on 4 cm^2 cells [20], EWT technology could not be successfully transferred to industrial production lines.

2.2.2 Metal Wrap Through (MWT) Solar Cells

Metal wrap through (MWT) is another BC architecture where front contact busbars are moved to the rear side through the laser drilled vias. Thus, front shading loses [21] and surface recombination is partially reduced, as a result cell efficiency will be improved [22]. Cross-sectional view of MWT cells with p-Si and n-Si is given in Figure 2.4.

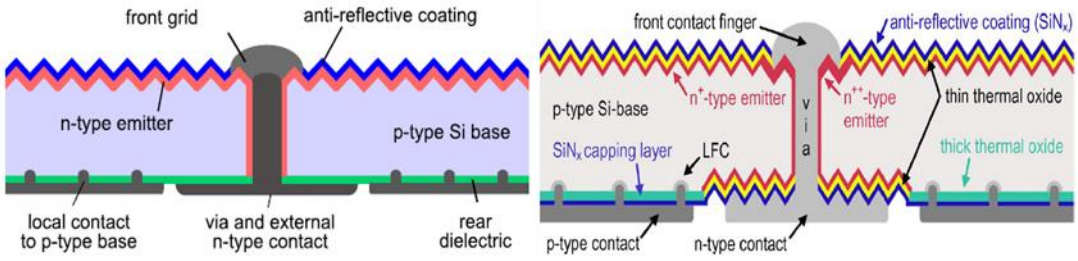


Figure 2.4. Cross-sectional view of a p-MWT (left) [10] and an n-MWT (right) [30] cells.

For cost effective p-MWT cell fabrication; additional laser drilling and laser induced damage removal steps could be adapted to already available standard p-type solar cell production lines [23]. To further improve the cell performance, additional steps of n-MWT cell process were successfully adapted to n-type cell production lines. Front and rear side of an n-MWT cell which is fabricated at full scale using industrial tools can be seen in Figure 2.5 [24].

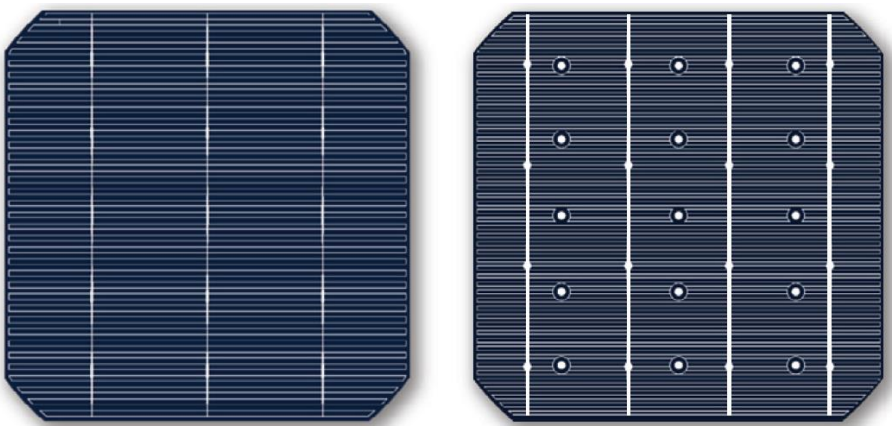


Figure 2.5. Image *of* an n-MWT cell, front side (left) and rear side (right) [24].

At the module side, a full back interconnection is offered for MWT cells. This results in lower resistive losses unlike the regular double-side interconnection of H-pattern solar cells with tabs, and lower cell to module loss is obtained. Moreover, the use of thinner cells is allowed for MWT technology which would directly reduce the cost [22].

20.1% and 19.4% efficiency values were obtained for p-MWT on p-type FZ and Cz Si wafers respectively. For the fabrication, $POCl_3$ diffusion was used for emitter formation whereas screen printing was utilized for contact formation. Best performing device on Cz wafer had a V_{oc} of 647 mV, J_{sc} of 39.3 mA/cm^2 and an FF of 76.2%. For the FZ case, best V_{oc} was 658 mV, J_{sc} was 39mA/cm^2 and FF was 78.4%. For n-MWT solar cells (239 cm^2), the best efficiency was obtained as 20.1%, with corresponding FF of 77%, V_{oc} of 653 mV and J_{sc} of 40.01 mA/cm^2. The best performing reference (n-PASHA) cell of the same batch had an efficiency of 19.98%, FF of 78.5%, V_{oc} of 653 mV and J_{sc} of 38.97 mA/cm^2 [25]. N-MWT module of 60 cells, had a maximum output power of 272 W with an average cell efficiency of 18.9%. Resulting cell to module (C2M) FF loss was 0.8%. The module of 60 n-PASHA cells had a maximum output power of 265 W with 18.6% average cell efficiency and C2M loss was 3%. Combining MWT with hetero-junction (SHJ) technology results in V_{oc}: 719 mV, J_{sc}: 39.3 mA/cm^2, FF: 80% and eta: 22.6% for a cell area of 243 cm^2 [21].

2.2.3 Interdigitated Back Contact (IBC) Solar Cells

Interdigitated back contact (IBC) is the most promising BC-BJ cell structure. Despite its more complicated design and process sequence, various research centers and their industrial partners have been putting great effort for the last decade to transfer this technology to industrial production lines.

Considering the device architectures, IBC cells can be separated into 3 main groups. For the first group, the front side of the cell is doped with the same polarity as the base Si wafer and it is called as *front surface field (FSF)*. For the second group, the front side is doped at the opposite polarity of the base Si wafer and it is called as *front floating emitter (FFE)*. Corresponding cross-sections of IBC cell with FSF and FFE are given in Figure 2.6.

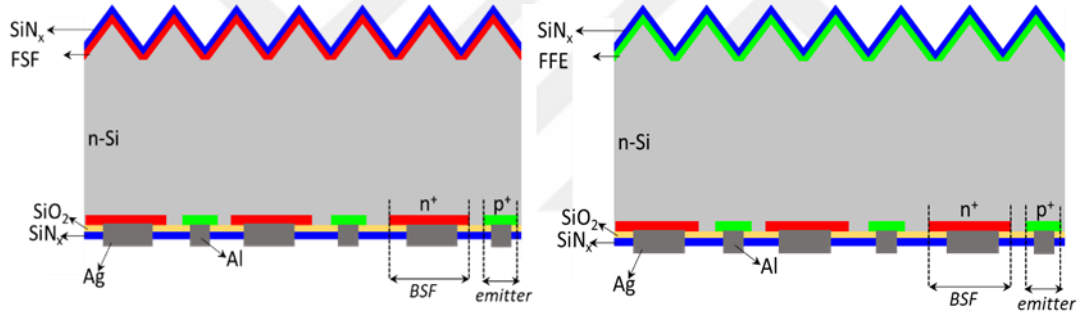


Figure 2.6. Cross-sectional view of IBC cell with FSF (left) and FFE (right).

IBC cells with undiffused front surface form the last group where the surface passivation quality becomes crucial. Thus, most of the current studies in the literature focuses on IBC with FFE or FSF where cells with undiffused front surface are barely studied. Although most of the studies utilizes photolithography-based patterning which requires additional alignment, patterning and cleaning steps, there exist two cell architectures aiming industrial application. The first one is *Mercury* cell developed by ECN which employs a FFE and is first developed for p-type Si wafer. Then, the technology is adapted for n-PASHA baseline. The second structure is *Zebra* cell employs a FSF and developed by University of Konstanz. For the fabrication of Zebra cells, 156x156 mm, p-type, Cz substrates

are aimed to be used with the possible minimum number of additional steps. Then, obtained knowledge is transferred to n-Si baseline to reach higher efficiency values.

i. Mercury Cells

For the fabrication of Mercury cells, $POCl_3$ and BBr_3 diffusions are applied for 156x156 mm^2, n-Cz Si wafers. Metallization of the cells are done using industrial screen printing with fire through (FT) pastes [26]. The cross-section of the resulting cell is given in Figure 2.7.

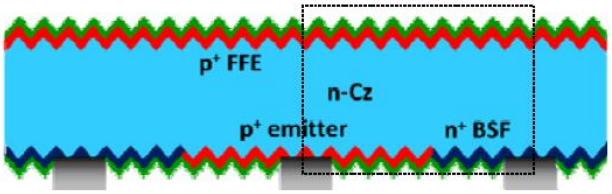


Figure 2.7. Schematic cross-section of a Mercury IBC cell [26].

The best performing cell with an area of 239 mm^2 results in 20.9% efficiency with V_{oc}: 656 mV, J_{sc}: 41.2 mA/cm^2 and FF: 77.1%. Combining Mercury cell concept with conductive foil-based module technology is expected to result in low cell to module losses.

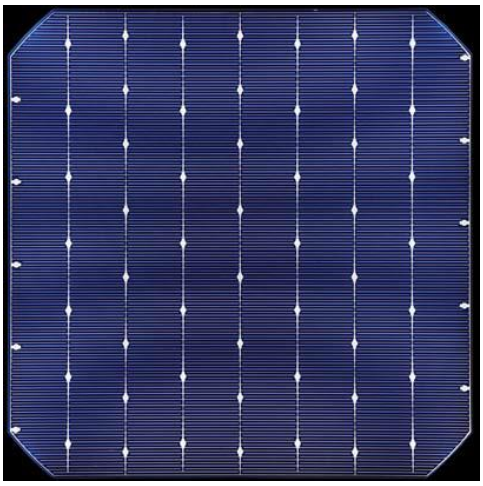


Figure 2.8. Interconnection design of Mercury IBC cell [26].

Although there is no reported module performance yet, the interconnection design of Mercury IBC cells consists of 62 interconnection points as shown in Figure 2.8. All busbars and interconnection points are directly screen printed using industrial FT-pastes. Then, the interconnection points on the cells are contacted to conductive foil by electrically conductive adhesive dots which are printed on the foil and cured during module lamination process [26].

ii. **Zebra Cells**

Zebra IBC cell is the other cell structure utilizing standard industrial size 156x156 mm^2, n-Cz wafers and only industrially proven technologies. Different than Mercury cells, Zebra cells employs an n diffused FSF with the given cross-section in Figure 2.9. Moreover, as a result of the reduced metal coverage at the rear side, Zebra-IBC cells can operate in bifacial mode [27].

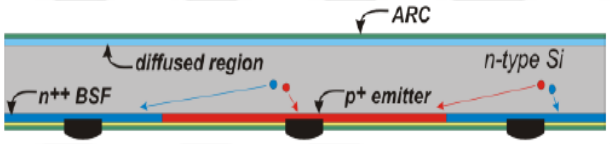


Figure 2.9. Schematic cross-section of a Zebra-IBC solar cell [27].

The process sequence of Zebra cells can be simply implemented in a standard Al-BSF production line by only adding a BBr_3 diffusion furnace which is already specialized for n-type solar cell production lines[27]. The best performing Zebra cell with screen printed metal contacts has an efficiency of 21.3% with V_{oc}: 647.9 mV, J_{sc}:41.9 mA/cm^2 and FF: 78.5% where the average efficiency for the corresponding batch of 28 cells was 21%[27]. One cell Zebra module results in a cell to module FF loss of 2.58% compared to Al-BSF module which has a cell to module loss of 3.32%. Moreover, with the help of bifaciality; a bifacial module shows 17.6% more power output than the monofacial Al-BSF module with the black back sheet [27]. Later, within the scope of a collaboration with an industrial partner, it was announced that Zebra cells reached an efficiency of 23.6% in a

production line with an accompanied cell V_{oc} of 691.6 mV, J_{sc} of 41.4 mA/cm^2 and FF of 80.9% [13].

There exists only one company, SunPower Corp., which has been the pioneer in interdigitating back contact technology since 1970's [28]. Their patented cell technology resulted in a world record of 25.2% efficiency (153.49 cm^2) in 2016. Although no process details have been shared, their production technology is known to be the passivating contact technology relying on industrial process steps. The corresponding cell V_{oc} was 737 mV, J_{sc} was 41.33 mA/cm^2 and FF was 82.7% [29]. Then, the modules constructed using 72 laboratory cells resulted in a module efficiency of 24.1% with V_{oc}: 52.77 V, I_{sc}:6.306 A and FF: 81.9% [29]. In addition to their cell production technology, SunPower's module technology is also unique. Combining their newest cell design Maxeon with their new generation module technology SunPower X-series has resulted in a record-breaking panel efficiency of 22.8% [30]. For Maxeon cells optimized front side texturing and anti-reflection coating (ARC) provides unique light trapping properties and grabs more power. A patterned solid copper sheet is placed at the rear side which provides massive strength and extreme resistance against corrosion. Thick connectors used between neighboring cells in X-series modules provides flexibility for expansion/contraction due to daily temperature swings [31].

(a) **(b)** **(c)**

Figure 2.10. Image of the front side (a), rear side (b) and module interconnection (c) of a Maxeon solar cell [31].

Coupling the IBC design with the excellent passivation properties of intrinsic thin amorphous Si (a-Si) layer generates hetero-junction-IBC (HJ-IBC). Kaneka developed a HJ-IBC cell with a record-breaking efficiency of 26.3% with V_{oc}: 744 mV, J_{sc}:42.3 mA/cm^2 and FF:83.8% (180.4 cm^2)[32]. The schematic cross-section and current-voltage curve are given in Figure 2.11.

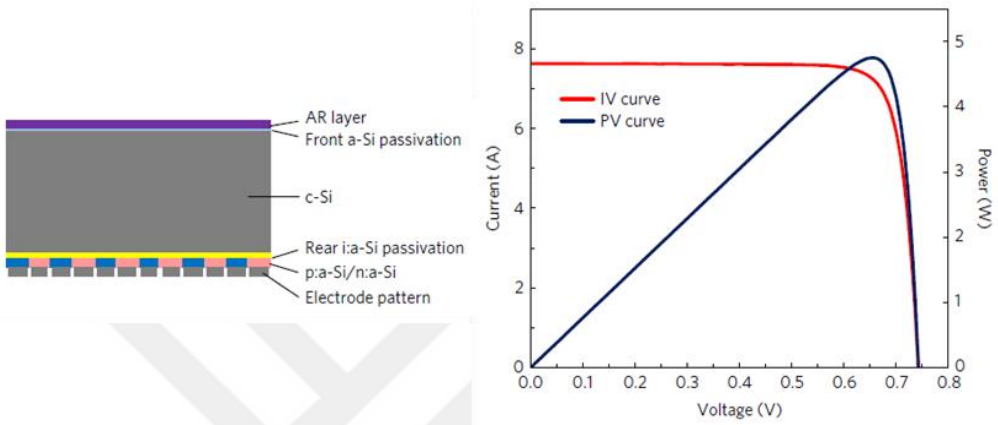


Figure 2.11. Schematic cross-section (left) and current-voltage curve (right) of the record-breaking HJ-IBC cell [19].

The HJ-IBC cell was fabricated using 3 Ω.cm, 165 μm thick, n-Cz Si wafer. Rear side is fully passivated by intrinsic a-Si (i:a-Si). Patterned p-type a-Si (p:a-Si) and n-type (n:a-Si) layers are placed on top of i:a-Si and used to collect holes and electrons, respectively. Front side is passivated using an a-Si layer which is capped by a dielectric anti-reflection layer [32]. Further improvements on the cell structure including increased wafer thickness, reduced optical losses and mainly improved FF from 83.8 to 84.6% increased the record efficiency from 26.3 to 26.6% at full scale [33].

Other than industrial IBC studies, many research centers are focusing on developing IBC cells using different techniques and cell architectures. Heterojunction with intrinsic thin silicon (HIT), polySi-passivating contact and homo-junction cell structures are widely applied in IBC cell studies. For the IBC cells with homo-junctions usually high temperature diffusion and ion implantation processes are applied. $POCl_3$ diffusion is widely utilized for the formation of n^+

doped BSF/FSF region whereas BBr_3 or BCl_3 diffusion is utilized for the formation of p^+ doped emitter/FFE regions. P^+ or B^+ implantation which is followed by an additional activation step is used as an alternative for $POCl_3$ or BBr_3 diffusion. However, both techniques require additional masking and patterning steps which makes fabrication more complex and more expensive.

For the IBC cell developed at Australian National University (ANU), all patterning is done using photolithography. High temperature phosphorus and boron diffusion was applied for the formation of FSF/BSF and emitter respectively. Another photolithography step was applied to define metal contact regions with diameter of 5 µm and pitch of 70 µm. PECVD deposited SiN_x was used on the front side whereas PECVD deposited SiO_2 layer for the rear side passivation. Aluminum (Al) is then deposited to blanket the rear side of the cell which is then lithographically patterned as an interdigitated pattern [34]. The image of the final device is given in Figure 2.12.

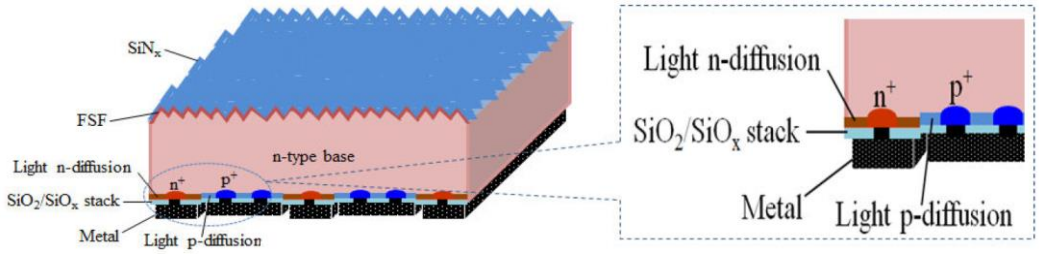


Figure 2.12. Cross-section view of the IBC cell developed at ANU [34].

Although no cell result was announced for that cell structure, total recombination current density (J_0) was obtained to be 26 fA/cm^2 after the final metallization step [34].

Similarly, in another study carried out by Polytechnic University of Catalonia, photolithography and high temperature phosphorus and boron diffusion processes were applied on 4-inch, p-type, FZ-Si wafers. Al_2O_3 was used for front side passivation whereas SiO_2 layer was used for that of rear side. The last patterning step and lift was done to obtain contact opening prior to metallization. E-beam evaporated Al is used for contacting of emitter and BSF regions at the rear side.

Then a last lift off and annealing steps were applied [35]. The image of the fabricated cell and current-voltage curve of the best performing device is given in Figure 2.13.

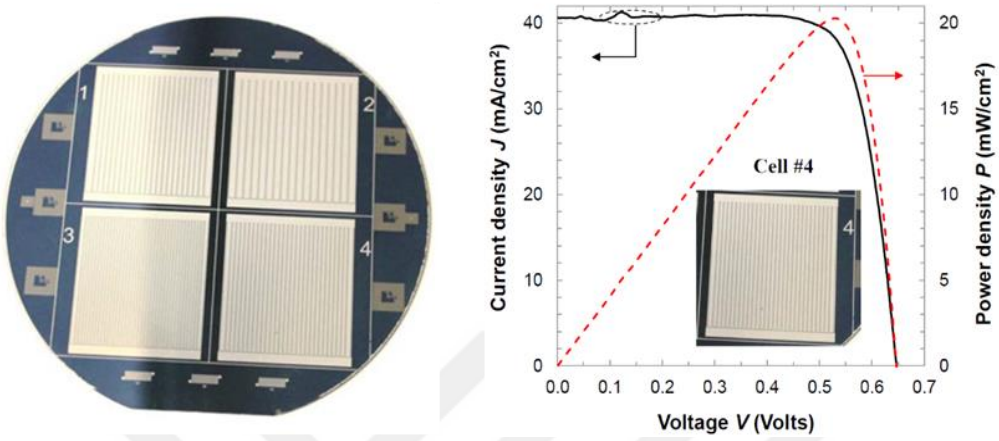


Figure 2.13. Image of the developed IBC cells (left) and I-V curve (right) of the best performing device [21].

The best performing device has an efficiency of 20.3% with V_{oc}: 648 mV, J_{sc}:40.6 mA/cm^2 and FF:77.2% [35].

Fabrication of IBC cells utilizing high temperature diffusion processes is generally coupled with photolithography-based patterning steps requiring alignment, patterning and cleaning steps. To facilitate process sequence, printable doping pastes with boron or phosphorus additives are developed. Application of a boron doping paste instead of BBr_3 or BCl_3 diffusion reduces fabrication cost and complexity. For the IBC structure developed by Fraunhofer ISE and Merck, boron doping paste is utilized for the formation of emitter region. Screen printed boron doping paste is activated simultaneously as BSF formation via $POCl_3$ diffusion or during the activation of PECVD/APCVD deposited PSG layer [36]. Full area, textured wafers are utilized as test structures for sheet resistance mapping and J_0 extraction. However, 2x2 cm^2 cells are fabricated on 156x156 mm^2 wafers for the proof of concept. The image of the designed cell structure is given in Figure 2.14.

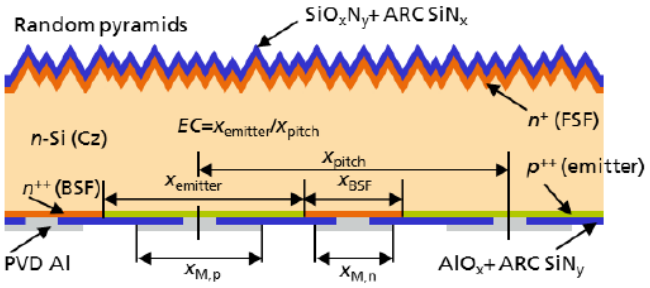


Figure 2.14. Schematic cross-section of the designed IBC cell [36].

SIMS measurements, given in Figure 2.15, revealed that exposing the boron-paste covered regions to $POCl_3$:O_2:N_2 ambient does not significantly affect the boron concentration. Since boron concentration is never overcompensated by that of phosphorus, the used paste is deemed to be a sufficient diffusion barrier during $POCl_3$ diffusion. Moreover, the observed boron concentration above solubility limit within the first 25-30 nm region of the surface indicates the existence of the boron rich layer (BRL). In order to avoid the formation of recombination-active BRL layer at the surface, diffusion processes and the following cleaning procedure is needed to be adjusted properly [36].

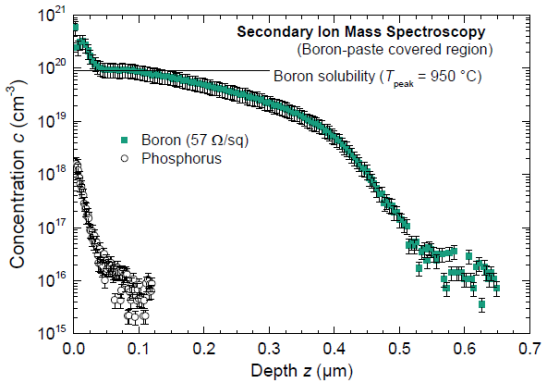


Figure 2.15. SIMS results for boron paste printed regions after $POCl_3$ exposure [36].

The first 4 cm^2 cells averaged over 9 devices showed an average efficiency of 20.9±0.3% with V_{oc}: 656±3 mV, J_{sc}:41±0.2 mA/cm^2 and FF:77.6±0.5%. Considering the reduced fabrication cost and saved process time, application of doping paste is observed to be promising for the fabrication of IBC cells.

In addition to IBC cells where the emitter and BSF regions are formed via high temperature diffusion processes, there exist some IBC studies where ion implantation is applied for the formation of doped regions. Although the implantation process itself is quite complicated, proper application of implant process for IBC cell fabrication shortens the process sequence significantly. For the implantation process where local doping is possible, complex patterning and successive cleaning steps become unnecessary. Also, it is possible to precisely control the dose and the depth of doping with implantation. Thus, it could be directly utilized for the formation of homo-junction IBC cells or combined with passivating contact technology to have IBC cells with doped polySi emitter and BSF regions.

For the IBC study carried out at Fraunhofer ISE, different implant doses were used both for boron and phosphorus doping. The resulting doping profiles for the samples annealed at 1050°C for 80 min. are given in Figure 2.16 [37].

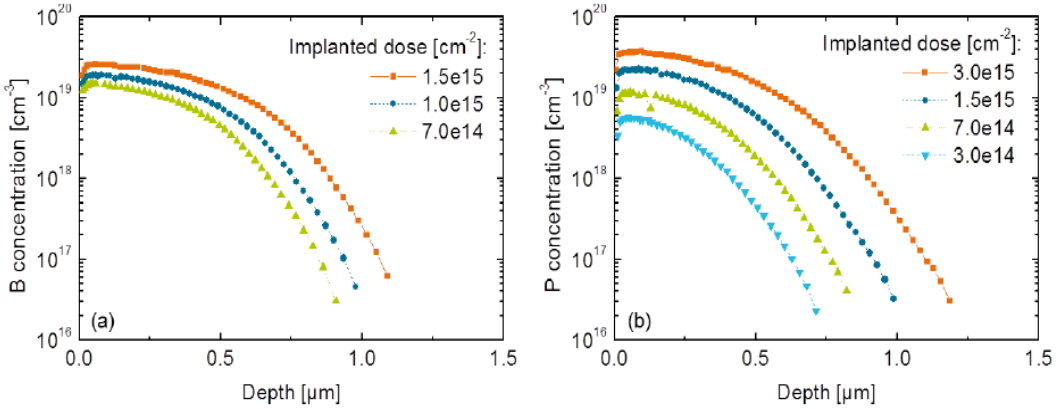


Figure 2.16. Resulting ECV profiles for various implant doses of boron (left) and of phosphorus (right) ions after annealing at 1050°C for 80 minutes [23].

Thus, various ion concentrations between 3E18 and 3E19 cm^{-3} could successfully be obtained. Then, using a dose of 1.5E15 and 3E15 cm^{-3} for boron and phosphorus implants respectively, a 2x2 cm^2 IBC cell with an industrial metal pitch of 2.1 mm with a lowly doped FFE. The corresponding emitter sheet resistance was 73 Ω/□ while that of BSF was 39 Ω/□. FFE is also implanted with a dose of 1E14 cm^{-2} and

the resulting sheet resistance was 650 Ω/□. SiO_2/Al_2O_3 stack is applied on the front side whereas SiO_2/SiN_x stack was used at the rear side to provide surface passivation. Then, Al was evaporated and structured in a wet chemical etch solution with a photoresist mask [37]. The corresponding current-voltage curve and schematic image is shown in Figure 2.17.

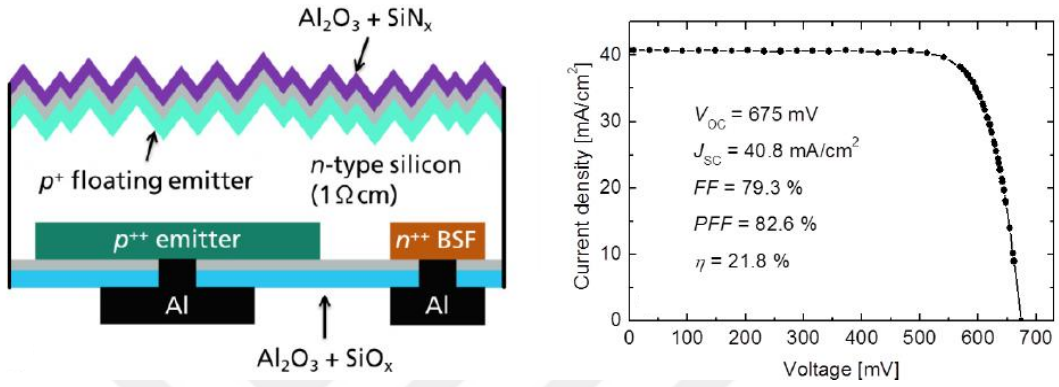


Figure 2.17. Schematic cross-section (left) and current-voltage curve (right) of the fabricated IBC cell [23].

The best performing device has an efficiency of 21.8% with V_{oc}: 675 mV, J_{sc}:40.8 mA/cm^2 and FF:79.3%[37]. Thus, application of ion implantation for IBC processes is highly promising. However, to enhance the cell performance, surface passivation of the IBC cells should be improved. Thus, the naturally induced damage at the surface during implantation step should be avoided. For this, ion implantation is coupled with HIT-IBC and passivating contact IBC cell structures.

For the ion implanted passivating contact IBC cell studies carried out at NREL, P and B implanted a-Si layers were applied on top of a thin SiO_2 layer so called *interdigitated back passivated contact (IBPC)* [38]. Saturation current densities (J_0) and contact resistivity values are analyzed for various implant doses and post annealing conditions. For the symmetrical test structures, the lowest J_0 for Si:P layer was 2.4 fA/cm^2 while it was 10 fA/cm^2 for Si:B layers[39]. The same layers were transferred to IBPC cell structure, and the corresponding cross-section is given in Figure 2.18.

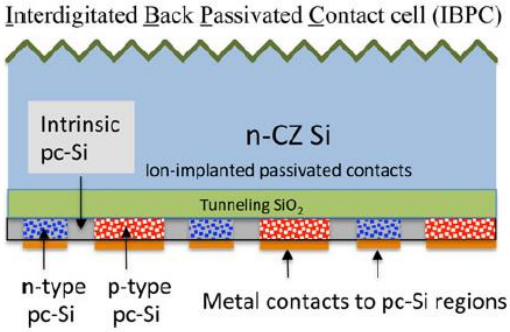


Figure 2.18. Schematic of a IBPC cell formed by ion implantation [25].

The resulting implied V_{oc} (iV_{oc}) values of the un-metallized cell with B and P implant was obtained as 692 mV with the corresponding total J_0 of 11 fA/cm^2. For the contact resistivity analysis, transmission line measurements (TLM) were applied and the metal pads for TLM measurements were defined by using photolithography. Obtained contact resistivity values were quite high (> 40 mΩ.cm^2). Although *iVoc* values are promising, metallization requires further optimization to reduce contact resistivity below 30 mΩ.cm^2 while not significantly increasing the J_0 under metal contacts [39].

In another passivating contact IBC study carried out by Delft University of Technology (TU-Delft), LPCVD deposited polySi layers were implanted with B and P for emitter and BSF/FSF regions respectively [40]. The schematic of the fabricated cell structure and ECV profiles of the possible B and P implants to be applied for the cell structure are given in Figure 2.19.

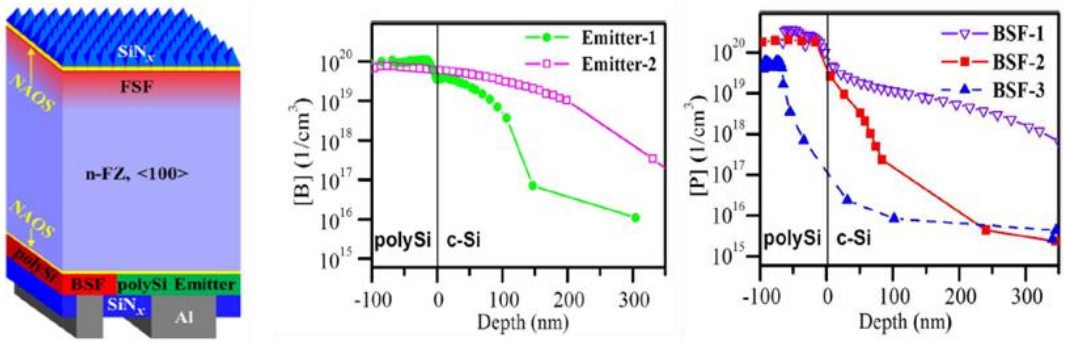


Figure 2.19. Cross-sectional view of the fabricated IBC cell(left), ECV profiles of B-implant (middle) and P-implant (right) to be used in cell fabrication for emitter and BSF regions respectively [26].

For the best performing cell structure BSF-2 and emitter-1 profiles were applied with the same dose of 5E15cm^{-2} at 20 keV. Front surface was passivated with FSF with a phosphor dose of 5E14 cm^{-2} at 20 keV. The resulting cell (9 cm^2) has an efficiency of 19.2% with V_{oc}: 673 mV, J_{sc}:38 mA/cm^2 and FF:75.2% [40]. In a later study of the same group where FSF is passivated with a thin a-Si layer and a gap is placed between emitter and BSF regions, the cell efficiency is increased to 22.1% with V_{oc}: 709 mV, J_{sc}:40.7 mA/cm^2 and FF:76.6% [41].

Unlike TU-Delft`s design, Fraunhofer ISE`s design skips successive photolithography steps for local implantation. A boron doped TOPCon layer is deposited to fully cover the rear side of the wafer. Then, local P-implant is carried out using a shadow mask [42]. As a result, boron concentration is locally overcompensated by that of phosphorus atoms as shown in Figure 2.20.

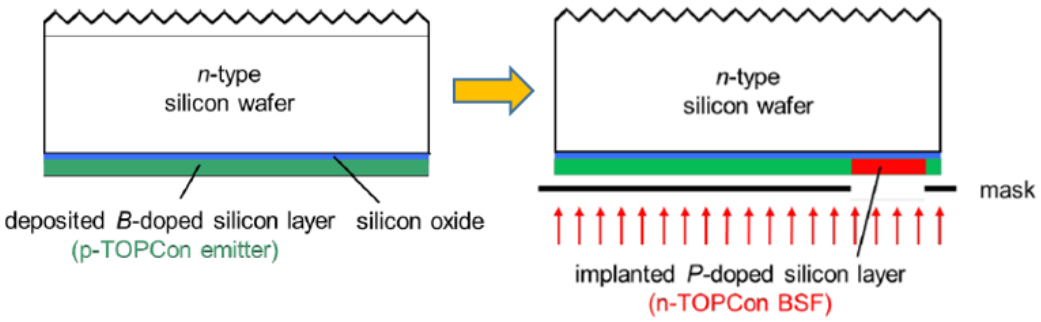


Figure 2.20. Schematic of local P-implant for TOPCon-IBC fabrication [42].

Final cell structure has an *iVoc* of 682 and 631 mV for respective annealing temperatures of 800 and 900 ºC [42]. With the help of improvements in the cell design and implant processes, the efficiency of a 4 cm^2 cell is increased to 23.7% with V_{oc}: 720 mV, J_{sc}:41.4 mA/cm^2 and FF:79.6%.

In another device structure designed and fabricated by EPFL, doped a-Si layers are deposited on top of a thin (i)a-Si layer as emitter and BSF region as shown in Figure 2.21. Patterned deposition of the emitter and BSF regions is provided by an in-situ shadow masking. Also, an (i)a-Si/(n)a-Si stack is used as FSF at the front side to provide surface passivation which is then capped by SiN_x layer. TCO/Ag

stack is deposited by physical vapor evaporation and then patterned by using a combination of hot-melt printing and wet chemical etching[43].

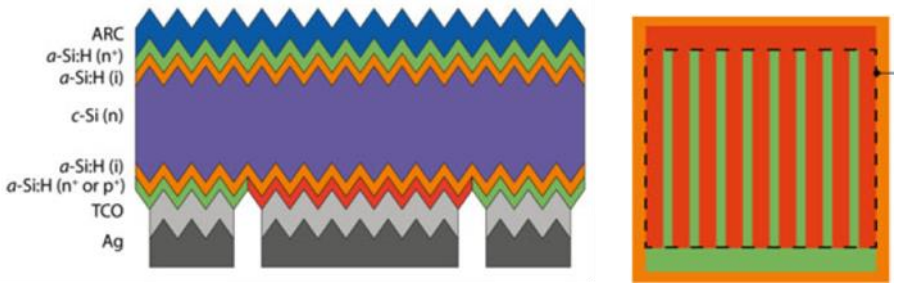


Figure 2.21. Schematic cross-section (left) and rear side image of SHJ-IBC cells [29].

The best performing cell (9 cm^2) has an efficiency of 22.0% with V_{oc}: 726 mV, J_{sc}:40.9 mA/cm^2 and FF:74.0% [43]. Further improvement of the FF is expected to increase the efficiency above 23%.

Like Fraunhofer-ISE's TOPCon cells, ISFH's POLO structure also uses polySi passivating layers. To combine POLO structure with IBC, initially deposited blanked i-polySi layers were locally converted to n-polySi and p-polySi using ion implantation and the contact separation was done via laser scribing[44], [45]. The resulting cell schematic and corresponding I-V curve are shown in Figure 2.22. Unlike many other IBC cell design, in POLO-IBC p type Si was used as the base material.

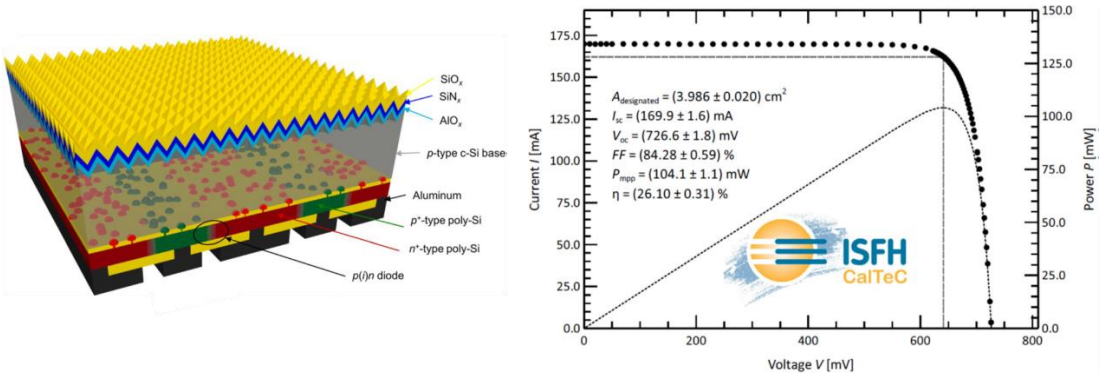


Figure 2.22. Schematic of the record POLO-IBC cell (left) and corresponding current-voltage characteristics (right).

For the cell area of 4 cm ^{2} cell, a record efficiency of 26.1% was obtained with the corresponding cell parameters of V_{oc}: 726.6 mV, I_{sc}: 169.9 mA and FF: 84.28% as shown in Figure 2.22 (right).

A summary of up-to-date efficiency values for different back contact-back junction cells from different institutes/companies is shown in Table 2.1.

To sum up, there are many different process sequences from different research centers to fabricate IBC solar cells with different designs. However, except two leading companies SunPower and Kaneka, there has been no optimized industrial process flow resulting in efficiencies exceeding 20% for full scale wafers. ISC Konstanz has just joined that group of two with their full area, 24% efficient Zebra cells. In this thesis, a novel process sequence will be designed and optimized for the fabrication IBC cells using only industry-compatible tools. It is aimed to be a lithography-free process flow applicable for 156.75x156.75 mm^2 wafers.

Table 2.1. Summary of best performing back contact-back junction cell efficiencies.

Institute	Country	Technology	Efficiency
Sun Power	USA	IBC (2016)	**25.2**
Kaneka	Korea	HJ-BC (2017)	**26.6**
ISFH	Germany	POLO-IBC (2021)	**26.1**
Konstanz	Germany	IBC (2020)	**23.6**
Advent Solar	USA	EWT	16.0
Konstanz	Germany	EWT	13.0
ISFH	Germany	EWT	21.4
QCELLS	Germany	EWT	17.1
Fraunhofer-ISE	Germany	EWT-photolithography	21.4
IMEC	Belgium	IBC	23.1
ANU	Australia	IBC	24.4
ISFH	Germany	IBC	23.1
IMEC	Belgium	IBC	23.3
Institut fur Photovoltaik	Germany	IBC	22
ANU & Trina Solar	Australia &	IBC	22.1
Varian & Fraunhofer-ISE	USA & Germany	IBC-Al_2O_3 passivation+ion implantation	20.0
Samsung	Korea	IBC- ion implantation	22.4
Fraunhofer-ISE	Germany	IBC- ion implantation	21.8
ISFH & Bosch & Amat	Germany & USA	IBC- ion implantation	22.1
ECN	Netherlands	IBC-Mercury	19.6
ISFH	Germany	IBC-n type RISE	23.1
Varian & Fraunhofer-ISE	USA & Germany	IBC-SiO_2 passivation+ion implantation	19.2
IMEC	Belgium	MWT	14.7
ECN	Netherlands	MWT	16.7
Fraunhofer-ISE	Germany	MWT	16.2
Konstanz	Germany	MWT	17.5

CHAPTER 3

SIMULATION OF INTERDIGITATED BACK CONTACT SOLAR CELLS

In this chapter, the effect various parameters defining bulk properties (dopant type (n-type or p-type), bulk lifetime, bulk resistance, wafer thickness), cell geometry (emitter, BSF and gap width), properties of back junctions (sheet resistances of emitter and BSF regions, corresponding recombination current densities) and front junction properties (sheet resistance, dopant type (n doped or p-doped), recombination current density) on resulting cell performance were modelled using Quokka2.

3.1 Introduction

Quokka2 is a free software developed for fast simulation of various silicon solar cell structures in one to three dimensions. To have less computational effort, thus, for faster simulations, some simplifications to the general carrier transport model were employed. Those simplifications could be named as quasi-neutrality and conductive boundary. For conductive boundary simplification, the near surface regions are defined by using lumped input parameters instead of being modelled in detail. That is, instead of defining the doping profile, sheet resistance of the doped region is required and the solutions are for the steady-state conditions [46]. As proposed in different studies, the diffusion at the surface could be treated as a recombinative boundary, thus, the solution of the transport equations in the diffused and space charge regions could be omitted [47], [48]. Outside the space charge region where quasi-neutrality condition holds true, the equality of excess carrier densities can be applied [49].

Bulk (Base) Equations

Under these conditions, the continuity equations of the quasi-Fermi potentials for a p-type base material are given by,

$$\nabla(\sigma_n \nabla\varphi_{Fn}) = q(G - R) \qquad (Eq.3.1)$$

$$\nabla\left(\sigma_p \nabla\varphi_{Fp}\right) = -q(G - R) \qquad (Eq.3.2)$$

Here σ denotes the conductivity of each carrier type, q stands for the elementary charge $1.6\text{x}10^{-19}$ C, G and R denote and generation and recombination rates, respectively. Injection level dependent conductivities are calculated using Klaassen's method [50]. Applying the expressions combining intrinsic carrier density n_i, thermal voltage V_t and quasi-Fermi potentials φ_{Fn} and φ_{Fp}, equilibrium carrier concentrations n and p could be calculated as in the following equations:

$$n = n_i exp\left(\frac{\varphi_{el} + \varphi_{Fn}}{V_t}\right) \qquad (Eq.3.3)$$

$$p = n_i exp\left(\frac{-\varphi_{el} - \varphi_{Fp}}{V_t}\right) \qquad (Eq.3.4)$$

Applying the condition of equal excess carrier densities which is $p \approx n + N_A - n_0$ where N_A is the ionized acceptor density and n_0 is the equilibrium electron concentration which could also be defined by $n_0 = \frac{n_i^2}{N_A}$ results in the following equation:

$$n = \exp\left(-\frac{\varphi_{Fp}}{V_t}\right) x\sqrt{n_i^2 exp\left(\frac{\varphi_{Fp}+\varphi_{Fn}}{V_t}\right) + \frac{(N_A-n_0)^2}{4}\exp\left(\frac{2\varphi_{FP}}{V_t}\right)} - \frac{N_A-n_0}{2} \qquad (Eq.3.5)$$

Boundary Conditions

i. Symmetry Planes: At the symmetry planes the gradient of the quasi-Fermi potential in the direction of the surface normal is zero.

$$\vec{n}\nabla\varphi_{Fn/p} = 0 \qquad (Eq.3.6)$$

ii. Undiffused Surfaces: Recombination at the undiffused surfaces either defined by dark saturation current densities (J_{01} and J_{02}) or by surface recombination velocity (SRV). Dark saturation current density and SRV concepts are equivalent for low injection condition and for ideal recombination with the following relation:

$$J_{01} = \frac{Sqn_i^2}{N_A} \qquad (Eq.3.7)$$

Then, the electron current becomes equal to:

$$\sigma_n \, \vec{n}\nabla\varphi_{Fn} = -J_{01}\left(\frac{np}{n_i^2} - 1\right) - J_{02}\left(\sqrt{\frac{np}{n_i^2}} - 1\right) \qquad (Eq.3.8)$$

iii. Diffused Surfaces: In a diffused layer, a 2-D continuity equation of the majority quasi-Fermi potential φ_{Fdiff} accompanied by the sheet resistance R_{sheet} account for the conduction of carriers.

$$\nabla_t\left(\frac{\nabla_t\varphi_{diff}}{R_{sheet}}\right) = -J_{diff} \qquad (Eq.3.9)$$

For the n-type emitter, continuity equation gives the boundary condition for the bulk electron quasi-Fermi potential as $\varphi_{Fn}=\varphi_{Fdiff,}$ and the J_{diff} is equal the total current density from the base into the emitter minus the current density into the contact [51].

$$J_{diff} = \sigma_n \, \vec{n}\nabla\varphi_{Fn} + \sigma_p \, \vec{n}\nabla\varphi_{Fp} - \frac{V_{term} - \varphi_{Fdiff}}{r_c} \qquad (Eq.3.10)$$

Here, r_c stays for contact resistivity and V_{term} stays for the terminal voltage for the case of contacted regions.

The hole current density into the boundary is equal to the difference of the recombination current density and the current density collected within the diffused

layer J_L. As a result, the boundary condition for the hole quasi-Ferro potential becomes as shown in the following:

$$\sigma_p \, \vec{n} \nabla \varphi_{Fp} = -J_{01}\left(\frac{np}{n_i^2} - 1\right) - J_{02}\left(\sqrt{\frac{np}{n_i^2}} - 1\right) - J_L \qquad (Eq.\,3.11)$$

Generation and Recombination

Spectrum of a monochromatic light with a given intensity for a specific wavelength and A.M.1.5G spectrum are the predefined generation models included into Quokka. Moreover, it is also possible to load a user defined generation profile or a J_L value which can be obtained by using free tools like OPAL and EDNA [51], [52], [53].

3.2 Simulation Approach

3.2.1 Determination of the Bulk Properties

In this part of the study, Quokka 2 was applied for various bulk parameters and cell geometries to generate a starting point for the experimental IBC studies. To better understand the effect of bulk resistivity, bulk lifetime, and the type of bulk material (p-Si or n-Si) each geometrical design is simulated for low, moderate, high resistivity and bulk lifetime parameters. Each parameter was simulated both for n-type and p-type base material. Moreover, each simulation was repeated for the cell structures with front floating emitter (FFE) and front surface field (FSF) to analyze the effect of front surface on the cell performance. Pitch value was set constant 2000 μm and the emitter fraction was varied between 30% and 90% to find the optimum emitter fraction. The summary of the varied parameters is given in Figure 3.1.

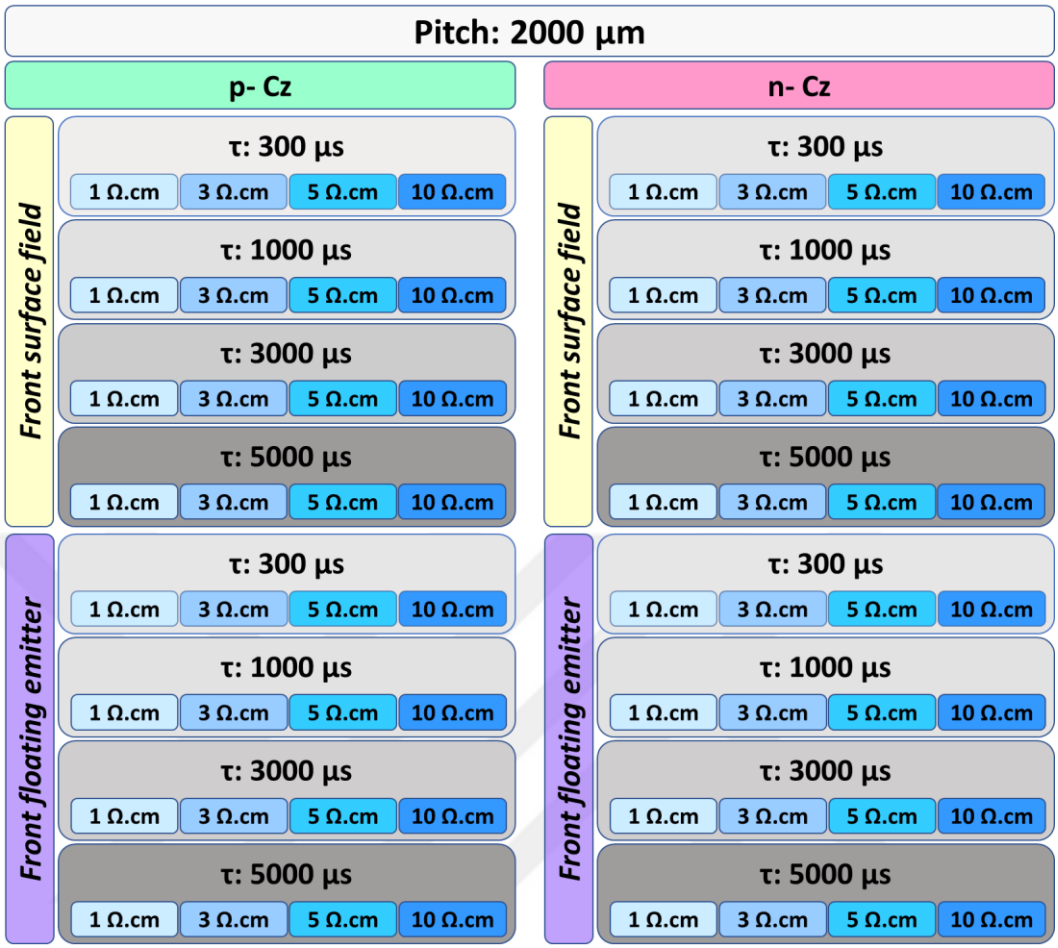


Figure 3.1. Varied parameters for the simulated IBC cells with constant pitch of 2000 µm.

For all simulations, metal fraction of emitter and BSF regions was kept constant at 70% to eliminate effect of resistive losses so that only the effect of varied parameters will dominate the cell performance. Wafer thickness was 180 µm whose effect will separately be examined after optimizing the cell geometry. Front side sheet resistance was set to 100 Ω/□ both for FFE and FSF cases, and only the doping type was changed from p to n or vice versa. Sheet resistance of the emitter and BSF regions were kept constant at 70 and 40 Ω/□, respectively. While the gap between emitter and BSF regions was assumed to be perfectly passivated, doped regions were assumed to have moderate passivation quality with corresponding J_0 values around 50 and 30 fA/cm^2, respectively.

Incident light spectrum was set to be AM 1.5G and hit the surface with an angle of 54.7° to mimic the real cell conditions with textured front surface. Contribution of the rear side was not taken into consideration since the metal fraction was 70% which was too high to contribute to the cell performance. Cross-sectional view of the simulated IBC cells with FFE is shown in Figure 3.2.

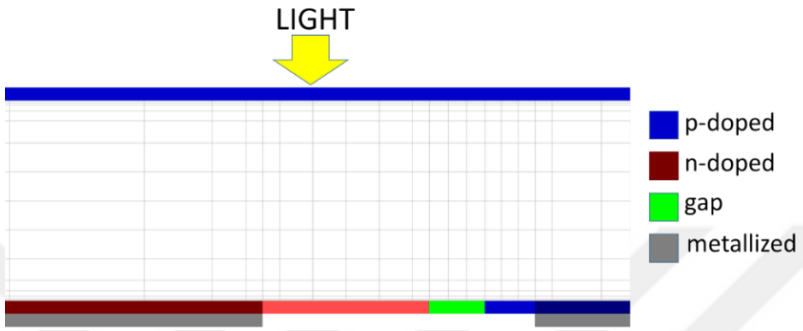


Figure 3.2. An exemplary cross-sectional view of simulated IBC cells with FFE.

3.2.2 Optimization of Unit Cell Properties

Based on the results of the first simulation part where the effect of bulk lifetime and bulk resistivity was figured out, a new simulation run was initiated to optimize the unit cell properties. Unlike the first set, sheet resistance of the doped layers (i.e., emitter & BSF) at the rear side and unit cell size were also varied. While the unit cell size was varied as 800, 1300 and 1800 µm, the gap between emitter and BSF was kept constant as 100 µm and the emitter fraction was varied from 30 to 80% for each unit cell. The respective sheet resistances of emitter and BSF regions were varied as 800, 100, 120, and 30, 50 Ω/□. Only n-Si was defined as the base material and the corresponding bulk lifetime was set as 5000 µs. Again, the bulk resistivity was kept as a variable between 1 and 10 Ω.cm, all simulations were run both for FFE and FSF structures. For this set, J_0 values of the doped regions were defined in accordance with the experimental results. That is $J_{0,\ emitter}$ was varied between 150-250 fA/cm^2 while $J_{0,\ BSF}$ was varied between 150-200 fA/cm^2. Moreover, the metal fraction was defined as 30% of the doped emitter and BSF

regions with a corresponding $J_{0,contact}$ value high enough to resemble fire-through contacts. All other inputs were varied as summarized in Table 3.2.

Table 3.2. Summary of varied simulation parameters.

Unit Cell [µm]	rho,bulk [Ω.cm]	Emitter Ratio [%]	Rsheet Emitter [Ω/□]	Rsheet BSF [Ω/□]	J0 front [fA/cm^2]	front side conductivity
800	1 6	30	80	30	90	n (FSF)
1300	2 7	40	100	50	50	p (FFE)
1800	3 8	50	120			
	4 9	60				
	5 10	70				
		80				

3.2.3 The Effect of the Varying Gap Properties and Wafer Thickness

Using the optimized parameters in the previous sections, wafer thickness, gap width and gap recombination were focused on in the last part of simulations. Sheet resistances of emitter ad BSF regions, bulk properties including base resistivity and bulk lifetime of the simulated cells were set constant. While the emitter sheet resistance was set to 120 Ω/□, that of BSF was set to 50 Ω/□. The base resistivity was set to 5 Ω.cm and the bulk lifetime was 5000 µs with the corresponding wafer thickness of 180 µm. Again, previously used unit cell sizes of 800, 1300 and 1800 µm were swept for varying gap fractions while the emitter fractions were kept the same as in the previous section. Simulations were carried out for FFE and FSF structures.

3.3 Results and Discussions

3.3.1 Determination of the Bulk Properties

Pitch: 2000 µm / FSF/ n-Si

First simulations were carried out for IBC cells with 2000 µm pitch. As shown in Figure 3.3, increasing emitter fraction increases the resulting cell efficiency for all bulk resistivity and bulk lifetime values.

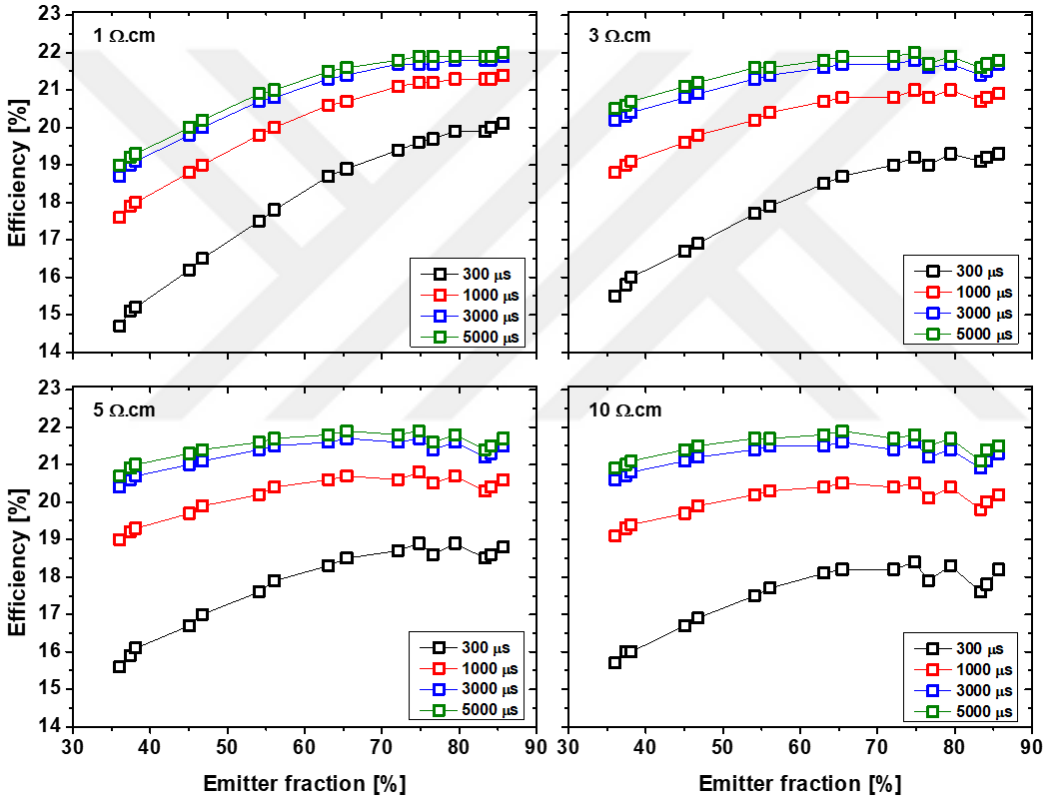


Figure 3.3. Effect of emitter fraction on cell efficiency of 2000 µm pitch, n-type cells with FSF.

Although the increasing emitter fraction enhances performance of cells with 300 µs bulk lifetime, they still have much lower efficiency compared to cells with higher bulk lifetime values. Comparing 3000 and 5000 µs cases for all resistivity values, one can deduce that the cell performance already reaches its maximum level by using the wafers with 3000 µs bulk lifetime. Further increase of the bulk lifetime

does not further improve the cell performance. Moreover, cell efficiencies saturate at the emitter fraction of 70% for 1 Ω.cm wafers while this value drops to 65% and 60% for 5 Ω.cm and 10 Ω.cm, respectively. Thus, cells with increasing bulk resistivity require relatively lower emitter fractions, thus wider BSF layers for similar cell performances as the cells with lower bulk resistivity values for the case of cell structure with FSF.

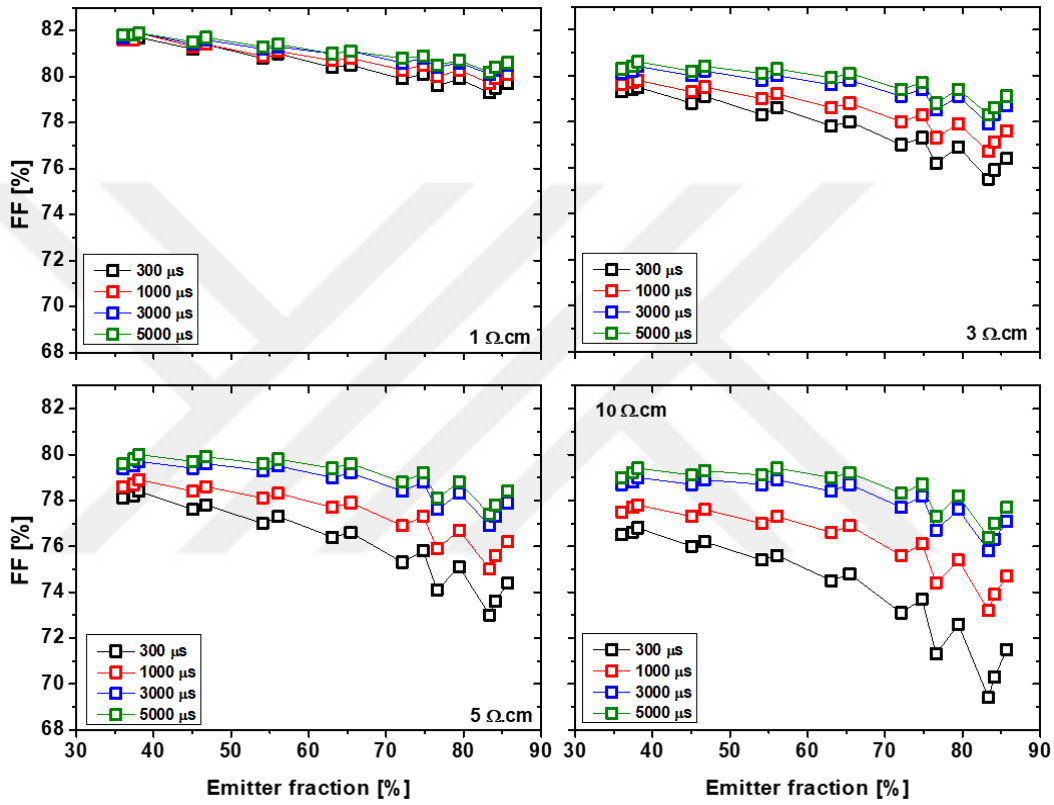


Figure 3.4. Effect of emitter fraction on fill factor (FF) of 2000 µm pitch, n-type cells with FSF.

As seen in Figure 3.4, increasing bulk resistivity reduces fill factor (FF) of the corresponding cells. Moreover, the effect of bulk lifetime on FF becomes more pronounced as the bulk resistivity increases. That is, for the case of 1 Ω.cm base material, all bulk lifetime values result in similar FF values while they show deviation as resistivity increases to 10 Ω.cm. Since FF is a function of open circuit voltage (V_{oc}) as formulated in *Eq*.3.12, it is expected to have lower FF values for

the cells with lower V_{oc} which explains observed decrease in FF for lower bulk lifetime values which was shown in Figure 3.4.

$$FF = \frac{V_{oc} - \ln(V_{oc} + 0.72)}{V_{oc} + 1} \qquad (Eq. 3.12)[54]$$

Considering the observed V_{oc} behavior in Figure 3.5, it could be said not only the V_{oc} but also the bulk resistivity affects FF of the cells.

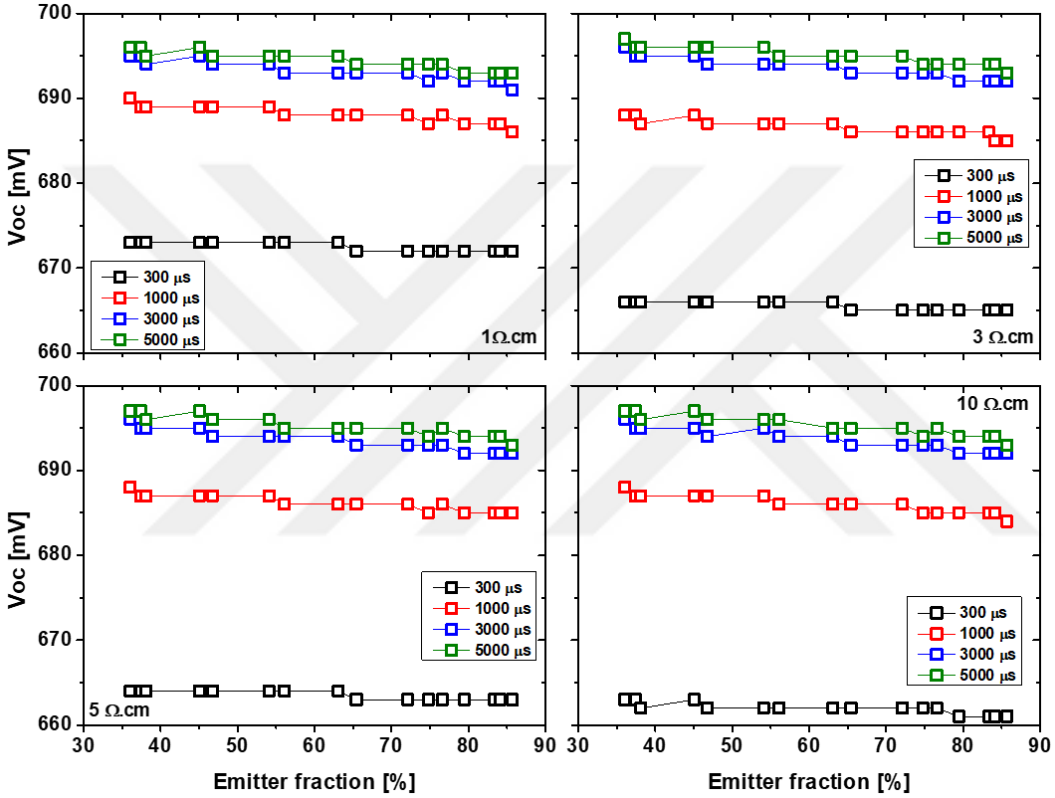


Figure 3.5. Effect of emitter fraction on open circuit voltage (V_{oc}) of 2000 µm pitch, n-type cells with FSF.

For the samples with bulk lifetime of 1000 µs with similar V_{oc} values (Figure 3.5), the observed slight decrease in FF could be related to increasing bulk resistivity. Since the series resistance (R_{series}) is contributed by bulk resistivity, and by contact resistivity, increasing bulk resistivity would increase R_{series} which would eventually reduce FF as observed in the simulations.

Short circuit current density (J_{sc}) was observed to increase as a function of increasing emitter fraction for all bulk resistivity values as shown in Figure 3.6.

Except the lowest bulk lifetime case (τ: 300 µs), J_{sc} values were observed to saturate at around 39-40 mA/cm^2. While this saturation occurs at an emitter fraction of 85% for 1 Ω.cm wafers, it reduces to 72% for 10 Ω.cm base material (Figure 3.6).

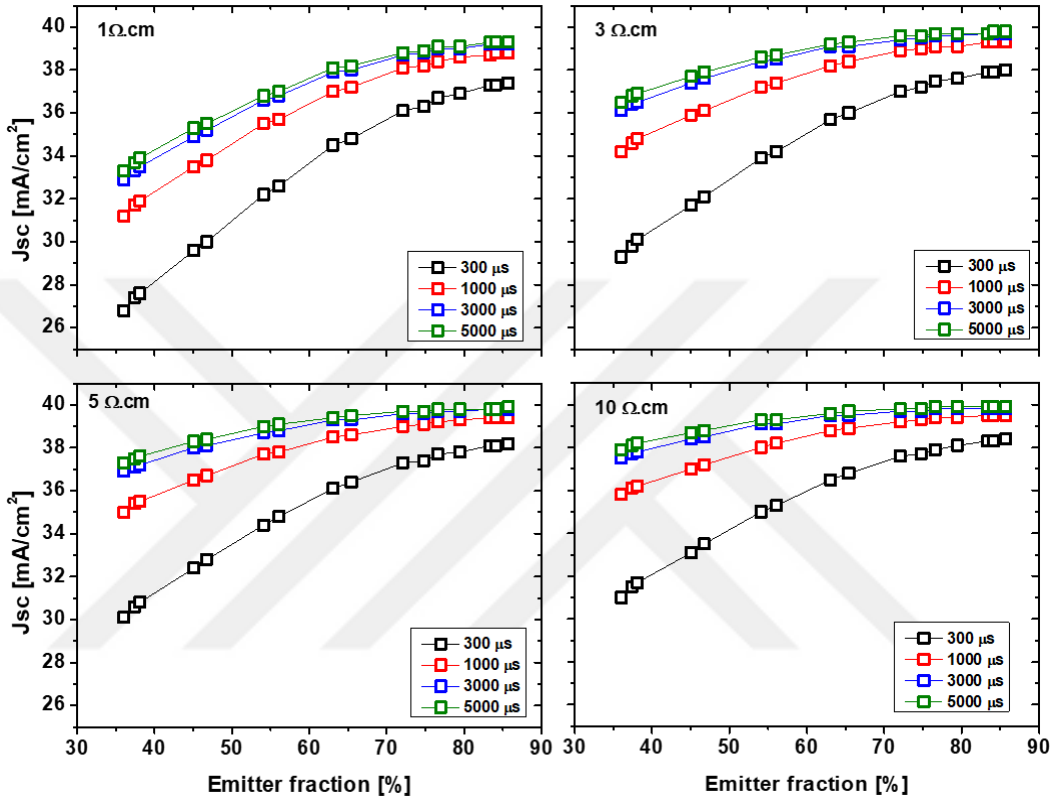


Figure 3.6. Effect of emitter fraction on short circuit current density (Jsc) of 2000 µm pitch, n-type cells with FSF.

Below these emitter fractions, J_{sc} is highly dependent on the bulk resistivity especially for low bulk lifetime value with τ: 300 µs. To better understand the reason of increasing J_{sc} with increasing bulk resistivity, additional simulations were carried out to observe hole carrier density for cells with emitter: 800 µm/ gap: 100 µm/ BSF: 1100 µm with the cross-section shown in Figure 3.7. The carrier density was checked for the cells with varying bulk resistivities from 1 to 10 Ω.cm and with FSF at the front side for the limiting bulk lifetimes of 300 and 5000 µs.

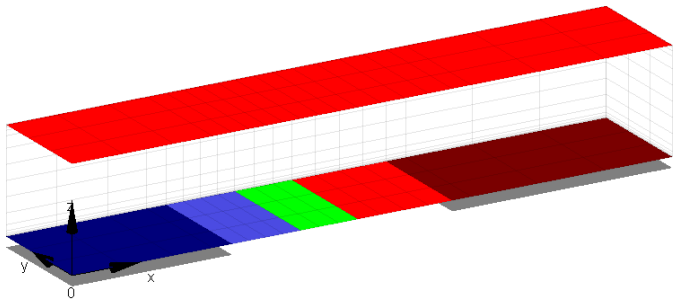


Figure 3.7. Cross-sectional view of the FSF cell with emitter: 800 µm/ gap: 100 µm/ BSF: 1100 µm. Blue region indicates p+ doping, red indicates n+ doping and green region indicates un-doped passivated gap.

In Figure 3.8, it was observed that the holes generated above BSF region had to travel laterally towards the emitter side.

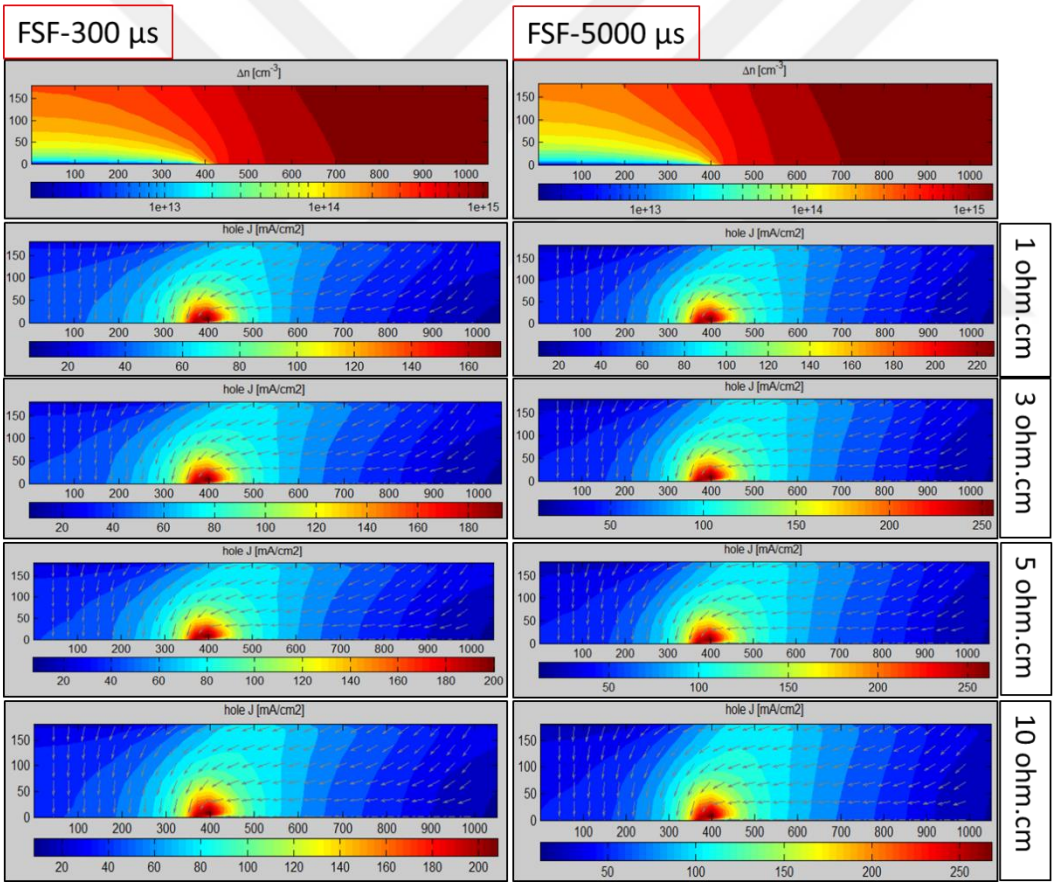


Figure 3.8. Simulated hole carrier density for FSF cell with various bulk resistivity values. The y-axis measures the distance from the rear surface into the wafer in microns where x-axis measures the distance from the center of the emitter to the center of the BSF.

While generated electrons are attracted towards the non-contacted front surface field, generated holes are repelled and are promoted to move laterally from BSF towards the emitter region. The cell with the bulk lifetime of 300 µs had the lowest hole density at around 400 µm where the boundary of the emitter region was staying. Increasing bulk resistivity form 1 Ω.cm to 10 Ω.cm slightly increased carrier density at the edge of the emitter, but the remaining emitter area had a low carrier density. Increasing bulk lifetime from 300 µs to 5000 µs, improves carrier density which explains observed higher J_{sc} values in Figure 3.6.

Pitch: 2000 µm / FFE/ n-Si

Repeating the same procedure for the cells with the same geometries but with the p^+ doped front floating emitter at the front surface instead of n^+ doped front surface field has shown improved cell performance. The resulting cell efficiencies are shown in Figure 3.9.

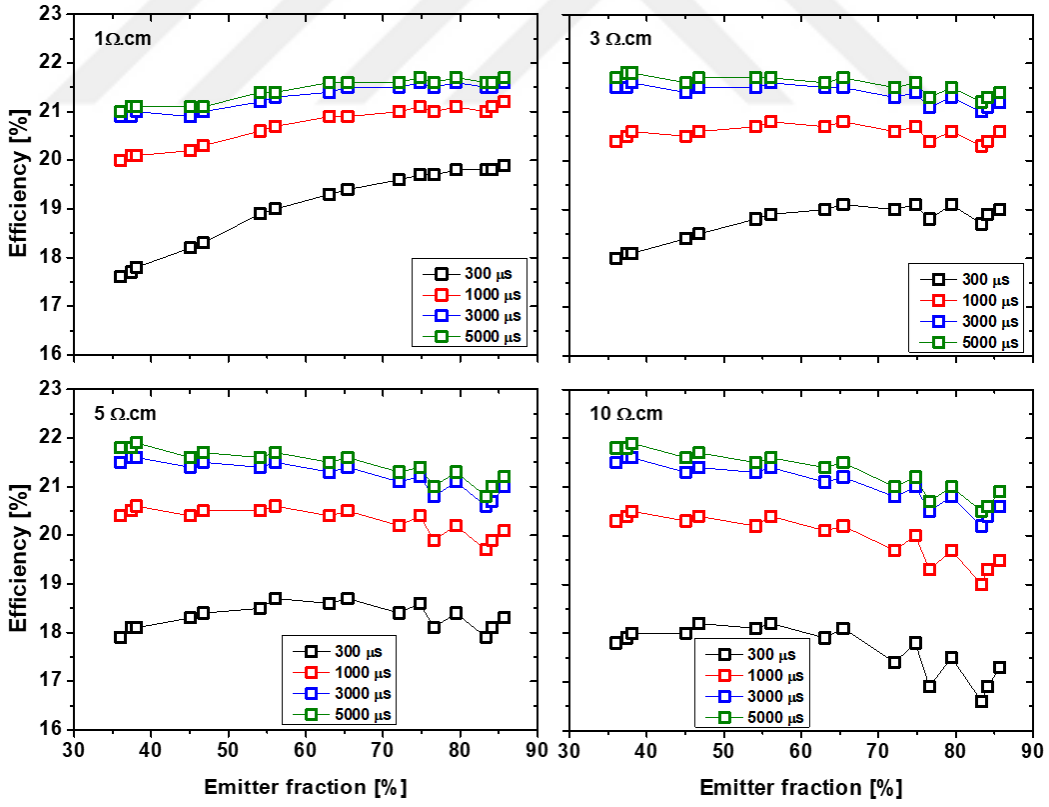


Figure 3.9. Effect of emitter fraction on cell efficiency of 2000 µm pitch, n-type cells with FFE.

Replacing FSF with FFE resulted in significantly better cell efficiencies even at lower emitter fractions. Unlike FSF, the existence of FFE makes cell efficiency to be less dependent on the bulk resistivity. The lowest emitter fraction for the lowest bulk lifetime (300 µs) resulted in efficiency of 17.8% while it was 15.2% for the cells with FSF. Moreover, the emitter fractions around 50% result in close efficiency values to those obtained with higher emitter fractions. Thus, for the case of FFE, wider BSF regions are allowed without significant performance loss which would provide more tolerance during metallization and module interconnection steps [18], [26].

Considering the fill factors, the cells with the 1 Ω.cm base material have similar FF values for all emitter fractions regardless of the bulk lifetime (see Figure 3.10).

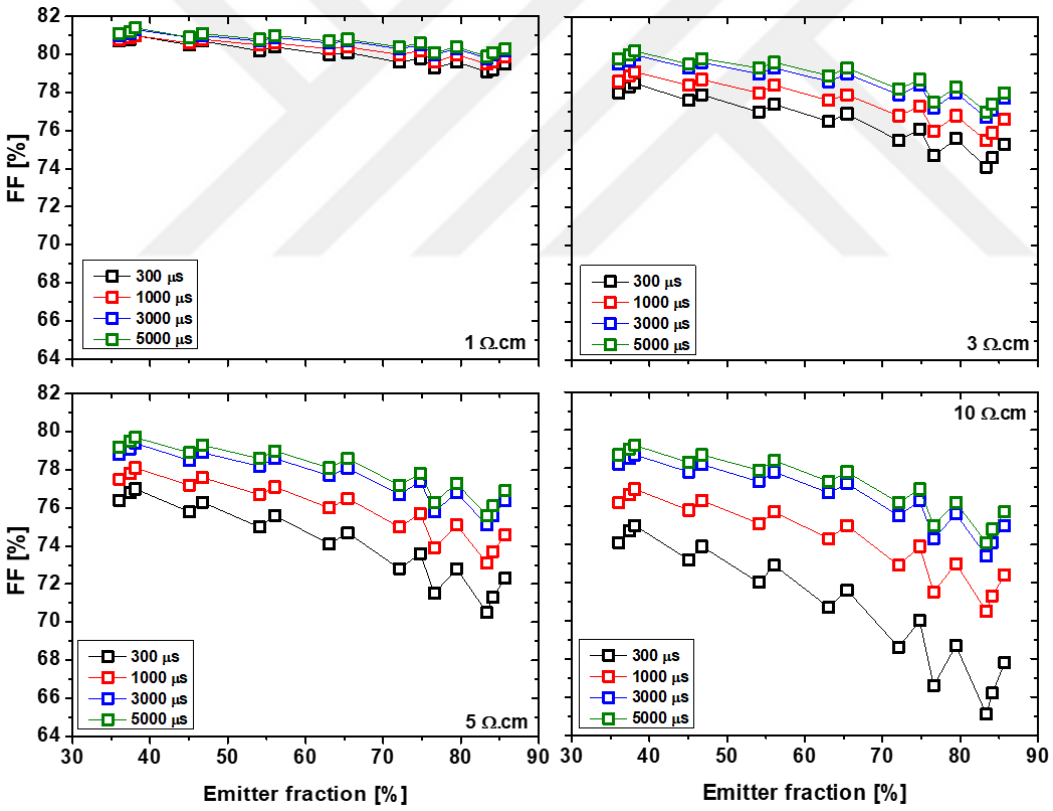


Figure 3.10. Effect of emitter fraction on fill factor (FF) of 2000 µm pitch, n-type cells with FFE.

As the resistivity of the base material increases, both emitter fraction and bulk lifetime effect becomes more pronounced.

For the case of open circuit voltages, a stabilization was observed for all resistivity values and bulk lifetimes above 1000 µs as seen in Figure 3.11.

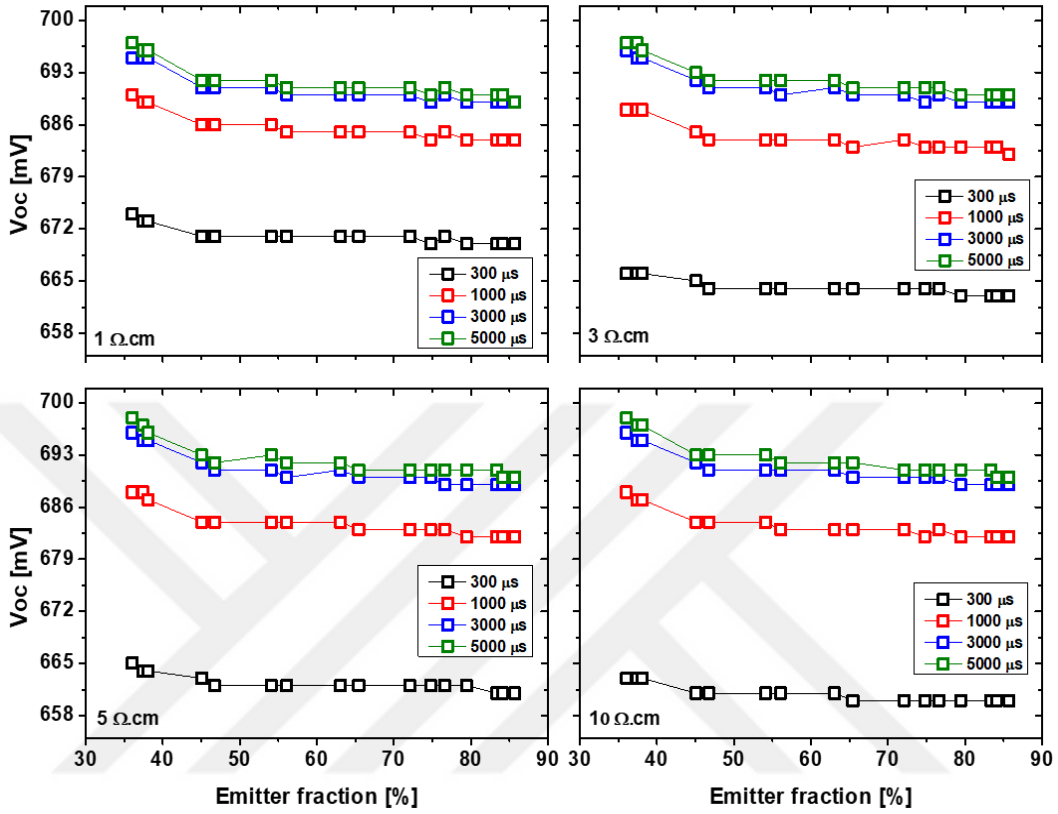


Figure 3.11. Effect of emitter fraction on open circuit voltage (V_{oc}) of 2000 µm pitch, n-type cells with FFE.

For 1000 µs, V_{oc} was lying in 682-685 mV range, which was 689-691 mV for 3000 µs and 691-694 mV for 5000 µs bulk lifetimes. For the case of the lowest bulk lifetime: 300 µs, all V_{oc} values stays constant in 661-663 mV range around for the samples with 3, 5 and 10 Ω.cm bulk resistivities. Only for the sample of 1 Ω.cm bulk resistivity, stabilization occurs at around 670 mV which could be related the higher built-in potential generated by higher doping concentration of the base material.

Considering the short circuit current densities shown in Figure 3.12, cells with different bulk resistivity values show stabilized J_{sc} values at different emitter fractions. While 1 Ω.cm wafers shows this stabilization above the emitter fraction of 85%, this value is 75, 70 and 65% for 3, 5 and 10 Ω.cm wafers respectively.

Cells with bulk lifetimes of 1000, 3000 and 5000 µs show similar performances for all bulk resistivities except the cells with the lowest bulk lifetimes. For all bulk properties, increasing emitter fraction enhances J_{sc}.

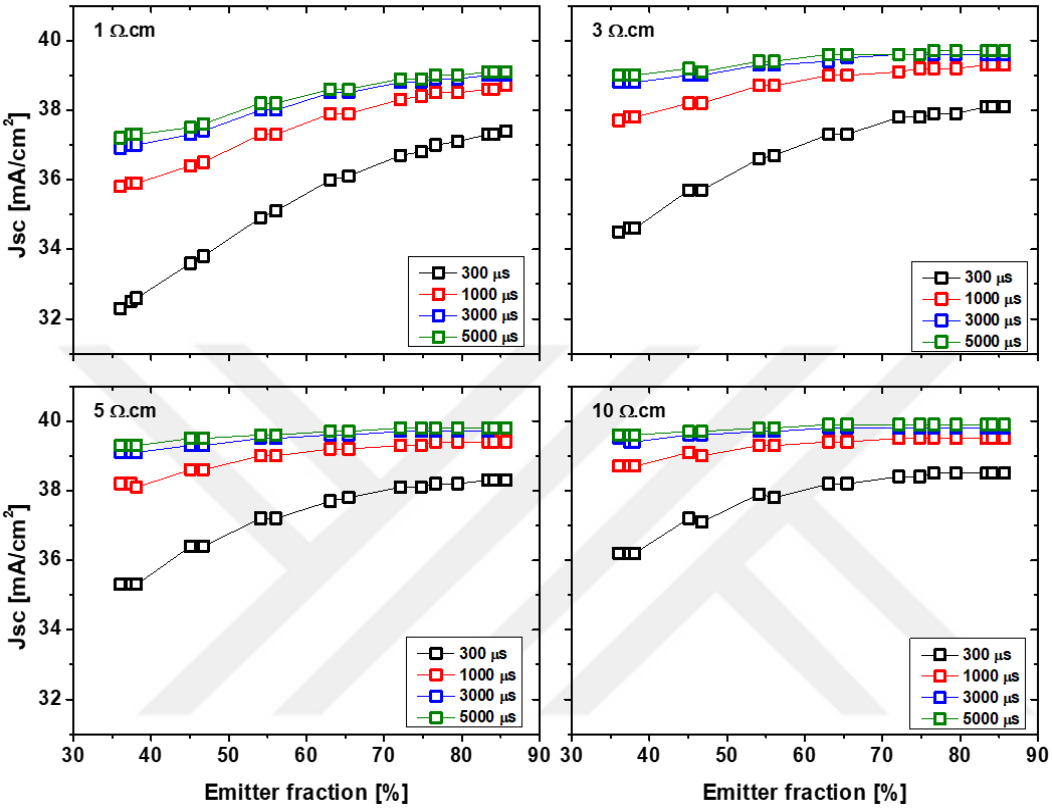


Figure 3.12. Effect of emitter fraction on short circuit current density (J_{sc}) of 2000 µm pitch, n-type cells with FFE.

To better analyze the effect of FFE on the cell performance, additional simulations for the cell structure with emitter: 800 µm/ gap: 100 µm/ BSF: 1100 µm were carried out as done for FSF case. Cross-sectional view of the simulated cell structure is shown in Figure 3.13.

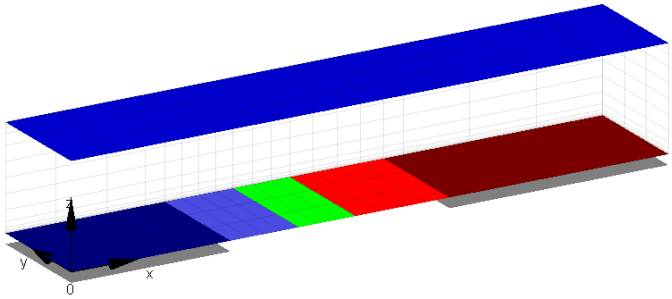


Figure 3.13. Cross-sectional view of the FFE cell with emitter: 800 µm/ gap: 100 µm/ BSF: 1100 µm. Blue region indicates p+ doping, red indicates n+ doping and green region indicates un-doped passivated gap.

The carrier density was checked for the cells of 1 and 10 Ω.cm bulk resistivity and with FFE at the front side for the bulk lifetimes of 300 and 5000 µs and given in Figure 3.14.

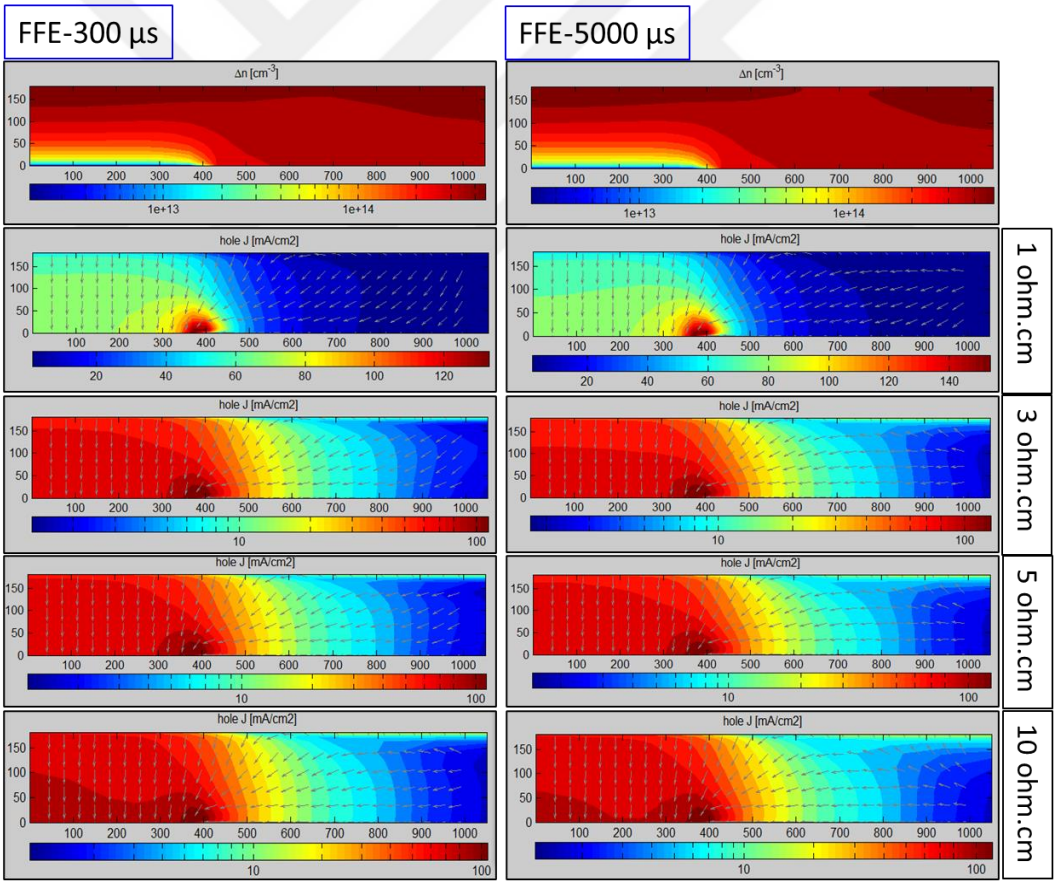


Figure 3.14. Simulated hole carrier density for FFE cell with various bulk resistivity values. The y-axis measures the distance from the rear surface into the wafer in microns where x-axis measures the distance from the center of the emitter to the center of the BSF.

As seen in Figure 3.14, hole density has significantly been increased above the hole-collecting emitter region. Unlike the lateral transport through the base in FSF case (electrical shading), holes only need to make a vertical travel with the path length equal to wafer thickness. Carriers generated above BSF region are first injected to the conductive FFE region where they can travel till emitter region. When the carriers are above emitter, they will be re-injected into the base and collected at the rear emitter contact which is so called "*PUMPING EFFECT*" [18]. Thus, at the end of the first set of simulations, it was concluded that increasing emitter fraction improves cell performance both for FSF and FFE cells. While the performance of FSF cells is more dependent on emitter fraction, FFE cells were observed to tolerate wider BSF regions with negligible losses in the cell performance.

Pitch: 2000 µm / FSF/ p-Si

After understanding the effect of front surface on the cell performance, the same simulations were carried out for the same cell geometries but with p-type base material. Corresponding efficiency values are shown in Figure 3.15. Comparing the performance of n-Si and p-Si based FSF cells, it was observed that both n and p-type cells perform similarly for all bulk resistivities. Increasing emitter fraction enhances the performance FSF cells with a similar stabilization behavior at high emitter fractions as in the case of FSF cells with n-type base material.

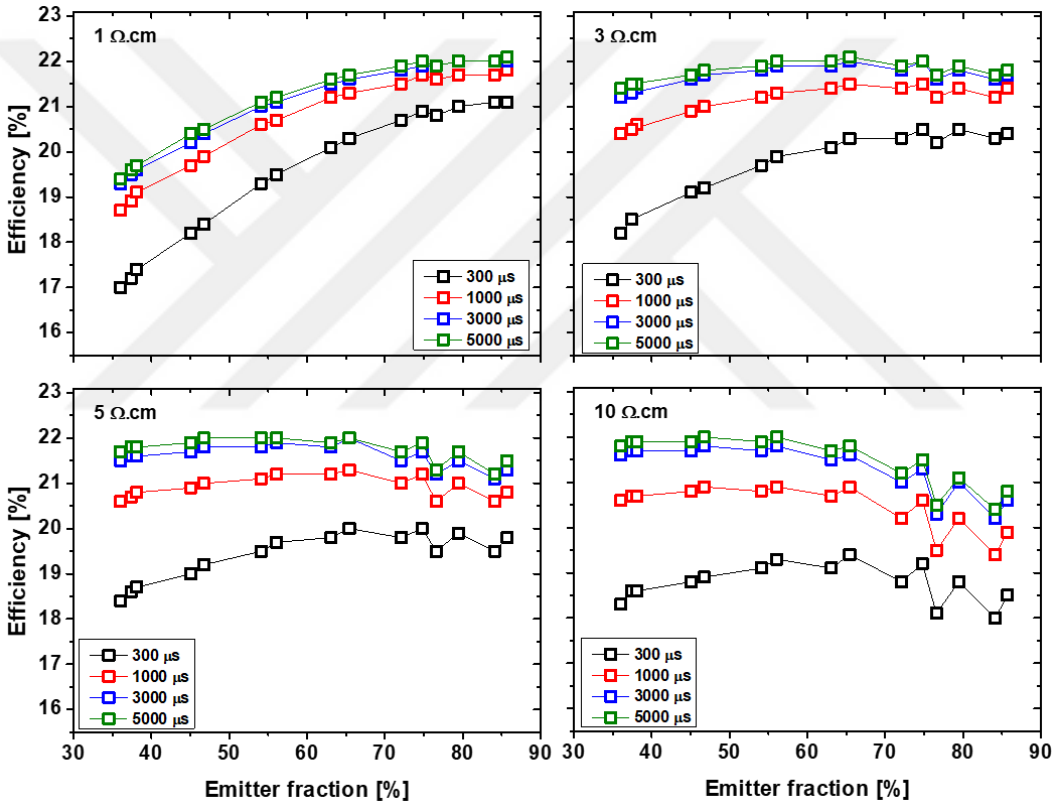


Figure 3.15. Effect of emitter fraction on cell efficiency of 2000 µm pitch, p-type cells with FSF.

Although efficiency plots of n-based and p-based FSF cells coincides for bulk lifetime values of 1000, 3000 and 5000 µs, efficiency of p-based FSF cells are better for 300 µs lifetime case. Regardless of base material, 22 % efficiency was observed to be the highest reachable efficiency for FSF cells of 2000 µm pitch with the given bulk properties.

As seen in Figure 3.16, highest fill factors were obtained for the highest bulk conductivity.

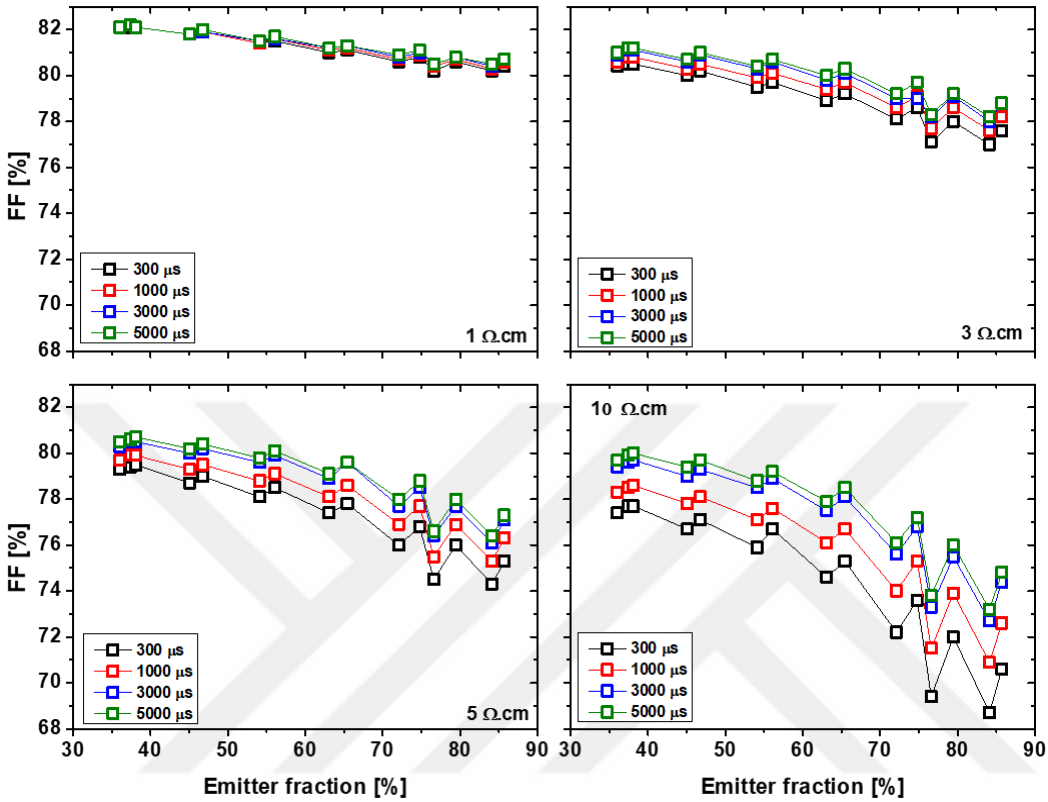


Figure 3.16. Effect of emitter fraction on fill factor (FF) of 2000 µm pitch, p-type cells with FSF.

FF of 1 Ω.cm and 3 Ω.cm wafers changes in a similar manner where increasing bulk lifetime has a negligible effect. Although increasing emitter fraction from 35 to 86% slowly reduces FF for the cells on p-Si wafers, lower limit of FF was obtained as 80% and 77% for 1 and 3 Ω.cm respectively. Increasing bulk resistivity pronounces both the effect of bulk lifetime and emitter fraction on FF of the corresponding FSF cells. The lowest FF values were obtained for emitter fractions greater than 60% on 10 Ω.cm wafers.

Open circuit voltages of p-based cells showed a similar behavior as their n-based counterparts, that is V_{oc} was almost independent on emitter fraction. It should be noted here that the adverse effect of boron-oxygen complexes during high temperature processes was not taken into consideration during simulations. As

shown in Figure 3.17, for all bulk resistivity values, similar V_{oc} values were obtained for high bulk lifetime condition (i.e., 3000 and 5000 µs).

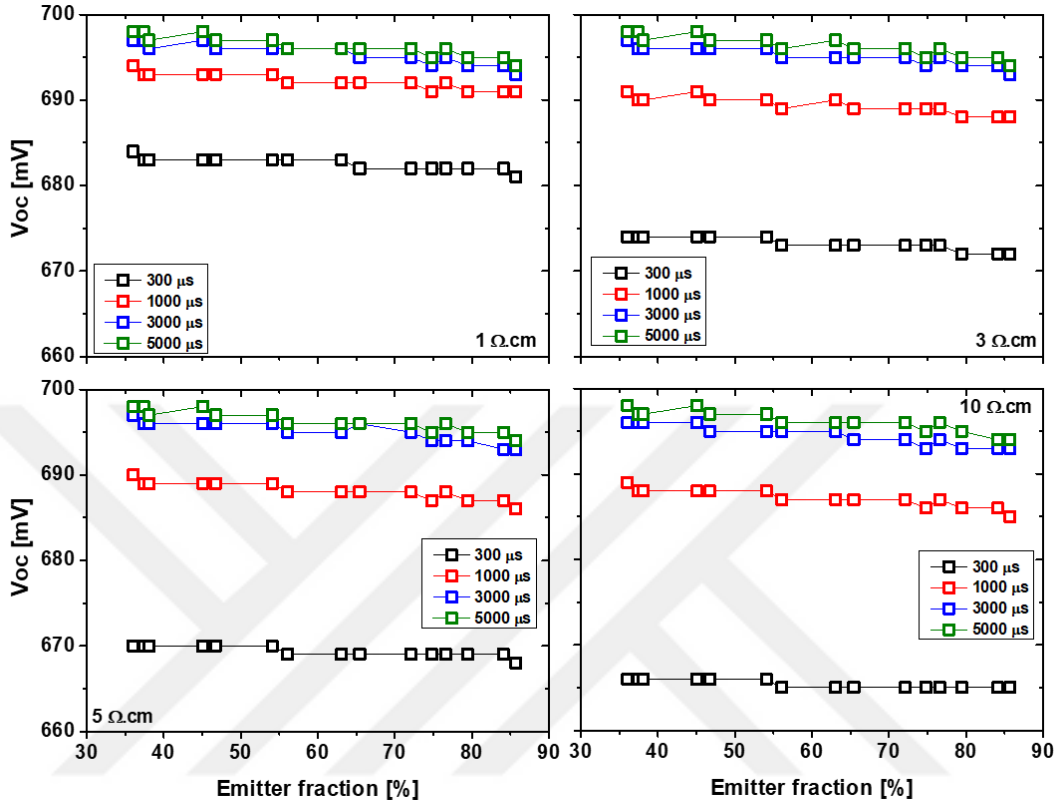


Figure 3.17. Effect of emitter fraction on open circuit voltage (V_{oc}) of 2000 µm pitch, p-type cells with FSF.

Increasing bulk resistivity reduces V_{oc} values of cells with bulk lifetimes of 1000 and 300 µs. The drop in V_{oc} for 1000 µs was around 4 mV while going from 1 Ω.cm to 10 Ω.cm whereas it was almost 20 mV for 300 µs case. Thus, lower bulk lifetime pronounces the negative effect of increasing bulk resistivity on FF of p based FSF cells. Compared to their n-based counterparts, p-based FSF cells shows slightly higher V_{oc} values for bulk lifetime ≥ 1000 µs while that difference between V_{oc} values becomes 10-14 mV for 300 µs case. Thus, it could be deduced that for low quality base materials, it would be beneficial to fabricate p-based FSF cells instead of n-based.

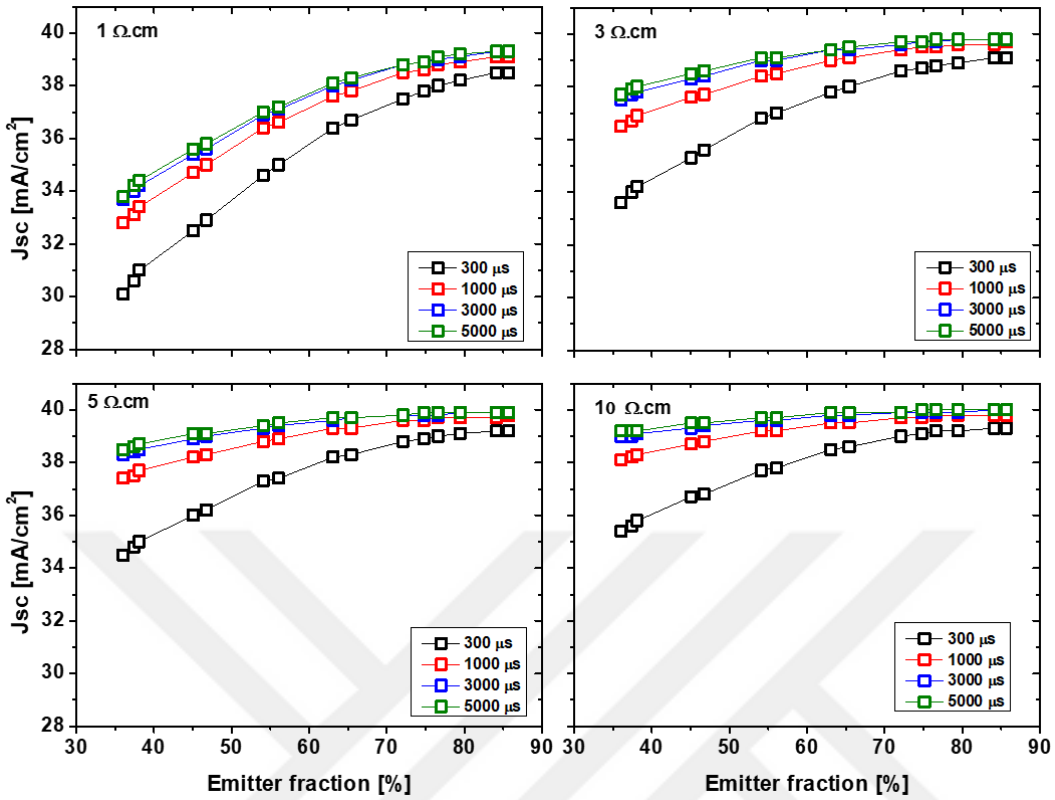


Figure 3.18. Effect of emitter fraction on short circuit current density (J_{sc}) of 2000 µm pitch, p-type cells with FSF.

Short circuit current density shown in Figure 3.18 showed a similar behavior as in the case of n based FSF cells. While 1 Ω.cm wafers had a saturated J_{sc} at around 39 mA/cm^2 above emitter fraction of 85 %, the same level was reached at emitter fractions of 70 %, 65 % and 60 % for 3, 5 and 10 Ω.cm wafer respectively. Moreover, the lowest J_{sc} values obtained for 300 µs lifetime were 30.1, 33.6, 34.5 and 35.4 mA/cm^2 for samples on 1, 3, 5 and 10 Ω.cm p-wafers whereas those values were 26.8, 29.8, 30.6 and 31.5 mA/cm^2 respectively for FSF cells on n-wafers.

Pitch: 2000 µm / FFE/ p-Si

For the case p-based FFE cells, efficiency showed similar behavior as n-based FFE cells. As seen in Figure 3.19, increasing emitter fraction improves cell efficiency for all bulk lifetime values of 1 Ω.cm, p based FFE cells. Not only for 1 Ω.cm but

also for 3 Ω.cm base materials, moderate and high bulk lifetime values (1000, 3000 and 5000 µs) result in similar cell performances.

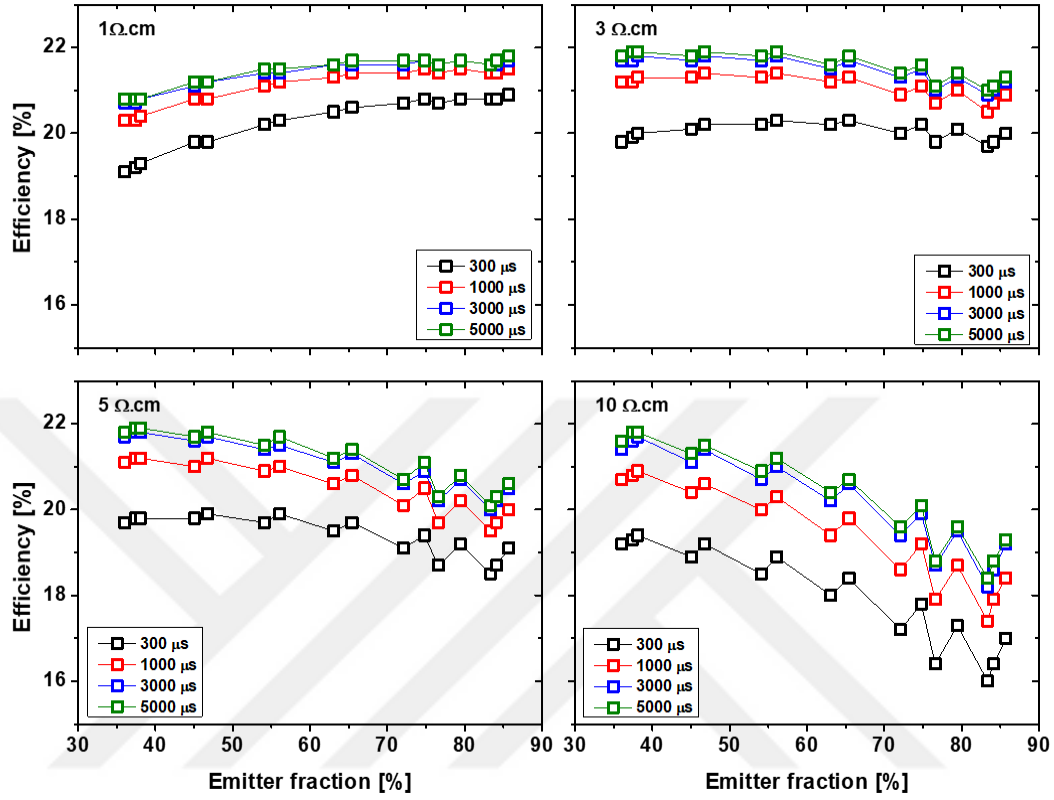


Figure 3.19. Effect of emitter fraction on cell efficiency of 2000 µm pitch, p-type cells with FFE.

FFE cells on low bulk lifetime (300 µs), p-Si have relatively lower efficiencies. While increasing emitter fraction improves the cell performance on 1 Ω.cm, p-based cells, efficiency of cells on 3 Ω.cm wafers is not significantly affected by increasing emitter width. Contrary to low bulk resistivity base materials, increasing emitter fraction has little or no effect on 5 Ω.cm while it reduces efficiency of the cells on 10 Ω.cm, p-Si.

Increasing emitter fraction reduces FF of the p based FFE cells which is more pronounced for higher bulk resistivity values as shown in Figure 3.20. The lowest FF was observed for 10 Ω.cm base with the emitter fraction of 83%.

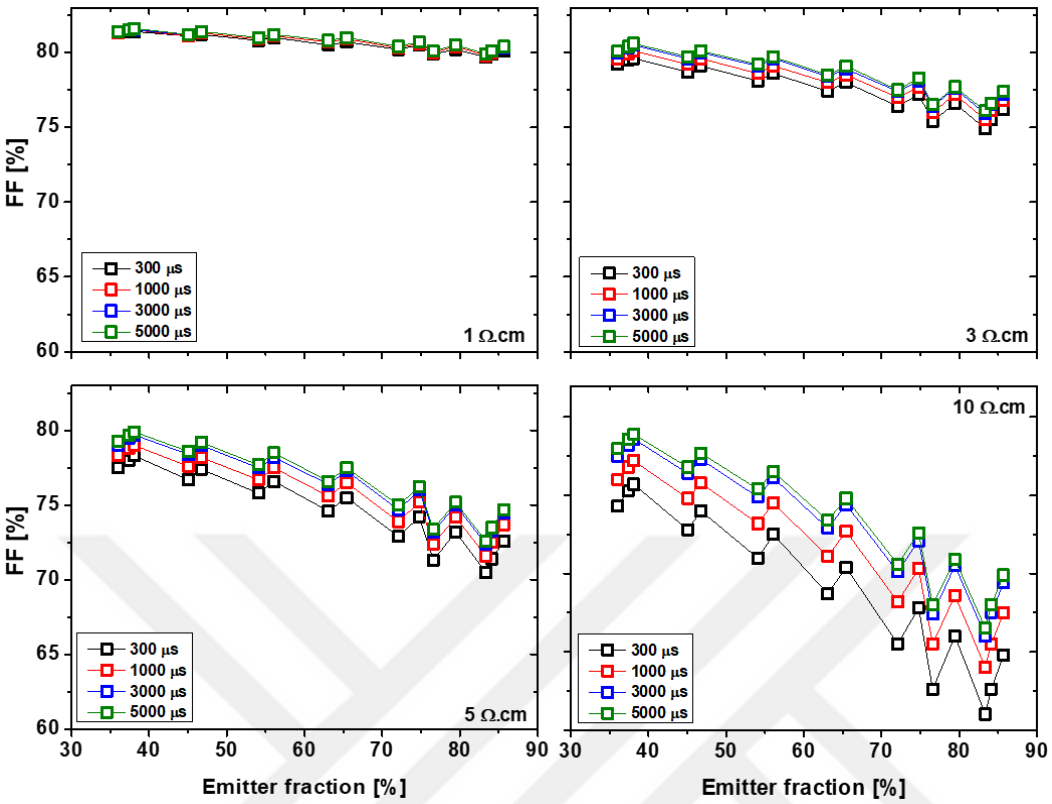


Figure 3.20. Effect of emitter fraction on fill factor (FF) of 2000 µm pitch, p-type cells with FFE.

It could be deduced that increasing emitter fraction which narrows BSF width, reduces the collection of carriers at the BSF contact since it becomes harder for the carriers to travel through the bulk wafer acting as a more resistive medium.

While FF reduced as an inverse function of emitter fraction, V_{oc} values stayed constant for medium and high bulk lifetime values. Regardless of the bulk resistivity, almost the same V_{oc} values were obtained for all emitter fractions except the lowest bulk lifetime as shown in Figure 3.21.

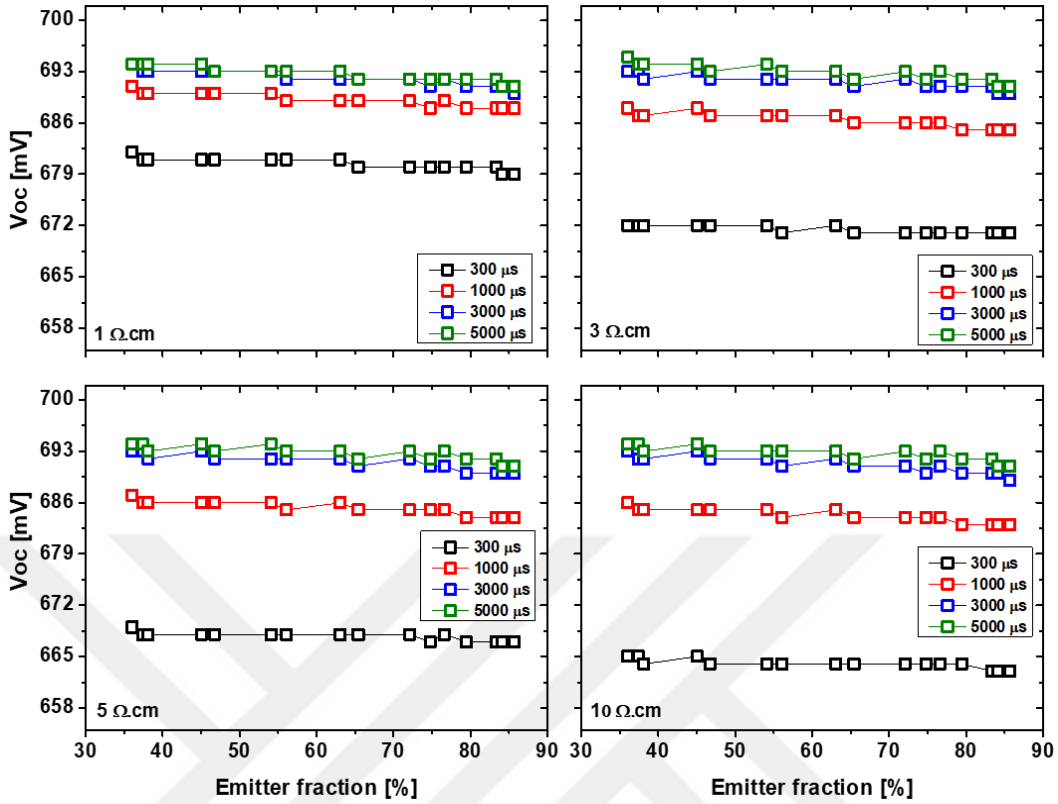


Figure 3.21. Effect of emitter fraction on open circuit voltage (V_{oc}) of 2000 µm pitch, p-type cells with FFE.

As shown in Figure 3.22, J_{sc} increases as a weak function of increasing emitter fraction as in the case n base FFE cells. Compared to p based FSF cells, the performance of FFE cells were observed to be less dependent on the cell geometry. This could be related to the suppressed electrical shading with the help of pumping effect of the FFE.

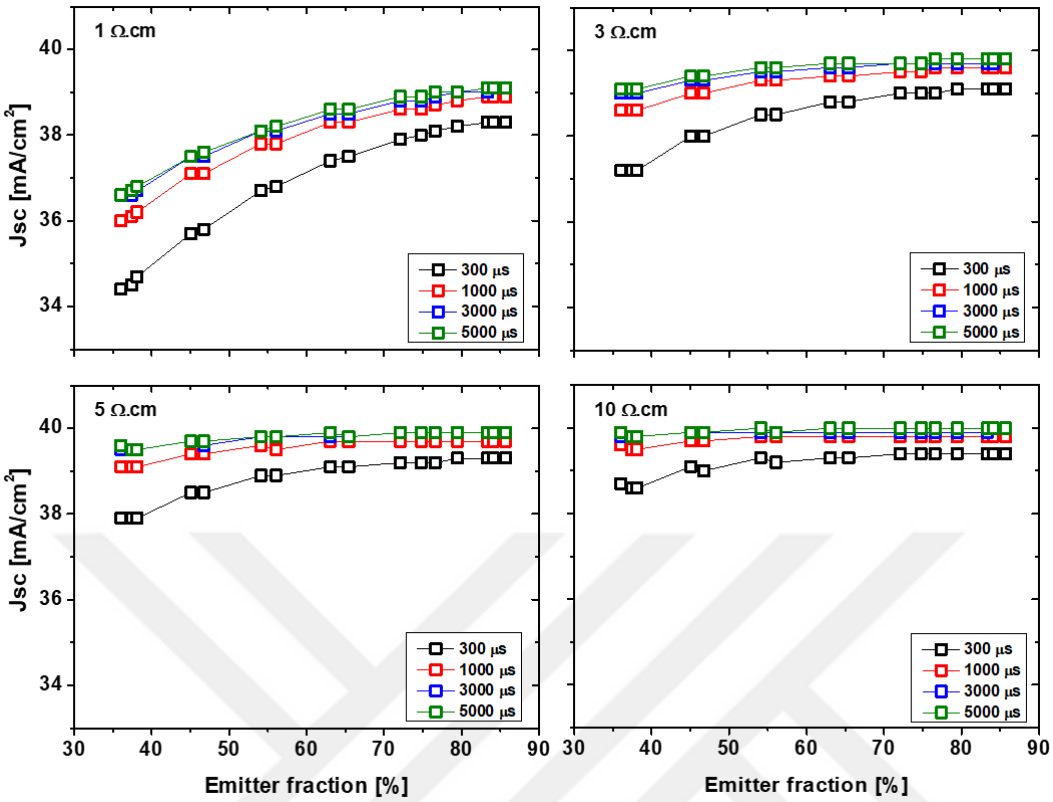


Figure 3.22. Effect of emitter fraction on short circuit current density (J_{sc}) of 2000 µm pitch, p-type cells with FFE.

At the end of this set of simulations, it was observed that FFE cells were less geometry dependent allowing wider BSF regions and pose higher efficiency values compared to FSF cells. Increasing emitter fraction could help to improve the device performance till a certain point above which FF losses start to degrade the cell performance. Moreover, the effect of front side doping polarity (i.e., FFE or FSF) on current transport was visualized.

3.3.2 Optimization of Unit Cell Properties

i. IBC Cells with FSF

In the second part of the simulation study, the effect of varying sheet resistance values for the emitter and BSF regions was analyzed both for FFE and FSF

structures. As an example, emitter fraction was fixed at 70% and the corresponding efficiency plots for the smallest unit cell (800 µm) of FSF-IBC cells are shown in Figure 3.23. As seen in Figure 3.23, increasing emitter and BSF sheet resistance improves the cell performance for all bulk resistivity values.

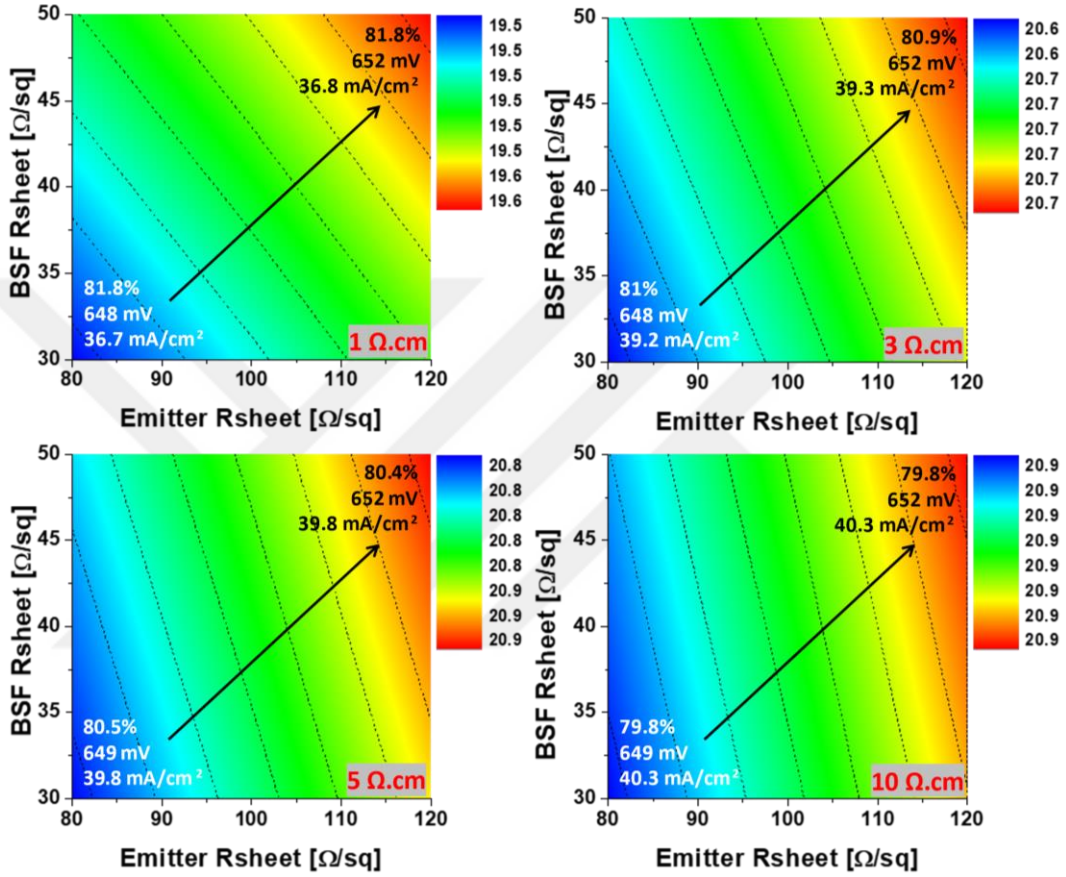


Figure 3.23. Distribution of efficiency as a function of emitter and BSF regions' sheet resistance for different bulk resistivity values for the cells with FSF. The unit cell size was 800 µm and the chosen emitter fraction was 70% of the unit cell. Minimum and maximum values for FF, Voc, and Jsc are shown at the corners of the plots. Color codes are showing the efficiency of the cells.

Increasing the bulk resistivity from 1 to 10 Ω.cm increased the best efficiency from 19.6 to 20.9%. This could be related to improving current density as a function of reducing base doping. The highest J_{sc} for the bulk lowest bulk resistivity (1 Ω.cm) was 36.8 mA/cm^2 which increased to 40.3 mA/cm^2 for the case of the highest bulk resistivity (10 Ω.cm). Making the same analysis for a wider unit cell (1300 µm)

resulted in slightly lower cell efficiencies as shown in Figure 3.24. The observed effect of emitter and BSF regions' sheet resistance was the same as in the case of smaller unit cell, that is the highest efficiency was obtained for the highest sheet resistance values. Increasing resistivity from 1 to 10 Ω.cm increased the J_{sc} from 35.6 to 40.0 mA/cm^2 which was accompanied by improved efficiency from 18.9 to 20.6%.

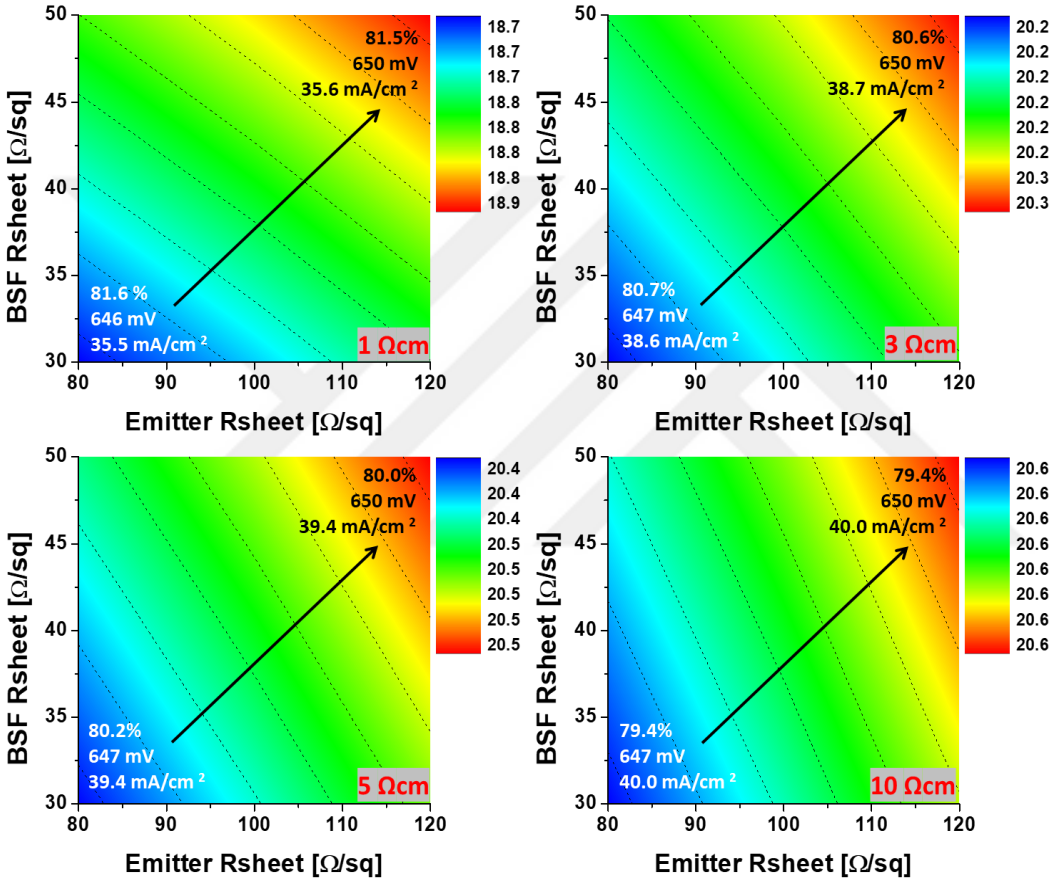


Figure 3.24. Distribution of efficiency as a function of emitter and BSF regions' sheet resistance for different bulk resistivity values for cells with FSF. The unit cell size was 1300 µm and the chosen emitter fraction was 70% of the unit cell. Minimum and maximum values for FF, Voc, and Jsc are shown at the corners of the plots. Color codes are showing the efficiency of the cells.

As the largest unit cell size, 1800 µm was analyzed for varying sheet resistance values. Like 800 and 1300 µm cases, increasing sheet resistance of the doped regions was observed to enhance the resulting cell efficiency as shown in Figure

3.25. The best efficiency increased from 18.2 to 20.3% as the bulk resistivity increased from 1 to 10 Ω.cm while the respective J_{sc} values increased from 34.6 to 39.6 mA/cm^2. The resulting FF values reduced from 81.2% to 78.7%. As a result, it was deduced that the smallest unit cell had the highest performance compared to larger unit cells.

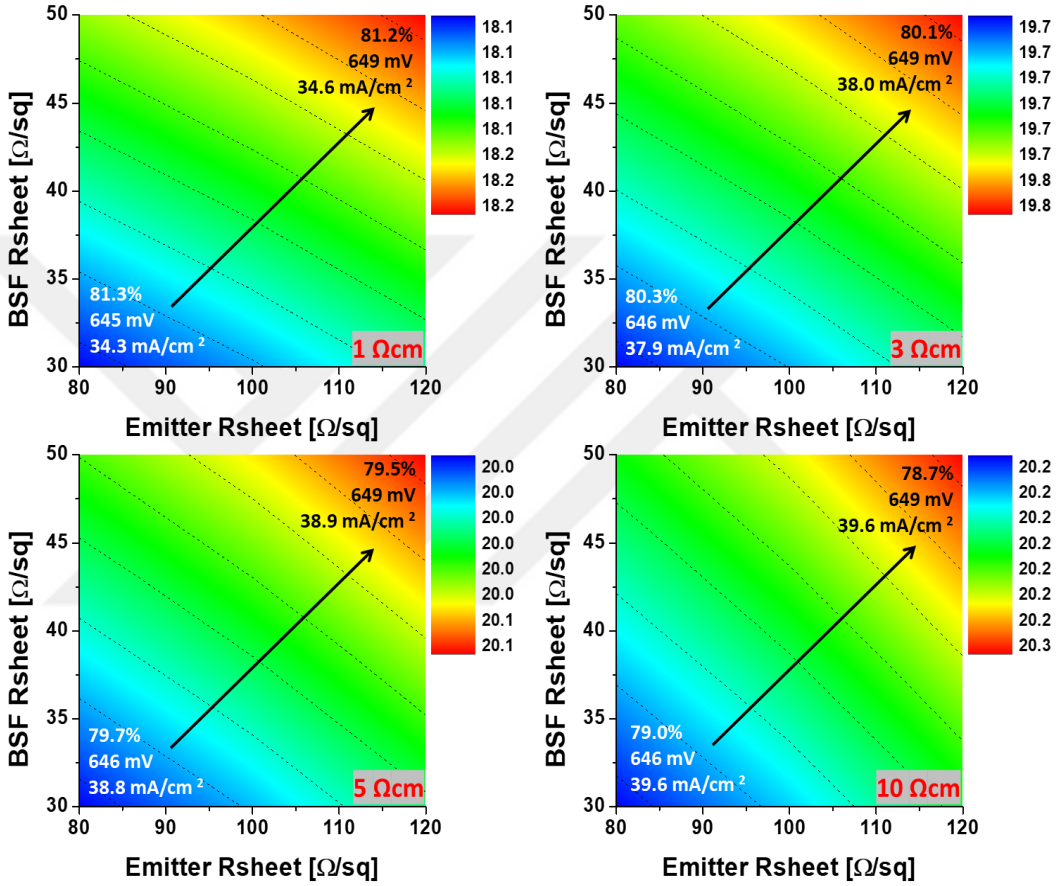


Figure 3.25. Distribution of efficiency as a function of emitter and BSF regions' sheet resistance for different bulk resistivity values for cells with FSF. The unit cell size was 1800 µm and the chosen emitter fraction was 70% of the unit cell. Minimum and maximum values for FF, Voc, and Jsc are shown at the corners of the plots. Color codes are showing the efficiency of the cells.

Moreover, increasing bulk resistivity improved J_{sc}, thus efficiency of the cells for all unit cell sizes. To further understand the effect of bulk resistivity and emitter fraction and compare for different unit cell sizes, simulation results for the fixed

emitter R_{sheet} of 120 and BSF R_{sheet} of 50 Ω/□ were analyzed and shown in Figure 3.26.

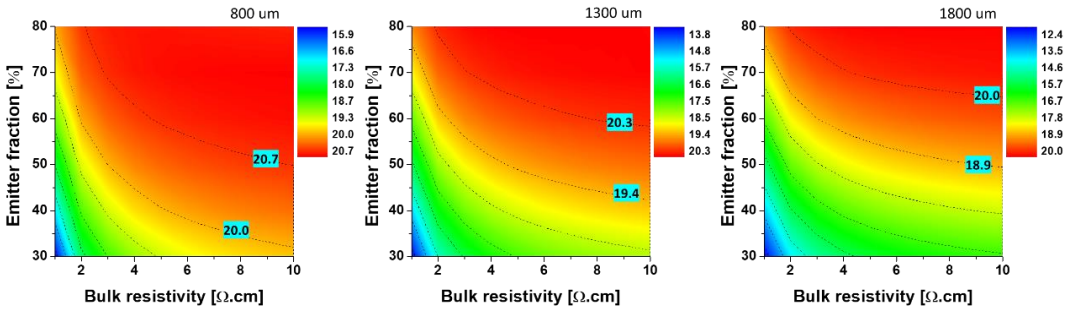


Figure 3.26. Effect of bulk resistivity on efficiency of IBC cells with FSF for varying unit cell sizes. Emitter and BSF regions' Rsheet values were chosen as 120 and 50 Ω/□, respectively.

As seen in Figure 3.26, for a certain emitter fraction, a different bulk resistivity is required to end up with the desired conversion efficiency. That is, to reach 20.0% efficiency for the smallest unit cell; if 8 Ω.cm base is used, approximately 35% emitter fraction will be required while emitter fraction is needed to be 50% for the case of 3 Ω.cm base material. Increasing unit cell size from 800 to 1800 µm increases the required emitter fraction for the same efficiency value. Unlike 800 µm, for 1800 µm unit cell size, the maximum efficiency was 20.0%. For 8 Ω.cm base material approximately 65% emitter fraction is needed which further increases to 74% when bulk resistivity reduces to 3 Ω.cm. Thus, for typical bulk resistivity values, the corresponding cell performance would be limited since the practical emitter fraction has also an upper limit.

As the next task, a certain emitter fraction (70%) and respective emitter and BSF sheet resistance values of 120 and 50 Ω/□ was focused on to analyze the effect of bulk resistivity on cell performance. The effect of varying rho,bulk on efficiency and fill factor is shown in Figure 3.27.

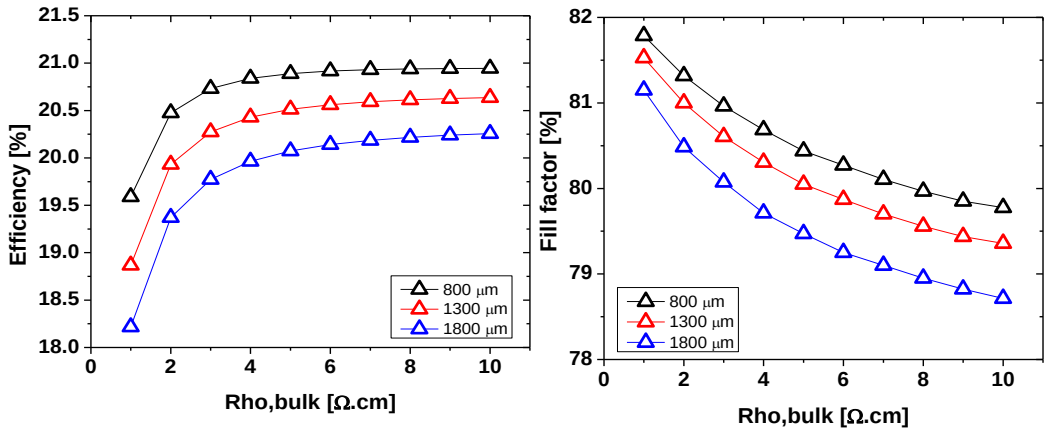


Figure 3.27. Effect of varying bulk resistivity on cell efficiency (left) and fill factor (right) for varying unit cell sizes of 800, 1300 and 1800 µm with a constant emitter Rsheet of 120 and BSF Rsheet of 50 Ω/□ for all resistivity values.

Based on the simulations, it was observed that the increasing bulk resistivity, i.e., reducing doping concentration, results in enhanced cell performance till 5 Ω.cm which then shows a saturation trend for all unit cell sizes as shown in Figure 3.27 (left). The same behavior was observed in different simulation and experimental studies focusing on various cell structures including IBC, SHJ, TOPCon, Al-BSF, PERL, PERT, etc. [55]–[57]. It could be deduced that, the trend in efficiency and other cell parameters does not only rely on material properties like wafer thickness, bulk resistivity, lifetime, etc., but also depends on the corresponding cell structure [56]. Analyzing the behavior of fill factor revealed that the increasing bulk resistivity (rho,bulk) reduces FF with a more pronounced effect with increasing unit cell size Figure 3.27 (right). Increasing bulk resistivity makes charge carrier transport more difficult accompanied by increased series resistance (R_{series}) which is more pronounced for the cell structures relying on lateral current flow [55]. Cells with uniform BSF with a blanket metal or conductive (Al-BSF, SHJ, PERT) layer are not affected by varying rho,bulk since the current flow in the base has a quasi-1 D character. However, the cells with local BSF layers (IBC, PERL) requiring 2 D current flow, show drop in FF values as rho,bulk increases. This effect could be suppressed by reducing metal pitch for PERL and reducing cell pitch, in other

words unit cell size for IBC cells [56], [57]. The same behavior was also observed for various emitter fractions as shown in Figure 3.28. Increasing bulk resistivity reduces fill factor for all unit cell sizes whose effect is more pronounce for larger unit cells.

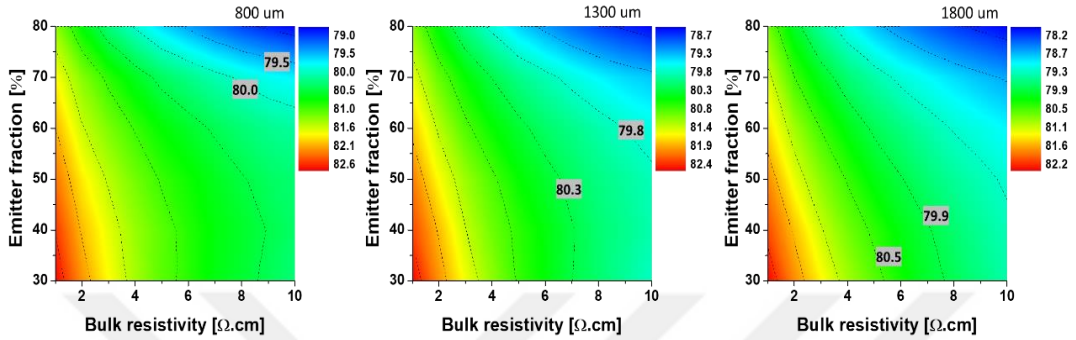


Figure 3.28. Effect of bulk resistivity on fill factor of IBC cells with FSF for varying unit cell sizes. Emitter and BSF regions' Rsheet values were chosen as 120 and 50 Ω/□, respectively.

Moreover, the larger emitter fraction reduces the FF of the device structure. Yet the resulting FF values above 78% were still reachable for all cases. Despite the decreasing trend of FF, the increasing and then saturating behavior of the efficiency could be mainly related to short circuit current density (J_{sc}) [57]. As shown in Figure 3.29 (left), increasing rho,bulk increases J_{sc} with a similar trend in efficiency.

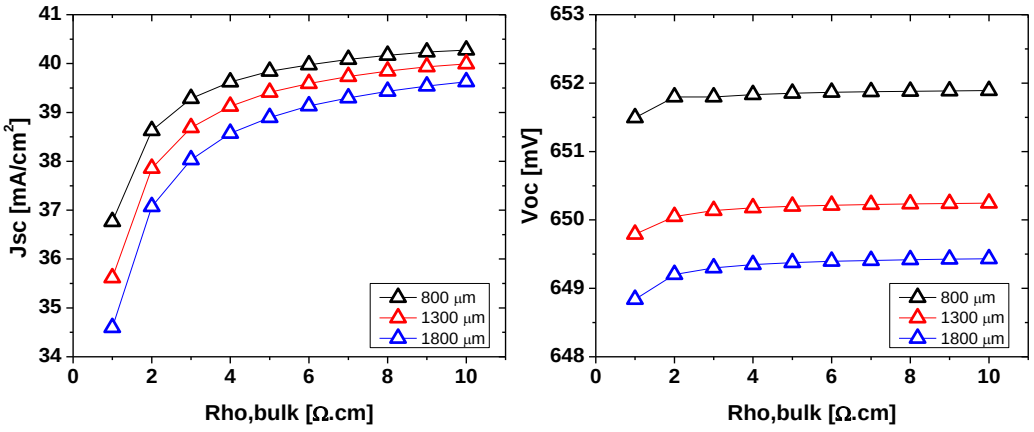


Figure 3.29. Effect of increasing bulk resistivity on short circuit current density (left) and open circuit voltage (right) for varying unit cell sizes of 800, 1300 and 1800 µm with a constant emitter Rsheet of 120 and BSF Rsheet of 50 Ω/□ for all resistivity values.

Short circuit current density (J_{sc}) is mainly determined by the performance of the high-low junction in the cell structure. For a lower base doping (i.e., higher rho,bulk), the doping step between the base and BSF region is increased, which reduces the effective surface recombination at the rear side (S_{eff}), and thus increases the effective diffusion length (L_{eff}) [56], [57]. While the effect of varying rho,bulk is less pronounced for PERT and PERL structures where peak doping concentrations of BSF regions are 1 order of magnitude higher than for the other cells, a relatively strong effect is observed for the Al-BSF and IBC structures [56], [58].

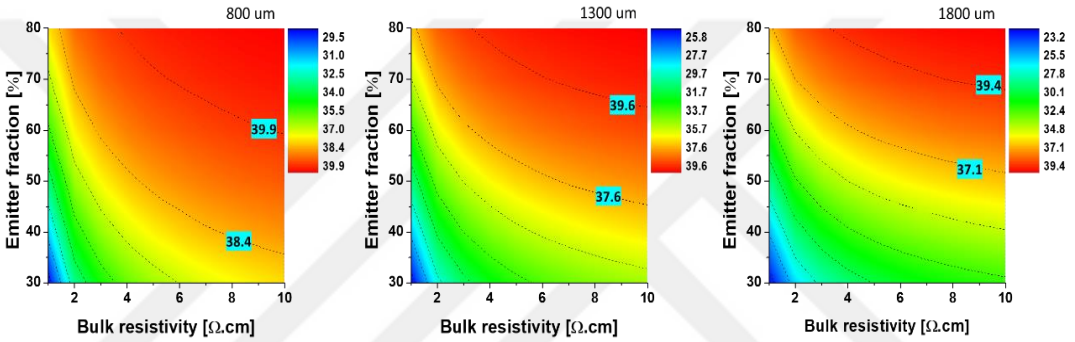


Figure 3.30. Effect of bulk resistivity on short circuit current density of IBC cells with FSF for varying unit cell sizes. Emitter and BSF regions' Rsheet values were chosen as 120 and 50 Ω/□, respectively.

The effect of bulk resistivity on J_{sc} given in Figure 3.29 (left) is the same for varying emitter fractions as shown in Figure 3.30. For a constant emitter fraction, J_{sc} first increases as a function of increasing rho,bulk and then saturates as already showed in Figure 3.29. For a constant rho, bulk, increasing emitter fraction also increases corresponding current till a certain level. Thus, the lowest J_{sc} value would be obtained for the combination of the lowest emitter fraction and low bulk resistivity values for FSF-IBC cells.

Unlike the other parameters, open circuit voltage (V_{oc}) was observed to be less dependent on rho,bulk as shown in Figure 3.29 (right). This is basically because the bulk is already in high-level injection (HLI) at V_{oc} conditions.

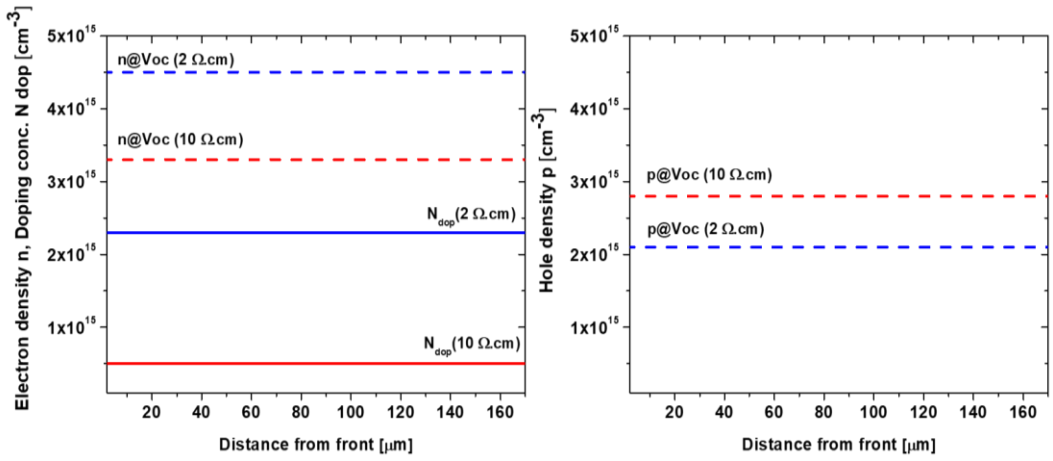


Figure 3.31. Simulated carrier densities for 2 and 10 Ω.cm base materials at V_{oc} conditions. Comparison of electron densities n and doping concentrations N_{dop} (left) and hole densities (right)[11]. The initial hole concentrations are calculated as $4.5x10^4$ and $2.0x10^4$ cm^{-3}.

Even the base with the 2 Ω.cm resistivity is in transition to HLI at V_{oc} conditions [57] which could explain the behavior of V_{oc} above 2 Ω.cm in Figure 3.31(right).

In the given graphs in Figure 3.31 which were plotted using the data of another study [57] verifies the HLI condition for n wafers with 2 and 10 Ω.cm base resistivity values.

$$Voc = \frac{kT}{q} ln\left(\frac{(N_{dop}+\Delta n)\Delta n}{n_i^2}\right) \qquad (Eq.3.13)$$

k: Boltzman's constant ($8.62x10^{-5}$ eV/K)

T: Absolute temperature in Kelvin

q: Elementary charge ($1.602x10^{-19}$ C)

N_{dop}: Base doping concentration (cm^{-3})

Δn: Excess carrier density (cm^{-3})

n_i: Intrinsic carrier concentration ($1x10^{10}$ cm^{-3} at 300K)

Considering the V_{oc} equation given in Eq.13 and applying the HLI condition where $\Delta n > N_{dop}$, the V_{oc} becomes independent of doping concentration which

corresponds to base resistivity. Thus, V_{oc} does not change as a function of varying bulk resistivity.

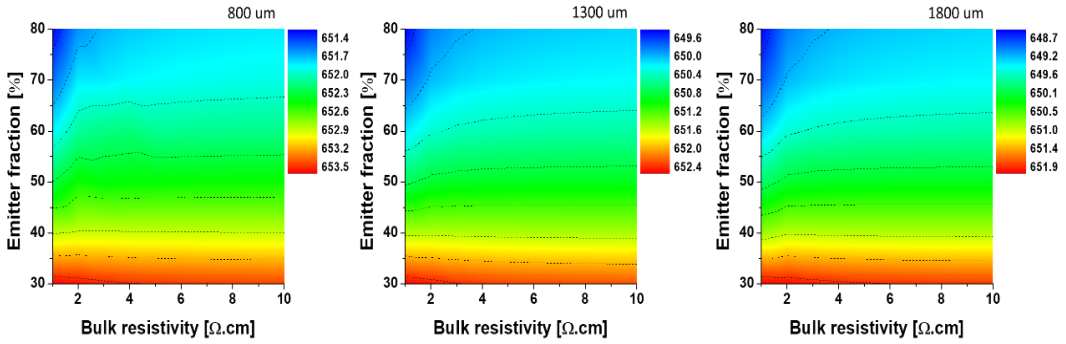


Figure 3.32. Effect of bulk resistivity on open circuit voltage of IBC cells with FSF for varying unit cell sizes. Emitter and BSF regions' Rsheet values were chosen as 120 and 50 Ω/□, respectively.

Effect of bulk resistivity on V_{oc} for different unit cell sizes is almost the same for all emitter fractions below 70% as shown in Figure 3.32. When the emitter fractions exceed 70% for 800 µm-wide unit cell, 65% for 1300 µm-wide unit cell and 60% for 1800 µm-wide unit cell, V_{oc} starts to reduce as the bulk resistivity reduces.

ii. IBC Cells with FFE

As shown in Figure 3.33, the combinative effect of emitter and BSF regions' sheet resistances is like that was observed on IBC cells with FFE. Increasing sheet resistance results in greater cell efficiency. Compared to FSF case, cells with FFE results in better performance.

While highest efficiency observed on the smallest unit cell for FSF-IBC cells was 20.9%, it was 21.2% for the case of cells with FFE. For the case of cells with FSF, simulated efficiency increases from 19.5 (1 Ω.cm) to 20.9% (5 Ω.cm) and stays constant at 20.9% (10 Ω.cm). However, for the case of cells with FFE, the simulated efficiency increases from 20.3 (1 Ω.cm) to 21.2% (5 Ω.cm) and then stays intact for 10 Ω.cm base resistivity.

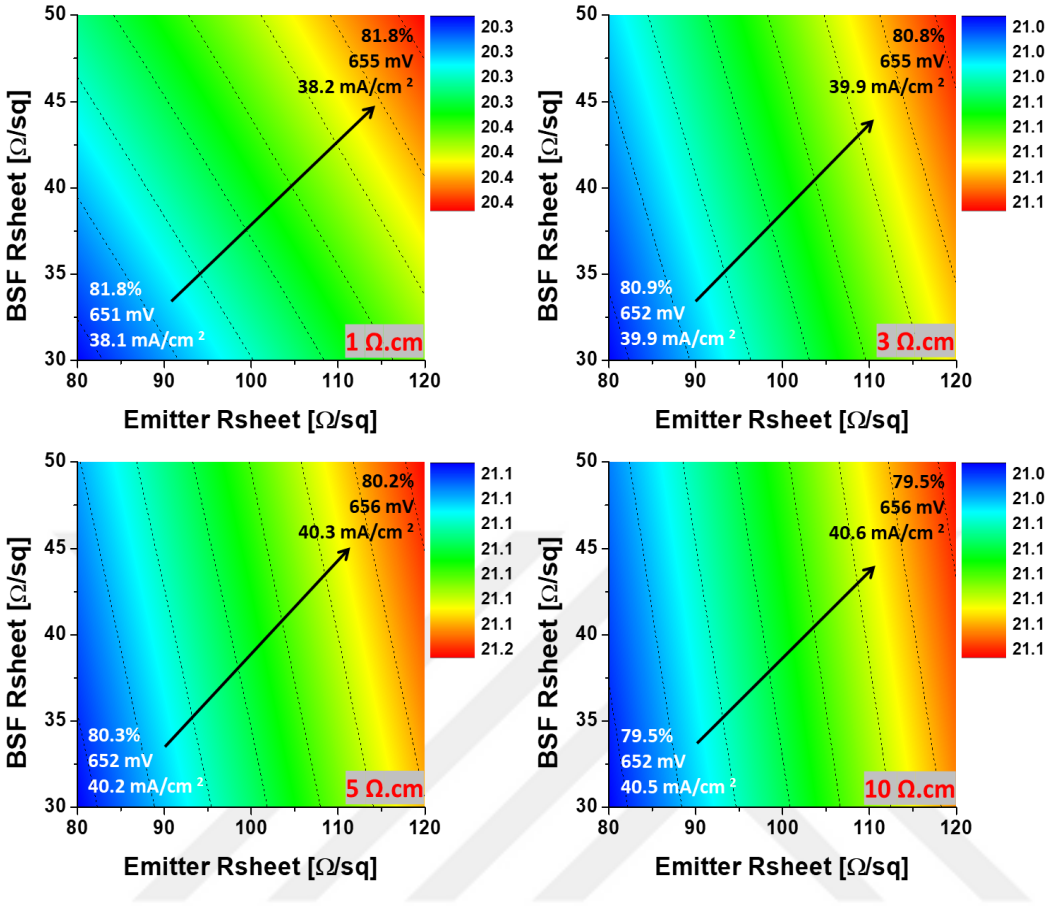


Figure 3.33. Distribution of efficiency as a function of emitter and BSF regions' sheet resistance for different bulk resistivity values for cells with FFE. The unit cell size was 800 µm and the chosen emitter fraction was 70% of the unit cell.

Increasing unit cell size to 1300 µm confines the resulting efficiency in 19.9-20.8% range which is further reduced 19.7-20.3% for 1800 µm which were 18.7-20.6% and 18.0-20.2% for the cells with FSF. Moreover, the J_{sc} values are lying within the range of 38.1-40.6 mA/cm^2 for the cells with FFE which was 36.7-40.3 mA/cm^2 for FSF case on the smallest unit cell. Increasing unit cell size reduces J_{sc} as in the case of FSF case. However, while the maximum J_{sc} was reduced from 39.3 to 38 mA/cm^2 for the cells with FSF, it was reduced from 39.9 to 39.8 mA/cm^2 for FFE case on 3 Ω.cm base material. It could be deduced that cells with FFE have greater tolerance to resistive losses, thus, bigger unit cells would be fabricated without a significant loss in the cell performance.

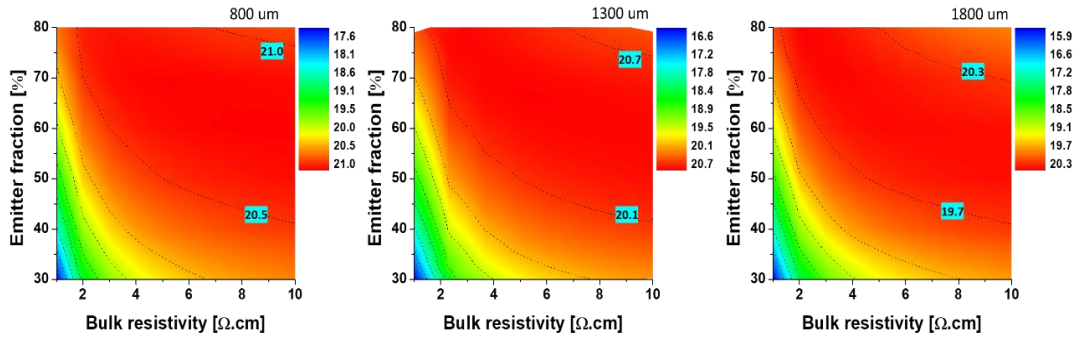


Figure 3.34. Effect of bulk resistivity on efficiency of IBC cells with FFE for varying unit cell sizes. Emitter and BSF regions' Rsheet values were chosen as 120 and 50 Ω/□, respectively.

Further analysis to understand the effect of emitter fraction and bulk resistivity on cell performance revealed that cells with FFE results in superior cell performance even for higher emitter fractions as shown in Figure 3.34.IBC cells with FFE show similar fill factor values as cells with FSF. The lowest FF values were obtained for the emitter fractions above 70% and bulk resistivities above 5 Ω.cm as shown in Figure 3.35. For the case of cells with FSF, critical emitter fraction was observed to be 70% with a base resistivity around 4.8 Ω.cm.

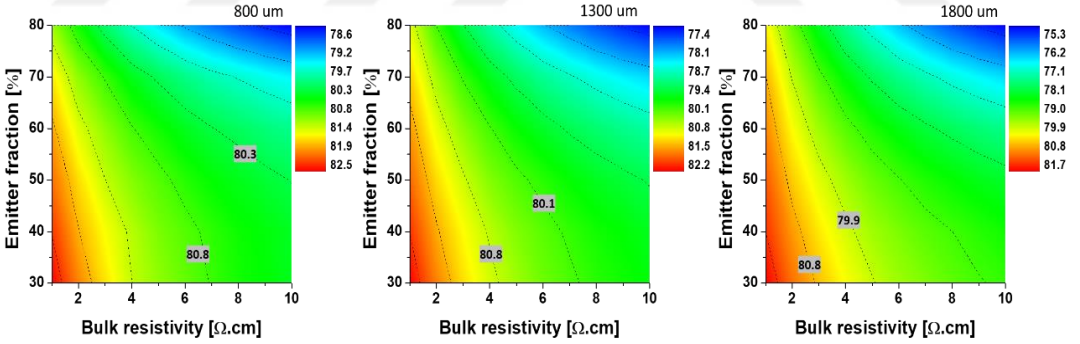


Figure 3.35. Effect of bulk resistivity on fill factor of IBC cells with FFE for varying unit cell sizes. Emitter and BSF regions' Rsheet values were chosen as 120 and 50 Ω/□, respectively.

As in the case of cells with FSF, cells with FFE also show almost constant V_{oc} values. While the maximum V_{oc} values of the former case varied as 653, 652 and 652 mV as a function of increasing unit cell, the same for the latter case varied as 657, 655 and 655 mV as the unit cell size increased as given in Figure 3.36.

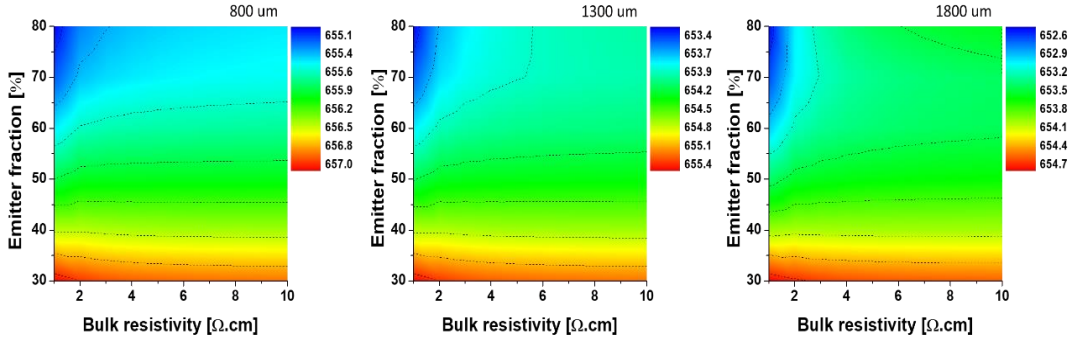


Figure 3.36. Effect of bulk resistivity on open circuit voltage of IBC cells with FFE for varying unit cell sizes. Emitter and BSF regions' Rsheet values were chosen as 120 and 50 Ω/□, respectively.

Increasing bulk resistivity shows no significant effect on the cell V_{oc} as discussed in the previous section. Having emitter fractions greater than 60% slightly reduces the simulated V_{oc} values which could be related to the effect of reducing FF as a function of increasing emitter fraction.

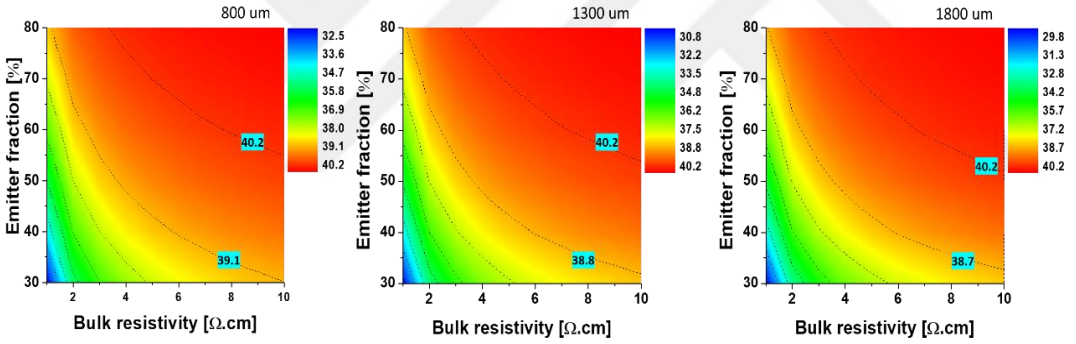


Figure 3.37. Effect of bulk resistivity on short circuit current density of IBC cells with FFE for varying unit cell sizes. Emitter and BSF regions' Rsheet values were chosen as 120 and 50 Ω/□, respectively.

Increasing bulk resistivity, improves J_{sc} value of the corresponding cell which is basically related to the suppressed recombination losses as the doping concentration reduces as discussed in the previous section. The cells with FEE could generate 40.2 mA/cm^2 short circuit current density regardless of the unit cell size while the cells with FSF could generate 39.9, 39.6 and 39.3 mA/cm^2 for respective unit cell sizes of 800, 1300 and 1800 µm. That is the IBC cell structure with FFE is less prone to cell geometry and bulk resistivity which would provide more tolerance in industrial fabrication processes.

At the end of this simulation set, the effect of bulk resistivity, emitter fraction, emitter/BSF sheet resistance on cell performance was realized. Although 5 Ω.cm was observed to be the critical bulk resistivity above which cell efficiency saturated at its maximum value, using 3 Ω.cm as the base resistivity did not generate a significant drop in cell performance. Thus, 3 Ω.cm n-Si wafers which were already available in GUNAM stock, were decided to be used in the following processes without a need for new wafer purchase. Moreover, reducing the unit cell size was observed to improve cell performance so that the unit cell size of 800 μm was decided to be more promising. Despite relatively better performance of FFE structure, cells with FSF will also be fabricated during the experimental studies till the baseline processes are optimized.

3.3.3 The Effect of the Varying Gap Properties and Wafer Thickness

Running simulations for varying gap and emitter fractions revealed the fact that increasing gap fraction reduces the cell efficiency after a certain gap value. That certain value mainly depends on emitter fraction of the corresponding cell structure. Since increasing gap width will reduce BSF width for a fixed emitter fraction, resistivity losses will dominate the cell performance.

As shown in Figure 3.38, increasing gap reduces FF factor by a factor of 4% from 79 to 75% for all emitter fractions. The drop in FF was almost the same for the cells with FFE and FSF. While the cells with smaller emitter fraction of 30% experience the drop in FF at a greater gap fraction of around 60%, for those with larger emitter fractions of 50 and 70% drop in efficiency starts at the respective gap fractions of 40 and 20%. However, it should be noted that the wider emitter region already limits the total width of gap and BSF region. Thus, it is expected to have the FF drop at lower gap fractions for the cells with wider emitter regions.

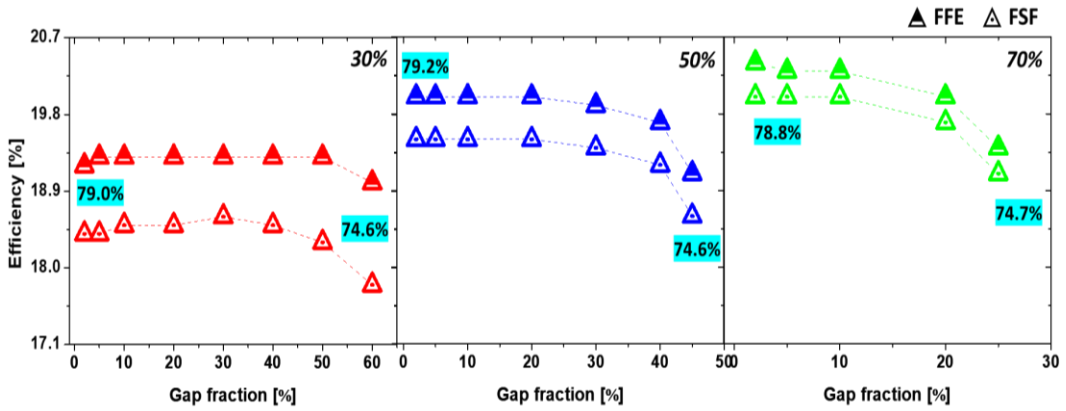


Figure 3.38. Effect of increasing gap fraction for the cells with varying emitter ratios. Half-filled symbols represent the cells with FFE and the symbol with dot in the middle represent the cells with FSF. Emitter fraction varies as 30, 50 and 70% from left to right. The inset highlighted numbers correspond to respective fill factors for the lowest and the highest gap fractions. Gap passivation was defined with J_0: 250 fA/cm^2.

While simulated V_{oc} values were constant at 656-658 and 653-655 mV for respective FFE and FSF structures regardless of the gap fraction, J_{sc} values showed 2-3mA/cm^2 improvement as a function of increasing emitter fraction. Thus, the observed drop in the simulated efficiency could be related to the increasing resistive losses resulting in reduced FF values.

To understand the effect of unit cell size for varying gap fractions, the constant emitter fraction at 50% and the two limiting unit cell sizes: 800 and 1800 µm were focused on both for FFE and FSF structures.

For the case of smallest unit cell (800 µm) shown in Figure 3.39 (left), increasing gap fraction starts to reduce the cell efficiency when its fraction reaches 40% of the unit cell. Although the initial and final FF values were the same for FFE and FSF structures, due their superior V_{oc} and J_{sc} values, cells with FFE structure show higher efficiency values. Increasing unit cell size from 800 to 1800 µm, significantly reduces the performance of the cells with FSF which is less pronounced for the cells with FFE. However, the effect of varying gap fraction is almost the same as in the case of the smallest unit cell as shown in Figure 3.39 (right). Above 40% gap fraction, FF drops significantly which reduces the corresponding cell efficiency.

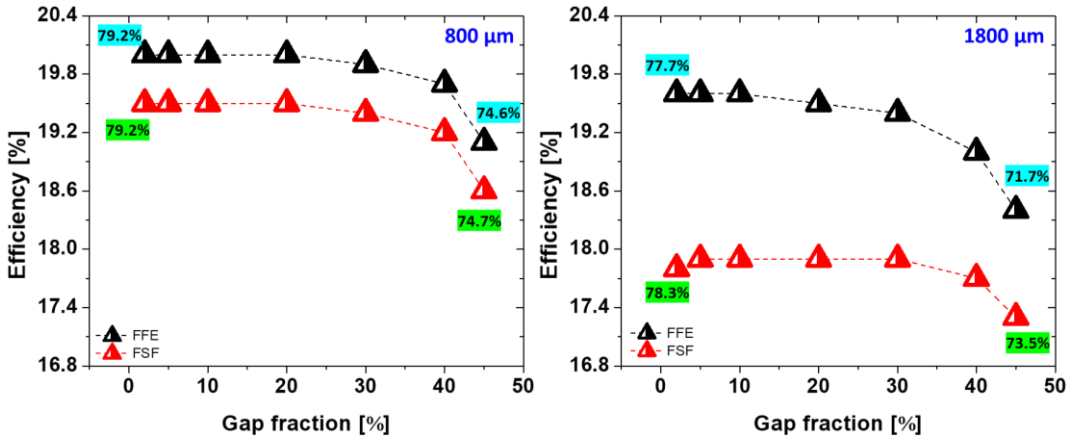


Figure 3.39. Effect of varying gap on the cells with the smallest (left) and the largest unit cell size (right) for FFE and FSF structures. Gap passivation was defined with J_0: 250 fA/cm^2.

To further analyze the gap effect, the smallest unit cell size was chosen for the unit cell with the emitter fraction of 50%. Different than the previous task, surface recombination velocity of the gap region was set two different values. While 50 cm/s was used to mimic a properly passivated gap region, 2000 cm/s was used to mimic a poorly passivated surface.

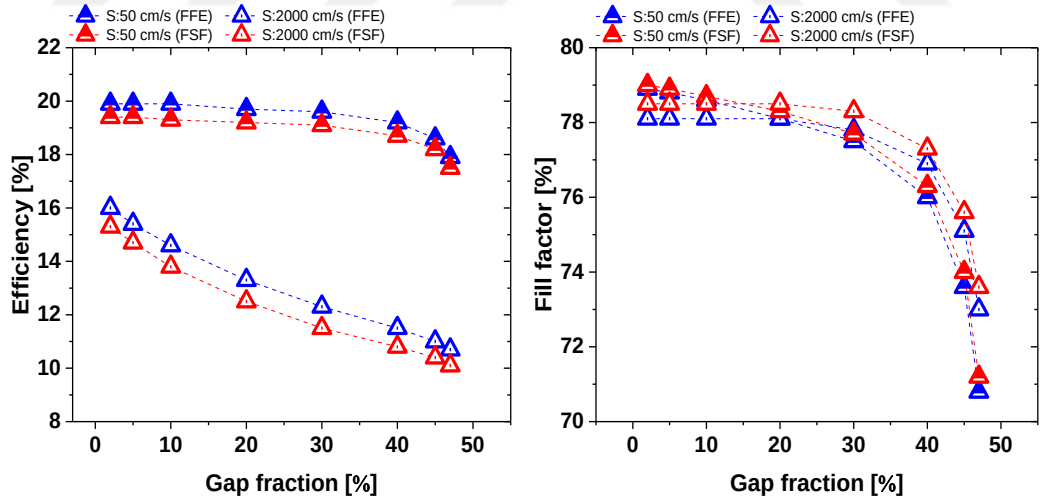


Figure 3.40. Effect of varying gap fractions on efficiency (left) and fill factor (right) of the IBC cells with FFE and FSF. Passivation properties of the gap region was defined using two different S values of 50 and 2000 cm/s.

As seen in Figure 3.40 (left), for a properly passivated gap region (S:50 cm/s), cell efficiency was almost independent of increasing gap fraction for both FFE and FSF structures. The drop in cell efficiency for the gap fractions above 40% could be related to the reducing FF values given in Figure 3.40 (right). Contrary to properly passivated surfaces, for the case of poorly passivated gap regions (S:2000 cm/s), the efficiency shows a linear dependence on the increasing gap fractions. Even for the smallest gap fraction (2%), the efficiency was lowered by 4% compared to the cells with S:50 cm/s. However, the fill factor was observed to be a weak function of surface recombination velocity (*S*) which was mainly determined by the gap fraction (Figure 3.40 (right)).

In Figure 3.41, it was observed that not only V_{oc} but also J_{sc} was independent of the varying gap fraction if the gap region was passivated properly.

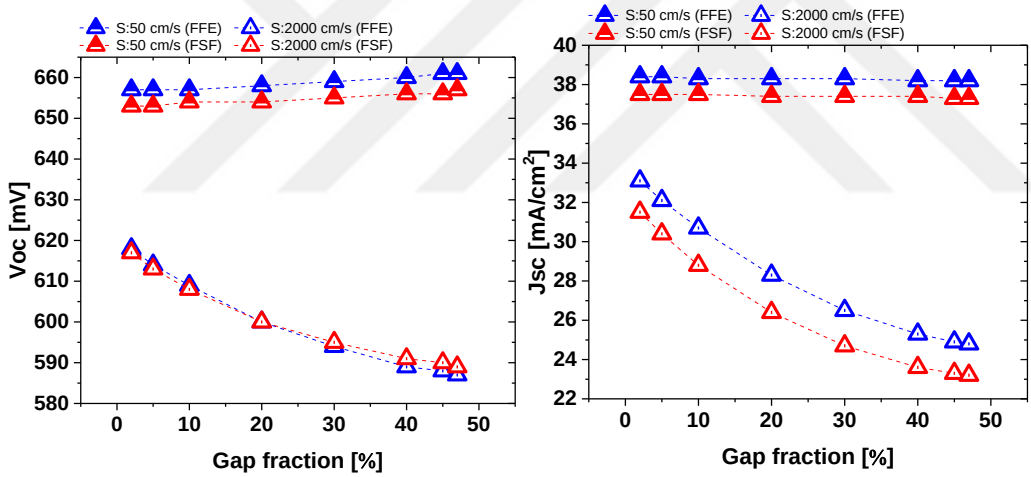


Figure 3.41. Effect of varying gap fractions on open circuit voltage (left) and short circuit current density (right) of the IBC cells with FFE and FSF. Passivation properties of the gap region was defined using two different S values of 50 and 2000 cm/s.

However, if it was poorly passivated accompanied by S: 2000 cm/s, then both V_{oc} and J_{sc} reduces as a function of increasing gap fraction. Thus, considering similar FF values for properly and poorly passivated gap conditions, the difference in efficiency could be related to the difference in V_{oc} and J_{sc} values which are determined by the passivation quality of the gap region.

As the final task of the simulation studies, wafer thickness optimization was carried out. For this, a constant emitter fraction of 50% was applied both for FFE and FSF cells. The smallest and the largest unit cell sizes were focused on as the limiting cases. As shown in Figure 3.42, for the smallest unit cell size (800 µm) cells with FFE show the maximum efficiency of 20.1 for the wafer thickness of 110 µm while their FSF counterparts have the maximum efficiency of 19.5% at the wafer thickness of 200 µm. However, the efficiency reached at the value of 19.4% for the corresponding thickness of 133 µm. Thus, it could be said that for the cells with FFE, wafer thickness could be 86-156 µm while it could be in the range of 133-250 µm for the cells with FSF.

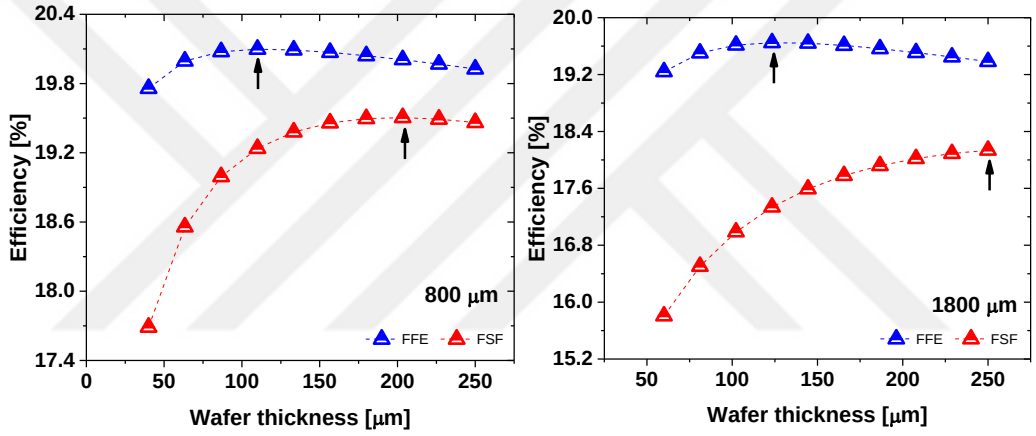


Figure 3.42. Change in cell efficiency for varying wafer thicknesses. The emitter fraction was kept constant at 50% for the unit cell sizes of 800 µm (left) and 1800 µm (right). Black arrows are pointing the maxima of the cell efficiency.

Unlike the smaller unit cell size (800 µm), for the case of the bigger unit cell (1800 µm) the FSF cell efficiency showed a different behavior than the former case. It was observed that increasing wafer thickness improved the cell performance. On the other hand, cells with FFE showed similar behavior as in the case of smaller unit cell so that 86 µm-thick wafer was enough to reach at the maximum cell performance.

3.4 Conclusions

At the end of simulation studies, important information about IBC cell design was extracted. In the first part, the effect of bulk properties was figured out for a constant cell pitch of 2000 μm where sheet resistances of emitter, BSF, FFE and FSF regions were also kept constant. Sweeping the bulk lifetime and bulk resistivity for various emitter fractions revealed that increasing bulk resistivity was increasing cell efficiency till a certain emitter fraction which was then either saturating or reducing. While the improvement in the efficiency was related to the improved short circuit current density, observed saturation or even reduction in cell efficiency was due to the drop in fill factor. The FF loss for higher emitter fractions was because of the increasing pathlength that the charge carrier (electron) should travel before being collected at the corresponding (BSF) contact. Moreover, increasing bulk resistivity made the fill factor more dependent on the bulk lifetime. As the performance of FSF cells was more dependent on emitter fraction, FFE cells were observed to tolerate wider BSF regions with slight losses in the cell performance. It was also observed that bulk lifetime of 3000 and 5000 μs was resulting in quite close cell performances for all base resistivity values both on FFE and FSF structures.

After having a general perception about the effect of bulk parameters on IBC cell performance, a more detailed simulation run was carried out. Different than the first part, unit cell geometry and sheet resistances of all doped regions (emitter, BSF, FFE, FSF) were varied in this part. It was observed that increasing emitter and BSF sheet resistances resulted in better cell performances for all bulk resistivity values. FFE-IBC cells were observed to have less geometry dependent performance compared to FSF-IBC cells as in the case of previous part. Increasing unit cell size was reducing the resulting cell performance both for FFE and FSF structures. The coupled effect of emitter fraction and bulk resistivity was obtained to provide a wider process window for the cells with FFE compared to those with FSF. Depending on the unit cell size, either a higher bulk resistivity with a

narrower emitter or a lower bulk resistivity with a wider emitter would result in the same cell efficiency. It was also observed that for each unit cell size, there was a certain bulk resistivity value above which cell efficiency stays the same which was 5 Ω.cm for the analyzed cell configuration. However, there was no significant difference between cell performances of the cells with 3 Ω.cm and 5 Ω.cm base resistivities. Open circuit voltage was observed to be almost independent of the bulk resistivity. That was because the bulk was already in high injection even for a wafer with 2 Ω.cm resistivity so that change in carrier density at V_{oc} conditions was always greater than the carrier density defined by the base doping. Observed enhancement in short circuit current density was mainly due to the suppressed recombination losses as the base doping concentration reduced which was accompanied by drop in fill factor. The fill factor losses were more pronounced as the unit cell size got bigger.

As the last task of simulation studies, the effect of gap properties and wafer thickness were studied. It was observed that if the gap is properly passivated, increasing gap fraction does not influence the resulting cell efficiency till a certain fraction which was 40%. However, above that certain value further increase in the gap width will reduce the corresponding BSF width which will reduce the collection probability of the charge carriers at the corresponding BSF contacts. This effect will return as reduced fill factor, thus reduced cell efficiency. Moreover, V_{oc} and J_{sc} values showed no dependency on the gap fraction. However, if the gap region is poorly passivated, then the efficiency has an inverse relation with the increasing gap fraction. Both V_{oc} and J_{sc} was inversely dependent on the increasing gap fraction while FF values were almost the same as in the case where the gap region was properly passivated. So that, for a proper passivation gap region could be kept as wide as possible till the FF losses dominate the cell performance. On the contrary, for poorly passivated gap regions, the narrower gap region would perform superior.

CHAPTER 4

DESIGN AND FABRICATION OF INTERDIGITATED BACK CONTACT SOLAR CELLS AND PRIMITIVE CELL RESULTS

In this chapter, design and fabrication of interdigitated back contact solar cells is presented. A new, completely industry compatible and lithography-free process flow is suggested and applied to fabricate the first IBC cells. Etch resist-based patterning process will also be discussed in this chapter.

4.1 Introduction

The novel fabrication method suggested in this thesis relies on the application of screen printable etch resist. Etch resist is a special type of ink with a greater viscosity than regular photoresists have but with a similar working principle. Depending on the curing temperature and etchant concentration, etch resists can resist in acidic or alkaline etchants for tens of minutes. Thus, the regions covered by etch resist will be protected against etching while the uncovered regions will be etched away. Using this principle, SiN_x layers will be patterned and used as diffusion barrier during boron and phosphorus diffusion. By this, the only additional process steps will be the screen printing of etch resist, its patterning and stripping. Remaining steps are the same as in a typical n-type cell fabrication including BBr_3/BCl_3 and $POCl_3$ diffusion, surface passivation and metallization. While SiO_2/SiN_x stack was aimed to be used as the first case passivation scenario due to the availability of the corresponding process tools in all production lines, Al_2O_3/SiN_x stack was also applied due to its superior passivation properties on p and p^+ doped regions. For the metallization, industrial fire-through metallization without any need for laser contact opening was applied.

4.2 Experimental Details

Following the analysis of the first simulations, a set of screens was designed to fabricate 4x4 cm^2 small area cells on each wafer. Two separate screens are required to pattern the emitter and BSF regions prior to boron and phosphorus diffusion, respectively. Each screen is decorated with a test pattern to analyze the corresponding diffusion process and seven small area cells with three different unit cell sizes. The layouts of the first screen design to process the emitter and BSF regions are given in Figure 4.1(left) and (right), respectively. The utilized pitch values are 750, 1250 and 1750 μm. Metal fraction was 70% of the diffused region both for emitter and BSF regions in the primitive version of the screens which were than reduced to 30% in the updated design.

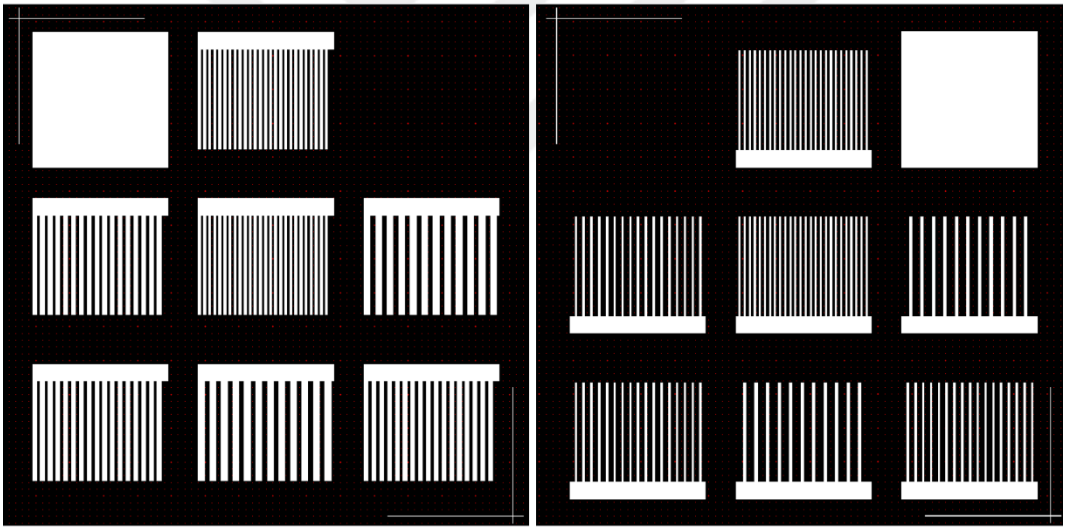


Figure 4.1. The first version of the screen design for the patterning of emitter (left) and BSF region (right).

The suggested process sequence will first start with surface texturing and following RCA-1 and RCA-2 cleanings as shown in Figure 4.2. RCA-1 and RCA-2 cleanings would be replaced with Ozone cleaning for the case of industrial process tools. Then, a thick layer of SiN_x is deposited by PECVD which will then be patterned and used as the diffusion barrier. After that, etch resist will be screen printed and cured at a temperature above 100^oC.

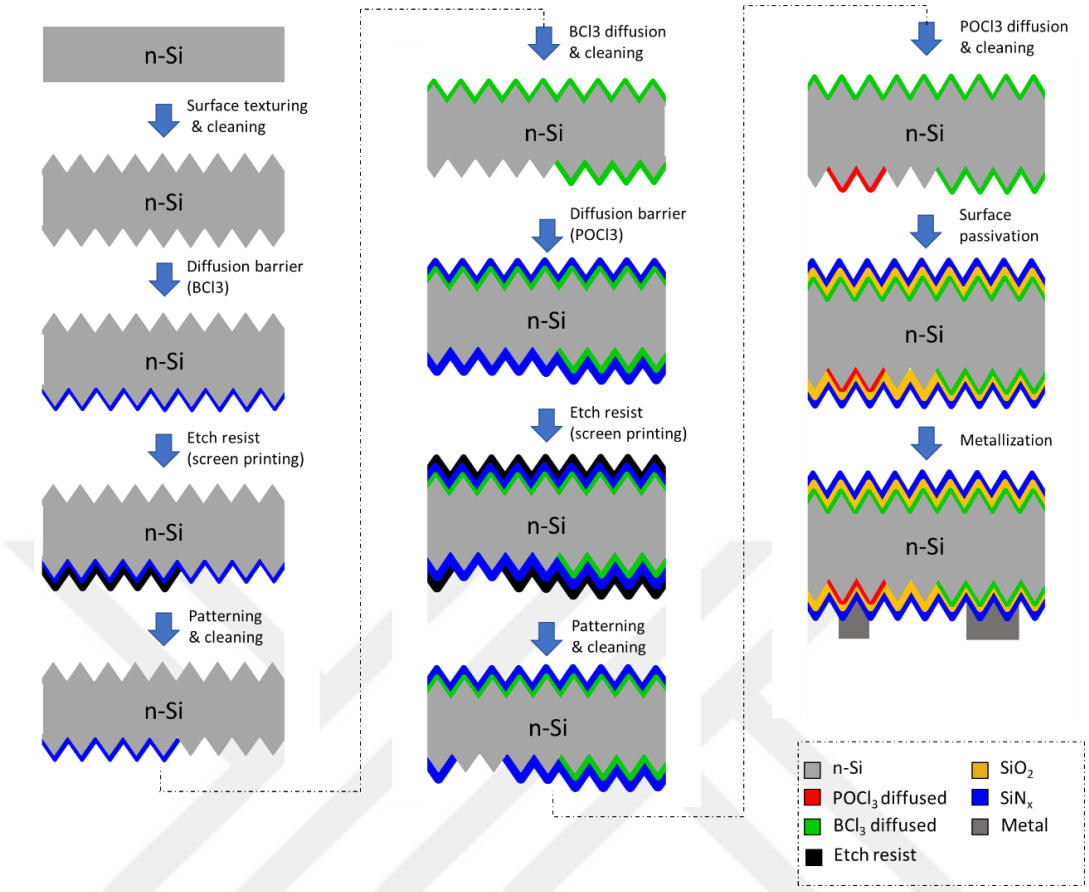


Figure 4.2. Designed process flow for the fabrication of FFE-IBC cells with etch resist-based patterning.

Following the HF patterning, resist stripping and cleaning steps, samples are then exposed to BCl_3 diffusion to form emitter at the rear side of the wafers. After stripping the borosilicate glass (BSG) and cleaning steps, another thick SiN_x will be deposited. This time the patterning will be done using BSF screen shown in Figure 4.2 (right). Following the same etching, stripping, and cleaning steps, $POCl_3$ diffusion will be carried out for BSF formation. Then, PSG layer will be stripped, and last cleaning steps will be applied prior to passivation. For the passivation SiO_2/SiN_x stack will be used where SiO_2 layer will be obtained by dry oxidation, SiN_x layer will be deposited by PECVD. As a second alternative, Al_2O_3/SiN_x stack will also be applied for surface passivation. As the last step of the fabrication, fire-through FT-AgAl and FT-Al will be screen printed on emitter and BSF regions respectively. Printed metal activation will be provided by co-firing using an

industrial conveyor belt type firing furnace. At the end of the fabrication sequence, three different cell structures with different emitter/BSF ratios will be formed on each wafer. In the case of FSF-IBC cell, the same process flow as given in Figure 4.2 will be followed with a difference that the front side will be protected during BCl_3 diffusion and exposed to doping gas during $POCl_3$ diffusion. At the end of metallization step, the rear side will have the interdigitated pattern shown in Figure 4.3.

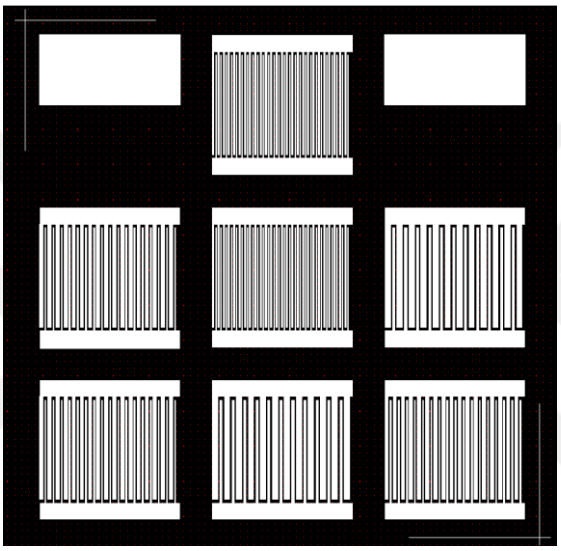


Figure 4.3. Screen design for fire-through metallization of the interdigitated emitter and BSF metals.

Using the first set of screens; patterning, boron, and phosphorus optimization studies were initiated. Application of boron doping paste or boron implantation instead of BCl_3/BBr_3 diffusion are the other alternatives for boron diffusion that were applied in other studies and will not be discussed within the scope of this thesis.

4.2.1 Etch Resist Optimization Studies

As the first step of fabrication sequence, etch resist printing and patterning was required to be optimized. For this purpose, two different SiN_x layers deposited with different SiH_4/NH_3 ratios were applied as diffusion barrier. While the so-called N-

rich SiN_x layer was deposited with a SiH_4/NH_3 ratio of 0.065, the so-called Si-Rich SiN_x layer was deposited with SiH_4/NH_3 ratio of 0.124. SiN_x deposition was carried out in a direct plasma PECVD system from SEMCO Engineering and screen printing was done with an ASYS-EKRA X1 type screen printer. The curing of the printed resist was done in a NUVE KD-200 furnace.

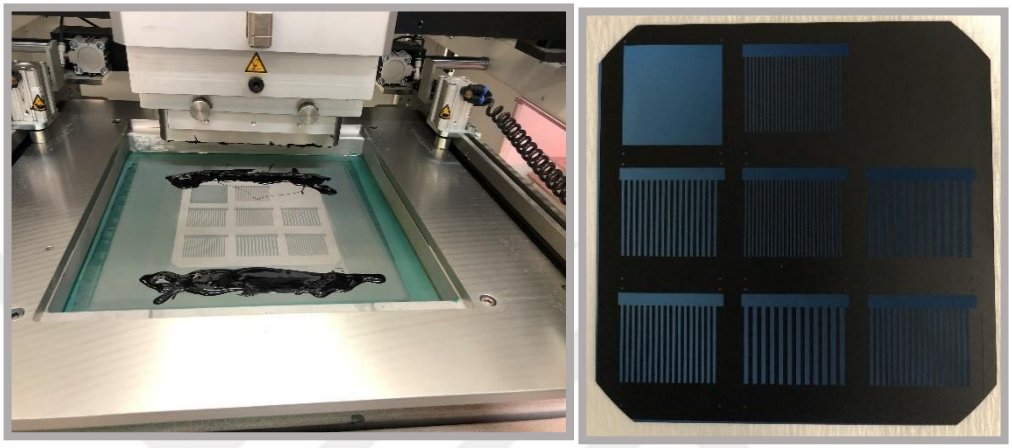


Figure 4.4. Appearance of etch resist during screen printing (left) and after printing/drying (right).

Appearance of etch resist during the printing and after drying, is shown in Figure 4.4. After optimizing the printing and the curing parameters resulting in a properly thick and uniform resist layer on wafer, the next step was patterning the diffusion barrier underneath. With the help of dilute hydrofluoric acid (HF) solution, deposited SiN_x layers were successfully patterned such that the regions lying under the printed resist stayed intact while the uncovered regions were etched away. Thus, the opened regions will be exposed to doping gas during diffusion step while the rest of the surface is protected.

4.3 Experimental Approach

The first set of cell fabrication was started with the optimization of etch resist-based patterning of the diffusion barrier which is SiN_x layer in our case. For this purpose, an ink, resistive to certain acids, was screen printed on top of the SiN_x layer. Depending on the process, a screen with emitter or BSF pattern was utilized.

While SiN_x layers capped with etch resist will be protected in dilute hydrofluoric acid (HF) solution, the uncovered regions will be etched away. Thus, the open regions of the SiN_x layer will let the dopant atoms diffuse through the wafer while the intact regions will block the incoming dopant atoms. For being a proper diffusion barrier, SiN_x layer is needed to be completely etched for the open regions and perfectly block the dopant for the covered regions on the same wafers. For the Si-rich SiN_x layers, the SiH_4 /NH_3 ratio fed to the system was 0.124 while for N-rich layers it was set to 0.065. For each thickness value namely 80, 100 and 120 nm, HF dip duration was separately optimized till the uncapped regions of the SiN_x deposited wafers became hydrophobic. Based on etching properties, the most suitable SiN_x thickness and composition were determined.

After determining the diffusion barrier recipe, the first set of IBC cell fabrication was initiated. Patterning the selected diffusion barrier for emitter diffusion was followed by RCA-1 and RCA-2 cleans. Then BCl_3 diffusion for emitter formation was carried out with BCl_3 flow of 40 sccm at 935°C. After BSG removal, sheet resistance, PL and iVoc measurements were carried out. After the characterization of the emitter region, a fresh diffusion barrier was deposited on the samples to be patterned for BSF region. $POCl_3$ diffusion was carried out at 838°C. Front side of half of the samples was protected during BCl_3 diffusion which were then exposed to $POCl_3$ diffusion to obtain front surface field structure while the other half was processed in the opposite way to end up with front floating emitter structure. As being the first cell trial, front side diffusions were kept the same as the rear side diffusion. After BCl_3 and $POCl_3$ diffusion steps, a thin passivation layer SiO_2 was grown in a reduced pressure furnace and then SiN_x layer was symmetrically deposited on both sides of the samples. After each process step, Sinton and PL measurements were carried out to trace the change of implied Voc. Then, the fabrication sequence was completed by screen printing and contact firing steps where FT-AgAl paste was used for emitter side, FT-Ag paste was used for the BSF region.

4.4 Results and Discussions

After the patterning and resist stripping steps, image of the resulting SiN_x layers is shown in Figure 4.5. It was observed that 80 nm of Si-rich layers could be successfully patterned while 100 and 120 nm thick layers cannot be patterned properly. This could be related to the enhanced chemical resistance of the Si-rich layers. The enhanced film resistance makes patterning harder. Thus, the corresponding etching duration is required to be increased as the film becomes richer in Si-content for the same thickness. However, the etch resist itself has a lifetime in the acidic solution, beyond that lifetime the resist layer starts to peel off. Thus, using a Si-rich diffusion barrier does not offer advantages.

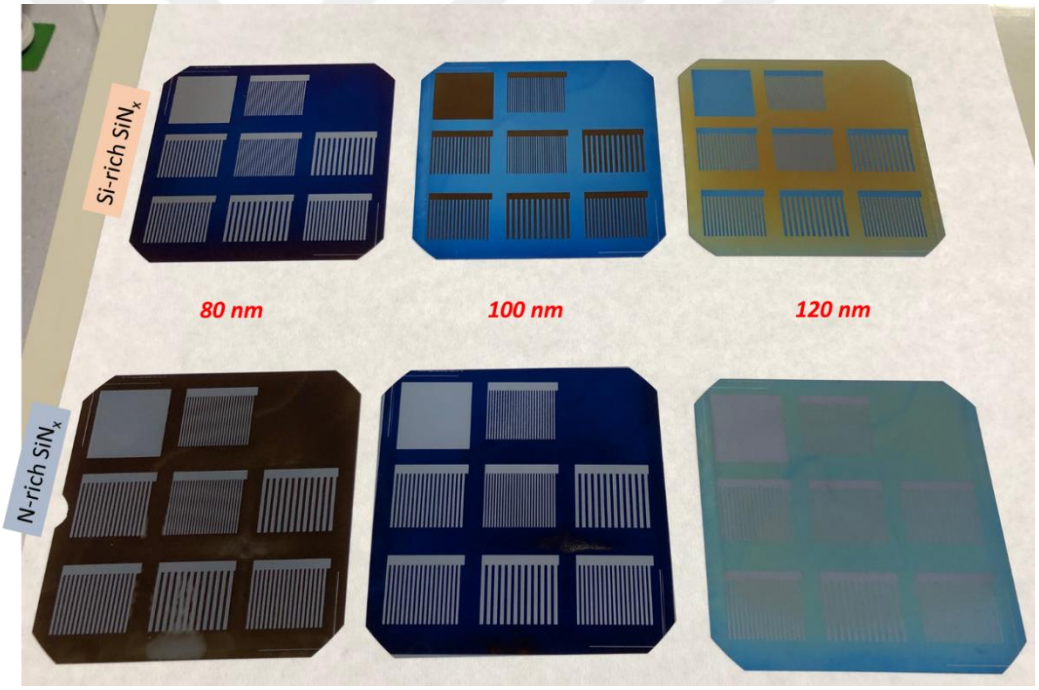


Figure 4.5. Appearance of Si-rich and N-rich SiN_x layers after patterning and cleaning.

Based on the pre-tests, N-rich SiN_x layers with a thickness of 100 and 120 nm could be patterned without any problems and could successfully block both B and P atoms during corresponding diffusion processes. Hence, these layers would be used as the diffusion barrier for the following cell fabrication processes. To ensure the blocking of the doping atoms, 120 nm thick layers were determined to be used

as diffusion barrier for the cell fabrication processes. After the first patterning and following cleaning steps, samples were exposed to BCl_3 diffusion. After BSG removal, sheet resistance, PL and iVoc measurements were carried out. Sheet resistance values were mapped over "*test pattern*" region on the selected samples and the corresponding results are given in Figure 4.6. The average Rsheet value was around 73 Ω/□ with a deviation of ± 3 Ω/□.

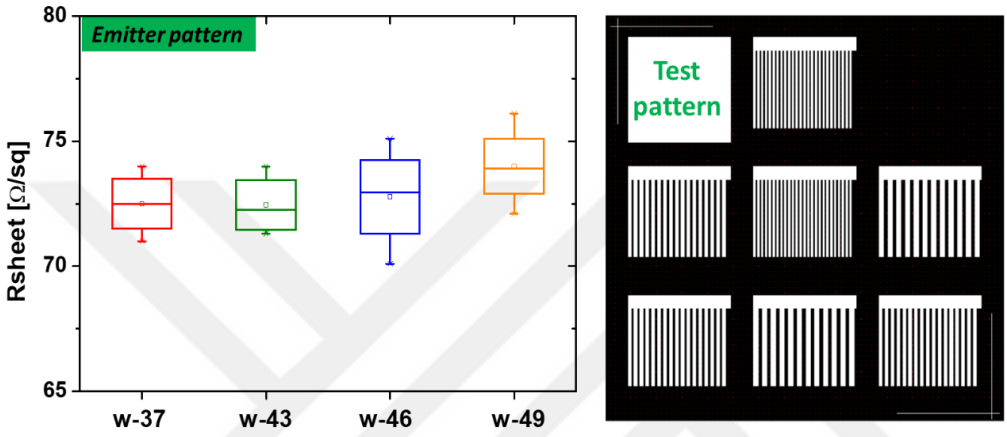


Figure 4.6. Sheet resistance distribution (after BCl3) mapped over emitter test pattern region (left) and corresponding screen design (right). The wafer numbers given in the horizontal axis of the plot stay for different wafers positioned in different slots on the process boat.

After BCl_3 diffusion, $POCl_3$ diffusion was carried out through the diffusion barrier patterned with BSF geometry. Sheet resistance mapping was done over test pattern for BSF regions, and the corresponding results are shown in Figure 4.7. The average sheet resistance of $POCl_3$ diffused regions on n-Si was around 30 Ω/□ which was around 130-135 Ω/□ before diffusion. This confirms that the patterned layer was successfully blocking the incoming boron atoms during emitter formation. After stripping the diffusion barrier used for $POCl_3$ diffusion, it was observed that sheet resistance of boron diffused regions increased by 5- 7 Ω/□ which could be related to the effect of high process temperature.

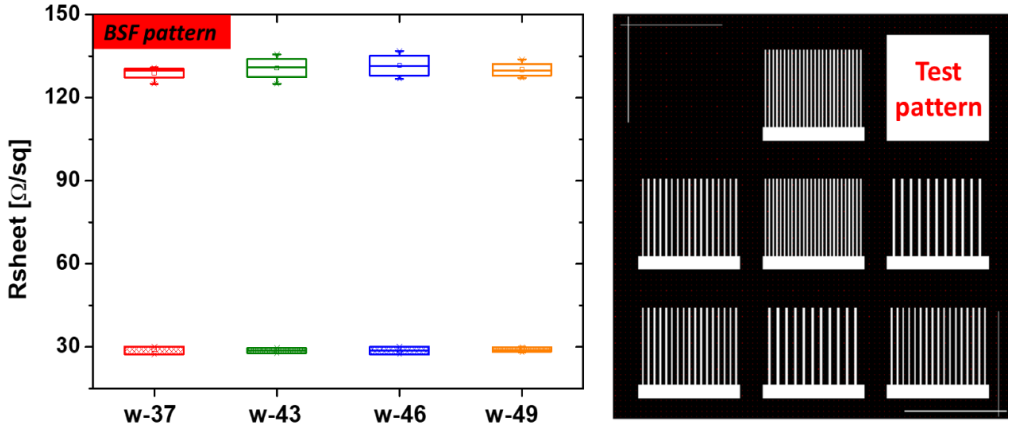


Figure 4.7. Sheet resistance distribution before $POCl_3$(empty boxes) and after $POCl_3$(textured boxes) mapped over emitter test pattern region (left) and corresponding screen design (right). The wafer numbers given in the horizontal axis of the plot stay for different wafers positioned in different slots on the process boat.

Moreover, it could be deduced that the diffusion barrier was also successfully blocking the incoming phosphorus atoms during BSF formation. Rear side of a selected sample was imaged after each step for visual inspection and shown in Figure 4.8.

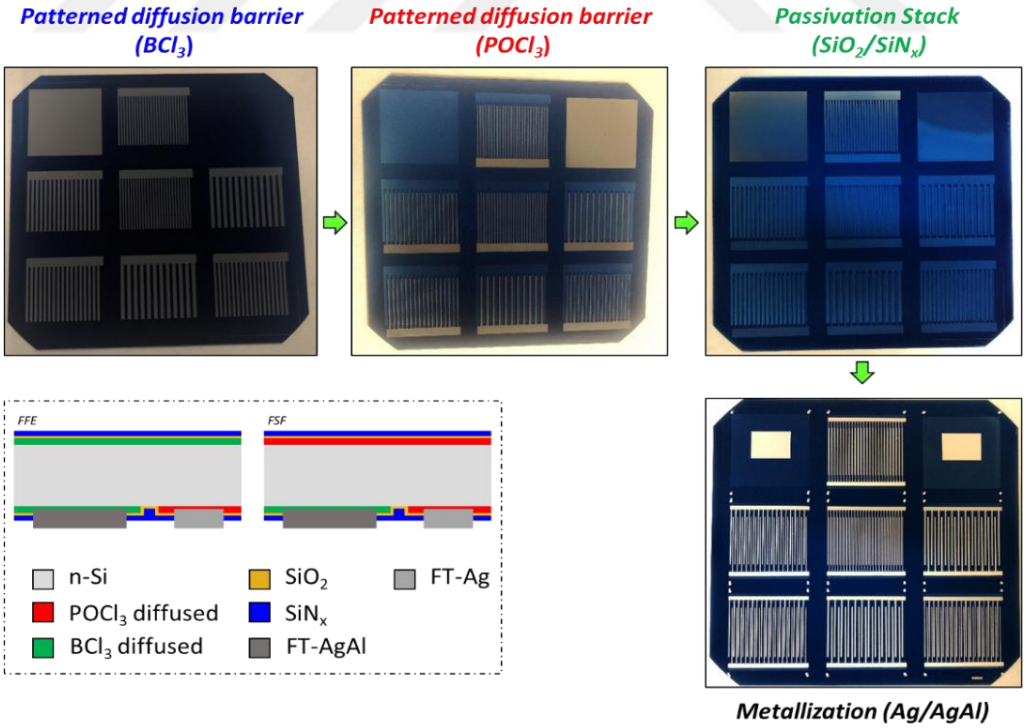


Figure 4.8. Visual inspection of samples during successive process steps.

The first generation of screen design is shown in Figure 4.9. While the emitter and BSF regions' test patterns are used for Sinton measurements during successive process steps and ECV measurements at the end of the whole process sequence, IBC cells with different pitches are distributed over the remaining area. For each pitch value, at least two cells are placed on the same wafer for statistical data. For the pitch values of 750, 1250 and 1700 µm, emitter values of 700, 1200 and 1800 µm were used, respectively.

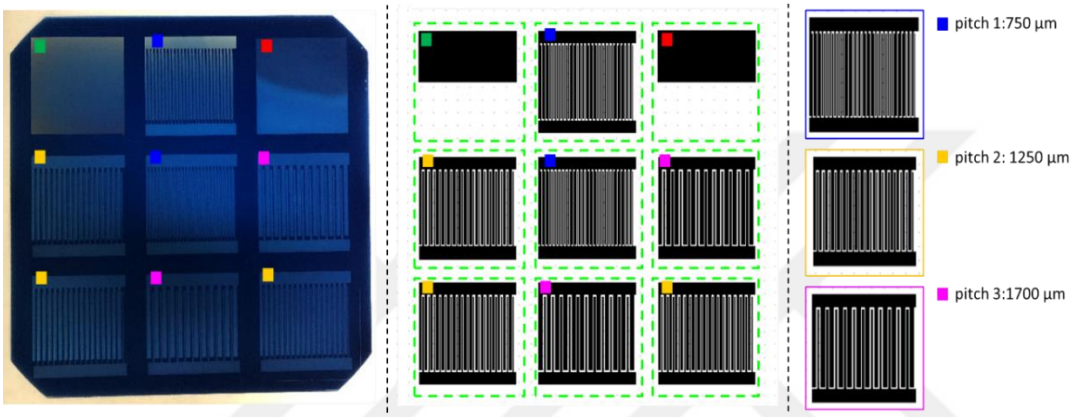


Figure 4.9. Appearance of a processed wafer after BCl_3 and $POCl_3$ diffusions and with SiO_2/SiN_x passivation stack (left), corresponding screen design (middle) and pitch values of small cells (right). Region(s) labelled with green square corresponds to emitter test pattern, red square corresponds to BSF test pattern; blue, yellow and pink squares correspond to cell regions with respective pitch values of 750, 1250, and 1700 µm.

Measured implied V_{oc} values measured over emitter and BSF test pattern after diffusion and passivation steps are shown in Figure 4.10 for both FFE and FSF structures. Implied Voc values of both emitter and BSF regions revealed that, cells with FSF show better performance compared to those with FFE. Moreover, iVoc values over emitter pattern regions were lower compared to those over BSF regions. Thus, we can deduce that the final cell performance would probably be limited by the inferior performance of the BCl_3 diffused emitter regions.

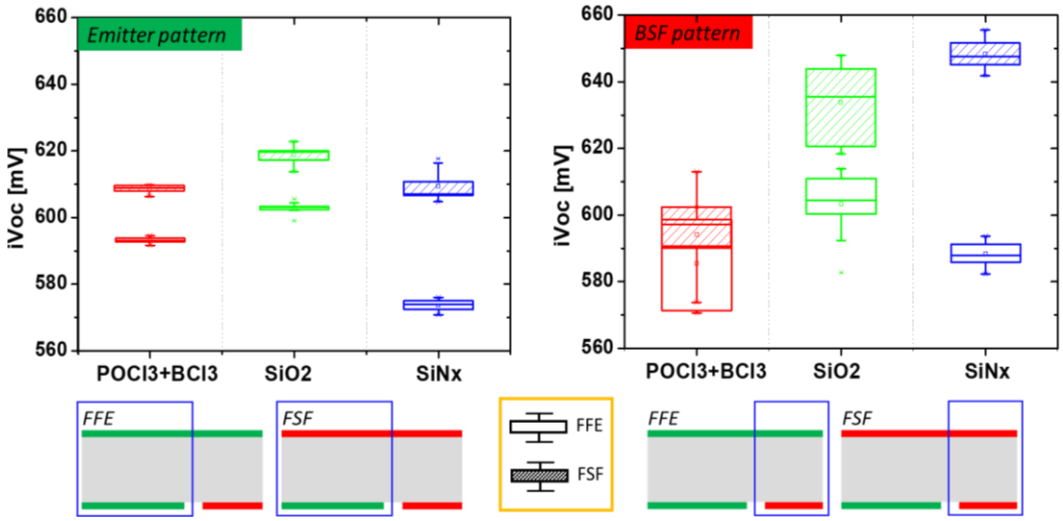


Figure 4.10. Change of iVoc values over emitter (left) and BSF (right) patterns for IBC structures with FFE and FSF. Empty boxes show IBC cells with FFE while hatched boxes show cells with FSF.

As seen in Figure 4.11 (left), cells with FSF show better performance compared to the cells with FFE. Putting a thin passivation SiO_2 layer to improve performances of both types while SiN_x layer results in a significant reduction in iVoc of cells with FFE.

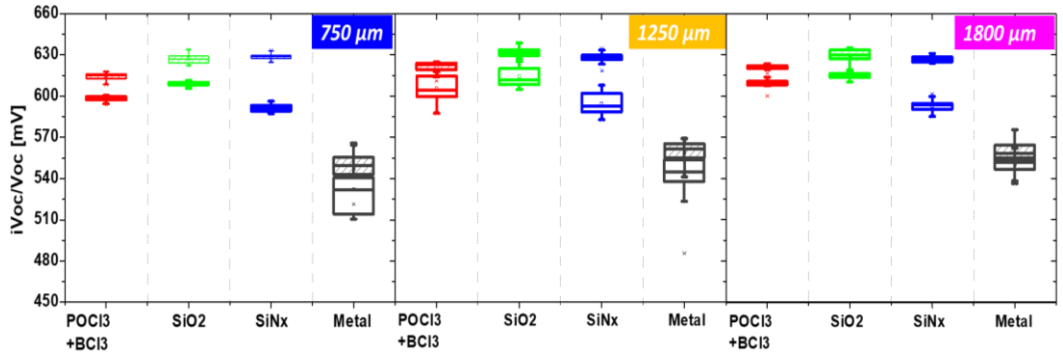


Figure 4.11. iVoc (till metallization step) and Voc (after metallization step) change of cells with FFE (empty boxes) and FSF (hatched boxes) for IBC cells with 750 (left), 1250 (middle) and 1800 µm (right) pitch. Results are averaged over 2 cells per each wafer.

Despite the difference of 30-40 mV in iVoc of both cell types, metallization and co-firing results in similar final values below 570 mV. At this stage, this significant drop could also be related to the reduced alignment tolerance due to small pitch.

For the case of moderate pitch (1250 μm) given in Figure 4.11 (middle), again cells with FSF show better performance compared to cells with FFE. Again, the metallization step significantly reduces the Voc at cell level but this time the average Voc was 559 mV (for FSF cells) while it was 552 mV for 750 μm pitch. For the case of the largest pitch, shown in Figure 4.11 (right), the average Voc at cell level was 561 mV which was slightly greater than that of the cell with moderate pitch. Although observed improvement could be the effect of changing cell geometry, this might also be the effect of suppressed misalignment as the cell pitch increases.

Considering the IBC cells with different pitches, we can deduce that the performance of the cells with FSF is superior compared to that of the cells with FFE. This could be related to the fact that the front and rear side BCl_3 diffusion was carried out simultaneously with the same boron recipe resulting in the same boron profiles at both sides. Thus, front side p^+/n junction provides a field effect as strong as that is provided by the rear side which reduces the collection probability of the holes at the rear emitter contacts. The next step will be to lightly dope the front side emitter while heavily doping the rear side.

In addition to the significantly degraded Voc upon metallization, depositing SiN_x on top thin SiO_2 layer was observed to reduce iVoc values. To trace the change in passivation quality, PL measurements were carried out throughout the whole process sequence. PL images of selected samples are shown in Figure 4.12.

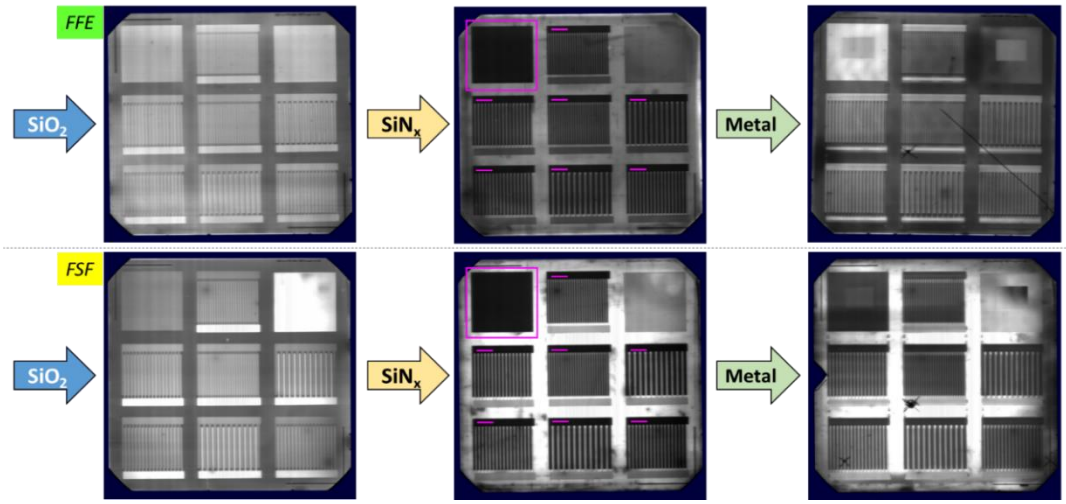


Figure 4.12. PL images of selected samples after each process step.

As seen in Figure 4.12, depositing SiN_x on top of SiO_2 layer reduces the PL signal intensity of BCl_3 doped regions which are labelled with pink squares and dashes. Moreover, drop in PL signal intensity is more pronounced for cells with FFE where front side of the samples are also boron doped. Thus, it can be concluded that the utilized SiN_x layer is not suitable to passivate the boron doped layers. Also, firing temperature was not optimized before and the cell suffered high series resistance. Thus, a detailed passivation study for boron doped regions and a firing study contacting of both boron and phosphorus doped regions is required as the future work.

Despite these problems, samples were carried till the cell level. After screen printing and firing steps, current – voltage measurements were carried out under flash tester with A.M. 1.5 G illumination. Cell parameters are analyzed according to different pitch values. For pitch:750 µm cells labelled as q2, q5, for pitch:1250 µm cells labelled as q4, q7, q9 and for pitch:1800 µm cells labelled as q6 and q8 are analyzed. For pitch: 750 µm cell region, q2 was not measurable due to misaligned metal patterns. Analyzed cell regions and corresponding graph legends are shown in Figure 4.13.

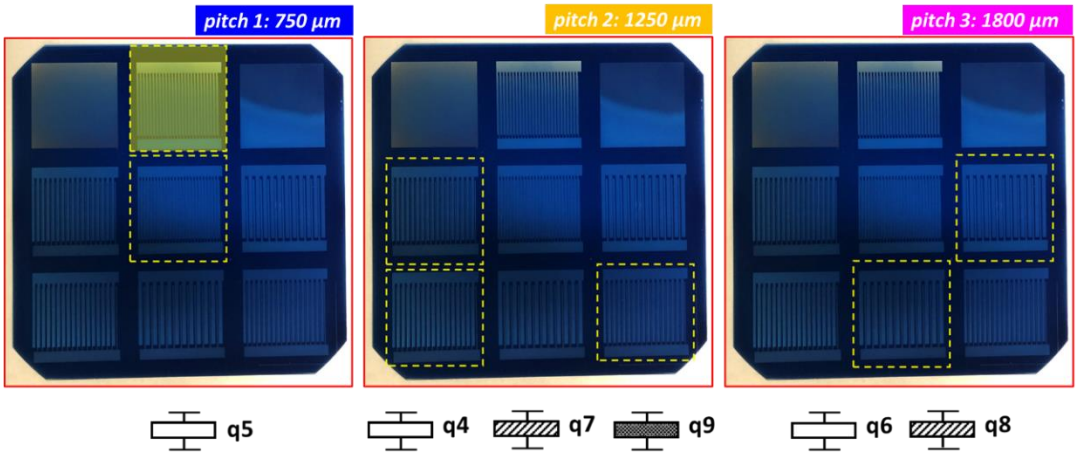


Figure 4.13. Analyzed cell region regions for pitch:750 µm (left), pitch: 1250 µm (middle) and pitch: 1800 µm (right) and corresponding graph legends.

For efficiency analysis of different cell regions for each pitch value, cells with FSF had higher efficiency values than cells those with FFE. Comparing the performances of the same cell geometries for different positions on the samples, there was no significant difference as seen in Figure 4.14.

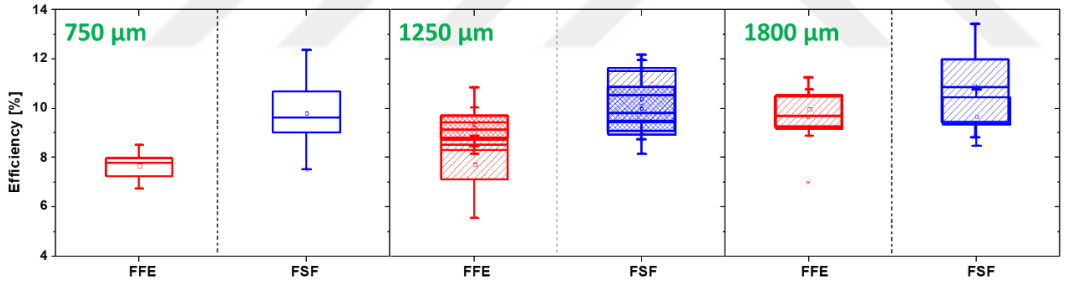


Figure 4.14. Efficiency values of IBC cells with FFE and FSF for different pitch values. Explanation of graph legends is given in Figure 4.13.

Increasing cell pitch results in an increase in average efficiency value both for the cells with FFE and FSF which is more pronounced for the former. The efficiency values were much lower than expected which could partially be related to improper contact formation resulting in low fill factor (FF) values.

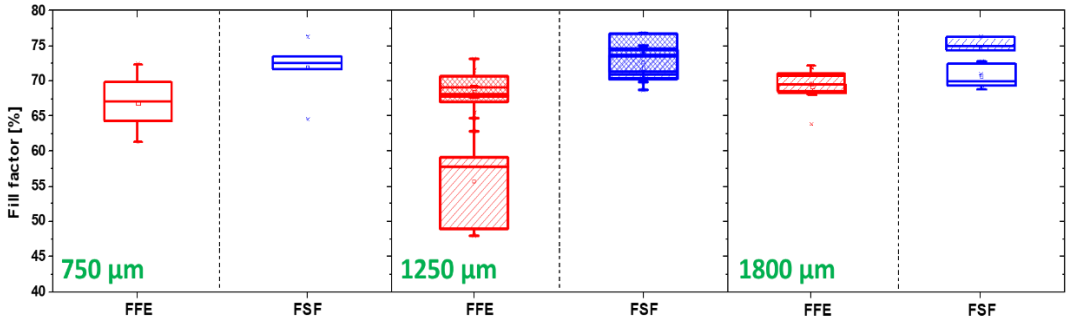


Figure 4.15. Fill factor values of IBC cells with FFE and FSF for different pitch values. Explanation of graph legends is given in Figure 14.

As shown in Figure 4.15, fill factor (FF) values were quite lower than generally obtained for industrial fire-through (FT) pastes. The first reason of low FF values is misaligned/partially misaligned region emitter and BSF regions. That alignment problem will be solved in the second version of the screen designs. The second reason is that there is no optimized firing recipe to co-fire FT-AgAl on BCl_3 diffused regions and FT-Ag paste on $POCl_3$ diffused regions.

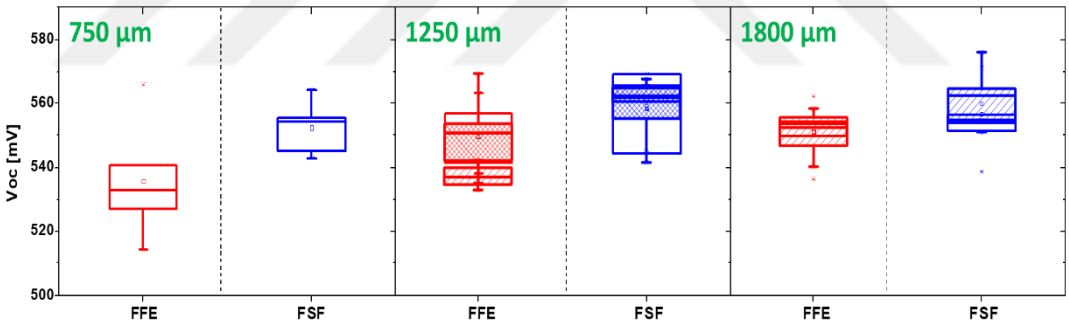


Figure 4.16. Open circuit voltage values of IBC cells with FFE and FSF for different pitch values. Explanation of graph legends is given in Figure 14.

Considering the open circuit voltage values, cells with FSF overperform those with FFE by 20-30 mV as seen in Figure 4.16. V_{oc} values increases as a function of increasing cell pitch. However, still the front surface doping concentration is required to be optimized for both FFE and FSF structures together with SiN_x layer.

As the final cell parameter, short circuit current density (J_{sc}) was analyzed as a function of cell pitch and shown in Figure 4.17. Despite slight increase in J_{sc} values as a function of increasing cell pitch, there was no clear trend.

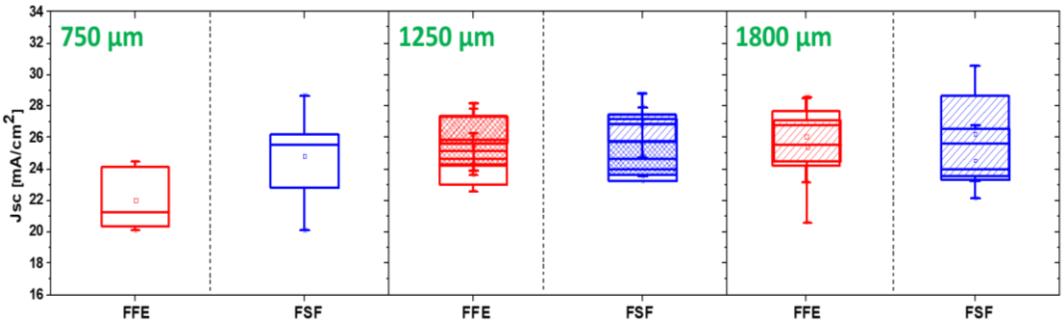
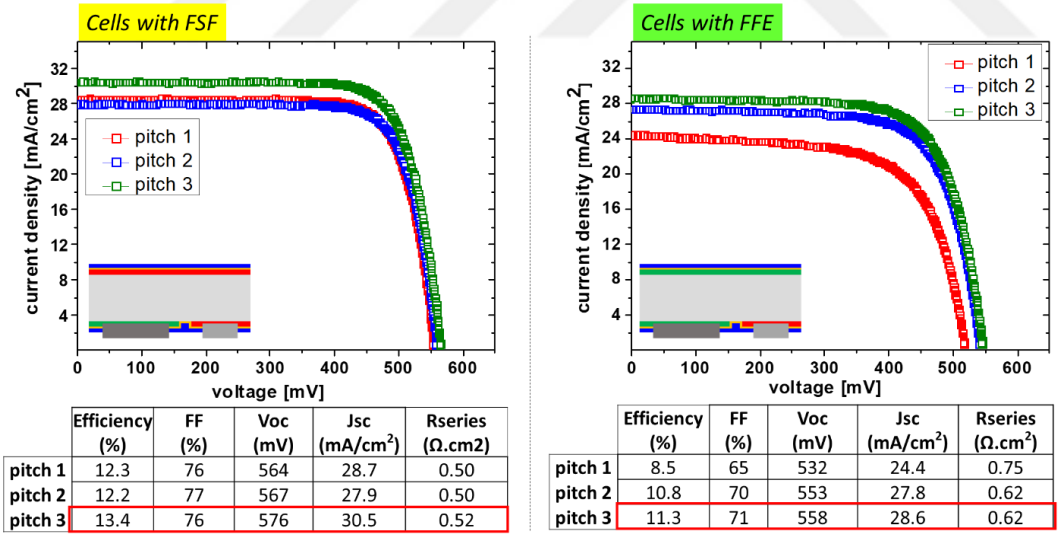


Figure 4.17. Short circuit current density values of IBC cells with FFE and FSF for different pitch values. Explanation of graph legends is given in Figure 14.

In Figure 4.18, current-voltage curves of best cells and corresponding cell parameters are given. For both FFE and FSF structures, pitch 3: 1800 µm performs superior compared to other pitches.



	Efficiency (%)	FF (%)	Voc (mV)	Jsc (mA/cm^2)	Rseries (Ω.cm2)
pitch 1	12.3	76	564	28.7	0.50
pitch 2	12.2	77	567	27.9	0.50
pitch 3	13.4	76	576	30.5	0.52

	Efficiency (%)	FF (%)	Voc (mV)	Jsc (mA/cm^2)	Rseries (Ω.cm^2)
pitch 1	8.5	65	532	24.4	0.75
pitch 2	10.8	70	553	27.8	0.62
pitch 3	11.3	71	558	28.6	0.62

Figure 4.18. Current-Voltage characteristics of best cells of each cell pitch of the cells with FSF (left) and FFE (right) with the corresponding cell parameters. Pitch 1, pitch 2 and pitch 3 refers to 750, 1250 and 1800 µm respectively.

It is observed that both cell types suffer high series resistance which reduces FF values and J_{sc} values in turn. The best cell of FSF structure has an efficiency of 13.4 % while that of FFE structure ends up with 11.3 % efficiency on the cell area of approximately 4 cm^2.

By the end of this study, it was confirmed that the suggested process flow was working properly with promising cell efficiencies. However, further optimization was required to improve V_{oc} and J_{sc}. For this, a detailed optimization study was carried out to improve not only the passivation but also the contacting properties of the diffused surfaces.

CHAPTER 5

OPTIMIZATION OF BORON AND PHOSPHORUS DIFFUSION PROCESSES

This chapter will focus on the detailed analysis of diffused surfaces to be used in IBC cells. Boron and phosphorus diffusion processes will be examined in terms of doping profiles, passivation, and contact formation properties. By the end of this chapter, BCl_3 and $POCl_3$ recipes would be optimized for both the contacted rear and non-contracted front junctions.

5.1 Introduction

As discussed in the literature section, doping of IBC cells could be done by different methods like ion implantation, the combination of implantation and diffusion, or solely diffusion. Also depending on the structure, the doped layers could either be deposited or directly obtained on the c-Si surface in a certain pattern as discussed in Chapter 2.

Using the suggested industry-compatible process flow, IBC cells fabricated within the scope of this thesis will only be obtained by high-temperature diffusion processes. Based on the primitive cell results obtained in the previous chapter, boron-doped surfaces were determined to be degrading upon firing, thus limiting the device performance. Although that effect could be due to the improper passivation layers, it could also be generated by the improper doping profiles. Thus, in this chapter optimization of boron diffusion especially for rear emitter will be focused on. Moreover, the front surface diffusion profile for both front floating emitter and front surface field cells will also be focused on. In addition to boron

diffusion, optimization of phosphorus diffusion for the rear side will also be studied within the scope of this chapter.

For boron diffusion, a reduced pressure BCl_3 furnace (Lydop^{TM}) from SEMCO Engineering was utilized. During the diffusion, N_2, BCl_3, and O_2 are the inlet gases while the process pressure is 400 bar, and the temperature is 935°C. During the diffusion process, the following reactions take place. While the first equation corresponds to the deposition step, the second one stays for the drive-in step [59].

i. Deposition step

In the deposition step, BCl_3 gas is fed to the system at a high temperature in the range of 900-960°C. Introducing O_2 gas to the system initiates the decomposition of BCl_3 via the following reaction equation [59].

$$2BCl_3(g) + \frac{3}{2}O_2(g) \rightleftarrows B_2O_3(s) + 3Cl_2(g) \qquad (Eq.5.1)[59]$$

Simultaneously as the decomposition of BCl_3, Si surface is also oxidized as a parallel reaction following Eq.5.2.

$$Si(s) + O_2(g) \rightleftarrows SiO_2(s) \qquad (Eq.5.2)[59]$$

The resulting mixture of B_2O_3 and SiO_2 is called boron silicate glass (BSG), and it will act as the boron source during the high-temperature annealing step.

ii. Drive-In step

At the contact of B_2O_3 with Si wafer surface, B_2O_3 will reduce to B as the doping element and SiO_2 through the following reaction.

$$2B_2O_3(s) + 3Si(s) \rightleftarrows 4B + 3SiO_2(s) \qquad (Eq.5.3)[59]$$

The side product of the first reaction which is Cl_2 would react with metal contaminants and produce volatile metal chlorides to be evacuated from the tube which is known as "*gettering effect*" [60]–[63].

The system used for the diffusion processes is shown in Figure 5.. Tube I is used for BCl_3 diffusion, Tube II is for oxidation, and Tube III is for $POCl_3$ diffusion. Tube IV is the direct plasma PECVD chamber and is used for SiN_x deposition.

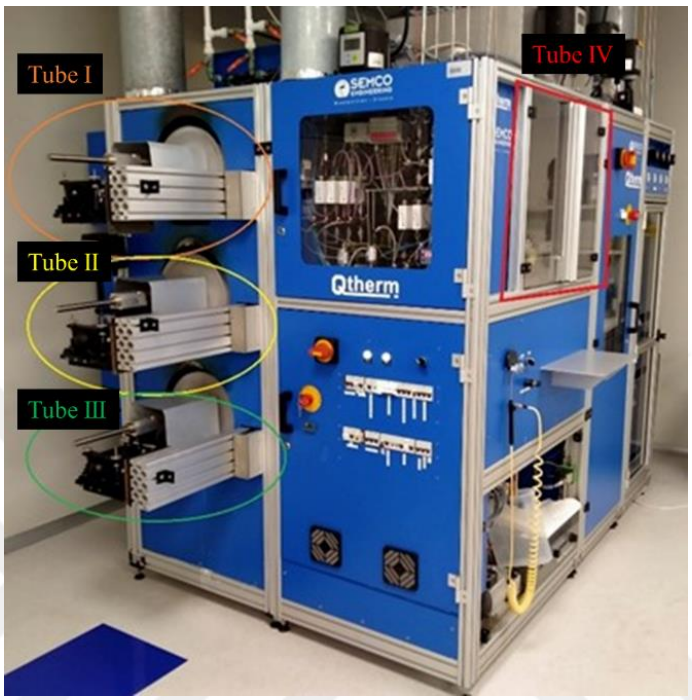


Figure 5.1. The compact system used for boron diffusion (1), oxidation (2), phosphorus diffusion (3), and PECVD SiNx deposition from SEMCO Engineering.

Like boron diffusion, phosphorus diffusion processes were also carried out in a reduced pressure $POCl_3$ furnace (Lydop^{TM}) from SEMCO Engineering as shown in Figure 5.1. During the diffusion process $POCl_3$, N_2 and O_2 are fed to the as reactants and the following reactions take place.

i. Deposition step

In the deposition step, $POCl_3$ decomposes at high temperature (>800°C) and reacts with O_2 to form P_2O_5 following the reaction given in Eq.5.4. Cl_2 gas is produced as the side product which would then react with metal contaminants and produces volatile metal halides to provide the gettering effect as in the case of BCl_3 diffusion.

$$4POCl_3(g) + 3O_2(g) \rightleftarrows 2P_2O_5(s) + 6Cl_2(g) \qquad (Eq.5.4)\ [2],[3]$$

Simultaneously as $POCl_3$ decomposes, Si wafer surface oxides following the reaction equation given in Eq.5.5

$$Si(s) + O_2(g) \rightleftarrows SiO_2(s) \qquad (Eq.5.5)[2],[3]$$

The reaction of P_2O_5 with SiO_2 generates phosphosilicate glass (PSG) following the reaction given in Eq.5.6 which will act as the dopant source in the high-temperature drive-in step.

$$P_2O_5(s) + SiO_2(s) \quad \rightleftarrows (P_2O_5)_x(SiO_2)_{1-x} \qquad (Eq.5.6)[2],[3]$$

ii. Drive-In step

In the drive-in step, PSG reacts with the Si surface and acts as the source of phosphorus.

$$2P_2O_5(s) + 5Si(s) \rightleftarrows 4P + 5SiO_2(s) \qquad (Eq.5.7)[2],[3]$$

For the passivation of the doped regions, SiO_2/SiN_x and Al_2O_3/SiN_x stacks were utilized. SiO_2 was grown via dry oxidation using Tube 2 shown in Figure 5.1 where O_2 was the inlet gas to the system for the case of dry oxidation and H_2 was additionally included for the case of pyrogenic oxidation. The followed dry oxidation reaction is given in Eq.5.8.

$$Si + O_2 \rightarrow SiO_2 \qquad (Eq.5.8)[66]$$

Unlike the SiO_2 layer, Si_3N_4 or SiN_x layer, in a more general definition, is deposited at temperatures below 400°C by plasma-enhanced chemical vapor deposition (PECVD) following the reaction given in Eq. 5.9.

$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2 \qquad (Eq.5.9)[67]$$

Depending on the inlet gas ratio SiH_4/NH_3, different SiN_x layers with different properties (i.e., refractive index, H content, etc.) could be deposited to passivate different regions with different doping profiles.

Al_2O_3 layer was deposited at 200°C using a spatial atomic layer deposition (ALD) system from SolayTech Corp. where trimethylaluminum (TMA) and water vapor (H_2O) are used as the gas phase precursors. The following SiN_x layers were deposited to cap the Al_2O_3 layer using an industrial direct plasma PECVD system from Don Guan Plasma Corp.

Metallization was the next step following the optimization of the doping profiles and passivation layers. For the optimization of the metallization step, fire-through silver (FT-Ag) and fire-through aluminum silver (FT-AgAl) pastes were screen printed on n^+ doped and p^+ doped regions, respectively. 1-D Transmission Line Method (TLM) was applied on an equidistant finger pattern to extract the corresponding contact resistivity (rho,co, or ρ_{co}). According to basic TLM theory, total resistance (R_T) between two contacts with the length of Z and the width of L is measured as a function of varying contact separation (d). Then, by plotting the R_T vs d plot, contact resistance (R_c), sheet resistance (R_{sh}) and transfer length (L_T) will be extracted [68], [69], [70]. The top view and cross-sectional view of the typical TLM contact design and an exemplary R_T vs. d plot are shown in Figure 5.2.

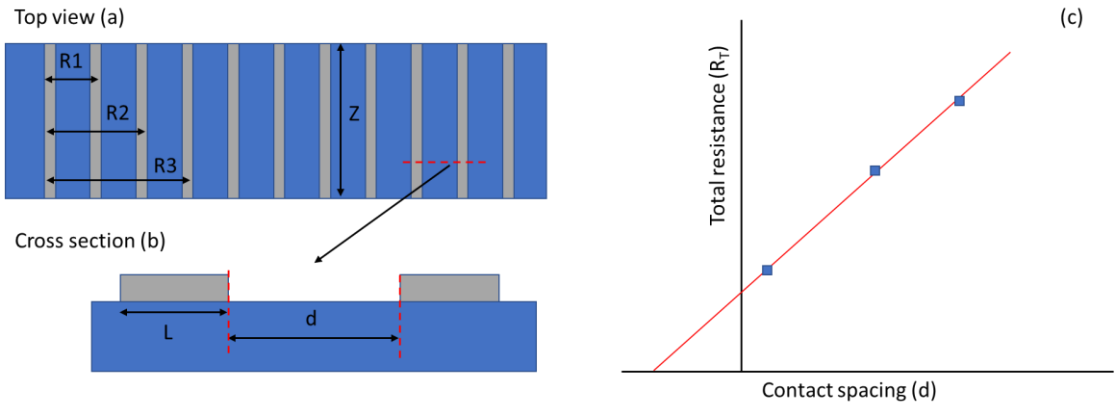


Figure 5.2. Top view (a), the cross-sectional view, (b) of a typical TLM structure, and fitted curve of total resistance versus contact spacing plot (c).

R_T stays for the summation of the contact resistance, the resistance of the metal, and that of the semiconductor which is expressed in Eq.5.10.

$$R_T = 2R_{contact} + 2R_{Metal} + R_{semiconductor} \qquad (Eq.5.10)[69], [70]$$

R_{Metal} is negligible compared to $R_{contact}$, and the slope of the fitted plot is related to R_{sheet} via Eq.5.11 where R_{sheet} is denoted as R_{sh}.

$$Slope = \frac{\Delta R_T}{\Delta d} = \frac{R_{sh}}{Z} \qquad (Eq.5.11)[69], [70]$$

The Transfer Length which is an important figure of merit to characterize contacting properties is defined as in Eq.5.12.

$$L_T = \sqrt{\rho_{co}/R_{sh}} \qquad (Eq.5.12)[69], [70]$$

R_c is extracted from the y-axis interception ($2R_c$) and L_T is obtained from the x-axis interception ($-2L_T$). Then, the contact resistivity is obtained using Eq.13.

$$\rho_{co} = R_c L_T Z \qquad (Eq.5.13)[69], [70]$$

By TLM measurements, variation in ρ_{co} as a function of underlying doping profiles and applied peak firing temperature would be investigated and then applied at the cell level.

5.2 Experimental Details

After the optimization of diffusion barrier properties and etch resist-based patterning procedure, the first set of IBC cells were fabricated using 1-3 Ω.cm, n-type wafers following the process sequence given in the previous sections. With the help of successive measurements throughout the whole process sequence, a degradation in the device performance was recognized. To solve the experienced degradation in the device performance upon metallization and firing, it was required to re-visit the optimization of doped regions. Both boron and phosphorus-doped regions were focused on in terms of diffusion profiles, passivation, and contacting properties for re-optimization.

5.2.1 Effect of Post-Oxidation Step

In the first part of the boron optimization studies, the BCl_3 recipe was aimed to be re-arranged to have proper implied V_{oc} (iV_{oc}) levels on n-Cz wafers together with good contacting properties. For this, three different post oxidation processes were applied to remove the boron-rich layer (BRL) and borosilicate glass (BSG). Based on the first optimization studies (not reported here), deposition was carried out at 937°C under BCl_3: 50sccm for 15 minutes, and the drive-in was carried out at the same temperature under O_2: 600sccm for 33 minutes for all recipes. While recipe B1 includes additional dry oxidation at 850°C (pass3), B2 stands for pyrogenic oxidation at 850°C (LTOnew), and B3 samples were exposed to an RCA-2 (HCl: H_2O_2) cleaning step at 80°C following the diffusion process.

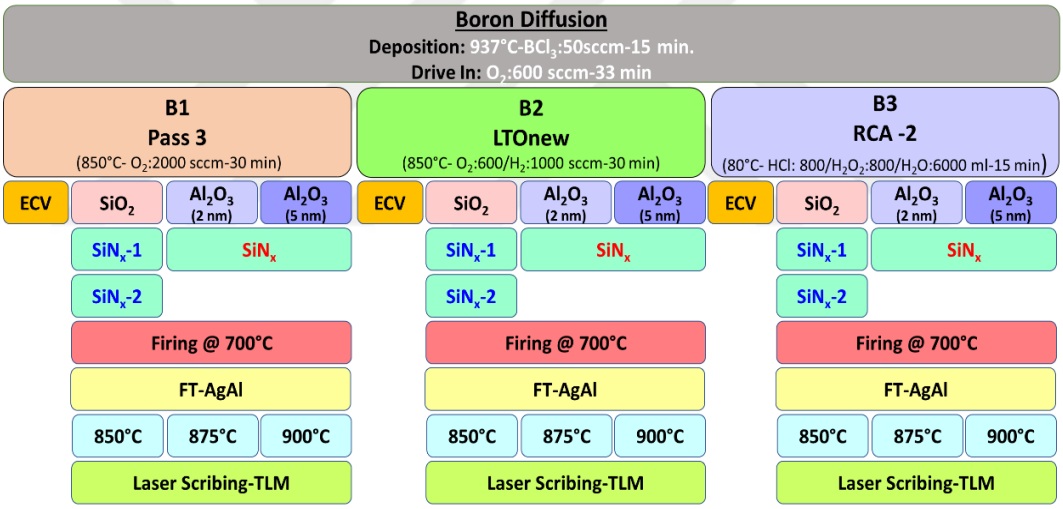


Figure 5.3. Design of Experiment for BCl_3 Diffusion

Following the diffusion and post-cleaning processes, samples were passivated using four different stack configurations: 2 nm Al_2O_3/SiN_x, 5 nm Al_2O_3/SiN_x, SiO_2/SiN_x (recipe1), and SiO_2/SiN_x(recipe2). While SiO_2 was thermally grown at 850°C under O_2:1000 sccm flow, SiN_x recipes 1 and 2 are deposited with SiH_4: 135/NH_3: 1088sccm (Sirich) and SiH_4: 80/NH_3: 1222sccm (Sirich3) respectively. The lifetime sample of each group was exposed to a firing step while TLM samples were metalized with FT-AgAl paste and fired at 850, 875, and 900°C, respectively.

After the firing, samples were cut into 1-cm strips and used for TLM measurement using an equidistant probe head. The corresponding experimental design is shown in Figure 5.3.

5.2.1.1 Separating BCl_3 Recipes for the Contacted and Non-contacted Emitter Regions

In the following part of the studies, optimization of BCl_3 diffusion was carried out with a motivation to separately obtain a proper rear and front emitter for IBC solar cells unlike the case of the primitive cells where the front and rear surfaces were diffused simultaneously. While the rear emitter was required to have a certain doping concentration to properly separate and collect the generated charge carriers, the front side doping concentration was aimed to be kept as low as possible for superior surface passivation. For this, three different recipes were designed, two of which were for rear emitter (i.e., heavy, and light diffusion) and one for front emitter (front floating emitter). For the optimization of diffusion recipes, textured, n-Cz and p-Cz test samples were used. In addition to the test samples, textured, n-type wafers were included initiate patterning processes of the cell fabrication sequence. While test samples were used for 4PP, ECV, Sinton PCD, and TLM measurements, the remaining samples were used for patterning and diffusion steps for the cell fabrication. After analyzing the results of the test samples, optimized recipes would be combined to fabricate the cell structure which will be discussed in the following sections.

5.2.1.2 Optimization of Phosphorus Diffusion

For the case of $POCl_3$ optimizations, three different recipes were applied to generate three different doping profiles. While P1 was derived from a 50 Ω/□ recipe (P0) which had been used for the emitter region of Al-BSF cells, P2 and P3 were derived to generate lower doping concentrations at the surface concerning P1.

While the P1 recipe was obtained by adding an ex-situ oxidation step to the P0 recipe, P2 was derived by applying an additional in-situ oxidation step to P0. Short dry oxidation was applied for the case of P1 where PSG was stripped before the oxidation step. On the contrary, PSG was intact during in-situ oxidation of P2 recipe. Moreover, a small amount of hydrogen was also introduced to the system during the oxidation step so that the oxidation was not dry but was a pyrogenic oxidation step. The expected oxidation rate was greater in the latter case. Finally, for the case of P3, the total drive-in time was reduced to 30 minutes which was 41 minutes for the case of P1 and P2. Following the glass removal and necessary cleaning steps, samples were passivated using a SiO_2/SiN_x stack while SiO_2 was grown by dry oxidation step, SiN_x layers were deposited using a PECVD system. The corresponding experimental design is shown in Figure 5.4.

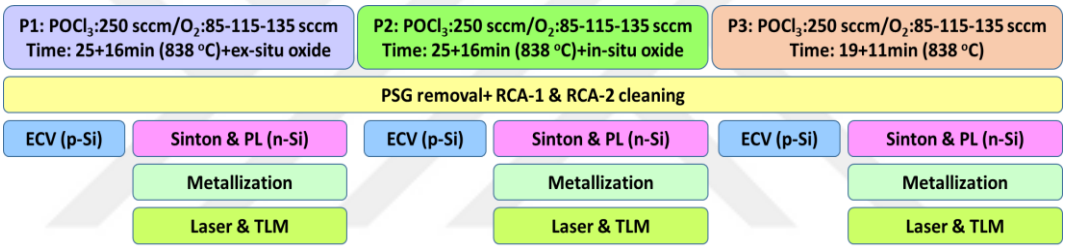


Figure 5.4. Design of Experiment for the Optimization of $POCl_3$ Recipe.

ECV, Sinton Lifetime, and PL imaging methods were applied to characterize the fabricated samples. As the last step, the metallization of the symmetrically diffused samples was carried out using industrial FT-Ag paste and the contact formation was achieved by the high temperature firing step. Following the metallization, the samples with screen-printed metal on one side were cut into 1-cm width stripes and used for TLM measurements.

5.2.1.3 Application of Optimized Recipes at the Cell Level

After optimizing the front and rear diffusions separately, the next step was to combine everything in the final device fabrication.

The experimental design for the IBC set is given in Figure 5.5.

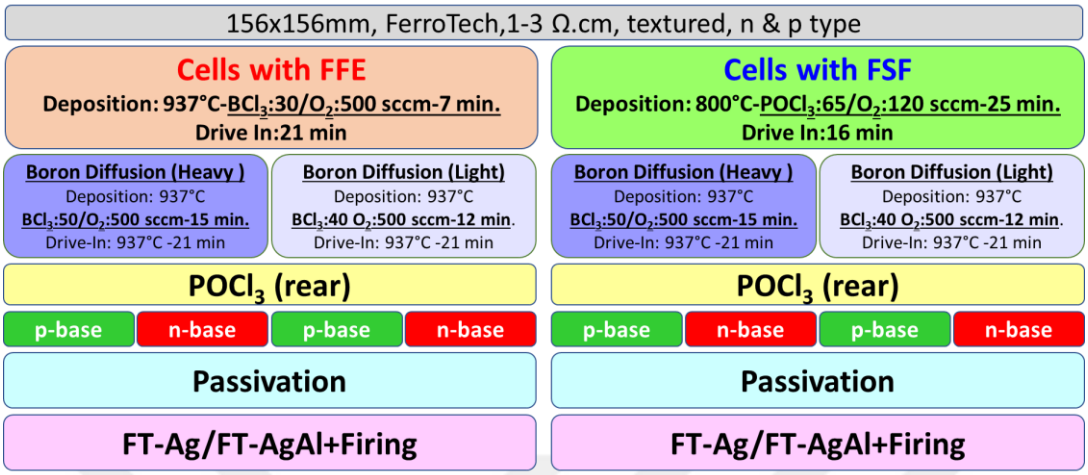


Figure 5.5. Design of Experiment for the 2nd IBC Split.

Based on the first part of this study, the LTOnew recipe was used for the oxidation of boron-doped regions before BSG removal. During the cell fabrication processes, the rear side was selectively boron-doped through the patterned diffusion barrier. Then, a thick SiN_x layer was deposited on top, before the diffusion of the front side. After the front side diffusion, either with boron or phosphorus, SiN_x from the rear side was stripped, and then the samples were exposed to short pyrogenic oxidation at low temperature with the selected recipe LTOnew for the case of cells with FFE. For the case of the cells with FSF, the front surface would only be exposed to $POCl_3$ diffusion after the boron diffusion of the rear side. As the last diffusion step, both the front side and rear side of the samples were capped with the diffusion barrier where the latter layer would be patterned for the BSF region. After the necessary cleaning and glass stripping steps, samples were passivated with SiO_2/SiN_x stack and then metalized using industrial FT-Ag and FT-AgAl pastes.

5.3 Results and Discussions

5.3.1 Optimization of Boron Diffusion for Modified Screen Design

5.3.1.1 Effect of Post-Oxidation Step

For the case of BCl_3 optimization, following the deposition and drive-in steps at 937°C, dry oxidation, pyrogenic oxidation, or wet chemical oxidation was carried out for respective sample sets of B1, B2, and B3. The sheet resistance values were measured over 9 points per wafer by the 4PP method and the results are shown in Figure 5.6. Wafers were symmetrically doped, and no significant difference was observed between the front and rear sides.

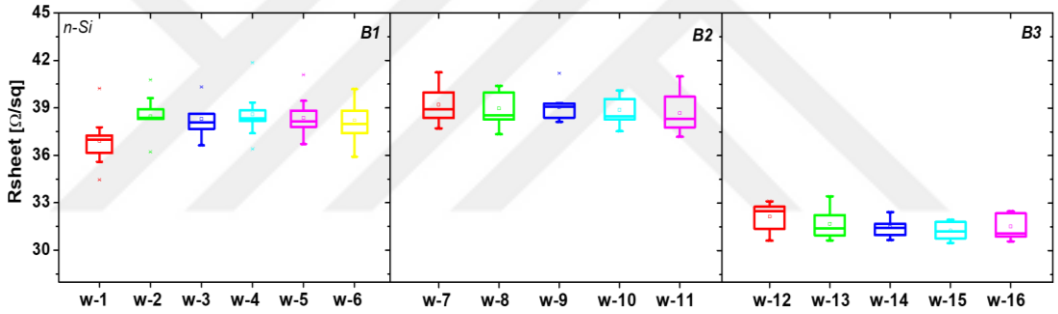


Figure 5.6. Measured sheet resistance values on n-Si for B1, B2, and B3 recipes.

In Figure 5.6, high temperature dry and pyrogenic oxidation recipes namely B1 and B2 were observed to result in similar sheet resistance values at around 40 Ω/□. Wafer to wafer uniformity was quite acceptable as well as the uniformity throughout each wafer. B3 recipe where RCA-2 was applied as the oxidation step resulted in significantly lower sheet resistance values compared to the other recipes whose reason would be then explained by ECV measurements. Despite the improved uniformity, obtained sheet resistance values were quite lower than desired for a typical emitter layer.

For the case of p-Si where the boron-doped region acts as a BSF region, measured sheet resistances were lower than those measured on n-Si. Measured sheet

resistance values on p-Si for three different recipes are given in Figure 5.7. As in the case of n-Si, B1 and B2 recipes resulted in similar sheet resistance values for p-Si at around 20 Ω/□ while B3 recipes resulted in lower sheet resistances at around 17 Ω/□. Again, wafer to wafer uniformity was quite good for all recipes.

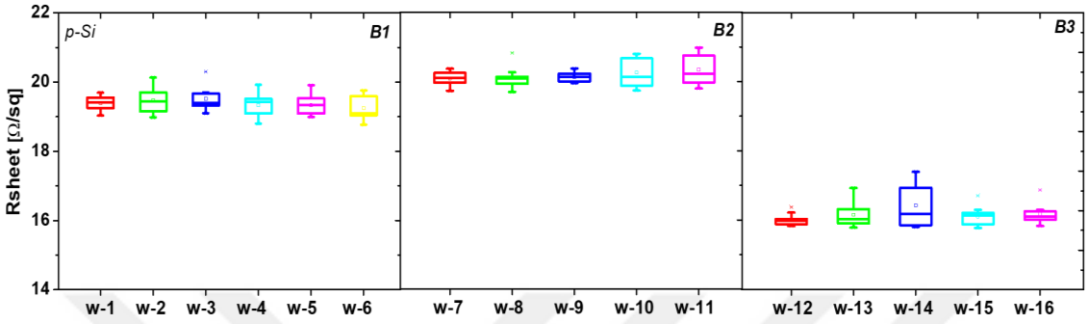


Figure 5.7. Measured sheet resistance values on p-Si for B1, B2, and B3 recipes.

Following the 4PP measurements, ECV measurements were carried out to visualize the doping profile as a function of etching depth. ECV measurements were carried out only for n-Si wafers and corresponding results are shown in Figure 5.8.

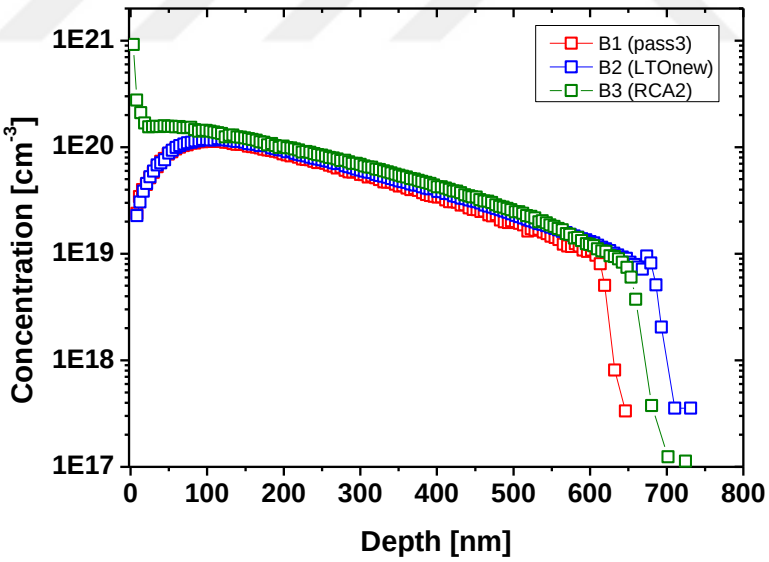


Figure 5.8. ECV profiles of boron diffused n-Si samples for B1, B2, and B3 recipes

B1 (pass3) and B2 (LTOnew) recipes were observed to have similar doping concentrations with a slightly deeper junction for B2. B3 recipe showed a great

jump in the boron concentration in the first 120 nm beneath the surface which is so-called "*boron-rich layer (BRL)*" could explain lower sheet resistance values compared to other recipes. This existing boron-rich layer (BRL) could be beneficial in terms of surface passivation and contact resistivity since the field effect provided by the doped layer would be enhanced. However, the BRL layer could also end up with the loss of surface passivation upon high-temperature processes like firing which would be examined by successive Sinton PCD measurements.

Considering the different passivation sceneries, Al_2O_3/SiN_x stack was expected to have superior performance with the help of stored negative charges in the Al_2O_3layer which would provide enhanced field-effect passivation compared to the other layers [71]–[75]. For the case of Al_2O_3/SiN_x stack on n-Si, 2 nm Al_2O_3 was observed to have a detrimental effect on iV_{oc} both in as-deposited and after firing cases Figure 5.9 (left). Despite the B2 recipe starting at 630 mV level which is 20 mV above that for B1 and 40 mV above that for B3, after firing, all recipes ended up with almost the same iVoc level.

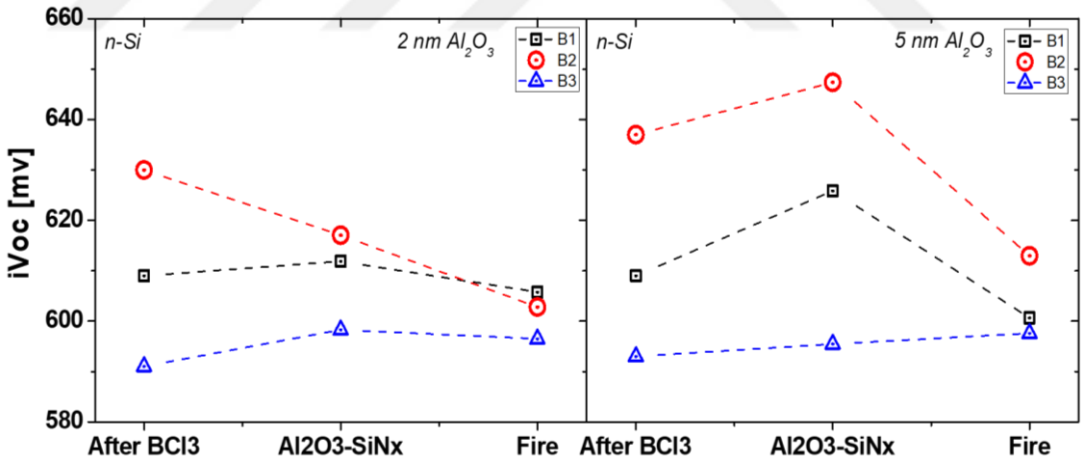


Figure 5.9. Change in iVoc of the boron-doped n-Si-based samples passivated by 2 nm (left) and 5 nm (right) Al_2O_3/SiN_x stack layers.

For the case of 5 nm Al_2O_3/SiN_x, deposition of passivation stack increases iV_{oc} of samples from B1 by 7-8 mV, while this increase was around 13-14 mV for the

samples from B2. However, the firing still had a negative effect on the passivation quality which will be examined in detail in a separate study.

Unlike the case of n-Si, for the case of p-Si, both 2 nm and 5 nm Al_2O_3/SiN_x stack could have passivated all recipes. However, the firing step had again an adverse effect of the iVoc of the passivated samples. The stack layer with 2 nm Al_2O_3 increased iV_{oc} from 580 to 625 mV level for B1 and B2 recipes which was approximately 612 mV for B3 split as given in Figure 5.10 (left).

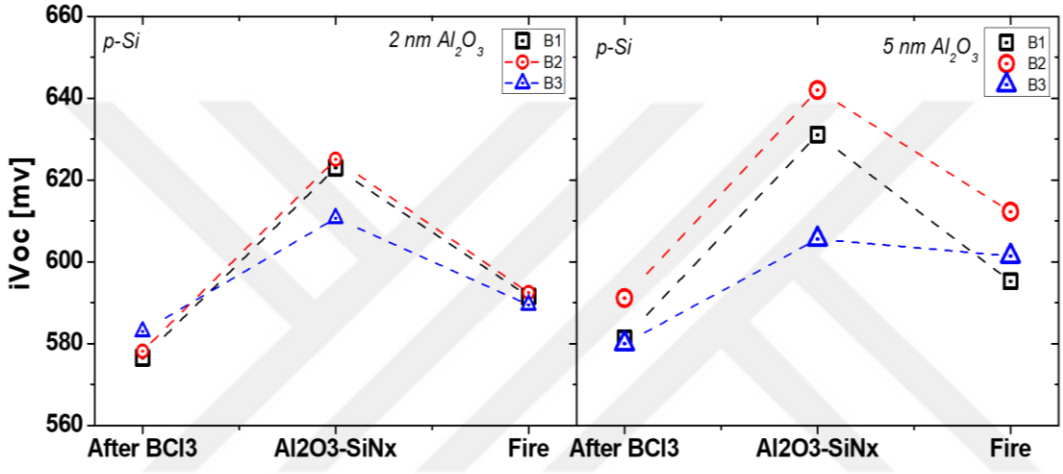


Figure 5.10. Change in iVoc of boron-doped p-Si based samples passivated by 2 nm (left) and 5 nm (right) Al_2O_3/SiN_x stack layers.

For the case of stack layer with 5 nm Al_2O_3, the improvement in the iVoc was more pronounced compared to that with 2 nm Al_2O_3 (Figure 5.10 (right)). The improvement was around 50 mV for B1 and B2 recipes while it was around 25 mV for the B3 recipe. B3 recipe samples were almost un-passivated with Al_2O_3/SiN_x stack when the bulk was n-Si. However, when the base material was switched to p-Si, the stack layer could have properly passivated the boron diffused surface. However, firing has again a detrimental effect for all samples.

As another passivation scenario, SiO_2/SiN_x stack passivation was applied where 5-6 nm thick SiO_2 layer was kept constant and the composition of the SiN_x was varied so that one layer would be richer in Si content compared to the other layer. The first SiN_x recipe was named Sirich and deposited with the process gas ratio of

SiH_4:135/NH_3:1088 sccm resulting in a refractive index of 1.92 at 632 nm while the second recipe was named Sirich3 deposited with the ratio of SiH_4:80/NH_3:1222 sccm with the resulting refractive index of 1.89 at 632 nm.

Considering the iV_{oc} values of SiO_2/SiN_x stacks with Sirich and Sirich3 on n-Si, oxidation itself was significantly degrading samples of B1 and B2 recipes while B3 recipe samples stayed still (Figure 5.11 (left)). This stable behavior during oxidation could be related to the high boron concentration at the surface of the B3 recipe which was significantly higher than that of B1 and B2 recipes. While any additional oxidation would further reduce the boron concentration at the surface of B1 and B2 samples, it would only partially reduce the concentration of the BRL layer of B3 samples which was already rich in boron.

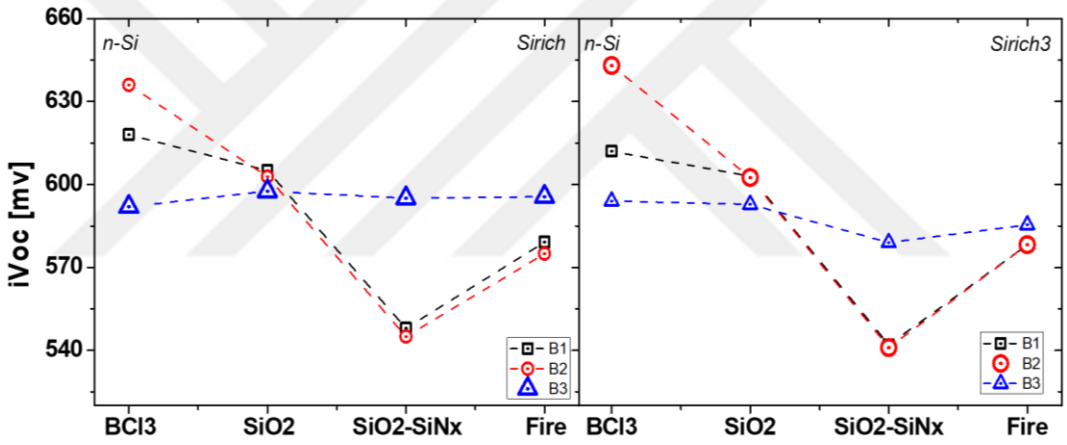


Figure 5.11. Change in iVoc of boron doped n-Si based samples passivated by SiO_2/SiN_x (Sirich) (left) SiO_2/SiN_x (Sirich3) (right) stack layers.

Deposition of SiN_x layer further reduced iVoc of group B1 and B2 sample while samples of B3 recipe had the same or slightly reduced iV_{oc} values. Moreover, no significant difference between samples of Sirich and Sirich3 recipes was observed. Unlike the Al_2O_3/SiN_x, SiO_2/SiN_x samples shows an enhancement in iV_{oc} upon firing. However, the resulting iVoc values were still much lower than expected. Thus, it could be deduced that none of the utilized SiN_x layers is suitable to passivate p^+ doped regions.

For the case of p-Si based samples, the trends were like those obtained for n-Si based samples for B1 and B2 recipes (Figure 5.12). For the samples of the B3 recipe, oxidation resulted in an unexpected enhancement in the iV_{oc}, which is reduced to the same level as the samples of B1 and B2 recipes after SiN_x deposition.

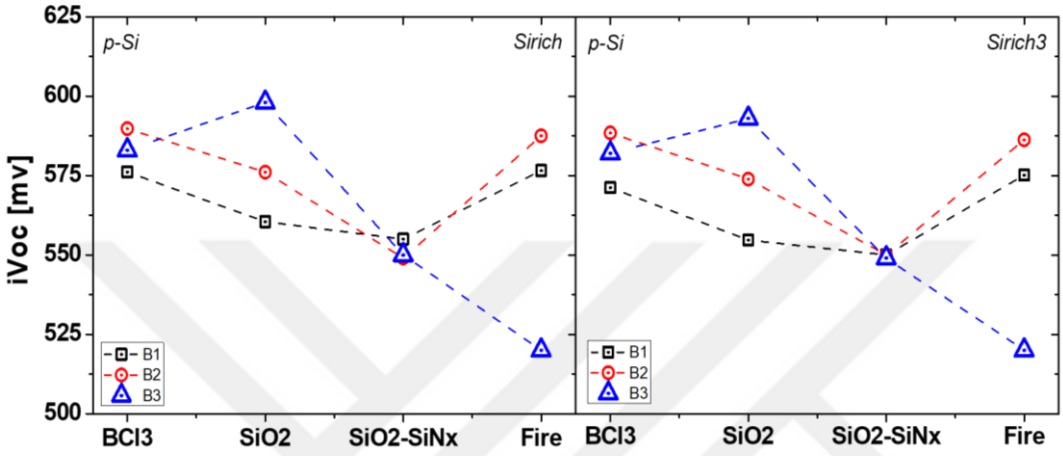


Figure 5.12. Change in iVoc of boron doped p-Si based samples passivated by SiO_2/SiN_x (Sirich) (left) SiO_2/SiN_x (Sirich3) (right) stack layers.

Upon firing, samples of the B3 recipe were the most severely degraded amongst the other samples for the case of p-based samples. Considering all iVoc results both on n-Cz and p-Cz samples, it was observed that the surface concentration should be increased to a certain extent. However, the existence of the BRL layer is resulting in severe degradation upon firing which is more pronounced when the p-Cz base is used. This degradation upon firing is expected since BRL and BSG layers are known as active recombination sites due to inactive boron, segregated metal impurities and structural defects [76], [77]. Thus, the dopant concentration should be increased while the BRL layer is completely removed for a proper and stable passivation performance.

In addition to iV_{oc} and R_{sheet} measurements, the samples were also traced by PL measurements throughout the process flow. Considering the PL images shown in Figure 5.13, the signal level reduced after firing for the samples passivated with Al_2O_3/SiN_x stack and the traces of the firing furnace's conveyor belt became

visible. Moreover, some small dark spots became visible which were also visible to the naked eye.

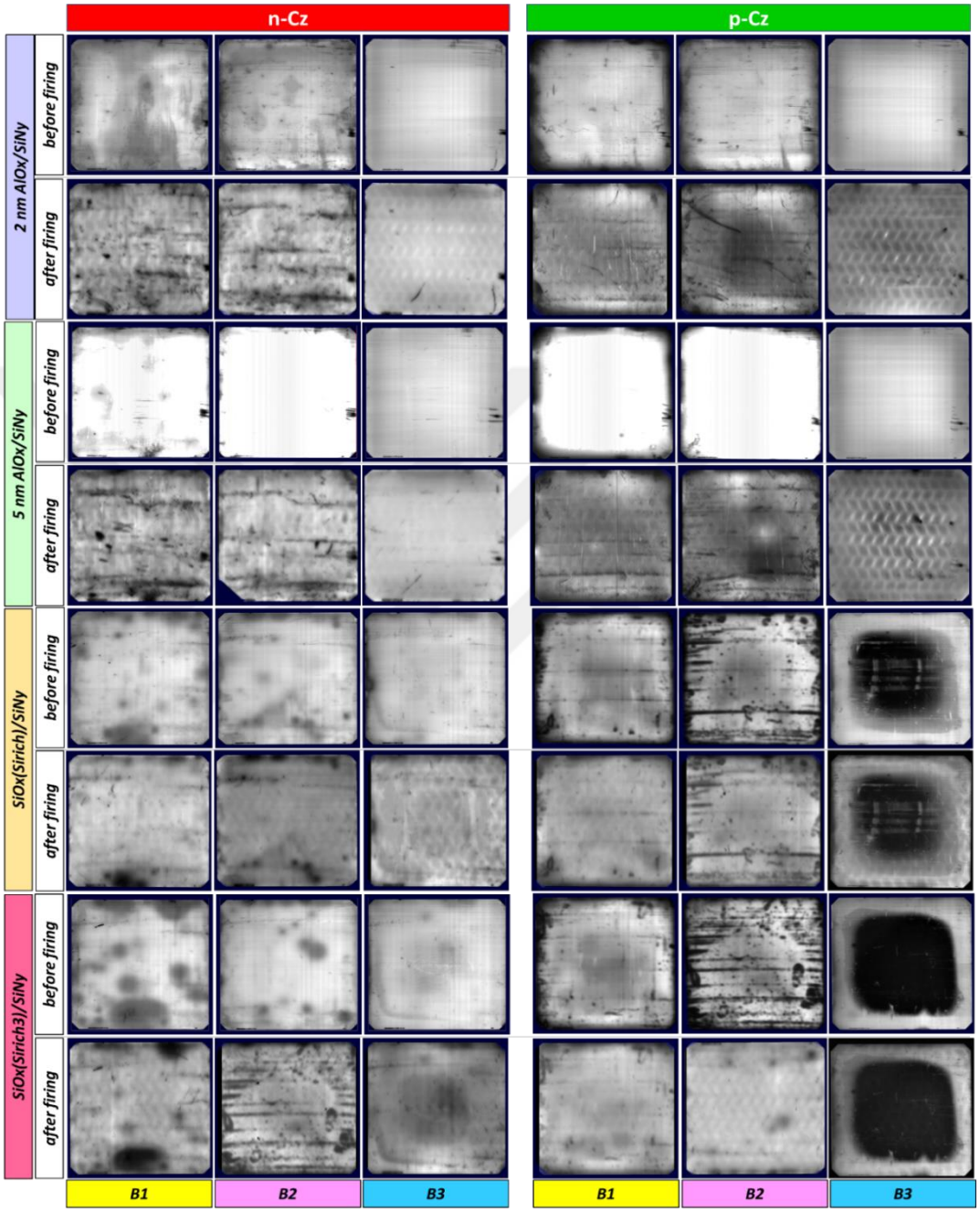


Figure 5.13. Photoluminescence images of selected samples for each process group. Selected samples were traced before and after firing conditions for all passivation sceneries of three boron diffusion recipes both on n-Si and p-Si wafers.

That issue is related to the blistering effect due to the excess amount of hydrogen provided by the deposited Al_2O_3 and SiN_x layers. The hydrogen stored in the deposited layers would diffuse towards the c-Si interface upon high temperature annealing and result in the local delamination of the film so that the unwanted blisters would be formed [78]–[80]. Saturated PL images obtained for the 5 nm Al_2O_3/SiN_x stack are in good agreement with the higher iVoc values compared to those of samples passivated 2 nm Al_2O_3/SiN_x layer before firing. The p-Si-based samples were observed to suffer dead regions for the B3 recipe for all passivation sceneries which were more pronounced for the case of SiO_2/SiN_x stack passivation. Those observed dead regions also confirms the remaining BRL layer on the surface [76], [77], [81].

That visualized dead region could confirm the drastic change in iV_{oc} after SiN_x deposition and firing. The traces of the conveyor belt were visualized for almost all samples after firing. That negative effect of firing could be solved by changing the temperature profile of the firing recipe or a thermal treatment at a lower temperature between 400-600°C before firing could also be beneficial.

As the next step, TLM samples were metallized using fire-through (FT) AgAl paste and activated at different temperatures. Analyzed contact resistivity values for samples passivated with 2 nm Al_2O_3/SiN_x shown in Figure 5.14. It was observed that both n-Cz and p-Cz samples were well contacted with the screen-printed FT-AgAl paste. Even at the lowest temperature of 850°C, the obtained contact resistivity was below 6.5 $m\Omega.cm^2$. Considering the previous BCl_3 study (not shown here), contact resistivity values were within the range of 15-20 $m\Omega.cm^2$ on n-Cz which was below 10 $m\Omega.cm^2$ for p-Cz. This improvement could be related to modified boron recipes. In the previous run, the peak boron concentration was varying between 5.2-5.6x10^{19} cm^{-3} while in this set it is around 1x10^{20} cm^{-3}. Increasing peak concentration significantly facilitates contact formation. Moreover, B3 recipes resulted in lower rho,co values compared to the B1 and B2 recipes which could be related to the BRL region with a corresponding peak concentration of 1x10^{21} cm^{-3} at the surface.

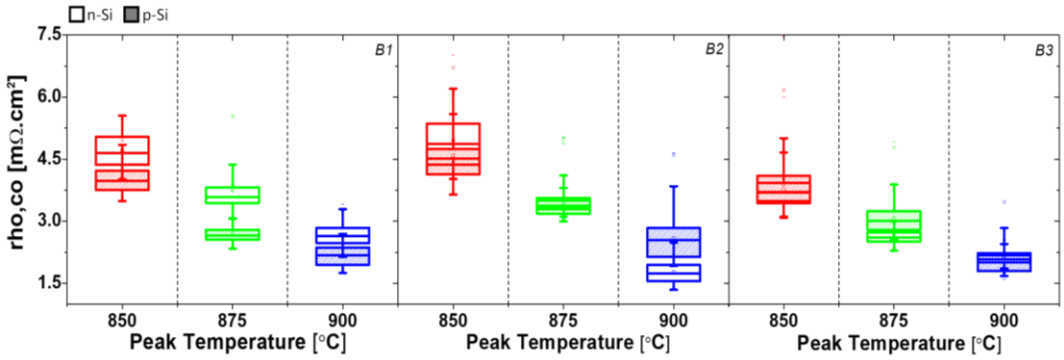


Figure 5.14. TLM results for 2 nm Al_2O_3/SiN_x passivated samples from B1 (left), B2 (middle), and B3(right). Empty boxes are for n-Cz, dashed patterns are for p-Cz samples**.**

For the case of 5 nm Al_2O_3 Al_2O_3 layer in Al_2O_3/SiN_x stack, no significant change in rho,co was observed as shown in Figure 5.15. A similar trend as in the case of 2 nm Al_2O_3 was observed for 5 nm Al_2O_3 case and the rho,co values were still below 6.5 $m\Omega.cm^2$ even for the lowest firing temperature of 850°C.

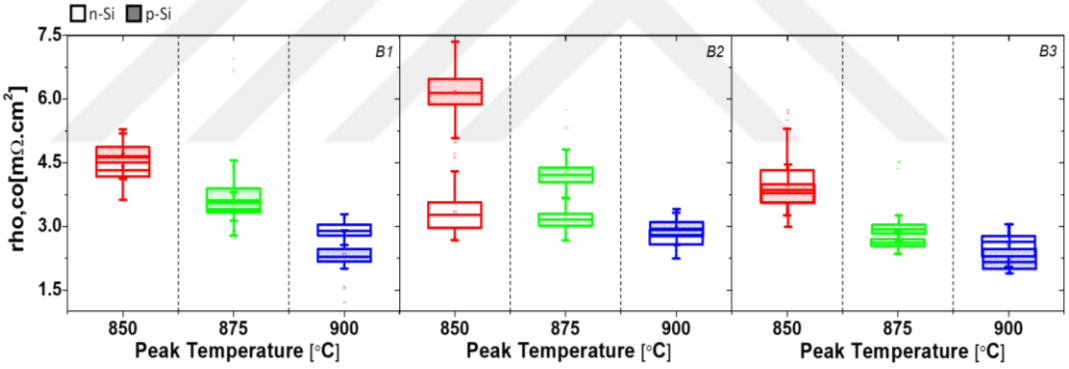


Figure 5.15. TLM results for 5 nm Al_2O_3/SiN_x passivated samples from B1 (left), B2 (middle), and B3(right). Empty boxes are for n-Cz, dashed patterns are for p-Cz samples.

For SiO_2/SiN_x (Sirich) passivation, measured rho,co values were quite similar to those obtained for Al_2O_3/SiN_x layers. TLM results are given in Figure 5.16.

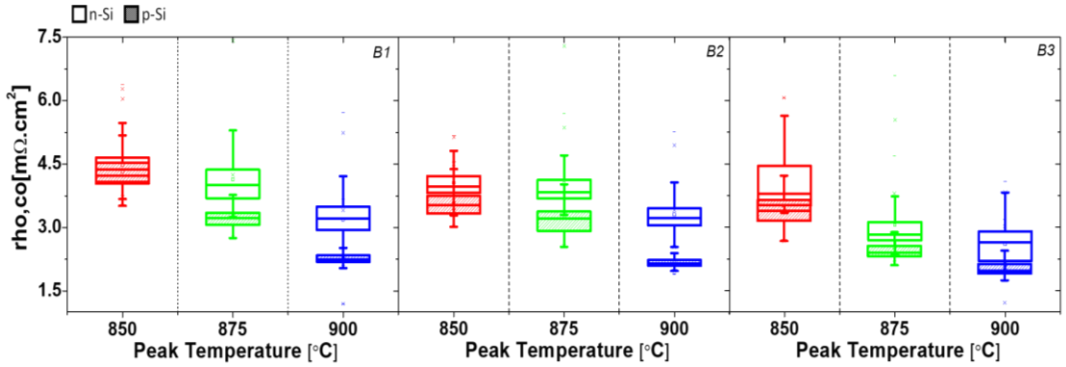


Figure 5.16. TLM results for SiO_2/SiNx (Sirich) passivated samples from B1 (left), B2 (middle) and B3(right). Empty boxes are for n-Cz, dashed patterns are for p-Cz samples.

Measured rho,co values of the B3 group were also similar to those obtained for B1 and B2 recipes.

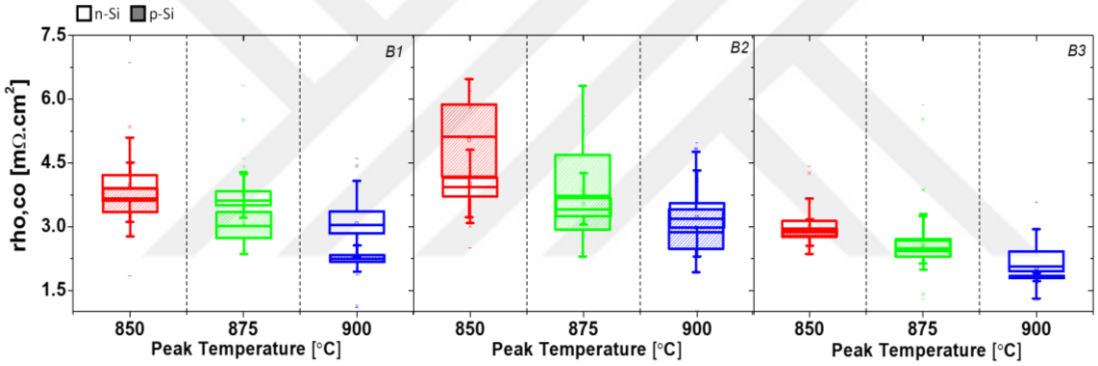


Figure 5.17. TLM results for SiO_2/SiN_x (Sirich3) passivated samples from B1 (left), B2 (middle) and B3(right). Empty boxes are for n-Cz, dashed patterns are for p-Cz samples.

To sum up, to have proper contact formation using FT-AgAl pastes, a certain amount of active dopant concentration at the surface is needed. However, the effect of inactive dopants is not fully understood yet. Comparing the previous and current studies, it could be deduced that the required doping level is above $5.6x10^{19}$ cm^{-3}. Keeping the BRL layer at the surface (B3) further reduces the rho,co values but considering the iVoc losses for that group, it would be more beneficial to strip the BRL layer.

5.3.1.2 Separating BCl_3 Recipes for the Contacted and Non-contacted Emitter Regions

After the optimization of the BCl_3 recipe, the next step was its application on IBC cell structures. Following BCl_3 diffusions for the heavy emitter, light emitter, and front floating emitter, glass layers were removed, and the corresponding measurements were carried out on symmetrical test samples. In addition to FFE, one recipe was applied to have FSF whose post diffusion oxidation step was simultaneously done as boron-doped layers to simplify the cell processes. ECV measurements were done on the wafers with opposite polarity as the dopant atom while sheet resistance measurements were done both on n-Cz and p-Cz wafers. For ECV measurements, test samples without any patterning were utilized while R_{sheet} was checked both on test and patterned IBC samples. The Resulting ECV profiles are given in Figure 5.18.

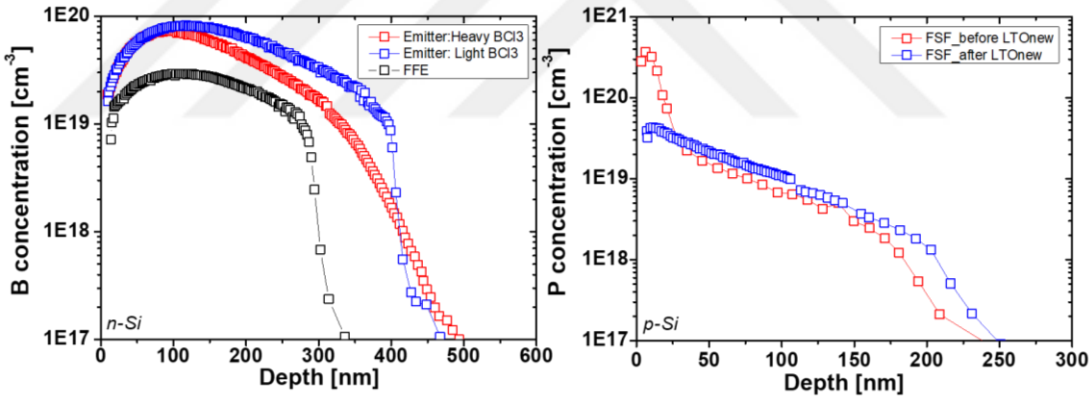


Figure 5.18. ECV profiles for optimized BCl_3(left) and $POCl_3$(right) diffusion

In Figure 5.18, BCl_3 profiles obtained for rear emitter (i.e., heavy & light), boron concentration was successfully increased to $1x10^{20}$ cm^{-3} level. For the case of the heavy emitter, the peak concentration was kept above $5x10^{19}$ cm^{-3} level approximately from 50 to 300 nm. The transition of the boron profile from the p^+ layer to the n-bulk was like a step function. For the light emitter, the decrease of boron concentration was more gradual, and the concentration was above $5x10^{19}$ cm^{-3} level approximately from 50 to 160 nm which was significantly narrower

compared to heavy diffusion. Like the last recipe of BCl_3, the front floating emitter (FFE) profile was tried to be optimized. Since there is no contacting concern, the doping level of FFE could be reduced as much as possible to have the best passivation properties. Reducing the BCl_3 flow to 30 sccm and deposition time to 7 minutes resulted in a shallow boron profile with a peak concentration of $2.9x10^{19}\,cm^{-3}$ as seen in Figure 5.18 (left).

For the case of $POCl_3$ diffused front surface field (FSF) structures, our standard $POCl_3$ recipe resulting in sheet resistance of 50 Ω/□ and a peak concentration of $4x10^{20}\,cm^{-3}$ was applied which was then exposed to LTO processes to mimic the real IBC cell process. LTO process was required to remove the BSG layer, and it was also simultaneously used to reduce the doping concentration of the $POCl_3$ diffused side to reduce the number of process steps. The resulting doping profile is given in Figure 5.18 (right) and it is seen that the LTO process reduces the peak concentration from $4x10^{20}$ to $4x10^{19}\,cm^{-3}$. Reduced doping concentration is expected to improve iVoc with the help of reduced Auger recombination at the front side [82], [83], [84].

In addition to ECV measurements, R_{sheet} mapping was done for each processed wafer over 9 points to verify the doping uniformity. When n-Si was used as the base material (Figure 5.19 (left)), R_{sheet} for the heavy emitter was around 50 Ω/□ while it was around 80 Ω/□ for the case of light emitter after BSG removal. Hence, the effect of reduced BCl_3 flow and shortened deposition time was directly reflected on doping profile and R_{sheet} values. For the FFE recipe which had the lowest dopant concentration and the shallowest junction, R_{sheet} was varying in the range of 100-110 Ω/□.

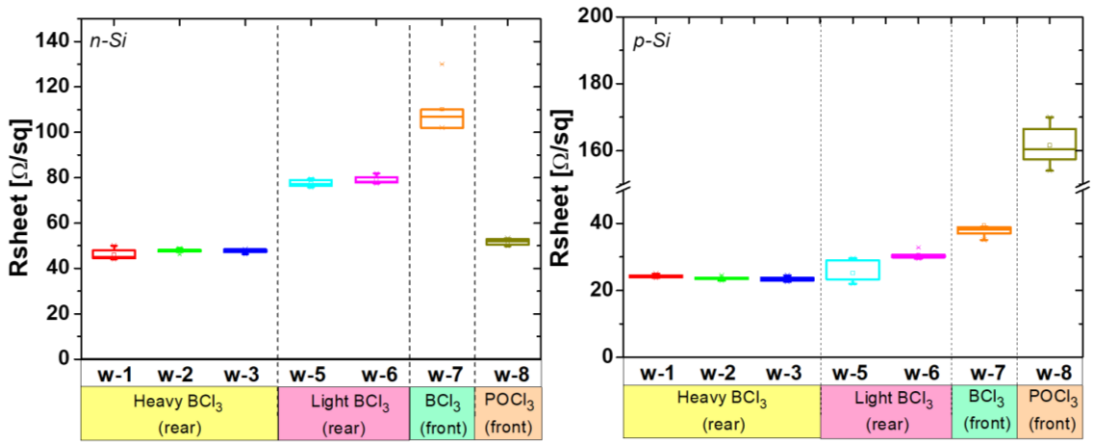


Figure 5.19. Sheet resistance measurements for various BCl_3 and $POCl_3$ recipes on n-Cz (left) and p-Cz (right) wafers.

For the case of the front surface field on n-Si where the front side is exposed to $POCl_3$ diffusion and a successive LTO process, R_{sheet} values were around 50 Ω/□ with a quite acceptable uniformity.

Switching the base material from n-Cz to p-Cz reduced the resulting R_{sheet} of heavy BCl_3 recipe from 45 to 25 Ω/□, and that of light BCl_3 recipe from 80 to 30 Ω/□. While the recipe for FFE structure resulted in approximately 40 Ω/□, the recipe for front $POCl_3$ diffusion resulted in 160-170 Ω/□ when p-Si was used as the base material.

To examine the effect of doping profile on iV_{oc} values, Sinton PCD measurements were carried out after glass removal and the following RCA cleans. The evolution iV_{oc} values of boron-doped regions on n-Si were observed to be quite promising (Figure 5.20 (left)). The average iV_{oc} value of heavy BCl_3 recipe was at around 645 mV level, while that of light BCl_3 recipe was at around 635 mV and was 655 mV for FFE recipe. Reduced dopant concentration enhanced iV_{oc} as expected for the case of FFE while it degraded for the case of FSF with a corresponding iV_{oc} of 595 mV which could be related to the shallow junction obtained by corresponding $POCl_3$ diffusion (Figure 5.18).

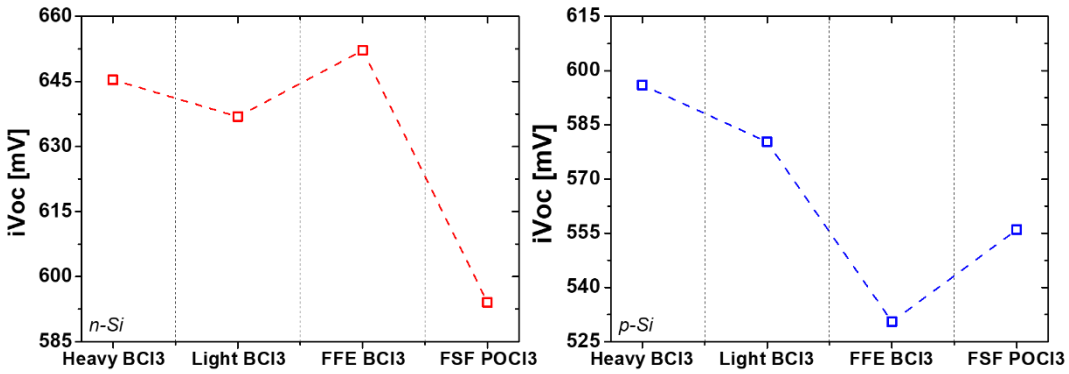


Figure 5.20. Change in iVoc values of test samples for different processes.

Unlike n-Si, p-Si samples had increasing iV_{oc} values as diffused boron concentration increased. The average implied Voc values were 595, 580, and 530 mV for respective heavy, light, and FFE BCl_3 recipes. Thus, it could be deduced that to have a proper BSF region on p-Si, boron concentration should be higher compared to that is needed for boron emitters on n-Si. Moreover, $POCl_3$ diffusion resulted in low iV_{oc} values as in the case of n-Si samples. Thus, the $POCl_3$ recipe should be re-optimized for both rear (BSF) and front surfaces (FSF) in the next set of samples.

Looking at the photoluminescence (PL) images on test wafers, shown in Figure 5.21, reveals that there was a dead region that is increasing in the area as the doping concentration reduced.

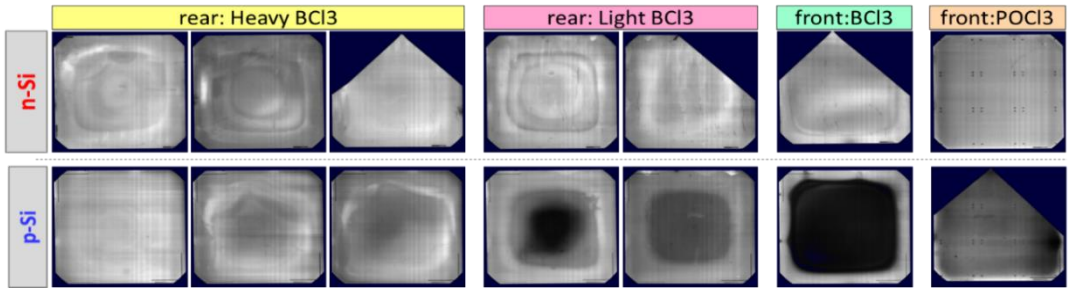


Figure 5.21. PL Images of test wafers for different diffusion processes.

This dead region became more pronounced for the case of p-Si where the BCl_3 diffused region acted as the BSF region. The same dead region was also visible for n-Si with much less contrast. Comparing the signal level $POCl_3$ diffused samples

with that of BCl_3 diffused one, the signal level was lower for the former case. This reduced signal also confirmed unexpectedly low iV_{oc} values of $POCl_3$ diffused samples.

5.3.2 Optimization of Phosphorus Diffusion for Modified Screen Design

Applying three different recipes for the $POCl_3$ diffusion whose details were given at the beginning of this section, resulted in the phosphorous profiles shown in Figure 5.22. Compared to the original recipe P0, adding an oxidation step (P1 and P2), either in-situ or ex-situ, was observed to help to reduce the peak dopant concentration and increase the junction depth. While ex-situ (P1) oxidation resulted in a peak concentration of $4.0x10^{20}$ cm^{-3} and a junction depth of 650 nm, in-situ oxidation (P2) resulted in a peak concentration of $4.1x10^{20}$ cm^{-3} and a junction depth of 500 nm.

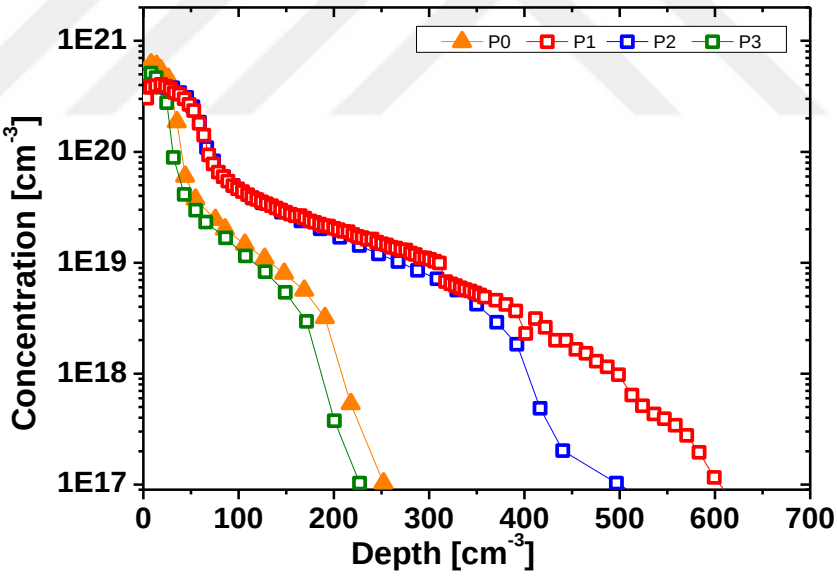


Figure 5.22. ECV profiles of three different $POCl_3$ recipes P1, P2, P3 with the reference recipe P0.

Unlike P1 and P2 recipes, the P3 recipe generated a dopant profile almost like that was generated by the original recipe P0 with a peak concentration reduced from $6.2x10^{20}$ to $5.1x10^{20}$ cm^{-3}. Reducing the peak concentration with almost the same junction depths increased the resulting R_{sheet} from 65 to 75 Ω/□ while switching

from the recipe from P0 to P1. The summary of the sheet resistance measured on n-type and p-type textured wafers is shown in Figure 5.23. Measurements were carried out over 16 points per wafer for each recipe. P0 and P3 recipes resulted in similar R_{sheet} values with slightly lower values for the former one. This could be related to the slight decrease in the peak concentration and junction depth for the case of P3. Similarly, due to similar dopant profiles matching till 400 nm, P1 and P2 recipes resulted in almost the same R_{sheet} values.

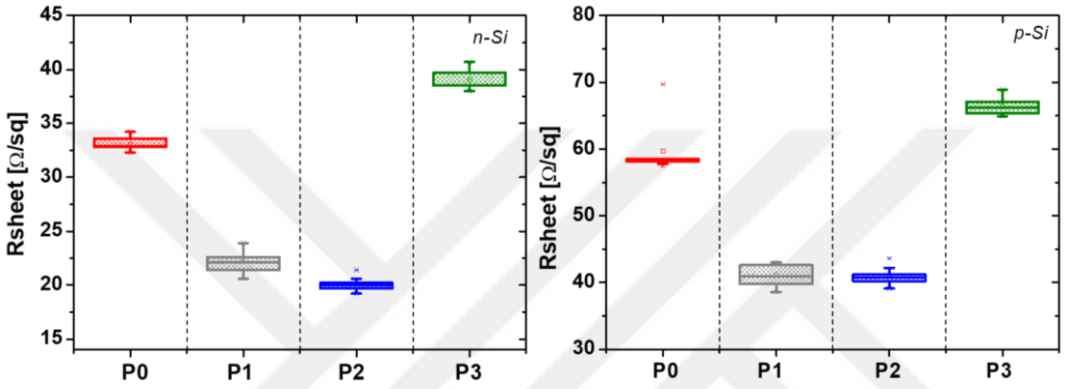


Figure 5.23. Sheet resistances of varying $POCl_3$ recipes measured on n-type (left) and p-type (right) wafers.

Switching the base material from n-type to p-type had shifted the measured sheet resistance values by an amount of 20 Ω/□ for all recipes. In Figure 5.24, the iV_{oc} values were measured over 8 wafers per recipe were shown. The iV_{oc} values measured on n-Si were 15-20 mV higher than those measured on p-Si.

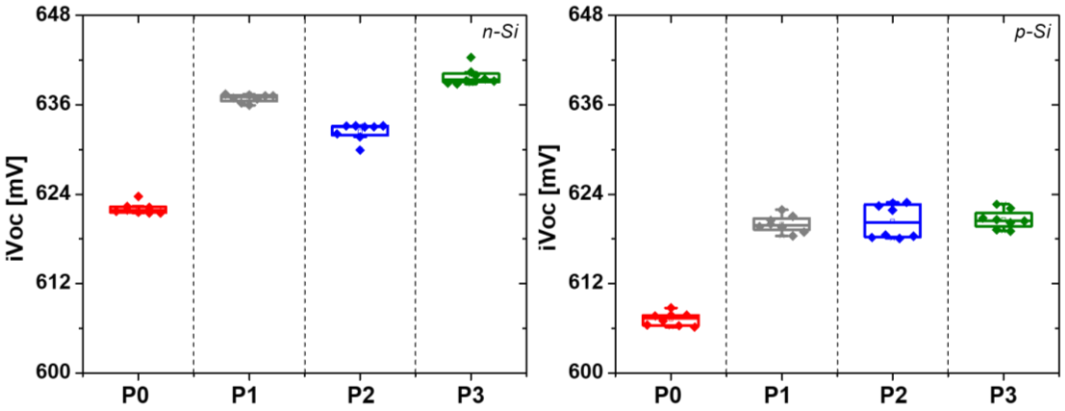


Figure 5.24. iVoc values of n-type (left) and p-type (right) Si wafers after $POCl_3$ diffusion. Samples are staying with PSG for P0, P2, and P3 recipes and with SiO_2 layer for P1 recipe.

Despite quite similar dopant profiles and R_{sheet} values, the iV_{oc} values of the samples doped using recipe P3 were significantly higher compared to those of the samples doped with P0. The respective maximum iV_{oc} values of recipe P3 and P1 on n-Si were 642 and 624 mV as shown in Figure 5.24 (left), This could be related to the reduced dopant concentration at the surface for the case of the lower drive-in period defined in P3. That is, reducing the drive-in duration would pump fewer phosphorus atoms through the underlying Si wafer so that more phosphorus would be stored in the PSG layer which would then be stripped of during glass removal. Comparing P1 and P2 recipes revealed the fact that ex-situ oxidation was more beneficial to improve iV_{oc}. Although the corresponding ECV and R_{sheet} values were quite similar, except for the difference in the tail region, the maximum iVoc value obtained on n-Si using P1 was 637 mV while that was obtained using P2 was 632 mV. Switching the base from n-Si to p-Si reduced the resulting iVoc values for all recipes. Yet, still, the lowest iV_{oc} was obtained from the samples doped using P0, P1, P2, and P3 recipes resulted in quite similar iV_{oc} values as seen in Figure 5.24 (right). The corresponding maximum iVoc values were 609, 622, 623, and 622 mV for the samples doped using P0, P1, P2, and P3 recipes, respectively.

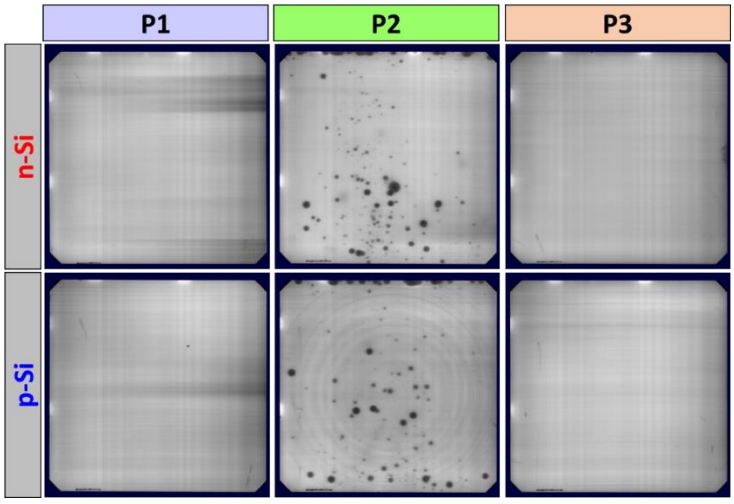


Figure 5.25. Photoluminescence images of the selected sample doped using P1, P2, and P3 on n-type and p-type wafers.

PL imaging was applied for all samples to trace the effect of successive process steps and the images of the selected samples are shown in Figure 5.25. While the samples of P1 and P3 recipes were quite uniform, those of recipe P2 had some dark spots on the surface which could not be eliminated upon cleaning and passivation. Those observed dark spots could be related to the hydrogen fed to the system during the in-situ oxidation step. Despite locally damaged regions, the samples doped using recipe P2 had similar performance as the ones doped using recipe P1.

To trace the effect of successive process steps on the performance of the doped samples, Sinton measurements were carried out to analyze iV_{oc} values. The change of iV_{oc} as a function of process step and diffusion recipe on n-Si is shown in Figure 5.26. The thin oxide layer grown at 850°C via dry oxidation improved the iV_{oc} of all recipes. The maximum iV_{oc} was improved from 637 to 653 mV for recipe P1, from 633 to 648 mV for recipe P2, and from 642 to 660 mV for recipe P3.

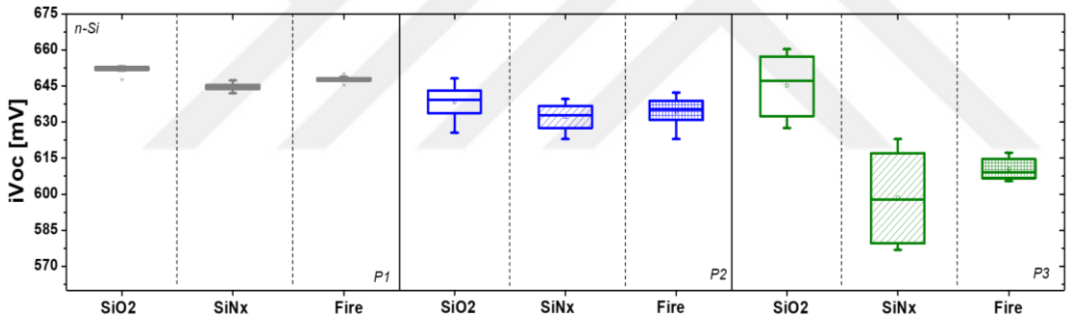


Figure 5.26. Evolution of iVoc during successive processes steps for three different $POCl_3$ recipes on n-Si wafers.

While the deposition of the SiN_x layer reduced iV_{oc} by 6-8 mV for the samples doped using recipe P1 and P2, the reduction was more pronounced for the case of P3 accompanied by the drop of 37 mV. As the last step, firing either generated a negligible increase of 2-3 mV for the cases of P1 and P2, iV_{oc} was further reduced to 617 mV upon firing for the case of recipe P3.

Unlike n-Si, for the case of p-Si wafer oxidation had an adverse effect on iV_{oc} as shown in Figure 5.27. While the samples doped using P1 and P2 recipes

experienced an iV_{oc} drop of 25-30 mV, depositing the SiN_x layer increased iV_{oc} to 622 and 609 mV for P1 and P2 recipes, respectively.

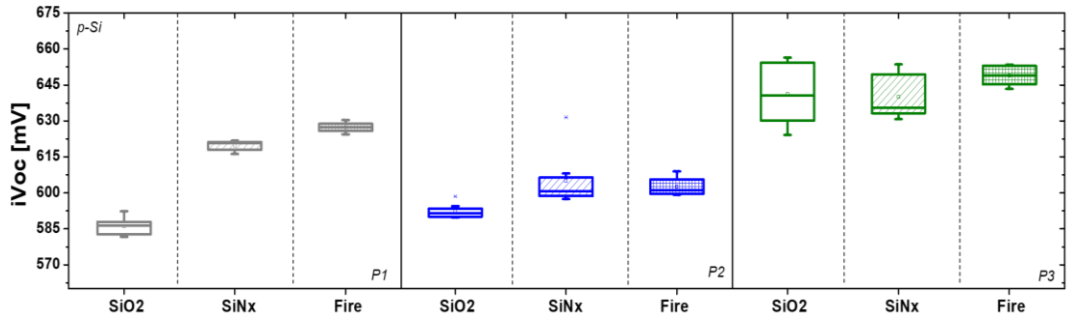


Figure 5.27. Evolution of iVoc during successive processes steps for three different $POCl_3$ recipes on p-Si wafers.

For the case of the samples doped using recipe P3, oxidation increased iV_{oc} from 622 to 656 mV. Depositing the SiN_x layer reduced the iV_{oc} to 654 which showed improvement upon firing. However, the maximum iV_{oc} was still 654 mV after the firing step.

After realizing the effect of the $POCl_3$ recipe on the passivation properties of n-Si and p-Si based samples, the last step was to optimize the contacting properties for each recipe. The change of contact resistivity as a function of peak firing temperature for the applied diffusion recipes on n-Si is shown in Figure 5.28. Increasing the peak temperature from 890 to 935°C with a constant belt speed reduced the resulting contact resistivity values below 3 $m\Omega.cm^2$ level.

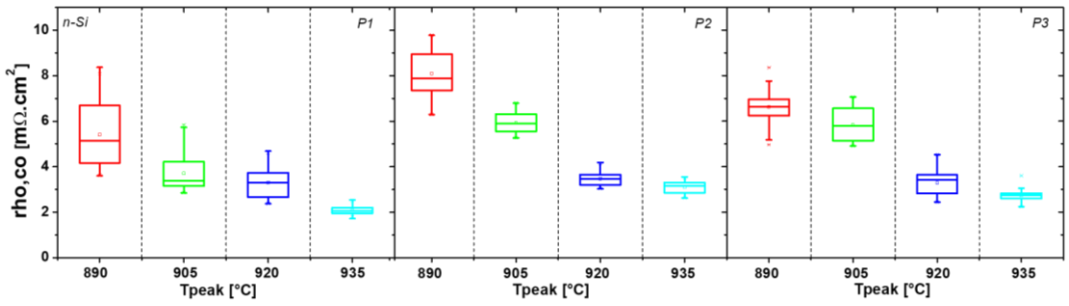


Figure 5.28. Contact resistivity change of the $POCl_3$ diffused n-based samples metallized with FT-Ag paste.

Even the lowest firing temperature 890°C was enough to form proper contact with the corresponding contact resistivities below 10 mΩ.cm^2. However, no explicit correlation between the doping profile (i.e., surface concentration, junction depth) and contact resistivity could be established.

Using p-Si as the base material resulted in similar contact resistivity values as the case of the n-Si wafer as shown in Figure 5.29.

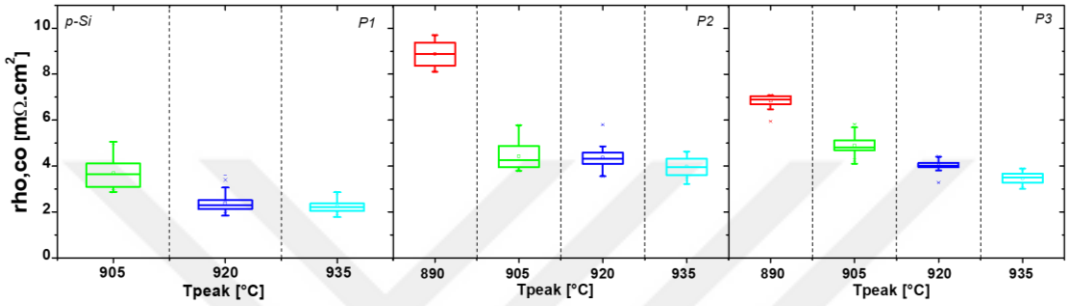


Figure 5.29. Contact resistivity change of the $POCl_3$ diffused p-based samples metallized with FT-Ag paste.

Again, even at the lowest firing temperature (890°C), the obtained contact resistivity values were lower than 10 mΩ.cm^2. Both for n-Si and p-Si cases, samples doped using the P2 recipe had slightly higher contact resistivity values compared to those diffused using P1 and P3 recipes. This could be related to the lower surface concentration and slightly shallower junction depth generated by P2. However, no explicit relation could be established as in the case of n-Si based samples.

To sum up, it was observed that the base material had a significant effect on the performance of the diffused samples. When $POCl_3$ diffusion was used as the BSF region on n-Si, deeper junctions resulted in better performance, thus higher iV_{oc} values. On the contrary, when $POCl_3$ diffusion was used to form the emitter region on p-Si, then the shallower junction with higher surface concentration was observed to be more beneficial in terms of passivation and firing stability.

5.3.3 Application of Optimized Recipes at the Cell Level

After the optimization of separate recipes for the front and rear boron diffusions, IBC samples were simultaneously processed as symmetrical samples. Following the etch resist printing and drying, patterning was done, and then the etch resist was stripped. The patterned diffusion barrier, against boron diffusion, for n-Si (upper row), and p-Si (lower row) is shown in Figure 5.30.

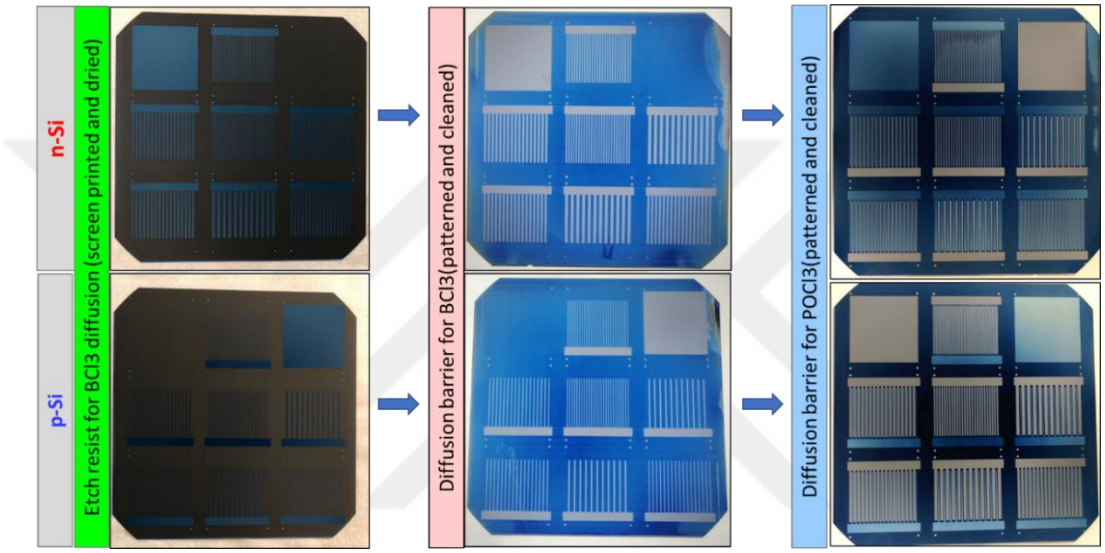


Figure 5.30. Visual inspection of samples throughout cell processes. Printed and dried etch resist (left), patterned diffusion barrier for BCl_3 diffusion (middle), patterned diffusion barrier for $POCl_3$ diffusion (right).

In this set of samples, patterning was successfully done and the alignment problems during screen printing were eliminated with the help of the modifications on the screen design. BCl_3 diffusions for the rear emitter, BCl_3 diffusion for the front floating emitter and $POCl_3$ diffusion for the front surface field, and post oxidation for glass removal were done. After the measurements, the diffusion barrier for the BSF region was deposited, patterned, and cleaned. After $POCl_3$ diffusion for BSF formation, samples were ready for passivation. Remembering our custom IBC design, shown in Figure 5.31, three different pitch values as 750, 1250, and 1700 µm were utilized to examine the effect of pitch on the cell performance.

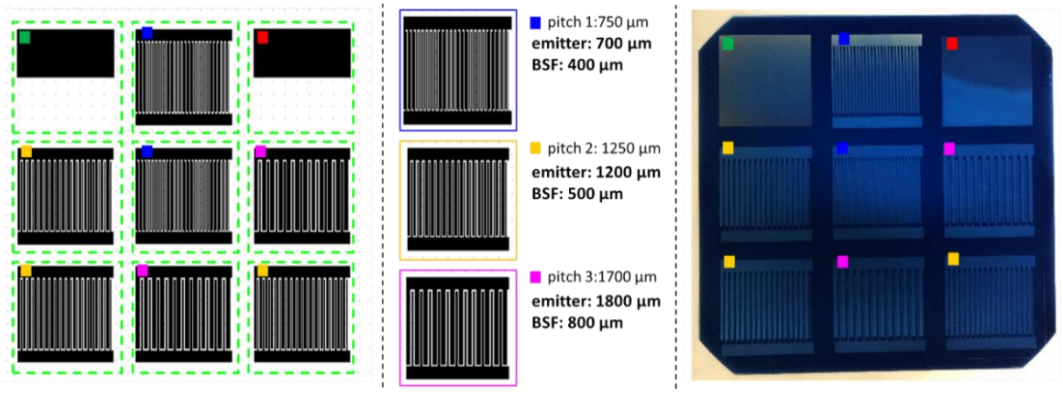


Figure 5.31. Design details of the used screen and pitch distribution over the wafer. Green represents the test pattern for the emitter region, red is the test pattern for BSF, blue is for the smallest pitch (750 µm), yellow is for the moderate pitch (1250 µm), and pink is for the largest pitch (1700 µm).

Considering the iV_{oc} values shown in Figure 5.32, cells with FFE (left) have significantly superior performance compared to cells with FSF (right). Considering the emitter pattern iV_{oc} values for FFE could reach at 660 mV level while that was limited at 605 mV for the cells with FSF. BSF regions show poor performance both for FFE and FSF samples since they were not doped yet.

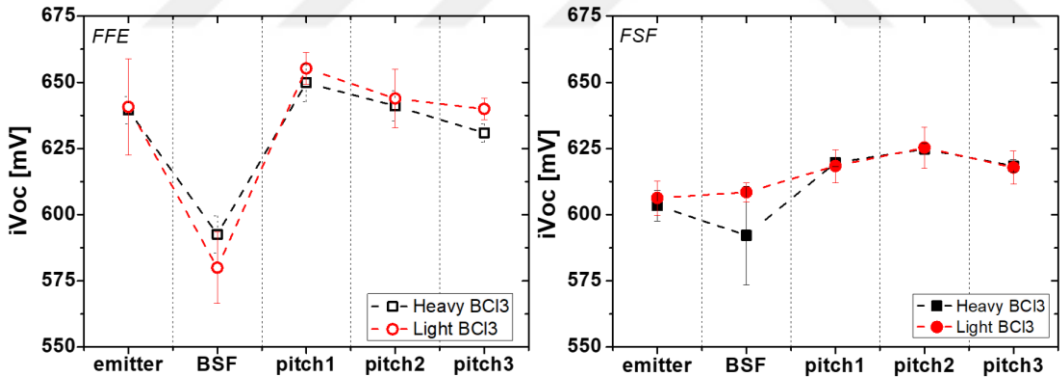


Figure 5.32. Implied Voc values for different cell pitches after rear emitter and front floating junction formation on n-Cz. The front surface is BCl_3 diffused for FFE (left) and $POCl_3$ diffuse for (FSF) structure.

For the samples with FFE, iV_{oc} was decreasing as the cell pitch increased with the highest value of 661 mV for 750 µm pitch before passivation. It was also observed that the samples of light BCl_3 split resulted in slightly better iV_{oc} values compared to those of high BCl_3 split. Samples with FSF showed a different behavior with the best iVoc of 633 mV coming from the moderate pitch (1250 µm). Pitch

dependence of the iV_{oc} values of FSF samples was less pronounced compared to FFE samples.

Considering the samples on p-Cz substrates, pitch dependence of FFE and FSF samples were the same as they were for n-Cz wafers as given in Figure 5.33.

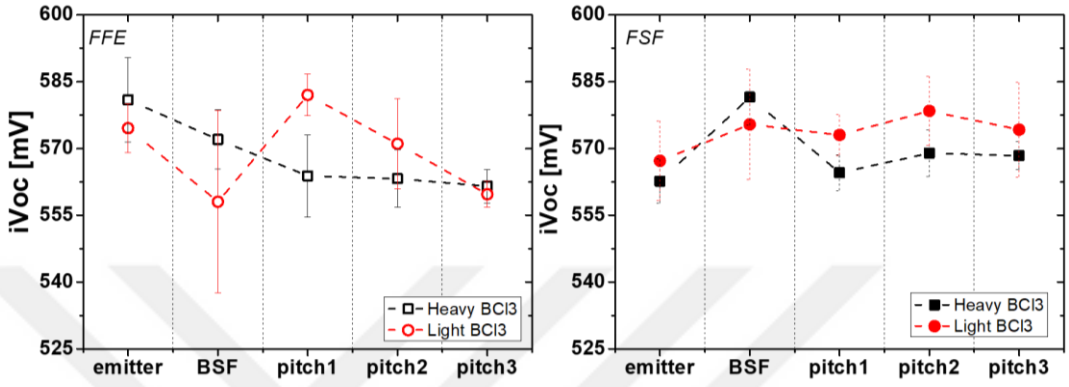


Figure 5.33. Implied Voc values for different cell pitches after rear emitter and front floating junction formation on p-Cz. The front surface is BCl_3 diffused for FFE (left) and $POCl_3$ diffuse for (FSF) structure.

That is, for FFE samples the highest iV_{oc} value was obtained as 593 mV from the cell with the smallest pitch (750 µm) while that of FSF samples was 590 mV from the moderate pitch (1250 µm). Light BCl_3 recipe results in higher iVoc values compared to heavy BCl_3 recipe.

After the $POCl_3$ diffusion for the formation of BSF, it was observed that the iV_{oc} of the cell patterns showed either a small improvement or no change for the case of heavy emitter diffusion on n-Si. The change of iV_{oc} values throughout the whole process sequence is shown in Figure 5.34.

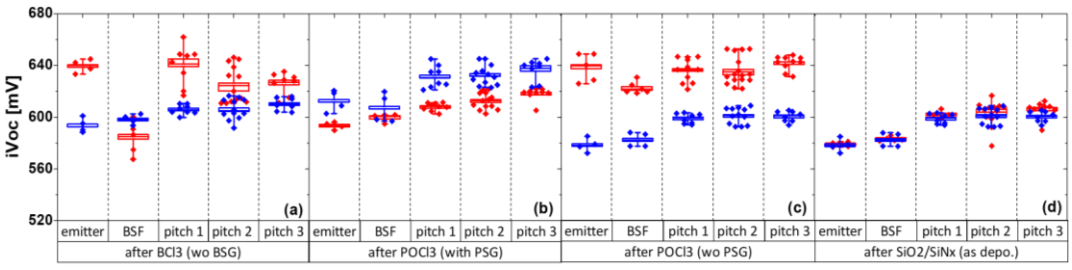


Figure 5.34. Change of iVoc for the cells with FFE with heavily doped (red) and lightly doped (blue) emitter on n-Si.

Comparing plots (a) and (c) in Figure 5.34, it was observed that introducing the BSF region of the cell did not generate a big difference in the performance of the cell patterns. While iV_{oc} of the emitter pattern degrades during the $POCl_3$ diffusion process, that of the BSF region improved since it was not doped in the former case. However, applying passivation degraded iV_{oc} values of all patterns as shown in Figure 5.34 (d). Compared to their heavily doped emitter counterparts, the cells with lightly doped emitters had inferior performance after the formation of emitter and BSF regions as shown in Figure 5.34 (c). Yet, passivation brought all cells to the same iV_{oc} level as seen in Figure 5.34 (d).

iV_{oc} change of the cells with FSF is shown in Figure 5.35 for heavily and lightly doped emitter regions on n-Si. Unlike the case of the cells with FFE, putting passivation stack did not degrade the performance of the patterned regions for the case of the cells with FSF.

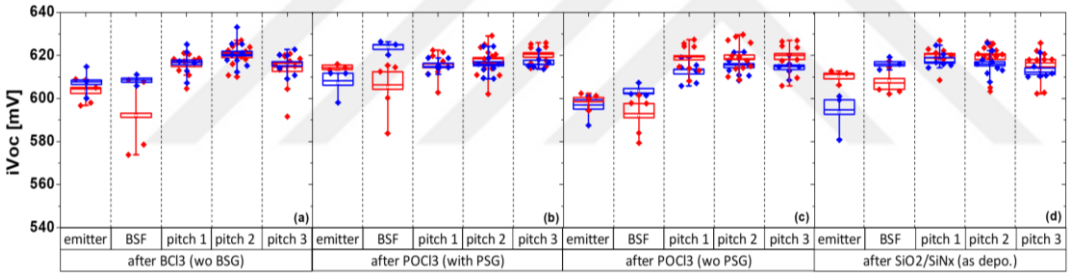


Figure 5.35. Change of iVoc for the cells with FSF with heavily doped (red) and lightly doped (blue) emitter on n-Si.

Moreover, after the passivation, the cells with FSF had iV_{oc} values within the range of 610-620 mV which was 600-610 mV for the case of FFE. It can be concluded that the used passivation stack is not suitable to passivate neither the heavily doped rear emitter nor the lightly doped front floating emitter regions.

Switching the base material from n-Si to p-Si had reduced the iV_{oc} values right after BCl_3 diffusion as shown in Figure 5.36 (a). Since boron-doped regions were acting as BSF on p-Si, it was expected to have lower iV_{oc} values right after the boron diffusion step.

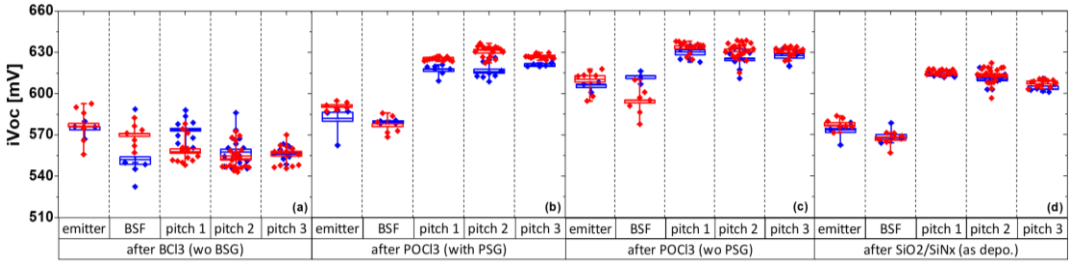


Figure 5.36. Change of iVoc for the cells with FFE with heavily doped (red) and lightly doped (blue) emitter on p-Si.

Introducing the emitter region by the following $POCl_3$ diffusion increased the iV_{oc} values of the cell patterns above 620 mV level with the slightly superior performance of the cells with heavy boron diffusion as seen in Figure 5.36 (b). However, depositing the passivation stack reduced the iV_{oc} values to the range of 600-620 mV.

As the last set of samples, cells with FSF on p-Si wafers were fabricated. While the performance of the cells right after the boron diffusion was quite low as in the case of the cells with FFE, placing the n^+ doped emitter regions significantly improved the corresponding performances of the patterned regions as shown in Figure 5.37 (b-c).

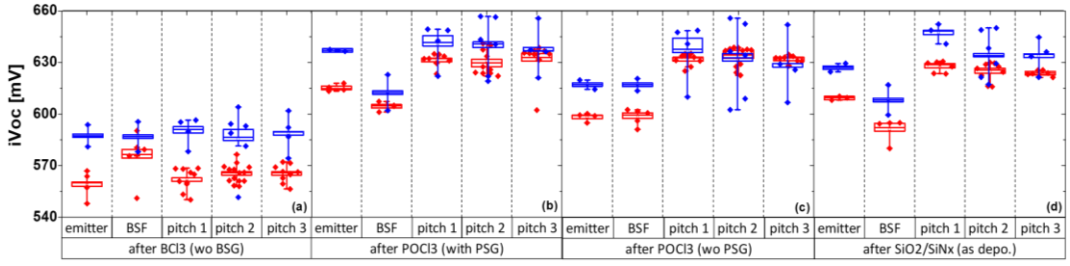


Figure 5.37. Change of iVoc for the cells with FSF with heavily doped (red) and lightly doped (blue) emitter on p-Si.

Unlike all the previous cases, introducing a passivation stack did not degrade the measured iV_{oc} values. Not only for the patterned cell structure but also the emitter and BSF patterns experienced an increase in the corresponding iV_{oc} vales with the superior performance of the cells with light boron diffusion Figure 5.37 (d). The

resulting average iV_{oc} values of the cell pattern were above 630 mV level and the highest iV_{oc} was measured on the smallest pitch which was around 650 mV.

The observed degradation of iV_{oc} values for all cell types which was more pronounced for the case of cells with FFE showed the fact that the utilized passivation stack SiO_2/SiN_x is not suitable to be used on boron-doped regions. Although the 5 nm Al_2O_3/SiN_x stack also showed a degradation as discussed at the beginning of this chapter upon firing, it is the best candidate for the passivation of the boron-doped regions for now. Further analysis and development of firing stable Al_2O_3/SiN_x stacks will be focused on as future work.

CHAPTER 6

FABRICATION AND CHARACTERIZATION OF THE IBC SOLAR CELLS USING THE PROCESS PARAMETERS OPTIMIZED IN THE PREVIOUS CHAPTERS

After understanding the effect of diffusion profiles on the passivation performance and contacting properties of the doped region, a new set of samples were prepared for cell fabrication. This chapter mainly will focus on the fabrication and characterization of the IBC solar cells with FFE and FSF using the optimized process parameters.

6.1 Introduction

In the previous chapter, both boron and phosphorus diffusion processes were studied in detail. While rear side diffusion processes were checked both for passivation and contacting properties, front side diffusions were only examined for passivation properties. Despite the drop in iV_{oc} upon firing, Al_2O_3/SiN_x stack was determined to be the best candidate to properly passivate the boron diffused regions. While an increase in the boron concentration at the surface made the measured iV_{oc} more stable upon firing, the existence of a dead layer with an excess amount of boron (BRL) was already limiting the iV_{oc} values. Thus, it was determined to obtain a new boron recipe resulting in higher boron concentration at the surface but would not leave a BRL layer behind. The phosphorus diffusion recipe would also be revisited in this chapter to obtain higher iV_{oc} values together with good contacting properties. The most important motivation of this chapter is to find a common capable of the simultaneously passivating boron-doped emitter and phosphorus-doped BSF regions at the rear side of the cell.

6.2 Experimental Details

After observing the effect of boron concentration at the surface, four alternative recipes were generated to dope the emitter regions at the rear surface. In addition to changing deposition time, the temperature of the ex-situ oxidation to remove BSG was also varied. While the oxidation at 850°C was kept as the reference recipe, 650°C was also applied to suppress the depletion effect at the surface of the boron-doped surface which was the case in the previous chapter. In addition to BCl_3 diffusion in the reduced pressure furnace, BBr_3 diffusion was also utilized for one recipe in the atmospheric furnace. For the boron diffusion of the front surface, deposition time and BCl_3 flow were reduced, and two oxidation temperatures were utilized. The table summarizing the process details of generated boron and phosphorus diffusion recipes is shown in Table 6.1.

Table 6.1. Recipe details used for front and rear side diffusion processes.

Split	Purpose	Details	Process Gas
A	Emitter-1	Deep with dry oxide at 650°C	BCl3
B	Emitter-2	Standard with dry oxide at 650°C	
C	Emitter-3	Deep with dry oxide at 850°C	
D	Emitter-4	Shallow with dry oxide at 650°C	BBr3
E	BSF-1	Deep heavily doped	POCl3
F	BSF-2	Standard	
G	BSF-3	High sheet resistance	
H	FFE-1	Shallow lightly doped with dry oxide at 650°C	BCl3
I	FFE-2	Shallow lightly doped with dry oxide at 850°C	
J	FSF-1	Shallow lightly doped with low POCl3 flow	POCl3
K	FSF-2	Shallow lightly doped with low POCl3+dryox after PSG removal	

Like boron diffusion recipes, phosphorus diffusion recipes were modified to generate different junction depths and peak concentrations for both the rear and front junctions.

Following the diffusion processes, various passivation sceneries were applied for all diffusion profiles. Three of the applied recipes had been optimized for the n^+ doped layers while the remaining two recipes had been optimized for the p^+ doped layer. Details of the passivation recipes are shown in Table 6.2.

Table 6.2. Recipe details used for boron and phosphorus-doped layers.

Split	Purpose	Recipe
PASS-1	n+ ARC	SiN1
PASS-2	SiOxNy/SiNx stack	new08-1
PASS-3	PERC front side	standard
PASS-4	p+ passivation	Al2O3/SiN1
PASS-5	p+ passivation	Al2O3/new08

After determining a common recipe to be used for the rear side, contacting properties were evaluated for three different industrial metal pastes. One of the screen-printed pastes was FT-AgAl designed for p^+ doped regions, the other two were designed for n^+ doped regions. The first paste used for n+ doped regions was FT-Ag paste and the other one was a new FT-Ag paste designed for the metallization of n^+ doped polySi layers which would be used for the first time within the scope of this thesis.

Doping profiles of the samples were measured using ECV right after the glass removal step before which R_{sheet} measurements had been completed. Lifetime measurements were carried out using Sinton WCT-120 at different process steps. All symmetrically diffused samples were measured right after diffusion and passivation steps. After the passivation, some of the samples were fired at a peak temperature of 885°C for a constant belt speed of 500 cmpm. While the fired samples were used for Sinton measurements, a new set of samples would be re-fabricated for the metallization and following TLM measurements. The passivated samples of the selected diffusion recipes were metalized using FT-AgAl and FT-Ag pastes. Two alternative pastes from the same supplier were utilized as FT-Ag. While the first paste was the regular Ag paste used for the front side of PERC cells (FT-Ag1), the second one was designed for the metallization of polySi layers (FT-Ag2).

As the last task of this chapter, IBC solar cells would be fabricated using the optimized process parameters. Both FFE and FSF- IBC cells were fabricated on n-type, textured, M2 wafers. In addition to optimized cell parameters, a thin SiO_2

layer was grown under a passivation stack via dry oxidation at 650°C. Moreover, some of the un-metalized IBC cells were fired at 885°C and used for Sinton measurements. For the fabricated cells, following the screen-printing, co-firing, and laser cutting steps, current-voltage characteristics were traced using a QUICKSUN-120CA Class A solar simulator equipped with a Xenon flash tube with an A.M 1.5G filter.

After solar simulator measurements, external quantum efficiency (EQE) measurements were carried out using Bentham PVE300 Tool. During the measurements, the spot size of the light was 0.74 mm and sent from the front side of the cells. Approximately 7 mm of the cell was scanned for whole spectrum measurements where the scan step was 0.75 mm. Moreover, measurements were also carried out at the regions close to the emitter and BSF busbar regions.

6.3 Results and Discussions

6.3.1 Optimization of Boron Diffusion and Passivation

To optimize boron diffusion for the emitter region placed at the rear side of the n-type Si wafer, four recipes were applied whose details were given in Table 6.1. For all recipes resulting doping profiles are shown in Figure 6.1. As seen in Figure 6.1, Split A and Split D samples had the same boron concentration at the surface with different junction depths of 600 and 500 nm, respectively. For the case of Split B and Split D samples, junction depths were the same while the respective peak concentrations at the surface were $7.9x10^{19}$ and $1.1x10^{20}$ cm^{-3}. Split C samples had a shallower and lightly doped junction compared to those of other splits.

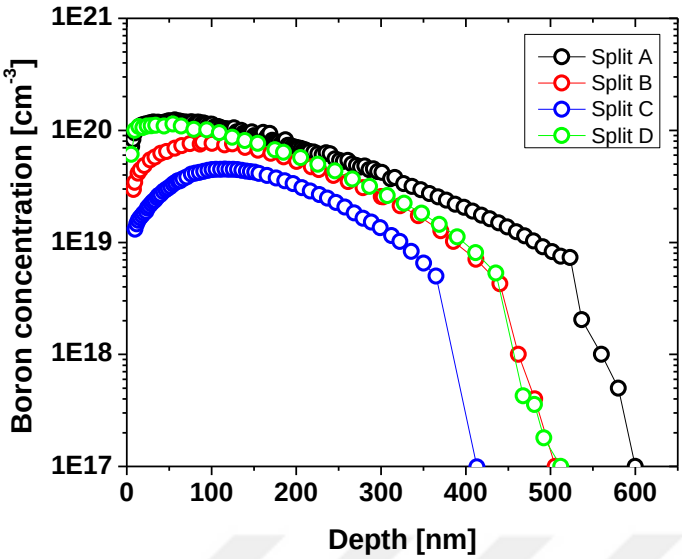


Figure 6.1. ECV profiles of applied boron recipes for emitter region. Measurements were done on symmetrically doped, n-Si wafers.

While the peak concentration was $4.5x10^{19}$ cm^{-3} and the corresponding junction depth was 410 nm. Considering the process details of Split A and Split C samples, it could be deduced that increasing ex-situ oxidation temperature from 650 to 850°C significantly reduced active boron concentration and junction depth. On the other hand, applying the same ex-situ oxidation temperature (650°C) for standard BCl_3 diffusion recipes resulted in a depleted region at the surface which was not the case for the case of deeper BCl_3 diffusion. Thus, it is not only the ex-situ oxidation temperature but also the applied BCl_3 diffusion recipe determining the final boron profile. The corresponding sheet resistance values were 34.1±2.6, 42.0±2.5, 75.2±11.9 and 41.7±2.7 Ω/□ for the samples of respective splits A, B, C, and D on n-Si wafers.

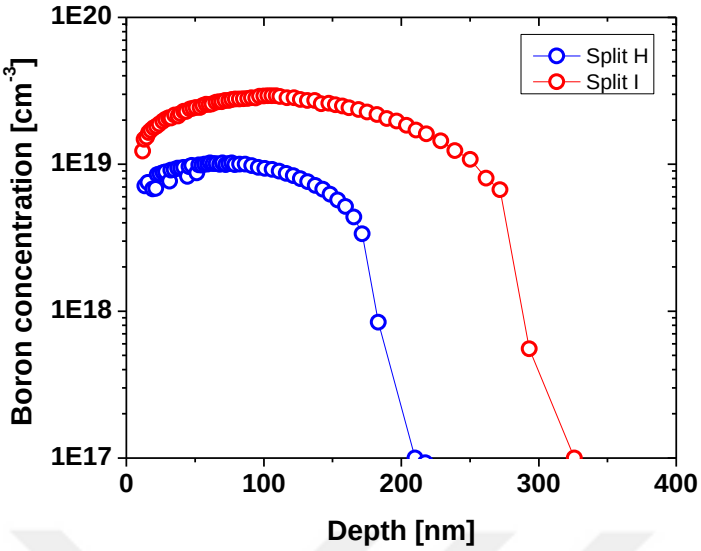


Figure 6.2. ECV profiles of applied boron recipes for front floating emitter region. Measurements were done on symmetrically doped, n-Si wafers.

To optimize the profile for the front side boron profile (FFE), two alternative recipes were applied with the same BCl_3 diffusion but different ex-situ oxidation temperatures of 650 and 850°C. The resulting diffusion profiles are shown in Figure 6.2. Split H resulted in a peak concentration of $1.0x10^{19}$ cm^{-3} with the corresponding junction depth of 210 nm while Split I resulted in a peak concentration of $2.9x10^{19}$ cm^{-3} with the corresponding junction depth of 330 nm. Unlike the rear emitter, the front emitter was designed to be shallower and lightly doped since there would not be contacting concern. The average sheet resistance values were 644±43.5 and 310.3±30.1 Ω/□ for the samples of Split H and Split I, respectively. Those high sheet resistance values are expected for low doping concentrations and shallower junctions. Implied Voc values were measured after each process step and summarized for the applied boron diffusion recipes for the rear emitter in Figure 6.3.

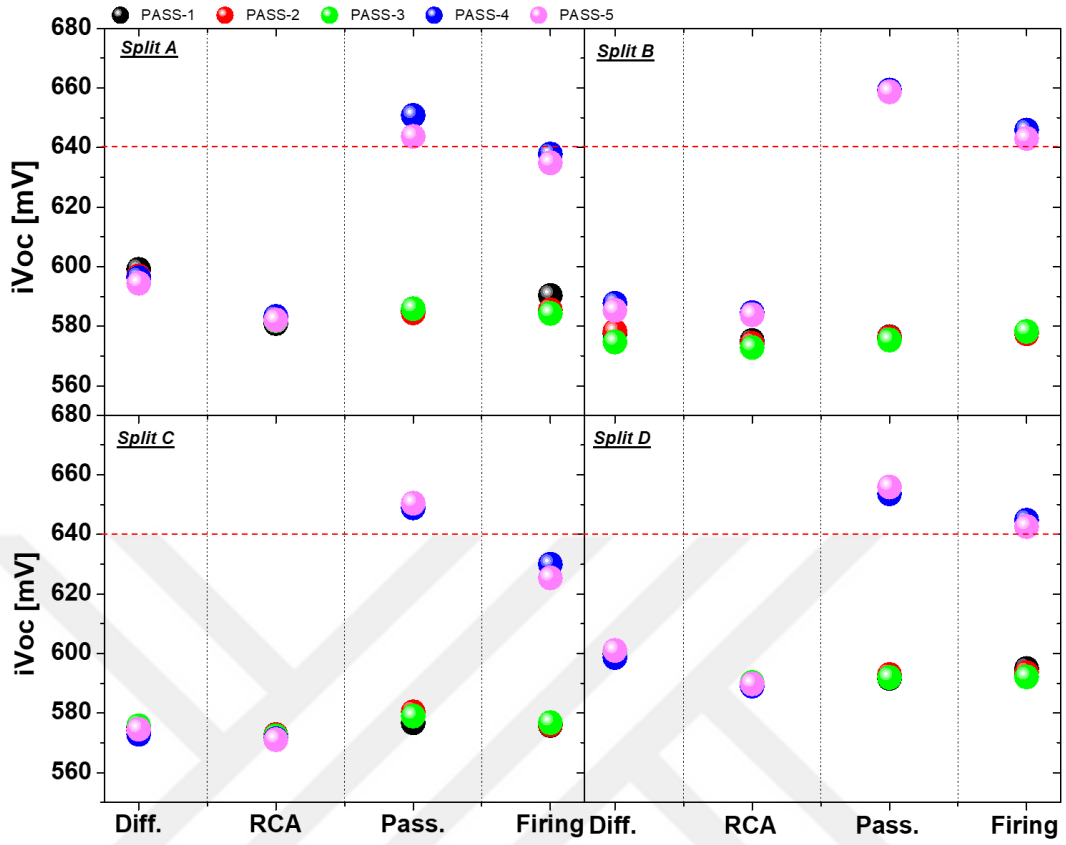


Figure 6.3. Change of implied Voc of the samples doped with four different boron recipes and passivated using five different passivation layers. Dashed lines are a guide for the eye.

It was observed that depositing SiN_x or SiO_xN_y/SiO_x stack directly on top of boron diffused layers were not suitable for proper passivation. For all boron diffusion recipes, the measured iV_{oc} values were lying within the range of 580-600 mV for the passivation recipes excluding Al_2O_3, namely PASS1, PASS2, and PASS3. For the cases of PASS4 and PASS5, although the resulting iV_{oc} values were quite promising right after the deposition of Al_2O_3/SiN_x, the high-temperature firing hurt the iV_{oc} of all diffusion sets. The samples with higher boron concentration at the surface showed a lower drop in iV_{oc} upon firing which was more pronounced as the surface is depleted or the doping concentration was reduced as in the respective cases of Split B and Split C. The samples of Split A and Split D where the peak boron concentration at the surface was approximately $1x10^{20}$ cm^{-3} for both while the corresponding junction depths were 600 and 500 nm, respectively. Moreover,

the PASS4 stack was performing slightly better compared to the PASS5 stack where the only difference was the composition of the used SiNx layers for those stacks. The refractive index of SiN1 used in PASS4 was 1.96 and that of new08 was 1.73 at 632 nm. Thus, it is not only the boron concentration or Al_2O_3 layer but also the SiN_x layer that influences the passivating properties and firing stability. For the cell fabrication, Split A and B were decided to be used either with PASS4 or PASS5. The performance of the phosphorus doped BSF layer would determine the passivation recipe to be used for the rear side in the final cell fabrication step.

For the case of the boron diffusion optimized for FFE, the measured iVoc values are shown in Figure 6.4. For Split H, the iV_{oc} value was 676 mV right after passivation which reduced to 662 mV after firing when PASS4 was used as the passivation stack. The respective values were 667 and 654 mV for the case of Split I.

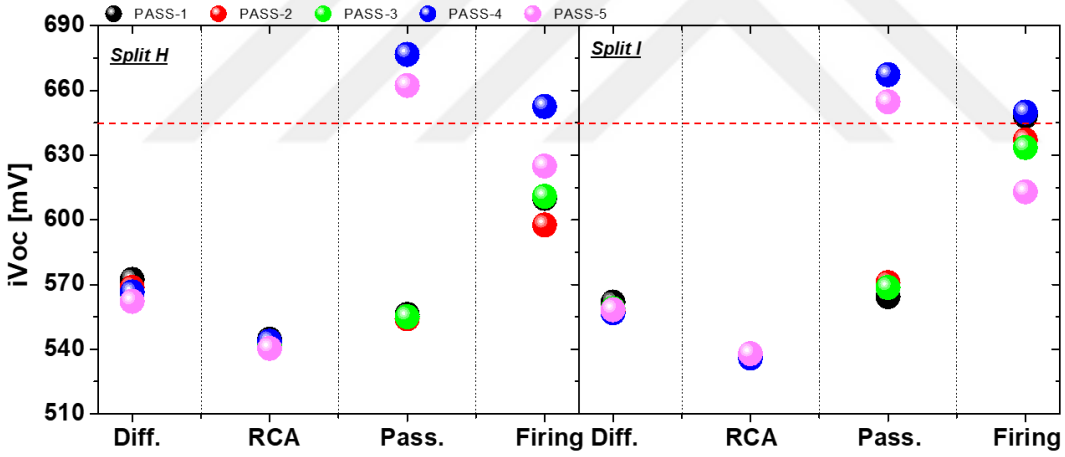


Figure 6.4. Change of implied Voc of the samples doped with two different boron recipes and passivated using five different passivation layers. Dashed lines are a guide for the eye.

Thus, the recipe applied for Split H samples was determined to be used for the FFE layer and passivated with the PASS4 stack in the device application.

6.3.2 Optimization of Phosphorus Diffusion and Passivation

Similar to the boron diffusion case, phosphorus diffusion recipes were separately optimized for rear side (BSF) and front side (FSF) regions. Three different recipes were applied for BSF, and two different recipes were applied for FSF regions. The details of the applied recipes are given in Table 6.1. For the passivation, five different recipes were applied as in the case of boron diffusion optimization and the details of the passivation recipes are given in Table 6.2.

For BSF recipes the resulting ECV profiles are shown in Figure 6.5. The peak concentration of the samples varied as $3.8x10^{20}$, $4.3x10^{20}$, and $3.1x10^{20}$ cm^{-3} while the junction depths were 200, 230, and 570 nm for the respective sample splits of E, F, and G. The average sheet resistance values were 87.0±7.1, 58.1±6.7, and 35.4±8.0 Ω/□ for the samples of Split E, F, and G, respectively.

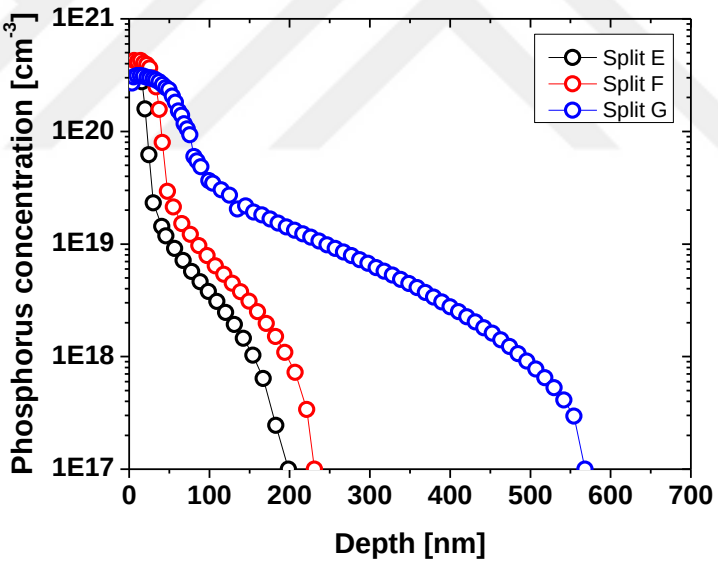


Figure 6.5. ECV profiles of applied phosphorus recipes for the BSF region. Measurements were done on symmetrically doped, p-Si wafers.

The shallower junction with the highest surface concentration resulted in the highest sheet resistance while the deepest junction with the lowest surface concentration resulted in the lowest sheet resistance value.

For the samples of FSF split, although it had been purposed to have two different diffusion profiles, due to a gas flow problem during the process, the resulting ECV profiles were almost identical as shown in Figure 6.6. While the peak concentration was $2.8x10^{20}$ and $2.6x10^{20}$ cm^{-3} for the respective splits of J and K, the corresponding junction depths were 160 and 166 nm. The resulting sheet resistance values were 96.4±8.8 and 104.7±13.3 Ω/□. Despite almost identical ECV profiles, the resulting sheet resistance values showed slight differences. Moreover, for increasing sheet resistance values, the sheet resistance distribution got poorer.

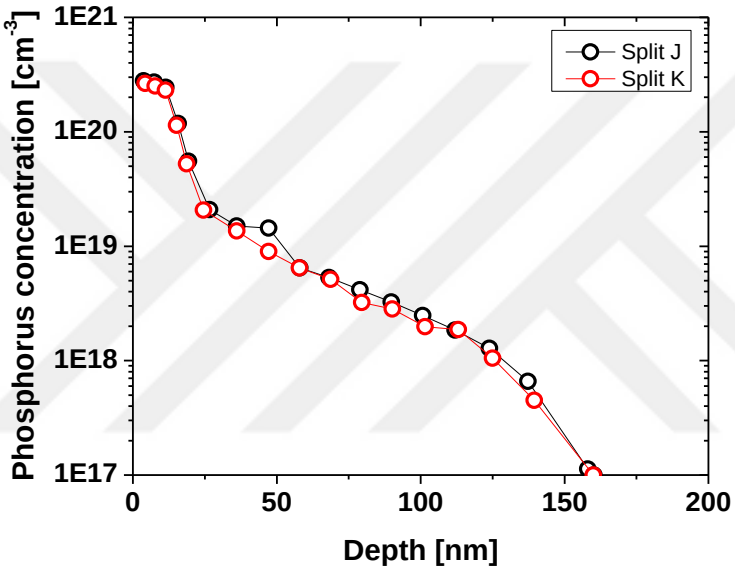


Figure 6.6. ECV profiles of applied phosphorus recipes for the FSF region. Measurements were done on symmetrically doped, p-Si wafers.

After diffusion and necessary cleaning steps, the samples were passivated with already defined passivation recipes. The measured iV_{oc} values measured on BSF samples are shown in Figure 6.7. Unlike the boron-doped samples, all phosphorus-doped samples showed improvement in iV_{oc} upon firing. Depending on the doping profile and applied passivation stack this improvement varied but it was always an improvement, not a degradation. The best iV_{oc} of 644 mV after firing came from Split E samples while it was below 640 mV line for the cases of Split F and Split G. Moreover, all passivation stacks, except PASS5, resulted in the same iV_{oc} values and the PASS5 stack showed the smallest improvement for all diffusion recipes.

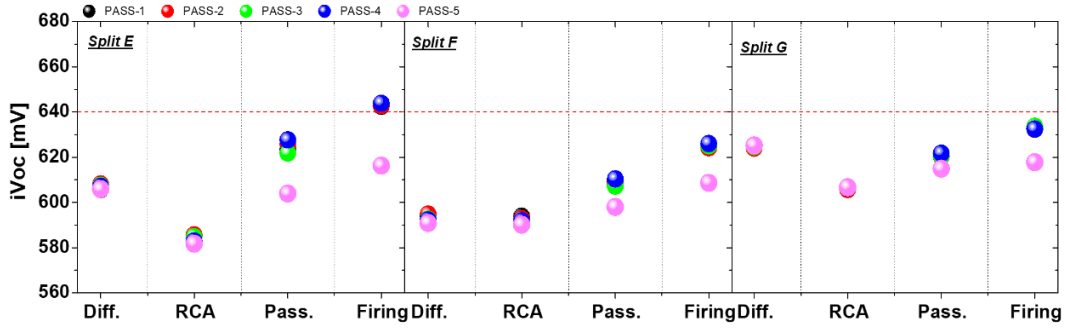


Figure 6.7. Change of implied Voc of the samples doped with three different phosphorus recipes and passivated using five different passivation layers. Dashed lines are a guide for the eye.

Comparing two shallow junction cases, Split E and F, Split E with the lower peak concentration had superior performance. However, comparing the deep and shallow junctions, Split E and Split G, the one with the higher doping concentration was observed to result in higher iV_{oc} values. The most important outcome of this part having PASS4 stack as the properly working passivation layer on the n^+ doped BSF region. Since the same stack also resulted in the highest iV_{oc} values for the case of the p^+ doped emitter region, PASS4 would be the common layer to passivate the rear side of the cells. Thus, TLM measurements would be carried on the determined doping recipes, recipe A and B for the emitter and recipe E for the BSF, all of which would be passivated using PASS4 stack.

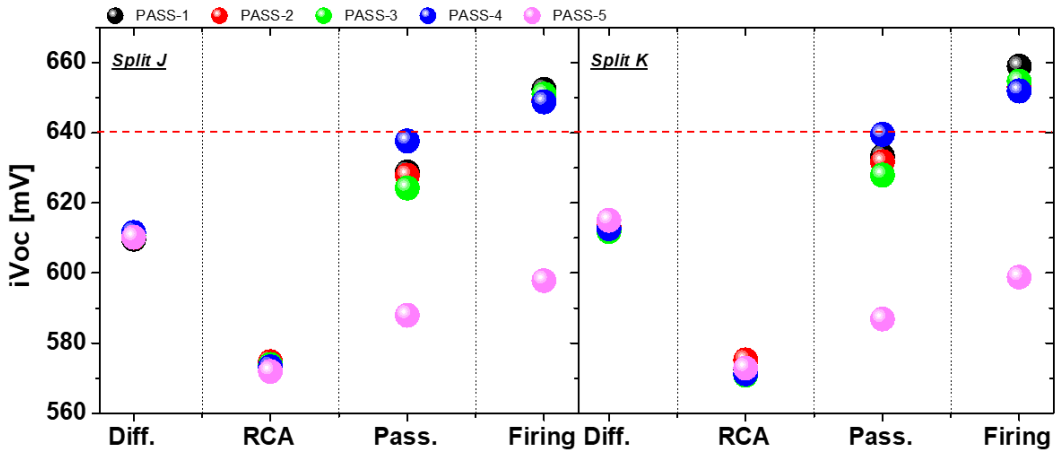


Figure 6.8. Change of implied Voc of the samples doped with two different phosphorus recipes and passivated using five different passivation layers. Dashed lines are a guide for the eye.

The change of iV_{oc} values for the FSF recipes as a function of successive process steps is shown in Figure 6.8. In this case, all passivation stacks, except PASS5, resulted in similar iV_{oc} values after passivation and firing conditions. Since the PASS1 recipe resulted in an iV_{oc} of 654 mV for the case of Split J and 660 mV for the case Split K, it was determined to be used at the front side of the cells with FSF.

6.3.3 Optimization of Metallization for the Rear Side

After determining the diffusion recipes and passivation stack for the emitter and BSF regions, the last step was to optimize the contact resistivity before the cell fabrication. For this, the BCl_3 recipe applied for Split A and Split B samples was re-visited to fabricate the test samples while Split E and Split F recipes were chosen for the $POCl_3$ samples.

After the corresponding diffusion processes, ECV measurements were carried out to check whether there was any problem or not. ECV profiles of the selected boron and phosphorus diffusion recipes are shown in Figure 6.9.

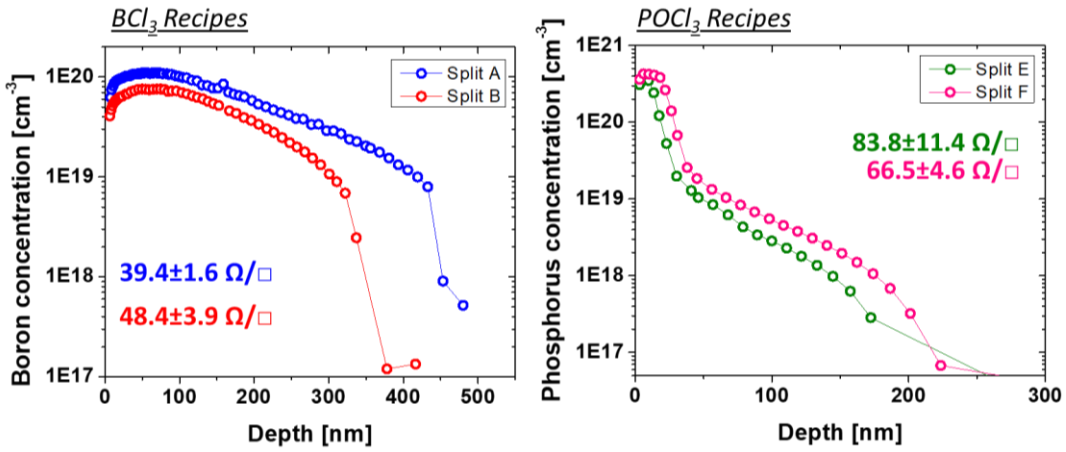


Figure 6.9. ECV profiles of the selected recipes to be used for the fabrication of TLM samples. The sheet resistance values are given as the same colors as given in the ECV plots.

After symmetrical passivation and required firing steps, iV_{oc} measurements were carried out to certify the passivation quality of the selected layers. The resulting iV_{oc} values are given in Figure 6.10.

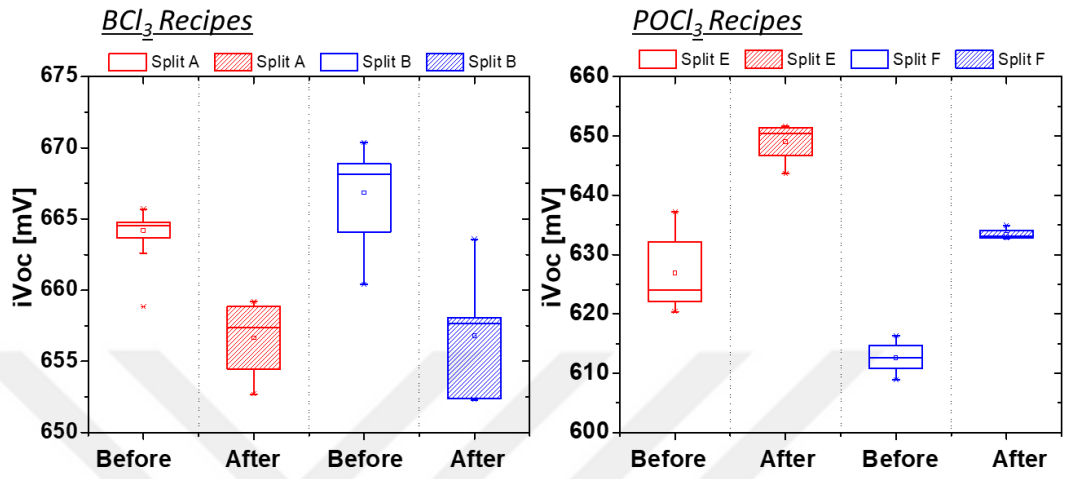


Figure 6.10. Implied Voc values of the boron and phosphorus diffused samples after passivation and after firing conditions.

Boron diffused samples passivated using PASS4 stack again showed degradation in iV_{oc} upon firing as obtained in the previous cases. Phosphorus diffused samples showed improvement upon firing. Following the metallization and firing steps, samples were cut into 1-cm strips and used for TLM measurements. The analyzed contact resistivity values are shown in Figure 6.11.

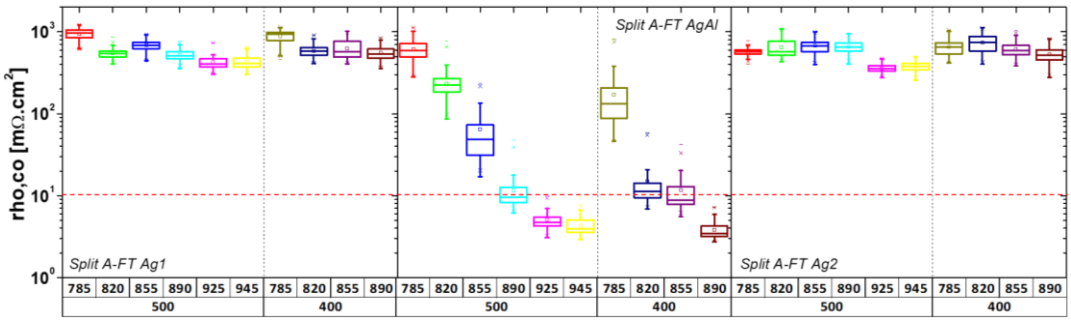


Figure 6.11. Contact resistivity values of the boron diffused samples (Split A) metalized using FT-Ag1(left), FT- AgAl(middle), and FT-Ag2(right). The applied peak firing temperature was varied from 785 to 945°C and the conveyor belt speed was varied from 500 to 400 cmpm. Dashed lines are a guide for the eye.

For both fire-through Ag pastes, the obtained contact resistivity values were of the order of 1000 mΩ.cm^2 regardless of the firing temperature and conveyor belt speed. Thus, to form proper contact on boron-doped surfaces, Al is needed as a paste ingredient. For the FT-AgAl case, 890°C was observed to be the critical temperature above which contact resistivity values dropped below 10 mΩ.cm^2 level when the conveyor belt speed was 500 cmpm. When the conveyor belt speed was reduced to 400 cmpm, the critical temperature shifted to 820°C.

Changing the boron diffusion profile from A to B resulted in a similar contact resistivity behavior as Split A as shown in Figure 6.12. Like the case of Split A, FT-Ag pastes resulted in the contact resistivity values in the order of 1000 mΩ.cm^2 for Split B.

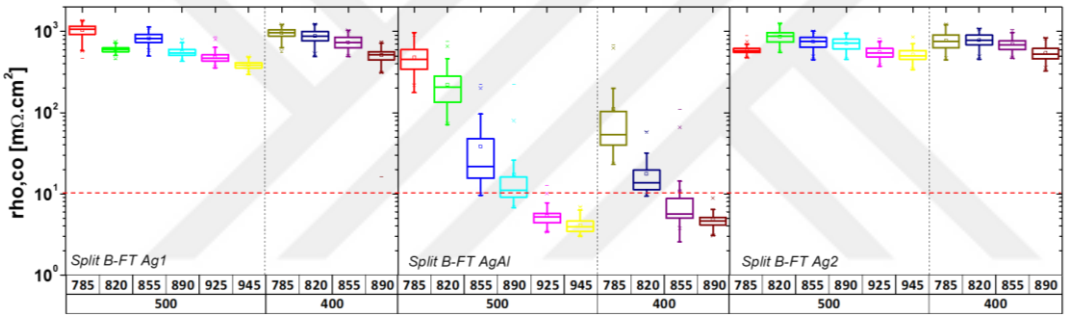


Figure 6.12. Contact resistivity values of the boron diffused samples (Split B) metallized using FT-Ag1(left), FT- AgAl(middle), and FT-Ag2(right). The applied peak firing temperature was varied from 785 to 945°C and the conveyor belt speed was varied from 500 to 400 cmpm. Dashed lines are a guide for the eye.

The temperature dependence of the measured rho,co values for the samples metalized with FT-AgAl paste was almost the same as those of Split A. Critical temperatures were 890°C and 855°C for the respective conveyor belt speeds of 500 and 400 cmpm. Thus, the peak firing temperature could be used at 890°C (for 500 cmpm) or 855°C (for 400 cmpm) if those temperatures are also suitable for n^+ doped BSF regions.

BSF regions were also metalized using the same pastes and firing parameters (i.e., peak temperature, conveyor belt speed) and the resulting contact resistivity values

are shown in Figure 6.13 for the samples of Split E. It was observed that n^+ doped surfaces could be contacted by both FT-Ag and FT-AgAl pastes.

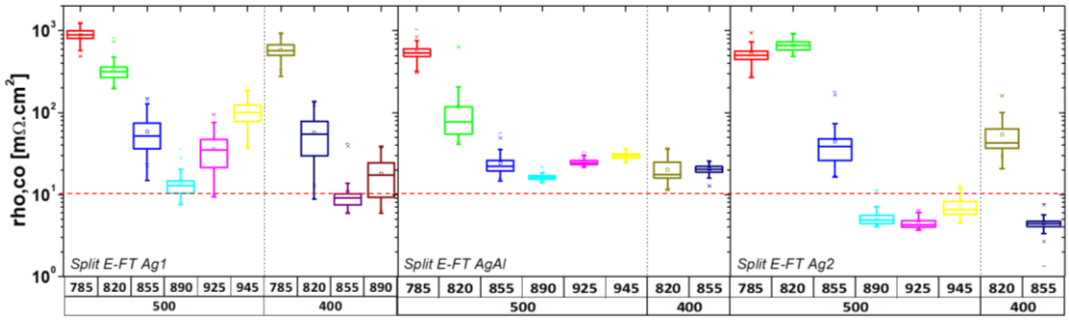


Figure 6.13. Contact resistivity values of the phosphorus diffused samples (Split E) metallized using FT-Ag1 (left), FT- AgAl (middle), and FT-Ag2 (right). The applied peak firing temperature was varied from 785 to 945°C and the conveyor belt speed was varied from 500 to 400 cmpm. Dashed lines are a guide for the eye.

For the samples metalized with FT-AgAl paste, the contact resistivity values were saturated at around 20 mΩ.cm^2. The samples metalized with FT-Ag1 paste, the corresponding contact resistivity values reduced to 10 mΩ.cm^2 when firing temperature was increased 890°C for 500 cmpm and 855°C for 400 cmpm. Further increasing the firing temperature, increased the resulting rho,co values for both conveyor belt speeds. When the samples were metalized using FT-Ag2 paste, again 890 and 855°C were observed to be the critical temperatures but with a more uniform contact resistivity distribution. Although FT-Ag2 paste was developed for polySi layers, it was also suitable for the metallization of the n^+ doped c-Si surfaces. Similar to Split E samples, Split F samples were also properly contacted both with AgAl and Ag pastes as shown in Figure 6.14. Unlike p^+ doped surfaces where Al is needed for acceptable contact resistivity values, n+ doped surfaces had no special requirements for the case of fire-through metallization. However, despite its proper contact formation properties, FT-AgAl paste could promote metal-induced recombination at the c-Si/metal interface and degrade the Voc at the cell level. Compared to Split E samples, the resulting rho,co values of the Spit F samples were more uniformly distributed. For the case of FT-AgAl paste, most of the measured values were just touching to the 10 mΩ.cm^2 line except those of the samples fired at 785 and 820°C at 500cmpm.

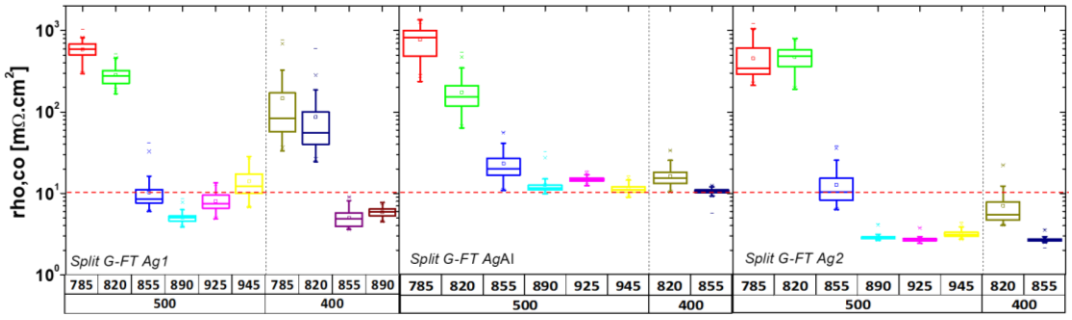


Figure 6.14. Contact resistivity values of the phosphorus diffused samples (Split E) metallized using FT-Ag1 (left), FT- AgAl (middle), and FT-Ag2 (right). The applied peak firing temperature was varied from 785 to 945°C and the conveyor belt speed was varied from 500 to 400 cmpm. Dashed lines are a guide for the eye.

Moreover, rho,co values reduced below 10 mΩ.cm^2 levels at 855°C for 500 cmpm for both FT-Ag1 and FT-Ag2 pastes while the corresponding temperatures were 855 and 820°C for the case of 400 cmpm. Thus, by the end of this section, the diffusion recipes, common passivation layer, and required firing temperature to be used at the rear side of the IBC cells were optimized.

6.3.4 Fabrication of IBC Cells

As the last task of this chapter, IBC solar cells were fabricated on n-type, M2, Cz wafers.

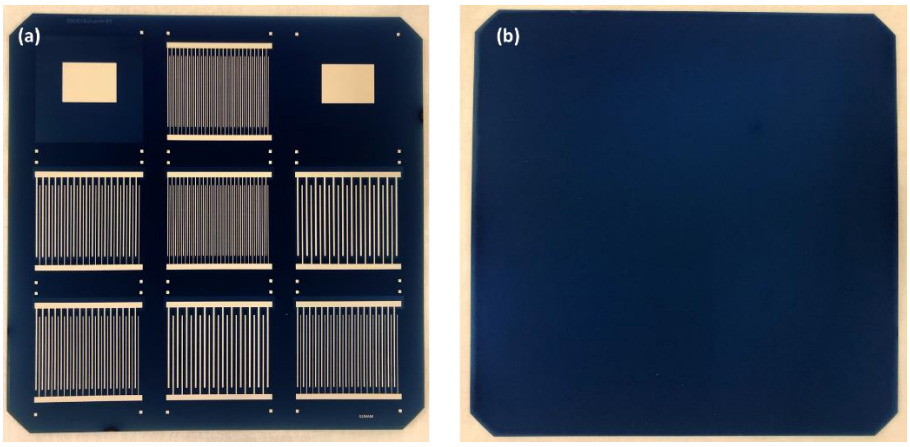


Figure 6.15. The appearance of the rear side (a) and front side (b) of the fabricated IBC cells after metallization.

The appearance of the rear side and the front side of the fabricated cells are shown in Figure 6.15.

While the cells with FFE were passivated with Al_2O_3/SiN_x and SiN_x (recipe1) layers at the front side, the cells with FSF were passivated with two different SiN_x recipes (recipe1 and recipe2). The rear sides of all cells were passivated with Al_2O_3/SiN_x based on the optimization results. The corresponding cross-sections are shown in Figure 6.16.

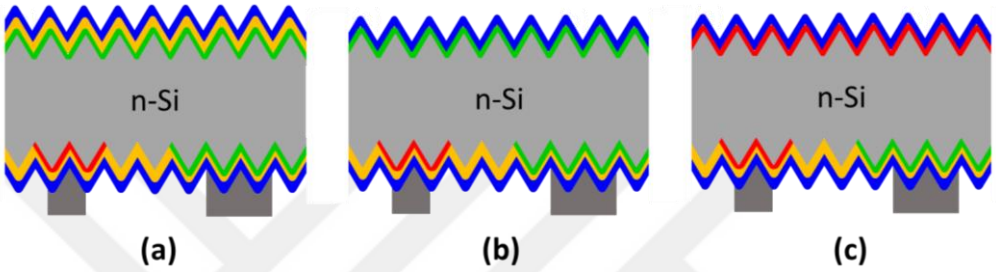


Figure 6.16. The cross-sectional views of the cells with various front surface passivation sceneries. The cells FFE with front: Al_2O_3/SiN_x (a), with FFE with front: SiN_x (b), and with FSF with front: SiN_x (c).

After the passivation, some of the half-fabricated cells were used for Sinton measurements to trace the performance till the end of the firing step. The measured iV_{oc} was analyzed as a function of the pitch of the cells with FFE which were passivated with Al_2O_3/SiN_x at the front side. The resulting iVoc values for the samples with and without a thin oxide layer between c-Si and passivation stack are shown in Figure 6.17. It was observed that putting an additional thin oxide layer did not provide any improvement in iV_{oc}. Emitter regions experienced an improvement from 630 to 648 mV upon firing which was from 611 to 620 mV for the BSF region. Considering the lower iV_{oc} values, the BSF region was determined to be the performance limiting region at the cell level. The observed improvement in iV_{oc} was also valid for the cells with the thin oxide layer but significantly suppressed for that case. IBC unit cells on the same wafers also showed improvement upon firing for all pitch values (i.e., 750, 1250, and 1700 µm). Although all cells resulted in similar iV_{oc} values, the cells with 1250 µm showed slightly higher values for both oxide cases as seen in Figure 6.17.

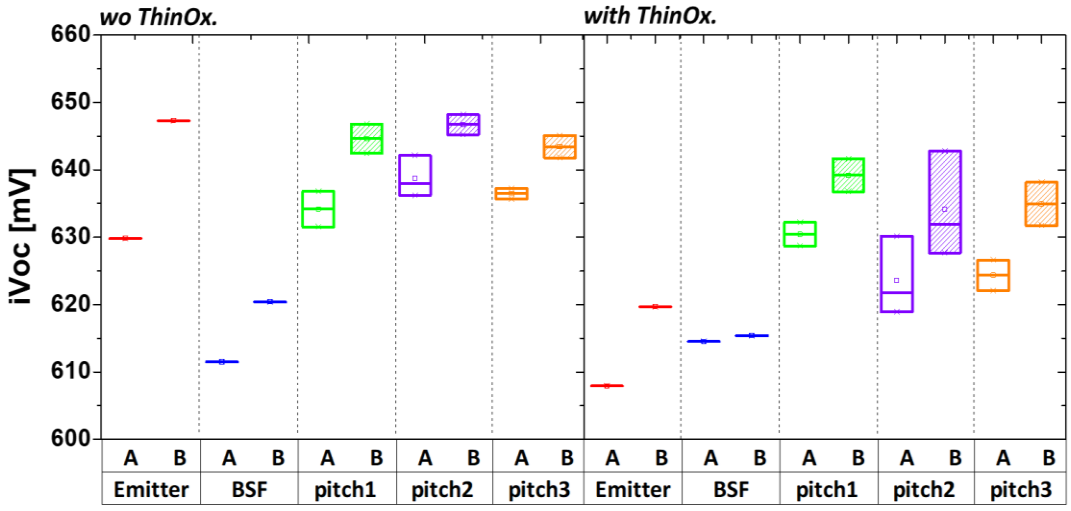


Figure 6.17. Change of iVoc for FFE-IBC cells without (left) and with (right) a thin oxide layer under passivation stack. The thin oxide layer was grown by dry oxidation at 650°C. Both front and rear surfaces were passivated using Al_2O_3/SiN_x stack. A refers to the as-deposited condition while B stays for the condition after firing at 885°C.

The average iV_{oc} values were 644.6±3.1, 646.7±1.5, and 643.4±2.3 mV for the respective pitches of 750, 1250, and 1700 µm. Replacing the front Al_2O_3/stack with the SiN_x layer significantly reduced the iV_{oc} values as seen in Figure 6.18.

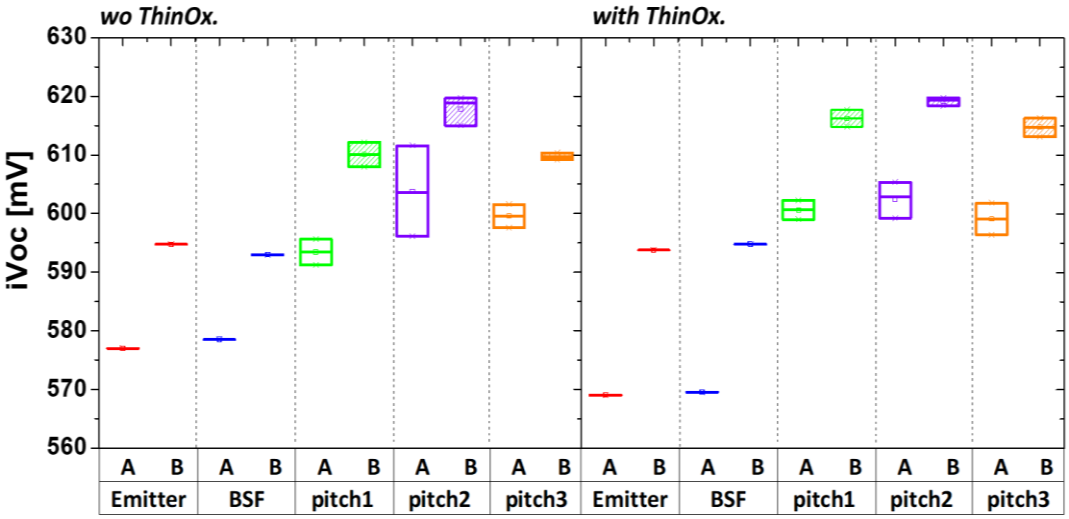


Figure 6.18. Change of iVoc for FFE-IBC cells without (left) and with (right) a thin oxide layer under passivation stack. The thin oxide layer was grown by dry oxidation at 650°C. The rear surfaces were passivated using Al_2O_3/SiN_x stack., and the front surfaces were passivated using the SiN_x layer (recipe1). A refers to the as-deposited condition while B stays for the condition after firing at 885°C.

Despite the iV_{oc} values, the performance of the BSF regions got closer to that of emitter regions. Moreover, using the thin oxide layer resulted in slightly better results for the case of BSF pattern and cell regions. Again, the cells with 1250 µm pitch resulted in higher iV_{oc} values as in the case of the cell with Al_2O_3/SiN_x passivation at the front side which was more pronounced for the latter case.

In Figure 6.18, the iVoc of the FSF-IBC cells with SiN_x (recipe1) passivation at the front side is shown. The resulting refractive index measured using a spectroscopic ellipsometer was 2.1 at 632 nm. Unlike the cells with FFE, for the case of FSF-IBC cells, the performance of the BSF region was either the same or even better than that of the emitter region. Using a thin oxide layer did not enhance the measured iV_{oc} values neither for the doped nor for the cell regions.

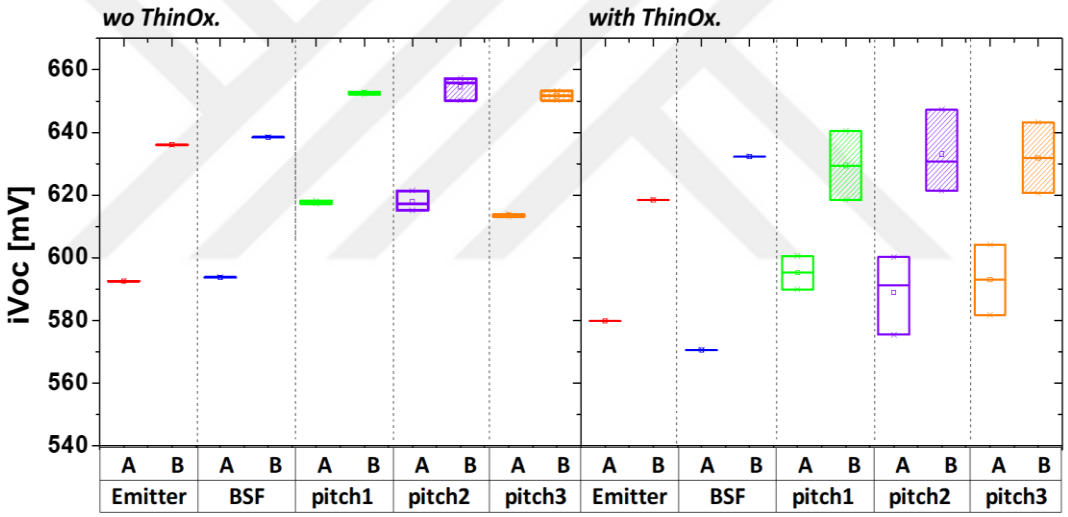


Figure 6.19. Change of iVoc for FSF-IBC cells without (left) and with (right) a thin oxide layer under passivation stack. The thin oxide layer was grown by dry oxidation at 650°C. The rear surfaces were passivated using Al_2O_3/SiN_x stack., and the front surfaces were passivated using the SiN_x layer (recipe1). A refers to the as-deposited condition while B stays for the condition after firing at 885°C.

The average iV_{oc} values were 652.5±0.5, 654.4±3.7, and 651.7±2.1 mV for the respective pitches of 750, 1250, and 1700 µm. The observed trend was the same as in the case of FFE-IBC cells, so the intermediate pitch resulted in the highest iV_{oc} values.

As the last set, the front passivation SiN_x (recipe1) was replaced with SiN_x (recipe2). The corresponding refractive index of that layer was 1.96 at 632 nm. The resulting iV_{oc} values of the emitter and BSF regions after firing were 650 and 667 mV, respectively.

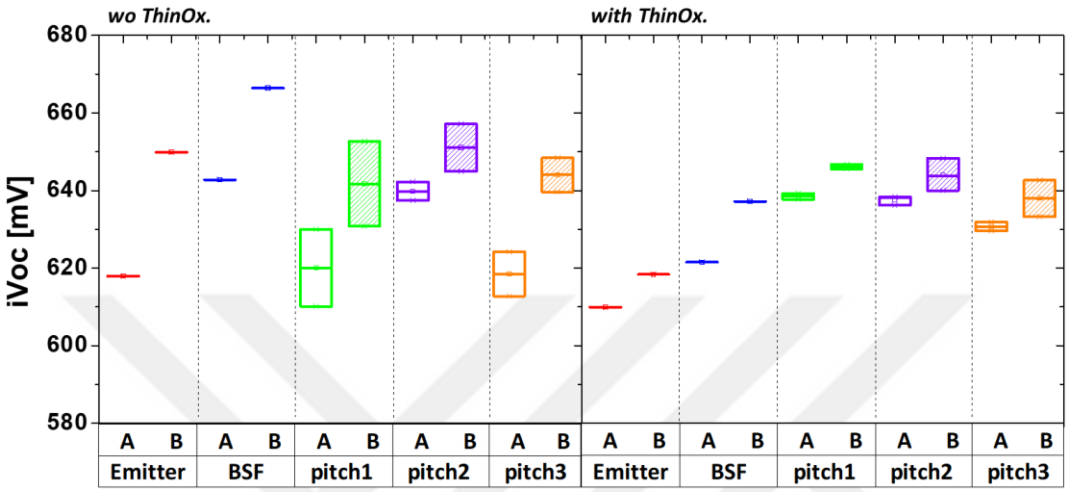


Figure 6.20. Change of iVoc for FSF-IBC cells without (left) and with (right) a thin oxide layer under passivation stack. The thin oxide layer was grown by dry oxidation at 650°C. The rear surfaces were passivated using Al_2O_3/SiN_x stack., and the front surfaces were passivated using the SiN_x layer (recipe2). A refers to the as-deposited condition while B stays for the condition after firing at 885°C.

Despite greater iV_{oc} values of the emitter and BSF regions, the iV_{oc} values of the cell regions were lower than expected. The average iV_{oc} values were 641.7±15.5, 651.1±8.6, and 644.1±6.2 mV for the respective pitches of 750, 1250, and 1700 µm. The trend was kept the same for the cells with a thin oxide layer but with relatively lower iV_{oc} values.

6.3.4.1 Electrical Characterization of the IBC Cells

Following the metallization and co-firing, current-voltage characteristics were traced for the cells of approximately 3 cm^2. For the first set of samples, boron-doped regions were contacted with FT-AgAl paste while the phosphorus-doped regions were contacted using FT-Ag2. The results were analyzed as a function of pitch, front side doping, and firing temperature.

Efficiency and fill factor values of FFE-IBC cells with Al_2O_3/SiN_x passivation at the front side are shown in Figure 6.21. The highest efficiency values were 19.2, 18.2, and 18.3% for the respective pitches of 750, 1250, and 1700 µm.

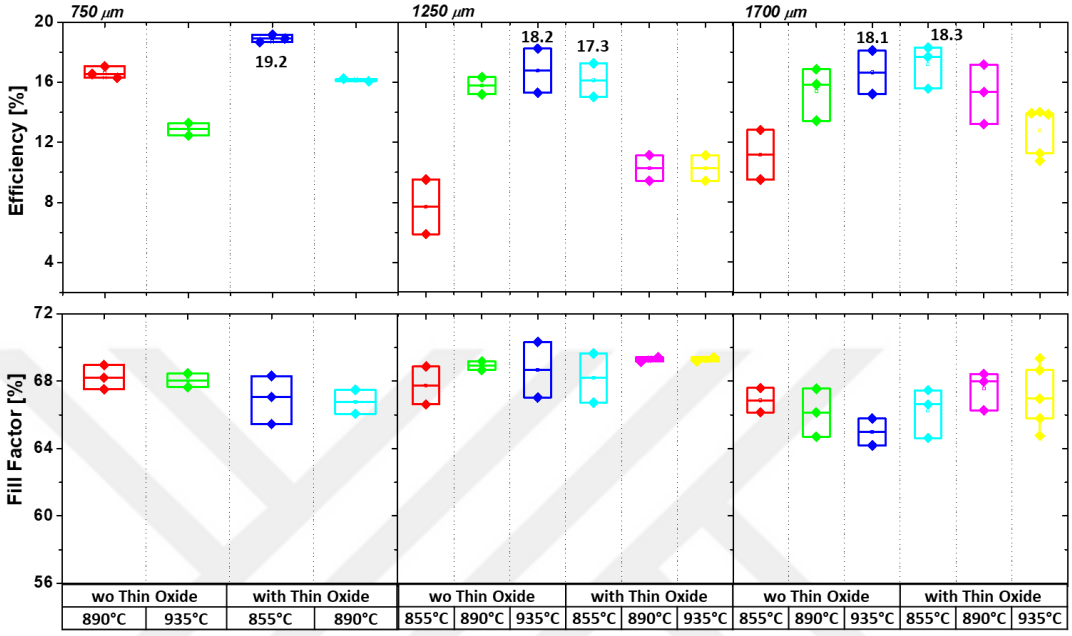


Figure 6.21. Efficiency and fill factor of FEE-IBC cells for 750, 1250, and 1700 µm pitches, and fired at various temperatures. The front surfaces of the cells were passivated using Al_2O_3/SiN_x stack.

Despite the promising efficiency values, some of the samples resulted in significantly low-efficiency values while corresponding fill factor (FF) values lying within the range of 66-70% for all samples. Low FF values were one of the main factors limiting cell efficiency.

In Figure 6.22, analyzing the open-circuit voltage (V_{oc}) values as a function of changing pitch revealed that the cells with the intermediate pitch were still holding the highest V_{oc} values as in the case of iV_{oc} measurements.

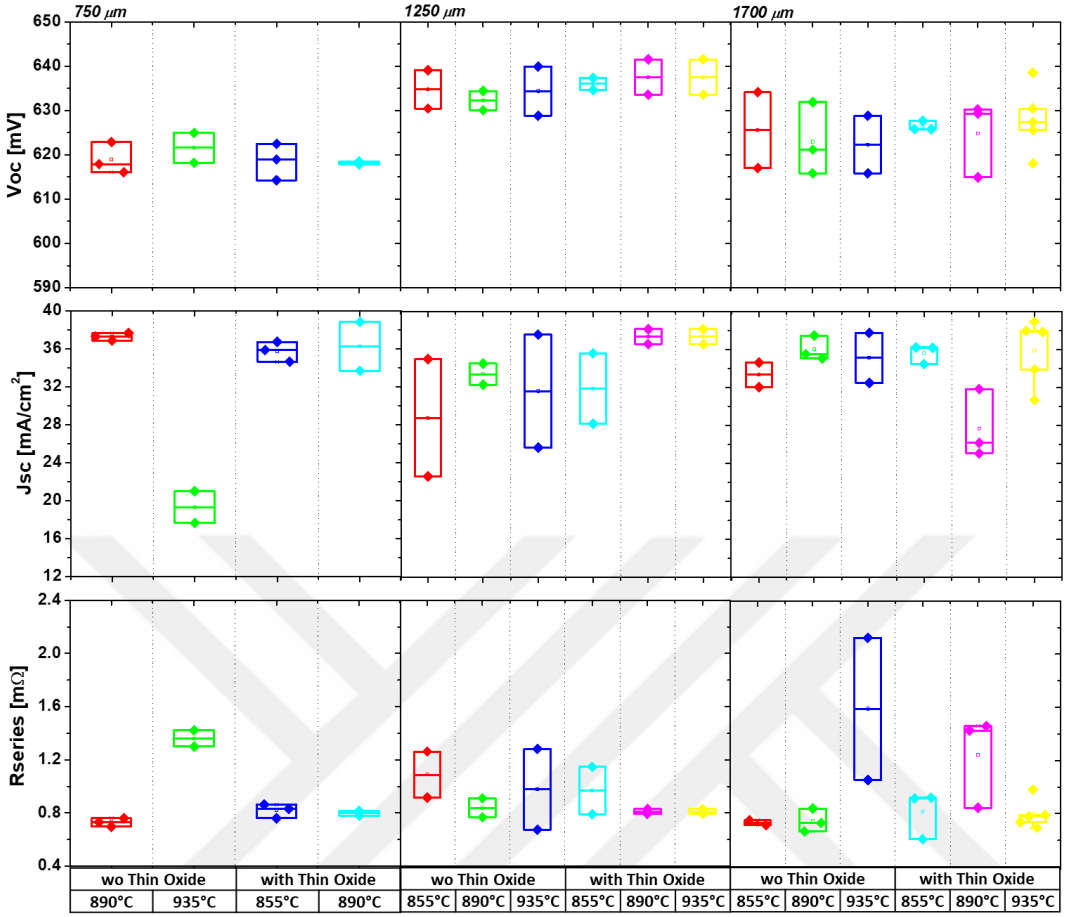


Figure 6.22. Open circuit voltage, short circuit current density, and series resistances of FEE-IBC cells for 750, 1250, and 1700 µm pitches, and fired at various temperatures. The front surfaces of the cells were passivated using Al_2O_3/SiN_x stack.

For some of the samples, short circuit density (J_{sc}) values were below 30 mA/cm^2 level. Correlating low J_{sc} values with the series resistance (R_{series}) revealed that when the R_{series} was above 1.0 mΩ the Jsc value was significantly reduced. However, no direct correlation between R_{series} and FF could be established. Replacing the front side Al_2O_3/SiN_x stack with the SiN_x layer resulted in significantly lower efficiency values as seen in Figure 6.23. For most of the measured cells, FF values were significantly lower than in the previous case. Although the lower FF values could be related to increased series resistance, putting the SiN_x layer with positive fixed charges would also have induced an inversion layer at the p^+ doped FFE region.

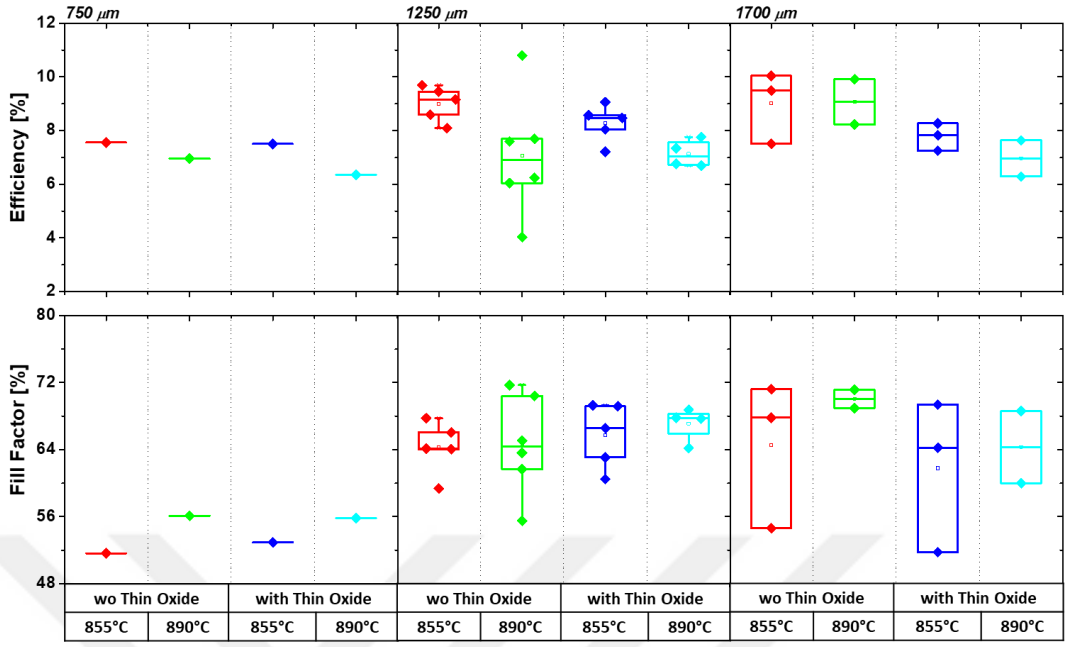


Figure 6.23. Efficiency and fill factor of FFE-IBC cells for 750, 1250, and 1700 µm pitches, and fired at various temperatures. The front surfaces of the cells were passivated using SiN_x (recipe1) layer.

Since the FFE region was introduced to provide a conductive channel for the minority carriers (holes for n-Si based cells), any capping layer with positive fixed charges would induce an inversion layer at the n-Si interface and repel the holes back to the bulk Si instead of laterally transport them [85]–[88]. This would explain the degraded cell performance for the case of SiN_x passivation instead of Al_2O_3/SiN_x.

The V_{oc}-pitch relation was like that of the half-fabricated cells so that the intermediate pitch, 1250 µm, had the highest V_{oc} values amongst the others as seen in Figure 6.24. The most explicit relation was the one between the series resistance and short circuit current density. The higher R_{series} resulted in lower J_{sc} values. The samples with a thin oxide layer did not experience a significant increase in the R_{series} compared to their counterparts without a thin oxide layer. Moreover, increasing firing temperature increased R_{series} when there was no thin oxide layer under the passivation stack. On the contrary, when there was a thin oxide layer,

increasing firing temperature did not increase the series resistance as seen in Figure **6.24**.

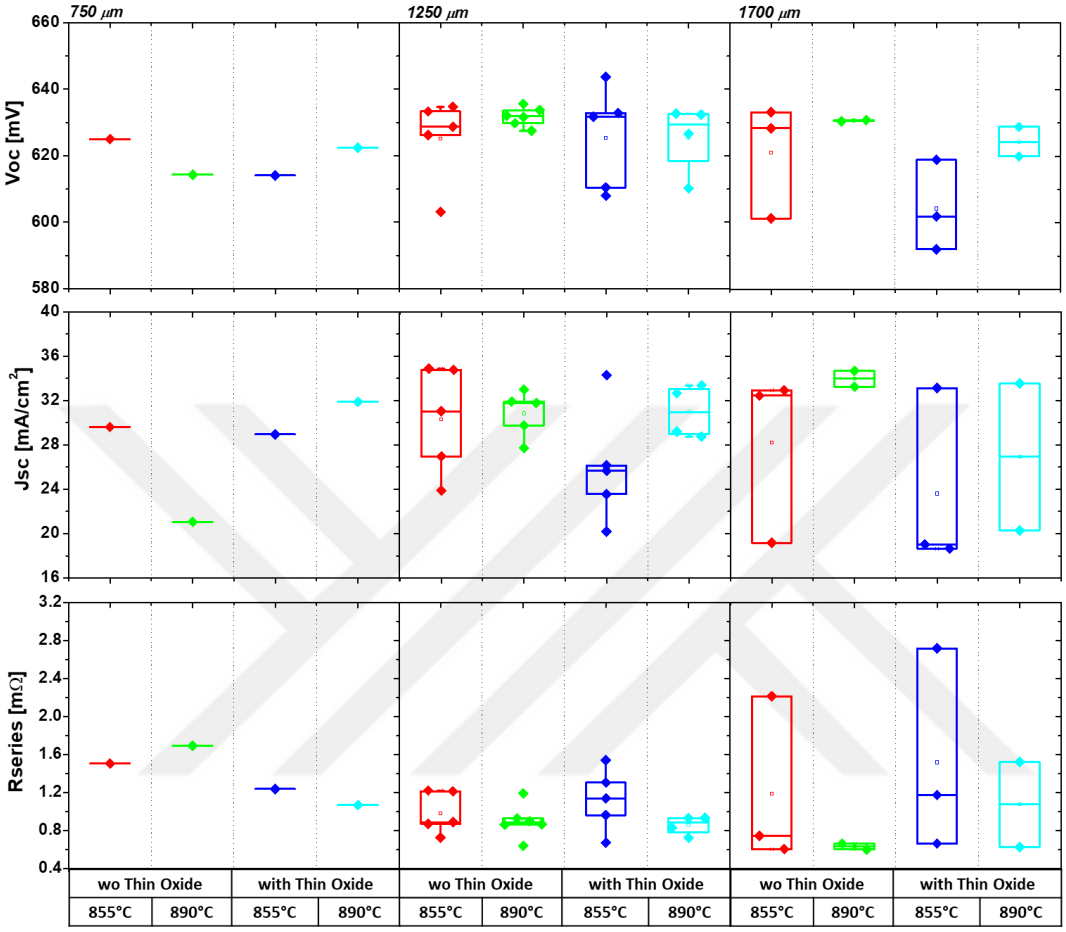


Figure 6.24. Open circuit voltage, short circuit current density, and series resistances of FFE-IBC cells for 750, 1250, and 1700 µm pitches, and fired at various temperatures. The front surfaces of the cells were passivated using SiN_x (recipe1) layer.

For the case of FSF-IBC cells with SiN_x (recipe1) passivation at the front side showed promising cell efficiencies as shown in Figure 6.25. The highest efficiency values came from the cells with 1250 and 1700 µm pitch as 19.3%. The cells with the smallest pitch had lower efficiency and fill factor values compared to others. The fill factor values were relatively higher compared to those of FFE-IBC cells.

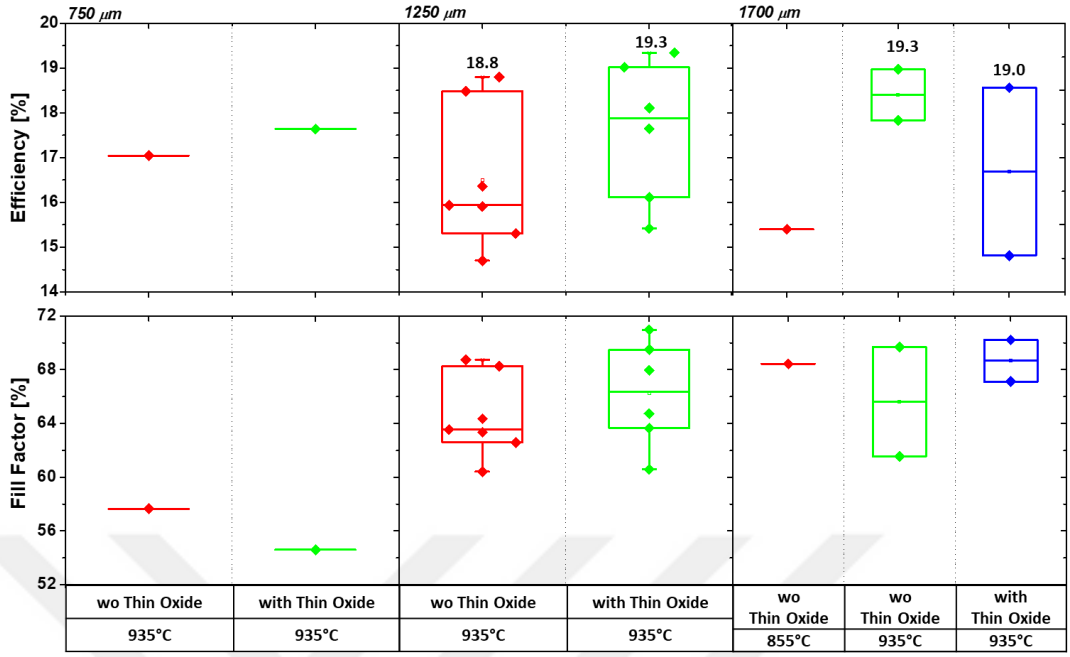


Figure 6.25. Efficiency and fill factor of FSF-IBC cells for 750, 1250, and 1700 µm pitches, and fired at various temperatures. The front surfaces of the cells were passivated using SiN_x (recipe1) layer.

The highest cell Voc was again obtained from the cells with the intermediate pitch (1250 µm) which were followed by the cells with the largest pitch as shown in Figure 6.26. Unlike the FFE-IBC cells with a degrading performance for increased firing temperatures, FSF-IBC cells were observed to be more resistive against increasing firing temperatures. As in the case of FFE-IBC cells, the negative effect of increasing firing temperature on series resistance for the samples without thin oxide layers was observed for the case of FSF-IBC cells, too.

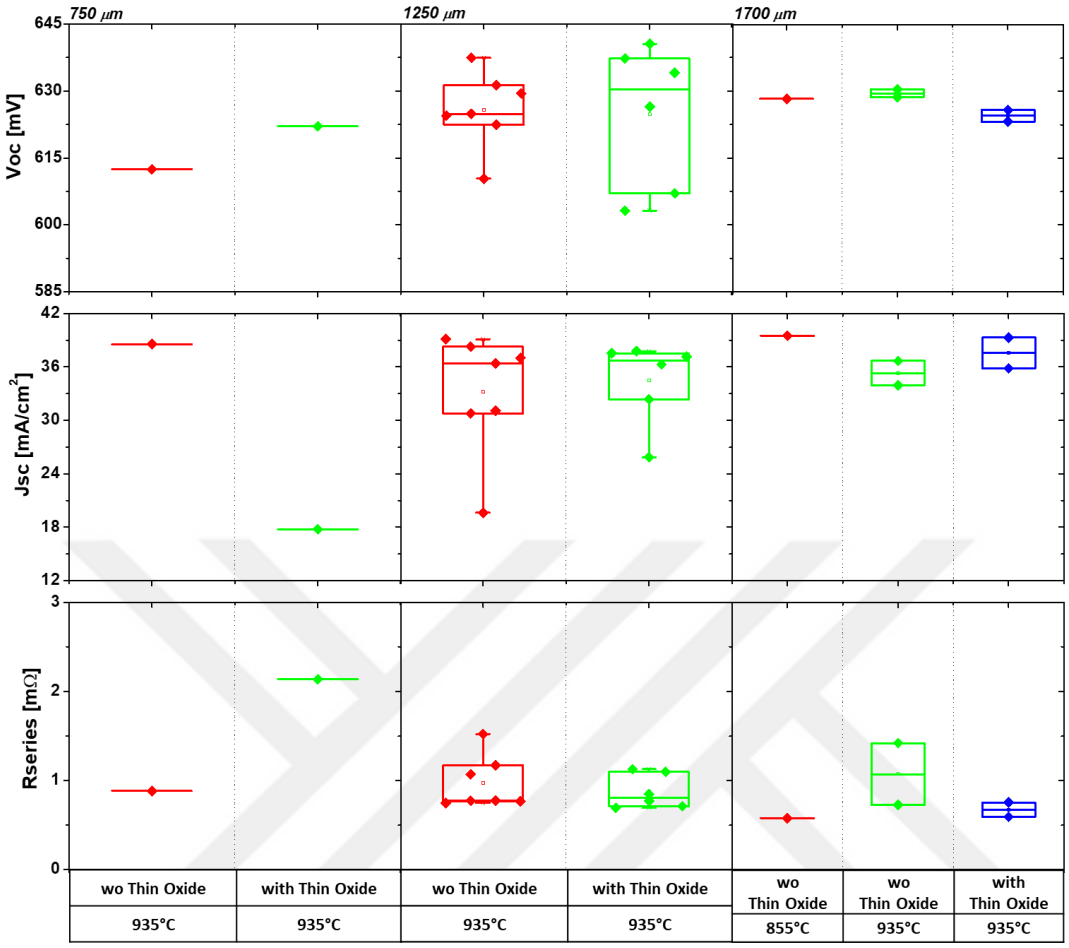


Figure 6.26. Open circuit voltage, short circuit current density, and series resistances of FSF-IBC cells for 750, 1250, and 1700 μm pitches, and fired at various temperatures. The front surfaces of the cells were passivated using SiN_x (recipe1) layer.

As the last set of samples, front (SiN_x (recipe1)) passivation of FSF-IBC cells was replaced with SiN_x (recipe2) which did not generate a significant difference in the cell performance as shown in Figure 6.27. Similar to the previous case, the highest efficiency was obtained as 19.2% for the largest pitch. The obtained FF values were as low as those obtained in the previous sections of this chapter.

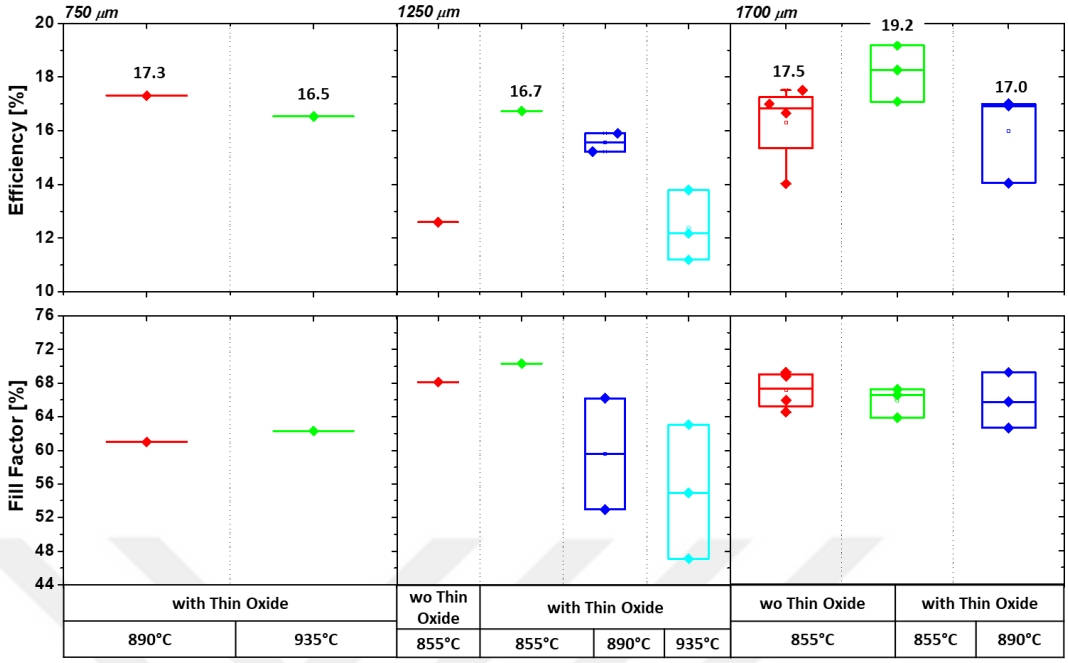


Figure 6.27. Efficiency and fill factor of FSF-IBC cells for 750, 1250, and 1700 µm pitches, and fired at various temperatures. The front surfaces of the cells were passivated using SiN_x (recipe2) layer.

The highest V_{oc} values reached at 640 mV level by the cells with 1250 µm pitch as seen in Figure 6.28. Increasing firing temperature was observed to reduce V_{oc} which was less pronounced for the cells with a thin oxide layer. Like the previous cases, when R_{series} was above 1 mΩ level, J_{sc} values were significantly reduced.

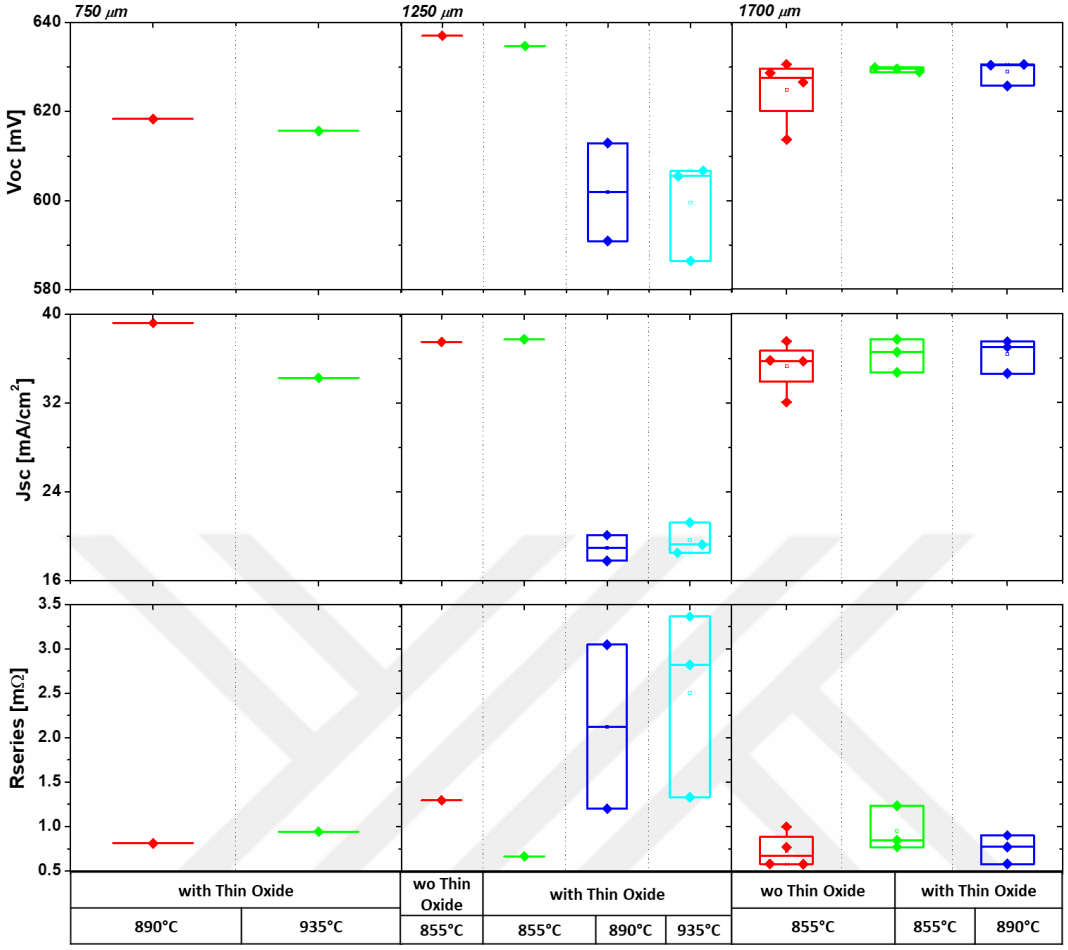


Figure 6.28. Open circuit voltage, short circuit current density, and series resistances of FSF-IBC cells for 750, 1250, and 1700 µm pitches, and fired at various temperatures. The front surfaces of the cells were passivated using SiN_x (recipe2) layer.

The current density-voltage characteristics of the best-performing cells are given in Figure 6.29. It was observed that both FFE-IBC and FSF-IBC cells, suffered high series resistance and low shunt resistance. The difference between pitches was almost negligible. The best performing cells were metallized with FT-Ag2 paste on the BSF and FT-AgAl paste on the emitter region, respectively.

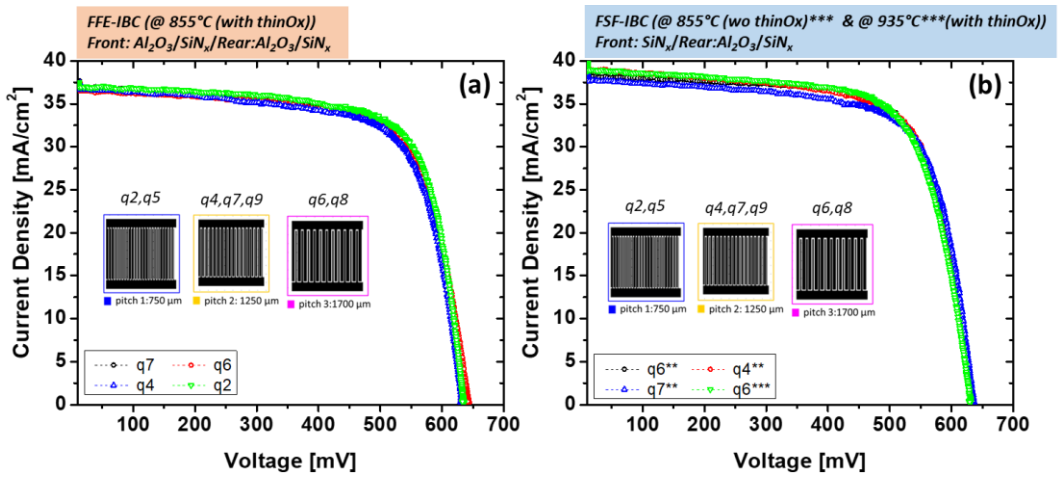


Figure 6.29. The current density-voltage characteristics of the best performing FFE-IBC (a) and FSF-IBC (b) cells.

Replacing the FT-Ag2 paste with FT-Ag1 did not help to enhance the cell performance. Although the resulting series resistance at the cell level was reduced to one-third of its previous version for the case of FT-Ag1 pastes, the corresponding fill factor values pinned at around 69-71% scale. Thus, the reason for the reduced shunt resistance and fill factor values was not only related to the metallization. The important cell parameters of the best performing cells are summarized in Table 6.3.

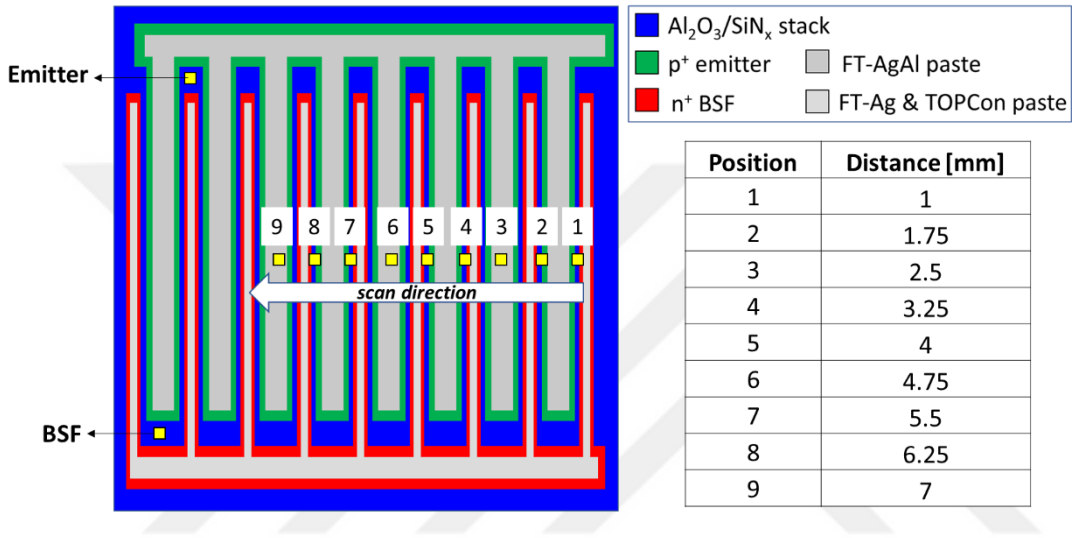
Table 6.3. Important cell parameters of the selected IBC solar cells.

Structure	Quarter	Eff. [%]	FF [%]	Jsc [mA/cm^2]	Voc [mV]	Rseries [mΩ]	Rshunt[Ω]
FFE	q7	18.5	70.4	36.9	631	0.68	109
	q6	18.3	69.4	36.5	642	0.83	98
	q4	17.5	69.7	35.3	630	0.73	79
	q2	18.8	71.2	37.0	633	0.60	137
FSF	q6	18.8	69.2	38.1	634	0.79	133
	q4	19.1	68.9	39.0	630	0.66	74
	q4	18.9	70.3	37.7	635	0.67	78
	q6	19.2	68.3	39.7	629	0.77	85

As the last measurement of this chapter EQE measurements were carried out to understand the reason for limited cell performance. The details of the EQE scan

procedure are given in Figure 6.30 together with the color codes of each region at the rear side of the fabricated IBC cells.

Scanning in the directions perpendicular to the unit cell finger would give information about the performance losses. Measurements in the gap regions close to the emitter and BSF busbars respectively would help to realize the performance limiting region in the final device structure.



Position	Distance [mm]
1	1
2	1.75
3	2.5
4	3.25
5	4
6	4.75
7	5.5
8	6.25
9	7

Figure 6.30. Details of the external quantum efficiency scan procedure and the rear side of the fabricated IBC cells.

As the first set of measurements, two different cells were chosen. One of the cells had a high efficiency while the other one had a significantly lower efficiency value. To make the plots more comprehensive, EQE signals are given for selected positions. In Figure 6.31, EQE spectra measured for the emitter, BSF, P1, P2, and P3 regions are given for two different cells.

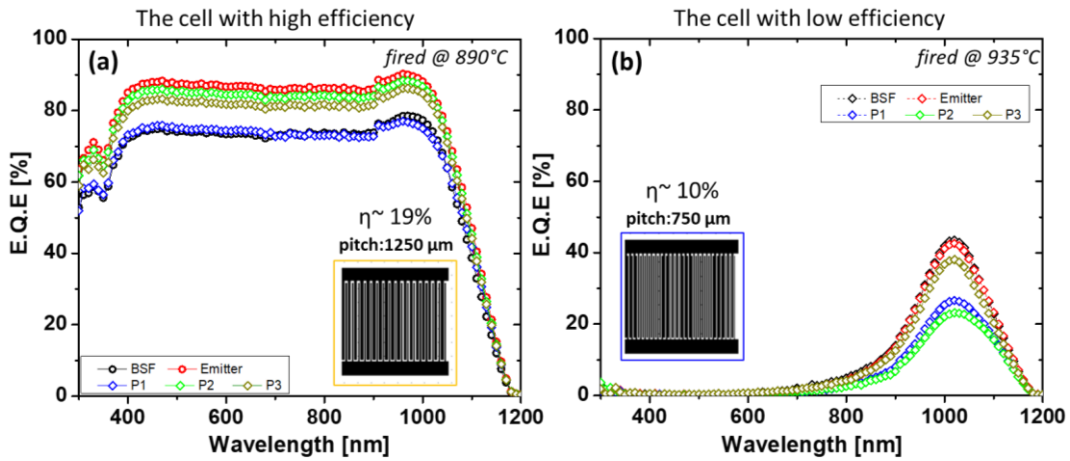


Figure 6.31. External quantum efficiency spectra over different positions for the FSF-IBC cell with high efficiency (a) and FFE-IBC low efficiency (b). P1, P2, and P3 refer to the respective stage positions of 1, 4, and 6.25 mm.

For the cell with high efficiency shown in Figure 6.31 (a), the highest signal was obtained for the collecting emitter region while the lowest came from the non-collecting BSF region as expected [18], [89], [90]. The corresponding signal level was around 87-88% for the emitter and 74-75% for the BSF regions. Spectra belonging to the other positions were lying between those of emitter and BSF regions. The bump in the signal at around 910 nm was observed for all regions and could be due to the back reflection from the metalized regions. In Figure 6.31 (b), the low wavelength signal was almost zero for the cell with low efficiency. The detectable signal was almost completely coming from the rear side of the device with a maximum EQE of 44% at around 1020 nm. Observed reduced signal could be related to the loss of passivation at the front side upon firing at 935°C. Degradation of passivation of the boron-doped surfaces passivated with Al_2O_3/SiN_x stacks was also observed in the previous sections throughout the thesis. To better understand that observed degradation, an FSF-IBC cell with SiN_x passivation at the front side and fired at 935°C was also analyzed. It was observed that firing at 935°C had detrimental effects both on FFE-IBC and FSF-IBC cells which was more pronounced for the former case. That was mainly related to the degradation of passivation at the Al_2O_3/SiN_x passivated surfaces. The FFE-IBC cells had

degradation not only at the front but also at the rear surface as seen in Figure 6.32 (b). The degradation at the front surface passivation completely reduced the short wavelength response of the cells. The degradation at the rear side was also significant but the existence of n^+ doped BSF regions help to collect some of the generated carriers with a reduced probability.

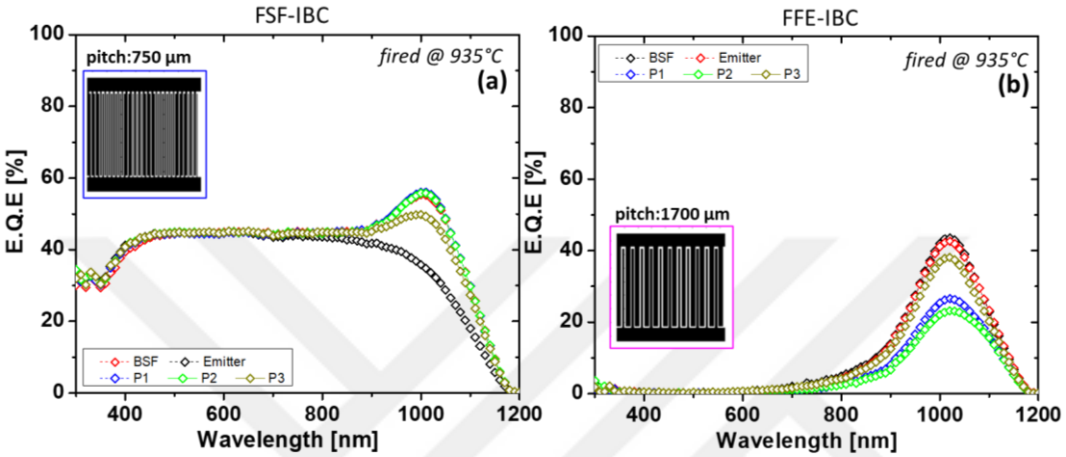


Figure 6.32. EQE spectra of FSF-IBC (a) and FFE-IBC (b) cells fired at 935°C.

For the case of FSF-IBC cells, the degradation was still valid but less pronounced as seen in Figure 6.32 (a). When the FFE-IBC cells were analyzed, it was speculated that the degradation was only at Al_2O_3/SiN_x passivated regions with a more pronounced effect on the boron-doped layers. However, considering the reduced signal of the FSF-IBC cells revealed that the degradation at the front surface was not eliminated. Although the signal level for the short wavelength regime was reduced, it was still significantly higher compared to FFE-IBC cells. Thus, it was not only Al_2O_3/SiN_x passivated but also SiNx passivated layers degrading upon firing at such a high temperature. However, it could be said that the n^+ doped layer passivated either by Al_2O_3/SiN_x or SiN_x layers were more stable against high-temperature process steps. This is due interaction of supplied hydrogen with available boron atoms [91], [92].

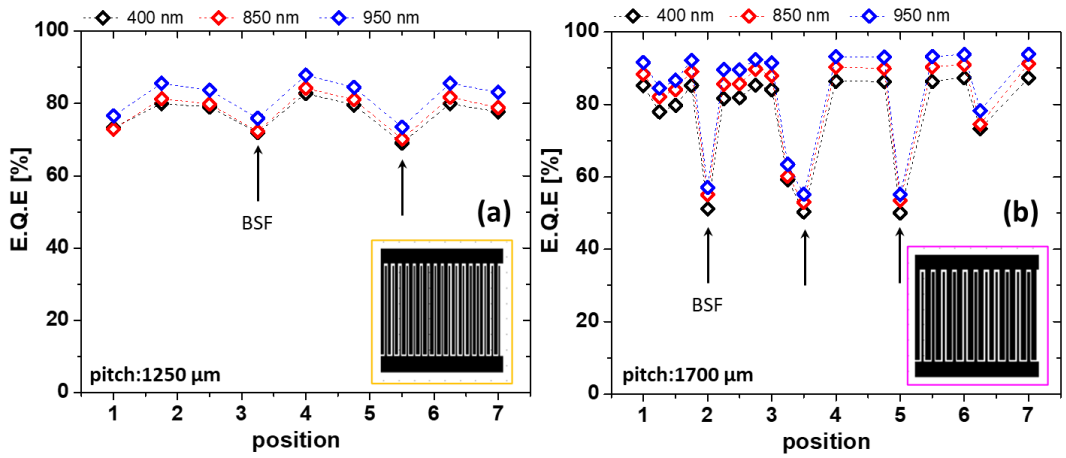


Figure 6.33. Spatial distribution of EQE signal for the selected wavelengths. Measurements were done on FSF-IBC cells with pitch:1250 µm (a) and pitch:1700 µm (b).

In Figure 6.33, the spatial distribution of EQE signals is shown for the selected wavelengths of 400, 850, and 950 nm. EQE responses got better for the longer wavelengths for both pitches. The minima of the curves correspond to the non-collecting BSF junction while the maxima correspond to the collecting emitter region.

To sum up, efficiency values at around 19.2-19.3% could be reached by both FFE-IBC and FSF-IBC structures. The low fill factor values could not be solved by changing the metal paste used for BSF metallization. Thus, despite the promising cell performance, the developed cell structure still requires further development.

CHAPTER 7

POLYSILICON PASSIVATING CONTACT SOLAR CELLS

In the second part of this thesis, passivating contact solar cells utilizing ex-situ doped polysilicon layers will be studied. The deposited layers will be analyzed in terms of their passivating and contacting properties. Extraction of contact recombination current density using different methods will also be focused on. As the final task polySi passivating cells will be fabricated and characterized.

7.1 Introduction

The optimization of the cell processes, using high-quality Si-wafers and more sophisticated cell structures resulted in higher conversion efficiencies. However, increasing cell efficiencies made the recombination losses at the metal-semiconductor interfaces the key factor limiting the cell efficiencies [93], [94]. To suppress the recombination losses at the metal interfaces, a new concept named "passivating contact" has been developed which could basically be divided into two categories depending on the utilized material type. Either silicon-based thin films or materials with extreme work functions could be utilized for passivating contact structures [95].

The stack use of doped/undoped a-Si:H layers for the silicon heterojunction cell architecture (SHJ or HIT) resulted in the most efficient cells with a record cell efficiency of 26.6 % [32], [96]. Although their extreme performance, SHJ cell structure has its downsides associated with the use of thin a-Si:H layers. The use of a-Si:H results in absorption losses [97] and thermal stability issues preventing the application of high-temperature process steps afterwards [98].

Another Si-based passivating contact structure is SiO_x/polySi which is a long-known technology in the semiconductor industry and has recently emerged as a promising passivating contact structure for c-Si solar cells [99]. In this cell structure doped polySi layer is combined with an ultra-thin SiO_x layer to provide surface passivating. While SiO_x layer, typically grown by thermal or wet chemical oxidation, reduces the D_{it} (density of interface trap states) at the c-Si/SiO_x interface and provides chemical passivation, it also acts as a diffusion barrier against the dopant atoms stored in the doped polySi layers [100], [101]. SiO_x/polySi passivated structures are known with different names like tunnel oxide passivated contact (TOPCon) [102], [103], polysilicon on oxide (POLO) [45], [104], and passivated emitter and rear poly-silicon (PERpoly) [105]. There are various methods to grow the interfacial oxide layer like plasma-assisted oxidation, wet chemical oxidation using hydrochloric acid or nitric acid solutions, thermal oxidation and UV/O_3 oxidation [106], [107]. Like the oxide layers, polySi layers could also be obtained using different methods like PECVD deposition followed by a high temperature annealing, LPCVD deposition and PVD deposition. Moreover, the layers could either be doped during the deposition or via an additional high temperature diffusion or ion implantation step following the deposition step [95].

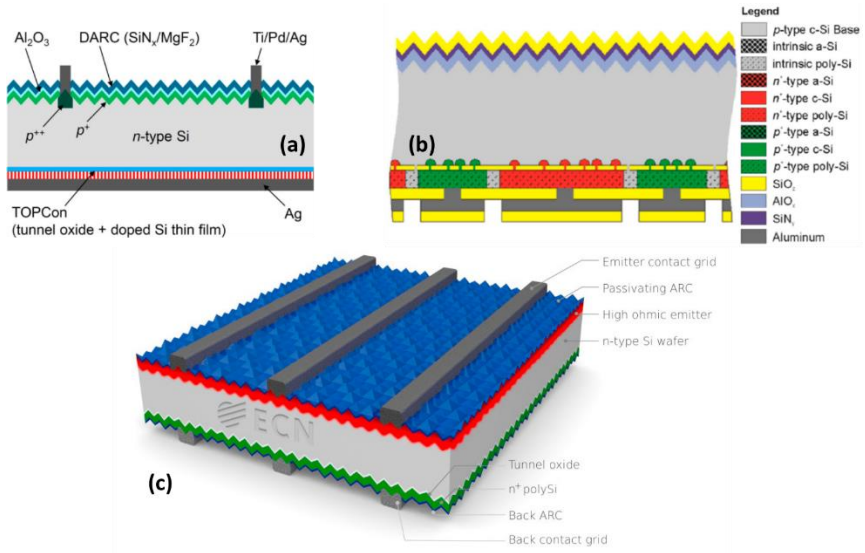


Figure 7.1. Cross-sectional views of TOPCon (a)[95], POLO (b)[95], and PERPoly (c)[105] type solar cells.

The TOPCon cells with the cross-section shown in Figure 7.1 (a) reached at an efficiency of 25.7% with the corresponding V_{oc} of 725 mV, FF of 83.3%, and J_{sc} of 42.5 mA/cm^2 [103]. For the case of POLO cells, shown in Figure 7.1 (b), extremely low recombination current density *(J_0)* values of 1 fA/cm^2 and 4 fA/cm^2 were obtained for n^+ POLO and p^+ POLO layers, respectively. A record efficiency on p-type Si wafers of 26.1% was announced in 2018 which was 24.25% for n-type Si wafers [108]. The record efficiency was updated as 26.1% in 2020 [44]. In Figure **7.1** (c), the cross-sectional view of a PERPoly cell is given. The record efficiency on 6" Cz wafers with an industrial boron emitter at the front and n-polySi BSF at the rear, was announced as 21.3% with the corresponding cell V_{oc} of 679 mV [105].

As the second type of materials, transition metal oxides, alkali/alkaline metals, oxides, salts and organic materials with their extreme work functions could also be used for the cells with passivating contacts [109].

In this chapter of the thesis, ex-situ doped polySi layers will be studied in terms of their passivation and contacting properties. Effect of doping level, layer thickness, surface morphology and applied metallization paste will be examined analyzed to extract $J_{0,contact}$ values. Finally, the best performing layer properties and metallization scenario will be used to fabricate passivating contact cells.

7.2 Experimental Details

7.2.1 Non-Fire-Through Metallization of the Doped polySi Layers and Their Passivating Properties

As the first set of samples for passivating contact studies at the Energy Research Center of the Netherlands (ECN), both phosphorus (P) doped n-poly and boron (B) doped p-polysilicon (Si) layers were deposited on 5 Ω.cm, chemically polished, 156x156 mm^2, n-Cz wafers. Following the surface etching and subsequent cleaning

steps, intrinsic polySi layers were deposited with different thicknesses (50, 100 and 200 nm) using an industrial LPCVD system from Tempress. During i-polySi deposition, a thin SiO_x layer is naturally formed between the n-Cz and i-polySi layer which act as the tunnelling oxide layer in the final structure. While ex-situ $POCl_3$ diffusion was applied for n-polySi layers, BBr_3 diffusion was carried out to have p-polySi layers. Both $POCl_3$ and BBr_3 diffusions were carried out in reduced pressure systems from Tempress at respective temperatures of 850°C and 880°C. In addition to polished wafers, p-polySi layers of various thicknesses were also deposited on textured wafers with the same properties as polished ones. Surface passivation of symmetrically processed samples was provided by 75-80 nm SiN_x layers. In addition to $POCl_3$ diffusion, phosphorus implantation was also applied for the fabrication of n doped polySi layers. The implant dose was $2x10^{15}$, $5x10^{15}$ and $1x10^{16}$ cm^{-2} for respective i-polySi thicknesses of 50, 100 and 200 nm aiming for similar doping levels for all polySi layers. Activation of the implanted phosphorus was carried out at the same temperature as BBr_3 diffusion which was 880°C. Implanted samples were included to verify the effect of the BBr_3 diffusion process on the activation and over-compensation of the implanted phosphorus. Then, screen printing was applied for the metallization of the samples using non-fire through (NFT) metal pastes. For the metallization, two different NFT pastes were utilized for both n-poly and p-polySi layers. While the first paste was named L9246 by one supplier, the other one was known by the name PVD2B. Metallized samples were exposed to five different curing temperatures of 610, 620, 630, 640, 650°C for L9246 and 560, 570, 580, 590, 600°C for PVD2B. Then, the samples were laser cut into 1-cm width stripes and TLM measurements were carried out to analyze the contact resistivity.

Fabricated symmetrical samples were characterized using Sinton WCT120 Lifetime tester, GreatEyes LumiSolar Cell photoluminescence system, WEP CVP21 Wafer Profiler for ECV measurements, PVTools TLM-SCAN+ for TLM analysis and SunLab Sherescan for sheet resistance measurements. The corresponding design of the experiment is shown in Figure 7.2.

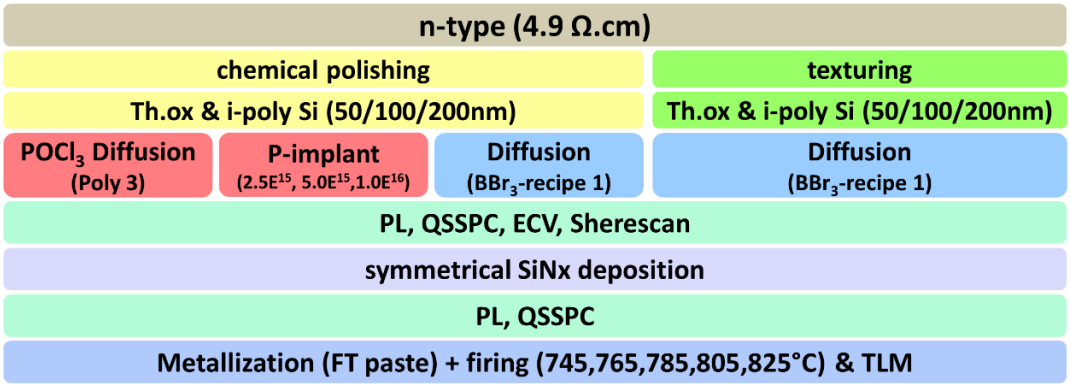


Figure 7.2. Details of the first passivating contact study conducted to understand the metallization of the doped polySi layers with non-fire through paste.

7.2.2 Fire-Through Metallization of the Doped polySi Layers and Understanding the Contact Formation Mechanisms

As the second part of the ECN study, a new set of samples were prepared on 4.9 Ω.cm, polished & textured, n-Cz wafers. Different than the first set, the polySi layer thickness was set to be 75, 125 and 200 nm for this set. Again, $POCl_3$ and BBr_3 diffusions were conducted to obtain n-poly and p-polySi layers both on chemically polished and alkaline textured n-wafers. Unlike the first set, industrial fire through (FT) metal pastes were used for the metallization of the samples. A new screen to print small-cell areas with varying metal fractions was designed and utilized for metallization. The metal pitch was varied from 0.25, 0.5, 1, and 2 mm. On the same screen in addition to small area cells, TLM patterns were also placed so that contact resistivity measurements would be carried out. The corresponding screen design and an exemplary printed sample are shown in Figure 7.3.

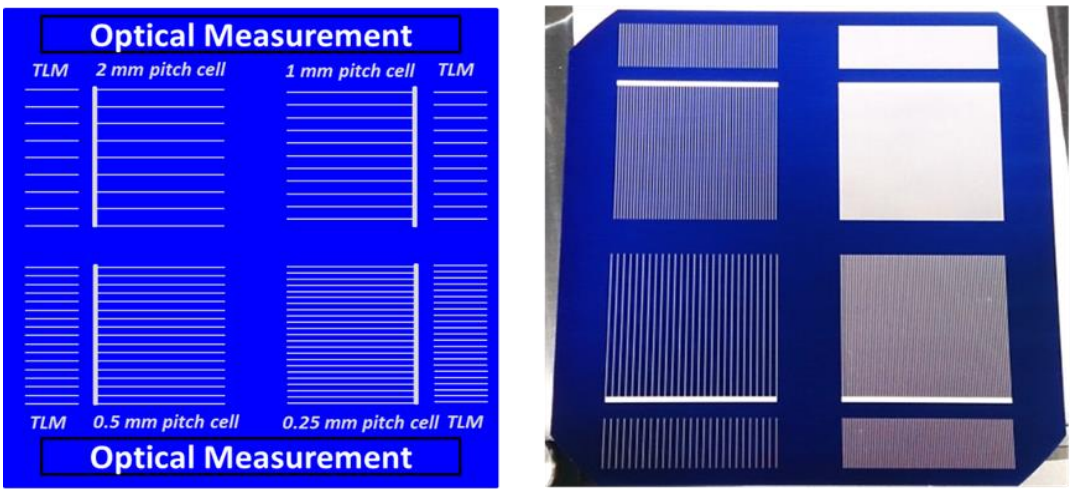


Figure 7.3. Designed screen for cells with different pitches (left), the image of a printed sample using designed screen (right).

The edges of the designed screen were intentionally left empty for optical measurements while the center was aimed to be used for PCD measurements after metallization. For the metallization of p-polySi layers, FT-AgAl (L9724) paste was used while FT-Ag (PV18A) paste was used for n-polySi layers. Following the screen printing and drying, firing was carried out for five different peak temperatures of 745, 765, 785, 805, and 825°C at a constant belt speed of 195 ipm. The corresponding experiment design is shown in Figure 7.4.

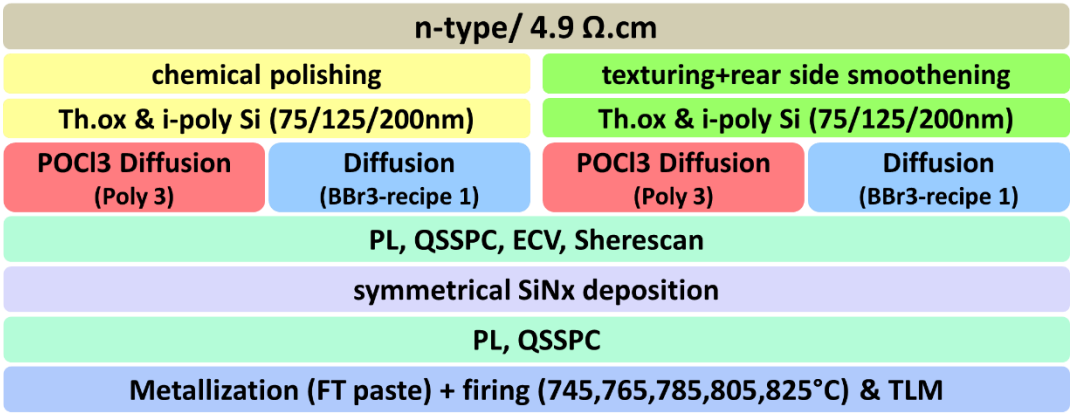


Figure 7.4. Details of the first passivating contact study conducted to understand the metallization of the doped polySi layers with fire-through paste.

Sinton PCD and PL measurements were conducted throughout the whole process sequence to trace the factors reducing implied Voc (iV_{oc}) and increasing saturation current density (J_0) values of the symmetrical samples. Following the screen printing and firing steps, samples were cut into stripes of 1-cm width and used for TLM measurements.

Measured iV_{oc} and PL values were used to develop a model to estimate the contact recombination current density ($J_{0,c}$). For this model, first, a normalization factor to correlate the measured PL and modelled PL intensity was defined. Measured sheet resistance and base resistivity of the wafer were defined as the input parameters where J_0 for passivated surfaces ($J_{0,pass}$) was the varying parameter. Then, using free software Quokka2 from PVLighthouse. $J_{0,pass}$ was varied until the modelled iV_{oc} and measured iV_{oc} becomes equal and the ratio of the modelled PL signal to the measured PL signal was taken as the normalization factor. Then, this normalization factor was used to calculate the modelled PL signal using the measured PL over metallized regions. Then, a new structure is generated in Quokka 2 so that metallized regions are defined with the experimentally used contact geometry (finger width, pitch, contact resistivity). The $J_{0,pass}$ for the non-contacted regions was already measured on the same wafer as the metallized regions after firing. Thus, $J_{0,pass}$ was defined as the input for the simulation while $J_{0,c}$ will be the varying parameter till the estimated PL signal is obtained as the simulation output. Unlike the first step where measured and modelled iV_{oc} values were matched, PL signals are needed to be matched after the metallization step since iV_{oc} data is no longer available for the metallized samples. Using this methodology, $J_{0,c}$ values were obtained as a function of polySi thickness and firing temperature both for n-polySi and p-polySi layers.

To better understand the contact formation mechanism, a sequential etch back study was also carried out through a collaboration with MESA+ Institute of TU Twente where FIB (focused ion beam)-SEM (scanning electron microscopy) imaging was applied for different samples. The samples metallized using FT-Ag and FT-AgAl paste were first exposed to aqua regia solution (HNO_3 :3 HCl) to

remove the bulk metal and leave the glass frit and nano-colloidal metal particles (Ag or AgAl) intact. Then, samples were dipped into hydrofluoric acid solution (10%) to remove the glass and remaining SiN_x layer. Finally, samples were dipped into aqua regia solution to etch the remaining metallic colloids and monitor the damage given on the surface. FIB-SEM images were taken after each etching step for both n-polySi and p-polySi layers.

7.2.3 Fabrication of Bifacial Cells with Double Side polySi Passivation

As the last part of the passivating contact studies, a big set samples were fabricated both as symmetrical test structures and as asymmetrical half fabricated samples. PolySi layers were symmetrically deposited on polished and smoothened-textured wafers for symmetrical test samples while asymmetrical samples were prepared with textured front and smoothened-textured rear surfaces. While doping of the p-polySi layers was provided by BBr_3 diffusion, n-polySi layers were doped with phosphorus implantation with a dose of $1x10^{16}$ cm^{-2}. For this set of samples, two different i-polySi thicknesses were utilized as 100 and 200 nm. To check the implant uniformity, a small set of textured, p-Cz samples were also included in the process flow without i-polySi layers at the surfaces. Activation of the implanted P atoms was carried out at 880°C, the same temperature as the BBr_3 diffusion. Moreover, for one part of the symmetrical and asymmetrical samples, P implanted surfaces of the samples were capped with a diffusion barrier prior to BBr_3 diffusion which were kept open and directly exposed to BBr_3 diffusion for the others. The purpose was to observe the effect of diffusion barrier deposition/stripping on the i-polysi layer and to verify whether implanted P dose would be enough to overcompensate diffusing boron atoms. The corresponding design of the experiment for the symmetrical samples is given in Figure 7.5. Tests samples were then deposited with SiN_x layers on both sides which were then passed through a firing process at a peak temperature of 785°C. Sinton PCD and PL measurements were carried out before and after firing.

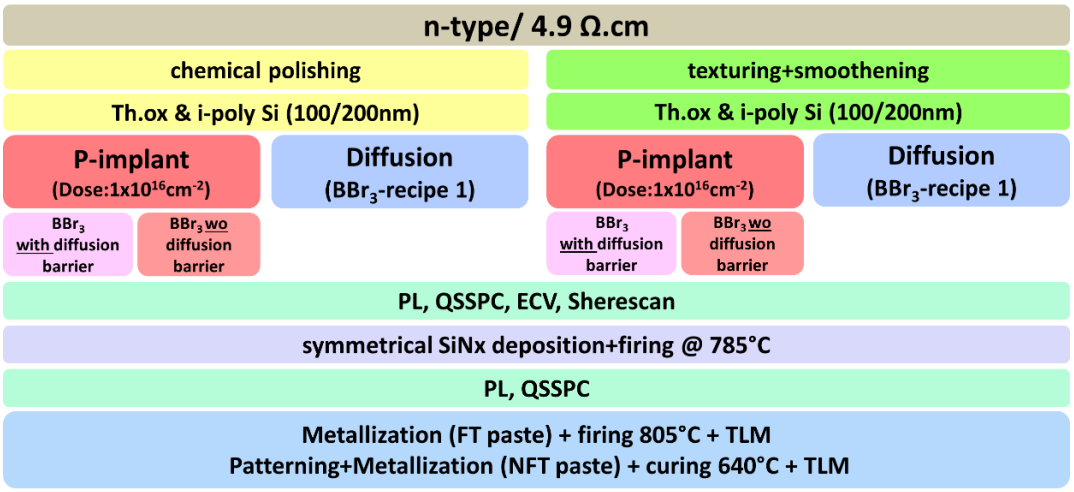


Figure 7.5. Design of experiment (DoE) for the symmetrical samples of the last passivating contact study at ECN.

Following the firing and subsequent measurements, FT-Ag, FT-AgAl, NFT pastes were screen printed using 4 busbar, H-grid design. While fire-through pastes were exposed to firing at 805°C, NFT paste was cured at 640°C. Unlike FT pastes, NFT paste was printed after a patterning step where 150 µm wide fingers were opened on SiN_x layers since NFT pastes are free of glass frit to etch the underlying SiN_x layers. Then, 100 µm wide metal fingers were aligned with those openings. After screen printing and following firing/curing processes, first PL measurements were carried out and then samples were cut into 1 cm-stripes to be used for TLM measurements.

In addition to symmetrical test samples, asymmetrical cell structures were also processed for both polished and textured samples. The corresponding experimental design is shown in Figure 7.6. For asymmetrical samples front side was textured while rear side was smoothened after the texturing. Following the deposition of i-polySi layers with the thicknesses of 100 and 200 nm, phosphorus implant was carried out for the smoothened rear side. Before exposing to BBr_3 diffusion, phosphorus implanted side some samples were capped with SiO_2/SiN_x diffusion barrier while some of them left uncapped and directly exposed to BBr_3 during the subsequent boron diffusion process. BBr_3 diffusion was used to dope the i-polySi

layer at the front side and activate the implanted phosphorus atoms at the rear side simultaneously. After the diffusion and following cleaning steps, samples were symmetrically coated with PECVD-SiN_x layer.

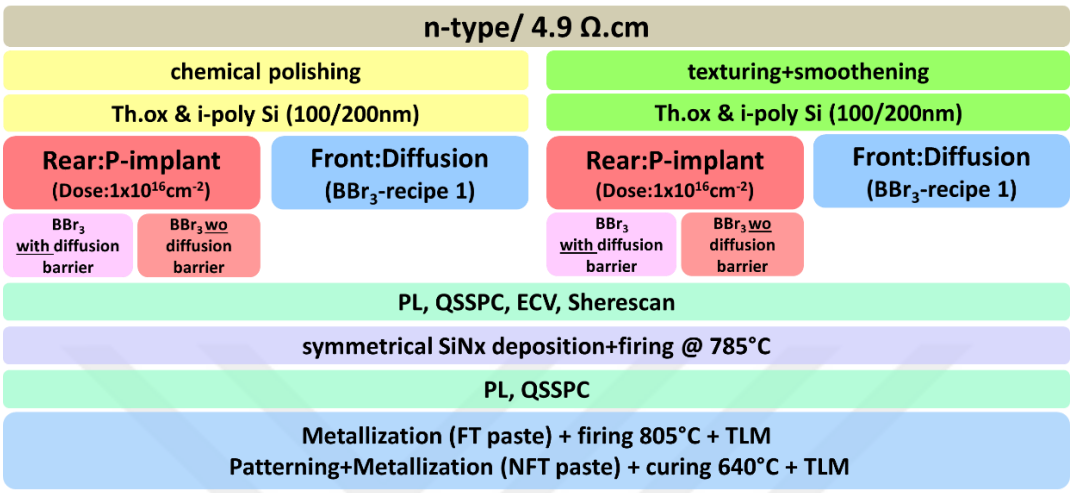


Figure 7.6. Design of experiment (DoE) for the asymmetrical samples of the last passivating contact study at ECN.

Passivated half fabricated cells were measured using Sinton PCD and PL prior to metallization. Different from the symmetrical samples, asymmetrical samples were screen printed on both surfaces using different pastes where both FT and NFT pastes were utilized. While p-polySi at the front side was always metallized with L9724 paste while n-polySi layer at the rear was metallized with Exojet, L9724 and PV18A from different suppliers.

Moreover, in addition to 4 busbar H-grid metallization, some of the samples were screen printed using a specially designed screen which was designed for J_0 measurements. Screen design for Jo test pattern and 4 busbar H-grid is shown in Figure 7.7 (left) and Figure 7.7 (right) respectively. For Jo test pattern, metallization fraction was varied from 2% to 25% where some regions were intentionally left empty for Sinton PCD measurements after metallization. Blanket metal regions were placed for PL measurements where the corresponding signal will be used for $J_{0,contact}$ extraction using the developed method in the previous section.

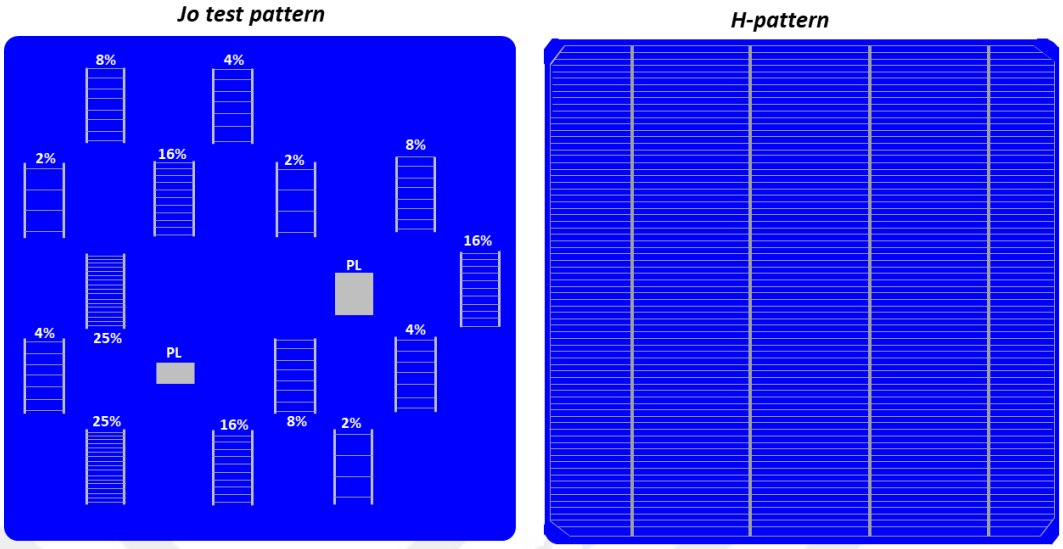


Figure 7.7. Screen design for J0 test pattern (left) and 4 busbar H-grid (right).

Samples metallized with 4 busbar, H-grid patterns went through current-voltage characterization using a class AAA, continues solar simulator from Wacom. After the I-V measurements, samples were cut into 1 cm wide stripes for the subsequent TLM measurements.

As the last analysis for the whole set of samples, a sequential etching study was carried out for FIB-SEM and HR (high resolution) -SEM imaging of the p-poly and n-polySi layers metallized with various FT and NFT pastes and fired (cured) at different temperatures. Combining all calculated and modelled $J_{0,contact}$ values, measured cell parameters and obtained TLM results with the observed SEM images, explored the contacting mechanism and contact properties of different pastes various temperatures on n-poly and p-polySi layers of different temperatures.

7.3 Results and Discussions

7.3.1 Non-Fire-Through Metallization of the Doped polySi Layers and Understanding Their Passivating Properties

As the first set of samples, the purpose was to obtain good quality doped poly layers. For this, it was required that the layers would have good implied V_{oc}, not be very leaky, and highly doped enough to have good contact resistivity values. Sheet resistance maps of $POCl_3$ diffused n-polySi layers on polished, n-Cz wafers are given in Figure 7.8.

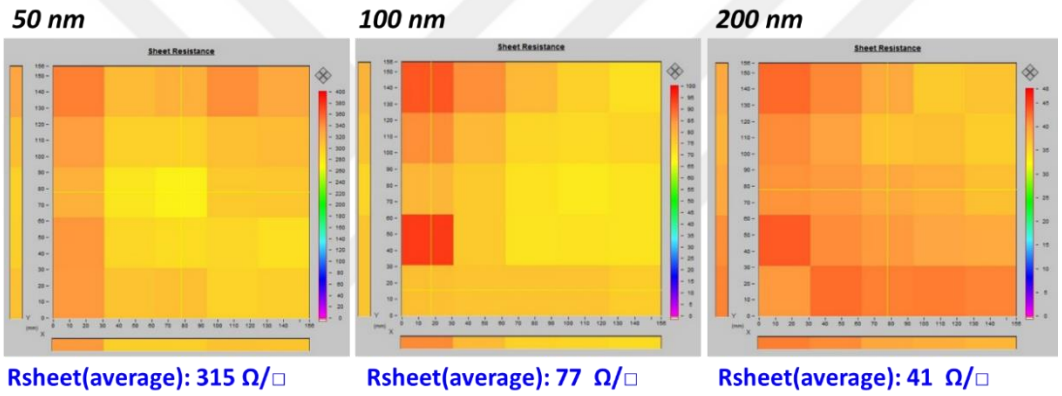


Figure 7.8. Sheet resistance maps for POCl3 diffused n-polySi layers (on polished wafers) of 50, 100 and 200 nm from left to right.

Increasing the doped polySi layer thickness from 50 to 200 nm reduced the sheet resistance from 315 to 41Ω/□. Depositing symmetrical SiN_x layer and subsequent firing step increased sheet resistance for all thicknesses with a more pronounced increase for 50 nm (Figure 7.9).

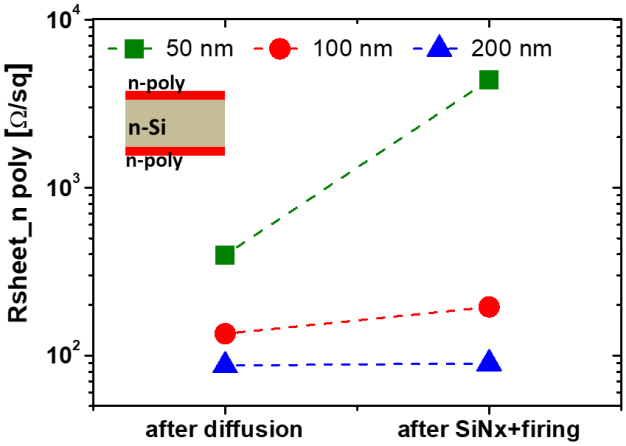


Figure 7.9. Change in sheet resistance for $POCl_3$ diffused n-polySi layers (on polished wafers) of different thicknesses throughout the regular processes sequence.

The more pronounced increase in sheet resistance for the thinnest polySi layer could be related to the possible polySi consumption during high-temperature $POCl_3$ diffusion process which would be later confirmed by ECV measurements shown in Figure 7.10.

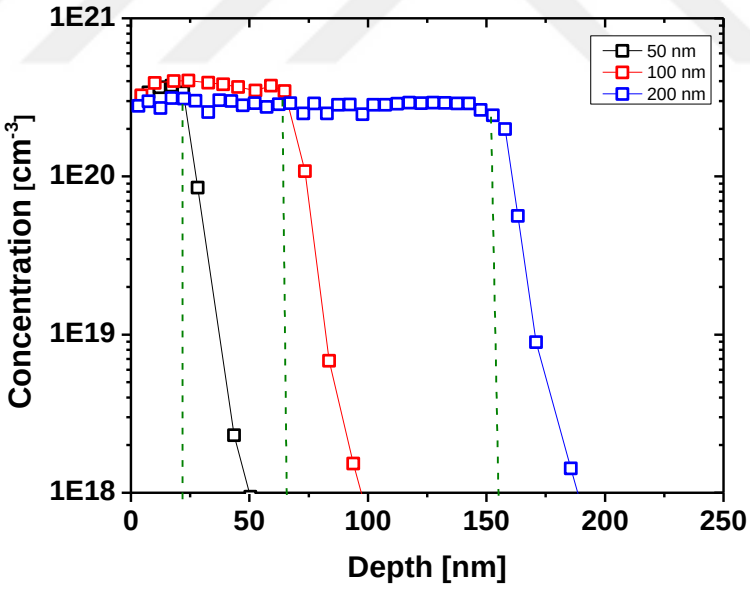


Figure 7.10. ECV profiles of $POCl_3$ diffused n-polySi layers (on polished wafers) of 50, 100 and 200 nm.

It was observed that polySi layer was consumed during PSG growth which resulted in reduced polySi thicknesses than expected by 25-30 nm for all set thickness values. Despite the lower thickness values, ECV profiles revealed that the

deposited polySi layers were uniformly doped with a constant peak concentration of $4x10^{20}$ cm^{-3} without any diffused tail through the underlying substrate. Corresponding implied Voc and J_0 values are shown in Figure 7.11.

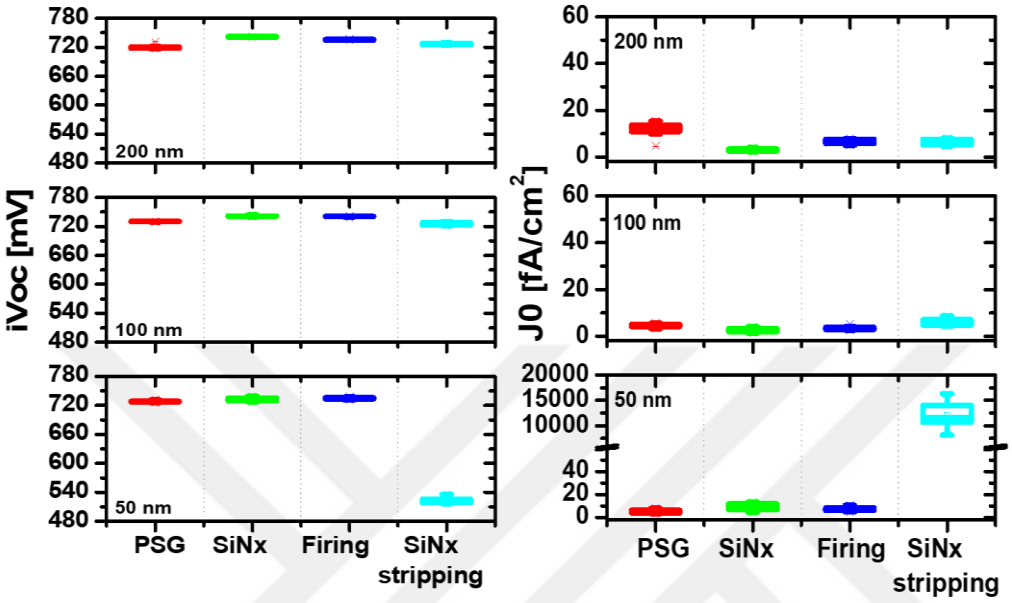


Figure 7.11. Change of implied Voc (left) and total J_0 (right) for $POCl_3$ diffused n-polySi layers on polished wafers. Values are averaged over 5 different points per wafer and 3 wafers were used for each split.

iVoc values and corresponding Jo values were quite similar for all polySi thicknesses. Putting symmetrical SiN_x layer improves iVoc values by 20-24 mV for all thickness values while firing reduces best iVoc of 50 and 200 nm thick layers by 6 and 9 mV, respectively. Stripping the SiN_x layers reduced iVoc values down to 521, 730, and 724 mV. While the highest total Jo values were 100 and 200 nm thick layers were 4.7 and 7.6 fA/cm^2, that for the 50 nm thick layers was within the range of $15\text{-}20x10^3$ fA/cm^2. That observed detrimental effect of the SiN_x for 50 nm layer could be related to consumed polySi layer during $POCl_3$ diffusion which could have been further reduced or even been locally etched back during HF dip for SiN_x stripping.

Considering the PL images shown in Figure 7.11, deposited n-polySi layers were quite uniform and no significant difference between different thicknesses could be observed.

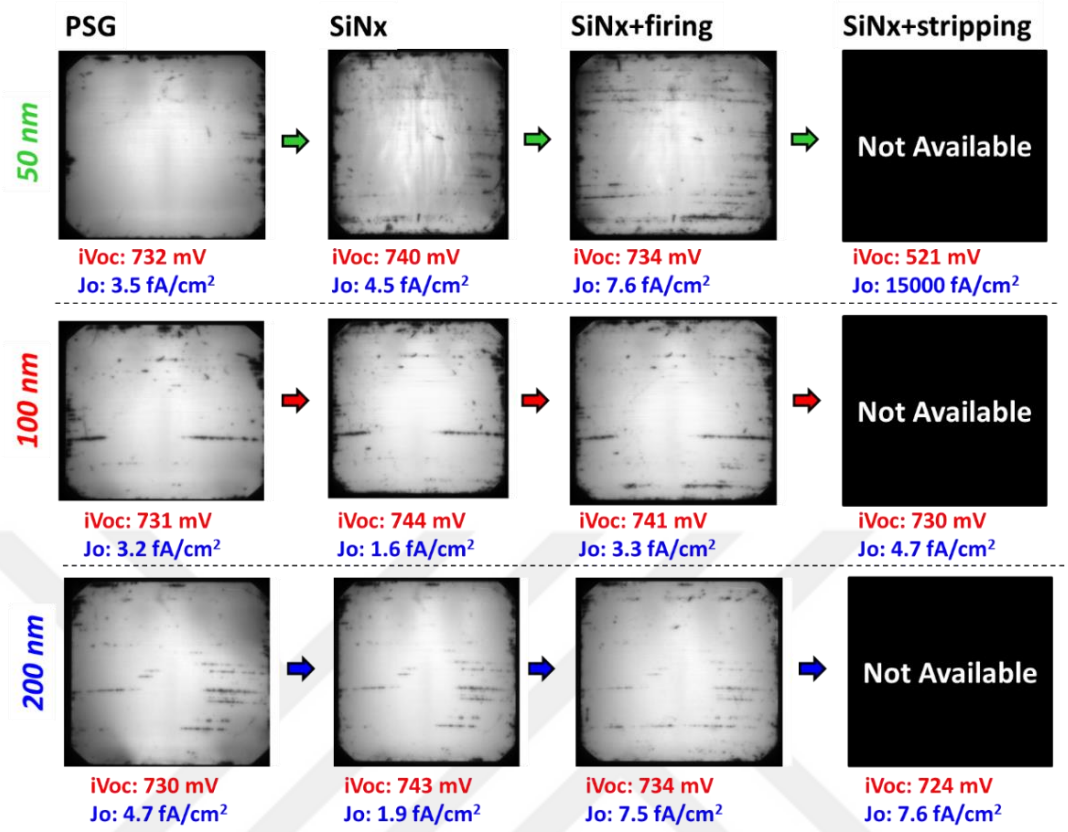


Figure 7.12. PL images of the best performing samples of each split at different process steps. Samples were in smaller size after SiN_x stripping step, thus no PL images could be taken.

For the selected samples, mobility values before and after firing were calculated applying the following equation;

$$\mu = \frac{1}{R_{sheet}.t_{poly}.N_D.q} \qquad (Eq.\ 7.1)$$

where Rsheet is the measured sheet resistance using Sherescan, t is the estimated polySi thickness using ECV, N_D is the constant doping level obtained via ECV and q is the elementary charge $1.6x10^{-19}$ C. Mobility values were calculated before and after firing conditions and given in Table 7.1. It was observed that firing reduced mobility values for all films which was more pronounced for the thinnest layer as the case of iV_{oc} measurements. The thickest layer seems to be the most resistant against the negative effect of firing. This change in mobility could be related to deactivation of the active dopant by hydrogen stored in the SiN_x film and released

during firing, change in crystallographic properties of the polySi layers due to high temperature firing step (i.e., change in grain boundaries, release of defects stored in the grain boundaries, etc.)

Table 7.1. Estimated mobility values for POCl3 doped n-polySi layers on polished wafers before and after firing.

		Before firing			After firing		
nominal thickness [nm]	**ECV estimated thickness [nm]**	n-poly Sherescan polished wafer [Ω/□]	Rsheet n-poly layer if rho=5.9 [Ω/□]	estimated mobility [cm²/V.s]	n-poly Sherescan full wafer polished [Ω/□]	Rsheet n-poly layer if rho=5.9	estimated mobility [cm²/V.s]
50	20	129	397	**21.8**	315	4374	**2.0**
100	65	57	135	**17.6**	77	195	**12.2**
200	150	39	87	**17.1**	40	90	**16.6**

For the case of BBr_3 diffused p-polySi on polished n-Cz substrates, much higher sheet resistance values were measured compared to n-polySi case. Unlike n-polySi case, p-polySi layers were quite non-uniform in terms of sheet resistance especially for the thinnest layer (Figure 7.13).

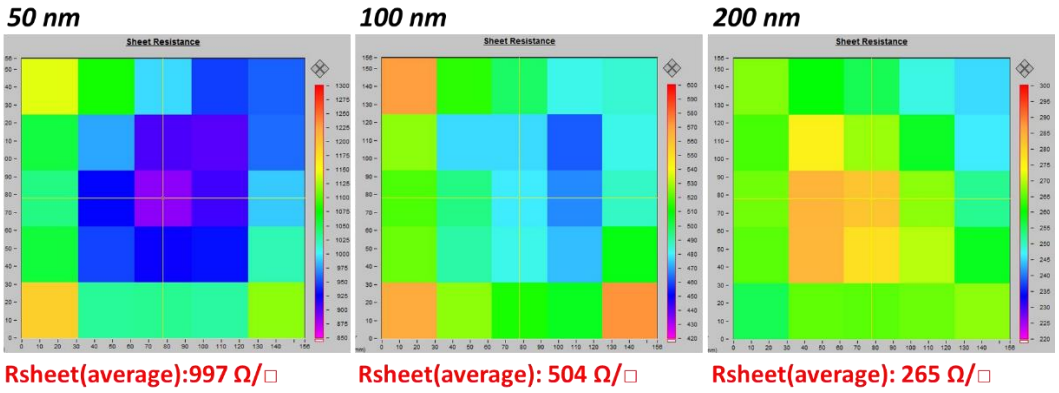


Figure 7.13. Sheet resistance maps for BBr_3 diffused p-polySi layers (on polished wafers) of 50, 100 and 200 nm from left to right on polished wafers.

Increasing the polySi layer thickness from 50 to 200 nm reduced the measured sheet resistance values from 997 to 265 Ω/□. The effect of SiN_x stripping increased sheet resistance of 100 and 200 nm thick p-polySi layers only by 5-6 Ω/□ while

that was 65 Ω/□ for the case of 50 nm p-polySi. The effect of SiN_x stripping was not as significant as in the case of n-polySi layers (Figure 7.14).

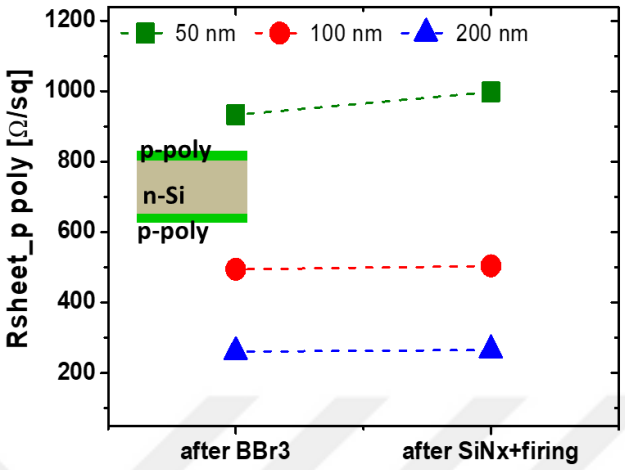


Figure 7.14. Change in sheet resistance for BBr3 diffused p-polySi layers (on polished wafers) of different thicknesses throughout the regular processes sequence on polished wafers.

ECV measurements revealed that BBr_3 diffusion has no significant effect on the thickness of the deposited i-polySi layer unlike the $POCl_3$ diffusion case which meant that BSG formation consumed much less i-polySi compared to the formation of PSG layer.

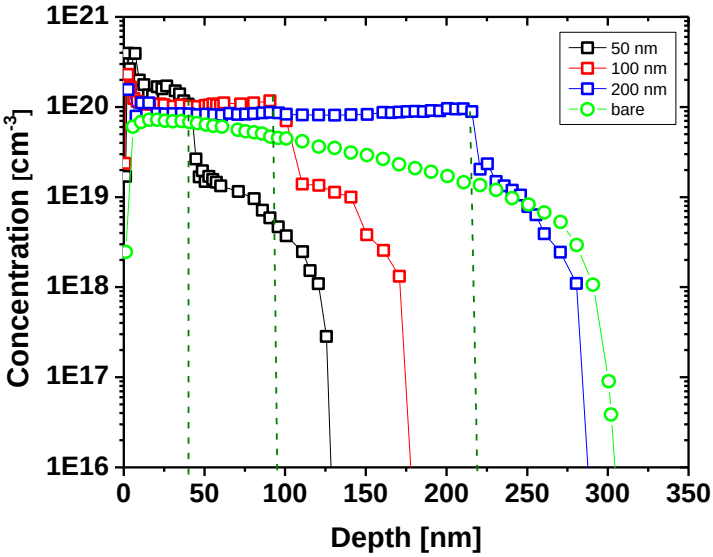


Figure 7.15. ECV profiles of BBr3 diffused p-polySi layers (on polished wafers) of 50, 100 and 200 nm on polished and that of boron emitter on textured n-Cz wafers.

Considering the ECV profiles shown in Figure 7.15, the thickness of the 50 nm layer was approximately 43 nm with a constant doping level of $1.5x10^{20}$ cm^{-3} which was 100 nm and 220 nm with the respective doping levels of $1.02x10^{20}$ cm^{-3} and $8.9x10^{19}$ cm^{-3} for the set thicknesses of 100 and 200 nm. Unlike the step-like doping profile of n-polySi layers, boron doped p-polySi layers resulted in a boron tail through the underlying substrate. Boron diffused bare Si was also included as a reference which resulted in the typical boron profile with a peak concentration of $7.21x10^{19}$ cm^{-3} and a junction depth of 410 nm.

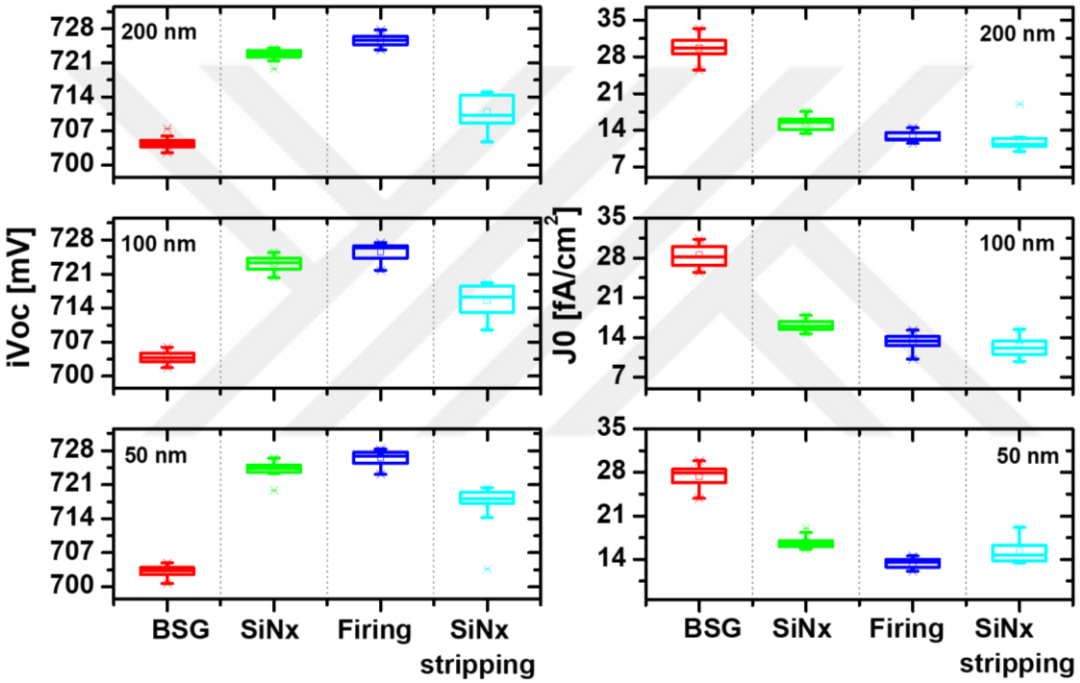


Figure 7.16. Change of implied Voc (left) and total J0 (right) for BBr3 diffused p-polySi layers on polished wafers. Values are averaged over 5 different points per wafer and 3 wafers were used for each split.

Considering the measured iV_{oc} and corresponding total J_0 values, samples performed similarly regardless of the p-polySi layer thickness (Figure 7.16). While the samples with BSG layer had the lowest iV_{oc} values which were improved upon SiN_x deposition and firing, SiN_x stripping resulted in V_{oc} drop in the range of 8-20 mV as in the case of n-polySi. Moreover, the lowest total J_0 value was around 12-13 fA/cm^2 which stayed still after SiN_x stripping.

PL images of the samples giving best iV_{oc} and total J_0 values are given in Figure 7.17. The samples were quite uniform, stable throughout the process sequence and no significant difference was observed in between different layer thicknesses. Unlike the n-polySi case, SiN_x stripping did not significantly deteriorate the iV_{oc} of the samples with 50 nm p-polySi layers. This effect could be related to the intact thickness of the p-polySi layer during BSG formation.

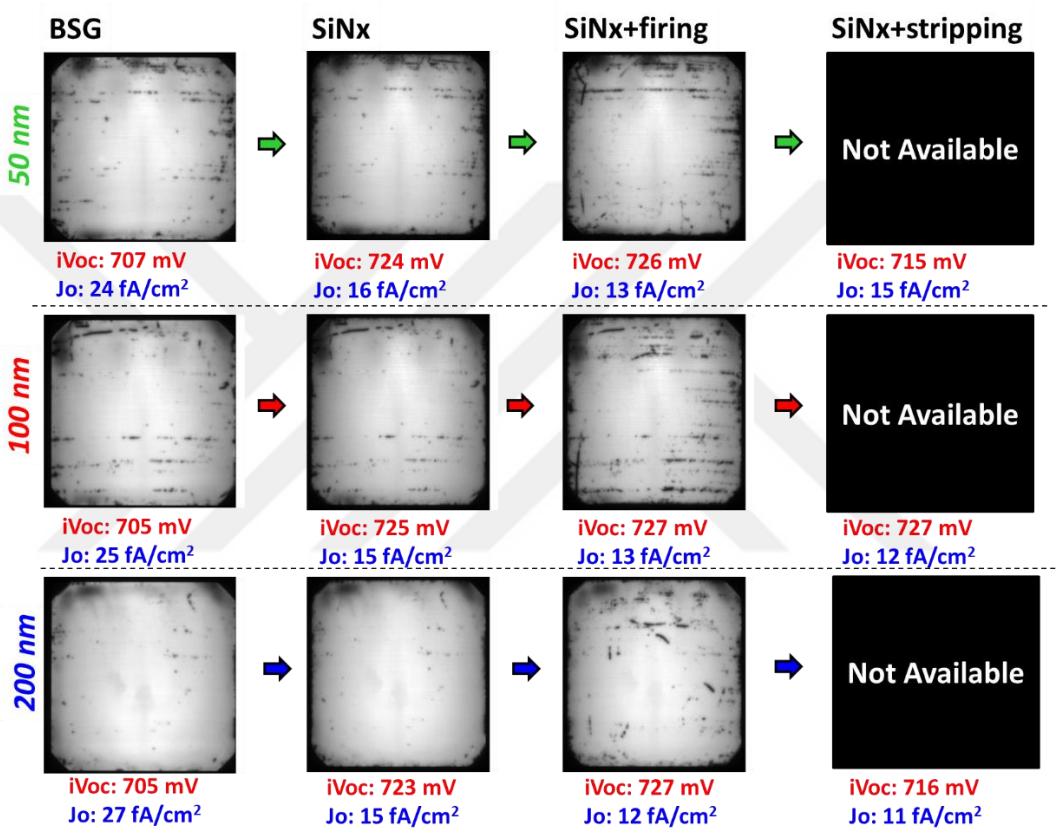


Figure 7.17. PL images of the best performing samples of each split at different process steps. Samples were in smaller size after SiNx stripping step, thus no PL images could be taken.

As the last step of analyses, mobility values of the deposited p-polySi were calculated using (*Eq.* 7.1). The profile for the thinnest layer (50 nm) was quite leaky and it was tough to estimate the doping level accurately. Still the calculation was carried out for 50 nm to have an idea and the results are given in Table 7.2. Considering Table 7.2, it was deduced that firing did not significantly affect the mobility values of p-polySi layers unlike the case of n-polySi.

Table 7.2. Estimated mobility values for BBr3 doped p-polySi layers on polished wafers before and after firing.

		Before Firing		After Firing	
nominal thickness [nm]	ECV estimated thickness [nm]	p-poly Sherescan polished wafer [Ω/□]	estimated mobility [cm^2/V.s]	p-poly Sherescan polished wafer [Ω/□]	estimated mobility [cm^2/V.s]
50	**	933	----	998	----
100	90	494	13.4	504	13.1
200	200	260	14.4	265	14.2

Moreover, compared to n-polySi layers, mobility of p-polySi layers were significantly lower which could be related to increased sheet resistance values or different crystallographic structure of the p-polySi layers.

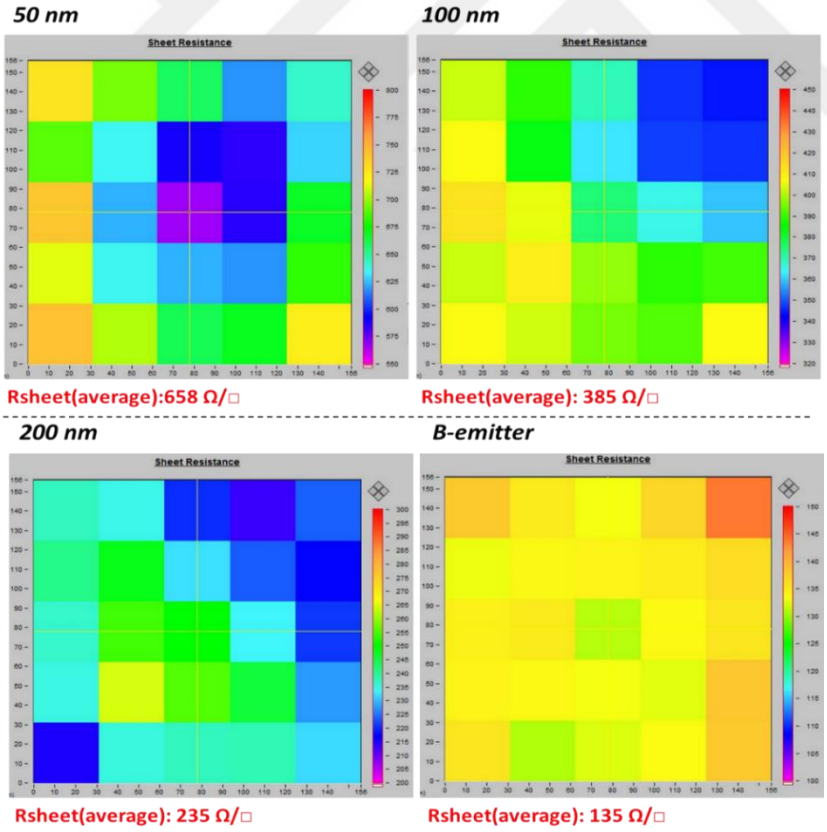


Figure 7.18. Sheet resistance maps for BBr3 diffused p-polySi layers of 50, 100, 200 nm and B-emitter on textured wafers.

In addition to polished substrates, BBr_3 diffused p-polySi layers were also deposited on un-smoothened textured substrates. Considering measured sheet resistance values (Figure 7.18), the uniformity and doping level were improved compared to the same layers on polished substrates.

Boron doped p-polySi layers still have greater sheet resistance values compared to boron emitter (135 Ω/□) even for the highest polySi thickness with the sheet resistance of 235 Ω/□. To understand the effect of firing, samples were symmetrically deposited with SiN_x layers and fired. After firing, SiN_x layers were stripped, and sheet resistance values measured. The resulting sheet resistances of the thicker polySi layers of 100 and 200 nm and that of the boron emitter were almost intact upon high temperature firing as shown in Figure 7.19.

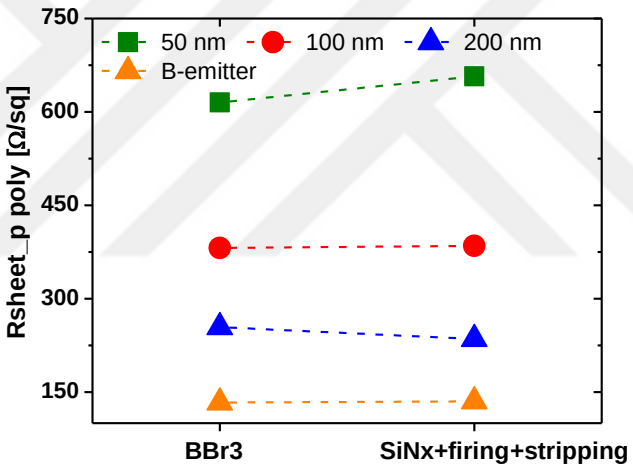


Figure 7.19. Change in sheet resistance for BBr3 diffused p-polySi layers of different thicknesses and that for boron emitter throughout the regular processes sequence on textured wafers.

Unlike relatively thicker polySi layers and boron emitter, the thinnest p-polySi layer (50 nm) showed an increase in sheet resistance from 615 to 657 Ω/□.

Following the sheet resistance measurements, ECV measurements were carried out for selected textured samples as shown in Figure 7.20. It was observed that the doped polySi layers were thicker than expected compared to their counterparts deposited on polished wafers.

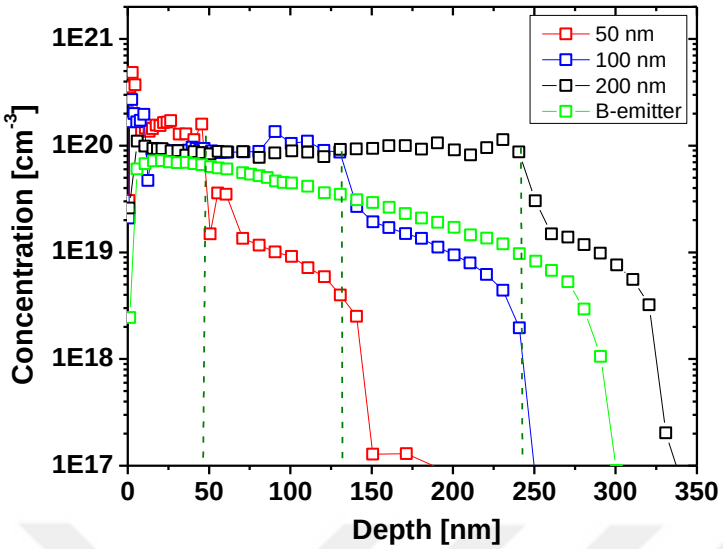


Figure 7.20. ECV profiles of BBr3 diffused p-polySi layers of 50, 100 and 200 nm and that of boron emitter on textured n-Cz wafers.

This difference in thickness could be related to the increased deposition rate on textured surfaces compared to polished surfaces.

Comparison of ECV profiles of the same p-polySi layers simultaneously deposited on polished and textured substrates is shown in Figure 7.21.

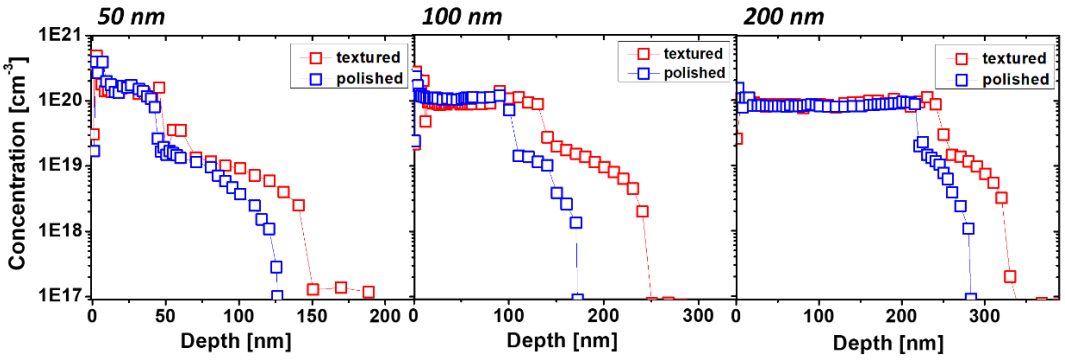


Figure 7.21. Comparison of ECV profiles of 50 (left), 100 (middle), and 200 nm (right) thick p-polySi layers on polished and textured, n-Cz substrates.

The doping profiles and peak doping concentrations are almost the same for polished and textured samples with increased layer thickness values for the textured ones.

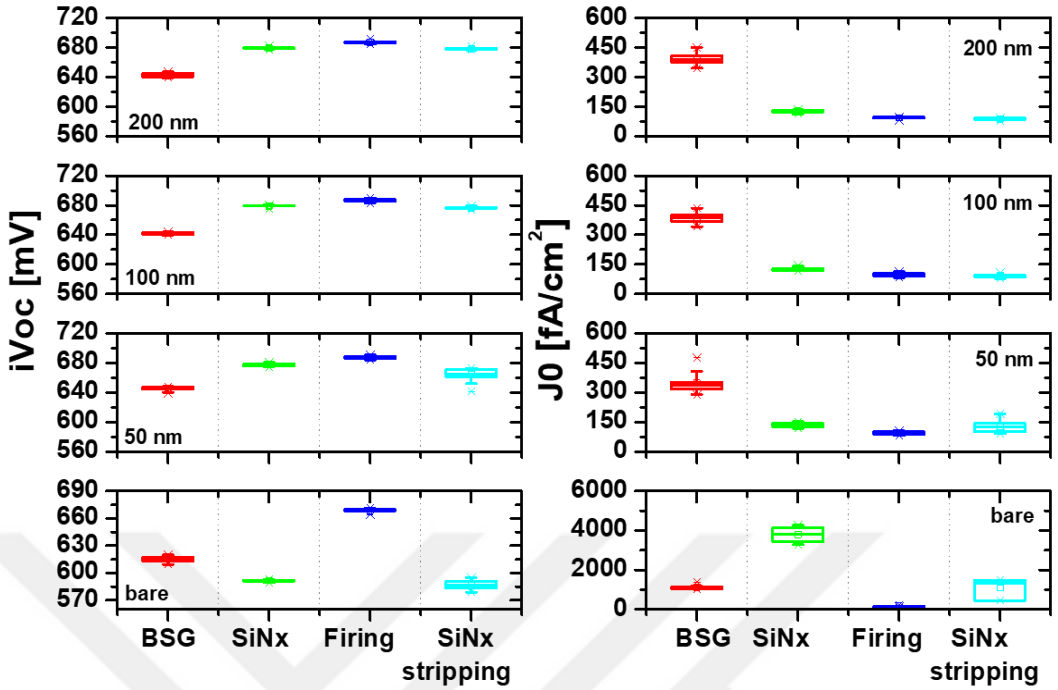


Figure 7.22. Change of implied Voc (left) and total Jo (right) for BBr3 diffused p-polySi layers and for boron emitter on textured wafers. Values are averaged over 5 different points per wafer and 3 wafers were used for each split.

Regarding the iV_{oc} and corresponding J_0 values (Figure 7.22), similar performance was observed right after BBr_3 diffusion before BSG removal, after SiN_x deposition and after firing conditions for all p-polySi thickness values. Thickness effect could only be observed after SiN_x stripping step. After SiN_x stripping, the thinnest p-polySi layer resulted in an average iV_{oc} value of 663 mV, while 100 nm layer resulted in 676 mV and 200 nm resulted in 678 mV. Unlike the samples passivated with symmetrical p-polySi layers, samples directly diffused with BBr_3 showed poorer performance as expected due to high amount of dopant atoms introduced to the underlying base wafer. Symmetrical deposited SiN_x layers reduced average iV_{oc} values from 615 to 591 mV which was increased to 669 mV after firing. Stripping the SiN_x layer deteriorated the surface passivation and reduced average iV_{oc} value down to 586 mV.

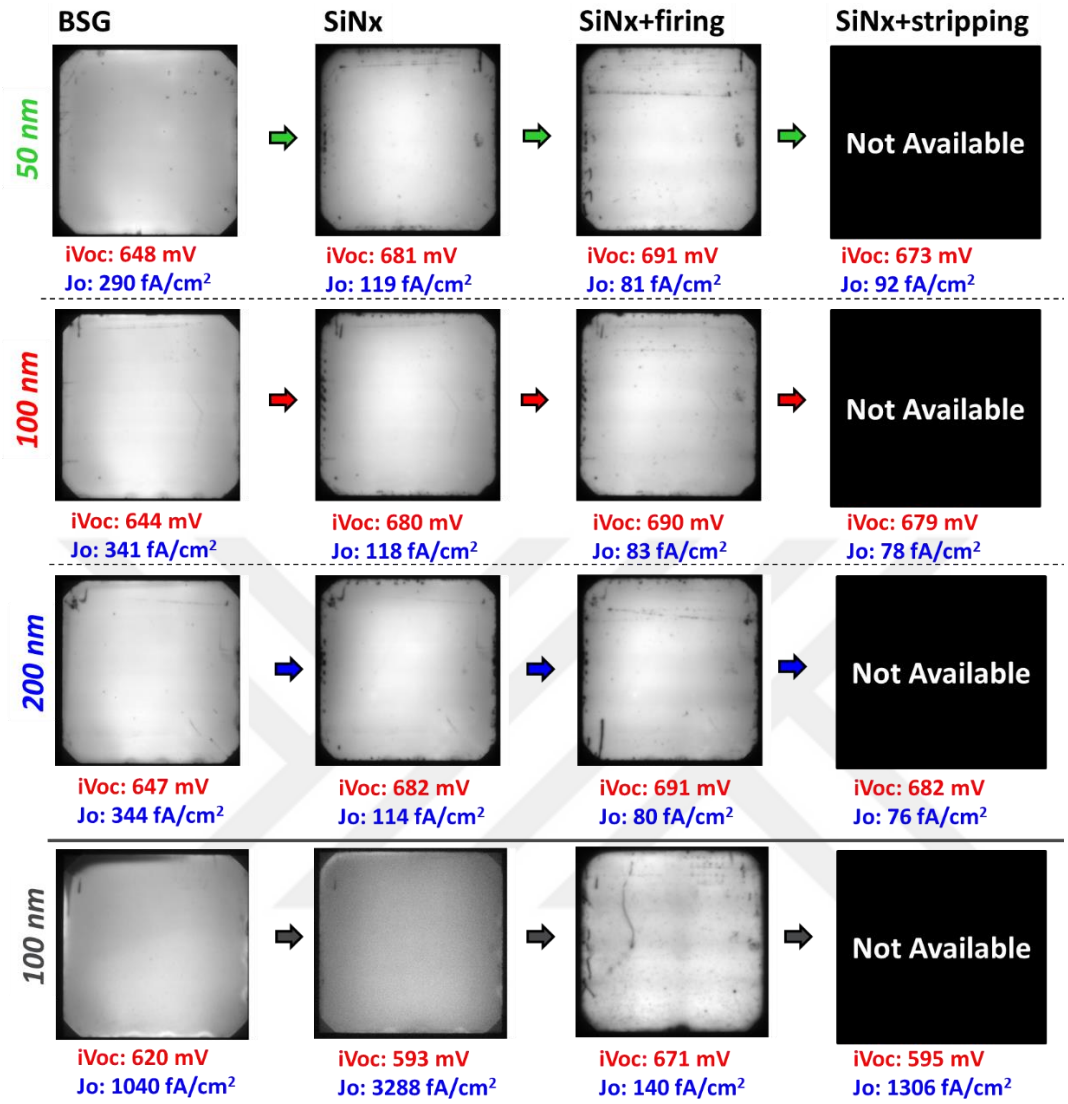


Figure 7.23. PL images of the best performing samples of each split at different process steps. Samples were in smaller size after SiNx stripping step, thus no PL images could be taken.

Estimated mobility values for the p-polySi layers and boron emitter on textured wafers are given in Table 7.3. Comparing the mobility values for p-polySi layer on polished and that on textured wafers revealed that p-polySi layers on textured samples had lower mobility values both before firing and after firing conditions. This could be related to the increased surface area and roughness for the case of textured samples. Samples with boron emitter on textured wafers overperform p-polySi layers deposited both on polished and textured wafers.

Table 7.3. Estimated mobility values for BBr3 doped p-polySi layers on textured wafers before and after firing.

		Before Firing		After Firing	
nominal thickness [nm]	ECV estimated thickness [nm]	p-poly Sherescan full wafer polished [Ω/□]	estimated mobility [cm²/V.s]	p-poly Sherescan full wafer polished [Ω/□]	estimated mobility [cm²/V.s]
50	44	615	14.90	657	13.95
100	110	381	16.56	385	16.40
200	230	254	12.57	235	13.60
Boron emitter	300	133	22.07	135	21.74

As the last set of samples for this part of the study, phosphorus implanted symmetrical and asymmetrical samples were prepared. For the case of symmetrical samples, phosphorus (P) implant doses of $2x10^{15}$, $5x10^{15}$ and $1x10^{16}$ cm^2 were symmetrically applied for i-polySi layers of 50, 100 and 200 nm, respectively. While for the case of asymmetrical samples, only rear side was implanted while front side was boron doped. Both symmetrical and asymmetrical samples were exposed to BBr_3 diffusion at 880°C during which P implanted surfaces were protected with a 100-110 nm SiN_x layer. However, due to process and equipment related problems, there was a huge difference between front and rear side sheet resistance values on the symmetrical samples. Moreover, uniformity over a sample and uniformity from sample to sample were extremely poor especially for the case of 50 nm i-polySi layer (Figure 7.24). While front side of one sample had a sheet resistance of 1170±438 Ω/□, the rear side of the same sample had 572±391 Ω/□ for 50 nm i-polySi layers. For thicker i-polySi layers, measured sheet resistance values were more suitable for proper device fabrication and uniformity was significantly improved as the layer thickness was increased.

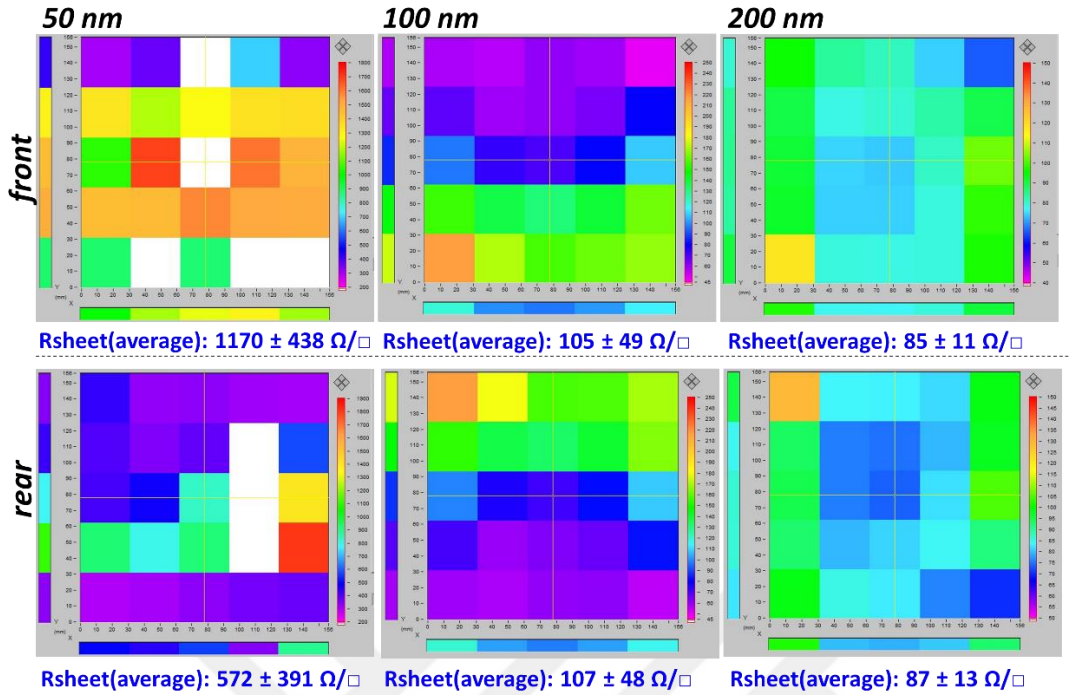


Figure 7.24. Sheet resistance maps for phosphorus implanted n-polySi layers of 50, 100, and 200 nm on polished wafers. White regions correspond to extremely high sheet resistances that cannot be measured properly.

Following the sheet resistance measurements, ECV measurements were carried out to examine the reason of extremely high sheet resistance values. For ECV measurements asymmetrical samples with BBr_3 diffused p-polySi at the front and P-implanted n-polySi at the rear side were utilized. While the thinnest polySi layer with the highest sheet resistance value (> 1000 Ω/□) was impossible to measure, doping profiles for 100 and 200 nm thick layers were shown in Figure 7.25. It was observed that doping profile of the 100 nm i-polySi layer different than the standard $POCl_3$ diffused n-polySi layers. Doping concentration was not constant in the polySi layer while a significant phosphorus tail through the underlying n-Cz was observed.

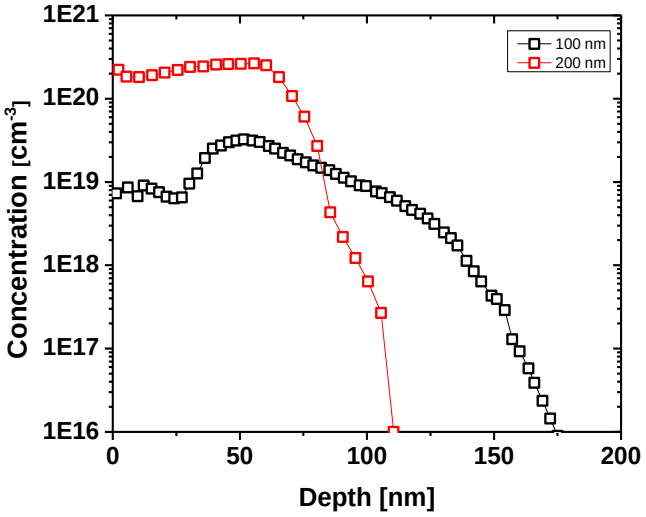


Figure 7.25. ECV profiles of Phosphorus implanted n-polySi layers of 100 and 200 nm on polished n-Cz wafers. Samples were activated during BBr3 diffusion at 880°C.

Non-uniform doping concentration could be related to the insufficient implant dose while phosphorus tail was related to the implant energy making implanted ions pass through the interfacial SiO_2 layer.

Considering the p-polySi deposited surfaces of the samples, it was recognized that the doping profiles were different than those obtained on symmetrical p-polySi samples which were discussed above. Comparison of ECV profiles of p-polySi layers on symmetrical and asymmetrical samples is shown in Figure 7.26.

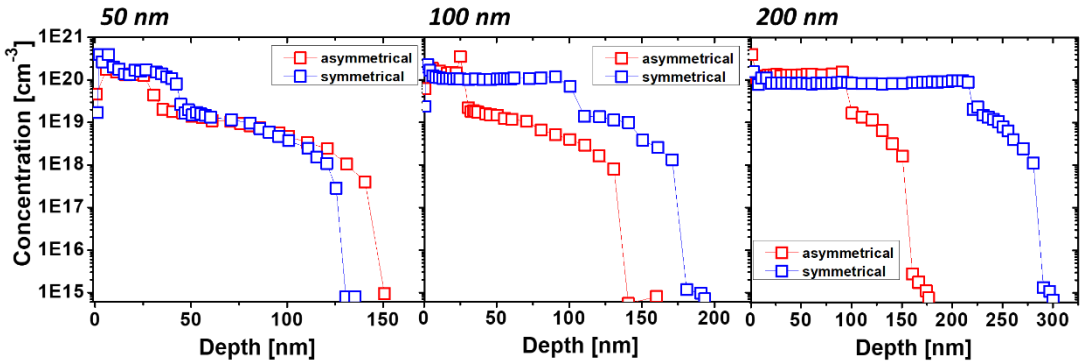


Figure 7.26. Comparison of ECV profiles of 50 (left), 100 (middle), and 200 nm (right) thick BBr3 diffused p-polySi layers on asymmetrical and symmetrical samples (on polished, n-Cz substrates).

It was observed that doping profiles of p-polySi layers on asymmetrical and symmetrical are quite similar for all thickness values. However, polySi thickness values for asymmetrical samples were 150, 150 and 175 nm while their respective counterparts on symmetrical samples were 125, 175 and 300 nm.

Following Sinton PCD measurements confirmed the non-uniformity of the samples which was recognized during sheet resistance measurements. Considering the measured iV_{oc} and J_0 values shown in Figure 7.27, it was not possible to make a reliable conclusion about the performance of different layers. While one corner of a sample had an iV_{oc} of 713 mV with the corresponding J_0 of 16 fA/cm^2, another corner of the same sample had 633 mV with a poor J_0 fitting. However, as observed during ECV and sheet resistance measurements, 200 nm i-polySi layers had more uniform doping profiles which resulted in superior performance compared to 50 and 100 nm thick layers.

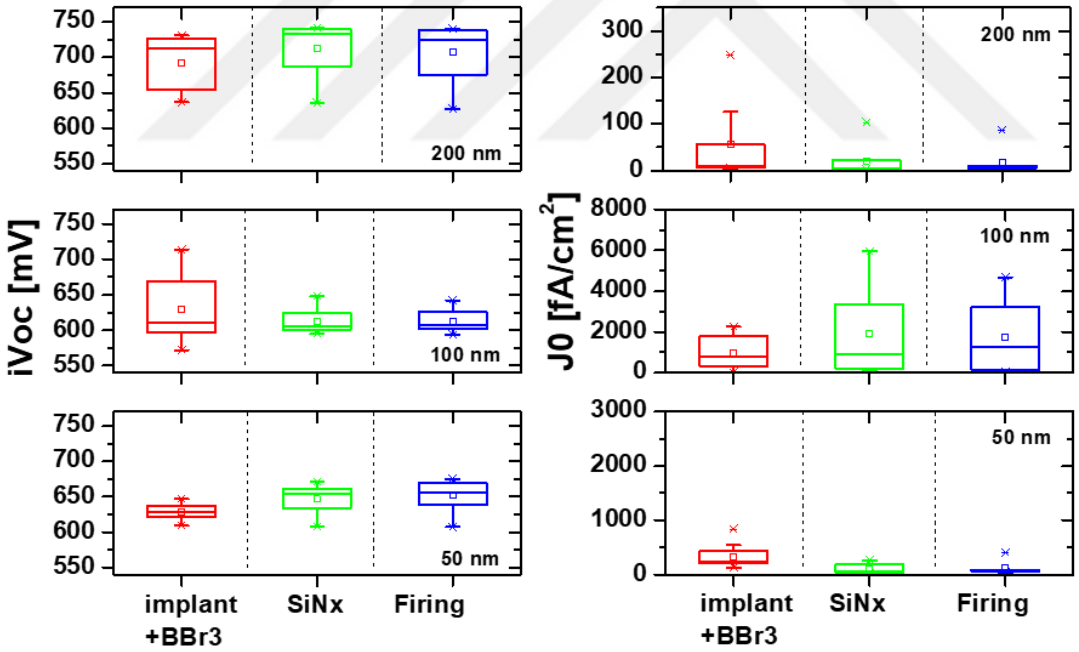


Figure 7.27. Change of implied Voc (left) and total Jo (right) for phosphorus implanted and activated (BBr3 at 880°C process with diffusion barrier) n-polySi layers on polished wafers. Values are averaged over 5 different points per wafer and 3 wafers were used for each split.

Following the activation and SiN_x passivation, best sample of the set had an iV_{oc} of 742 mV with a corresponding total J_0 of 2.3 fA/cm^2. However due to non-uniform ion beam during the implant process, the neighboring sample of the same sample had an iV_{oc} of 636 mV with the corresponding J_0 of 103 fA/cm^2.

PL measurements visualize the uniformity problem and poor iV_{oc} levels. Considering the PL image of the selected sample shown in Figure 7.28, implantation process related problems become more visible.

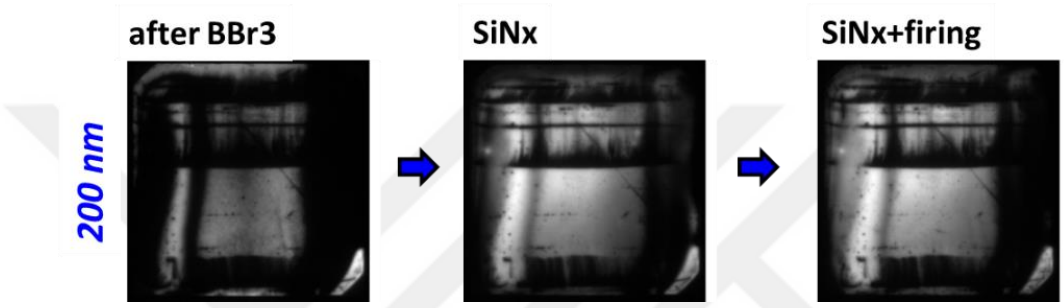


Figure 7.28. PL images of a selected sample with 200 nm n-polySi layer.

The non-uniform phosphorus ion beam had generated locally dead regions, dark regions on PL images, which could not be completely recovered by SiN_x deposition or firing. That was an equipment related problem and would be fixed for the following experiments.

To trace of effect of successive process steps, PL images were taken throughout the whole process sequence and shown in Figure 7.29 for the selected samples. It was observed that, PL signal of the samples with 50 and 100 nm polySi layers was lower than that of samples with 200 nm thick polySi layer (Figure 7.29). Brighter PL images of samples with 200 nm polySi layer could explain relatively better performance of the same samples.

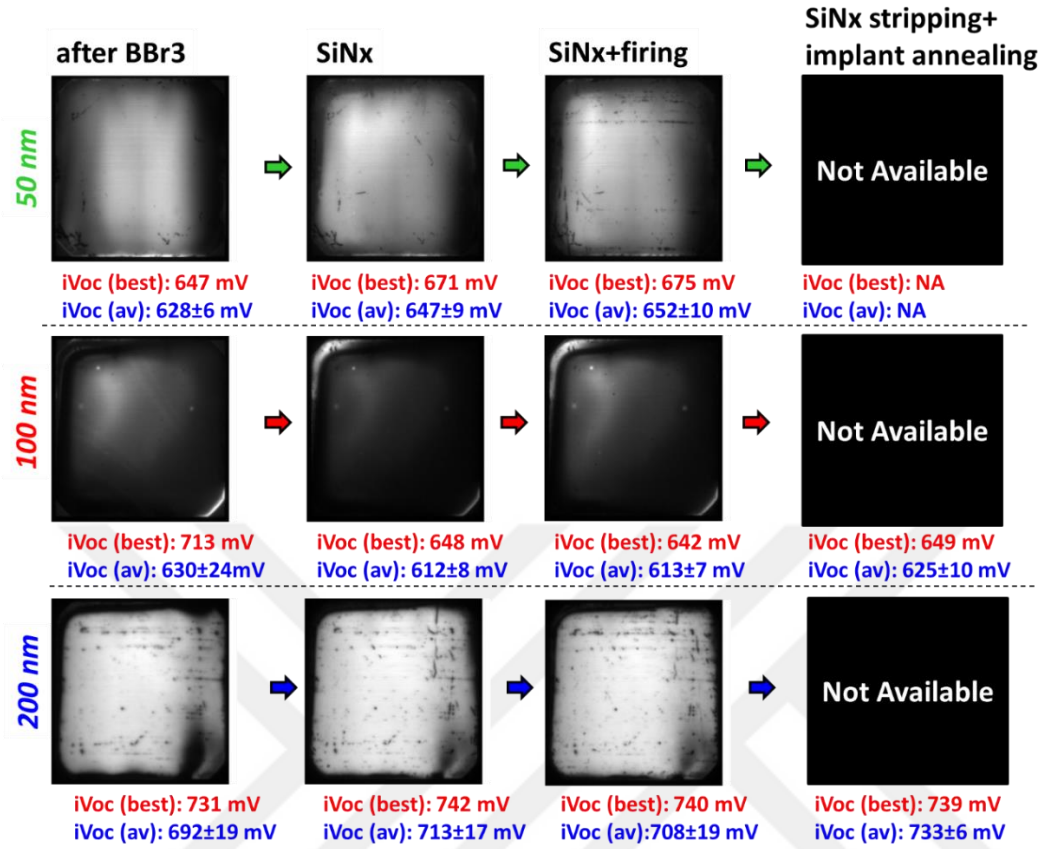


Figure 7.29. PL images of the best performing samples of each split at different process steps. Samples were in smaller size after SiNx stripping step, thus no PL images could be taken.

As the last process step, screen printing-based metallization was carried out using two NFT pastes from different suppliers. All n-polySi and p-polySi samples were exposed to SiN_x stripping and then metallized with PVD2B and L9246 pastes. Five different curing temperatures of 610, 620, 630, 640, 650°C were applied for the curing of L9246 while those of 560, 570, 580, 590, 600°C were applied for the curing of PVD2B. For the metallization study, only samples with 50 and 200 nm thick polySi were used to understand the limiting cases. Samples with 100 nm polySi layers were not metallized.

TLM results for L9246 paste on samples with 50 and 200 nm polySi layers are given in Figure 7.30. $POCl_3$ diffused n-polySi layers resulted in extremely high contact resistivity values which could be related to the polySi layer consumption during SiN_x stripping. Despite extremely high sheet resistance values, samples with

P implant had the lowest contact resistivity values below 100 mΩ.cm^2 with a slight dependence on curing temperature. For the case of p-polySi layers, texturing improves contact resistivity which could be related to the enhanced paste adhesion.

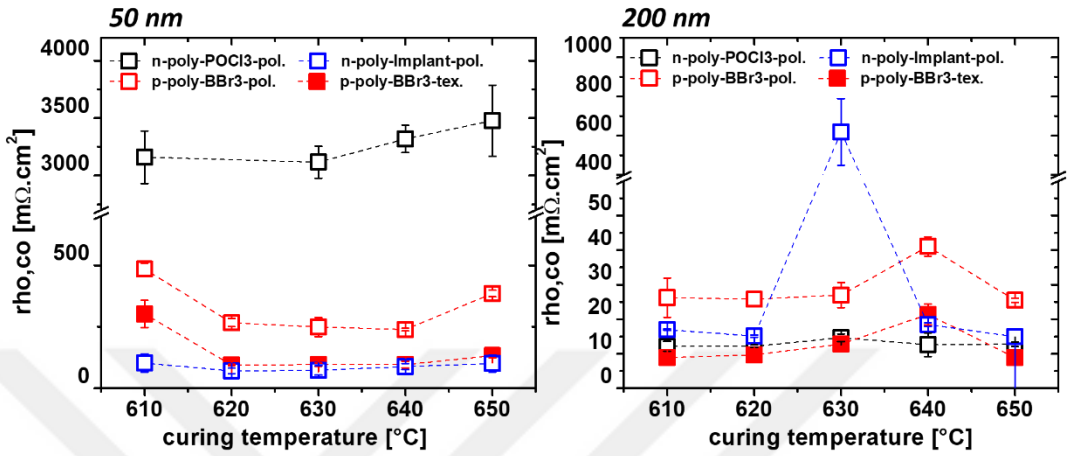


Figure 7.30. TLM results for L9246 NFT-paste on 50 nm (left) and 200 nm (right) n/p-polySi layers.

Unlike samples with 50 nm polySi layers, samples with 200 nm polySi layers resulted in more reasonable contact resistivity values for all layers as shown in Figure 7.31. P implanted and $POCl_3$ diffused n-polySi samples resulted in similar rho,co values except the implanted samples cured at 630°C. While rho,co values for p-polySi layers on textured wafers were close to those for n-polySi layers on polished wafers. p-polySi layers on the polished wafers results in rho,co values are double those on the textured wafers.

TLM results for the other NFT-paste (PVD2B) were significantly greater than those obtained for L9246. Samples with 50 nm p-polySi layers resulted in the same rho,co values both on polished and textured wafers (Figure 7.31 (left)). P implanted sample resulted in extremely high rho,co values within the range of 3000-8000 mΩ.cm^2. For the case of 200 nm thick polySi layers, $POCl_3$ diffused n-polySi layers had lower rho,co values compared to p-polySi layers (Figure 7.31(right)). Despite slight improvement in rho,co values as a function of polySi thickness, still PVD2B paste was observed to be not properly contacting.

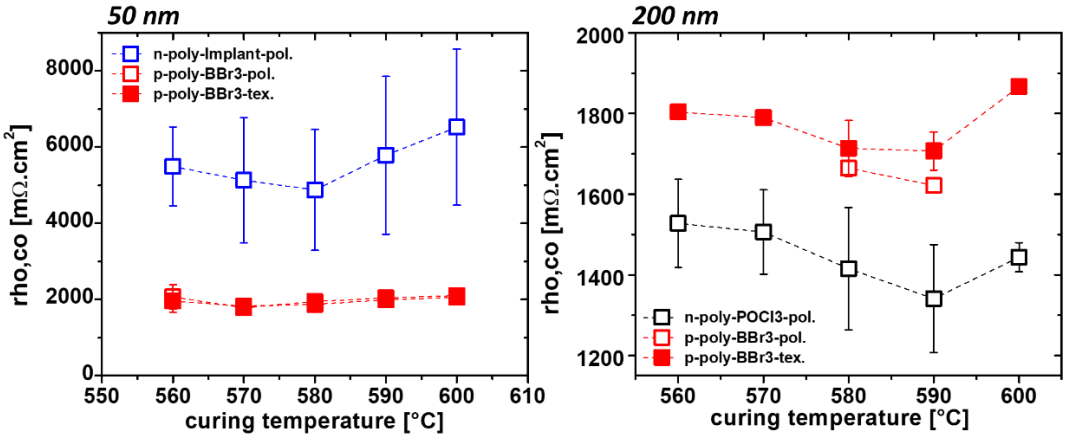


Figure 7.31. TLM results for PVD2B NFT-paste on 50 nm (left) and 200 nm (right) n/p-polySi layers.

Applying high temperature firing for L9246 and PVD2B pastes also did not help to reduce the contact resistivity values. The resulting contact resistivity values were still of the orders of few thousands of mΩ.cm^2 for both n-polySi and p-polySi samples. Moreover, iV$_{oc}$ values were also observed to degrade upon firing. Samples with 100 nm thick polySi layers were used for firing check of metallized and non-metallized samples. As show in Figure 7.32, firing reduced the iV$_{oc}$ values of all metallized and non-metallized samples to the same level.

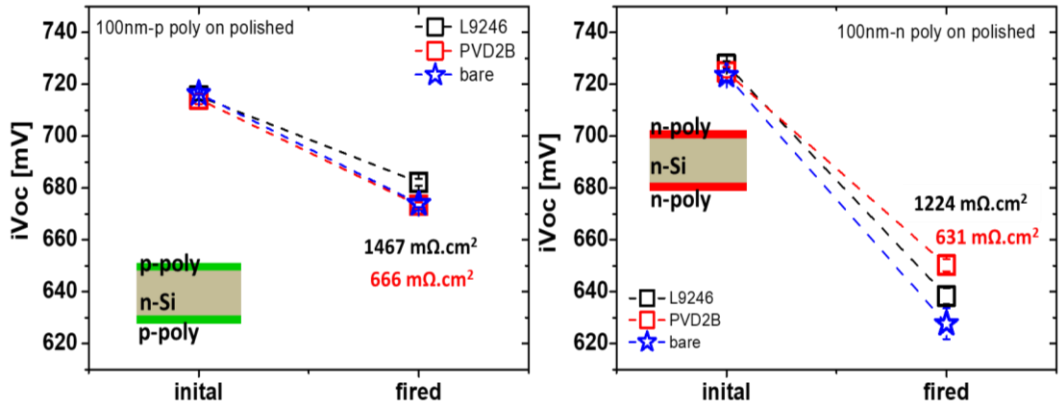


Figure 7.32. Change in iVoc values of metallized and non-metallized 100 nm p-polySi (left) and 100 nm n-polySi (right) layers on polished, n-Cz wafers during firing.

Considering rho,co values of the samples with p-polySi and n-polySi samples give similar results. While PVD2B paste resulted in rho,co of 631 and 666 mΩ.cm^2,

L9246 paste resulted in 1224 and 1467 mΩ.cm^2 for respective n-polySi and p-polySi samples.

Based on these results, iV_{oc} drop was decided to be irrelevant of metal-polySi interaction; instead, firing was observed to create this iV_{oc} loss. To better understand the effect of firing, samples were exposed to multiple firing steps after SiN_x stripping. Change in iV_{oc} is shown in Figure 7.33.

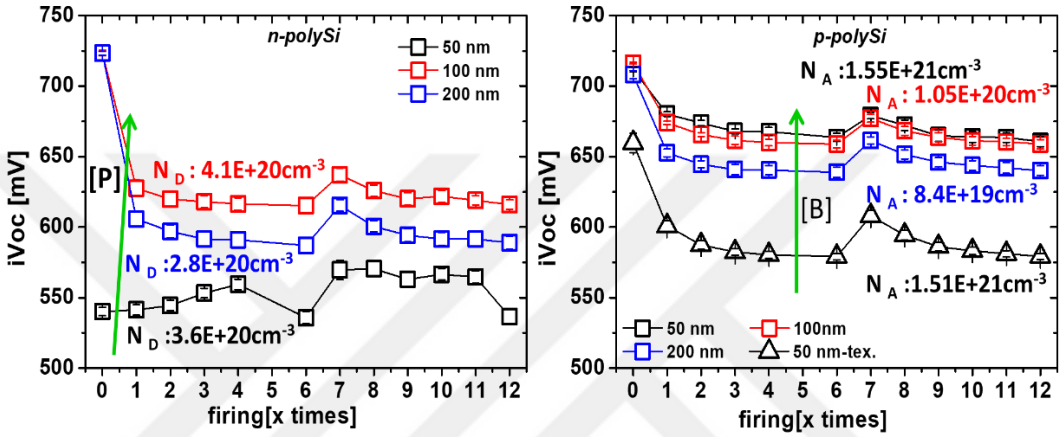


Figure 7.33. Effect of multiple firing on iVoc of n-polySi (left) and p-polySi (right) samples after SiNx stripping.

Initial values were measured right after the SiN_x stripping which were approximately the same as the values before SiN_x stripping for 100 and 200 nm thick layers of n-polySi and for all thicknesses of p-polySi layers. Significant degradation of iV_{oc} for 50 nm n-polySi layer after SiN_x stripping was due to the reduced n-polySi during $POCl_3$ diffusion as discussed before. Thus, the thinnest layer affected the most severely. It was observed that the first firing was already enough to dehydrogenate the polySi layers and additional firing steps did not generate a significant difference in iV_{oc} level. The seventh firing generated a jump of 20-35 mV in iV_{oc} values of n-polySi samples which were then leveled off for the additional firing steps except the thinnest layer. For the p-polySi samples a jump of 16-30 mV was observed at the seventh firing as in the case of n-polySi samples. The respective drop in iV_{oc} upon the first firing of 50, 100 and 200 nm n-polySi layers were 1, 96 and 118 mV. Considering the ECV profiles of n-polySi layer

(Figure 7.10), it was deduced that the higher the doping level resulted in less iV_{oc} loss during dehydrogenation. A similar trend was observed for p-polySi layers. Drop in iV_{oc} was 30, 43 and 56 mV for respective thickness values of 50, 100 and 200 nm. Remembering the ECV profiles of p-polySi layers (Figure 7.15), it could be said that increasing doping level reduces V_{oc} drop during dehydrogenation. Comparing the performance of 50 nm p-polySi layer on polished and textured wafer, it was observed that increasing surface area promotes hydrogen effusion out of the layer and increases iV_{oc} drop from 30 mV to 59 mV.

7.3.2 Fire-Through Metallization of the Doped polySi Layers and Understanding the Contact Formation Mechanisms

In the second part of the polySi studies at ECN, again passivating properties of n-polySi and p-polySi layers were focused on together with contacting properties. Different from the previous part of the study, this time industrial fire through pastes were utilized for the metallization and a method combining PL and modelling (Quokka2) was developed to extract $J_{0,contact}$.

Table 7.4. Measured sheet resistance values of n-polySi and p-polySi layers both on polished and textured samples. Measurements were done before stripping PSG and BSG layers.

	n-polySi		p-polySi	
thickness [nm]	polished	textured	polished	textured
75	59±5	55±1	443±16	376±24
125	59±3	42±3	315±12	290±4
200	79±4	54±3	222±14	211±15

Considering the measured sheet resistance values given in Table 7.4, n-polySi layers had approximately the same sheet resistance values for all thicknesses while increasing layer thickness reduced the sheet resistances of the p-polySi layers. Moreover, textured samples resulted in lower sheet resistance values than their polished counterparts for both n-polySi and p-polySi layers.

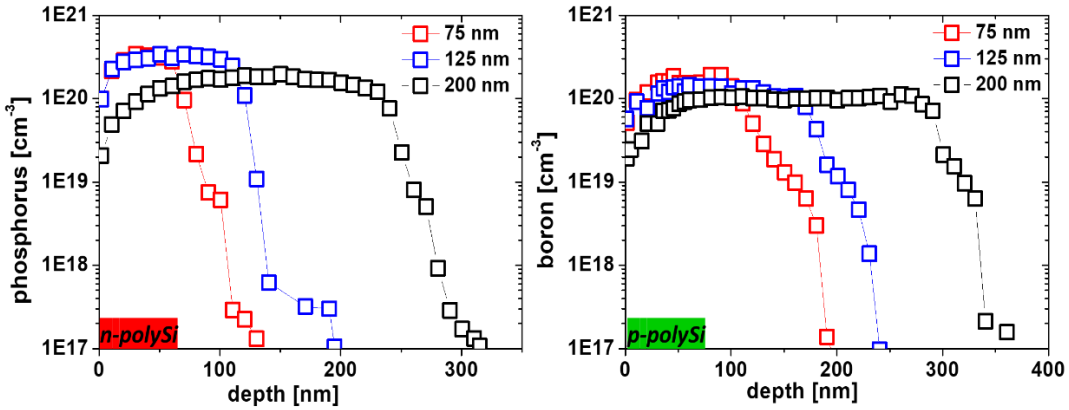


Figure 7.34. ECV profiles of $POCl_3$ diffused n-polySi (left) and BBr3 diffused p-polySi (right) layers on textured samples.

ECV measurements were carried out on textured samples after stripping the SiN_x layers and the corresponding profiles of n-polySi and p-polySi layers are shown in Figure 7.34. It was observed that layer thicknesses were greater than corresponding set values. Except the depleted surfaces, both n-poly and p-polySi layers had uniform dopant concentration through the polySi layer.

Sinton PCD and PL measurement were carried out right after $POCl_3$ diffusion with staying glass layer (PSG) and after symmetrical SiN_x deposition. It was observed that the highest iV_{oc} (the lowest J_0) was obtained for the thinnest n-polySi layers (75 nm) both on polished and textured n-Cz wafer (Figure 7.35). Despite the different iV_{oc} values, depositing symmetrical SiN_x layer equalized iV_{oc} and corresponding J_0 values regardless of the n-polySi layer thickness. Moreover, the performance of the samples passivated with 75 and 125 nm n-polySi layers had quite similar J_0 values while those with 200 nm n-polySi had significantly increased total J_0 values. Switching the substrate surface morphology from chemically polished to textured reduces average iVoc values by an amount of 30-40 mV for all thickness values as expected.

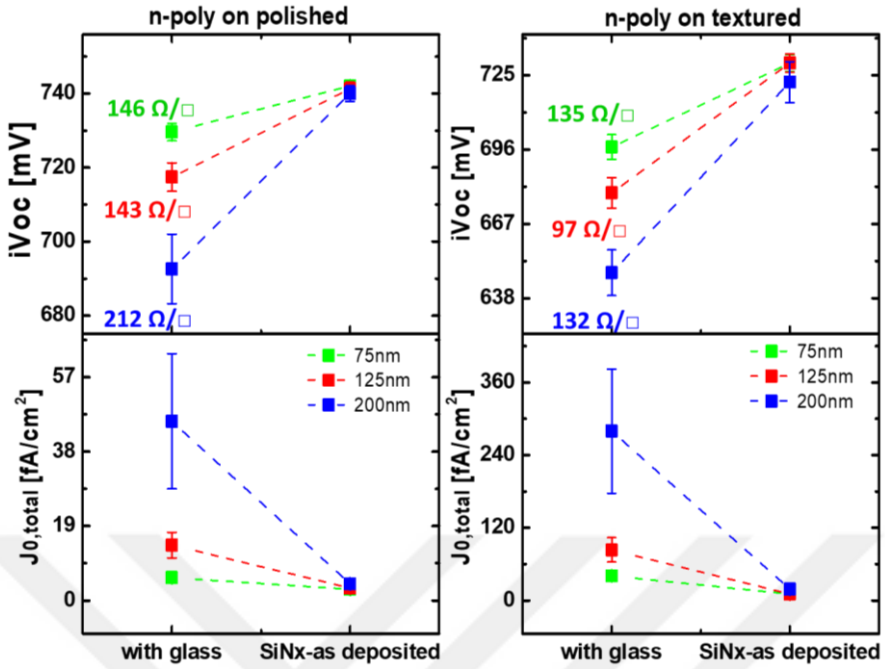


Figure 7.35. Average iVoc and J0,total values for n-polySi on polished (left) and on textured (right) n-Cz wafers. Measured values are averaged on 5 samples per split and 5 different points per sample.

That behavior could be related to the fact that the increased surface area would increase recombination as well as to that polySi layer consumption would be promoted for the textured samples during the following diffusion steps. Considering the best performing samples (see Figure 7.36), the highest iV_{oc} was obtained as 745 mV with the corresponding total J_0 of 1.6 fA/cm^2 for the case of 125 nm thick polySi layer on polished wafer.

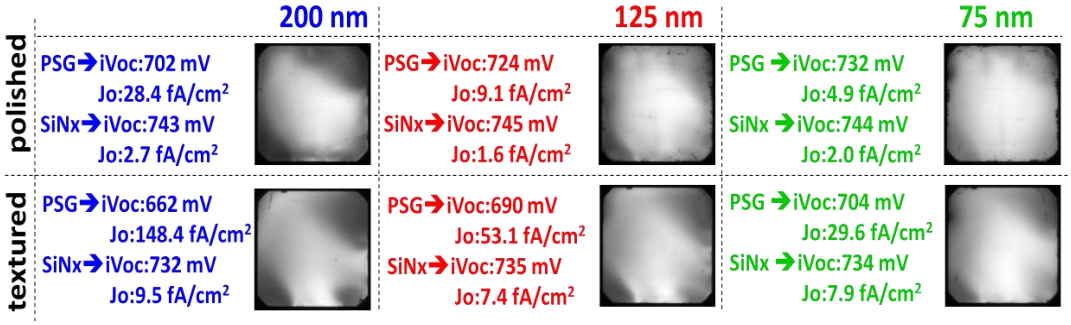


Figure 7.36. Best iVoc and J0 values for n-polySi layer on polished and textured n-Cz wafers with corresponding PL images. PL images were taken for the samples staying with PSG layer.

It was quite similar for the case of textured samples where the highest iV_{oc} was obtained for 125 nm thick n-polySi layer as 735 mV with the corresponding total J_0 of 7.4 fA/cm^2.

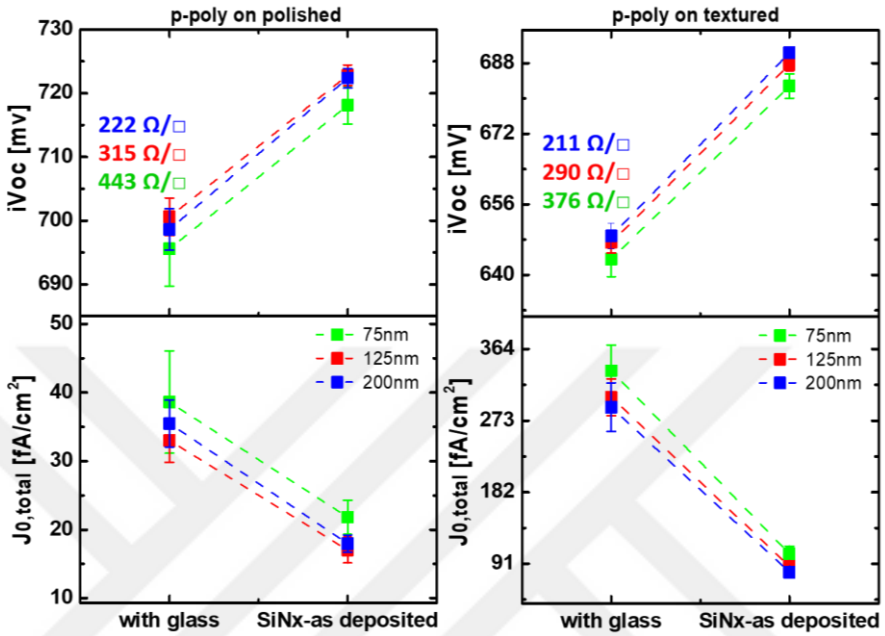


Figure 7.37. Average iVoc and J0,total values for p-polySi on polished (left) and on textured (right) n-Cz wafers. Measured values are averaged on 5 samples per split and 5 different points per sample.

Average iV_{oc} and total J_0 values for p-polySi layers on polished and textured samples are shown in Figure 7.37. Unlike the case for n-polySi, iV_{oc} and corresponding J_0 values for the case of p-polySi layer before SiN_x passivation were approximately the same (Figure 7.37). Putting symmetrical SiN_x layers increased iV_{oc} values of all samples to the same level regardless of the p-polySi layer thickness both for the polished and the textured samples. While the best iV_{oc} for the samples with BSG layer was within the range of 700-704 mV which was increased to 722-725 mV for the polished samples, those for the textured samples were between 649-655 mV and 688-693 mV for the samples staying with BSG and those were passivated with symmetrical SiN_x (Figure 7.38).

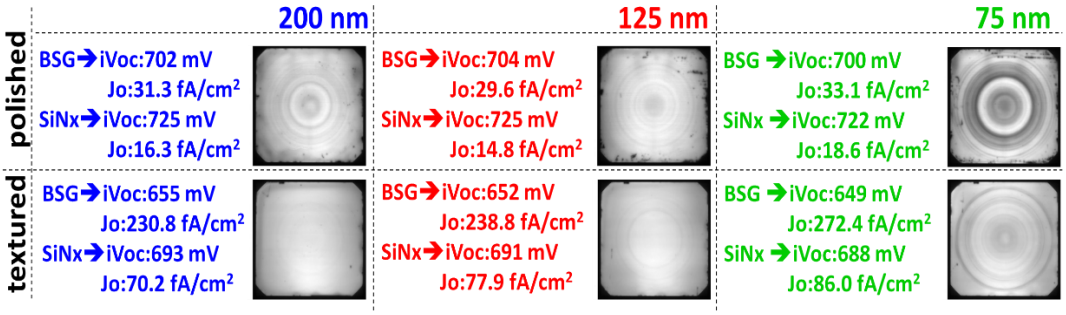


Figure 7.38. Best iVoc and Jo values for p-polySi layer on polished and textured n-Cz wafers with corresponding PL images. PL images were taken for the samples staying with BSG layer.

As the next step samples passivated with n-polySi and p-polySi layers were metallized with FT-Ag and FT-AgAl pastes using the screens shown in Figure 7.3. Sinton PCD measurements were carried out on the regions metallized with various finger pitches and then the samples were fired at various peak temperatures from 745 to 825°C.

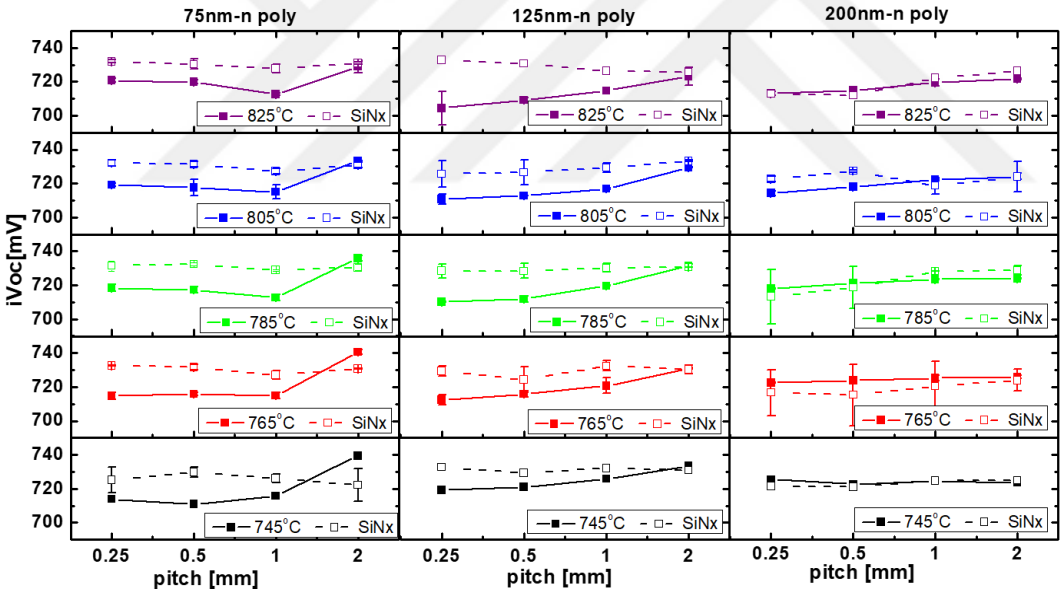


Figure 7.39. Measured iVoc values as a function of varying pitch for 75, 125 and 200 nm thick n-polySi layers. Peak firing temperature was increased from 745 to 825°C. iVoc values of the same samples with symmetrical SiN_x before metallization were given as reference.

The measured iV_{oc} values for $POCl_3$ diffused n-polySi layers are given in Figure 7.39. It was observed that increased pitch was resulting in reduced metallization fraction on constant sample area, and that resulted in increasing iV_{oc} values for all

thickness values of n-polySi layers. For the cases of 75 and 125 nm n-polySi layers, the measured iV_{oc} values for the non-metallized samples were almost always greater than their metallized counterparts with the corresponding pitch values of 0.25, 0.5 and 1 mm. For the samples with the finger pitch of 2 mm, metallized and non-metallized samples performed quite similar for all firing temperatures which means that the lowest metallization fraction results in almost negligible iV_{oc} loss for all n-polySi thicknesses as expected. Unlike 75 and 125 nm thick layers, 200 nm n-polySi layer experienced almost negligible iV_{oc} loss upon metallization for all pitch values. Thus, it could be deduced that the metallization induced losses ($J_{0,c}$) was not only related to the metal fraction and peak firing temperature, but it was also affected by the thickness of the doped polySi layer.

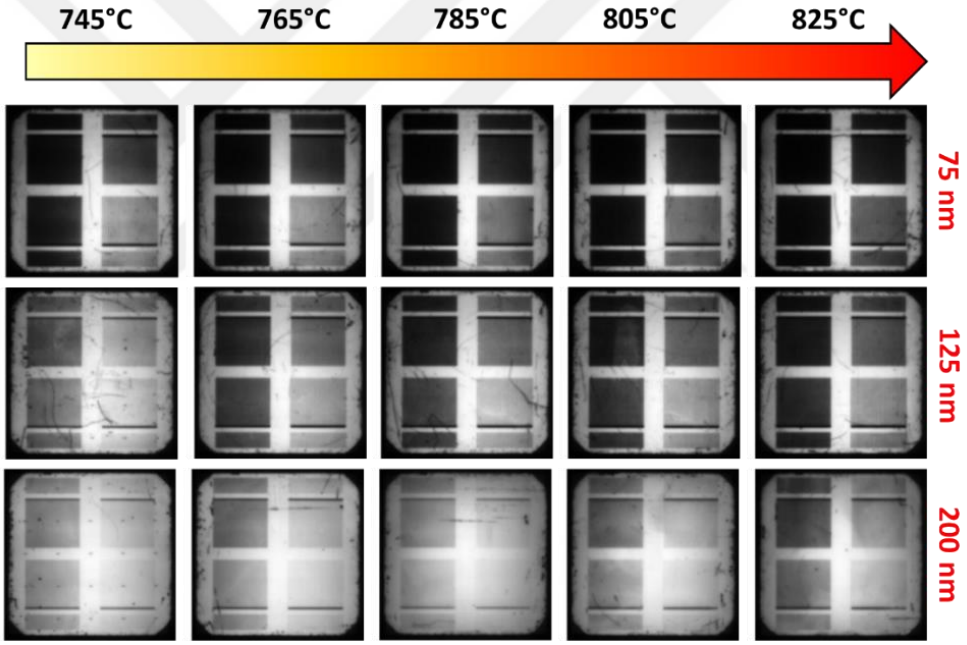


Figure 7.40. PL images for the metallized n-polySi layers on n-Cz wafers after firing.

Considering the PL images given in Figure 7.40, increasing firing temperature was observed to increase contrast in the metallized regions. That could be related to the increased metal induced recombination as a function of increasing firing temperature. Moreover, as the n-polySi layer thickness increases, metallization induced (contact recombination) losses were observed to be suppressed. Thus, PL

images also confirmed the claim that it is not only firing temperature and metallization fraction but also the thickness of passivating layer also determines the contact recombination losses.

For the case of boron doped p-polySi layers on textured n-Cz wafers, the effect of metallization and peak firing temperature on iV_{oc} is given in Figure 7.41. Unlike n-polySi case, firing had a positive effect for all thickness values of p-polySi layers which was more pronounced as the metal pitch increased. Moreover, increasing p-polySi thickness also improved iV_{oc} of the samples not only before metallization but also after metallization and subsequent firing steps. Also considering the iV_{oc} values of the samples before metallization shown with "SiN_x" legend on the graphs of Figure 7.41, it could be deduced that p-polySi layers were quite uniform.

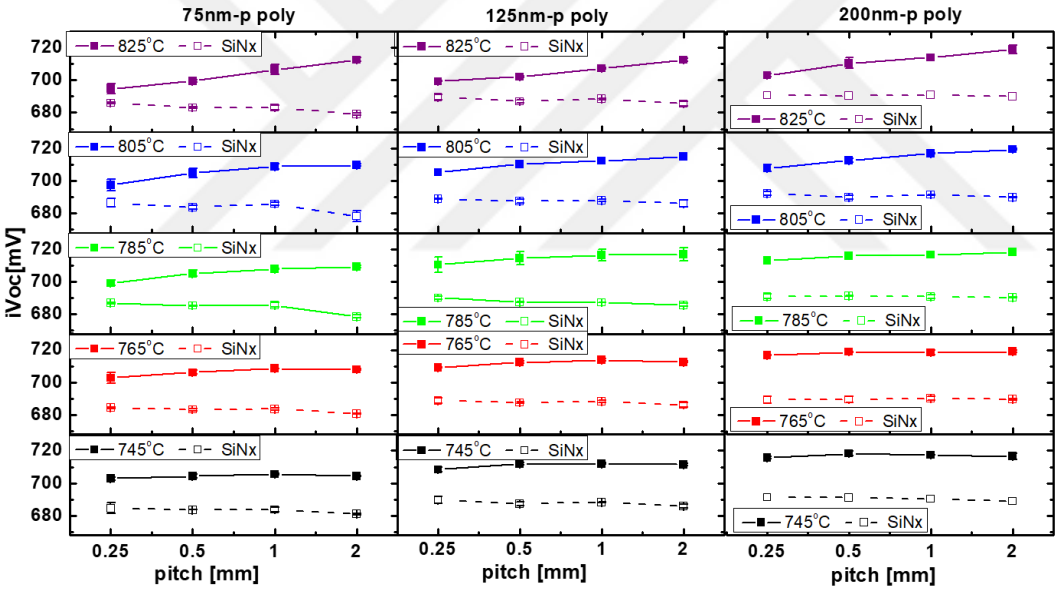


Figure 7.41. Measured iVoc values as a function of varying pitch for 75, 125 and 200 nm thick p-polySi layers. Peak firing temperature was increased from 745 to 825°C. iVoc values of the same samples with symmetrical SiN_x before metallization were given as reference.

While the pitch dependency of n-polysi layers was observed to start at 745°C (except 200 nm thick layers), for the case of p-polySi layers it was starting at 805°C. This could be related to the different contact formation mechanisms of different pastes, and different behavior of n-doped and p-doped p-polySi layers.

Considering PL images given in Figure 7.42, no significant difference was observed for varying p-polySi layer thicknesses while the thickness of n-polySi layers had a more pronounced effect on PL images. The recombinative effect of the metallized regions became more visible starting at the firing temperature of 805°C which was also confirmed by the measured iV_{oc} values given in Figure 7.39.

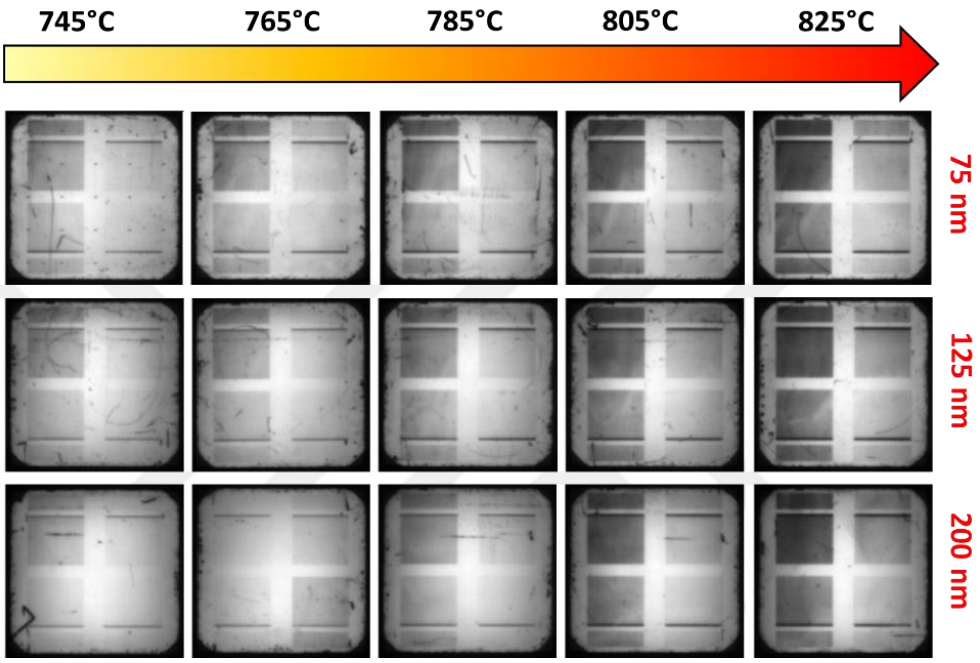


Figure 7.42. PL images for the metallized p-polySi layers on n-Cz wafers after firing.

The purpose at that level was to develop a method relating measured iV_{oc} values and PL images to extract $J_{0,contact}$ on symmetrical samples. For this, measured iV_{oc} values and averaged PL signal for each pitch value was plotted as a function of finger pitch and firing temperature for n-polySi on textured n-Cz wafers (see Figure 7.43).

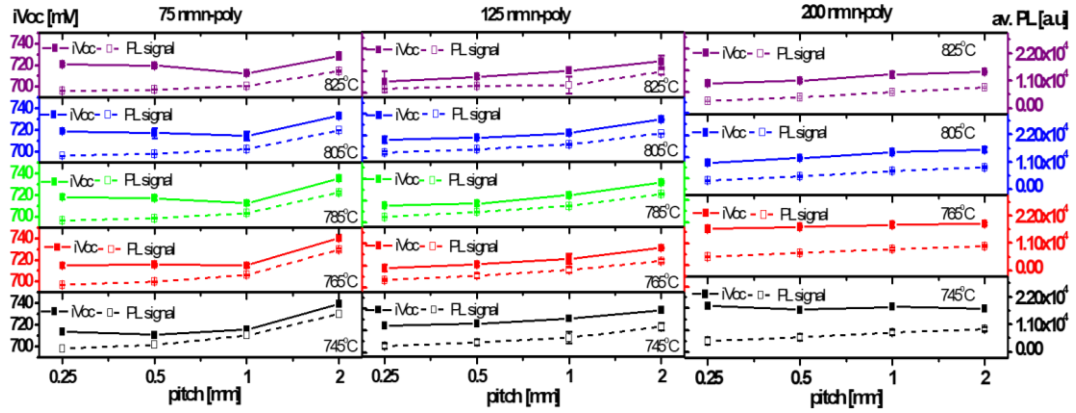


Figure 7.43. Average PL signal and iVoc values for n-polySi on n-Cz wafers. PL signal was averaged over 1.5 cm x 1.5 cm area on metallized regions. PL image for 200 nm layer and 785°C peak firing temperature was missing so no iVoc/PL vs. pitch graph could be plotted for that sample.

It was observed that the same behavior as iV_{oc} with respect to increasing pitch was followed by the average PL signal in arbitrary units. Increasing peak firing temperature was observed to slightly degrade the measured iV_{oc}, the same behavior was observed for the average PL signal, too.

The same procedure was also applied for p-polySi layers on n-Cz wafers where PL images were taken after metallization and firing, and the corresponding results were plotted in Figure 7.44.

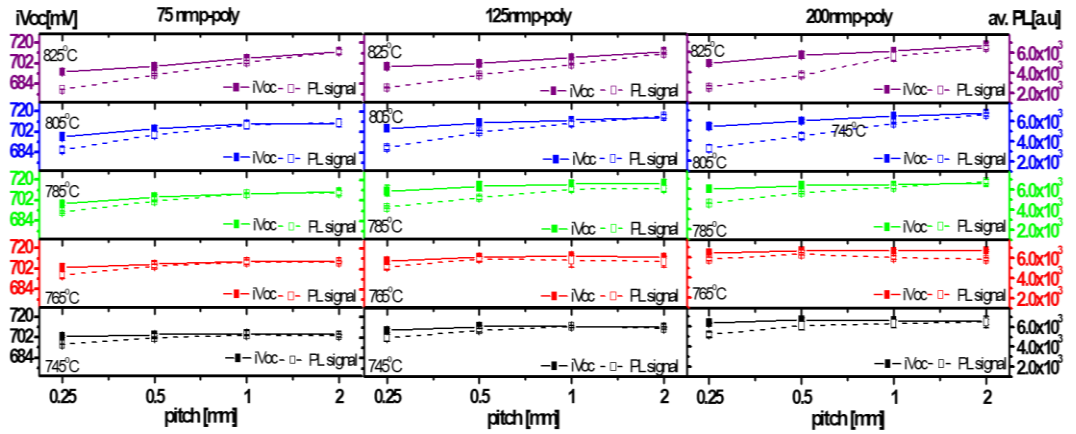


Figure 7.44. Average PL signal and iVoc values for p-polySi on n-Cz wafers. PL signal was averaged over 1.5 cm x 1.5 cm area on metallized regions.

The behavior of average PL signal and iV_{oc} was in perfect agreement especially for the cases of 1- and 2-mm finger pitches. PL signal iV_{oc} values were improved as a function of increasing p-polySi layer thickness.

Despite the agreement in measured iV_{oc} values and average PL signal, still the Voc loss and the reduction in PL signal upon firing was not clarified yet. To better understand the effect of metallization process and to quantify the corresponding losses, drop in iV_{oc} and PL signal was additionally analyzed for both n-poly layers metallized with FT-Ag and p-polySi layers metallized with FT-AgAl, respectively. For this, lumped loss parameters as "*ΔiV_{oc}/uncovered area fraction*" and "*ln[ΔPL]/uncovered area fraction*" were defined for iVoc loss and PL loss, respectively.

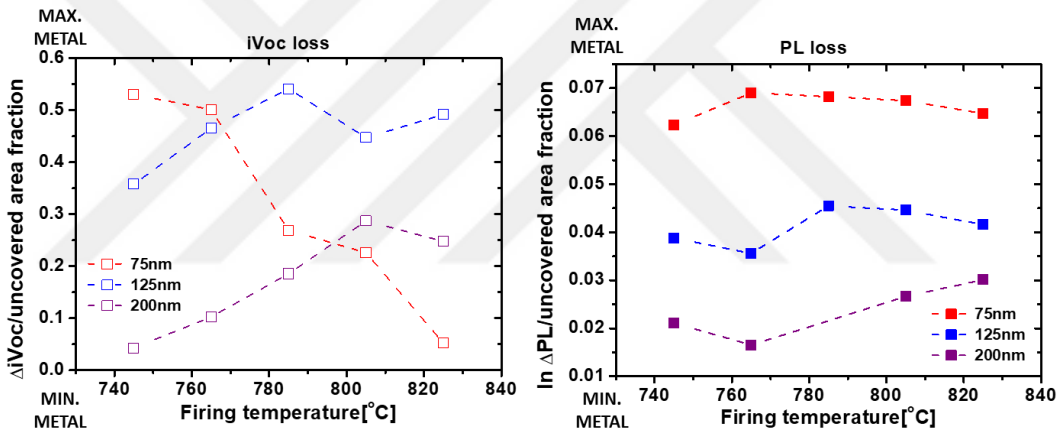


Figure 7.45. Drop in iVoc (left) and PL signal (right) for 75, 125, and 200 nm n-polySi layers as a function of firing temperature and metallization fraction.

For the case of n-polySi layers contacted with FT-Ag paste, iV_{oc} loss behavior as a function of firing temperature was not straightforward as shown in Figure 7.45 (left). Drop in PL loss was observed to be more consistent with respect to polySi layer thickness and peak firing temperature as shown in Figure 7.45 (right). The minimum loss in PL signal was observed for the thickest layer while the maximum loss was observed for the thinnest layer. Moreover, increasing firing temperature increased the loss in PL signal corresponding to increased contact

recombination current. However, the effect of peak firing temperature is not as dominant as the effect of layer thickness.

Considering the iV_{oc} and average PL signal drop as a function of metal fraction and firing temperature, it was observed peak firing temperature had a dominant effect on all thickness values of p-polySi layers while layer thickness had almost no effect on iV_{oc} and PL signal losses as shown in Figure 7.46. Unlike n-polySi case, drop in iV_{oc} for p-polySi case showed firing temperature and layer thickness dependence (see Figure 7.46 (left)).

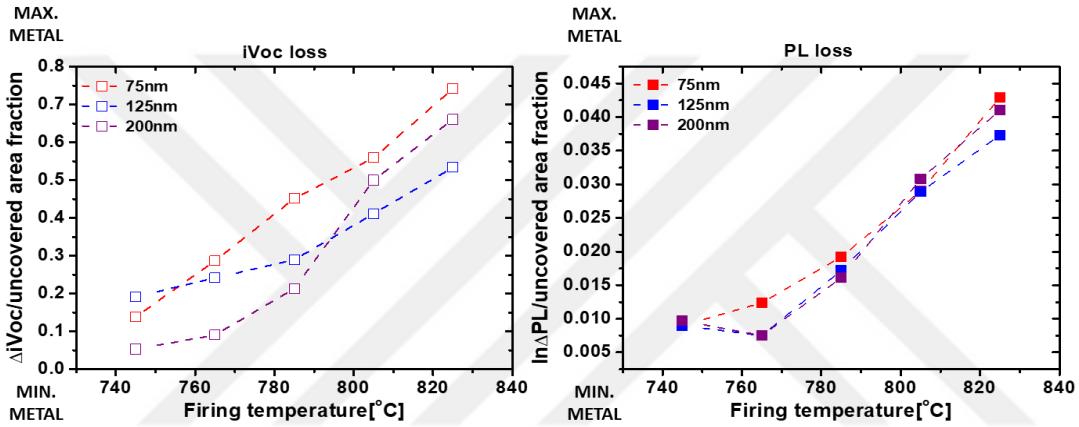


Figure 7.46. Drop in iVoc (left) and PL signal (right) for 75, 125, and 200 nm p-polySi layers. as a function of firing temperature and metallization fraction.

While the layer thickness was the dominant factor affecting the iV_{oc} and PL loss for the case of n-polySi, peak firing temperature had more pronounced influence on the iV_{oc} and PL loss for the case of p-polySi passivated surfaces. Thus, three different sceneries were offered to explain the interaction of FT-Ag with n-polySi and that of FT-AgAl paste with p-polySi passivated surface whose schematics were given in Figure 7.47. For the case of p-polySi contacted with FT-AgAl paste, one scenario (scenario-1) was fitting better compared to the others. Considering the dominant effect of peak firing temperature, it can be speculated that the metal was already confined within the p-polySi layer so that varying the layer thickness did not generate a difference on iV_{oc} and PL signal loss. Thus, the area of interaction between the metal penetrating through the underlying p-polySi layer determines the

metallization induced losses. Regardless of the total thickness of the polySi layer, the area of interaction was affected by the peak firing temperature. The layer thickness could only determine the final position of the penetrated metal, that is the thinner the layer the closer stop to the polySi/SiO_x interface. However, it could be deduced that even the thinnest polySi was thick enough to stop the penetrating metal at a distance without affecting the passivating properties.

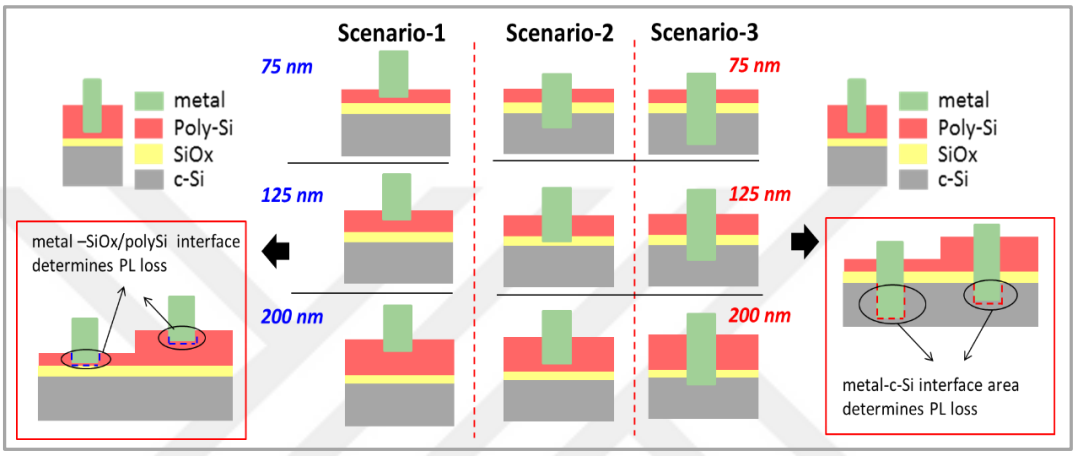


Figure 7.47. Suggested metallization sceneries for p-polySi layers contacted with FT-AgAl and n-polySi layers contacted with FT-Ag paste.

Unlike p-polySi case, two different scenarios were suggested for n-polySi layers contacted with FT-Ag paste named as scenario-2 and scenario-3. Drop in iV_{oc} and PL signal were mainly influenced by layer thickness could be related to more aggressive metal penetration through the n-polySi layer even underlying SiO_x and c-Si. If scenario-2 were valid, the thicker layer would block the penetrating metal more, so that corresponding loss would be suppressed. Thus, the distance between SiO_x/c-Si interface and metal would determine the degree of passivation loss. Considering the loss in PL signal, detrimental effect of metallization on n-polySi was expected to be greater compared to that was observed for p-polySi layers. If scenario-3 were valid, then metal would have already passed through the underlying n-polySi and SiO_x layers and penetrate deep inside the bulk Si. As the n-polySi layer gets thicker, the metal penetrates less through the bulk Si. Thus, the

total interaction area between the metal and c-Si could be speculated as the factor determining the amount of loss.

To confirm above mentioned scenarios and correlate the measured iVoc values and taken PL images in a $J_{0,contact}$ parameter, a methodology was developed based on Quokka2 simulations. The details of the developed model was discussed in Ciftpinar et al. 2017 [110]. As a quick check for the developed methodology, PL images for all thicknesses of n-polySi and p-polySi layers, limiting conditions were checked. Finger pitches of 2 mm and 0.25 mm were chosen as the most and the least metal conditions, with the lowest and the highest firing temperatures of 745 and 825°C, respectively. The regions where PL signal was averaged for modelling are shown on a representative PL image (Figure 7.48).

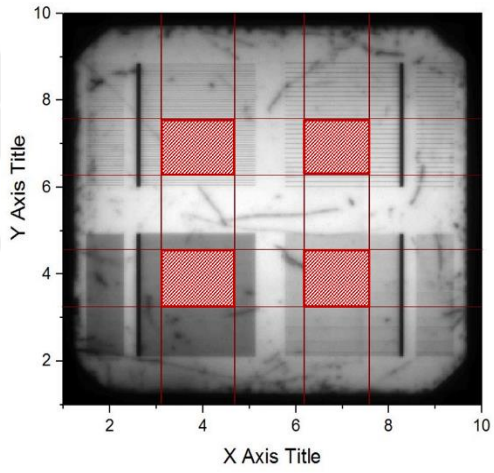


Figure 7.48. A representative PL image used for modelling. The PL signal was averaged over the marked regions. The whole image was 1024 pixels x 1024 pixels, and the marked region was 180 pixels x 180 pixels.

The modelled $J_{0,c}$ and iV_{oc} values are shown in Figure 7.49. The effect of firing temperature on p-polySi and that of film thickness on n-polySi average were observed for the modelled $J_{0,c}$ values, too. Based on Quokka2 simulations, it was observed that FT-Ag paste induced more damage compared to FT-AgAl paste which increased as a function of increasing peak firing temperature. The effect of layer thickness was more dominant for the metallized n-polySi layers while the

effect of increasing firing temperature was more pronounced for the case of metallized p-polySi layers.

significant thickness dependence

n-poly	most metal				least metal			
PV18A	LT		HT		LT		HT	
thickness	Jo,c	iVoc	Jo,c	iVoc	Jo,c	iVoc	Jo,c	iVoc
75	626.0	661	1415.0	642	150.2	718	487.6	706
125	105.4	696	483.3	666	39.4	716	317.0	702
200	77.6	692	234.2	675	142.1	701	251.7	699
p-poly	**most metal**				**least metal**			
L9724	LT		HT		LT		HT	
thickness	Jo,c	iVoc	Jo,c	iVoc	Jo,c	iVoc	Jo,c	iVoc
75	134.2	682	548.1	667	267.7	685	14.7	691
125	79.6	691	409.3	672	199.0	691	255.3	680
200	82.3	692	349.4	676	181.5	695	263.9	695

less thickness dependence

more recombination as T↑

Figure 7.49. Fitted $J_{0,\,contact}$ values for the selected samples of n-polySi and p-polySi layers metallized with FT-Ag and FT-AgAl pastes, respectively. The results taken into red circles were unexpectedly low.

After the preliminary results, both for 0.25- and 2-mm pitches proving that the methodology was working, missing data points in Figure 7.49 were completed. The resulting $J_{0,co}$ values were plotted as a function of peak firing temperature and layer thickness as shown in Figure 7.50.

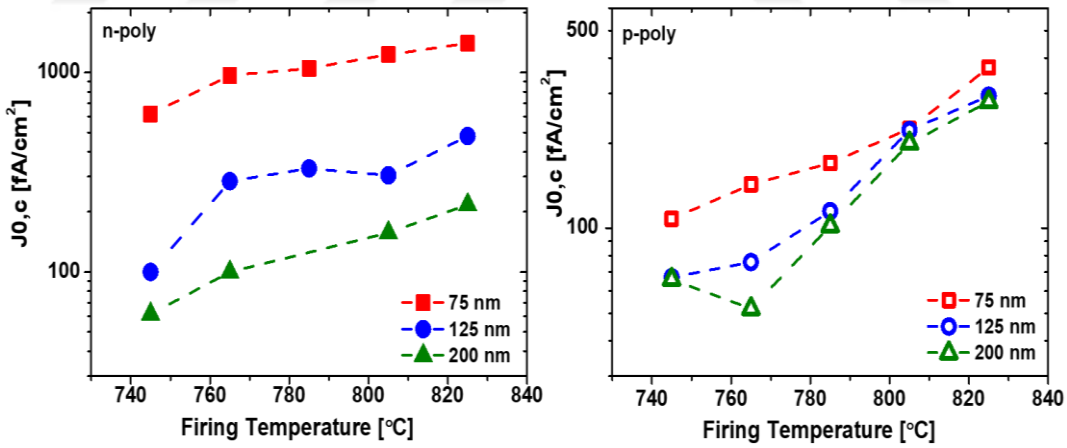


Figure 7.50. Modelled $J_{0,co}$ values for n-polySi (left) and p-poly (right) layers metallized with FT-Ag and FT-AgAl pastes, respectively and fired at various peak temperatures. Method was only applied for the smallest metal pitch of 0.25 mm.

In accordance with the preliminary results, FT-Ag paste was observed to be a strong function of the layer thickness while peak firing temperature had less

pronounced effect on the resulting $J_{0,co}$. The thinner the n-polySi layer resulted in the greater the $J_{0,\ contact}$. Unlike n-polySi, for the case of p-polySi layers, resulting $J_{0,\ contact}$ had a strong dependence of the peak firing temperature. However, especially for higher temperatures above 800°C, the layer thickness had no significant effect on $J_{0,\ co}$.

Following the PL and iV_{oc} measurements, TLM measurements were also carried out as the last and the most detrimental measurement step. Measured contact resistivity (rho,co) values were also used as inputs for the Quokka simulations together with the measured iV_{oc}, sheet resistance and average PL signal. Obtained results revealed that FT-Ag paste could not form proper contacts at the firing temperature of 745°C with extremely high rho,co values around 100 $m\Omega.cm^2$ as shown in Figure 7.51. Increasing the peak firing temperature from 745 to 765°C reduced rho,co values below 10 $m\Omega.cm^2$ level for all thickness values and further increase of the firing temperature did not generate a significant enhancement in contact resistivity. While 75 and 200 nm n-polySi layers with respective sheet resistance values of 135 and 132 Ω/□ had similar contact resistivity values of around 7-8 $m\Omega.cm^2$, 125 nm n-polySi layer with a sheet resistance of 97 Ω/□ had lower rho,co values around 4-5 $m\Omega.cm^2$.

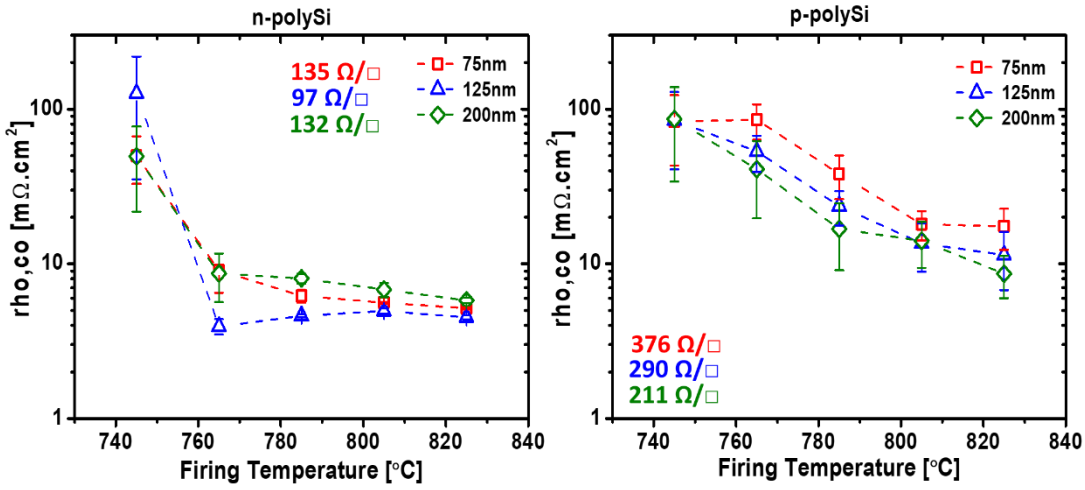


Figure 7.51. Contact resistivity results for FT-Ag (PV18A) on n-polySi (left) and FT-AgAl (L9724) on p-polySi (right). Measurements were carried out for 2 mm finger pitch.

For the case of p-polySi layer, all thickness values had similar rho,co values as shown in Figure 7.51 (right). Unlike n-polySi layers which were properly contacted at firing temperatures above 765°C, it was 805°C for p-polySi layers where rho,co values decreased to 15 $m\Omega.cm^2$ level. It could be said that 805°C is the minimum temperature required to form proper contacts for FT-AgAl paste p-polySi layers. The same behavior was observed for the cases of iV_{oc} loss and PL loss analyses which were shown in Figure 7.46.

Based on the obtained results and suggested contacting scenarios, a FIB-SEM study was designed to understand the contact formation on polySi layers because if the suggested scenarios are valid, then it means that the fire through contacts are not really passivating. For that purpose, a set of samples were taken to TU Twente-MESA+ Institute/NanoLab where cross-section SEM images of the fingers were taken.

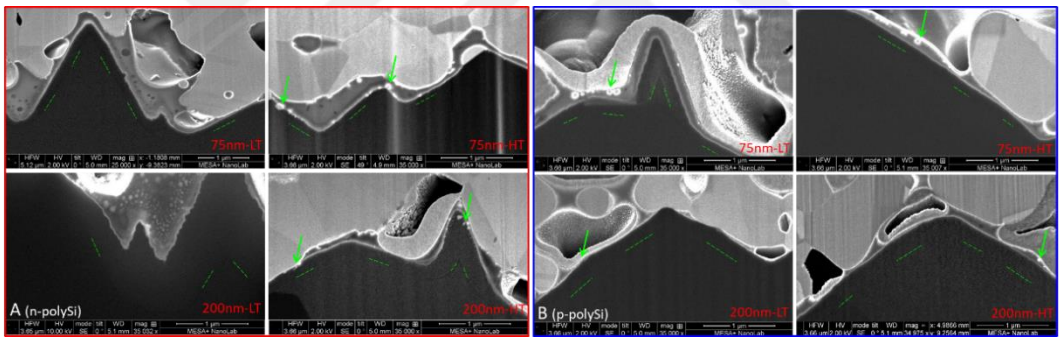


Figure 7.52. Selected FIB-SEM images of the selected samples. For the thickness 75 and 200 nm were chosen where LT refers to the lowest firing temperature 745°C and HT refers to the highest firing temperature of 825°C. The images shown in the red square belong to n-polySi samples while those shown in blue square belong to p-polySi samples.

SEM images revealed the existence of metallic intrusions which were either staying very close to the polySi-SiO_x/c-Si interface or even penetrated through the c-Si side as shown in Figure 7.52. There was no clear effect of polySi layer thickness and peak firing temperature traced by SEM images. However, still, those observed metallic intrusions could be related to the metallization induced recombination losses.

7.3.3 Fabrication of Bifacial Cells with Double Side polySi Passivation

As the last part of polySi studies, a new set of samples whose details were given in the experimental part, was fabricated and used for further analyses. As the starting point, ECV measurements were carried out on BBr_3 diffused p-polySi and P-implanted n-polySi layers. For this study, the set thickness values were 100 and 200 nm for as deposited i-polySi layers which were then exposed to corresponding doping processes. The resulting ECV profiles are shown in Figure 7.53.

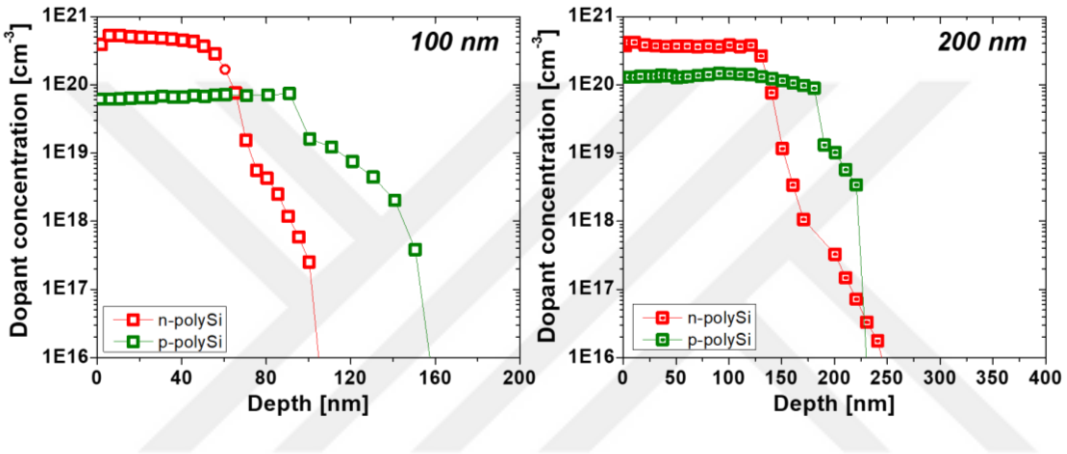


Figure 7.53. ECV profiles of 100 nm thick (left) and 200 nm thick (right) n-poly and p-polySi layers.

It was observed that the respective peak doping concentrations for 100 nm and 200 nm thick p-polySi layers were $7.1x10^{19}$ cm^{-3} and $1.3x10^{20}$ cm^{-3}. While the resulting thicknesses of p-polySi layers were 100 and 200 nm as the set values, corresponding n-polySi layers were approximately 75 and 150 nm thick which were thinner than the set values. Moreover 100 nm thick n-polySi layers were doped with a peak concentration of $5.1x10^{20}$ cm^{-3} while it was $4.8x10^{20}$ cm^{-3} for the case of 200 nm thick n-polySi layers.

Measured iV_{oc} values for polished and textured, n-type, CZ samples symmetrically passivated with n-polySi and p-polySi layers are summarized in Figure 7.54. It was observed that the surface morphology influenced iV_{oc} values right after activation in the BBr_3 furnace. The polished wafers had superior passivation performance compared to their textured counterparts as seen in Figure 7.54 (left). However, after

SiN_x deposition and firing at 785°C, iV_{oc} values reached similar values for all samples.

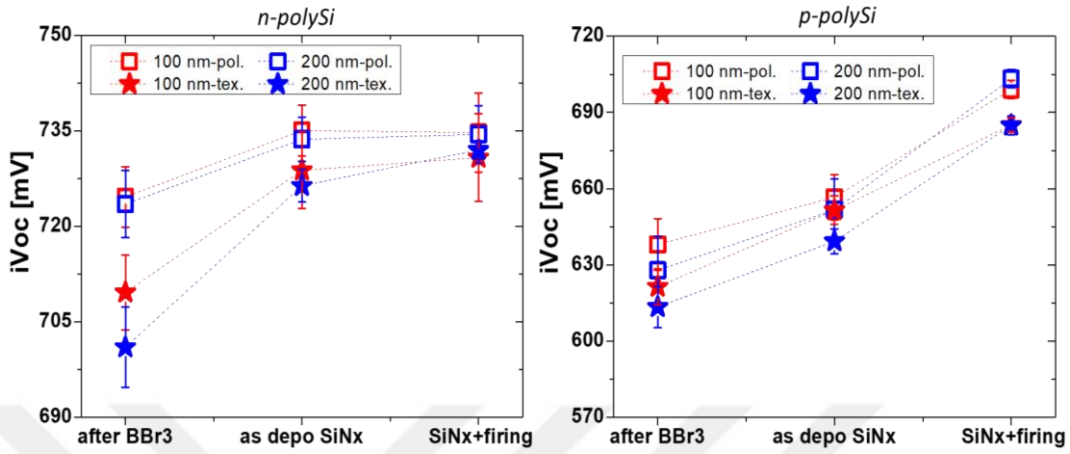


Figure 7.54. iVoc values for various samples passivated with n-polySi (left) and p-polySi (right) layers. Results are averaged over 4 samples for each group. In the graphs' legends "pol." refers to polished and "tex." refers to textured wafers.

Unlike the n-polySi case, for the samples passivated with p-polySi layers both SiN_x deposition and firing steps had a positive effect on measured iV_{oc} values as seen in Figure 7.54 (right). After the firing step, polished samples had greater iV_{oc} values by an amount of 15 mV compared to their textured counterparts.

Following the fabrication and characterization of the symmetrical passivation samples, cells with p-polySi at the front and n-polySi at the rear were fabricated whose cross-section is given in Figure 7.55.

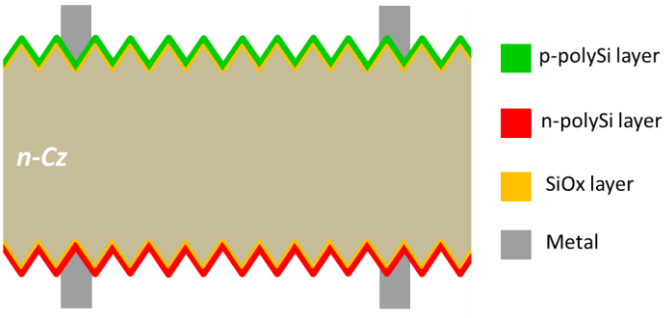


Figure 7.55. Cross-sectional view of both sides passivated solar cell.

As shown in Table 7.5, the best iV_{oc} with the corresponding low J_0 values were obtained on polished samples.

Table 7.5. The iVoc/Voc values of both sides passivated/metallized samples. For the case of both side passivated samples the maximum iVoc and minimum J_0 values are also given.

		half fab. SiNx (as deposited)		**cells FT+firing 785°C**			**cells NFT+curing**		
	thick. (nm)	iVoc (mV)	Jo (fA/cm²)	Voc (mV)	FF (%)	Rseries (mΩ)	Voc (mV)	FF (%)	Rseries (mΩ)
pol.	100	Max:729 715±15	Min:11 30±21	700	37	62.2	709	76.2	7.44
	200	Max:727 722±6	Min:12 16±4	691	51	26.7	706	69.4	11.2
tex.	100	Max:712 709±2	Min:30 33±3	666	73.0	7.4	681	73.1	7.0
	200	708 704±4	Min:35 39±5	676	73.4	7.5	681	73.8	7.9

Metallization with low temperature NFT paste resulted in an iV_{oc} drop of ~20 mV for polished samples and that of ~30 mV for polished samples. The drop in iV_{oc} was more pronounced for the case of FT pastes which would be related not only to the increased thermal budget but also to the more aggressive behavior of the FT paste. Moreover, contact formation of FT-paste on polished samples was quite poor resulting in FF values of 37 and 51% with the corresponding series resistances of 62.2 and 26.7 mΩ. Unlike FT-paste, NFT-paste was less dependent on surface morphology. On polished samples 76.2 and 69.4% FF was obtained for corresponding thicknesses of 100 and 200 nm which were 73.1 and 73.8% for their counterparts on the textured samples.

Analyzing the I-V data revealed a decrease in cell Voc while FF values experienced little or no change for increasing peak firing temperature as given in Table 7.6. Keeping the metal paste at the front side constant (L9724) for various rear side metal pastes (ExoJet, L9724, PV18A) revealed that ExoJet and PV18A were more gently contacting compared to L9724 as cell V_{oc} values were lower for the latter case. Moreover, J_{sc} values were decreasing as the polySi layer thickness was increased from 100 to 200 nm which would be related to the parasitic

absorption of polySi layers. However, varying firing temperature had no significant effect on J_{sc} values.

Table 7.6. Cell parameters for different front/rear metal paste combinations and different firing temperatures. The upper line for each group refers to 100 nm thick polySi layers while the lower line refers to 200 nm.

Tpeak (°C)	rear paste	front paste	Jsc (mA/cm^2)	Voc (mV)	FF (%)	Eta (%)
785	ExoJet	L9724	34.5	666	70	16.1
785			32.3	670	73	15.7
805	ExoJet	L9724	34.6	660	71	16.3
805			32.3	668	74	15.9
825	ExoJet	L9724	34.4	655	72	16.2
825			32.2	660	73	15.6
785	L9724	L9724	34.4	658	70	15.7
785			32.2	663	72	15.4
805	L9724	L9724	34.4	656	71	16.0
805			32.6	658	73	15.7
825	L9724	L9724	34.3	650	71	15.9
825			32.3	649	74	15.4
785	PV18A	L9724	34.5	664	70	16.1
785			32.4	676	73	16.0
805	PV18A	L9724	34.5	662	71	16.2
805			32.3	669	74	16.0
825	PV18A	L9724	34.5	654	72	16.2
825			32.3	663	74	15.9
765	PV18A	PV18A	25.6	671	32	5.5
765			30.0	679	37	7.5
785	PV18A	PV18A	33.6	659	42	9.4
785			31.8	677	49	10.6
640	NFT-L9246	NFT-L9246	32.9	681	73	16.4
640			33.3	680	73	16.5

Switching the rear side paste from L9724 to PV18A had significantly reduced FF values meaning that PV18A (FT-Ag paste) was not contacting properly on p-polySi

layers as expected. As the last combination, both n-polySi and p-polySi sides were metallized with gentler NFT paste resulting in V_{oc} of 680 mV. Despite its gentle contact formation nature, NFT paste results in acceptable FF values of 73%. Thus, for the case of FT pastes, p-polySi layers require to be contacted by an Al-containing paste. On the contrary, n-polySi was properly contacted with FT-Ag or FT-AgAl pastes with a slight drop in cell V_{oc} for the latter. However, the resulting cell efficiencies were much lower than expected from a passivating contact cell structure. So, it was determined to investigate the V_{oc} drop upon metallization or firing in detail. For this, a specially designed screen was utilized to obtain various metallization fractions on the same sample which would be used to extract $J_{0,\,co}$. After the metallization and firing step, V_{oc} values were measured for each metal fraction to calculate $J_{0,\,total}$. Then, plotting $J_{0,\,total}$ vs. metal fraction graph enabled us to extract $J_{0,\,co}$ which is so-called linear fit method. As an alternative method taken PL images were analyzed for $J_{0,co}$ extraction [110] which was also applied in the previous section.

For the linear fit method, plotted $J_{0,\,total}$ vs. metal fraction graphs for 200 nm thick n-polySi and p-polySi layers are shown in Figure 7.56.

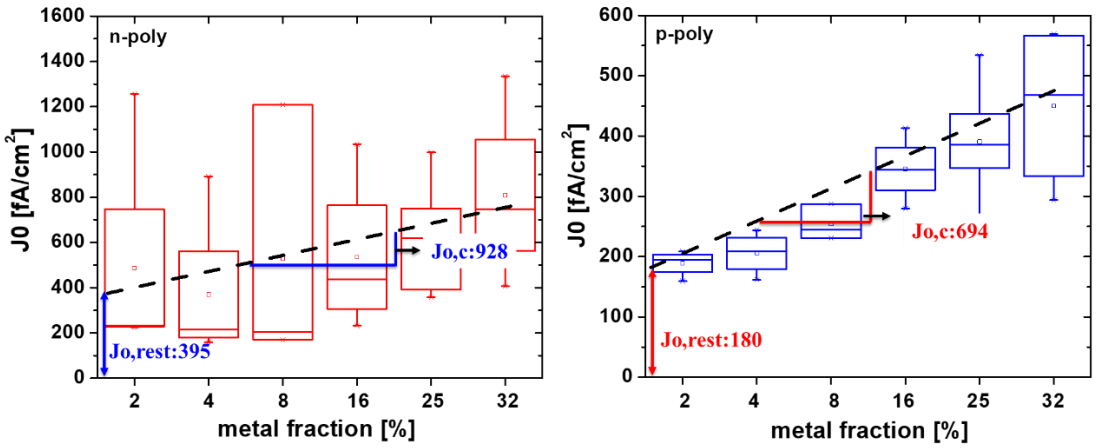


Figure 7.56. Exemplary J_0 vs. metal fraction plots used for a linear fit method to extract $J_{0,\,contact}$ for 100 nm thick n-polySi (left) and p-polySi (right) layers metallized with FT-Ag and FT-AgAl pastes respectively.

The slope of the graph gives the $J_{0,co}$ of the metal (n or p)-polySi interface being analyzed while the offset gives the contribution of un-metallized (n or p)-polySi and the metallized (p or n)-polySi that is in short the contribution of everything else. The calculated $J_{0,co}$ values for n and p-polySi layers were summarized in Table 7.7.

Table 7.7.Calculated J_0 and $J_{0,\ contact}$ values using linear fit method for n-polySi and p-polySi layers.

thickness [nm]	n-polySi $J_{0,co}$ [fA/cm^2]	n-polySi $J_{0,total}$ [fA/cm^2]	p-polySi $J_{0,co}$ [fA/cm^2]	p-polySi $J_{0,total}$ [fA/cm^2]
100	928±1007	5.4	694±240	24.4
200	355±74	15.0	288±38	22.7

The un-metallized n-polySi layers had a quite good passivation quality with respective J_0 values of 5.4 and 15 fA/cm^2 for 100 and 200 nm thick layers. On the other hand, the samples passivated with p-polySi layers had J_0 values of 24.4 and 22.7 fA/cm^2 for 100 and 200 nm thick layers, respectively. Despite their superior passivation performances, n-polySi layers experienced the most significant increase in J_0 upon metallization corresponding to the most severe drop in V_{oc}. The thinner layers had a greater $J_{0,\ co}$ value compared to thicker layers not only for n-polySi but also for p-polySi layers. The p-polySi layers metallized with FT-AgAl paste resulted in lower $J_{0,\ co}$ values compared to n-polySi layers metallized with FT-Ag paste. This could be related to the less aggressive contacting behaviour of FT-AgAl paste compared to FT-Ag or the stability of the doped polySi layers during contact formation. Despite the increased errors for 100 nm polySi, still, the calculated $J_{0,\ co}$ values were greater than expected from passivating contact structures.

For the case of $J_{0,co}$ modelling using PL imaging coupled with Quokka2 simulations, the modelling was carried out for the metal fraction of 2%. The extracted $J_{0,co}$ values using the modelling and linear fit methods are summarized in Table 7.8.

Table 7.8. Comparison of $J_{0,co}$ values extracted using PL images and also linear fit methods.

				from PL modelling		from Voc measurement	
	thickness (nm)	Jo,p-n poly (fA/cm^2)	Jo,p-p poly (fA/cm^2)	Jo,c-n poly (fA/cm^2)	Jo,c-p poly (fA/cm^2)	Jo,c-n poly (fA/cm^2)	Jo,c-p poly (fA/cm^2)
Jo calculated using	100	5.4	24.4	485	540	928±1007	694±240
32% finger+6.5%BB	200	15	22.7	250	145	355±74	288±68
Jo calculated using	100	5.4	24.4	815	820	928±1007	694±240
8% finger+6.5%BB	200	15	22.7	450	300	355±74	288±68
Jo calculated using	100	5.4	24.4	855	800	928±1007	694±240
2% finger+6.5%BB	200	15	22.7	470	250	355±74	288±68

It was realized that, especially with lower metal fractions, the $J_{0,\,co}$ values obtained via PL modelling and linear fit methods get closer. The results obtained in this part of the thesis are compatible with the results obtained in the previous part. Since the modelled and extracted $J_{0,co}$ values were unexpectedly high and some metallic intrusions had been visualized in FIB-SEM measurements in the previous section, a more detailed analysis was required to better understand the contact formation mechanism on doped poly-Si layers. For this a sequential etching study was carried out for the selected samples n-polySi and p-polySi splits metallized with FT and NFT pastes. HR-SEM images of FT-Ag paste on n-polySi layers revealed that the interaction with the metal paste was generating damage to the layers as seen in Figure 7.57.

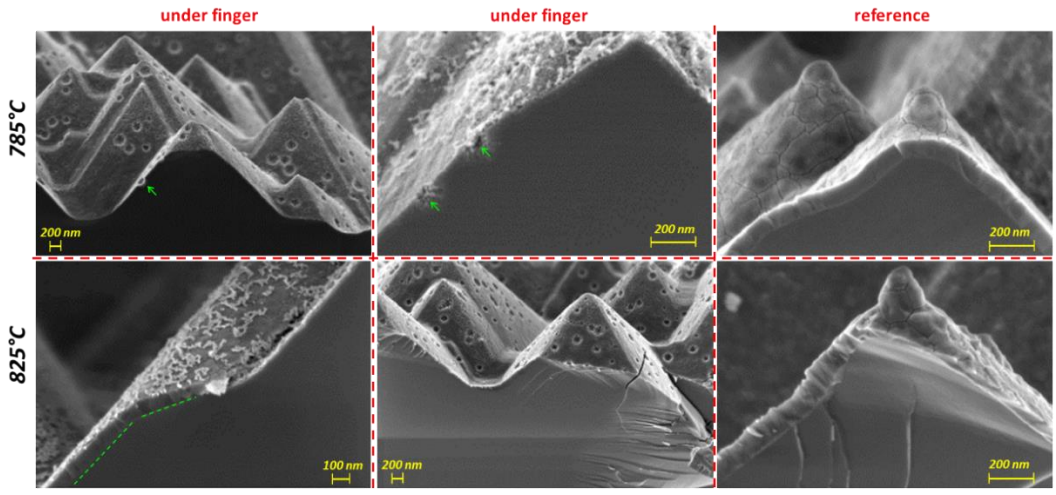


Figure 7.57. High-resolution SEM (HR-SEM) images of n-polySi layers metallized with FT-Ag and fired at 785 and 825°C. The metal was selectively etched and the regions lying under etched metal are named "*under finger*" and the non-metallized regions are named as "*reference*". The analyzed n-polySi thickness was 100 nm. Lines and arrows are for visual aid.

It was observed that the regions lying under metal fingers and busbars were covered with holes where the polySi layer was thinned down or etched away. No clear difference could be observed between the corresponding SEM images of the two firing temperatures as shown in Figure 7.57.

Remembering the fitted and modelled $J_{0,co}$ values for the n-polySi layers which were a function of thickness, not temperature, it could be speculated that the thicker the layer means the slower the penetration of the metallic intrusions through the layer. Moreover, since the n-polySi layer beneath the metal layer is thinned down or completely etched away, using a thicker layer would leave a thicker layer on the surface after contact formation. This would explain the higher V_{oc} values for 200 nm thick layers compared to their 100 nm thick counterparts given in Table 7.6.

For the case of p-polySi metallized with FT-AgAl paste, the visualized polySi damage was suppressed compared to the n-polySi case. However, as shown in Figure 7.58 at the tips of some of the pyramids, inverted pyramids were observed which was correlated with the existence of Al in the metal paste.

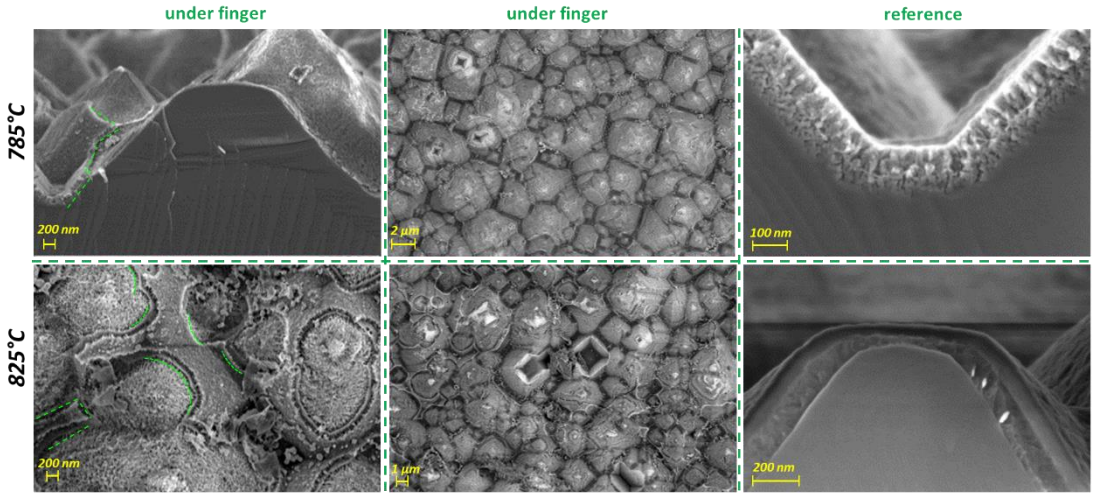


Figure 7.58. High-resolution SEM (HR-SEM) images of p-polySi layers metallized with FT-AgAl and fired at 785 and 825°C. The metal was selectively etched and the regions lying under etched metal are named "*under finger*" and the non-metallized regions are named as "*reference*". The analyzed p-polySi thickness was 100 nm. Lines are for visual aid.

Despite the existence of thinned down or etched regions as in the case of n-polySi, for the case p-polySi layer the generated damage on the layer was mostly concentrated at the tips of the pyramids instead of being distributed all over the surface. The depth of the inverted pyramids is expected to increase as a function of increasing firing temperature and this would explain the temperature dependence of the modelled and fitted $J_{0,contact}$ values shown in Figure 7.50 (right). For the analyzed surfaces passivated with n-polySi and p-polySi layers, corresponding contact resistivity, cell V_{oc} and $J_{0,contact}$ values are shown in Table 7.9.

Table 7.9. Contact resistivity, Voc and $J_{0,contact}$ values of the samples used for the analyses as a function of firing temperature.

	n-polySi/FT-Ag			p-polySi/FT-AgAl		
Tpeak [°C]	rho,co [mΩ.cm^2]	Voc [mV]	$J_{0,co}$ [fA/cm^2]	rho,co [mΩ.cm^2]	Voc [mV]	$J_{0,co}$ [fA/cm^2]
785	5.8±1.6	664	1050	60.1±13.1	664	170
825	3.4±0.7	654	1400	45.0±23.0	654	225

Highly damaged n-polySi layers shown in Figure 7.57 and existing inverted pyramids and locally etched p-polySi layers shown in Figure 7.58 could explain the modelled $J_{0,contact}$ values given in Table 7.9. It means that the applied FT-Ag and FT-AgAl pastes are detrimental to the surface passivation with more pronounced damage for the former. Considering the total metal coverage being less than 5% for a standard H-grid design, the net loss in cell Voc may still be tolerated especially for the case of single-side deposited passivating layers as in the case of PERpoly *(Passivated Emitter and Rear poly-silico*n) cells.

After realizing the damaging behavior of the FT pastes, samples metallized with NFT pastes were also required to be analyzed. In Figure 7.59, the metal etched surfaces of the n-polySi and p-polySi layers are shown. Despite its gentle contact formation nature, NFT paste was also observed to leave some damage on the polySi layers.

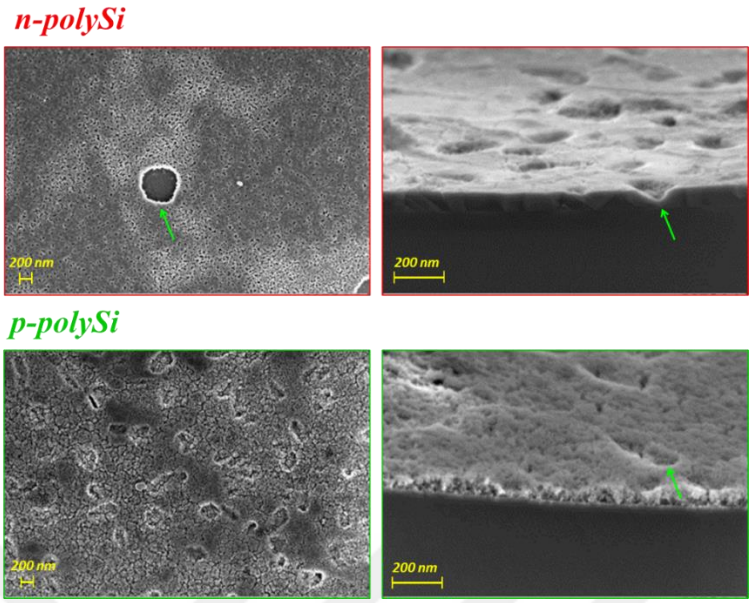


Figure 7.59. High-resolution SEM (HR-SEM) images of n-polySi and p-polySi layers after metal etch-back where the samples were metallized with NFT paste, cured at 650°C. The selected polySi layer thickness is 100 nm. Arrows are for visual aid.

Unlike FT-pastes' aggressive etching mechanism during contact formation, NFT paste was significantly gentler. Despite locally thinned regions, contacted layers were still continuous resulting in much lower $J_{0,contact}$ and higher cell Voc values. NFT paste was resulting in a contact resistivity of 12.9±2.2 mΩ.cm^2 on the n-polySi layer and that of 142±20 mΩ.cm^2 on the p-polySi surface. The corresponding cell V_{oc} was 701 mV which was significantly higher compared to the samples contacted with FT-pastes. By this, it was confirmed that passivating contact cells were partially passivating when the metallization was done using FT-pastes. Moreover, FT-Ag paste used on n-polySi layers were inducing more damage compared to FT-AgAl paste used on p-polySi layers upon firing.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

In this thesis, design and fabrication of high efficiency interdigitated back contact solar cells were studied. The focus was put on the development of a lithography-free, industry-compatible fabrication method without a need for any additional special process equipment in a typical n-type cell production line.

The IBC solar cell structure consists of an emitter and a back surface field region separated by a passivated, undoped gap region. The width of those three regions and the total width of the unit cell is from the key factors determining the device performance. Conducted Quokka2 simulations were used to understand the effect of bulk properties, cell geometries, and the properties of the doped regions on cell performance. The increasing bulk resistivity has a positive effect on the cell performance till a certain value of 3 Ω.cm which then saturates for higher values. The effect of bulk resistivity is almost the same for both FFE-IBC and FSF-IBC cell structures with the superior performance of the former one. For the case of cells with FFE, the emitter fraction has a negligible effect on the cell performance which improves till an emitter fraction of 65-70% and then, saturates for the case of cells with FSF. For proper cell performance, bulk lifetime should be at least 3000 μs and above that value, no significant change could be observed at least for the applied cell designs. Increasing sheet resistances and bulk resistivity were observed to reduce the fill factor. Increasing pitch also reduces the fill factor of the cells which is more pronounced for the case of p-type Si wafers and lower bulk lifetime values (<3000 μs). By the end of the simulation studies, three different pitch values of 750, 1250, and 1700 μm were decided to be used for the fabrication of small area cells while the emitter and BSF sheet resistances were optimized as 115-120 Ω/□ and 45-50 Ω/□, respectively.

The multiple patterning steps required in IBC cell fabrication were done using screen printing. For this, a screen-printable ink was used as the etching resist during the patterning of the diffusion barrier in the dilute acidic solution. The thickness and composition of the utilized diffusion barrier SiN_x layer were optimized as the first step of the fabrication sequence. While the utilized SiN_x layer was deposited with the gas flow ratio of SiH_4:80/NH_3:1220, the thickness was determined to be 120 nm to ensure the blockage of the dopant atoms during high-temperature diffusion processes. Applying the optimized SiN_x parameters and using BCl_3 and $POCl_3$, the first interdigitated pattern could be successfully obtained without any leaky diffusion. Using the SiO_2/SiN_x stack as the front and rear side passivation, and fire-through AgAl and Ag paste for contacting, the first IBC cells were fabricated. The first cell trial resulted in 13.4% and 11.3% conversion efficiencies for FSF-IBC and FFE-IBC cells with the corresponding cell area of approximately 4 cm^2. The FSF-IBC cell had an FF of 76%, V_{oc} of 576 mV, and J_{sc} of 30.5 mA/cm^2 while the FE-IBC cell had FF:71%, V_{oc}: 558 mV, and J_{sc}: 28.6 mA/cm^2.

Next to the fabrication of the first IBC cells, detailed optimization of the BBr_3/BCl_3 and $POCl_3$ diffusion recipes was studied. BBr_3/BCl_3 recipes were separately optimized for the contacted rear emitter and non-contacted front floating emitter regions while the same procedure was applied for the POC_{l3} recipe to be used for contacted BSF and non-contacted front surface filed region. Different passivation sceneries were applied including Al_2O_3/SiN_x, SiO_2/SiN_x, and SiO_xN_y/SiN_x stacks for both boron-doped and phosphorus-doped regions. Passivation performance was examined after diffusion, deposition, and firing steps. For the case of contacted rear junctions, different pastes were used for metallization and contact resistivity studies. In addition to two different Ag pastes, FT-Ag1 and FT-Ag2, one FT-AgAl paste was also utilized for the contact resistivity studies. The optimized BCl_3 recipe resulted in sheet resistance of 48.4±3.9 Ω/□ for the rear and 644.0±43.5 Ω/□ for the front side of the cell. The corresponding iV_{oc} of the passivated symmetrical samples was 662 mV (before firing) and 655 mV (after firing) for the case of the

rear emitter recipe which increased to 676 mV (before firing) and 662 mV (after firing) for the case of front floating emitter recipe. Similarly, the optimized $POCl_3$ recipe resulted in sheet resistance of 83.8±11.4 Ω/□ and 104.7±13.3 Ω/□ for rear and front surfaces, respectively. While the corresponding iVoc values were 626 mV (before firing) and 650 mV (after firing) for the BSF region, they were 635 mV (before firing) and 660 mV (after firing) for the case of the front surface field recipe. Combining those optimized recipes into the interdigitated cell design resulted in iVoc values of 644.6±3.1, 646.7±1.5, and 643.4±2.3 mV for the respective pitches of 750, 1250, and 1700 µm after firing at 885°C for FFE-IBC cells. For FSF-IBC cells, the resulting iVoc values were 652.5±0.5, 654.4±3.7, and 651.7±2.1 mV for the respective pitches of 750, 1250, and 1700 µm. After metallization and co-firing, the best cell efficiency was 19.3% and 19.2% for the respective cases of FFE and FSF-IBC cells. Despite the significant improvement in the cell V_{oc} (635-642 mV) values compared to the first set of IBC cells, the fill factor values were lying within the range of 68-72%. The low fill factor values were mainly due to increased series resistance and decreased shunt resistance at the cell level which was also limiting the short circuit current density at the cell level.

In the second part of the thesis, polySi passivating contact studies were focused on. The passivating properties of the ex-situ doped n-polySi and p-polySi layers have been analyzed together with their contacting properties. The highest iVoc was obtained as 745 mV on polished and 735 mV on the textured wafers with the corresponding total J_0 values of 1.6 fA/cm^2 and 7.4 fA/cm^2 for the case of $POCl_3$ diffused n-polySi layers. For the case of BBr_3 diffused p-polySi layers, the highest iV_{oc} was 725 mV on polished and 693 mV on the textured wafers. The corresponding total J_0 values were 16.3 fA/cm^2 for the case of polished and 70.2 fA/cm^2 for the case of textured surfaces. To better understand the contact passivation properties, two different methods was applied to extract $J_{0,contact}$. For the first method, V_{oc} of the cells with varying metal fractions were measured while a new method was developed to correlate the measured PL signal with the $J_{0,contact}$. The extracted $J_{0,contact}$ values were in the range of 300-400 fA/cm^2 for both n-polySi

and p-polySi layers. Thinner n-polySi layers were resulting in even higher $J_{0,contact}$ values greater than 1000 fA/cm^2 while it was around 700 fA/cm^2 for the case of thinner p-polySi layers. To better understand this, a sequential etching study coupled with HR-SEM imaging was conducted. The images proved that the fire-through metallization was damaging to the polySi layer even to the underlying c-Si surface. The damage given to the n-polySi layer was more pronounced compared to the case of p-polySi layer which was also in line with the extracted $J_{0,contact}$ values. Finally, combining all obtained information into all polySi cell structures resulted in the iV_{oc} of 666 and 676 mV for the respective polySi thicknesses of 100 and 200 nm.

As the future work plan, degradation of iV_{oc} upon firing for the p^+ doped surfaces upon firing will be focused on. Moreover, the low fill factor values at cell level will be taken into consideration. Since the undoped base region passivated with Al_2O_3/SiN_x stack was responsible for parasitic shunting, a new passivation stack should be developed to use at the rear side of the IBC cells. Finally, the developed IBC process flow would be combined with the excellent passivation properties of the polySi layer to produce passivating contact IBC cells which would significantly boost the cell performance.

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