ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

AC-COUPLED SUPPLY MODULATOR DESIGN IN 130 nm PD-SOI TECHNOLOGY

M.Sc. THESIS

Furkan Barin

Department of Electronics and Communication Engineering

Electronics Engineering Programme

JUNE 2023

ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

AC-COUPLED SUPPLY MODULATOR DESIGN IN 130 nm PD-SOI TECHNOLOGY

M.Sc. THESIS

Furkan Barin
(504201216)

Department of Electronics and Communication Engineering

Electronics Engineering Programme

Thesis Advisor: Assist. Prof. Dr. Ahmet Tekin
Thesis Co-Advisor: Assist. Prof. Dr. Ertan Zencir

JUNE 2023

İSTANBUL TEKNİK ÜNİVERSİTESİ ★ LİSANSÜSTÜ EĞİTİM ENSTİTÜSÜ

130 nm PD-SOI TEKNOLOJİSİNDE AC-KUPLAJLI KAYNAK MODÜLATORÜ TASARIMI

YÜKSEK LİSANS TEZİ

Furkan Barin
(504201216)

Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

Elektronik Mühendisliği Programı

Tez Danışmanı: Dr. Öğr. Üyesi Ahmet Tekin
Eş Danışman: Dr. Öğr. Üyesi Ertan Zencir

HAZİRAN 2023

Furkan Barin, a M.Sc. student of ITU Graduate School student ID 504201216 successfully defended the thesis entitled "AC-COUPLED SUPPLY MODULATOR DESIGN IN 130 nm PD-SOI TECHNOLOGY", which he/she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

Thesis Advisor :	**Assist. Prof. Dr. Ahmet Tekin** Istanbul Technical University	.....
Co-advisor :	**Assist. Prof. Dr. Ertan Zencir** University of Turkish Aeronautical Association	.....
Jury Members :	**Assoc. Prof. Dr. Tufan Coşkun Karalar** Istanbul Technical University	.....
	Prof. Dr. Günhan Dündar Boğaziçi University	.....
	Assoc. Prof. Dr. Metin Yazgı Istanbul Technical University	.....

Date of Submission : **26 May 2023**
Date of Defense : **14 June 2023**

To my family,

FOREWORD

I would like to express my sincere gratitude to my advisor, Dr. Ahmet Tekin, and my co-advisor, Dr. Ertan Zencir, for their guidance, knowledge, and support throughout my MSc thesis. Their support made this challenging road much easier for me.

I also would like to express my eternal gratitude to my family, who have been the greatest supporters of my life. I couldn't have completed this thesis without their support.

Finally, I would like to convey special thanks to my friends at TUBITAK BILGEM TUTEL, who never hesitated to share their knowledge with me. It has always been a pleasure to work with such people in the same environment.

JUNE 2023 Furkan Barin

TABLE OF CONTENTS

ABBREVIATIONS

PAPR : Peak-to-Average Power Ratio
C-V2X : Cellular Vehicle-to-Everything
ZCD : Zero Current Detection
LDO : Low-Dropout
SOI : Silicon on Insulator
QFDM : Orthogonal Frequency-Division Multiplexing
PD : Partially Depleted
PA : Power Amplifier
NR : New Radio
LTE : Long-Term Evolution
QPSK : Quadrature Phase-Shift Keying
DCB : DC-Bias Current
DCV : DC-Bias Voltage
EE&R : Envelope Elimination and Restoration
ET : Envelope-Tracking
QAM : Quadrature Amplitude Modulation
AM : Amplitude Modulation
PM : Phase Modulation
CCCS : Current-Controlled Current Source
DAC : Digital-to-Analog Converter
CMRR : Common-Mode Rejection Ratio
VCVS : Voltage-Controlled Voltage Source
OTA : Operational Transconductance Amplifier
PWM : Pulse-Width Modulation
LDMOS : Laterally Diffused Metal-Oxide-Semiconductor
VMC : Voltage-Mode Control
L2H : Low-to-High
H2L : High-to-Low
CMC : Current-Mode Control
SOA : Safe Operating Area
DCM : Discontinuous Conduction Mode
CAD : Computer-Aided Design
APT : Average Power Tracking
I/Q : In-phase and Quadrature
ETSM : Envelope-Tracking Supply Modulator

SYMBOLS

C	**:** Capacitance
R	**:** Resistance
L	**:** Inductance
W	**:** Watt
F	**:** Farad
A	**:** Ampere
f	**:** Frequency
V	**:** Volt
P	**:** Power
η	**:** Efficiency
p	**:** Pico
dB	**:** Decibel
mm	**:** Milimeter

LIST OF TABLES

Page

LIST OF FIGURES

Page

AC-COUPLED SUPPLY MODULATOR DESIGN IN 130 nm PD-SOI TECHNOLOGY

SUMMARY

High peak-to-average values (PAPR) of modern telecommunications standards tend to drop the efficiency of the power amplifiers. The drop in efficiency causes excessive power consumption, which leads to a shortened battery life for mobile systems. As a result, envelope-tracking supply modulator (ETSM) systems are developed to improve power amplifier efficiency by varying their supply voltage. There are different envelope-tracking supply modulator topologies in the literature that combine different amplifier structures with each other. The most popular topologies can be considered hybrid topologies, which take advantage of using two amplifiers in parallel with each other. This hybrid structure allows high-frequency components to be provided by the linear amplifier while low-frequency power is provided by a highly efficient switching amplifier.

The linear amplifier is generally designed with a Class AB output driver, which increases the driving capability and reduces the power consumption of the linear amplifier. A buck converter is mostly used as a switching amplifier to generate DC current for the load. In the literature, a hysteretic control loop is commonly used to control the buck converter with the linear amplifier, and an additional dc-dc converter is added to control the supply voltage of the linear amplifier. To improve efficiency, AC-coupled hybrid topologies are introduced to lower the power consumption of the linear amplifiers.

In this thesis, an AC-coupled hybrid ETSM is designed for 5G cellular vehicle-to-everything (C-V2X) systems that support up to 40 MHz of baseband bandwidth. The system consists of a proposed operational amplifier, a switching amplifier, a current-mode hysteretic buck converter to control the supply of the linear amplifier, a proposed zero-current detection (ZCD) current to detect the reverse current flowing through the inductor, and low-dropout regulators (LDO) for supplying the internal analog circuits. The ETSM is implemented in a 130 nm partially depleted (PD) silicon on insulator (SOI) process, and the die size is 3.051 mm^2.

130 nm PD-SOI TEKNOLOJİSİNDE AC-KUPLAJLI KAYNAK MODÜLATORÜ TASARIMI

ÖZET

Günümüzde kablosuz haberleşmenin ilerlemesiyle birlikte mobil aygıtlar hayatımızda oldukça sık bir şekilde yer bulmaya başlamıştır. Mobil iletişimin bu denli yükselmesi teknolojinin hızlı bir şekilde gelişmesini sağlamıştır. Karmaşık sistemlerde kullanılan entegreler, yeni haberleşme protokolleri ile birlikte daha fazla bilgi işlemeye ve bilgi aktarmaya başlamıştır. Bilgi hızındaki bu artış devam ederken analog ve dijital devre tasarımları gelişmeye devam etmiştir. Transistor boyutlarındaki küçülme birim alanda yapılan işlem hacminde artma yaşanmasını sağlamış ve güç tüketiminin önemli ölçüde azalmasına katkıda bulunmuştur. Verici yapılarındaki iletişimin yapılmasını sağlayan güç kuvvetlendiricilerinin tasarımı, kullanılan bant genişliklerinin artması ve gereken güç seviyelerinin yükselmesi sebebiyle oldukça zorlaşmıştır. Aynı zamanda güç kuvvetlendiricilerin düşük verimliliği mobil aygıtlarının kullanım ömürlerinin önemli bir ölçüde azalmasına neden olmaktadır.

Hücresel V2X teknolojisinin gelişmesiyle birlikte akıllı ulaşım sistemlerinin kullanımı yaygınlaşmaya başlamıştır. 5.895-5925 GHz bandını kullanılan bu iletişim standardı; araçtan-araca, araçtan yayaya ve araçtan internet ağına bilgi aktarımı sağlamaktadır. Bilgi aktarımı yapılırken kullanılan alıcı-verici (transceiver) yapısının yanı sıra güç kuvvetlendiricisinin doğrusallığını iyileştirmek için dijital ön bozma (Digital Pre-distortion) bir gözlem alıcısı da (observation receiver) kullanılmaktadır. Dijital ön bozma, güç kuvvetlendiricisinin doğrusal olmayan davranışından yola çıkarak ürettiği katsayıları kullanarak güç kuvvetlendiricisine iletilen sinyalde bir bozunum yaratır ve bu sayede doğrusallığın artmasını sağlamış olur.

İletişimde kullanılan güç kuvvetlendiricileri yüksek doğrusallık göstermeleri için tasarlandıklarından verimlilikleri oldukça düşüktür. Verimin düşük olması gereksiz güç harcanmasına sebep olmakta, batarya ömrünü kısaltmakta ve istenmeyen ısı yayılımına neden olarak yonga performanslarında düşüşe sebep olmaktadır. Bu istenmeyen durumun önüne geçebilmek ve güç kuvvetlendiricilerinin verimliliğini artırmak amacıyla kaynak modülatörü devreleri tasarlanmaya başlanmıştır. Kaynak modülatörü devreleri, güç kuvvetlendiricinin girişlerine gelen yüksek frekans sinyalin zarf bilgisini kullanarak güç kuvvetlendirici devresinin besleme gerilimini zamana bağlı olarak değiştirir. Sabit bir gerilimin aksine zamana bağlı değişken bir gerilim uygulanması gereksiz güç harcanmasının önüne geçerek güç kuvvetlendiricilerin verimliliğini önemli ölçüde artırmaktadır. Tasarlanan kaynak modülatörü de belirli bir güç harcamasına rağmen toplam verimliliğe bakıldığında önemli bir ölçüde artım gözlenmektedir.

Kaynak modülatörü devrelerinin ilk örneklerine mobil telekomünikasyonun yükselmesinden önce rastlayabiliriz. İlk olarak ses kuvvetlendiricilerinde kullanılan

bu devreler günümüzdeki sürümlerinden farklı olarak düşük bant genişliklerine sahipti. Kullanılan topolojilerinde çok az değişiklik olmuş olsa da literatürde yapılan çalışmalar, farklı kuvvetlendirici topolojilerini birbirleriyle seri veya paralel bağlayarak optimum çözümü bulmaya çalışmıştır. Günümüzde popüler olarak kullanılan ve bu tezin de konusu olan hibrit topolojiler en yüksek verimliliğe ve en yüksek bant genişliğine ulaşılmasını sağlayan topolojilerdendir. Yüksek hızlı ve düşük verimliliğe sahip bir kuvvetlendirici ile düşük hızlı ve yüksek verimliliğe sahip bir kuvvetlendiricinin birbirine paralel olarak bağlanmasıyla oluşturulan bu kaynak modülatörü yapısı, en popüler kaynak modülatörü yapılarındandır. Genel olarak düşük hızlı kuvvetlendirici, hızlı kuvvetlendiriciden aldığı geri besleme sinyali ile çalışır. Yüksek hızlı kuvvetlendiricinin yüksek akım sağladığı durumlarda düşük hızlı kuvvetlendirici bu bilgiyi geri besleme yöntemiyle elde eder ve yüksek hızlı kuvvetlendiriciye akım desteği sağlar.

AC-kuplaj kapasiteli kaynak modülatörleri ise klasik topolojilerde yapılan bir iyileştirmeye dayanmaktadır. Yüksek hızlı kuvvetlendiricinin besleme gerilimi düşürmek ve bu sayede harcanan enerjiyi azaltmak amacıyla yüksek hızlı kuvvetlendirici ile güç kuvvetlendiricinin arasına bir AC-kuplaj kapasitesi yerleştirilir. Yerleştirilen bu kapasitenin üzerindeki DC gerilim seviyesi sisteme eklenen fazladan bir geri beslemeye bağlı olarak kontrol edilmektedir. Yavaş geri besleme olarak da adlandırılan bu geri besleme, yüksek hızlı kuvvetlendiricinin çıkış akımına DC akım ekleyerek kuplaj kapasitesini yükler ve DC gerilim oluşturur. Oluşan bu DC gerilimin değeri, sistemin içerisindeki sayısal analog dönüştürücü (DAC) ile isteğe bağlı olarak değiştirilebilir bir yapıdadır.

Sistem içerisindeki yüksek hızlı kuvvetlendirici genel olarak AB sınıfı çıkış sürücüsü ile tasarlanmaktadır. AB sınıfı çıkış sürücü ile kuvvetlendirici, çıkışına kutuplama akımından çok daha yüksek akım sağlayabileceğinden kuvvetlendiricinin DC güç kaybını düşürür. Düşük hızlı kuvvetlendirici yapısı olarak kullanılan Buck dönüştürücü yonga dışı bulunan bobin ile güç kuvvetlendiricisine DC akımı sağlamaktadır. Yüksek hızlı AB sınıfı kuvvetlendirici ile Buck dönüştürücü arasındaki geri besleme histerik bir yapıdadır ve kontrol sinyalinin frekansı zamana bağlı değişim göstermektedir. Histerik kontrol döngüsünü oluşturabilmek için histerik bir karşılaştırıcı devresine ihtiyaç duyulmaktadır. Pozitif geri besleme ile elde edilebilen karşılaştırıcı devresi, güncel CMOS teknoloji ile kolayca tasarlanabilmektedir. AB sınıfı kuvvetlendirici, girişindeki zarf sinyaline bağlı olarak güç kuvvetlendirici devresine akım sağladığından bu akımı oluşturabilmek için besleme gerilimi genel olarak yonga içi bir dc-dc dönüştürücü ile sağlanmaktadır. Çekilen akımın miktarı ve bant genişliği, giriş sinyalinin zarf bilgisine bağlı olduğundan tasarlanması gereken dc-dc dönüştürücü buna bağlı olarak değişiklik göstermektedir. Aynı zamanda yonganın tamamını besleyen gerilimde düşüm meydana gelmesi durumda kaynak modülatörünün çalışmaya devam edebilmesi için AB sınıfı kuvvetlendiriciyi besleyen dc-dc dönüştürücü genel olarak Buck-Boost olarak tasarlanır. Besleme gerilimin düşmesi durumda Buck-Boost dönüştürücü Boost yapısına geçerek AB sınıfı kuvvetlendiricinin çıkışında bozunum oluşturmamasını sağlar.

Bu tezde 5G NR standardı için 40 MHz bant genişliğini destekleyecek AC-kuplajlı bir kaynak modülatörü tasarlanmıştır. Tasarlanan yüksek hızlı kuvvetlendirici, iki

aşamalı bir işlemsel kuvvetlendirici devresidir. İlk aşaması işlemsel geçiş iletkenliği kuvvetlendiricisi (OTA) olarak tasarlanmıştır. İkinci aşaması ise yüksek akım sağlayabilmek için AB sınıfı olarak tasarlanmıştır. Tasarlanan kuvvetlendiricinin içerisinde yüksek gerilimden kaynaklanan kırılmaları engellemek amacıyla koruma devreleri eklenmiştir. Düşük hızlı kuvvetlendirici olarak klasik Buck devre yapısı kullanılmıştır. AB sınıfı yüksek hızlı kuvvetlendiricinin besleme gerilimini sağlamak üzere akım modlu histerik Buck dönüştürücü tasarımı yapılmıştır. Bobin üzerindeki ters akımı engellemek amacıyla Buck dönüştürücünün içerisine bir sıfır akım tespit devresi eklenmiştir. Tasarlanan devrelerin serimleri tez içerisinde gösterilmiştir. Kaynak modülatörünün ve alt-bloklarının benzetim sonuçları tez içerisinde belirtilmiş ve yorumlanmıştır. Kaynak modülatör tasarımı 130 nm PD-SOI CMOS teknolojisi ile tasarlanmıştır. Kaynak modülatörünün kapladığı alan 3.051 mm^2 olarak ölçülmüştür.

1. INTRODUCTION

In today's wireless communication systems, power amplifiers (PA) are used to transmit the complex baseband signal with high power and efficiency. On the other hand, modern telecommunication standards such as Long-Term Evolution (LTE) or 5G New Radio (NR) use modulation schemes such as orthogonal frequency-division multiplexing (OFDM), quadrature phase-shift keying (QPSK), and 64 - quadrature amplitude modulation (QAM), which have a high PAPR. This high PAPR value in modulation schemes tends to drop the efficiency of the overall transceiver system because RF PAs operate at average power most of the time with a large backoff.

To increase the efficiency of the RF PAs with time-varying envelope signals, several solutions have been proposed [1]–[4]. The dynamic biasing technique reduces the RF PA's DC power consumption by changing the dc-bias voltage (DCV) or dc-bias current (DCB) of the PA depending on the output power level [5]. In the load modulation technique, the load impedance of the RF PA is changed depending on the input signal, so the maximum efficiency of the PA is always maintained [6,7]. In both envelope elimination-restoration (EE&R) and envelope-tracking (ET) techniques, the supply of the RF PA is dynamically varied according to the input envelope voltage, as seen in Figure 1.1 [8]–[10]. Thus, excessive power consumption caused by constant supply voltage is prevented.

ET supply modulators use the amplitude-modulation (AM) information of the envelope signal to modulate the supply voltage of the RF PAs [11]–[13]. Instead of using a constant voltage for RF PAs, the ET system provides a dynamic supply voltage with minimum distortion. ET systems can also be considered as an improvement on EE&R technique, which both amplitude-modulation and phase-modulation (PM). Since the EE&R technique is dependent on both AM and PM information, a timing mismatch in EE&R becomes much more crucial than in the ET technique [14].

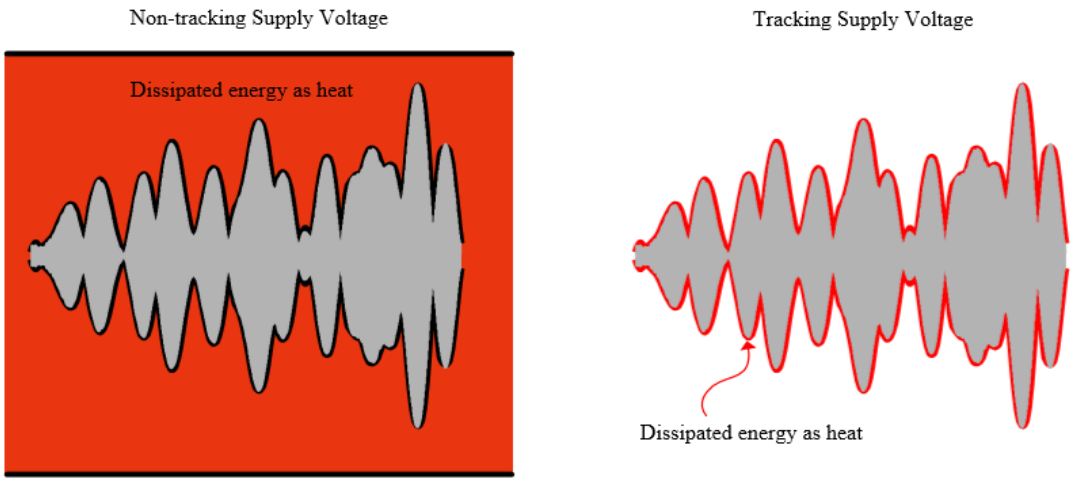

Figure 1.1 : Non-tracking Supply Voltage vs ET

1.1 Purpose of Thesis

The design of an AC-coupled envelope tracking hybrid supply modulator is the main purpose of this thesis. A supply modulator circuit generates a supply voltage for PAs and consists of many subcircuits with local feedback. All of these subcircuits must operate without limiting the supply modulator's performance. This thesis aims to provide a thorough explanation of the system's operation and the subcircuits' operating principles.

1.2 Literature Review

Designing a supply modulator for a power/audio amplifier has been a highly preferred research field for the last 15 years. Even before the rise of wireless communication, there has always been a need for efficiency improvements for power amplifiers. In the literature, there have been several works that increase the power amplifier's efficiency by combining different amplifier topologies in parallel or series with each other.

LDO-based linear modulators take advantage of their simple structure and high bandwidth [6,15,16]. However, efficiency of this modulators can be considered quite low because all the RF power is delivered by the power transistor of the LDO, which is mostly always on.

Modulating the supply of the RF PAs with highly efficient switching regulators are reported in [17,18]. Despite highly efficient operation, high ripple noise and low bandwidth limit the usability of this kind of the supply modulator topologies.

Parallel hybrid envelope amplifiers are well-known topologies, even before they have found a place in mobile telecommunication systems. Several studies have been done to improve the efficiency of the audio amplifiers. These studies have explored the utilization of a Class-AB operational amplifier in parallel with a switching amplifier [19,20]. Additionally, the behavior of hysteretic hybrid structures has been analyzed in [21] for different output voltages and load resistances.

In recent years, classical hybrid amplifiers have been resurfaced to be used in mobile telecommunication systems to increase the efficiency of the RF PAs. In this methodology, a high-speed Class AB linear amplifier is used in parallel with a highly efficient switching amplifier to provide the power required by PA [22]–[31].

The AC-coupled ETSM is introduced in [32] to reduce power consumption of the linear amplifier by shifting the output voltage of the linear amplifier with a large off-chip capacitor [33]–[39].

As an alternative to these methods, multi-level converter topologies are proposed to change the supply voltage with discrete voltage levels depending on the input envelope voltage [40,41].

1.3 Organization of Thesis

The thesis is organized as follows: In Chapter 2, envelope tracking systems and conventional envelope tracking supply modulator architectures are explained. In Chapter 3, the structure of the designed AC-coupled ETSM and its sub-blocks are explained. In Chapter 4, the simulator results of the supply modulator and sub-blocks are presented. Finally, in chapter 5, the conclusions about the thesis are given, and future works about the design improvements are discussed.

2. ENVELOPE TRACKING SUPPLY MODULATOR ARCHITECTURE

2.1 Introduction

RF PAs are the key building blocks in modern telecommunication systems for the transmission of high-speed data. Modern telecommunications standards, such as LTE or 5G NR, have high PAPR values, which drop the efficiency of the RF PAs. ET supply modulators use the envelope information of the transmitted signal to provide a varying supply to RF PA, thereby increasing the efficiency of RF PA.

Figure 2.1 shows the block diagram of the conventional ET supply modulator architecture. The envelope signal is provided to the supply modulator with a digital-to-analog converter (DAC) and is low-pass filtered to remove unwanted switching noise from the converted envelope signal. An envelope-shaping function is applied to improve the efficiency of the supply modulator by artificially manipulating the input envelope. The supply modulator's output is connected to the power amplifier to produce a dynamic supply. A delay element is usually put into the input of the power amplifier to match the timing between the input envelope signal and the dynamic supply voltage.

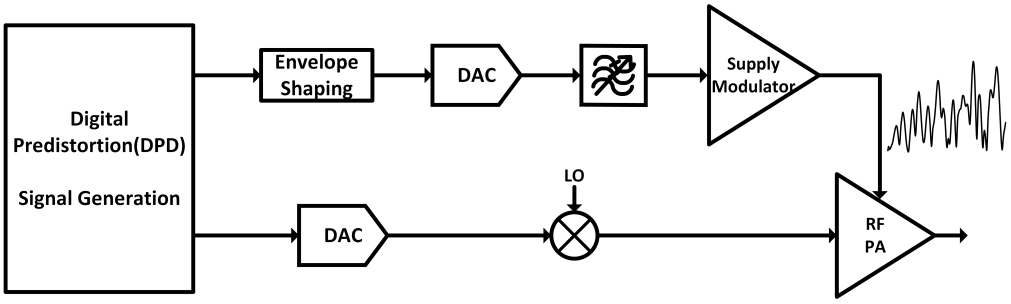

Figure 2.1 : Conventional ET Supply Modulator Block Diagram

2.2 Parallel Hybrid Envelope Tracking Supply Modulator

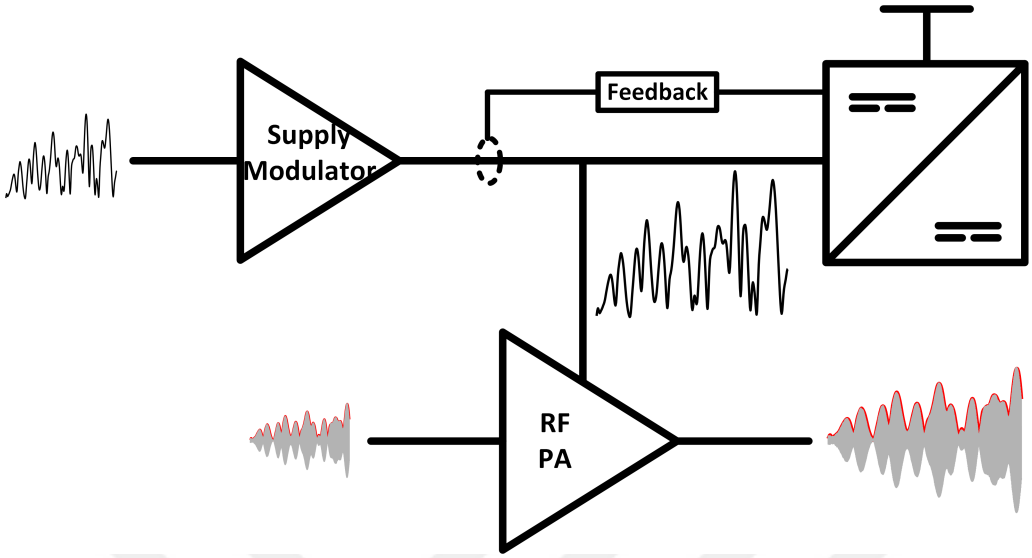

Figure 2.2 : The parallel hybrid envelope-tracking supply modulator

Figure 2.2 shows the block diagram of the parallel hybrid envelope tracking supply modulator. The system consists of a low-efficiency, high-speed linear amplifier and a high-efficiency, low-speed switching regulator. Typically, linear amplifiers are selected as a rail-to-rail Class AB topology to increase efficiency and cover the whole supply range. An additional switching regulator is usually inserted to dynamically change the supply of the linear amplifier under various operating conditions.

A circuit-level description of the hysteretic parallel hybrid supply modulator is depicted in Figure 2.3. Input envelope signals are usually applied differentially to increase the common-mode rejection ratio (CMRR). The sensing mechanism is usually accomplished by inserting a small resistor between the RF PA's supply and the output of the linear amplifier. However, this additional sensing resistor drops the efficiency of the supply modulator, and several other works have been published to solve this problem [2,16].

There are two different feedback loops in the system. The first feedback is applied to the high-speed linear amplifier to maintain the time-varying AC current, and the second one is applied to the PWM switching converter to maintain the DC current.

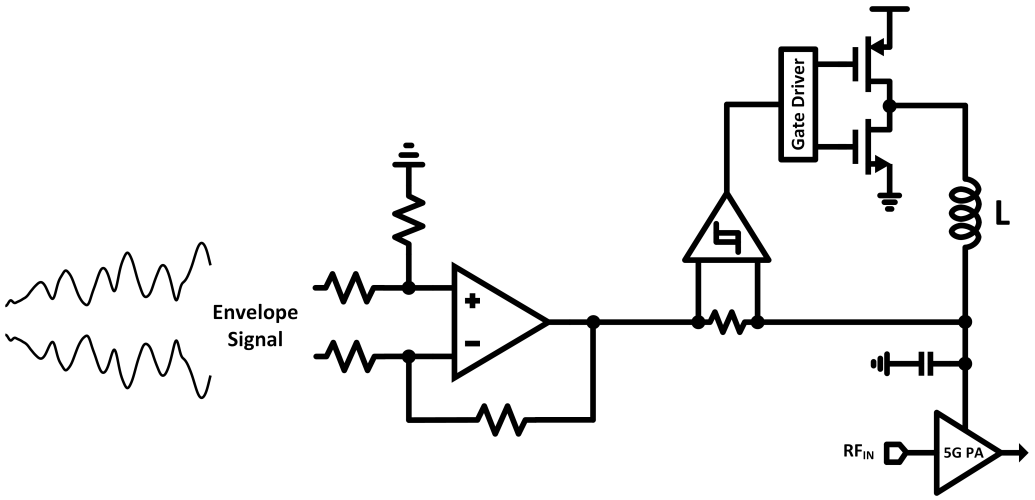

Figure 2.3 : Circuit level description of hysteretic hybrid supply modulator

As illustrated in Figure 2.3, the supply modulator has a hysteretic type of control loop. Hysteretic loops are self-oscillating (bang-bang) types of loops in which the oscillation frequency is non-constant and varies depending on the circuit parameters. The speed and simplicity (no compensation is needed) make hysteretic control loops highly selectable for supply modulator architectures. In Figure 2.3, the hysteretic comparator creates a control signal when the linear amplifier generates an AC current, which passes through the sensing resistor and creates a differential voltage higher than the hysteresis value. If the linear amplifier generates too much AC current that flows through the supply of the power amplifier, the control loop turns on the PMOS transistor in the buck converter and reduces the current of the linear amplifier. Similar behavior happens when the linear amplifier generates too much AC current in the opposite direction, and the control loop turns on the NMOS transistor and reduces the output current of the buck converter.

The switching frequency of the hysteretic hybrid supply modulator can be expressed as [10]

$$f_{sw} = \frac{R_{\text{sense}} \cdot V_{ETSM}(t) \cdot (V_{DD} - V_{ETSM}(t))}{2 \cdot V_{DD} \cdot N \cdot L \cdot V_{HYSTERESIS}} \tag{2.1}$$

where R_{sense}, V_{ETSM}, V_{VDD}, N, L, and $V_{\text{HYSTERESIS}}$ are the values of the sensing resistor, the supply modulator's output, the supply voltage of the overall system, the current gain ratio, the inductor value of the buck converter, and the comparator's hysteresis, respectively.

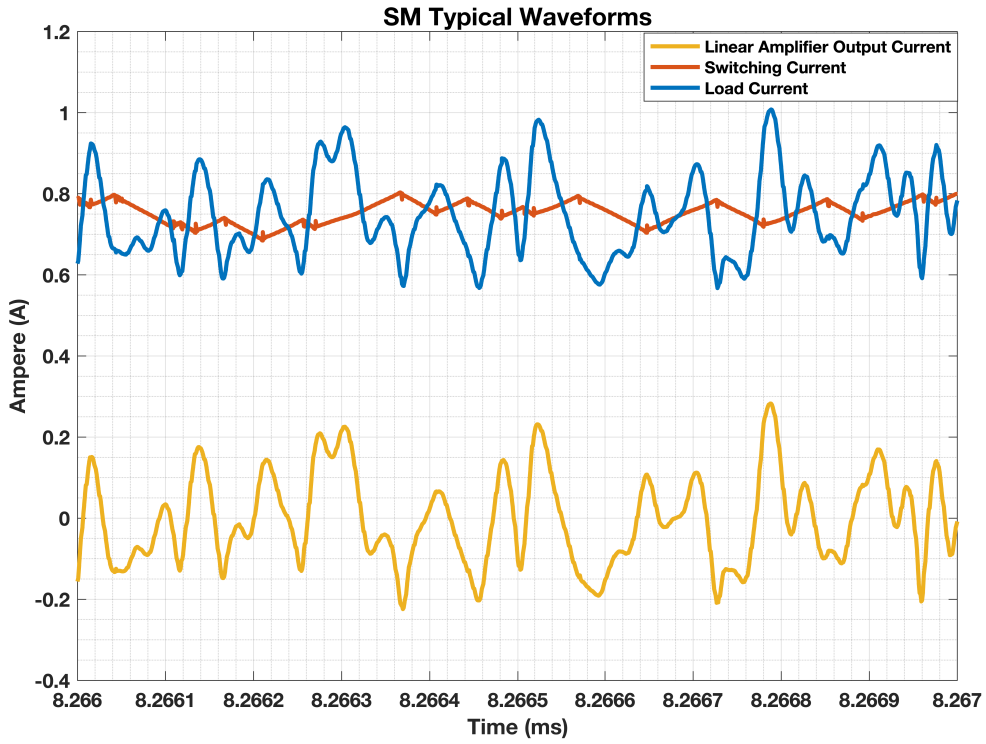

Figure 2.4 : The typical current waveforms of conventional supply modulators

The typical current waveforms of the parallel hybrid envelope tracking supply modulator can be seen in Figure 2.4. The average output power is supplied by the Isw, which is the current of the switching converter. The linear amplifier senses the output voltage with feedback and applies an additional AC current to set the supply voltage of the RF PA relative to the differential envelope voltage.

The AC-coupled version of the supply modulator is depicted in Figure 2.5. The output voltage of the linear amplifier is shifted by a large off-chip coupling capacitor. Thus, a lower supply voltage can be used for the linear amplifier, which increases the system's efficiency. However, the new DC feedback control loop that controls the DC voltage level across the off-chip capacitor makes the design more complicated and increases the design time.

The DC feedback loop controls the DC voltage across the capacitor by generating a DC current offset in the linear amplifier output. The DC offset voltage equations are

given in [37]

$$\Delta V_{OFFSET} = -\frac{1}{C} \cdot \int I_{\text{LAOUT}}(t)dt \tag{2.2}$$

$$I_{\text{LAout}}(t) = I_{\text{Supply}}(t) - I_{SW}(t) \tag{2.3}$$

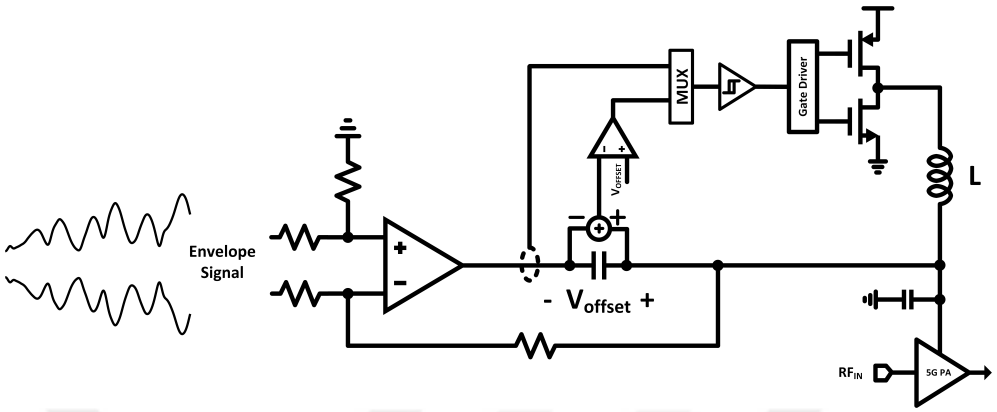

Figure 2.5 : The schematic diagram of the AC-coupled supply modulator

2.3 Parallel Hybrid Supply Modulator Power Loss Sources

The total efficiency of the RF transmitter heavily depends on the combined efficiency of the supply modulator and RF PA [6]. This can be described as

$$\eta_{\text{overall}} = \eta_{\text{ETSM}} * \eta_{RFPA} \tag{2.4}$$

So, increasing the efficiency of the supply modulator also increases the efficiency of the RF transmitter. However, the high bandwidth requirements of modern telecommunications standards create a challenge for high-efficiency supply modulators. This can be attributed to the nonlinear bandwidth extension of the complex baseband signal as

$$E_{nv}(t) = \sqrt{I(t)^2 + Q(t)^2}, \quad \phi(t) = e^{\arctan\left(\frac{Q(t)}{I(t)}\right)} \tag{2.5}$$

As can be seen from (2.5), envelope extraction causes a nonlinear operation for the I(t)/Q(t) data. This spectral growth can be three times of the original RF bandwidth [2]. Thus, a high-bandwidth linear amplifier must cover the increased envelope signal's bandwidth without adding distortion to the output of the RF PA.

Major power losses in an envelope-tracking supply modulator system are shown in Figure 2.6. Main losses can be classified as: dynamic and static power consumption of

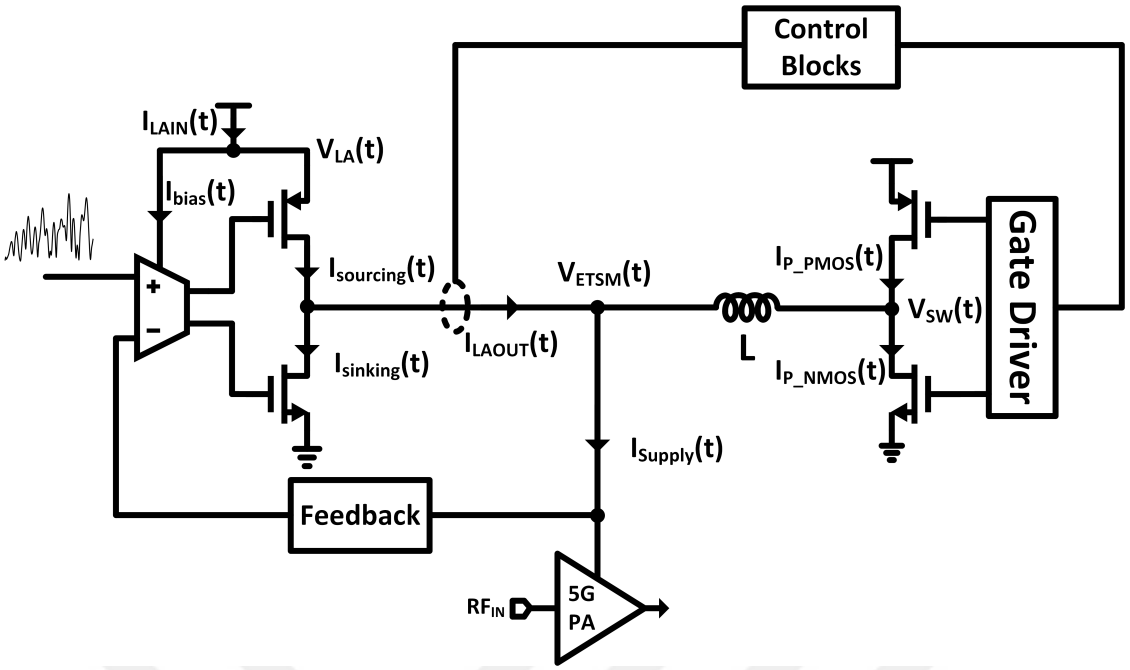

Figure 2.6 : Loss sources of hybrid supply modulator

the linear amplifier; switching and conduction losses of the buck converter; and power consumption of the control blocks [26,39].

The dynamic and static power consumptions of the linear amplifier can be shown as

$$P_{\text{sourcing}} = \frac{1}{T}\int_0^T (V_{LA}(t) - V_{ETSM}(t)) \cdot l_{\text{sourcing}}(t)dt \tag{2.6}$$

$$P_{\text{sinking}} = \frac{1}{T}\int_0^T V_{ETSM}(t) \cdot I_{\text{sinking}}(t)dt \tag{2.7}$$

$$P_{\text{bias}} = \frac{1}{T}\int_0^T V_{LA}(t) \cdot I_{\text{bias}}(t)dt \tag{2.8}$$

$I_{\text{sourcing}}(t)$ and $I_{\text{sinking}}(t)$ currents can be expressed in terms of the output current of the linear amplifier, $I_{\text{LAout}}(t)$, as

$$I_{\text{sourcing}}(t) = \frac{|I_{\text{LAout}}(t)| + I_{\text{LAout}}(t)}{2}, \quad I_{\text{sinking}}(t) = \frac{|I_{\text{LAout}}(t)| - I_{\text{LAout}}(t)}{2} \tag{2.9}$$

When a power MOSFET switch is turned on, the finite series resistance of the switch exhibits a power loss. This power loss can be reduced by increasing the width of the power transistor, but at the cost of increasing the switching power loss. The conduction power losses can be expressed as average current (I_{avg}) and duty cycle ratio (D) as [42]

$$P_{P_{PMOS}}(t) = \frac{1}{T}\int_0^T (V_{Buck} - V_{SW}(t)) \cdot I_{P_{PMOS}}(t)dt = I_{avg}^2 * R_{ONP} \cdot D \tag{2.10}$$

$$P_{P_{NMOS}}(t) = \frac{1}{T}\int_0^T V_{SW}(t) \cdot I_{P_{NMOS}}(t)dt = I_{avg}^2 * R_{ONN} \cdot (1-D) \tag{2.11}$$

where R_{ONN} and R_{ONP} are unwanted series resistances of the power MOSFET transistors.

When a transistor is switched, the parasitic capacitance of the power MOSFET devices must be charged or discharged. This dynamic charging and discharging mechanism creates a power loss, which can be expressed as

$$P_{SW} = V_{Buck}^2 \cdot f_{SW} \cdot C_p \tag{2.12}$$

where f_{sw} and C_p are the switching frequency and parasitic capacitance of the MOSFET device, respectively. The output power of the supply modulator can be expressed as

$$P_{ETSM}(t) = \frac{1}{T}\int_0^T V_{\text{ETSM}}(t) \cdot I_{Supply}(t)dt \tag{2.13}$$

where $V_{ETSM}(t)$ and $I_{Supply}(t)$ are the output voltage supply modulator and total added currents of both the linear amplifier and switching regulator, respectively.

The supply modulator's efficiency can be described as

$$\eta_{\text{ETSM}} = \frac{P_{\text{ETSM}}}{P_{\text{ETSM}} + P_{\text{sourcing}} + P_{\text{sinking}} + P_{\text{bias}} + P_{P_{\text{PMOS}}} + P_{P_{\text{NMOS}}} + P_{\text{Control}} + P_{\text{ETC}}} \cdot 100 \tag{2.14}$$

As can be seen from (2.14), efficiency can only be increased by reducing the power losses of the internal circuitry. Three-level converter topologies can be used to decrease the power losses of the power MOSFETs. Dynamic biasing and AC-coupled SM topologies also reduce the linear amplifier's power consumption [37].

3. AC-COUPLED HYBRID SUPPLY MODULATOR DESIGN

3.1 Introduction

As mentioned in Chapter 2, AC-coupled hybrid supply modulators are a proposed version of classical hybrid supply modulators. The primary distinction lies in the placement of a capacitor between the PA's supply and the linear amplifier's output, which serves the purpose of DC level shifting. The designed AC-Coupled ETSM for this thesis is depicted in Figure 3.1.

Internal feedback consists of two feedback loops. The slow feedback loop, which constantly monitors and stabilizes the offset voltage by adding a DC current offset to the linear amplifier's output current, controls the DC voltage of the coupling capacitor. The fast feedback loop operates as a current-controlled current source (CCCS) to supply the average current to the power amplifier. The linear amplifier in the global feedback acts as a voltage-controlled voltage source (VCVS) to set the output voltage related to the differential input envelope voltage. An internal variable capacitance bank is added to the supply modulator's output to change the load capacitance in active operation.

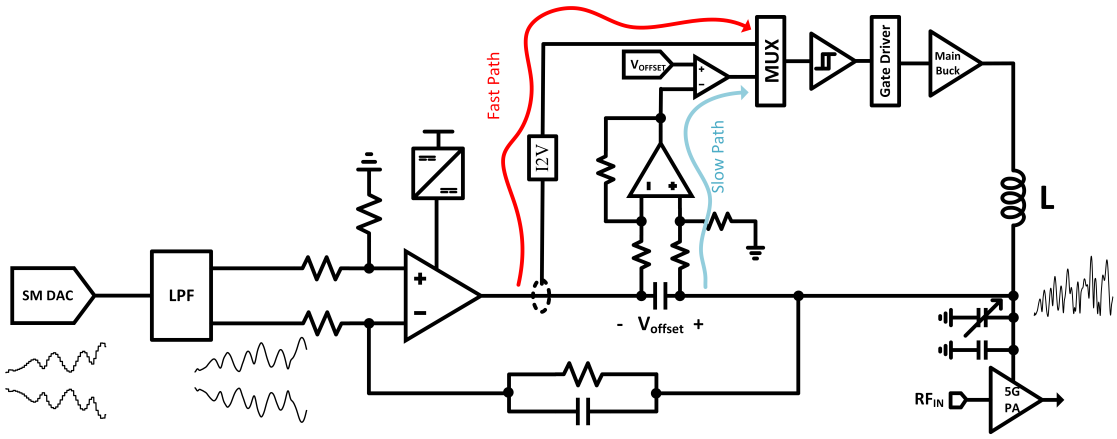

Figure 3.1 : The designed AC-coupled hybrid supply modulator

The system consists of many subblocks. The linear amplifier can be considered the most important block in the system. The linear amplifier should have sufficient loop bandwidth to not restrict the bandwidth of the envelope and create distortion. Also, the envelope amplifier must sink and source the current that is needed for the load. In addition, the envelope amplifier must be stable over a vast range of load variations. These attributes make the design of the linear amplifier challenging, and several works have been done to improve the efficiency, bandwidth, and current handling capacity of the linear amplifier [25,28,35].

3.2 Proposed Linear Amplifier

3.2.1 Core design

The schematic of the proposed linear amplifier can be seen in Figure 3.2. The first stage of the linear amplifier is designed as operational transconductance amplifier (OTA). M_3, M_4 cascode transistors are implemented to protect M_1 and M_2 input differential pair transistors from overvoltage. The M_7 and M_8 diode-connected transistors create a level-shifting voltage for cascode transistors. The driver stage is designed as Class AB to drive the heavy load rail-to-rail without increasing the quiescent current of the linear amplifier.

Conventional linear amplifier topologies use regular voltage transistors at the output stage of the linear amplifier. To decrease parasitic capacitances and improve the bandwidth of the linear amplifier, the M_{18} and M_{24} transistors are implemented with low-voltage transistors that have lower length values. However, low-voltage transistors are more suspectable to voltage breakdown than regular transistors. So, a protection circuitry must be embedded in the linear amplifier to prevent drain-source breakdown.

In Figure 3.2, red lines denote the proposed protection circuit. M_{19} and M_{26} transistors form a protection mechanism that prevents the drain to source voltages of both M_{18} and M_{24} transistors from exceeding beyond breakdown voltage. This structure is very similar to the gain-boosted amplifier with a common-source stage, which is used to increase the DC gain of operational amplifiers [43]. The only difference is that the

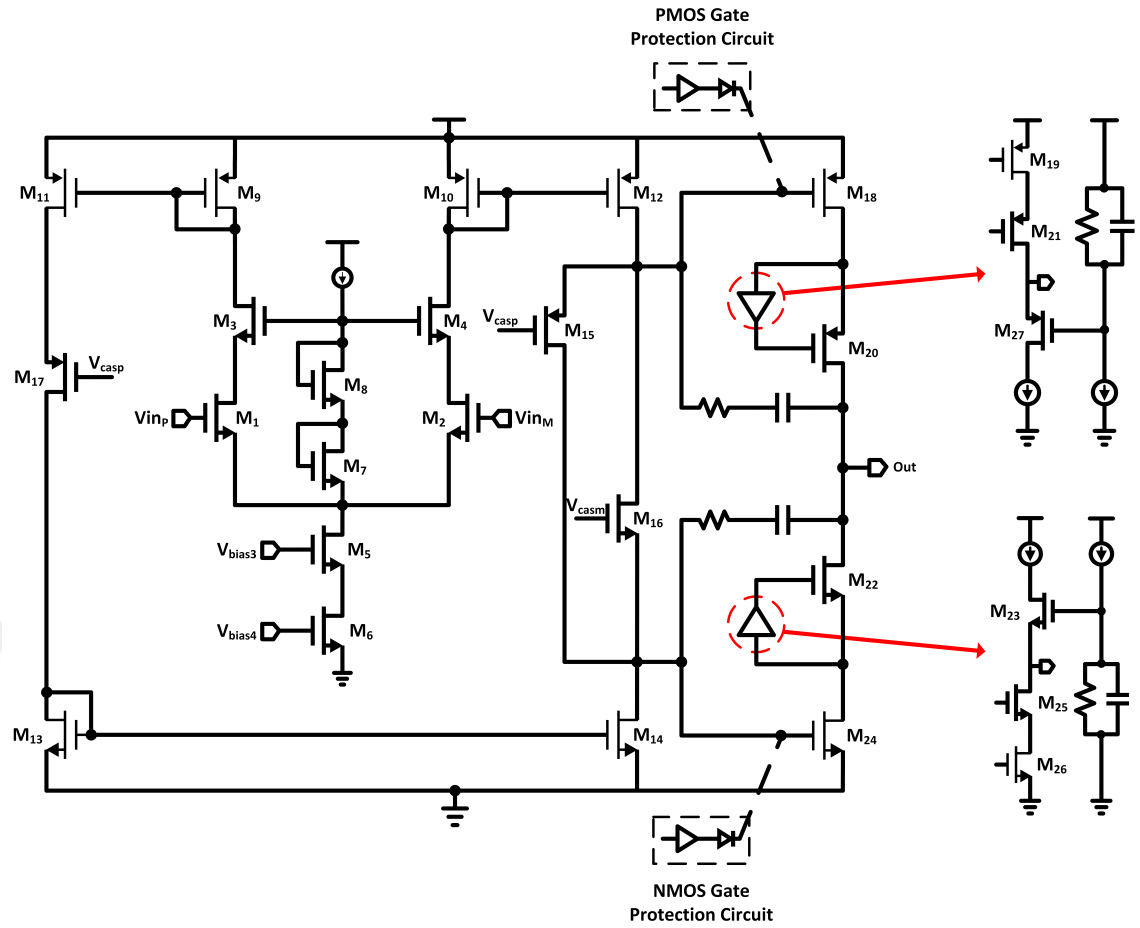

Figure 3.2 : The proposed linear amplifier

M_{23} and M_{27} transistors act as clamps that prevent the gate-source breakdown of the M_{20} and M_{23} transistors. The clamp voltages are set by precise voltage references.

To bias the M_{18} and M_{24} transistors, M_{15} and M_{16} laterally diffused metal-oxide-semiconductor (LDMOS) transistors are used to create a floating voltage source [44]. This biasing structure is also called trans-linear loop and provides a supply voltage-independent quiescent current [45]. The V_{casp} and V_{casn} biasing voltages are also applied to M_{17}, M_{21}, and M_{25} transistors to protect M_{11}, M_{19}, and M_{26} low-voltage transistors.

NMOS gate protection and PMOS gate protection circuits are embedded in linear amplifier to prevent the gate-source voltages of the low-voltage transistor from exceeding beyond the breakdown region.

3.2.2 The current-sensing circuit

A current-sensing circuit is needed to precisely control the internal feedback loop of the hybrid supply modulator. The current sensing methods are shown in Figure 3.3. The simplest method is to use a resistor connected between the linear amplifier's output and the supply of the PA, as shown in Figure 3.3(a). Although this method is very effective and simple, power consumption can be significantly high, even for low power applications.

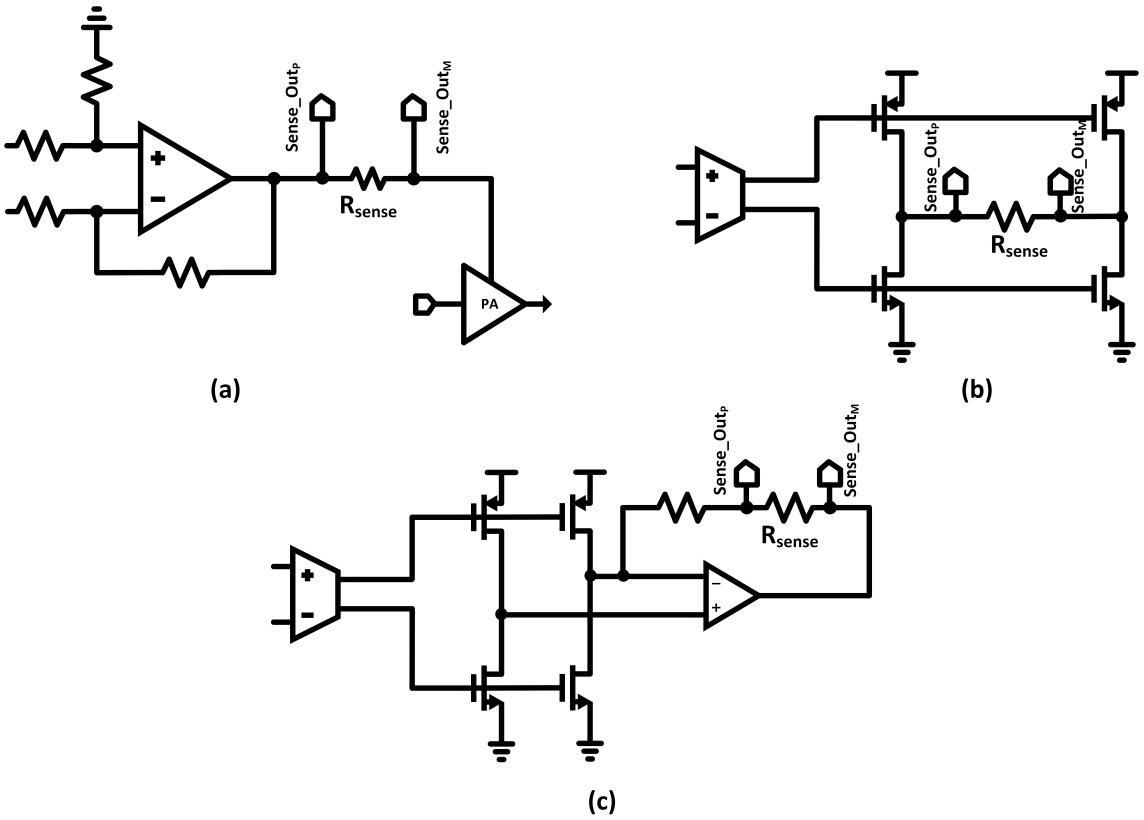

Figure 3.3 : The current sensing circuit types

A more advanced method is to use a replica branch to generate sensing voltage, as shown in Figure 3.3(b) [27]. While this method solves the power consumption problem, the nonlinear effects can be significantly higher for linear sensing.

As shown in Figure 3.3(c), using a replica branch with an opamp in feedback solves both problems in previous cases [3]. The opamp senses the linear amplifier's output

and creates a current that flows through the replica branch. The resistor in the feedback path can be used as a current-sensing circuit. The drawback of this approach is that the opamp must have rail-to-rail input and output and must be fast enough to track the linear amplifier's output.

In this thesis, the last method is used to implement a current-sensing circuit. The schematic diagram of the sensing circuit is depicted in Figure 3.4. The replica current is nth times-divided by the linear amplifier's output current for reducing power consumption. The differentially sensed voltage is converted to single-ended voltage to be processed by the hysteretic control loop.

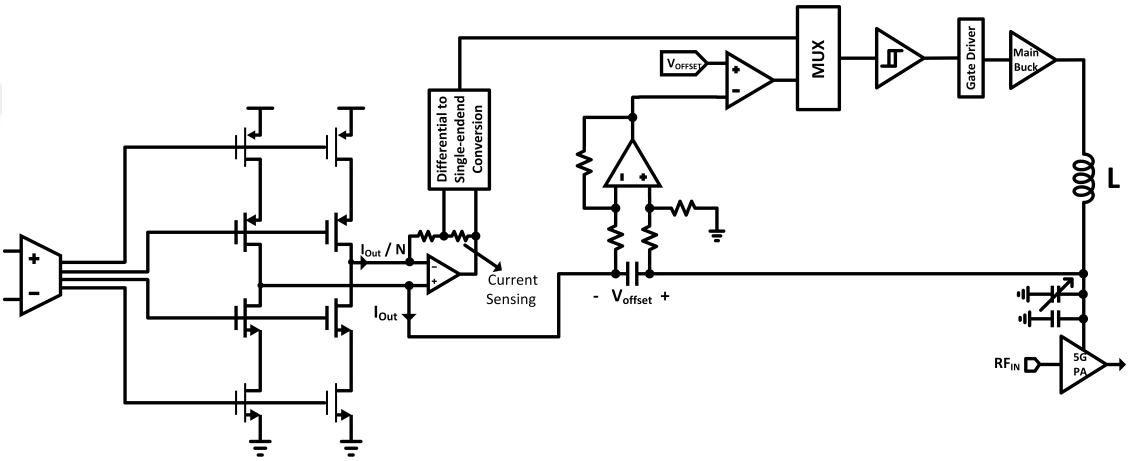

Figure 3.4 : The schematic diagram of the current sensing circuit

3.2.3 The layout of the linear amplifier

The layout of the linear amplifier is illustrated in Figure 3.5. The output transistors are positioned at the top of the layout, as shown in the figure. The sensing transistors are placed in the center of the output transistors to increase the matching. Common-centroid and interdigitation techniques are applied to the circuit blocks that need to be matched.

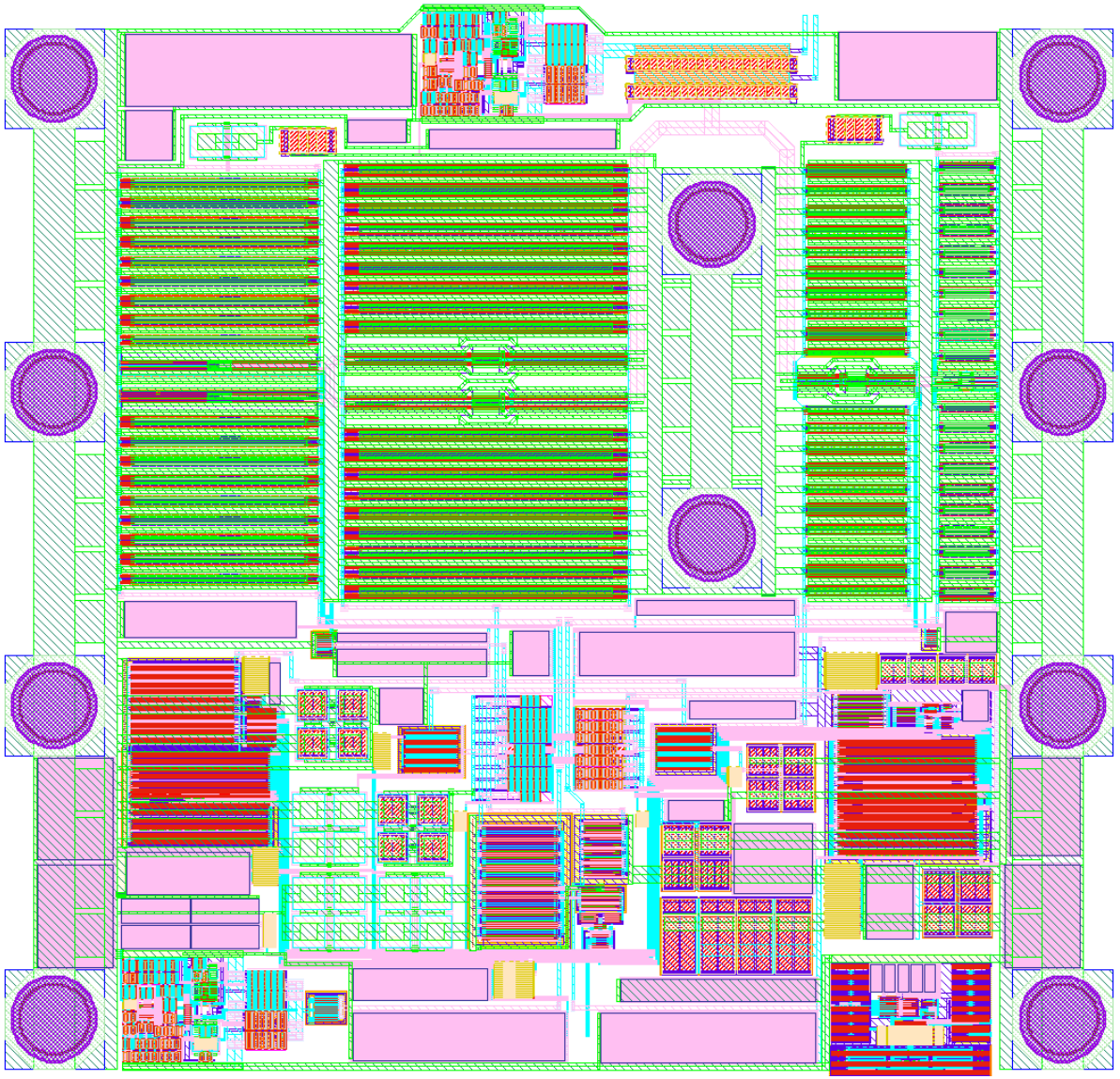

Figure 3.5 : The layout of the linear amplifier

3.3 Hysteretic Comparator

A comparator circuit is one of the most fundamental building blocks of today's microelectronics. An analog comparator compares two analog signals with each other and generates a digital output based on the difference. In hysteretic supply modulators, a hysteretic comparator is generally used in the internal feedback system. A hysteresis can be defined as the change in the comparator threshold value depending on the state of the comparator's output. [46]. A transfer curve of a typical hysteresis graph is given in Figure 3.6.

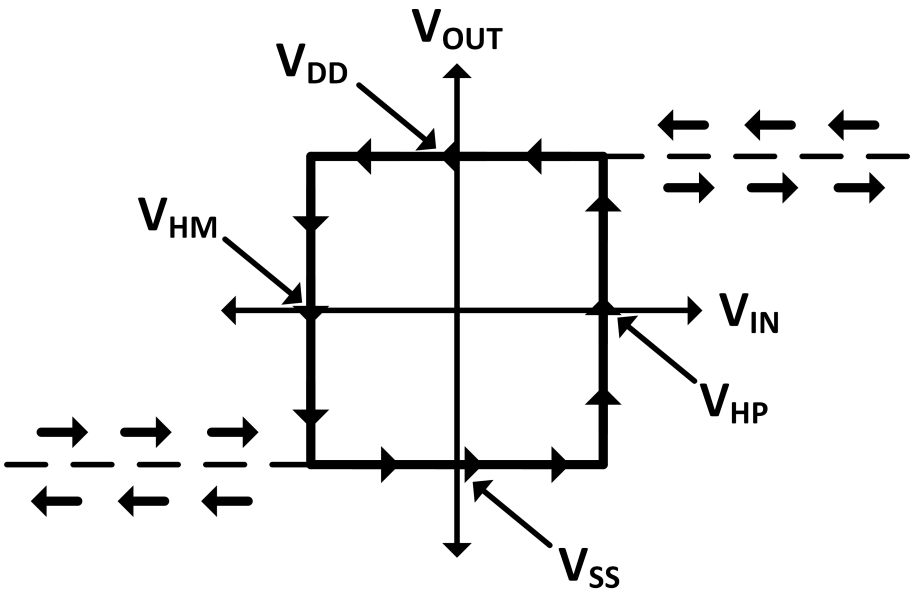

Figure 3.6 : The typical diagram of the hysteresis

The hysteretic comparator that is used in this work is shown in Figure 3.7. Internal positive feedback, which is the result of M_5 and M_6 transistors creating a positive feedback loop, creates the hysteresis. If the transconductance values of the M_4 and M_7 transistors exceed those of the M_5 and M_6 transistors, hysteresis cannot be formed. To increase the voltage swing and gain of the hysteretic comparator, a Class AB-type output driver is embedded in the hysteretic comparator. The hysteretic comparator layout is given in Figure 3.8.

3.4 Hysteretic Current Mode Buck Converter

3.4.1 Overview

DC-DC converters are popular choices in mobile systems where power conversion must be handled with high efficiency [47]. Most modern ETSM systems use DC-DC converters to dynamically control the supply of linear amplifiers because they maintain high efficiency values for large load variations.

The most commonly used control strategies for pulse-width modulator (PWM) DC-DC converters can be classified into three different categories: voltage-mode control (VMC), current-mode control (CMC), and hysteretic control. A representation of these control strategies is given in Figure 3.9.

VMC DC-DC converters fundamentally consist of an error amplifier, a ramp voltage generator, a comparator, and a power stage to perform the conversion. The error amplifier serves the purpose of amplifying the error voltage, which is defined as the difference between the output of the DC-DC converter and the reference signal.

VMC converters usually have very complex compensation schemes that increase the design time. The ramp generator is used to generate a PWM signal to vary the duty cycle (D) to control the power stage. While VMC DC-DC converters have excellent properties of predictable EMI and good dynamic line response, the increased complexity of the compensation scheme and the high quiescent current demand of

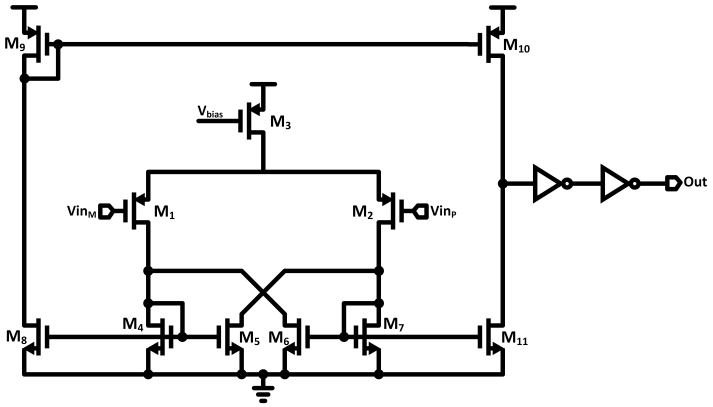

Figure 3.7 : The schematic diagram of the hysteretic comparator

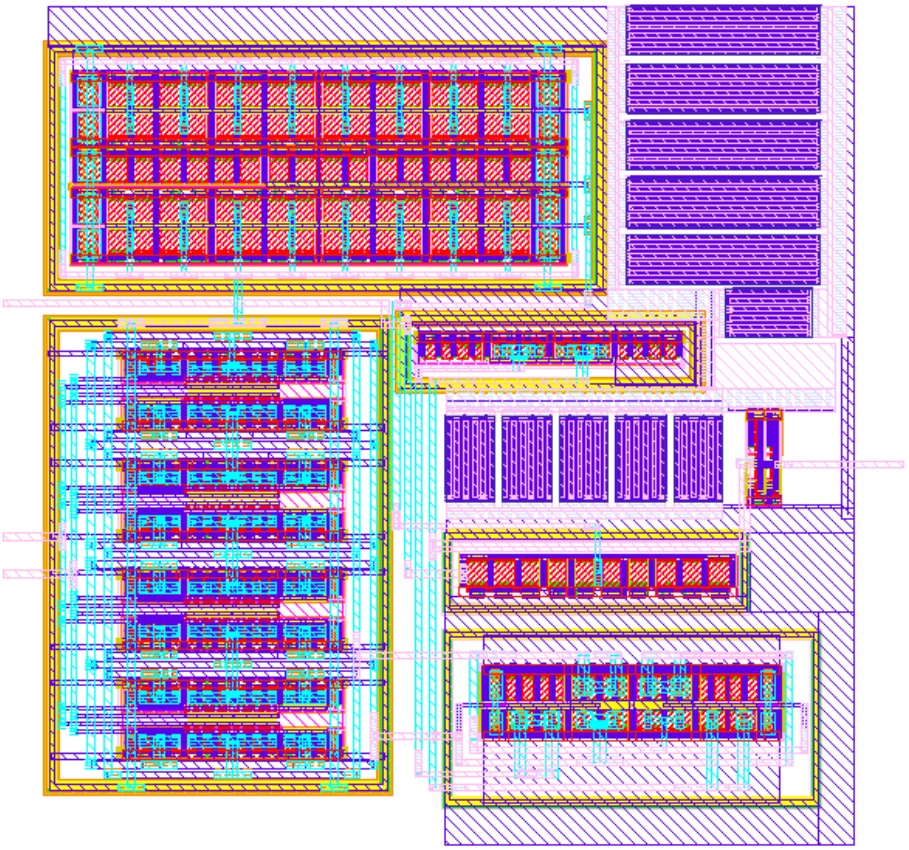

Figure 3.8 : The layout of the hysteretic comparator

internal blocks reduce the practical applications of VMC DC-DC converters. The functional block diagram of the VMC can be seen in Figure 3.9(a).

CMC DC-DC converters are very similar to the VMC, with the difference that the ramp signal is generated from the inductor current. Controlling the internal loop with the inductor current reduces the transfer function of the control system into a single-pole loop, which reduces the compensation complexity far more than the VMC converters. However, CMC DC-DC converters have a very serious problem known as subharmonic oscillation in continuous conduction mode (CCM) for duty-cycle values that are greater than 0.5. A compensation ramp might be added to the feedback system to solve this problem, but introducing a ramp compensation makes the control scheme closer to the VMC [48,49]. The functional block diagram of the CCM is depicted in Figure 3.9(b).

The hysteretic (bang-bang) DC-DC converters are one of the oldest known converter topologies in the literature. The simple nature, lack of compensation, and high loop bandwidth properties make this converter topology an excellent choice for

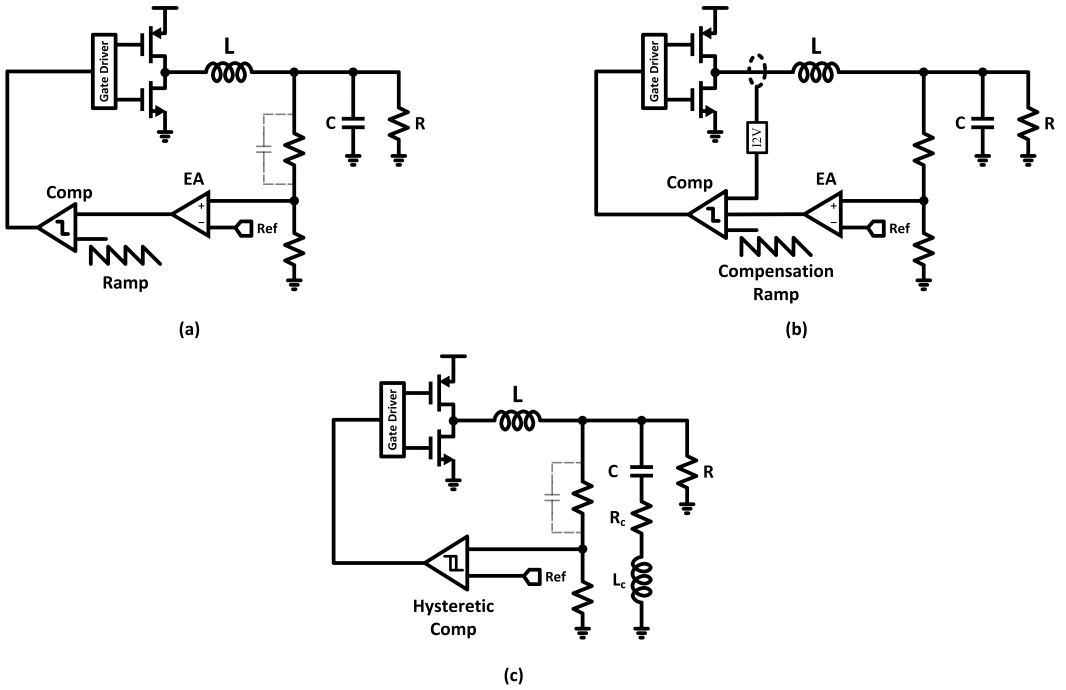

Figure 3.9 : The control strategies of DC-DC converters

state-of-the-art, highly efficient supply modulator systems. However, the non-constant switching frequency and high sensitivity to the off-chip components increase the unpredictability of the hysteretic DC-DC converters. Fortunately, several works have been done to reduce the unpredictability of the hysteretic DC-DC converter by applying constant ON-time, constant OFF-time, and artificial ramp generation [49,50].

3.4.2 Core design

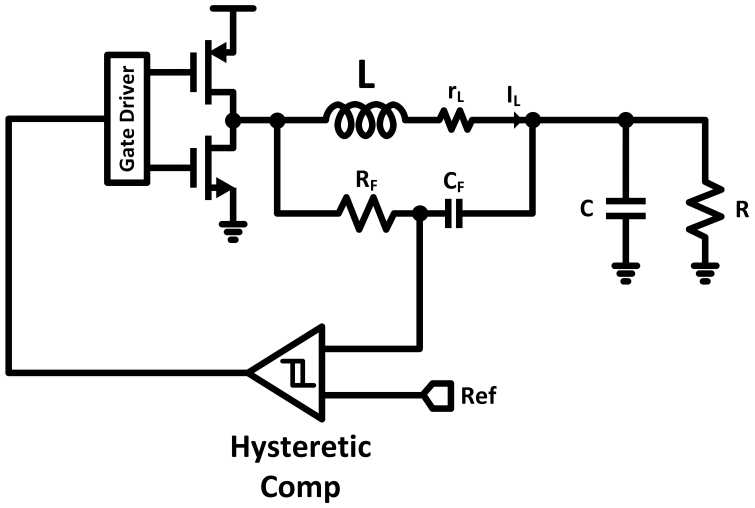

Figure 3.10 : The schematic of the hysteretic current-mode buck converter

A current-mode hysteretic DC-DC converter is designed in this work to produce a dynamic supply voltage to the linear amplifier. A conventional schematic diagram of the hysteretic buck converter is shown in Figure 3.10. The feedback signal is generated from the inductor current via the passive Filter-sense method [51]. As indicated in Figure 3.11, the passive Filter-sense method is one of the simplest and most efficient methods for measuring the inductor current with high efficiency and low complexity. For proper sensing, the passive component values should be chosen as follows:

$$\frac{L}{r_L} = C_F \cdot R_F = T_C, \quad I_L \cdot r_L = V_{CF} \tag{3.1}$$

As shown in (3.1), the voltage difference across the capacitor becomes the same as the voltage across the parasitic resistance of the inductor if the time constants of the inductor's parasitic resistance and inductor match C_F*R_F.

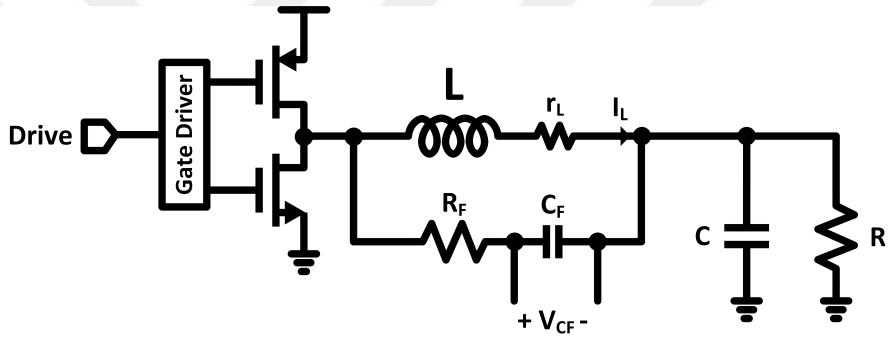

Figure 3.11 : The Filter-sense method to measure the inductor current

Similar to conventional supply modulator architectures, the hysteretic buck converter in Figure 3.10 operates in a self-oscillation condition. The switching frequency is heavily dependent on the hysteresis windows V_H, V_{VDD}, and V_{out}, which can be expressed as [52]

$$f_{sw} = \frac{1}{\frac{T_C \cdot V_H}{V_{DD} - V_{\text{out}}} + \frac{T_C \cdot V_H}{V_{\text{out}}}} = \frac{(V_{DD} - V_{out}) \cdot V_{out}}{V_{DD} \cdot V_H \cdot T_C} \tag{3.2}$$

The schematic diagram of the designed buck converter is depicted in Figure 3.12. The current of the inductor is sensed and injected into the resistive feedback node to reduce the sensitivity of the buck converter to PCB parasitics. A feed-forward capacitor is added to the feedback node to improve the transistor response of the buck converter [49]. The hysteresis range and DC output voltage are dynamically controlled with

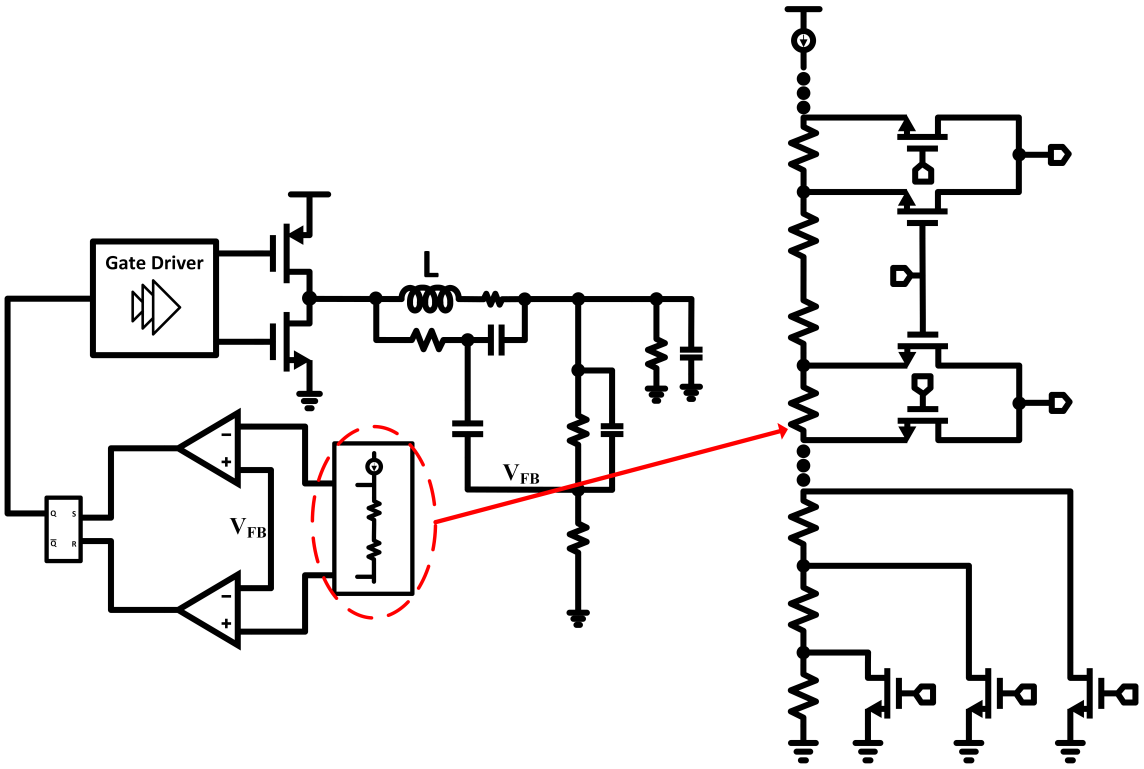

Figure 3.12 : The designed hysteretic current mode buck converter

an embedded DAC. A ZCD circuit is embedded in the gate driver to prevent reverse inductor current.

The gate-driver schematic is shown in Figure 3.13. The circuit in [53] is adopted to create dead-time in driving signals to prevent short-circuit conduction and reduce power consumption. Since it is intended that the overall design must operate at voltage levels that are higher than the gate-source breakdown voltage of the transistors, low-voltage to high-voltage (L2H) and high-voltage to low-voltage (H2L) level shifters are embedded in the buck converter. The control signal is provided by the ZCD circuit. Cascaded drivers are placed at the output to reduce the delay time of the power MOSFET gate drivers.

The detailed schematic diagram and layout of the proposed zero-current detector can be seen in Figures 3.14 and 3.15, respectively. The work in [54] is improved to relax the input common-mode range requirements of the comparators. The Schmitt trigger and delay cell are used to buffer the driver signal to prevent glitches. Since the supply voltage of the buck converter is beyond the safe operating area (SOA) limits of the

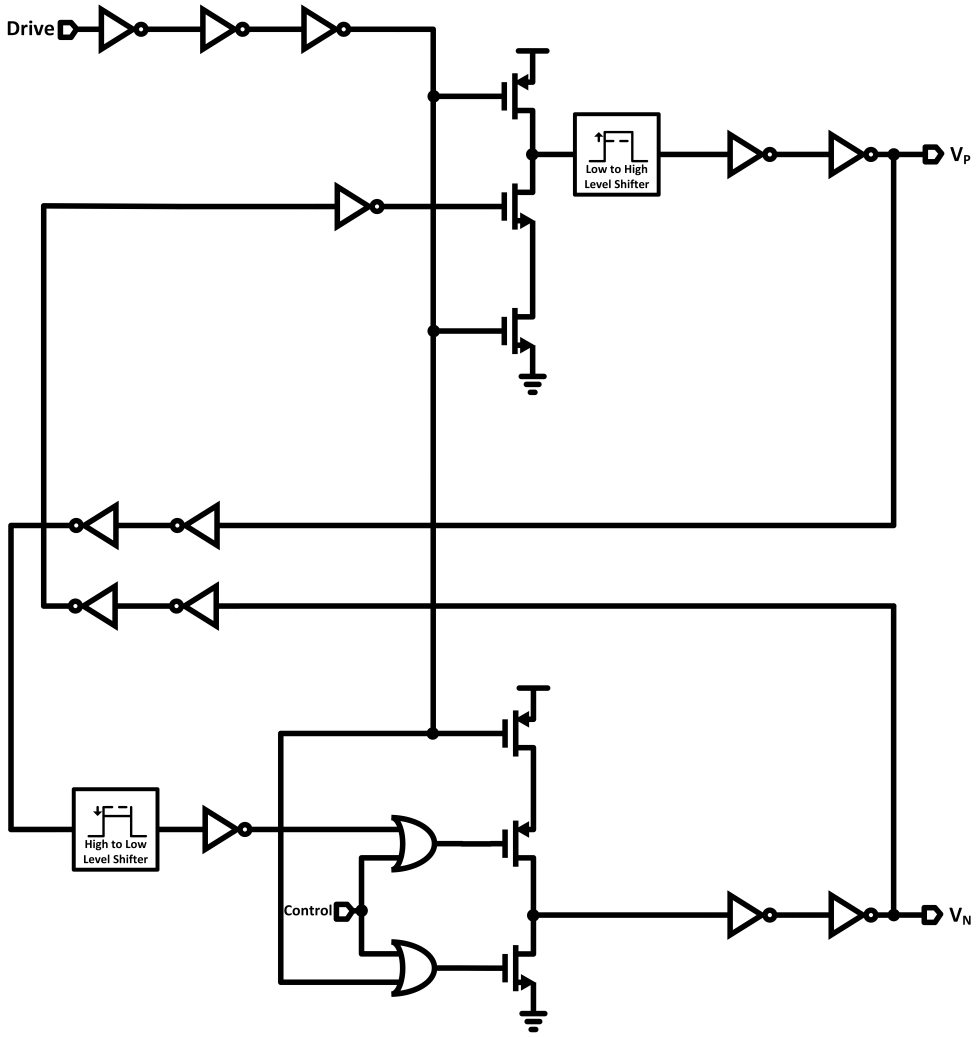

Figure 3.13 : The gate-driver circuit

transistors, the switching node of the buck converter cannot be applied directly to the comparator inputs. To overcome this, the M_1 LDMOS transistor is used as a buffer to isolate the switching node from the input transistors.

R_1-R_5 resistors are used to create a DC offset voltage to increase the common-mode voltage of the comparator. The drawback of this approach is that when the M_1 transistor is turned on, the voltage levels of the comparator inputs are usually very close to each other, and slow settling of the "Comp In_p" node can cause a wrong decision. This turns off the NMOS power transistor, and all the high current must flow through the parasitic diode of the power transistor, which lowers the efficiency. So, in the proposed version, the M_2 transistor is placed to create a DC offset to remove the potential glitches.

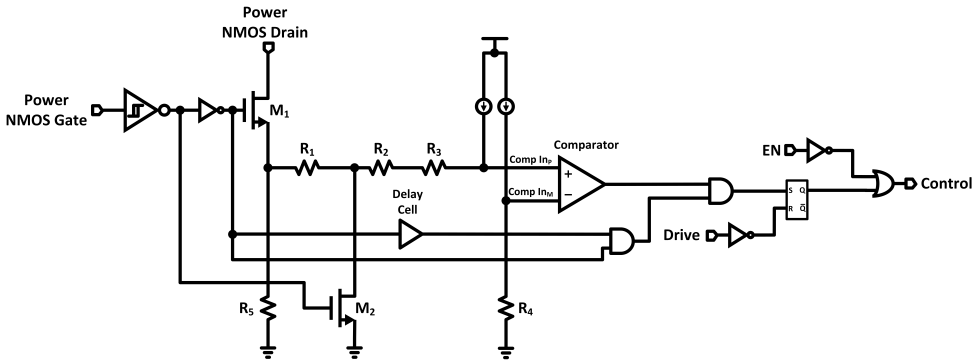

Figure 3.14 : The proposed ZCD circuit

The schematics of the level shifter circuits are shown in Figure 3.16. To drive the PMOS power transistors, a level conversion must be handled from V_{DD}-0 to $2{\cdot}V_{DD}$ -V_{DD}. Since the gate-driver circuit has a feedback mechanism that requires the state of the gate voltage of the PMOS power transistor, a level shift is also needed from $2{\cdot}V_{DD}$-V_{DD} to V_{DD}-0. The layouts of the L2H and H2L circuits are given in Figures 3.17 and 3.18, respectively.

The L2H level shifter can be seen in Figure 3.16(a). M_1-M_2 transistors use LDMOS structure. The design is very similar to the conventional level shifter circuit, with the difference of M_3-M_4 transistors. M_3-M_4 transistors are biased with internal

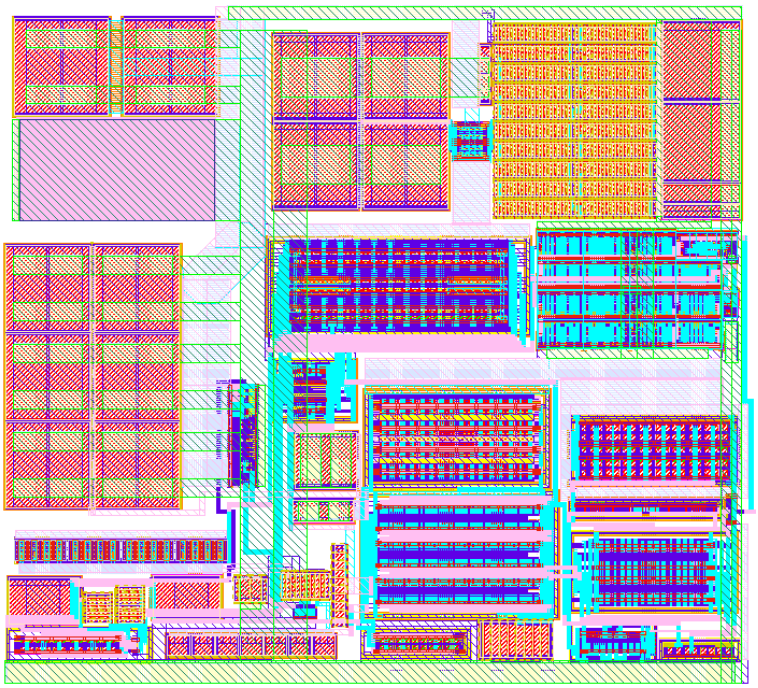

Figure 3.15 : The layout of the proposed zero-current detector

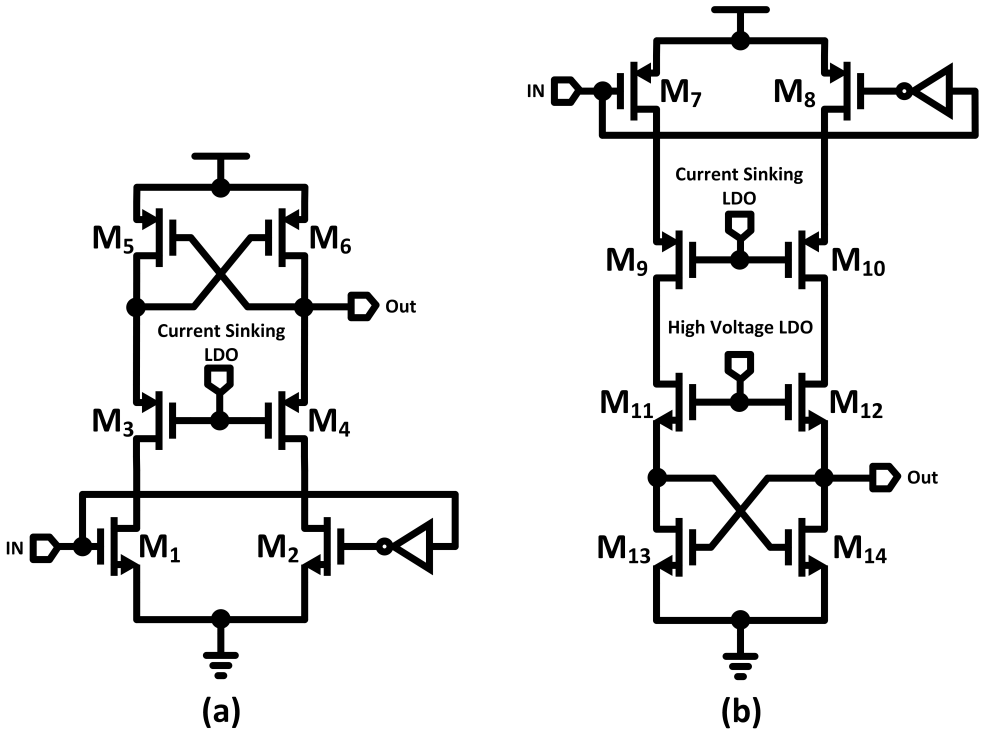

Figure 3.16 : The level-shifter circuits

current-sinking LDO to protect M_5-M_6 transistors from overvoltage stress. The H2L level shifter circuit can be seen in Figure 3.16(b). The circuit is an inverted form of the L2H level shifting circuit. Similar to the L2H circuit, M_9-M_{12} are biased with internal LDOs to protect M_7-M_8 and M_{13}-M_{14} transistors from overvoltage stress.

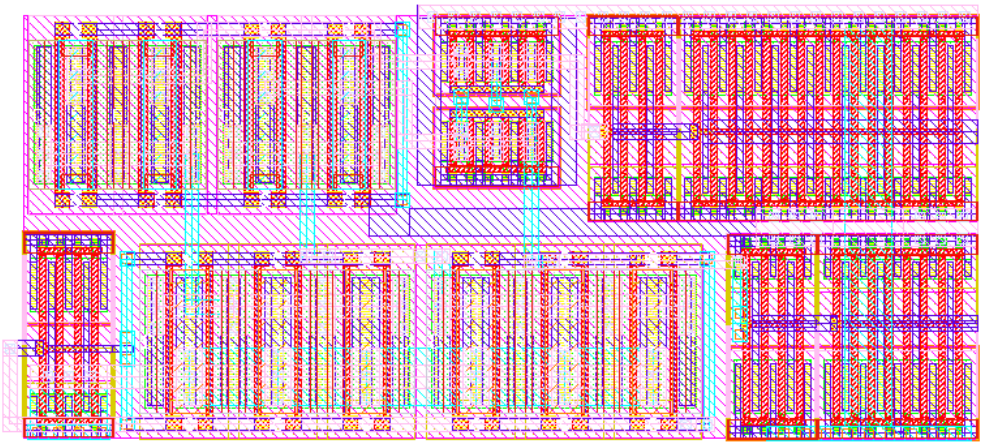

Figure 3.17 : The layout of the L2H level shifter

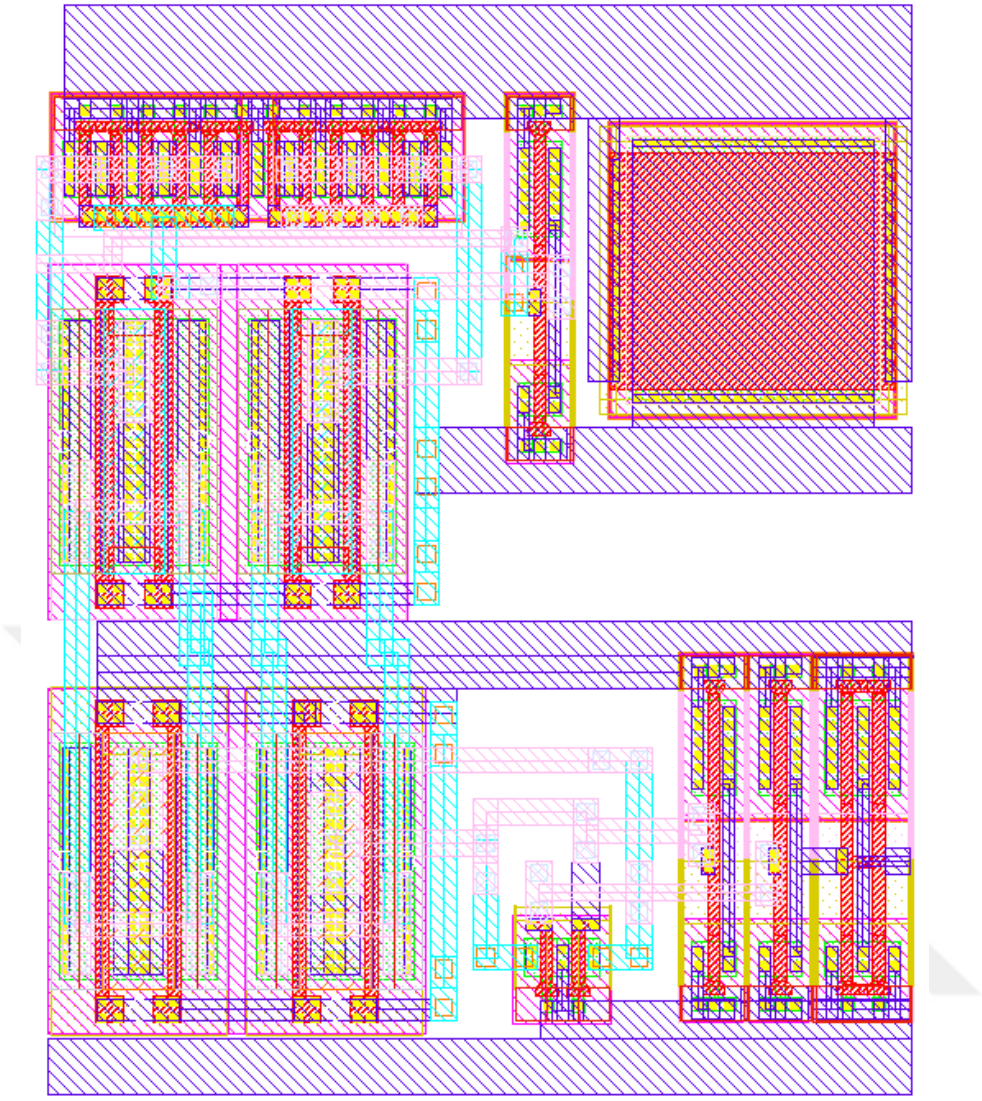

Figure 3.18 : The layout of the H2L level shifter

3.4.3 Hysteretic buck converter layout

The hysteretic current-mode buck converter layout is shown in Figure 3.19. The gate-driver circuit is placed between the NMOS and PMOS power transistors to match the delay of the driver signals. The ZCD circuit is placed at the top of the switching node to reduce the delay and patch inductance to remove glitches. The sensitive analog circuits are placed close to the ground pad to increase isolation and remove switching noise. The decoupling capacitors are added near the power lines to reduce the switching noise. The area of the hysteretic buck converter is 0.511 mm^2.

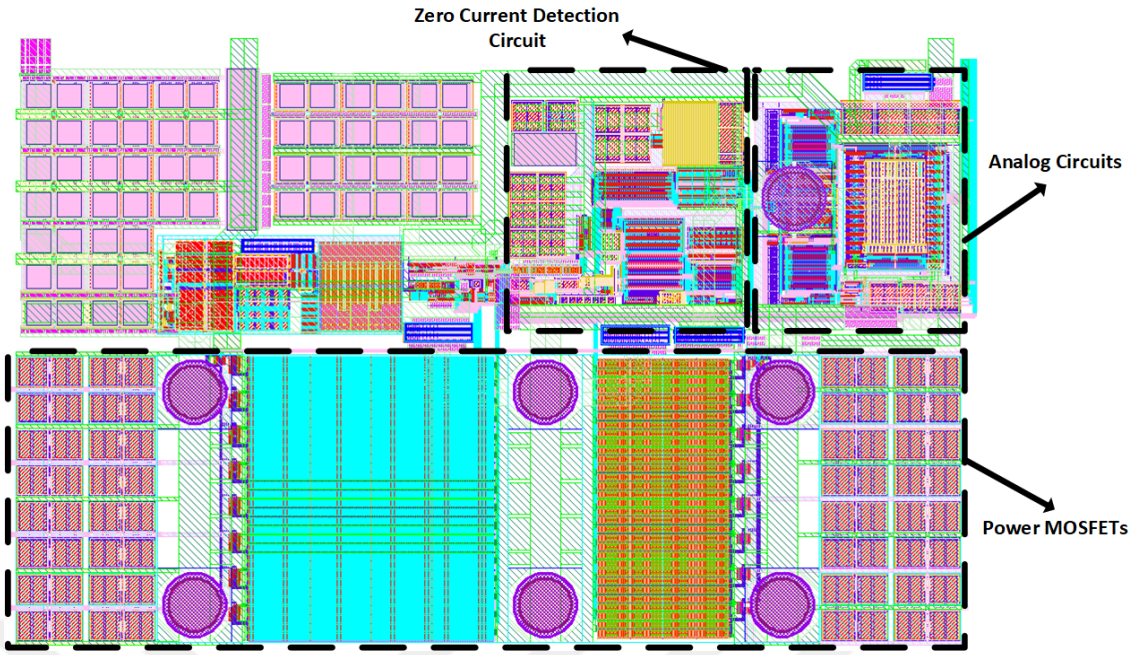

Figure 3.19 : The hysteretic converter layout

3.5 LDOs

Nearly all on-chip analog circuits require a stable voltage to operate properly. A LDO circuit produces an output voltage with minimal noise and ripple by using a highly accurate voltage reference. A conventional LDO regulation loop consists of an error amplifier, a feedback network, and a pass transistor. The error amplifier is used to amplify the error between the output voltage and the reference voltage. The feedback network consists of a resistor divider for simplicity. A feedforward capacitor is usually added to the feedback network to increase the stability and enhance the transient response of the LDO. A pass transistor is used to source current to the load or sink current from the load for regulation [55]. The conventional block diagrams of LDOs are shown in Figure 3.20.

The feedback loop's stability is a major concern in designing a LDO. Since the LDO must cover a wide range of load current and output capacitance variations, the design space grows exponentially. The LDO in Figure 3.20(a) has a low output impedance thanks to the NMOS pass transistor, so the output pole of the error amplifier can be used as the dominant pole. However, the LDO's output in Figure 3.20(b) is a high-impedance node. So, the output of the LDO can be the dominant pole in the

presence of an external output capacitor. In capless LDOs, where capacitances for LDO outputs are provided on-chip, no off-chip components are used. Thus, Miller compensation can be applied to the circuit in Figure 3.20(b). The disadvantage of this approach is that output regulation becomes challenging for a specific frequency range because the LDO's output impedance typically peaks between 1 MHz and 10 MHz.

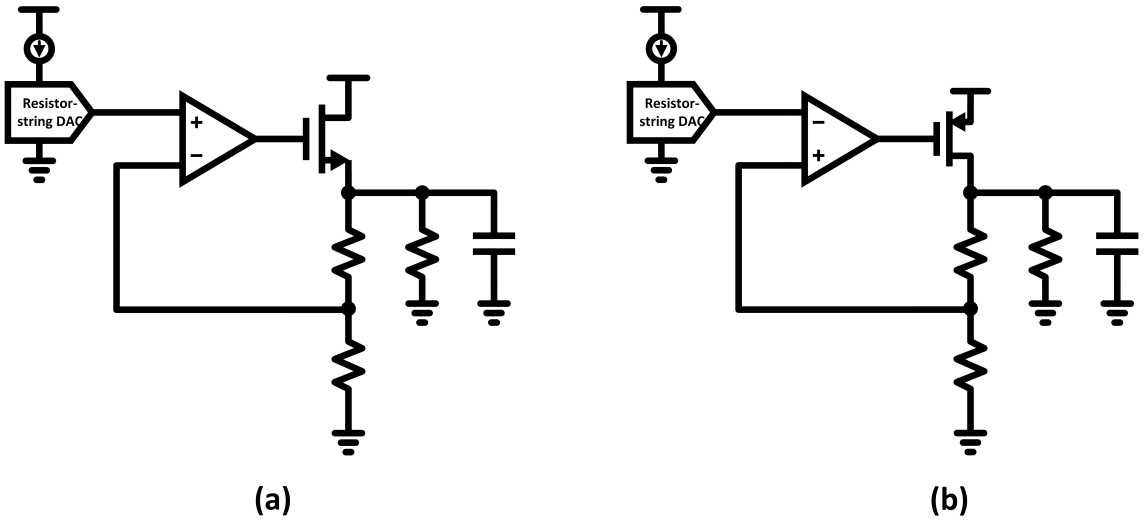

Figure 3.20 : The circuit diagrams of the LDO types

3.5.1 Primary high voltage/Auxiliary LDO

The designed high-voltage LDO can be seen in Figure 3.21. The system is very similar to the LDO topology in Figure 3.20(b). The high voltage opamp is designed with an internal protection circuit to prevent overvoltage breakdown. The voltage reference is supplied to the LDO by a high-precision internal resistive-DAC circuit. C_1 feedforward capacitor is added to the feedback network to improve stability and transient response. R_5 and C_2 components are added to create the miller compensation.

According to Figure 3.21, the internal bandgap reference (BGR) circuit supplies the current reference that creates the voltage reference for the LDO. Since the supply voltage of the BGR is dependent on the LDO and the current reference of the LDO is dependent on the BGR, a chicken-and-egg situation arises. To solve this, an auxiliary LDO is embedded in LDO core to wake up the BGR circuit at start-up [55]. A programmability is added to the R_4 resistor to cover the different supply voltage levels.

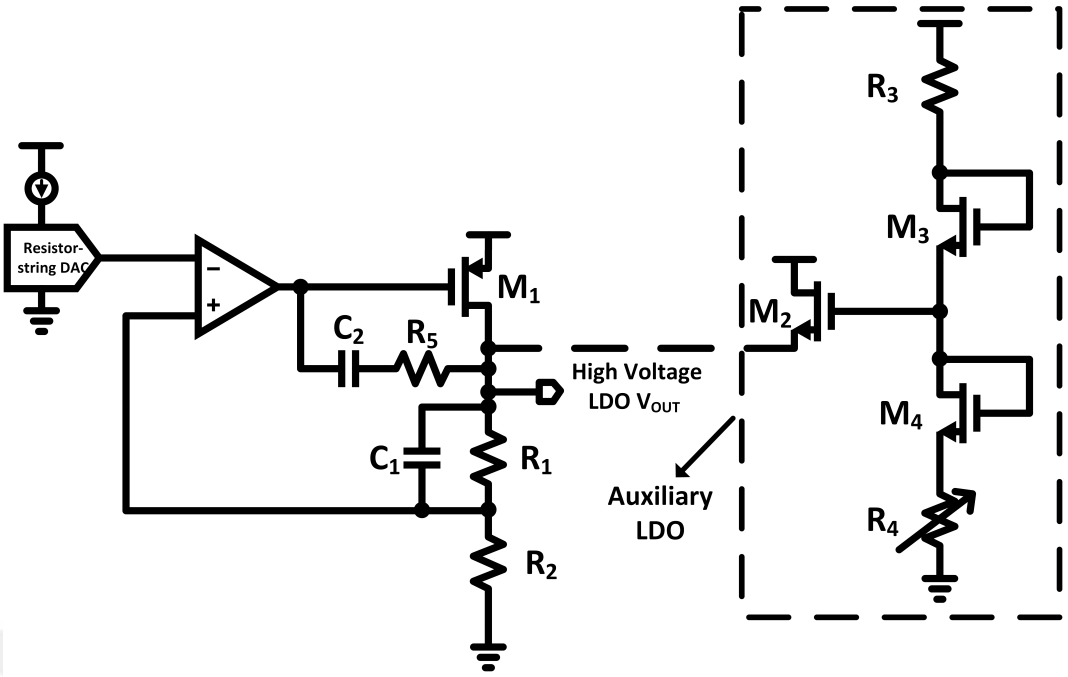

Figure 3.21 : The schematic diagram of the high voltage LDO

The layouts of the high voltage and auxiliary LDOs are given in Figure 3.22 and 3.23, respectively.

3.5.2 Current sinking LDO

The power PMOS transistor in the buck converter operates at $2 \cdot V_{DD}$ voltage, so the L2H and H2L level shifters are designed to convert the voltage levels of the driver signal to different voltage domains. The level shifted driver signals are buffered with cascaded inverters that operates between the $2 \cdot V_{DD}$ and V_{DD} voltage levels. Therefore,

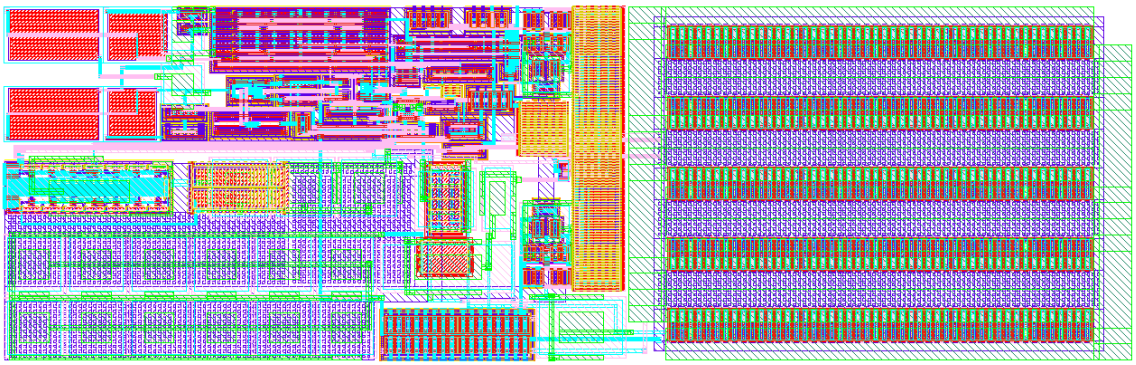

Figure 3.22 : The layout of the high voltage LDO

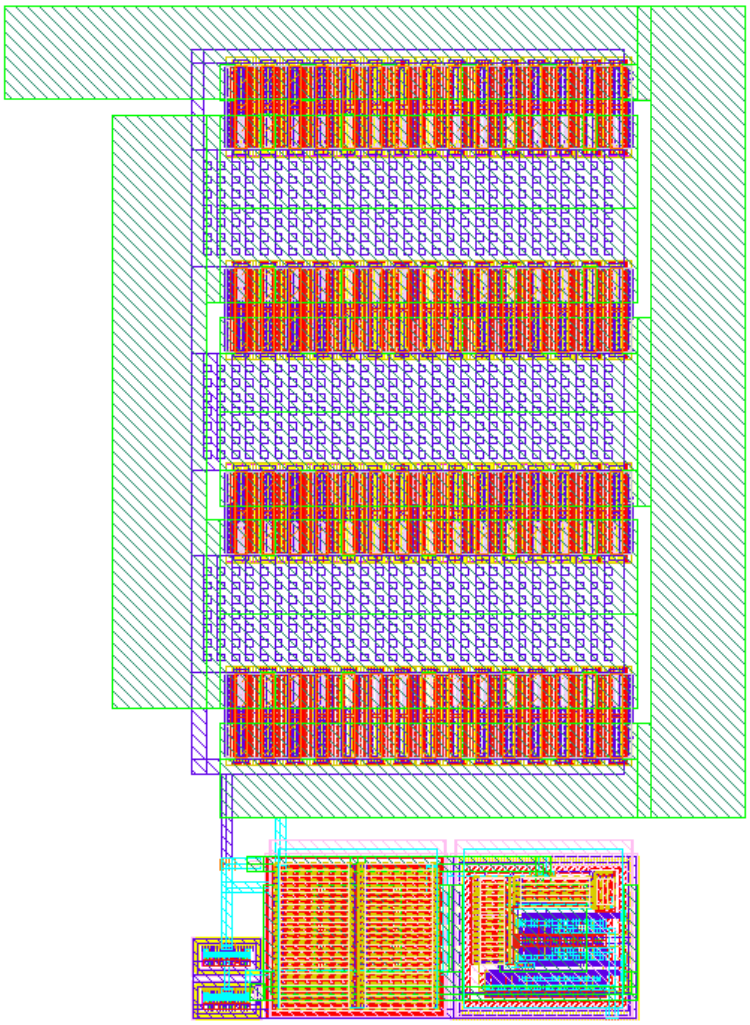

Figure 3.23 : The layout of the auxiliary LDO

the current that flows through the V_{DD} pins of these inverters must flow to a block that is capable of sinking the incoming currents.

The schematic of the designed current-sinking LDO is shown in Figure 3.24. The M_1 pass transistor is implemented with an LDMOS transistor to handle the overvoltage. Similar to high-voltage LDO, C_1 and R_1 components are used to create the Miller effect. Since the output pole of the circuit is heavily dependent on the R_2 resistor, the minimum value must be chosen carefully to satisfy the stability requirements. The resistor DAC is designed to always maintain V_{DDsink} - 2.5 V voltage at the output of the current sinking LDO. The layout of the current sinking LDO can be seen in Figure 3.25.

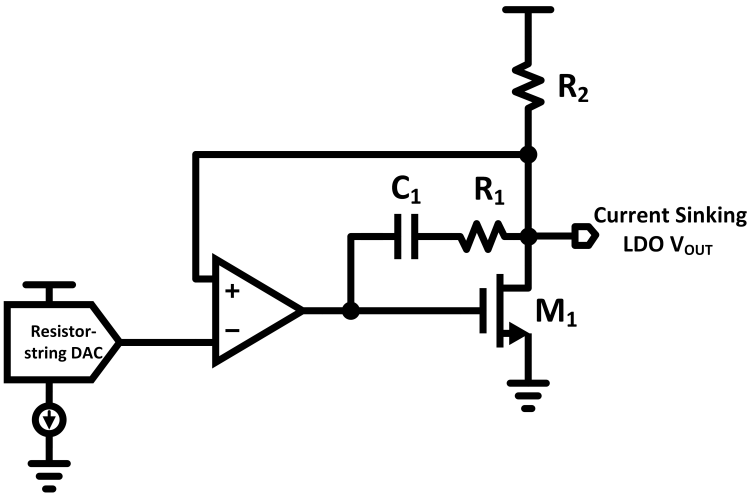

Figure 3.24 : The schematic diagram of the current-sinking LDO

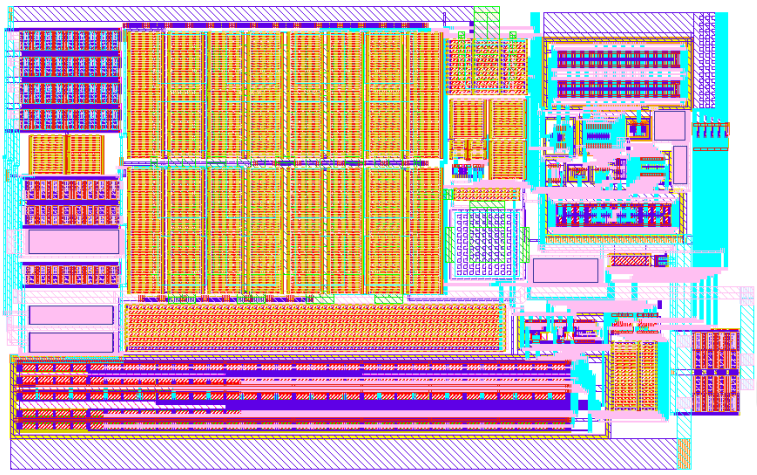

Figure 3.25 : The layout of the current-sinking LDO

3.6 Layout of the supply modulator

The layout of the supply modulator is given in Figure 3.26. The hysteretic buck converter is positioned at the bottom of the supply modulator. The linear amplifier is placed in the center of the modulator to shorten the internal feedback loops' sensing path. The switching amplifier is placed at the top of the layout. The decoupling capacitors are placed close to the switching amplifier to reduce the glitch in the sensitive analog signals. The sensitive analog circuits are placed between the linear amplifier and switching amplifier to make the loop signals as short as possible. The total area of the supply modulator is 3.051 mm^2.

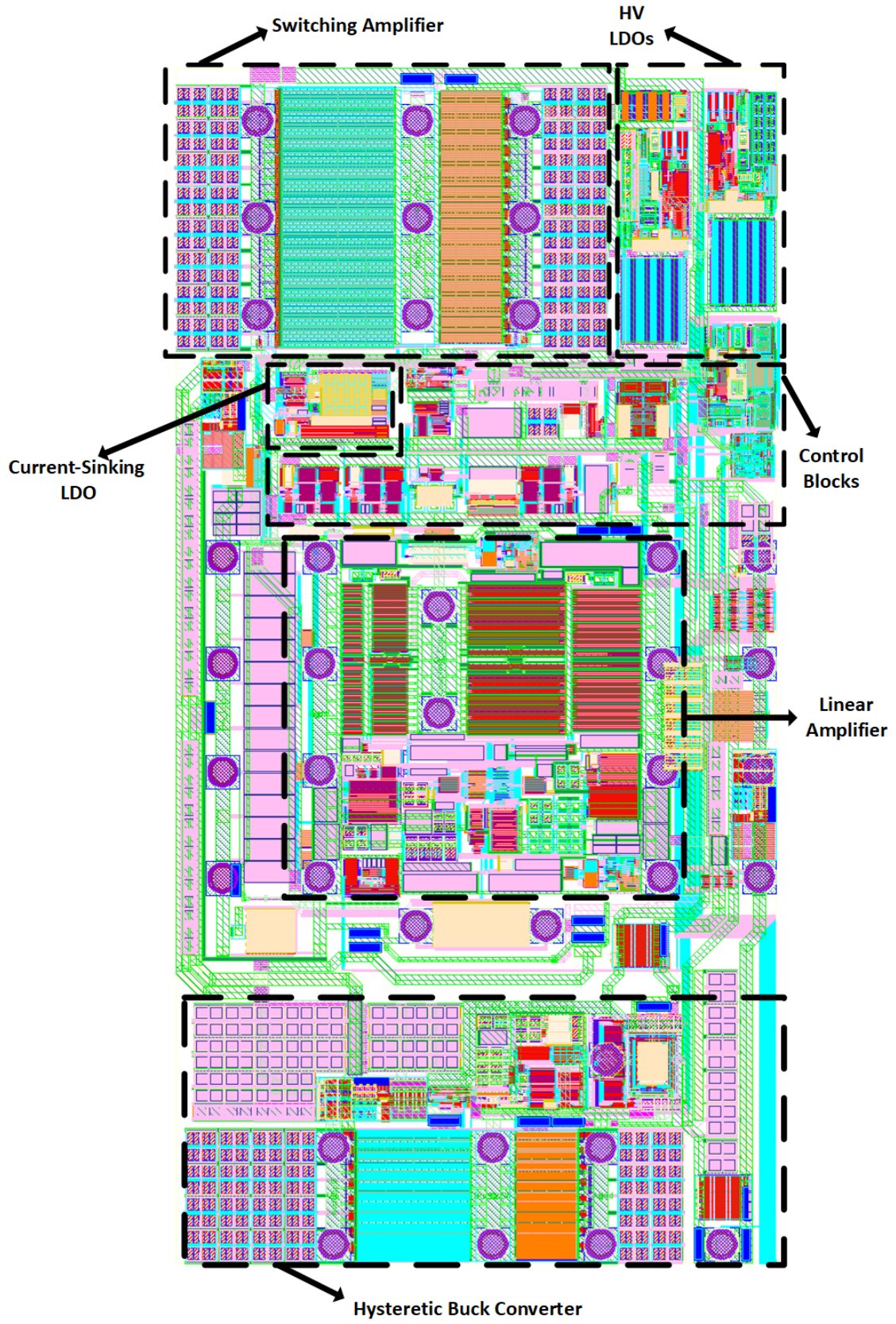

Figure 3.26 : The layout of the designed AC-coupled hybrid supply modulator

4. SIMULATION RESULTS

The circuit-level simulations of the supply modulator are given in this chapter. Each subblock is simulated individually and their performance is discussed.

4.1 Linear Amplifier Simulation Results

The linear amplifier is one of the most crucial blocks in the supply modulator system. Given that the linear amplifier generates AC current, it is important to consider how the loop may vary when the linear amplifier sources or sinks current. The simulation results of the linear amplifier under different loading conditions for different process corners are shown in Figures 4.1, 4.2, and 4.3. All simulations are done with 4-ohm load and 100 pF output capacitance, while the output voltage of the linear amplifier is set to 1.9 V.

The bode plots of the linear amplifier while sourcing 300 mA of current are shown in Figure 4.1. The linear amplifier shows 40.44 dB of DC gain at the SS -40°corner and 35.83 dB at the FF 85°corner. The minimum phase margin is 58.54°.

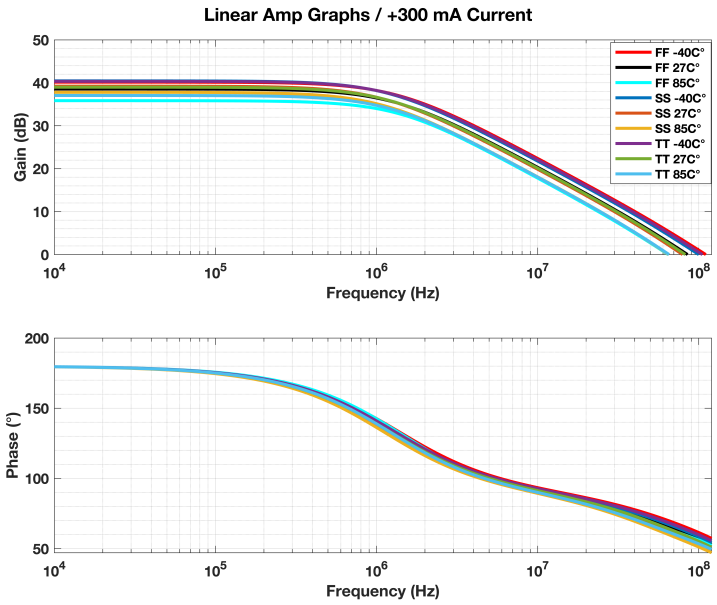

Figure 4.1 : The feedback plots of the LA while sourcing 300 mA of current

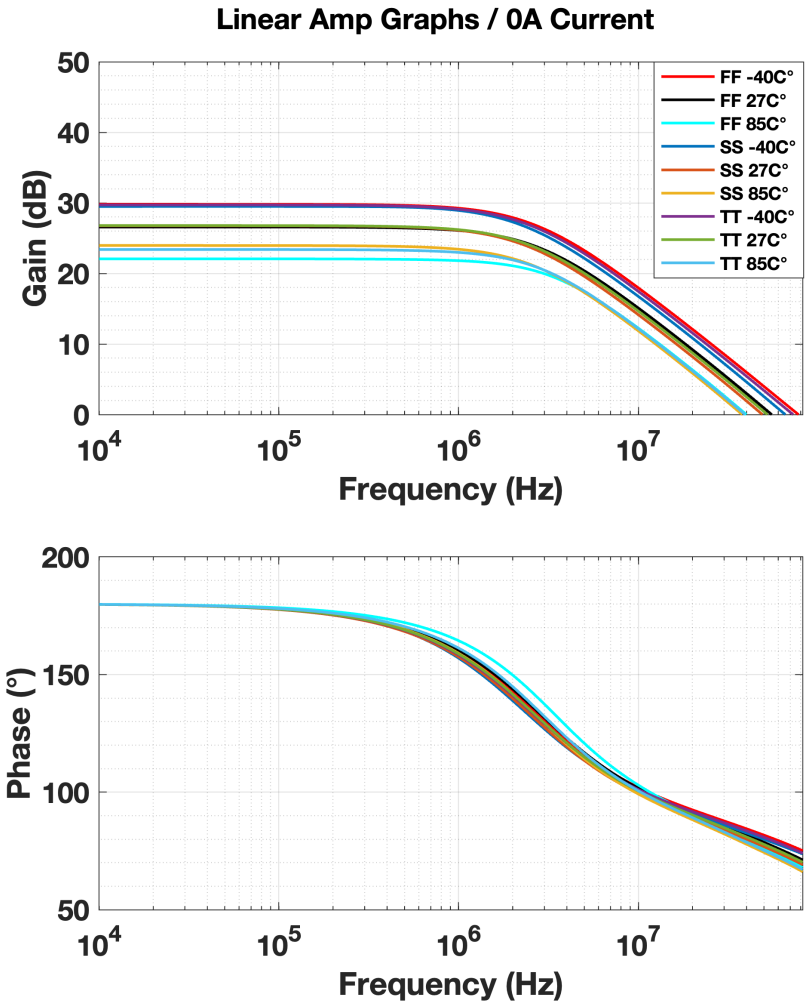

Figure 4.2 : The feedback plots of the LA while supplying zero output current

The bode plots of the linear amplifier at zero output current are shown in Figure 4.2. Since the output stage of the linear amplifier generates no current, the output transconductance and the overall gain drop considerably. The linear amplifier shows 29.8 dB DC gain for the FF -40°corner and 22.06 dB DC gain for the FF 85°corner. In addition, the minimum phase margin for whole corners is 75.83°.

Lastly, the simulation results of the linear amplifier while sinking 300 mA of DC current are shown in Figure 4.3. The linear amplifier exhibits 38.68 dB of DC gain at the FF -40°corner and 30.48 dB at the FF 85°corner. The minimum phase margin is 58.99°.

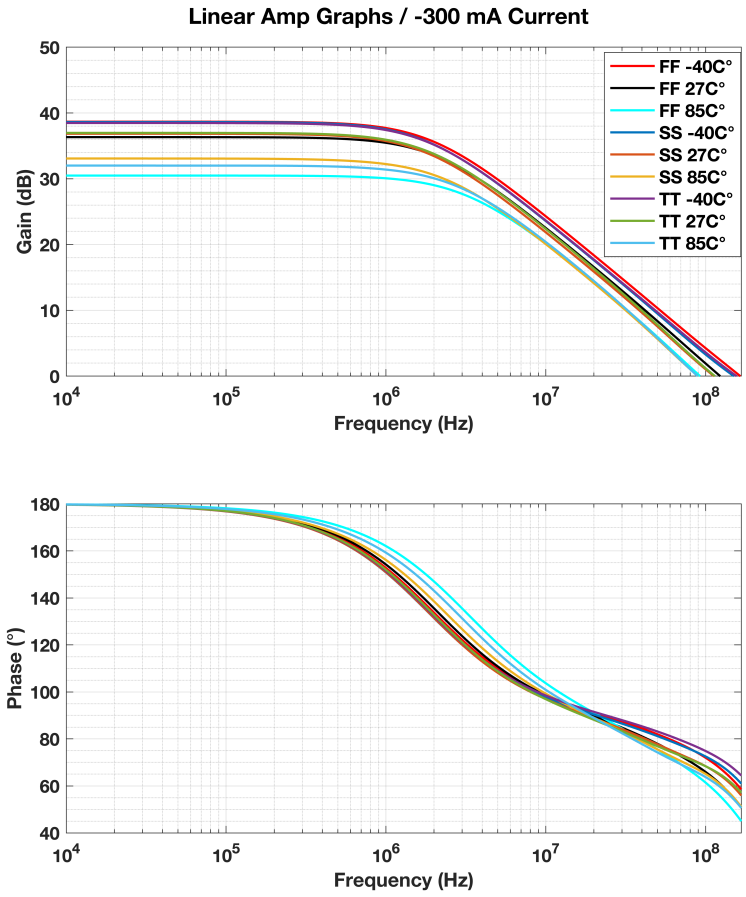

Figure 4.3 : The feedback plots of the LA while sinking 300 mA of current

4.2 Simulation Results of the Current Sensing Circuit

The best regulation is achieved by increasing the speed and linearity of the sensing mechanism. Figure 4.4 shows the performance of the sensing circuitry under a 40 MHz 5G NR signal. As can be seen from the graph, the sensing circuit's output linearly tracks the output current of the linear amplifier.

4.3 Hysteretic Comparator Simulation Results

The hysteresis value of the hysteretic comparator has a great influence on the operating frequency of the buck converter. By varying the switching frequency, the hysteresis value indirectly affects the efficiency of the SM. So, designing a hysteretic comparator with low hysteresis and low offset variation is an important design consideration for

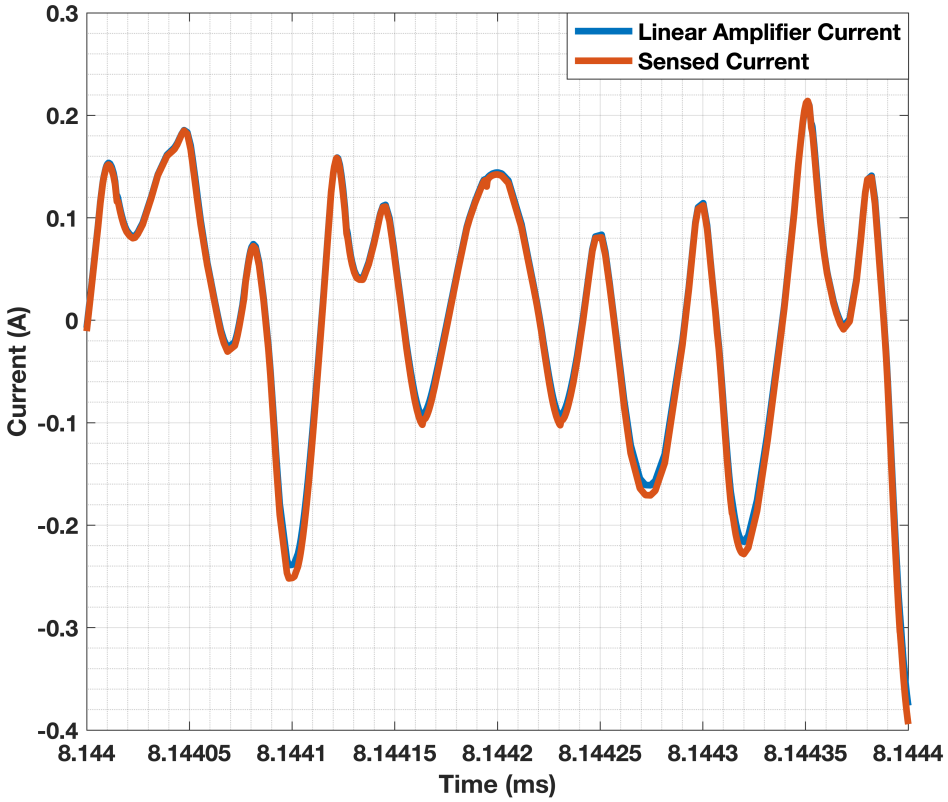

Figure 4.4 : The transient response of the current sensing circuit

overall implementation. The Monte-Carlo simulations of the hysteresis value and the offset value are shown in Figures 4.5 and 4.6, respectively. To obtain the results, 250 Monte-Carlo simulations are performed. The 21.83 mV mean, 693.131 µV standard deviation in hysteresis, and 1.05 mV standard deviation in offset are achieved.

4.4 Simulation Results of the Hysteretic Buck Converter

The hysteretic buck converter's efficiency variations for 2.5 V and 3.8 V output voltages are shown in Figure 4.7. The hysteretic buck converter achieves a maximum efficiency of %96.13 when providing a load of 200 mA for an output of 2.5 V and a maximum efficiency of %94.4 when providing a load of 200 mA for an output of 3.8 V.

The steady-state transient response of the hysteretic buck converter is shown in Figure 4.8. A 2.2 µF off-chip inductor and a 3.3 µH off-chip capacitor are used to form the output LC filter. The voltage ripple is approximately 17 mV for a 300-mA load current.

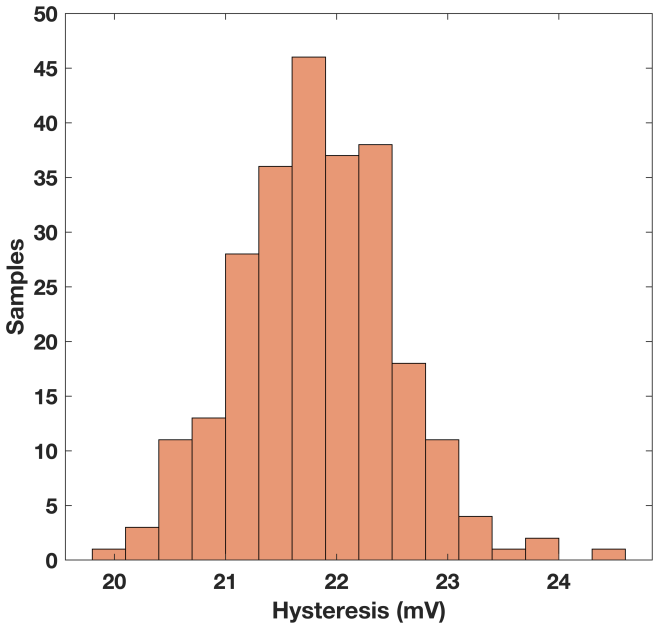

Figure 4.5 : The histogram of the comparator hysteresis

The output transient response to a 500 mA load step for 3.8 V output is depicted in Figure 4.9. As can be seen from the figure, when the load current is increased from 20 mA to 520 mA, the output voltage changes by 60 mV. Similarly, when the load current decreases from 520 mA to 20 mA, the output voltage changes by 30 mV.

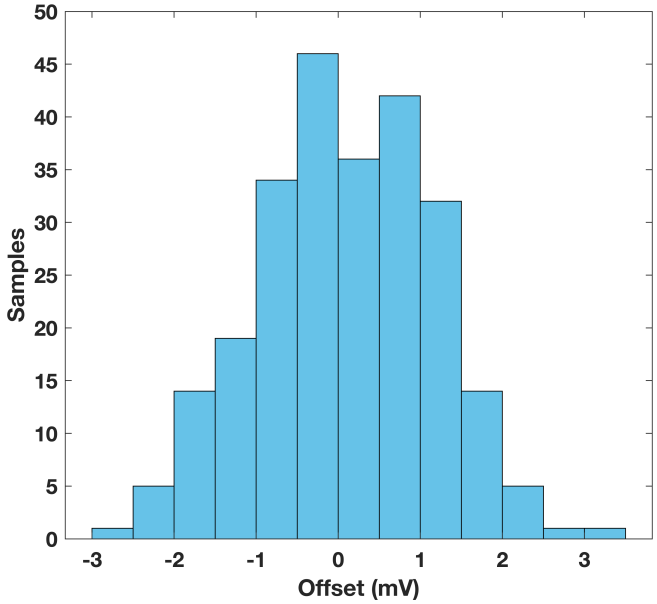

Figure 4.6 : The histogram of the comparator offset

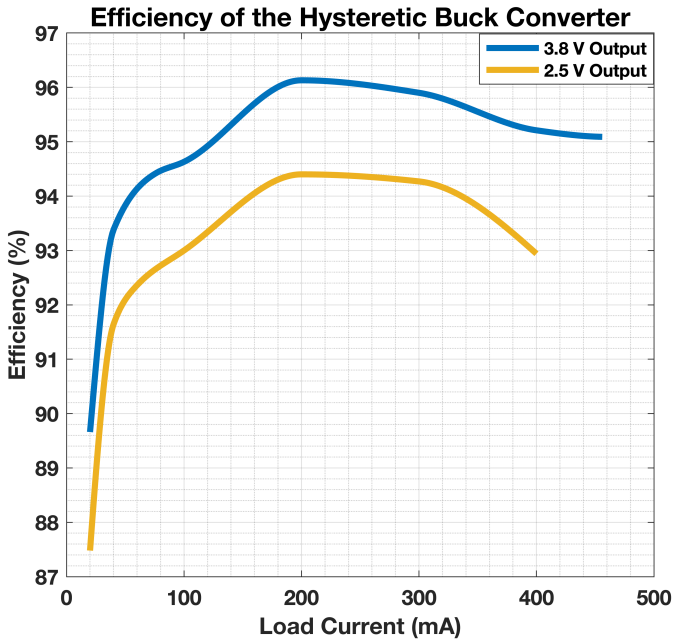

Figure 4.7 : The efficiency graph of the hysteretic buck converter

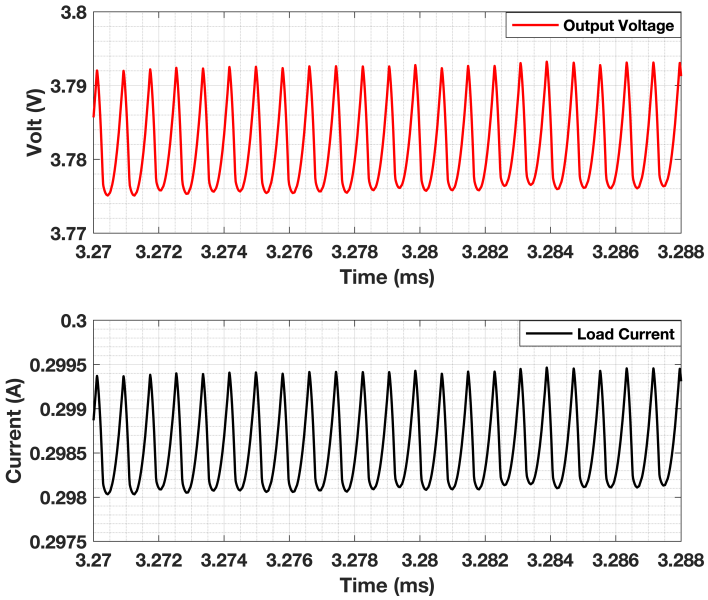

Figure 4.8 : The hysteretic buck converter transient response

The transient response of the ZCD circuit is given in Figure 4.10. The hysteretic buck converter operates in discontinuous conduction mode (DCM) while the test signal is applied. The control signal of the ZCD circuit is triggered when the inductor current approaches 0 A. After the control signal is sent to the gate driver, the NMOS power transistor is closed, thereby allowing the current to flow through the parasitic diode of the NMOS transistor.

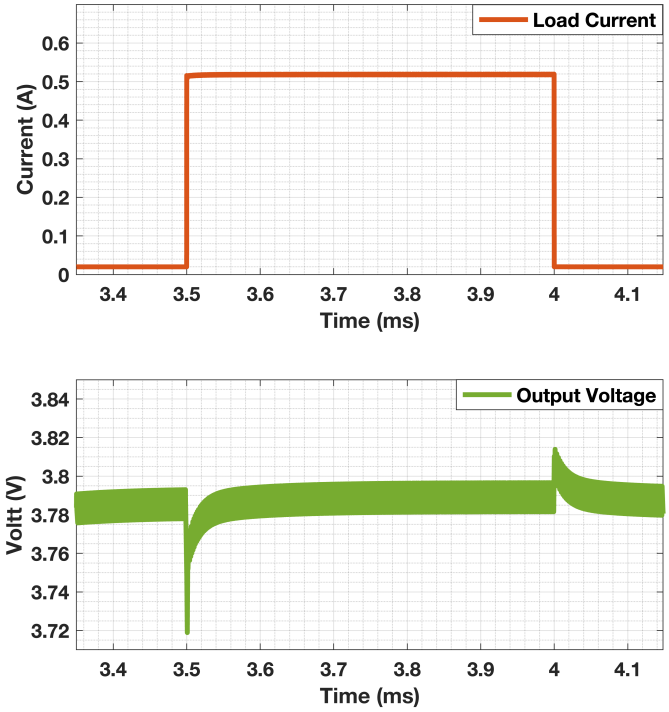

Figure 4.9 : Load step simulation for 3.8 V output

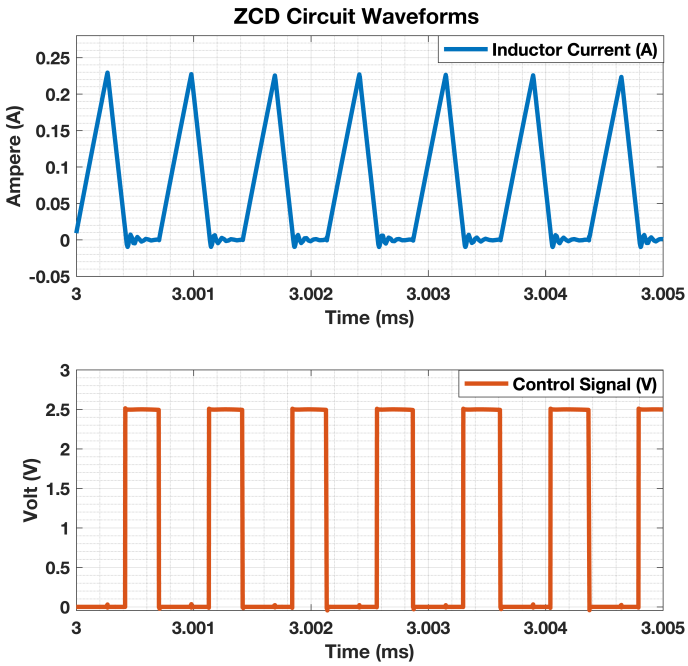

Figure 4.10 : The transient waveforms of the ZCD circuit

The simulations of the L2H and H2L level shifter circuits are given in Figures 4.11 and 4.12, respectively. The input signals with a 4 MHz switching frequency are applied to

level shifter circuits. It can be said that the level shifter circuits operate properly as intended.

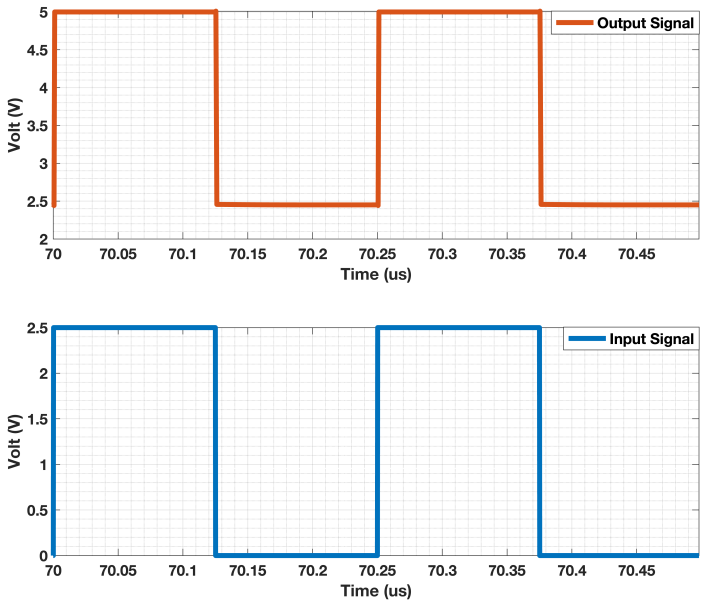

Figure 4.11 : The simulation of the L2H level shifter

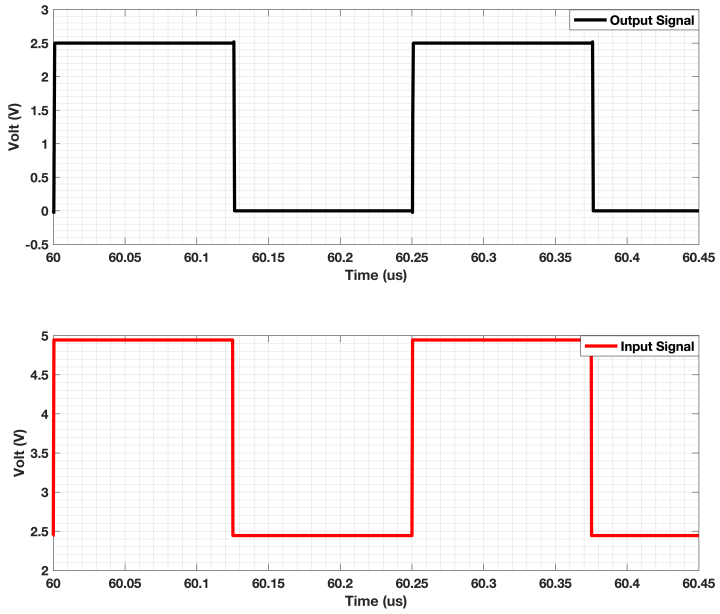

Figure 4.12 : The simulation of the H2L level shifter

4.5 HV / Auxiliary LDO Simulation Results

The bode plots of the high-voltage LDO are depicted in Figure 4.13. The simulation is done with a 2 mA load current and 600 pF output capacitance with process and temperature variations. The maximum loop gain is 105.25 dB at FF -40°corner and the minimum loop gain is 86.22 dB at SS 85°corner. The minimum phase margin of the high voltage LDO is 84°at FF -40°corner.

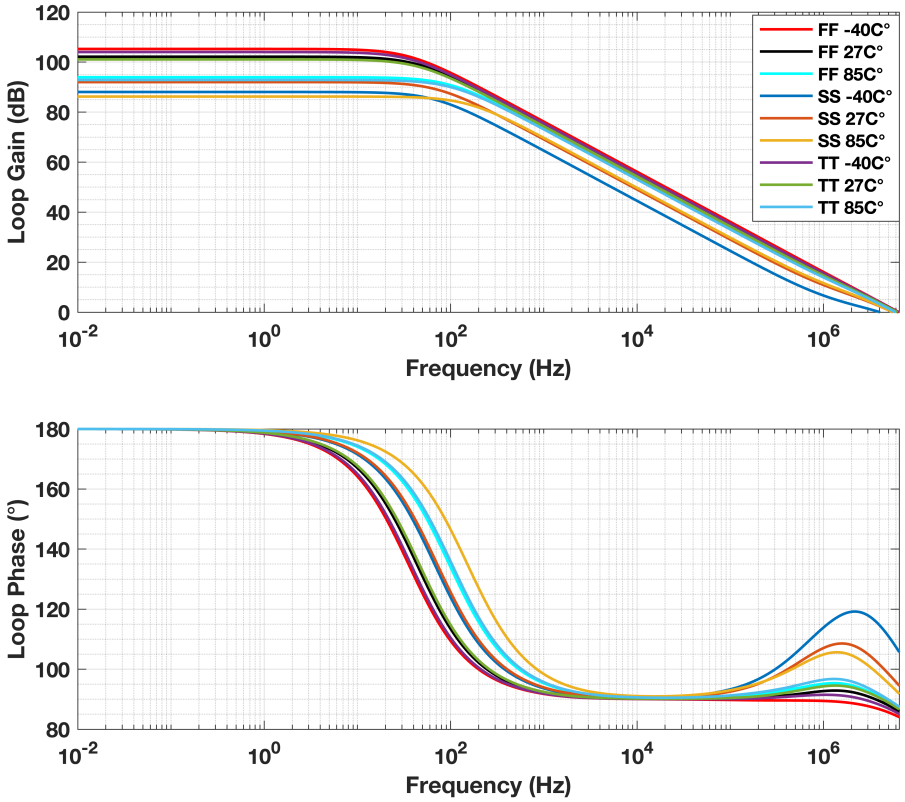

Figure 4.13 : The Bode plots of the HV LDO

4.6 Current-Sinking LDO Simulation Results

When the supply modulator is powered up, the gate driver circuits of the internal buck converters may experience an overvoltage breakdown. To remove the overvoltage stress, the current-sinking LDO is designed to follow the supply voltage of the modulator at start-up. The simulation result of the start-up sequence of the current-sinking LDO is shown in Figure 4.14.

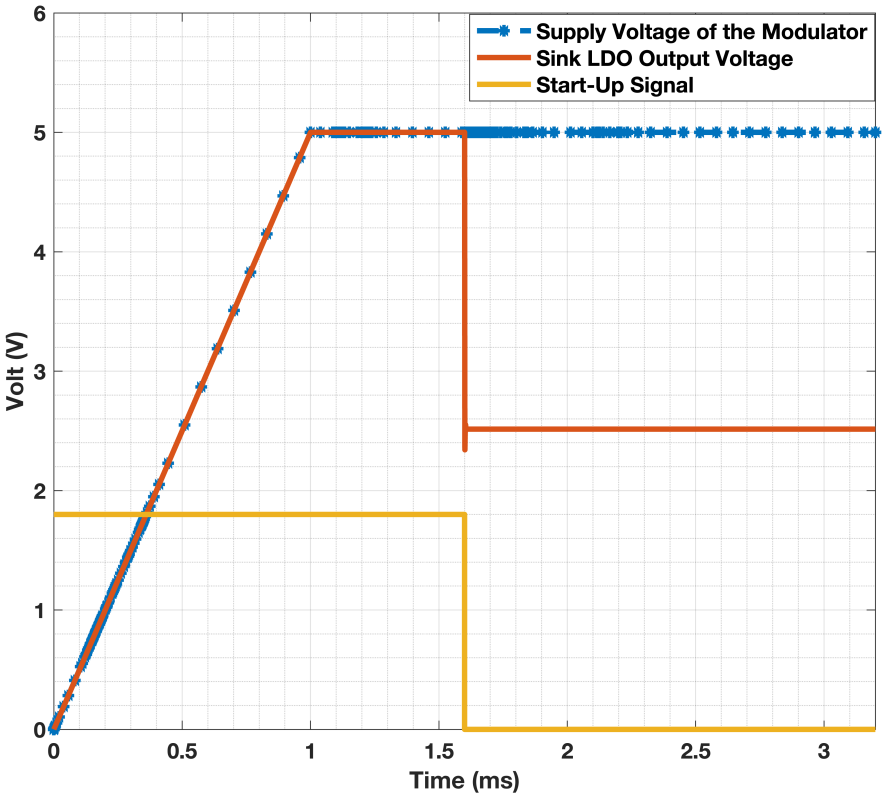

Figure 4.14 : The start-up sequence of the current-sinking LDO

The stability simulation of the current-sinking LDO for different process and temperature variations is shown in Figure 4.15. An 870 pF capacitance is placed at the LDO output to accurately simulate the stability of the LDO. The LDO exhibits a 75.45 dB loop gain at the FF -40°corner and 71.82 dB at the SS 85°corner. The minimum phase margin is 51°at the TT 85° corner.

4.7 Supply Modulator Simulation Results

The output waveform of the AC-coupled envelope tracking supply modulator for a 40 MHz 64 QAM 5G NR envelope signal is given in Figure 4.16. To simulate the RF PA, a 4-ohm resistor and 100 pF capacitor are placed in parallel. The graph illustrates that the supply modulator is capable of tracking the envelope signal without any bandwidth limitations, and the internal feedback loop generates a stable DC voltage across the coupling capacitor. The simulated efficiency variation of the supply modulator for various output power levels is shown in Figure 4.17. The maximum efficiency of

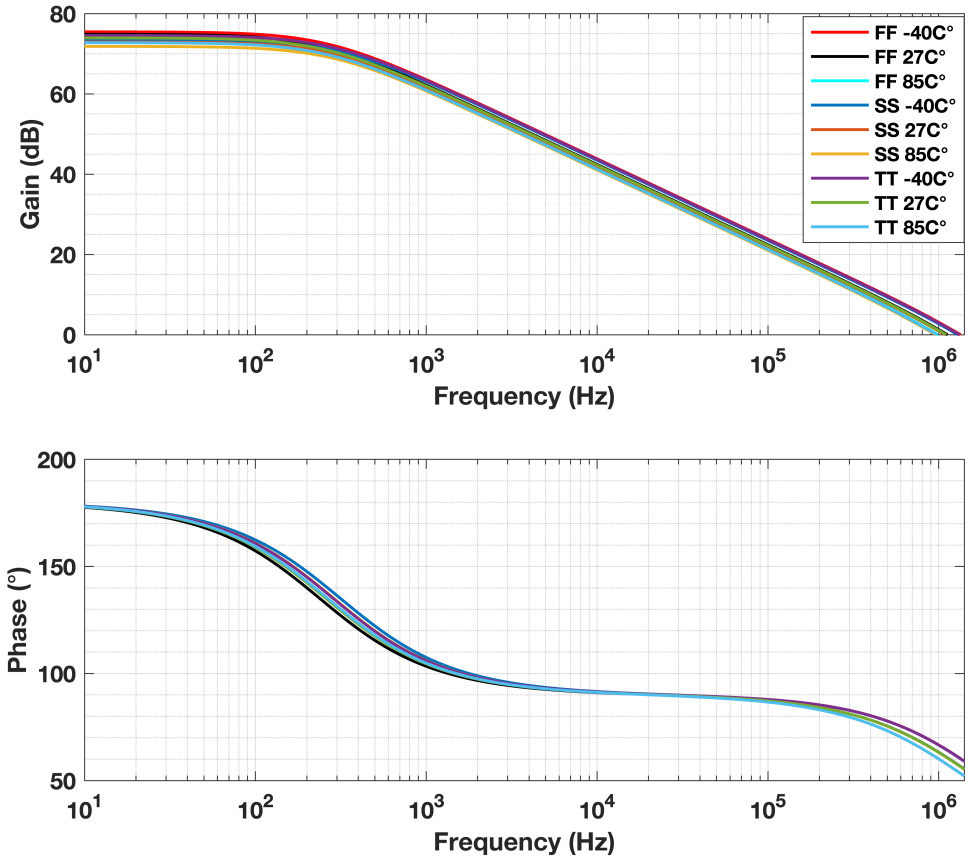

Figure 4.15 : The Bode plots of the current-sinking LDO

%82.848 is achieved at the maximum output power, and the minimum efficiency of %75.38 is obtained at the minimum output power. When the output power increases, the power consumption of the internal circuit starts to become less detrimental to the overall supply modulator efficiency. Therefore, efficiency increases proportionally with output power. Table 4.1 provides the summary of the designed supply modulator.

Table 4.1 : Summary table of the supply modulator

Parameter	Value
Technology	130 nm PD-SOI
Supply Voltage	5V
PAPR	9.796 dB
Application	5G NR C-V2X
Bandwidth	40 MHz
Output Power	2.25 W
Efficiency	%82.131
SM Area	3.051 mm^2

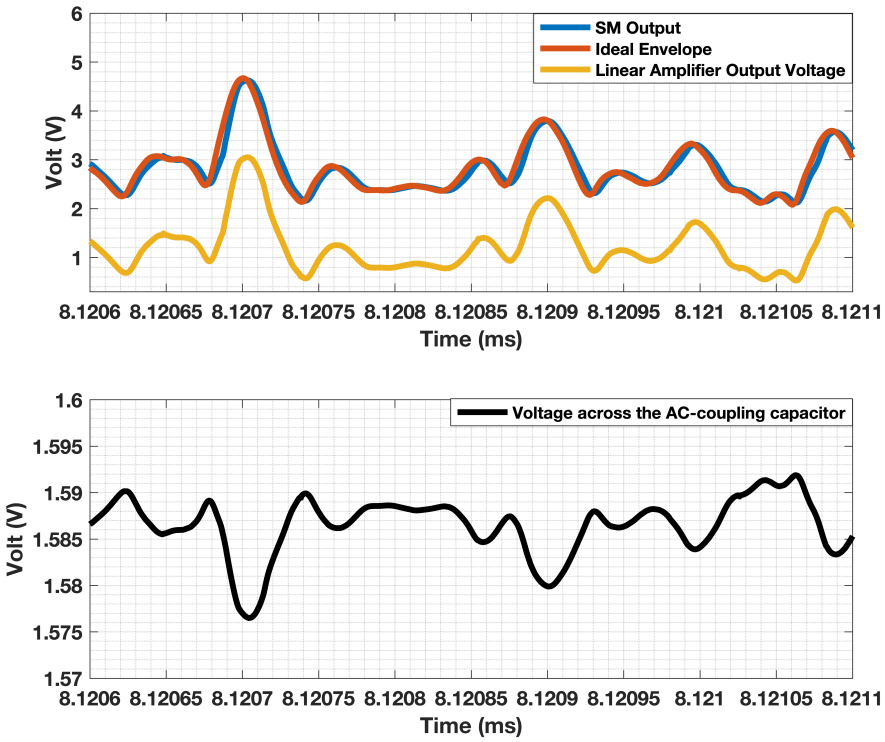

Figure 4.16 : The transient waveforms of the envelope-tracking supply modulator

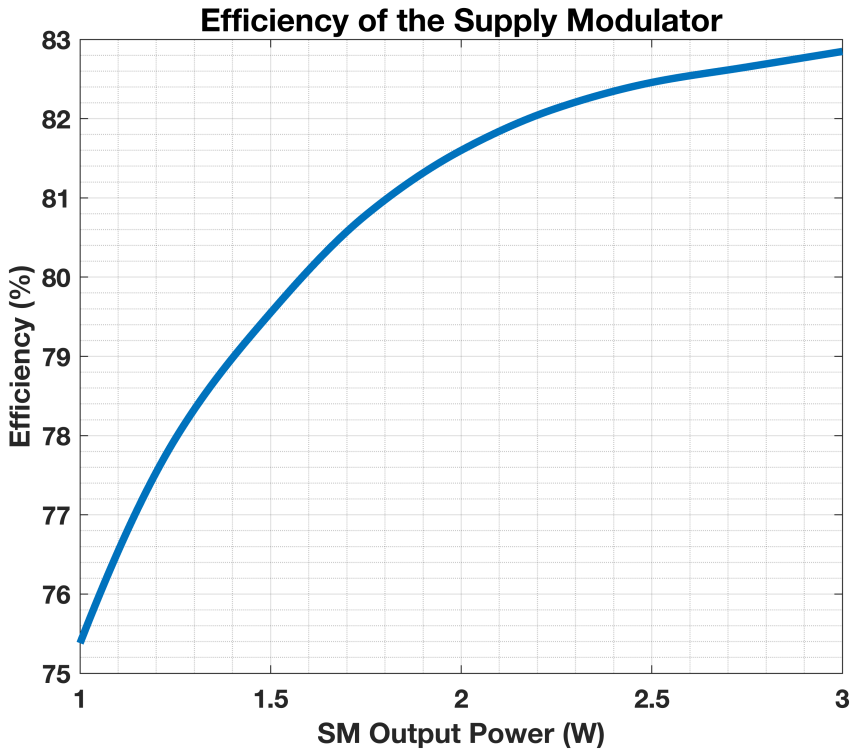

Figure 4.17 : Supply modulator efficiency vs output power

5. CONCLUSIONS

Envelope-tracking supply modulators are fundamental building blocks in today's microelectronics to increase the efficiency of transceiver systems. As an efficiency improvement method, AC-coupled modulators are widely used in the literature. In this thesis, an AC-coupled envelope tracking supply modulator that supports up to 40 MHz 64 QAM 5G NR signals is designed in ST 130 nm PD-SOI technology and verified in the Cadence Virtuoso computer-aided design (CAD) environment. The supply modulator is implemented with wide-range programmability to withstand process and temperature variations. The %82.848 efficiency is achieved at 3W output power. The overall layout occupies 3.051 mm^2.

5.1 Future Works

Considering the efficiency of the hysteretic current-mode buck converter drops considerably at low current loads, the power consumption of the internal circuit will be optimized. To handle the extreme low-voltage conditions, the buck converter will be transformed into a buck-boost converter. In order to integrate the average power tracking (APT) option into the supply modulator, a switch will be added between the internal DC-DC converter and the output of the PA. Since all verifications of the supply modulator are done with simulations, the first objective is to get the measurement results of the ETSM.

REFERENCES

[1] **Yousefzadeh, V.**, **Alarcon, E. and Maksimovic, D.** (2006). Three-level buck converter for envelope tracking applications, *IEEE Transactions on Power Electronics*, *21*(2), 549–552.

[2] **Chu, W.Y.**, **Bakkaloglu, B. and Kiaei, S.** (2008). A 10 MHz Bandwidth, 2 mV Ripple PA Regulator for CDMA Transmitters, *IEEE Journal of Solid-State Circuits*, *43*(12), 2809–2819.

[3] **Hassan, M.**, **Larson, L.E.**, **Leung, V.W. and Asbeck, P.M.** (2012). A Combined Series-Parallel Hybrid Envelope Amplifier for Envelope Tracking Mobile Terminal RF Power Amplifier Applications, *IEEE Journal of Solid-State Circuits*, *47*(5), 1185–1198.

[4] **Sung, S.**, **Hong, S.W.**, **Bang, J.S.**, **Paek, J.S.**, **Lee, S.C.**, **Cho, T.B.H. and Cho, G.H.** (2016). Envelope Modulator for 1.5W 10MHz LTE PA without AC Coupling Capacitor achieving 86.5% Peak Efficiency, *IEEE Transactions on Power Electronics*, 1–1.

[5] **Junxiong Deng**, **Gudem, P.**, **Larson, L. and Asbeck, P.** (2005). A high average-efficiency SiGe HBT power amplifier for WCDMA handset applications, *IEEE Transactions on Microwave Theory and Techniques*, *53*(2), 529–537.

[6] **Hassan, M.** (2012). *Wideband high efficiency CMOS envelope amplifiers for 4G LTE handset envelope tracking RF power amplifiers*, University of California, San Diego.

[7] **Leng, W.**, **Abidi, A.A.**, **Mundlapudi, S.R.**, **Darabi, H.**, **Chowdhury, D.**, **Afsahi, A. and Li, S.** (2022). Envelope Tracking Supply Modulator with Trellis-Search-Based Switching and 160-MHz Capability, *IEEE Journal of Solid-State Circuits*, *57*(3), 719–733.

[8] **Kahn, L.** (1952). Single-Sideband Transmission by Envelope Elimination and Restoration, *Proceedings of the IRE*, *40*(7), 803–806.

[9] **Kwak, T.W.**, **Lee, M.C. and Cho, G.H.** (2007). A 2 W CMOS Hybrid Switching Amplitude Modulator for EDGE Polar Transmitters, *IEEE Journal of Solid-State Circuits*, *42*(12), 2666–2676.

[10] **Jinsung Choi**, **Dongsu Kim**, **Daehyun Kang and Bumman Kim** (2009). A Polar Transmitter With CMOS Programmable Hysteretic-Controlled Hybrid

Switching Supply Modulator for Multistandard Applications, *IEEE Transactions on Microwave Theory and Techniques*, *57*(7), 1675–1686.

[11] **Watkins, G.T. and Mimis, K.** (2018). How Not to Rely on Moore's Law Alone: Low-Complexity Envelope-Tracking Amplifiers, *IEEE Microwave Magazine*, *19*(4), 84–94.

[12] **Kim, B.**, **Kim, J.**, **Kim, D.**, **Son, J.**, **Cho, Y.**, **Kim, J. and Park, B.** (2013). Push the Envelope: Design Concepts for Envelope-Tracking Power Amplifiers, *IEEE Microwave Magazine*, *14*(3), 68–81.

[13] **Asbeck, P. and Popovic, Z.** (2016). ET Comes of Age: Envelope Tracking for Higher-Efficiency Power Amplifiers, *IEEE Microwave Magazine*, *17*(3), 16–25.

[14] **Wang, Z.** (2014). *Envelope Tracking Power Amplifiers for Wireless Communications*.

[15] **Reynaert, P. and Steyaert, M.** (2005). A 1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE, *IEEE Journal of Solid-State Circuits*, *40*(12), 2598–2608.

[16] **Wang, F.**, **Kimball, D.F.**, **Lie, D.Y.**, **Asbeck, P.M. and Larson, L.E.** (2007). A Monolithic High-Efficiency 2.4-GHz 20-dBm SiGe BiCMOS Envelope-Tracking OFDM Power Amplifier, *IEEE Journal of Solid-State Circuits*, *42*(6), 1271–1281.

[17] **Amo, P.**, **Thomas, M.**, **Molata, V. and Jerabek, T.** (2014). 17.6 Envelope modulator for multimode transmitters with AC-coupled multilevel regulators, *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*.

[18] **Pinon, V.**, **Hasbani, F.**, **Giry, A.**, **Pache, D. and Garnier, C.** (2008). A Single-Chip WCDMA Envelope Reconstruction LDMOS PA with 130MHz Switched-Mode Power Supply, *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*.

[19] **Zhang, X. and Siek, L.** (2017). An 80.4% Peak Power Efficiency Adaptive Supply Class H Power Amplifier for Audio Applications, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *25*(6), 1954–1965.

[20] **van der Zee, R. and van Tuijl, E.** (1999). A power-efficient audio amplifier combining switching and linear techniques, *IEEE Journal of Solid-State Circuits*, *34*(7), 985–991.

[21] **Yundt, G.B.** (1986). Series- or Parallel-Connected Composite Amplifiers, *IEEE Transactions on Power Electronics*, *PE-1*(1), 48–54.

[22] **Wang, F.**, **Kimball, D.**, **Popp, J.**, **Yang, A.**, **Lie, D.**, **Asbeck, P. and Larson, L.** (2005). Wideband envelope elimination and restoration power amplifier with high efficiency wideband envelope amplifier for WLAN 802.11g

applications, *IEEE MTT-S International Microwave Symposium Digest, 2005.*

[23] **Lin, Y.C. and Chen, Y.J.E.** (2021). A CMOS Envelope Tracking Supply Converter for RF Power Amplifiers of 5G NR Mobile Terminals, *IEEE Transactions on Power Electronics*, *36*(6), 6814–6823.

[24] **Kang, D.**, **Park, B.**, **Kim, D.**, **Kim, J.**, **Cho, Y. and Kim, B.** (2013). Envelope-Tracking CMOS Power Amplifier Module for LTE Applications, *IEEE Transactions on Microwave Theory and Techniques*, *61*(10), 3763–3773.

[25] **Mahmoudidaryan, P.**, **Mandal, D.**, **Bakkaloglu, B. and Kiaei, S.** (2019). Wideband Hybrid Envelope Tracking Modulator With Hysteretic-Controlled Three-Level Switching Converter and Slew-Rate Enhanced Linear Amplifier, *IEEE Journal of Solid-State Circuits*, *54*(12), 3336–3347.

[26] **Paek, J.S.**, **Kim, D.**, **Choo, Y.**, **Youn, Y.S.**, **Lee, J. and Cho, T.B.H.** (2019). Design of Boosted Supply Modulator With Reverse Current Protection for Wide Battery Range in Envelope Tracking Operation, *IEEE Transactions on Microwave Theory and Techniques*, *67*(1), 183–194.

[27] **Jing, Y. and Bakkaloglu, B.** (2017). A High Slew-Rate Adaptive Biasing Hybrid Envelope Tracking Supply Modulator for LTE Applications, *IEEE Transactions on Microwave Theory and Techniques*, *65*(9), 3245–3256.

[28] **He, H.**, **Kang, Y.**, **Ge, T.**, **Guo, L. and Chang, J.S.** (2019). A 2.5-W 40-MHz-Bandwidth Hybrid Supply Modulator With 91% Peak Efficiency, 3-V Output Swing, and 4-mV Output Ripple at 3.6-V Supply, *IEEE Transactions on Power Electronics*, *34*(1), 712–723.

[29] **Kim, D.**, **Kang, D.**, **Kim, J.**, **Cho, Y. and Kim, B.** (2012). Highly Efficient Dual-Switch Hybrid Switching Supply Modulator for Envelope Tracking Power Amplifier, *IEEE Microwave and Wireless Components Letters*, *22*(6), 285–287.

[30] **Shrestha, R.**, **van der Zee, R.**, **de Graauw, A. and Nauta, B.** (2009). A Wideband Supply Modulator for 20 MHz RF Bandwidth Polar PAs in 65 nm CMOS, *IEEE Journal of Solid-State Circuits*, *44*(4), 1272–1280.

[31] **Li, Y.**, **Lopez, J.**, **Wu, R. and Lie, D.Y.C.** (2012). A Fully Monolithic BiCMOS Envelope-Tracking Power Amplifier With On-Chip Transformer for Broadband Wireless Applications, *IEEE Microwave and Wireless Components Letters*, *22*(6), 288–290.

[32] **Riehl, P.**, **Fowers, P.**, **Hao-Ping Hong and Ashburn, M.** (2013). An AC-coupled hybrid envelope modulator for HSUPA transmitters with 80% modulator efficiency, *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*.

[33] **Paek, J.S.**, **Youn, Y.S.**, **Choi, J.H.**, **Kim, D.S.**, **Jung, J.H.**, **Choo, Y.H.**, **Lee, S.J.**, **Lee, S.C.**, **Cho, T.B. and Kang, I.Y.** (2016). 20.7 An RF-PA supply modulator achieving 83% efficiency and −136dBm/Hz noise for LTE-40MHz and GSM 35dBm applications, *2016 IEEE International Solid-State Circuits Conference (ISSCC)*.

[34] **Paek, J.S.**, **Kim, D.**, **Bang, J.S.**, **Baek, J.**, **Choi, J.**, **Nomiyama, T.**, **Han, J.**, **Choo, Y.**, **Youn, Y.**, **Park, E.**, **Lee, S.**, **Kim, I.H.**, **Lee, J.**, **Cho, T.B. and Kang, I.** (2019). 15.1 An 88%-Efficiency Supply Modulator Achieving 1.08μs/V Fast Transition and 100MHz Envelope-Tracking Bandwidth for 5G New Radio RF Power Amplifier, *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*.

[35] **Ho, C.Y.**, **Lin, S.M.**, **Meng, C.H.**, **Hong, H.P.**, **Yan, S.H.**, **Kuo, T.H.**, **Peng, C.S.**, **Hsiao, C.H.**, **Chen, H.H.**, **Sung, D.W. and Kuan, C.W.** (2018). An 87.1% efficiency RF-PA envelope-tracking modulator for 80MHz LTE-Advanced transmitter and 31dBm PA output power for HPUE in 0.153μm CMOS, *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*.

[36] **Liu, X.**, **Zhang, H.**, **Mok, P.K.T. and Luong, H.C.** (2019). A Multi-Loop-Controlled AC-Coupling Supply Modulator With a Mode-Switching CMOS PA in an EER System With Envelope Shaping, *IEEE Journal of Solid-State Circuits*, *54*(6), 1553–1563.

[37] **Paek, J.S.**, **Lee, S.C.**, **Youn, Y.S.**, **Kim, D.**, **Choi, J.H.**, **Jung, J.**, **Choo, Y.H.**, **Lee, S.J.**, **Han, J.Y. and Cho, T.B.** (2016). A − 137 dBm/Hz Noise, 82% Efficiency AC-Coupled Hybrid Supply Modulator With Integrated Buck-Boost Converter, *IEEE Journal of Solid-State Circuits*, *51*(11), 2757–2768.

[38] **Huang, C.S.**, **Tzeng, T.Y.**, **Huang, W.C.**, **Kao, Y.H.**, **Wu, J.L.**, **Chen, K.H.**, **Lin, Y.H.**, **Lin, S.R. and Tsai, T.Y.** (2022). An Energy Recycling Envelope Tracking Supply Modulator Assisted by Small Cap Replica With 89.7% Efficiency and 37% Reduced Linear Amplifier Current for 150 MHz Bandwidth 5G New Radio RF Applications, *IEEE Journal of Solid-State Circuits*, *57*(11), 3361–3369.

[39] **Paek, J.S.**, **Kim, D.**, **Han, J.Y.**, **Choo, Y.**, **Bang, J.S.**, **Park, S.**, **Baek, J.**, **Nomiyama, T.**, **Kim, I.H. and Lee, J.** (2022). Efficient RF-PA Two-Chip Supply Modulator Architecture for 4G LTE and 5G NR Dual-Connectivity RF Front End, *IEEE Journal of Solid-State Circuits*, *57*(4), 1075–1089.

[40] **Liu Qing**, **Zhang Donglai and Liu Mingyu** (2012). A novel control method for multilevel converter used inenvelope tracking power supply, *Proceedings of The 7th International Power Electronics and Motion Control Conference*.

[41] **Rodriguez, M.**, **Rodríguez, A.**, **F. Miaja, P. and Sebastián, J.** (2009). Fast Dynamic Response Multilevel Converter for Voltage Tracking

Applications, *13th European Conference on Power Electronics and Applications*.

[42] **Mahmoudidaryan, P.** (2019). *Hybrid Envelope Tracking Supply Modulator Analysis and Design for Wideband Applications*, Arizona State University.

[43] **Razavi, B.** (2000). *Design of Analog CMOS Integrated Circuits*, McGraw-Hill Science, Engineering Mathematics.

[44] **Baker, R.J.** (1997). *CMOS Circuit Design, Layout and Simulation*, volume 7 of *IEEE Press Publication Ser.*, Wiley-IEEE Press.

[45] **C. Sansen, W.M.** (2006). *Analog Design Essentials*, volume859 of *The\Springer International Series in Engineering and Computer Science Ser.*

[46] **Allen, P.E. and Holberg, D.R.** (2011). *CMOS Analog Circuit Design*, The\Oxford Series in Electrical and Computer Engineering.

[47] **Wan-Rone Liou**, **Mei-Ling Yeh and Yueh Lung Kuo** (2008). A High Efficiency Dual-Mode Buck Converter IC For Portable Applications, *IEEE Transactions on Power Electronics*, *23*(2), 667–677.

[48] **Hsu, S.P.**, **Brown, A.**, **Rensink, L. and Middlebrook, R.** (1979). Modelling and analysis of switching DC-to-DC converters in constant-frequency current-programmed mode, *1979 IEEE Power Electronics Specialists Conference*.

[49] **Maniktala, S. and Microsemi Corporation** (2012). Voltage-Mode, Current-Mode (and Hysteretic Control), **Technical Report**, [Online; accessed 2022-09-15].

[50] **Su, F.**, **Ki, W.H. and Tsui, C.Y.** (2008). Ultra Fast Fixed-Frequency Hysteretic Buck Converter With Maximum Charging Current Control and Adaptive Delay Compensation for DVS Applications, *IEEE Journal of Solid-State Circuits*, *43*(4), 815–822.

[51] **Forghani-zadeh, H. and Rincon-Mora, G.** Current-sensing techniques for DC-DC converters, *The 2002 45th Midwest Symposium on Circuits and Systems, 2002. MWSCAS-2002.*

[52] **Nabeshima, T.**, **Sato, T.**, **Yoshida, S.**, **Chiba, S. and Onda, K.** Analysis and design considerations of a buck converter with a hysteretic PWM controller, *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*.

[53] **Changsik Yoo** (2000). A CMOS buffer without short-circuit power consumption, *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, *47*(9), 935–937.

[54] **Cho, Y.K.**, **Kim, M.D. and Kim, C.Y.** (2018). A Low Switching Noise and High-Efficiency Buck Converter Using a Continuous-Time Reconfigurable Delta-Sigma Modulator, *IEEE Transactions on Power Electronics*, *33*(12), 10501–10511.

[55] **Çoban, M.** (2023). *GF 22nm FDSOI POWER MANAGEMENT UNIT WITH INTEGRATED SRAM DESIGN*, Istanbul Technical University Graduate School.

CURRICULUM VITAE

Name SURNAME: Furkan Barin

EDUCATION:

- **B.Sc.:** 2020, Yıldız Technical University, Faculty of Electrical and Electronics Engineering, Department of Electronics and Communication Engineering

PROFESSIONAL EXPERIENCE AND REWARDS:

- 2020-Present TUBİTAK BILGEM TUTEL.

PUBLICATIONS, PRESENTATIONS AND PATENTS ON THE THESIS:

- **Barin F.**, Tekin A., & Zencir E. (2023). Hysteretic Buck Converter for C-V2X Supply Modulator. 2nd INTERNATIONAL GRADUATE RESEARCH SYMPOSIUM .

OTHER PUBLICATIONS, PRESENTATIONS AND PATENTS:

- **Barin, F**. and Zencir, E. (2021). A High-Speed Fully Differential Telescopic Op-Amp for Active Filter Designs in V2X Applications, Journal of Circuits, Systems and Computers, 31(05).

- **Barin, F**. and Zencir, E. (2022). Gain and Bandwidth Programmable Fourth-Order Multiple Feedback Butterworth Low-Pass Filter for C–V2X Applications, Journal of Circuits, Systems and Computers, 31(09)