A FULLY-INTEGRATED AND BATTERY-FREE INTERFACE ELECTRONICS FOR LOW VOLTAGE VIBRATION-BASED ELECTROMAGNETIC ENERGY HARVESTERS

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ABSTRACT

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Energy harvesters use environmental energy sources such as heat, light, and vibration, and convert them to electrical energy. The development of micro-scale energy harvesters together with the decreasing power demand of new generation integrated circuits, allow the use of these harvesters as energy source in microsystems as an alternative for batteries. Energy harvesting can then be used for supplying power to the sensors which operate in inaccessible environments, as an enabling technology. However, the generated electrical energy from vibration is in AC form, and design of an efficient and low power interface electronic circuit is crucial especially if the generated voltage and power of these harvesters are at low levels.

The aim of this study is to design a fully-integrated and battery-free interface circuit for electromagnetic (EM) energy harvester with low voltage output. The voltage generated by EM energy harvesters is considerably low (<1 V) at low vibration levels (< 10Hz). Hence a low voltage and highly efficient interface circuit must be designed in order to efficiently transfer the power generated by the harvester to the load at a standard system voltage.

The interface circuit requires various blocks for efficient power transfer from the harvester to the electrical load. Firstly, there should be an AC to DC converter or a rectifier for converting the generated AC voltage to a DC voltage. Another important block is the DC to DC converter which enables the step-up of the converted voltage to a desired value. Finally, a voltage regulator block should be used for obtaining a stable DC voltage as of a typical battery. The amount of power dissipated by the interface electronics must be kept as low as possible compared to the generated power since the available output power from the harvester is typically low.

The designed interface circuit includes all necessary blocks for a full system solution and shows good performance especially at low input AC voltages (<0.5 V peak). The circuit includes a novel rectifier circuit which uses an AC/DC doubler structure to benefit from the full cycle of the input signal. The proposed rectifier uses active diode structure to minimize the effective voltage drop at the output. The comparator circuits utilized at the active diodes are powered internally by another passive rectifier and external power requirement of the circuit is eliminated. The DC/DC converter block of the interface circuit includes a low voltage charge pump and a low power on- chip oscillator design. The final block of the system is a low power voltage regulator which regulates the output to 1 V DC voltage.

The proposed interface electronic is designed and fabricated by using TSMC 90 nm CMOS technology. The designed system is merged with an in-house EM energy harvester module and tested with various vibration conditions. The maximum power conversion efficiency of the rectifier stage of the circuit is 67%, while providing 0.61 V for 40 µA load, and it is able to operate down to 100 mV input peak voltages. When the rectifier block is combined with the DC/DC converter, the circuit is able to generate more than 1 V output voltage on 1 MΩ load resistance for input peak voltages higher than 0.4 V.

During the tests of the fabricated IC, it is observed that the voltage regulator block does not operate as expected. The reason for this is investigated through tests and simulations, and it is concluded that the fabricated transistors were slower than the typical transistors in this specific IC run. The regulator block is then re-designed to be more robust to fabrication variations for another IC run.

In the frame of this study, a low voltage CMOS interface electronics have been designed and tested together with a vibration based electromagnetic energy harvester module. The results show that the designed rectifier has the lowest operation voltage among the fully-integrated and self-powered interface circuits for low vibration range, to the best of our knowledge. Furthermore, the rectified voltage is stepped up with the DC/DC converter, so that the output of the circuit reaches to typical battery voltages even with very low AC input signals, enabling the use of the system as an alternative energy source for wireless microsystems.

Keywords: Self-powered rectifier, low voltage AC/DC conversion, vibration-based energy harvesting, electromagnetic energy harvester, Low power interface electronic design, on-chip power management design.

ÖZ

DÜŞÜK VOLTAJ SEVIYELERINDE ÇALIŞAN TITREŞIM TABANLI ELEKTROMANYETIK ENERJI ÜRETEÇLERI IÇIN TAMAMEN ENTEGRE VE PIL GEREKTIRMEYEN BIR ELEKTRONIK DEVRE

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Enerji üreteçleri sıcaklık, ışık ve titreşim gibi çevresel enerji kaynaklarını kullanırlar ve bu kaynakların elektrik enerjisine çevirimini sağlarlar. Mikron düzeyli enerji üreteçlerinin gelişmesi ve yeni jenerasyon entegre devrelerin düşük güçlerde çalışabilmesi sayesinde, bu sistemlerin bataryalar yerine enerji kaynağı olarak kullanılmasını sağlamaktadır. Bunun sonucunda enerji üreteçeleri ulaşılması zor alanlara yerleştirilmiş sensörlere güç sağlamak amaçlı kullanılabilirler. Titreşimden üretilen elektrik enerjisi AA formunda olduğundan dolayı; verimli ve düşük güçlü bir arayüz elektronik devresi, özellikle düşük güç ve voltaj seviyelerinde üretilen sinyaller için önemli rol oynamaktadır.

Bu çalışmanın temel amacı düşük voltaj seviyelerinde çalışan titreşim tabanlı elektromanyetik (EM) enerji üreteçleri için tamamen entegre ve pil gerektirmeyen bir elektronik devrenin tasarlanmasıdır. Düşük titreşim seviyelerinde (< 10 Hz) EM enerji üreteçlerinden elde edilen voltaj seviyeleri de düşüktür (<1 V). Bundan dolayı düşük voltajlarda ve yüksek verimlilikte çalışan bir arayüz devresinin tasarlanması üretilen gücün yüke aktarımı için önemli bir rol oynamaktadır.

Üretilen gücün verimli bir biçimde elektriksel yüke aktarılabilmesini sağlamak için arayüz devresinin farklı bloklardan oluşturulması gerekmektedir. İlk olarak, üretilen AA (Alternatif Akım) voltajını DA (Doğrusal Akım) voltajına çevirmek için bir AA/DA çevirici veya doğrultucu kullanılmalıdır. Bir diğer önemli blok ise çevrilin DA voltajı istenilen değere getirecek bir DA/DA çeviricisidir. Son olarak, pil görevi görecek sabit bir DA voltajı üretmek için bir voltaj regülatörü bloğu kullanılmalıdır. Arayüz devresi tarafından tüketilen güç miktarı üretilen güce göre mümkün olduğunca küçük tutulmalıdır ki enerji üreteci ile arayüz entegre devresinin bağlanması kullanışlı olsun.

Tasarlanan sistem tam bir sistem çözümü sağlamaktadır ve özellikle düşük giriş voltaj değerleri (< 0.5 V peak) için çok iyi performans göstermektedir. Devre giriş voltajının bütün tepe-tepe voltajını kullanmasını sağlayan AA/DA çiftleyici (AC/DC doubler) yapısını kullanan yeni bir doğrulayıcı tasarımı içermektedir. Önerilen doğrulayıcı devresi çıkış voltajındaki voltaj düşümünü minimize etmek için aktif diyot yapısını kullanmaktadır. Kullanılan aktif diyotlardaki karıştırıcı devrelerinin güç gereksinimini karşılamak için ekstra bir pasif doğrultucu devresi kullanılmış ve devrenin dışardan güç alma problemi giderilmiştir. Devrenin bir diğer kısmı olan DA/DA çevirici devresinde tamamen entegre bir yapı oluşturmak için düşük voltajda çalışan bir şarj pompası ve düşük güçte çalışan bir osilatör devresi tasarlanmıştır. Tasarlanan sistemin son bloğu düşük güçte çalışan ve çıkış voltajını 1 V'a regüle eden bir voltaj regülatörü devresidir.

Önerilen arayüz elektroniği TSMC 90 nm CMOS teknolojisi kullanılarak tasarlanmış ve ürettirilmiştir. Tasarlanan sistem bir elektromanyetik enerji üreteci ile birleştirilmiş ve farklı titreşim koşullarında test edilmiştir. Devrenin doğrultucu kısmının en yüksek güç verimliliği, 0.61 V çıkış voltajı ve 40 µA yük akımı koşulları altında %67 olarak ölçülmüştür ve doğrultucu devresi 100 mV giriş tepe voltajından yüksek değerlerde çalışabildiği doğrulanmıştır. Doğrultucu ve DA/DA çevirici devresi birleştirildiğinde elde edilen devre, 0.4 V'tan yüksek giriş tepe voltajları için 1 MΩ yük direnci ile 1 V'tan fazla çıkış voltajı üretebilmektedir.

Üretilen arayüz devresinin (IC) testleri sırasında, devrede bulunan voltaj regülatörünün istendiği gibi çalışmadığı gözlemlenmiştir. Yapılan testler ve simülasyonlar sonucunda, üretilen transistörlerin kullanılan teknolojideki tipik transistör performanslarından daha yavaş çalıştığı doğrulanmıştır. Bunun sonucunda regülatör bloğu üretimden kaynaklı sapmalara daha dayanıklı olacak şekildeyeninde tasarlanmıştır.

Bu çalışma kapsamında, düşük voltajda çalışan bir CMOS arayüz elektroniği tasarlanmış ve titreşim tabanlı bir elektromanyetik enerji üreteci ile test edilmiştir. Sonuçlar, tasarlanan doğrulayıcı devresinin düşük titreşimlerde çalışan tamamen-entegre ve pil gerektirmeyen arayüz elektronikleri içinde bilinen en düşük çalışma voltajına sahip olduğunu göstermektedir. Bunun yanında, doğrultulan voltaj DA/DA çevirici devresi ile yükseltilerek düşük seviyelerdeki AA giriş voltajlarının bile tipik bir pil voltajına ulaşması sağlanmıştır, böylece tasarlanan sistem kablosuz mikrosistemler için alternatif bir güç kaynağı olarak kullanılabilmektedir.

Anahtar kelimeler: Kendi gücünü sağlayan doğrultucu, düşük voltajlar için AA/DA çevirici, titreşim tabanlı enerji üreteci, elektromanyetik enerji üreteci, düşük güçlü arayüz elektroniği tasarımı, çip seviyesinde güç yönetimi tasrımı.

To my parents,

my brother,

and

my love

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INTRODUCTION

Improvements in microelectronics and MEMS technology increasingly enabled portable low cost and low power micro devices. These portable devices have become a part of our daily life in many application areas, such as wireless sensor networks, direction sensors as accelerometer and gyroscopes, automotive systems e.g. tire pressure monitoring systems, implantable systems for health care and monitoring, and military applications. For many years, batteries have been used as the main power sources in these systems. However, the advance of the battery technology is not as pronounced as that of the MEMS technology. In addition to their large dimensions with respect to the portable systems, limited capacity of the batteries make them unsuitable for embedded applications. Moreover, the replacement cost of batteries generates a major obstacle to the formation of wireless sensor networks with hundreds of nodes [1]. Therefore, using batteries as the power sources of these systems is impractical when their desired dimensions and lifespan considered. Hence, the need for efficient and compact energy harvesting devices for powering these portable systems arises. Low cost, durable and eco-friendly properties of energy harvesters make them much more attractive. All power of the new generation integrated circuits can be supplied from energy harvester modules, because of the reduced power demands of the systems. This results in the replacement of the temporary storage elements, like batteries, with the continuously self-charging energy sources.

Studies on the design and implementation of mechanical part of the transducers for harvesting ambient energy take up a huge portion of the researches on energy scavengers. However, interface electronics part of the system is also a significant concern due to low power and low voltage profile of the scavenged energy. Furthermore, interface electronics helps to manage the harvested energy efficiently.

This thesis aims to design low voltage, low power, and efficient interface electronics for the signals generated from electromagnetic energy harvesters stimulated by low frequency environmental vibration. The interface electronics is used for converting the generated alternating signal to DC and often stepping it up to higher voltage levels to be utilized at practical applications. In this chapter, a brief introduction to energy harvesting and interface electronics for vibration based energy harvesters is provided. The electromagnetic energy harvester system receives the main focus among the vibration based harvesters due to its challenging low output voltage levels.. Section 1.1 summarizes types of ambient energy sources and the transducers that can be used to

convert these sources into electrical energy. Section 1.2 explains the operation principle of electromagnetic energy harvesters and reviews the recent work on the technology. Section 1.3 describes interface electronics for different types of vibration based energy harvesters and each type is clarified with examination of a most commonly used circuit example. Section 1.4 presents the objective of the thesis by considering goals and achievements gained by the thesis. Finally, the organization of the thesis is outlined in Section 1.5.

1.1. Ambient Energy Sources and Energy Harvesters

The most well-known ambient energy sources are light, heat, and vibration which are also widely used as the sources for energy harvesters [2–4]. Some commercially established products are available such as the wristwatches developed by Seiko and self-powered calculators [5], [6]. Table 1.1 shows the comparison of energy harvesting sources and other power sources for including batteries [7], [8]. The table also includes different transduction mechanisms for these sources and the generated power densities for 1 year and 10 year lifetimes. Since the ambient energy sources are always available in the nature, the power density of these energy sources stays constant with the increasing lifetime (first five rows). Although the power densities of batteries and fuel cells look superior at short lifetime, the advantage disappears under long term usage. The additional disadvantage of energy sources with electrochemical transduction is that they consume precious underground resources. Furthermore, dead batteries need appropriate treatment to avoid environmental pollution.

Table 1.1: Comparison of energy sources according to generated power densities

Energy Source	**Transduction Mechanism**	**Power Density ($\mu W/cm^3$) 1-year lifetime**	**Power Density ($\mu W/cm^3$) 10-year lifetime**
Solar	Photovoltaic	15,000 $_{sunny}$ 150 $_{cloudy}$	15,000 $_{sunny}$ 150 $_{cloudy}$
Vibration	**Piezoelectric Electrostatic Electromagnetic**	**4-800**	**4-800**
Temperature Gradient	Thermoelectric	60 @ 5ºC gradient	60 @ 5ºC gradient
Radio Frequency @ 2.4 GHz [35]	Electromagnetic induction	400 @ 1 m 15.8 @ 5 m	400 @ 1 m 15.8 @ 5 m
Fluid Flow	Wind, Wave	air: 200-800 water: 500 mW/cm^3	-
Batteries (Lithium) (non-rechargeable)	Electrochemical	89	7
Batteries (Lithium) (rechargeable)	Electrochemical	13.7	0
Fuel Cells (methanol)	Electrochemical	560	56

The data shows that photovoltaic solar cells have higher power density compared to other ambient energy sources and long lifetime operation. However, performance of the cell is highly dependent on the environmental variations such as geographic location and indoor or outdoor usage. Hence, applications of these cells are limited. Further comparison of ambient energy sources and detailed information about the operation principles of transduction mechanisms of harvesters can be found in [7]. Vibration based energy harvesters are especially attractive among these sources due to abundance of vibration in the environment and clean and higher generated energy profile. The ambient vibrations can be observed at large variety of forms like human and vehicle motions, moving structures such as buildings and bridges, seismic noise, and acoustic noise. These vibration sources has a wide spectrum of frequency, however most of them are observed at low frequencies (<10 Hz). As a result of these low vibrations the power generated by vibration based energy harvesters is also low, making efficient system design challenging.

Basic principle of vibration-based energy harvesters is, with the relative movement of mechanical structures kinetic energy is converted to electrical energy. There are three different methods which are suggested in the literature for electrical energy generation from vibration-based energy harvesters; electrostatic (capacitive), piezoelectric, and electromagnetic (inductive) [9–12]. In electrostatic harvesters, the incoming vibration leads to change the distance between previously charged plates which changes the capacitance between them. Due to the basic equation between charge and voltage (Q=CV) the output voltage or charge variation is generated by keeping constant either charge or voltage, respectively. The structure of electrostatic energy harvesters is similar with gyroscope or accelerometer where usually they include an inertial mass with comb fingers. Figure 1.1 shows typical electrostatic energy harvester designs where in plane type energy harvesters are utilized to convert vibration in plane with the harvester to electrical energy and out-of-plane energy harvesters uses the vibrations which are perpendicular to the harvester plane.

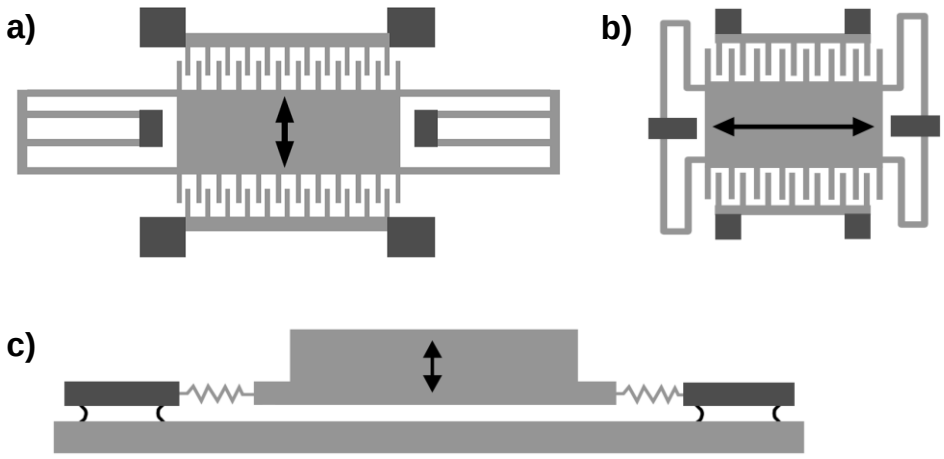


Figure 1.1: Typical electrostatic energy harvester designs, a) in-plane overlap, b) in-plane gap closing, c) out-of-plane gap closing converter.

In piezoelectric harvesters vibration leads to deformation of the piezoelectric material and due to generated strain and stress on the piezoelectric material a voltage change is observed at the piezoelectric terminals. Figure 1.2 presents a conventional piezoelectric energy harvester design where a piezoelectric layer is attached on a cantilever beam and one side of it is fixed on a base. When an external vibration is applied to the system the cantilever bends and a voltage difference is occurred at two different layers due to this bending. The tip mass is utilized to arrange the resonance frequency of the harvester.

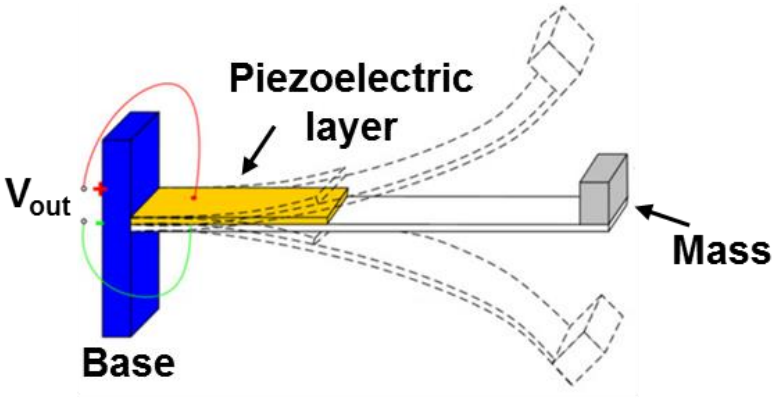


Figure 1.2: Conventional piezoelectric energy harvester design, a fixed-free cantilever beam with tipmass [13].

The average electrical power generated by a single piezoelectric layer on a fixed-free cantilever beam is analytically modeled by Lu *et al.* and can be given as:

$$\bar{P} = \frac{\omega^2 b^2 h^2 e_{31}^2 [\varphi(l_0) - \varphi(l_1)]^2}{8\left(1 + bL\varepsilon_{33}\frac{\omega R}{\Delta}\right)^2} R \tag{1.1}$$

where ω is the frequency of external vibration b and h are the width and thickness of the beam, L and Δ are length and thickness of piezoelectric layer, e_{31} is piezoelectric constant in 31 coupling direction, ε_{33} is dielectric constant, R is the load resistance connected to the harvester, and $\varphi(x,t)$ is flexibility of the beam, hence $[\varphi(l_0)\text{-}\varphi(l_1)]$ is the difference of bending slopes at both ends of the piezoelectric layer.

In electromagnetic energy harvesters, relative movement of a coil and a permanent magnet causes a magnetic field variation inside the coil and this result with an alternating voltage generation on the coil due to Faraday's law of induction. Electromagnetic energy harvesters are explained in detailed at section 1.2.

High level output voltages can be generated by piezoelectric and electrostatic harvesters however, most of the reported results are at high frequency applications. In literature, piezoelectric and electrostatic energy harvesters which show high performance at low frequency operations is also reported [13–16]. However, because of the high output impedance of these scavengers they need external impedance matching circuit which increases the complexity and power requirement of the system.

On the contrary, due to the permanent magnet used at the electromagnetic harvesters which acts like a proof mass, resonance frequency of the harvesters is at low vibration range (1-10 Hz). Moreover, output impedance of electromagnetic harvesters is low (at most in kΩ's range), implementation of them is much easier, and they have a simple structure. Different than electrostatic energy harvesters electromagnetic scavengers don't require external components like electrets. Although, they have such advantages, the peak value of induced voltage at electromagnetic harvesters is low at low vibration which leads to major challenges at the efficient interface electronic design.

1.2. Electromagnetic Energy Harvesters

In electromagnetic energy harvesters, the electrical energy generation principle is based on Faraday's law of induction. With the relative movement of a conducting coil and a permanent magnet the magnetic field enclosed by the coil is changing and a voltage is induced at the terminals of conductor. The induced voltage depends on rate of change of the flux and velocity. The flux change is highly proportional to the number of coil turns and specifications of magnets. Moreover, the whole system design, arrangement of magnet and coils, area enclosed by each coil turns has significant effects on the performance of the system.

$$\varepsilon(t) = -\frac{d\Phi}{dt} = -\frac{d(\sum_{i=1}^{n}(B \cdot A_i))}{dt} \tag{1.2}$$

where ε is the electromotive force induced voltage, Φ is the magnetic flux density, B is the magnetic field strength of the utilized magnets, Ai is the area enclosed by each coil turn, t is time, and n is the total number of coil turns. Schematic that illustrates the operation principle of electromagnetic energy harvesters is presented at Figure 1.3[17].

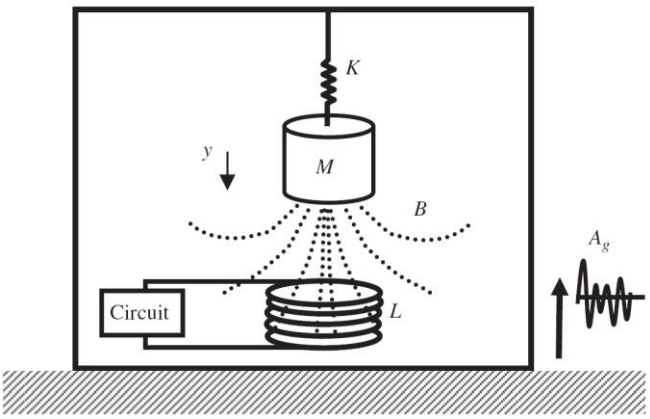


Figure 1.3: Electromagnetic energy harvester operation principle[17].

Previous works in our group show that simple structure of electromagnetic energy harvesters allows to optimize the harvester with macro model devices [18], [19]. With the implementation of macro model devices the effect of different parameters (like number of coil turns) on the generated voltage and power can be observed. Most of the

recently studied energy harvester modules have operation frequencies larger than 50 Hz which helps to generate more power. El-Hami *et al.* presents an electromagnetic energy harvester that generates maximum of 2208 μW/cm^3 AC power density. This power is obtained at 320 Hz which is the resonance frequency of the harvester [20]. The generator proposed by Ching *et al.* is a multimodal energy harvester with 1 cm^3 volume and generate maximum power of 830 μw for frequencies between 60 and 110 Hz [21]. Beeby *et al.* designed a electromagnetic energy harvester where coil of the harvester is mounted on a cantilever and optimize the magnet geometry accordingly. The harvester able to generate 306 μW/cm^3 power at 52 Hz external vibration [22].

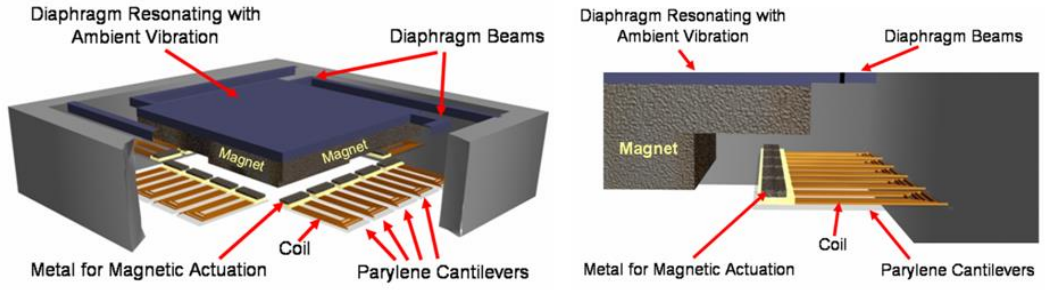


Figure 1.4: Frequency up-conversion based electromagnetic micro harvester [23].

Previously reported energy harvesters show that the generated power tends to decrease as the excitation frequency and volume of the devices decrease. However, the frequencies observed in the nature are lower than 10 Hz and it is desired to use these vibrations for powering the portable devices. Külah and Najafi proposed a novel method for up-converting the excitation frequency and improve the energy harvesting efficiency [24]. This technique is called as frequency up-conversion and based on magnetic pull force between a magnetic material and a permanent magnet. In the reported prototype the permanent magnet is placed on a diaphragm which is moving with the external vibration frequency and smaller magnetic materials are placed on cantilever beams which have larger resonance frequency. Operation frequency of the reported device is 1 Hz and it is able to generate 0.022 μW power with 2.3 cm^3 device volume. The micro model of the proposed system is also fabricated ad presented by Sarı *et al.* [23] (Figure 1.4). Beside this, another up-conversion method which is known as mechanical frequency up-conversion is demonstrated by our group [25]. This new technique helps to remove out the necessity of the extra magnet. The fabricated prototype generates 62.2 μW power at 10 Hz vibration frequency and volume of the device is 2.96 cm^3. Another frequency up-conversion device is reported by Galchev *et al.* where the permanent magnet used for power generation is placed on a diaphragm with a higher resonance frequency [26] (Figure 1.5). When a low frequency external vibration applied the inertial mass magnet vibrates and catches and release the small magnet on the diaphragm, hence a higher frequency output is obtained. The reported device gives 57 μW of maximum power at 2 Hz external vibration and the device volume is 43 cm^3.

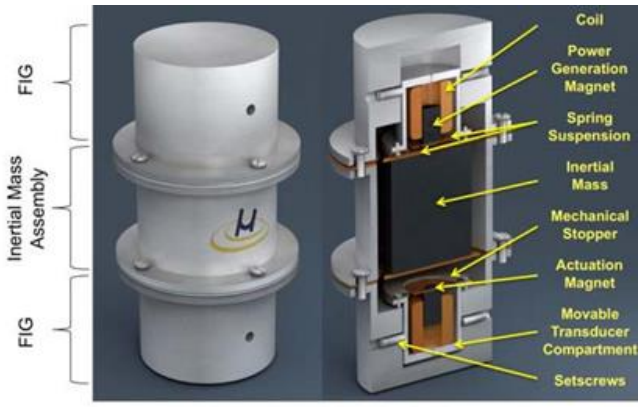


Figure 1.5: The frequency-increased generator design for low frequency harvesting [26].

The electromagnetic energy harvesters illustrated above don't consider the interface electronic parts of the system. The results include the AC power generated by the harvesters and calculated by utilizing the resistance of coil as the load resistance. While considering the usage of the generated power in real load applications they ignore the losses at conversion of the generated power into a usable form. However, the main problem of electromagnetic energy harvesters is at low vibration levels the generated voltage and power is considerably low where most of the case it is lower than turn on voltage of the transistors. However, in piezoelectric or electrostatic energy harvesters generated input voltage is higher and it is much easier to rectify it efficiently. Therefore, a low voltage and efficient interface electronics for electromagnetic energy harvesters is challenging.

1.3. Interface Electronics for Vibration-based Energy Harvesters

In this section, basic design approached of interface electronic circuits for all types of vibration based energy harvesters (piezoelectric, electrostatic, and electromagnetic) is going to be briefly explained. Figure 1.6 presents the common interface electronics circuit used for vibration based energy harvesters. Since the power generated from the vibration based transducers is alternating, first block of the circuit is utilized as an AC/DC power converter which converts the input AC signal to a DC voltage. After the voltage is converted into DC with the help of power processing block which contains post DC conversion like a DC-DC convert which step up the incoming DC voltage, and a voltage regulator which regulates the converted DC voltage. A super capacitor, a rechargeable battery or other storage devices can be used as the internal energy storage elements. Finally, a power management block is needed to decide whether the input conditions are sufficient for powering the load. If the input conditions are below the desired condition the power management circuit disconnects the connection to the load and charges the storage element up to chosen threshold. The basic concern at the design of each sub-block is to decrease the power consumption as low as possible. Hence, with the minimum power consumption of the interface electronics the efficiency of the system is maximized.

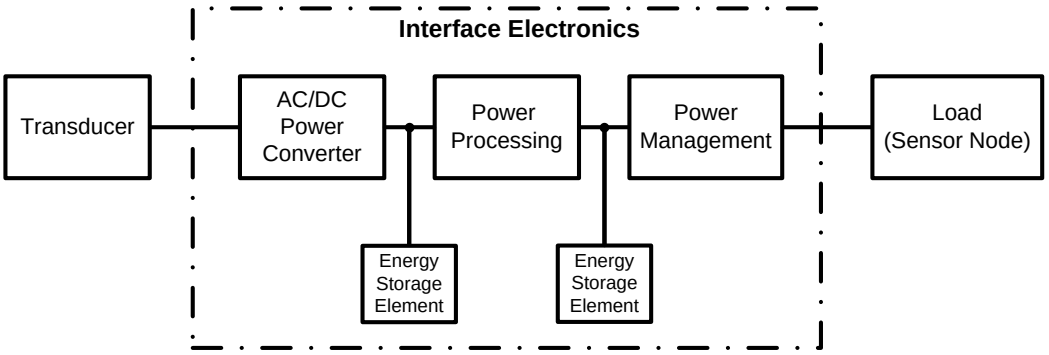


Figure 1.6: Basic interface electronic circuitry for vibration based energy harvesters.

1.3.1. Interface Electronics for Piezoelectric Energy Harvesters

Depending on the ambient vibration level and specifications of piezoelectric material piezoelectric energy harvesters can generate high output voltages. Many kinds of studies are reported as the interface electronics of these harvesters due to their high output voltages. However, there is a huge drawback at piezoelectric harvesters that they have relatively high output impedance (in the range of hundreds of kΩ's) which require extra circuits before connecting them to network. Figure 1.7 shows the electrical model of the piezoelectric energy harvester and the conventional voltage doubler used at the rectification of generated AC voltage [27]. The piezoelectric harvester is modeled as parallel connection of a current source, a capacitor, and the output resistance. The harvester should charge and discharge the internal capacitor (C_P) at each period; hence most of the generated current is lost at this operation due to large internal capacitance. The design presented in [27], uses a switch based voltage doubler which shorts the output terminals of energy harvester once in each cycle and provide higher charging rate for the internal capacitance. This results with higher charge transfer to the load instead of the internal capacitor, which significantly enhances performance of the output power conversion circuit.

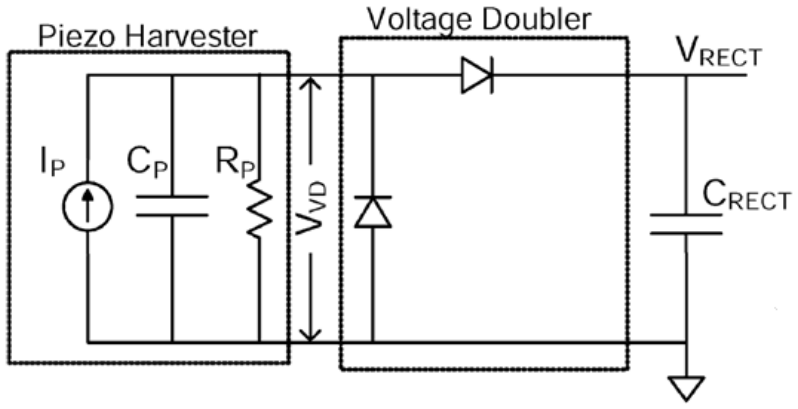


Figure 1.7: The electrical model of piezoelectric energy harvester, and the conventional voltage doubler circuit [27].

In [28], an adaptive piezoelectric energy harvesting circuit is proposed which provide continuous power flow from input to the load and maximize the power stored at the output storage element. The design use Pulse Width Modulated (PWM) signal to control the switch at the DC-DC converter part and discrete controller card is utilized to satisfy that signal. In [29], an interface circuit for piezoelectric harvesters that does not depend on the piezoelectric structure's parameters is presented. The major improvement of the design is, the inductor used at the DC-DC converter part of the design is minimized which highly improve the potential of the system to be integrated. In [30], a passive full-wave rectifier which utilizes the boot-strap technique is illustrated. The internal capacitor of the piezoelectric harvester is used as the storage element at half of the cycle like the one in voltage doubler. The proposed circuit gives about 66% maximum efficiency at 220 kΩ load resistance. The same study also includes synchronous rectifier which utilizes active diodes for rectification. The results show that active rectifier is a plausible solution for efficient rectification, where the proposed circuit reaches more than 85% efficiency for the load currents larger than 5 µA.

1.3.2. Interface Electronics for Electrostatic Energy Harvesters

In electrostatic energy harvesters capacitance change of two previously charged parallel plates leads to harvest energy. The change of capacitance between plates causes to generate voltage or current from the harvester. The primary problem of the electrostatic energy harvesters are, the generated voltage is extremely high (e.g. 150 V) which avoids them to be used with standard CMOS processes. To solve this problem a pre-charge stage is added after the energy harvester module which is used to charge an intermediate rechargeable battery (Figure 1.8). At this intermittent charger stage a highly tolerant components which highly increase cost of the system are used to transfer generated charge from the scavengers to a constant voltage battery. The reported interface circuits for electrostatic devices utilize a rechargeable battery as the storage element and reduce the generated voltage to the desired battery voltage for charging it [31–33].

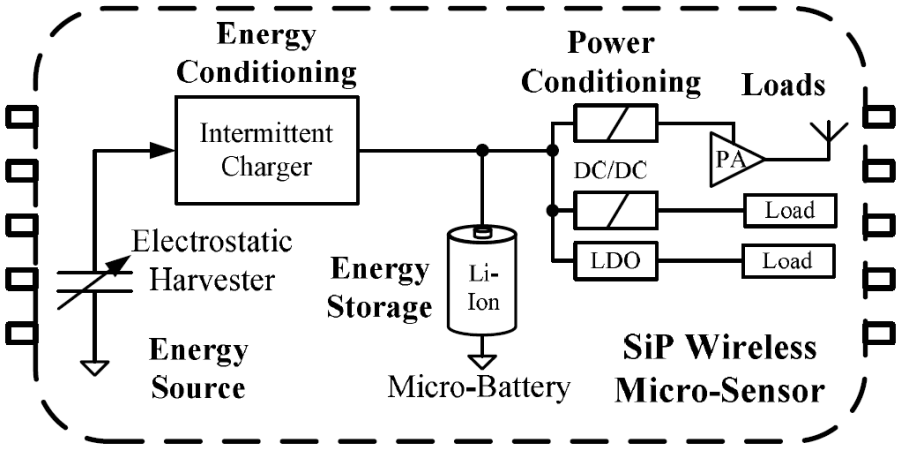


Figure 1.8: Typical interface electronics for electrostatic energy harvesters [33].

1.3.3. Interface Electronics for Electromagnetic Energy Harvesters

Most of the reported electromagnetic energy harvesting systems does not consider the interface electronics part or they only use a simple bridge rectifier as the power conversion element [2], [7]. Although related works in literature successfully design and optimize the mechanical transducer part of the system, the overall system performance of these systems is considerably low due to low efficiency power conversion circuit.

There are only a few works in the literature that presents a full system solution for electromagnetic energy harvesters by combining the transducers with the custom designed power conversion circuit. In [34], a full system solution for electromagnetic energy harvesting which uses a full-wave bridge rectifier and a PWM DC-DC converter as the power conversion circuit is proposed. Figure 1.9 shows the proposed interface circuit where the rectified DC voltage is boosted with a feed-forward and feed-back PWM boost converter and stored on a super capacitor. The operation frequency of the system is 42 Hz and the maximum power generated by the system is 4 mW. In addition to high frequency operation of the system, it also requires a 3.3 V power source for the PWM control signal generator. This external supply source increases the volume and cost of the system and add extra work load by requiring periodical replacement.

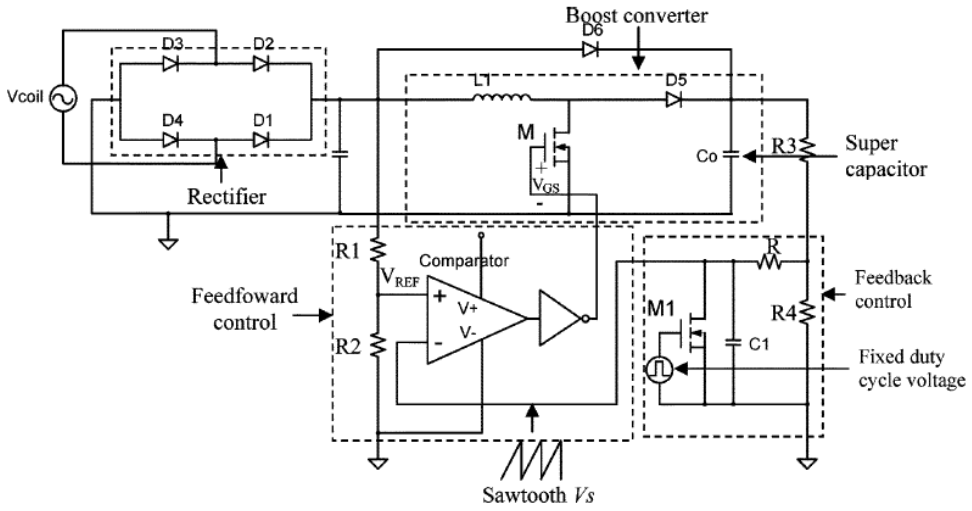


Figure 1.9: The PWM controlled power management circuit for electromagnetic energy harvesting applications [34].

In [35], a conventional Cockroft-Walton multiplier is used to rectify and boost the input AC signal generated by the electromagnetic energy harvester. The converted DC voltage then stored on a capacitor and with the help of a hysteresis switch which is used as a power management circuit; the stored charge is periodically transferred to a load. The ambient frequency applied to the harvester is 2 Hz but the Frequency-Increased Generation technique is used to step-up the frequency. Like the previous example the circuit has low power conversion efficiency which yields lower generated output power density.

The state-of-the-art electromagnetic energy harvesting systems mostly occupy large area and have considerably low power output due to low efficiency interface electronics. Besides, the operation frequency of the previously reported works is kept higher than ambient vibrations due to the high resonance frequency of the harvesters. There is an absence at the electromagnetic energy harvesting systems that requires a combination of harvester with a fully-integrated (low volume) and highly efficient power conversion circuit that converts low AC voltages with low power dissipation from low frequency vibrations.

1.4. Objective of the Thesis

The aim of this thesis is to design and implement a low voltage, low power and fully integrated interface electronics for vibration-based electromagnetic energy harvester especially with low input power. A comprehensive list of objectives of this thesis is as follow:

1. Study and specification of the blocks required for the high efficiency power conversion circuit for vibration-based electromagnetic energy harvesters.

2. Design and implementation of fully-integrated and battery-free interface electronics with different types of rectifiers and a DC-DC converter block. The specified rectifier converts the low AC voltages generated by the electromagnetic energy harvesters to DC with a fully-self powered topology which does not need any external battery and has high power conversion efficiency. The DC-DC converter block efficiently boost and stabilize the rectified voltage to 1 V DC voltage.

3. Implement a test platform for the fabricated interface electronics and integrate it with an in-house electromagnetic energy harvester module. Test the optimized system to realize an autonomous system that is able to harvest energy under low frequency vibrations and convert it to a usable form that generates at least 1 μW output power.

4. Discover the problems encountered at the fabricated chip and identify reasons of these problems. After verification of the problems, decide possible solutions to overcome these problems and prepare the circuit for error free fabrication.

1.5. Outline of the Thesis

The remaining part of the thesis includes 4 chapters. Chapter 2 describes the theory and design of all of the required sub-blocks utilized at an interface circuit of vibration based energy harvesters. The literature review of each block with state-of-the-art examples is presented in this chapter.

Chapter 3 introduces the design and simulation results of the fully-integrated and battery free interface electronics for low voltage electromagnetic energy harvester, which was designed in TSMC 90 nm CMOS technology. The theory of each of the blocks utilized in the designed system is explained in detailed in this chapter and design considerations for these blocks are also given.

Chapter 4 gives the experimental results obtained from the fabricated circuit in TSMC 90 nm technology and gives the comparison of the fully integrated and self-powered rectifier topology with a state-of-the-art rectifier which was implemented on the same chip. The operation voltage of the rectifier is the lowest achieved value among the self-powered and fully integrated circuit. The fully-integrated structure of the overall circuit is one of the main considerations of the system. The performance of the circuit is also observed with an electromagnetic energy harvester and results are given in this chapter. The problems encountered at the fabricated chip are also defined and possible solutions of them are given.

Chapter 5 finalizes the thesis by summarizing the achievements obtained at this work and outlines possible directions for future works on this topic.

CHAPTER 2

INTERFACE ELECTRONICS FOR ENERGY HARVESTERS

The main purpose of energy harvesting systems is to utilize the ambient energy sources to power an applicable load like a sensor node. These nodes generally require DC supply, however the power generated by vibration based energy harvesters is alternating (AC). Hence, an interface circuit is required to convert the generated AC signal into a usable DC voltage. This requirement makes interface electronics one of the fundamental challenges behind the power harvesting systems. Although the power losses of the power converter are a big concern at low power levels, this issue is not considered at most of the reported studies. Most of the reported energy harvesting system with a rectifying interface electronics are designed for piezoelectric harvesters because of the high output voltage at piezoelectric energy harvesters [27–30]. On the other hand, there are some good examples in the literature which gives full system solution for electromagnetic energy harvesters [34], [35]. However, the power conversion efficiency of these systems is considerably low due to the losses at the conventional passive diodes utilized at the rectification.

This chapter describes the operation principle and gives the literature review of all the necessary sub-blocks of the interface circuits for vibration-based energy harvester. Section 2.1 explains the overall block diagram of the system discussed in this chapter by introducing the action of each block and explaining relation of the blocks. In section 2.2, the passive and active rectifiers which are used for AC to DC converters are examined and state-of-the-art rectifiers proposed in the literature for low power applications are illustrated. Section 2.3 gives brief information about different types of DC-DC converters and explains design requirements of on-chip and low voltage interface electronics for energy harvesting applications. Besides, basic theory and some state-of-the-art examples of charge pump circuits which are significant blocks for on-chip DC-DC converters are explained in this section. Section 2.4 explains the concept behind the voltage regulation and conventional voltage regulator circuits. It also introduces voltage regulator designs for ultra-low power applications. Section 2.5 describes necessity of the on-chip power management circuits in low power energy harvesting applications. Finally, Section 2.6 contains a summary of this chapter.

2.1. Overall Block Diagram of the System

Figure 2.1 shows the overall block diagram of a vibration-based energy harvesting system including the detailed illustration of sub-blocks of the interface electronics.

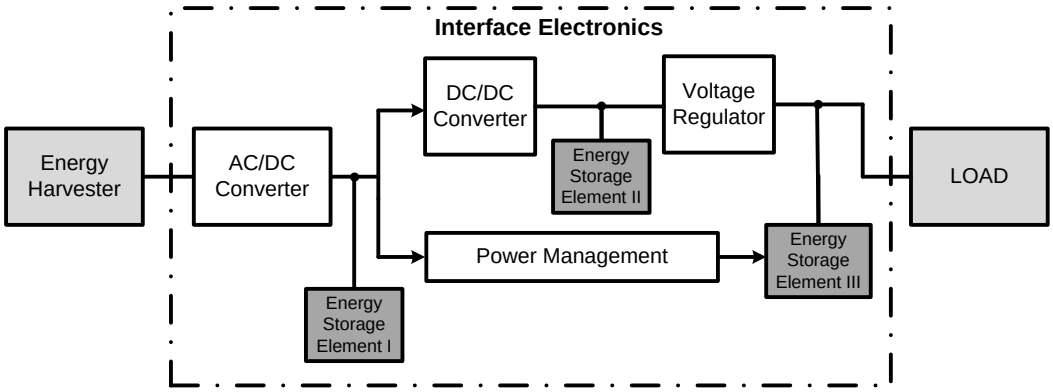


Figure 2.1: Overall block diagram of the interface electronics for vibration-based energy harvesters

The signal generated by the vibration-based energy harvesters is alternating; hence first block of the system is an AC/DC converter. This block converts the input AC signal into DC and stores it on an energy storage element like a capacitor. The second block of the system is a DC/DC converter that shifts level of the rectified DC voltage where operation and necessity of this circuit highly depends on level of the input AC signal. At low mechanical excitations, the input voltage generated from the electromagnetic energy harvesters is also low, thus the DC/DC converter is usually used to boost the rectified voltage at low frequency electromagnetic energy harvesting systems. The energy storage element II stores the converted DC voltage at the output of the DC-DC converter. Finally, a voltage regulator block is used to stabilize the output voltage that is delivered to the load. The regulator removes the output voltage variation with respect to input excitation and permanently stores the desired output voltage on an even larger storage element such as a super capacitor. Since the generated input power changes according to excitation conditions, a power management circuit is need to cut the power to the load whenever the input is not able to supply sufficient power.

2.2. The AC/DC Converters

The harvested signal from the vibration based energy harvesters is AC. Hence, the main block of the AC/DC converters is a rectifier which is used to rectify the alternating AC voltage or current and charge an output capacitor with a DC voltage. The rectifiers can be divided into two main types as passive and active rectifiers. Passive rectifiers are generally composed of half-wave or full-wave diode bridge rectifiers. However, voltage drop and power dissipation of the used passive diodes become a significant concern at low voltage and low power energy harvesting applications. Hence, to enhance performance of these converters, either special semiconductor technologies which include low threshold voltage transistors can be used or different circuit techniques may

be applied at standard technologies. On the other hand, performance of the active diodes is similar with an ideal diode: they pass the current only in one way and have very low voltage drop. Therefore, in low voltage applications using an active diode may be much more beneficial compared to passive rectifiers. But, the active diodes need an external power source to operate. The power requirement of the active diode may also be supplied from the input; however a pre-charged power source is still necessary for successful operation. In the next sections detailed information about the passive and active rectifiers is introduced.

2.2.1. Passive Rectifiers

The operation principle of passive rectifiers depends on a simple diode operation where no external source is needed. At on-chip IC design technologies, diode connected transistors are utilized as the diodes. The simplest passive rectifier is a half-wave rectifier which passes the current at positive voltages and loses the negative input signals. The improved version of this rectifier is a simple full-wave bridge rectifier (FWBR) which is composed of four diodes and uses whole input period for rectification (Figure 2.2 a). In [36], a piezoelectric energy harvesting system which uses Schottky diodes to eliminate the high voltage drop and low power conversion efficiency is presented. Although Schottky diodes have low voltage drop, their high reverse current prevents to have high power conversion efficiency.

In [37], the gate cross coupled rectifier (GCCR) which is the improved version of the full-wave bridge rectifier is presented. The proposed structure is applied for inductive RF energy harvesters and proved to improve voltage drop. Figure 2.2 shows schematics of the FWBR and GCCR structures. To decrease the voltage drop, in GCCR circuit two diode connected NMOS transistors at the bottom of the FWBR is replaced with two cross-connected NMOS transistors. Hence, the PMOS diode-connected transistor pair at the upper part of the circuit rectifies the input with threshold voltage drop (V_{TH}) and the cross-connected pair passes the current with drain-to-source voltage drop. Detailed explanation of the GCCR circuit is done at Section 3.2.

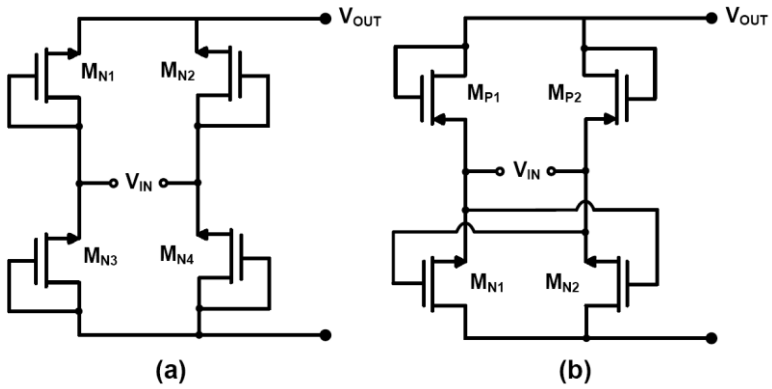


Figure 2.2: Schematic of the (a) full-wave bridge rectifier (FWBR), and (b) gate cross coupled rectifier (GCCR).

Figure 2.3 shows a passive full-wave rectifier which enhances the power conversion efficiency by decreasing the voltage drop across the rectifying transistors [38]. The proposed architecture includes a cross coupled transistor pair (M_1 and M_2) like the one in GCCR; however the diode connected transistor pair is replaced with modified diodes which are at the bottom part of the circuit. Operation principle of the modified rectifying diodes is as follows: when the negative input terminal falls below ground the M_8 transistor starts conduction and shorts the gate of M_6 transistor to negative input terminal which forces M_6 to turn ON. When M_6 is turned ON, gate of M_4 is connected to positive input terminal and it starts to pass the current rectified by M_1. At the same time, since the gate of M_9 is connected to positive input terminal it starts conduction and connects gate of M_9 to ground and turns it OFF. For negative input peaks vice versa operation occurs at modified diodes. Therefore, output voltage drop is decreased to two drain-to-source voltage instead of one threshold and one drain-to-source voltage in the case of GCCR. The output voltage of the proposed circuit at positive peaks can be expressed as:

$$V_{Out} = V_{in} - \left(V_{DS,M_1} + V_{DS,M_4}\right) \tag{2.1}$$

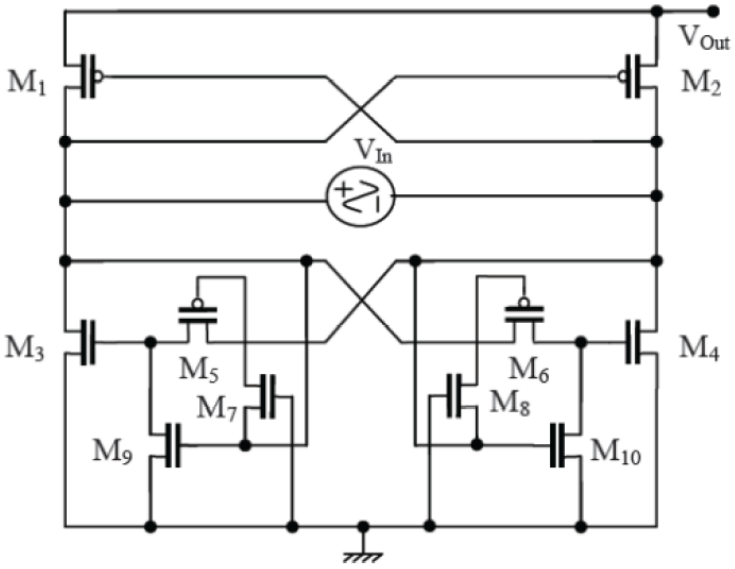


Figure 2.3: The proposed modified passive rectifier circuit in [38].

Performance of the design is good at high input voltage peaks; the power conversion efficiency of the circuit achieves more than 90% for high input voltages. However, at low voltages (< 2 V), the proposed circuit shows very low performance due to the turn ON process of control transistors (M_5 – M_{10}). At very low input peak voltages (lower than V_{TH}) the control signals cannot be turned ON, hence the proposed circuit is not able to operate.

Figure 2.4 presents the design proposed in [39] which uses the boot-strap rectification (BSR) technique to decrease the voltage drop of the passive diodes and enhance the power conversion efficiency of the system. In the design, a cross coupled transistor pair (M_{N1}-M_{N2}) is utilized to pass the current rectified by the boot-strap connected modified

diodes. The modified diode (at left part of the circuit) is composed of boot-strap transistors M_{P1}, M_{P2}, and M_{P5} and a boot-strap on-chip capacitor, C_{BS1}. Furthermore, bulk regulation transistors (M_{PB1}-M_{PB8}) are connected to bulks of the PMOS transistors M_{P1}-M_{P4}, to prevent the latch-up at PMOS transistors. As a result, the boot-strap technique helps to decrease the threshold voltage drop at the rectifying diodes to the voltage difference V_{THP5}-V_{THP2}. Hence, the output voltage of the rectifier can be expressed as:

$$V_{Out} = V_{in} - (|V_{THP5}| - |V_{THP2}|) - V_{DSN2} \tag{2.2}$$

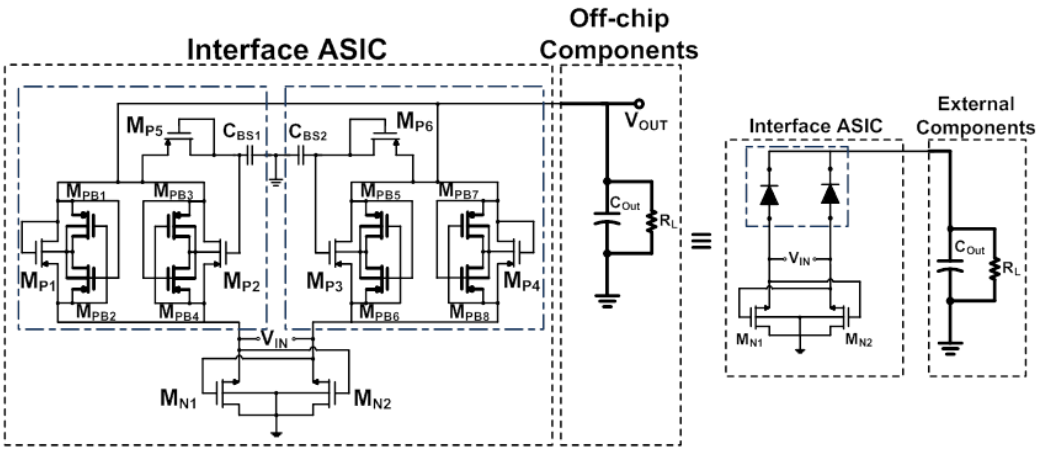


Figure 2.4: Schematic of the boot-strap rectifier (BSR) presented in [39].

According to [39], the proposed rectifier achieves 75% power conversion efficiency at low vibration EM energy harvesting applications which yields to low input voltages. However, performance of the circuit is still not good at voltages below 1 V.

The reported studies show that passive rectifiers are suitable for on-chip rectification; however, it is hard to achieve low voltage operation with these rectifiers. Therefore, works on low voltage (<1 V) and high efficiency interface circuits are inadequate in literature.

2.2.2. Active Rectifiers

Active rectifier is one of the best solutions for the problem encountered from voltage drop at the rectifying diodes. Active diodes are simply composed of a pass transistor and a comparator circuit which turn ON and OFF the pass transistor according to the input. The active rectifiers act like an ideal diode and charge the output capacitor whenever the input voltage is higher than the output voltage. Active rectifiers can satisfy much higher power conversion efficiency, due to the much lower drop-out voltage of active diodes. However, supply requirement of these circuits is a major drawback in the design of fully self-powered systems.

In [30], an improved version of the full-wave voltage doubler circuit, which is explained in Section 1.3.1, is proposed. The diodes utilized in the circuit are replaced with active diodes and with this modification more than 90% power conversion efficiency is achieved for load current more than 4 µA and the power dissipated by the active parts is around 165 nW. Furthermore, to enhance the boosting performance of the rectifier, more efforts have been done on optimization of designed comparators and on switching schemes. In [40], an active AC/DC doubling circuit which can generate output voltages as high as peak-to-peak voltage of the input signal is presented (Figure 2.5). The circuit uses two active diodes to rectify the positive and negative portions of the input signal and generate dual rail positive and negative output voltages. The circuit is able to rectify input peak voltages as low as 0.2 V with more than 80% efficiency. However both of the designs presented in [30] and [40] use external power source to supply the power needed by the active diodes.

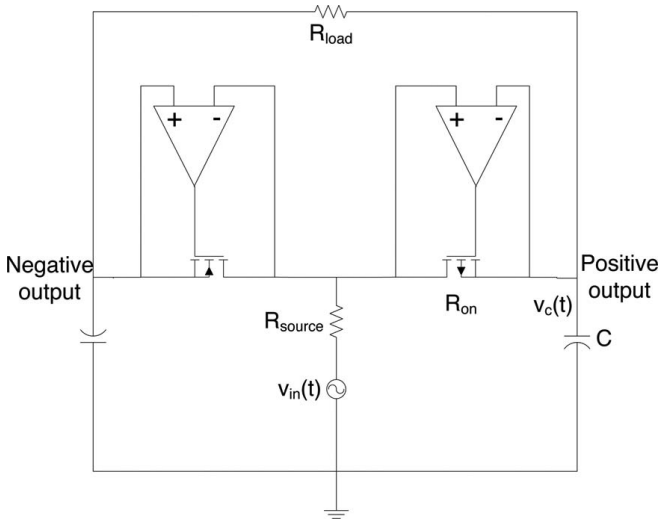
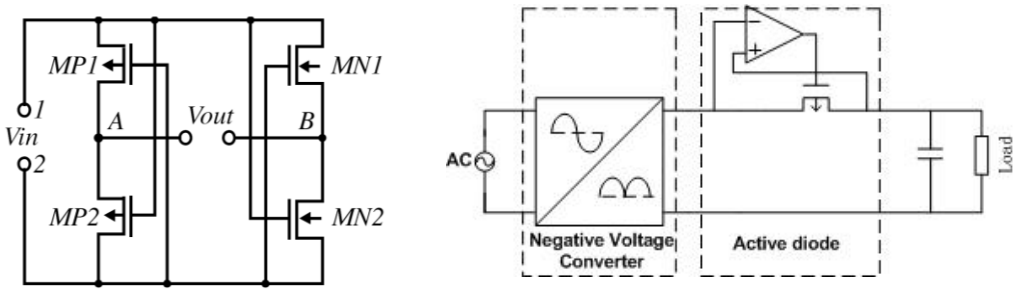


Figure 2.5: The voltage doubler circuit using active diodes proposed in [40].

The power dissipated by the active rectifiers is also affecting the power conversion efficiency of the overall system; hence, the power consumption of these components must be kept as low as possible. In conventional full-wave rectifiers, at least two rectifying diodes are used and this leads to consume two times larger comparator power. In [41], a full-wave rectifier which uses only single active diode is used. In the proposed circuit, which is shown at Figure 2.6, negative portions of the input voltage is converted to positive voltages and the rectification satisfied with only one diode. Furthermore, the comparator circuit which is utilized to control the switch is designed such that its supply is coming from the input. Hence, the external power supply requirement of the circuit is eliminated. Although around 87% power conversion efficiency is achieved by the circuit the minimum operation voltage of the circuit is depicted as 0.7 V.



(a) (b)

Figure 2.6: Schematic of the a) negative voltage converter (NVC) and b) full-wave rectifier with NVC and an active diode [41].

Figure 2.7 shows a fully self-powered highly efficient active rectifier circuit which was designed in 0.35 µm CMOS technology [42]. The circuit uses peak-to-peak voltage of the input signal and generates dual rail outputs with two distinct active diodes which are utilized in active rectifier part of the circuit. A bias generator circuit is implemented by using SMD components to satisfy the external power requirement of the active diodes. In the designed system two separate coils are used to for the active rectifier and bias generator circuit. The circuit is able to operate low in put frequencies (< 10 Hz) and has larger than 81% power conversion efficiency for a wide range of load current (0-42 µA). However, the utilized SMD components limit the minimum operation voltage of the circuit and prevent a fully-integrated system solution. Besides, the utilized second coil also generates a complexity at the design. An improved version with fully-integrated and ultra-low voltage rectifier topology is presented in this work and explained in Section 3.2.

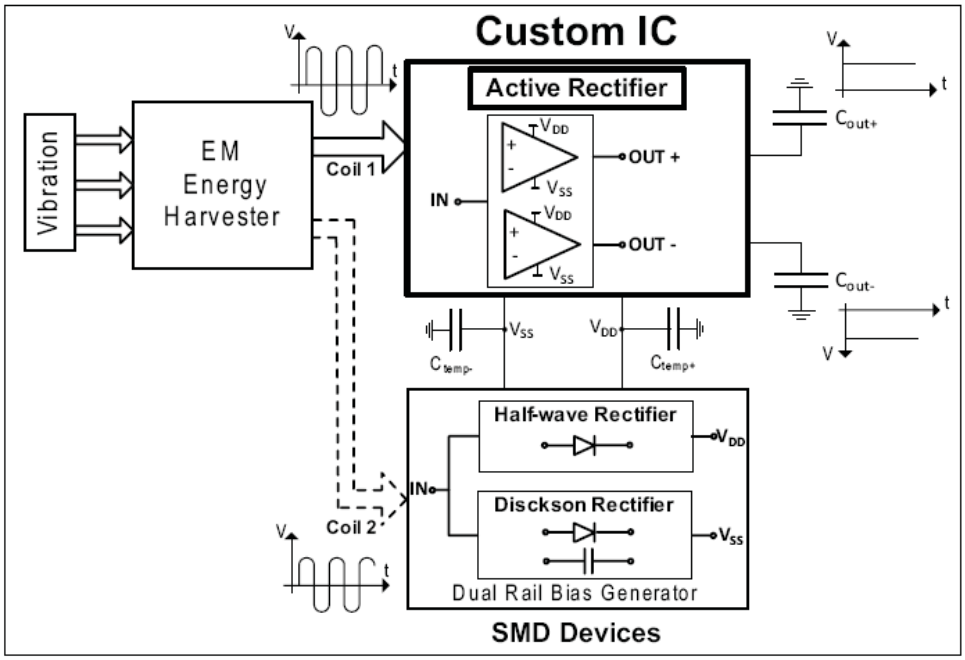


Figure 2.7: Self-powered active rectifier circuit with dual rail outputs [42].

2.3. DC-DC Converters

DC-DC converters are used as the second stage of the interface electronics for energy harvesting applications. These blocks are used to shift level of the rectified DC voltage by either boosting (step-up) or bucking (step-down) it according to the level of the rectified voltage. There are many switching converters in literature; but, only a few of them are designed for efficient operation at low power applications. Inductor based conventional DC-DC converters are not appropriate for low power energy harvesting applications since they have high power losses. Moreover, it is nearly impossible to integrate the proper inductors on-chip for such applications. On the other hand, charge-pump based DC-DC converters are much more suitable at low power and low voltage application and can be easily integrated since they don't include inductors. The power conversion efficiency of low power (about 20 µW) DC-DC converters are typically above 60% [43–47].

2.3.1. Switching DC-DC Converters

There are mainly two types of switching DC-DC converters: inductive-based and capacitive-based converters. The inductive-based converters use a modulation technique to charge the inductor and boost the DC voltage on the output capacitor by transferring the current on the inductor to it. However, at capacitive switching converters a switching scheme which is satisfying the charge transfer between the capacitors is used to shift the level of the DC voltage.

2.3.1.1. Inductive-Based Switching Converters

The inductive-based switching converters use the charge stored on the inductor to boost the output voltage. Output voltage of these converters is regulated to a desired value with the help of a Pulse Width Modulation (PWM) technique which is illustrated in Figure 2.8. The operation principle of the boost switching regulators can be explained as follows: when the switch M is ON, the inductor L1 is charged via the input source. After the switch M turned OFF, the charge stored on the inductor is transferred to the storage capacitor and boost the output voltage. The regulation of the output voltage satisfied with the comparison of a feedback coming from the input voltage (V_{REF}) and a sawtooth waveform. When the sawtooth voltage exceeds V_{REF} the gate voltage of the switch M is triggered and turns ON the switch, similarly when it falls below, the switch is turned OFF. By adjusting the duty cycle of the gate control signal (PWM) the output voltage is regulated to a desired value. The illustrated converter is able to drive load currents higher than a few micro-amperes up to amperes. The most usual application of such type of converters is in high current LED flash drives. In order to satisfy high efficiency at the desired converter the required inductor must be kept in mH ranges. However, such a high sized inductor is not suitable to be fabricated as on-chip. Typical value of on-chip inductors is in the range of 100 nH to 1 µH [44].

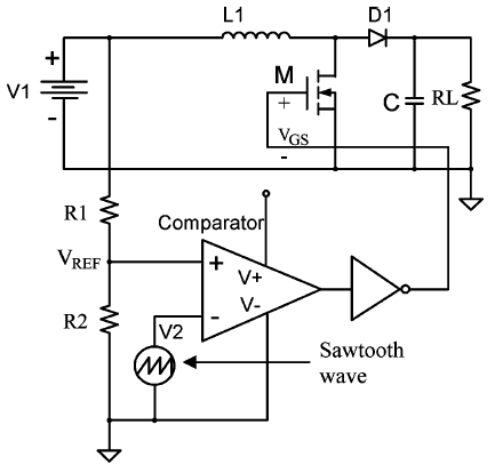


Figure 2.8: Schematic of the DC-DC PWM switching converter using feedforward control [34].

2.3.1.2. Capacitive-Based Switching Converters

The capacitive-based switching converters' operation principle is also based on charge transfer as the one in inductive-based DC-DC converters. However, for this case, charge transfer occurs between capacitors and generates the required output voltage according to this issue. Similar with the inductive-based converters, they can either boost or buck the input voltage. The integration capability of the switched capacitor circuit at a standard CMOS technology is their major advantage compared to inductive based converters. These converters are also proper for output currents within the range from a few tens of micro-amperes to a few hundred milli-amperes.

The basic operation principle of capacitive-based switching converters can be explained by using the schematic of the switched capacitor DC-DC voltage doubler shown at Figure 2.9. The operation can be divided into two parts: at first phase switches shown with "1" are ON and the others are left OFF hence the input voltage (V_{DD}) charges the capacitor C_1. At the second phase switch "1"s are turned OFF and switch 2s are turned ON and charge stored on C_1 is transferred to output capacitor which results with doubling the output voltage.

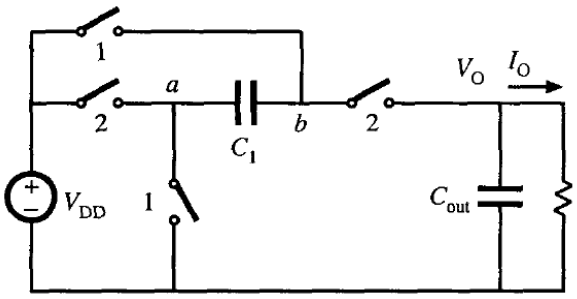


Figure 2.9: Switched capacitor DC-DC voltage doubler [48].

The switched capacitor DC-DC converter proposed in [49] includes a 4-stage DC-DC converter (Figure 2.10). At the first phase of the clock all of the intermediate capacitors are connected in parallel and charge with the help of the input voltage V_{rect}. When the clock is changed to the second phase the capacitors are connected in series and transfer the charge stored on them to output capacitor which generates nearly $4xV_{rect}$ as the output. The proposed circuit is able to give 1 V output voltage for 25 µW input power and for 2.5 mW input power it gives about 0.9 V output voltage with 162 nW output power for 10% duty cycle of the clocks (stays high only at 10% of the period). Although the circuit finely boosts the input voltage the efficiency of the circuit is very low.

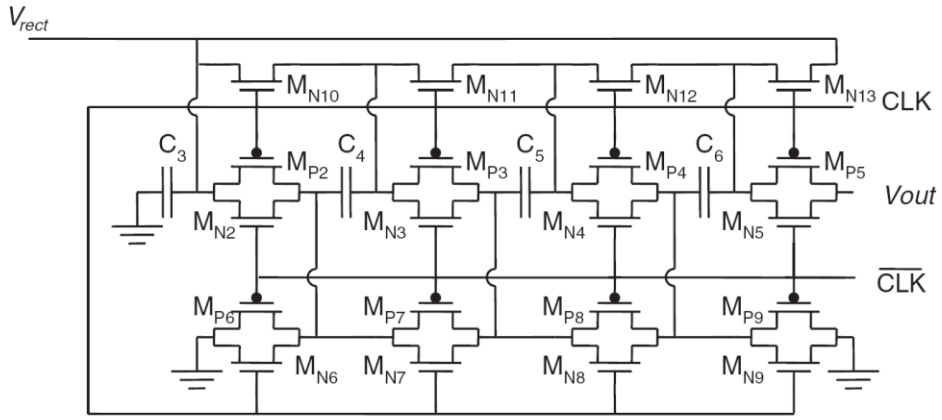


Figure 2.10: 4-stage switched capacitor DC-DC converter [49].

2.3.2. Charge-pump DC-DC Converters

The charge-pump circuits can be considered as a different type of a switched capacitor DC-DC converter, their basic principle is continuous charge transfer between input and output with the help of non-overlapping clock phases. Similar with the switched capacitor circuits, their main advantage is possibility of on-chip integration which gives opportunity to design a fully integrated interface circuit for low voltage vibration based energy harvesters.

In the literature there are different types of charge-pumps. Figure 2.11 shows the first charge-pump topology which is proposed by John F. Dickson and is named as Dickson charge-pump [50]. In the proposed circuit the charge-pump is pumping the charge to the next stage which boosts the voltage at the next stage two times of the previous stage. Due to the utilized diodes which cause voltage drops and power losses, efficiency of the Dickson charge-pump is low. Dickson also showed that the output current is independent of the number of stages for ideal case [51]:

$$I_{Out} = f \times (C_c + C_s) \times V_L \tag{2.3}$$

where, f is the frequency of clock, C_c is the intentional coupling capacitor capacitance, C_s is the stray capacitance per node, and V_L is the voltage by which capacitors charged and discharged.

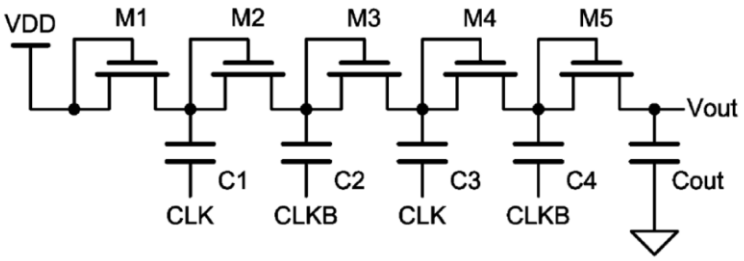


Figure 2.11: The conventional 4 stage Dickson charge-pump [50].

Output voltage of the charge pump depends on many parameters as:

$$V_{Out} = V_{in} + N\left[\left(\frac{C_c}{C_c + C_s}\right) \cdot V_{CLK} - V_{TH}\right] - V_{TH} - N \cdot \left(\frac{I_{Out}}{(C_c + C_s) \cdot f}\right) \tag{2.4}$$

where N is the number of stages, V_{CLK} is the clock amplitude, and V_{TH} is the forward bias diode voltage. The voltage swing at each stage of a Dickson charge-pump is:

$$\Delta V = \left(\frac{C_c}{C_c + C_s}\right) \cdot V_{CLK} - \left(\frac{I_{Out}}{(C_c + C_s) \cdot f}\right) \tag{2.5}$$

Hence, by considering the given equation the full term can be approximated as V_{CLK}, when C_c is chosen significantly larger than C_s and I_{Out} is small. The main problem of Dickson charge pump is ground body bias. When bulk of the NMOS transistors grounded at higher stages body effect at the threshold voltage significantly increase the voltage drop at diodes. The voltage gain stage N can be expressed as:

$$Voltage\ gain = \Delta V - V_{TH}(N) \tag{2.6}$$

where $V_{TH}(N)$is the threshold voltage of MOSFET at stage N. Therefore, the output voltage for K stage Dickson charge-pump is expressed as:

$$V_{Out} = \sum_{N=1}^{K} \left(V_{in} - V_{TH}(N)\right) \tag{2.7}$$

The high voltage drop and high power losses of the Dickson charge-pump prevent its usage in low voltage applications. In the literature there exist many studies which have focused on boosting the performance of the charge-pump circuit for low voltage applications. The boosted pump clock scheme, a Charge-Transfer-Switch (CTS) scheme, the 4-phase charge-pump utilizing the 4-phase clocking phase, and several modified version of these topologies are included in the literature which try to eliminates V_{TH} dependent problems and enhance the efficiency of the circuits operating below 2.5 V supply voltages. In [52], different types of charge-pumps and their design consideration is discussed in a detailed manner.

In the conventional 4-phase charge pumps, gate to source voltage of the transistors is increased with the help of special 4-phase clocks. Hence, losses due to threshold voltage drop decreases and the pumping gain is enhanced. Moreover, for further improvement, using a 2 times or 4 times boosted clock signal is an easy way to increase the efficiency and the output voltage.

In the CTS scheme, each stage of the charge pump includes an external pass transistor, where gate of this transistor is controlled by the next stage. Since consecutive stages are at different phases control of these pass transistors is much more easy and beneficial. The advantages and disadvantages of different charge pump topologies is also described in [52].

An inductor-based charge pump circuit which boosts the clock signal with the help of inductor is presented in [53]. The circuit is able to operate at very low voltages down to 0.2 V. Structure of the charge pump is same with the previous examples; however, it includes a pass transistor in series with an inductor which is connected to input voltage (V_{DD}) (Figure 2.12). The boosting operation can be explained as follow: when the clock changes its state, the current on the inductor prevents instant change of the the charge pump. Therefore depending on the value of inductance voltage levels higher than input voltage observed. Although the proposed circuit finely boosts the input voltage an off-chip inductor is needed for operation.

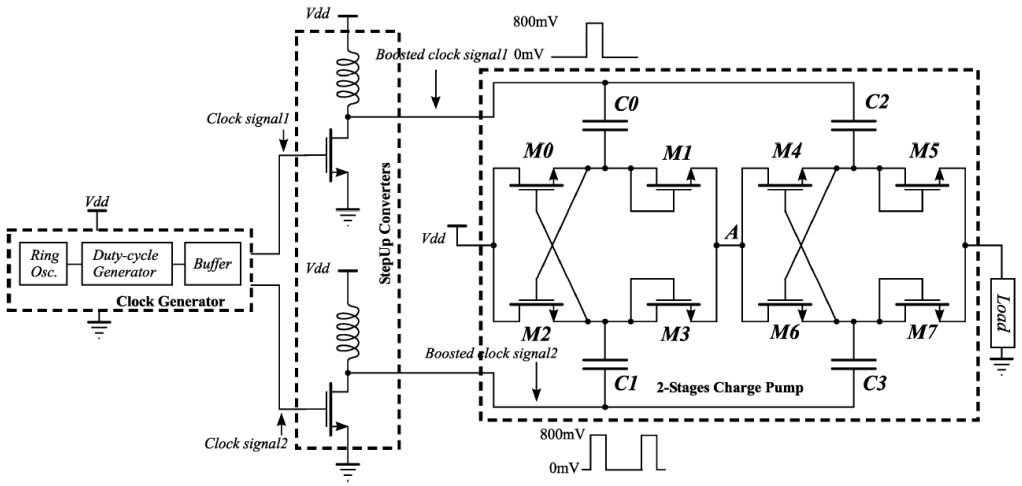


Figure 2.12: Inductor based charge pump structure presented in [53].

The charge pump circuits which uses NMOS transistors has lower conversion efficiency due to the body effect at the threshold voltage of NMOS transistors. To overcome this problem a 4 phase charge pump circuit which utilize PMOS transistors as the switches is designed in [54]. The proposed 4 stage charge pump circuit has 70% power conversion efficiency for 15 µA load current. The 2 stage charge pump circuit gives about 3.55 V output voltage for 1.8 V input voltage where the ideal value of the output is 3.6 V.

Figure 2.13 presents a new charge pump design approach which uses CMOS cross-connected transistors to degrade the effect of threshold voltage [55]. In the proposed design, the threshold voltage drop of the diode connected transistors is replaced with drain-to-source voltage of an NMOS and a PMOS transistor, which is typically much lower than V_{TH}. Moreover, since the voltage drop at the output is not directly related with the V_{TH}, the body effect problem at higher stages is also solved. The circuit is designed and implemented in 0.35 µm CMOS process and results show remarkable improvement at the output voltage compared to previously reported charge pump circuits. A modified and optimized version of this design has been implemented in 90 nm CMOS process and explained in Section 3.3.

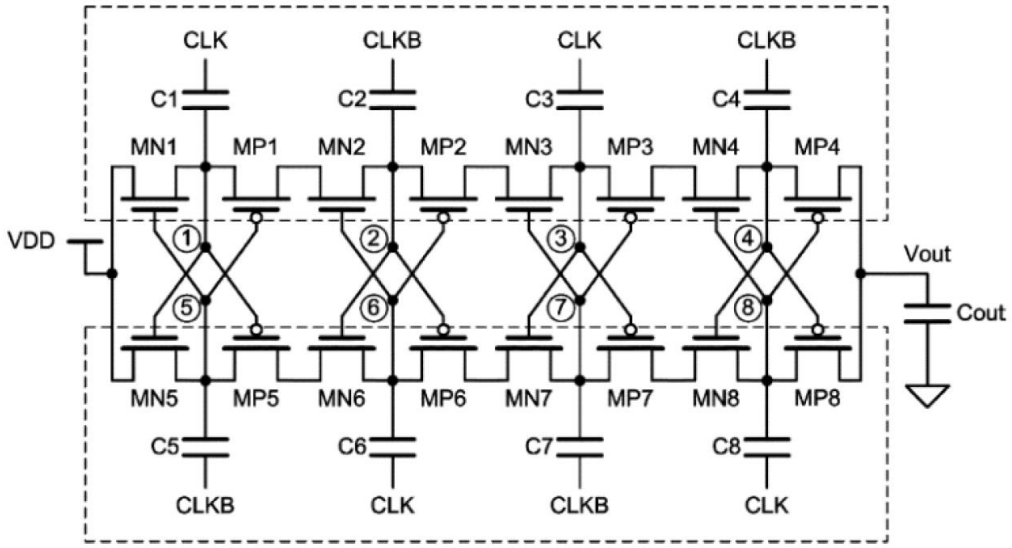


Figure 2.13: The cross-connected charge-pump circuit proposed in [55].

2.4. Voltage Regulators

The voltage regulator block is needed to stabilize the output voltage at a desired value so that battery like behavior is retired. There are different voltage regulation strategies to be discussed in this section. While considering the regulation strategies for energy harvesting application the key parameter is the power dissipation of the block. In other words, the quiescent power dissipated by the voltage reference and the regulator must be much lower than harvested ambient power. Therefore, many kind of conventional voltage regulator blocks which requires more than hundreds of micro watts power are not appropriate and not discussed here.

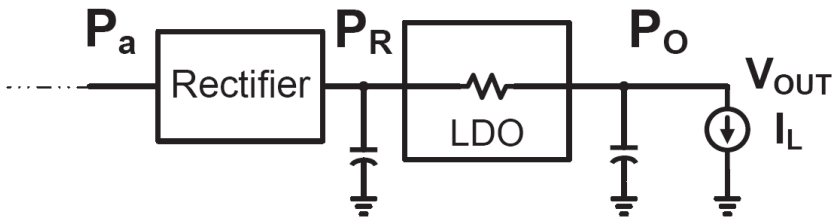
2.4.1. Linear Voltage Regulators

The simplest and most well-known voltage regulator structure is a DC-DC linear voltage regulator, which regulates the input voltages higher than the desired output voltage. The regulation strategy of the circuit is based on dissipating the dropout voltage (voltage

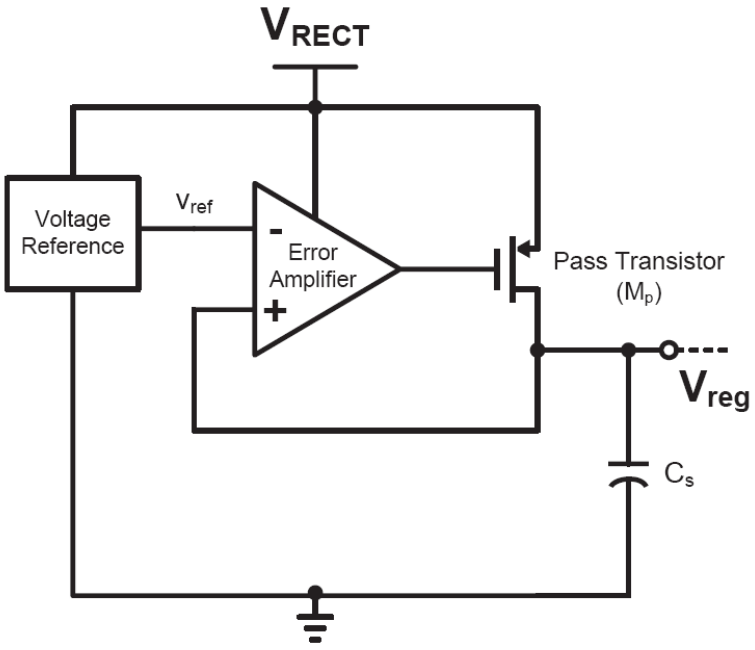
difference between input and output) as heat on a pass transistor (Figure 2.14 a). This internal power loss on the pass transistor causes to make the linear voltage regulator the most inefficient regulator for the input voltages much higher than required output voltage. The linear voltage regulators are also known as low dropout (LDO) regulators due to the voltage drop on the pass transistor. Figure 2.14 (b) simple summaries the operation principle of the low dropout (LDO) voltage regulator, where the comparator (error amplifier) compares the output voltage with a reference voltage generated from the input and control the pass transistor and charge the output capacitor into the required output voltage. The voltage gain of the linear regulator is:

$$LDO\ Voltage\ Gain = \frac{V_{Out}}{V_{in}} = \frac{V_{Out}}{V_{Out} + V_{do}} < 1 \tag{2.8}$$

where V_{in}, V_{Out}, and V_{do} are the input, output and dropout voltages of the regulator, respectively. As the equation implies the regulated output voltage is always lower than input voltage.



(a)



(b)

Figure 2.14: Operation principle of the linear voltage regulator (LDO) [44].

The power conversion efficiency of the LDO can be expressed as:

$$LDO\ Efficiecny:\ \eta_{LDO} = \frac{P_{Out}}{P_{in}} = \frac{V_{Out} \times I_{Out}}{V_{in} \times (I_{Out} + I_q)} \times 100 \quad (2.9)$$

where I_{Out} and I_q are output load current and internal circuitry loss, respectively. If the loss at the regulator circuitry (I_q) is assumed to be negligible, the power conversion efficiency can be simplified as:

$$\eta_{LDO} = \frac{V_{Out}}{V_{in}} \quad (2.10)$$

As the Equation (2.10) implies, the power conversion efficiency of linear regulators is good only when the output voltage is close to the input voltage and maximized when the dropout voltage is very small. In [56], a linear voltage regulator circuit is utilized for energy harvesting application, however the overall power conversion efficiency of the circuit is low due to high voltage difference between input and output voltages. The power dissipation of the regulator circuit must be minimized to enhance the power conversion efficiency of the circuit.

2.4.2. Sub-threshold Voltage Regulation

In previous section, it is declared that conventional voltage regulators are not suitable for low power energy harvesting applications, due to their high quiescent power consumption and low power conversion efficiency. Table 2.1 shows comparison of specifications for a conventional voltage regulator and a low power voltage regulator [57]. The performance of the circuit can be upgraded to the given conditions by operating the circuit in sub-threshold region which highly decrease the power requirement of the circuit.

Table 2.1: Comparison of specifications for a conventional voltage regulator and a low power voltage regulator [57].

Specifications	A conventional LDO	An LDO for energy harvesting applications
Output capacitance	5 µF	250 pF
Load current range	0.1 mA – 100 mA	0.1 µA – 25 µA
Quiescent current	< 100 µA	< 1 µA
PSRR	< -20 dB @ 1 kHz	< -20 dB @ 100 kHz

2.4.2.1. Sub-threshold Voltage Reference

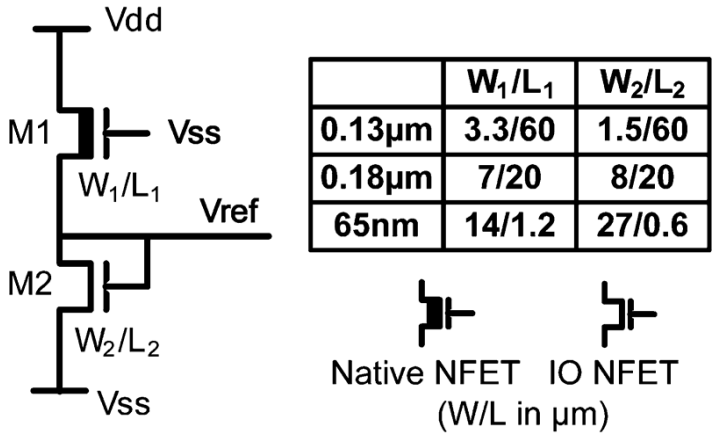
The voltage reference circuit is used to generate a reference voltage which is independent of the supply (input) voltage and the temperature. Since the voltage reference circuit is always drawing current from supply the quiescent current of this block must be kept as low as possible. Most of the typical band-gap voltage references generate reference voltage higher than 1.2 V. However, in low voltage and low power applications reference voltages lower than 1 V is required. Therefore, band-gap voltage references are not suitable for low voltage energy harvesting applications. Instead of them, for generating a PTAT reference, sub-threshold voltage reference circuits can be used. By keeping the transistors in the circuit in sub-threshold region the current consumption of the circuit can be decreased.

In [58], a voltage reference circuit which is only composed of 2 transistors operating in sub-threshold region is proposed. Figure 2.15 shows schematic of the 2T voltage reference circuit where the M1 is a special zero threshold NMOS transistor (Native NFET) and the M2 is a regular NMOS transistor. Since a special zero threshold transistor is used, by connecting its gate to Vss (negative supply voltage) leads to draw current on the transistors. Therefore, the current on the transistors is same and since they operate in sub-threshold region the current on them can be expressed as:

$$\begin{aligned} I &= \mu_1 C_{ox1} \frac{W_1}{L_1} (m_1 - 1) V_T^2 \exp\left(\frac{0 - V_{ref} - V_{th1}}{m_1 V_T}\right) \\ &= \mu_2 C_{ox2} \frac{W_2}{L_2} (m_2 - 1) V_T^2 \exp\left(\frac{V_{ref} - V_{th2}}{m_2 V_T}\right) \end{aligned} \tag{2.11}$$

where μ is the mobility of transistors, C_{ox} is the oxide capacitance of transistors, W/L is the aspect ratio of transistors, m is the sub-threshold slope factor, V_T *(=* $k_B T/q$*)* is the thermal voltage, V_{TH} is the threshold voltage of a MOSFET, and V_{ref} is the reference voltage. The analytical solution of the voltage reference can be calculated by solving this equation. Equation (2.12) shows the analytical solution of V_{ref}, where both first and second terms are proportional to absolute temperature with negative and positive signs, respectively.

$$V_{ref} = \frac{m_1 m_2}{m_1 + m_2} (V_{th2} - V_{th1}) + \frac{m_1 m_2}{m_1 + m_2} V_T \ln\left(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1}\right) \tag{2.12}$$



	W_1/L_1	W_2/L_2
0.13µm	3.3/60	1.5/60
0.18µm	7/20	8/20
65nm	14/1.2	27/0.6

Figure 2.15: Schematic of the 2T voltage reference proposed in [58].

The generated reference voltage is totally independent of the supply voltage and with the adjustment of the width and length of two transistors temperature insensitive reference voltage can be achieved. Moreover, since the circuit does not contain any resistor and only use two transistors, the design is completely area efficient. In order to keep power consumption of the circuit at lowest level, W/L ratio of the transistors is kept as low as possible. W/L ratios of the transistors for different CMOS technologies are also given in Figure 2.15.

2.4.2.2. Sub-threshold Voltage Regulator Design

A series voltage regulator which takes feedback from the output voltage and compares it with a reference voltage is usually used in the regulation of the input voltage. Figure 2.16 shows a typical three stage voltage regulator circuit which is mostly used in passive RFID applications [59]. First stage of the regulator is an opamp which compares the regulated output voltage with the reference voltage. The second stage is a buffer which improves performance of the opamp. The final stage is a pass transistor which is used to regulate the output voltage. Most of the dissipated power in this circuit is consumed by the opamp stage; hence power consumption of the opamp must be kept as low as possible.

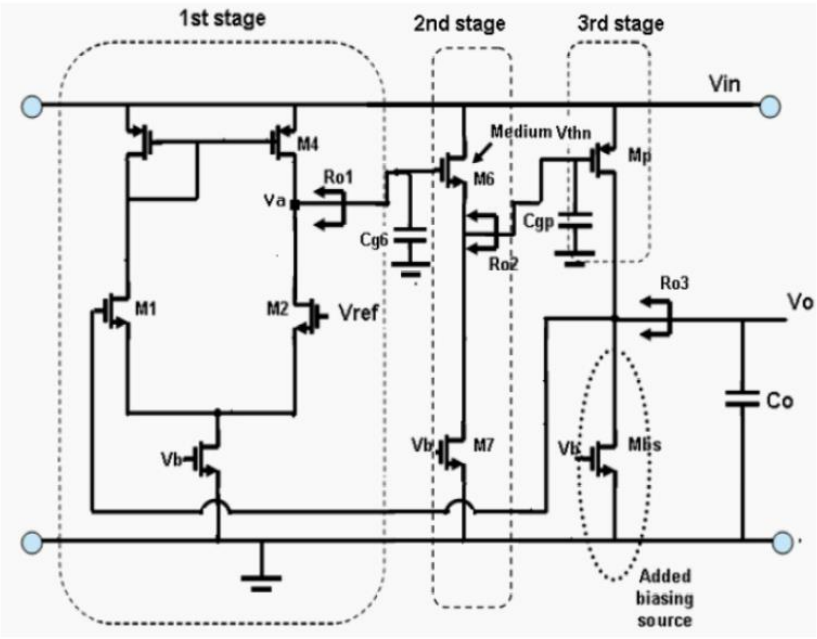


Figure 2.16: The typical voltage regulator for low voltage RFID applications [59].

2.5. On-Chip Power Management

The on-chip power management circuit in interface electronics for energy harvesting applications is used to control the connection of harvested power to the load. The control unit is particularly needed when driving a real load like a sensor to take the sensor into standby when the harvested power is not enough to drive the sensor. The power management circuit both monitors the harvested power and the power requirement of the load and cuts the connection whenever the harvested power is not sufficient. In the standby mode, mechanical transducer charges the storage capacitor at the end of the rectifier and power management circuit turns ON the load connection when it reaches to enough voltage level. Since the power management block is always active, it must draw very low quiescent power from the supply.

In [60], an input powered power management circuit for vibration based electromagnetic energy harvesters is proposed (Figure 2.17). The control generator block is used to monitor the voltage level of the input. If the input voltage is not sufficient to drive the load the controller chip disables the operation of oscillator and cut the current drawn by the resistors R1 and R2. As a result whole the blocks in DC/DC converter part is turned OFF which causes to draw zero current at the standby. After the input voltage reaches sufficient level the control generator turns the remaining system ON.

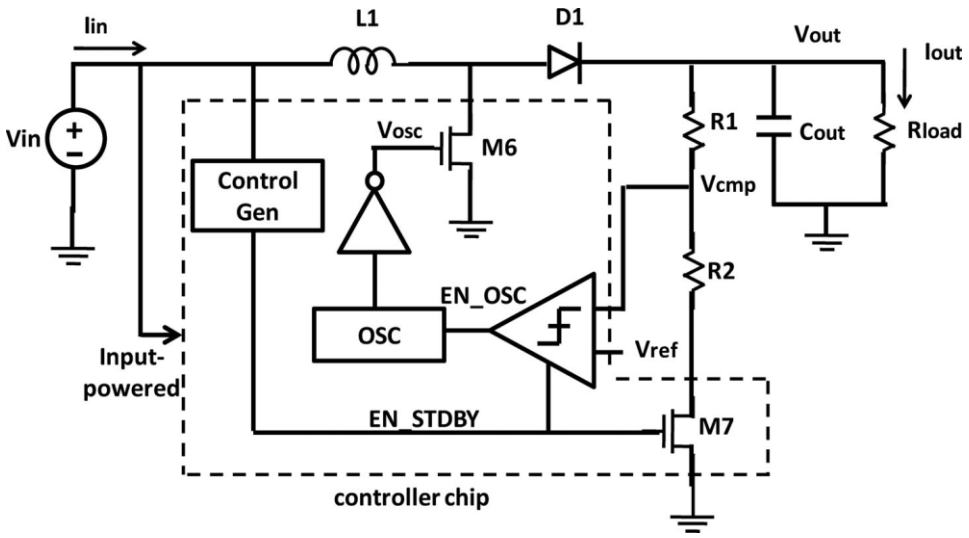


Figure 2.17: The power converter circuit proposed in [60].

In [61], a mode selector circuit is proposed as the controller unit and two trigger points are generated by using resistive ladders. At these trigger points, the output of mode selector is goes from low to high and high to low according to the input voltage level. The power consumption of this block is 2.7 µW and power consumption of the overall power converter block is 5 µW in standby mode. When the power management circuit block takes the converter circuit into standby mode the overall power consumption of the circuit is highly decreased which leads to charge the intermediate storage capacitor much faster.

2.6. Summary of the Chapter

In this chapter, detailed description of required blocks for a typical vibration based energy harvesting interface electronics has been given. The theory and design of each block is explained with the help of state-of-the-art designs in the literature. Also important parameters of each block for low voltage and low power applications have been discussed. Next chapter explains the design and simulation results of the proposed IC for low voltage and low power vibration-based electromagnetic energy harvesting applications designed in 90 nm CMOS process.

CHAPTER 3

THE DESIGNED ENERGY HARVESTING IC IN 90 nm CMOS TECHNOLOGY

The previous chapter introduced brief description of the required building blocks for a typical interface circuit for energy harvesting applications. The interface electronics for vibration based electromagnetic energy harvesters is especially challenging at low vibration levels due to the generated low peak voltages. Therefore, design of interface electronics for such systems poses with two basic challenges which are efficient conversion of incoming AC signal into DC voltage and generation of a stable DC power source to drive a realized load.

In this chapter, the theory, design, and simulation results of the blocks of a complete interface electronics circuit for electromagnetic energy harvesters which is designed in 90 nm CMOS technology is explained. Section 3.1 explains general overview of the proposed energy harvesting system by introducing each sub-block. Section 3.2 focuses on the design and simulations of the ultra-low voltage fully-self powered rectifier circuit. Section 3.3 describes the DC/DC converter block for low voltage application which includes a low voltage charge-pump design and a low power ring oscillator to drive the charge-pump. Section 3.4 presents theory, design and simulation results of a low voltage and low power voltage regulator circuit which regulates the output to 1 V DC voltage. The voltage regulator circuit includes three sub-blocks which are a sub-threshold voltage reference, a low power voltage divider and a low power comparator. The circuit is designed to get 1 V stabilized output voltage for input peak voltages larger than 0.35 V with frequencies below 10 Hz. Finally, section 3.5 summarizes the chapter and points the achieved goals.

3.1. The Energy Harvesting IC Overview

Figure 3.1 shows the overview of the proposed interface circuit (IC) for low vibration electromagnetic (EM) energy harvesting applications, designed in TSMC 90 nm CMOS technology. All sub-blocks of the system is designed and implemented on a single chip which generate a fully integrated system that is powered with an electromagnetic harvester. The first block of the proposed system is an AC/DC converter block which efficiently rectifies the incoming AC signal. After the rectification a DC/DC converter block is used to change the level of the rectified signal. The DC/DC converter block is composed of a charge-pump and an oscillator block which helps to step up the DC voltage. The final block of the system is a voltage regulator block which operates at low

voltage and low power conditions. The voltage regulator block monitors the output voltage and compares it with a voltage reference block and gives feedback to the oscillator block to stabilize the output voltage at a desired value.

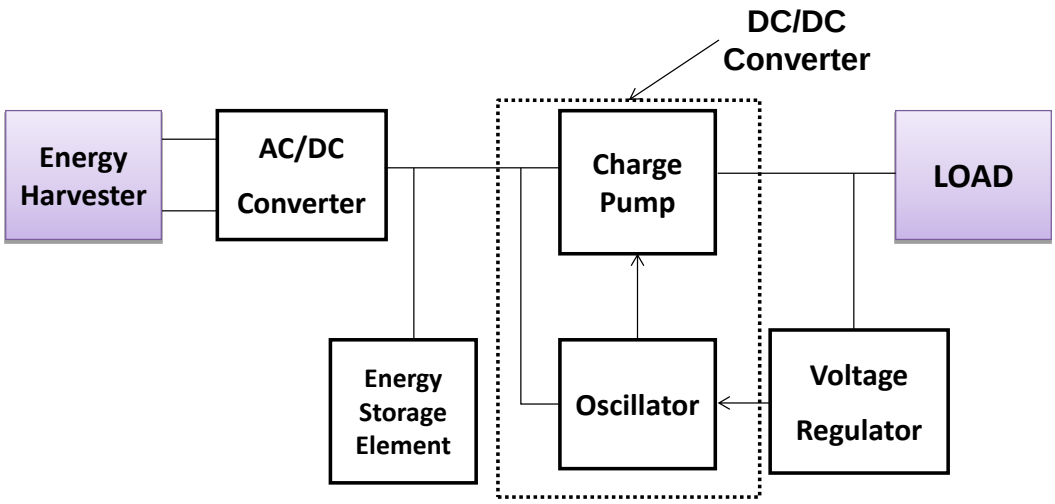


Figure 3.1: Block diagram of the interface circuit designed in TSMC 90 nm CMOS technology.

3.2. AC/DC Converter

The generated peak voltage at vibration based Electromagnetic energy harvesters is considerably low at low vibration levels. Therefore, converting the generated voltage into DC is challenging. Various different methods can be applied to rectify such low voltages [62]. For example, the harvested AC voltage can be amplified which helps to rectify it much more easily. An active amplifier circuit can be used for amplification; however it needs an external power supply. A transformer or an LC resonator can be used for passively amplifying the AC voltage, but non-CMOS components are required in this method which in turn increases the cost and area of the interface circuit. Besides, these components have low efficiency performance at low frequencies. A CMOS rectifier circuit can be used for AC to DC conversion at the first stage. However, using passive semiconductor diodes causes a forward voltage drop at the output, which is a significant problem at low voltage levels. To eliminate this problem, active diodes with much lower voltage drop can be used instead. Performance of the active rectifier is similar with an ideal diode: it has nearly zero drop-out voltage. However, active rectifiers require an external power source to operate which is a limiting condition for energy harvesting applications. In this study a self-powered and fully-integrated active rectifier topology is designed and implemented. Besides, the conventional gate cross-coupled rectifier (GCCR) topology is also implemented on the same chip for a fair comparison between the proposed circuit and previously reported work [37].

The GCCR is the improved version of full wave bridge rectifier (FWBR) which is also depicted in Section 2.2.1. The GCCR topology includes a PMOS diode connected transistor pair for rectification and a cross-coupled NMOS transistor pair for passing the

current through its drain to source. Due to the cross coupled transistor pair the voltage drop at the output decreases, i.e. one of the threshold voltage drop replaced with a drain-to-source voltage of an NMOS transistor (Figure 3.2).

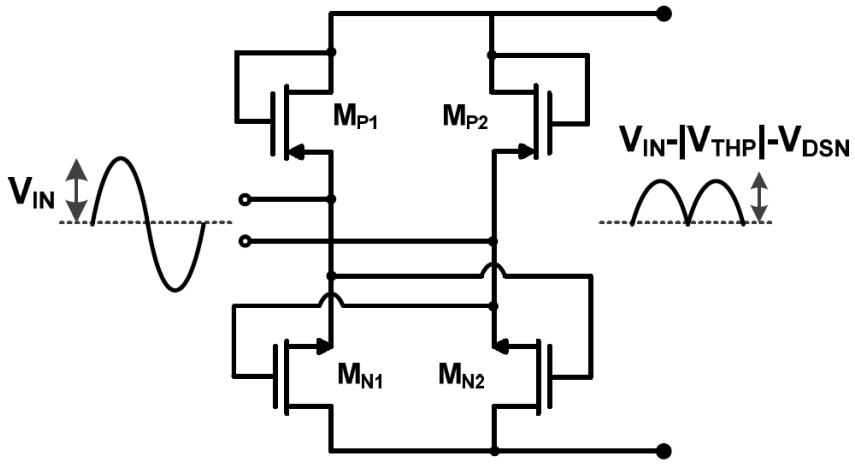


Figure 3.2: Schematic of the gate cross-coupled rectifier (GCCR) [37].

Output voltage of the GCCR can be expressed as:

$$V_{OUT} = V_{IN} - (|V_{THP}| + V_{DSN}) \tag{3.1}$$

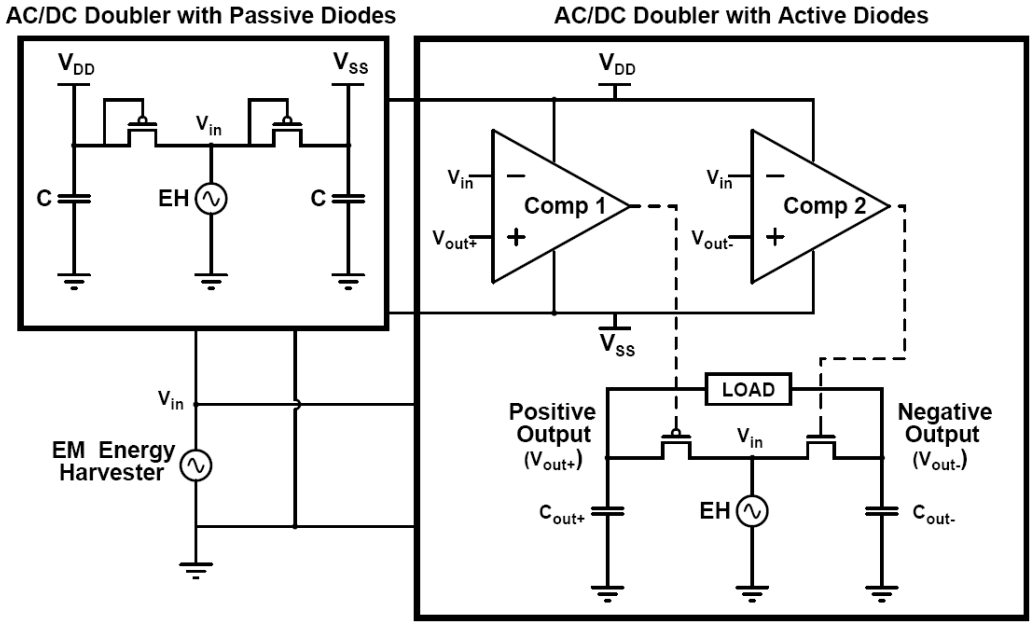
where the voltage drop on the diode connected PMOS transistors operating in saturation region is:

$$|V_{SG}| = |V_{SD}| = |V_{THP}| + \sqrt{\frac{2I_D}{\mu_p C_{ox}(W/L)}} \tag{3.2}$$

where V_{GS}, V_{DS}, and V_{THP} are source-to-gate, source-to-drain, and the threshold voltage of the transistor, I_D is its source-drain current, $\mu_n C_{ox}$ is the intrinsic transconductance, and W and L are width and length of the transistors in the utilized technology, respectively. Threshold voltage depends on utilized process and it is possible to minimize it with the body effect [63]. To eliminate the effect of second term in Equation (3.2), the aspect ratio (W/L) of the transistor must be increased as much as possible by considering the available area and the parasitic capacitances.

Although the GCCR topology shows good performance among passive rectifiers the power conversion efficiency of the rectifier is still low for low voltage applications and its output voltage is limited by the peak voltage of the input. The proposed active rectifier topology enhances the power conversion efficiency of the rectifier by utilizing active diode as the rectification element which has considerably lower voltage drop and higher load driving capability compared with a passive diode. Besides, a voltage doubler topology is used at the circuit to get a dual rail output where the output voltage can reach up to peak-to-peak voltage of the input.

Figure 3.3 shows block level representation of the active rectifier circuit where an active AC/DC doubler structure is utilized to rectify the input and drive the output load. The utilized active diodes composed of a pass transistor and a comparator circuit where gate of the pass transistor is controlled with the comparator [62]. The designed rectifier circuit is improved version of the self-powered rectifier circuit explained in Section 2.2.2 which was previously reported by our group [42]. Similar with the previous design an additional passive rectifier is used to supply the comparators of the active diodes. However, a passive AC/DC doubler circuit is utilized instead of the previously utilized bias generator circuit which includes a Dickson rectifier and a half wave rectifier. With the help of this modification, power losses at the passive rectifier part of the circuit are decreased. The improvement at the utilized CMOS technology and custom designed comparator helps to improve the minimum operation voltage of the circuit. Moreover, the designed circuit requires only single input voltage and does not require off-chip components which decreases complexity of the circuit and provides a fully-integrated solution.



*Designed with Kaveh Gharehbaghi.

Figure 3.3: Block level representation of the proposed active rectifier.

Operation of the active AC/DC doubler circuit is as follows: For positive input signals, when the input exceeds the positive output (V_{out+}) the output of the comparator at the positive output side (Comp 1) is changed to low which turns the PMOS pass transistor ON and charge the positive output capacitor (C_{out+}). When the input voltage falls below the positive output the comparator turns the pass transistor OFF and positive charge is stored on the capacitor. Similarly, for input voltages lower than negative output (V_{out-}) the comparator at negative output side (Comp 2) turns the NMOS pass transistor ON and charge the output node (V_{out-}) negatively. To store the charge on the capacitor (C_{out-}) the NMOS transistor is turned OFF by changing the output of the comparator to low. It is

noteworthy that PMOS pass transistors are poor at low levels, so NMOS pass transistor is used to transfer the charge at negative side.

The positive and negative outputs of the passive AC/DC doubler circuit are used as power supplies (V_{DD} and V_{SS}) of the custom comparators utilized in the active rectifier. The source and bulk of PMOS transistors can be connected to each other due to the N-well process. However bulk of the NMOS transistors must be connected to most negative voltage which is negative output of the active AC/DC doubler circuit. Therefore, at passive AC/DC doubler circuit diode connected PMOS transistors are utilized for rectification.

Figure 3.4 shows the simulation result of the rectified output voltage taken from passive AC/DC doubler circuit for different values of W/L ratio of diode connected transistors for 250 mV input peak voltage, 10 Hz input frequency and 5 MΩ load resistance. The given results are taken for optimization of the rectifier circuit. As the size of the transistors increase the current handling capability of the rectifier also increases, which leads to higher output voltage. However, for large sizes, the parasitic components of the transistors degrade their performance. Besides, the area occupied by the circuit is increased too much for high valued transistors. As W/L ratio of the transistors is changed from 100 to 400, the improvement in the rectified voltage is only around 40 mV (~10%). The effect of this slight difference on the overall circuit performance is relatively small compared to the increased area and cost. Therefore, W/L ratios of the transistors were chosen as 100.

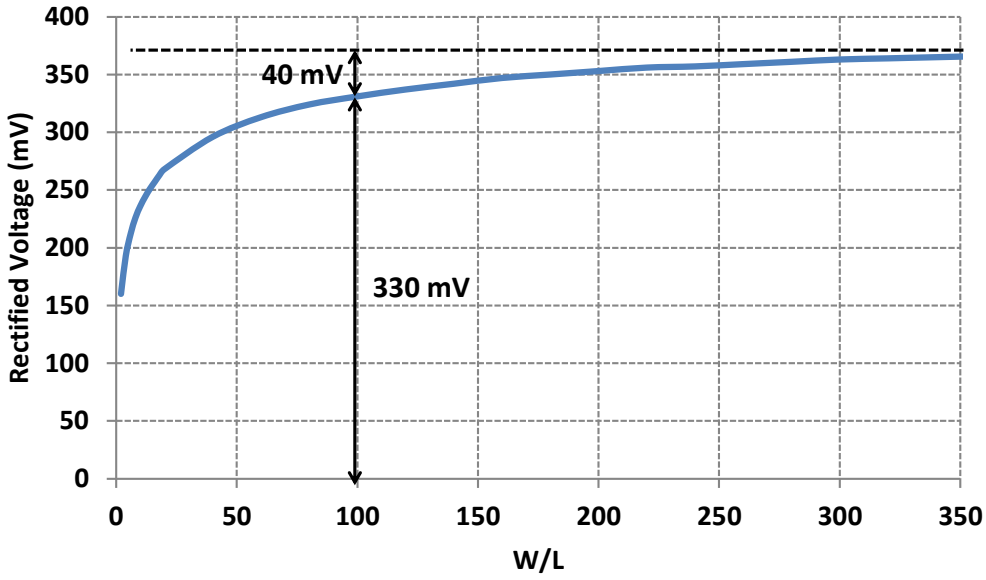


Figure 3.4: Change of the rectified output voltage with respect to the W/L ratio of the diode connected PMOS transistors.

Since the comparator circuits are powered by the passive AC/DC doubler circuit, a simulation of the optimized passive AC/DC doubler circuit was done to determine limit

of the current drawn by the comparators. Figure 3.5 shows change of the rectified output voltage from the passive AC/DC doubler with the varying load current at 10 Hz frequency, 250 mV input peak voltage and 5 µF storage capacitors. As expected the output voltage of the rectifier is decreases with the increasing load current. Figure 3.5 shows that the current consumption of the comparators should be lower than 30 nA to achieve rectified voltage higher than input peak voltage.

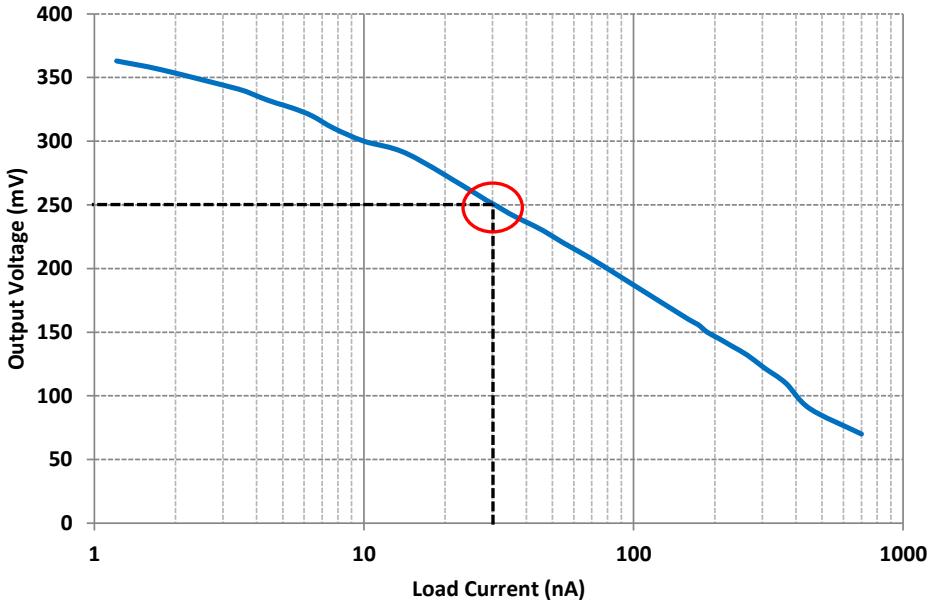
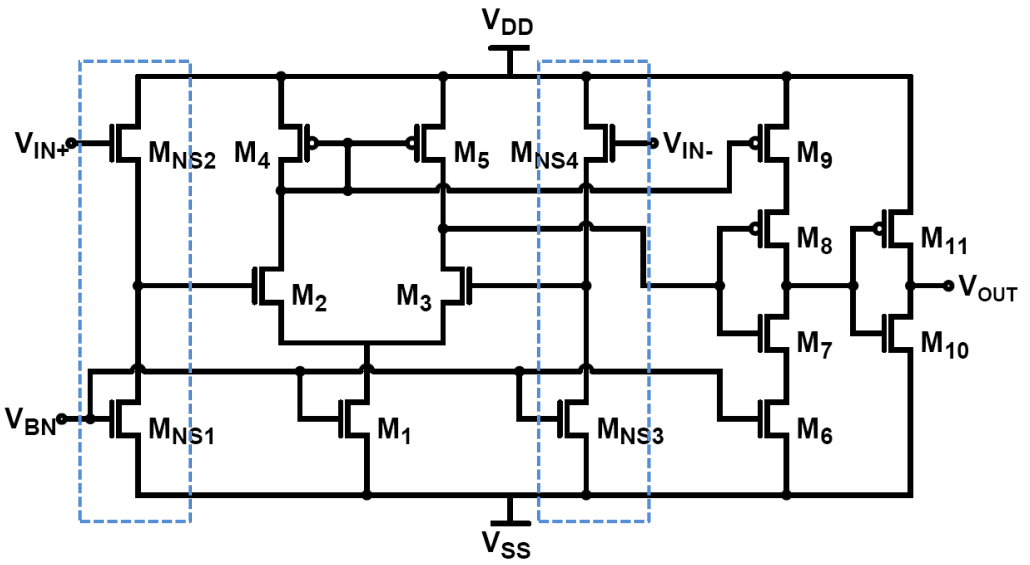


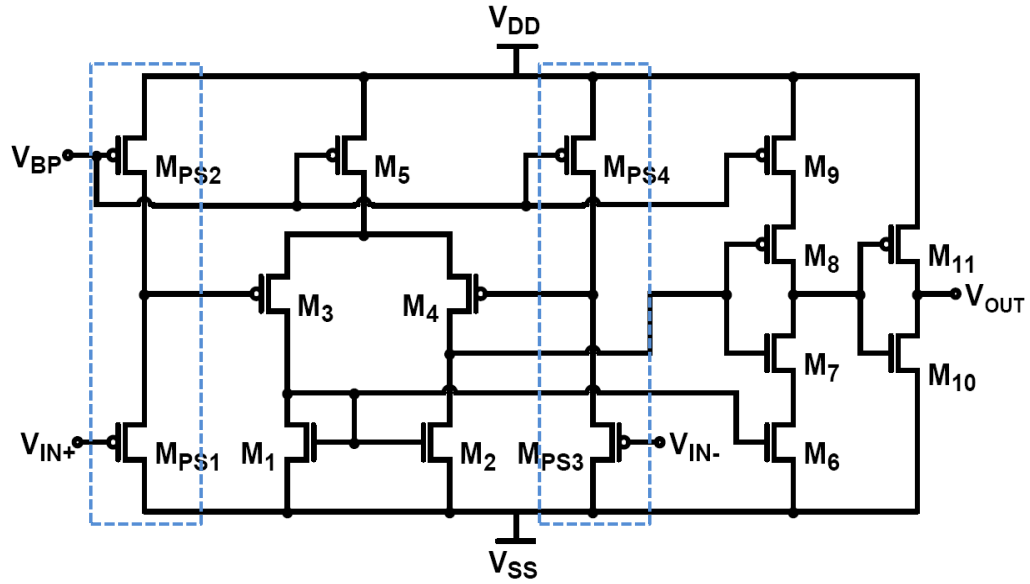
Figure 3.5: Rectified voltage versus the load current of passive AC/DC doubler at 10 Hz and 250 mV input peak voltage.

Performance of the proposed active rectifier circuit is improved further by two custom designed comparator circuits for positive and negative sides. Figure 3.6 depicts schematics of the comparators utilized at active diodes. At positive output side a comparator circuit with NMOS input transistors ($M_{2,3}$ at Figure 3.6 (a)), whose input common mode range is close to positive supply, is utilized. Similarly, at negative output side PMOS transistors ($M_{3,4}$ at Figure 3.6 (b)) are used as the input transistor of the comparator which has common mode range close to negative supply voltage [64].

Since the supplies of the comparator circuits comes from the passive AC/DC doubler, at some cases inputs of the comparator exceed the supply voltage. To put the inputs into common mode range of the comparators, source follower level shifters are utilized. Since the comparator circuit with NMOS input transistors works at the positive voltages, level shifting NMOS transistors (M_{NS1}-M_{NS4}) are added to reduce the DC level of input signals of the comparators. On the other hand, PMOS level shifter (M_{PS1}-M_{PS4}) is added to the comparator circuit with PMOS input transistors. Adding level shifters increases the sensitivity of the comparators to the voltage difference at the source and drain terminals of the pass transistors. Hence, the comparator accuracy is increased, which consequently enhances magnitude of the rectified voltage.



(a)



(b)

Figure 3.6: Schematic of the comparator circuits used at (a) positive and (b) negative output terminals of the active AC/DC doubler circuit.

The designed comparator circuit requires 2 bias voltages (V_{BN} and V_{BP}) for proper bias of the NMOS and PMOS transistors. For this purpose a sub-threshold voltage reference circuit which works at low voltages with very low power requirement is utilized [65]. Figure 3.7 shows schematic of the voltage reference which was adapted to TSMC 90 nm technology where V_{BN} is taken from gate of diode connected NMOS transistor (V_{REF}) and V_{BP} is taken from gate of upper bias transistor (M_9).

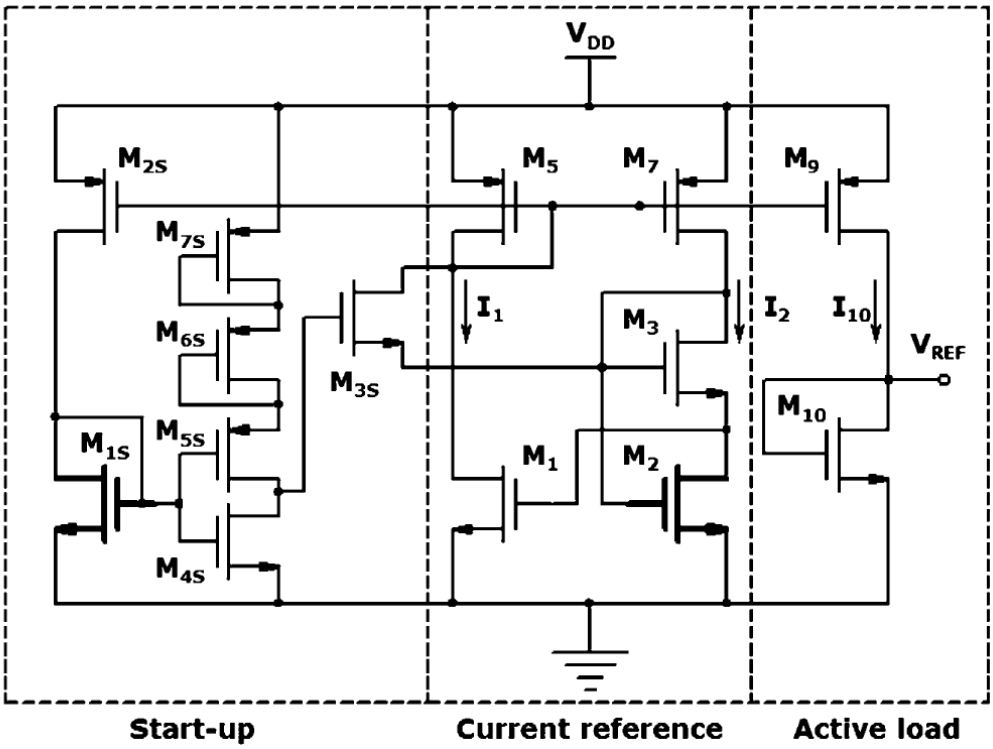


Figure 3.7: Sub-threshold voltage reference circuit adapted to TSMC 90 nm CMOS technology [65].

Operation principle of the circuit is based on the sub-threshold characteristic of the transistors. The current expression for an NMOS transistor at sub-threshold region can be expressed as:

$$I_D = \mu_n C_{ox} \frac{W}{L} V_T^2 \exp\left(\frac{V_{GS} - V_{TH}}{mV_T}\right)\left[1 - exp\left(-\frac{V_{DS}}{V_T}\right)\right] \tag{3.3}$$

where μ_n is mobility of the transistor, C_{ox} is the oxide capacitance, (W/L) is aspect ratio of the transistor, V_T is the thermal voltage ($V_T=k_BT/q$; k_B is the Boltzmann constant, q is the elementary charge and T is the absolute temperature), V_{TH} is threshold voltage of the MOSFET, m is the sub-threshold slope parameter, V_{GS} and V_{DS} are gate-to-source and drain-to-source voltages of the transistor, respectively. If the active load part of the circuit is taken into consideration and considers I_D as the current passing on M_{10} (I_{10}), an analytical solution can be expressed for the reference voltage. For $V_{DS}>4V_T$ the current expression can be approximated as it is almost independent of V_{DS}. Hence, the reference voltage can be expressed as:

$$V_{REF} = V_{GS_{10}} = V_{TH} + mV_T \ln\left(\frac{I_{D_{10}}}{\mu_n C_{ox}(W/L)V_T^2}\right) \tag{3.4}$$

In the given equation all of the parameters other than the transistor current are supply independent, hence by generating a supply independent current reference, a supply

independent voltage reference can be generated. For this reason a current reference circuit which uses self-biasing is utilized to get supply independent current source. However, the reference voltage has a start-up problem due to the utilized self-bias circuit. Therefore, a start-up circuit which guarantees proper operation of the reference circuit is utilized.

To have temperature compensated reference voltage, change of the reference voltage with respect to temperature must be as low as possible. By considering the current equation as $I_D = \alpha\mu_n T^2 f(T)$ (where α is a temperature independent constant) a solution for the current can be found. As a result, the temperature dependency of the voltage reference can be found as:

$$\frac{\partial V_{REF}}{\partial T} = \frac{k_{t1}}{T_0} + m\frac{k_B}{q}\ln\left(\frac{\alpha}{C_{ox}\left(\frac{W}{L}\right)\left(\frac{k_B}{q}\right)^2}\right) + m\frac{k_B}{q}\left\{\ln(f(T)) + \frac{T}{f(T)}\frac{d(f(T))}{dT}\right\} \quad (3.5)$$

where k_{t1} is a temperature independent constant coming from threshold voltage and T_0 is reference temperature ($T_0 \cong 300.15$°C). One of the possible solutions of $f(T)$ is a constant; however this could not be satisfied with sub-threshold transistors. Another solution for the current equation is,

$$I_D = \alpha\mu_n T^2 exp\left(\frac{AT + B}{CT}\right) \quad (3.6)$$

where A, B, and C are independent of the temperature. Given current equation can be easily satisfied by the sub-threshold current reference shown in Figure 3.7. The W/L ratios and type of the transistors used in the sub-threshold voltage reference circuit is given in Table 3.1. Where the LVT, SVT and HVT MOSFETs are low, standard and high threshold voltage transistors, respectively.

Table 3.1: W/L ratios and types of the transistors used in sub-threshold voltage reference

Transistor	W/L	Type
M_1	1 µm / 10 µm	SVT MOSFET
M_2	1 µm / 20 µm	SVT MOSFET
M_3	1 µm / 2 µm	LVT MOSFET
M_5, M_9	10 µm / 5 µm	SVT MOSFET
M_7	5 µm / 5 µm	SVT MOSFET
M_{10}	0.2 µm / 5 µm	HVT MOSFET
M_{1S}, M_{4S}	0.2 µm / 6 µm	HVT MOSFET
M_{2S}, M_{5S}, M_{6S}, M_{7S}	0.2 µm / 5 µm	HVT MOSFET
M_{3S}	0.2 µm / 4 µm	HVT MOSFET

Figure 3.8 shows simulation result of the voltage reference circuit for varying supply voltages. The adapted circuit gives about 0.2 V reference voltage for supply voltages larger than 0.3 V. The variation of the reference voltage from 0.3 V to 1.5 V is in the range of ±15 mV. Figure 3.9 shows variation of the generated reference voltage with respect to the temperature. As the temperature has been swept from 0°C to 60°C the change at the reference voltage is lower than 25 mV. The maximum power dissipation of the sub-threshold reference circuit is 4.5 nW. Although the reference voltage slightly deviates from the ideal reference performance the current consumed by the circuit is considerably low which can be easily satisfied from the passive AC/DC doubler structure.

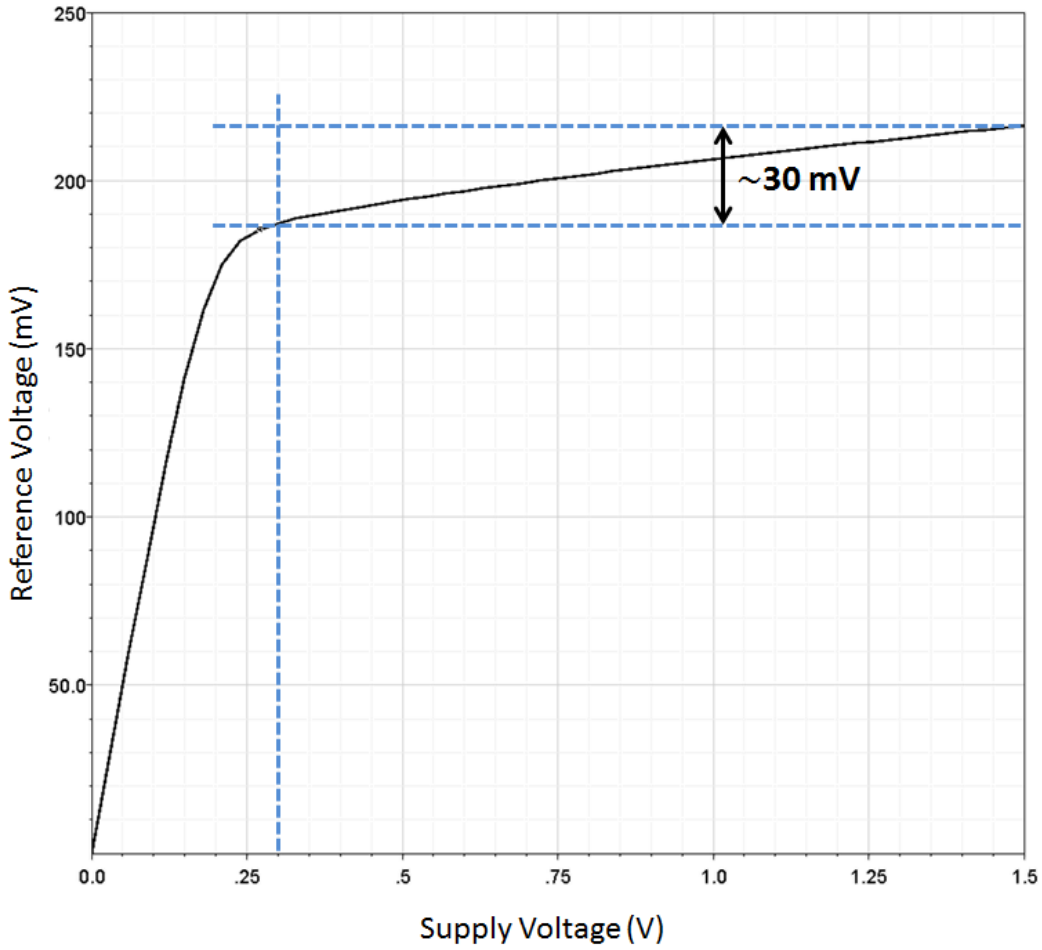


Figure 3.8: Change of the generated reference voltage with supply voltage.

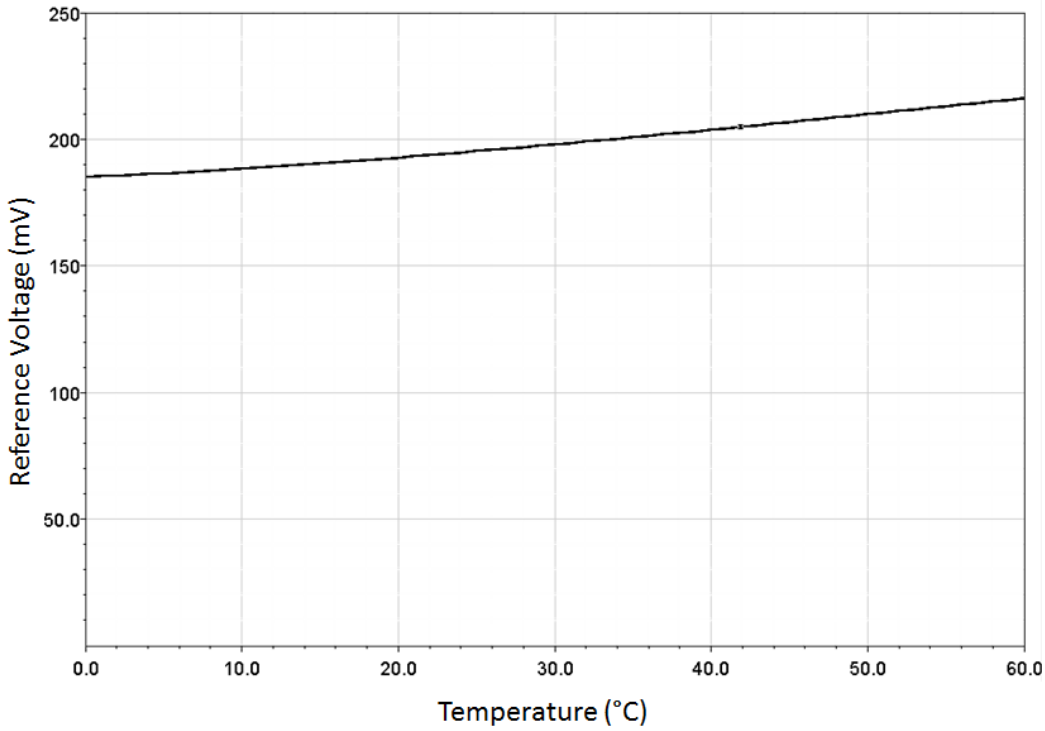


Figure 3.9: Change of the generated reference voltage with temperature.

After the sub-blocks of the rectifier designed properly, all of the blocks are integrated to each other and tested. As the final the optimization, size of the pass transistors at the active diodes are determined according to the simulations. The optimization is made to ensure the minimum voltage drop with maximum current drivability. In addition to that, parasitic components of the switches are also taken into account for best solution. As a result size of the pass transistors is chosen as 100 µm / 500 nm.

Figure 3.10 and Figure 3.11 show transient simulation results of GCCR and the proposed active rectifier circuits for 10 Hz, 250 mV input peak voltage and 5 µF storage capacitors. The output voltage of the GCCR circuit is only about 0.185 V for the given conditions. For the proposed active rectifier both positive and negative outputs are observed on the same figure. If we consider the dual rail output only about 20 mV voltage drop is occurred at the output which means that output of the rectifier is about 0.48 V. The results show that the new architecture improves performance of the architecture more than two times compared to GCCR circuit.

The result in Figure 3.11 also depicts the operation principle of the active diode at positive output side. As explained earlier, when the input voltage exceeds the positive output, the comparator output is triggered to low voltage and turn the pass gate ON. After the input voltage falls below the output the gate signal is again triggered to store the voltage at the output. The gate control signals are always lower than peak value of the input voltage; however, the proposed level shifters at the comparators work properly and the gate signals are accurately controlled.

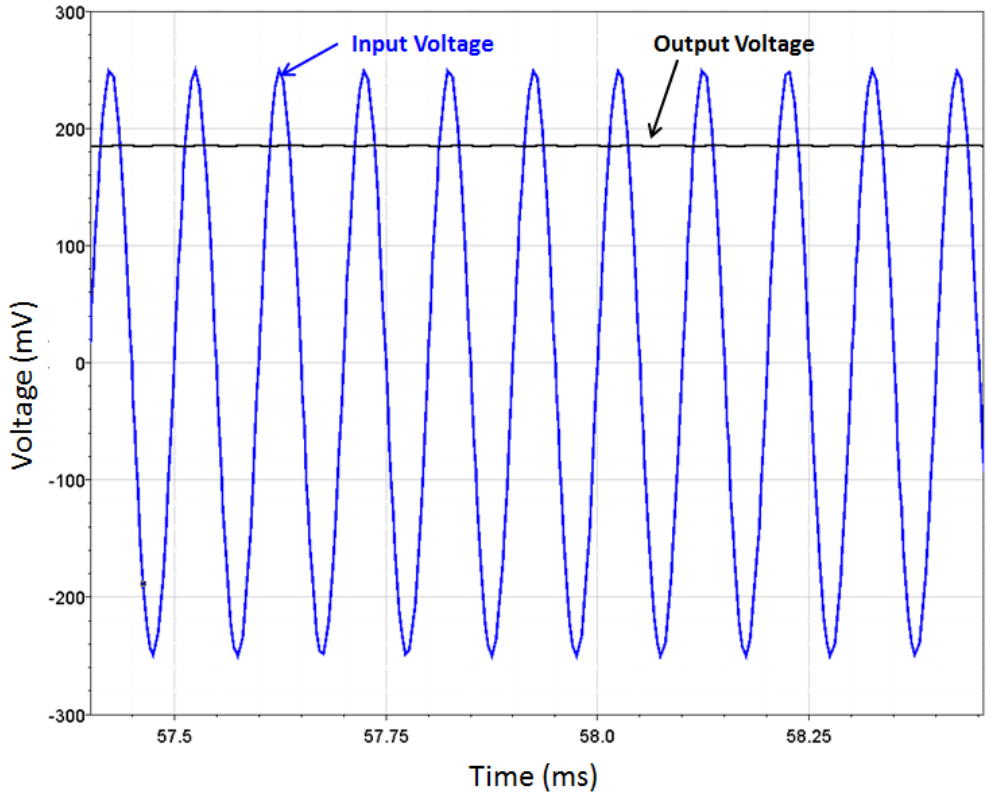


Figure 3.10: Simulation result of the GCCR for 10 Hz, 250 mV input peak voltage.

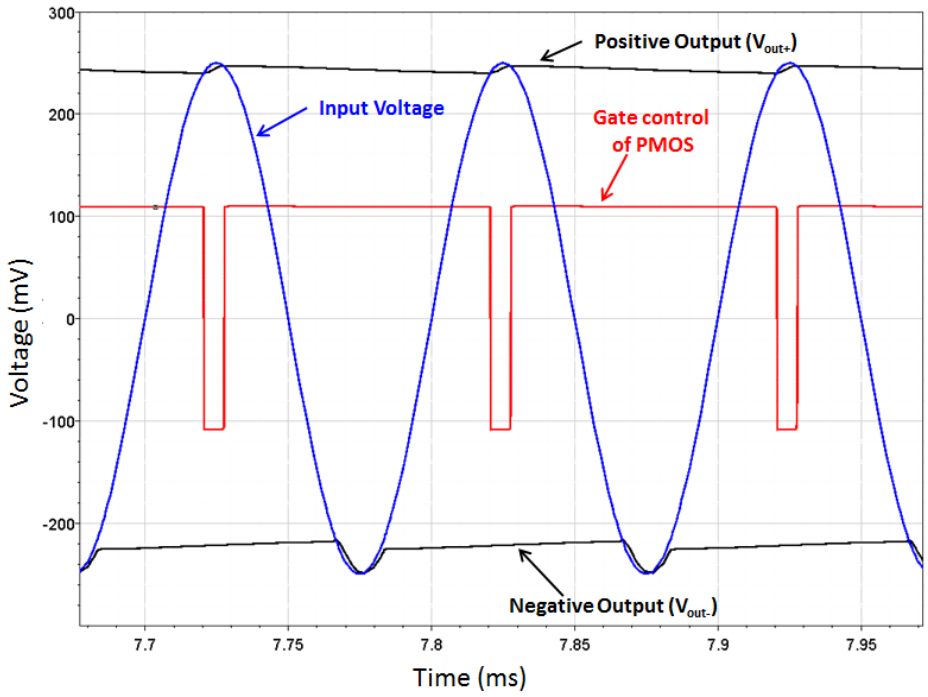


Figure 3.11: Simulation result of the active rectifier output for 10 Hz, 250 mV input peak voltage.

The following simulations of the active rectifier circuit is observed at 10 Hz input AC signal frequency and with 5 µF storage capacitors. Figure 3.12 shows change of the DC voltage at the output of the proposed active rectifier circuit, i.e. difference of positive and negative outputs with respect to applied input voltage amplitude for open load condition. As depicted in figure, the rectifier circuit converts the input AC voltage into a DC voltage with nearly twice the amplitude especially at low input voltages. Moreover, the circuit operates properly with minimum input amplitude voltage as low as 100 mV. Since threshold voltage of the utilized low voltage transistors are about 150 mV the current driving performance of the circuit highly decreases below this voltage; however, it is still acceptable down to 100 mV.

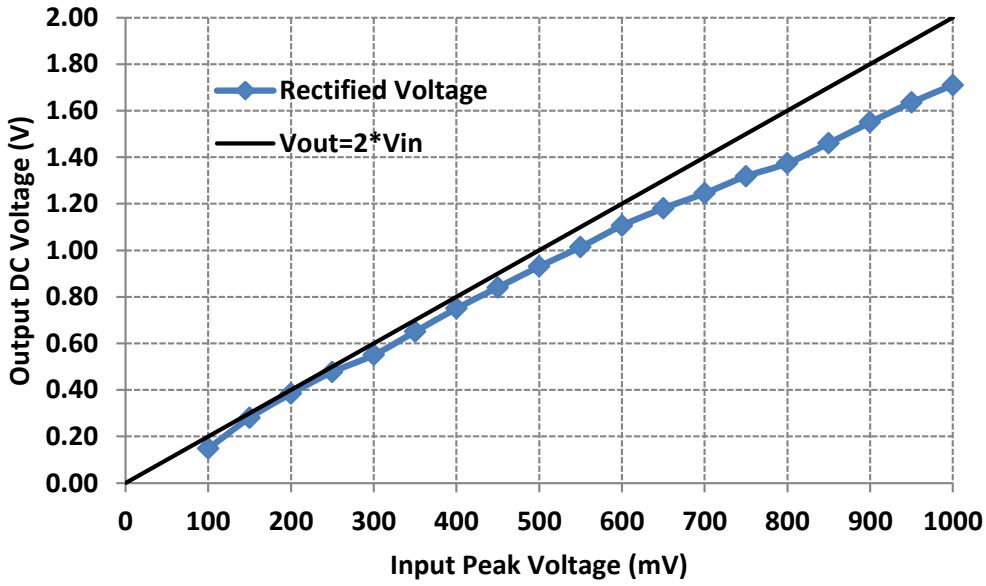
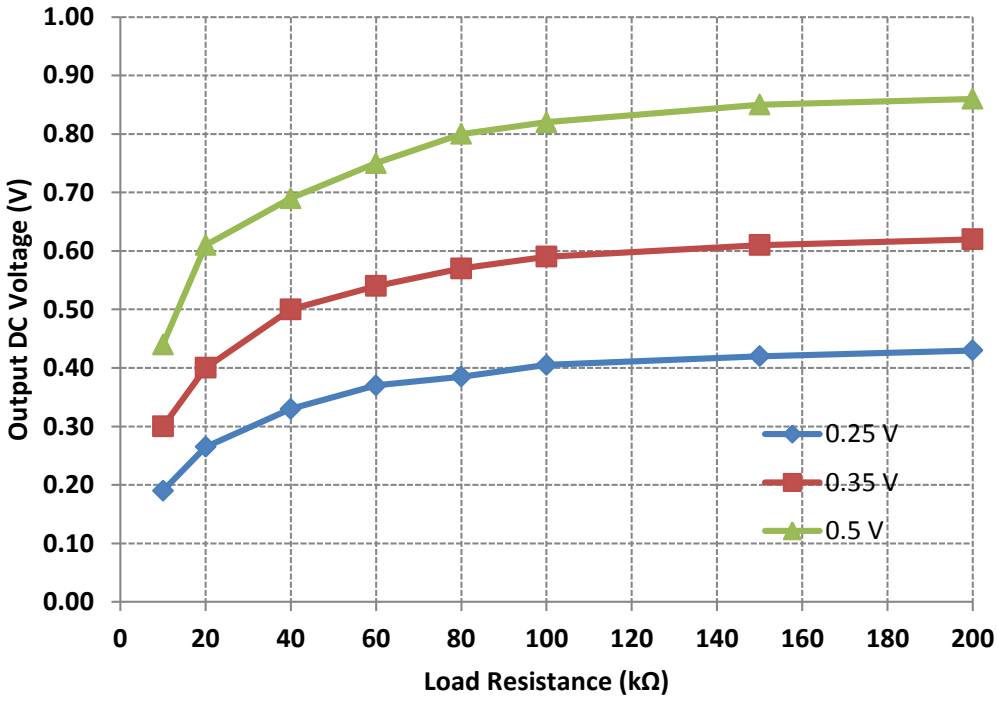


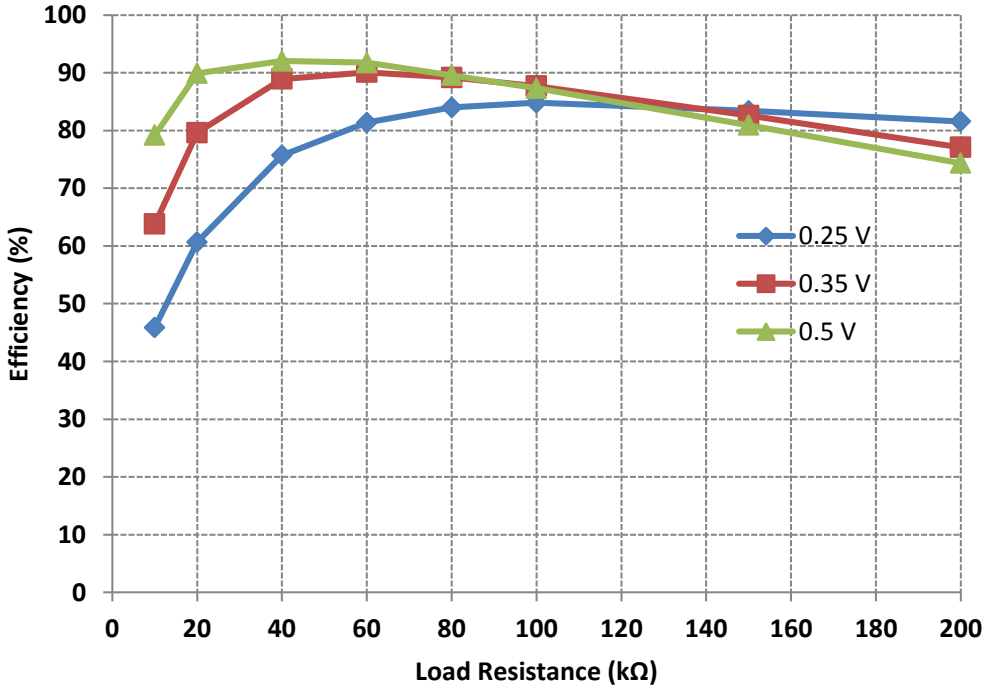
Figure 3.12: Output DC voltage versus the input voltage amplitude of the active rectifier circuit at 10 Hz frequency.

Figure 3.13 shows the transient simulation results of the active rectifier with varying load resistance. Figure 3.13 (a) depicts the change in output DC voltage versus the load resistance at 0.25, 0.35 and 0.5 V input voltage. Increasing the load resistance reduces the load current, which consequently decreases the discharging rate of storage capacitors. Hence, the output voltage decreases by reduction of load resistance.

Figure 3.13 (b) shows the power conversion efficiency of the active rectifier circuit with the variation of load resistance at different input voltages. The circuit operates with power conversion efficiencies higher than 80% with input amplitude voltages of 0.5 V, 0.35 V and 0.25 V when the load resistance is higher than 10 kΩ, 20 kΩ and 60 kΩ, respectively. Power conversion efficiency of the circuit is decreasing rapidly for load resistances lower than 20 kΩ due to increased power losses at pass transistors. The maximum power efficiency of the circuit is about 90% and is achieved at 40 kΩ load resistance with 0.5 V input voltage amplitude.



(a)



(b)

Figure 3.13: (a) The output DC voltage and (b) the power conversion efficiency of the proposed active rectifier circuit versus load values at different input amplitude voltages at 10 Hz frequency.

3.3. DC/DC Converter

The rectified DC voltage at the output of the AC/DC converter block is not at a sufficient level to drive a real load, hence a DC/DC converter block which steps up the rectified voltage is required. The theory and design of state-of-the-art examples of the charge-pumps are previously explained in Section 2.3.2. In this work a low voltage charge-pump circuit is utilized for boosting operation to satisfy fully-integrated and low voltage operation.

Figure 3.14 shows schematic of the 3-stage cross-connected charge pump circuit [66]. The utilized circuit solves the efficiency problem of the conventional charge pump circuits by changing the threshold voltage drop of the pass transistors with drain-to-source voltage of the cross-connected transistors. The basic element of the charge pump circuit is cross-connected NMOS pair which doubles the input DC voltage. Besides, PMOS switches are utilized to satisfy the connection between stages. In this work, to avoid the latch-up between NMOS and PMOS transistors and improve the threshold compensation, bulk regulation transistors (M_{PB1}-M_{PB12}) are added to the circuit.

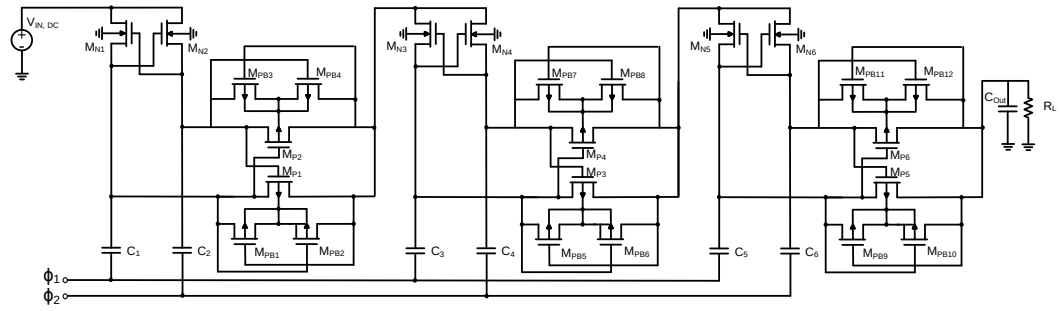


Figure 3.14: 3 stage cross-connected charge pump circuit.

The optimum stage number of the circuit is desired as 3 by considering the boosting ratio and power conversion efficiency of the circuit. The 3 stage charge pump configuration theoretically boosts the input voltage 4 times. However, little deviations from the ideal output voltage occur due to non-ideal clocks and voltage drops on the transistors. The optimized design parameters of the charge-pump circuit are given in Table 3.2, where low threshold transistors are used at the circuit to minimize the voltage drop at the output. The optimum boosting capacitance of the circuit is chosen according to the boosting performance of the circuit. Figure 3.15 shows change of the output voltage of the charge pump with different boosting capacitances for 0.5 V input voltage, 2 Hz clock frequency and 1 MΩ load resistance. When the boosting capacitance increases the output voltage also increases; however after a level the increment at the output voltage is not significant compared to the increment at the area needed by the capacitor. Hence the optimum boosting capacitance is chosen as 4 pF.

Table 3.2: Design parameters of the cross-connected charge pump.

Components	Size
M_{N1}-M_{N6}	7.5 µm / 100 nm
M_{P1}-M_{P6}	7.5 µm / 100 nm
M_{PB1}-M_{PB12}	500 nm / 100 nm
C_1-C_6	4 pF

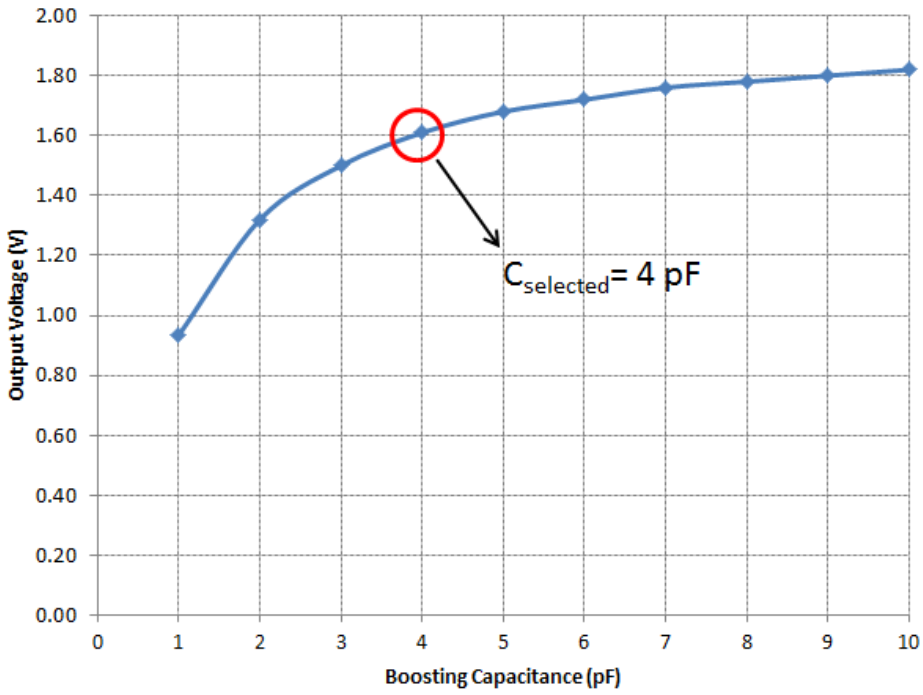
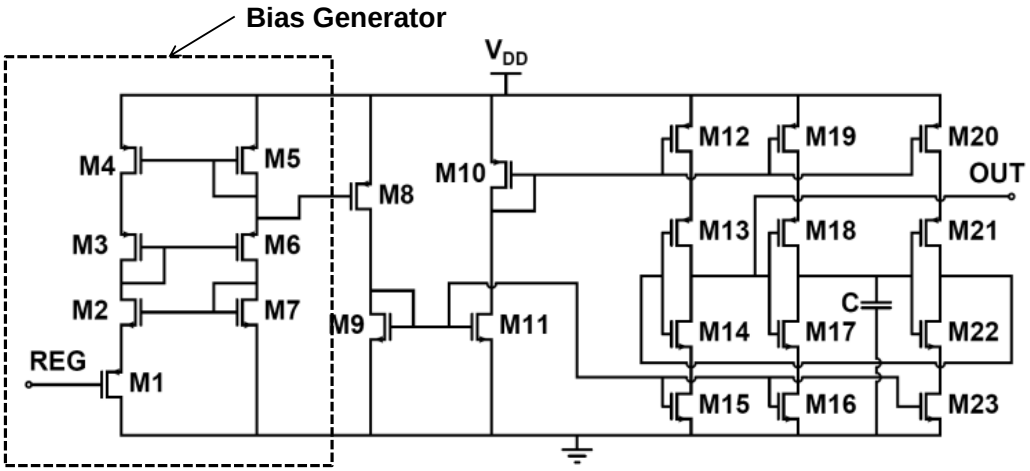


Figure 3.15: Change of output voltage of the charge pump with respect to size of boosting capacitance.

As shown in Figure 3.14 for proper operation of the charge pump circuit two non-overlapping clocks are required which can be supplied with an oscillator circuit. Typically, ring oscillators are used to generate a clock signal in CMOS technology. The power consumption of a ring oscillator is directly related with the frequency of the oscillator, the load capacitance and the supply voltage. Frequency of the oscillator must be in the range of 1 to 10 MHz for the best pumping performance of the circuit. To satisfy the required frequency and reduce the power consumption of the circuit a 3 stage current starved ring oscillator topology which limits the current drawn from the supply is used at this work [67].

Figure 3.16 shows schematic of the 3 stage current starved ring oscillator with constant Gm (PTAT) biasing. The inverter circuits at the inner side of the circuit (M13,M14,M17, M18, M21, M22) forms the ring oscillator part of the circuit and the PMOS and NMOS current mirror transistors at the outer layer which are biased from the

bias generator limits current of the oscillator. Only one of these current mirrors is sufficient for limiting the current; however symmetry at the circuit guarantees the 50% duty cycle and improves the jitter. Size of the transistors are arranged to get the desired frequency from the oscillator. Moreover a stray capacitance (C=50 fF) is added before the last stage to keep the frequency in the operation range.



*Designed with Kaveh Gharehbaghi.

Figure 3.16: Schematic of the current starved ring oscillator with constant Gm biasing.

The bias current of the transistors and frequency of the oscillator can be controlled with the help of the bias generator. As discussed earlier, frequency of the oscillator directly affects output of the charge-pump and by using this idea; the output voltage can be set to desired value. For this purpose a PTAT bias generator where the bottom PMOS transistor (M1) acts like a resistor and used to control the generated current is designed. The control signal of the oscillator circuit comes from the regulator circuit and used to control frequency of the oscillator. The bias generator circuit also uses self-biasing to generate supply independent current source. Table 3.3 shows the design parameters of the designed 3 stage current starved ring oscillator with constant Gm biasing.

Table 3.3: Designed parameters of the current starved ring oscillator.

Transistor	W/L	Type
M_1	15 µm / 0.1 µm	LVT MOSFET
M_2	7.5 µm / 1 µm	SVT MOSFET
M_3, M_6	5 µm / 1 µm	SVT MOSFET
M_4, M_5	8 µm / 1 µm	SVT MOSFET
M_7	2.5 µm / 1 µm	SVT MOSFET
M_8	1 µm / 1 µm	LVT MOSFET
$M_9 - M_{23}$	0.24 µm / 0.72 µm	LVT MOSFET

The boosting capacitors used at the charge-pump circuit are considerably high, and such huge capacitors highly affect performance of the oscillator. Therefore, a driver stage is added after the oscillator which both satisfies generation of the non-overlapping clocks

and includes higher sized (stronger) inverters at the last stage for improving the drivability of the circuit. As the first block of the driver stage small sized (weak) inverters are utilized that have low parasitic capacitances and don't affect performance of the oscillator. Since two non-overlapping clocks are needed by the charge pump, an extra weak inverter is added to one of the signal paths. Figure 3.17 shows schematic of the driver stage where OSC is the input coming from the oscillator and CLK and CLK_BAR are non-overlapping clocks. Table 3.4 shows sizes of the used transistors at the driver stage where all of the transistors are used as low threshold transistors to increase the current driving capability of the circuit.

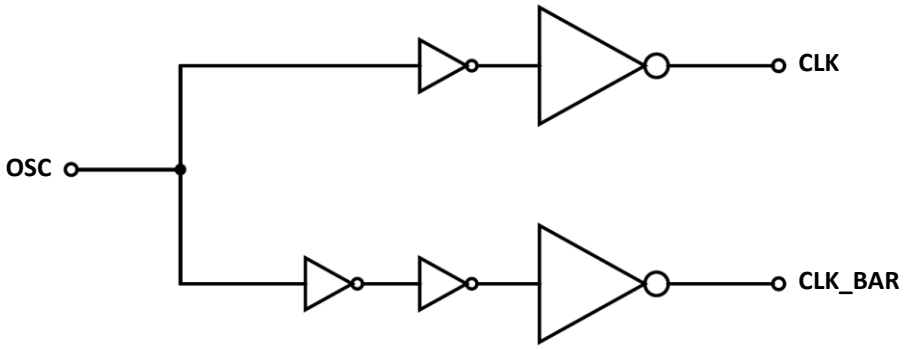


Figure 3.17: Schematic of the driver stage.

Table 3.4: Size of the transistors utilized in driver stage.

Transistor	W/L
M_P (Weak Inverters)	0.5 µm / 0.1 µm
M_N (Weak Inverters)	0.2 µm / 0.1 µm
M_P (Strong Inverters)	5 µm / 0.1 µm
M_N (Strong Inverters)	2.5 µm / 0.1 µm

Figure 3.18 shows the transient simulation result of the oscillator circuit with the drive stage for 0.6 V supply voltage and 1 pF load capacitance. The designed circuit is able to generate two non-overlapping clocks and for the given conditions the frequency of the clocks is around 6 MHz. Moreover, the added driver stage leads to get sharper rise and fall time, which also enhances performance of the circuit. If the rise and fall time of the clocks are not good enough the efficiency of the charge pump significantly decreases.

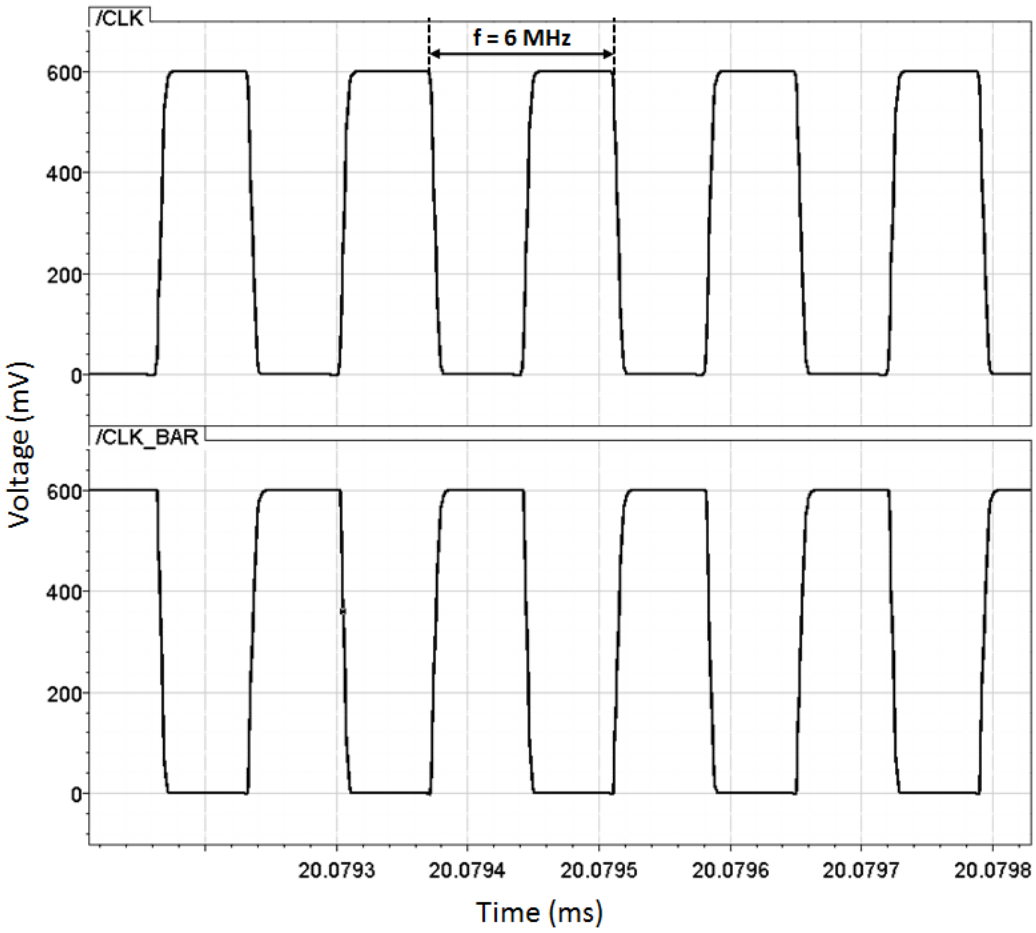


Figure 3.18: Simulation result of the oscillator circuit with driver stage for 0.6 V supply voltage and 1 pF load capacitance.

Figure 3.19 presents the simulation results of the proposed DC/DC converter block. Change of output voltage of the converter with respect to load resistance at different input DC voltages is depicted at the figure. The results show that at 0.3 V input supply voltage and 500 kΩ load resistance the circuit is able to give 1 V output voltage which is the desired value for this work. For larger input voltages the generated output voltage is higher than 1.2 V for load resistances higher than 300 kΩ. The output load capacitance of the circuit for given simulations is 100 pF. The output voltage of the circuit reaches up to 1.8 V for 0.5 V input DC voltage where the theoretical value is 2 V. The output voltages higher than 1 V are going to be regulated with the help of the voltage regulator.

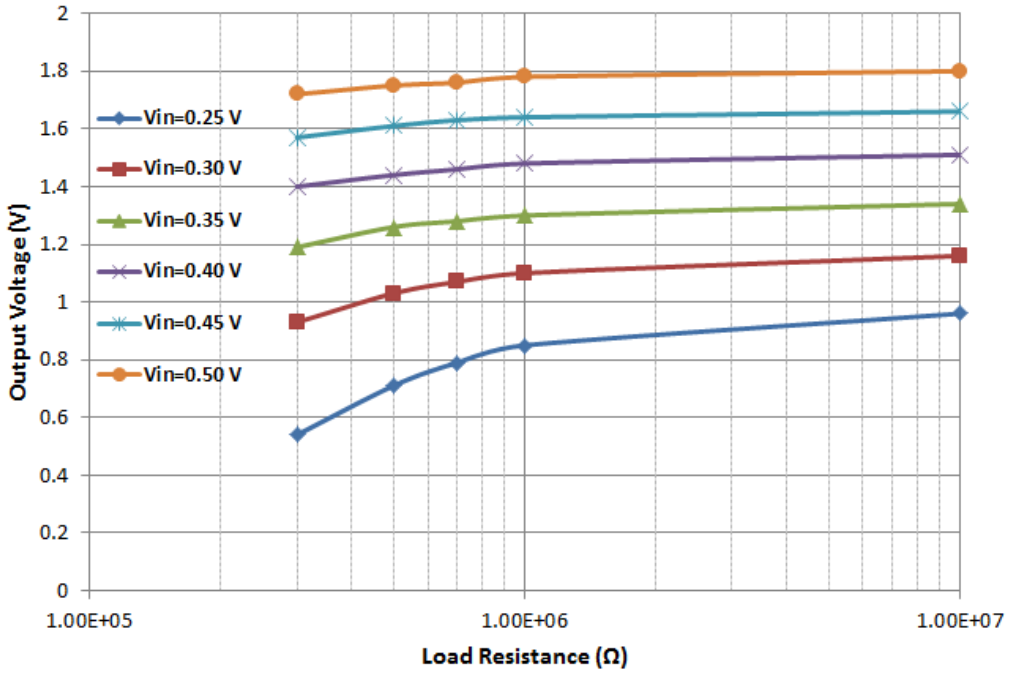


Figure 3.19: Change of output voltage of the proposed DC/DC converter block with respect to the load resistance for different input DC voltages.

3.4. Designed Voltage Regulator

The regulation strategy of the circuit is based on tuning the frequency of the oscillator by feeding the regulator output to the bias generator of the oscillator. A sub-threshold voltage regulator is designed to give feedback to the oscillator. The advantages of the sub-threshold voltage regulators compared to the commercial regulators are explained at section 2.4. The conventional LDO regulators suffer from low power conversion efficiency when there is a huge difference between incoming voltage and regulated output voltage. Besides, the unregulated voltage must exceed the desired voltage level to satisfy the regulation. However, in the proposed voltage regulator structure, it is enough to reach the desired value which is 1 V for this work.

Figure 3.20 shows block level representation of the proposed voltage regulator [68]. The basic principle of the regulator is it monitors the output voltage with a voltage divider and compares it with a reference voltage by the help of an error amplifier. Output of the error amplifier is used as a feedback to the oscillator bias. When the output voltage reaches to the desired voltage output of the error amplifier starts to increase and tune the bias of the oscillator to keep the output voltage at the desired value.

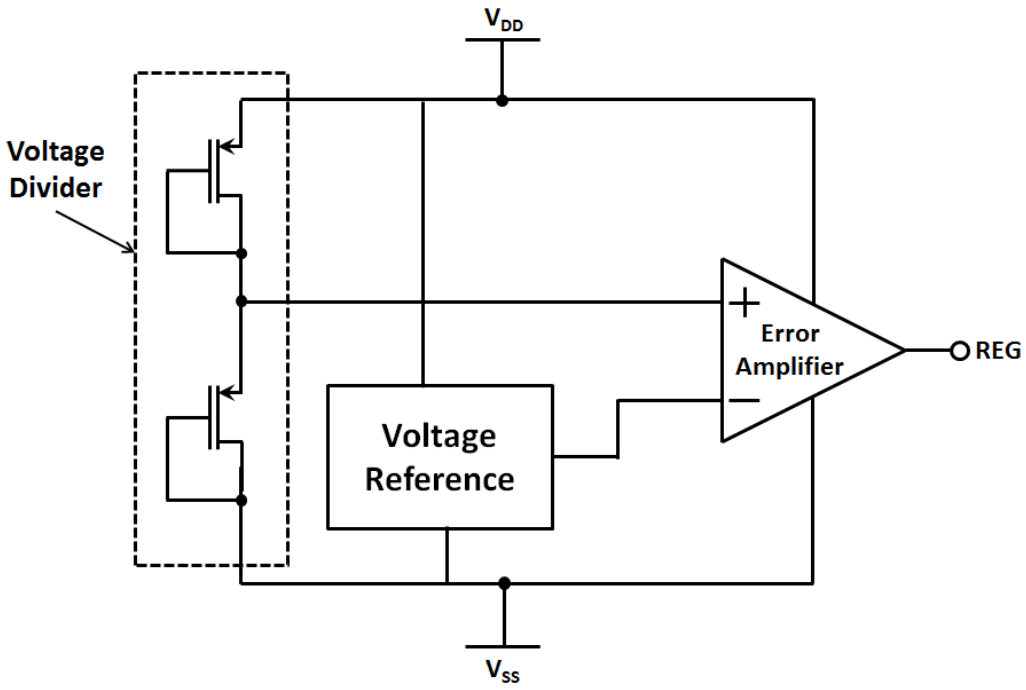


Figure 3.20: Block level representation of proposed voltage regulator [68].

To minimize the current consumption of the circuit and satisfy low voltage operation, a sub-threshold voltage reference circuit is utilized (Figure 3.21) [69]. The circuit includes a current source generator which generates current to create a supply and temperature independent reference voltage. The current generator uses a MOS resistor (M_R) which operates in linear region. Using this MOSFET highly decrease the area occupied by the circuit and eliminates the noises coming from a passive resistor. To satisfy the supply independent operation the current generator uses a β multiplier self-biasing circuit. Moreover, NMOS current mirror (M_{N1} and M_{N2}) transistors are used to decrease the effect of channel length modulation and increase the sensitivity of the current generator. The added NMOS current mirrors and the operational amplifier also improve the power supply rejection ratio (PSRR) of the circuit.

The current generated by the current generator (I_P) is copied to the bias voltage sub-circuit via the PMOS current mirrors and used to generate the reference voltage (V_{REF}). The bias voltage sub-circuit includes the transistor M_{N5} and two source-coupled pairs (M_{N6}-M_{N7} and M_{N8}-M_{N9}). All the MOSFETs in the designed circuit except the M_R operate in the sub-threshold region and the MOSFET resistor M_R operates in deep-triode region.

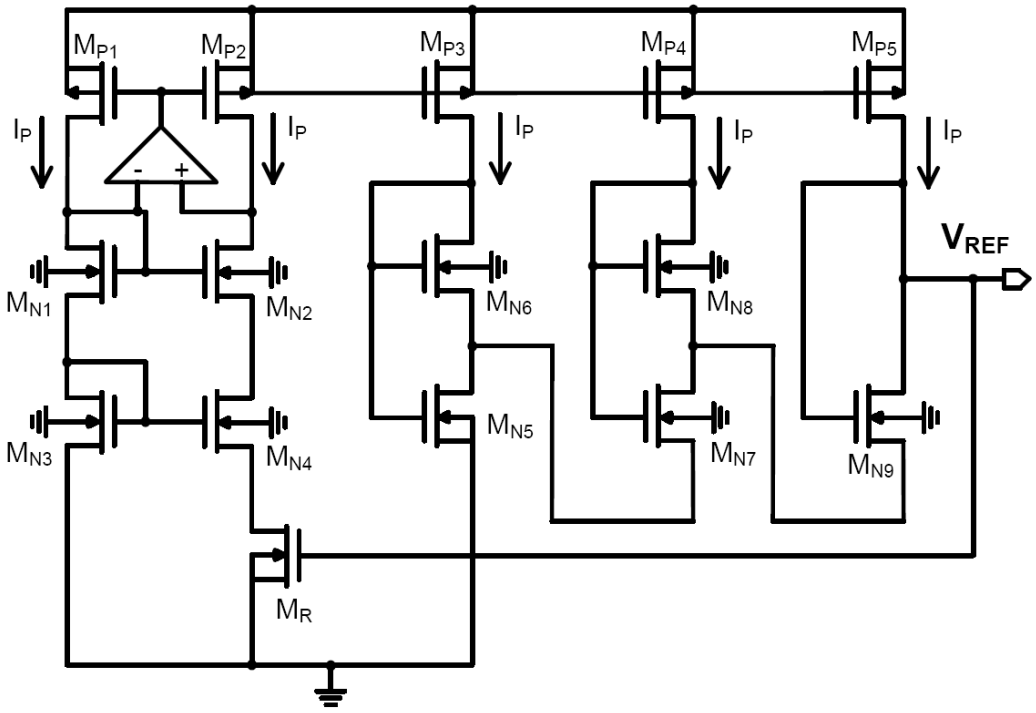


Figure 3.21: Schematic of the voltage reference designed in TSMC 90nm CMOS [69].

The operation principle of the circuit can be explained by considering the sub-threshold operation of the transistors. The current expression of a MOS at sub-threshold region can be expressed as:

$$I_D = KI_0 exp\left(\frac{V_{GS} - V_{TH}}{mV_T}\right) \tag{3.7}$$

where K is the aspect ratio of the transistors (W/L), $I_0 (= \beta(m-1)V_T^2)$ is the process dependent parameter, V_T $(= k_B T/q)$ is the thermal voltage, V_{TH} is the threshold voltage of a MOSFET, and m is the sub-threshold slope factor. The current generated by the current source (I_P) is determined by ratio of size of the current mirror transistor pair (M_{N3} and M_{N4}) and the resistance of MOS resistor M_R which takes feedback from reference voltage. Hence, the expression of the generated current is derived as:

$$I_P = \beta(V_{REF} - V_{TH})mV_T \ln\left(\frac{K_{MN4}}{K_{MN3}}\right) \tag{3.8}$$

where $\beta (= \mu_n C_{ox})$ is the current drive strength. In the bias-voltage sub-circuit, the gate-to-source voltages of the transistors (M_{N5} through M_{N9}) and the reference voltage form a closed loop, so it can be expressed as:

$$\begin{aligned} V_{REF} &= V_{GS,MN5} - V_{GS,MN6} + V_{GS,MN7} - V_{GS,MN8} + V_{GS,MN9} \\ &= V_{GS,MN5} + mV_T \ln\left(\frac{2K_{MN6}K_{MN8}}{K_{MN7}K_{MN9}}\right) \end{aligned} \tag{3.9}$$

where,

$$V_{GS,MN5} = V_{TH} + mV_T \ln(3I_P/K_{MN5}I_0) \quad (3.10)$$

As the Equations (3.9) and (3.10) imply the reference voltage is completely independent of the supply voltage. The voltage reference equation has two components, one of them is related with V_{TH} and the other is related with V_T. Temperature dependences of V_{TH} and V_T have negative and positive signs, respectively; therefore a constant reference voltage with very low temperature dependence can be arranged by adjusting size of the transistors. The threshold voltages of the source coupled transistor pairs (M_{N6}-M_{N7} and M_{N8}-M_{N9}) cancel each other as can also be observed from Equation (3.9). The temperature dependence of V_{TH} can be expressed as:

$$V_{TH} = V_{TH0} - \kappa T \quad (3.11)$$

where V_{TH0} is the threshold voltage of the transistor at 0 K, and, κ is the temperature dependence of V_{TH}. On the condition that mV_T and $(V_{REF}\text{-}V_{TH0}) << \kappa T$, temperature coefficient of the reference voltage is:

$$\frac{dV_{REF}}{dT} = -\kappa + \frac{mk_B}{q} \ln\left\{\frac{6qm\kappa}{k_B(m-1)} \frac{K_R K_{N6} K_{N8}}{K_{N5} K_{N7} K_{N9}} \ln\left(\frac{K_{MN4}}{K_{MN3}}\right)\right\} \quad (3.12)$$

Therefore, by adjusting size of the transistors temperature coefficient of the reference voltage can be equated to zero ($dV_{REF}/dT=0$). The reference voltage when this condition is satisfied, is given by

$$V_{REF} = V_{TH0} \quad (3.13)$$

Therefore, threshold voltage of M_{N5} at absolute zero temperature is generated as the reference voltage. Figure 3.22 presents the opamp circuit which is used to improve the sensitivity of the PMOS current mirrors at the circuit. The circuit is composed of a single stage differential amplifier and operates in sub-threshold region.

Table 3.5 shows the design parameters of the designed sub-threshold voltage reference circuit. Since low voltage operation is considered low threshold transistors are utilized at the circuit.

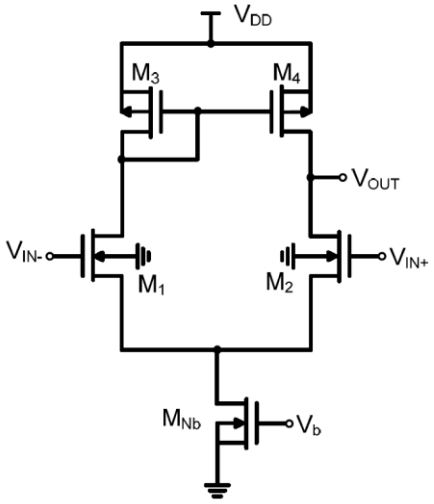


Figure 3.22: The single stage sub-threshold opamp which is designed and utilized in voltage reference.

Table 3.5: Design parameters of the sub-threshold voltage reference (Figure 3.21 and Figure 3.22).

Transistor	**W/L**
M_{P1} - M_{P5}	10 µm / 10 µm
M_{N1}, M_{N3}	3 µm / 0.1 µm
M_{N2}, M_{N4}	60 µm / 0.1 µm
M_{N5}, M_{N7}, M_{N9}	6 µm / 3 µm
M_{N6}, M_{N8}	40 µm / 0.5 µm
M_R	0.5 µm / 20 µm
M_{Nb}	0.5 µm / 3 µm
M_1 - M_2	2 µm / 2 µm
M_3 - M_4	0.2 µm / 10 µm

Figure 3.23 shows the simulation result of the voltage reference circuit for the varying supply voltages. The designed circuit gives about 478 mV reference voltage for supply voltages larger than 0.6 V. The variation of the reference voltage from 0.7 V to 2 V is in lower than ±1 mV. Figure 3.24 shows variation of the generated reference voltage with respect to the temperature. As the temperature has been swept from 0°C to 75°C the change at the reference voltage is in the range of ±5 mV. The maximum power dissipated by the sub-threshold reference circuit is around 0.75 µW.

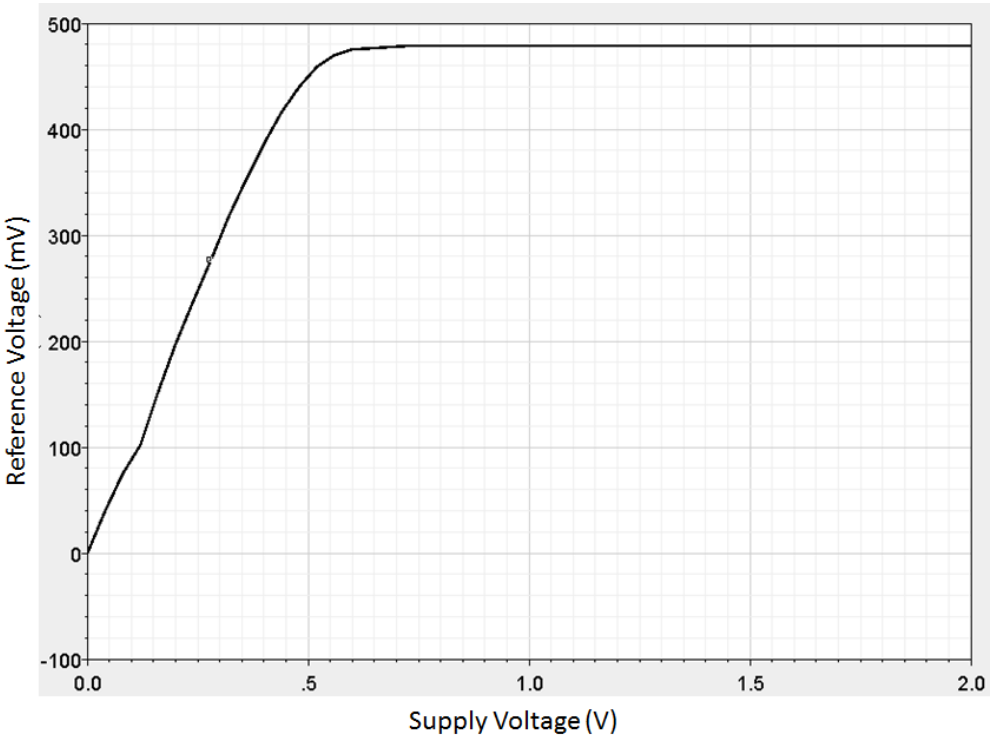


Figure 3.23: Change of the reference voltage with the supply voltage.

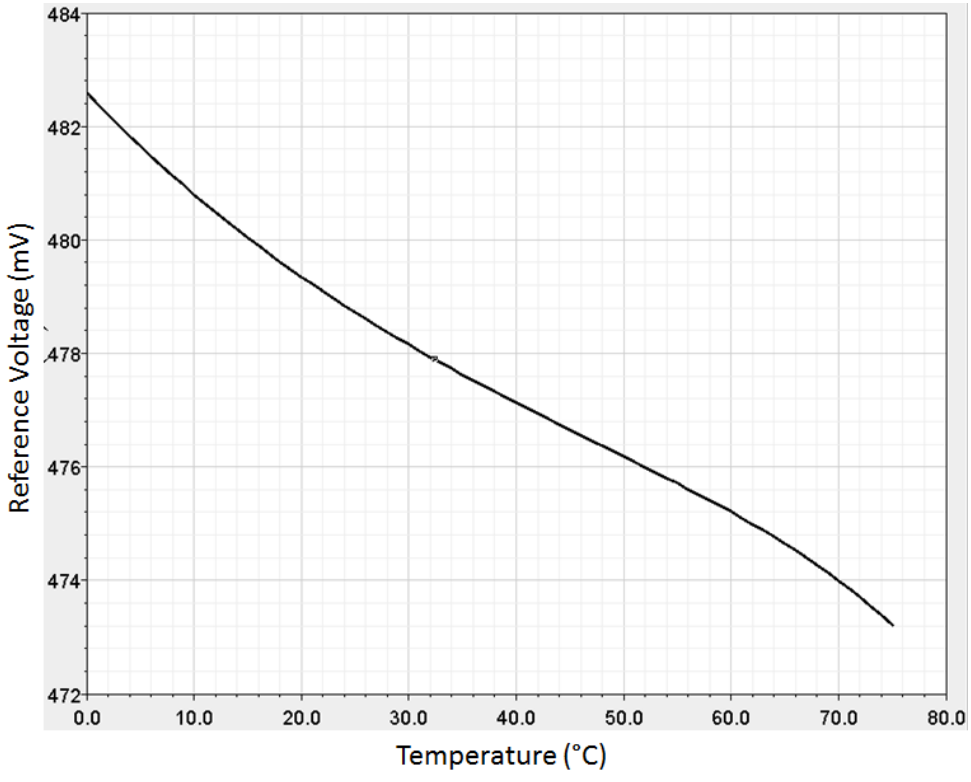


Figure 3.24: Change of the reference voltage with the temperature.

For the voltage divider of the regulator block diode connected PMOS transistors as shown in Figure 3.20 are used. Since only two series transistors are used at the circuit high threshold transistors are utilized to minimize the power consumption of the circuit. Besides, aspect ratios of these transistors are decreases as low as possible and arranged to get about 478 mV output at 1 V supply voltage. Aspect ratios of the upper and lower transistors are 0.25 µm/20 µm and 0.4 µm / 10 µm, respectively. Figure 3.25 demonstrate the variation of the voltage divider output with the supply voltage. As expected the output of the voltage divider changes linearly with the supply voltage. The maximum power dissipation of the voltage divider circuit is 5 nW which is pretty good for low voltage applications.

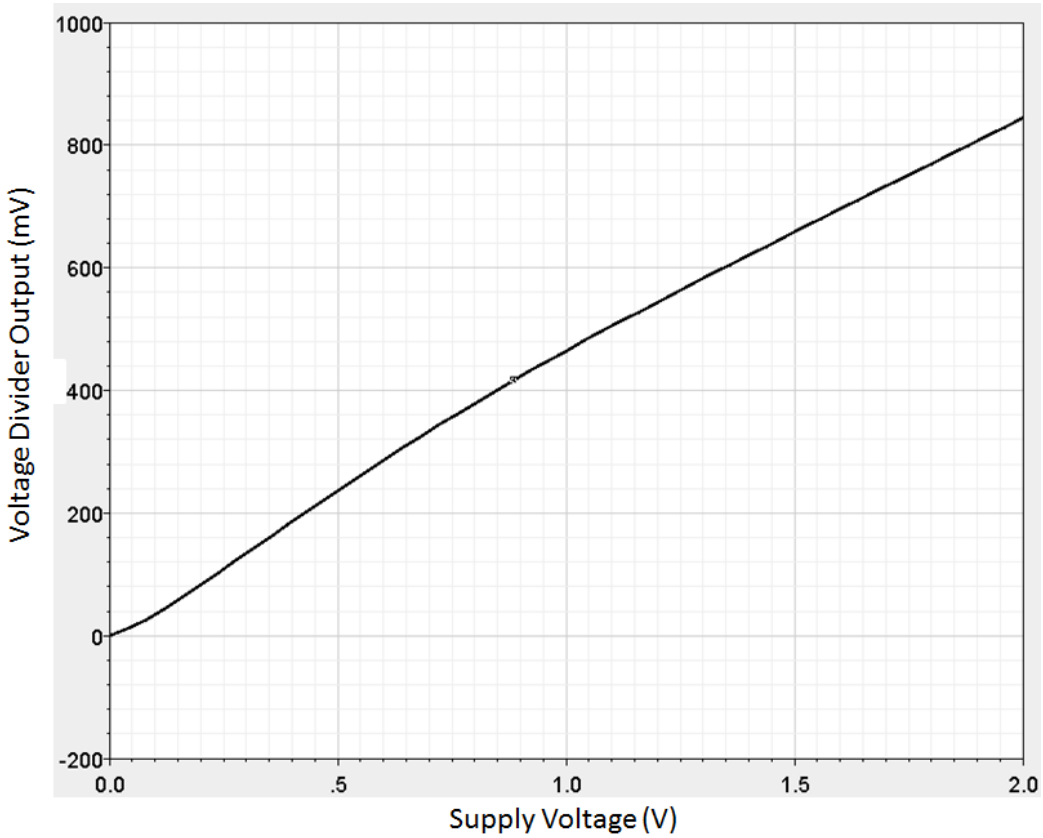
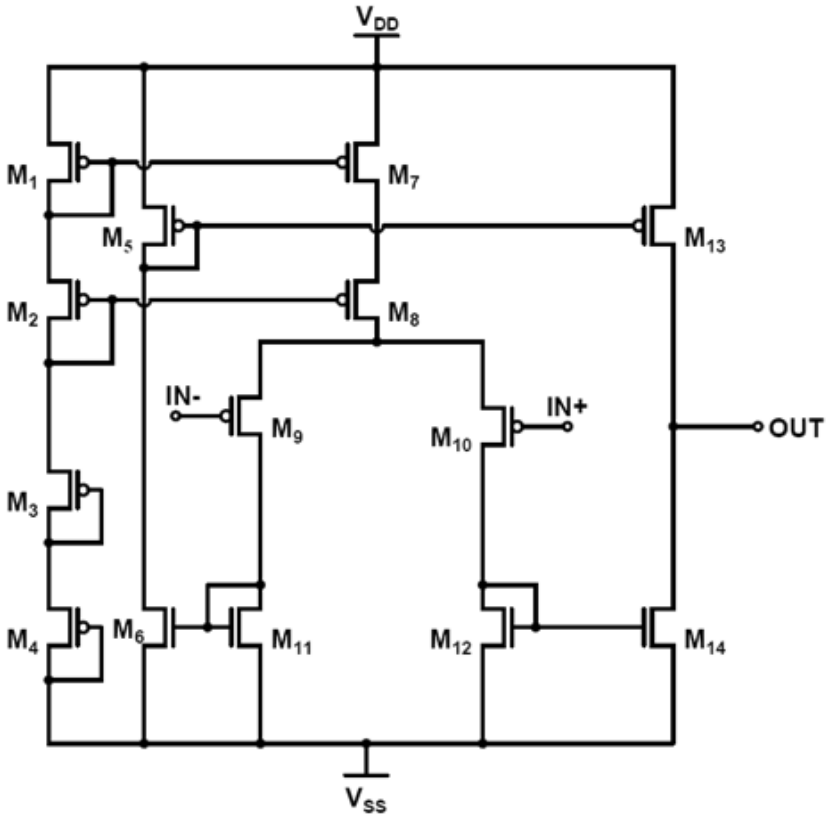


Figure 3.25: Variation of the voltage divider output with the supply voltage.

The final block of the voltage regulator block is an error amplifier which compares the voltage reference and voltage divider outputs and gives feedback to the oscillator for regulation. Figure 3.26 presents schematic of the low voltage comparator circuit designed for the regulation block. Since N-Well process is used, the comparator is designed by PMOS input transistors that reduce the input offset by connecting their bulk terminal to their source. A cascade current mirror is utilized to generate the tail current of the input stage. Hence, higher output resistance is obtained which leads to better common mode rejection ratio for the comparator. A simple diode-connected ladder is used to produce reference current, because supply voltage for this comparator is known and the desired bias current can be produced by proper sizing of diode-connected PMOS transistors. The current mirror active load structure is chosen as the output stage and the

gain enhancement is achieved by means of current scaling at the mirror transistors. As a result a low power high gain comparator circuit is designed as the error amplifier. Table 3.6 presents aspect ratio of the transistors utilized at the comparator circuit. To minimize the leakage at the transistors high threshold transistors are utilized.



*Designed by Kaveh Gharehbaghi.

Figure 3.26: Schematic of the comparator circuit utilized at the regulation.

Table 3.6: Design parameters of the comparator circuit utilized at regulation.

Transistor	**W/L**
M_1, M_2	5 µm / 0.1 µm
M_3, M_4	0.2 µm / 5 µm
M_5, M_{13}	35 µm / 0.5 µm
M_6	15 µm / 0.5 µm
M_7, M_8	10 µm / 0.1 µm
M_9, M_{10}	4 µm / 1 µm
M_{11}, M_{12}	2 µm / 0.5 µm
M_{14}	30 µm / 0.5 µm

Figure 3.27 presents the simulation result of the regulator block, which demonstrates the operation principle. As explained earlier, the voltage reference and voltage divider outputs are compared with the comparator. At low supply voltages the reference voltage is higher than divided output voltage. Hence the comparator gives low voltage which means the oscillator is working with full power. When the supply voltage reaches to the desired value (1 V for this work) the divider output starts to exceed the reference voltage. Hence, the comparator output started to increase and decrease the bias current of the oscillator. After about 1.2 V the regulator output is completely triggered to supply voltage which leads to completely turn OFF the oscillator circuit. The slight offset at the triggering voltage is to provide a safety margin to the circuit.

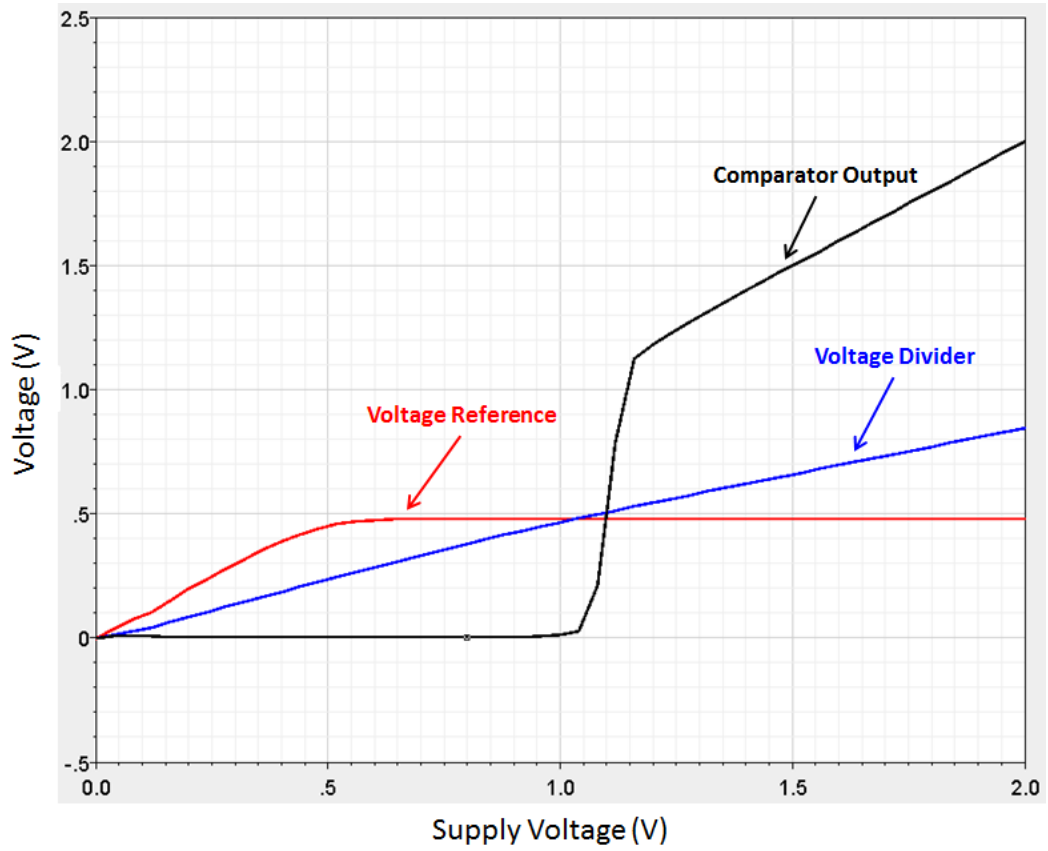


Figure 3.27: Simulation result of the comparator block for varying supply voltage.

After all the sub-blocks are designed they are combined to observe the performance of the overall circuit. Figure 3.28 presents the transient simulation results of the overall circuit for 0.25 V input peak voltage, 10 Hz input frequency, 1 MΩ output load resistance, and 5 nF output storage capacitor. As expected, the circuit converts the input AC voltage to to DC and stabilize it at 1 V DC voltage and this is the lowest reported voltage that a self-powered and fully-integrated interface electronics can operate. Similarly, Figure 3.29 presents the transient simulation result of the circuit for the same load conditions and with 0.35 V input peak voltage.

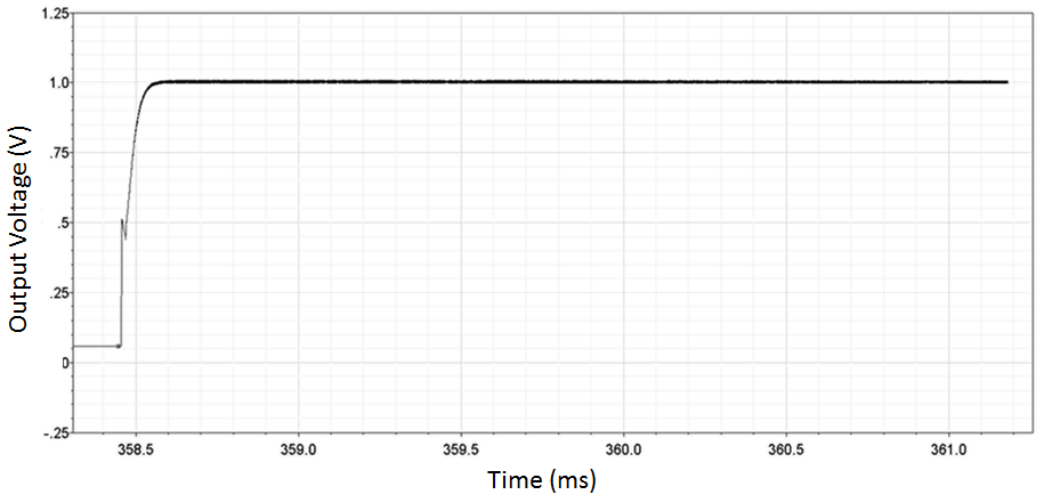


Figure 3.28: Transient simulation result of output voltage of the overall circuit with 0.25 V input peak voltage, 1 MΩ output load resistance, and 5 nF output storage capacitor.

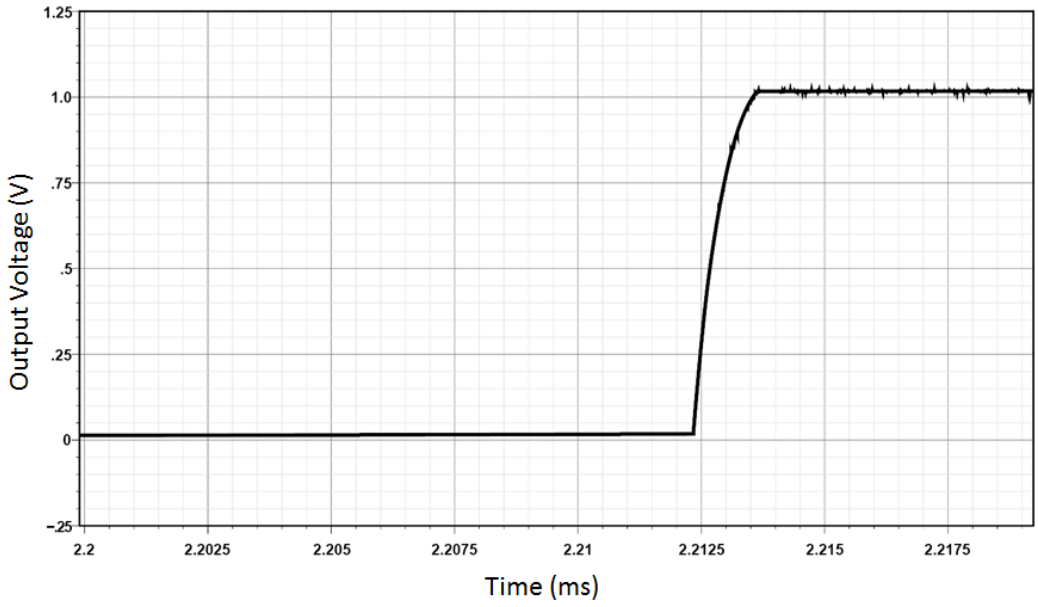


Figure 3.29: Transient simulation result of output voltage of the overall circuit with 0.35 V input peak voltage, 1 MΩ output load resistance, and 5 nF output storage capacitor.

Figure 3.30 presents layout of the overall circuit drawn at TSMC 90 nm CMOS technology. The area occupied by the circuit is 200 µm x 200 µm. The overall layout of the chip which also includes sub-block of the circuit is shown at Figure 3.31. The sub-block of the circuit is also added to overall chip to test the circuit more precisely.

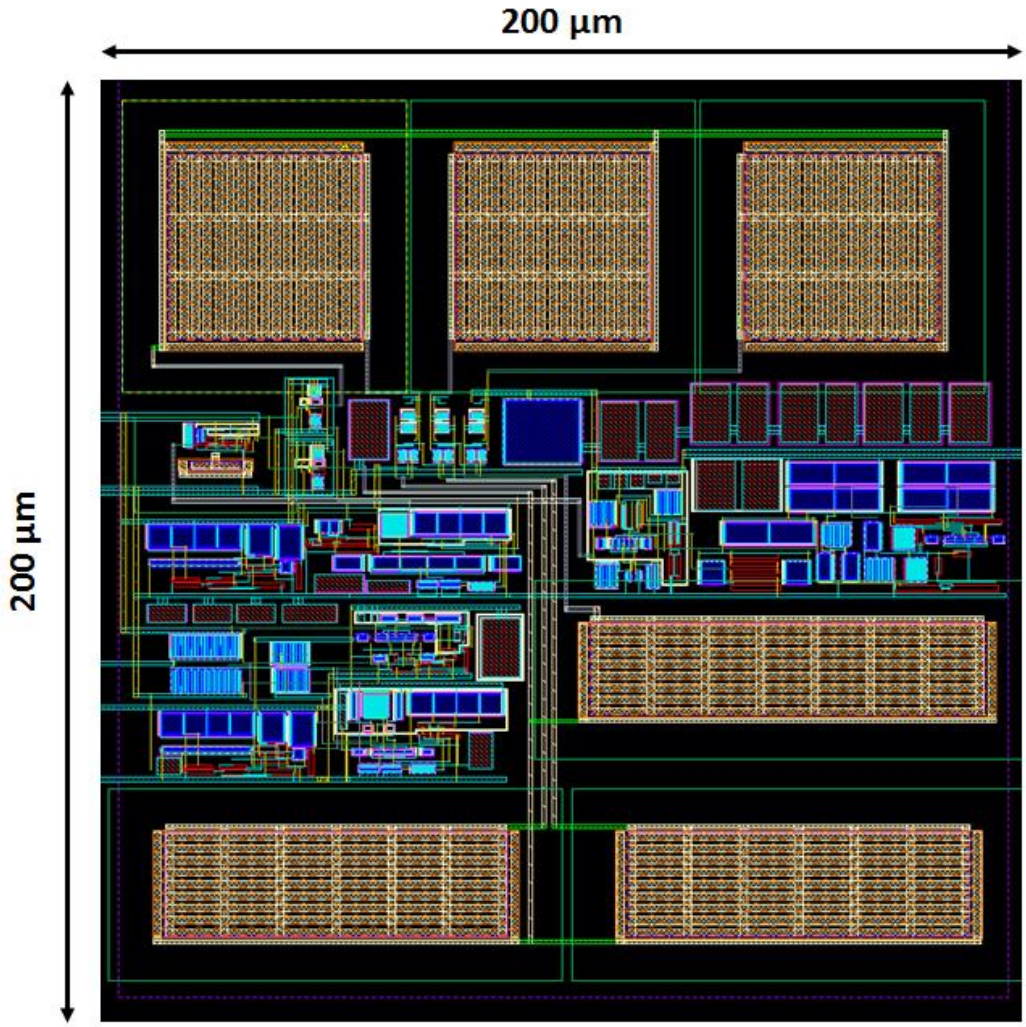


Figure 3.30: Overall layout of the designed TSMC 90 nm circuit.

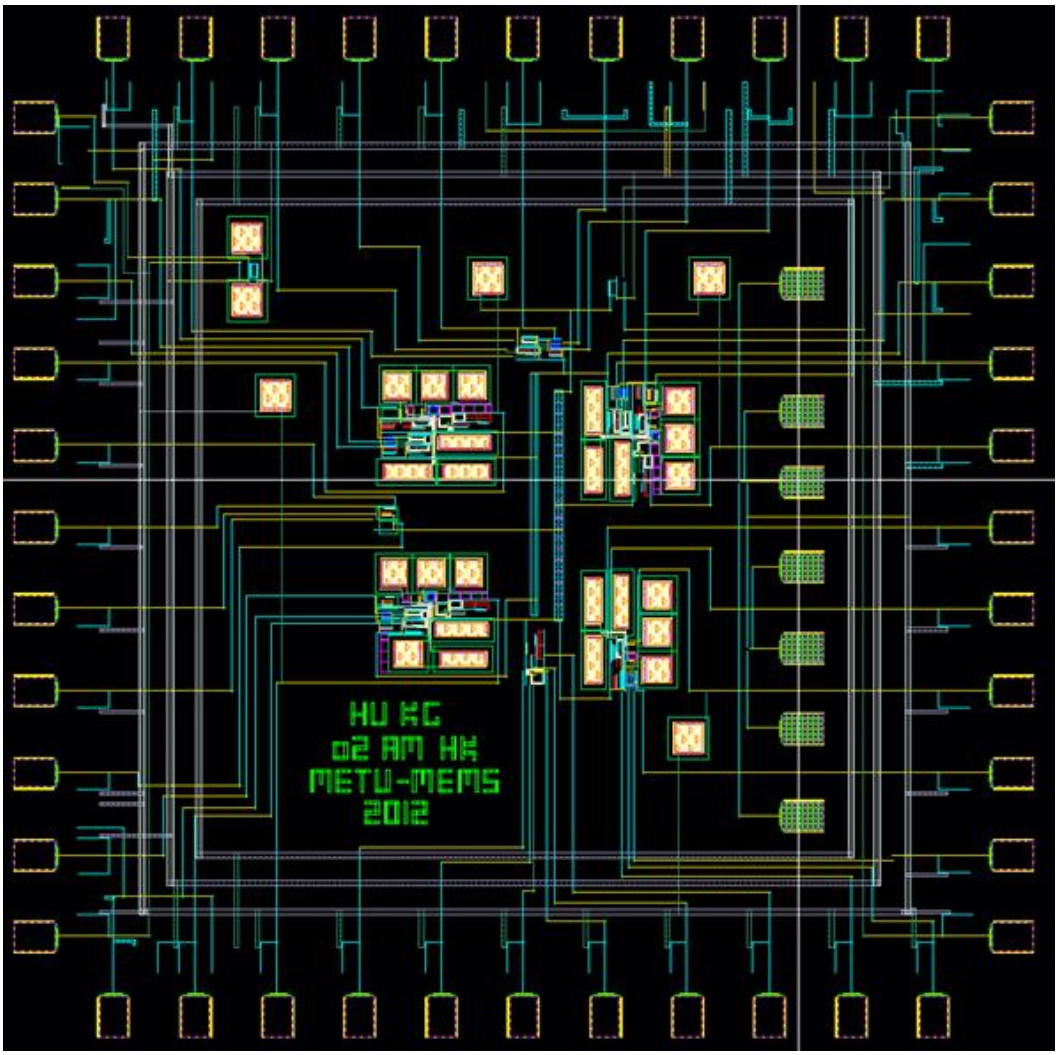


Figure 3.31: Overall layout of the chip that also includes test circuits.

3.5. Summary of the Chapter

In this chapter, the theory, design and simulation results of the proposed interface circuit for low voltage electromagnetic energy harvesting applications has been presented. The demonstrated architecture includes a complete system for energy harvesting applications and designed in TSMC 90 nm CMOS technology. The discussed design blocks in this chapter are, self-power low voltage active rectifier, fully integrated low power DC/DC converter block with charge pump and oscillator sub-blocks, and a low voltage sub-threshold voltage regulator block. The operation principles and performance of each of the sub-blocks are demonstrated with simulations. The proposed IC is a novel solution to be interfered to low voltage and low power micro power generators.

CHAPTER 4

THE EXPERIMENTAL TEST RESULTS

This chapter presents experimental measurements of the fabricated interface electronics and the energy harvesting system that is prepared to test the designed IC. The design and mechanical characterization of the energy harvester prototype is also explained in this chapter. Besides, test results of energy harvesting IC sub-blocks under different excitation characteristics have been demonstrated. Finally, problems encountered after the fabrication of the designed chip and their possible solutions is explained.

Section 4.1 describes block diagram of the energy harvesting system and presents the electromagnetic energy harvester prototype that is used to test the designed interface circuit. Section 4.2 explains the measurement results of the designed active rectifier circuit and compares it with a previously reported structure. Section 4.3 presents the test results of combination of the AC/DC and DC/DC converters. Section 4.4 depicts results obtained from sub-threshold voltage regulator part and verifies problems at the fabricated energy harvesting interface electronics. Finally section 4.5 contains a summary of the chapter.

4.1. The Energy Harvesting System and the Energy Harvester Prototype

Figure 4.1 depicts block diagram of the test setup that is utilized to test the proposed interface electronics. The system consists of an EM energy harvester module, the interface circuit (IC), and an external output storage capacitor. The EM energy harvester module converts the kinetic energy extracted from the ambient vibrations to electrical energy. The incoming kinetic energy is generated via a vibration table which can generate various vibrations at different excitation levels. The generated electrical energy is induced on the coil of the EM energy harvester and used to feed the interface circuit. The interface circuit converts the generated AC voltage into a desired DC value by using the structure explained in Chapter 3. The converted DC signal is stored on a storage capacitor and used to drive a resistive load. As a result a compact energy harvesting system is prepared which means that whole the power needed by the interface electronics is supplied from the energy harvester.

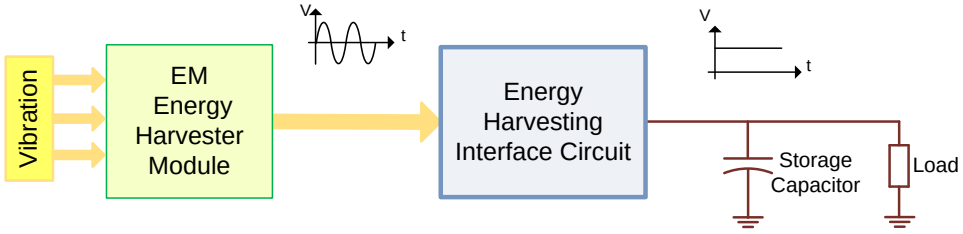
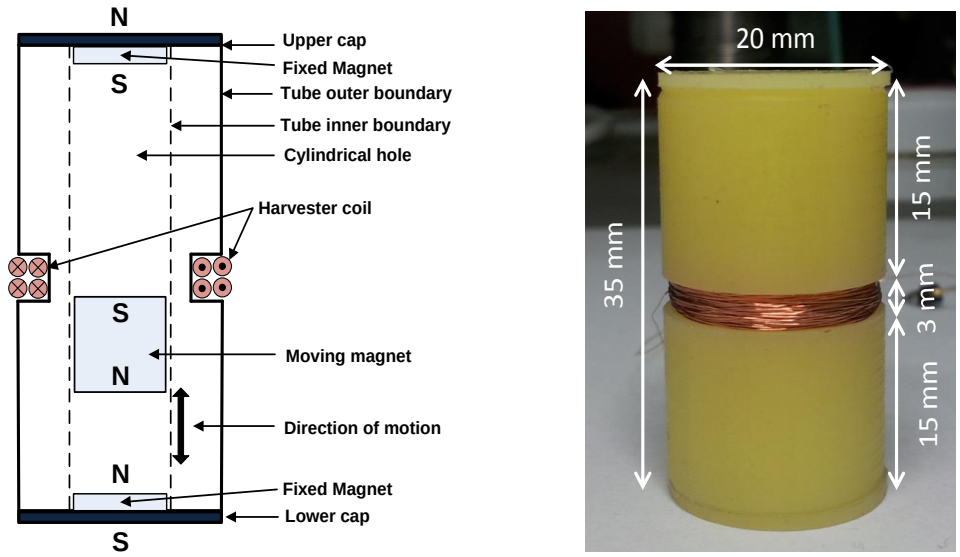


Figure 4.1: The energy harvesting system utilized to test the proposed interface circuit.

A modified version of a simple and low cost EM energy harvester module [42] is utilized as the power source of the system[64]. Figure 4.2 presents schematic of the EM energy harvester module and picture of the fabricated prototype. The prototype is composed of a cylindrical tube package, two fixed magnets (5.3 mm x 5.3 mm x 0.5 mm) at upper and bottom caps, and a free moving magnet (7.5 mm x 7.5 mm x 7.5 mm). The free magnet is suspended in the air inside the tube by the effect of magnetic field developed by the fixed magnets. A pick-up coil is wounded around the designated cavity on the outer boundary of the tube. When a vibration is applied towards the tube axis, the fixed magnet starts to move and an induced voltage is generated across the coil according to Faraday's law of induction.

The energy harvester has 11 mm and 20 mm inner and outer diameters, respectively. Length of the prototype is kept at 35 mm which is shorter than regular AA size battery. The harvester coil wound around the tube has 500 turns and has 180 Ω internal resistance.



(a) (b)

Figure 4.2: (a) Schematic of the EM energy harvester prototype and (b) fabricated energy harvester prototype.

When the free magnet moves inside the tube several forces are acting on it, which are: the external force applied to the system $\vec{F}_{ext}$, the gravitational force $m\vec{g}$, magnetic repulsion force resulting from the interaction between two fixed magnets $\vec{F}_{mag}$ (resultant force coming from both of the magnets), frictional force between the magnet and the tube walls $\vec{F}_{fric}$, electromagnetic damping force coming from magnetic field generated by the coil $\vec{F}_{b,coil}$, and the damping force generated by the air $\vec{F}_{b,air}$. Hence, the net force on the magnet can be expressed as:

$$\vec{F}_{net} = \vec{F}_{ext} + m\vec{g} + \vec{F}_{mag} + \vec{F}_{fric} + \vec{F}_{b,coil} + \vec{F}_{b,air} = m\vec{a}(t) \tag{4.1}$$

where m is the mass of the free moving magnet, $\vec{g}$ is the gravitational acceleration, and $\vec{a}(t)$ is the instantaneous acceleration of the magnet. The forces acting on the magnet must be optimized to increase the efficiency of the energy conversion, such that effect of the undesired components like the friction force and the air damping force must be minimized. A cube magnet is utilized inside the tube to decrease the effect of friction between the walls of tube; however this change also decreases the effect of magnetic field. Hence, size of the moving magnet must be chosen properly. Moreover, extra holes are opened at the top and bottom caps.to decrease the air damping force.

The operation frequency range of the transducer is determined by size of the magnets which effects strength of the generated magnetic field, mass of the free moving magnet, and length of the tube which limits the distance that the magnet can move and affects the resultant magnetic force. Besides, during regular operation, the free magnet moves accurately inside the tube; however, if a high external force is applied to the system, this will cause the free magnet to crash the upper or lower caps. With such a crash an extra force is applied on it and this also affect performance of the system.

For the energy harvester prototype with the properties given above the frequency of operation is between 8 to 15 Hz. Figure 4.3 presents the test results of the given energy harvester at different peak-to-peak vibration amplitudes at a frequency range of 8 to 15 Hz. The vibration to the system is given with a vibration table and peak-to-peak output voltage of the energy harvester is observed with an oscillator. The results show that resonance frequency of the system slightly increases with the increasing vibration amplitude and for 1 mm to 2.5 mm peak-to-peak vibration amplitudes it changes between 11.5 Hz to 13 Hz.

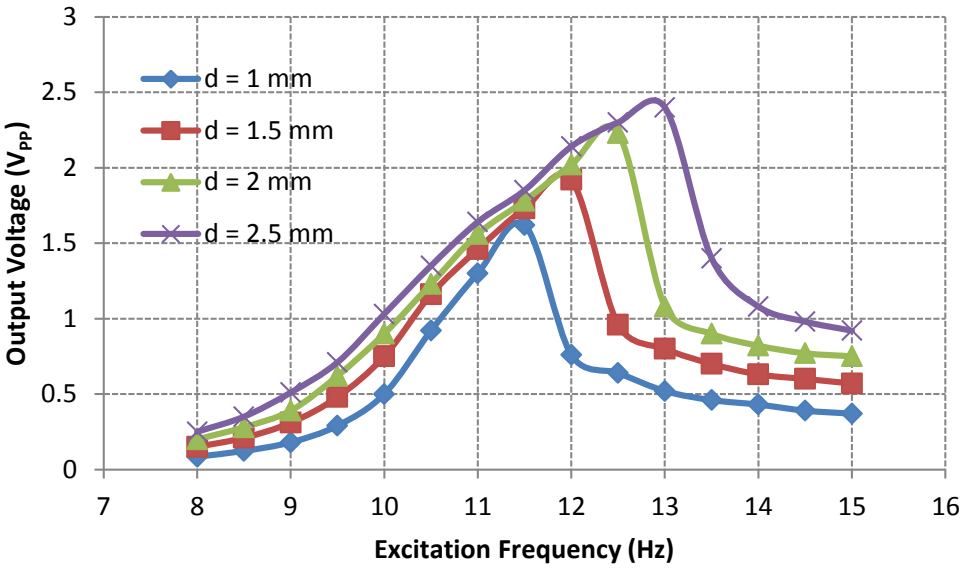


Figure 4.3: Peak-to-peak value of the harvested AC voltage versus the vibration frequency at different vibration displacements.

Figure 4.4 presents harvested AC voltage from the EM energy harvester for 10 Hz frequency, 2.5 mm peak-to-peak vibration amplitude and 0.5g acceleration. The harvested peak to peak output voltage for the given conditions is 0.82 V and its shape is slightly different than sinusoidal waveform due to the other forces acting on the free moving magnet.

Figure 4.4: Harvested AC voltage from the EM energy harvester for 10 Hz frequency, 2.5 mm peak-to-peak vibration amplitude and 0.5g acceleration.

4.2. Verification of the Designed Active Rectifier

Figure 4.5 presents the energy harvesting system used to test the designed active rectifier (AC/DC doubler) and compare it with a previously reported rectifier circuit. The well-known gate cross-coupled rectifier (GCCR) circuit is also fabricated on the same chip with the same technology for a fair comparison.

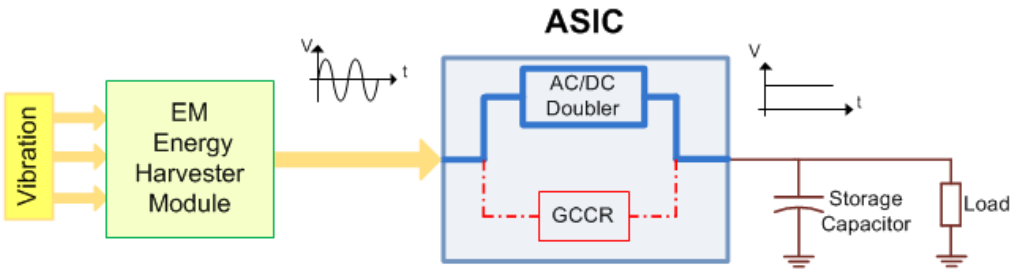


Figure 4.5: Block diagram of the energy harvesting system used to test the designed active rectifier circuit.

Figure 4.6 shows the test setup that is used at the test of the system where vibration input of the system is generated by the vibration table. The vibration table is supplied from the controller and amplifier which are controlled by the software running on a computer. The controller takes feedback from the shaker with the help of an accelerometer to settle the vibration at the desired condition.

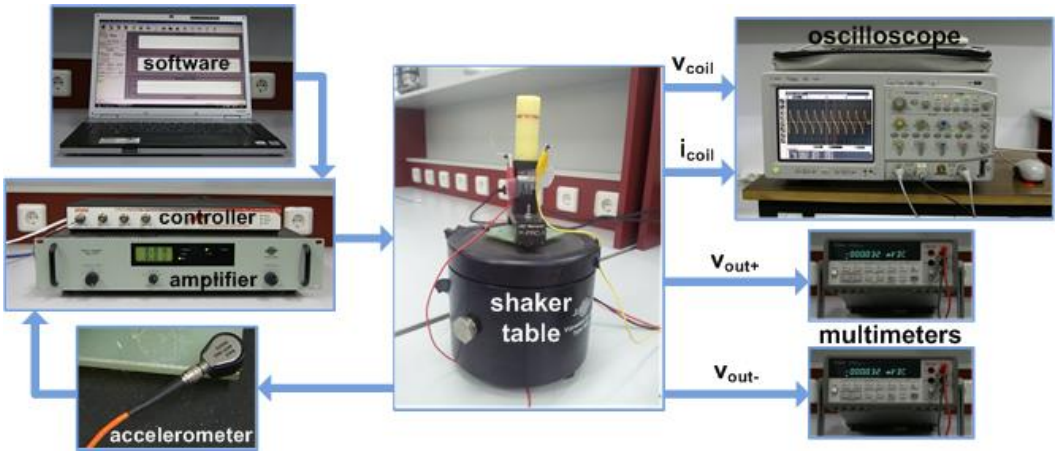


Figure 4.6: Test setup and the devices used at the setup.

The generated AC voltage and the current drawn from the harvester are observed with an oscilloscope and the harvested power is calculated. To calculate the total input power the instantaneous AC voltage and the instantaneous current must be multiplied and averaged for one period. The expression of the input power can be given as:

$$P_{in} = \frac{1}{T}\int_0^T V_{in}(t)\, I_{in}(t)dt \tag{4.2}$$

where $T(=1/f)$ is one period of input voltage, $V_{in}(t)$ is the instantaneous input voltage, $I_{in}(t)$ is the instantaneous current drawn from the harvester and t is the time. Since the output voltage of the rectifier system is dual rail, the output voltage of the rectifier is measured with the help of two multimeters like shown in the figure. The output voltage can be calculated by taking the difference of positive and negative output voltages:

$$V_{out} = V_{out+} - V_{out-} \tag{4.3}$$

The load current drawn by the system (I_{out})is calculated by using the load resistance as shown in Equation (4.4). The total output power of the system can be calculated by using the output voltage and output current.

$$I_{out} = \frac{V_{out}}{R_{Load}} = \frac{V_{out+} - V_{out-}}{R_{Load}} \tag{4.4}$$

$$P_{out} = I_{out} \times V_{out} = I_{out} \times (V_{out+} - V_{out-}) \tag{4.5}$$

The power conversion efficiency of the interface circuit is the ratio of total output power and the harvested input power.

$$Power\ Conversion\ Efficiency\ [\%] = \frac{P_{out}}{P_{in}} \times 100 \tag{4.6}$$

A test board is designed on a PCB to get more precise results from the chip. Figure 4.7 presents the designed PCB which is ready for test. The designed chip requires some extra components like the storage capacitors or the load resistance. The prepared test PCB includes spaces that these components are mounted. Moreover, testing the circuit on a PCB instead of a breadboard also helps to decrease the effects of parasitic components coming from the test setup.

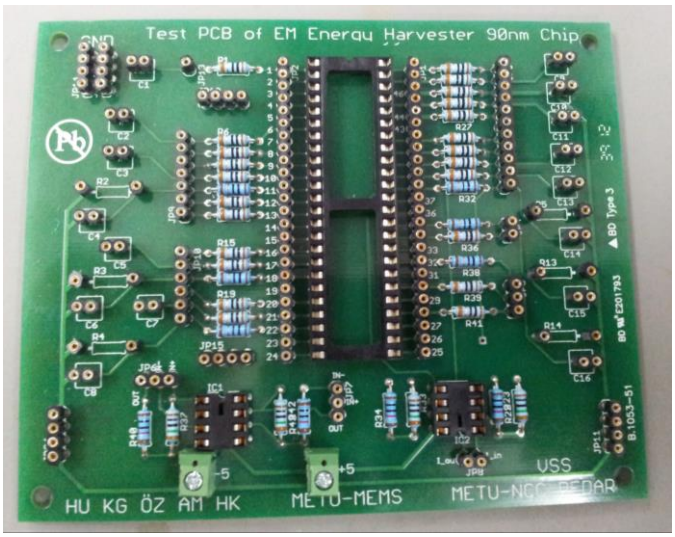


Figure 4.7: Designed test PBC for the TSMC 90 nm chip.

Figure 4.8 shows the prepared test setup for the implemented TSMC 90 nm CMOS chip which is placed on the test PCB. The input voltage of the circuit comes from the EM energy harvester that is excited with the vibration table.

Figure 4.8: The test setup of the TSMC 90 nm chip with the test PCB and the energy harvester.

Figure 4.9 shows the input voltage generated by the EM energy harvester prototype and the rectified positive and negative output voltages of the active rectifier circuit for 10 Hz vibration frequency with 2.5 mm peak-to-peak amplitude corresponding to 0.5 g peak

acceleration. Although the peak output voltage is observed at around 13 Hz, the vibration frequency is chosen as 10 Hz for the tests to observe the low voltage performance of the circuit. The circuit generates a DC output (V_{out+} - V_{out-}) which is close to the peak to peak value of the input AC signal. For the given conditions the harvested peak-to-peak AC voltage is 0.82 V and the rectified output voltage is 0.8 V. The voltage drop at the output is only about 20 mV which is considerably low compared to voltage drops coming from passive diode structures.

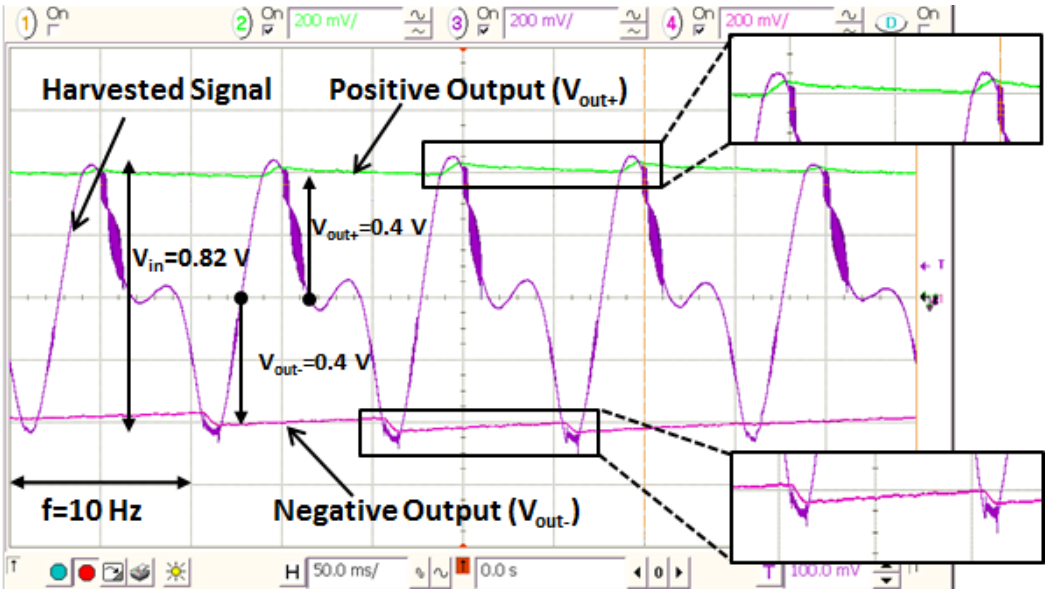
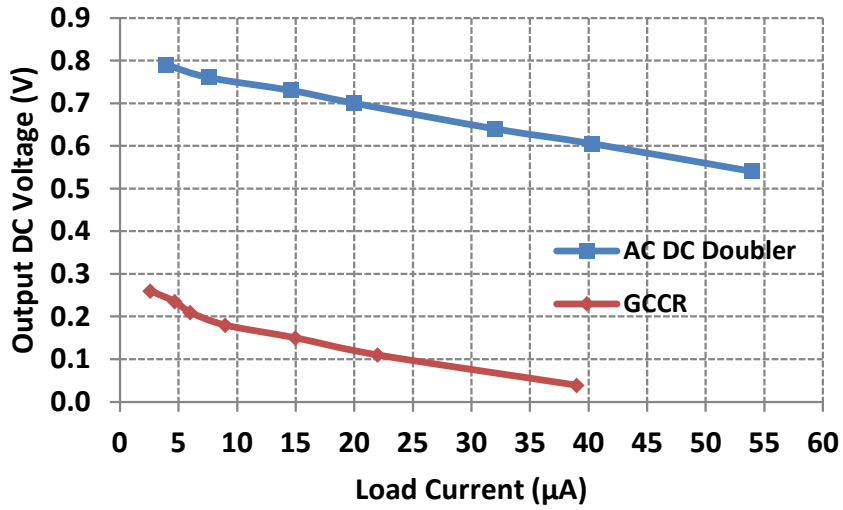
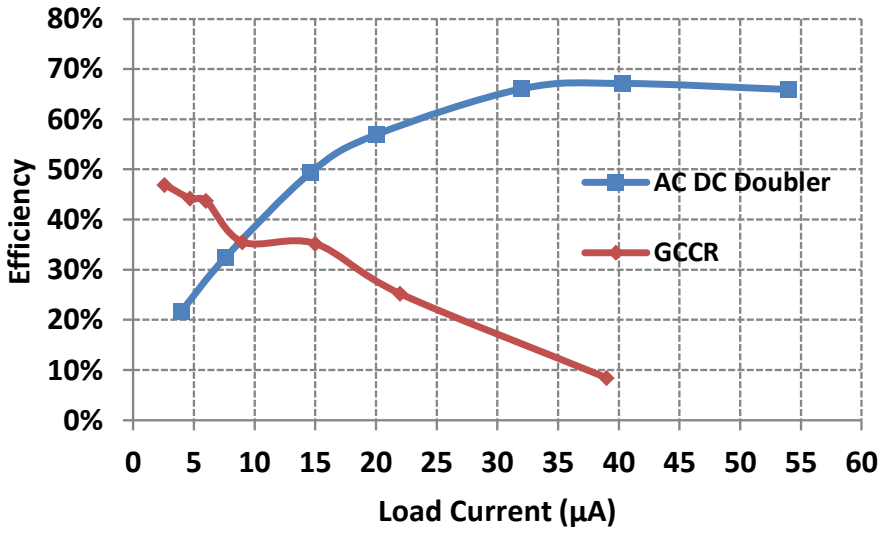


Figure 4.9: The positive and negative output DC voltages of the AC/DC Doubler circuit and the input AC voltage coming from the EM energy harvester for 0.5 g peak acceleration.

As depicted earlier both AC/DC doubler and the GCCR circuits are fabricated on the same chip and tested by using the same EM energy harvester module. Figure 4.10 presents the power conversion efficiency and the output voltage comparison of the AC/DC doubler with the GCCR circuit versus the load current. The external vibration applied to the harvester is at 10 Hz frequency with 2.5 mm peak-to-peak vibration amplitude corresponding to 0.5 g peak acceleration. The improvement at the output voltage of the AC/DC doubler is more than three times larger than that of the GCCR. Although the GCCR circuit has higher efficiency at very low output current values, the AC/DC doubler is significantly more advantageous for applications with a higher current demand. The AC/DC doubler has more than two times better efficiency for load currents larger than 20 µA. Performance of the circuit at high load current is important because of the next stage of the circuit which is used to step-up the DC voltage level is much more power hungry compared to rectifier block.



(a)



(b)

Figure 4.10: a) Output DC Voltage and (b) Efficiency of the AC/DC Doubler and the GCCR circuits versus the load current for 10 Hz input frequency, 2.5 mm peak-to-peak vibration amplitude and 0.5g external acceleration profile.

The circuits are also tested with a signal generator to get a more precise control at the input peak voltage and compare the performance of the circuit at different input voltages. Figure 4.11 presents open load test result of circuits for 10 Hz input frequency. The output storage capacitors of the circuit are chosen as 47 µF. The AC/DC doubler provides about two times larger output compared to GCCR circuit at open load conditions. The AC/DC doubler is functional for input voltages as low as 100 mV.

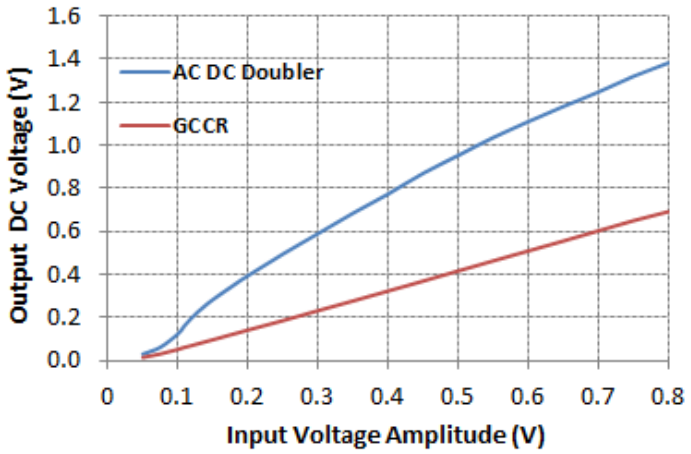


Figure 4.11: The output DC voltage versus the input voltage peak at 10 Hz input frequency and open load condition.

Figure 4.12 shows change of the rectified DC voltage of the proposed AC/DC doubler circuit with respect to the excitation frequency for 0.25 V input peak voltage and 47 µF storage capacitor. The circuit is able to operate properly up to 5 kHz without any problem, after 5 kHz the output voltage of the circuit is started to decrease and at 20 kHz the decrement at the output voltage is about 10% of the low frequency output. The main reason of the performance loss at high frequencies is, supply of the utilized comparator circuits at the active diodes is at low voltage levels since it is generated from the passive AC/DC doubler. Hence, bandwidth of the utilized comparators is in kHz range.

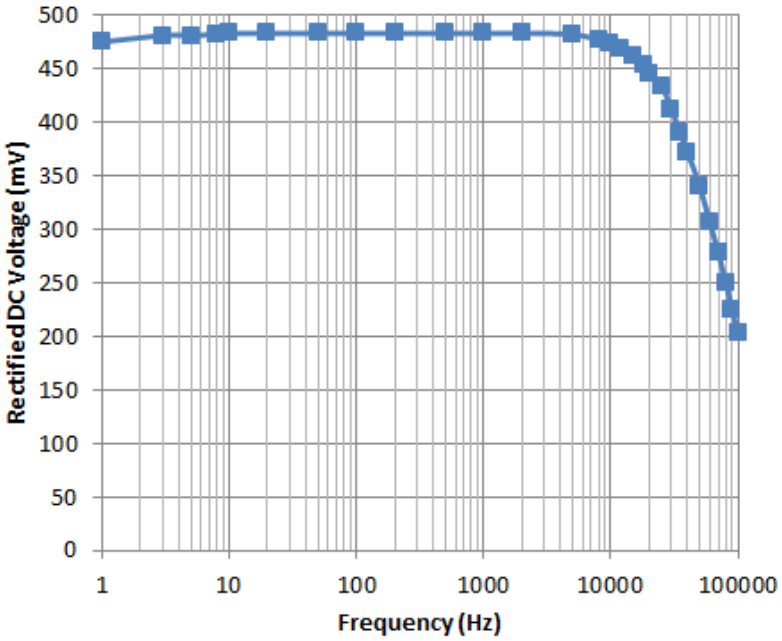


Figure 4.12: Change of the rectified DC voltage of the proposed AC/DC doubler circuit with respect to the excitation frequency for 0.25 V input peak voltage.

Table 4.1 shows the system specifications of the fabricated electromagnetic energy harvester prototype and the AC/DC doubler structure. With 2.5 mm peak to peak vibration at 10 Hz (corresponding to 0.5 g acceleration), 0.82 $V_{peak\text{-}to\text{-}peak}$ AC voltage is generated and rectified to 0.8 V DC with no load and to 0.61 V with 40 µA load, with the AC/DC doubler circuit.

Table 4.1: Specifications of the designed system.

Moving magnet dimension	7.5 mm x 7.5 mm x 7.5 mm
Fixed magnets dimension	5.3 mm x 5.3 mm x 0.5 mm
Saturation magnetization	1.2 T
Number of coil turns	500
Coil resistance	180 Ω
IC technology	TSMC 90 nm CMOS
Vibration conditions	2.5 mm peak to peak, 10 Hz, 0.5 g
Harvested AC voltage	820 $mV_{peak\ to\ peak}$
Max. DC output voltage	0.8 V @ no load
Max. power conversion efficiency	67% @ 0.61 V, 40 µA load
Min. operation voltage	100 mV peak

Table 4.2: Comparison of the designed rectifier with recently reported works.

Reference	**Min V_{in} [V_{peak}]**	**PCE_{max} [%]**	**Integration Level**	**External Supply**	**IC Technology**
[40]	0.005	90	Off-the-Shelf Components	+/- 1.25 V	-
[42]	0.200	81	IC + Discrete Components	Self Powered (+/- 1.5 V at minimum voltage)	0.35 µm
[70]	0.350	90	Off-the-Shelf Components	3.3 V Battery	-
This work	**0.100**	67	**Fully Integrated**	Self Powered	90 nm

Table 4.2 shows the comparison of the designed active rectifier circuit with other recently reported work. The minimum input amplitude required by the designed rectifier circuit is the lowest among self-powered implementations. Furthermore, the presented circuit is the only one providing a fully integrated rectifier alternative as an energy harvester interface. The minimum input voltage amplitude rectified by the circuit in [40] is an impressive 5 mV at 20 Hz. However, the circuit needs an external power

supply to operate. The system in [42] is previously designed by our group and fully-self powered system solution. However the minimum input voltage is higher than this work although it is supplied with +/- 1.5 V supply sources. Besides, the circuit is designed with off-chip components. The power conversion efficiency of the design presented in [70] is pretty good, but the minimum input voltage of the circuit is limited due to the use of off-the-shelf discrete components. As the most significant difference from the previously reported implementations, the proposed rectifier circuit in this work is fully integrated.

4.3. Test Results of the Unregulated System

The designed interface circuit is tested by removing the voltage regulator block to see the unregulated performance of the circuit. Figure 4.13 demonstrates block diagram of the unregulated interface circuit, where the AC/DC converter and DC/DC converter blocks are driven by the energy harvester prototype. The unregulated performance of the system is also an important parameter to see the minimum requirements for the circuit to reach the desired output voltage (1 V).

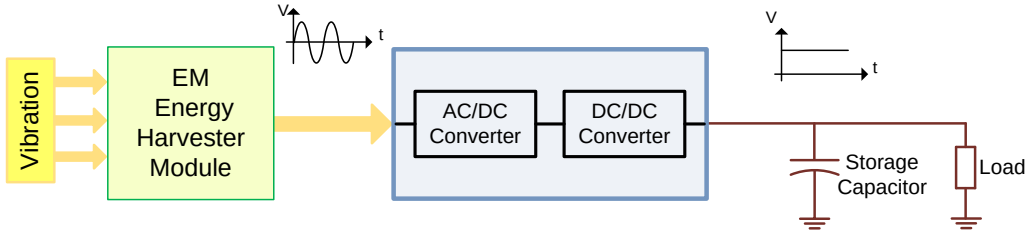


Figure 4.13: Block diagram of the unregulated energy harvesting system.

The test setup of the system is similar with the one given in previous section. A shaker table is utilized to generate the external vibration at the EM energy harvester prototype and the generated AC voltage and current is measured by the oscilloscope and the output voltage is observed with multimeters. The positive output of the circuit comes from output of the charge-pump circuit and the negative output comes from the active rectifier circuit.

Figure 4.14 shows the harvested AC signal and output of the unregulated system for 10 Hz frequency, 2.5 mm peak-to-peak vibration amplitude and 0.5g acceleration condition. The circuit is able to generate 2.48 V output voltage when the load resistance is 4.4 MΩ and the load capacitance is 1 µF. Ideally for 0.82 V peak-to-peak input voltage the circuit must give about 3.3 V output voltage, however voltage drop at the rectifier circuit and the finite load resistance causes to have about 2.5 V output voltage.

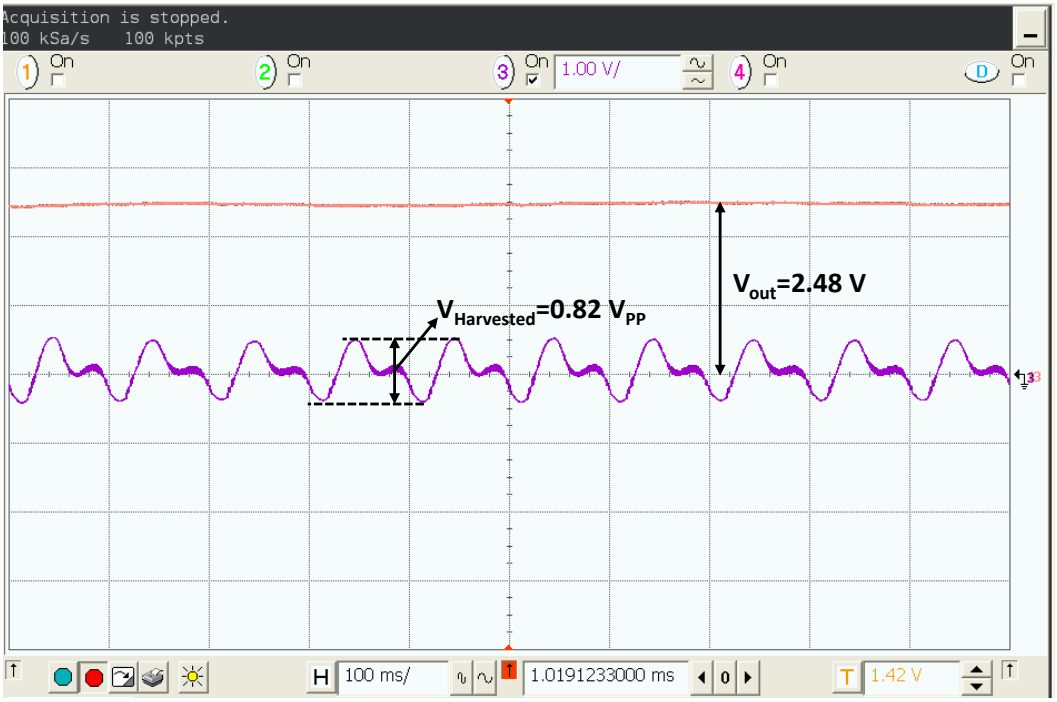
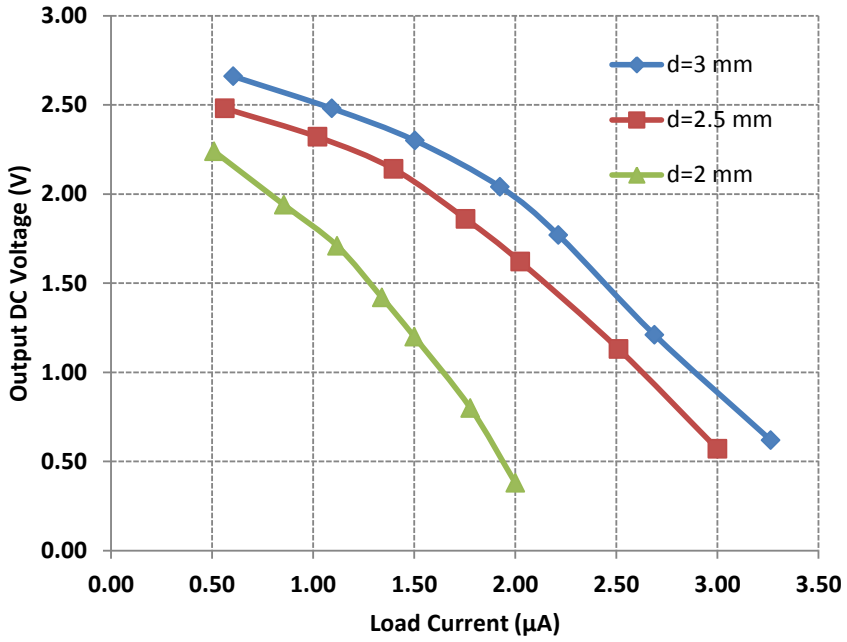


Figure 4.14: The harvested AC voltage and output of the unregulated system for 10 Hz frequency, 2.5 mm peak-to-peak vibration amplitude and 0.5g acceleration.

Performance of the unregulated system is tested at different excitation conditions. Figure 4.15 shows change of the output voltage and the power conversion efficiency of the unregulated circuit for varying load current at different vibration conditions. The system is tested at 10 Hz vibration frequency and 2 mm (0.4g acceleration), 2.5 mm (0.5g acceleration), and 3 mm (0.6g acceleration) peak-to-peak vibration amplitude conditions. The storage capacitors of the rectifier circuit are chosen as 47 µF and the storage capacitor at the output is utilized as 1 µF.



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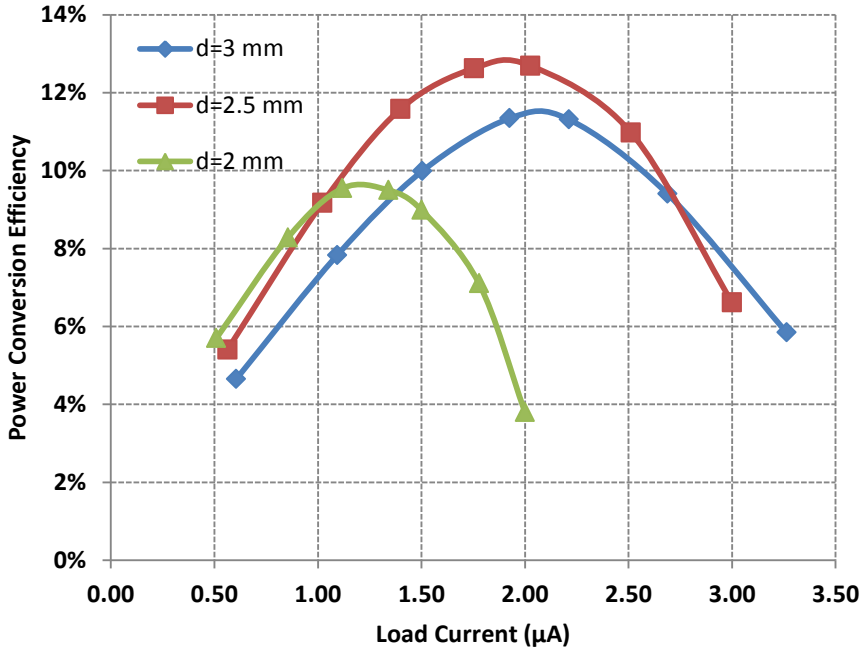


(b)

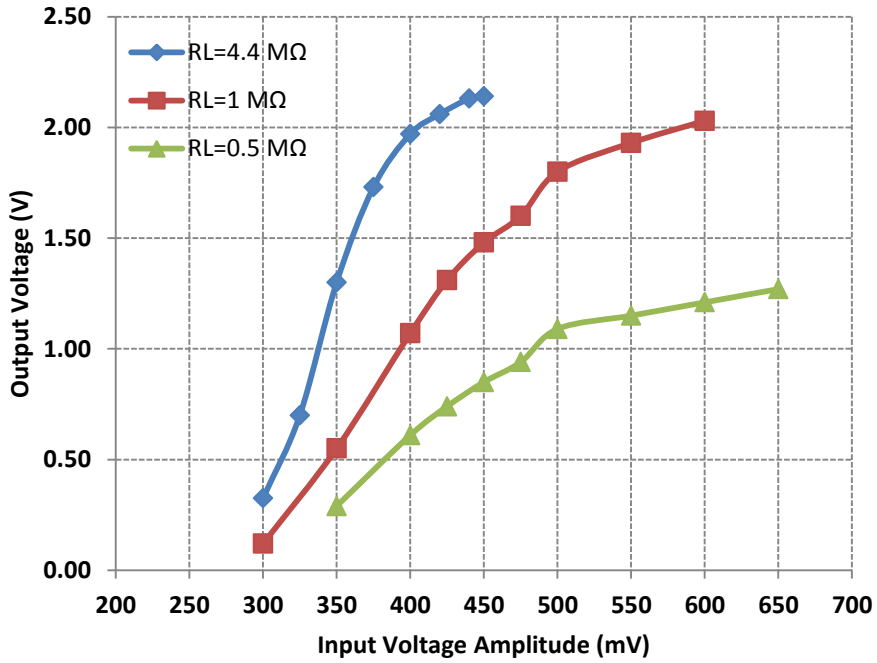
Figure 4.15: a) Output DC Voltage and (b) Efficiency of the unregulated circuit versus the load current for 10 Hz input frequency and 2 mm, 2.5 mm, and 3 mm peak-to-peak vibration amplitudes.

The desired output condition is, to get 1 V output voltage for 1 µA load current which is satisfied by the unregulated system. The circuit is able to generate more than 1 V output voltage for load currents lower than 1.7 µA, 2.6 µA, and 2.9 µA with peak-to-peak

vibration amplitudes 2 mm, 2.5 mm and 3 mm, respectively. The maximum power conversion efficiency of the circuit for 2 mm, 2.5 mm and 3 mm peak-to-peak vibration amplitudes is about 10%, 13 % and 12%, respectively. Although, the efficiency of the system is lower than 15% it is meaningful to get such a low efficiency at fully-integrated and low voltage power converter systems. It is possible to get much higher efficiency by using off-chip components like inductor or transformer; however it is nearly impossible to integrate these components on-chip. The presented results show that with a proper regulation circuit it is possible to get 1 V regulated output with at least 1 µA load current.

The performance of the circuit is also tested for different input peak voltages by using the signal generator. The minimum operation voltage of the circuit and efficiency of the circuit at different input voltages is observed with the help of these tests. Figure 4.16 shows test results of the circuit for different load resistance values (0.5 MΩ, 1 MΩ, and 4.4 MΩ). The input voltage frequency of the circuit is 10 Hz and the storage capacitors of the rectifier circuit and the output are chosen as 10 µF and 1 µF, respectively.

Figure 4.16 presents change of the output DC voltage and power conversion efficiency of the unregulated circuit for varying input peak voltages and different load resistances. The output voltage of the circuit reaches 1 V DC voltage at 0.34 V, 0.4 V, and 0.49 V input peak voltages for the load resistances 0.5 MΩ, 1 MΩ, and 4.4 MΩ, respectively. For input peak voltages larger than 0.4 V the circuit achieves more than 1 µW output powers which satisfies the desired condition and leads to drive a real load like a temperature sensor. The maximum power conversion efficiency of the circuit for 0.5 MΩ, 1 MΩ, and 4.4 MΩ load resistances is measured as 8.5%, 11 % and 7%, respectively. For input peak voltages larger than 0.4 V the efficiency of the system is higher than 5%. Although the power conversion efficiency of the circuit is low, it finely converts the low input AC voltages to more than 1 V DC voltages.



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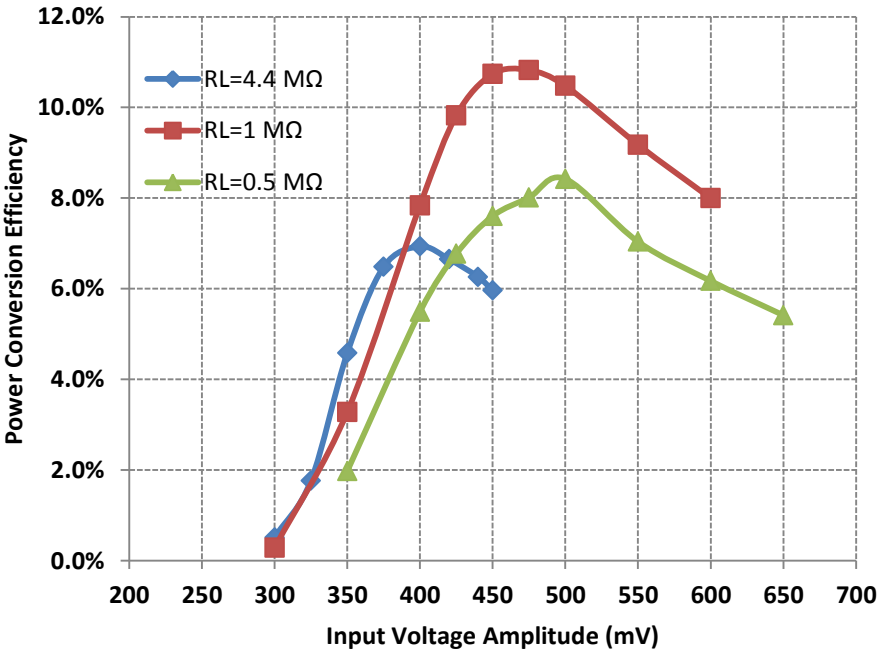

(b)

Figure 4.16: a) Output DC Voltage and (b) Efficiency of the unregulated circuit versus the input peak voltage for 10 Hz input frequency and 0.5 MΩ, 1 MΩ, and 4.4 MΩ load resistance conditions.

4.4. Test Results of Designed Voltage Regulator

Last part of the designed circuit that finalizes the design is the voltage regulator which was explained in Section 3.4. In order to test the voltage regulator block more precisely and controllable a power supply is used to give the supply voltage. When the overall regulator block is tested the obtained results don't fit with the expected results. As depicted earlier when the supply voltage of the regulator (output voltage of the system) exceeds 1 V output of the regulator must be triggered to high voltage (supply voltage); however at the obtained result the output voltage always stay at zero voltage. At this stage to understand the problem at the circuit sub-block of the circuit is started to be tested.

Firstly, the voltage divider sub-block is tested to observe its operation. Figure 4.17 presents the observed test result for the voltage divider circuit with the varying supply voltage condition. The results are similar with the simulations, after a certain voltage the output voltage linearly changes with the supply voltage; however little deviations are observed from the expected results. The circuit start to operate properly after about 0.6 V, the reason for this is, the circuit contains two diode connected transistors which needs at least two threshold voltages as the supply voltage to turn ON. The output of the circuit is slightly lower than expected results due to the parasitic components coming from the fabrication. The parasitic capacitances such as the PAD capacitances decrease the driving capability of the circuit and this leads to voltage drop at the output. Although the voltage divider block does not work perfectly, it is still usable and can be used at voltage regulator as the input of comparator. To improve the performance of the voltage divider size of the utilized transistors can be increased; however this also leads to increase the power dissipation of the circuit.

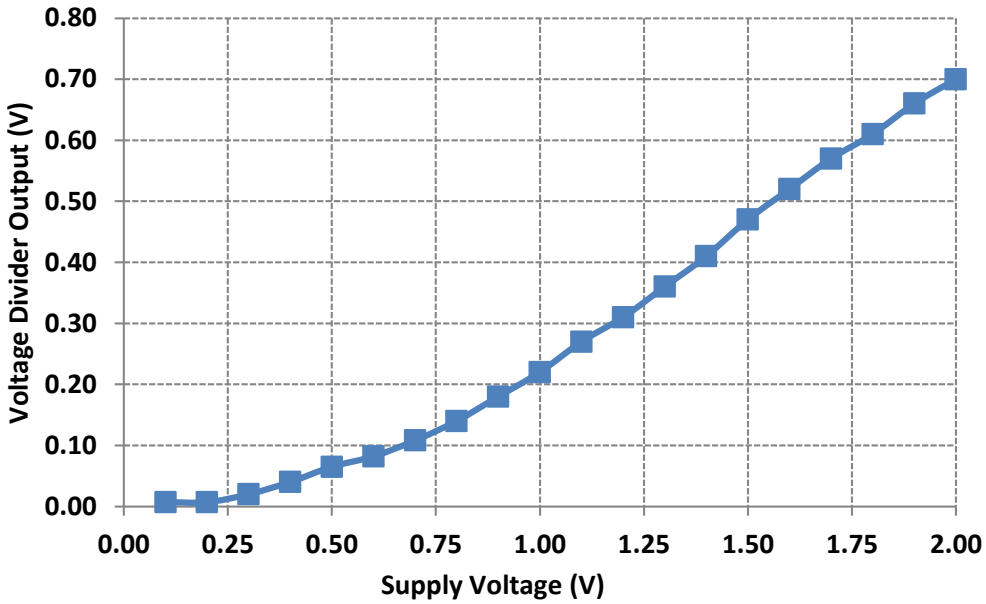

Figure 4.17: Change of the voltage divider output with respect to supply voltage.

The next tested sub-block of the voltage regulator is the designed sub-threshold voltage reference circuit. Figure 4.18 presents the result obtained from tests of the sub-threshold voltage reference circuit. The results are completely different with the expected results. According to the simulation results the reference voltage output must be stabilized at about 478 mV after 0.6 V supply voltage, however at the obtained result the reference voltage continues to increase with the increasing supply voltage and after 1.6 V it falls to 400 mV. This result completely explains why the regulator circuit does not work properly and always stay at low voltages until 1.6 V supply voltages.

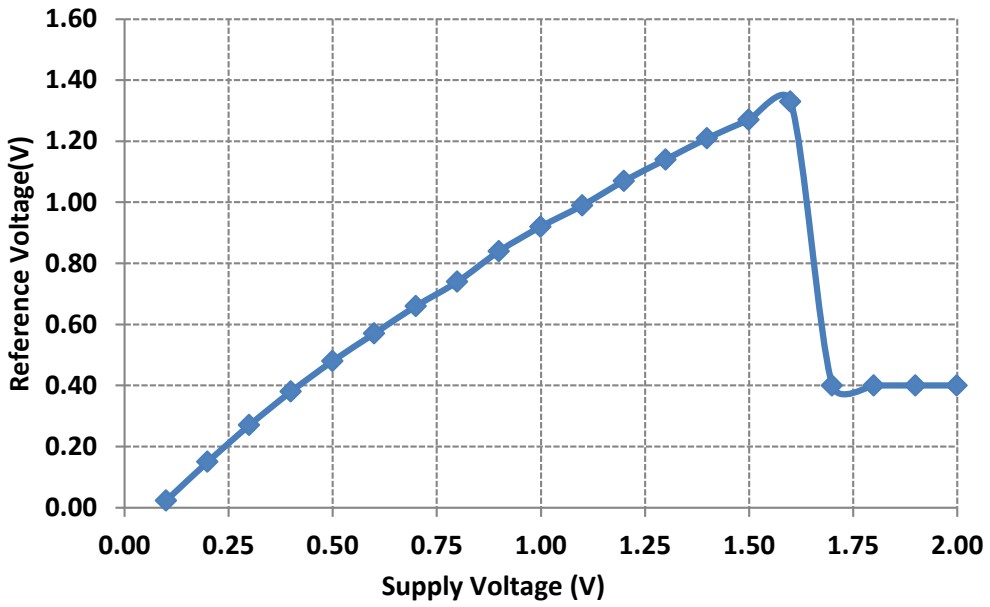

Figure 4.18: Change of the reference voltage output with respect to supply voltage.

To identify the problem at the voltage reference first of all post-layout simulations of the circuit is handled, but the post-layout simulation of the circuit gives completely same results with the schematic simulations. After that the process corner simulations of the circuits which tests the circuit at different process corners is taken into consideration. There are five different process corners: “Slow-Slow”, “Slow-Fast”, “Fast-Slow”, “Fast-Fast”, and “Typical-Typical”. The slow ad fast terms at the name of the corners depict the reaction of the transistors at that process conditions. At process corner simulations process dependent parameters (such as threshold voltage, channel length, etc.) are moved to their possible limits occurred due to process variation. Possible reasons for these different process conditions are variation at doping concentration at a doped area, temperature, and utilized metal thicknesses. The terms in the name of these corners show the performance of the NMOS and PMOS transistors at these conditions, respectively. As an example at “Slow-Fast” corner the NMOS transistors shows slower performance compared to typical case; however the PMOS transistors works with high speed or stronger performance. The “Typical-Typical” corner represents the typical conditions for operation.

The result obtained from the "Slow-Slow" corner simulation of the circuit is highly matched with the test results. Figure 4.19 presents the "Slow-Slow" and "Typical-Typical" process corner simulation result of the voltage reference circuit for varying supply voltage. At typical simulation the reference voltage is stabilized after 0.6 V; however at "Slow-Slow" process corner simulation similar with the test results the reference voltage increase with supply and falls to desired reference voltage at 1.8 V.

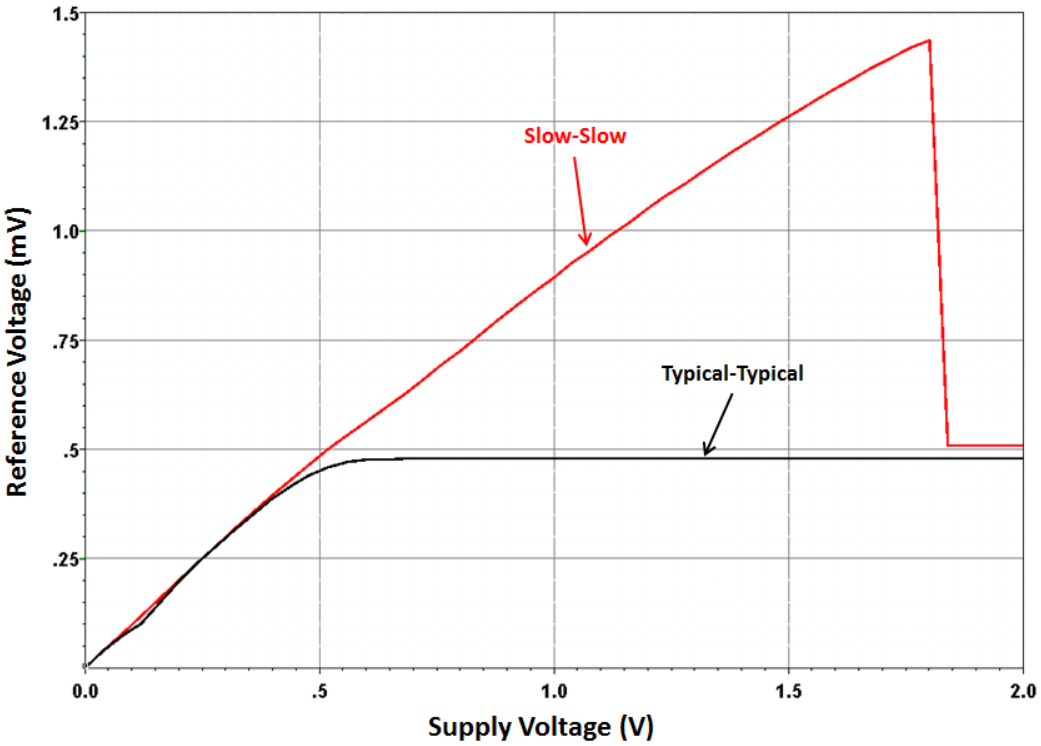

Figure 4.19: "Slow-Slow" and "Typical-Typical" process corner simulation result of the voltage reference circuit for varying supply voltage.

The results show that the performance of the transistor is below the typical case and they are weaker than normal condition. To solve the problem at the voltage reference transistors at the circuit must be strengthen. Therefore, size of the transistors at the current reference circuit is increased and optimized to get the same reference voltage from the output. Table 4.3 shows the previous and new size of the transistor for that is changed to solve the problem. Sizes of the bolded transistors are increased and the process corner problem is eliminated. Figure 4.20 shows performance of the circuit for all of the process corners. The optimized circuit is stabilized at 482 mV reference voltage and the output is changed ±12 mV when the supply voltage swept from 0.6 V to 2 V. As a result, the problem at the voltage reference circuit is identified and with the given modification the problem is solved.

The problem at the voltage reference circuit also explains the problem at the voltage regulator block. The generated reference voltage is connected to the negative input of the comparator and since it always gives high voltages, the comparator always gives low voltages.

Table 4.3: Corrected size of the transistors at sub-threshold voltage reference circuit.

Transistor	W/L Previous	W/L New
M_{P1} - M_{P5}	10 µm / 10 µm	10 µm / 10 µm
M_{N1}, M_{N3}	**3 µm / 0.1 µm**	**15 µm / 0.13 µm**
M_{N2}, M_{N4}	**60 µm / 0.1 µm**	**120 µm / 0.13 µm**
M_{N5}, M_{N7}, M_{N9}	6 µm / 3 µm	6 µm / 3 µm
M_{N6}, M_{N8}	40 µm / 0.5 µm	40 µm / 0.5 µm
M_R	**0.5 µm / 20 µm**	**0.5 µm / 15 µm**
M_{Nb}	0.5 µm / 3 µm	0.5 µm / 3 µm
M_1 - M_2	2 µm / 2 µm	2 µm / 2 µm
M_3 - M_4	0.2 µm / 10 µm	0.2 µm / 10 µm

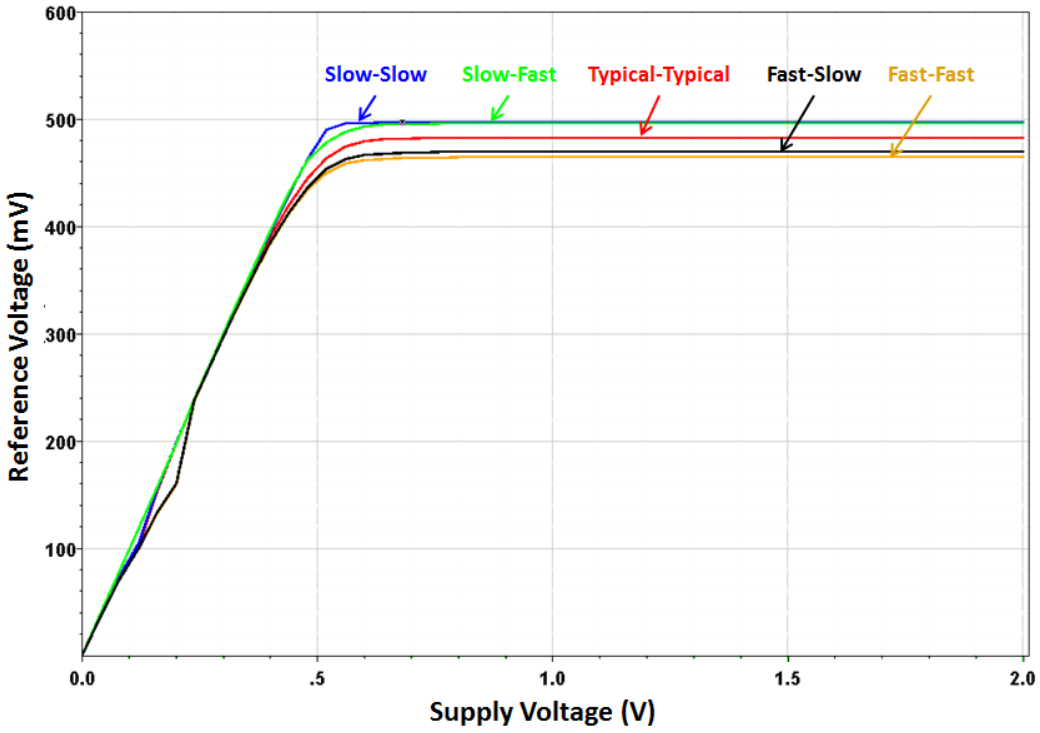

Figure 4.20: Process corner simulation result of the voltage reference circuit for all of the corners with varying supply voltage.

CHAPTER 5

CONCLUSION AND FUTURE WORK

In this thesis, a fully-integrated and self-powered interface electronics for low voltage electromagnetic energy harvesters has been designed and implemented. The aim of the designed interface electronics is to efficiently rectify the low voltage and low power signals generated by the electromagnetic energy harvester and convert it into a stable DC output voltage to be used at real applications. The implemented interface circuit is finally merged with a low vibration electromagnetic energy harvester prototype and the full-system performance of the circuit is verified.

Accomplished tasks and results of this research can be listed as follows:

1. An inclusive study on efficient design of building blocks of interface electronics for vibration-based electromagnetic energy harvesters has been made. State-of-the-art examples of all of these blocks that take place in the literature have also been reviewed. Moreover, improvements and drawbacks of these works are also specified.

2. A new interface electronics architecture for low voltage and low power electromagnetic energy harvesters is designed to efficiently convert the low AC voltages into a usable DC voltages. The major advantage of the designed circuit is, it is fully-integrated and does not require any external power source like a battery. A novel ultra-low voltage rectifier circuit is proposed as the first block of the designed system and compared with previously reported works to presents its improvement. The next block is a fully-integrated DC-DC converter which is utilized to step up the rectified low DC voltage. The final block of the system is a low voltage regulator circuit which stabilizes the output to 1 V DC voltage. The proposed interface circuit is designed and implemented in TSMC 90 nm CMOS technology which has special transistors to be used at low voltages.

3. An electromagnetic energy harvester prototype which works at low vibration levels has been developed and merged with the implemented circuit in TSMC 90 nm CMOS process to realize a complete energy harvesting system. The performance of the designed circuit is verified with the test results and the reasons for functionless blocks are validated. Possible solutions of these problems are also given. The designed self-powered

rectifier circuit is able to operate down to 100 mV input peak voltages and the unregulated energy harvesting system is able to convert input peak voltages higher than 350 mV to more than 1 V DC voltage at an external vibration of 10 Hz. These values are the minimum reported voltage levels in the literature among the battery-free and fully-integrated circuits.

4. Part of the obtained results from this work has been presented in conferences such as *ICEAC'12* and *TRANSDUCERS'13*. Also a journal paper is prepared to be submitted in *Sensors and Actuators: A. Phys. Journal*.

Since this work is one of the first researches on full system solution of interface electronics for electromagnetic energy harvesters, the potential to the future research is highly impressive.

A comprehensive list of future works is listed below:

1. Voltage generated by the MEMS based electromagnetic energy harvesters fabricated in METU-MEMS center has too low output voltages which are not enough to turn on a transistor. Hence, macro model of the electromagnetic energy harvesters are utilized to test the performance of the circuit. Currently, researches on micro electromagnetic energy harvesters are continuing and with a slight improvement of fabricated devices they can be combined with the designed circuit to realize a complete micro power generation systems.

2. The problems encountered at the implemented chip are solved and the rearranged circuit is ready for a new fabrication. Some further improvements can be added to the circuit to enhance the efficiency of the system. Furthermore, a power management circuit which monitors the output voltage and put the circuit into standby mode when needed can be also added to the new design.

3. Design of a similar interface circuit with CMOS 180 nm technology which is cheaper than the one used in this technology was started. The new circuit is planned to be used with slightly higher voltages and regulates the output voltage to 3 V DC voltage.

4. An on-chip sensor which is compatible with CMOS can be added on the same chip with the proposed circuit to have a completely integrated sensor system. A probable example for this sensor is a temperature sensor.

5. A hybrid energy harvesting system can be generated by utilizing the designed system and with another energy harvesting topology such as an RF energy harvester to improve the power output of the system.

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