DATA ACQUISITION SYSTEM

by

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Submitted to

The Faculty of the School of Engineering

in Partial Fulfilment of the Requirements for

the Degree of Master of Science

in Electrical Engineering.

BOĞAZİÇİ UNIVERSITY

September 1981

APPROVAL SHEET

This thesis, submitted by Sabri Metin İskit to the Electrical Engineering Department of Boğaziçi University in partial fulfilment of the requirements for the degree of Master of Science, is approved.

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ACKNOWLEDGEMENTS

The following is not the work of a single person,but it has been realized with the helps of many individuals.

At the first stage,I would like to express my sincere gratitude for the thesis supervisors.Prof.Dr.Sabih Tansal and Doç.Dr.Bülent Sankur.

I would also like to thank Dr.Ömer Cerid for his valuable suggessions on the design.

Also,I am very thankful to ÇNAEM Electronic Department for their help in practical realisation of the instrument.

ABSTRACT

In this study several analog to digital converter systems are described and their advantages and disadvantages are told. Among them,a successive approximation type one is designed and built.To obtain flexibility,it is designed as a bus compatible device.Also device addressing is used,by use of which , more similar devices will be able to be connected to the bus.The bus is so designed that it is not possible for more than one pair of devices to be active on it at any time.The system also has analog multiplexing facility which selects one of eight analog inputs.This selection can either be done by the peripheral device or by the system itself,according to the information on the bus.Output of the system is 12 bits,in addition to the parallel output,serial output with preselectable baud rate is put for long distance communication. The results obtained are quite satisfactory in performance.

TABLE OF CONTENTS

LIST OF FIGURES

Complete Circuit Diagrams

PREFACE

In the last years,after the power of digital systems are distinguished,the digital measuring instruments became to play a very important role in industry.Beginning with the simplest digital voltmeters,more precise analog to digital converters were made and finally they became unavoidable interfaces of digital computers and microprocessors.During this evolution,many approaches were made to obtain the cheapest and the most powerful conversion systems.Some of the basic types are discussed in this thesis.

The choise among these types of ADC's in this thesis is the successive approximation type which is the second fastest type of the converters.Principally it performs the conversion in KxN clock pulses where N is the number of bits and K is the number of clock pulses required to decide the state of the corresponding bit.It is easier to chose K as 2 or more to simlify the design,but to obtain maximum conversion speed, it is tried to keep K as 1 and successful results are obtained.

To increase the flexibility of tne ADC,it is designed as a bus compatible device with multiplexed 8 analog inputs.The

ADC will be a service unit on the bus,and of course at least one consumer unit must also be present.The channel number of analog inputs can either be identified by this consumer device or can be let free such that it increases by one each time a service request comes.To be able to connect more than one service unit on the bus,a two bits service unit address line is added,so,three service units can be connected to the bus. Also for long distance communication,a variable baud rate serial output is added.The detailed description of the operation of the bus and the system will be given in the text.

Neither part of this design is directly copied from any reference.The references are used to get information about the operations of the individual subsystems used in the circuit,so it is possible that the diagrams cannot be found in the references given.

PRINCIPLES OF ADC SYSTEMS

In this section,several types of analog to digital converters will be discussed.These are single slope,dual slope,successive approximation,flash,voltage to frequency,Wilkinson and dual ramp ADC's.

The single slope ADC is the simplest of the present systems. It has one comparator which compares a ramp with the input voltage and measures tha time for the ramp to reach this voltage.This time,when multiplied by a constant,gives the value of the input voltage.

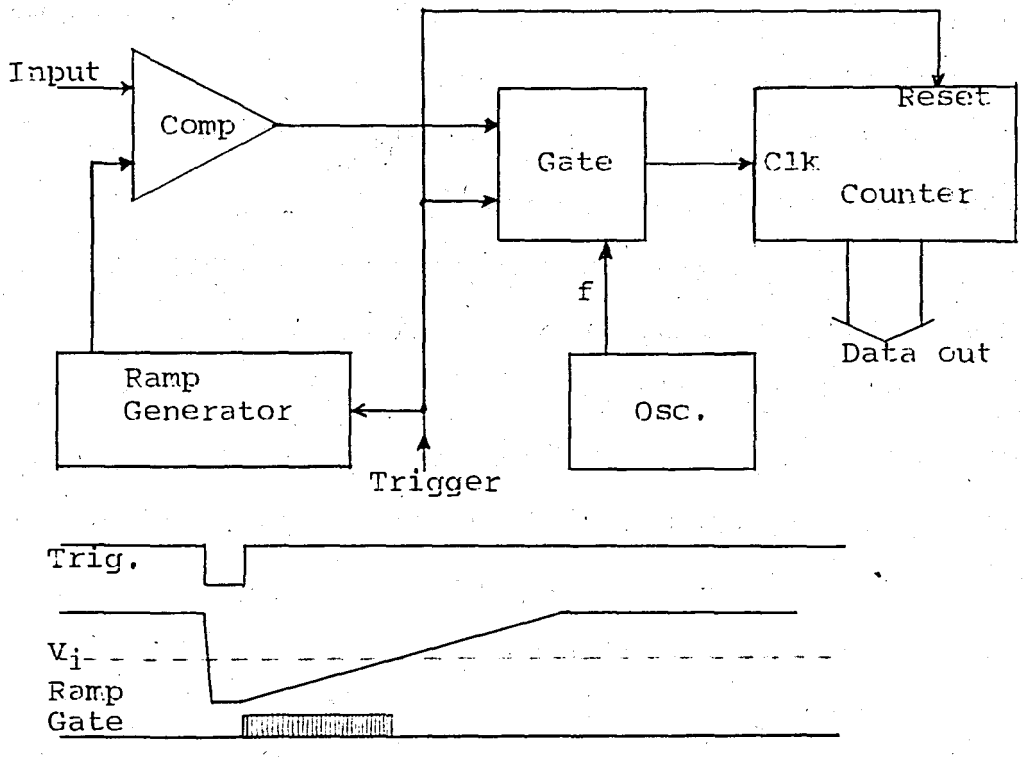


Figure 1:Block diagram and the waveforms of a single slope ADC

At steady state,ramp generator output is at its highest value and the gate is closed (i.e. no signal is present at the output of the gate).When trigger signal goes low,the counter is reset and the gate is kept closed,also the ramp generator output is set to zero volt.At the time the trigger signal goes high the gate is opened and the counter begins to count the incoming pulses.During this time the ramp output increasas, and when it reaches the analog input voltage,the comparator changes its state and closes the gate.The number of counts gives the voltage for appropriate choise of the oscillator frequency.To read the next sample,trigger signal must go low and then high again.

As can easily be seen,the slope of the ramp generator,the frequency of the oscillator and the number of bits are closely related to each other.The number of bits,N,will be chosen according to the design specifications.To give a realistic example,for a 12 bit converter,a convenient full scale voltage will be 4.096 volts,each step corresponding to one millivolt. Let the maximum number of conversions per second be N.Then, it means that 4096 pulses are required to be counted in 1/N seconds.So the necessary oscillator frequency must be 4096xN cycles per second.Also in 1/N seconds,ramp must reach to its maximum value of 4.096 volts,so tha slope of the ramp generator must be 4.096xN volts/second.By use of these data,an appropriate

oscillator and an integrator (as the ramp generator) can be designed.Since the limitation mostly comes from the comparator, for which we have to take the propogation delay to be less than the period of the oscillation,by choosing a quite high value for the oscillator frequency such as 2 MHz,we find

$$N=2000000/4096\cong 500 \text{ conversions/second,}$$

which is quite unsatisfactory for most systems.This is why these types of systems are used as digital voltmeters where only a few conversions/second are necessary instead of fast computer interfaces.

One important problem olso arises in hardware design,which is setting the ramp generator voltage to zero volt before beginning of counting.This is because of the offset voltages and/or the saturation voltages and on state resistances of the components used.Besides this uncertainties,a small deviation in oscillator frequency or in the slope of the ramp results in an error.To overcome these two errors,a feedback type single slope ADC can be designed by use of a digital to analog converter (DAC) as shown in figure 2.

In this type of ADC,trigger pulse only resets the counter.The all zero output of the counter causes the output of the DAC to be at zero volt,and comparator opens the gate.Each pulse the counter counts increases the output voltage of the DAC by

one least significant bit (LSB) voltage,e.g. if full scale voltage is 4.096 volts for a 12 bit ADC,each pulse increases the voltage by one millivolt.So a staircase type ramp is obtained directly dependent on the total number of counts.This eliminates the uncertainty coming from zero volt start of the ramp generator and independent deviations of the clock frequency and the ramp voltage slopes.But the setup time of the DAC,which is usually much greater than the propogation delay of the comparator and the propogation delay of the counter are added to the propogation delay of the comparator,which reduces the speed considerably.Also since the DAC is the most expensive component of this system,financial problems may arise.

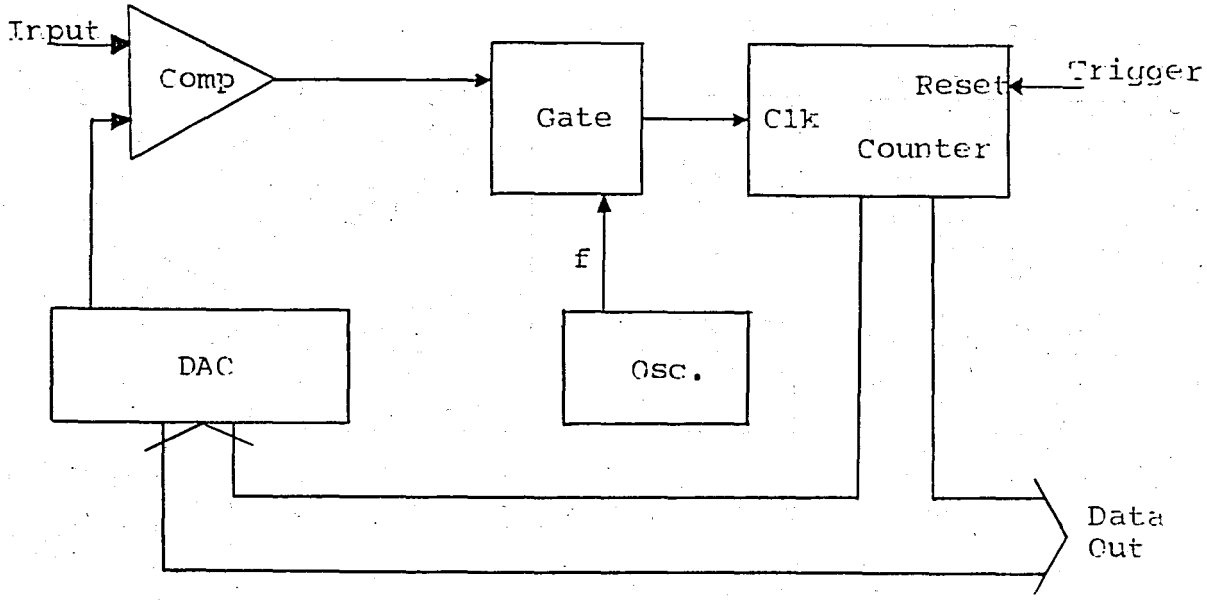


Figure 2:Single slope ADC with DAC feedback

Dual slope ADC is the type which overcomes the problem of zero volt start of the ramp generator ~~without~~ by using ~~a DAC but instead~~ a second comparator.When it is desired to take a sample, the memory element ME1 is set by a trigger pulse.This causes the output of the ramp generator to increase (by any slope which is not important).When it reaches the input voltage, comparator 1 sets ME2 which opens the gate and resets ME1 which turns ramp generator output to a known negative slope waveform.The counter counts until the ramp voltage falls to zero volt,at that time comparator 2 resets ME2 and closes the gate.After the gate is closed,ramp output will continue to fall down to the saturation voltage specified by the designer,which is a negative voltage,and waits until next trigger pulse.

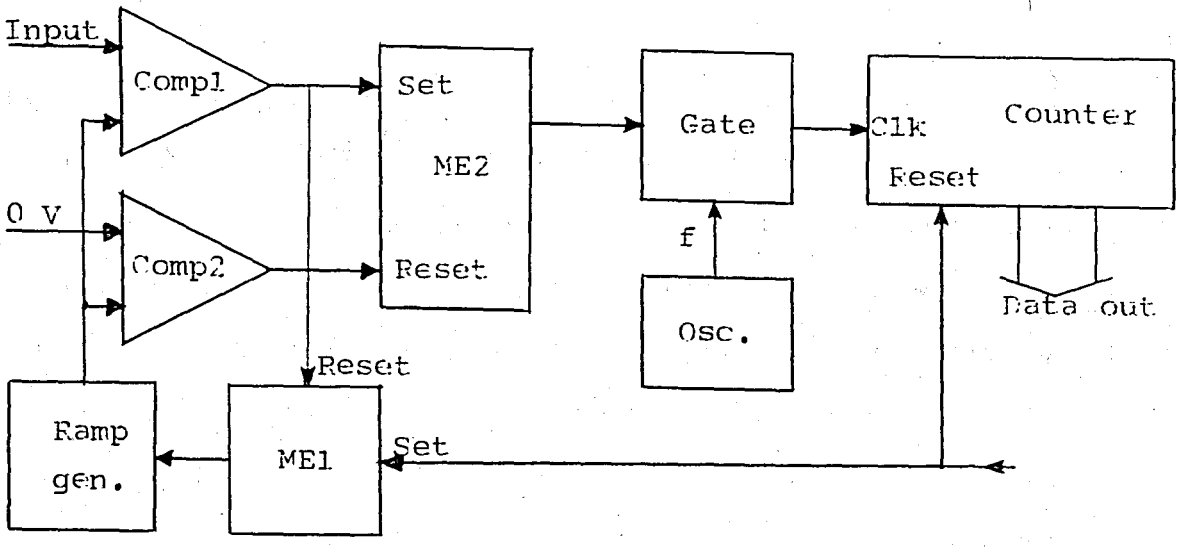


Figure 3:a) Block diagram of a dual slope ADC

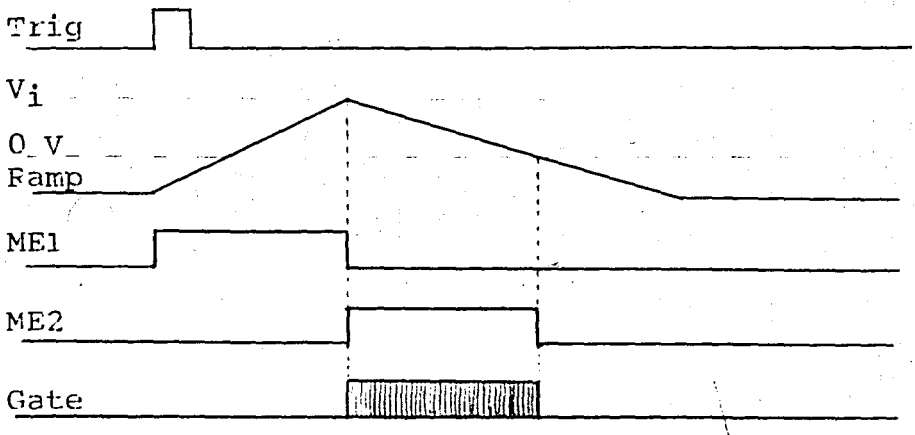


Figure 3:b)Waveforms of a dual slope ADC

Since two sweeps are used for one conversion,it is obvious that maximum conversions per second will decrease to about half the value of the single slope systems.In fact for double slope systems,propogation delay of the memory elements are added,so the speed becomes less than what is expected.

But for this system again the clock frequency and the slope of the ramp generator can vary independently,so enough precision cannot be obtained.It is possible to control one of the slopes by use of the input voltage as shown in figure 4. For this circuit,the trigger pulse resets the counter and sets the ME which switches the single pole double throw (SPDT) analog switch to the analog input voltage.The integrator output begins to increase,and when it passes through zero volt,it opens the gate by use of the comparator.From now on, the counter counts until it reaches its maximum value,sends

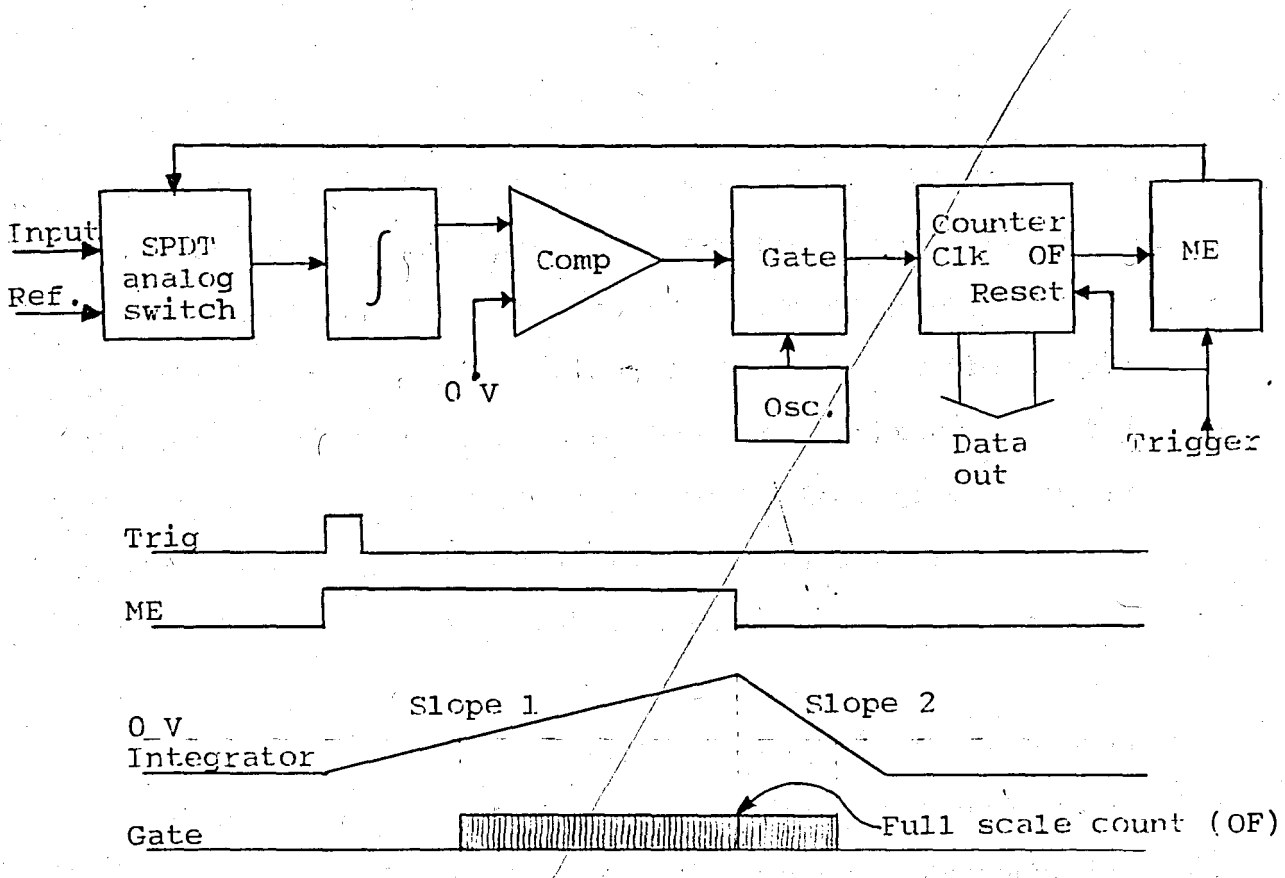


Figure 4:Block diagram of a precise dual slope ADC

an overflow (OF) to reset ME and begins to count beginning from zero again.The ME switches the SPDT switch to the reference voltage.At this time,the output voltage of the integrator is proportional to the slope of the ramp (slope 1) which is also proportional to the input voltage.The reference voltage causes the cutput voltage of the integrator to fall dow by slope 2.Since slope 2 is a known value,or actually slope 1 / slope 2 for a specific input voltage is known,the number of counts during slope 2 until it reaches zero volt gives the voltage with a high precision.

The errors from variations of the clock frequency and the time constant of the integrator are mostly eliminated by this type of configuration,this is why quite high precisions are obtained.This elimination of the error is the result of the ramp period controlled by the clock instead of letting the ramp to be free.Dual slope analog to digital converters mostly find applications in digital voltmeters,where speed is not important but precision is.

Voltage to frequency type ADC's work by use of a voltage to frequency converter (VCO), by measuring the frequency of the VFC.By appropriate choise of voltage versus frequency curve, direct readout of the applied voltage can be obtained.For example,by counting the pulses for 10 msec.and using a VFC which generates 10 kHz/volt,2 volts cause 200 pulses to be counted,which is 100 times the input voltage.i.e. two decimal point movements is required.

The major disadvantage of this type of ADC's are the speed (because of the quite large counting period requirement),the influence of the signals coming from the mains supply and the unavoidable effects of the transients at the input.In addition to these error sources,the complexity of a wide range linear VFC makes this type of ADC's useless for many systems.

Successive approximation type ADC's are the most common types for fast conversion requirements because of its low price / speed ratio.It consists of a bit selector,a bit memory array, a DAC and a comparator tc decide the state of the bit.

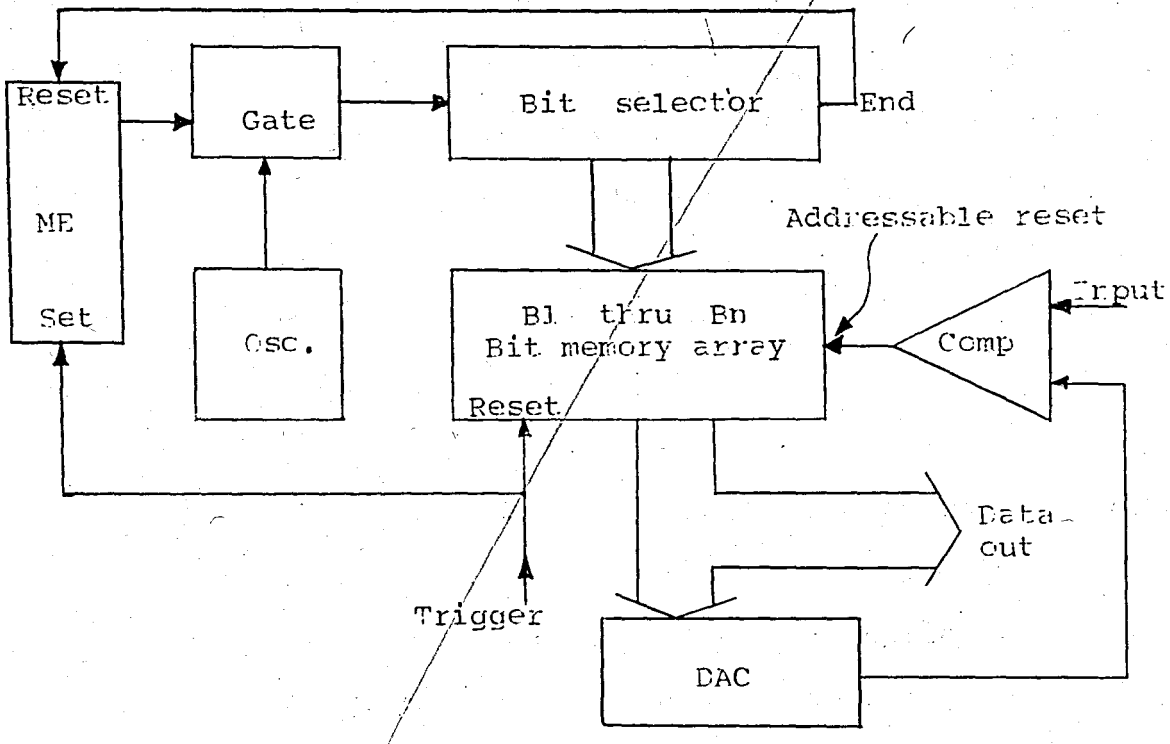


Figure 5:Block diagram of successive approximation ADC

When a trigger pulse is applied,ME is set to open the gate and all the bits in bit memory array are cleared.The clock pulses passing through the gate causes bit selector to sweep the bits beginning from the most significant bit (MSB).Corresponding value of MSB is half of the full scale voltage,which is con-

verted to analog by DAC.The comparator decides about the state of this bit,if it is larger than the input voltage it resets the bit,ifnot,lets it set.Then second MSB is tried which corresponds to one quarter of the full scale voltage.This voltage is added to the previously decided MSB value by the DAC,i.e. if MSB is "1",output of the DAC will be 3/4,if MSB is "0",output will be 1/4 of the full scale voltage.The comparator again decides on resetting or letting at "1".Continuing this way,after n comparisons,result becomes ready.After the LSB is set,bit selector sends an END message to reset ME and the system stops operation.For the next sample a new trigger pulse must be applied.

The operation of the bit selector and the addressed reset may be not as simple as it appears because of the practical problems arising while using the DAC.A step applied to the DAC results in some overshoot,which may give wrong information to the comparator and reset the wrong bit.To overcome this error source,addressed reset is gated by the clock to wait half a clock period before deciding to reset the bit or not. During this time,DAC output must settle to the desired value. It is possible to wait more than half a clock period.This of course reduces the speed of the system.A typical DAC and comparator output waveforms of a 6 bit and half clock period waiting ADC is shown in figure 6.

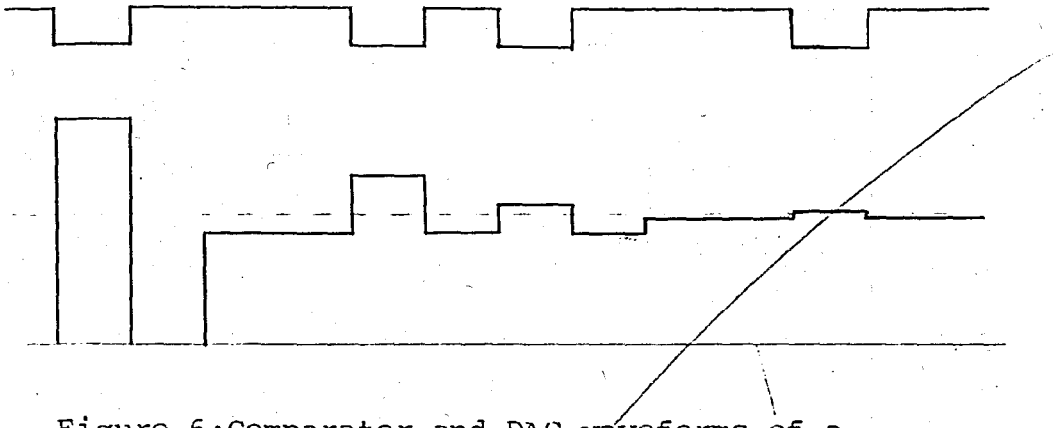


Figure 6:Comparator and DAC waveforms of a 6 bit successive approximation ADC

Comparing the successive approximation ADC's with the single slope or dual slope ADC's,a great advantage of speed can easily be seen.A single slope ADC performs its operation in 2^n clock pulses while the successive approximation ADC needs only n clock pulses to complete the same job.The power of this system can be shown by a typical numerical example,for a 12 bit ADC, successive approximation is $2^{12}/12 \cong 300$ times faster than a single slope one.But of course it costs more since too many logic circuits must be used compared with the other systems.

Flash ADC is the fastest type,for which no clock is required for conversion.It consists of 2^n voltage comparators and reference voltages and a combinational logic to decode the output of comparators to binary.Figure 7 shows the block diagram of a basic flash ADC.

The voltage on each resistor is $V_r/2^n$,which corresponds to one

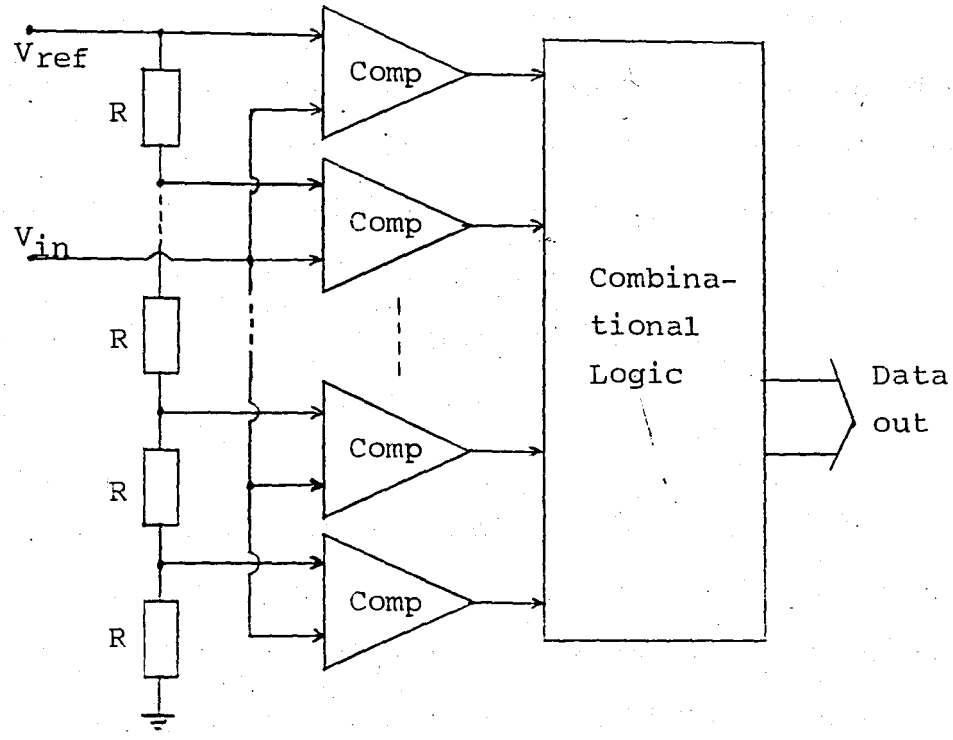


Figure 7:Block diagram of a flash ADC

LSB voltage.So,to each comparator,a different reference voltage is applied,each upper comparator having the reference voltage of the previous one plus one LSB voltage.For an analog input voltage of less than $kV_r/2^n$ and greater than $(k-1)V_r/2^n$,the outputs of the comparators from 1 to k-1 will be "1" and the remaining "0".By decoding it,binary output is obtained.The speed of the conversion is restricted by the speed of the comparators only.The propogation delay of the decoder will result with time domain shift.i.e. the value read at time t is actually the value of the voltage at time $t-t_{pc}-t_{pd}$,where t_{pc} is the propogation delay of the

comparator and t_{pd} is the propogation delay of the decoder. To give an idea about the speed of this system, if a 40 nsec. comparator is used with 100 nsec. delay time decoder, conversions per second will be 25 million while the propogation delay was 140 nsec. According to Nyquist theorem, up to 12.5 MHz frequencies can be sampled.

But this very high speed conversion capability of this type of ADC's have a great restriction in practice, which is exponantially increasing number of comparators required to increase the number of bits. For a 4 bit ADC, only 16 comparators were enough, but if 8 bit one is desired, 256 comparators are required, which effects the cost considerably. This property limits the use of the flash ADC's to very special applications.

To decrease the required number of comparators, two different flash ADC circuits are developed. One is called parallel ripple ADC, which consists of two m bit flash ADC's, one m bit DAC with 2m bit resolution and an analog subtractor resulting with 2m bit flash ADC. ADC1 selects the 'page' of the voltage. This value is again converted to analog and subtracted from the input voltage. Resulting voltage gives the least significant part of the input and is converted to digital by ADC2. This technique reduces the number of comparators considerably, but because of the analog devices used in the circuit, speed will

be lower.

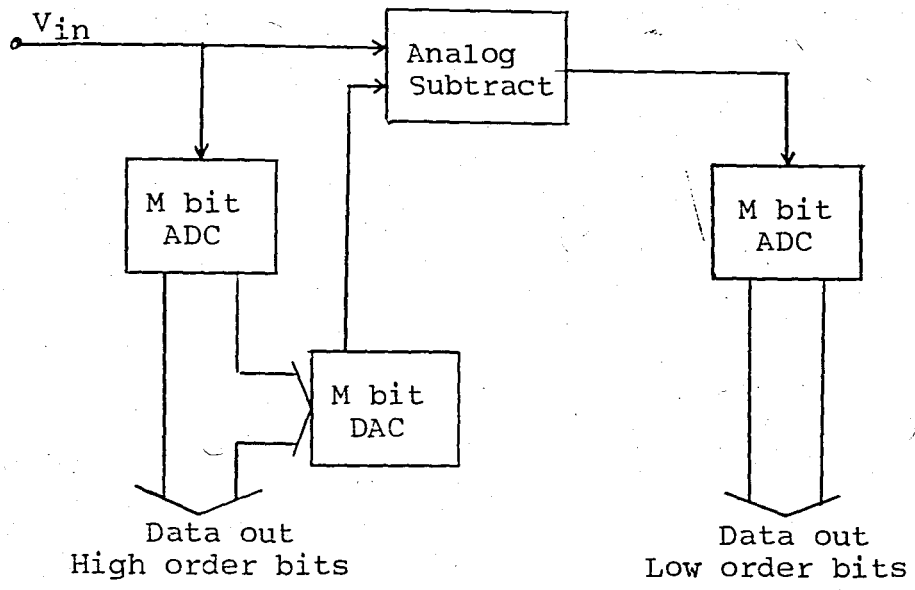


Figure 8:Parallel ripple ADC

Another type of flash ADC is called Variable Treshold Flash, for which only n comparators for an n bit ADC is used.It requires also n DAC's of from 1 bit to n bits.To obtain accuracy,these DAC's must have n bits resolution.As seen in figure 9.each comparator has its treshold voltage as a feedback from the upper comparators.Whenever an upper comparator turns to "1",all the treshold voltages of lower comparators increase and they turn to "0".When input voltage increases a little more,comparators begin to turn to "1" beginning from the LSB.Since the settling of the comparators and the DAC's take time and it appears to be settling sequencially,

the conversion time increases considerably.

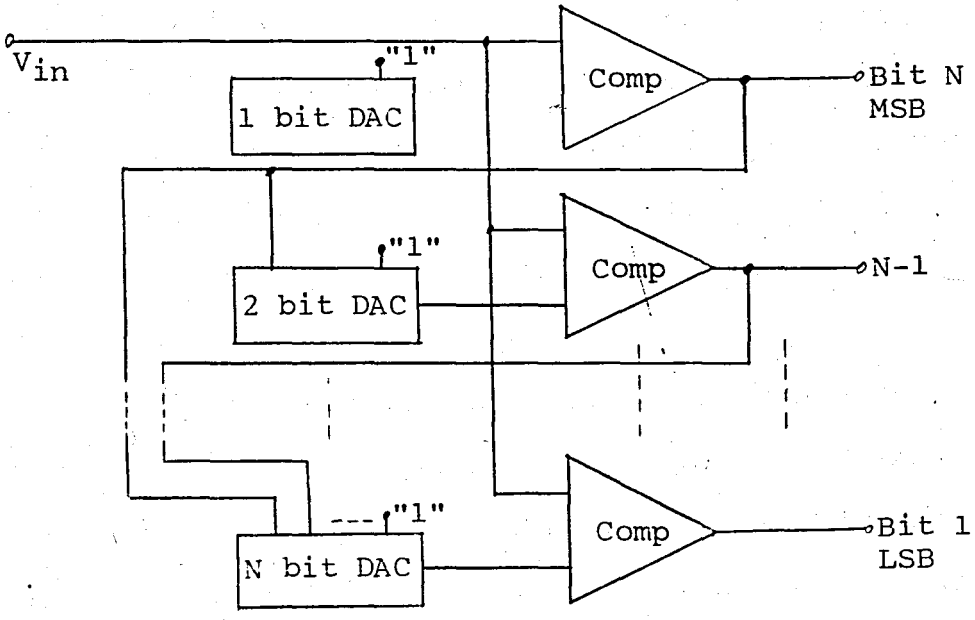


Figure 9:Variable treshold flash ADC

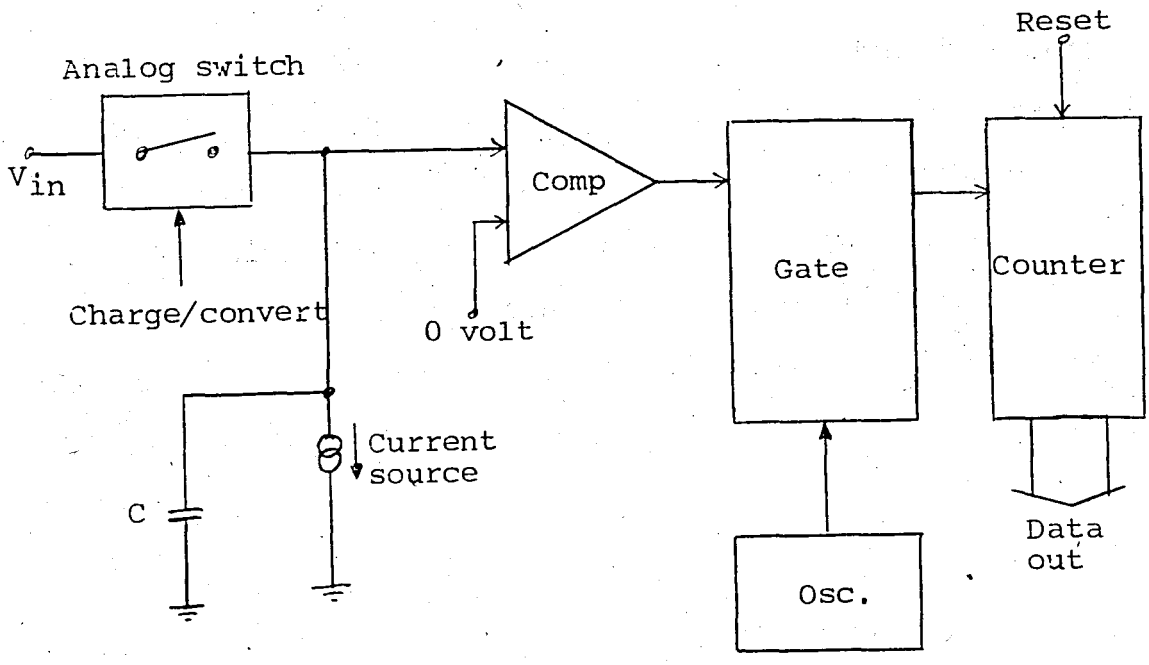


Figure 10:Wilkinson ADC

Wilkinson ADC (figure 10) is a very similar one to the single slope ADC.The only difference is that instead of the input voltage is being kept constant and a ramp beginning from zero volt is applied,a capacitor is charged to the input voltage and discharged with a constant current while counting the time for the capacitor voltage to cross zero volt.

This system has a special use in pulse techniques since its accuracy is not good but it has very high resolution and very low differential non-linearity.The basic use of Wilkinson ADC's are in the multichannel analizers,where,before a measurement,always a calibration procedure has to be performed, (so accuracy is not important).

A developed version of the Wilkinson ADC is the dual ramp ADC. (figure 11).It has seceral times higher conversion speed with the same clock frequency.The principle is to discharge the capacitor with,for example,64 times the required current for Wilkinson type,while counting 64 each time instead of 1,with the first clock pulse after zero crossing,to apply a reverse normal current and count down by one until next zero crossing occurs.

After convert signal comes,the decision unit switches S to I_1 by which the capacitor discharges rapidly,and connects the

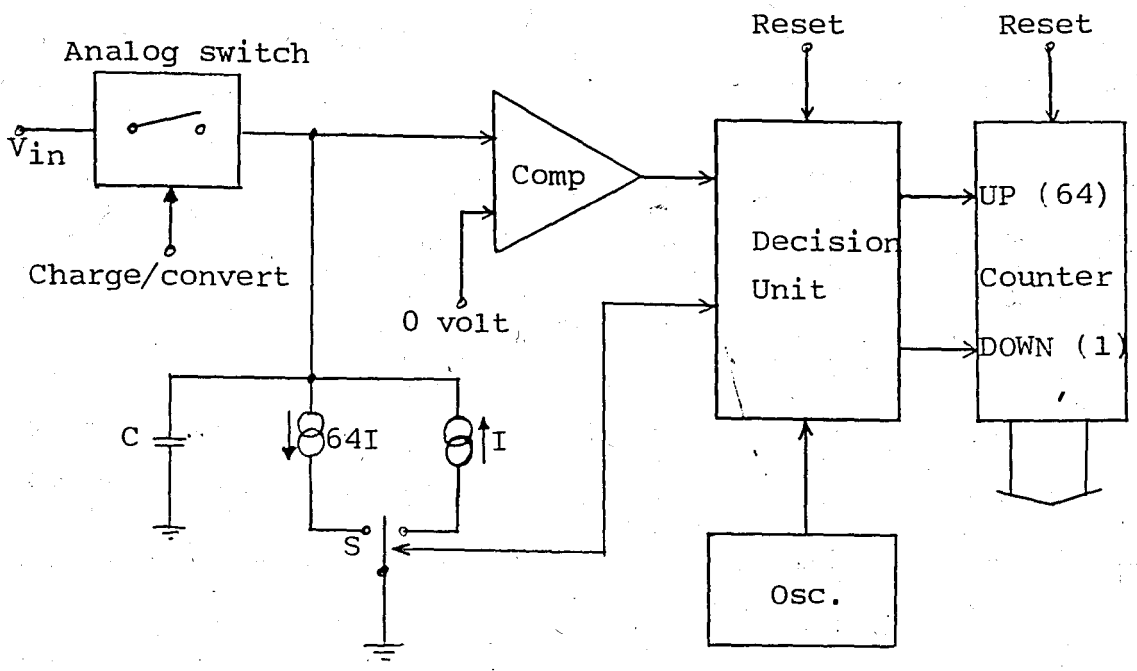


Figure 11:Dual ramp ADC

oscillator output to the count up input of the counter.Each clock pulse increments the counter by 64.After zero crossing, the decision unit switches S to I_2 and connects the clock to count down by one at each clock.So the excess number of counts are taken back.Since two different slopes are used, the ratio of these two must be very precisely adjusted.Also the switching times must be very short comparing with the clock period to avoid false counting,because the delay of only 1/64 of the clock period will result with 1 LSB higher result than the expected number.

It is convenient to tabulate the basic properties of these

ADC's to have a complete idea:

TYPE	SPEED	PRICE	ACCURACY	LINEARITY	PRECISION
Sing.sl.	low	low	medium	high	very high
Dual sl.	low	low	high	high	very high
VFC	very low	high	high	high	very high
Succ.ap.	high	medium	high	medium	low
Flash	very high	very high	high	medium	medium
Wilkinson	low	low	low	high	very high
Dual ramp	medium	medium	low	medium	high

GENERAL DESCRIPTION OF THE BUS AND THE BUS COMPATIBLE ADC

The bus compatibility of the ADC, or in general the data acquisition system (DAS) is achieved by using open collector outputs which are wired-OR to the other units by the bus. The parallel outputs and inputs are designed as negative logic because of the restriction of the wired-OR connection, only the serial output is kept positive logic . The digital bus contains 13 data lines one being the serial output, 3 channel number lines (Since there are 8 analog channels), 2 service unit address lines, one line to inform that the bus is busy, one line to inform that the service unit is working and one line to indicate which unit is specifying the channel number, total of 21 lines. Analog section contains 8 lines. The shortened names of these lines are listed below:

D1...D12 :From LSB to MSB data lines (negative logic)
SO :Serial output (positive logic)
A1,A2 :Service unit address lines (negative logic)
C1,C2,C3 :Channel number lines (negative logic)
FA :Forced address line (negative logic)
BSY :Bus buisy line (negative logic)
WRK :Service unit is working (negative logic)
AD0...AD7:Analog data lines ($0 < V_i < 2.048$ V)

The operation of the bus is very similar to that of a telephone system.When a consumer device needs service,it looks at BSY line.If BSY is low,it has to wait,because it means that another consumer is using the bus.When it sees BSY high,i.e. bus is free,it pulls it low informing that bus will be used.Then it applies the analog voltage to one of the analog data lines (AD0 thru AD7) if this voltage has to be identified by itself (If the analog data lines are already connected to the points to be measured,there is no such step),sets the corresponding (or desired) channel number on C1,C2 and C3 while pulling down FA line (which means "you have to process the voltage on the line I specified") and finally it specifies from which service unit it wants the data by use of the lines A1 and A2.When one of the service units sees that it is addressed,it pulls WRK line low indicating that it understood that it is addressed and is working.When data becomes ready,it pulls WRK high again,which means that the data is ready on the bus.After the consumer device takes the data,it pulls BSY line high, leaving the bus free.

If FA is not pulled down,the analog channel lines must be kept high.In this condition,the counter in the service unit counts one and processes the next channel voltage and as the output it gives the channel number besides the data.

A service unit cannot have the address 00 ,i.e. A1 and A2 both high because the service unit is triggered by its address and 00 is the idle position of the bus.

The serial output has a variable BAUD rate,presettable by the jumpers on the DAS digital input-output and successive approximation register (SAR) logic board,1801.When data becomes ready,the DAS pulls SO line low for one bit long as the start bit,then gives the data starting from the MSB,adds the three bit channel address at the end,then pulls SO high.

The internal counter for channel addressing is put to decrease the required number of lines for long distance communication. This way a consumer has to specify only the service unit address by two lines,and take the data from the serial output line.If channel number is not the desired one,it can request a new data by keeping BSY low (that way it does not lose control of the bus).It can go on until the consumer receives the data of the desired channel.So only 4 lines are used for this purpose:BSY,A1,A2,SO.

PRINCIPLE OF OPERATION

When the system is addressed,Address Sense Block sends a message to the State Information.If BSY is low,State Information Block sends a message to output by pulling WRK low, increments the channel number by applying a pulse to Channel Incrementer and also applies a pulse to the Bit Selector of the SAR which clears all the bits of the Bit Memory Array. The Channel Select looks at FA,if it is low,takes C lines as inputs,if high,puts the data of the Channel Incrementer on C lines.Analog Data Selector selects one of the analog channels according to the data given by Channel Incrementer. This analog data is buffered,sampled and hold,and applied to one of the inputs of the comparator.The bit selector , then,starts to sweep the sits to be tested.Each time the DAC gives an analog equivalent of the new combination of the bits and applies it to the comparator.The bit selector also specifies the bit that has to be resetted if necessary and this information is given to the Addressed Reset Block. After the test of all the bits are comleted,the bit selector informs that the job is comleted,and by this information the parallel to serial converter is loaded while the state information was pulling WRK high.The parallel data passes

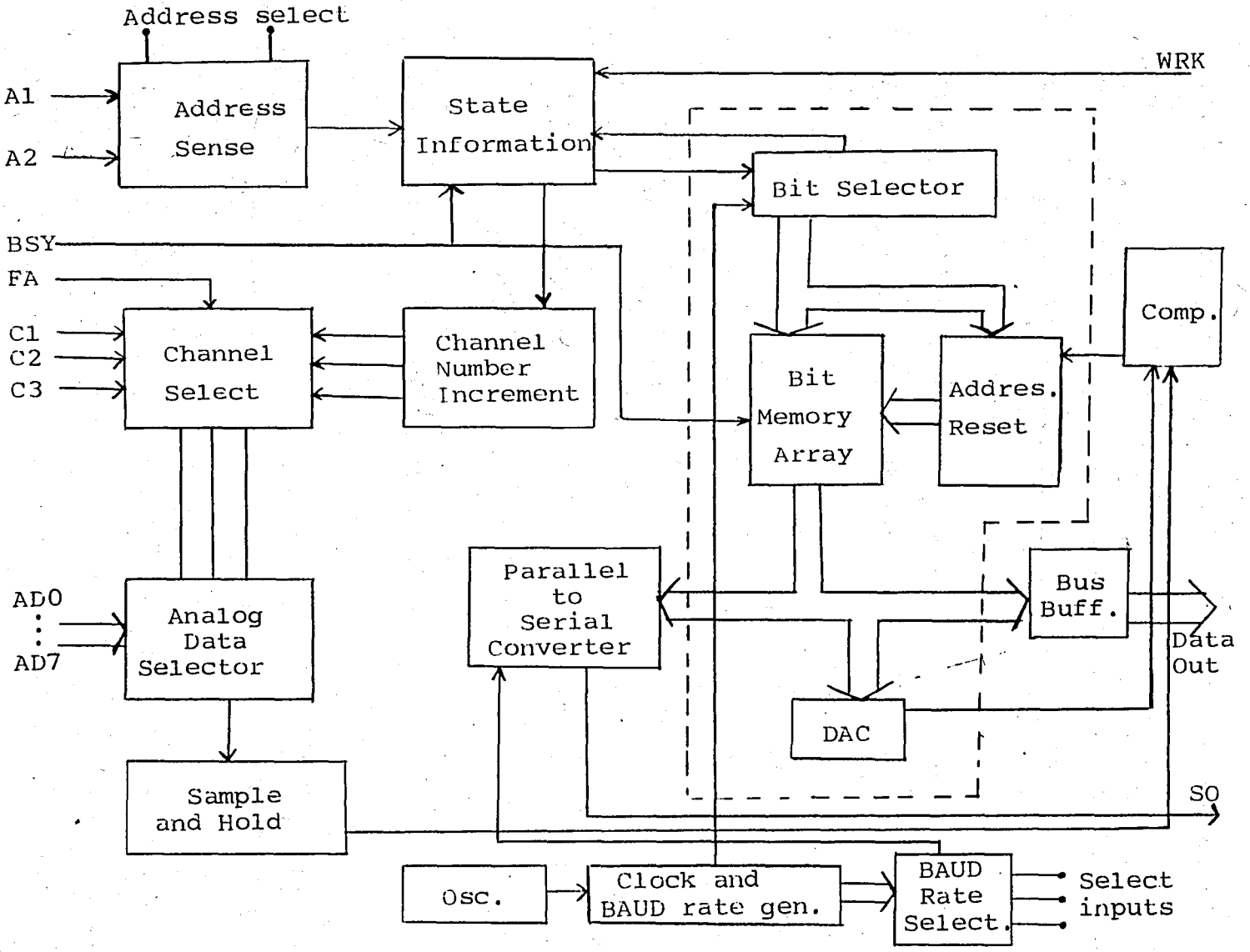


Figure 12:Block diagram of the Data Acquisition System

through the bus buffer,which is a set of open collector invertors.The parallel to serial converter sends the data on the SO line with the BAUD rate specified by the Baud Rate Generator and the Baud Rate Selector.To convert a new sample, the address must be removed and applied again.

The Address Sense circuit consists of two inverters and an AND gate.The address inputs are negative logic (i.e. 0 volt means "1" state).

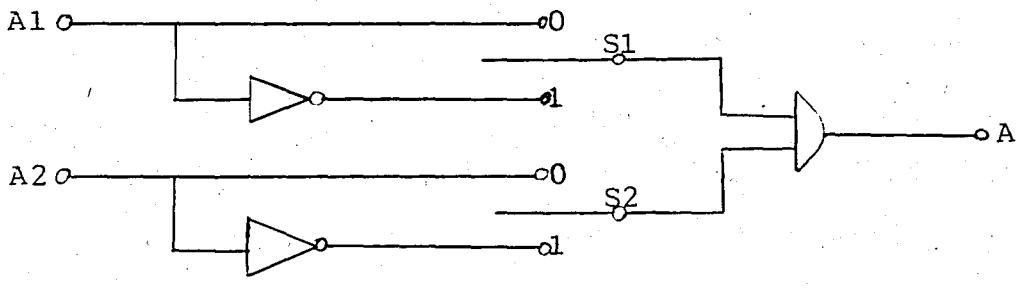


Figure 13:Address Sence circuit

By use of S_1 and S_2 ,address can be changed.00 cannot be used as an address since it is the idle position of the bus.

The State Information logic has a 4 μsec monostable and three flip-flops for the sequential informations.The flip-flops are used as D flip-flops with D="1".When the DAS is addressed, mono is triggered and the FF2 is triggered by $\bar{Q}$ of the mono.

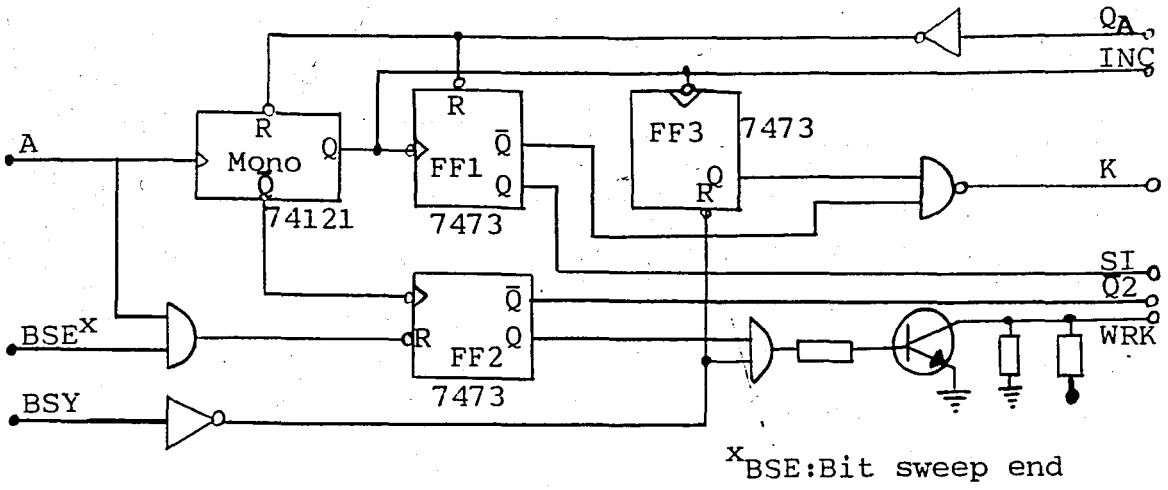


Figure 14:State Information circuit

Since BSY is "1",Q2 and BSY results with WRK="1".After waiting for about 4 μsecs for the Sample and Hold to settle,Q of the mono triggers FF1 and FF3,Q1 and Q2 gives K="1" and SI="1". After the first clock pulse,Q_A becomes "1" resetting FF1, resulting with SI="0" from then on.At the end of the sweep of the bits,BSE becomes low which resets FF2,so pulls WRK high.

The Bit Selector is made up of two shift registers,to obtain 12 bits,one 8 bit and one 4 bit shift registers are cascaded. The different clock signal requirements of these two caused the need of two phase clock.The SI is shifted by this 12 bit shift register,each time one bit being "1".Ck1 is 180 degrees phase shifted and about 20 nsec. delayed,so AND gating them results with a 20 nsec. spike at BSE if Q_D is "1",which is

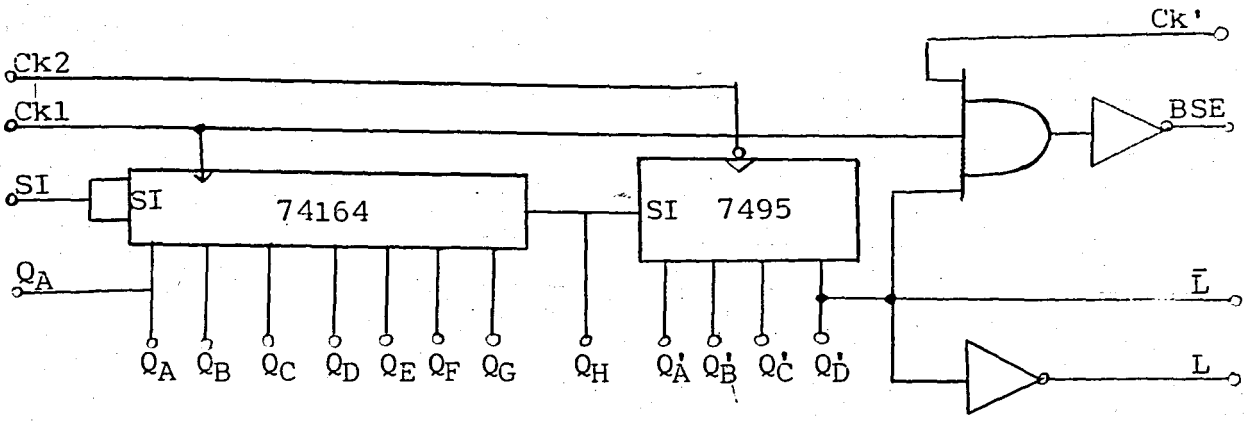


Figure 15:Bit Selector circuit

the end of the conversion.After BSE is given,all the bits of the shift register are left as "0".

The Addressed Reset consists of 11 NAND gates and an invertor drived by a three input AND gate.Each bit of the Bit Memory Array is an independent flip-flop each connected to one of the NAND gates.The gates are drived by a three input AND gate according to the state of the comparator and the clocks.

When K is "1",at the first clock pulse,QD12 becomes "1" while all others were turning to "0".At the second clock,next flip-flop is set to "1",and according to the state of the comparator the output of the three input AND fate gives the information if FFD12 must be resetted or not,and this is NAND gated by Q_A to reset only FFD12 if required.The procedure goes on similarly

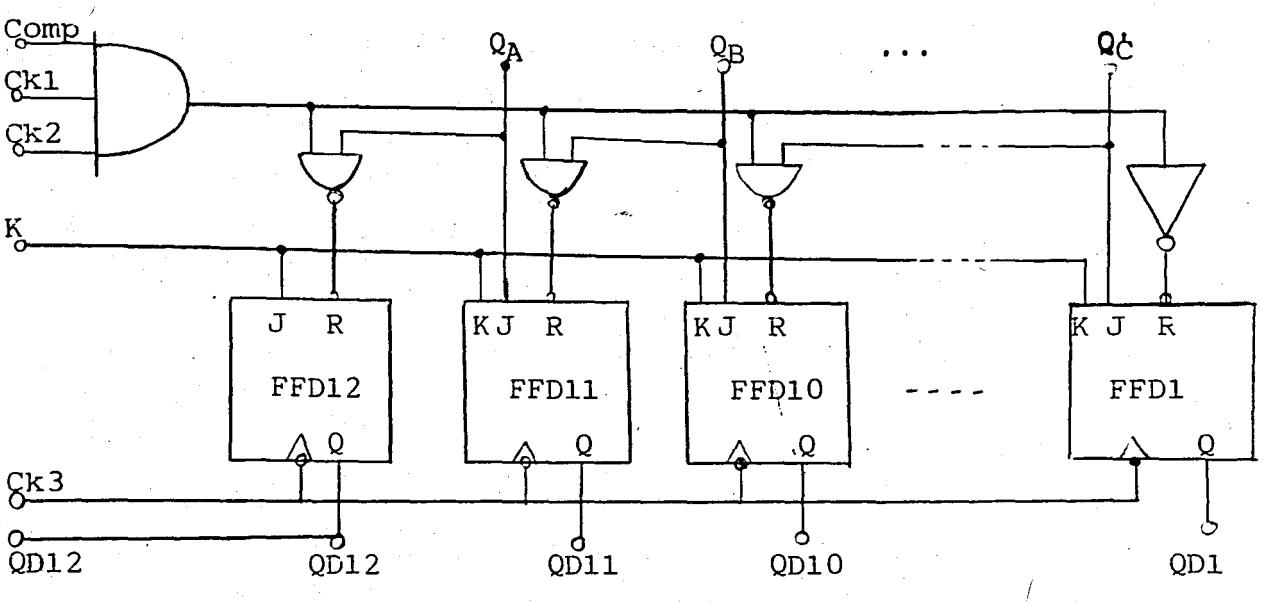


Figure 16:Addressed Reset and Bit Memory Array

for the remaining bits.The reset input of the last flip-flop does not require gating because it is the last bit to be decided and no other reset information will be applied to the bit memory array from then on.

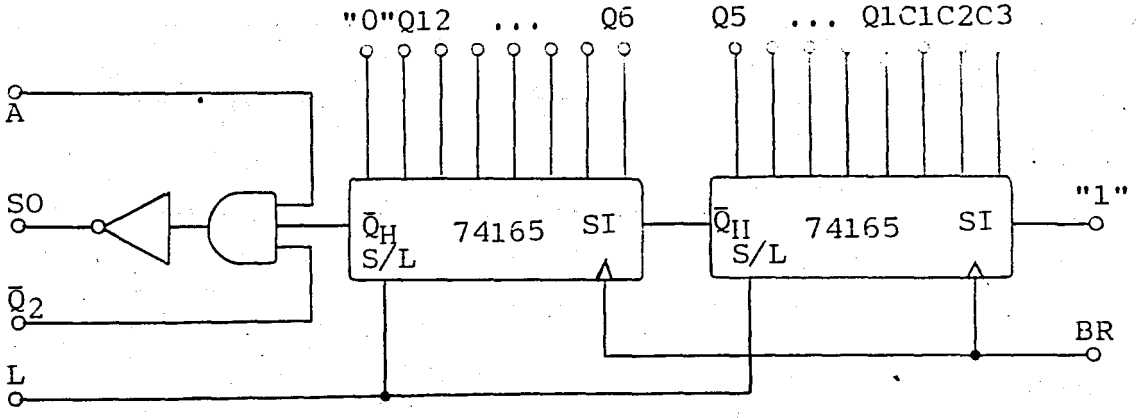


Figure 17:Parallel to Serial Converter circuit

Parallel to Serial Converter is a 16 bit parallel in serial out shift register obtained by cascading two 8 bit ones. One start bit,12 data bits and 3 channel address bits are sent by this shift register,a total of 16 bits.When the conversion is end (i.e. $\bar{Q}2$ is "1"),at the first clock pulse while L was low loads the shift register with a "1" appearing at $\bar{Q}_H$.This results with one start bit of "0" appearing at SO. Then,according to the BAUD rate selected and applied to BR, 12 bits are sent (starting from the MSB),adding the three channel number bits starting from the LSB.If the address is removed before the end of the serial output,sending of the data is stopped.At the end of the message,the "1" at the serial input of the shift register fills all the bits and SO remains at "1".

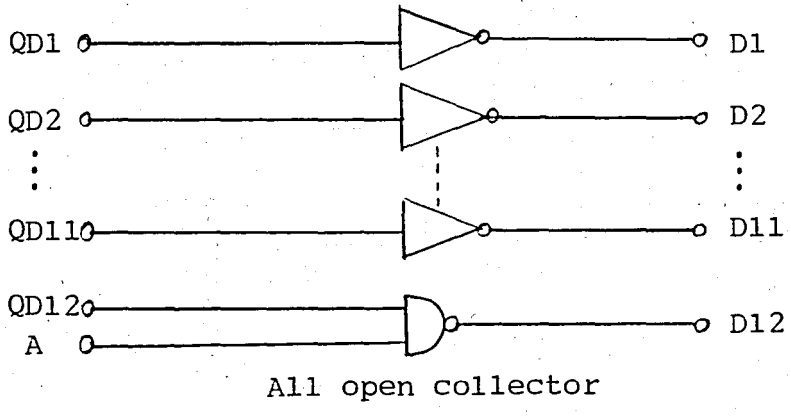


Figure 18:Bus Buffer

The Bus Buffer is made up of 11 open collector invertors and an open collector NAND gate.The Q's of the bit memory array flip-flops from 1 to 11 are directly connected to the invertors. The 12'th bit is NAND gated by the address information ,A, because when the DAS is not addressed,QD12 stays at "1" and if it is directly applied to the buffer-invertor,it will pull the D12 line low as a wrong information.

The channel incrementer is a three bit counter made up of one 7490.The channel select block consists of a quad 2 to 1 line multiplexer,74157,in which three of the multiplexers are used, a quad latch,7475,and open collector NAND gates.

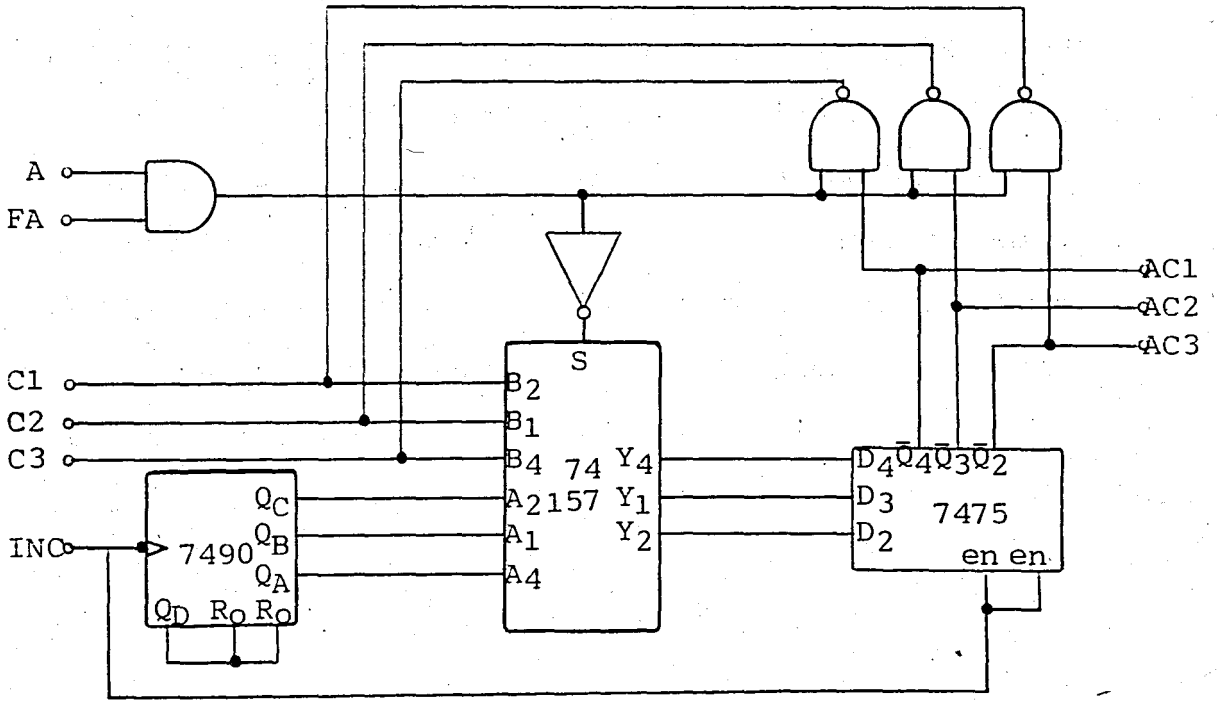


Figure 19:Channel incrementer and channel selector circuit

When the DAS is addressed,INC becomes "1" for 4 usecs and the outputs of the multiplexer are latched in 7475.This data is selected according to the state of FA.If it is "0" (i.e. it is high),the channel number selected by the 7490 counter is accepted as the channel number and the open collector NAND gates are opened to force this number on the C lines.If FA is "1",the NAND gates are closed letting the C lines as the inputs to be selected.The outputs of 7475 are then sent to the analog multiplexer by AC lines.At the end of the INC pulse,latch is disabled and the counter counts one to be prepared for next data request.

Analog data selector is a single chip CMOS 8 to 1 analog multiplexer (14051).Buffer and the samle and hold circuitrary is accomplished by use of a double FET input op-amp (TL082). High slew rate of 12 volts/usec. of these op-amps were satisfactory in application of this sample and hold circuit.Inputs of the multiplexer are protected by connecting 1.1 kohm resistors in series.Output of the multiplexer,which is connected to the first op-amp is biased by inserting a 90 Mohms resistor between this point and ground.The multiplexer select inputs are connected to AC1 thru AC3,the outputs of the latch. As the analog switch of the sample and hold circuit,a CMOS one with low ON resistance (14066) is used.Output of the S/H is connected to the comparator.

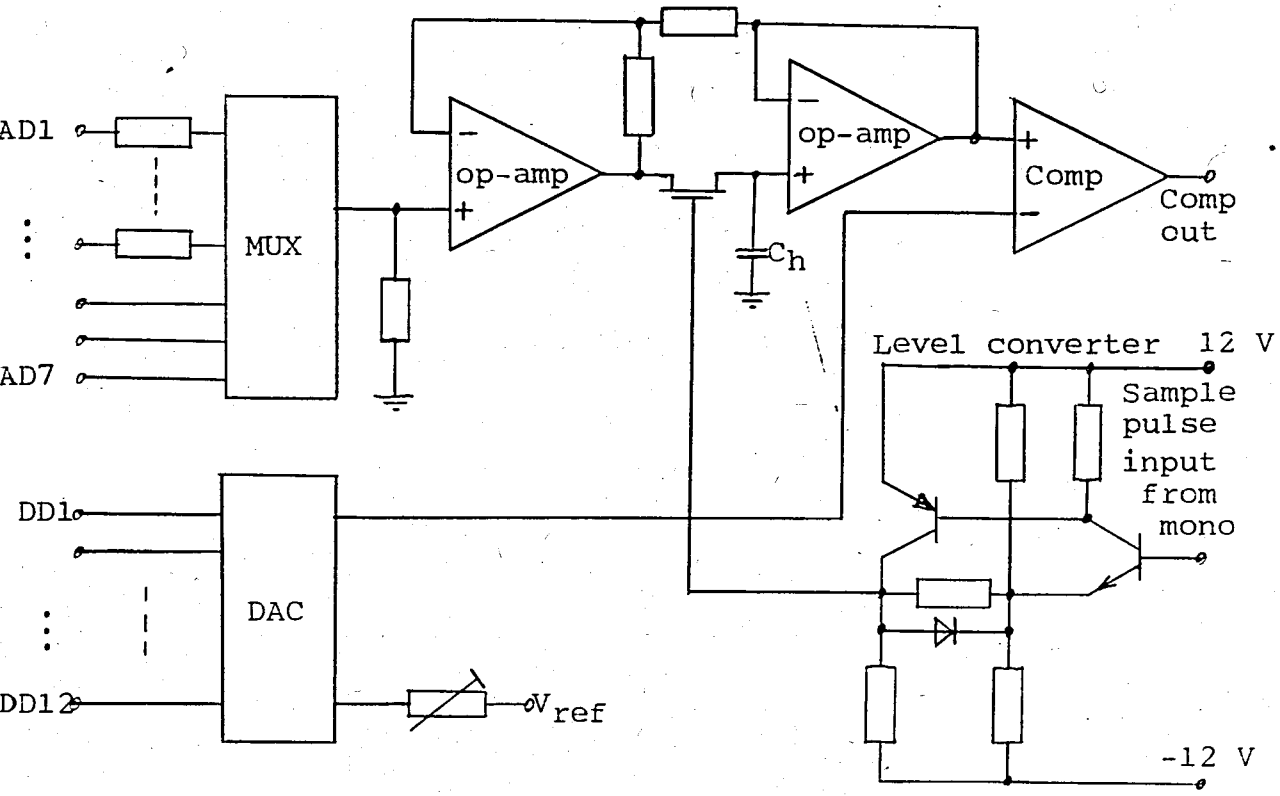


Figure 20:Analog section circuitrary

The comparator used is a very sensitive and fast one,LM361, with gain of 5000 and propogation delay of less than 15 nsec. This much sensitivity was required because the input voltage and the DAC voltage are restricted at 2.048 volts maximum. For 12 bits, it makes .5 mvolts per LSB.The 4 μsec. pulse coming from the first monostable is fed to a level converter to obtain the required ON and OFF voltage levels of the analog switch.The analog multiplexer and the analog switch are fed with plus-minus 5 volts which are obtained from the 12 volts by use of zener diodes.

The DAC is made up of discrete components instead of buying one from the market.This is decided because of the hardness of finding a fast 12 bits one.It is designed with the current switches to achieve low setup time.For 12 bits,12 current sources and 12 current switches are used.The outputs of the current switches are connected to an R-2R ladder network which has 100 ohms characteristic impedance..

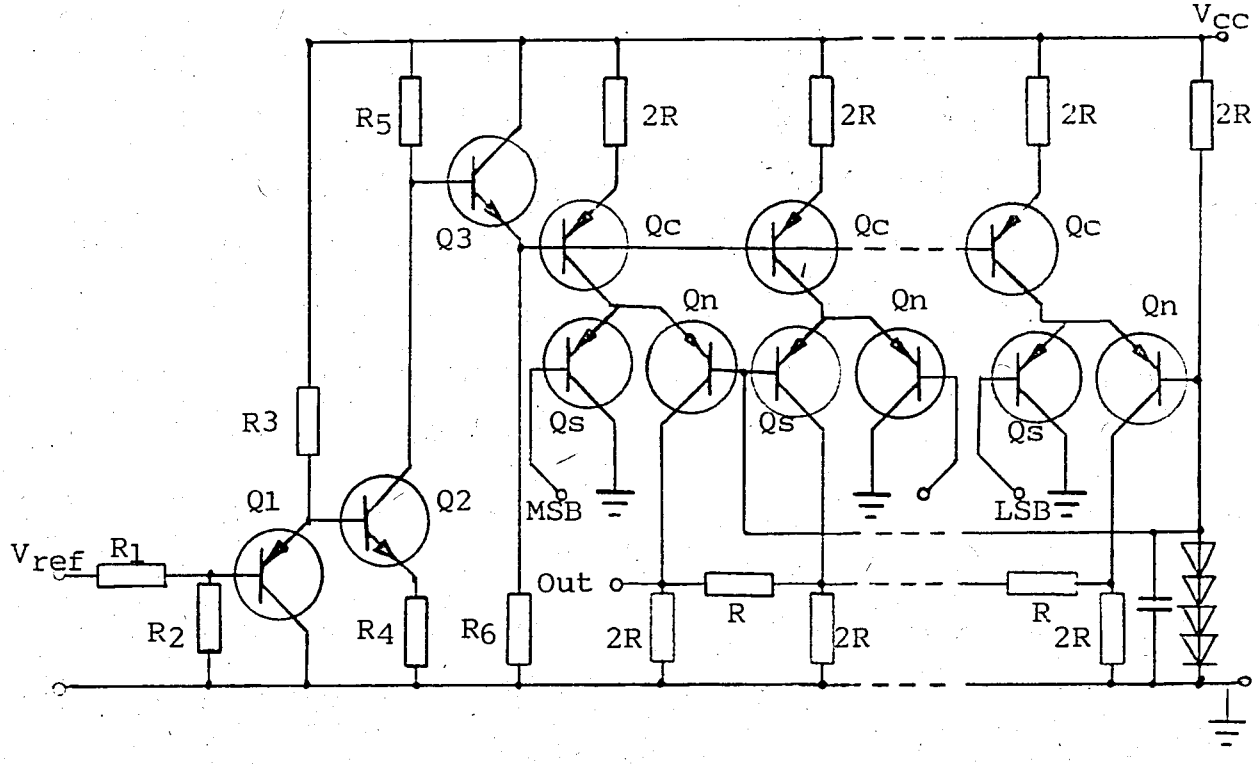


Figure 21:DAC circuit

High speed switching is accomplished by use of emitter coupled logic configuration . The Qs and Qn in the DAC circuit diagram makes a current switch.The bases of all Qn's are connected together to a constant voltage of approximately 2.5 volts. This voltage is assumed to be the reference voltage of these switches,such that if the voltage at the base of Qs is lower than this voltage,Qs will conduct and sink all the current that the current source is sourcing.If it is higher,then the current will flow into the ladder network.

To obtain a current source with low temperature drift,the transistors are connected in such a way that the voltage drift of one of the transistor's base-emitter junction is ~~been~~ compensated by the other's.Q2 is used as a current source to shift the reference voltage to with respect to Vcc.This current is determined by the voltage on R4,so at first it is required to keep this voltage stable.This is accomplished by inserting one more base-emittor junction,Q1.This way the voltage at the base of Q1 is transferred to R4 with high stability.It resulted with a stable voltage on R5,too.The Qc's are the current sources,again requiring stable voltages on the 2R resistors at their emittors.Now,Q3 is put to improve two effects,one is it is used as a buffer to reduce the current sinked from R5,other , the base-emittor junction is compensating the unstability of the base-emittor voltages

of Qc's.

As the reference voltage,a high stability one is used.The only problem left was the precise resistors.This is solved by selecting the identical ones among many high quality metal film resistors.As a result,all resistors are selected within 0.05% tolerance.

CONCLUSION

The desired specifications could not be obtained completely because of the practical problems that arose in the analog section of the system.The conversion time that was desired to be achieved was as low as 2.5 μsecs,but this was thought without a sample and hold circuitry.The insertion of the sample and hold circuit increased the time by 4 μsecs.

To obtain bipolar operation characteristics,it was thought to design a DAC with bipolar output and compare it directly with the input voltage.This type of operation is tried to be realised by feeding the DAC with two split supplies,but it resulted with sustained oscillation.So the design is changed to a single supply DAC and the input voltage is shifted up and applied to the comparator.

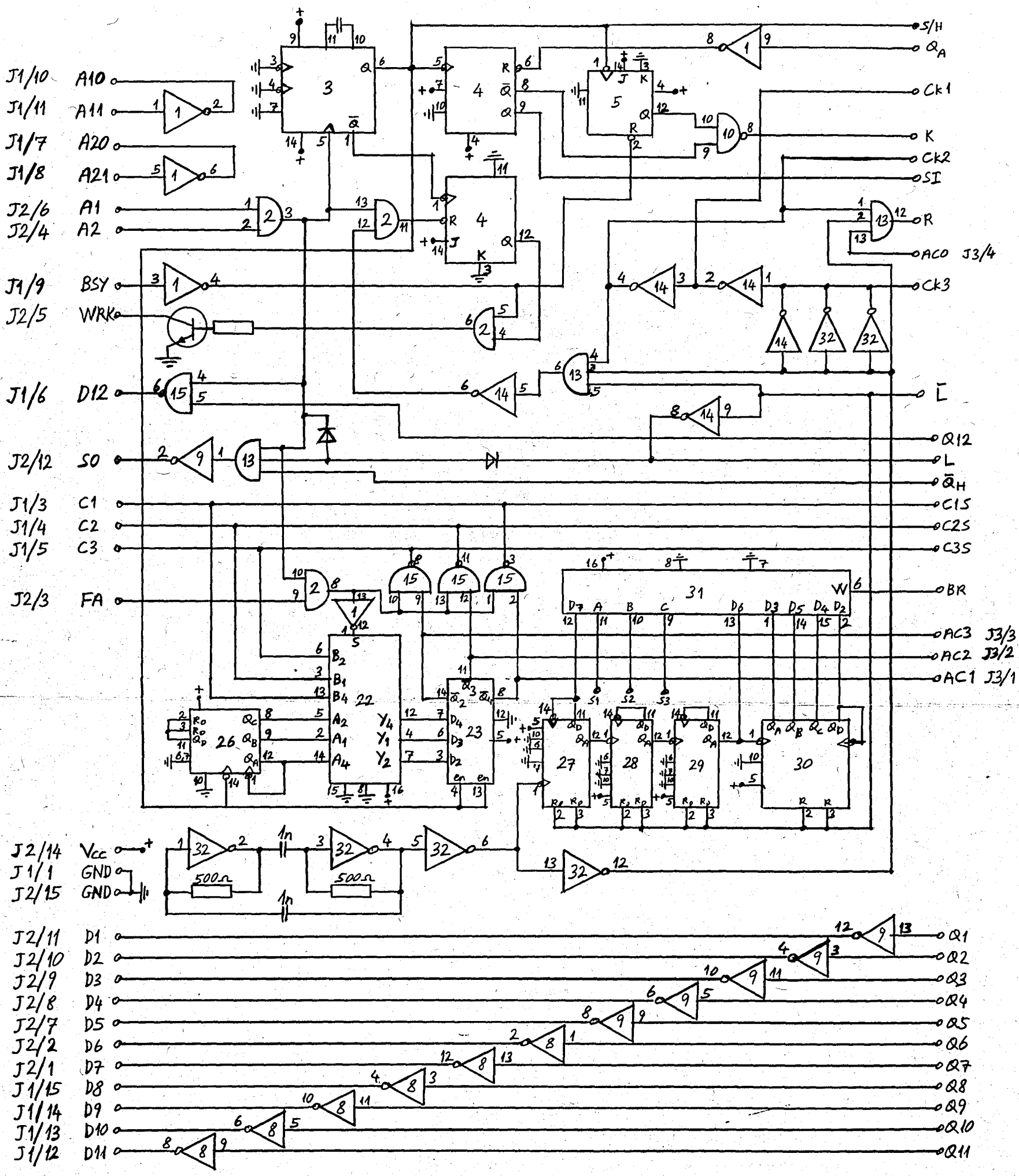
Even in this condition,there still were some overshoot and dumping oscillation at the output of the DAC.To optimize the readout accuracy,system speed had to be reduced and this way an accuracy of 9 bits is reached.Remaining 3 bits are left in in the oscillating region.By use of a computer,if higher

resolution is desired,it is possible tc take more samples and calculate the statistical average,which is almost equivalent to decreasing the system speed.

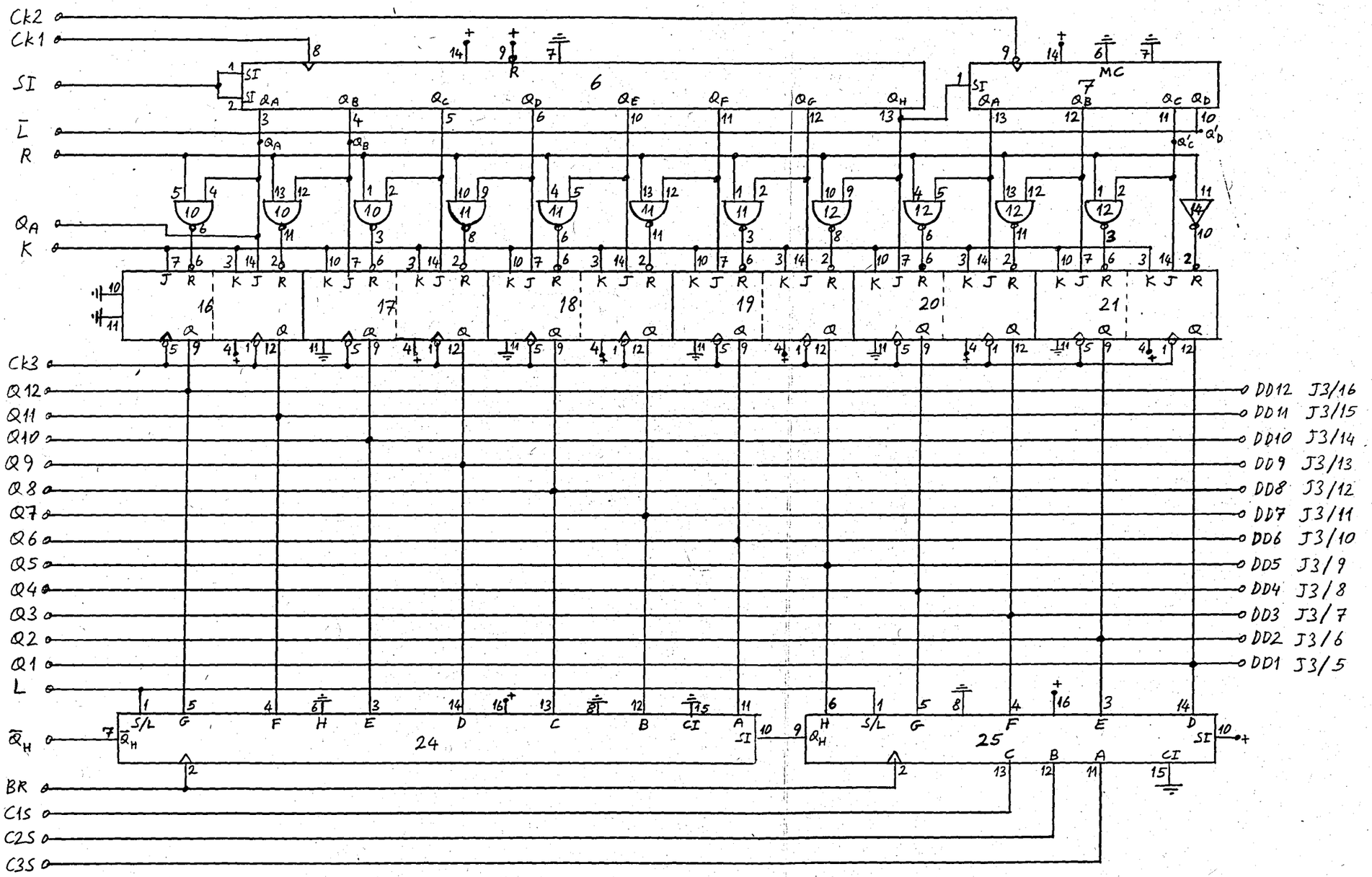
The successive approximation register part,i.e. the digital part of the system is working successfully.It is seen that all of the problems arose in the analog part.As a further study,it is possible to design a better analog part for this system to achieve true 12 bit accuracy.In this case only the upper printed circuit board has to be changed.

This system is thought to be operated in conjunction with a computer.But the bus system itself has a drawback for such an operation without a hardware between the computer and the bus.Since there is no controller on the bus,it is required to "catch" the bus immediately after BSY is seen high. For a computer,it is the easy way to look at this line,then, if it is high,send BSY according to the program flow.But the time which passes between seeing it high and sending the message,which is in the order of μsecs for a computer,may cause problems in such a way that during this time it is possible for another consumer to begin to work on the bus. To overcome this,a simple hardware has to be connected between the computer and the BSY line.

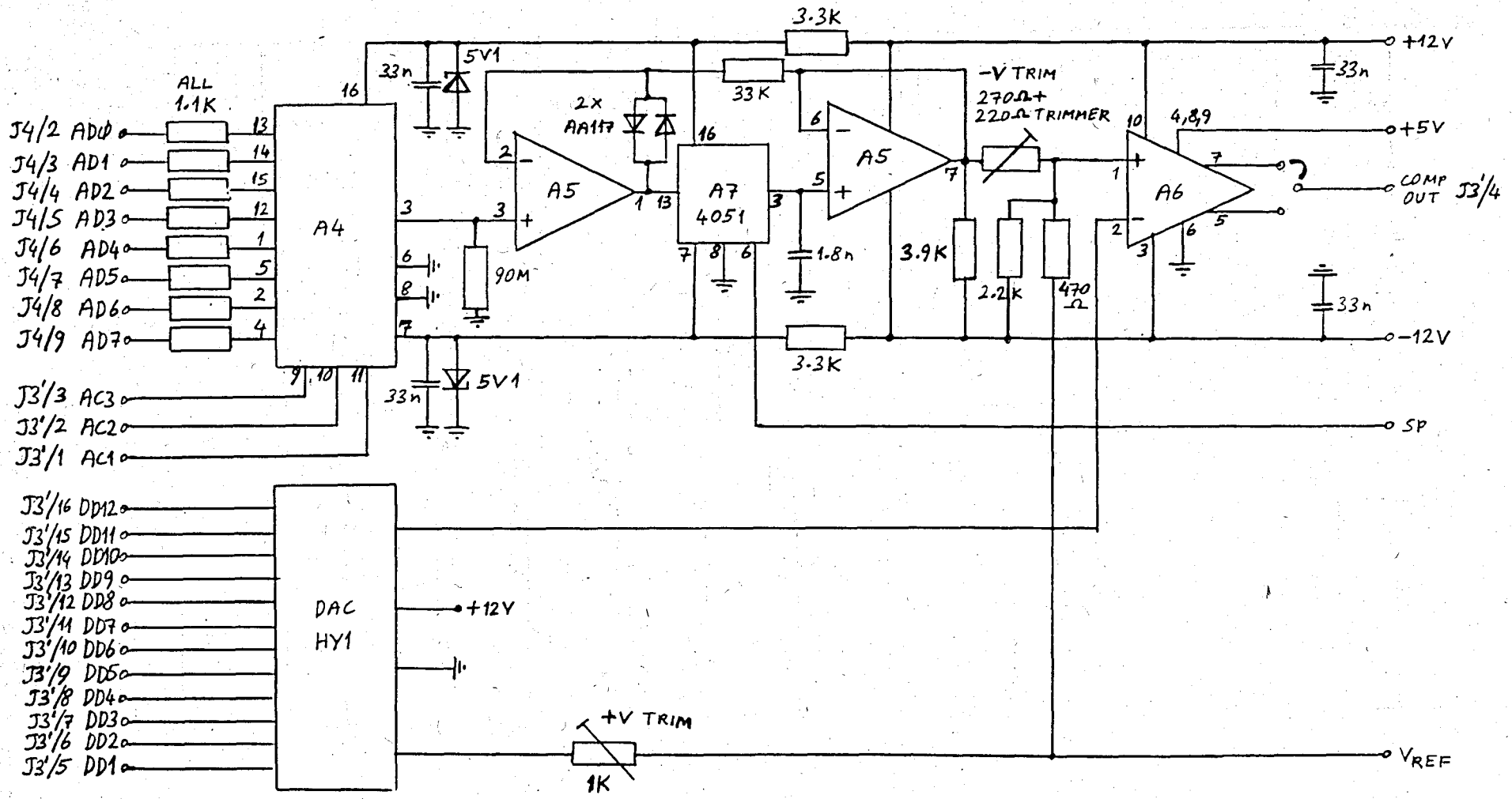
The system,now,is in such a situation that it can be used in many applications,and it is open to further developments.



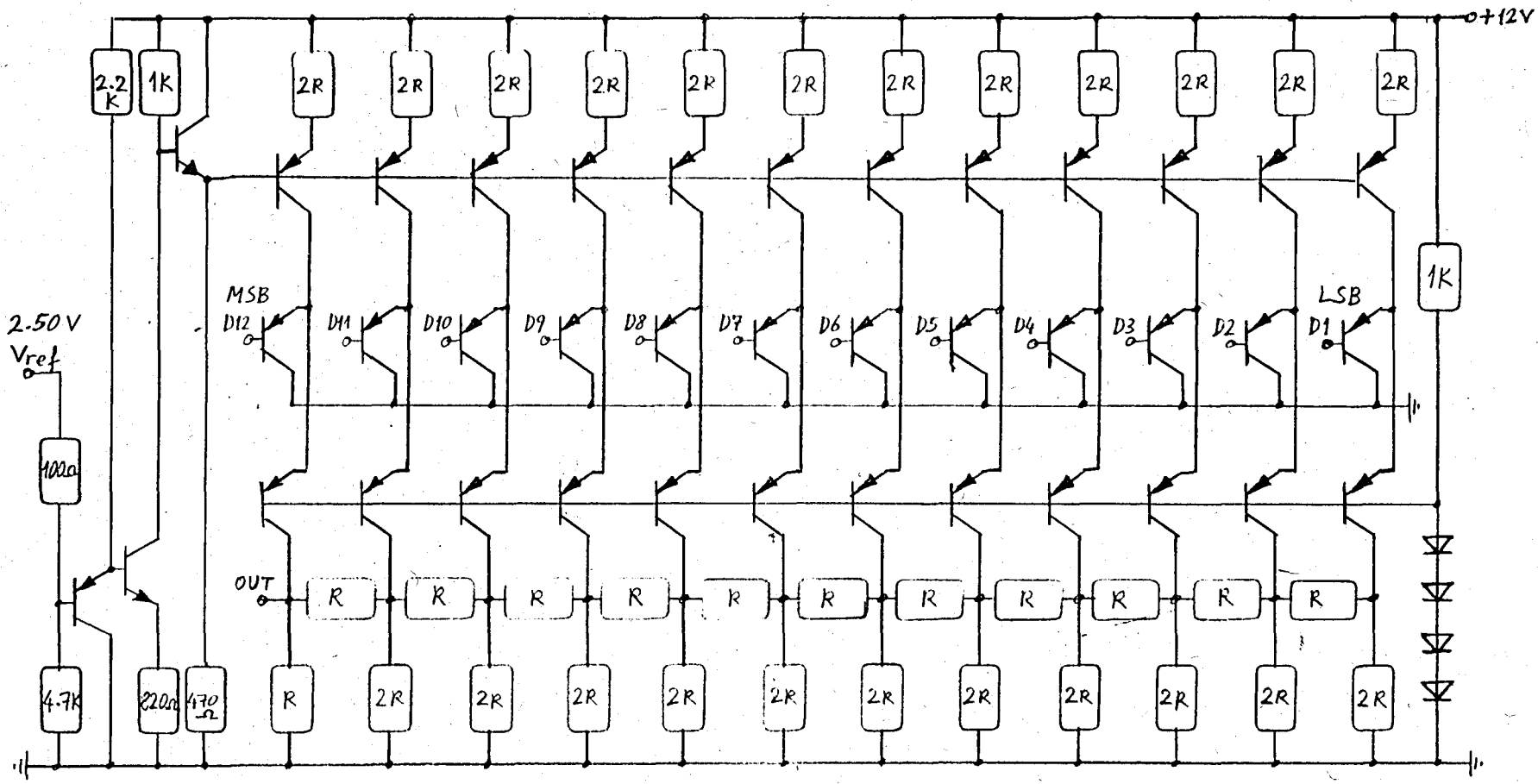
DIGITAL PART (A)



DIGITAL PART (B)



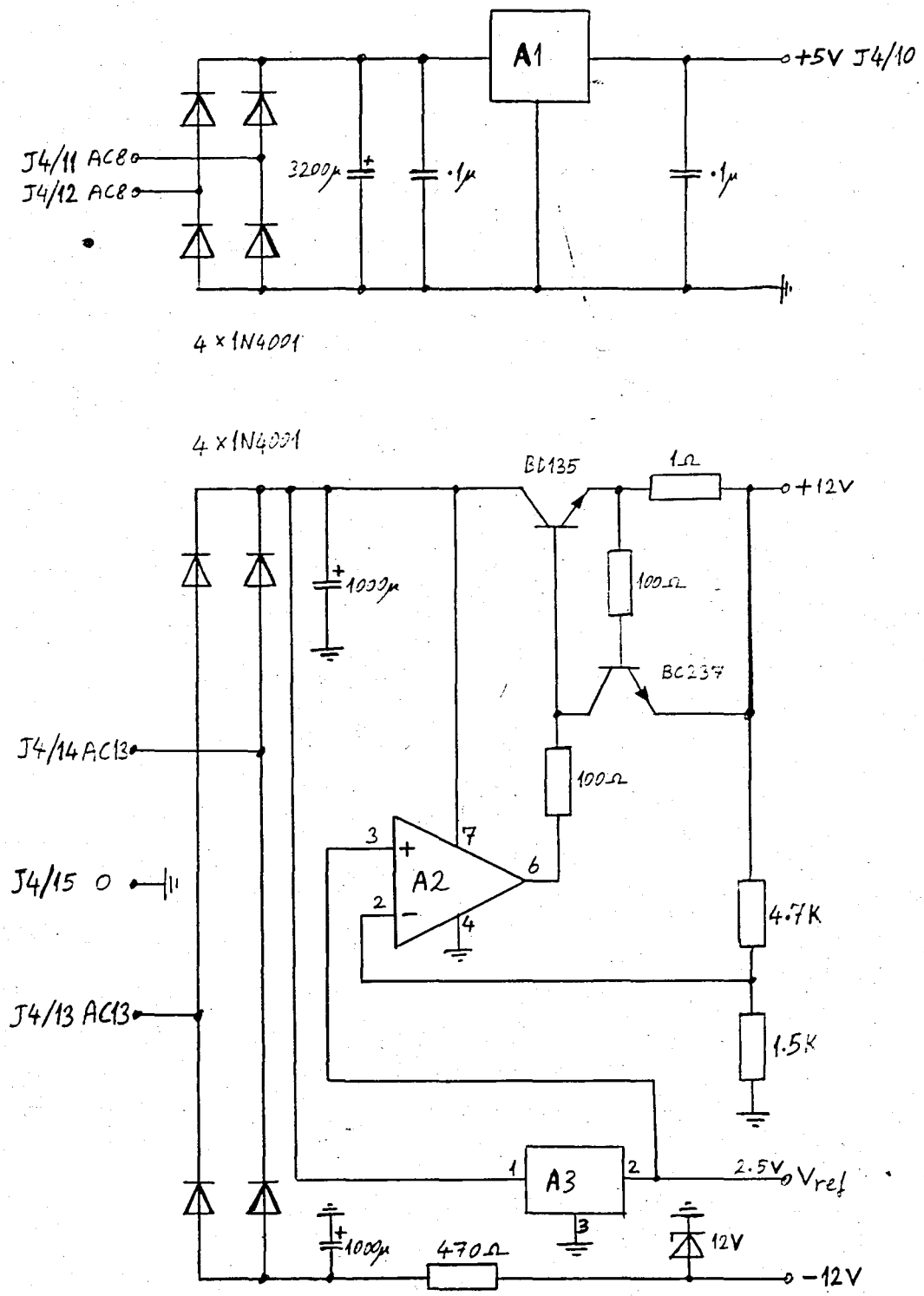
ANALOG MUX AND S/H



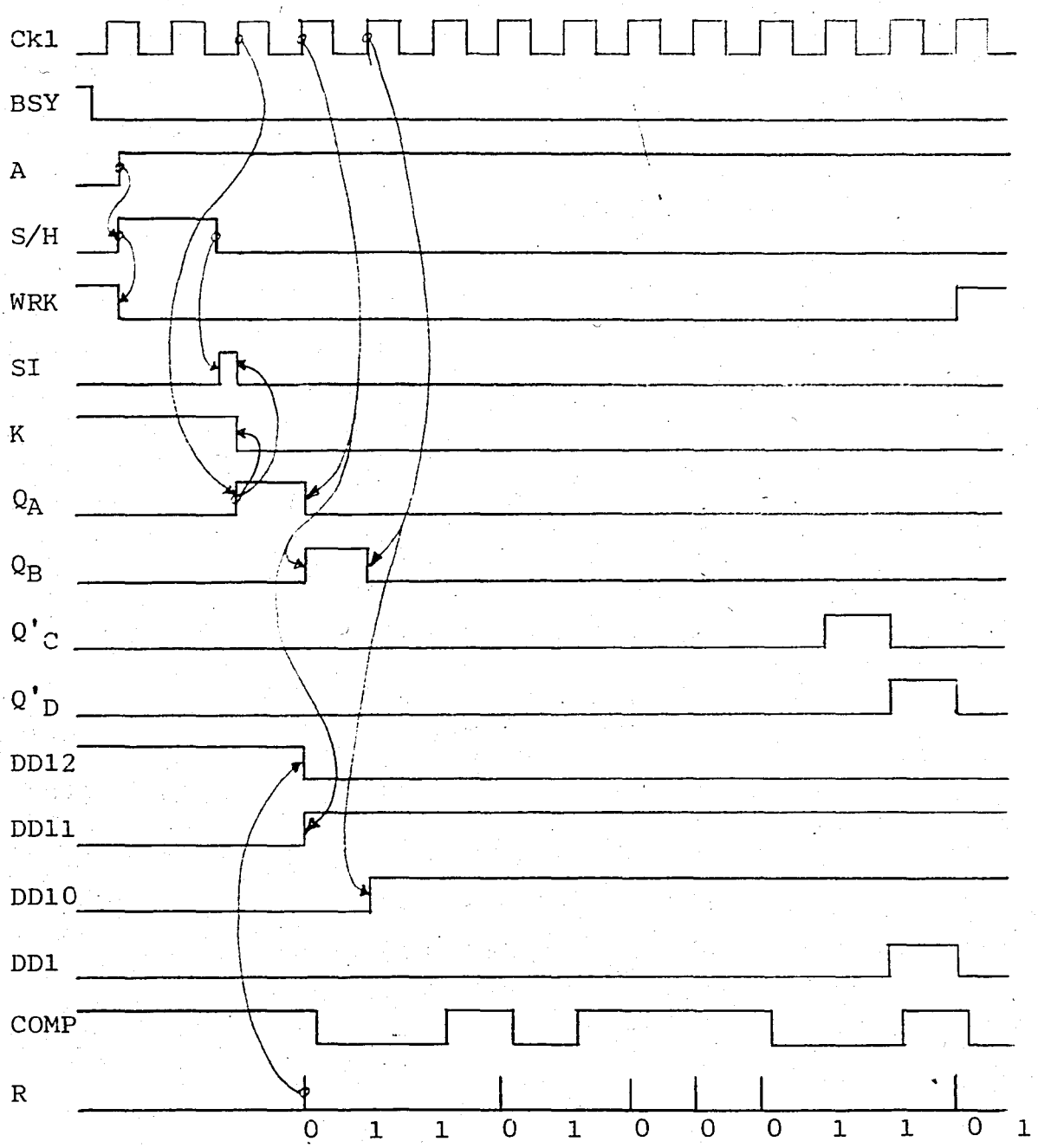
ALL NPN TRANSISTORS ARE BC237, PNP ARE BC308

R = 150Ω 0.5% METAL FILM

DAC



POWER SUPPLY



WAVEFORMS OF ADC

TECHNICAL SPECIFICATIONS

Analog part:

Input voltage range	:0 to 2.048 volts
Input resistance	:90 Mohms
Number of channels	:8
S/H time	:4 µsecs
Power requirement	:12 V 160 mA
	-12 V 20 mA

Digital part:

Clock frequency	:1.5 MHz
Conversion time	:8 µsecs
Inputs fan in	:2 standart TTL
Outputs fan out	:9 standart TTL
Power requirement	:5 V 700 mA

COMPONENTS LIST

Digital Part (Integrated Circuits)

1	7404	17	7473
2	7408	18	7473
3	74121	19	7473
4	7473	20	7473
5	7473	21	7473
6	74164	22	74157
7	7495	23	7475
8	7406	24	74165
9	7406	25	74165
10	7400	26	7490
11	7400	27	7490
12	7400	28	7490
13	7411	29	7490
14	7404	30	7493
15	7403	31	74151
16	7473	32	7404

Analog Part (Integrated Circuits)

1	7805
2	741
3	MC 1403
4	MC 14051
5	TL 082
6	LM 361
7	MC 14066

APPEDDIX A

Interfacing with a microprocessor

For demonstration,the system is interfaced to a microcomputer based on 8085.Interfacing is done via a triple port, 8255 of Intel.The C and B ports are assigned to be inputs and A port to be output.The first 7 lines of port A are used as outputs from the computer.These are assigned in such order:

A0,A1,A2	:Channel address
A3	:FA line
A4,A5	:Device address
A6	:BSY line
A7	:Not used

The B port is connected to first 8 of the data lines.i.e. to the lowest 8 bits.Low half of the C port is connected to the remaining 4 bits.WRK line is connected to C7.C4,C5 and C6 are not used.

The inputs to the computer are connected directly to the bus.The outputs of the computer,A0 thru A6,are connected to the bases of 7 transistors and the collectors of these

transistors are connected to the bus since the bus configuration is open collector.

As the input-output of the computer, a teletype is used. The program is such prepared that entering the desired channel number is enough to operate the system. Computer asks for the voltage of that channel, converts it to BCD and writes the channel number and the voltage. The source code of the program is given in Appendix B.

APPENDIX B

Sample program for 8085 to use the DAS

In this program,it is assumed that the port is previosly programmed and the monitor program has the input-output subroutines available for the user program.

```
START  MVI A,CR      SEND CARRIAGE RETURN
       CALL OUTCHR
       MVI A,LF      SEND LINE FEED
       CALL OUTCHR
       CALL INCHR    GET CHANNEL NUMBER
       SUI 30H
       CPI 8         BETWEEN 0 AND 7?
       JNC START     IF NO DON'T ACCEPT ENTRY
       MOV B,A       IF SO START CONVERSION,SAVE NUMBER
       LDA 30H
       STA DECIM     STORE 0 TO THE PLACE AFTER
                     DECIMAL POINT
       LDA 2EH
       STA DP        STORE DECIMAL POINT
       MVI A,BSY
```

```
        OUT PORTA       SET BSY LINE
        ORI 80H         SET FA
        ORA B
        OUT PORTA       SET CHANNEL NUMBER
        ORI 30H
        OUT PORTA       SET DEVICE ADDRESS
LOPWRK  IN PORTC
        ANI WRK         TEST FOR END OF WORK
        JZ LOPWRK       IF NOT END YET
        IN PORTC        TAKE HIGHEST 4 BITS
        CMA             COMPLEMENT TO OBTAIN IN POSITIVE LOGIC
        ANI 15          DISCARD NON DESIRED BITS
        RRC             TAKE HIGHEST 3 BITS
        MOV H,A
        IN PORTB        TAKE LOW 8 BITS
        CMA
        RRC             LSB TO CARRY FLAG
        MOV L,A
        JNC CONT1       IF LSB IS ZERO
        LDA 35H         IF LSB IS '1',IT HAS A VALUE OF
        STA DECIM       0.5 MILLIVOLTS
CONT1   LXI D,BCDSAV    ADDRESS OF THE CONVERTED BCD NUMBERS
                        TO BE STORED
        PUSH B          SAVE CHANNEL NUMBER
        CALL BIDE       PERFORM BINARY TO BCD CONVERSION
```

```
        POP B
        MOV A,B
        ADI 30H         ASCII EQUIVALENT OF THE CHANNEL NO
        CALL OUTCHR     SEND CHANNEL NUMBER
        MVI A,SP
        CALL OUTCHR     SEND A SPACE
        LXI D,BCDSAV    BCD NUMBERS TO BE SENT
        MVI B,COUNT     NUMBER OF CHARACTERS TO BE SENT
OUTLOP  LDAX D
        CALL OUTCHR     SEND THE NUMBER
        INX D           DE POINTS NEXT NUMBER TO BE SENT
        DCR B           COUNT
        JNZ OUTLOP      IF NOT END OF CHARACTERS YET
        JMP START       GO TO WAIT FOR NEXT ENTRY
CR EQU 13
LF EQU 10
BSY EQU 40H
WRK EQU 80H
DP EQU BCDSAV-4
DECIM EQU BCDSAV-5
COUNT EQU 6
                        INPUT AND OUTPUT ROUTINE ADDRESSES
                        AND THE PORT ADDRESSES HAVE TO BE
                        SPECIFIED BY THE USER
```

```
                    THIS SUBROUTINE PERFORMS 12 BIT
                    BINARY TO BCD CONVERSION
BIDE    MVI B,3     COUNTER
        PUSH B      SAVE COUNTER
        PUSH H      SAVE NUMBER TO BE CONVERTED
        LXI H,TABLO TABLE OF CONSTANTS
NXTNO   MOV B,M     GET THE CONSTANT IN BC
        INX H
        MOV C,M
        INX H
        XTHL        TAKE NUMBER IN HL AGAIN
        MVI A,-1    BCD NUMBER COUNTER
NXTLOP  INR A
        DAD B       SUBTRACT CONSTANT FROM HL
        JC NXTLOP   IF NEGATIVE NUMBER NOT FOUND YET
        ADI 30H     ASCII OF THE BCD NUMBER FOUND
        STAX D      STORE IN (DE)
        INX D       NEXT LOCATION TO BE STORED IN
        XRA A
        SUB C
        MOV C,A
        MVI A,0
        SBB B
        MOV B,A     NEGATIVE OF THE CONSTANT CALCULATED
        DAD B       PREVIOUS NUMBER OBTAINED IN HL
        POP B       TABLE ADDRESS TO BC
```

```
        XTHL            COUNTER TO H
        DCR H           COUNT
        XTHL
        PUSH B
        XTHL            RETURN TO ORIGINAL POSITION
        JNZ NXTNO       IF NOT END OF CONVERSION
        POP H
        POP B           ADJUST STACK
        MOV A,L         LEAST SIGNIFICANT DIGIT
        ADI 30H         ASCII EQUIVALENT
        STAX D          STORE
        RET
TABLO   BYTE ECH,18H
        BYTE FFH,9CH
        BYTE FFH,F6H
```

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DATEL INTERSIL Data Acquisition Component Handbook

ANALOG DEVICES Data Acquisition Components and Systems