DESIGN AND FABRICATION OF RF MEMS SWITCHES AND INSTRUMENTATION FOR PERFORMANCE EVALUATION

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ABSTRACT

DESIGN AND FABRICATION OF RF MEMS SWITCHES AND INSTRUMENTATION FOR PERFORMANCE EVALUATION

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This thesis presents the RF and mechanical design of a metal-to-metal contact RF MEMS switch. Metal-to-metal contact RF MEMS switches are especially preferred in low frequency bands where capacitive switches suffer from isolation due to the limited reactance. Frequency band of operation of the designed switch is from DC to beyond X-band. Measured insertion loss of the structure is less than 0.2 dB, return loss is better than 30 dB, and isolation is better than 20 dB up to 20 GHz. Isolation is greater than 25 dB below 10 GHz. Hence, for wideband applications, this switch offers very low loss and high isolation.

Time domain measurement is necessary for the investigation of the dynamic behavior of the devices, determination of the 'pull in' and 'pull out' voltages of the

membranes, switching time and power handling of the devices. Also, failure and degradation of the switches can be monitored using the time domain setup. For these purposes a time domain setup is constructed. Moreover, failure mechanisms of the RF MEMS devices are investigated and a power electronic circuitry is constructed for the biasing of RF MEMS switches. Advantage of the biasing circuitry over the direct DC biasing is the multi-shape, high voltage output waveform capability. Lifetimes of the RF MEMS devices are investigated under different bias configurations. Finally, for measurement of complicated RF MEMS structures composed of large number of switches, a bias waveform distribution network is constructed where conventional systems are not adequate because of the high voltage levels. By this way, the necessary instrumentation is completed for controlling a large scale RF MEMS system.

Keywords: RF MEMS, metal-to-metal contact switch, EM modeling, mechanical modeling, switching time setup, power handling, reliability, biasing, distribution network, power electronics, actuation waveforms.

ÖZ

RF MEMS ANAHTAR TASARIMI VE ÜRETİMİ VE PERFORMANS DEĞERLENDİRME SİSTEMİ

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Bu tezde metal metal kontaklı anahtarların RF ve mekanik tasarımları anlatılmıştır. Metal metal kontaklı anahtarlar, kapasitif anahtarların sınırlı reaktans göstermesinden dolayı, özellikle düşük frekanslı uygulamalarda tercih edilmektedir. Tasarlanan anahtar için çalışma bandı DC'den başlayarak X-bandı içermektedir. Üretilen yapılarda 20 GHz'e kadar ölçülen araya sokma kaybı 0.2 dB'den daha düşük, dönüş yitimi 30 dB'den yüksek ve yalıtım 20 dB'den yüksek olarak ölçülmüştür. Aynı yapı için 10 GHz'e kadar yalıtım 25 dB'den yüksek olarak ölçülmüştür. Bu tip anahtarlar, geniş bantlı uygulamalarda, düşük araya sokma kaybı ve yüksek yalıtım sağlamaktadır.

Yapının dinamik analizinin yapılabilmesi, hareketlendirme ve geri bırakma potansiyellerinin ölçümü, anahtarlama süresi ve RF yük kaldırımı değerlerinin

ölçümü için zamana bağlı ölçümlerinin yapılması gereklidir. Bununla birlikte, ölçülen elemanlardaki aksama ve bozulmalar, zamana bağlı olarak ayırt edilebilmektedir. Bu nedenle, zamana bağlı değişikliklerin izlenebileceği bir donanım üretilmiştir. Ayrıca RF MEMS yapıların bozulma nedenleri incelenerek, hareketlendirme dalgalarının oluşturulması için bir güç elektroniği devresi tasarlanıp üretilmiştir. Üretilen güç elektroniği devresiyle, anahtarlar doğrudan DC beslenmek yerine, değişken dalgalı, tek veya çift kutuplu ve çok seviyeli dalgalarla beslenebilecektir. RF MEMS yapıların yaşam süresi, farklı hareketlendirme dalgaları altında ölçülmüştür.

Bu tezde son olarak, üretilen anahtarların karmaşık sistemlerde kullanılmasına olanak sağlamak ya da bu devrelerin üretim sonrası ölçümlerini gerçekleştirebilmek için kontrol devresi geliştirilmiştir. RF MEMS devre elemanlarının hareketlendirilmesi yüksek gerilimli dalgalarla sağlanmaktadır. Yüksek gerilimli dalgaların kontrol ve dağıtımı için düşük gerilimlerde kullanılan devre elemanları yeterli olmamaktadır. Dağıtım kartı anahtarların açılıp kapanmasını, gereksinimlere göre kontrol edecek şekilde tasarlanmıştır. Böylece, büyük ölçekli RF MEMS sistemlerin kontrolü mümkün olacaktır.

Anahtar sözcükler: RF MEMS, metal metal kontaklı anahtar, elektromanyetik modelleme, mekanik modelleme, dinamik analiz donanımı, RF yük kaldırımı, güvenilirlik, hareketlendirme, dağıtım devresi, güç elektroniği, hareketlendirme dalgaları.

To My Mother and
My Father

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CHAPTER 1

INTRODUCTION

Micro Electro Mechanical Systems (MEMS) has emerged in the 70's with sensors and actuators. According to the available process techniques, accelerometers, gyroscopes and pressure sensors are developed using surface and bulk micromachining techniques. MEMS systems use the mechanical movement of the devices and alter the electrical performance. Hence, electrical and mechanical functionality is combined on the same device.

The RF Micro Electro Mechanical Systems (RF MEMS) has emerged in 90's and demonstrated superior RF performance [1]-[11]. Due to its low insertion loss, high isolation, low intermodulation distortion (IMD) combined with low power consumption, RF MEMS devices are promising candidates for the low cost and high performance systems. In the initial designs, polysilicon is used for the structures and results in higher losses. By introducing metallic membranes to the device, lower insertion loss can be obtained.

As in the case of a MEMS device, operation of the RF MEMS devices rely on the movement of a membrane placed on a transmission line. With the movement of the membrane, impedance of the transmission line varies and hence electrical performance of the line is tuned with the mechanical movement of the membrane. In ideal case, one of the states corresponds to total reflection of the transmitted signal and in other state; signal can be transmitted without any disturbance.

There are problematic issues, related to the reliability of the RF MEMS devices. Several researchers are exploring the reasons behind the degradation; however failure mechanisms are not totally clarified and need considerable amount of work. Packaging and integration are among the other contemporary research topics.

1.1. RF MEMS Switch

RF MEMS switches can be used in the high frequency applications due to the low loss and high isolation characteristics of the devices [1]-[11]. A typical device consists of a transmission line for the transmission of the signal and a movable electrode placed on top of the transmission line section. A common substrate is used for the fabrication of the devices, like high resistivity silicon, quartz, glass or GaAs. Coplanar waveguides or microstrip lines are utilized for the transmission medium. Different actuation mechanisms are used for actuating the membrane. Electrostatic actuation is widely used due to the ease of integration with the RF devices and it is the most mature one among the other actuation mechanisms. Thermal, piezoelectric and magnetostatic type of actuation mechanisms are also present in the literature.

Type of the switches can be divided into two subgroups according to the behavior of the switching mechanism. An ideal series switch, as the name implies, is placed between the input and output terminals and transmits the signal in the 'down' state of the switch and isolates the terminals in the 'up' state by disconnecting the terminals from each other. Shunt switches are placed between the ground terminal and signal line connecting the two ports. In the 'down' state of the switch both terminals are shorted to the ground and switch isolates the ports. In the 'up' state of the switch, ports are directly connected to each other and signal transmission is enabled. Performance of the switch is restricted by the parasitic elements and devices can operate in a limited frequency band.

RF MEMS switches can be divided into two subgroups according to the type of their contact formation. For the capacitive type RF MEMS switches, contact is formed by means of variable capacitance between transmission lines. Hence, by varying the capacitance between the lines, effective impedance is changed. For an ideal short circuit, high capacitance values are desired between the transmission lines. For the reverse case, capacitance should be lowered to have an open circuit. In general, for the operation of the capacitive type switches, limiting factor is the capacitance (in the order of fF) between the transmission line and the membrane in the 'down' state of the switch. Since mechanical considerations are also effective in the operation of the device, parallel plate capacitance can not exceed some practical values and leads to poor contact formation. With the increased frequencies, impedance of the capacitance decreases and forms a better contact. Therefore, capacitive types of switches are not suitable for lower frequency bands. Moreover, parasitic capacitance in the 'up' state of the switch becomes dominant with increased frequency and should be considered in the design steps.

The second subgroup is the metal-to-metal contact switches. As the name implies, contact is formed by the touching two metal lines. By forming a metal contact between the transmission lines, a short is obtained and by breaking the metal contacts an open is obtained. Limiting factors for the RF performance of the switches are the contact resistance of the touching materials and parasitic capacitance between the plates. In the 'down' state of the switch, a metal-to-metal contact is formed between the plates. Quality of the contact and hence the effective series resistance determines the low frequency band performance of the structure. With improved contact quality of the switch, RF performance also improves. Hence, for the lower frequency band contact resistance should be optimized. With proper contacts, switch is capable of operating in a wide frequency band. A limitation comes from the 'up' state capacitance of the switch. Due to the mechanical considerations, contacting plates are separated by a finite distance from each other and hence, parasitic capacitance is introduced between the two plates. With the increased frequency, parasitic

capacitance between the lines reduces the impedance and degrades the isolation. Therefore, ideal open is transformed to finite impedance and can not isolate the transmission lines. In general, metal-to-metal contact switches are used in the applications requiring wideband operation and at low frequency bands. Details of the RF MEMS switches are given in Chapter 2.

The major advantages of the RF MEMS switches over the other competitors in the market can be expressed as:

- ***Low power consumption:*** RF MEMS devices consume no DC power and only power loss comes during the switching of the device. Hence systems constructed using RF MEMS device are applicable to the portable systems and satellite applications.

- ***Low insertion loss:*** Insertion loss introduced by the switch comes from the substrate loss and metallic losses. With the use of high conductivity materials and low tangent loss substrates, insertion loss of a switch can be much lower than the semiconductor rivals. With reduced losses in the system some of the amplifying stages can be removed, which leads to reduced power consumption. PIN diodes offers the nearly same insertion loss characteristic, however power consumption of the diodes are high compared to the MEMS devices.

- ***High isolation:*** Reduced parasitic capacitances results in high isolation for the 'off' switches. Also, 'on' switches provide low impedance to ground and provide high isolation. Hence, there is no need to pi or tee designs to enhance the isolation of the switches, reducing the complexity of the designs. Especially, metal-to-metal switches provide high isolation in the low frequency bands and capacitive type switches offer high isolation in higher frequency bands.

- ***Low IMD:*** Switch is constructed using mechanical movement of membranes on substrate. Hence, intermodulation distortion products are very small compared to semiconductor switches, which results in linear operation of devices.

- ***Low cost:*** RF MEMS devices are fabricated using surface micromachining process and can be built on low cost glass or high resistivity silicon substrates.

RF MEMS have superior RF performance and ideally zero power consumption, however suffer from the mechanical and fabrication related issues:

- ***Low switching speed:*** Since switching action relies on the mechanical movement of the membrane, switching speed is determined by the mechanical properties of the material and mechanical design. Switching speed of a RF MEMS device is in the order of microseconds. For a semiconductor device, switching speed is in the order of nanoseconds. RF MEMS switches cannot be used in the applications requiring high switching speeds.

- ***Packaging:*** For the reliable operation, RF MEMS devices require controlled environment and needs hermetic packaging. Hermetic seals are expensive and long-term reliability is not explored. In addition, package can alter the behavior of the switch.

- ***Reliability:*** Most of the devices stated in the literature is a prototype and can not become a commercial product because of the limited lifetime of the devices. Capacitive contact devices suffer from the dielectric degradation and metal-to-metal contact switches degrades due to wear out of contact

materials. For a reliable operation, successful operation of the devices should be verified from 1 to 10 years for switching cycle exceeding 10 billions.

- ***Power handling:*** Power handling of the MEMS devices is several watts and for increased lifetime, input power should be reduced. For moderate power levels, RF properties of the RF MEMS devices are better than PIN diodes and FET switches, however for the higher power levels, MEMS devices are not operational and can not be used for high power applications.

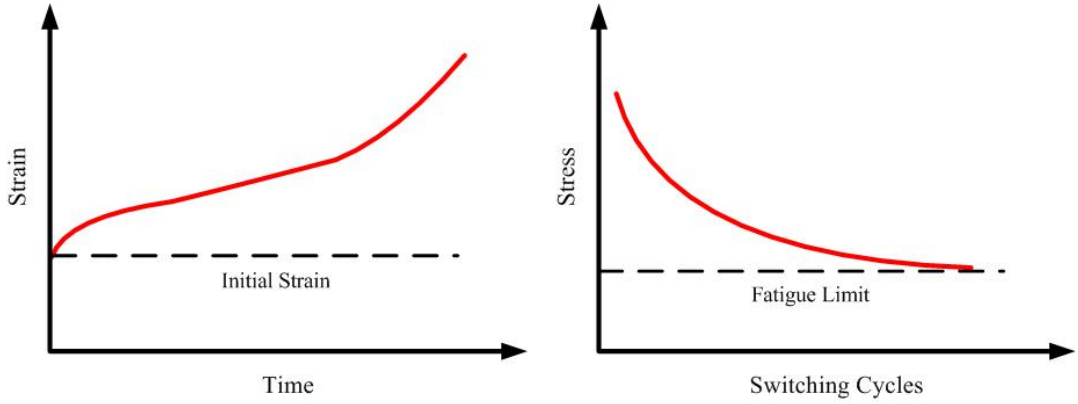
- ***High actuation voltage:*** Due to the RF requirements of the switch like increased isolation, 2 to 4 μm gaps are designed. For the electrostatic actuation, 20 to 80 V need to be applied to the switch due to small forces between the electrodes and hence actuation voltage increases. Such a high voltage level is not present in a semiconductor-based system and separate actuators are needed.

1.2. Lifetime of RF MEMS Devices

There is variety of RF MEMS designs in the literature, however only limited number of commercially available device has been announced [12]-[14]. The major reason behind low number of commercial devices is the short lifetime of the RF MEMS devices. Several research groups are investigating the lifetime and the failure modes affecting the lifetime of the devices [16]-[21]. Some commercially available products rise in the market however; methods underlying a reliable operation are not published yet.

For the investigation of the lifetime of the RF MEMS device, one has to identify the reasons behind the failure. Several possible modes affecting the lifetime of the MEMS devices can be stated as:

- ***Creep and Fatigue:*** Creep is the mechanical deformation that continues to increase under the same applied force. Hence, material deforms to relieve stress applied on it. Creep is observed in metallic membranes and higher melting point materials or compounds should be selected for reducing creep on membranes. Also heating due to RF power can increase the effect of creep on the membranes. Figure 1-1 (a) shows a typical creep graph of a material.



(a) (b)

Figure 1-1: Material deformation on structural layer (a) typical creep graph, and (b) typical fatigue graph.

Fatigue is the progressive structural damage due to the repeated stress on the membrane. Figure 1-1 (b) shows a typical fatigue graph of a material. Investigation on some specific materials reveals that fatigue is reduced in the micro scale structure than its macro scale counterparts.

- ***Stiction:*** Observed in the process steps and during the operation of devices. Stiction, in fabrication is observed in the release step of the process and is out of scope of this thesis. With increased surface interaction energy between the

contacting surfaces, restoring spring forces are not sufficient to overcome the surface interaction forces and stiction is observed. Dominant modes constituting the surface interaction energies are capillary condensation, Van der Waals forces, hydrogen bridging and solid bridging. Capillary forces are most dominant in the humid environments and humidity should be removed for increased lifetimes. Figure 1-2 presents the stiction of the cantilever type membrane.

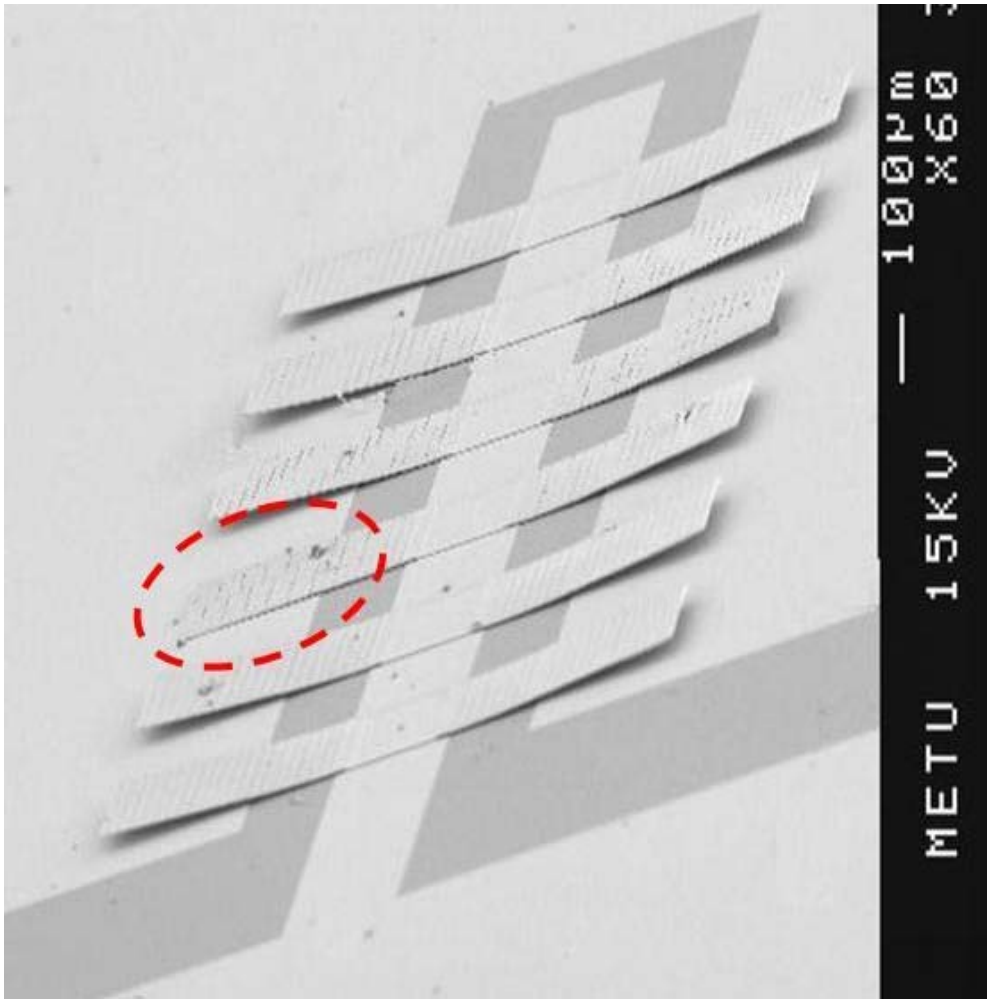


Figure 1-2: Stiction of the cantilever type bridge.

- ***Contamination:*** For the reliable operation of the MEMS devices, controlled environment is necessary. Residues coming from the process or environment can degrade the contact of the bridges. Moreover, controlled humidity is required. Hence hermetic or near hermetic packages filled with inert gases should be used. Figure 1-3 presents process related residues under the bridge results in possible failure of the switch.

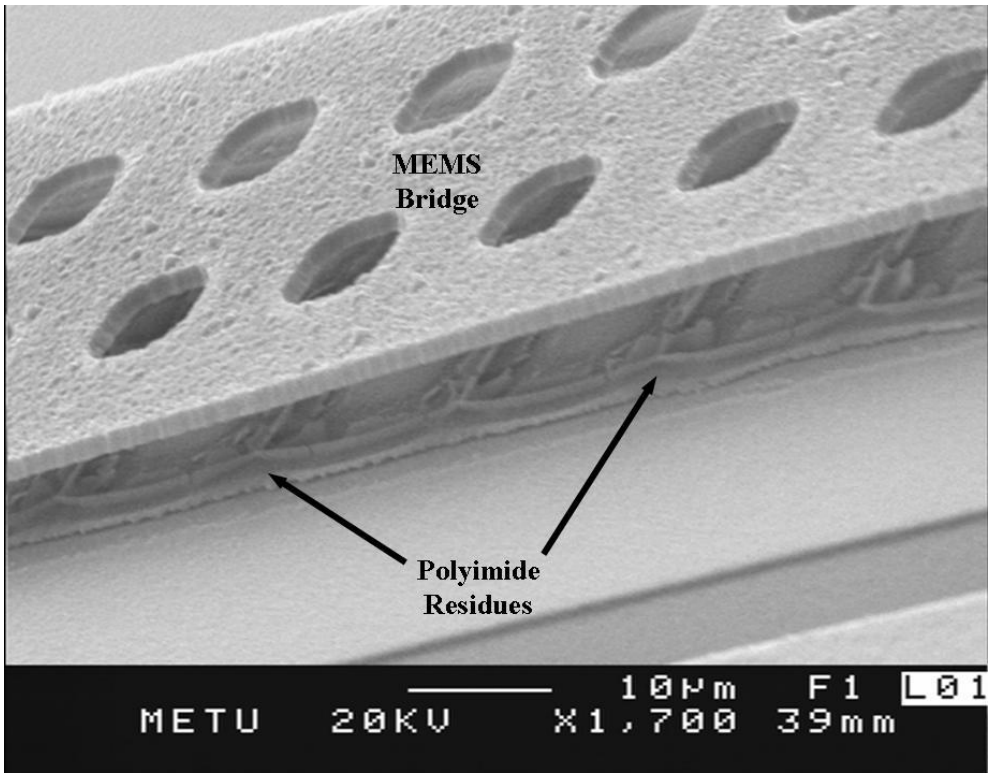


Figure 1-3: Residues under the bridge, coming from the fabrication.

- ***Dielectric charging:*** Charging is observed in the isolation layers of the RF MEMS switches. Due to increased stressing levels of the dielectric layers, trapped charges induce attraction between the actuation plates and 'pull in' or 'pull out' voltages can drift from the original values. Hence, stiction related to the charging or increase in the actuation voltage can be observed.

In the lifetime of the RF MEMS devices dielectric charging plays an important role. With the increased number of charge trapped behavior of the device shifts from the ideal situation leading to a degradation or even total failure of the switch. Figure 1-4 illustrates the dielectric charging mechanism in the isolation layer of the MEMS device.

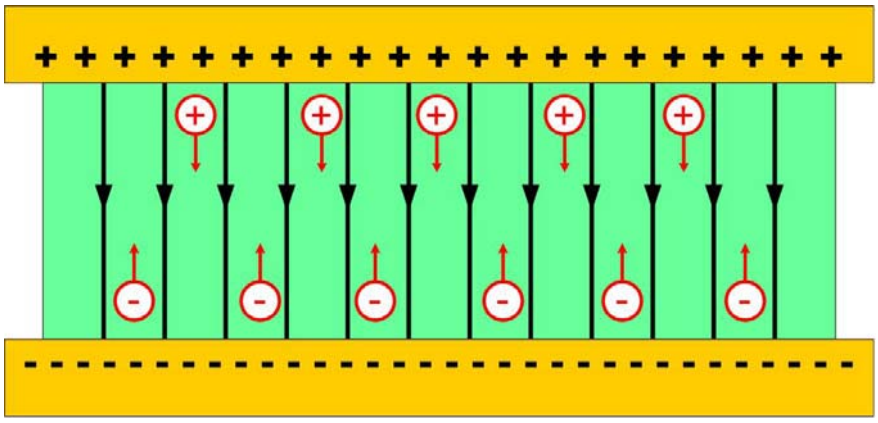


Figure 1-4: Charging of the dielectric due to applied electrical stress.

Charging is studied by other researchers and an equation relating the applied stress, total trap density of material and trapped charge density in time is presented [16]. Hence, parasitic charge trapped on dielectric layers can be modeled as a function of applied stress and material properties. Equation given by Zafar [16] is mathematically modeled by Van Spengen [17]. According to the solution of given mathematical model, charging can be modeled as a charging capacitor. With increased charging rates, lifetimes of the devices are very limited. According to the model, lifetime mostly depends on the applied stressing time and not to the frequency of the biasing. Hence, device can operate for a specified period independent of the frequency of the switching. Injection rate is determined by the material properties and applied electrical stress on the materials. According to

Goldsmith [21], applied electrical stress strongly affects the lifetime of the devices and for a 5 to 7 volts of reduced bias voltages lifetime improves about a decade.

According to model presented in [17], a possible improvement method based on actuation voltage waveform is proposed in this thesis and a custom circuit is designed and fabricated to generate the specific waveform for the improvement of the lifetime of MEMS devices. Idea is based on the charging and discharging of the capacitance that stores the parasitic charges and obtain a neutral parasitic charge distribution along the dielectric layer. Also for further improving the lifetime of the MEMS devices, applied voltages are reduced according to studies of Goldsmith and lifetime of the devices according to the applied bias waveforms are measured.

Biasing equipment is proposed for the generation of special wave shapes. Wave shape generation circuit utilizes the power electronic circuitry for the generation of high voltage and high-speed waveforms and used for the actuation of the RF MEMS devices. Some of the equipments used in constructing the circuitry is:

- ***Power MOSFET:*** Power MOSFET is similar to the conventional MOSFET; however, it can withstand increased voltage and current levels. In general, it is used for routing the power to load. Power MOSFET enables switching with higher speeds than ordinary power switches. High speed is required due to the mechanical response time of the MEMS devices. With lower switching speeds, the RF MEMS switch can respond to the variations in the applied actuation voltage and modulate the RF power in an undesired manner.

- ***Gate driver:*** Gate drivers are used for controlling the switching of the power MOSFET. Since high voltages present in the system, logic controls cannot turn on and off the power switches. Gate drivers perform a translation between the logic circuits and power circuits. It amplifies the incoming message signal to a power signal, sufficient to operate the power circuit.

Different topologies exist for the construction of the gate driver and pros and cons for each topology. Two different gate drivers are used in conjunction in order to get desired performance in final design.

- ***Inverter:*** Inverter is a power converter and used for converting DC power to AC power. Inverter is similar to the CMOS inverters in the logic design and used for the shaping output signal. According to the control mechanisms square wave or sinusoidal like waveforms can be obtained at the output.

- ***Bridge:*** Constructed using one or more inverters. With the use of bridges, neutral point to load can be provided to load. With multilevel bridge inverter design, amplitude switching multi shape output can be generated according to the logic circuitries.

- ***Snubber:*** Snubbers are used for reducing the electrical stress on the components. Design is carried according to functionality, cost and design complexity of the circuit.

Different bias waveforms are generated using the waveform generating circuitry and effects of biasing on the lifetime of the devices are observed. Since RF MEMS switches are used as individual parts of the design or part of other components, failure and degradation should be inspected carefully for the reliability of the system.

1.3. System Integration

For the integration of MEMS switches into the part of other components, control of the system becomes complicated due to the increased combination of the switches. Aim of the RF MEMS design is not focused on a single switch. With the use of several switches, designs that are more complicated are projected. Hence, with the

increased number of switches control of the devices becomes complicated. Since every component in the systems performs different tasks, control of the elements should be separated from each other. However, controlling so many devices at the same time can be difficult due to the applied high voltage bias waveforms. Conventional circuits cannot be used for the routing actuation waveforms due to the increased voltage levels and hence design of a custom circuit is necessary. With the increased combination of the switch states, measurements of the devices are also tedious and can be carried by use of an automated measurement setup.

In order to use the same configuration in different type of system requirements and structures, circuit should be able to adopt itself to variations in the RF MEMS product.

1.4. Research Objectives and Organization of Thesis

The main objectives of this thesis are to design and fabricate a metal-to-metal contact switch and characterize the lifetime of the MEMS devices. Furthermore, investigating the dielectric failure and improving the lifetime of the devices with custom wave shapes are intended. Also for the characterization of the devices in the system level, an automated measurement setup is introduced.

The specific objectives in the frame of this thesis can be summarized as:

- ***Metal-to-metal contact RF MEMS switch design:*** Metal contact switches offers excellent characteristic in a broad band and hence utilization of this type of switches in the design can improve the overall performance. Low loss and high isolation can be achieved with the use of the metal contact switch.

Moreover, mechanical properties should be investigated and designed to operate in quick and reliable manner. Also for understanding and improving the switch, RF performance should be modeled and investigated for possible improvements.

- ***Fabrication:*** Most important part of the thesis is to obtain a reliable, high performance product. Hence, fabrication of the devices plays an important role in the design of the devices. Therefore, process cycle and development is important for the products.

- ***Lifetime improvements:*** A commercial product should perform at least billion cycles before the failure and this number can be increased according to the requirements of the application. Hence, lifetime of the MEMS devices should be investigated carefully. Failure modes affecting the devices should be investigated and possible enhancements established.

- ***Measurement and operation of system:*** For the integrated systems, manual control is not fast and accurate. Hence, an automated measurement is required. Moreover, during the operation of the system, it should manipulate the required operations automatically. Hence, an integrated system with the MEMS product is necessary.

This thesis includes the accomplishments up to date according to the stated objectives in six chapters.

Introduction chapter is followed by the Chapter 2 and explains the design and modeling of the RF MEMS devices. RF design parameters and mechanical design are given. RF measurements with the time domain switching results are also covered in this chapter.

Chapter 3 presents the fabrication process used for the manufacturing the switches.

Chapter 4 focuses on the lifetime and reliability of the devices. Failure modes and related degradation is explained. A custom wave shape generator circuit for the biasing MEMS devices is presented.

Chapter 5 presents an automated measurement setup for the measurement and operation of systems composed of increased number of switches.

Chapter 6 concludes the thesis with a discussion on the future work requiring further research.

CHAPTER 2

DESIGN AND MODELING OF METAL-TO-METAL CONTACT RF MEMS SWITCH

RF MEMS switches are used for microwave signal routing in communication systems, antennas, front-end transreceive systems, phase shifters, tunable filters, and switching networks. RF MEMS have the advantages of wideband operation, low power consumption, cost efficiency, and superior RF characteristics like low insertion loss, low intermodulation products, and high isolation. Possible competitors in the market are PIN diodes and FET switches. PIN diodes also offer low insertion loss; however suffer from difficult integration, complicated biasing circuitry and high power consumption, which causes problems in the system integration due to increased power dissipation and complexity of designs. On the other hand, for the FET devices, system level integration is simpler due to straightforward biasing circuit and lower power consumption; however, it introduces high insertion loss at microwave frequencies, hence requires amplifying sections after switching.

There are two basic types of the RF MEMS switches, which are metal-to-metal contact and capacitive contact switches. Both types operate based on the same principle. Switch acts like an open or short circuit for isolating and transmission line for transmitting the signal. Each type of switch either reflects or transmits the incoming signal due to low loss nature of the RF MEMS structures.

This chapter focuses on the metal-to-metal contact switches. Section 2.1 explains the basics of the RF MEMS and Section 2.2 covers the RF design of the metal-to-metal contact RF MEMS switch. Section 2.3 presents the mechanical modeling of

switches. Then, switching time modeling and comparisons with the simulations will be presented. Finally, Section 2.5 covers, power handling and switching time tests.

2.1. Description of RF MEMS Switch

An RF MEMS switch is composed of a transmission line and a mechanically movable system used for the routing of RF signals. CPW or microstrip lines can be used for transmission line. Mechanically movable system forms a connection between the input and output terminals or connects both ports to ground or open circuited. Hence, signal is transmitted or reflected over the mechanical movable part.

The mechanical membrane of RF MEMS switches are composed of two main structures, which are the movable plate and an actuation electrode. Figure 2-1 depicts the general structure of a RF MEMS switch. Idea of switching is based on mechanical movement of the micromachined cantilever or fixed-fixed beam structures with the help of electrostatic, thermal, magnetostatic or piezoelectric forces acting on the movable plate. With altering the position of movable plate, separation between membrane and signal line is changed, hence variation in the performance is obtained.

With the ‘up’ and ‘down’ movement of the switch, capacitive or metallic contact is formed between the input and output ports according to desired specifications. For the parallel capacitive contact type switches, switching is carried by means of altering the effective capacitance between the signal and transmission line. In the ‘up’ state of the switch signal is transmitted to the output port, where in ‘down’ state due to increased capacitive coupling signal is reflected back in a certain frequency band. In a series switch, signal transmission is interrupted by a slot in the signal line. For the transmission of the signal, membrane forms capacitive coupling between the input and output signal line. Performance of capacitive contact switches is limited

by the mechanical properties of the membrane, since capacitances about tens of pF can be achieved due to increased size of the switches. Hence, this type of switch is suitable for high frequency operation.

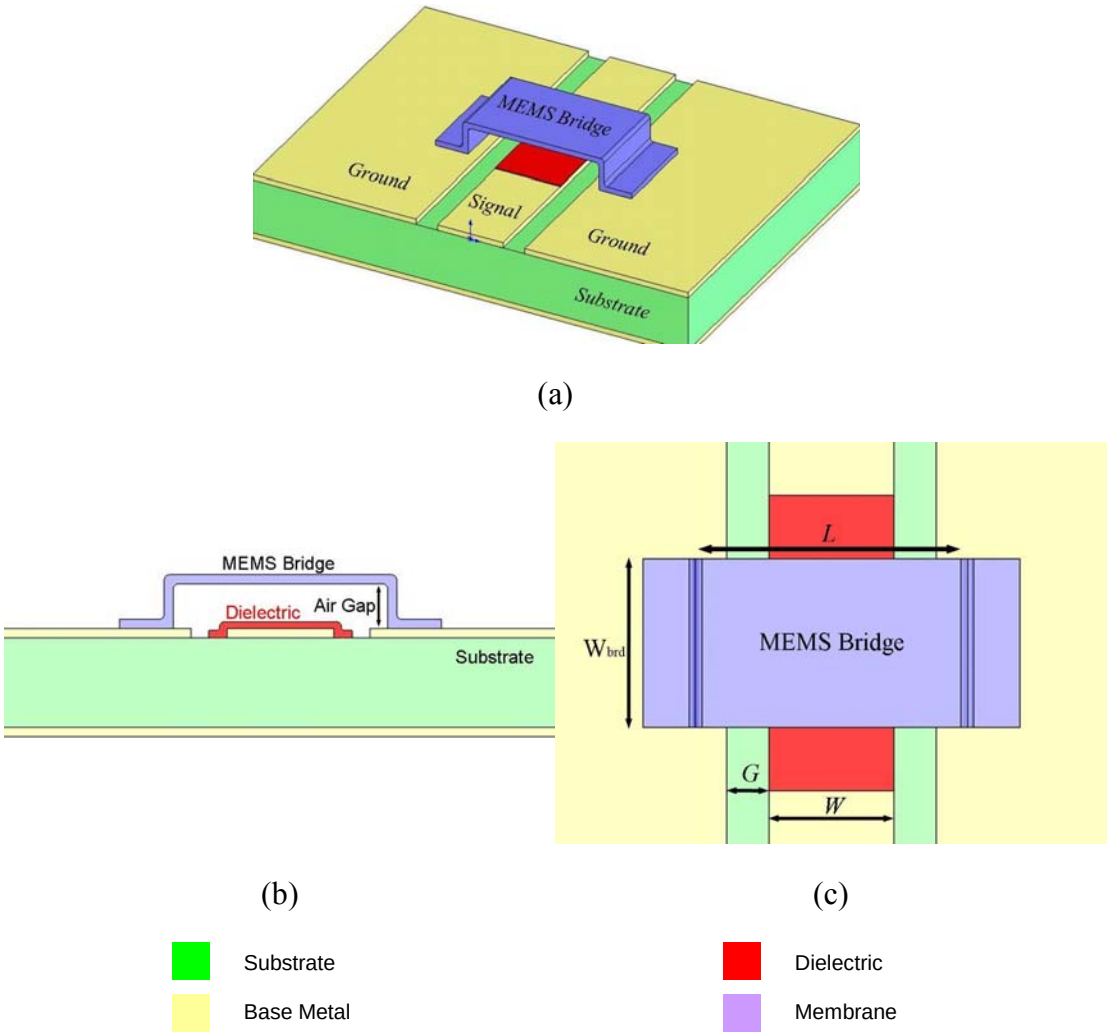


Figure 2-1: MEMS structural view. (a) Isometric view of MEMS switch, (b) side view, and (c) top view.

For the metal-to-metal contact switches, switching is performed by the metallic contact of the transmission lines and the bridge. Parallel switch transmits the signal in the 'up' state of the membrane and reflects the signal in the 'down' state of the membrane. Membrane is placed perpendicular to the transmission line and for the 'up' state signal can be transmitted without any disturbance. In the 'down' state of the switch membrane forms short circuit between the signal and ground planes, therefore signal reflects back. Series switch operates very similar to the capacitive contact case. Signal line is interrupted by a slot in the signal line for the 'up' state of the membrane, hence signal reflects back from the open circuited line. In order to transmit signal membrane forms a connection over the cut in the signal line. This connection is maintained by metal-to-metal contacts, when membrane touches the signal line. Contacts are formed between the metal signal lines and membrane portions, and hence signal can be transmitted over the membrane. In the metal-to-metal contact type switches insertion loss is mainly determined by the quality of the contact formation and good quality contacts offers wideband operation. Limitation generally comes from the overlap between the signal line and membrane in 'up' state, since capacitive coupling between the plates causes reduced isolation with increase in frequency.

Independent of the switch type, each switch needs to be actuated; the most common actuation mechanism is electrostatic actuation due to the ease of fabrication steps, low power requirement and reduced complexity of the designs. All of the designs, covered in this thesis, are based on the electrostatic actuation. Electrostatically actuated switches consist of an actuation electrode and a movable plate. In general, for the actuation of the movable plate, actuation electrode is placed underneath. In addition, some designs in literature contain more than one electrode for mechanical stability, power handling and improved rise and fall times of the membrane [15]. For the capacitive contact designs, signal line can be used as an actuation electrode, however for the metal-to-metal contact switches this is not the usual way, since

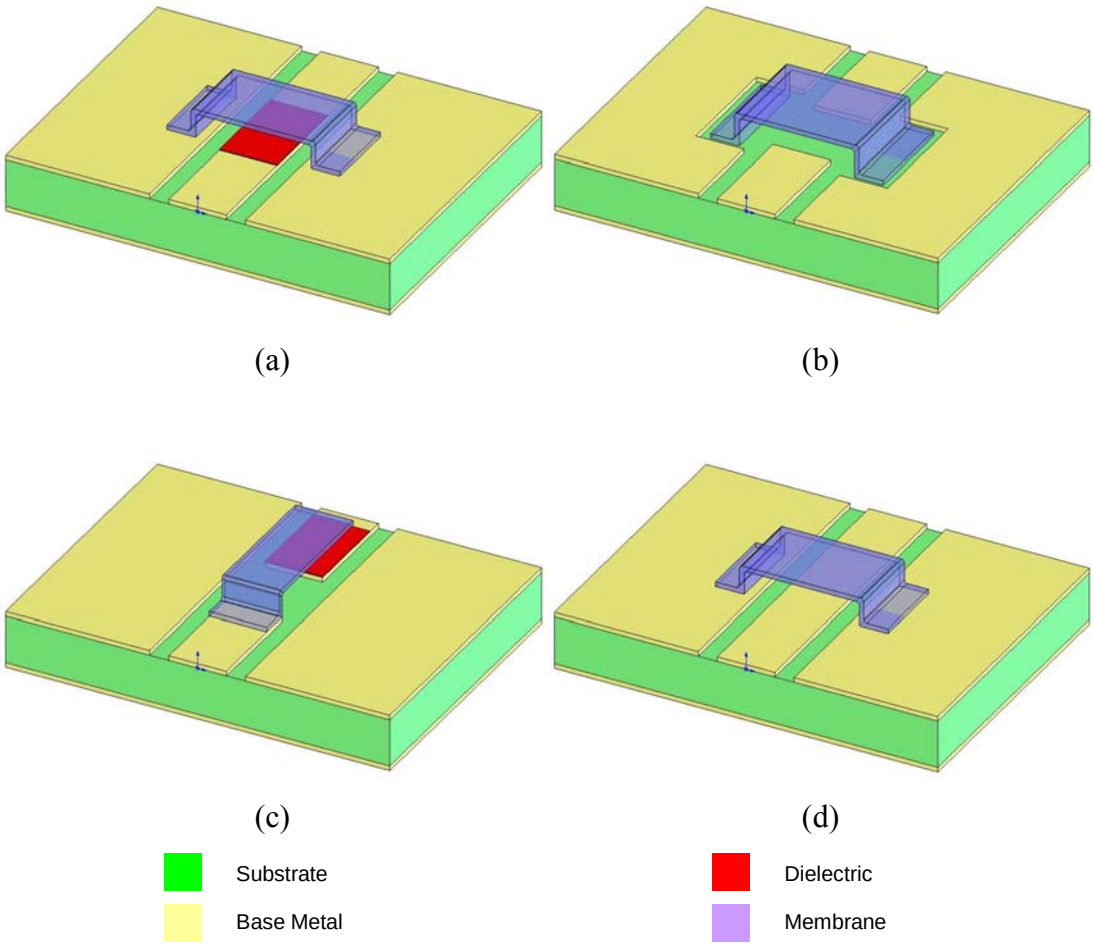


Figure 2-2: Different RF MEMS switch types. (a) Shunt capacitive switch, (b) Series metal-to-metal contact switch, (c) Inline capacitive switch, and (d) Shunt metal-to-metal contact switch.

potential difference between the plates will lead to possible deformations on the contact points or even worse welding of the metal plates to each other. This problem can be solved by introducing separate actuation plates and isolating from both lines. Same procedure can also be applied to capacitive contact types. Separate actuation plates in capacitive contact designs used for the reduced actuation voltages due to larger pad area. This reduces the coupling between signal and ground planes with

decreased metallization and increased power handling because of smaller signal and membrane interaction.

Using cantilever or fixed-fixed beams is the most common way to implement a movable membrane. Mechanical support of the membranes is formed by the anchors connecting the beams to rigid bodies. According to placement of the anchor point membrane is designated as cantilever or fixed-fixed. Cantilever type of membrane is supported from the single edge. Other ends are free to move and maximum vertical displacement occurs in opposite tip of the anchor. For fixed-fixed beams, membrane is supported from two opposite edge and remaining edges are free to move. Deflection is at its maximum in the middle of anchors and hence midpoint is suitable for the analog tuning of capacitance because of increased tuning range.

Typical values for switch geometry are 300-500 μm of bridge length and 40-120 μm bridge width. According to process conditions, bridge height can be between 1-4μm. Actuation electrodes are placed at least 100 μm away from the anchor points of the cantilever switches. For the fixed-fixed beam designs, electrodes are longer than 200 μm. Membrane thickness is 1-2 μm according to materials used and desired mechanical properties of the switch. Dielectric layer with permittivity ε_r of 5-7 and thickness of 100-300 nm is used for capacitance formation and DC isolation layer. Usual actuation voltages are around 10-80 V due to constrains in the mechanical designs and lifetime limitations for the switches [44].

2.2. Circuit Modeling of Series Switches

Series switch covered in this chapter is composed of two transmission lines in the input and output ports and an 80 μm length slot separates two signal lines. Ground planes are connected to each other. On top of the slot, fixed-fixed membrane is placed. In addition, actuation electrode is placed on the slot underneath the

membrane. Nitride layer covers the actuation electrode, in order to prevent possible short circuits. With this topology, compact designs can be implemented. Anchors placed to the recesses in the ground plane in order to reduce the coupling between the signal and ground planes. Input and output transmission lines are selected as 22μm /176μm /22μm for better input and output matching since resulting system yields port impedance of 50 Ω as calculated in Section 2.2.1. Figure 2-3 shows picture of fabricated metal-to-metal contact series switch.

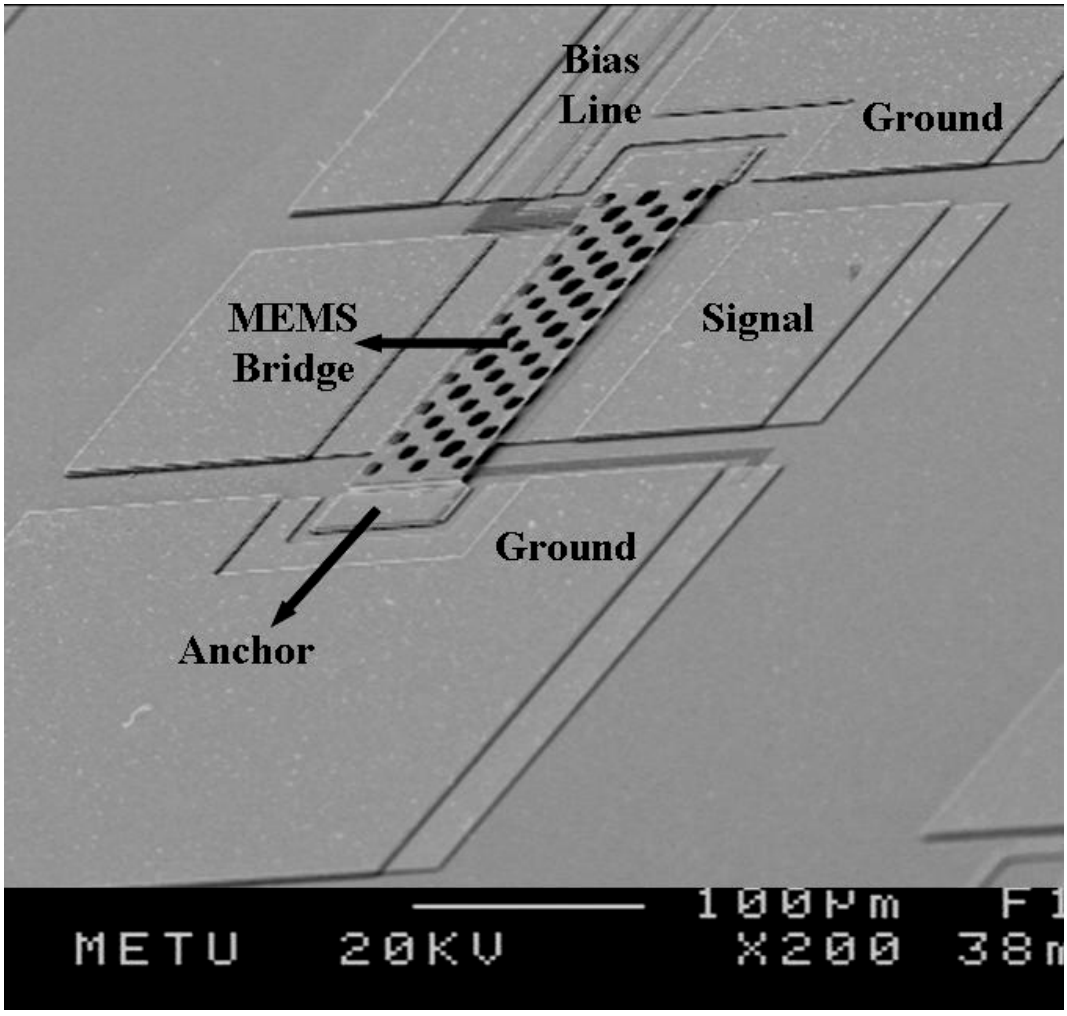


Figure 2-3: SEM picture of the series metal-to-metal contact switch, showing bridge, anchor and transmission line sections.

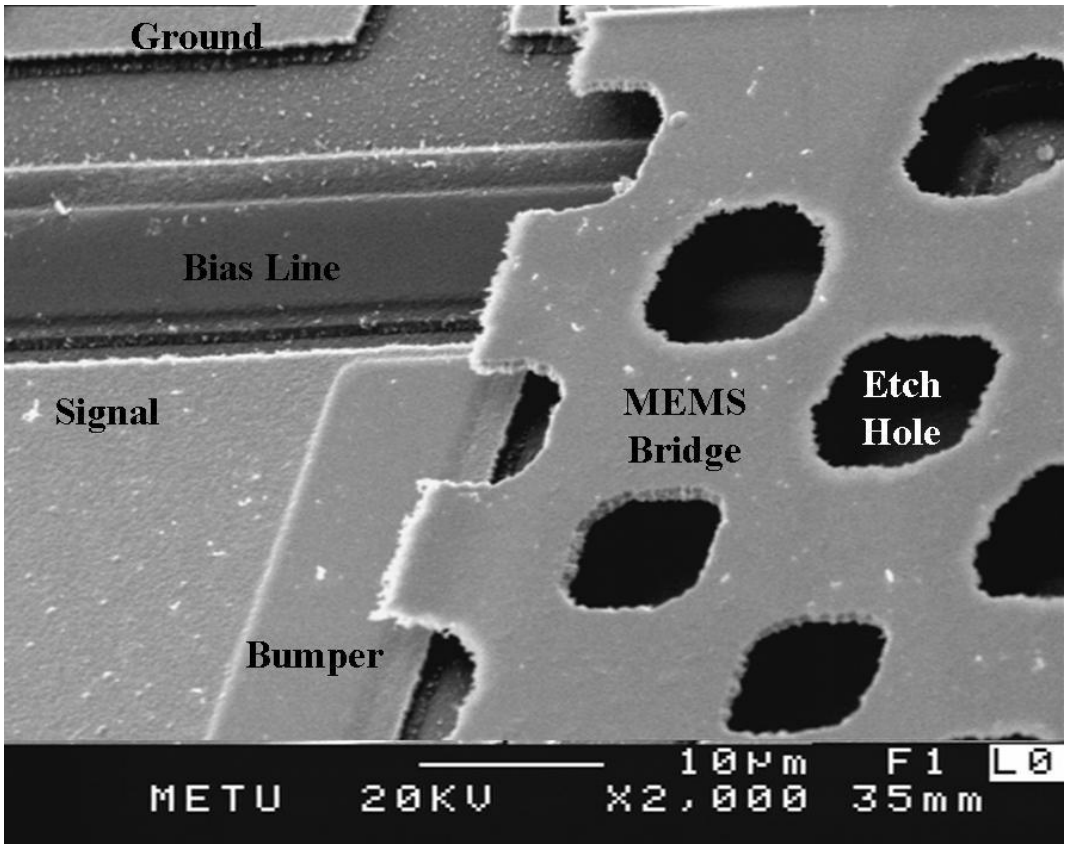


Figure 2-4: A closer SEM picture of the switch showing contact area of the switch. Bias line is covered with dielectric and a bumper is formed for better contacts.

Down state of the series switch can be modeled by three sections of transmission lines. Two short section of transmission line represents the input and output lines of switch. Membrane part is modeled by another short transmission line section. Contact points are modeled as a series resistance due to the DC contact resistance. Additional shunt resistance is added for the representation of the bias resistance.

Up state of the switch is fundamentally very similar to the model given in the down state. Contacts are modeled as a capacitance due to the parallel plate capacitance between the signal and the bridge plates. Only additional component for the modeling upstate situation is the coupling between the input output lines over the

actuation electrode, whose effects are suppressed in the down state by the membrane. Effect of the coupling is shown by a series capacitance and resistance pair.

Parameters used for the modeling are based on physical structure of the switch. Capacitance value can be found from the parallel plate capacitance formulation adding the fringing fields. Resistance values can be calculated from the physical dimension of the bias resistance. However, for simplicity, parasitic capacitances are fitted from the measured S-parameters.

2.2.1. Coplanar Waveguide Transmission Line Design and Modeling

Transmission lines are needed for guiding the microwave signals into the RF MEMS switch. Figure 2-5 presents the side view of the CPW line and field distribution over the medium. CPW structures are easy to design and integrate with the MEMS structures. Since transmission lines constitute an important portion of the switch, care should be taken in the design of the CPW lines.

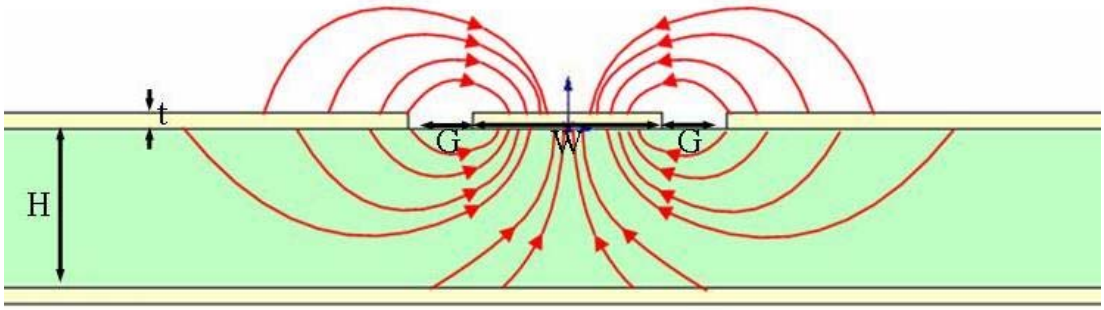


Figure 2-5: Electric field distribution of CPW and parameters used in the modeling.

According to the [22], following equations relate dimensions to the electrical properties of the CPW for a given width (*W*), gap (*G*) and thickness (*t*) of the CPW line, together with the height of the dielectric substrate (*H*):

$$k_1 = \frac{\tanh(\pi W/4H)}{\tanh[\pi(W+2G)/4H]} \tag{2-1}$$

$$k_2 = \frac{W}{W+2G} \tag{2-2}$$

$$k_i^{'} = \sqrt{1-k_i^2} \qquad i = 1,2 \tag{2-3}$$

$$q = \frac{\frac{K(k_1)}{K(k_1^{'})}}{\frac{K(k_1)}{K(k_1^{'})} + \frac{K(k_2)}{K(k_2^{'})}} \tag{2-4}$$

$$\varepsilon_{eff} = 1 + q(\varepsilon_r - 1) \tag{2-5}$$

$$Z_o = \frac{60\pi}{\sqrt{\varepsilon_{eff}}} \frac{1}{\frac{K(k_1)}{K(k_1^{'})} + \frac{K(k_2)}{K(k_2^{'})}} \tag{2-6}$$

where *K(k)* denotes the elliptic integral. Using the equations above, an equivalent impedance of 50.1 Ω is calculated for the given physical dimensions of transmission line as 22μm /176μm /22μm, which is consistent with electromagnetic simulations and measurements. These equations are verified to be used for design purposes.

2.2.2. Loss of the CPW

Substrate losses and the conductor losses constitute the total loss of the transmission line. Using the notation shown in Figure 2-5 substrate loss can be found as:

$$k_3 = \frac{\sinh(\pi W/4H)}{\sinh[\pi(W+2G)/4H]} \tag{2-7}$$

$$q' = \frac{K(k_3)}{2K(k_3')}\frac{K(k_2')}{K(k_2)} \tag{2-8}$$

$$\alpha_d = \frac{8.686\pi f}{c}\frac{\varepsilon_r}{\sqrt{\varepsilon_{eff}}}q'(\tan\delta_e) \tag{2-9}$$

where $tan\delta_e$ is the loss tangent of the dielectric.

In addition, conductor losses can be found from:

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{2-10}$$

$$R_s = \frac{1}{\delta\sigma} \tag{2-11}$$

$$R_C = \frac{R_s}{4W(1-k_2^{\,2})K^2(k_2)}\left(\pi + \ln\left(\frac{4\pi W}{t}\right) - k_2\ln\left(\frac{1+k_2}{1-k_2}\right)\right) \tag{2-12}$$

$$R_G = \frac{k_2 R_s}{4W(1-k_2^{\,2})K^2(k_2)}\left(\pi + \ln\left(\frac{4\pi W}{t}\right) - \frac{1}{k_2}\ln\left(\frac{1+k_2}{1-k_2}\right)\right) \tag{2-13}$$

$$\alpha_c = 8.686 \frac{R_C + R_G}{2Z_o} \tag{2-14}$$

Total loss can be expressed as:

$$\alpha_{tot} = \alpha_d + \alpha_c \tag{2-15}$$

Evaluating the loss formulas gives 29 dB/m conductor losses and 6 dB/m dielectric losses. Hence, total loss of the line is 35 dB/m.

2.2.3. Up-State Capacitance and Resistance

Up-state capacitance is formed by series connection of a parallel plate capacitance, between the signal and membrane plates. Combination of these capacitances determines the isolation of the switch at the high frequency band. Hence parallel plate capacitances should be considered during the mechanical design of the membrane.

Due to the actuation electrode, a parasitic capacitance forms in the shunt arm of the upstate capacitance. Value of the parasitic capacitance can be found from the fitting of the measured and modeled values.

Including the fringing field capacitances, parallel plate capacitance can be expressed as [23]:

$$C_{pp} = \varepsilon_0 \left[1.15\left(\frac{W.w}{g}\right) + 2.8.(w+W)\left(\frac{t}{g}\right)^{0.222} + 4.12.g\left(\frac{t}{g}\right)^{0.728} \right] \tag{2-16}$$

where t denotes the metallization thickness of the plates, g is the gap between the electrodes, and w and W are width and length of the overlap area . For the resistance calculation, well know formula for the resistance is used. ρ is the resistivity of the material, ℓ is the length, and A is the area.

$$R = \frac{\ell \rho}{A} \tag{2-17}$$

2.2.4. Up-State Circuit Model of the Series Switch

Figure 2-6 shows the upstate modeling of the series switch.

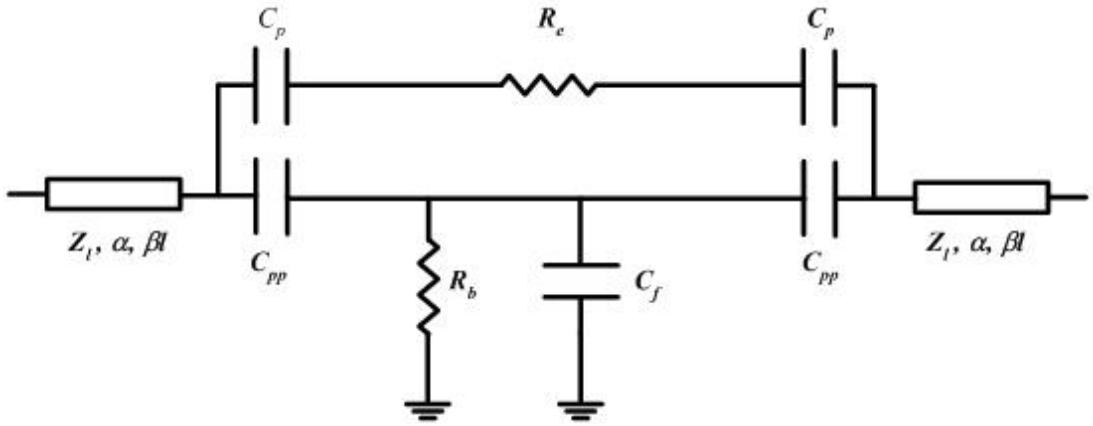


Figure 2-6: Up-state circuit modeling of the series switch.

For modeling of input and output transmission lines, short length transmission lines are introduced to circuit model. Parameters of the short length lines can be found using the transmission line formulations and the physical dimensions of the CPW lines. C_{pp} is the parallel plate capacitance between the signal line and membrane, placed after the input and output transmission lines for modeling the capacitive coupling at contact regions of the switch. Capacitance value can be found using the

formula given in Equation (2-16). For each contact region, one capacitance is inserted to the model, yielding two series connected capacitances between the input and output transmission lines. R_b stands for the bias electrode used for the DC feeding of the movable membrane. Lower bias electrode values will lead to higher RF loss on the switch and higher bias electrode values will consume chip area and cause delay on the bias line. Hence, optimization on bias electrodes, according to the specifications of the system is necessary.

For evaluation of the parasitic components, ADS Momentum is utilized. The parasitic component is a gap between two coplanar metal plates. This structure is constructed as a gap between two transmission lines and simulated using Momentum. S-parameters of the simulation is imported to the circuit simulator of ADS and compared with the results of the circuit constructed using two transmission lines and a series capacitance in between. Parameters of the transmission lines are kept same as the simulated structure. Hence, the parasitic capacitance between the transmission lines is the only unknown variable. The value of the parasitic capacitance is evaluated by comparing the Momentum simulation and circuit simulation results. On the other hand, the empirical formulations for interdigital capacitances that are constructed by separation of coplanar metal plates are also evaluated; however, they did not give the same results.

The parasitic coupling capacitance (C_p) between the signal line and actuation electrode can be found using the method provided. Moreover, center conductor of the switch is perturbed due to the bridge structure. This perturbation is modeled as a capacitance (C_f), which is evaluated again in Momentum.

Finally, the resistance of the bias electrode placed underneath the bridge is calculated from Equation (2-17). Table 2-1 gives component values evaluated using the calculation and fitting.

Table 2-1: Modeling results for the up-state of series switch. “Fitted” results are obtained by fitting to EM simulation of discrete sections.

	Z_l (Ω)	C_f (fF)	C_{pp} (fF)	C_p (fF)	R_b (kΩ)	R_e (Ω)
Calculated	50.1	-	12	-	17.76	1184
Fitted (EM simulation)	-	11.72	-	8.65	-	-

Figure 2-7 demonstrates obtained results from the circuit modeling and measurements. Moreover, full-wave electromagnetic simulation is carried in a 3D electromagnetic field simulator, HFSS 9.2 and compared with the measurements. For the measurement of the devices 40 V bipolar actuation wave is applied (for further details, see Chapter 4).

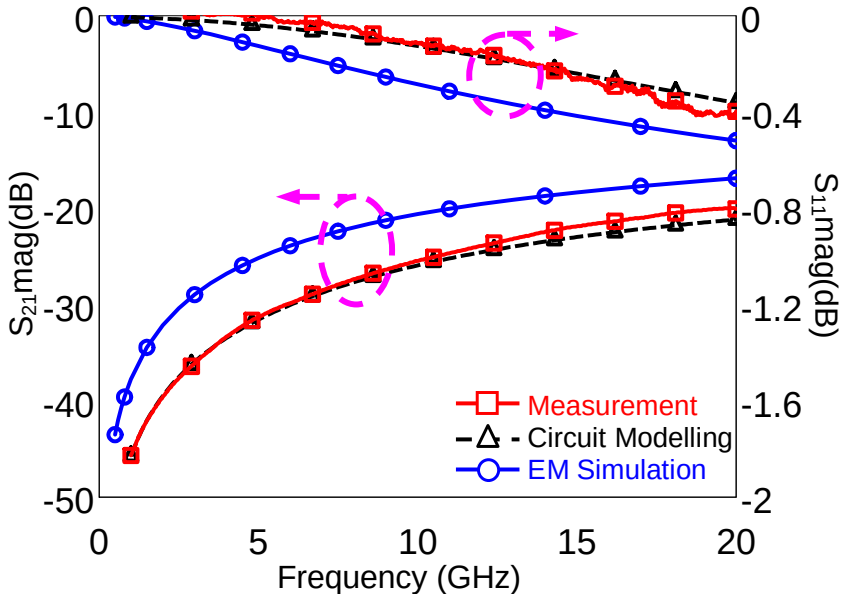


Figure 2-7: Results of up-state modeling of the series switch.

2.2.5. Down State Circuit Model of the Series Switch

Figure 2-8 demonstrates the downstate circuit modeling of the series switch with lumped components.

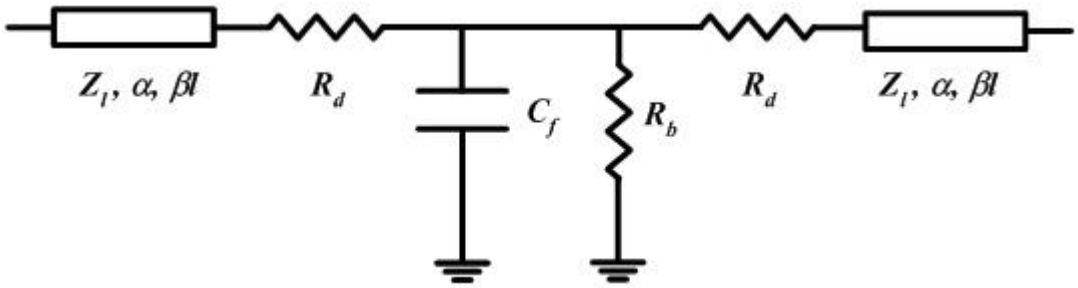


Figure 2-8: Down-state circuit modeling of the series switch.

Downstate modeling of the switch is very similar to the up state modeling of the switch. Difference between the two states is the model used for the contact. In the down state of the switch, capacitance between the membrane and the signal line does not exists, since membrane and signal lines forms a metallic contact in the down-state of the switch. Hence, capacitances are replaced by series resistances, due to the contact resistance of the metal-metal contacts. With improved contact pressure and material selection, better contact resistances can be achieved. The parasitic arm used for the modeling of the up state is ignored in downstate, since the series resistance, between the input and output ports of the switch, is much lower than the capacitive coupling between the ports, due to metal-metal contacts. Hence, in the total switch response, this parasitic arm can be totally ignored.

R_b and C_f are evaluated at the up-state modeling section. Hence, the contact resistance (R_d) is the only unknown parameter. R_d is evaluated using parameter fitting. Table 2-2 gives component values evaluated, using the calculation and fitting.

Table 2-2: Modeling results for the downstate of series switch. "Fitted" results are obtained by fitting to EM simulation of discrete sections.

	Z_l (Ω)	C_f (fF)	R_d (Ω)	R_b (kΩ)	R_e (Ω)
Calculated	50.1	-	-	17.76	1184
Fitted (EM Simulation)	-	11.72	0.33	-	-

Figure 2-9 presents obtained results from the circuit modeling, measurement, and HFSS simulation. For the measurement of the devices 40 V bipolar actuation wave is applied (for further details, see Chapter 4).

As can be seen from Figure 2-9, results of the circuit simulation and measurement are not in a good agreement. For better matching, value of C_f is reduced to the 4.5 fF and better match is obtained. Figure 2-9 presents obtained results from the circuit modeling for reduced C_f, measurement, and HFSS simulation.

For this case, measurement and circuit simulation are in quite well agreement. Reason behind the reduced capacitance can be the bridge layer over the recessed ground plane. The bridge layer extending to the slots on the ground plane acts like a series capacitance, reducing the effective capacitance.

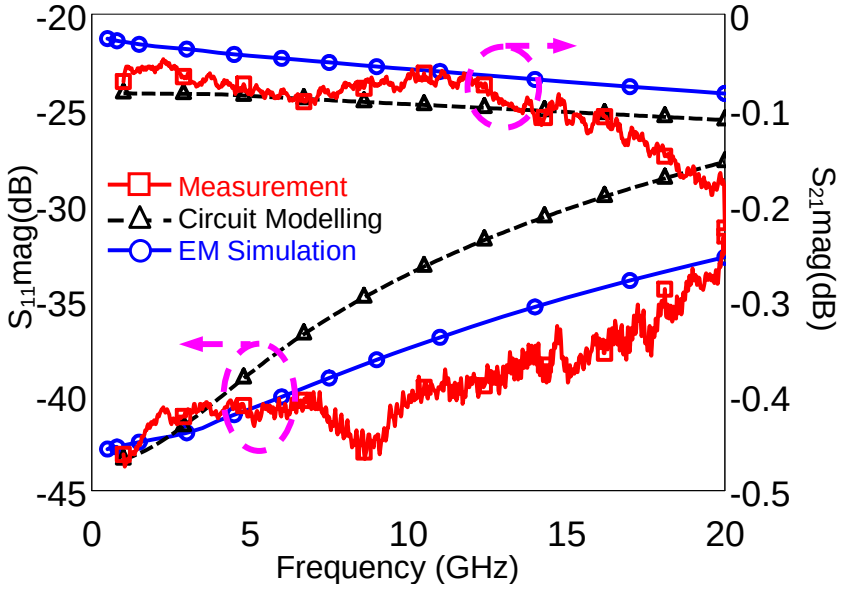


Figure 2-9: Results of downstate modeling of the series switch.

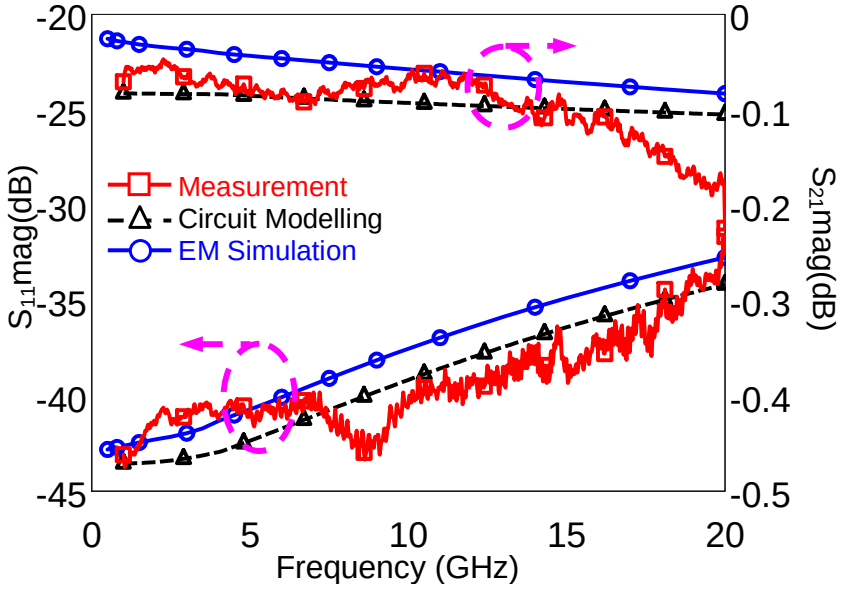


Figure 2-10: Results of downstate modeling of the series switch with reduced C_f.

2.3. Mechanical Modeling

In MEMS systems, design of the mechanical parts has crucial importance for overall system performance. Parameters like actuation voltage and switching time of the switch is closely correlated with the mechanical design of the switch. Most of the semiconductor-based systems operate in 0-5V range and sub-microsecond time scales. However, actuation voltages of the RF MEMS systems are in the range of 10-80V and typical switching time values are in the order of tenths of msec to few μsec. Hence careful design procedure should be followed for proper operation.

2.3.1. Mechanical Spring Design

Membranes deforms from its original position, under the effect of the applied forces. Understanding and using the deformation of beams forms the first step of the MEMS design. Analysis of the fixed-fixed beams carried in this part of the thesis. Cantilever type structures are very similar in the derivations and left to reader. Also, deformation of the bodies is assumed to be small and analysis will be carried according to this assumption.

In MEMS applications, in order to obtain smaller actuation voltages, bias electrode and movable membrane kept larger. Furthermore, actuation electrode is as large as possible and covers the whole membrane for saving bridge area, and reducing actuation voltage at the same time. Hence, for most of the designs force acting on the membrane is uniform. Figure 2-11 depicts the conventions used in the derivations in the mechanical modeling.

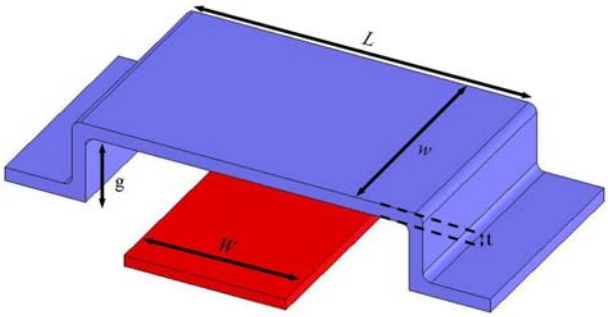


Figure 2-11: Conventions used for the mechanical modeling.

For a concentrated load, applied to a distance of "a" from the anchor of a fixed-fixed beam, L denotes the length of the beam, w stands for the width of the beam, g is the suspended air gap of the membrane and W is width for the actuation electrode. Forces and moments acting on the beams can be found as [24]:

$$M = EI\frac{d^2v}{dx^2} \tag{2-18}$$

$$V = \frac{dM}{dx} \tag{2-19}$$

$$q = \frac{dV}{dx} \tag{2-20}$$

$$q = EI\frac{d^4v}{dx^4} \tag{2-21}$$

where v is the deflection of the beam, V is the shear force, M is the moment, E is the Young's modulus and I is the moment of inertia. For any x on the beam ($x<a$)

$$M = -\frac{Pab^2}{L^2} + P\frac{b^2}{L^3}(3a+b)x \text{ for } x \le a \tag{2-22}$$

$$\theta = -\frac{(a-L)^2 Px(Lx + 2a(-L+x))}{2EIL^3} \tag{2-23}$$

$$v = -\frac{(a-L)^2 Px^2(-3aL + 2ax + Lx)}{6EIL^3} \tag{2-24}$$

V is the deflection of the any point on the membrane. For the evaluation of the behavior of midpoint, under the affects of the applied forces entirely on the beam:

$$x = \frac{L}{2} \tag{2-25}$$

$$v = -\int_{\frac{L}{2}}^{L} 2\frac{(a-L)^2 Px^2(-3aL + 2ax + Lx)}{6EIL^3} \tag{2-26}$$

$$v_{tot} = -\frac{L^4}{384EI} \tag{2-27}$$

For a particular case, integration limits can be changed. For the loads concentrated in the centre "y" away from the anchor, evaluation of the integrals yield:

$$v_{tot} = -\frac{(\frac{L^4}{16} + y(-L+y)^3)}{24EI} \tag{2-28}$$

or for the case where loads are applied between "y" and "z" away from the anchor.

$$v_{tot} = -\frac{(-y(-L+y)^3 + z(-L+z)^3}{24EI} \tag{2-29}$$

For an applied force, one can obtain the deflection in the centre using the Equations (2-28) and (2-29), since we know from the definition of the spring constant one can define an effective spring constant as:

$$F = kx \tag{2-30}$$

and for a distributed load P, effective force on the line is

$$\xi = \frac{P}{L} \tag{2-31}$$

$$v_{tot} = -\frac{L^4}{384EI}\frac{P}{L} \tag{2-32}$$

$$k = \frac{P}{L^3 P}384EI \text{ or } k = \frac{1}{L^3}384EI \tag{2-33}$$

where I is the second moment of inertia defined as:

$$I = \int y^2 dA \tag{2-34}$$

For beam of width w and thickness t evaluation of Equation (2-34) gives:

$$I = \frac{wt^3}{12} \tag{2-35}$$

Hence, substituting in Equation (2-33) gives:

$$k = \frac{32Ewt^3}{L^3} \tag{2-36}$$

Carrying the same analysis for the loads concentrated on the centre, one can find the spring constant as:

$$k = \frac{32Ewt^3}{2L^3W - 2LW^3 + W^4} \tag{2-37}$$

For the design of the cantilever type beams same approach can be used.

In addition, effects introduced in the production steps, which results in residual stress, affect the behavior and spring constant of membrane. Bending of the beam related to the residual stress can be derived. Lateral forces acting on the bridge due to the uniaxial residual stress are given by [25]. For an applied force "*P*", "*a*" distance to anchor of beam, vertical deflection is "*u*". Due to the applied force beam stretches and forces acting on the beam can be found as:

$$F = \sigma(1-\nu)tw \tag{2-38}$$

$$F_1 = F + \frac{twE(\Delta_1)}{a} \text{ and } F_2 = F + \frac{twE(\Delta_2)}{(l-a)} \tag{2-39}$$

where σ is the uniaxial residual stress and υ is the Poisson's ratio. Forces F_1 and F_2 opposes the applied force P. Hence, vector addition of F_1 and F_2 gives the P. Assuming deflections are small, vertical components of the forces are found to be:

$$F_{1ver} + F_{2ver} = P \tag{2-40}$$

$$F\frac{u}{a}+F\frac{u}{l-a}=P \tag{2-41}$$

$$u=\frac{a(l-a)P}{Fl} \tag{2-42}$$

Using, similarity of the triangles deflection in the center of the line is

$$u_{\frac{l}{2}}=\frac{(l-a)P}{2F} \tag{2-43}$$

For the distributed uniaxial residual stress over the beam, total deflection is:

$$v_{\frac{l}{2}}=2\int_{\frac{l}{2}}^{l}\frac{(l-a)P}{2F}da=\frac{l^2P}{8F} \tag{2-44}$$

Using same definitions as in the case of the Equation (2-44), spring constants for the distributed load and concentrated in the middle are given:

$$k_{distributed}=\frac{\frac{P}{l}}{\frac{l^2P}{8F}}=\frac{8F}{l} \tag{2-45}$$

$$k_{centered}=\frac{8F}{3l-2y} \tag{2-46}$$

Total spring constant of the device can be found by summing up two spring constants together. Hence total spring constant becomes the forces acting due to the stiffness of the beam and the residual stresses coming from the process conditions or previous deformations of the membrane.

2.3.2. Actuation Voltage

Movement of the electrostatic actuation is based on the electrostatic forces acting between the plates due to the potential difference across the plates. Initially membrane and actuation electrodes are modeled as a capacitor and the fringing fields neglected for the simplicity of the analysis. Force acting on the plates can be found as:

$$W_{stored} = \frac{1}{2} C V^2 \text{ where } C = \frac{\varepsilon w W}{g} \tag{2-47}$$

where E is the stored energy on the capacitor and the g is the distance between the plates.

$$F = -\frac{1}{2} V^2 \frac{\varepsilon w W}{g^2} \tag{2-48}$$

Equating the electrostatic forces and mechanical spring constants gives displacement for an applied voltage V:

$$\frac{1}{2} V^2 \frac{\varepsilon w W}{g^2} = k(g_{initial} - g) \tag{2-49}$$

$$V = \sqrt{\frac{2k(g_{initial} - g)g^2}{\varepsilon w W}} \tag{2-50}$$

For the actuation voltage derivation with respect to g and substituting in Equation (2-50), actuation voltage is found to be:

$$g_{unstable} = \frac{2g_i}{3} \tag{2-51}$$

$$V_{act} = \frac{2}{3\sqrt{3}}\sqrt{\frac{2k\left(g_{initial}\right)^3}{\varepsilon w W}} \tag{2-52}$$

Also carrying a similar analysis for the hold down voltage one can find the following equations:

$$V_{hold} = \sqrt{\frac{2g_{diel}g_{initial}k}{\varepsilon_r \varepsilon_0 w W}} \tag{2-53}$$

2.3.3. Switching Time

Switching time of the semiconductor devices are in the order of nsecs. However, due to the mechanical limitations of the MEMS most of the RF MEMS switches operate in the μsecs. Understanding the operation of the switching time mechanism is crucial for this reason. In most of the cases, RF MEMS shows excellent RF characteristics like low insertion loss and high isolation, however switching time is the limiting factor for application areas of MEMS devices.

For our particular case, switching time mostly depends on the formation of the metallic contact. In the release stage of the switch, metallic contact behaves like a capacitive contact. Due to low contact area, capacitive coupling is low and hence isolation is high. For the reverse case, same procedure applies. Hence, for the metal-to-metal switch under investigation, mechanical properties of membrane are not dominant in switching time. However, response time of the switch is determined by the mechanical properties.

For the analysis of the switching time, following assumptions are made for simplicity of the analysis:

- The electrostatic force between the bridge and the actuation electrode is constant.
- Damping is small. ($b \approx 0$)

Using the d'Alembert principle [26], the following analysis is carried:

$$m\frac{d^2x}{dt^2} + b\frac{dx}{dt} + kx = F \tag{2-54}$$

where m is the effective mass, x is the displacement from original position, b is the damping, k is the spring constant and F is the external force.

$$-m\omega^2 x - jwbx + kx = F \tag{2-55}$$

$$\omega = \sqrt{\frac{\frac{-F}{x} + k}{m}} \tag{2-56}$$

$$t_s = \frac{T}{4} = \frac{1}{8\pi}\sqrt{\frac{m}{\frac{-F}{g_0} + k}} \tag{2-57}$$

2.3.4. Comparison with the Simulations

Mechanical simulations of the metal-to-metal contact switch are carried with the ANSYS Multiphysics 9.0 by Dr. David Elata[1]. According to the simulations following data is obtained.

Table 2-3: Comparison of mechanical simulations with modeling.

	Actuation Voltage (V)	*Switching Time* (μsec)	*Applied Voltage* (V)
ANSYS	22.5	5.7	35
Modeling	17	9.7	35

By using the formulation provided, results similar to the FEM (Finite Element Modeling) solution is obtained as given in Table 2-3.

2.4. RF Measurement Setup

For the on-wafer s-parameter measurements, a network analyzer with a manual probe station is used. Figure 2-12 illustrates the measurement setup used for the on-wafer measurements of the RF devices.

RF measurements are carried with HP 8720D 0.5 – 20 GHz vector network analyzer. For probing components, Cascade Microtech Summit 9000 manual probe station is used. Picoprobe 40-A-GSG-150P CPW probes with on wafer SOLT calibration are

[1] AMICOM FP6 NoE partner; Technion University, Tel Aviv, Israel

used for connection to devices. For biasing devices and protection of the network analyzer, Picosecond 5542-230 bias tees are connected to the RF lines.

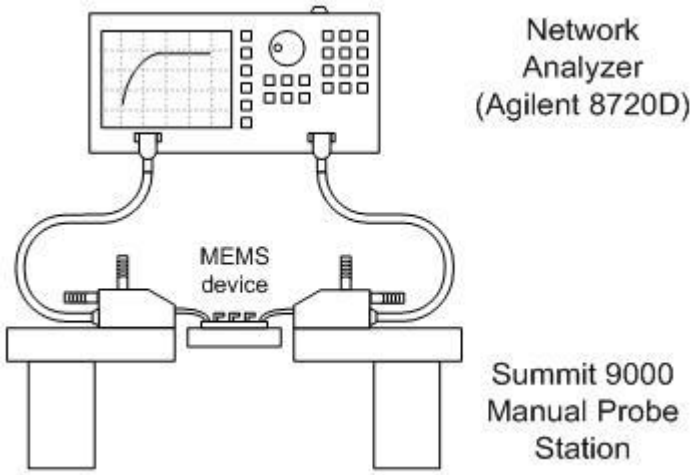


Figure 2-12: RF measurement setup used for on-wafer measurements.

2.5. Switching Time and Power Handling Measurement

Industry uses figure of merits to judge the different technologies and different components, like switching time, power handling, IMD (Intermodulation Distortion), capacitor on/off ratio, insertion loss, isolation, etc. For the analysis of the component, full characterization of the stated parameters is necessary. However, due to the high voltage requirement of the RF MEMS devices, measurement of these parameters cannot be done with customary equipments and special equipments are required. For the measurement of the switching time of the switch, a custom system is designed and produced.

2.5.1. Measurement Setup

With the “on” and “off” states of the switch, output waveform is AM modulated and with proper detector circuit, demodulation of output signal is possible. Detectors are used for converting the amplitude-modulated signals to baseband signals. Basic detector topology is a halfwave rectifying circuit constructed using a diode and resistor capacitor pair. Figure 2-13 demonstrates the circuit diagram of the constructed detector circuit. Diode charges the capacitor and capacitor discharges over the shunt resistance. Detector time constant is defined as:

$$\tau = R \cdot C \tag{2-58}$$

and for proper operation, time constant should be smaller than the successive peaks of the message signal and larger than the period of carrier signal.

$$T_m > \tau > T_c \tag{2-59}$$

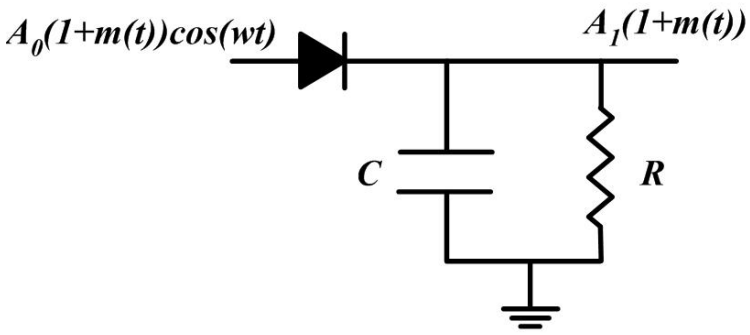


Figure 2-13: Circuit diagram of the demodulating circuit.

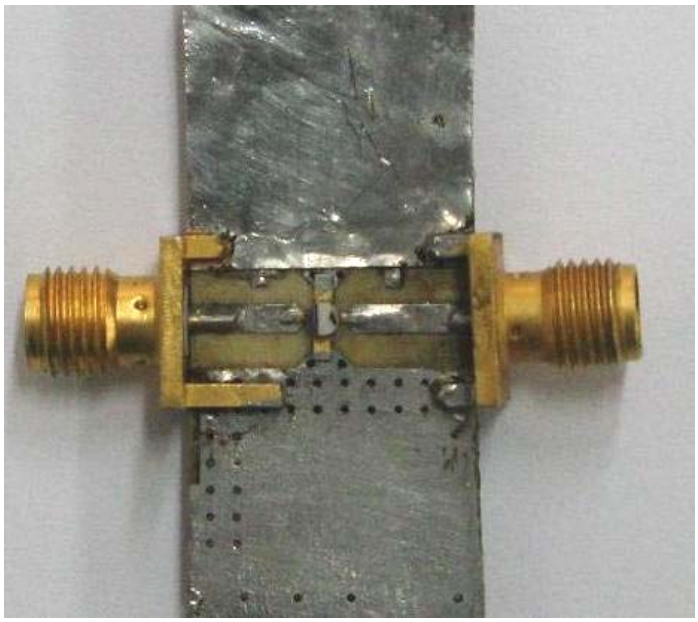


Figure 2-14: Demodulating circuit.

However, in the actual circuit, instead of the diode, Schottky diode of a HEMT transistor is used (FHX13LG) and for the low pass filter input impedance of the oscilloscope is used (HP54645D). Also for further amplification of the small signals, additional amplifying sections can be added after the diode section (LF353). Figure 2-14 shows the demodulating diode section of the switching time setup.

After introducing an RF generator and bias voltage for the modulation, necessary components for the switching time equipment are completed. For the RF signal source HP 8350B is used and for modulating the bias voltage of RF MEMS switch, custom waveform generator is used. Details of the waveform generator are given in Chapter 4.

The RF power at a certain frequency is fed to the switch, output of the switch is connected to the demodulating circuit, and behavior of the switch is observed on the oscilloscope. Using a high voltage waveform generating circuit, the switch is opened

and closed at a low frequency (~100Hz). Hence, switching time can be observed on the screen. However, the high voltage waveform circuit can produce up to 100V. Such a high voltage can damage the RF source and demodulating circuit. In order to prevent a possible damage in the system, DC blocks are needed. Available bias tee has an attenuation of 20 dB and is not sufficient for proper operation. For higher attenuation levels two back to back WR90 waveguides are used. Moreover, for the total isolation of the lines, a dielectric layer placed between the adapters and connected using non-conducting wires. Figure 2-15 shows the constructed DC block. Hence, total isolation better than 150 dB is achieved with new topology. Furthermore, instead of the waveguides, couplers can be used for saving space according to desired frequency bands.

Figure 2-15: DC blocks formed by WR90-SMA adapters.

Total system is formed by a signal source, followed by a switch to be measured and connected to biasing circuit over a bias tee. The RF signal generator and the demodulation circuit is protected against high voltage using two DC blocks at input and output ports of the MEMS switch. The output of the switch is connected to a demodulating circuit and an oscilloscope for better visualization. Figure 2-16 illustrates the general structure of the time domain measurement setup.

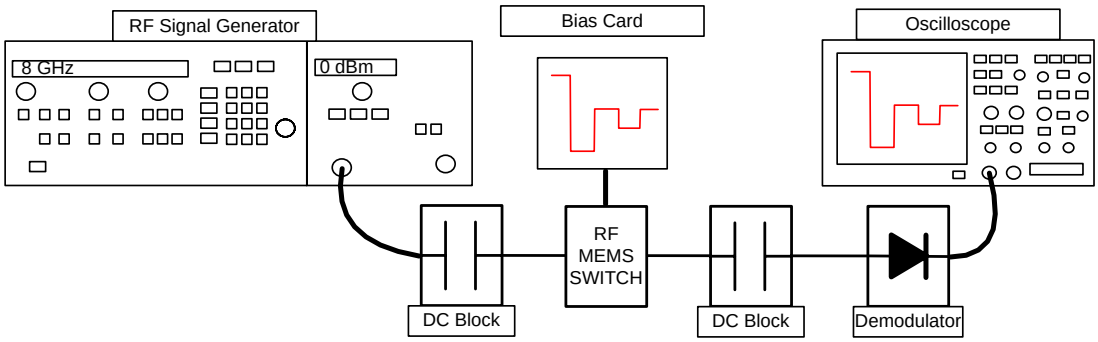


Figure 2-16: Time domain measurement setup.

2.5.2. Time Domain Measurements

Operation of the system given in Figure 2-16 is based on the tracking the signal level difference on the demodulation circuit and hence several measurement can be carried at the same measurement cycle. Function of the detector diode is the power level detection. Hence tracing the time domain data gives rise and fall times of the switch. Moreover, with the precise control of the applied bias voltage, actuation voltage can be deduced from the measurement. With the actuation and de-actuation of the switch, diode reading changes, hence actuation and release voltages can be found.

An AM modulated signal is generated using HP 83640A 8360 series synthesized sweeper and fed to the input of the demodulating diode. With the demodulator and oscilloscope section shown in Figure 2-16, rise and fall times better than 1 μsec can be measured, therefore this setup can be used for most of the RF MEMS switches without any particular problem. Resolution of the system is limited by the resolution of the oscilloscope and can be increased by the additional amplifying sections, however is not necessary for this case (~5mV resolution). Figure 2-17 presents a sample measurement result of an RF MEMS switch.

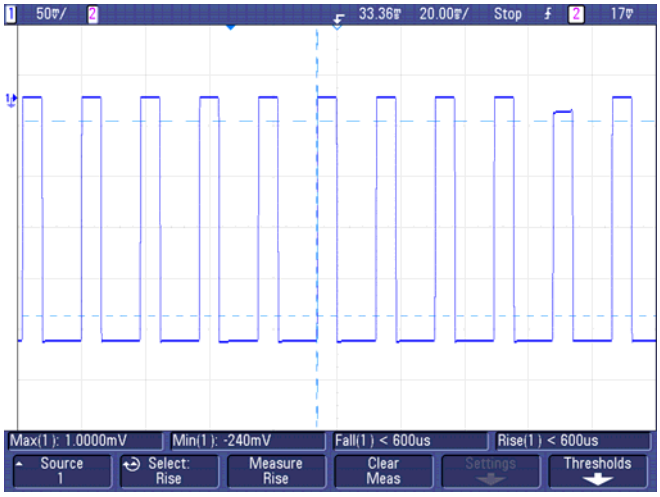


Figure 2-17: Output of the measurement setup.

Both capacitive and metal-to metal contact switches are measured using the same setup. Initial measurements are carried on the capacitive type switches. Measurement results are compatible with the expected results.

Fall time of the switch (up to down movement of bridge) is mainly determined by the applied actuation voltage and mechanical spring design of the switch. For the measured devices, fall times of 5 to 65 μsec are observed. Rise time (down to up movement) of the switch is caused by the restoration forces of the membrane and expected to be much lower than the fall time of the same switch. According to the measurement results rise times of 15 to 140 μsec is observed. Measurements are taken with a carrier frequency of 71 kHz and a message signal of 14 Hz. Table 2-4 gives measurement results of the capacitive type RF MEMS switches.

As can be seen from the Table 2-4, switches that have lower actuation voltages have larger rise times and hence lower spring constants. Type C2 switch has long meandered arms and therefore its spring constant is low. Types B1, B2, B3 and A1 have a bridge width of 50 μm. Type A2 has a bridge width of 80 μm. Types B4 and B5 have a bridge width of 100 μm. All switch types have a bridge length of 320 μm.

Types C1 and C2 have meandered bridge arms. Detailed description is given in appendice. Differences between the same types of bridges are due to the process related stress and can be solved by optimizing process conditions. However, in general with wider bridges, actuation voltage tends to be smaller and rise times increases.

Measurement of the metal-to-metal switches cannot be carried with same carrier frequency due to increased impedance of the bias electrodes and has to be lowered for proper biasing. After reducing the carrier frequency down to 330 Hz and switching frequency of 54 Hz, switching response of the metal-to-metal contact switch is measured.

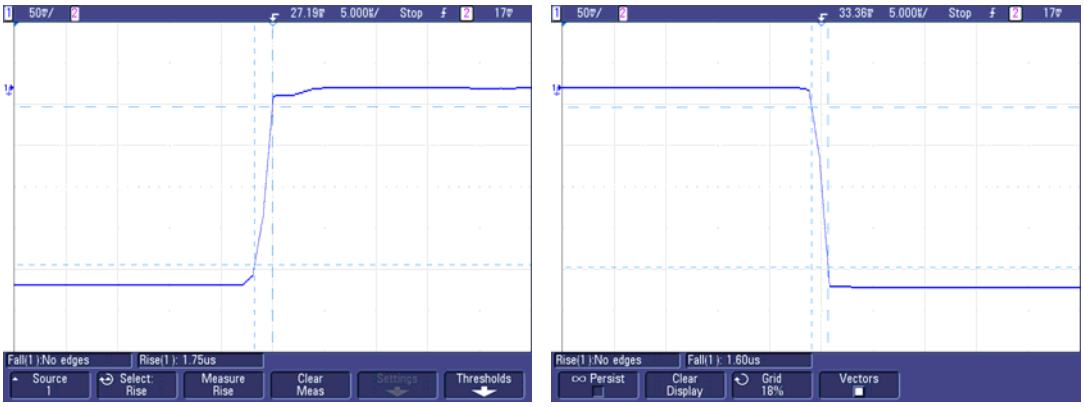
Table 2-4: Switching time measurements of several capacitive switch types

Switch types	*Actuation Voltage* (V)	*Fall Time* (μsec)	*Rise Time* (μsec)
A1	24	10	37
A2	23	10	38
B1	18	10	16
B2	22	5	24
B3	21	10	15
B4	23	20	26
B5	16	20	15
C1	11	50	97
C2	10	65	138

Figure 2-18 presents the switching time measurements of the metal-to-metal contact switch. Measured rise time is 1.75 μsec and fall time is 1.6 μsec for an bipolar actuation of +/- 40 V. Both rise time and fall time of the switch are less than 2 μsec, which is faster than any of the capacitive type switches. In addition, measured response is faster than the simulated and the modeled values. These measured values are comparable to the reported best values in the literature [28], and [29]. As the spring constant of the beams increases, the switching times decreases. On the other hand, actuation voltage also increases. A switch with 0.4 μsec switching time and 120V actuation voltage is the reported fastest RF MEMS switch.

In case of the capacitive switches, switching time is related to the mechanical movement of the membrane. Since the capacitance is varied with the movement of the bridge layer, faster movement of the bridge results in faster switching time for the switch. For the metal-to-metal contact type switch, switching time is not limited by the mechanical characteristics of the membrane. Capacitance of the contact region is very small and variation on this parasitic capacitance can be ignored. At the down state of the switch, with the increased contact pressure between the layers capacitive contact is replaced with the metallic contact. Switching time of the metal-to-metal contact switch depends to the formation of the metallic contact. Quality of the contact formed and time of contact formation determines the switching time.

Investigating the rise time and fall time of the switch reveals that, transitions of the switch are clean and hence bouncing is not observed during the actuation and release states.



(a) (b)

Figure 2-18: Switching time of the metal-to-metal contact switch. (a) Rise time, and (b) Fall time

For better visualization of the contact degradation, output power of the demodulator is recorded for increased switching cycles. With an applied voltage of 32 V and switching frequency of 52 Hz, diode output is recorded. Initially diode reading is at 310 mV and with increased number of switching, diode output falls down to 13 mV. Figure 2-19 illustrates the power and number of switching relation.

For the direct contact of metallic surfaces, contact forces and applied pressure should be high. With increased number of switching, contact points wear out and pressure between the metal surfaces decreases due to smoothed surfaces and hence output power of diode degrades. After 7000 switching, contacts act like capacitive type and diode reading reduces to 13 mV. To be able to get faster switching times, contact formation should be as fast as possible. Harder material deposition to the contact points and additional dimples can solve the problem.

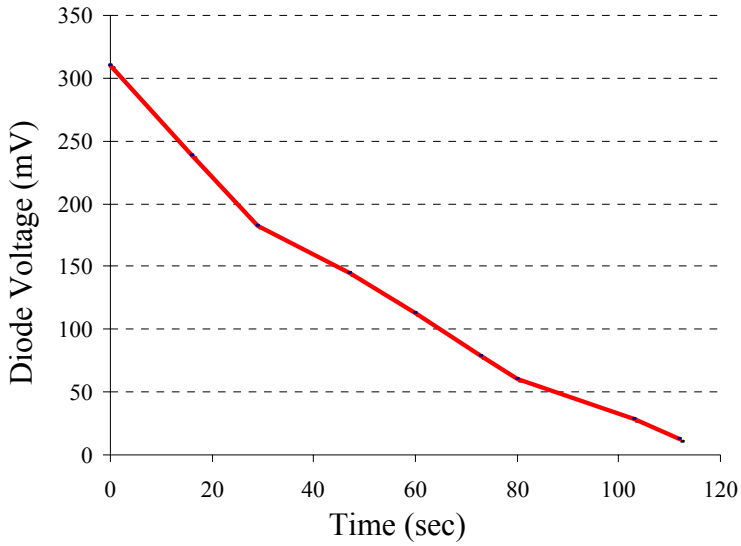


Figure 2-19: Output power of the switch at a switching frequency of 52 Hz.

2.5.3. Power Handling Measurements

Power handling of the switches are mainly depends on the mechanical design of the switches and the materials used in fabrication of the switch. For the measurement of the power handling of the switches, setup shown in Figure 2-16 is used with some minor modifications.

The measurement setup is calibrated for the evaluation of the exact power level, applied on the switch. Calibration procedure is as follows:

Initially, power level output from the HP 8350B is measured using E4408B spectrum analyzer for various power levels of HP 8350B. Then, output of the signal source is connected to the input port of the probe station. RF probes are connected to each other with a short length, low loss, and 50 Ω transmission line. Hence, introduced by the transmission line section is minimized. Finally, output power from the output

port of the probe station is measured. Therefore, difference between the input and output port power of the probe station reveals the power dissipated on the transmission lines of the probe station. Probes and transmission lines used in the probe station is identical. Hence, power loss on a single line can be found as half of the total loss on the probe station.

There are various definitions for power handling, such as hot switching, cold switching, average power, and peak power [29]. For the hot switching, RF power is present at the ports of the switch during switching. Hence, switch experiences stress on its contacts. In the case cold switching, RF power is removed from system. Therefore, stress on the contacts is reduced. Hence, expected lifetime of the switches is increased. There is a limit that can be applied to the switches due to the heating of the materials used in the switch. With increased power levels applied to the switch, power dissipation increases. Excessive heating of the switch may cause material deformations and degradation on the switch performance. The heat that can be handled by the switch limits average power. In pulsed applications, instantaneous power handling of the switch should be exceeded. Moreover, average of the RF pulse should be lower than average power handling of the switch.

Power handling of the type A1 switch is measured and compared with the metal-to-metal contact switch. Up to 20 dBm input power, which is the limit of the signal source, both switch types are operational. Table 2-5 shows the hot switching response of the type A1 switch at 8 GHz. Switch is actuated with bipolar actuation waveform of magnitude +/- 10 V. With increased power levels, output power of the demodulating section also increases. Hence, switch is functional up to 20 dBm of input power.

Table 2-5: Power handling measurement of the A1 type switch for hot switching.

Applied Power (dBm)	Up-Diode Output (mV)	Down-Diode Output (mV)
5	-24.7	-16.2
10	-88.2	-65.1
15	-174.5	-150
16	-191	-167
18	-230	-206
19	-249	-221
20	-265	-234

For the case of the metal-to-metal switches, for a bipolar actuation waveform of magnitude +/- 40V, diode readings are -1mV and -240 mV for the ‘up’ and ‘down’ states of the switch respectively.

Time domain setup is not sufficient for the measurement of the power handling and an amplifying section is required for increased RF power levels. Therefore, two amplifying sections are added to the output of the signal generator. For the input stage, Eudyna FLM8569-15F X-band internally matched FET amplifier is used. Output stage is formed with the Fujitsu FMM5057VF 7.1-8.5 GHZ power amplifier MMIC. Hence, output power of the signal source can be increased. Demodulating diode experiences high power levels with such configuration and 12 dB attenuator is connected in series for the protection of the diode section.

With new configuration, power handling of the type A1 switch is measured. It is observed that switch can handle 4 W (36dBm) of RF power at 8 GHz. Lifetime of the switch for higher power levels are under investigation. In [30], it is reported that, for their capacitive switch 5.5W is the catastrophic failure RF power level.

Measurements with metal-to-metal contact switches shows that, this type of switch cannot handle 250 mW input power for hot switching applications. However, for cold switching this type of switches are operational.

2.6. Summary

Chapter 2 presented metal-to-metal contact switch design for the wideband RF MEMS systems. Switches are developed, fabricated and tested. Electromagnetic modeling including loss of the transmission lines, upstate and downstate modeling of the components in conjunction with mechanic modeling including, actuation voltage and switching time has presented. Equivalent circuit modeling is presented and compared with the electromagnetic simulators and the measurement of the devices. For the characterization of the switches, a time domain measurement setup has constructed for the dynamic behavior of the components. Switching time and power handling measurements have taken with new setup. In addition, measurement data has compared with the modeling results.

CHAPTER 3

FABRICATION OF METAL-TO-METAL CONTACT SWITCHES

For the fabrication of the MEMS devices, METU Micro Electronics Facillities (METU MET) is used. This facility is specialized on the fabrication on several MEMS devices like microsensors, microbolometers, gyroscopes and RF MEMS. Hence, for the production of the metal-to-metal RF MEMS switches, process developed in the METU MET is used[2].

Fabrication is based on the surface micromachining techniques due to thin layers of materials for the construction of the overall structure. First step is the design and layout drawing of the devices composed of several masks. At the fabrication steps, deposition of thin layers of materials followed by patterning of the layers using photolithography and finally etching of the remaining parts. Total structure is formed by stacking of several layers. For the movable parts, sacrificial layers are used and removed at the end of the process. Section 3.1 presents the masks required in the fabrication steps. Section 3.2 defines the production steps and materials used during the fabrication steps. Finally, Section 3.3 gives the process flow of the METU RF MEMS process.

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[2] *Researchers involved in the development of the RF MEMS processes are: Mr. Hüseyin Sağkol, Mr. Mehmet Ünlü, Dr. Kağan Topallı, Ms. İpek İstanbulloğlu, Mr. Engin Ufuk Temoçin, and Mr. Halil İbrahim Atasoy.*

3.1. Mask Production

Masks are used for the definition of the process areas optically. For this purpose mask are build on an optically transparent materials and intended portions of the mask are covered by a opaque materials. Hence, ultraviolet light send from one side is selectively transferred to the other side.

The photoresist is a light sensitive material used in the microfabrication processes. Spin coating or spray coating can be used for the applying uniform layer of photoresist on wafer. Using the selective transmission of light and photo definable photo resist layer, pattern on the mask can be transferred on to the wafer. According to the polarity of the photoresist used, after the development stage UV absorbed regions dissolve (positive) or unabsorbed regions dissolve (negative) in developer. Hence, desired pattern is transferred to wafer.

For the mask drawings CADENCE IC design 4.4.5 is used. For the production of the masks mask maker available in the METU MET is used. Masks are built on a 5 inch x 5 inch quartz substrates and chrome coating is used for the opaque material. 7 different masks are used for the processing. Definition of each mask layer given briefly and detailed description will be presented in following sections.

Mask #1: (clear field mask) Resistive bias line implementation. Used for patterning highly resistive bias lines.

Mask #2: (dark field mask) Electroplating mask. Thick electroplating metallization used for reducing line losses.

Mask #3: (clear field mask) Base metallization mask. Thin metallization used for CPW lines.

Mask #4: (clear field mask) Dielectric mask. Isolation layer is used for protection against short circuit or capacitance formation.

Mask #5: (dark field mask) Anchor mask. Placements of anchor areas are defined.

Mask #6: (clear filed mask) Structural layer mask. A movable portion of the switch is defined.

Mask #7: (clear filed mask) Backside metallization mask. For the compatibility of the designs, backside is selectively etched.

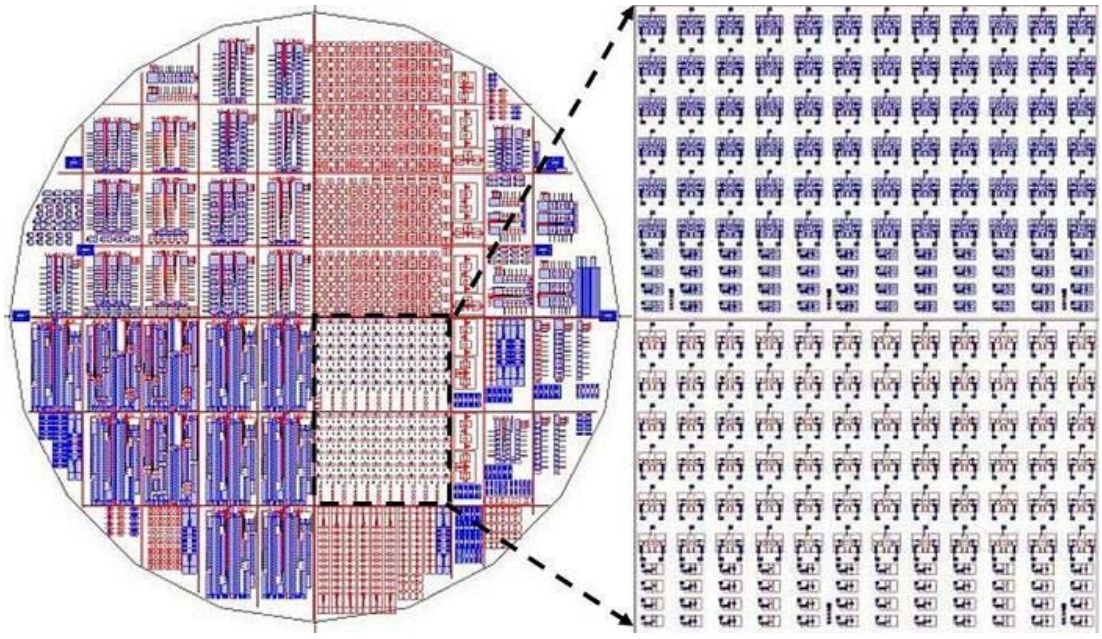

Figure 3-1: Switch placement on total layout.

Process steps of the metal-to-metal switch are same with the conventional process steps developed for RF MEMS devices. Only difference is the variation in purpose of some layers. Also processing is similar to other devices and can be produced in

the same run. Indeed a special wafer is not prepared for this specific switch type and produced on the same wafer with capacitive type switches.

3.2. Fabrication Techniques and Required Layers for RF MEMS Technology

Fabrication is based on the surface micromachining technology. Basic production steps are, thin film deposition, lithography, electroplating and etching. Figure 2-1(b) shows the general view for a sample RF MEMS device. General structure composed of a base metallization for transmission line formation, thick electroplating for reducing losses, dielectric layer for the isolation and a movable membrane section. Movable membrane formed by a use of sacrificial layer. Membrane constructed on sacrificial layer and at the end of process, sacrificial layer is removed.

Process yield and reliability of the product highly depends on the materials and interaction between the materials. Hence, selection of the materials, process conditions, process types and equipments are important for the overall production and device performance. In order to obtain best characteristic form the devices, optimization on the processing conditions are necessary.

Substrate section is mostly depends on the RF concerns. However due to the integration with other technologies, special care should be taken if integration is necessary. Several substrate types are used for the production of the RF MEMS devices. High resistivity silicon with the use of insulation layers can be used for the substrate material. Semi insulating GaAs can be used due to easier integration with the active devices. Hence amplifying sections can also be built on the same substrate. LTCC is also used as substrate. With LTCC substrates, packaging of the MEMS is possible, since LTCC is used in the packaging industry. Glass, alumina

and quartz is also used for the substrate, since all offer low dielectric loss. Glass is selected for the reduced dielectric losses and low cost of the substrates.

Base metal is constructed using gold, aluminum, copper or nickel. Higher conductivity materials selected for the reduction of losses on transmission lines. Some hard materials like platinum, tungsten, titanium, gold-palladium alloys or proprietary alloys are used in the contact formation. Since gold is a noble metal, effects of the subsequent process steps is lower, which is not the case especially for copper. In addition, deposition of gold is easier due to the soft nature of the gold; hence, gold base metal is selected.

Isolation materials are used for preventing DC shorts between the movable membrane and actuation electrodes on device. According to the actuation voltages applied, thickness of the dielectric should be modified. For higher actuation voltages, thicker dielectric layers can be used according to applied electric field stress. Several dielectric types used in the RF MEMS processes are, silicon nitride (Si_xN_y), aluminum nitride (AlN), strontium-titanate-oxide ($SrTiO_3$), barium-strontium-titanate (BST), tantalum pentoxide (Ta_2O_5), lead zirconium titanate (PZT) and hafnium dioxide (HfO_2). According to the available instrumentation silicon nitride is used for the dielectric. Silicon nitride has a dielectric strength of 10^7 V/cm.

The sacrificial layer forms scaffolding for the construction of the bridge. At the end of the process, it is removed from the structure. Hence, it should be non-volatile during the process steps. However, at the end of the process it can be removed under the structural layer without residue, introducing residual stress or deformation to rest of the structure. Also for the proper operation and uniformity of the process, deposition should be uniform along the wafer. There are several sacrificial layers presented in the literature. Some of them are photoresist, silicon oxide, polyimide or copper. Photoresist and copper can be easily affected by the process conditions and chemicals used during the fabrication. Photoresist outgas in hot environments and

causes cracks on the structural layer and easily dissolve with acetone. In addition, copper is sensitive to most of the chemicals in the environment and even reacts with the air and DI. Moreover, most critical issue in the copper sacrificial layer is the uniformity. Copper electroplating gives non-uniform results in sacrificial layer thickness for most of the structures. Hence, polyimide process is optimized and used. Polyimide is resistant against most of the chemicals used in the process steps and does not affected from the higher temperatures after curing. Polyimide is coated with spinning and uniformity is much better than copper. For the removal of the polyimide, wet etching with SVC or dry etching with RIE is used.

Structural layer is the movable part of the RF MEMS device and mechanical properties of the structural layer play an important role in the overall design parameters and system performance (Section 2.4). Residual stress introduced in the fabrication steps results in increased spring constant values and even worse, total buckling of the membrane. Formation of the structural layer is based on the sputtering or electroplating of the metal layers or stack of the metal layers. In addition, silicon nitride can be used as movable membrane with metal plates implemented on the membrane. In the METU process, sputtered gold layer is used as structural layer due to the higher conductivity and ease of the fabrication. In addition, gold material is durable and does not affect form the environmental conditions.

To be able to get more familiar with the processing terms several fabrication terms are explained in detail below:

Deposition of the thin material is collecting aerosol particles in a surface. Deposition can be carried in two ways. In the physical vapor deposition technique, in a vacuum environment, material is transformed in to aerosol form by means of evaporation or bombardment of energetic ions and collected on another surface. For the chemical vapor deposition technique, wafers are exposed to precursors and react with the

substrate or decompose on substrate surface. Several available chemical deposition techniques are CVD and Plasma enhanced CVD (PECVD). In the PECVD process, plasma is used for the enhancing process and hence deposition can be obtained with much lower temperature values. Hence, materials, which cannot withstand high temperatures like gold, can be used in the fabrication. In the METU MET evaporation, sputtering, PECVD are available and hence used in the process of the RF MEMS. CVD is also available; however not compatible due to the increased process temperature with the materials is used and hence not used in the process steps.

Photolithography is used for the pattering before process. Patterning the surface according to the mask, defines the regions allowed for the removing thin film. Using the UV light to transfer the pattern on to the light sensitive chemical called photoresist (PR) and developing the photoresist in a special chemical gives desired pattern. Photoresist coated to the wafer with the help of the spinning, where a 3-6 ml of photoresist dispensed on the center of the wafer and spin at a certain frequency to obtain uniform layer on the wafer. Most of the photoresists types are soft baked after spinning due to the sticky nature of the photoresist and removing solvents in the photoresist. Hence, after soft bake 0.3 μm to 3 μm thick photoresist is obtained according to the type of the photoresist. The spinning process is followed by the exposure. High intensity light is applied to PR, using mask between as protective layer and chemical changes occur on the light sensitive PR. Exposure stage is followed by the development stage. Some of the photoresist is removed in a special chemical called developer. Developers are TMAH or NaOH based according to the resist used. According to the photoresist type, light interfering PR strips (positive PR) or light interfering PR stands (negative PR). Hence, pattern on the mask is transferred to the PR. In some of the PR hard baking is required in order to obtain a rigid structure as in the case of polyimide.

The last step of the process is the etching. Etching can be made in two ways. In "wet" etching part that are not protected by PR is etched, generally selective etchant according to the thin film material types is used. However, wet etching can cause undercuts and "dry" etching techniques are utilized for anisotropic etching. Instead of the etching process, electroplating can take place. Wafer is placed in a chemical solution for the plating and current used for coating surface. However, wafer should be conductive for the electroplating and total surface is covered with a conductive material before the photolithography. Anode is connected to the depositing material, cathode is connected to the wafer, and both are in a conductive chemical solution. When current flow, material dissolves from anode in to the solution and collects on the cathode.

After the etching or electroplating steps, photolithography step finishes. However, remaining PR parts has to be removed for the following process steps.

3.3. Process Flow

This section briefly presents the process cycle developed in METU MET.

- ***Wafer cleaning:*** For possible organic/inorganic residues, wafers are cleaned using Piranha solution. Piranha is a hot mixture of sulfuric acid and hydrogen peroxide.

- ***Surface roughness:*** In order to increase adhesion between the substrate and deposited layers, polished surfaces are etched slightly with buffered HF. Buffered HF contains NH_4F and HF.

- ***Resistive lines:*** Bias lines, used for the actuation of the MEMS devices are deposited and patterned in the first mask. 2000 Å thick Si-Cr layer is

deposited and after photolithography, etched using buffered HF. Figure 3-2 and Figure 3-3 depicts deposition and patterning of the Si-Cr layer.

- ***Base metal deposition:*** Base metal layer used for the construction of the transmission lines is sputter deposited. Seed layer is composed of a thin layer of Ti (300 Å) for increasing adhesion between the substrate and gold layer. 5000 Å Au is deposited for reducing line losses and reducing current density in electroplating stage. Figure 3-4 shows deposition of Ti/Au layers.

- ***Electroplating on base metal:*** Sputtered base metal is thin and has to be thicken for the lowering line losses. Thick PR layer is deposited and patterned and 3μm gold layer is electroplated in a cyanide-based gold electroplating solution. Figure 3-5 shows the deposition of electroplating layer.

- ***Post etching of base metal:*** Redundant part of the base metal, after electroplating stage is patterned and etched using selective Au and Ti etchants. Figure 3-6 shows the removal of redundant base metal layer.

- ***Dielectric deposition:*** A dielectric layer, used for the short circuit prevention and capacitance formation, is deposited. This layer is a 3000 Å thick Si_xN_y layer deposited with PECVD equipment. After the lithography, etching is carried with reactive ion etching (RIE) technique. RIE is a dry etching technique, undercuts are small, and process is reliable compared to wet etching. Figure 3-7 depicts the formation of dielectric layer.

- ***Sacrificial layer deposition:*** For the sacrificial layer formation, a photo definable polyimide (PI2737) is used. Photolithography stage is same with other photoresists, however contaminates the environment, hence special care should be taken. 2 μm of polyimide is deposited and anchor regions are

defined with the photolithography stage. For the robustness of the material, the wafer is hard baked in oven after the photolithography stage. Figure 3-8 shows deposited and patterned sacrificial layer section.

- ***Structural layer deposition:*** One μm thick gold layer is deposited via sputtering on sacrificial layer. Anchor areas defined by previous lithography stage are forms the anchors of the switch and connect the movable membrane to the base metal. After the lithography step, remaining gold layer is etched with selective gold etchant. In addition, top plates of other structures are formed with the structural layer mask. Figure 3-9 shows finalized structural layer.

- ***Sacrificial layer removal:*** For the easier removal of the sacrificial layer, etch holes are implemented in the structural layer. Hence, isotropic etchants can etch from various locations of the sacrificial layer, resulting faster removal of the layer. Several etch mechanism are utilized for the removal of the sacrificial layer. In the "wet" etching, photoresist striping chemical called SVC175 is used. Wet etching is completed by the critical point drying of the wafer. Critical point drier is used for preventing stiction of the bridges. IPA is replaced by liquid CO_2 and then evaporated rapidly to overcome surface tension of liquids. In "dry" etching, RIE is used to form oxygen plasma in chamber. In addition, CF_4 is added to process, for faster removal of the polyimide residues. Figure 3-10 shows the finalized structure after the removal of the sacrificial layer.

- ***Finalization:*** After the release of the wafer, devices are ready to measure. However, after the release stage, wafer cannot be diced due to the mechanical vibration of the dicer. Hence, dicing should be carried before the release stage of the devices.

Process explained above is used for the capacitive and series switch implementation and system constructed using these components. In addition, MIM capacitors and inductors can be fabricated.

Figure 3-2: 2000 Å Si-Cr layer deposition on substrate using sputtering.

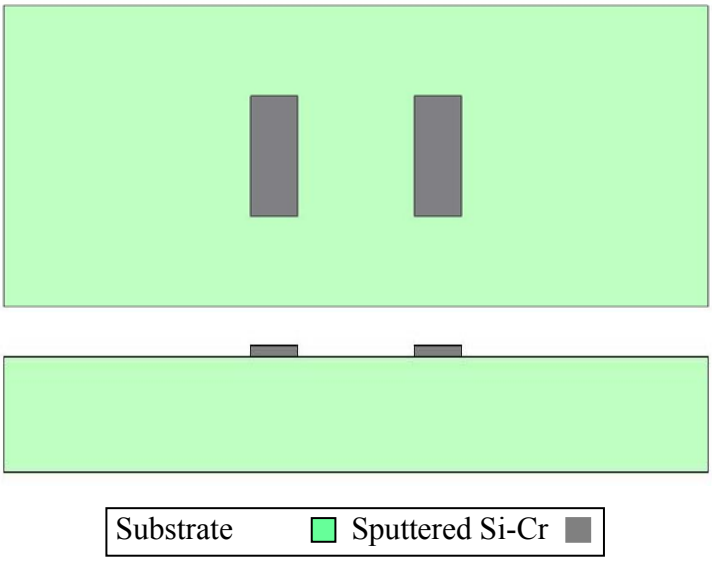

Figure 3-3: Si-Cr patterning using buffered HF.

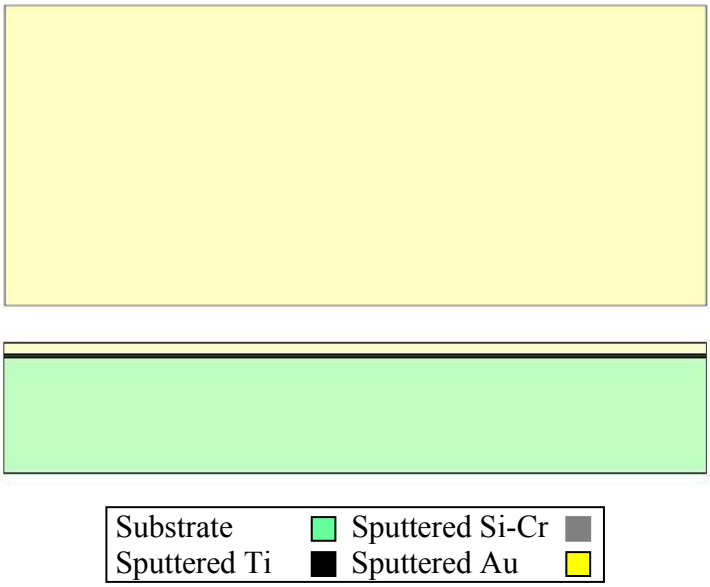

Figure 3-4: Ti/Au (300 Å/5000 Å) layer deposition using sputtering.

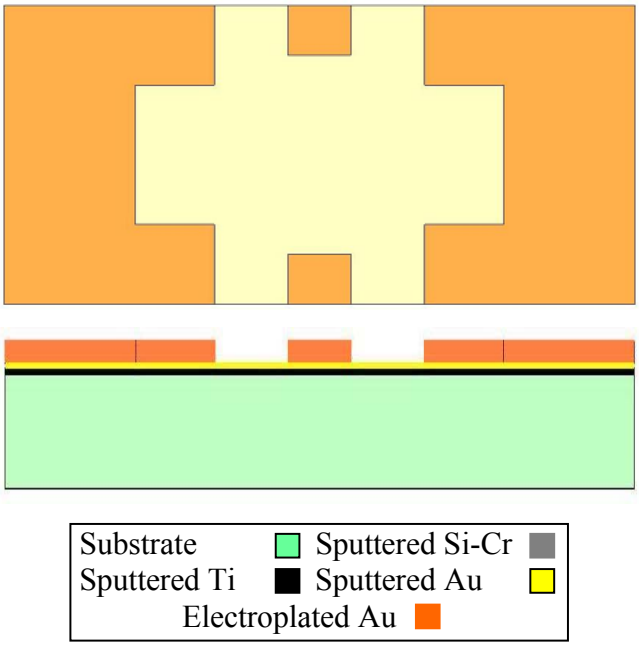

Figure 3-5: 3 μm gold electroplating.

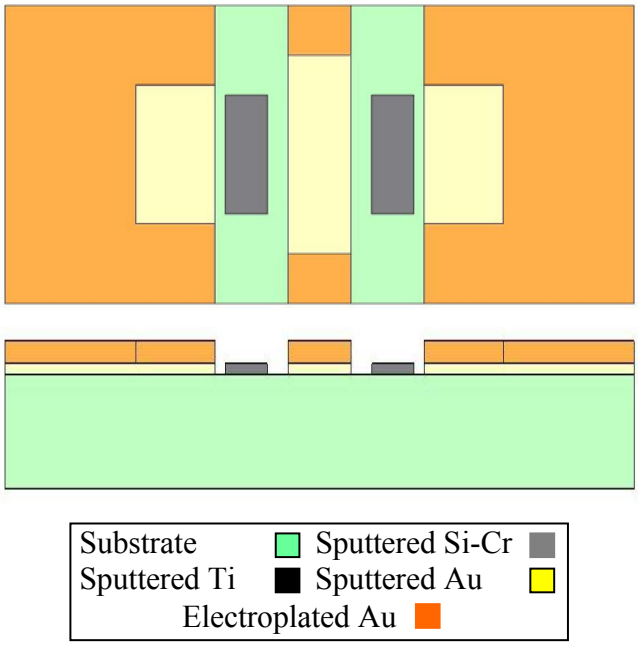

Figure 3-6: Base metal etching of redundant parts.

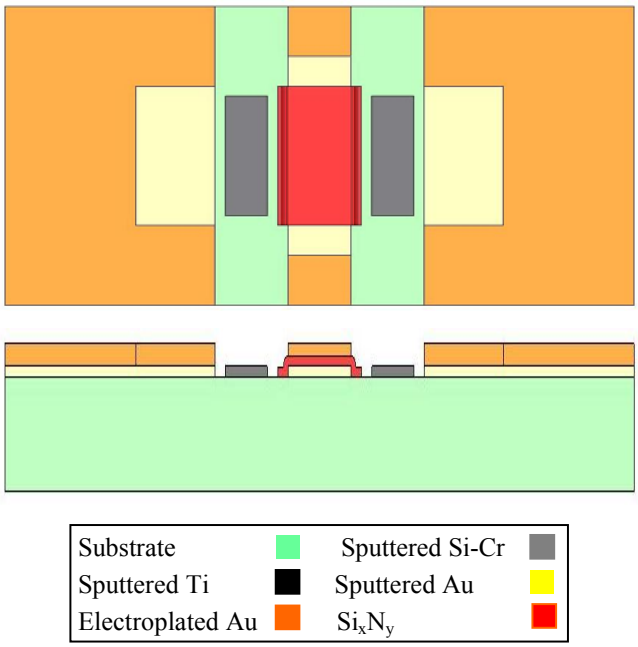

Figure 3-7: Deposition and patterning of Si_xN_y dielectric layer.

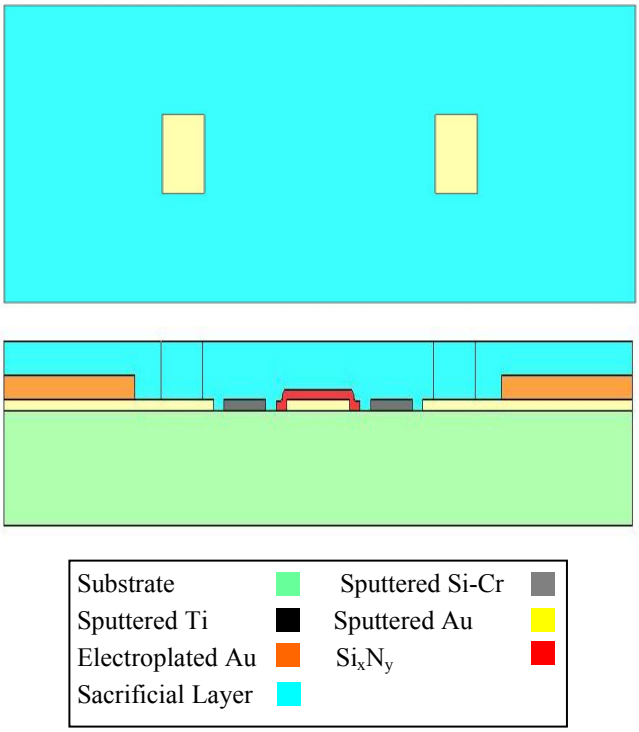

Figure 3-8: Sacrificial layer deposition and definition of anchor regions.

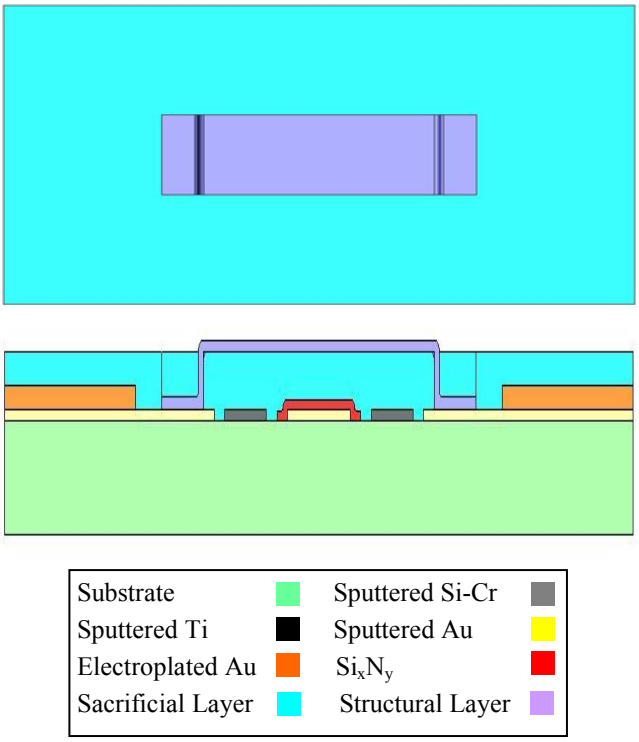

Figure 3-9: Structural layer deposition and lithography.

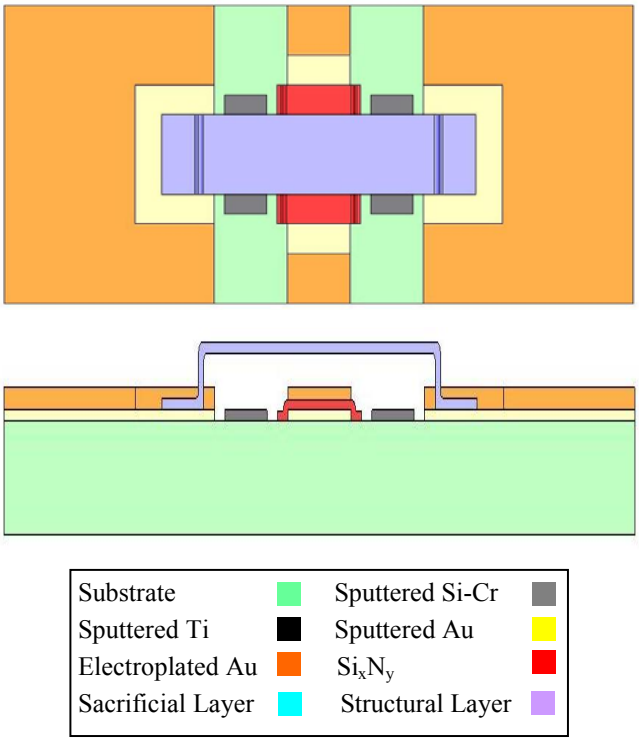

Figure 3-10: Removal of the sacrificial layer.

3.4. Summary

Chapter 3 explained the tool used for the design of the layouts of the RF MEMS devices. Surface micromachining and photolithography process are explained briefly. Steps of micromachining are covered. Moreover, definition and objectives of the mask layers used in the fabrication are provided. Effects of substrate and material selection on the performance and reliability of MEMS devices are discussed. Pros and cons of some materials used in the fabrication are given. Finally, pictorial process flow is presented.

CHAPTER 4

BIASING SCHEME AND LIFETIME OF MEMS STRUCTURES

With the improvements in RF MEMS devices, demand for commercially available components arise. RF MEMS has outstanding performance compared to other technologies; also it offers potentials for wide range of RF applications. However, only limited numbers of commercially available components are announced [12]-[14]. Main limiting factor for the commercial products is the reliability of the devices. Considerable amount of research effort is devoted to increase reliability of the RF MEMS devices [17]-[21].

RF and mechanical performance of a MEMS switch can be affected from various factors. For clarifying the reliability issues of a switch, failure modes are investigated and modeled to observe the influence of these effects on the lifetime and behavior of devices.

For the improvement of the lifetime of the switches, environmental conditions, fabrication steps, materials used in the process are need to be controlled. In addition to these, actuation voltage waveforms are critical. Special equipments are needed for the generation of the desired actuation waveforms [32], [33]. For integrating the RF MEMS switches to practical applications, development of equipments for generating the desired waveforms are also necessary. One of the major contributions of this thesis is the design, implementation and development of specific equipments. Using these equipments, several actuation voltage waveforms are proposed for improving the reliability of the RF MEMS switches. In the following parts, failure mechanisms are explained in detail and charging of the dielectric layer is modeled. Moreover, for

the reducing the affects of the charging a custom circuit capable of producing specific high voltage bias waveforms is presented. In addition, relationship between the applied bias waveforms and lifetime of the devices are observed. Section 4.1 covers the common degradation and failure mechanisms of the RF MEMS devices. Section 4.2 explains the most severe failure mode, dielectric degradation, in detail. Section 4.3 presents design of a power electronic circuitry for improving dielectric degradation. Finally, Section 4.4 gives the waveforms available with constructed circuitry and measured lifetime of the switches with applied bias waveforms.

4.1. Failure Mechanisms

According to studies in the literature, identified degradation and failure mechanisms are stiction, dielectric charging, contamination, creep, fatigue and friction. These failure modes are investigated by researchers in macro scale; however in micro scale effects of most these failure modes are unknown. Stiction is mainly due to the surface interaction energies. Contamination is based on the environmental effects. Creep and fatigue is determined by the mechanical properties of the membrane. Dielectric charging is related to the applied stresses on the dielectric layer and nature of the used dielectric layer. Friction between the contacting surfaces is formed according to the materials and roughness of the materials.

Creep is the plastic deformation that continues to increase under same applied forces. Metal membranes are affected from the creep. In general, higher melting point materials are resistant to creep. In the operation of the switch, bridge material can warm up due to RF power carried on switch. According to the power level transmitted and duty cycle of the switching operation, temperature of the membrane can exceed the environmental temperature and effects of creep may become severe. Hence, care should be taken in the mechanical design of the membrane and selection

of materials used. In the micro scale structures, it is found that Al is resistant to the creep than the macro scale structures.

Fatigue is caused by the repeated stresses in the membranes. Failure introduced with fatigue starts with a crack and widens with repeated movement of the membrane. However, expected degradation in the metal membrane is in the order of billions and 100 billions is reported in the literature [34]. Creep and fatigue is the limiting factor for the reliability of the metallic membranes of RF MEMS devices and expected failures related to mechanical failures are bounded with at least billion cycles. Hence, for the failures less than billion cycles other failure mechanism should be blamed.

Stiction is the short form of the "static friction" and used for the total failure of the device. Membrane cannot be separated from the bottom plate by the restoring forces of the membrane, and hence stiction occurs. Stiction is observed after the actuation cycle. Membrane touches bottom plate and due to the surface interaction forces can not return to its original position in the removal of the external forces. Surface interaction energy opposes the restoring forces of membrane. Surface interaction energy arises from the capillary condensation, van der Waals forces, hydrogen bonding and solid bridging between the surfaces.

Capillary condensation is due to the water vapor in the environment. Water vapor tends to condense in cracks and forms a thin layer on the surface. Hence, when two surfaces touch each other, water layer presents between the two surfaces. Surface tension of the water causes capillary action. For example, some insect species or a needle can float on the water surface using the surface tension of the water. Since surface tension decreases the pressure inside the water layer, surface interaction between the plates increases. Surface tension is caused by the interaction of water molecules and molecules on the surface tries to minimize the surface area of water layer. Reducing the water environment in the environment reduces the capillary

condensation. Filling the environment with inert gases or providing a vacuum environment can enhance the lifetime of the device. Surface roughness of the surfaces affects the capillary condensation. Capillary forces on the rough surfaces are lower than the smooth surfaces. In the rough surfaces, contacting surfaces are reduced compared to the smooth surfaces and hence interaction energy between the surfaces is reduced, yielding reduced capillary forces between the surfaces.

Van der Waals forces emerge from the dipole-dipole forces of the polar molecules. Since effects of the van der Waals forces are small, compared to the capillary forces, examination in the water free environment is required. For the rough surfaces van der Waals forces are reduced and exhibit its importance in smooth surfaces. Also medium between the surfaces are important for the strength of the induced forces. Fluoro-hydrocarbon coatings are used for reducing surface interaction energies. Fluoro-hydrocarbon coatings prevent the condensation of the water vapor to the surface due to its hydrophobic nature.

Solid bridging is a problem for the soft metals. With increased pressures on the contacting surfaces, soft metals subject to plastic deformation. Atoms on the surfaces of the membranes come close to each other and do not know to which surface it belongs. Hence, solid bridging forces decreased with increased roughness.

Hydrogen bridging is also possible in the MEMS devices. Surfaces covered with materials having OH bonds, interact to each other and increase surface interaction energy. Most of the hydrophilic materials contain OH bonds and increase the affects introduced by the hydrogen bonding. These affects are also reduced with rough surfaces like previous interaction forces. However effects introduced by the hydrogen bonding is small and materials covered in this thesis does not include OH bonds, hence no further details will be presented here.

Contamination sources are important for the lifetime of the RF MEMS structures. As stated previously, water vapors highly degrade the operation and lifetime of the switches hence there should be a protective layer for the structure. In addition, residues coming from the device fabrication and packaging can stick the surfaces together. Hence, isolation of the mechanical part from the outer world is an important issue for the lifetime of the switches. Using inert gases for preventing contamination and using molecular gatherers, like Ti and Ba can reduce the contamination of the membranes.

Contact potentials have very limited effect and can be ignored. Tribocharging is contact electrification by rubbing surfaces to each other. Hence, voltage difference is induced on the surfaces. Charges induced by the friction of the plates decrease with the end of contact.

Most important of the failure mechanisms is the charging of the dielectric layers. Charge injection due to the applied stresses causes parasitic charging on dielectric interface and diffuses into the dielectric body. Also with the increment in the electric fields in the dielectric layer, charge injection becomes severe. With the charging of the dielectric, electrostatic forces generated by these charges disturb the operation of the membrane and causes stiction or reduces the influence of the external bias voltages. Dielectric charging can be reduced by the low electric fields applied to the dielectric, trap free dielectrics, leaky dielectric or total removal of the dielectric layer.

4.2. Dielectric Charging

To be able to solve the dielectric charging problem faced in the lifetime measurements of the RF MEMS devices, it is important to understand the physical reasoning behind the charging phenomenon. According to the analytical models presented in the literature, charge accumulation on the dielectric layers are

investigated and charging mechanism are reduced with the utilization of special type of actuation mechanisms.

According to the [16], parasitic charge trapped on the high-k dielectric layer, during stressing as a function of time is given by the equations:

$$n(t) = N_o q(1 - \int_0^{\infty} (\frac{\rho(\tau)}{N_o}) e^{(\frac{-t}{\tau})} d\tau) \approx qN_o(1 - e^{\frac{-t\beta}{\tau_o}}) \qquad (4\text{-}1)$$

where $n(t)$ denotes trapped charge density, N_o is total trap density, $\rho(\tau)$ is the distribution in τ, q is the elementary charge and τ_o, β are the model parameters.

Charging introduced by the applied stress can be mathematically modeled as a simple circuit [17]. Figure 4-1 demonstrates the mathematical modeling of charge trapping as a resistor capacitor circuit.

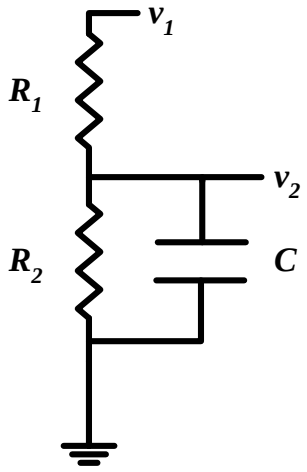

Figure 4-1: Charge trapping mechanism modeled as a resistor, capacitor circuit.

Differential equation modeling the circuit can be found as:

$$\frac{dv_2(t)}{dt} = \frac{v_1}{R_1 C} - \frac{(R_1 + R_2)}{R_1 R_2 C} v_2 \tag{4-2}$$

Solution for the equation gives v_2 as:

$$v_2(t) = v_1 \frac{R_2}{(R_1 + R_2)} [1 - e^{-\frac{(R_1+R_2)}{R_1 R_2 C} t}] \tag{4-3}$$

When we compare Equations (4-1) and (4-3), we can observe an analogy between the equations. $v_2(t)$ is the parasitic charge trapped, v_1 is multiplication of the trap density and elementary charge. When we look at Figure 4-1, one can see that there are two mechanisms affecting the parasitic charge trapping. R_1 charges the capacitance and hence models the charging time constant together with C. Also R_2 discharges the capacitance and models the discharge path of the dielectric layer. Hence, charging and discharging of the parasitic charges take place at the same time in dielectric layer. However, time constants for both charging and discharging mechanism are different. Hence, substituting the time constants, $\tau_1 = R_1 C$ and $\tau_2 = R_2 C$ in Equation (4-3) gives:

$$n(t) = N_o q \frac{\tau_2}{(\tau_1 + \tau_2)} [1 - e^{-\frac{(\tau_1+\tau_2)}{\tau_1 \tau_2 C} t}] \tag{4-4}$$

For the equilibrium condition, total trapped electric charge on the dielectric can be found as:

$$n(t \to \infty) = N_o q \frac{\tau_2}{(\tau_1 + \tau_2)} \tag{4-5}$$

For the reduction of the trapped charges in the dielectric Equation (4-5), states that total stored charge can be reduced by:

- Reducing trap density of material (N_o), hence reducing the defects of dielectric.
- Large τ_1, results in a long charging time and hence total trapped charge is small for operational life of the switch.
- Smaller τ_2, compared to τ_1 in order to increase discharging rate compared to charging rate. Hence total charge accumulated on the dielectric remains low.

For decreasing the dielectric layer reasoned failures, trap free dielectrics (low N_o) and leaky dielectrics (low τ_2) can be utilized. Moreover, time constants depend on the applied stress on dielectric. An equation relating the applied voltages and time constants are not presented, however there is a strong correlation between the applied voltages and parasitic charging of devices. Effects of the charging are observed on the lifetime of the devices and according to Goldsmith [21], lifetime of the switches are related exponentially to the applied voltages. Hence, lower electric fields applied to dielectric improve the reliability of devices.

If we investigate the effects of the charges accumulated in the dielectric layer, then we get the full picture in the parasitic charging of the switches. When we follow the methodology of Wibbler [20] and model the parasitic charges as a thin sheet of charges, total effect on the switch can be found.

Figure 4-2 shows the conventions used in the derivations of the charging effects.

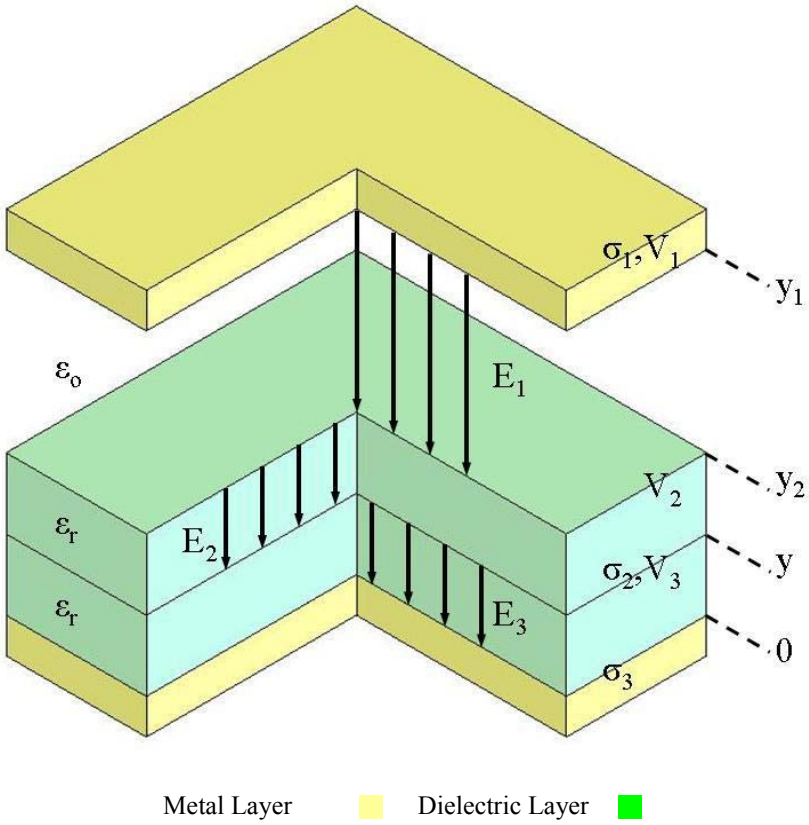

Figure 4-2: Distribution of charges and fields on a cross section of switch.

Charge on the plates and potential difference between the plates can be related to each other by:

$$E_1 = -\hat{a}_y \frac{\sigma_1}{\varepsilon_0}, E_2 = -\hat{a}_y \frac{\sigma_1}{\varepsilon_0 \varepsilon_r}, E_3 = \hat{a}_y \frac{\sigma_3}{\varepsilon_0 \varepsilon_r} \tag{4-6}$$

$$V_1 - V_2 = \frac{\sigma_1}{\varepsilon_0}(y_1 - y_2), V_2 - V_3 = \frac{\sigma_1}{\varepsilon_0 \varepsilon_r}(y_2 - y), V_3 = -\frac{\sigma_3}{\varepsilon_0 \varepsilon_r}(y) \tag{4-7}$$

$$\sigma_1 + \sigma_2 + \sigma_3 = 0 \tag{4-8}$$

$$\sigma_1 = \frac{\varepsilon_0 \varepsilon_r V_1 - y\sigma_2}{\varepsilon_r y_1 + y_2 - \varepsilon_r y_2} \tag{4-9}$$

Using Equation (4-9) and integration for the charges distributed over the dielectric and charges at the air dielectric interface results in:

$$\sigma_1 = \frac{\varepsilon_0 \varepsilon_r V_1 - y_2\sigma_i - \int_0^{y_2} y\sigma_2 dy}{\varepsilon_r y_1 + y_2 - \varepsilon_r y_2} \tag{4-10}$$

Then, let us assume a deflection of the bridge an amount of d from its original position and hence position of the membrane becomes, $y_1 - d$. Moreover, uniform charge distribution in the dielectric is assumed. Substituting in Equation (4-10) gives:

$$\sigma_1 = \frac{\varepsilon_0 \varepsilon_r V_1 - y_2\sigma_i - \frac{y_2^2}{2}\sigma_2}{\varepsilon_r (y_1 - d) + y_2 - \varepsilon_r y_2} \tag{4-11}$$

For the forces acting on the capacitor plates, Chang [31] gives:

$$F = -Q\frac{\partial V}{\partial y} = -\frac{Q^2}{2\varepsilon_o S} \tag{4-12}$$

Hence, effects of the charges on the buckling of the bridge can be related by:

$$F = -\frac{Q^2}{2\varepsilon_o S} = -\frac{S\sigma_1^2}{2\varepsilon_o} = kd \tag{4-13}$$

Total capacitance of the device after the deflections becomes:

$$C = \frac{1}{\frac{(y_1 - d - y_2)}{\varepsilon_o S} + \frac{y_2}{\varepsilon_o \varepsilon_r S}} = \frac{\varepsilon_o \varepsilon_r S}{\varepsilon_r (y_1 - d - y_2) + y_2} \qquad (4\text{-}14)$$

For a typical values of, total area of $S = 100\mu m \times 100\mu m$, dielectric thickness of $y_2 = 0.3\mu m$ and permittivity of $\varepsilon_r = 7$ and air gap of $y_1 - y_2 = 2\mu m$ capacitance according to the deflection of bridge is calculated. Figure 4-3 illustrates the variation of the total capacitance according to the movement of the top plate.

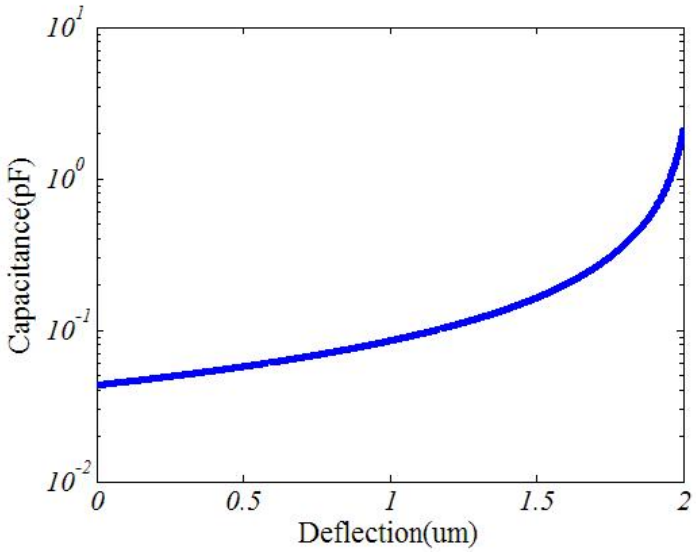

Figure 4-3: Variation on the capacitance according to the deflection of membrane.

Substituting $Q = CV$ and solving for V results in:

$$V = \frac{\sqrt{2kd\varepsilon_o S}}{C} \qquad (4\text{-}15)$$

Figure 4-4 presents the deflection for an applied voltage for the problem given in Figure 4-3 and a typical spring constant of $k = 1\ N/m$. As can be seen from the graph, there are two solutions for a given voltage value. However, physically one solution is unstable and bridge contacts with the dielectric for the deflections larger than 2/3 of air gap. Figure 4-5 illustrates the variation of the capacitance of the switch with applied voltages (graph represents the static solution). For the practical situation, capacitance obtained in the downstate of the switch differs from its theoretical value. Obtained capacitance values are in the 30% to 50% range of the expected values, due to the surface roughness of the dielectric layer.

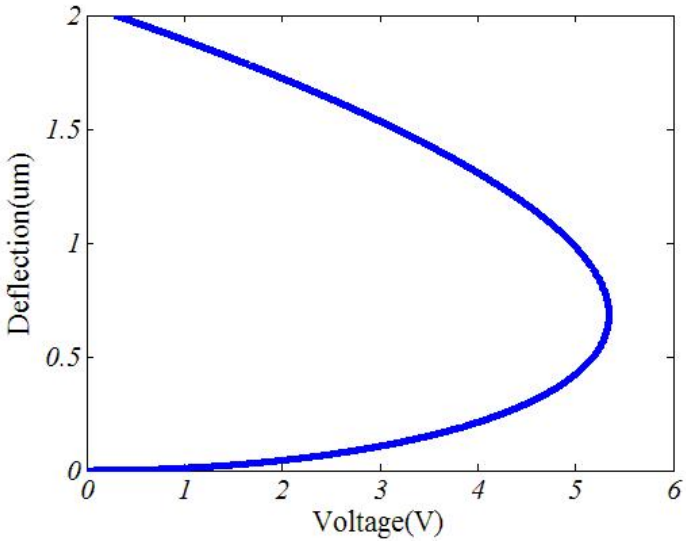

Figure 4-4: With increased applied voltages, deflection of the switch.

Failure of the devices related to the charging of the dielectric is mainly due to the shift in the C-V curve. With the injected charges, curve will deviate from its original position.

$$V = \frac{-\sqrt{2}d\varepsilon_r\sqrt{\frac{d\varepsilon_0 k}{S}} + \sqrt{2}\varepsilon_r\sqrt{\frac{d\varepsilon_0 k}{S}}(y_1 - y_2) + (\sigma_2 + \sqrt{2}\sqrt{\frac{d\varepsilon_0 k}{S}})y_2}{\varepsilon_0\varepsilon_r} \qquad (4\text{-}16)$$

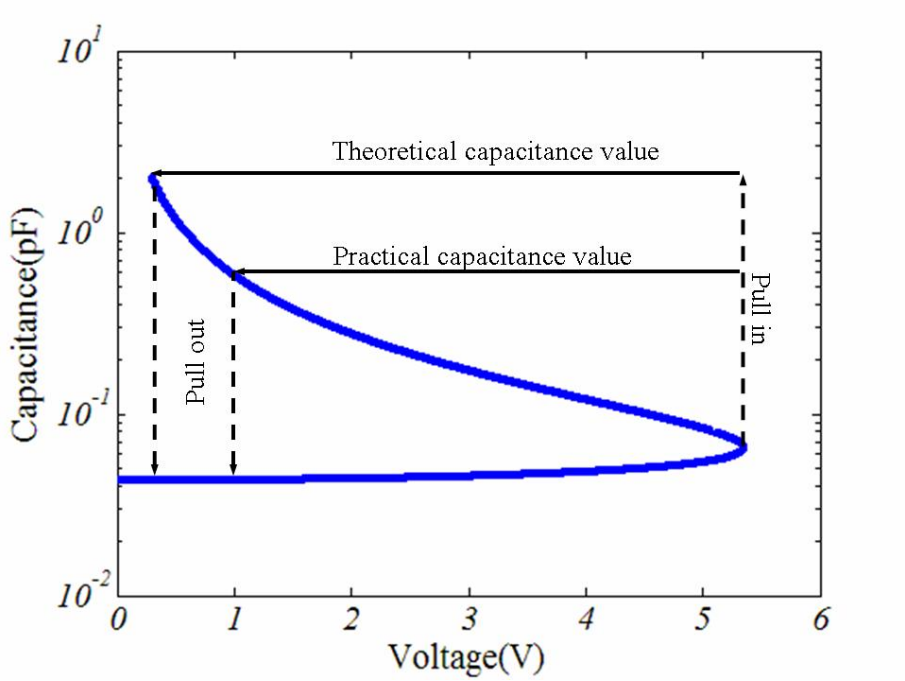

Figure 4-5: Relation of applied voltage and capacitance of the device.

Figure 4-6 shows the variation in the C-V characteristic with the increase in the parasitic charges located on the air dielectric boundary of switch. As can be seen from the graph with increase in the residual charge, a considerable shift in the C-V curve is obtained from the Equation (4-16). Also investigating the Figure 4-5, reveals that increased charge trapping can cause the malfunctioning of the switch.

With the negative pull out of the value exceeding the applied pull out voltage of the structure, switch will remain in the down state hence stiction will occur. For the reverse case, pull in value of the structure can exceed the applied bias value and

switch cannot be actuated with the applied voltage. Hence, trapped charges should be kept as small as possible.

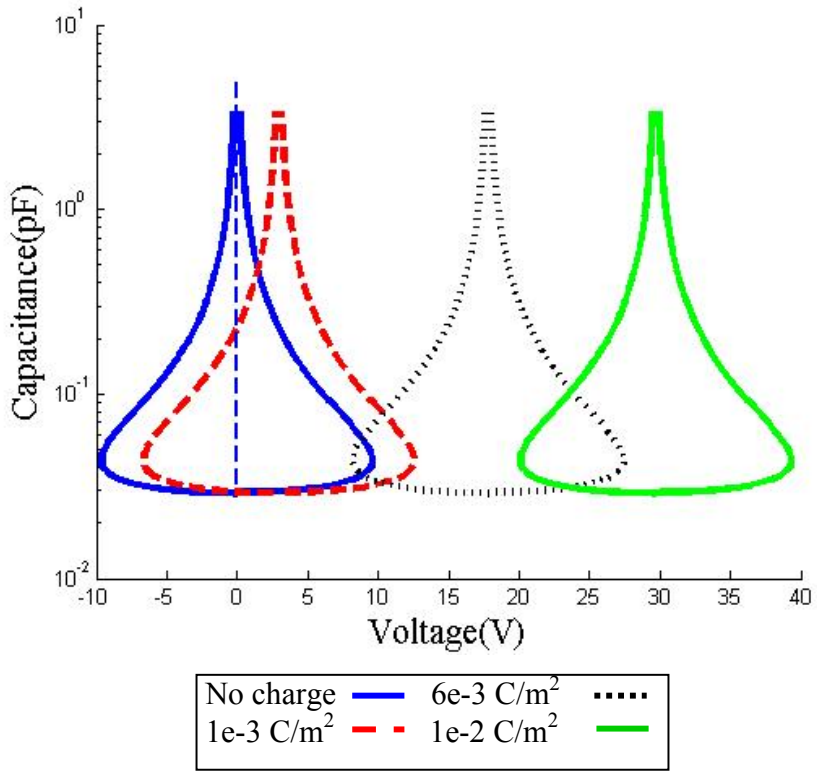

Figure 4-6: Variation of the C-V curve with increased parasitic charges.

Investigating Equation (4-4) shows that, charging depends mainly on the applied stressing duration and stress magnitude. If the switching frequency and applied field strengths are constant, failure occurs after a specific time interval. Since charge accumulated on the dielectric exceeds a specific threshold. This threshold is named as critical amount of charge and defined by Equation (4-17) [17]:

$$\sigma_{critical} = \sqrt{\frac{2\varepsilon_0 k(y_1 - y_2)}{S}}\left(\frac{\varepsilon_r 2(y_2 - y_1) + y_1}{y_1}\right) \qquad (4\text{-}17)$$

4.3. Waveshaping Bias Circuit

Using the circuit model shown in Figure 4-1, an analogy is constructed between the output of the circuit and parasitic charging in the dielectric with the Equation (4-3), in previous section. Equation (4-3) indicates that dielectric charging depends on the stressing time of the dielectric and applied stress magnitudes on the dielectric. Hence, applied voltages are directly related to the lifetime of the RF MEMS structures and a special care should be taken while biasing the devices.

Investigating Equation (4-3) reveals that, magnitude of the applied voltages determines the time constants of the charging and discharging. Moreover, polarity of the applied fields determines the polarity of the trapped charges in the dielectric layer. Hence, application of bipolar waveforms to the MEMS devices introduce both positive and negative charges and increase the recombination on the dielectric, hence total charging on the dielectric layer can be reduced. By this way, it decreases the failure rates related to the dielectric charging in the RF MEMS structure. Further improvements can be achieved with lower field stresses on the dielectric.

Bipolar forms applied to the MEMS devices can cause problems in the transients of the bias waveform. Since MEMS requires high biasing waveforms for the closed state of the bridge, membrane can return to its original position during the transients of the bias waveform. Hence, for the proper operation of the switch, transients should be kept as small as possible. Transition from low to high bias voltage should be lower than the mechanical response time of the membrane and hence, circuits capable of providing sub-microsecond transient times are required. Also, circuit should be capable of actuating different types of RF MEMS structure, hence application of the high voltage magnitudes are necessary for variety of the applications. Moreover, since further improvements can be obtained with the lower stresses applied on dielectric, application of lower voltages should be possible during the actuation of the devices.

In order to fulfill the specifications given, a custom power electronic circuit, designed for the actuation of RF MEMS circuit is constructed. This section focuses on the design and realization of the circuit and with the applied intelligent waveforms, improvements on the lifetime of RF MEMS devices.

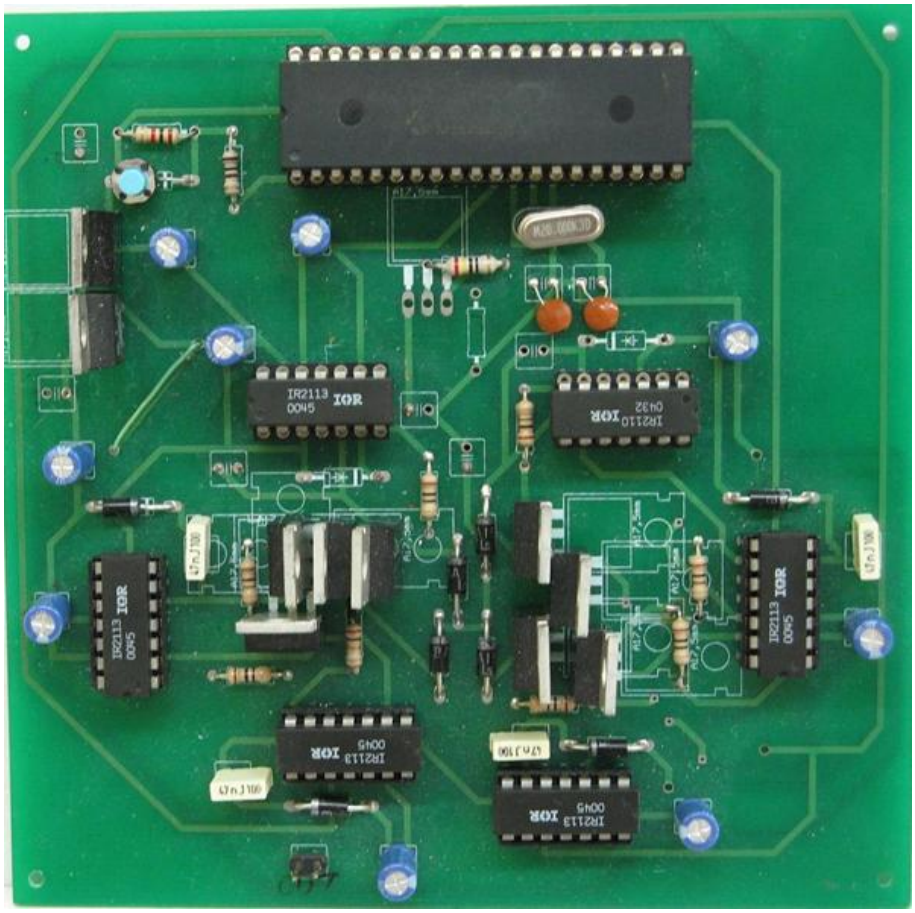

Figure 4-7: Constructed power electronic circuitry.

To be able to get more familiar with the power electronics terms, several modules used for the construction of the circuit are explained in detail in following sections [35].

4.3.1. Power MOSFET

Power MOSFET is a specific type of MOSFET, used for handling high currents and voltages. Main advantage compared to other semiconductor switches is the high switching speed of the device, which is crucial for biasing of MEMS applications. Most of the power MOSFET devices have a switching time in the range of a few tens of nanoseconds to few hundred nanoseconds. In power applications, switches are used for routing the power flow to load.

Operation is the same for the usual MOSFET devices. Transistor is in cutoff, when the gate voltage is below a certain threshold voltage and behaves like an open circuit between the drain and source terminals. During the off state of the transistor, it should be able to withstand the voltage applied between the terminals. Hence, transistors should be selected according to the breakdown specifications of circuit. In the linear region, transistor is turned on with applied gate to source voltage (V_{GS}) above its threshold value. Power dissipation can be reduced due to the lower drain to source voltage (V_{DS}) in linear region. In the active (saturation) region of the device current is independent of the V_{DS} related to the V_{GS}.

Voltage rating of the MOSFET should not be exceeded during operation. Gate oxide layer determines the break down voltage of V_{GS}. Typical values for the breakdown of gate oxide are 20-30V. V_{DSmax} is determined by the doping concentration of the drain drift region. Using lightly doped drain drift regions results in higher break down voltages. V_{DSmax} is the avalanche breakdown voltage of the reverse diode between the drain and body junction.

4.3.2. Gate Driver

Main function of the gate driver circuit is establishing communication between the control circuitry and power switch. Hence, it should switch the states of the power switch from on to off and off to on. Usually faster turn on and turn off times are desired due to the higher power consumption. During the turn on and turn of the power switches, transistor enters the active region where power consumption is high and hence faster transitions are desired for reduced power consumption on the switch. Also for the MEMS applications lower transition times are required. In the on state of the switches, driver has to maintain the required power to sustain the on state of the switch. For the off state of the power switch, driver has to provide the negative voltage levels for maintaining off state of the switch. Moreover, negative bias can be applied for further improving the transition times.

Gate drivers are the interfaces between the logic circuits controlling the timing of circuit and power switches. Since control circuits generate low power and low voltage, which is insufficient for the control of the power switch, driver has to amplify the incoming signal. Moreover, some applications require electrical isolation between the control circuits and power switches and hence driver should isolate its input for the output.

Topologies used for the design of the driver circuits, depends on the functional characteristics of the circuit. Output forms of the driver circuit, coupling of the signals are the main factors for the determination of the circuit topology. Unipolar output gate drivers are simpler; however, bipolar output gate drivers are complex but offers faster transition times compared to unipolar case. For the isolated drives, isolated supplies are required. Also for the protection against excessive currents, modifications can be added to the driver circuit. In bridge circuits, blanking time is required for safer operation of the power switches. In generally speaking, faster

switching times increases the complexity of the designs, power consumption and requires additional power supplies.

Types of the drive circuits can be summarized as follows:

4.3.2.1. DC coupled drive circuits

For the higher frequency of operations, power switches should be turned on and off at higher speeds. Hence, design of the driver circuits should enable the faster switching of the power switches. Unipolar output driver circuits are slower than the bipolar output driver circuits and hence avoided in the high-speed driving circuits. Hence, for providing faster turn off times, negative bias is required and driver should be compatible with bipolar output. Additional negative supplies are required for the bipolar outputs of the drivers. For a BJT power switch, antisaturation diodes are placed between the base and collector terminals of the transistor. Hence, diode prevents the deep saturation of the BJT transistor and hence it operates in slightly above its saturation value.

4.3.2.2. Electrically isolated drive circuits

Commonly, isolation is required between the controlling circuits and power switches. Widely used tools for isolating the two circuits from each other are optocouplers, fiber optics and transformers. Optocoupler uses light for establishing communication between the circuits. Optocoupler utilizes a light emitting diode (LED), output transistor and a Schmitt trigger as the circuitry. Signal coming from the control circuit turns on the LED and light is focused on the base of the output transistor. Light generates electron hole pairs in the light sensitive base of the output transistor and hence transistor turns on. Collector voltage drops and Schmitt trigger alters its state. Output of the Schmitt trigger is connected to the input of the power transistor

and controls the operation of the device. For further reduction of coupling between the input output ports of the optocoupler, fiber optic cables are used. Transformers are used in the higher frequencies and duty cycles close to 50%, due to the saturation of the core. In order to transmit lower frequencies, control signal modulated with higher frequencies can be transmitted over the transformer. Modulation technique enables the use of the smaller transistors and hence cheaper and introduce lower stray capacitances.

4.3.2.3. Cascode connected drive circuits

Previous drive circuit configurations are connected in shunt to the power switches. Hence, only a small portion of the current flow over the drive circuit. For the cascode topology, same current flows over the drive circuit. As an example, MOS devices have fast transitions however suffer from the lower breakdown voltages. Cascode connecting with a BJT type transistor enhance the break down characteristic due to the increased breakdown voltage of the BJT and provides faster transition due to the nature of the MOS device.

4.3.2.4. Thyristor drive circuits

Control is maintained with a short current pulse applied to the gate of the tyhristor. Once thyristor is opened, it resumes the operation due to the regenerative action of device. Limits for the magnitude of firing current is specified by maximum and minimum curves in datasheets. Thyristors are usually used in the line-frequency converters, where thyristors are naturally closed by line voltage.

In the bridge circuits blanking times should be provided for preventing cross conduction. In the half bridge and full bridge circuits, power switches are connected in cascade to form an inverter leg. Blanking time is required to delay the turn on

time of the power switch, according to the turn off time of the other switch in the inverter leg. Timing is selected according to the maximum possible storage time of the switches to avoid cross conduction.

4.3.3. Inverter

A converter is the basic module of the power electronics systems. Inverter refers to the converter when the average power flow is from DC to AC side, and rectifier refers to a converter when the average power flow is from the AC to DC side. Inverts are the basic building block of the circuit given in Figure 4-7.

4.3.3.1. Pulse Width Modulated Inverters

Switch mode inverters are used in the AC motor drives and single phase UPS. Their function is to provide a sinusoidal output and control the phase and magnitude. Magnitude and frequency are controlled by means of pulse-width modulation (PWM) of the power switches. Hence, inverters using PWM are called, PWM inverters.

4.3.3.2. Square Wave Inverters

For the square wave inverters, magnitude of the output waveform cannot be controlled. For the magnitude control, input DC has to be controlled by other mechanisms. The circuit is only capable of controlling the frequency of the output waveform. Since, waveforms like square wave are generated at the output; these types of inverters are called square wave inverters.

Figure 4-8 illustrates the one leg inverter topology. For the square wave inverters, power switches in the inverters legs are in conduction for 180° of the operating frequency. Since opening both power switches at the same time results in a short circuit of the voltage source. Hence, for the power switches, there are only two definite states. Square wave inverters are used for reducing losses during the switching, since power switches are switched only twice in one cycle. For the high power applications, power switches have slow turn on, turn off times, and power loss on the switches is considerably high. Main disadvantage of the square wave inverters is the lack of regulation of the output waveform magnitude.

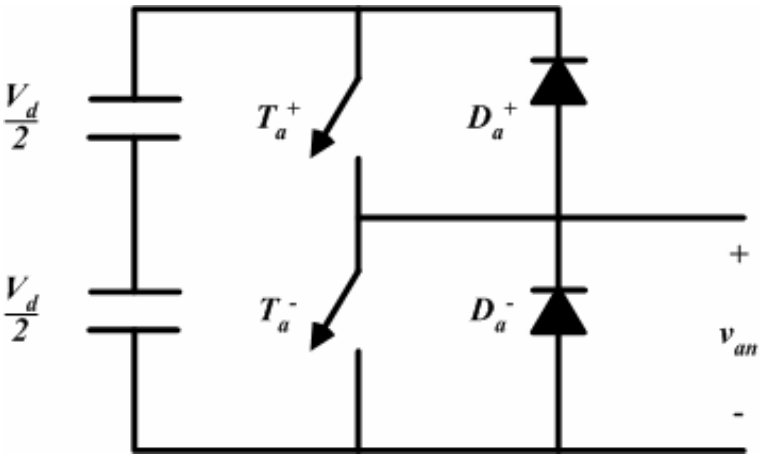

Figure 4-8: One leg switch mode inverter.

4.3.3.3. Single Phase Inverters with Voltage Cancellation

These types of inverters combine the properties of the pulse width modulated inverters and square wave inverters. For the single-phase outputs, magnitude and frequency is controlled by square waves.

4.3.3.4. Bridge Inverters

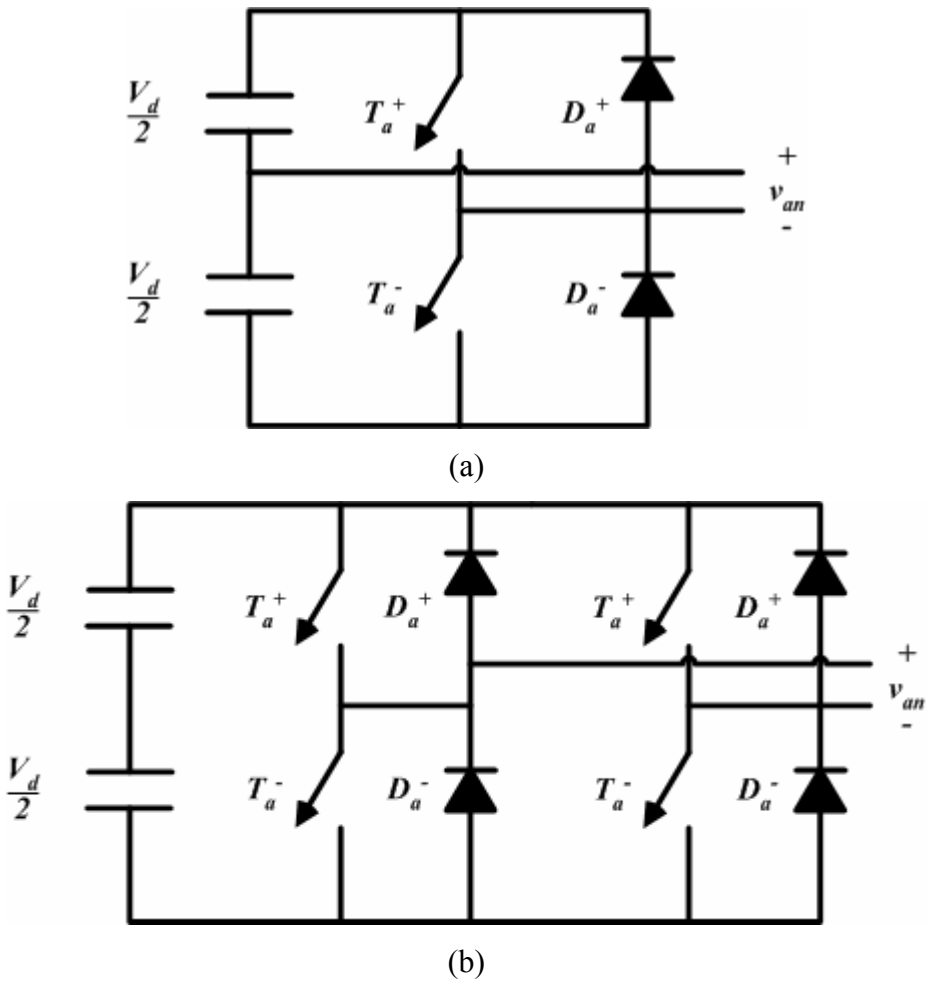

Figure 4-9: Inverter topologies (a) Half bridge inverter, and (b) Full bridge inverter.

Figure 4-9 shows the power topology of half and full bridge inverters. Half bridge inverter consists of one 'one leg' inverter and has lower power rating. Full bridge inverter consists of two 'one leg' inverters and has higher power rating, since voltage output of the full bridge inverter is the twice of the half bridge inverter. Second leg of the inverter provides a neutral point to the load. Hence for the same output power, current reduces to half of the previous arrangement and requires less paralleling of

power switches. Output of the full bridge inverter is the four combinations of the switch states and corresponding voltage levels. In order to prevent any possible short circuit across the supply, control unit should verify that either of power switches on the same leg of the inverter is closed.

4.3.3.5. Multilevel Bridge Inverters

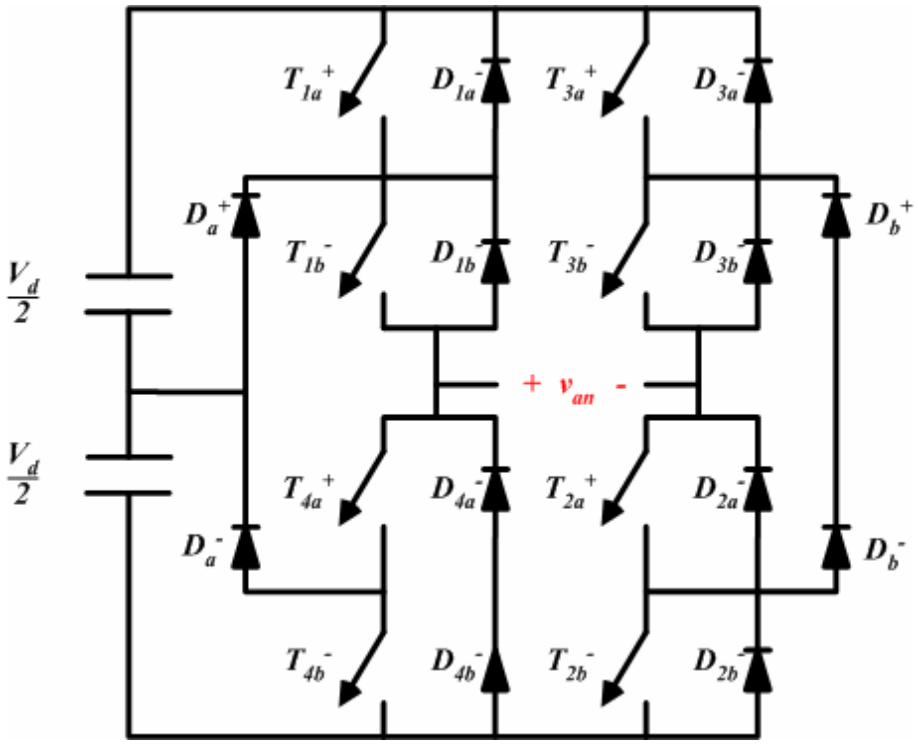

Figure 4-10: Multilevel, two phase bridge inverter.

In the bridge inverters, output of 'one leg' is either $\frac{V_d}{2}$, or $-\frac{V_d}{2}$, hence output can take only two values [36]. In the multilevel topologies, N level output is possible [37]. For the 3 level topology, $\frac{V_d}{2}$, 0 or $-\frac{V_d}{2}$ is possible at the output. With

parallel combination of the legs and valid switch states, multilevel signals at the output are possible. Figure 4-10 illustrates the power topology of the three levels, two-phase bridge inverter.

Not all of the switches can be open on the same leg, which will lead to a short circuit of the supply. Also, a detailed analysis shows that T_{1a} and T_{4a} operates in a complementary manner and the same is true for T_{1b} and T_{4b}. In Figure 4-10, two legs are shown. Legs have the very same switch configuration and hence their switch states are the same. However, since they are connected in parallel, operation is independent for each leg section.

4.3.4. Snubber Circuits

For the power electronic converters, stress on the components can be reduced by two different ways. One way is to replace the components with the ones having higher ratings. The other is the usage of snubber circuits. Final choice depends on the cost and availability of the higher rating components and cost and complexity of the snubber circuit. The use of the snubber circuit provides reduced electrical stresses on the power switches during the switching of the components. Common ways of reducing electrical stresses on the device are:

- Limiting the voltage on device during turn off transients
- Limiting the current on device during turn off transients
- Limiting the $\frac{di}{dt}$ on device during turn on transients
- Limiting the $\frac{dv}{dt}$ on device during turn off transients

There are three class of snubber circuits used widely on power electronics:

Un-polarized series R/C snubber circuits: used to limit the maximum voltage and $\frac{dv}{dt}$ on device during reverse bias of the diodes and thyristors.

Polarized R/C snubber circuits: used to control turn off portion of switching and to clamp voltages applied or limit $\frac{dv}{dt}$ rating during turn off.

Polarized L/R snubber circuits: used to control turn on switching and to limit $\frac{di}{dt}$ rating during turn on.

Snubber circuits are not a fundamental part of the converter; hence advantages of the snubbers should be compatible with the cost and complexity of the design.

4.3.5. Finalized Design

Based on the explanations above, a custom high voltage waveform generator circuit is designed with the use of multilevel bridge topology, commercially available gate drivers used in conjunction with optically isolated gate drivers, power HEXFET transistors and a simple snubber circuit. Figure 4-11 illustrates the photograph of the wave shaping circuit. In the appendice, layout of the constructed circuit is given.

Multilevel bridge circuit is used for the generation of multilevel actuation forms. Multilevel waves are required for providing actuation and hold down voltage to the RF MEMS switches. Hence, three-level inverter topology is used in the wave shaping circuit design [38]. Output of the 'one leg' inverter can provide 0, V_{s1} or $V_{s1}+V_{s2}$ to the output, V_{s1} and V_{s2} being the isolated voltage supplies. Moreover, for decreasing the parasitic charging due to the charge injection into the dielectric, bipolar waves are necessary. Hence second inverter leg is needed for providing negative bias levels to the output. Isolated supplies are required due to the second inverter leg, since bipolar wave shape is generated by connecting the input supplies

to the ground terminal of the load. Therefore, second leg provides the neutral point to load.

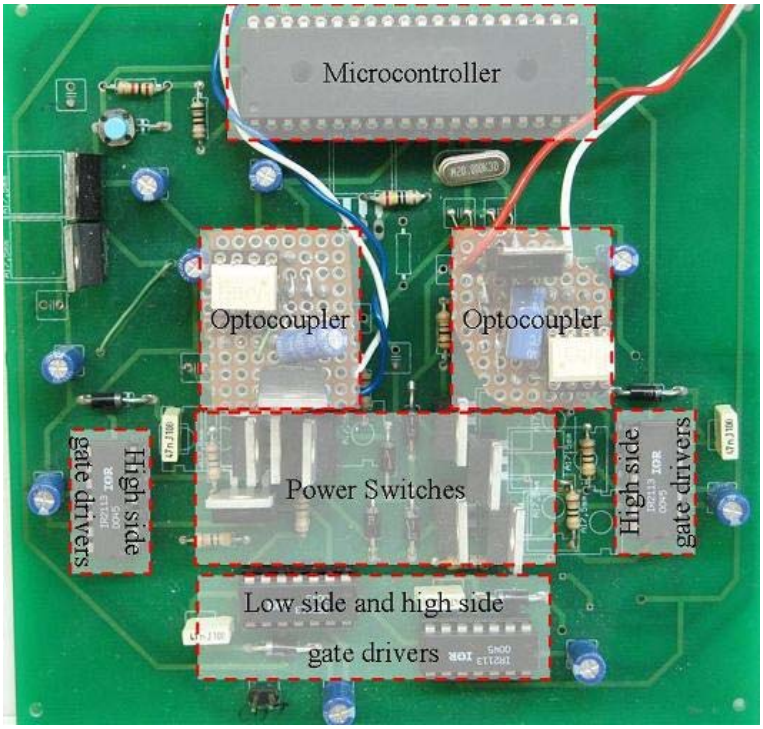

Figure 4-11: Component layout of the finalized waveshaping circuit.

For the design of the gate drivers, speed is the primary concern. In order to switch in a fast and reliable manner, commercial gate drivers are used. Gate drivers selected from the website of the IRF[3] and IR2113 is used due to availability of the component. IR 2113 is a MOS driving circuit owing independent high and low side drivers [39]. Voltage is limited by 600 V, which is far above the targeted 200V value. Final circuit is constructed on a custom PCB and 14 pin DIP package type of driver is used. Current output of the driver circuit is up to 2000mA which is not

[3] International Rectifier

necessary for driving MOSFET devices however high current values ensures the fast operation of the multilevel bridge circuit. Output voltage of the independent drivers are in the 10-20 V range and sufficient for the control of the power switches.

A single gate driver is used for the control of the T_{4a} and T_{4b}, high and low sides respectively. For the rest of the switches on the same leg, high side drivers are required. In the initial design, high side driver of the same component is used for the ease of the design. However, circuit is not functional since, high side driver requires the potential of source terminal to be less than 6 V. Hence, this topology is modified with electrically isolated gate drivers. For the control of the T_{1a} isolated gate drivers are used. However, functionality of the device comes with an expense of the one isolated voltage source for each leg of the inverter and slower operation of the power switches. Therefore, additional two isolated supplies are required. Circuit used for the biasing IR2113 is same as given in the datasheet and will not be presented here. Figure 4-12 presents the electrically isolated optocoupler driver, constructed using TLP 521. Output of the circuit can be up to 9.6 V at 200 kHz, which is sufficiently high for turning on the power switches.

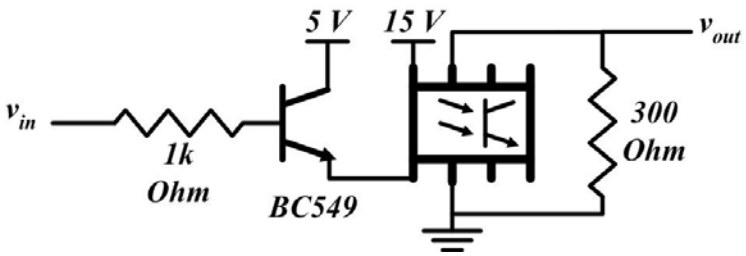

Figure 4-12: Optocoupler driver circuit.

For the power switches, discrete HEXFET power MOSFET's are used. Components are selected from the website of IRF and according to the availability of the

component in market. IRF 630 is selected for the low turn on and turn off durations [40]. N-type transistors offer 9.5 Amps drain current which is sufficiently high for a RF MEMS application, moreover suitable for the system integration of the MEMS components, which is presented in next chapter.

In addition, for the reduction of the ripples at the output, polarized RC snubber is placed in the circuit. Snubber resistance is very small and placed in series with the gate of the power switch. Component value is optimized on a separate PCB and used in the final circuit. 10 Ω is the used value for snubber resistance. A separate capacitor is not used and gate capacitances of the power switches are used. Snubber circuit limits the $\frac{dv}{dt}$ rating during turn off and reduces the ripples at the output waveform. Also in the layout drawing of the circuit, placements of the power switches are crucial for the ripple generation. Since increased line length in the power line induces parasitic inductances, variations in the currents produce voltage ripples at the output. Hence, for reduced ripple values, line lengths between the power switches should be minimized. Figure 4-13 illustrates the schematic of the finalized high voltage waveform generator circuit.

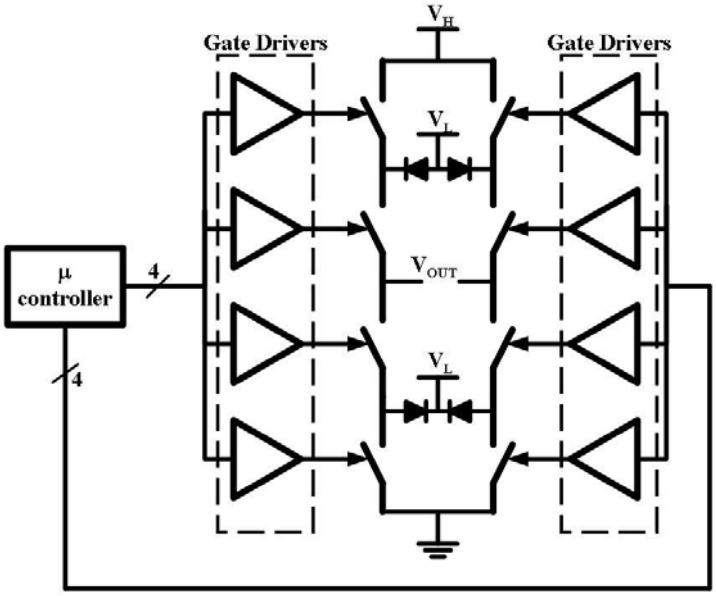

Figure 4-13: Simplified schematic of the high voltage waveform generator circuit.

4.4. Available Waveforms and Corresponding Lifetimes

For the control and synchronization of the power switches, a PIC16F877 microcontroller is utilized. With proper programming the microcontroller, desired waveforms can be obtained.

However, objective of the circuit is to reduce the dielectric charging and hence increase the lifetime of the RF MEMS devices. Hence, available waveforms used for the actuation of the MEMS devices, will be presented in this part. Figure 4-14 illustrates a sample biasing waveform generated, using the custom circuit. Rise and fall times of the waveform are smaller than 100 nsec and hence can be used in the switching time measurements and biasing of MEMS components.

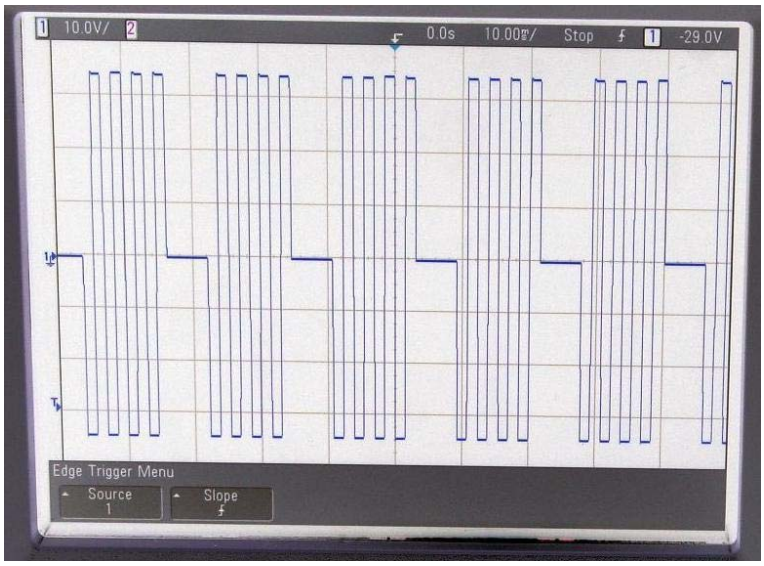

Figure 4-14: A sample output from the waveshaping bias circuit.

4.4.1. DC Bias

For the biasing of the RF MEMS devices, direct DC can be applied to the devices. Magnitude of the applied bias should be higher than the actuation voltage of the switch. Hence, device will experience maximum charge accumulation on dielectric. As explained in part 4.3, RF MEMS device will fail to operate after a certain time. Failure condition is defined as any visible degradation at the output response of the switch. Therefore, 5 mV degradation at the switch response is stated as failure. Most of the 'failed' switches are operational with certain degradation at their responses. Using the setup presented in Figure 2-16, degradation in the dielectric is observed on type B1 switches.

Initial measurements show that, for the applied DC bias to a capacitive RF MEMS switch, degradation is observed within 6-7 secs for an applied voltage of 12 V. Failure is sensed by the output power of diode detector. Due to the decreased

capacitance of the RF MEMS device, input power of diode increases, hence applied bias voltage is not sufficient to overcome the stored charges and switch fails. Early degradation due to the charge trapping in the dielectric is most probably related to the trap density of the material (N_o) and charge injection rate to the dielectric (τ_1). Figure 4-15 (a) illustrates the applied DC bias waveforms. The actual waveforms observed on an oscilloscope are given in appendice.

4.4.2. Uni-level DC Bias

For reducing the accumulated charges in dielectric, bias on the dielectric can be applied for a certain period. If the period of the relief state exceeds the mechanical response time of the switch, membrane can return to upstate and observing the difference at the output value failure of the device can be spotted. With the applied uni-level DC bias to the RF MEMS device, actual aim is to increase the discharging time of the dielectric. Hence trapped charges on the dielectric, recombines in the meantime. Figure 4-15 (b) illustrates the applied uni-level DC bias waveform. For this configuration, down time is equal to the charging time for the dielectric and up time increases the discharging time of dielectric. For a duty cycle of 50%, effective discharge time constant is half of the DC bias case. Degradation occurs at 35 seconds for an applied voltage of 15 V and 8120 switching of membrane.

4.4.3. Uni-level Pulsating DC Bias

Charging time can be further decreased by the pulsating the applied bias waveform above the mechanical response time of the membrane. Hence charging time of the dielectric can be decreased, moreover discharging time can be increased for the same switching period. For a switching duty cycle of 50% and pulsating duty cycle of 50%, effective discharge time constant is the one fourth of the DC bias case.

Degradation for this type of switching occurs at 45 seconds for an applied voltage of 17 V and 10440 switching. Figure 4-15 (c) illustrates the applied uni-level pulsating DC bias waveform.

4.4.4. Bi-level DC Bias

Applying a DC bias larger than the pull down voltage of the device for a sufficient time to enable actuation of device and reducing to the pull down voltage after the actuation is called as bi-level DC bias. Since time constants of the dielectric material depend to the stresses applied over the materials, reduced stresses applied will improve the lifetime of the device. However, for the actuation of the device, initially applied voltage magnitude definitely exceeds the pull down voltage of the switch, which is the same case in the DC bias. However, hold down voltage of the devices is smaller than the actuation voltage of the device. Hence, reduction of the bias voltage reduces the charge injection rate to the dielectric and expected lifetime of the device increases. Figure 4-15 (d) illustrates the applied bi-level DC bias waveform. In the full cycle of the applied bias waveform up and down durations are same for uni-level DC bias case. Degradation occurs at 60 seconds for an applied pull down voltage of $V_2 = 15.5\,\mathrm{V}$ and hold down voltage of $V_1 = 12$ V and 8280 switching.

4.4.5. Bi-level Pulsating DC Bias

Same convention used in the uni-level pulsating DC bias can be used for improving the bi-level DC bias. Hence, time constant for discharging reduced to the half of the previous configuration. Degradation occurs at 70 seconds for an applied pull down voltage of $V_2 = 19\,\mathrm{V}$ and hold down voltage of $V_1 = 16$ V and 9660 switching.

Up to now uni-polar wave are applied and effects on the lifetime of the RF MEMS devices are observed. With DC bias, switch degrades only at 7 seconds, which indicates a poor dielectric material. With the improved bias waveforms, devices can withstand the applied electrical stresses at most by 70 seconds, which is not sufficient for a product. Uni-polar waveforms can be used for observing the progressive charge accumulation on the dielectric since positive charges injected to the dielectric and only discharging mechanism is the recombination of parasitic charge.

4.4.6. Bi-polar, Uni-level DC Bias

For decreasing effect of the accumulated charges in dielectric, negative charge can also be injected to the dielectric by applying negative bias voltages. Also by this way, recombination rate can be increased due to increased number of positive and negative charges in the dielectric. Hence, total electric field can be compensated with opposite charges. In the case of uni-polar biasing, simplest case of bi-polar waveform generation is the bi-polar, unilevel DC biasing. In every switching cycle, polarity of the applied bias is reversed. Also for analogy between the uni-level DC bias applied voltage kept constant during the down state of the switch only in the next cycle polarity is reversed. Figure 4-16 (a) demonstrates the bi-polar, unilevel actuation waveform. Degradation occurs at 2 hours 46 minutes for an applied voltage of $V_2 = 13.6\,\mathrm{V}$ and 8.6×10^6 switching.

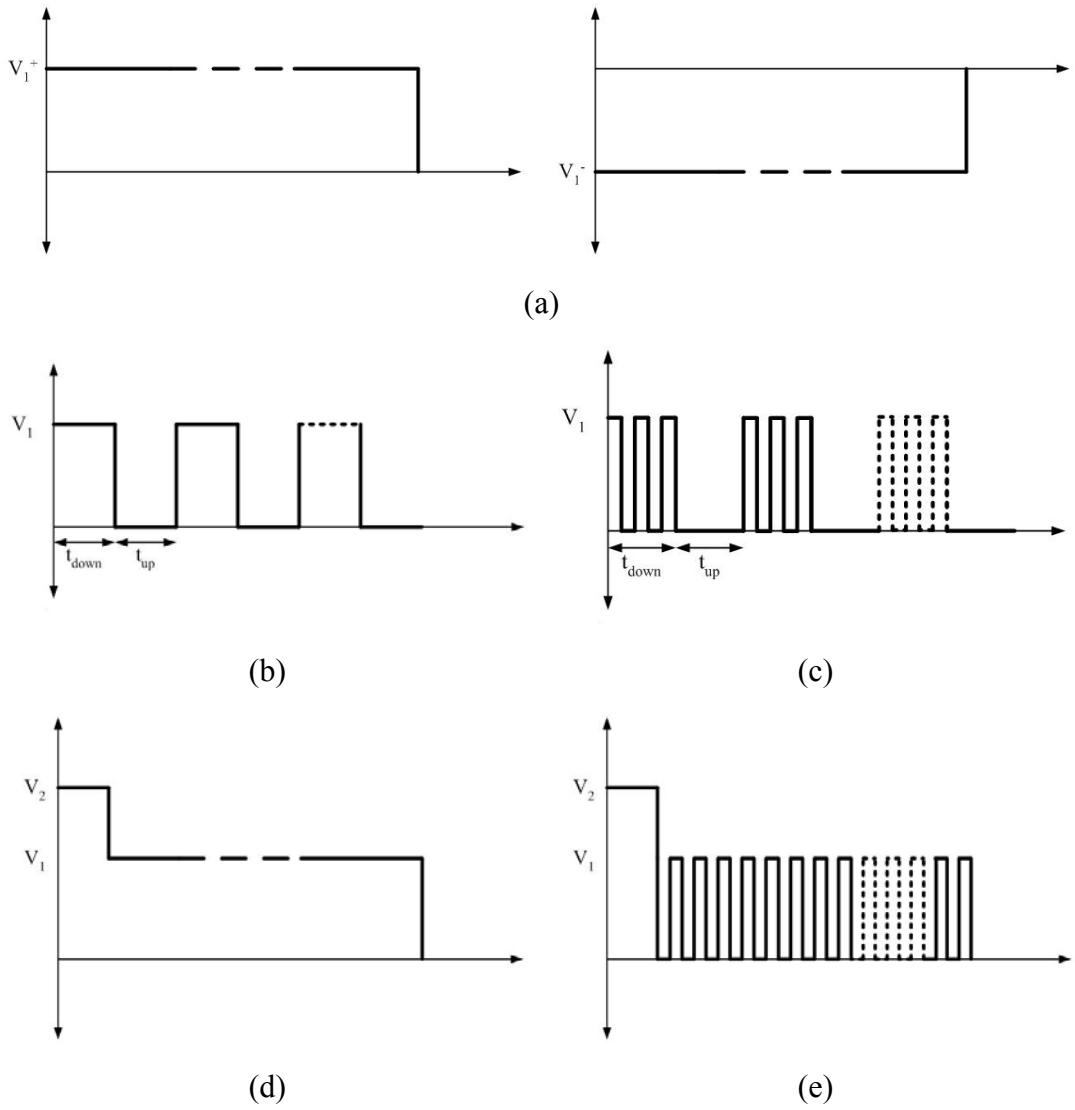

Figure 4-15: Uni-polar output waveforms. (a) DC bias, (b) Uni-level DC bias, (c) Pulsating uni-level DC bias, (d) Bi-level DC bias, and (e) Pulsating bi-level DC bias.

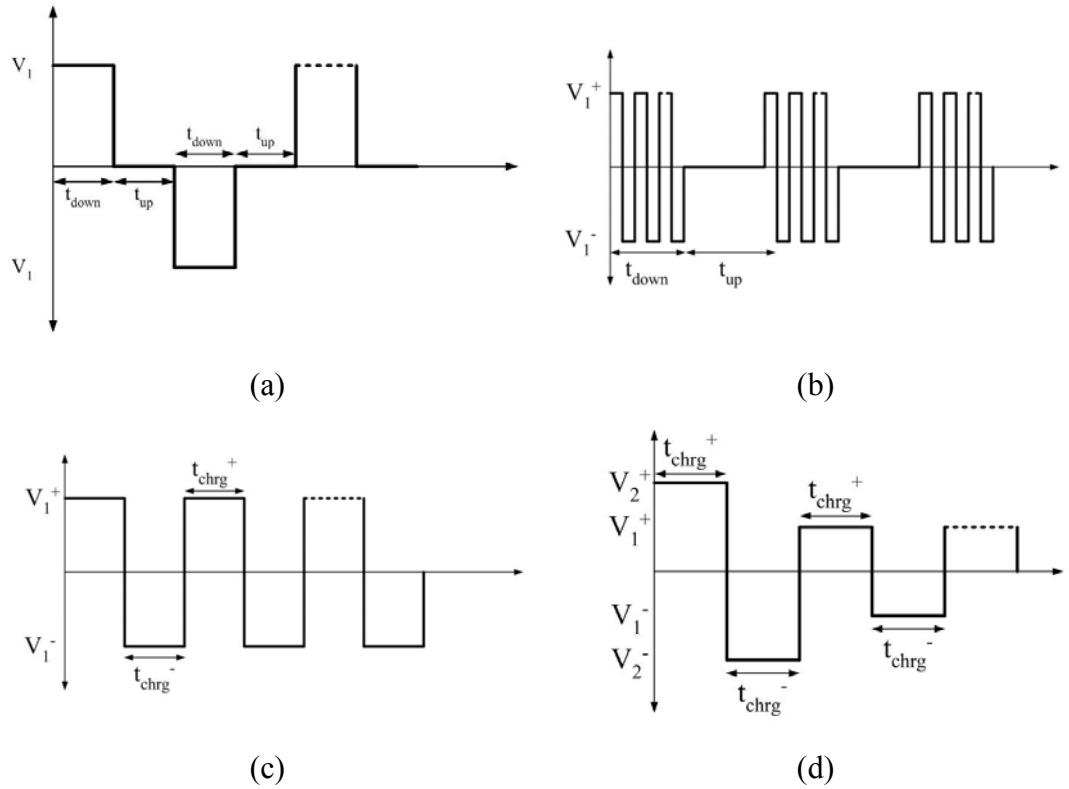

Figure 4-16: Bi-polar output waveforms. (a) Bi-polar uni-level DC bias, (b) Bi-polar pulsating Uni-level DC bias, (c) Switch down duration of bi-polar pulsating uni-level DC bias, and (d) Switch down duration of bi-polar pulsating bi-level DC bias.

4.4.7. Bi-polar, Pulsating Uni-level DC Bias

In the case of the bi-polar uni-level DC bias, charge is accumulated in dielectric during the down time of the membrane. Since actuation voltage is constant during the actuation, only positive or negative charges accumulate on the dielectric and give rise to failure of the device after certain duration. In order to decrease the total charge accumulated in dielectric during the actuation of the device, small duration bias pulses of the reverse magnitude is applied for the actuation of the device.

Hence, accumulation of the parasitic charge during one positive charging period compensated with negative charging period. By this way, overall charging can be reduced. Removing the bias results in the upstate of the device. Failure is observed when the device cannot return its original position hence in the up state. However, during the actuation, downstate of the membrane is very reliable and does not fail. Figure 4-16 (b) shows the membrane up and down durations for bipolar uni-level pulsating DC bias and Figure 4-16 (c) illustrates corresponding positive and negative charging during the down state of the membrane. Degradation occurs around 25 hours and 42 minutes for an applied voltage of $V_2 = 13.5\,\mathrm{V}$ and 8×10^7 switching.

4.4.8. Bi-polar, Pulsating Bi-level DC Bias

As in the case of Bi-level DC bias, hold down voltage can be applied to the switch after actuation of the membrane. By utilization of two different magnitudes in same waveform, lifetime of the device can be further increased. Hence applying a short pulse of high voltage for actuating the membrane and reducing the applied voltage to the hold down voltage can improve the lifetime of the devices. For the compensation of the injected charges during the initial actuation, a negative pulse of the same magnitude is also applied to switch. Figure 4-16 (d) illustrates corresponding positive and negative charging during the down state of the membrane. Degradation occurs around 28 hours and 30 minutes for an applied pull down voltage of $V_2 = 12.5\,\mathrm{V}$ and hold down voltage of $V_1 = 9.5$ and 9×10^7 switching.

With improved actuation waveform schemes and utilization of the bi-polar waveforms, lifetime of switch is increased up to 28 hours and 30 minutes for a specific type of switch in an uncontrolled environment. Bias card improved the lifetime of the same device from 7 seconds to 28 hours and 30 minutes, corresponds to a 10k improvement. However, specified lifetime is not sufficient for an industrial application since switch can withstand the bias bit more than a day. Some

applications may require a lifetime of a decade; therefore, additional improvements are necessary for the reliability of the devices.

Table 4-1: Switching lifetime measurements of type A1 capacitive switch according to applied bias type.

Bias Type	*Applied Voltage* (V)	*Duration* (sec)	*# of cycles* (#)
DC	12	6-7	-
Unilevel	15	35	8120
Unilevel pulsating	17	45	104440
Bilevel	15.2-12	60	8280
Bilevel pulsating	19-16	70	9960
Bipolar	13.6	2 h 46 min	8.6×10^{6}
Bipolar pulsating unilevel	13.5	25 h 42 min	8×10^{7}
Bipolar pulsating bilevel	12.5-9.5	28 h 30 min	9×10^{7}

As explained in the Chapter 4, lifetime of the switch is not related to the number of cycles of the switch. Hence, with increasing the switching frequency of the applied bias waveform, total number of cycles can be increased. The lifetime of the switch is related to the 'down' time and electrical field stresses on the dielectric layer. In addition, reducing the duty cycle may improve the total number of cycles.

Further improvement can be achieved with the use of controlled environment and removing the humidity of the environment. In addition, presence of the inert gases can improve the behavior of the device by reducing the oxidation or any other chemical reaction of the materials used in the process like copper or aluminum, with

the ambient air. Equipments ordered for proper measurements at controlled environment.

4.5. Summary

In this section, common failure and degradation modes affecting the MEMS components are identified. From the studies presented in the literature, effects of failure modes on the MEMS devices are presented and possible improvement modes are proposed. Creep and fatigue is observed on the structural layer of the MEMS devices. For the lower creep on the structural layer, materials with higher melting points should be selected. Stiction and surface interaction energy concepts are studied and related to the material and environmental conditions, like humidity. Humidity degrades the performance of the device and is responsible from the increased surface interaction forces. In most of the electrostatic actuated switches, actuation electrodes are designed to be large, in order to decrease the actuation voltage of the switch. Hence, even low humidity can degrade the performance of the membrane and should be avoided in the final product. Dielectric charging, which is one of the most effective failure mode, is investigated in detail. According to the literature survey on the dielectric charging, degradation mechanisms are identified. Effect of the charging on the dielectric is presented by an equation and solution to this equation is modeled as a simple RC circuit. Possible improvement methods are presented to reduce dielectric charging. Moreover, degradation related to the charging is modeled and variation on the behavior is identified. From the mechanical models, formulations relating capacitance, applied DC voltage and deflection are derived. According to the degradation model for the dielectric, a power electronic circuitry is proposed and designed. Components and circuit topologies are optimized for the improved circuit performance. Finally, lifetimes of the devices are measured using the finalized power electronic circuitry, in an uncontrolled environment. It is found that bipolar actuation is crucial for the RF

MEMS components designed in METU and up to 9×10^7 cycle operational lifetime is possible with the bipolar, bilevel, pulsating actuation waveforms. The highest value of switching cycles is reported as 100×10^9 which corresponds to about 19 days of operation [41]. As it is noted before, the total down time is a significant factor determining the life-time of the switch. Therefore, the comparison of the lifetime of our switch with that of the reported best one shows that there is about a factor of 20 (28 hrs versus 19 days). In a controlled measurement environment, this factor can be reduced. Lifetime can be increased with the controlled environment like vacuum, inert gas or humud free environment. Furthermore, effect of the applied stress magnitude on the lifetime of the switches has been investigated. In addition, from model, it is found that, the major factor affecting the lifetime of the RF MEMS devices are not the number of cycles, but the total down time of the switch. Lifetime of the RF MEMS devices is challenging and further investigation on the physical structure of the dielectric and the environmental stressing conditions is required. Contamination coming from the environment and processing stage should be reduced for the increased yield and the lifetime of the devices. In addition, measurements should be carried in a controlled environment. For the control of the humidity in the environment, hermetic or semi-hermetic packages are required and ambient environment should be filled with inert gases for possible leakages.

CHAPTER 5

BIASING DISTRIBUTION OF RF MEMS SYSTEMS

Ultimate goal of the RF MEMS devices is the system integration of the stand-alone components with other designs. However, integration of a single component to another system may not be preferred due to the increased losses coming from the bonding wires and increased voltage level requirement of the MEMS devices compared to other technologies. Hence, MEMS reveals its advantage in the system level integration. Since each component on systems performs different tasks independent of the remaining components, separate control of the individual subsystems is required for the system level operation of the devices. Due to the complexity of the actuation waveforms (Chapter 4) and increased number of components that need separate actuation timings, a general controlling mechanism is required.

For a device composed of several switches placed for tuning the response of the systems, like stub tuner [43] or a phase shifter application [44], number of the switches can exceed 20 or even more. Separate actuation of every switch results in a total combination, exceeding 1×10^6. Measurement of the devices also needs to be automated due to the increased number of possibilities. For accomplishing the task specified, a custom distribution card is designed and produced. Also for the synchronization with the other instruments, a computer interface with HP-VEE is prepared. Section 5.1 explains the distribution control circuit, used for synchronization between the other circuits and measurement devices. Section 5.2 explains the operation of the high voltage distribution circuit, used for the controlling high voltage signals. Section 5.3 covers the layout design of the circuits. Section 5.4

gives the component used for integrating the high voltage circuits and RF MEMS devices. Last section provides simplified schematic of the system and a measurement carried with the automated measurement system.

5.1. Distribution Control Circuit

Figure 5-1 demonstrates the distribution control circuit. The purpose of the distribution control card is to act like a master circuit between the PC and the other slave circuits and buffer the info coming from the PC. Hence, data coming from the PC is stored in the registers and send to slave circuits with correct timing and address information.

The general structure of the circuit is simple and consists of a microcontroller and buffers. To be able to get familiar with the terms used and operation of the devices, general information about microcontrollers are provided below:

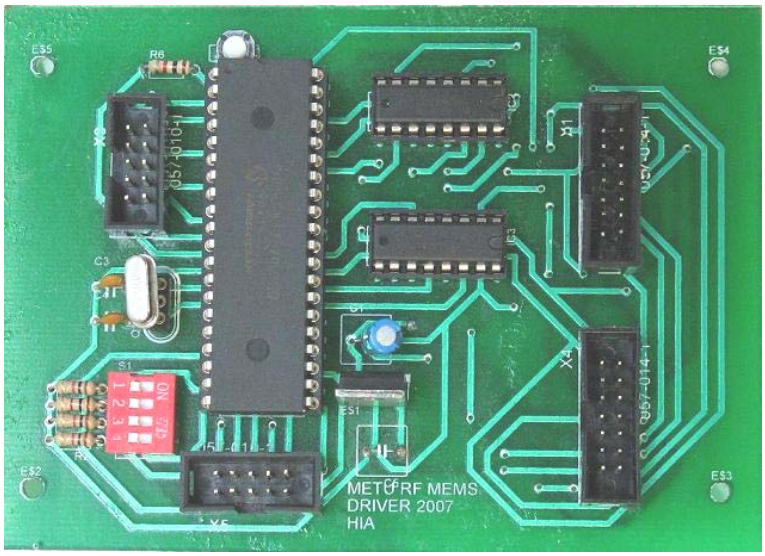

Figure 5-1: Distribution control circuit.

In brief, a microcontroller is a complete computer on a single chip. It combines the microprocessor, peripheral components, ROM and RAM to a single chip and hence reduces the cost of the finalized system. Most of the microcontrollers are used for the control, monitoring and processing systems. General structure composed of an arithmetic logic unit, a program memory, a data memory and I/O interface. Microcontroller fetches data, perform limited calculations and control its environment according to the data.

Arithmetic logic unit (ALU) is designed to perform arithmetic like addition and subtraction and logical operations like OR, AND, NOT and exclusive OR. ALU is the heart of any microcontroller or microprocessor unit and hence it has to be fast and powerful.

Memory elements of the microcontroller can be divided into two main groups. One is the program memory used for the executing the program instructions. The second is the data memory where data generated during the arithmetic operations are stored. According to the microprocessor architecture, program memory and data memory can be combined on the same memory.

The I/O interface is used for the communication with outer world. With the program stored and data received from the I/O ports, microcontroller controls its environment.

Buffer circuits mainly amplify the incoming data from the microcontroller and buffers to the output terminal. Total of 8-bit data and 3-bit address information is carried over the buffer circuits. Output buffers are capable of sourcing up to 25 mA and sinking 20 mA current. In addition, buffers protect the microcontroller from any overload or short circuit due to the failure of the slave circuits.

There are one output, two input and one bi-direction output port of the circuit. Output port is used for transmitting data to the slave circuits. 8-bit data and 3 bit

address information is transmitted from the output port. There are two slots for the output port for the ease of connection to the slave circuits and decreased connection resistance. One input port is used for the computer interface. Remaining ports are placed for the possible future applications. One input port placed with four DIP switches, for enabling multi-mode operation with a single microcontroller. In addition, one bi-directional port is placed for any possible outer interaction.

5.2. High Voltage Distribution Circuit

Figure 5-2 shows the high voltage distribution card. This card is a slave card and gets input from the controller card. Distribution card is used for the control of the high voltage signals using low voltage controls. Hence, data coming from the master card is stored on the register of the slave card according to the address information.

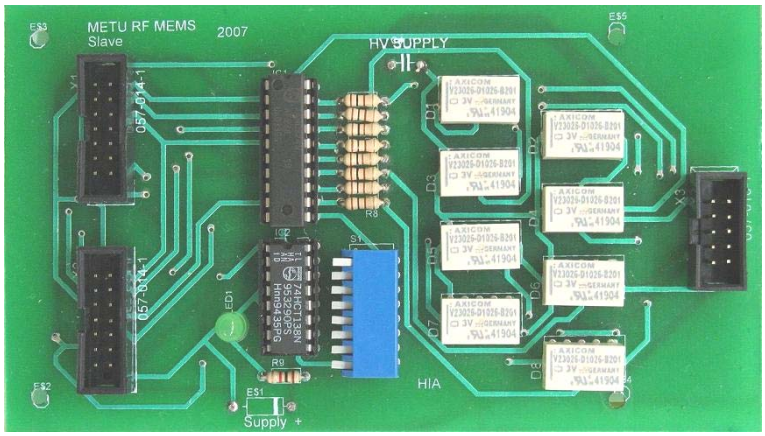

Figure 5-2: High voltage distribution circuit.

General structure consists of an octal D-type flip-flop, 3-to-8 line demultiplexer, an 8-bit DIP switch and 8 high voltage SPDT relays. Brief description and operation of the components can be expressed as follows [42]:

In digital systems, data is represented as binary codes. An 'n' bit of binary data is capable of representing '2^n' elements of coded information. A decoder circuit is capable of transforming the 'n' bit data to the one of the '2^n' elements of coded information. With an enable control added to the decoder, circuit operates as a demultiplexer. Demultiplexer transmits the input signal to one of the '2^n' elements of the output channel. Decoder is used in the distribution circuit and checks the address information coming from the control circuit with the data set with the DIP switches and triggers the enable input of the register. Hence, correct data is transmitted to the output.

Flip-flop is a data storage system used to store information in logic circuits. Data can be stored indefinitely in the circuit, until a new data is fed to the system. Binary input can be transferred to the output, when the enable signal high and data is hold for the enable low duration. Generally, D flip-flops are used in the I/O systems and asynchronous systems. A register is a group of binary cells used for holding binary data. A group of flip-flop forms a register, since only one-bit information can be stored in a D flip-flop. In high voltage distribution circuit, D type registers are used for the data storage and according to the stored data, input signal is transmitted to the relays.

Relay is a mechanical switch, operates under the control of another electric circuit. An electromagnet is used for operation of the device and the electromagnet opens and closes a set of contacts. Relay enables the control of high power levels with lower power levels. The aim of the distribution card is the proper operation of the relays, according to the data coming from the control card. The function of the relay in the circuit is to route high voltage signals to the MEMS devices under the control of the driver circuit. For each MEMS device a single pole, double throw (SPDT) relay is required in the circuit. One terminal of the MEMS device is connected to the output of the relay circuit and the other terminal is connected to the common ground

of the waveshaping circuit. Hence, for the actuation of the device relay connects its output to the output of the waveshaping circuit and for the release of MEMS device, relay connects its output to the common ground. By this way, voltage difference across the MEMS device is definite in down and up states of the device. However, for the single pole, single throw (SPST) case, voltage across the device is indefinite in at least one of the states and may lead to malfunction of device from possible leakages in the circuits.

There is one input bus of the circuit. Two parallel connections are provided for the decreased contact resistance and simplicity of interconnections. Data and address information supplied by the distribution control circuit is received from the input port. Output port of the device is connected to the MEMS devices. High voltage waveforms are transmitted from the output terminal and used for the actuation of the MEMS devices.

There are only eight relays located on the circuit. Since, a relay is needed for every MEMS device, paralleling of the slave circuits are required. Hence using separate address for each slave card, up to 64 switches can be controlled using a single driver card. Also paralleling of driver card enables the control of increased number of switches (multiples of 64). Figure 5-3 gives the simplified schematic of the system constructed with the distribution control circuit and the high voltage distribution circuit.

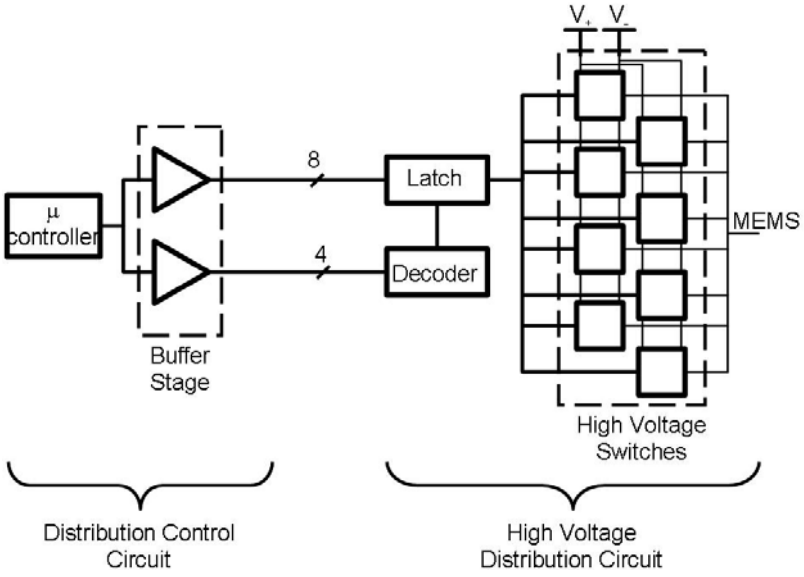

Figure 5-3: Simplified schematic and interconnection of the distribution control circuit and the high voltage distribution circuit.

5.3. Layout of Circuits

For the driver circuit, a PIC16F877 is selected as a microcontroller, availability and cost of the devices. In addition, devices can be re-programmed and hence reduces the cost of development. For the buffer circuits a 74HC367 is used due to its high output current capability. Output buffers are capable of sourcing up to 25 mA and sinking 20 mA of current. Figure 5-4 shows the layout of the driver circuit.

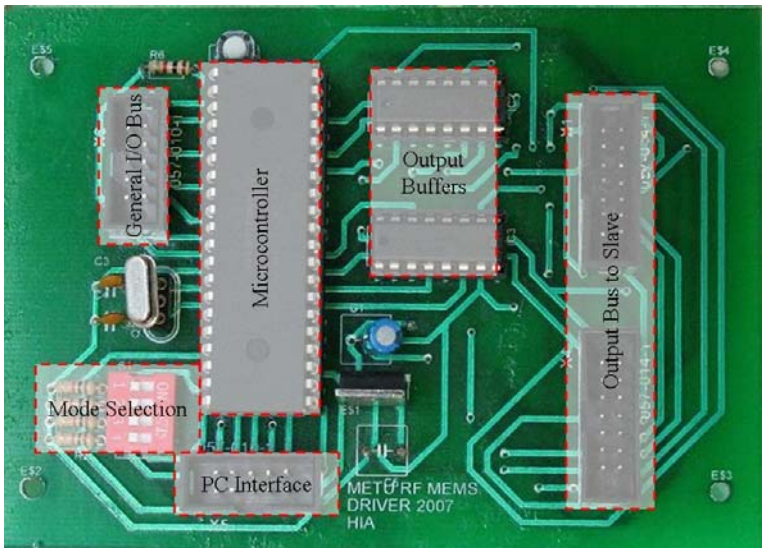

Figure 5-4: Layout of distribution control circuit.

For the slave circuit, 74 HC574 octal D type flip-flop is used as a register due to high output current capability of the device. Since registers are used for the control of the relays, high output current is needed for the proper operation of the relays. Output of the flip-flops can supply up to 25 mA. In addition, a limiting resistance added between the register output and relay. Relays are operated at 5 V and V23026, mono stable, and change over type contacts are used. Relays can withstand up to 125 V AC voltagesand hence, upper limit of the operation is set by the relays.

Operation frequency of the devices is not a design parameter, since the limiting factor for the operation is the data acquisition rate of the network analyzer. Each set of S-parameters are measured in 10 to 15 seconds and hence operation speed of the circuits are much faster compared to the measurement setup.

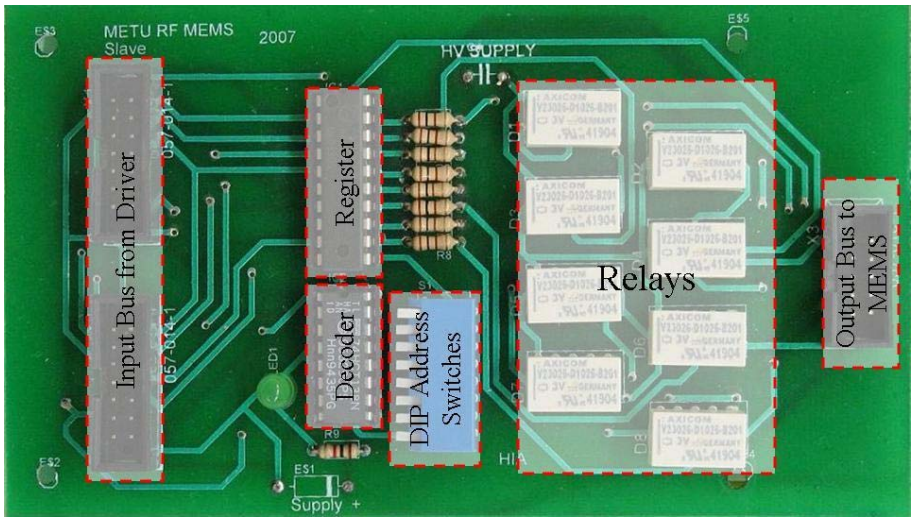

Figure 5-5: Layout of high voltage distribution circuit.

5.4. Integration with MEMS

For the actuation of the MEMS devices, actuation waveforms have to be connected to the pins of the RF MEMS devices. Hence, for establishing a DC connection between the slave circuits and MEMS components, a several custom PCB's are produced. Figure 5-6 demonstrates a connection card, capable of integrating up to four distribution cards and 32 high voltage pins. Figure 5-6 demonstrates a smaller connection card, capable of integrating up to 2 distribution cards and 16 high voltage pins.

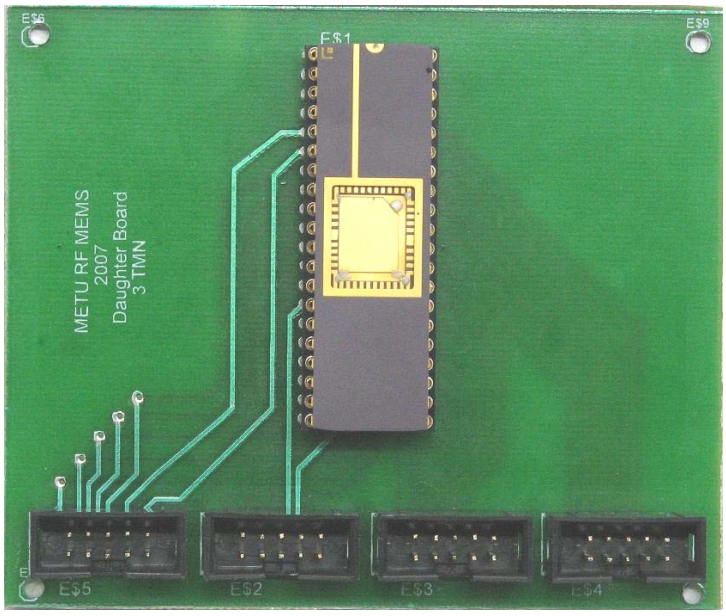

Figure 5-6: Connection card to the MEMS devices (up up to 4 bias cards).

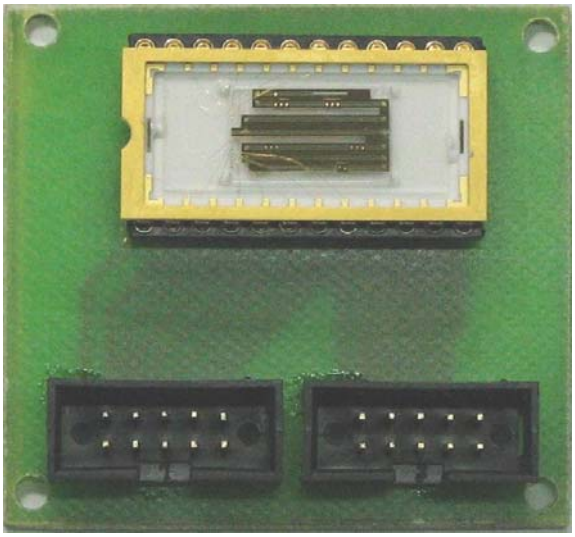

Figure 5-7: Connection card to the MEMS devices (up to 2 bias cards).

5.5. Operation of the Final Circuit

Distribution control circuit and high voltage distribution circuit are operational without high voltage waveforms applied to the circuits. Data from one can be transmitted without any disturbance and error. However, in the integration level with the waveshaping bias circuit (Section 4.4) errors on the transmitted data are observed. Such an error is not expected, since high voltage lines and control lines are electrically isolated from each other. However, measurement of the data lines reveals that high frequency signal (up to few hundred kHz) on the power lines couples to the data lines and induces noise on the transmitted data. With increased voltage levels on the power lines, noise also increases and data transmission totally collapses.

Most probably, source of the coupling between the data and the power lines is the relay itself. Since a coil is used for actuating the relay, fields can couple to the input port, hence control circuit, and distort the low power signals.

For the driver circuit, the problem is solved by utilization of signal processing and filtering the input data. However, problem is much more complicated and severe for the slave circuits. Since coupling is over the relays and placed in slave circuit, data line can easily be disturbed from the noise. In order to solve the noise problem in the circuit, data is sent more than once to the slave circuit to verify the transfer of the correct information. In the final configuration, both circuits are functional in the operation range of the MEMS devices. However, for further improving the design, optocouplers can be inserted between the relay and the registers.

In the final stage, a computer interface is established for the automated measurement setup using HPVEE and HPIB capabilities of the instruments. Figure 5-8 presents the schematic of the automated measurement setup.

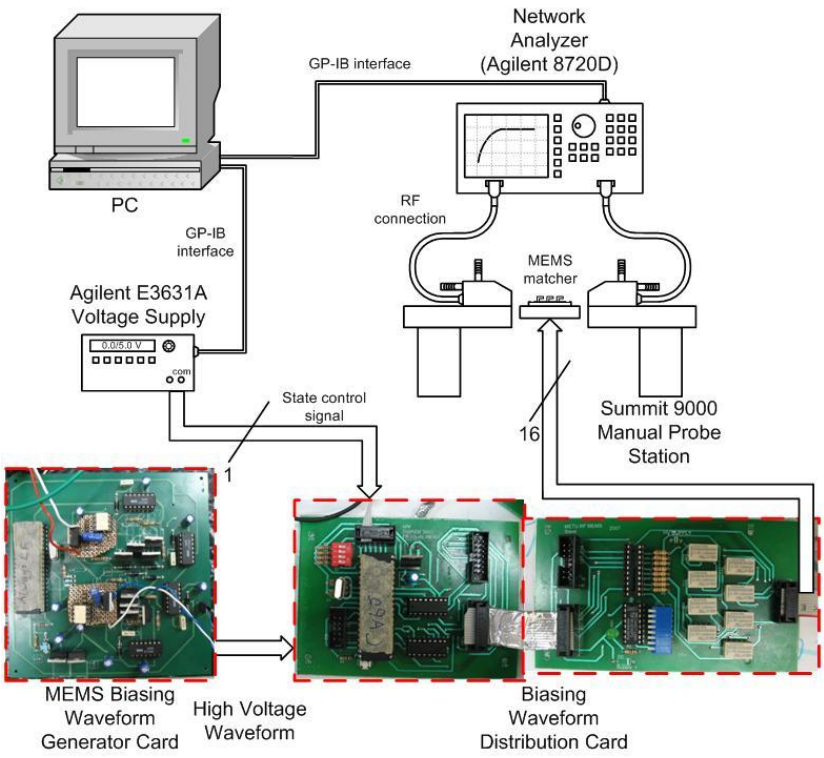

Figure 5-8: Schematic of the automated measurement setup.

For demonstrating the capabilities of the automated measurement setup constructed, a double stub matcher designed by M. Unlu using metal-to-metal contact RF MEMS switches (Chapter 2) is measured. Figure 5-9 shows the output of the automated measurement setup for 72 different states of the double stub matcher design.

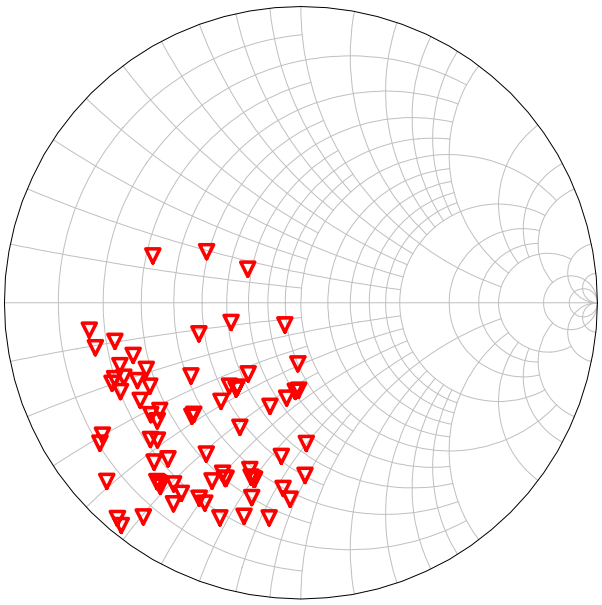

Figure 5-9: Different states of matching network (S21 @ 15 GHz).

5.6. Summary

This chapter presented general information about the distribution control circuit. Moreover, function of the high voltage distribution circuitry is explained. Components used in the construction of the circuit are given and their operations are explained briefly. Microcontrollers are explained briefly and their subsystems are given. General structure, data storage and addressing verification of the high voltage distribution circuit is presented. Communication protocol between the distribution control and high voltage distribution control circuit is explained. Relays used in the high voltage switching applications are explained. Layout and electrical rating of the circuits are given. Also, integration with MEMS components is explained. Problems encountered during the system integration and possible solution mechanisms are presented. Finally, an automated measurement setup is constructed with the components described and used in the measurement of the RF MEMS devices.

CHAPTER 6

CONCLUSION AND FUTURE WORK

In the last decades, commercial and military applications have created an increased demand for high-speed communication systems. Due to the increase in the demand, markets also lead to the enabling technologies for higher communication speeds and new functionalities. Hence, new technologies providing superior RF performance with the increased functionalities, like increased bandwidth, multi frequency operation and adaptive systems in compact sizes are required. Also for the cost efficiency, integration with the current technologies and introducing new aspects to the operation of the systems is a necessity.

With the current MEMS technology, functionality of the micromachining is introduced to RF systems. Novel RF MEMS components are designed and superior performance compared to semiconductor counter parts were obtained. RF MEMS offers advantages over current PIN diode or FET switch like low insertion loss, high isolation, low power consumption and low IMD.

In this thesis, electromagnetic and mechanical modeling of the RF MEMS metal-to-metal contact series switches and lifetime improvements for the RF MEMS components are presented. For this purpose, failure modes leading to degradation of the devices are investigated. Also new equipments are constructed for examining the failure and properties of the RF MEMS devices. Moreover, a custom setup is constructed for applying multi-shape and multilevel high voltage bias waveforms. Finally, for the system integration and measurement of the complicated RF MEMS

system a bias network is produced. The main contributions demonstrated in this thesis can be summarized as:

- For wideband RF MEMS systems, metal-to-metal contact switches are designed, fabricated, and tested. Electromagnetic modeling including loss of the transmission lines, upstate and downstate modeling of the components in conjunction with mechanic modeling including, actuation voltage and switching time is presented. Equivalent circuit model is derived, and verified with the electromagnetic simulations, and the measurement of the devices. This is the first metal-to-metal contact switch study in METU.

- For the dynamic behavior characterization of the switches, a time domain measurement set-up is constructed. As stated in the following parts, actuation waveform generation and distribution circuits are also developed to be used in the set-up. This set-up is necessary for RF MEMS measurements and such a comprehensive set-up is not commercially available as an instrument. For industrial use, similar actuation waveform generation and distribution circuits should accompany the RF MEMS components/systems.

- RF MEMS switching time and power handling measurements is taken with the developed setup, for the first time in METU. Measurement data is compared with the modeling results.

- The designed switch has an insertion loss of 0.2 dB, return loss of 30 dB, and isolation of 20 dB at 20 GHz. For 10 GHz, measured insertion loss is 0.1 dB, isolation is 25 dB, and return loss is better than 40 dB. Switching time of the metal-to-metal contact switch is less than 2 μsec and switch can handle 20 dBm input power with hot switching. The measured switching times are comparable to the best performances reported in the literature.

- For the capacitive designs, measured power handling exceeds 36 dBm input power. Hot switching of 36dBm power is comparable to state-of-the-art designs. For better comparison, the effect of hot switching on the lifetime will be studied.

- Process steps required for the fabrication of the metal-to-metal contact RF MEMS devices are explained in detail. Fabrication steps of the devices are especially important for the mechanical characterization of the structures and reliability of the devices. In addition, the RF characterization depends to the fabrication stage of the components. Especially, process uniformity and repeatability is an important issue for the yield of the larger systems. Mature fabrication is necessary in the commercialization of the final products. Thin film stress and its effects on the mechanical characteristic and performance of the material should be characterized for this purpose. The deposited dielectric layer should be defect free and total trap density should be as low as possible. For post processing, a packaging step, compatible with the previous process steps, can be added for the control of the ambient environment of the switch. Moreover, the package should not distort the RF performance of the structure.

- Lifetime of the RF MEMS switches is investigated. For the proper operation of the devices, extensive studies on the reliability are needed. Hence, possible failure modes are investigated and results behind the degradation of the devices clarified. However, much more work is required for the fully characterization of the structures. Humidity and dielectric charging are stated as main degradation mechanisms.

- For reducing the dielectric charging related failure, a custom circuit is designed and fabricated. Circuit is capable of producing multilevel and

multi-shape high voltage waveforms. With several different types of waveforms, lifetime of the RF MEMS devices has been investigated. Lifetime of the capacitive contact type switches are increased up to 28 hours of operation without any degradation and corresponding switching cycle of 9×10^7 in an uncontrolled environment, i.e., in open environment laboratory conditions. However, with control over environmental conditions, i.e., controlled humidity, dust, temperature, inert gas environment, etc., lifetime of the devices can be increased. Other than this, actuation waveform is a significant factor in the lifetime of the switches and it is shown that the bipolar actuation waveform is necessary and sufficient for increased lifetime.

- A high voltage control and distribution circuit used for the control of the complicated RF MEMS systems is designed. Due to the increased number of the switches, manual control of the structure is not meaningful. Hence, circuit is designed for the automated measurement and operation of the system. Since, circuit needs to be operational under different conditions, like increased switch numbers and different orientations of the switches; circuit is designed with increased modularity. Hence, with a single controller card up to eight distribution cards can be controlled and each control card contains eight switches. Therefore, 64 switches can be controlled at the same time. Moreover, with the paralleling two or more control cards, controller number can be increased according to the requirements of the RF MEMS device.

The future works can be summarized as follows:

- Improving the contact materials of the metal-to-metal contact switches, in order to reduce the wear out of the layers might be studied. Hence, additional steps can be introduced to the process and dimples can be added on top of the first metallization layer and/or under the structural layer. Harder materials should be selected for the formation of the dimple layer. In addition,

mechanical designs of the membrane should be able to withstand increased pressure on the contact regions and applied stress should be below the yield stress of the materials.

- The trap density of the materials should be reduced during the dielectric layer deposition. In addition, different materials with lower trap density can be used instead of the Si_xN_y. For reducing trap density of the Si_xN_y, CVD can be utilized. However, most of the materials in the current process are not compatible with the high temperatures associated with the CVD process; hence, some of the steps can be modified according to the CVD deposition. Moreover, for different material selection, SiO_2 and HfO_2 can be used with less trap density than the Si_xN_y. In addition, some lossy dielectrics can be utilized, enabling the faster discharging in the isolation layer.

As a result, the work carried in this thesis is believed to be helpful in the development of RF MEMS structures and investigation of their performance.

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APPENDIX A

DETAILED FABRICATION STEPS

Some common abbreviations used in the process terminology are:

IPA (isopropyl alcohol): A solvent used for the removing acetone residues from the wafer.

HF: Hydrofluoric acid.

BHF: Buffered Hydrofluoric acid. NH_4:HF 1:5

Piranha solution: A wafer cleaning solution. H_2SO_4:H_2O_2 1.2:1

DI: Deionized water used for rinsing the wafers in cleanroom.

HMDS: A chemical used for the enhancing the adhesion between photoresist and wafer.

Following part describes the fabrication steps developed at the METU-MET process facilities.

A.1 Detailed Fabrication Flow

A.1.1 Wafer Cleaning

- Piranha cleaning of glass wafers using H_2SO_4:H_2O_2 1.2:1
- DI rinse ×2 (15 min each)
- Dehydration (120 °C 20 min)

A.1.2 Resistive Line Deposition

- RF sputter from Si-Cr target, 10×10^{-3} mbar, 100 W, 90 minutes, for a 2000-Å thick bias resistor deposition
- Dehydration (120 °C 20 min)
- Spin HMDS as adhesion layer
- Spin S1828 for 30 secs at 3750 rpm
- Softbake at 115 °C for 1 min 20 secs on the hotplate
- Align wafer and expose 8 secs at 15 mW/cm^2
- Develop in MF26 A for 1 min
- Hardbake at 120 °C for 10 min in the oven
- Descum: O_2 plasma, 0.3 mT, 300 W, 1 minute
- Etch Si-Cr in BHF for 4-5 minutes
- Strip photoresist-spray acetone and IPA
- O_2 plasma for 10 minutes

A.1.3 Base Metal Deposition

- Dehydration (120 °C 20 min)
- DC Sputter from Ti/Au target for base metal seed layer,
    - 2×10^{-3} mbar, 300 W, 100 secs, for a 300 Å-thick Ti
    - 2×10^{-3} mbar, 150 W, 1000 secs, for a 5000 Å-thick Au
- Dehydration (120 °C 20 min)
- Spin AP140 as adhesion layer
- Spin SPR220-3 for 30 secs at 3750 rpm
- Softbake at 115 °C for 1 min 20 secs on the hotplate
- Align wafer and expose 16 secs at 18 mW/cm^2
- Relaxation period for 30 minutes in humidity environment

- Develop in MF24 A
- Hardbake at 120 °C for 10 min in the oven
- Descum: O_2 plasma, 0.3 mT, 300 W, 1 minute
- Gold electroplating for 10 min with 60 mA current
- Strip photoresist-spray acetone and IPA
- Dehydration (120 °C 20 min)
- Spin HMDS as adhesion layer
- Spin S1828 for 30 secs at 3750 rpm
- Softbake at 115 °C for 1 min 20 secs on the hotplate
- Align wafer and expose 8 secs at 15 mW/cm^2
- Develop in MF26 A for 1 min
- Hardbake at 120 °C for 10 min in the oven
- Descum: O_2 plasma, 0.3 mT, 300 W, 1 minute
- Etch Au and Ti
- Strip photoresist-spray acetone and IPA
- O_2 plasma 10 minutes

A.1.4 Dielectric Layer Deposition and Pattern

- PECVD nitride deposition-isolation layer deposition
- Dehydration (120 °C 20 min)
- Spin HMDS as adhesion layer
- Spin S1828 for 30 secs at 3750 rpm
- Softbake at 115 °C for 1 min 20 secs on the hotplate.
- Align wafer and expose 8 secs at 15 mW/cm^2
- Develop in MF26 A for 1 min
- Hardbake at 120 °C for 10 min in the oven
- Descum: O_2 plasma, 0.3 mT, 300 W, 1 minute

- RIE-Nitride etch
- Strip photoresist-spray acetone and IPA. SVC-175 stripper is required for the residues on top of silicon nitride.

A.1.5 Sacrificial Layer Deposition

- Dehydration (120 °C 20 min)
- Spin PI2737 for .30 secs at 3000 rpm
- Softbake at 75 °C for 4 min 30 secs on the hotplate.
- Align wafer and expose 15 secs at 18 mW/cm2
- Develop in DE9040 for 1 min 20 secs
- Rinse in PA401R
- Hardbake: ramp from 50 °C -150 °C in 40 min, hold at 150 °C for 50 min, cool down to 50 °C in 20 min

A.1.6 Structural Layer Deposition and Pattern

- DC Sputter from Au target-structural layer formation
    - 10×10^{-3} mbar, 214 W, 300 secs ×4, for a 1.2-µm thick Au
- Spin HMDS as adhesion layer
- Spin MaN1420 for 30 secs at 7000 rpm
- Align wafer and expose .13 secs at 15 mW/cm^2
- Develop in MaD532S for 1 min 10 secs
- Hardbake (120 °C 10 min)
- Descum: O_2 plasma, 0.3 mT, 300 W, 1 minute
- Wafer Dicing

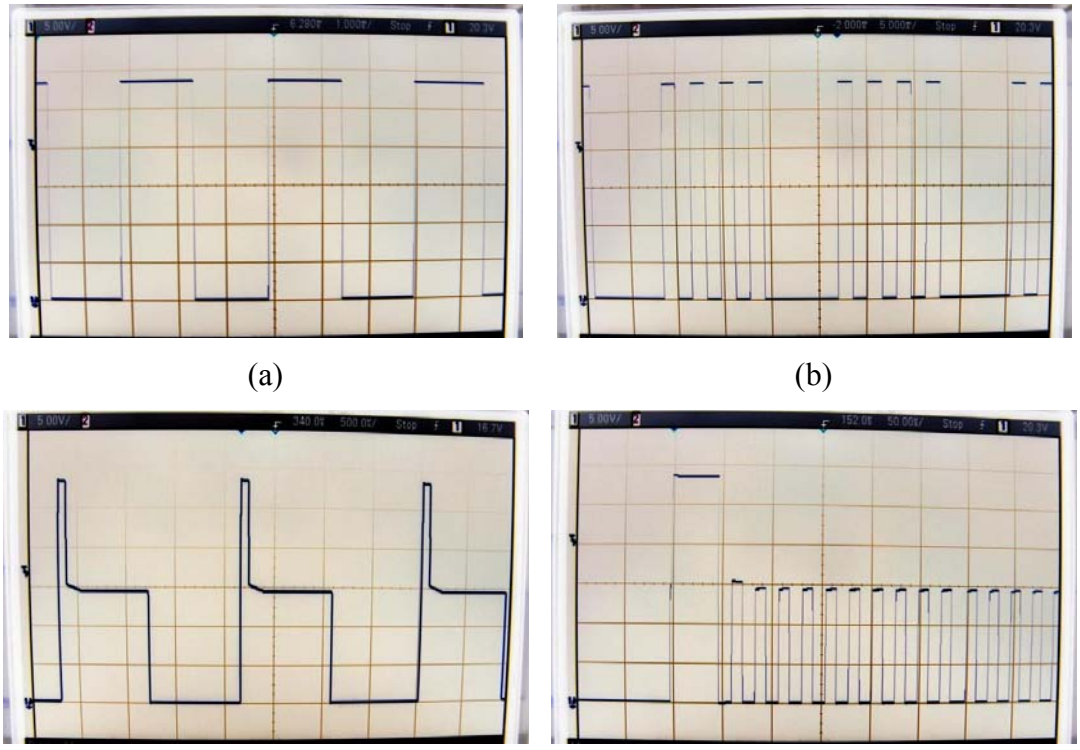
A.1.7 Sacrificial Layer Removal

- RIE-Release (O_2 and CF_4 is added into plasma)

APPENDIX B

AVAILABLE OUTPUT WAVEFORMS WITH WAVESHAPING BIASING CIRCUIT

As presented in Section 4.4, waveshaping bias circuit is capable of producing several different types of output waveforms. Figure 4-15 and Figure 4-16 illustrates schematically some of the output waves for better visualization. Figure B-1 presents the scope output of the biasing circuitry for the unipolar output.

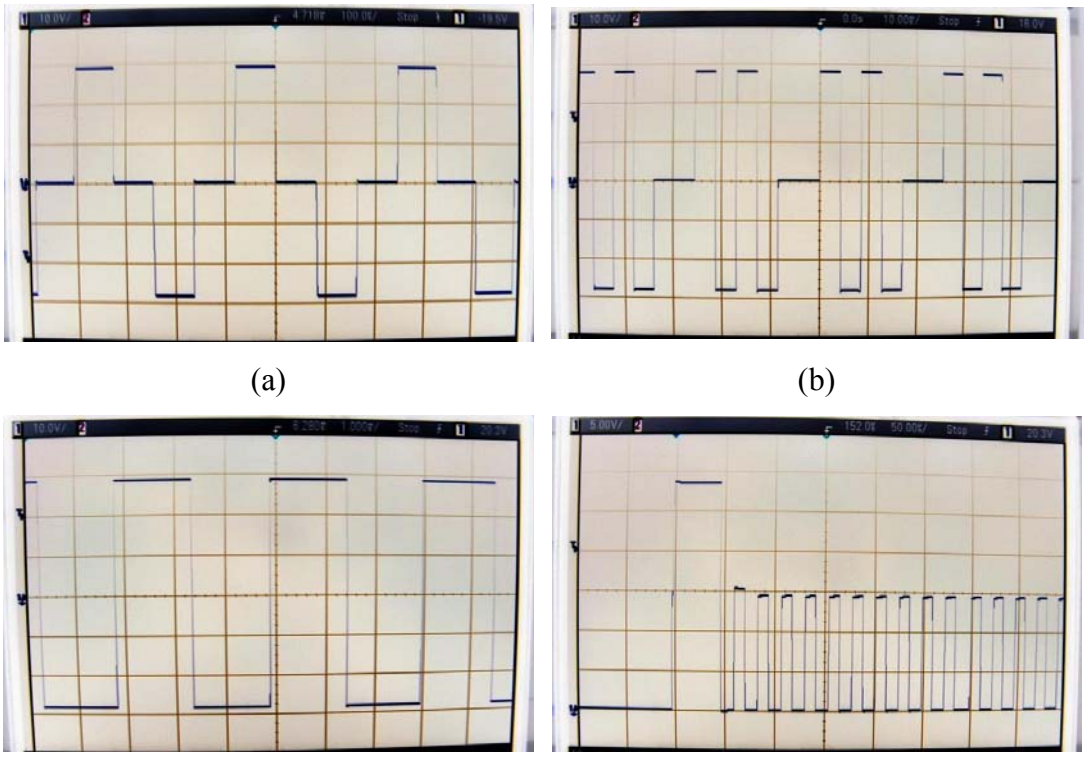


(a) (b)

(c) (d)

Figure B-1: Uni-polar output waveforms. (a) Uni-level DC bias, (b) Pulsating uni-level DC bias, (c) Bi-level DC bias, and (d) Pulsating bi-level DC bias.

Figure B-2 presents the scope output of the biasing circuitry for the unipolar output.



(a) (b)

(c) (d)

Figure B-2: Bi-polar output waveforms. (a) Bi-polar uni-level DC bias, (b) Bi-polar pulsating Uni-level DC bias, (c) Switch down duration of bi-polar pulsating uni-level DC bias, and (d) Switch down duration of bi-polar pulsating bi-level DC bias.

APPENDIX C

LAYOUT DRAWINGS OF THE CONSTRUCTED CIRCUITRIES

Layout drawings of the waveshaping biasing circuit, distribution control circuit, high voltage distribution circuit and connection cards are presented in this section. Figure C-1 to Figure C-4 presents the layout of the constructed circuitries in this thesis.

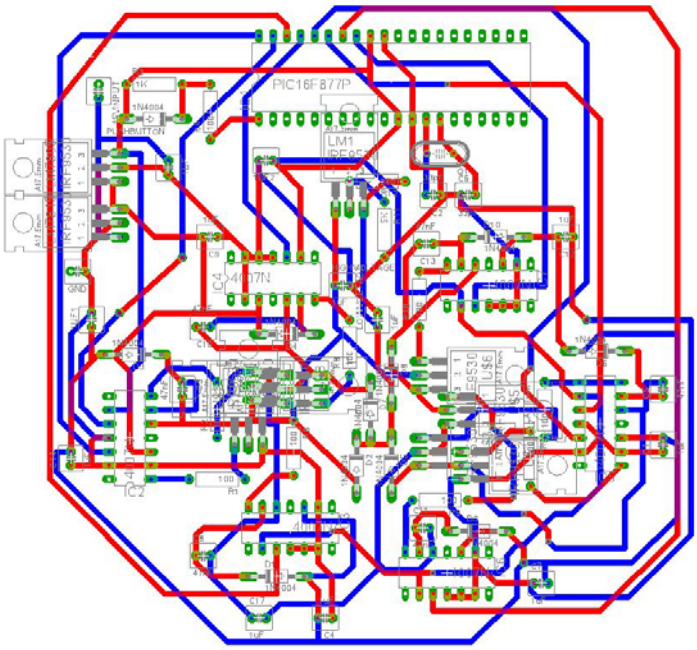


Figure C-1: Layout and component placement of the waveshaping biasing card.

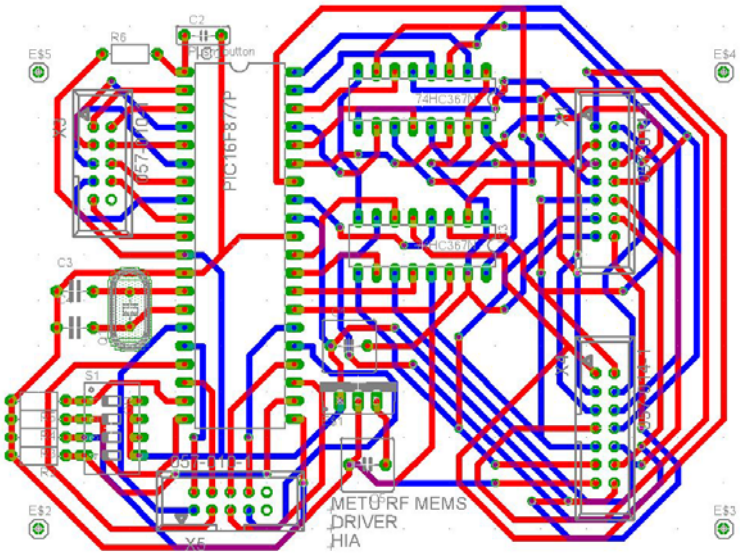


Figure C-2: Layout and component placement of the distribution control circuit.

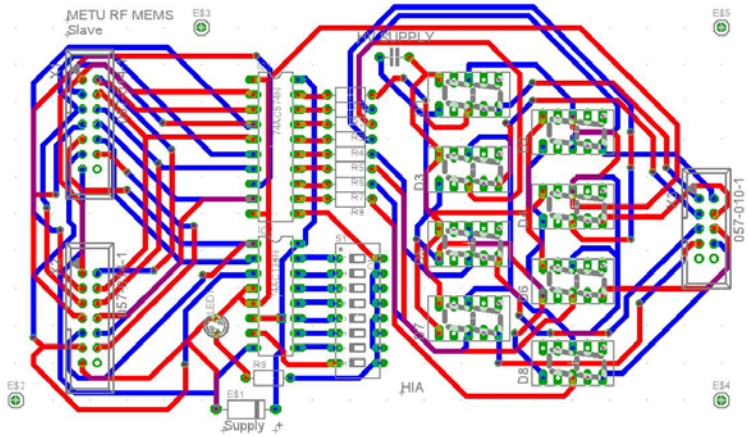


Figure C-3: Layout and component placement of the high voltage distribution circuit.

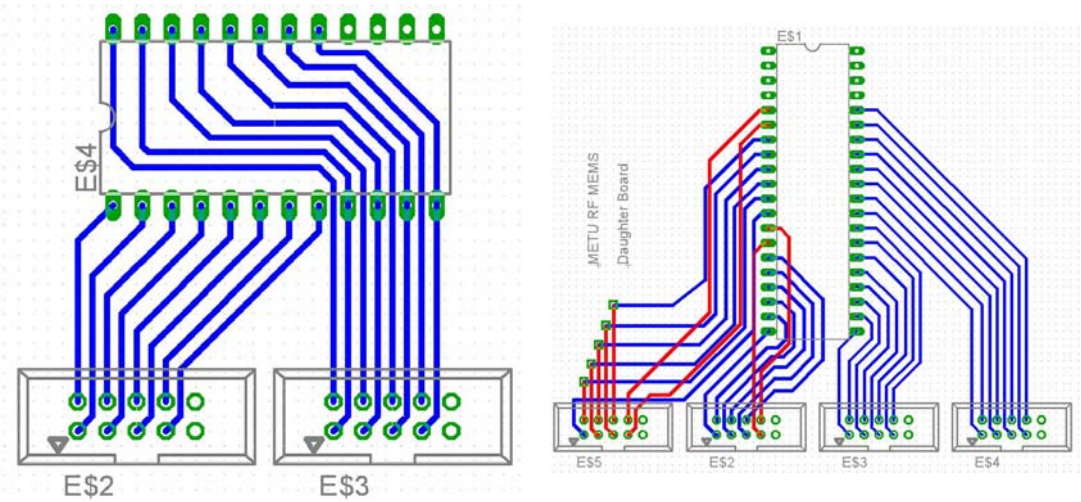


Figure C-4: Layout and component placement of the connection cards.

APPENDIX D

MICROCONTROLLER CODES

For the control and the synchronization of the external circuitry and for the flexibility of the circuits, reprogrammable microcontrollers are used in the design of the waveshaping bias circuit and distribution control circuit. Segments of the code are provided for each controller.

D.1 Sample Code for the Waveshaping Bias Circuit

```
#include "pic.h"
#include "delay.h"
#define PULSE 20
#define LOW 2
#define MULT 1
#define MAX 12
#define INI 200
/*2006.11.2  Halil Ibrahim ATASOY
Bilevel bipolar actuation
Carrier freq:4.6 kHz /Repetition rate: 1.3 kHz
Pulse duration: 43 usec
*/
void main ( ){
int a,b,c;
PORTB=0;
TRISB=0x00;
for(;;){
a=LOW;
PORTB=0b00111100;
DelayUs(INI);
PORTB=0b11000011;
DelayUs(INI);
while(a){
```

```
b=MULT;
while(b){
PORTB=0b01101100;
c=PULSE;
while(c){
DelayUs(MAX);
c=c-1;}
PORTB=0b11000110;
c=PULSE;
while(c){
DelayUs(MAX);
c=c-1;}
b=b-1;}
a=a-1;}
a=LOW;
while(a){
b=MULT;
while(b){
PORTB=0b11001100;
c=PULSE;
while(c){
DelayUs(MAX);
c=c-1;}
b=b-1;}
a=a-1;}}}
```

D.2 Sample Code for the Distribution Control Circuit

```
#include "pic.h"
#include "delay.h"
#define PULSE 240
/*2007.05.03 by Halil Ibrahim ATASOY\
4 card control for capacitive contact type measurement only!
*/
void main ( ){
int
reg1,reg2,reg3,reg4,Adr,Tog,i,y,j,m,dummy,dummy2,dummy3,t1,t2,t3,t4,t5,t6,t7,t8,
t9,d;
int delay1, delay2,dummy4,count,cs;
cs=1;
PORTB=0;
PORTC=0;
```

```
PORTD=0;
TRISB=0x00;
TRISC=0xFF;
TRISD=0x0F;
DelayUs(250);
DelayUs(250);
DelayUs(250);
DelayUs(250);
reg1=0;
reg2=0;
reg3=0;
reg4=0;
Adr=0;
count=0;
PORTD=3;
DelayUs(200);
PORTB=0;
DelayUs(200);
PORTD=0;
i=8;
while(i){
        Adr=Adr+1;
        y=Adr;
        y=y<<4;
        PORTD=y;
        i=i-1;
        PORTB=0x00;
Tog=100;
while(Tog){
        j=100;
        while(j){
                j=j-1;}
        Tog=Tog-1;}}
Adr=0;
Tog=0;
DelayUs(250);
DelayUs(250);
DelayUs(250);
DelayUs(250);
for(;;){ d=254;
        t1=(PORTC & 0x01);
        DelayUs(250);
        t2=(PORTC & 0x01);
        DelayUs(250);
        t3=(PORTC & 0x01);
```

```
DelayUs(250);
t4=(PORTC & 0x01);
DelayUs(250);
t5=(PORTC & 0x01);
DelayUs(250);
t6=(PORTC & 0x01);
DelayUs(250);
t7=(PORTC & 0x01);
DelayUs(250);
t8=t1|t2|t3|t4|t5|t6|t7;
t9=t1&t2&t3&t4&t5&t6&t7;
while(d){
t1=(PORTC & 0x01);
DelayUs(250);
t2=(PORTC & 0x01);
DelayUs(250);
t3=(PORTC & 0x01);
DelayUs(250);
t4=(PORTC & 0x01);
DelayUs(250);
t5=(PORTC & 0x01);
DelayUs(250);
t6=(PORTC & 0x01);
DelayUs(250);
t7=(PORTC & 0x01);
DelayUs(250);
t8=t1|t2|t3|t4|t5|t6|t7|t8;
t9=t1&t2&t3&t4&t5&t6&t7&t9;
d=d-1;}
if(t8==0)
m=0;
if(t9==1)
m=1;
if(m!=Tog){
        Tog=m;
        if(reg1==0)
                dummy=0x01;
        else if(reg1==0x01)
                dummy=0x02;
        else if(reg1==0x02)
                dummy=0x04;
        else if(reg1==0x04)
                dummy=0x08;
        else if(reg1==0x08)
                dummy=0x10;
```

```
else if(reg1==0x10)
        dummy=0x20;
else if(reg1==0x20)
        dummy=0x40;
else if(reg1==0x40)
        dummy=0x80;
else
        dummy=0;
reg1=dummy;
PORTD=0;
DelayUs(100);
DelayUs(250);
PORTB=reg1;
DelayUs(100);
DelayUs(250);
PORTD=0x70;
if(reg1==0){
        if(reg2==0)
                dummy2=0x01;
        else if(reg2==0x01)
                dummy2=0x02;
        else if(reg2==0x02)
                dummy2=0x04;
        else if(reg2==0x04)
                dummy2=0x08;
        else if(reg2==0x08)
                dummy2=0x10;
        else if(reg2==0x10)
                dummy2=0x20;
        else if(reg2==0x20)
                dummy2=0x40;
        else if(reg2==0x40)
                dummy2=0x80;
        else if(reg2==0x80)
                dummy2=0;
        else
                dummy2=0;
reg2=dummy2;
PORTD=0x10;
DelayUs(100);
DelayUs(250);
PORTB=reg2;
DelayUs(100);
PORTD=0x70;
DelayUs(100);
```

```
if(reg2==0){
        if(cs==1){
        if(reg3==0)
                dummy3=0x01;
        else if(reg3==0x01)
                dummy3=0x02;
        else if(reg3==0x02)
                dummy3=0x04;
        else if(reg3==0x04)
                dummy3=0x08;
        else if(reg3==0x08){
                dummy3=0x00;
                cs=0;}
        else {
                dummy3=0;
                cs=0;}
reg3=dummy3;
PORTD=0x20;
DelayUs(100);
DelayUs(250);
PORTB=reg3;
DelayUs(100);
PORTD=0x70;
DelayUs(100);}
if(cs==0){
        if(reg4==0)
                dummy4=0x08;
        else if(reg4==0x08)
                dummy4=0x04;
        else if(reg4==0x04)
                dummy4=0x02;
        else if(reg4==0x02)
                dummy4=0x01;
        else if(reg4==0x01){
                dummy4=0x00;
                cs=1;}
        else{
                dummy4=0;
                cs=1;}
reg4=dummy4;
PORTD=0x30;
DelayUs(100);
DelayUs(250);
PORTB=reg4;
DelayUs(100);
```

```
        PORTD=0x70;
        DelayUs(100);}}}}
if(0<=count && count<=0x02){
delay1=1;
while(delay1){
        PORTB=reg1;
        DelayUs(100);
        PORTD=0;
        delay2=10;
        while(delay2){
        DelayUs(250);
        delay2=delay2-1;}
        DelayUs(250);
        PORTB=reg1;
        DelayUs(250);
        delay2=100;
        while(delay2){
        DelayUs(250);
        delay2=delay2-1;}
        PORTD=0x70;
        delay1=delay1-1;}}
else if(0x02<count && count<=0x04){
delay1=1;//module starts
while(delay1){
        PORTB=reg2;
        DelayUs(100);
        PORTD=0x10;
        delay2=10;
        while(delay2){
        DelayUs(250);
        delay2=delay2-1;}
        DelayUs(250);
        PORTB=reg2;
        DelayUs(250);
        delay2=100;
        while(delay2){
        DelayUs(250);
        delay2=delay2-1;}
        PORTD=0x70;
        delay1=delay1-1;}}
else if(0x04<count && count<=0x06){
delay1=1;
while(delay1){
        PORTB=reg3;
        DelayUs(100);
```

```
                PORTD=0x20;
                delay2=10;
                while(delay2){
                DelayUs(250);
                delay2=delay2-1;}
                DelayUs(250);
                PORTB=reg3;
                DelayUs(250);
                delay2=100;
                while(delay2){
                DelayUs(250);
                delay2=delay2-1;}
                PORTD=0x70;
                delay1=delay1-1;}}
        else {
        delay1=1;
        while(delay1){
                PORTB=reg4;
                DelayUs(100);
                PORTD=0x30;
                delay2=10;
                while(delay2){
                DelayUs(250);
                delay2=delay2-1;}
                DelayUs(250);
                PORTB=reg4;
                DelayUs(250);
                delay2=100;
                while(delay2){
                DelayUs(250);
                delay2=delay2-1;}
                PORTD=0x70;
                delay1=delay1-1;}}
count=count+1;
if (count==0x08)
count=0;}}
```

APPENDIX E

CAPACITIVE CONTACT RF MEMS SWITCHES

Capacitive contact types of switches covered in this thesis are designed by K. Topalli [44]. The work carried is based on compensation of the reduced downstate capacitance with the increased bridge inductance. In order to investigate the affects of the patterning of the ground layer and bridge arms over the inductance of the bridge, several different switch geometries are utilized. To be able to carry control experiment a standard type of ground and bridge combinations utilized (A). In the second group, ground patterning is investigated and slots are implemented on the ground lines (B). At the final group, both patterning of the ground planes and meandered bridge arms applied on a switch for further improving the shunt inductance of the switch (C).

Some of the switches have very similar bridge designs; however, microwave performance of the devices differs for each group due to differences in the ground patterning. In this thesis, switches are investigated according to the mechanical properties of the devices and differences in the microwave performance are ignored. Section 2 describes the differences in the mechanical performance of the devices. However, microwave characterization of the switches is out of scope of this thesis.

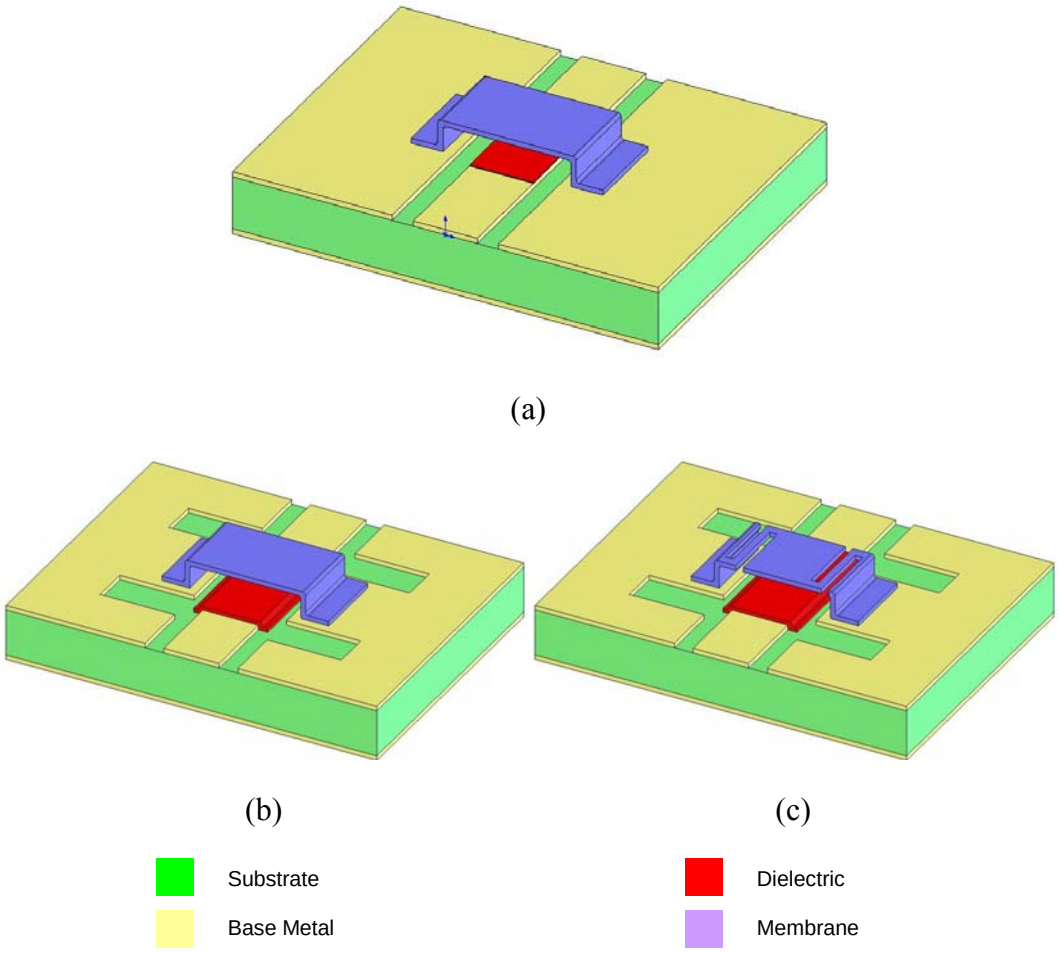


Figure E-1: Capacitive switch types. (a) Standard capacitive switch (Type-A), (b) Slots on the ground plane (Type-B), and (c) Combination of slots on the ground planes and meanders on the bridge arms (Type-C).

Type B-1, type B-2, type B-3, and type A-1 have the same mechanical performance; however slots on the ground planes differs hence posses different microwave characteristics. Type B-4 and type B-5 have the same mechanical characteristic, but slot widths differ. Therefore, mechanical properties should be similar. Type C-1 and type C-2 have meandered structure and expected to perform switching at a lower applied potentials. Type C-2 has wider bridge with and lower actuation voltage.

Mechanical properties of the switches follow an expected behavior; however, process related conditions drift the performance of the membrane from its original values. Especially membranes with lower mechanical spring coefficients, affected badly from the excessive heat in the process steps. Hence, deformations can be observed during the release cycle, due to the residual stress induced on the membrane.

According to the measurement results, bridges can deflect up to 11 μm and behave in a different manner. In addition, uniformity along the wafer plays an important role and similar devices on the same wafer can perform different characteristics. Hence, fabrication of the devices is crucial for the reliability of the devices.