A 1GS/S, 9-BIT DAC INTERLEAVED (2+1)-BIT THEN 2-BIT PER CYCLE, REFERENCE FREE SAR ADC

A Thesis

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A 1GS/S, 9-BIT DAC INTERLEAVED (2+1)-BIT THEN 2-BIT PER CYCLE, REFERENCE FREE SAR ADC

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To ..... My Mother who has always been encouraging me to take the further step in my life.

ABSTRACT

This work presents a high speed, medium resolution Successive Approximation Register Analog to Digital Converter (SAR ADC) designed for low-noise, low- power satellite transceiver applications. The proposed system is a (2+1) then 2-bit per cycle SAR ADC of 1GS/s sampling rate, 9-bits resolution designed and characterized in a 65nm standard CMOS technology. The designed system resolves 9 bits with a special switching scheme in a total of 4 cycles per sample effectively. This is achieved by interleaving 4 Capacitive Digital to Analog Converter (C-DACs) of unit capacitance 1fF. Since the interleaving is limited to the passive DACs only which match well, the design does not suffer from the drawbacks of full interleaving. Hence, significantly better power efficiency and performance metrics have been obtained in comparison to regular interleaved ADCs. A special timing scheme with a single extra first-bit comparator is optimized to leave proper timing margins for every step from a single 4- GHz low noise clock source which is readily available in the 8- GHz direct conversion front-end. This comparator as well is reused as all the other active comparators in both interleaving phases. The proposed design achieves an effective number of bits (ENOB) of 8.5 bits at Nyquist with total power consumption of 15mW (1.25V supply), resulting in a Figure of Merit (FoM) of 38.37 fJ/conversion-step.

ÖZETÇE

Bu çalşma düşük gürültülü ve düşük güçlü uydu alcı-vericisi için yüksek hızlı orta çözünürlüklü bir SAR ADC (Analogtan Sayısala Çevirici) tasarımı sunar. İleri sürülen sistem 65nm CMOS teknolojisi kullanılarak 9-bit çözünürlüklü tasarlanmış olup, (2 +1) ve sonrasında 2-bit cevirimi ilerleyen 1Gsps hızında bir SAR ADC niteliğindedir. Tasarlanan sistem 9-biti özel bir anahtarlama metodu ile toplamda 4 dönüşümde çözümleyebilmektedir. Bu performans değerleri 1-fF ünite kapasiteli 4 adet serpiştirmeli C- DAC kullanılarak başarılmıştır. Serpiştirme sadece tutalı işleşme gösteren pasif DAC devreleri ile sınırlı tutulduğundan full serpiştirme yöntemlerinde karşılaşılan problemler önlenmiştir. Böylece standart metodlara karşın daha yüksek performans değerleri elde edilmiştir. Sistem, önarayüzde hali hazırda var olan 8-GHz zamanlama sinyalinden türetilen 4GHz düşük gürültülü zaman kaynağı ile özel anahtarlanan ekstra bir karşlaştırıcı ile optimize edilmiştir. Diğer karşılaştırıcılar ile birlikte bu karşılaştırıcı da her bir serpişrime çevriminde tekrar kullanılmıştır. Bu tezde önerilen tasarm toplam 38.37 fJ per conversion merit başararak, Nyquist hızında 8.5 ENOB çözünürlük sergilemiştir.

ACKNOWLEDGEMENTS

Success doesn't come from individuality, those who succeed those who appreciate every piece of information, every piece of help and every sentence of encouragement that were shared with one by others. Firstly, I would like to show my gratitude to Allah, who has always heard my prayers and gave me the patience to reach what I have reached so far.

I am so delighted that I had the chance to work under the supervision of professor Ahmet Tekin. I had a great opportunity to learn a lot of innovative solutions that aroused along the way in my design. He was always giving me the chance to try my ideas even if he doubted them, so I would learn along the way. I would also like to thank professor Fatih Uğurdağ who offered me help whenever I needed it and he welcomed me at any time for any question.

I should never forget to mention my family and friends that were always there for me to encourage me and offer me advice both technically and emotionally. I would first start with my mother who has continuous faith in me and encouraged me to do be patient and to work harder. Moreover, I would like to thank all of my colleagues and friends that offered me technical help and had the patience to explain me basic information, Ahmed Gharieb, Sherif El-hossainy, Mahmoud Saeed, Mahmoud Abdelwahab, Eman Salah, Shrouk Shafie, Heba Ahmed, and Heba Eid.

Last but not least I want to show my gratitude to Ozyegin university that accepted me as a scholarship student to pursue my master degree under its campus.

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CHAPTER I

INTRODUCTION

Space and satellite communication is one of the hot topics of the current century as it receives the attention of various research and industrial communities. Wide-band transceiver is one of the main components that are essential in telecommunication. The block diagram of a generic transceiver is illustrated in Figure. 1.

Data Converters play an important role in the transceiver design. Analog to Digital Converter (ADC) is as previously illustrated in Figure. 1, the last block of the RF front-end in the receiver side, where its output bits interface with the digital modem. Coming to the conclusion that the ADC is the main block to limit the dynamic range, thus a proper design is necessary. This work represents the design of a low-power, high-speed with interleaving DACs SAR ADC. Later in this chapter, the specifications and requirements of the system are discussed and furthermore, the reason for this architecture selection.

1.1 System Specifications

The specifications set to define the outlines of the ADC block are defined by the whole transceiver system. A Low drop out regulator (LDO) supplies the ADC supply voltage of 1.25V. A 4-GHz low noise clock source is fed to the ADC, which is readily available in the 8-GHz direct conversion front-end. A power amplifier buffers the input signal to the ADC block to be ready for conversion with a peak to peak voltage of 2.4 volts and frequency up to 500MHz. This input range, allows the system to operate with a reference voltage to be the same as the supply voltage of 1.25V. For Nyquist operation, the sampling speed of the ADC should be double the input frequency, implying that the ADC should operate to output 1GS/s. The

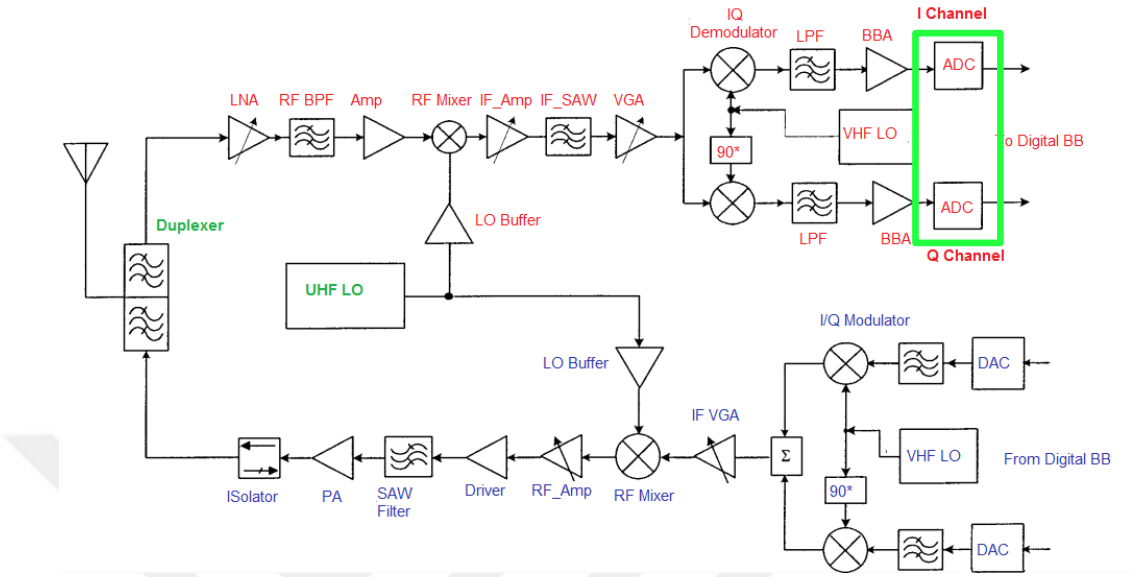


Figure 1: Transceiver generic block diagram.

resolution of the ADC is defined by minimal Signal to Noise Ratio (SNR) defined by the transceivers requirements. This SNR should minimally correspond to the ADC's quantization noise, hence to achieve 50dB SNR, 8-bits is the minimum number of bit. It was decided to have a resolution of 9-bits to assure better SNR if any degradation in the ENOB takes place.

1.2 Architecture Selection

After defining the specifications of the ADC system, from input range, operational frequency, resolution, and system supply, this block is limited by the power budget as well.

Several surveys have been done to state the operation of different ADCs topologies represented by several research works with respect to the resolution, power consumption, Figure of Merit (FoM), and sampling frequency [1].

Figure 2 shows that for the proposed system given the specification of 1GS/s and SNDR around 50dB, SAR ADC shows the best performance. Moreover, the iterative

nature of the SAR ADC, makes it a better choice from the power point of view, as it has less number of comparators compared to Flash ADC.

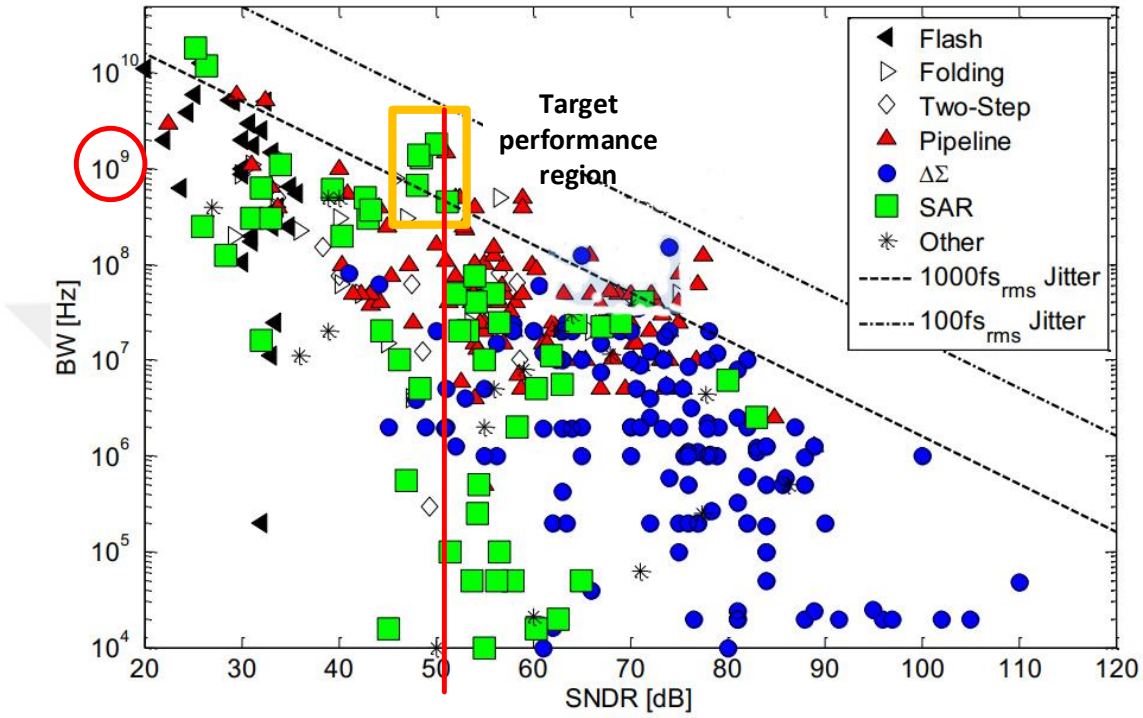


Figure 2: Survey on ADC topologies SNDR Vs. Bandwidth.

1.3 Thesis organization

The following chapters discuss the details of this research work. Chapter 2 tackles the proposed system operation and its ideal model and performance. A Detailed explanation of the circuitry implementation of every sub-circuit, their operation, performance, and limiting factors are approached in chapter 3. Proceeding with the full system performance and system simulations explained in chapter 4. Chapter 5 discusses the layout techniques applied for best performance to match the schematics results. Finally, this work is concluded in chapter 6 followed by future work in chapter 7.

CHAPTER II

SYSTEM DESIGN AND MODELING

Various topologies of SAR ADCs are introduced by different research work. These presented topologies can be categorized according to the following diagram in Figure 3. The classification has been made from the point of view of the number of bits resolved per cycle, the number of stages, timing, switching scheme, and the reference voltage. The decision of choice should be made according to the application and requirements.

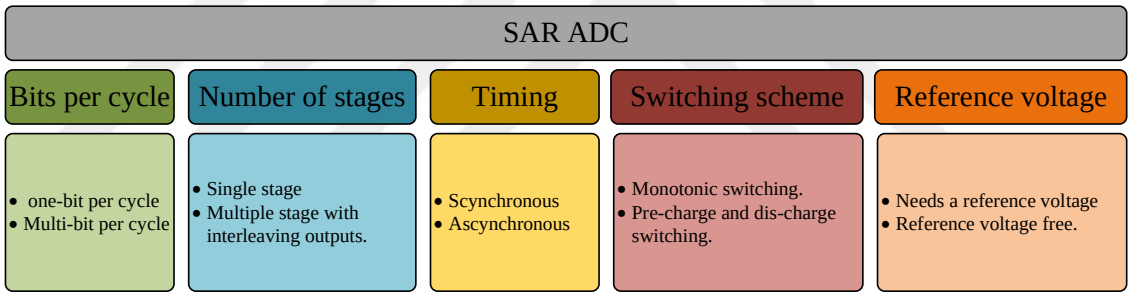


Figure 3: SAR ADC topologies classification

SAR ADCs were previously confined to medium speed, medium resolution application, due to its iterative sequential scheme to resolve the sampled input which takes at least n number of cycles to resolve n number of bits. However, the advances in technology and the variety of innovative architectures in the field proved it is possible to push the limits of the SAR ADC from the speed point of view to reach hundreds of MS/s to few GS/s. Several approaches have been introduced to enhance the capabilities of SAR ADCs to be used for higher frequency applications. Moreover, SAR ADCs are considered power efficient systems compared to FLASH and pipeline, as they depend mainly on digital logic and a single comparator that is considered to

be the only active analog block in the circuit. Some systems use the advantage of asynchronous systems, eliminating any idle conversion time [2, 3, 4, 5]. Differential SAR ADCs [2, 3, 4] are used rather than single-ended topologies [5] to enhance the linearity and to balance any possible mismatch. This required doubling the capacitive DAC and increased the switching power. The disadvantage of differential SAR ADCs from the power consumption point of view has been addressed with the design of a monotonic switching scheme to resolve the same number of bits with less switching steps [2], [6]. This technique has both decreased the power consumption and cut the area by 2 by excluding the MSB binary capacitor and taking the advantage of resolving the first bit while sampling. However, it may severely suffer from the dynamic changes in the input common-mode seen by the comparators. A Tri-level monotonic switching SAR ADC [7] addressed the variations due to dynamic input common mode disadvantage and suggested a switching scheme that keeps the input common mode voltage of the comparator constant.

Researchers showed noticeable interest in interleaving SAR ADCs to relax the speed constraint on the single stage of the ADC, and increase the sampling speed by n number of interleaved stages. It is achievable by doubling both the area and the power [8, 9, 10]. Although time interleaving is widely used to enhance the speed, considering the linear relation between the sampling speed and the number of stages, it can face a noticeable degradation in performance due to channel to channel mismatches, putting a constraint on the number of stages that can be used. Some has proposed to use an extra channel for calibration[10], which made it sound a less preferable solution for low power applications.

Another approach was introduced to increase the sampling rate with a single stage, by resolving multi-bits per cycle rather than 1 bit at a time. In the meantime, multi-bits per cycle SAR ADC has been a point of interest to a good number of researchers [8, 11, 12]. Multi-bit per cycle SAR ADCs can achieve higher frequencies

with less power, area, and circuit complexity compared to interleaving ones, only by sacrificing additional power consumed by the extra comparators needed. Reference [4] introduced a system that resolves 1-bit then 2-bit per cycle, due to top plate sampling. The first bit can be identified immediately after sampling without waiting for any pre-charge operation.

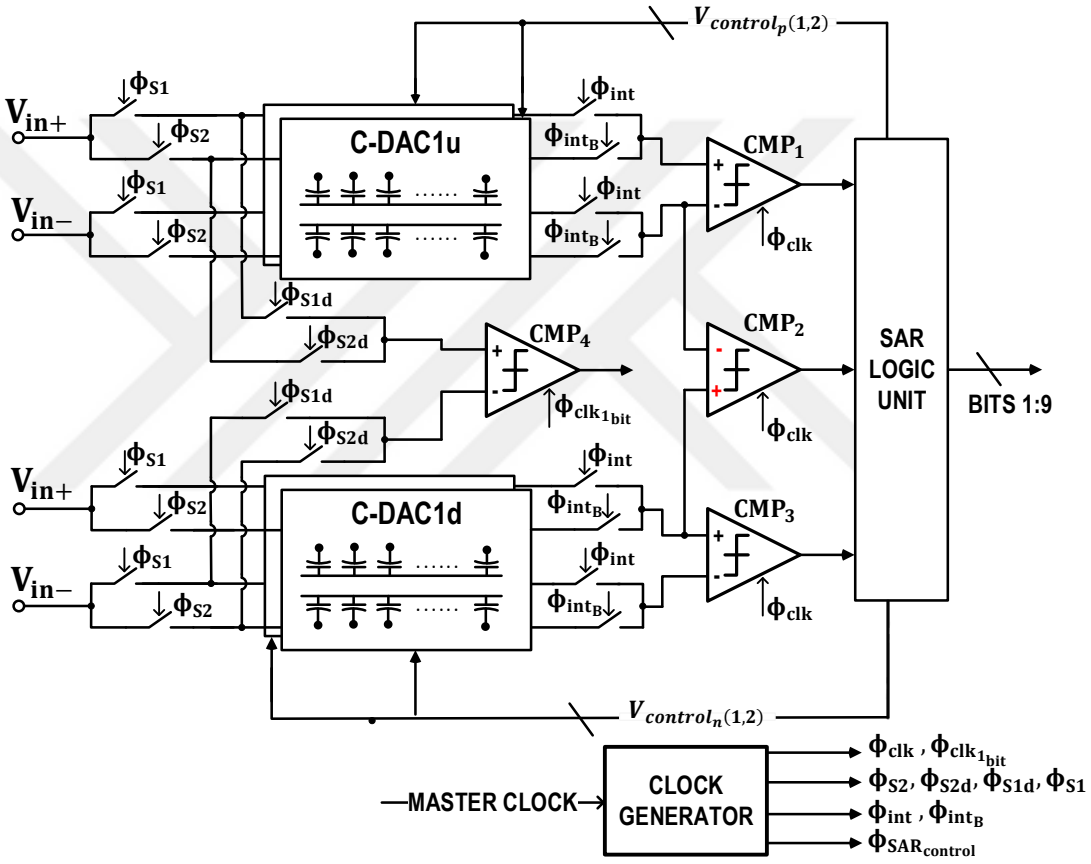


Figure 4: System block diagram.

This work introduces an unconventional design technique based on (2+1) then 2-bit per cycle SAR ADC with interleaving capacitive DACs. Since the interleaving is limited to the passive DACs only which match well, the design does not suffer from the drawbacks of full interleaving. Hence, significantly better power efficiency and performance metrics are obtained in comparison to regular interleaved ADCs. A

special timing scheme with a single extra first-bit comparator is optimized to leave proper timing margins for every step from a single 4-GHz low noise clock source, which is readily available in the 8-GHz direct conversion front-end. This comparator as well is reused as all the other active comparators in both interleaving phases. The system block diagram is illustrated in Figure. 4.

The system consists of 4 sets of sampling switches, 8 sets of interleaving switches, 4 comparators; 3 operate at a 4-GHz clock (CMP1, CMP2, CMP3) and 1 operates at 1-GHz with a narrow pulse (CMP4). Four differential capacitive DACs are used for dumping the charge during bit cycling. SAR logic unit uses the output of the comparator to make the decision and dump the charge to the corresponding capacitor in the capacitive DAC. Lastly, a memory register bank is used to latch the output bits and update it each sample.

This system is modeled on Cadence with VerilogA custom designed blocks to check the proper operation of the proposed design before circuit implementation. Next section, the operation of the system is further discussed and illustrated through the outputs of the modeled design.

2.1 System Model

The schematic of the modeled system is shown in Figure. 5. This system is built using ideal passive devices, such as capacitors and switches, and custom VerilogA coded blocks such as D-flipflops, latched comparators and SAR Logic. In the next subsections, each block is discussed thoroughly mentioning its interfacing, its outputs and how it operates.

2.1.1 Clock Generation

In order to have a clear view of the operation of the system, it is better to start by illustrating the control signals generated by the clock generator that controls each block in the desired manner. Figure. 6 and Figure. 7 show the illustration of all the

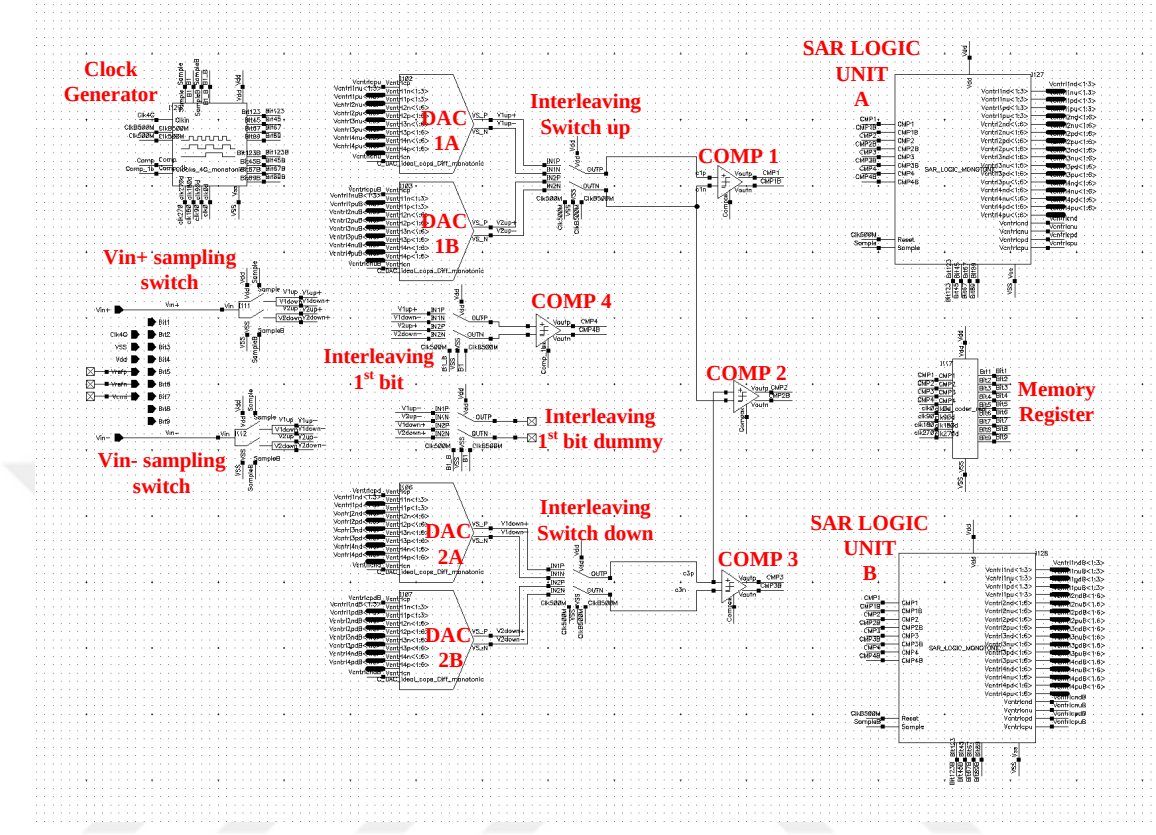


Figure 5: System schematic.

control signals and their simulated result of the modeled system respectively.

A 4GHz clock is fed from an on-chip oscillator to the ADC block Φ_{4G}. The clock generator block is designed to generate all of the needed control signals using a single 4-GHz clock. The 4-GHz clock is divided by 4 using 2 D-FF to generate a 1-GHz clock with its 4 phases (Φ_0,Φ_{90},Φ_{180},Φ_{270}), which are necessary for the definition of SAR logic control signals and the extraction of the output bits. The interleaving switches interleave between the 2 DACs; DAC A and DAC B, with 2 phases of 500MHz nonoverlapping clocks (Φ_{intA} and Φ_{intB}) to assure that there is no voltage sharing taking place during switching. The sampling period and the 1st bit sampling period are ideally 500ps and 750ps respectively and are repeated every 500MHz (Φ_{S1} and Φ_{S1d}) which relaxes the design of the sampling switch for better settling. The

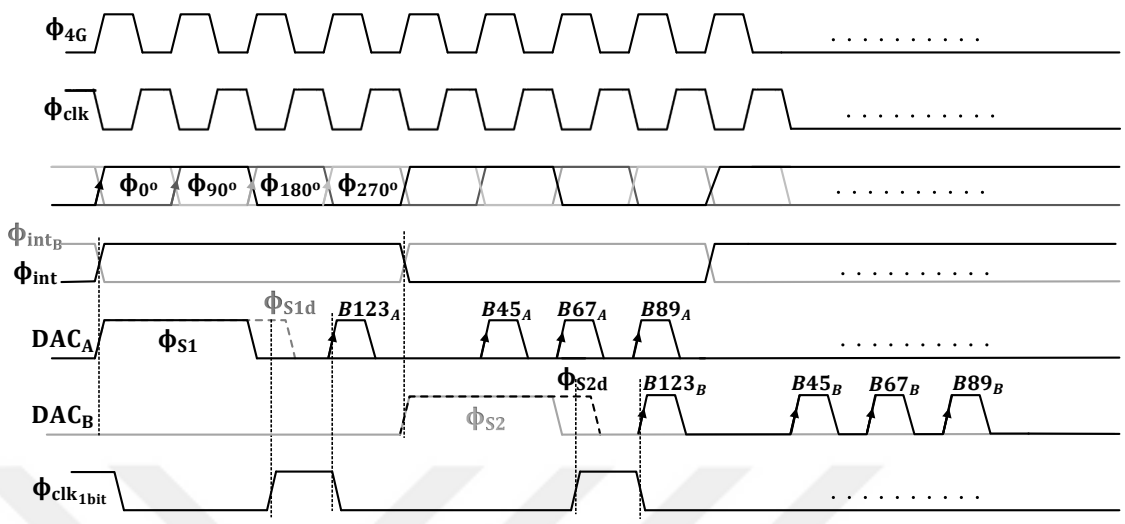


Figure 6: Timing signals.

other DAC signals (Φ_{S2} and Φ_{S2d}) are similarly produced by the complement of the 500MHz clock. The control signals of each DAC are denoted by B_{123A},B_{45A},B_{67A},B_{89A} and B_{123B},B_{45B},B_{67B},B_{89B} are the control signals used by the SAR logic unit to latch the output of the comparator at each rising edge and dump the charge according to that decision into the capacitive DAC.

2.1.2 Switching Scheme

This topology has a unique switching scheme. It starts by taking a 1-bit decision first then 2-bits at a time. This switching scheme is well illustrated in the flowchart in Figure.8 .

2.1.3 Feedback system operation

In this section, a random sample is taken as an example to demonstrate the operation of the whole SAR ADC. Each sample starts with disconnecting the DAC from the 3 essential comparators (CMP1, CMP2, CMP3). Simultaneously, resetting the capacitive DAC charge to their start configuration and sampling the input on the top plate of the DACs deferentially. Directly after sampling, (CMP4) decides the first

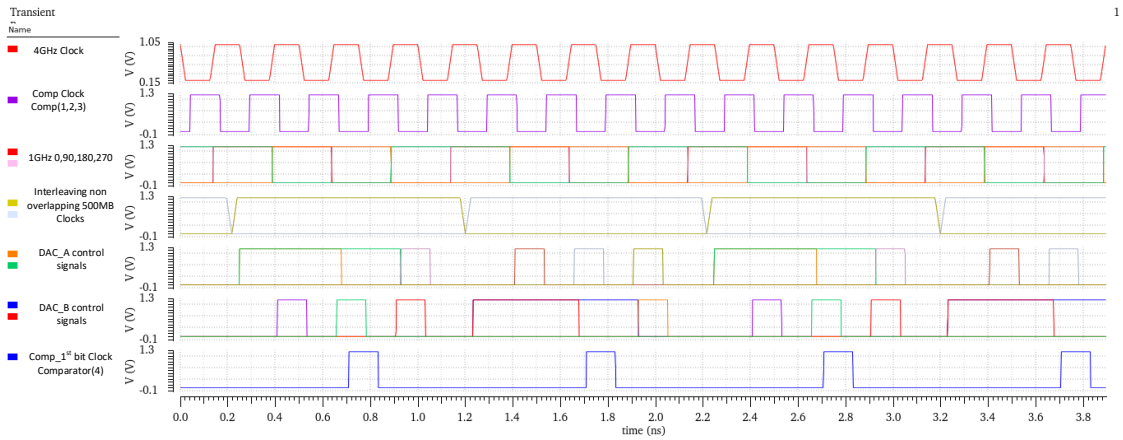


Figure 7: Timing signals simulated from Modeled system.

bit, and the first charge dump takes place preparing the comparison nodes to resolve the 2 consecutive bits when they are connected back to the essential comparators for the resolution completion. Figure. 9 gives a good explanation to the operation of the whole system and the decoding scheme of the output of the comparator.

2.2 Operation Verification

Eventually, after modeling the system and assuring that every signal falls into place, a test-bench has been constructed to measure the spectrum and Effective Number Of Bits (ENOB) for this system at 2 different input frequencies. Simulations show that ideally, the system can resolve the 9 bits in both low frequency and Nyquist frequency as shown in Figure. 10 and Figure. 11 respectively. Next Chapter represents the circuitry of each block and the constraints that limit the performance.

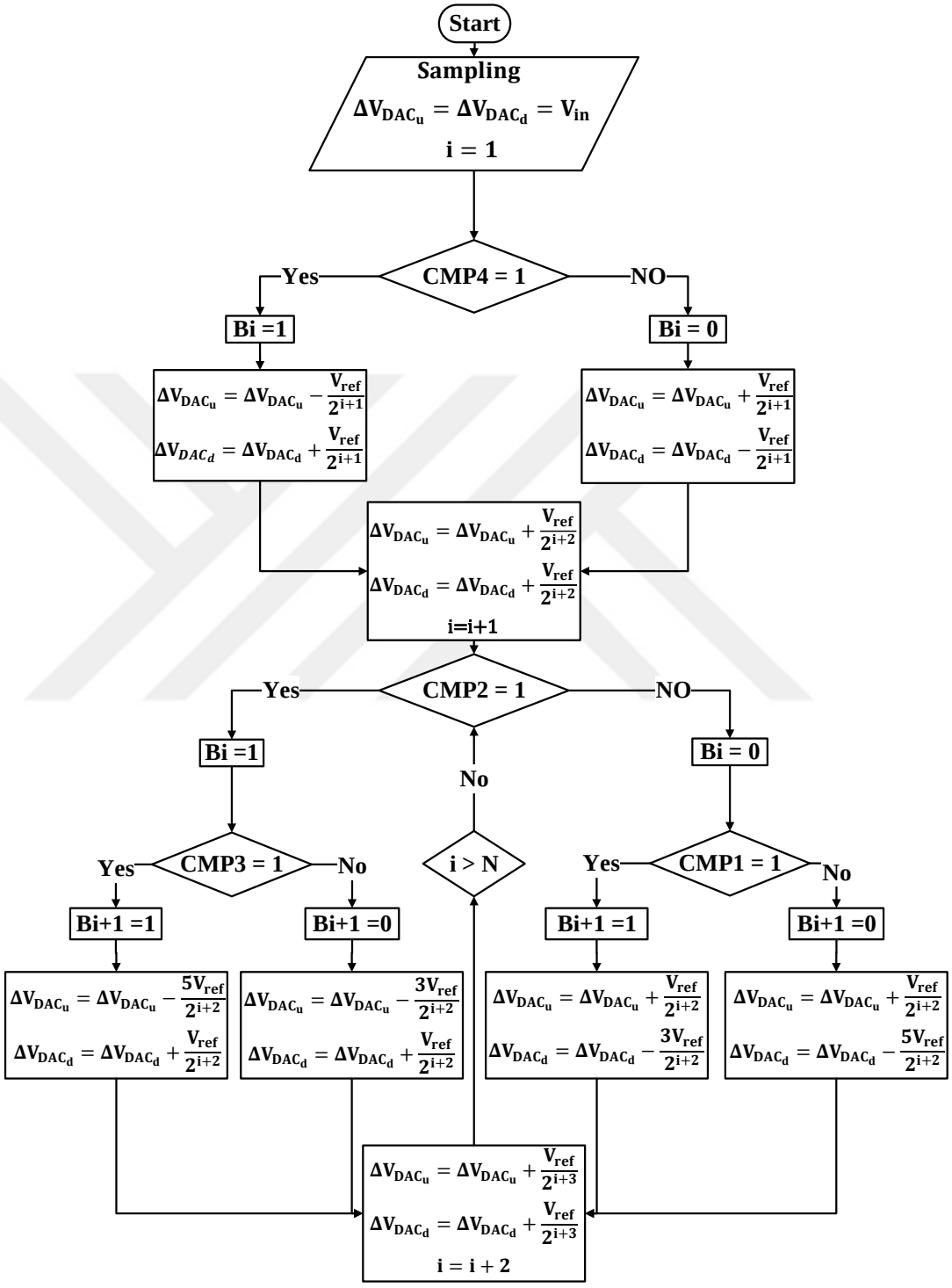
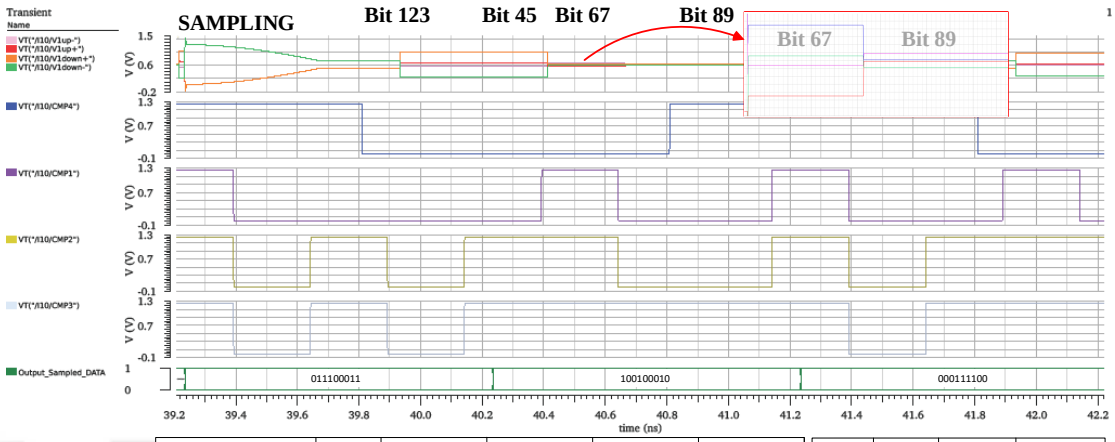


Figure 8: Switching scheme of 1 complete sample flow chart.



SAMPLING	Bit 1	Bit 2,3	Bit 4,5	Bit 6,7	Bit 8,9
	500ps	750ps	250ps	250ps	250ps
Vin+ < Vin-	CMP4=0	CMP1=0 CMP2=0 CMP3=0	CMP1=0 CMP2=1 CMP3=1	CMP1=1 CMP2=1 CMP3=1	CMP1=0 CMP2=0 CMP3=1
	Bit1=0	Bit2,3=00	Bit2,3=11	Bit2,3=11	Bit2,3=00

CMP1	CMP2	CMP3	Bit (N,N+1)
0	0	0/1	00
1	0	0/1	01
0/1	1	0	10
0/1	1	1	11

Figure 9: Sample resolution example and decoder scheme

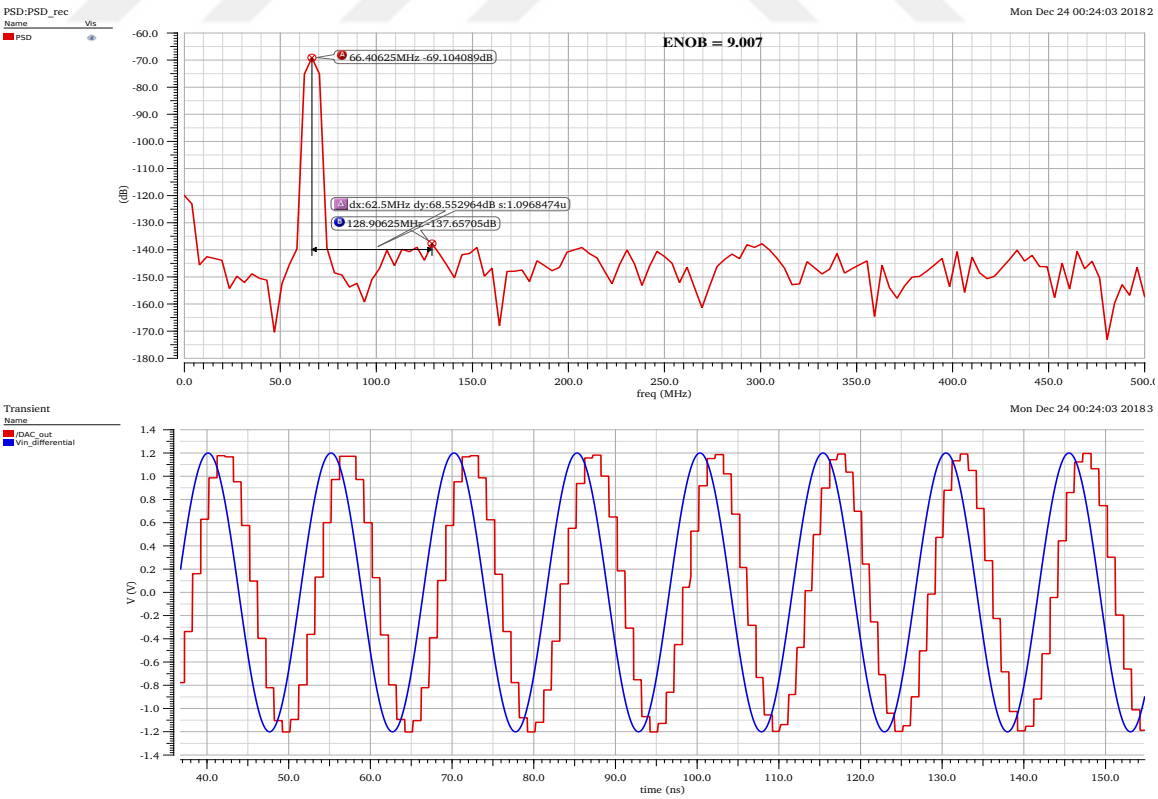


Figure 10: Spectrum , input, output at 66MHz frequency.

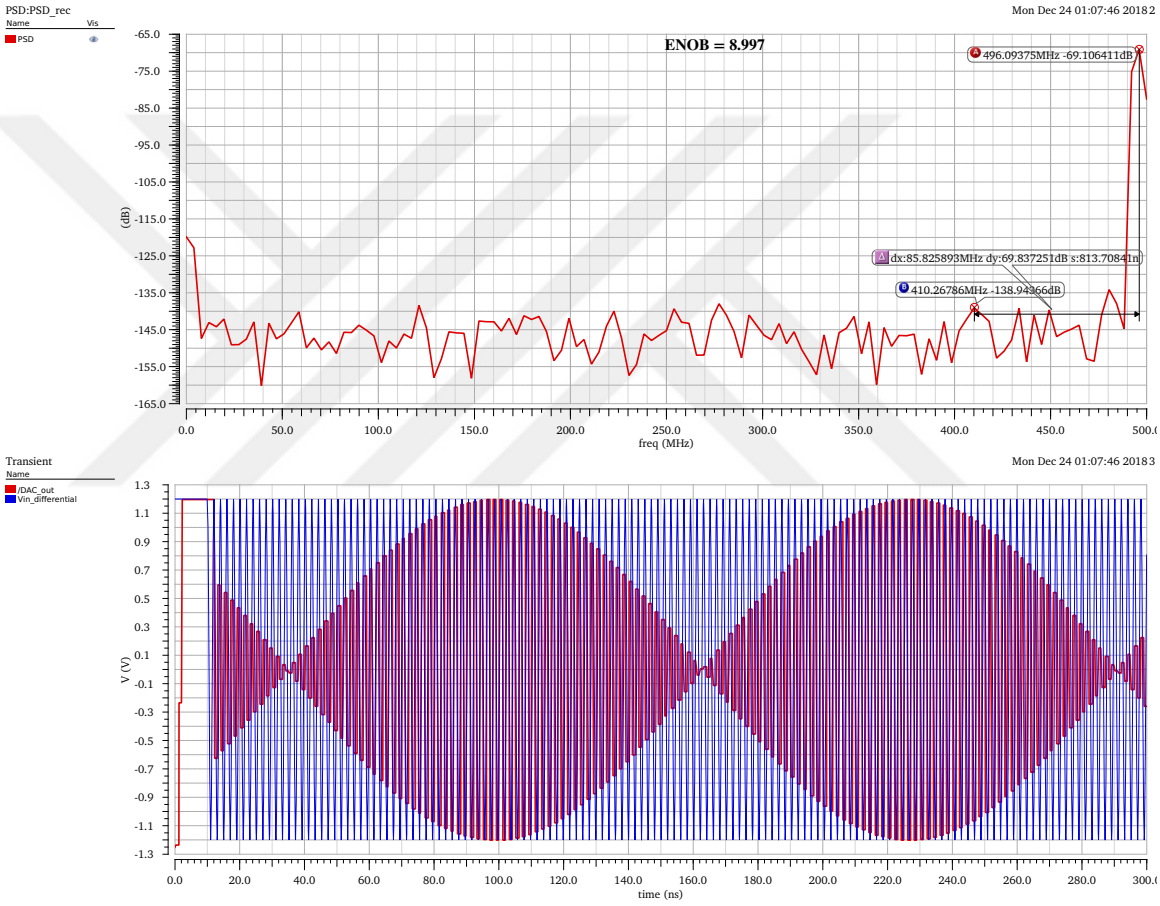


Figure 11: Spectrum , input, output at 497MHz frequency.

CHAPTER III

CIRCUIT DESIGN

This chapter presents the circuit implementation of the previously mentioned modeled SAR ADC. This system is designed using TSMC 65nm technology, for low power operation, the whole system operates at a supply voltage of 1.25 volt. Given an input range of 2.4 volts, the reference voltage is chosen to be the same as the supply voltage of 1.25 volt, assuming that the common mode voltage of the input signal is midway of the supply voltage of 625 millivolts. The following sections discuss the implemented circuits and their performance.

3.1 Capacitive DAC

SAR ADCs operation is considered as an iterative process. This operation depends mainly on adding and subtracting a specific fraction amount of the reference voltage from the sampled signal and comparing it deferentially to decide the bits. In order to dump the required charge each cycle, a DAC is required. Passive DACs are considered the best choice for SAR ADC for better power consumption. Resistive DACs are used in some applications. However, capacitive DACs show better area efficiency.

In this system, a unique capacitive DAC is introduced as in Figure.12. It is not binary weighted as in conventional DACs [2], but it has the same distribution illustrated in [8]. This distribution guarantees that only 1 switching takes place at a time. This also helped the control register units to be simple digital inverters, rather than analog switches, hence speeding up the switching process giving more margin for the comparator decision. Furthermore, since the operation starts by resolving the first-bit alone so a ratio of 1 to 2 is needed, proceed with the next 4 remaining cycles, where 1 to 3 or 2 to 3 ratio is needed. The distribution was designed in this manner

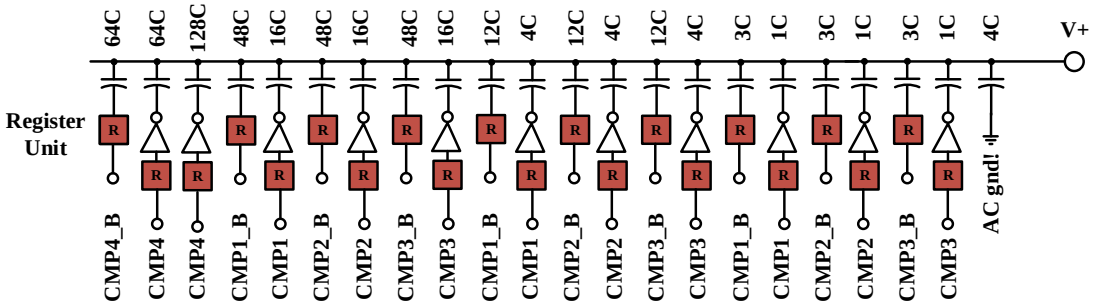


Figure 12: Single capacitive DAC representation.

accordingly.

The capacitive DAC is implemented using 1fF Metal-on-Metal(MOM) unit capacitance, resulting in a total capacitance of 512fF. The total capacitance of the single DAC is considered the sampling capacitance of the system. In the given technology the smallest MOM capacitance in the library is double our unit capacitance. Therefore, a custom-made unit capacitance is designed. Hence, it wasn't applicable to operate mismatch simulation to identify the standard deviation of the chosen unit capacitance. With the help of other previous studies [13], that have implemented and fabricated 0.5fF, 1fF, and 2fF unit structures using 65nm technology, it is concluded through their measurements that the mismatch factor can be below 0.3% 0.2% and 0.15% respectively. Relying on these values, INL and DNL are guaranteed to be less than 1/2 LSB .

3.2 Switches

Many switches are used in the design; sampling switches, interleaving switches, and 1-bit sampling switch. Each switch is elaborated in details in the following subsections.

3.2.1 Sampling Switch

Sampling switch is considered the most critical block in the system since any error taking place in the sampling phase cannot be retrieved in the subsequent processes. Therefore, sampling should have the best linear operation. CMOS switches are known to be input voltage-dependent, which make them not a good choice for their non-linearity. Bootstrapping switch is considered the most convenient solution as it assures that the source-gate voltage of the NMOS sampling switch remains constant with a value near the supply voltage [14]. The used switch is shown in Figure.13. It operates in a certain matter, where it samples the input on a boosting capacitance to boost the gate of the NMOS by the supply voltage added to it the input voltage.

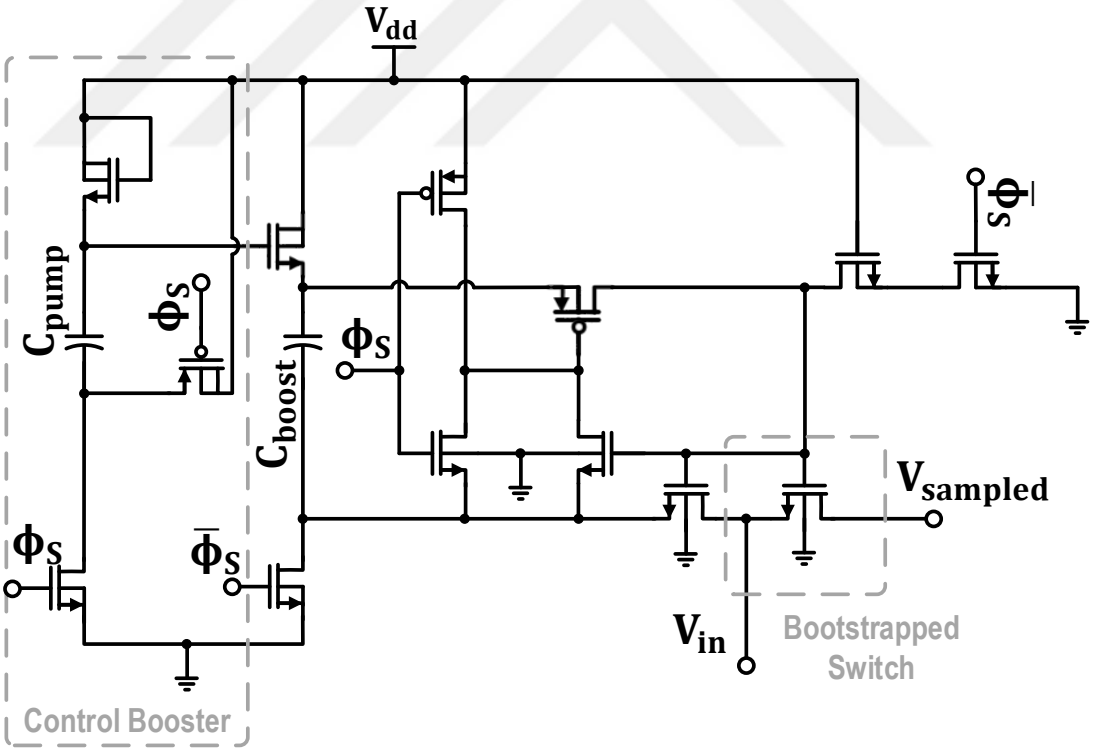


Figure 13: Designed bootstrapped sampling switch.

The bootstrapped NMOS transistor is sized according to the tracking period that is designed to be 500ps. For more accurate marginal calculation, the period is assumed

to be 400ps. Using equation (1), the NMOS ON resistance came to be 125Ω. Hence, this device has been sized accordingly, to have similar on resistance with a width of 16μm and minimum length of 60nm.

$$t_{tracking} = R_{sw} * C_u * 2^n * ln(2^n) \tag{1}$$

Figure. 14 and Figure. 15 show the operation of the sampling switch at 66MHz and 497MHz respectively. The sampled output tracks the input signal rapidly with a tolerable gain error at Nyquist and good tracking at the low frequency.

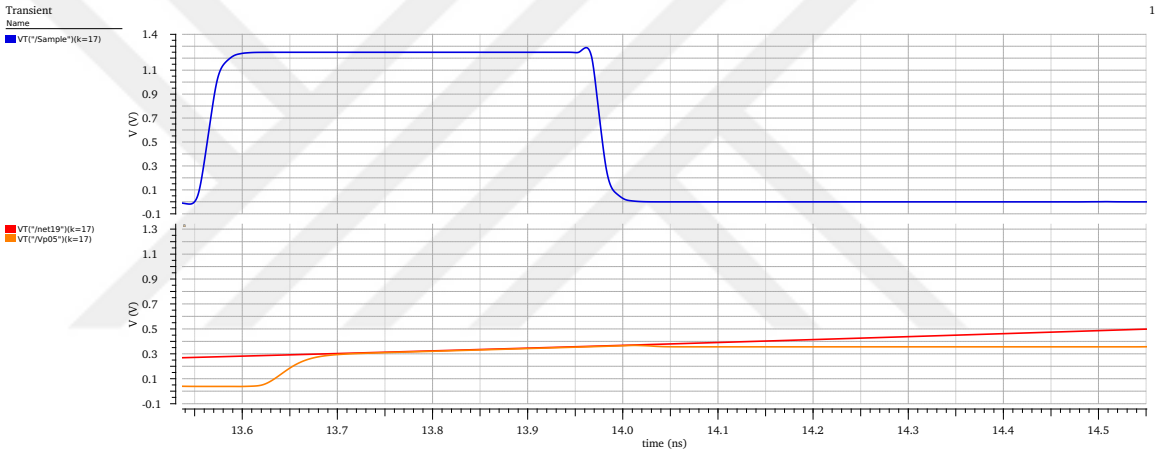


Figure 14: 66MHZ, Sampling.

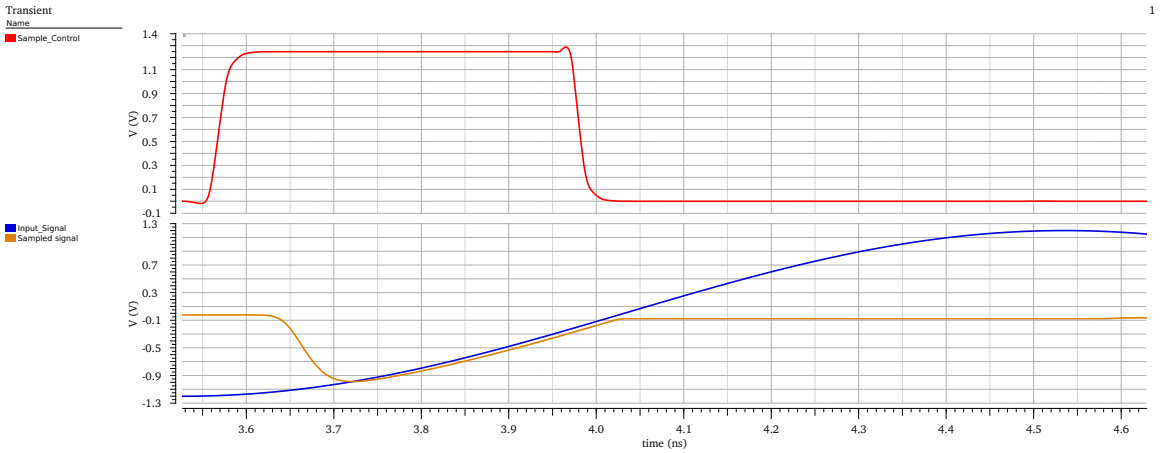


Figure 15: 497MHZ, Sampling.

3.2.2 Sampling 1-bit switch

Sampling 1-bit switch is a switch that samples the input directly to the extra comparator to resolve the first bit just after sampling. This switch is designed using the same circuitry of the bootstrapped switch, but hence its sampling capacitance is the comparator's input capacitance which is relatively smaller than the DAC capacitance, the sizing of this switch was proportionally designed to the difference between the capacitive loads.

3.2.3 Interleaving switch

This switch is a series-connected switch between the capacitive DAC and the comparator. There are various concerns regarding this switch that should be taken into consideration during the design. One advantage of having this switch is that it acts as a buffer between the DAC and the comparator as the comparators input capacitance is comparable with the unit capacitance that would have caused noticeable degradation in operation.

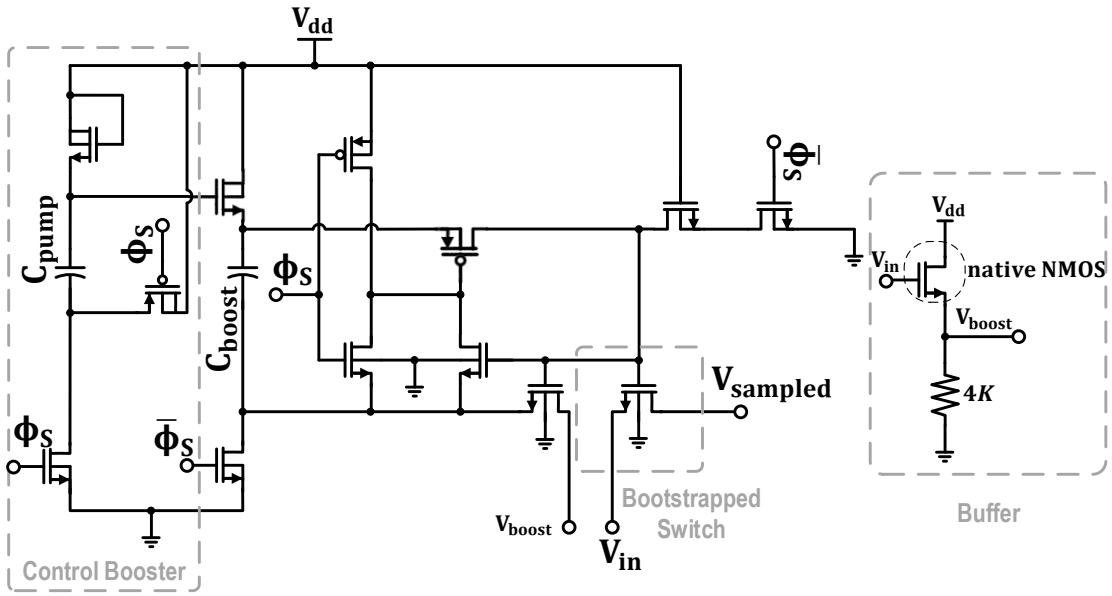


Figure 16: Interleaving bootstrapped switch.

It is decided to use bootstrapped switch for this switch as well, for its linearity properties. However, sampling a high impedance voltage might cause the signal level to drop significantly, consequently lowering the input dynamic range. A small circuitry was added to the bootstrapped switch shown in Figure 16. A source follower buffer is added to the sampling switch with a native NMOS device to increase the gain of this buffer. This buffer separates the input node from boosting path. Figure 17 shows the output of the interleaving switch with and without the buffer. The switch without the buffer shows a voltage drop of 13mV, while with the buffer only a 7mV drop is noticed.

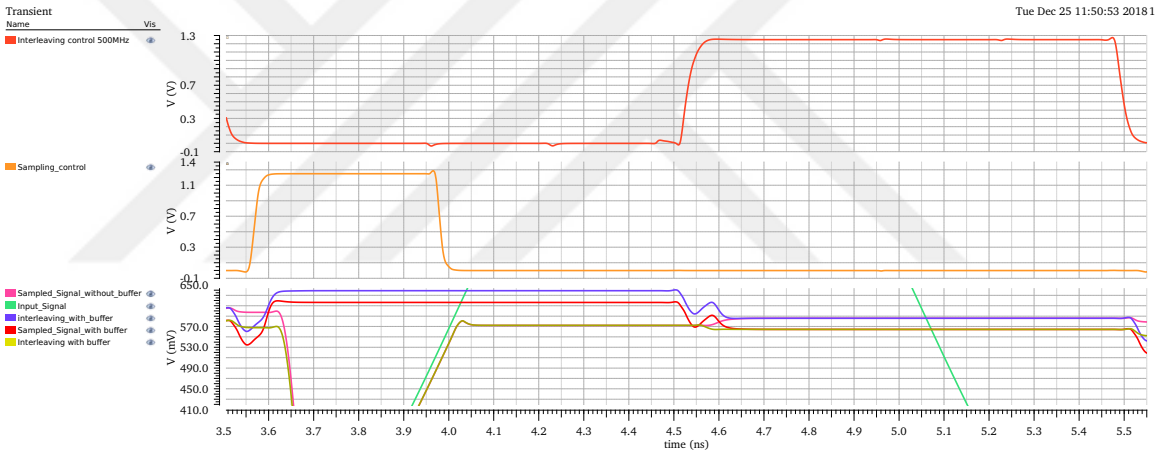


Figure 17: Sampled signal Vs. interleaved signal with and without the buffer.

A special testbench has been constructed to monitor the performance of the sampling switch and the interleaving switch together. Their spectrum analysis at Nyquist frequency is as shown in Figure 18.

3.3 Comparator Design

The comparator is the only active element in the design and it is considered as the second critical block in the system after the sampling switch. Voltage offset calibration circuit has been implemented to assure the best performance to the designed comparator. In Figure 19, it is shown that the comparator consists of 3 main stages;

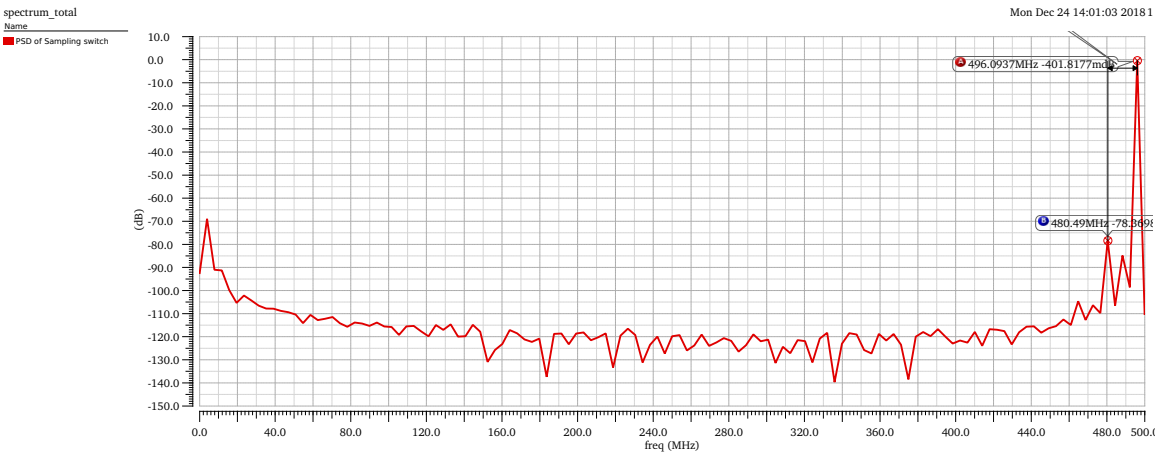


Figure 18: Sampling system spectrum.

pre-amplifier to amplify, latch stage, and SR-Latch. The pre-amplifier purpose is to boost the input signal to make the decision both easier and faster for the latch stage. Moreover, the pre-amplifier immunes the inputs from the kickback of the latch stage. Lastly, an SR-Latch is used to latch the outputs of the comparator differentially.

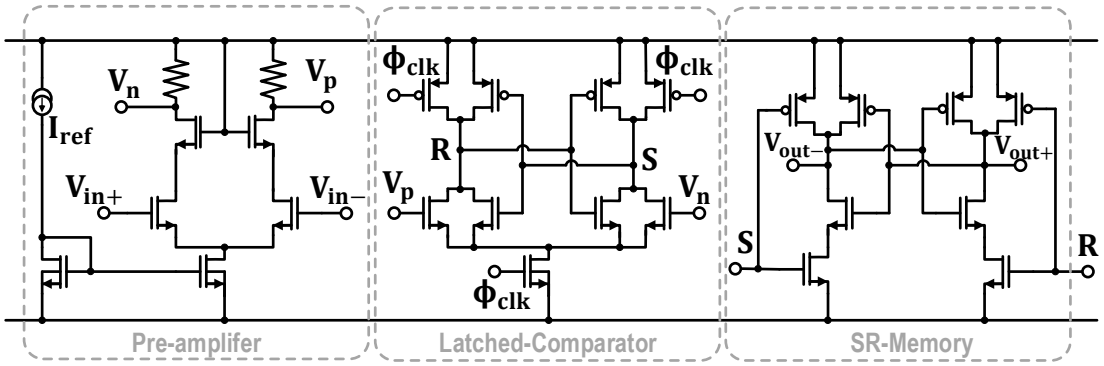


Figure 19: Comparator design.

Offset calibration circuitry has been added to the schematics of the pre-amplifier stage to balance any offset voltage in the circuit, 7 bit calibration resistors are added for this matter as shown in Figure 20.

A testbench has been constructed specially to measure the delay of the comparator at the worst case input of 500μV difference. It has been simulated twice; once with

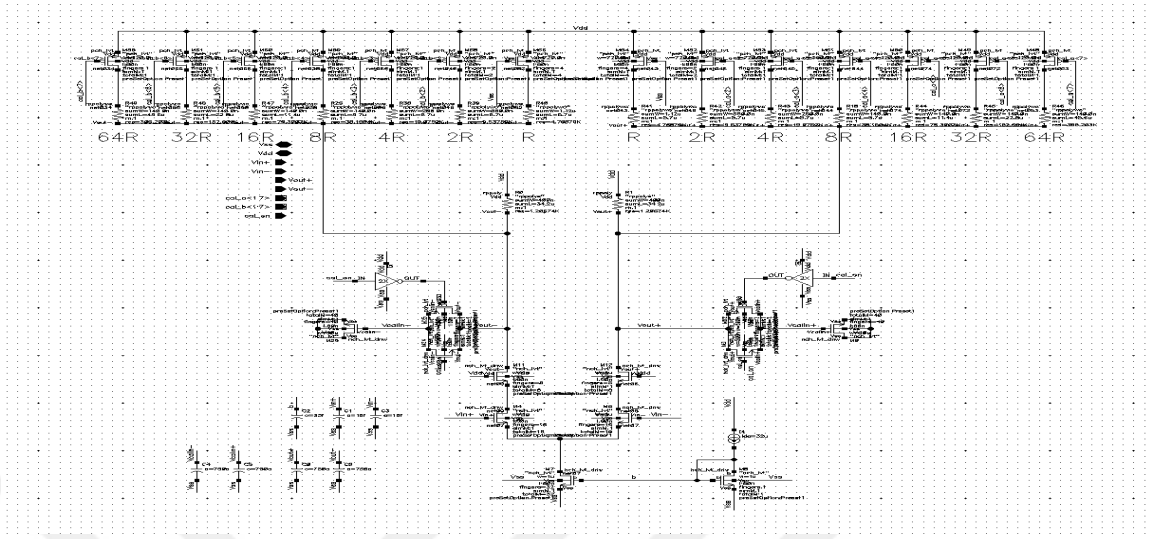


Figure 20: Pre-amplifier schematic with offset calibration circuitry.

the original design and the other with extra parasitic estimation capacitors added. The output delays have been noticed to be 78ps and 105ps for the original and with the parasitic estimation respectively. The waveforms in Figure 21 elaborate clearly the mentioned delays.

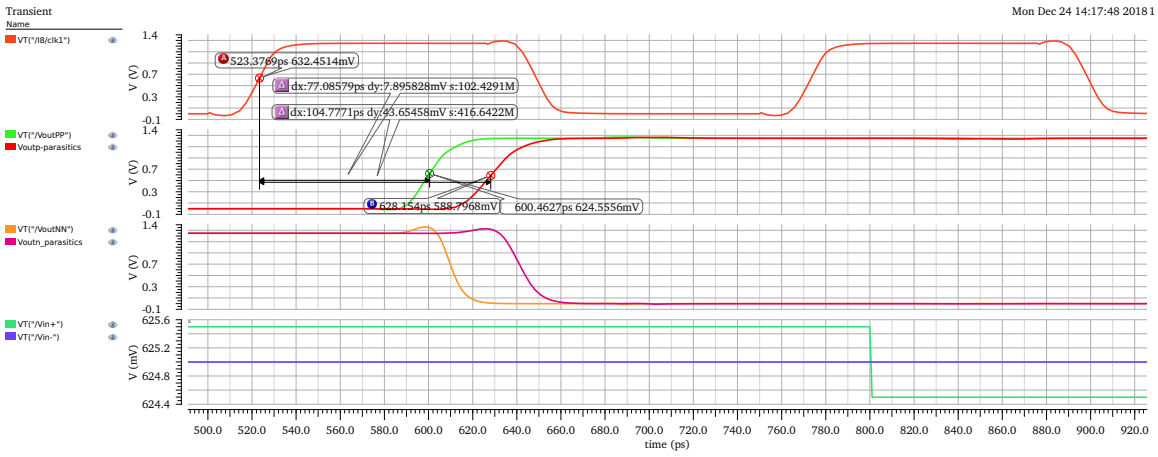


Figure 21: Comparator operation with and without parasitic estimation.

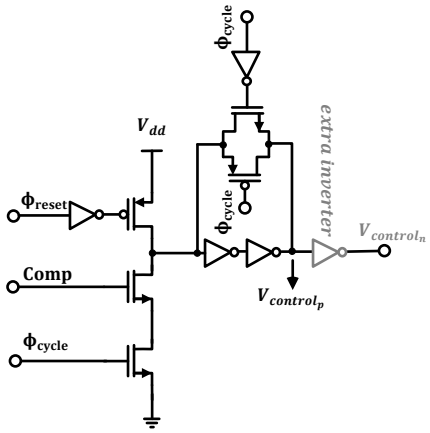


Figure 22: SAR Logic Unit

3.4 SAR LOGIC UNITS

The SAR logic unit is the interface between the comparator outputs and the capacitive DAC. As shown in Figure 12, each capacitance is either connected directly with register unit or with an extra inverter to get the inverted version of it. This SAR logic unit is as illustrated in Figure 22. The SAR logic unit consists of 2 stages; custom logic unit and inverters chain with a latch. All the capacitors are reset to their original state either Vdd or ground when the reset signal arrives. This reset signal is the sampling control signal. After reset, the logic is ready to sample the comparator output when the rising edge of the cycle control signal arrives. When the cycle control signal is down, the voltage on the output node is latched to assure no loss of charge.

This Logic unit is scaled according to the capacitor it is driving, to assure that all the signals have the same delay when they are fed back to the capacitors. Thus, these register units have been designed individually to have approximately the same delay. A testbench has been arranged and the delay is 49ps, and 75ps with parasitic estimations as shown in Figure. 23.

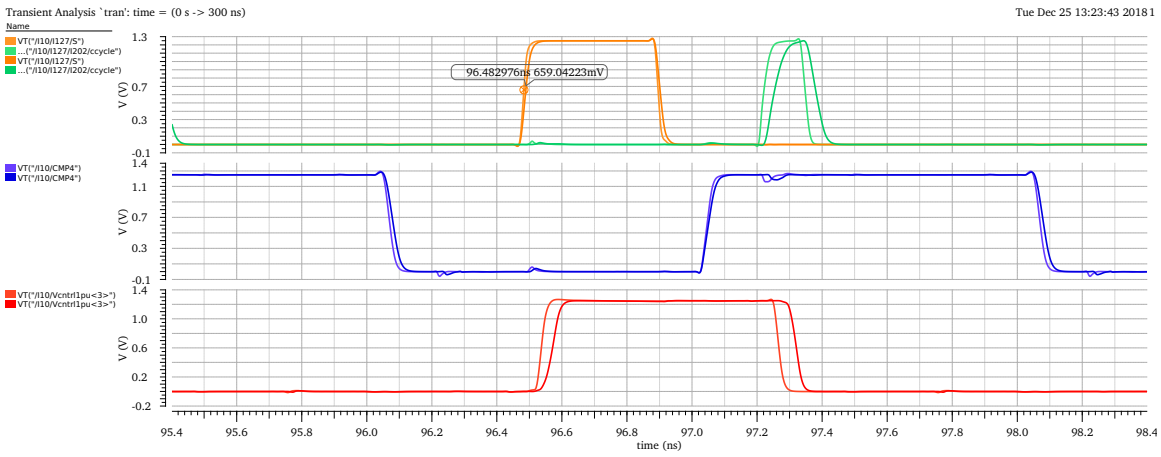


Figure 23: SAR LOGIC UNITS delay with and without parasitic estimations.

3.5 Clock Generator

The proposed system is a synchronous system. In order to maintain high performance, the control signals should be well synchronized. Therefore, a clock generator block is essential to generate every control signal needed by each unit block in our system. A 4-GHz clock is fed initially to the system. Consequently, any other controlled signal is generated using this 4-GHz clock. As illustrated in chapter 1, that the system operates at the 4 clock phases of a 1-GHz clock in addition to a 500-MHz clock required for interleaving. Therefore, clock division is necessary and is implemented as elaborated in Figure. 24.

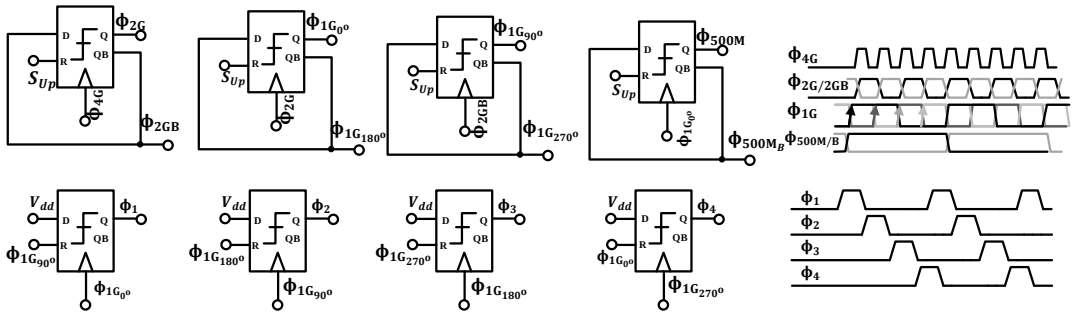


Figure 24: Clock dividers and control signals generation.

Operating at a high frequency, the conventional D flipflop isn't the best choice for clock division. A True Single Phase Clock D Flip-Flop (TSPC DFF) is designed for division purpose, where it has good performance and better power efficiency at high frequencies. In Figure 25, the used topology is shown. This circuit has carefully been designed to obtain a duty cycle of 50% which is necessary for clock phases alignment.

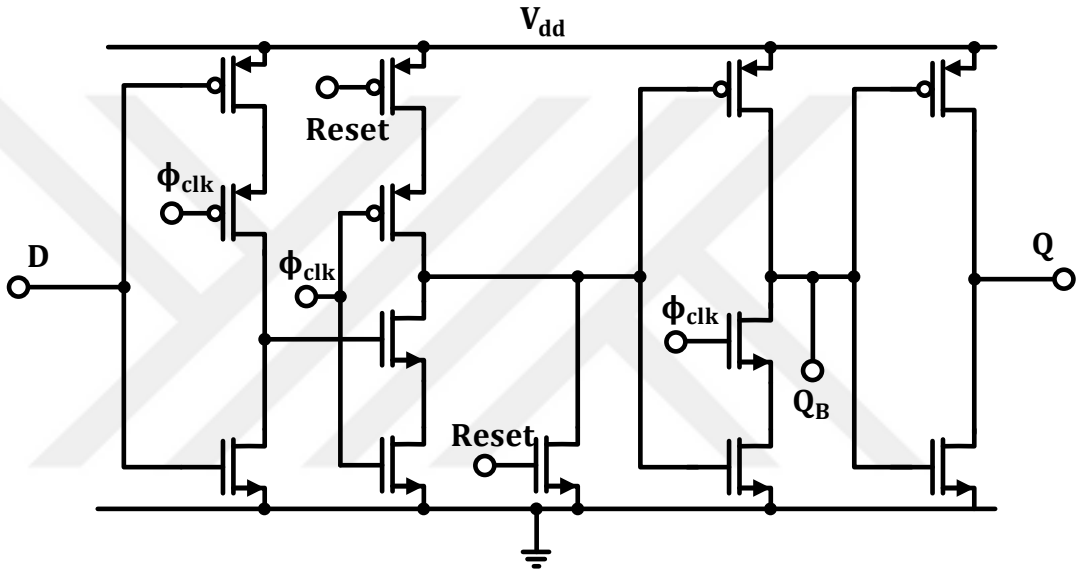


Figure 25: TSPC circuit design.

As previously illustrated in Figure 6, sample controls, 1st-bit sample controls, interleaving controls, and SAR register controls are to be defined. Figure 26 and 27 further explain the construction of previously mentioned control signals.

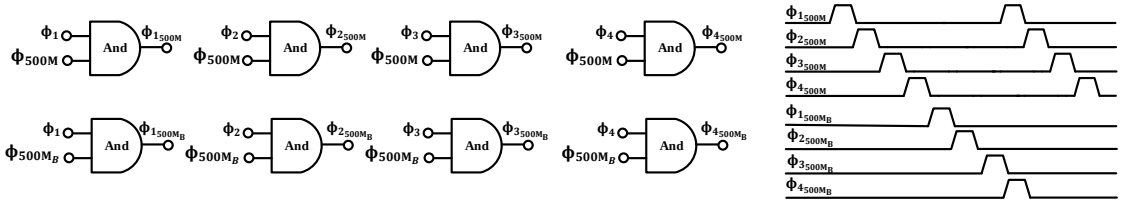


Figure 26: 4 phases interleaved clocks.

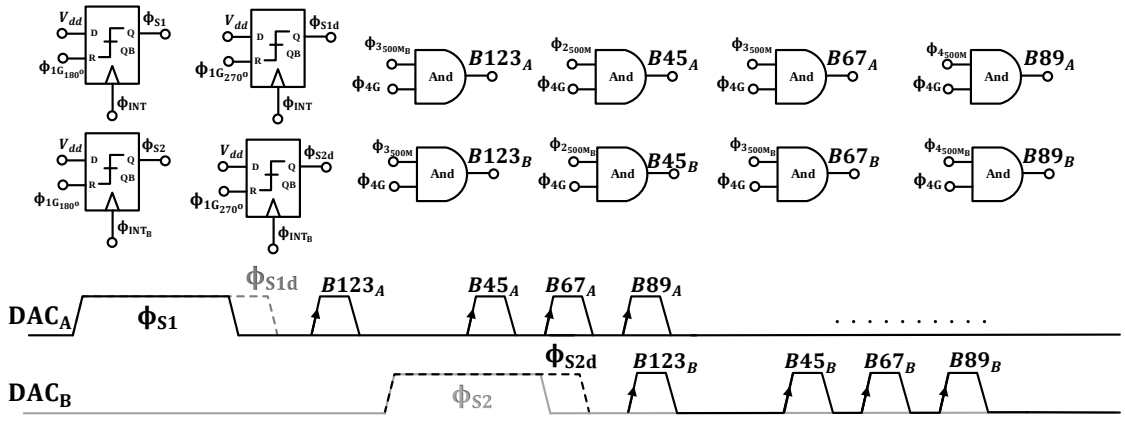


Figure 27: circuit control signals generator.

3.6 Memory register (output decoder)

After discussing thoroughly the operation of resolving the sampling signal, it is necessary to capture the output and translate it into output bits. As for the proposed system that has 9-bit resolution, with its unique scheme, the first bit is decided by latching the output of (Comp4) first thing after sampling. The remaining bits are decoded in a manner that even bits are decided by (Comp2) and odd bits are the output of a multiplexer whose inputs are (Comp1) and (Comp3) and their select is (Comp2). After latching each bit individually at a time, it is important to sample all the bits at the same time to deliver it in a periodic manner to the output. The output decoder is as shown in Figure 28.

In the decoder, the output delay is not a hard constraint at that time, where it only differs in the ADC overall latency but not sample to sample period. Therefore the used registers are chosen to be transmission-gate based DFF as shown in Figure 29.

3.7 Supply and reference buffers

The performance of the ADC is depending directly on the quality of the reference voltage. Therefore, the reference voltage should be buffered to the circuit with very small variations. Previously designed LDO buffers are used to buffer the ADC with the two voltages required; supply voltage and a reference voltage. These two buffers are used in a setup that is elaborated in Figure 30. An 8-bit trim code is necessary to produce the required voltage level with respect to the current pulled from the LDO. Using the average simulated value for the ideal supply and reference voltage sources for the whole ADC, the trim code for each buffer has been defined as in Table. 1. These reference voltage takes around 40μs to settle to the required voltage. Hence, It has been a hard task to simulate the whole ADC system with the buffers for that long time with high precision especially at this high-frequency operation. With liberal simulation for the whole system, the system shows an ENOB of 7.9 bits after the output of the buffer has settled.

Table 1: LDO 8-bits trim code for supply and reference buffers.

$Buffer$	$Bit7$	$Bit6$	$Bit5$	$Bit4$	$Bit3$	$Bit2$	$Bit1$	$Bit0$
Reference buffer	1	1	0	0	1	1	0	0
Supply buffer	1	1	1	1	0	0	0	0

Next chapter the system layout is briefly discussed followed by the simulation results elaborated in chapter 5.

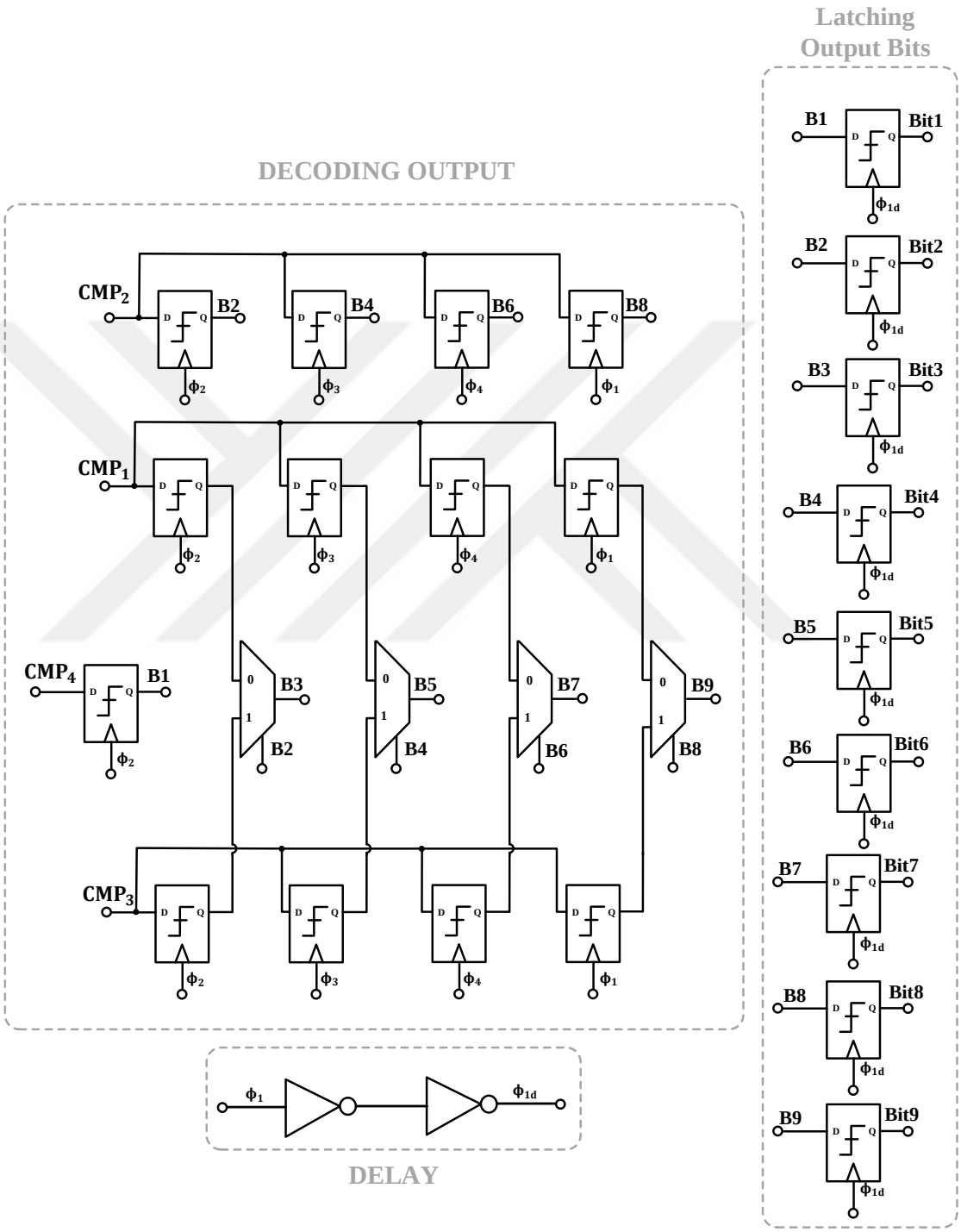


Figure 28: Output Decoder.

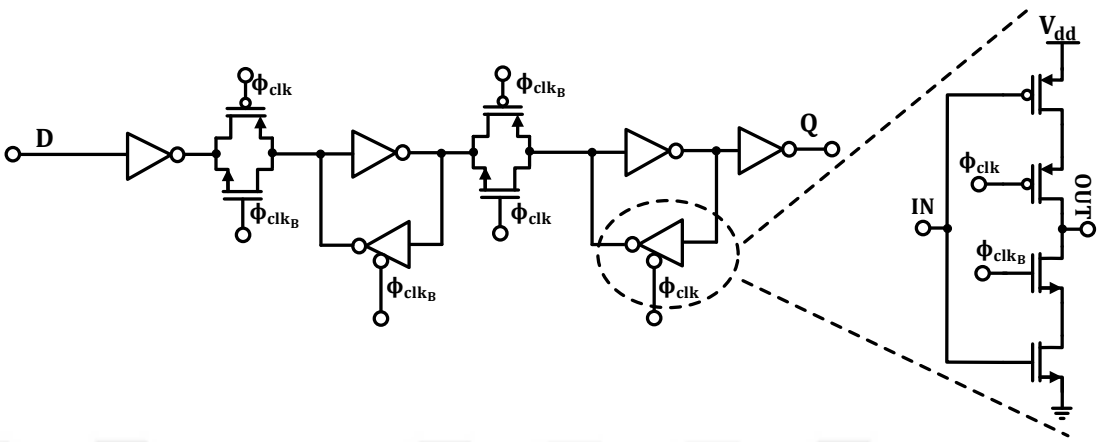


Figure 29: Transmission gate based DFF.

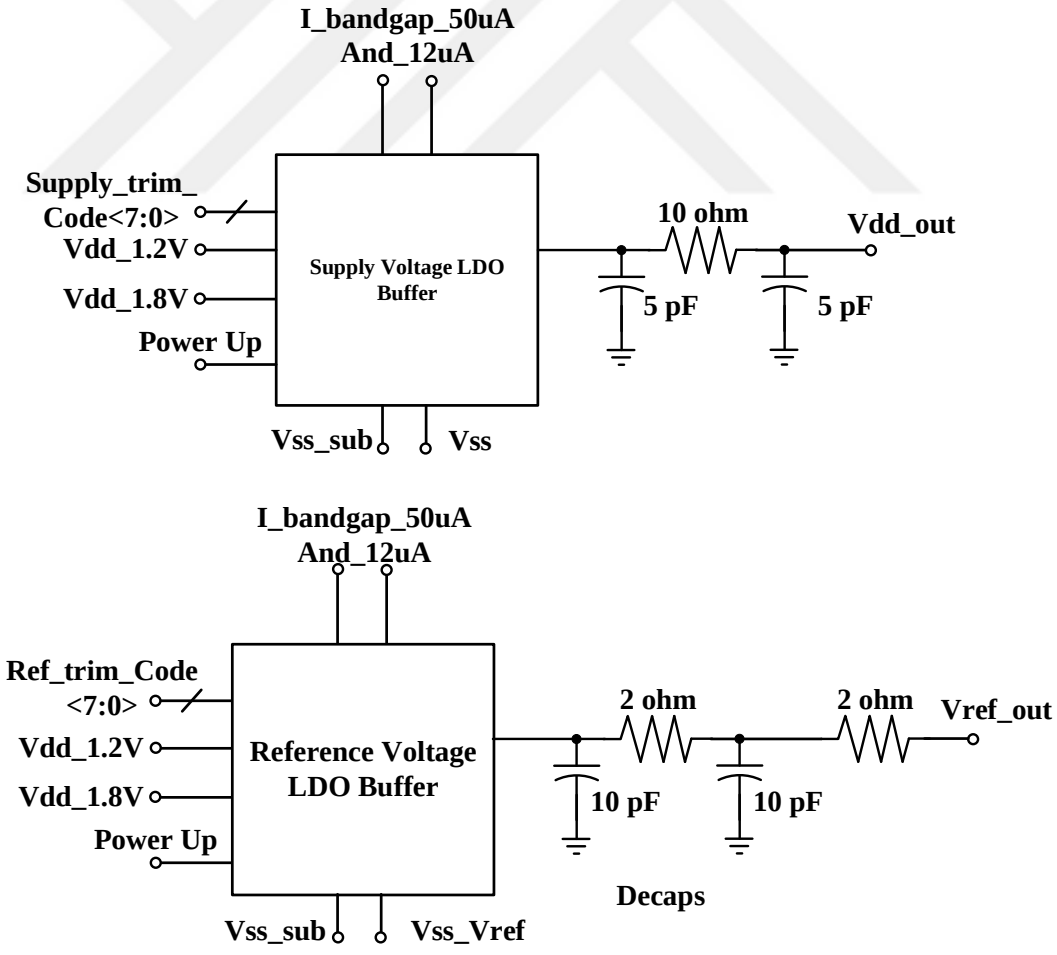


Figure 30: Supply and reference voltage LDO buffer setup.

CHAPTER IV

LAYOUT AND PLACEMENT

A layout floor plan early phase idea is mentioned in Figure. 31

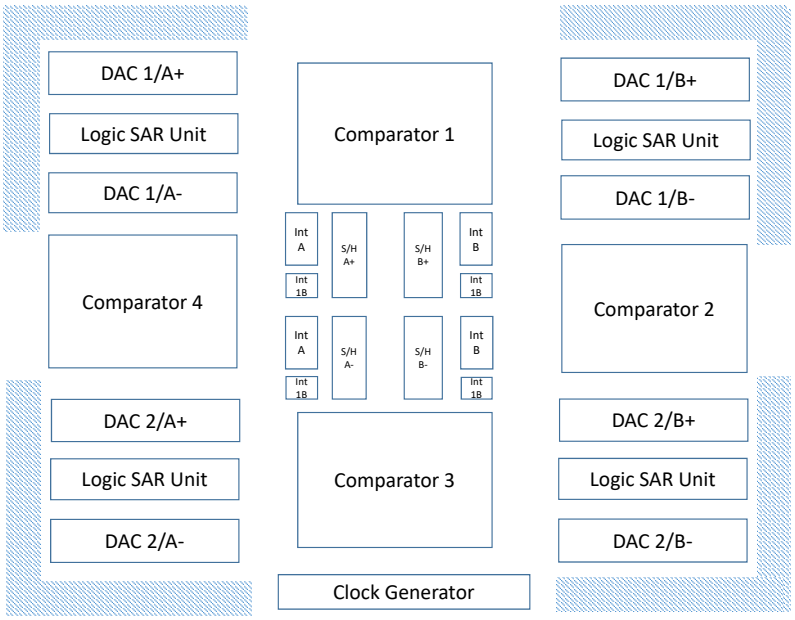


Figure 31: Early Idea of system layout

CHAPTER V

SIMULATION RESULTS

This chapter discusses the performance of the design in typical conditions. For typical spectrum analysis simulation, the full system is run under a constructed test-bench that takes 256bins. In Figure. 32 and 33 the spectrum of the output of the ADC modeled and real are illustrated for 66MHz and 496MHz frequencies respectively.

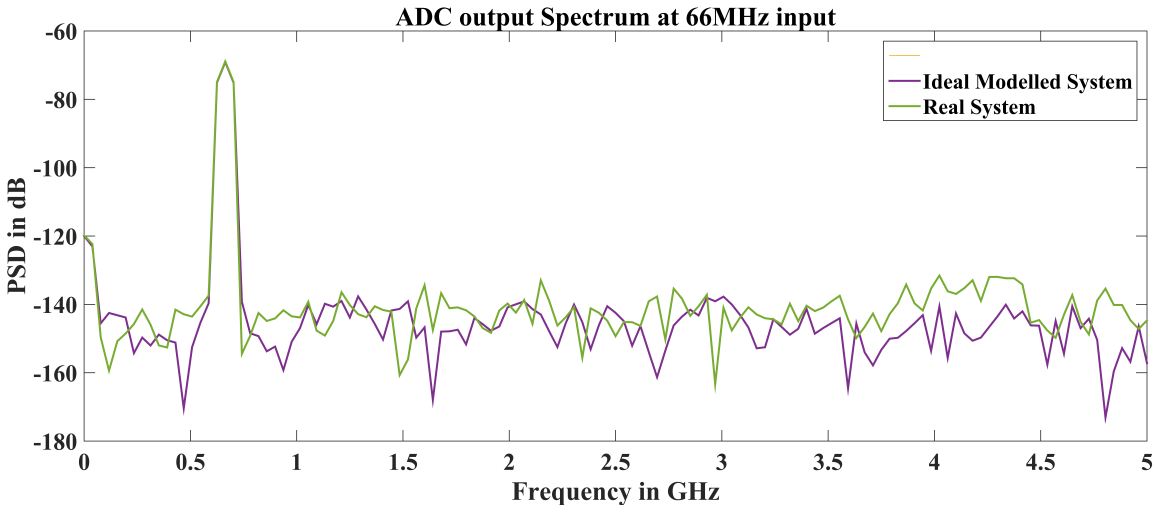


Figure 32: Ideal modelled Vs. Real system spectrum at 66MHz.

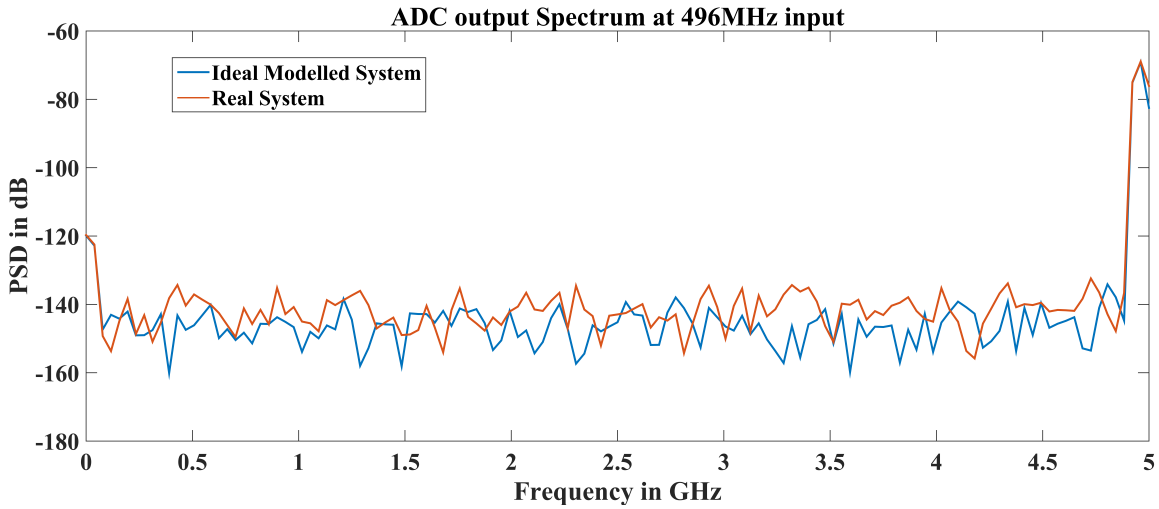


Figure 33: Ideal modelled Vs. Real system spectrum at 496MHz.

CHAPTER VI

CONCLUSION

The performance summary of the proposed work and some of the previous art are summarized in Table 2. A nontraditional SAR approach of this study provides a unique opportunity for a low-power robust ADC design in 65-nm with simple quadrature clock phases. Utilizing only one extra comparator, doubling up the passive C-DACs with corresponding interleaved timing an 8.5-bit ENOB performance could be attained with less than 13mA total current consumption from a single power supply of 1.25V.

Table 2: Comparison between the proposed work and previous work.

Publications	[8]IJSSC'18	[11]ISCAS'14	[15]CICC'17	This work
Architecture	2 X TI 2-b SAR	SAR	SAR	(2+1) then 2b SAR DAC TI
Technology	28nm	65nm	40nm	65nm
Supply (V)	0.9	1.2	1.2	1.25
Resolution	7	8	10	9
f_s GS/s	2.4	0.4	0.3	1
Unit Cap (fF)	-	2.5	0.5	1
Total Cap (fF)	64	4*640	935*0.5	4*512
Power (mW)	5	5.6	2.1	15
FoM (fJ/conv.-step)	25.3	67	19	38.37

Figure 34 shows the percentage of power consumption of each block in our system,while table 3 shows the exact current values consumed by each block as well.

Table 3: Current consumed by each block.

Comparators	Switches	SAR logic	Decoder	Clock Generator	Total
6.77mA	1.408mA	2.97mA	300μA	1.52mA	12.977mA

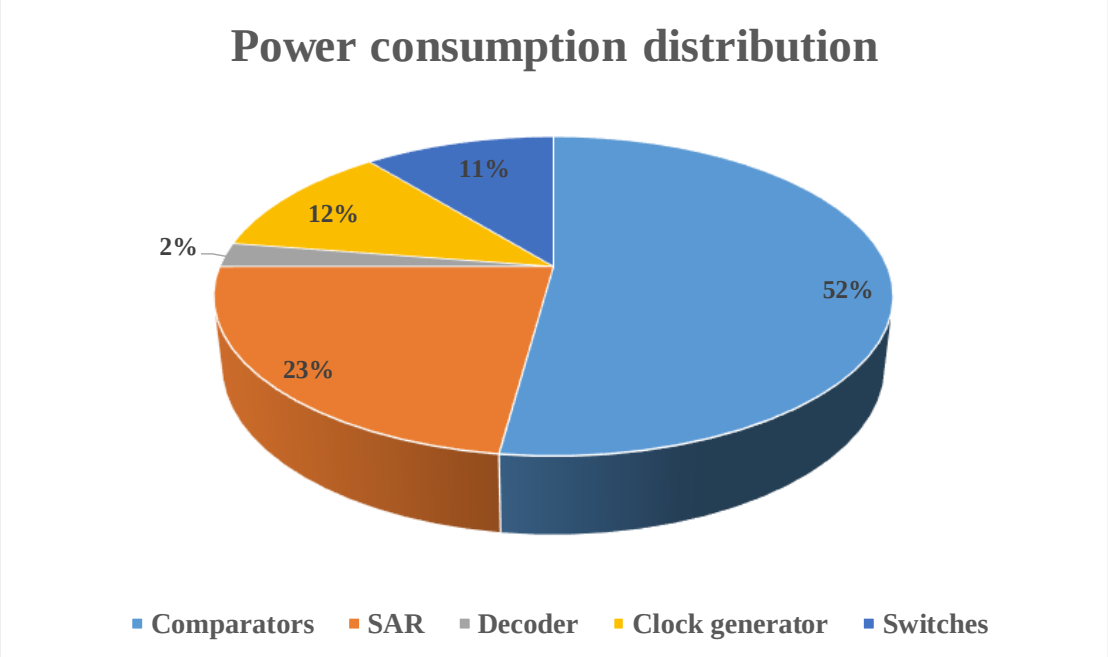


Figure 34: Power consumption distribution of each block in the proposed system.

CHAPTER VII

FUTURE WORK

For future work, finalizing the layout of the whole block will be a priority. Moreover, performing post layout simulations to assure robustness of the system. Meanwhile PVT simulations are on going.

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