DESIGN OF AN X-BAND GAN BASED MICROSTRIP MMIC POWER AMPLIFIER

A THESIS SUBMITTED TO

THE GRADUATE SCHOOL OF ENGINEERING AND SCIENCE

OF BILKENT UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR

THE DEGREE OF

MASTER OF SCIENCE

IN

ELECTRICAL AND ELECTRONICS ENGINEERING

By

Ulaş Özipek

February 2019

Design of an X-Band GaN Based Microstrip MMIC Power Amplifier
By Ulaş Özipek
February 2019

We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

Ekmel Özbay(Advisor)

Abdullah Atalar

Uğur Baysal

Approved for the Graduate School of Engineering and Science:

Ezhan Karaşan
Director of the Graduate School

ABSTRACT

DESIGN OF AN X-BAND GAN BASED MICROSTRIP MMIC POWER AMPLIFIER

Ulaş Özipek
M.S. in Electrical and Electronics Engineering
Advisor: Ekmel Özbay
February 2019

RF power amplifiers are crucial components of modern radar and communication systems. However, their design poses some challenges due to device limitations in high power and high frequency regime, as well as inherent difficulties of designing for nonlinear large-signal device operation. Gallium Nitride (GaN) based High Electron Mobility Transistors (HEMT) are promising candidates due to their superior material qualities, high power densities and ability to operate up to mm-wave frequencies.

In this thesis, 0.25 µm GaN on SiC microfabrication process of Bilkent University Nanotechnology Research Center (NANOTAM) is presented. Transistor characterization procedure is demonstrated. Ideal transistor layout for design goals is selected and the transistor gate structure is optimized for X-band performance. A model library for microstrip passive circuit elements based on electromagnetic simulations has been developed. Finally, design and measurements of an X-band microstrip Class AB two-stage Monolithic Microwave Integrated Circuit (MMIC) PA, based on the same process are presented in detail.

With die sizes smaller than 4.3 mm by 2.3 mm, fabricated MMICs operate at 8.5 - 11.5 GHz band with 24 dB small-signal gain. More than 13.5 W (41.3 dBm) output power (P_{6dB}) and 31 - 38 % power-added efficiency are achieved throughout the 8.5 - 11 GHz band in pulsed mode on-wafer measurements.

Keywords: Gallium Nitride, MMIC, microwave, X-band, power amplifier.

ÖZET

X-BANT GAN TABANLI MİKROŞERİT MMIC GÜÇ YÜKSELTECİ

Ulaş Özipek
Elektrik ve Elektronik Mühendisliği, Yüksek Lisans
Tez Danışmanı: Ekmel Özbay
Şubat 2019

RF ve mikrodalga güç yükselteçleri, günümüz iletişim ve radar sistemlerinin hayati bileşenlerindendir. Bu bileşenlerin tasarımları, yüksek güç ve yüksek frekans rejimindeki aygıt kısıtlamaları ile; doğrusal olmayan büyük-işaret çalışma koşullarında tasarımın kendi çetinlikleriyle birlikte, ciddi zorlukları da beraberinde getirmektedir. Galyum Nitrür (GaN) tabanlı yüksek elektron hareketlilikli transistör (HEMT) teknolojisi, yüksek güç yoğunlukları, mm-dalga frekanslarına kadar çalışabilme kabiliyetleri ve üstün malzeme özellikleriyle, önemli bir potansiyel barındırmaktadır.

Bu çalışmada, Bilkent Üniversitesi Nanoteknoloji Araştırma Merkezi'nde (NANOTAM) geliştirilen 0.25 µm Silisyum Karbür (SiC) tabanlı GaN mikrofabrikasyon prosesi, ve bu proses ile üretilen aygıtların karakterizasyon adımları gösterilmiştir. X-bant uygulamalarına yönelik transistör başarımının iyileştirilmesi için gerçekleştirilen deneysel transistör serimi ve kapı geometrisi tarama çalışmaları sunulmuştur. Pasif devre elemanlarının elektro-manyetik benzetim tabanlı model kütüphanesi oluşturulması anlatılmıştır. Son olarak, X-bant için tasarlanan monolitik mikrodalga entegre devre güç yükselteci tasarımı ve adımları, ayrıntılı biçimde açıklanmıştır. Üretilen yükselteç devrelerinin benzetim ve ölçüm sonuçları paylaşılarak yorumlanmıştır.

Yonga boyutları 4.3 mm x 2.3 mm'nin altında olan devreler, ölçümlerde 8.5 GHz - 11.5 GHz frekans aralığı boyunca 24 dB üzerinde küçük işaret kazancı vermektedir. 13.5 Watt (41.3 dBm) üzerindeki çıkış güçleri ve %31 ile %38 arası güç ekli verimlilik değerleri, oda sıcaklığında gerçekleştirilen darbeli mod ölçümlerinde 6 dB kazanç kısılması altında, 8.5 GHz - 11 GHz bandı boyunca elde edilmiştir.

Anahtar sözcükler: Galyum Nitrür, MMIC, mikrodalga, X-bant, güç yükselteci.

Acknowledgement

I would like to extend my regards to my advisor Prof. Ekmel Özbay for providing the basis and opportunity for this work. To whom wits and discipline I can only aspire to. He was a continuous source of support and motivation throughout my studies while also permitting a vast space of freedom.

I wish to express my sincere gratitude to Prof. Abdullah Atalar, whose character and ingenuity to seamlessly fuse profoundness and clarity, inspires many young people, and whom I was fortunate enough to be a student of.

My luck continued as I met Dr. Özlem Şen as my first supervisor and later mentor, from whom I learned not only many technical aspects related to field, but also the virtues of kindness, diligence and humility.

I was surrounded by brilliant colleagues at NANOTAM RF group, with whom I enjoyed working and learning together. Although each one of its past and current members are *sui generis*, I should mention Armağan Gürdal for his collaboration during the course of this work. Without his ambition, scientific curiosity, inquisitiveness and diligent efforts; many aspects of this work would be lacking. And also I should thank Muhammet Kavuştu for his comradeship throughout the journey of our studies.

I would like to celebrate the tireless efforts of NANOTAM fabrication team in pioneering the development of a GaN process.

Last but not least, I would like to offer my love and respects, to my family and friends, for providing me with inspiration and motivation, strength and passion.

I would also like to thank Prof. Baysal for reviewing this thesis.

I hereby dedicate this work to all my teachers and to people who work altruistically towards dissemination and the pursuit of knowledge.

Contents

1 Introduction **1**

2 Technology and Process Overview **3**

2.1 Why GaN 3

2.2 NANOTAM GaN Microfabrication Process Overview 6

3 Transistor Characterization **13**

3.1 DC Characterization 13

3.2 RF Small-Signal Measurements 16

3.3 Large-Signal (Load-Pull) Measurements 18

4 MMIC Design **22**

4.1 Transistor Optimization 23

4.1.1 Layout Design/Comparison/Selection 25

4.1.2 Parametric Gate Study 29

4.2 Topology Selection 33

4.3 Passive Component EM Model Library 37

4.4 Stability 40

4.4.1 Even-Mode Stability 41

4.4.2 Odd-Mode Stability 44

4.5 Bias and Matching Networks 49

4.5.1 Gate and Drain Bias Networks 50

4.5.2 Output Matching 52

4.5.3 Interstage Matching 57

4.5.4 Input Matching 60

5 Measurement Results and Analyses 65

5.1 Measurement Setup 65

5.2 Measurement Results 66

5.2.1 Small-Signal Measurements 66

5.2.2 Power Sweep Measurements 67

5.3 Discussions and Future Work 71

6 Conclusion 73

List of Figures

2.1 Transistor technology performances in high frequency and high power domains 4

2.2 Comparison of various performance metrics for transistor semiconductor materials 4

2.3 Thermal camera image from an operating GaN MMIC where temperature peaks can be seen in gate finger/channel locations 5

2.4 A perspective drawing of the epitaxial and fabrication layers in a GaN HEMT device 7

2.5 Cross-sectional drawing of the wafer after GaN epitaxial growth on SiC substrate at the beginning of fabrication 8

2.6 Cross-section of wafer after ohmic metallization step 9

2.7 Cross-section of wafer after first passivation step 9

2.8 Cross-section of wafer after gate-foot dielectric opening and gate metallization 10

2.9 Cross-section of wafer after 2nd passivation step 10

2.10 Cross-section of wafer after TFR coating and gate field plate metallization 11

2.11 Cross-section of wafer after Metal 1 layer coating and final dielectric passivation 11

2.12 Cross-section of wafer after air-bridge formation and thick metal layer coating step 12

2.13 Cross-section of wafer after finalization of backside fabrication process 12

3.1 On-wafer DC-IV measurement setup 13

3.2 IV curves of a 8×125 µm HEMT 14

3.3 g_m and I_{DS} vs V_{gs} curves of 8×125 µm HEMTs 15

3.4 Gate & drain leakage or breakdown characteristics of a 8×125 µm HEMT 15

3.5 CW on-wafer small-signal measurement setup 16

3.6 RF measurement setup with DC pulsers and thermally controlled chuck for measurements in pulsed mode and at different temperatures 17

3.7 Input and output reflection coefficients of 8x125 µm HEMTs . . . 17

3.8 Forward transmission characteristics of 8x125 µm HEMTs under CW operation at room temperature 18

3.9 Measurement and device reference planes 18

3.10 G_t, PAE and P_{out} contours of an 8 × 125 µm HEMT at 10 GHz under 3 dB gain compression 19

3.11 Maury VNA based passive load-pull bench 20

3.12 Block diagram of the vector network analyzer based load-pull system 20

3.13 P_{out} circles of an $8 \times 125\,\mu m$ HEMT at 10 GHz under 3 dB gain compression 21

4.1 Photomask view of the microstrip transistor reticle 23

4.2 Relation between total gate periphery and small-signal performance 25

4.3 Photomask views of 4 HEMTs with 1 mm gate peripheries and different finger configurations 26

4.4 Transistor layout parameters as marked on the SEM image are: a) gate width, b) drain contact length, c) source contact length and d) drain-to-source distance or channel length 27

4.5 Geometry of gate structures and corresponding surface electric field intensities 29

4.6 G_T (green) and P_{3dB} (red) load-pull contours (@ 10 GHz) of the HEMT type with the best power density at 3 dB compression . . 32

4.7 G_T (green) and P_{3dB} (red) load-pull contours (@ 10 GHz) of the HEMT type with better large-signal gain at 3 dB compression . . 32

4.8 Power sweep simulation of 2 stage MMIC with 2:4 topology at 10 GHz 34

4.9 Power sweep fittings for a) 1st and b) 2nd stage transistors and load-pull measurements superposed 35

4.10 Power sweep simulation of 2 stage MMIC with 1:4 topology at 10 GHz 35

4.11 Power sweep fittings for a) 1st and b) 2nd stage transistors and load-pull measurements superposed 36

4.12 Power simulation results at 6 dB compression for 2:4 topology in 8.5 GHz - 11 GHz band 36

4.13 Schematic and EM model data table view of spiral inductor . . . 37

4.14 EM substrate stack used in ADS 38

4.15 Layout of the on-chip spiral inductor that correspond to 600 pH . 39

4.16 Comparison of inductor measurement and simulation results with ideal inductor response 39

4.17 Comparison of transmission line measurement and simulation results with ideal TL response 40

4.18 Stability and MAG of a 8x125 µm HEMT before stabilization . . . 42

4.19 Layout of the transistor with input stability cell 43

4.20 Layout partitioning of 1st and 2nd stages in even-mode stability tests 43

4.21 Even-mode stability results of both stages 44

4.22 One of the ADS schematics for calculating odd-mode impedances and admittances at the input and output of 2nd stage transistors for odd-mode stabilization 45

4.23 Schematic representations of odd excitation modes 46

4.24 Highlighted odd-mode suppression resistors between the gate and drain manifolds of the HEMTs 46

4.25 Odd-mode impedances calculated at the input and output of 2nd stage transistors before odd-mode stabilization 47

4.26 Odd-mode impedances calculated at the input and output of 2nd stage transistors after odd-mode stabilization 48

4.27 Odd-mode admittances calculated at the input and output of 2nd stage transistors after odd-mode stabilization 48

4.28 Schematic and merged layout views of a meandered microstrip transmission line 49

4.29 Frequency responses of schematic simulation vs. merged layout of a meandered transmission line structure 50

4.30 SEM images of on-chip inductors 51

4.31 Layout view of the 1st stage gate and drain bias networks 51

4.32 RF isolations of a) 1st stage gate and b) drain bias networks . . . 52

4.33 P_{out} (red) and G_T (green) contours of the 8x125 µm HEMT under a) 0.5 dB and b) 4.5 dB G_T compression 53

4.34 Layout (a) and schematic (b) view of the 2nd stage transistors and OMN (TL electrical lengths in schematic view are @10GHz) . . . 54

4.35 P_{out} (red), transducer gain (green) and drain efficiency (blue) contours of the 8x125 µm HEMT at 3 dB compression at 10 GHz . . 54

4.36 P_{out} contours of the 8x125 µm HEMT at a) 8.5 GHz and b) 11 GHz at 3 dB compression 55

4.37 Load impedances presented to output stage transistors between 8.5 GHz - 11 GHz 55

4.38 Impedance and phase asymmetry between OMN branches at 8.5 GHz - 11 GHz band 56

4.39 Net insertion loss of output matching network at 8.5 GHz to 11 GHz band in dB scale 57

4.40 Source-pull contours of an 8x125 µm HEMT at 3 dB compression at 9.5 GHz 58

4.41 Schematic view of top half of the interstage matching network (TL electrical lengths are given @10GHz) 58

4.42 Layout view of top half of the interstage matching network 59

4.43 Output stage source (a) and driver stage load (b) impedances at 8.5 GHz - 11 GHz band 59

4.44 Net insertion losses of interstage and output matching networks at 8.5 GHz to 11 GHz band in dB scale 60

4.45 Schematic view of the input matching network (TL electrical lengths are defined @10GHz) 61

4.46 Layout view of the input matching network 61

4.47 Source impedances presented to 1st stage transistors 62

4.48 Calculated source-pull contours of an 8x125 µm HEMT at 1 dB compression at 9.5 GHz 62

4.49 Small-signal simulation results of the design, performed using S-parameter data of 30 HEMTs 63

4.50 Schematic view of the finished design (given TL electrical lengths are @10GHz) 64

4.51 Layout view of the finished design 64

5.1 SEM view of a fabricated MMIC 66

5.2 S-parameter measurement results of the fabricated 25 MMICs . . 66

5.3 S-parameter measurements (darker tones) and simulation results (lighter tones) superposed 67

5.4 Output power, large-signal gain and PAE results of a fabricated MMIC at 8.5 GHz - 11 GHz band at 6 dB compression 68

5.5 Power sweep measurements of MMICs at 8.5 GHz 69

5.6 Power sweep measurements of MMICs at 10 GHz 69

5.7 Power sweep measurements of MMICs at 11 GHz 69

5.8 Comparison of large-signal measurements and power simulation results of a MMIC 70

List of Tables

2.1 Semiconductor material properties comparison of Si, GaN, GaAs and SiC 5

2.2 Baliga's, Baliga's High Frequency, Johnson's and Keyes' figure of merits for Si, GaN, GaAs and SiC 6

2.3 Properties of grown wafers and typical 2DEG performance 8

3.1 Overall DC, RF and load-pull results of 8x125 µm HEMTs 21

4.1 G_{TUmax}, power and large-signal gain comparison of 1 mm HEMTs with different finger configurations 26

4.2 G_{TUmax} comparison of transistors @12 GHz with various drain & source contact lengths versus channel lengths 28

4.3 Load-pull results (at 10 GHz) of different contact length variants are compared at 25 °C and 110 °C base temperatures 28

4.4 Output power and large-signal gain comparison of transistors at 3 dB compression at 10 GHz, for gate geometries without SCFP structures 31

4.5 Large-signal performance comparison of gate geometries with SCFP structures at 10 GHz 31

4.6 Design specifications of the power amplifier 33

4.7 Power output and gain of the 8x125 µm HEMT (at 3 dB compression) used in design 33

4.8 2nd stage load impedances presented by OMN 56

4.9 1st stage load and 2nd stage source impedances presented by ISMN 60

4.10 Load and source impedances presented to 1st stage transistors . . 62

5.1 Table of power measurement results of a fabricated MMIC at 8.5 GHz - 11 GHz band at 6 dB gain compression 68

5.2 Performance comparison of measured MMIC results with commercial counterparts 72

Chapter 1

Introduction

X-band of the electromagnetic spectrum is utilized by many radar and communications systems. Power amplifiers (PA) are crucial elements of transmitter modules in these systems since their output power and efficiency figures largely define overall system performance. Their design however, poses some challenges due to material limitations in high power and high frequency regime, as well as inherent difficulties of designing for nonlinear large-signal device operation. Ever increasing demand for better performance in modern systems, require higher output power and efficiency values, while keeping overall dimensions as small as possible. Especially in systems where an array of modules are tightly stacked together, minimizing the chip size without compromising the output power capabilities becomes imperative.

For these reasons, Gallium Nitride (GaN) based High Electron Mobility Transistors (HEMT) are promising candidates due to their superior material qualities. High breakdown voltages of GaN transistors enable them to achieve high power densities. Their ability to withstand high junction temperatures during operation is a favored characteristic for PA design. Monolithic Microwave Integrated Circuit (MMIC) technology is well suited to realize amplifier designs in a small die area with high performance, reliability and low cost [1]. Therefore, GaN MMICs receive a great deal of attention from academics and commercial field [2–12].

This thesis presents design and measurements of a 2-stage microstrip GaN power amplifier MMIC, fabricated using Bilkent University NANOTAM's 0.25 µm GaN on Silicon Carbide (SiC) process. MMICs operate at 8.5 - 11.5 GHz band with small-signal gain of 24 - 29 dB and pulsed mode output power of more than 14 W at 6 dB compression. These gain and output power figures are comparable with similar commercially available chips [13, 14].

Properties GaN on SiC HEMT technology are examined and a brief overview of NANOTAM microfabrication process is given in 2nd chapter. 3rd chapter details the DC, small-signal RF and large-signal characterization steps of transistors. Detailed MMIC design process is described in chapter 4. Starting from the transistor selection and optimization phase, passive component model library development, amplifier topology selection, transistor stabilization and design of matching networks are explained. In chapter 5, small-signal and power measurement results of MMICs are presented. Simulations are compared with measurement results and possible future works are discussed.

Chapter 2

Technology and Process Overview

2.1 Why GaN

Gallium Nitride is a relatively new semiconductor material when compared to other mature technologies such as Gallium Arsenide and Silicon. However it quickly dominated several fields of applications (Fig. 2.1) where high frequency and high power are required [15] such as radars, transmitter systems, satellite communications, etc.

Popularity GaN technology in high power RF applications stems from its three main properties which distinguishes it from its rivals: high breakdown field, high saturation velocity and superior thermal properties (Fig. 2.2) [16].

Large bandgap of the GaN leads to higher breakdown field capability as seen on Table 2.1, which provides the opportunity for much higher operating voltages. Secondly, high saturation velocity in the two-dimensional electron gas (2DEG) channel in GaN devices allows for high current densities. Larger voltage and current swings means that RF output power capacity (which is simply approximated

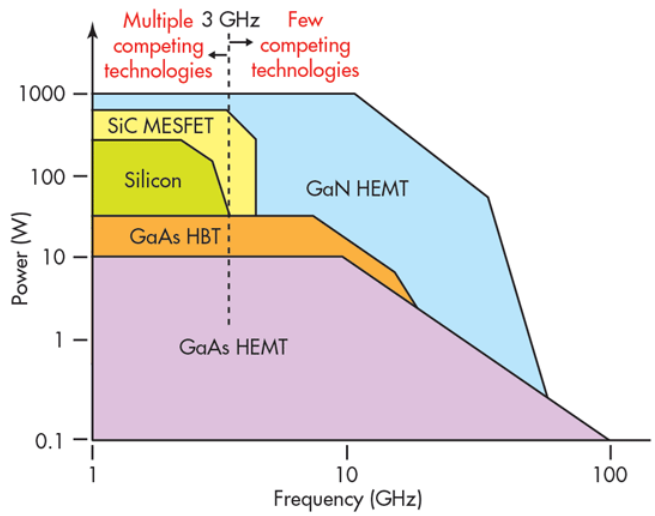


Figure 2.1: Transistor technology performances in high frequency and high power domains

source: electronicdesign.com [15], original source: RF Micro Devices, Inc.

by the product of these two values) will be higher.

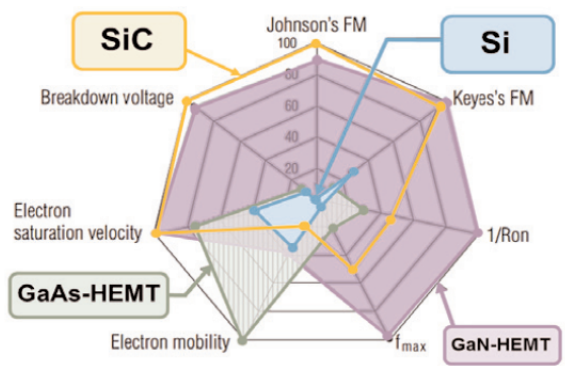


Figure 2.2: Comparison of various performance metrics for transistor semiconductor materials

source: semiconductor-today.com [16], original source: OKI Semiconductors

In addition to high RF power densities, GaN devices offer another crucial element of superior thermal properties. Although the thermal conductivity of bulk GaN is comparable to Silicon, its maximum operating temperature is much higher as seen in Table 2.1 [17, 18], which boosts its power handling capability and allows it to withstand much higher channel temperatures (Fig. 2.3).

	Si	GaN	GaAs	SiC
Band gap energy, E_g, eV	1.1	3.4	1.4	2.9
Electric breakdown field, E_{crit}, 10^6 V/cm	300	3300	400	2500
Thermal Conductivity, k, W/(K cm)	1.5	1.3	0.46	4.9
Electron Mobility, μ, $cm^2/(V\,s)$	1300	2000	5000	260
Saturation velocity, v_{sat}, 10^7 cm/s	1.0	2.5	1	2
Maximum operation temperature, T_{max} °C	200	700	300	500

Table 2.1: Semiconductor material properties comparison of Si, GaN, GaAs and SiC

In practical implementations of high power applications, GaN devices are often limited by their ability to dissipate heat through base substrate rather than their electronic properties [19]. Luckily, GaN lattice is suitable to grow on a number of substrate options with superb thermal properties such as Silicon Carbide (SiC) or diamond, both of which are very good thermal conductors. GaN-on-SiC devices have also the advantages of low lattice mismatch and relatively low thermal expansion mismatch, constituting ideal candidates for high power applications.

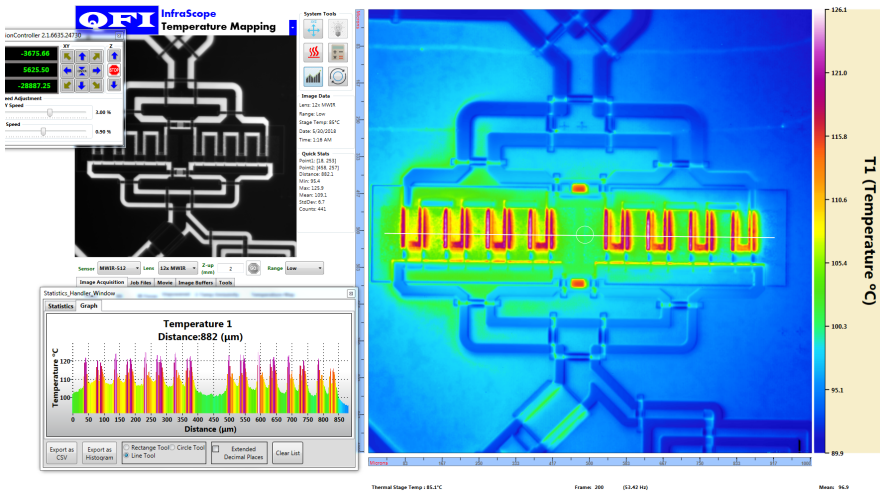


Figure 2.3: Thermal camera image from an operating GaN MMIC where temperature peaks can be seen in gate finger/channel locations

Advantages offered by GaN in various applications are reflected well in several figures of merits (FOM), listed in Table 2.2. Different figures of merits has been proposed to benchmark semiconductors by combining relevant material properties with application specific merits of the semiconductors [17]. Johnson's figure of merit (JFOM), which is a function of breakdown electric field and saturation electron velocity, indicates material's suitability for high frequency and high power applications. Baliga's FOM (BFOM) represents performance of transistors at low-frequency power switching applications. Another modified version of BFOM, Baliga's high-frequency FOM (BHFOM) gives an idea about material's high-frequency switching performance. Finally, the Keyes FOM (KFOM) considers thermal properties and current capabilities of material [18, 20].

	Si	GaN	GaAs	4H-SiC
$\mathrm{BFM_{Si}}$, $\epsilon_n \mu_c E_{\mathrm{crit}}^3$	1	910	28	290
$\mathrm{BHFOM_{Si}}$, $\mu_c E_{\mathrm{crit}}^2$	1	100	16	34
JFM_{Si}, $v_{\mathrm{sat}} E_{\mathrm{crit}}/2$	1	790	11	410
KFOM	1	1.8	0.45	5.1

Table 2.2: Baliga's, Baliga's High Frequency, Johnson's and Keyes' figure of merits for Si, GaN, GaAs and SiC

These figures of merits, together with high power densities and high operation frequencies, justify the distinguished position GaN has in modern RF and microwave applications.

2.2 NANOTAM GaN Microfabrication Process Overview

0.25 µm AlGaN/GaN on SiC process of NANOTAM starts with carefully controlled epitaxial wafer growth on SiC substrate using metal organic chemical vapor deposition (MOCVD) system. GaN/AlGaN epitaxial structure mainly consists of AlN Nucleation, High Resistive (HR) GaN, Channel GaN, AlGaN Barrier, AlN Spike and GaN Cap layers from bottom to top, as seen in Fig 2.4.

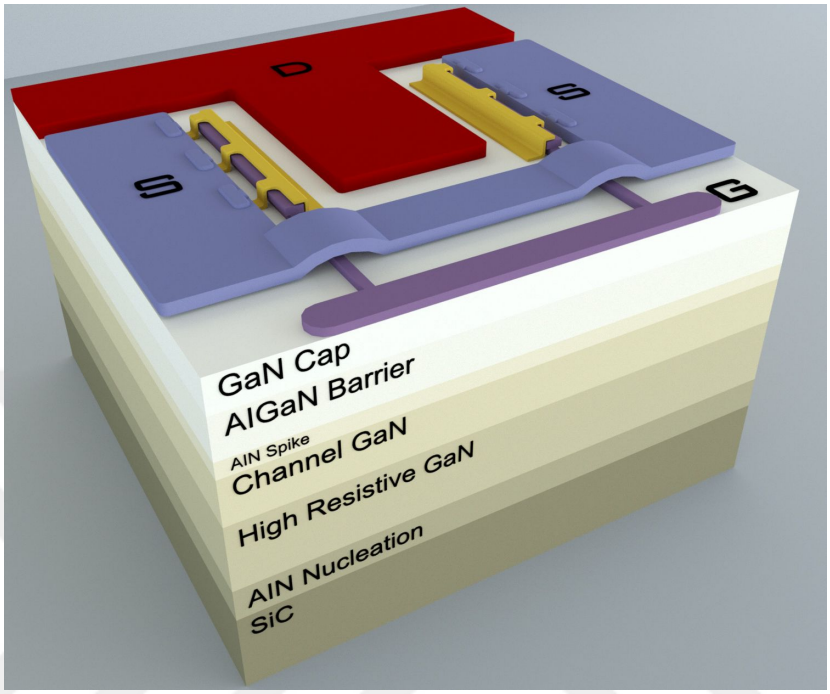


Figure 2.4: A perspective drawing of the epitaxial and fabrication layers in a GaN HEMT device

First AlN nucleation layer of 20 nm-35 nm thickness is laid on SiC to improve surface roughness and ensure a more smooth transition from SiC to GaN lattice. This layer also helps with the vertical breakdown limit of the structure as it acts as an insulating dielectric layer.

A high resistive GaN buffer layer of 1.5 µm thickness typically consisting of iron or carbon doped GaN acts as a buffer to restrict the movement of electrons to the channel above and prevent current leakages through the bulk material.

Channel GaN of approximately 100 nm thickness is the region where a high quality GaN crystal is grown to provide high mobility and saturation velocity, which together allow for higher saturation currents at the drain-to-source channel.

An ultra thin AlN Spike layer of 1 nm is grown on channel GaN to increase charge confinement and mobility in the channel [21].

AlGaN barrier of 20 nm-25 nm thickness is grown to utilize the lattice mismatch between the GaN and AlGaN crystals to induce spontaneous piezoelectric polarization which creates a very thin layer of free electrons called Two Dimensional Electron Gas (2DEG) which constitutes the conductive channel between the drain and source contacts of the device, controllable by the applied gate voltage.

Finally, epitaxial growth phase of the wafers conclude with a 3 nm-5 nm thick GaN-Cap layer for better ohmic contact formation and for physically isolating AlGaN layer from outside factors for better device reliability.

General properties of grown wafers and typical 2DEG performances are illustrated in Table 2.3.

Wafer and 2DEG Properties

Surface RMS Roughness	$< 1\,\mathrm{nm}$
Electron Mobility	$> 1800\,\mathrm{cm}^2/(\mathrm{V\,s})$
Sheet Charge Density	$> 1 \times 10^{13}\,\mathrm{cm}^{-2}$
Mesa Sheet Resistance	$< 400\,\Omega/\square$

Table 2.3: Properties of grown wafers and typical 2DEG performance

Grown wafers as seen in Fig. 2.5 provide the basis for the microfabrication steps that follow.

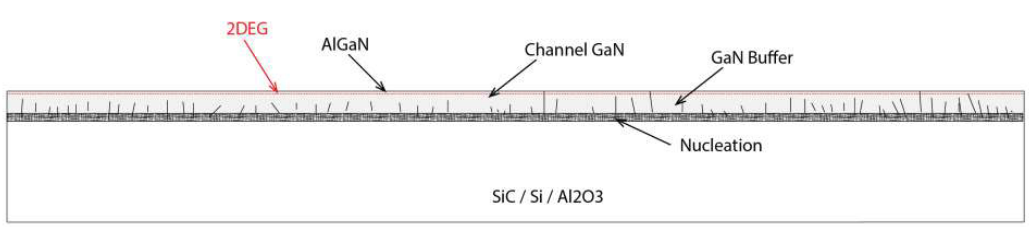


Figure 2.5: Cross-sectional drawing of the wafer after GaN epitaxial growth on SiC substrate at the beginning of fabrication

First step in the fabrication process is ohmic contact formation for active devices. This layer forms the low resistance junctions at the metal-semiconductor interfaces. A metal stack consisting of Ti/Al/Ni/Au is deposited (Fig. 2.6) by an electron beam evaporator system with the respective thicknesses of 20 nm,

100 nm, 40 nm and 50 nm. The metal stack is annealed in a nitrogen atmosphere at 850 °C for 30 s.

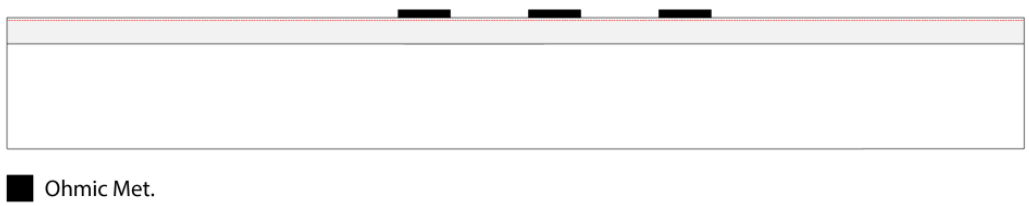


Figure 2.6: Cross-section of wafer after ohmic metallization step

As the next step, mesa isolation etching is performed (Fig. 2.7) in which the AlGaN/GaN epitaxial layers forming the 2DEG are removed from everywhere on the wafer surface except active areas. This way all separate active devices are electrically isolated. Mesa etching is done with an inductively coupled plasma reactive ion etching (ICP-RIE) system by using Cl_2/BCl_3 plasma-based dry etch. Mesa islands' heights are measured approximately as 100 nm by surface profilometer. After ohmic contact formation and mesa isolation, a series of transmission line measurements are taken using the four-probe technique. The measured ohmic contact resistances are around 0.25 Ω mm.

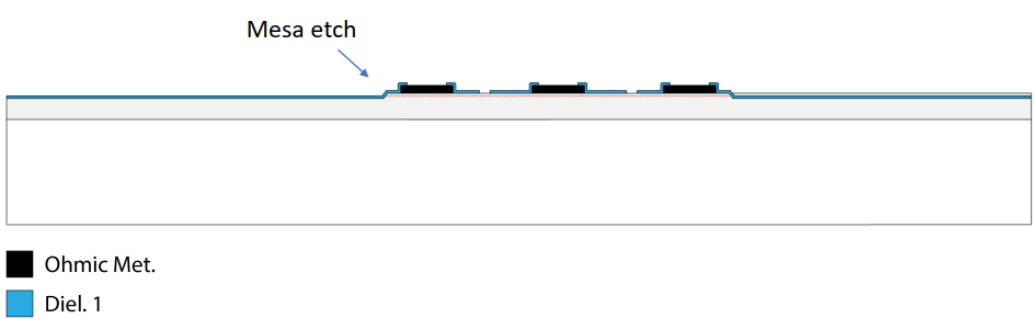


Figure 2.7: Cross-section of wafer after first passivation step

Surface of the sample is then passivated with a 75 nm thick Si_3N_4 layer grown by a plasma-enhanced chemical vapor deposition (PECVD) system. The gate feet regions of the devices are patterned (Fig. 2.7) by dry etching this passivation layer using the ICP-RIE system with an SF_6/Ar gas mixture.

Metal layer forming the gate feet and gate heads of devices is deposited

(Fig. 2.8) with a Ni/Au metal stack using the electron beam evaporator system with thicknesses of 50 nm and 300 nm, respectively.

Figure 2.8: Cross-section of wafer after gate-foot dielectric opening and gate metallization

A passivation layer consisting of a 210 nm thick Si_3N_4 is deposited (Fig. 2.9) as the next step, using the PECVD system. This Si_3N_4 layer also mechanically supports the source connected field plate structures stationed above the gates. Then, dielectric openings for source and drain contacts, as well as the openings where the field plates connections and back-side via hole metals would be deposited on, are formed (Fig. 2.9) by means of ICP-RIE dry etching system with SF_6/Ar gas mixture.

Figure 2.9: Cross-section of wafer after 2nd passivation step

Afterwards, source connected field plate gate structure is patterned (Fig. 2.10) with direct electron-beam lithography and these regions are deposited with a Ti/Au metal stack (with thicknesses of 10 nm and 440 nm, respectively) for field plate metallization formation, using the electron beam evaporator system (Fig. 2.10). Resulting gate structure can be seen in Fig. 2.4.

A 86 nm TaN thin film resistor layer, which is used for realizing on-chip resistances in circuits and devices, is deposited (Fig. 2.10) by RF magnetron sputter

system.

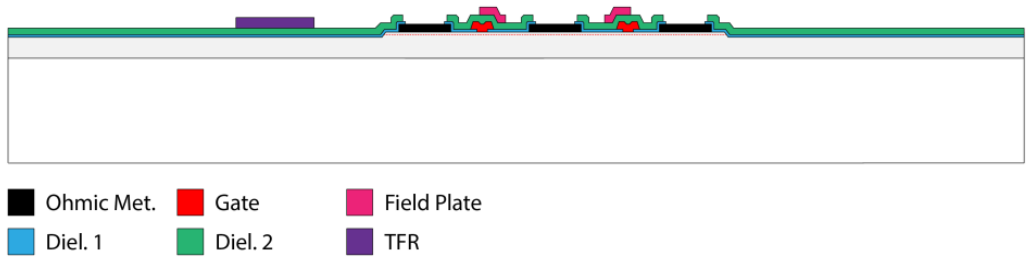


Figure 2.10: Cross-section of wafer after TFR coating and gate field plate metallization

Thereafter, Ti/Au metal stack is deposited (Fig. 2.11) using the electron beam evaporator system with thicknesses of 10 nm and 1000 nm, respectively. This metal layer constitutes the metal contacts in transistor drain and source regions as well as forming the 1st metal layer of metal-insulator-metal capacitors. This is the first metal layer accessible to circuit designer and is used in various connections of the active and passive elements of integrated circuits.

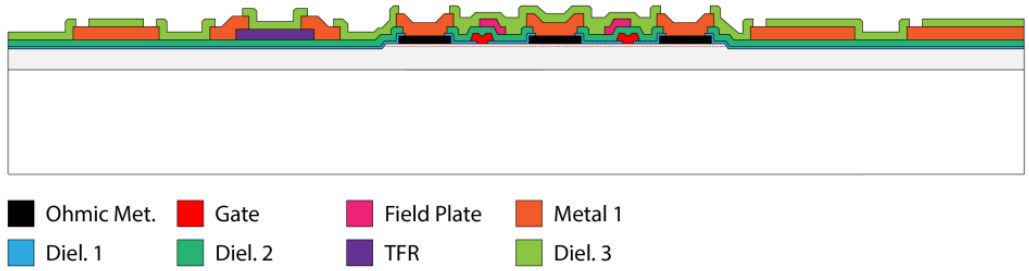


Figure 2.11: Cross-section of wafer after Metal 1 layer coating and final dielectric passivation

3rd Si_3N_4 layer with a 240 nm thickness is deposited (Fig. 2.11) with PECVD to form the dielectric material of the capacitors. The air-bridge post structures are utilized (Fig. 2.12) to form air bridges which reduce the parasitics and prevent short circuits at the metal-metal crossovers.

Thick metal layer of 4 µm Au is coated (Fig. 2.12) as the main interconnection layer using the electroplating system, concluding the front-side fabrication process.

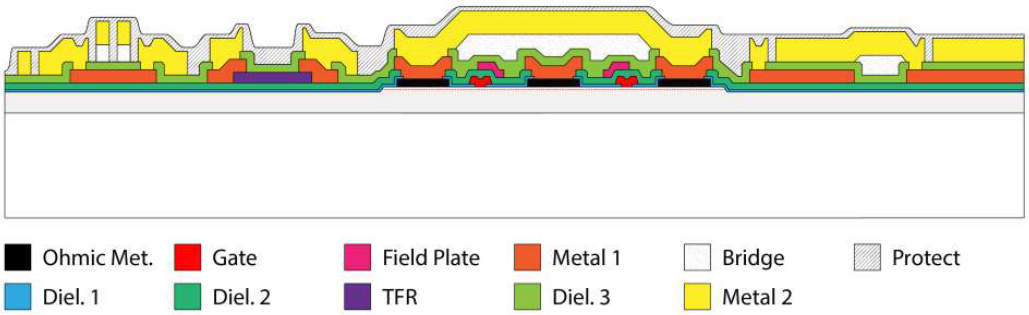


Figure 2.12: Cross-section of wafer after air-bridge formation and thick metal layer coating step

For the back-side fabrication process, the sample is grinded down to 100 µm thickness and back-via holes are opened through the SiC substrate by means of ICP-RIE dry etching. Finally, 4 µm thick Au layer is coated (Fig. 2.13) on the back side of the sample using the electroplating system. Walls of the via holes are also coated in the process. Ground connections of microstrip transistors and circuits are formed through these back-vias.

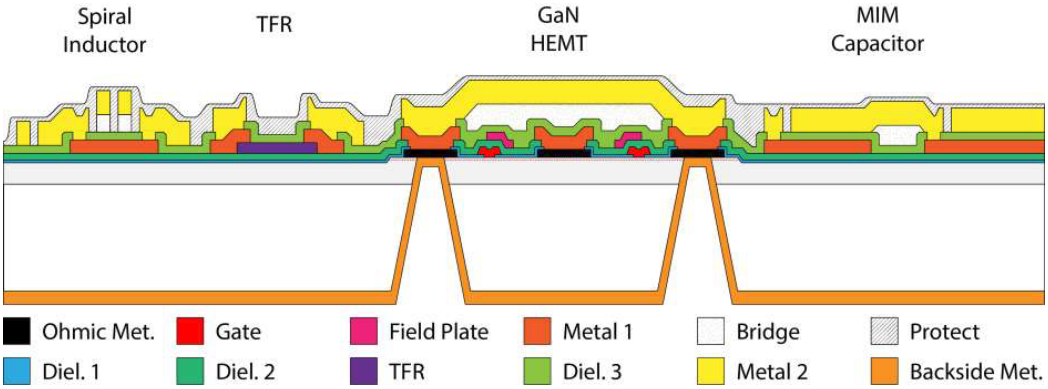


Figure 2.13: Cross-section of wafer after finalization of backside fabrication process

Chapter 3

Transistor Characterization

3.1 DC Characterization

A set of DC measurements are the first steps in HEMT characterization. On-wafer DC test setup is seen in Figure 3.1.

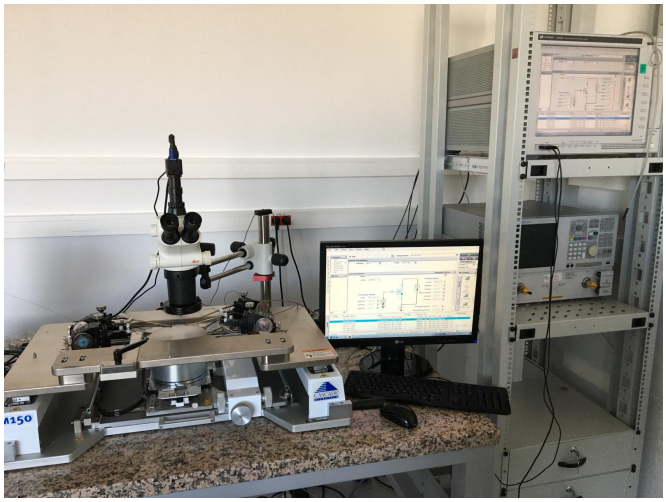


Figure 3.1: On-wafer DC-IV measurement setup

Formally, maximum saturated drain current, transconductance and IV curves can be used to derive a simple transistor model. In practice, DC measurements are also used to obtain an idea about device reliability and overall expected RF

and large-signal performance. A higher drain breakdown voltage high saturation current densities are associated with a higher maximum RF power, since they determine how large of a voltage and current swing can be maintained at the output of device [22]. Also gate and drain leakages are indicators of possible future device degradation under DC and RF stress.

Figure 3.2 is a typical IV curve for a 8×125 µm GaN HEMT. The transistor has an I_{dss} of 1 A equalling 1 A/mm which is considered standard for GaN HEMTs.

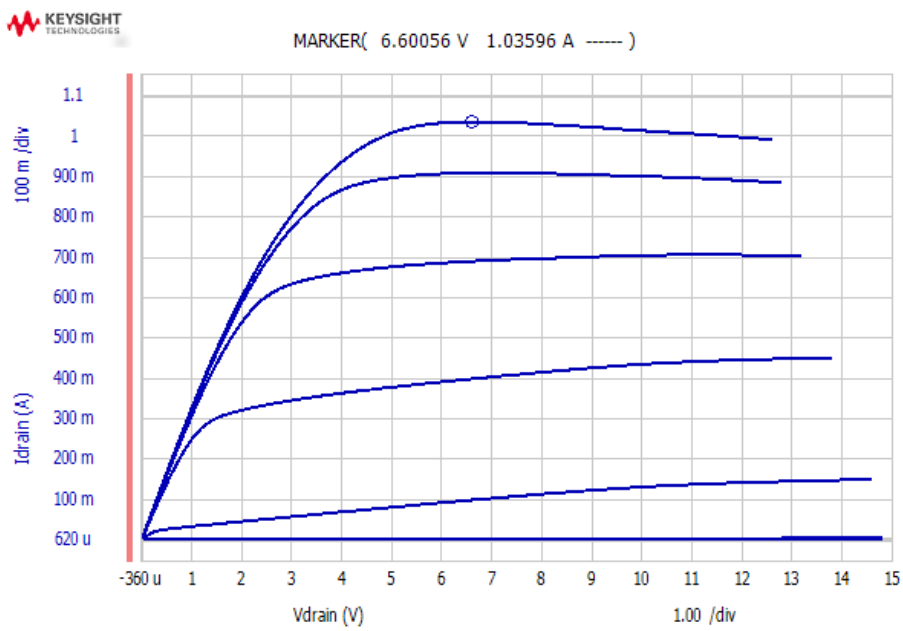


Figure 3.2: IV curves of a 8×125 µm HEMT

Figure 3.3 is the transconductance curve of a 8×125 µm GaN HEMT. Transconductance which is defined as $g_m = \frac{\mathrm{d}I_d}{\mathrm{d}V_{gs}}$, is a measure of transistor output current source's sensitivity to small gate voltage perturbations. Thus, it gives an idea about small-signal gain transistor could produce without accounting for the parasitic effects that will kick-in at higher frequencies.

Figure 3.4 is the breakdown characteristics of the device. The drain leakage was measured as 820 µA while the HEMT was in pinched-off state ($V_{GS} = -6V$) and the drain-to-source voltage was swept to 90 V. As seen from the measurement, drain leakage is smaller than 1 mA/mm which is considered as the accepted level for GaN HEMT devices.

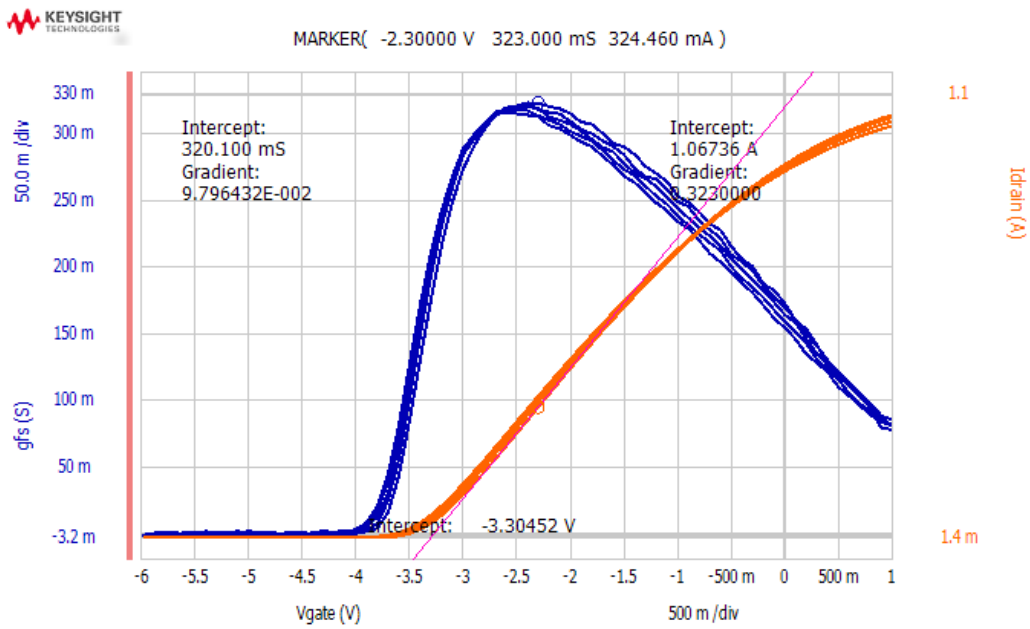


Figure 3.3: g_m and I_{DS} vs V_{gs} curves of 8×125 µm HEMTs

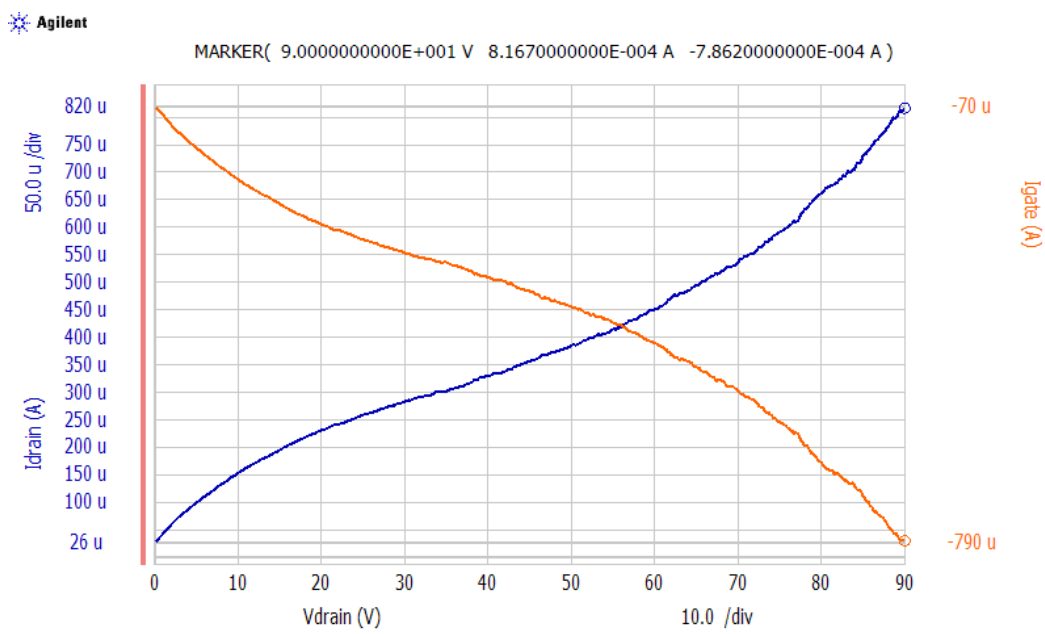


Figure 3.4: Gate & drain leakage or breakdown characteristics of a 8×125 µm HEMT

3.2 RF Small-Signal Measurements

Characterizing the device behaviour is first done via small signal analysis. At higher frequencies, parasitics that are normally dormant at lower frequencies, become quite prominent and affect the input and output impedance of these devices. These reactance/susceptances need to be resonated so that maximum gain can be obtained from the devices. Therefore, frequency responses of the transistors are measured using vector network analyzers. Small-signal linear behaviour of devices are captured with these S-parameter measurements.

Figure 3.5 is the small signal setup used for continuous wave S-parameter measurements.

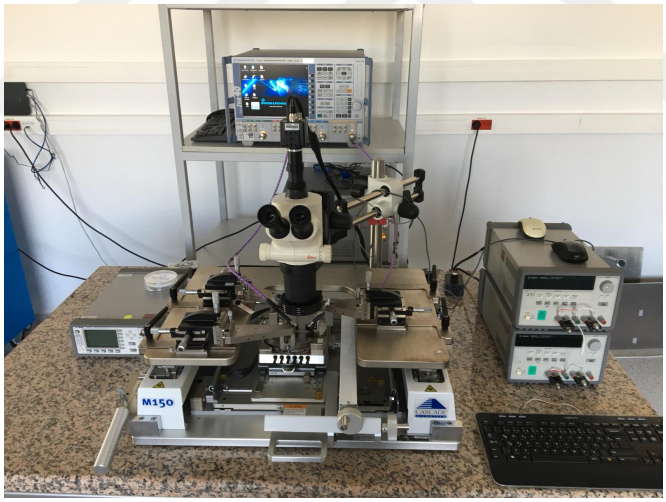


Figure 3.5: CW on-wafer small-signal measurement setup

At various operation conditions such as bias point, temperature and operation mode -e.g. pulsed or CW-, device behaviour can change, therefore at different conditions, these linear behaviours are separately characterized using small-signal measurements. The superposition of all these behaviours are expected to conform to the design specifications.

Probe station with thermally controlled chuck in the setup in Figure 3.6 and DC pulsers are used for pulsed S-parameters measurements, as well as measurements at various base temperatures.

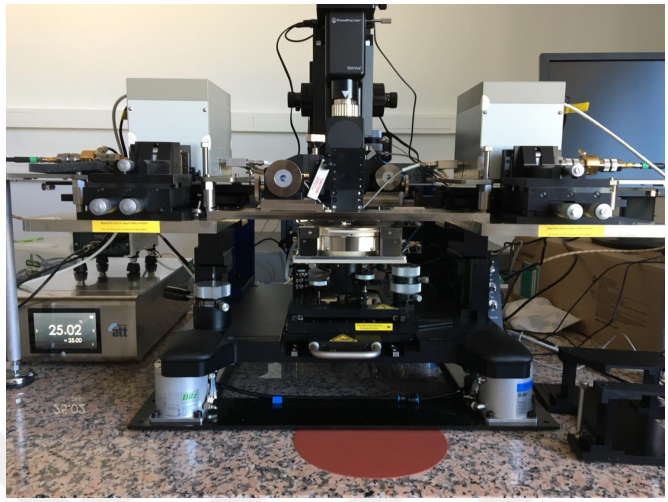
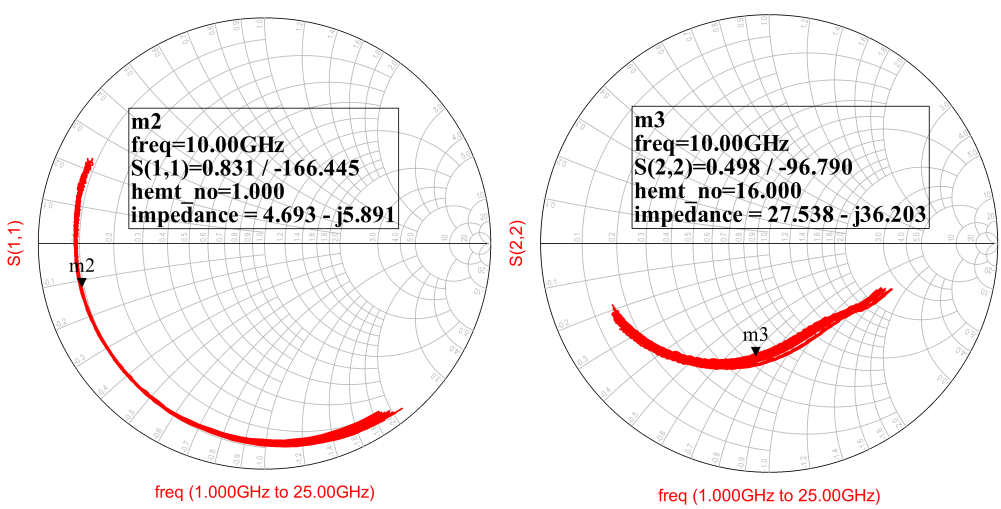


Figure 3.6: RF measurement setup with DC pulsers and thermally controlled chuck for measurements in pulsed mode and at different temperatures

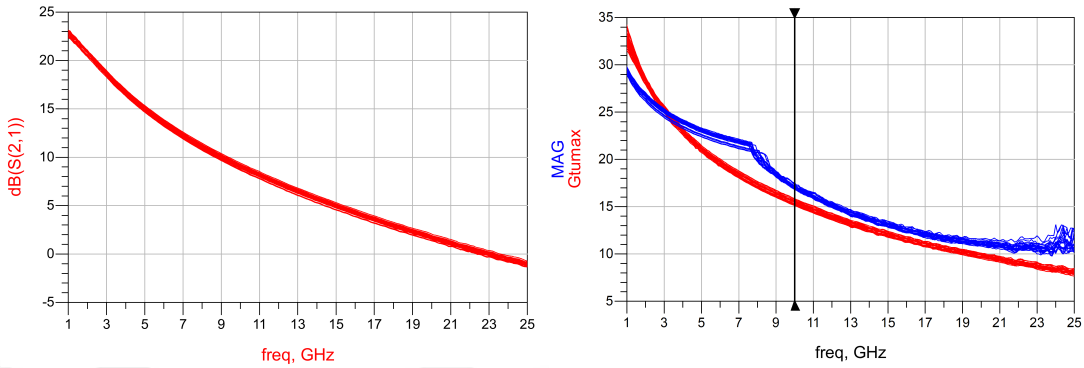
Bulk results of S-parameter measurements for 8x125 µm HEMTs are shown in Figure 3.7 and Figure 3.6.



(a) (b)

Figure 3.7: Input and output reflection coefficients of 8x125 µm HEMTs

Since on-wafer calibration of the vector-network-analyzer (VNA) brings measurement reference planes to the probe tips, measurement results of devices also include RF probe pads and extra transmission lines between the pads and the device reference planes as shown in Figure 3.9. In other words, parasitic pad capacitances and open end effects together with the transmission line between



(a) Multiple $|S_{21}|$ graphs of HEMTs (b) MAG and G_{TUmax} graphs of HEMTs

Figure 3.8: Forward transmission characteristics of 8x125 µm HEMTs under CW operation at room temperature

probe's tip to the designated transistor should be taken into account [23].

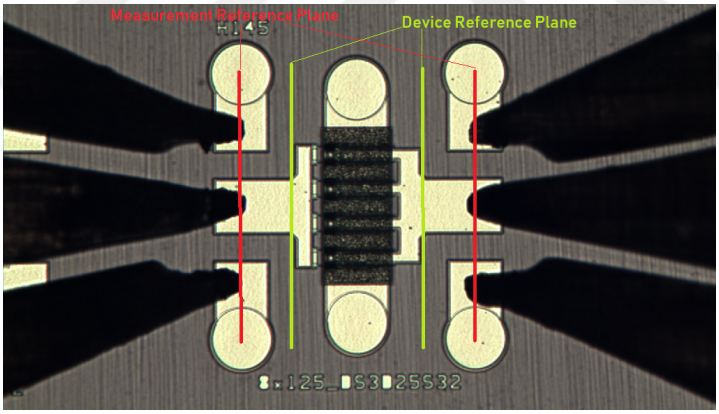


Figure 3.9: Measurement and device reference planes

Therefore, the tranmission lines and RF measurement pads between reference planes are EM simulated and de-embedded from the overall measurement [24].

3.3 Large-Signal (Load-Pull) Measurements

Optimum load impedances for maximum power and maximum gain are the same for low input powers. But as the devices are driven to large-signal operation, due to the non-linear characteristics of the transistor, optimal output impedances for

gain and power become gradually separated [25] (Examined in more detail in Section 4.5.2 and 4.5.3). Figure 3.10 shows the load-pull contours of G_t, PAE and P_{out} at 3 dB compression at 10 GHz for an $8 \times 125\,\mu$m HEMT. It should be noted that the circles for all these parameters converge on different impedances.

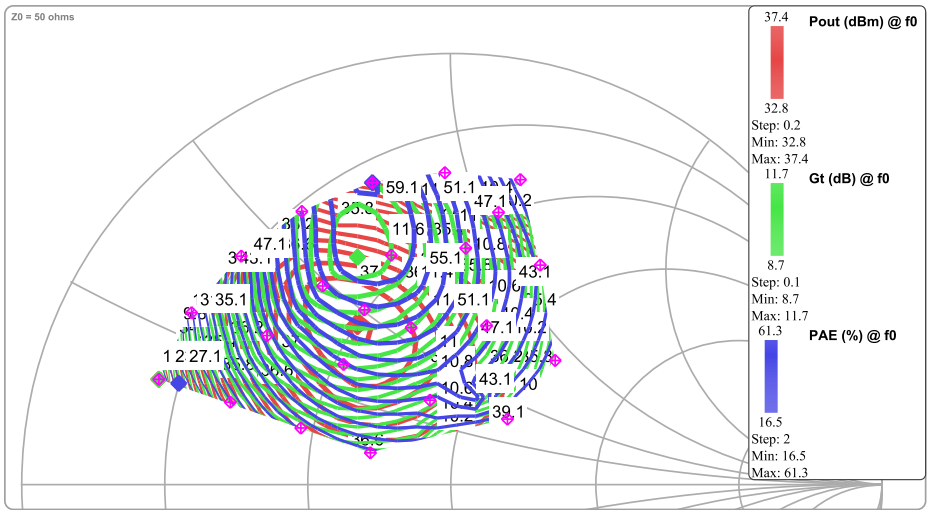


Figure 3.10: G_t, PAE and P_{out} contours of an $8 \times 125\,\mu$m HEMT at 10 GHz under 3 dB gain compression

Since, main function of PAs is to deliver highest possible power, aside from other performance merits, these power contours need to be modelled to receive more power out of the device at the given conditions. To achieve this, either a large signal model ought to be available, or these impedances need to be emprically determined. In our design methodology, load-pull measurements are used to determine these impedances. Figure 3.11 is the Vector Network Analyzer (VNA) based Maury passive load-pull system that is used for large-signal transistor characterization. Tuners operate from 0.8 GHz to 18 GHz.

This is a vector based load-pull system, block diagram of which can be seen in Fig. 3.12. Incident and reflected power waves at the input and output of the DUT are sampled via the low-loss couplers connected immediately before the tuners. That way available and delivered input and output powers can be directly calculated via a and b waves; as well as the source, input, output and load impedances at the DUT reference planes.

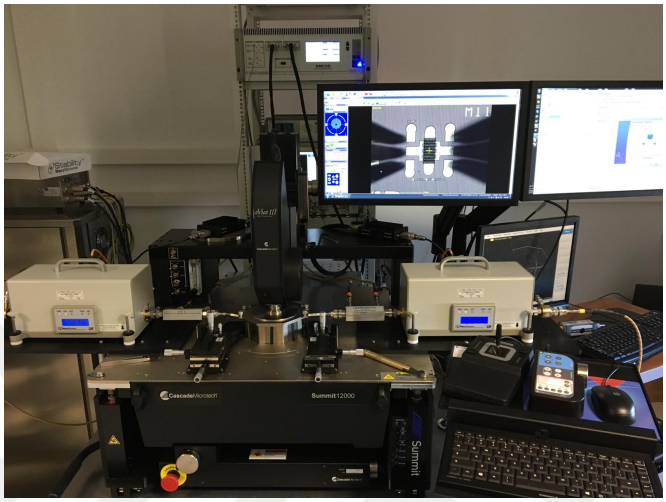


Figure 3.11: Maury VNA based passive load-pull bench

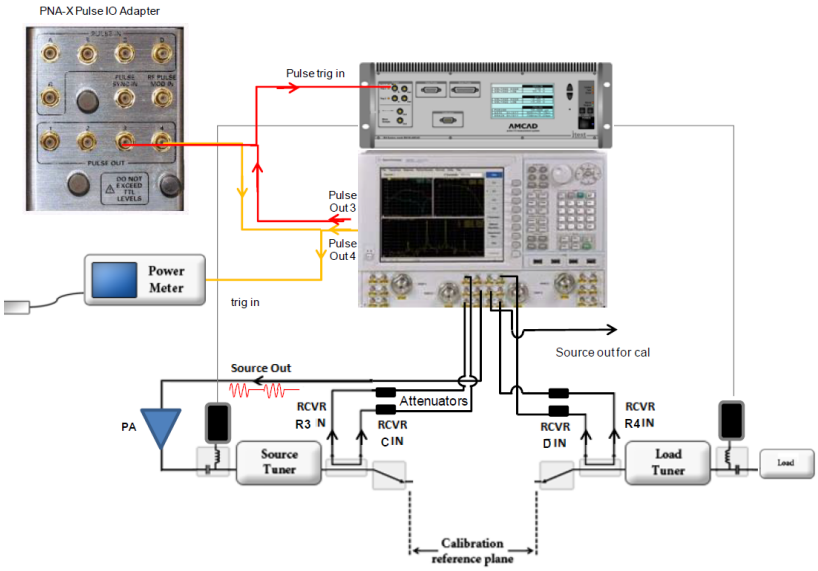


Figure 3.12: Block diagram of the vector network analyzer based load-pull system

Figure 3.13 is the output contours of a typical $8 \times 125\,\mu m$ HEMT measured at 10 GHz under 3 dB gain compression.

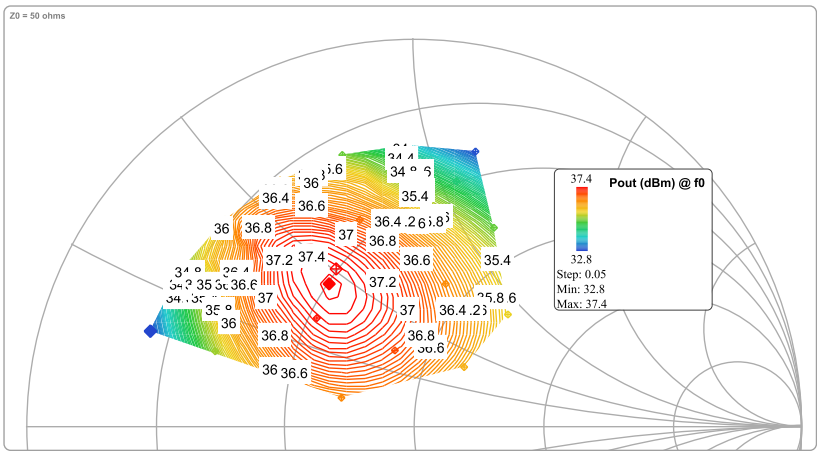


Figure 3.13: P_{out} circles of an $8 \times 125\,\mu m$ HEMT at 10 GHz under 3 dB gain compression

Overall HEMT performance parameters can be seen in the table below.

Parameter	**Symbol**	**Typical value**
Max. Drain Current	I_{dss}	1000 mA/mm
Peak Transconductance	g_m	300 mS/mm
Breakdown Voltage	V_{br}	>90 V
Gate Threshold Voltage	V_{th}	−3.5 V
On Resistance	R_{on}	2.2 Ω mm
Max. Available Gain @10 GHz	G_{max}	17 dB
Quiescent Drain Voltage	V_{DD}	28 V
Power Density	P_{3dB}	5.5 W/mm

Table 3.1: Overall DC, RF and load-pull results of 8x125 µm HEMTs

Chapter 4

MMIC Design

In this chapter, design steps of the 2-stage MMIC PA are described in detail. Our aim for this design was to achieve more than 13.5 W output power under pulsed mode operation with less than 6 dB gain compression. Also a minimum large-signal gain of 19 dB was targeted. Design is based on the S-parameter and load-pull measurement data of transistors. Small-signal simulations, layout design and EM simulations are carried out in Keysight's Advanced Design System (ADS) software. Bulk analysis of vector based load-pull measurements of transistors and power sweep simulations for MMICs are performed on MATLAB.

In order to achieve design goals with minimum amount of transistors (hence with greater efficiency and smaller circuit area), optimal transistor size, layout and gate structure have been investigated first. After the ideal transistor and gate type has been determined, preliminary small-signal and power analyses have been performed to decide the possible amplifier topologies for specified design goals. As the first step of the amplifier design, stability circuits are added to selected transistors for even-mode stability of both stages. Next, gate and drain bias lines with sufficient in-band RF grounding and isolation are realized. Output, inter-stage and input matching networks have been designed in sequence. Parametric optimization for the merged layouts of matching networks have been performed to account for any unwanted effects coming from discontinuities and EM couplings.

Finally, even and odd-mode stability analyses for the circuit have been done and additional stability elements have been added to reinforce stability under various bias, temperature and pulse conditions.

4.1 Transistor Optimization

For investigating optimal transistor size, layout and gate structure for X-band performance, a HEMT development photomask is prepared (Fig. 4.1); where transistors of different gate peripheries with varying gate widths and number of fingers are placed.

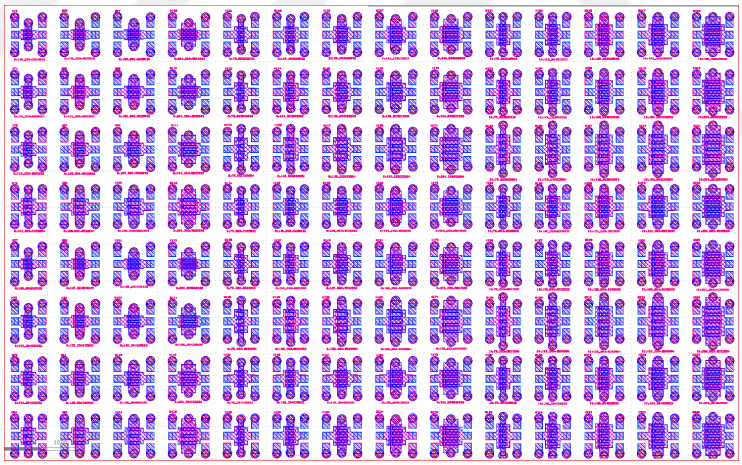


Figure 4.1: Photomask view of the microstrip transistor reticle

In the same photomask, also a parametric study of various gate geometries has been conducted, since transistor gate structure is crucial in determining overall transistor performance.

Both small-signal and large-signal measurements are taken into account when comparing performances of various types of transistors. However due to the time consuming nature and more demanding infrastructure requirements of load-pull measurements, automated small-signal measurements are used to initially sift through the large number of transistor variants and minimize the number of candidates to a manageable size.

For the purpose of ranking small-signal performances of transistors among themselves, their maximum available gains are compared; which equals to the gain when simultaneous perfect conjugate match is achieved at the input and output of transistors. Instead of the widely used criterion of *Maximum Available Gain* ($MAG, GMax, MSG$), another figure of merit called *Maximum Unilateral Transducer Gain* (G_{TUmax}) is considered.

Definition of MAG is dependent on the value of stability factor K and therefore implemented as a piece-wise function [26]. For $K > 1$:

$$MAG = \left|\frac{S_{21}}{S_{12}}\right| (K - \sqrt{K^2 - 1}) \tag{4.1}$$

And for $K \leq 1$, MAG is calculated as:

$$MAG = \left|\frac{S_{21}}{S_{12}}\right| \tag{4.2}$$

At the unstable (or conditionally stable) regions of the frequency band and the transition zones around the discontinuities, value of MAG may give misleading information about device performance. Whereas G_{TUmax} is independent of device stability and is a continuous function which helps to determine trends in the device performances more accurately.

Setting the $|S_{12}| = 0$ in the transducer gain equation [27], we obtain the *unilateral transducer gain*:

$$G_{TU} = \frac{1 - |\Gamma_S|^2}{|1 - S_{11}\Gamma_S|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \tag{4.3}$$

When the input and output of the device is conjugate matched simultaneously for maximum gain, $\Gamma_S = S_{11}^*$ and $\Gamma_L = S_{22}^*$, *maximum unilateral transducer gain* becomes:

$$G_{TUmax} = \frac{1}{1-|S_{11}|^2}|S_{21}|^2\frac{1}{1-|S_{22}|^2} \tag{4.4}$$

Although this gain definition is based on the unilaterality assumption of the two-port network and gives only an approximate estimation, it is used here for comparing the relative performances of different devices.

4.1.1 Layout Design/Comparison/Selection

Total gate periphery of the device directly controls the amount of current passing from the drain-source channel, hence the maximum power output of the device. However as the electrical length of the device increases, gain drops significantly. This may be attributed to the amplitude and phase imbalance among gate fingers, as well as the growing effects of parasitics in higher frequencies. Fig. 4.2 shows the average G_{TUmax} values calculated from many HEMT S-parameter measurements of various gate peripheries.

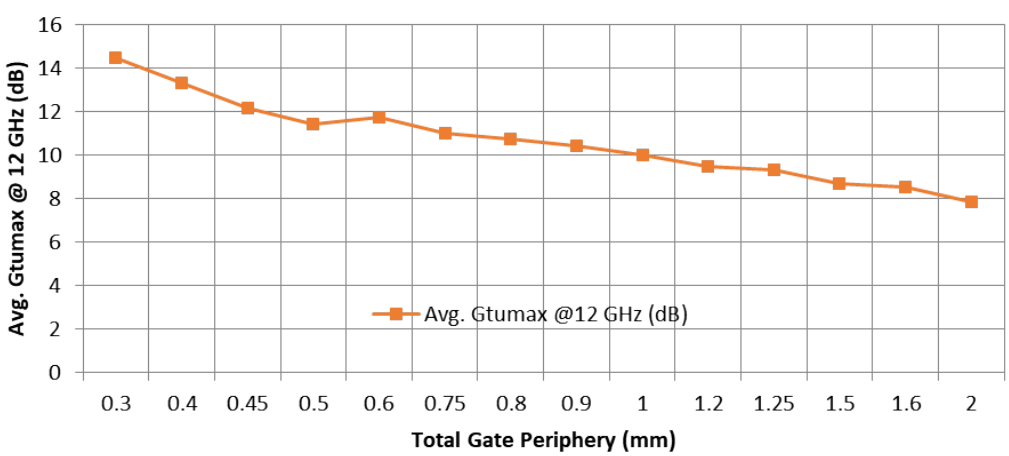
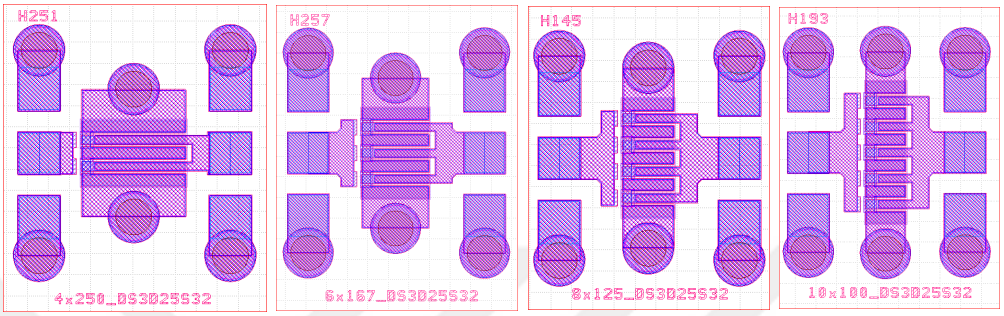


Figure 4.2: Relation between total gate periphery and small-signal performance

For a given total gate periphery, there is an optimal balance between the length of the transistor, which is determined by the number of gate fingers and the length of individual drain and source contacts; and the gate width of the transistor. For

devices with 1 mm total gate periphery, 4 different layouts seen in the Fig. 4.3 are compared.



(a) 4x250 μm (b) 6x167 μm (c) 8x125 μm (d) 10x100 μm

Figure 4.3: Photomask views of 4 HEMTs with 1 mm gate peripheries and different finger configurations

It is found that among the 1 mm HEMTs, 8x125 μm finger configuration is at the sweet spot in terms of small signal performance (Table. 4.1).

		Gtumax @ 12 GHz (dB)	**P3dB @ 10 GHz (Watts)**	**Large-Signal Gain @ P3dB @ 10 GHz (dB)**
Finger Config.	**4x250**	9.1	3.6	8.8
	6x167	10.1	3.6	10.0
	8x125	10.7	3.4	10.4
	10x100	10.5	3.2	10.1

Table 4.1: G_{TUmax}, power and large-signal gain comparison of 1 mm HEMTs with different finger configurations

Transistor layout parameters mentioned in this section are marked on the SEM image of a 8x125 µm HEMT in Fig. 4.4.

Channel length (or drain-to-source (DS) distance) of the transistor also plays an important role both in small-signal and large-signal performance of the device. While a smaller DS distance contribute to gain and power performance of the device, below certain values may be problematic from fabrication and reliability perspective and may result in premature breakdown of transistor under high RF and thermal stress. When all other parameters kept constant, drain-to-source

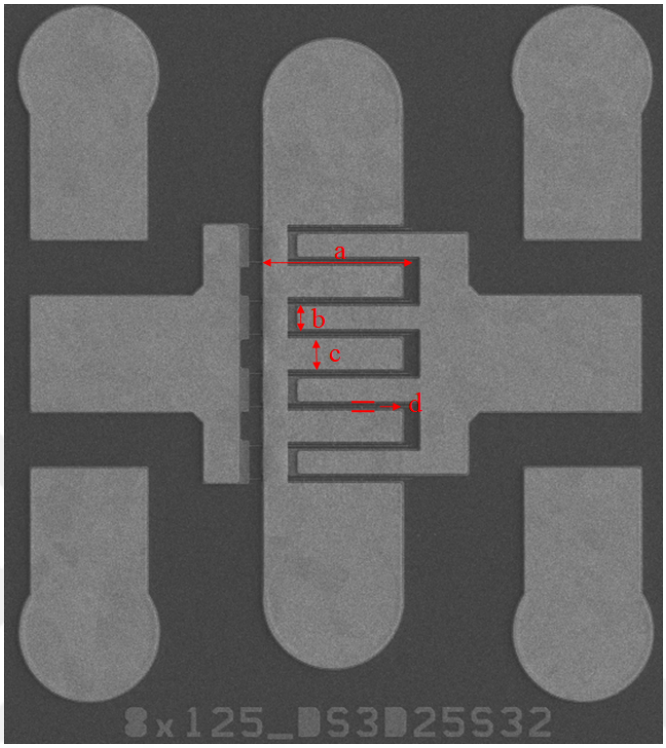


Figure 4.4: Transistor layout parameters as marked on the SEM image are: a) gate width, b) drain contact length, c) source contact length and d) drain-to-source distance or channel length

distance (DS) is swept from 3 μm to 5 μm. Small-signal and large-signal performances of DS3 type devices have found to be better (Table 4.2) as expected, and no reliability problems have been observed with these devices.

There is also a trade-off regarding the drain and source contact lengths. When they are shorter, overall device becomes more compact, thus small-signal gain increases. As we see in the Table 4.2, variants with 18 μm drain and source contact lengths are the ones with highest G_{TUmax}.

However compact device length also means that gate fingers are stacked more tightly, which leads to higher channel temperatures under large-signal operation. Transistors with the best small-signal performance therefore, may not be the ideal option for high power and/or high base temperature regime.

Gtumax @12 GHz (dB)		Channel Length			
		3 um	**3.5 um**	**4 um**	**5 um**
Drain & Source Contact Variants	**D18_S18**	10.8	10.7	10.6	-
	D25_S32	10.7	10.4	10.4	10.1
	D32_S32	10.6	10.1	10.1	9.9
	D32_S54	10.1	-	9.8	9.6
	D40_S40	10.0	9.8	9.7	-

Table 4.2: G_{TUmax} comparison of transistors @12 GHz with various drain & source contact lengths versus channel lengths

To compare large-signal performances of different layouts, a set of pulsed load-pull measurements at two different chuck temperatures (25 °C and 110 °C) have been performed on these devices with 28V drain voltage. When the drain and source contact lengths are swept while keeping other variables constant, results in the Table 4.3 are obtained.

Load-pull results @10 GHz		25 C		110 C	
		Power Gain (dB)	**P3dB (Watts)**	**Power Gain (dB)**	**P3dB (Watts)**
Drain & Source Contact Variants	**D18_S18**	12.3	5.0	11.0	4.0
	D25_S32	11.6	5.5	10.1	4.8
	D32_S32	11.4	5.6	10.3	4.8
	D32_S54	10.3	6.0	10.0	4.9
	D40_S40	11.2	5.6	10.1	4.7

Table 4.3: Load-pull results (at 10 GHz) of different contact length variants are compared at 25 °C and 110 °C base temperatures

It becomes apparent that smallest variant with 18 μm drain and source contact lengths (*D18_S18*) performs poorly under large signal in both temperature conditions. Gain and power density relation is as expected in 25 °C measurements; as the size shrinks, gain increases and power decreases and vice versa. However measurements at 110 °C show that performance of all transistors except the smallest *D18_S18* variant converges, indicating that elevated base plate temperature is the limiting factor for the channel temperature in these variants rather than the power dissipation in the channels. Based on these observations, *DS3_D25_S32* variant with 3 μm drain-to-source distance, 25 μm drain and 32 μm source contact lengths has been chosen as the transistor layout.

4.1.2 Parametric Gate Study

Transistor gate structure is one of the most critical elements defining overall performance by determining the small-signal gain and power capability of device. It has been shown that by controlling the gate geometry, it is possible to modulate the electric field in the channel and modify numerous device characteristics [28–33]. Figure. 4.5 shows multi level gate structure consisting of gate foot, gate head (a.k.a. gate field plate), source connected field plate (SCFP) and corresponding surface electric field intensity graphs across the source-drain channel.

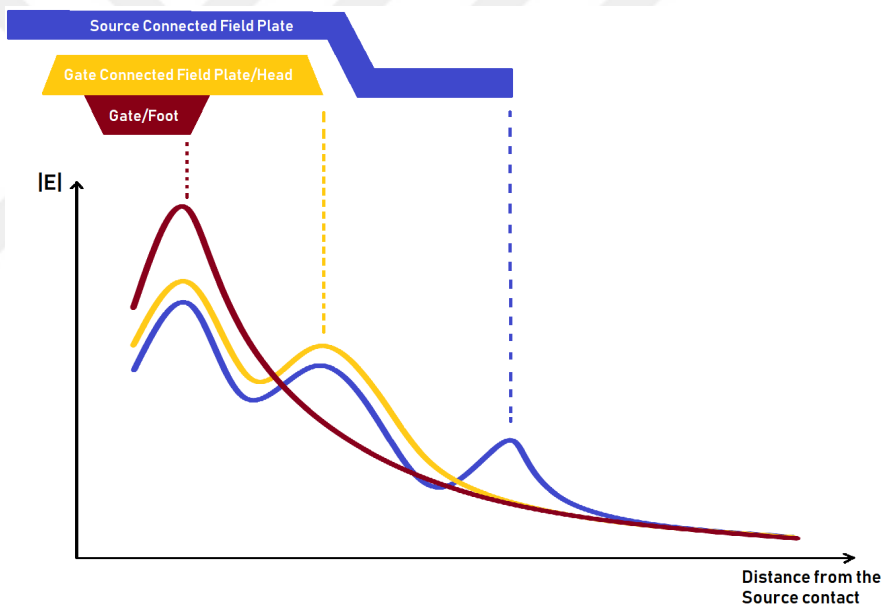


Figure 4.5: Geometry of gate structures and corresponding surface electric field intensities

In the simple gate configuration (with only gate foot), most of the voltage drop between the gain and source occurs at the single large electric field peak concentrated at the drain side of the gate. Addition of a gate head (a.k.a. T-gate or Γ-gate) reduces the maximum field strength by adding another peak at the drain end of the gate structure. Finally, utilizing an overhanging field plate electrically connected to the source of the device (which sits at 0 Volts potential) creates a third peak and more evenly distributes the surface electric field.

Gate design affects many physical properties such as gate-to-drain and gate-to-source capacitances, breakdown voltages. Gate fabrication process has also a role in surface trap related effects such as current collapse, which may degrade large-signal performance of the device. Therefore, gate process and gate geometry require careful optimization.

In order to find the optimum gate structure for X-band applications, a parametric gate study has been performed in the HEMT development photomask. Three parameters of the gate geometry (length of the gate foot, gate head and field plate overhang) are swept across a range of values.

VNA based load-pull measurement results are processed with the help of a MATLAB code that scans all possible source and load impedance pairs to find maximum gain and output power at a given compression value. Load-pull measurements are done with a single fixed source impedance and a number of load impedance points that cover areas of interest in the Smith Chart. Source impedance space is then spanned for every load impedance point using a virtual source-pull method [34] to calculate device performances corresponding to every load-source impedance pair.

Table 4.4 presents the results of gate types without SCFP structures. Keeping the distance between source contact and the gate metal constant, lengths of the gate heads are swept from 400 nm to 800 nm and the gate feet are fabricated at 200 nm, 250 nm and 300 nm lengths. Load-pull measurement results for transistor gains and output powers at 10 GHz under 3 dB compression are compared in the Table 4.4 below.

To improve transistor large-signal performances, source connected field plate structures with various geometries are tested. A similar parametric study has been performed with gate types with SCFP structures, where both gate feet and gate head lengths are swept parametrically. Table 4.5 presents the results of gate types with SCFP structures. Keeping the distance between source contact and the gate metal constant, lengths of the gate heads are swept from 400 nm to 800 nm and the gate feet are fabricated at 200 nm, 250 nm and 300 nm lengths.

		Gate Foot Length (nm)					
		200		**250**		**300**	
		Power Gain (dB)	P3dB (dBm)	Power Gain (dB)	P3dB (dBm)	Power Gain (dB)	P3dB (dBm)
Gate Head Length (nm)	**400**	10.2	36.6	-	-	-	-
	500	11.4	37.0	11.7	36.8	10.9	36.4
	600	11.3	37.0	11.6	36.9	11.6	36.6
	700	10.9	36.8	11.3	36.7	11.1	36.9
	800	-	-	10.8	36.4	-	-

Table 4.4: Output power and large-signal gain comparison of transistors at 3 dB compression at 10 GHz, for gate geometries without SCFP structures

SCFP overhang distances are also kept constant at 375 nm in this comparison. Load-pull measurement results for transistor gains and output powers at 10 GHz under 3 dB compression are compared in the Table 4.5 below.

		Gate Foot Length (nm)					
		200		**250**		**300**	
		Power Gain (dB)	P3dB (dBm)	Power Gain (dB)	P3dB (dBm)	Power Gain (dB)	P3dB (dBm)
Gate Head Length (nm)	**400**	11.6	36.9	-	-	-	-
	500	12.0	37.4	12.6	36.8	12.3	36.6
	600	11.7	37.3	12.7	36.9	12.6	36.8
	700	12.1	37.0	12.4	36.9	12.5	36.9
	800	-	-	11.9	36.7	-	-

Table 4.5: Large-signal performance comparison of gate geometries with SCFP structures at 10 GHz

Load-pull measurement results (@ 10 GHz) of the gate type with the best power density (200 nm *gate foot and* 500 nm *gate head variant with* 375 nm *SCFP overhang distance*) is presented in Fig. 4.6.

37.4 dBm P_{3dB} is obtained at maximum power match and a G_T of 12.3 dB was achieved with maximum gain match at 10 GHz with this gate geometry (Fig. 4.6). Also a simultaneous 12.0 dB transducer gain, 37.4 dBm output power and %52.8 drain efficiency is obtained at (3.0+5.9i) Ω source and (26.2+16.8i) Ω load impedances.

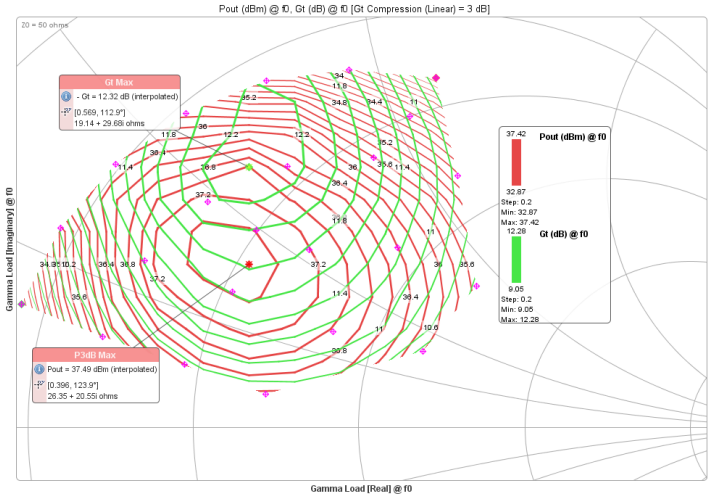


Figure 4.6: G_T (green) and P_{3dB} (red) load-pull contours (@ 10 GHz) of the HEMT type with the best power density at 3 dB compression

Load-pull measurements of various gate types reveal that other similar gate geometries yield comparable results with trade-offs between G_T and P_{3dB}. In Fig. 4.7, load-pull contours of the HEMT type (250 nm *gate foot and* 600 nm *gate head variant with* 375 nm *SCFP overhang distance*) with slightly lower output power and better transducer gain are given.

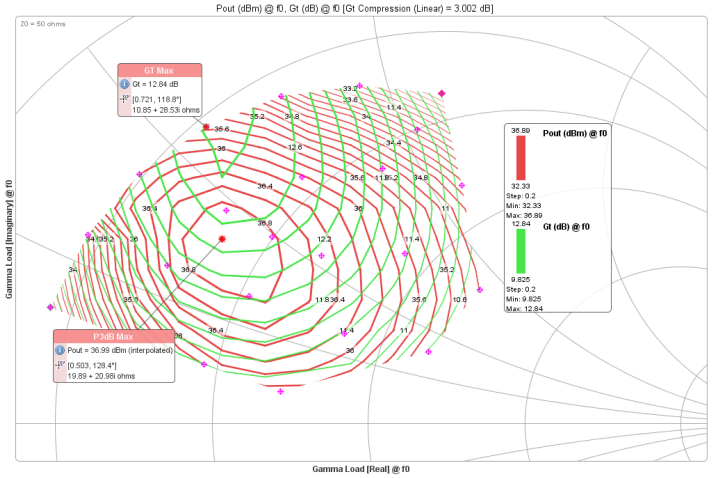


Figure 4.7: G_T (green) and P_{3dB} (red) load-pull contours (@ 10 GHz) of the HEMT type with better large-signal gain at 3 dB compression

36.9 dBm P_{3dB} is obtained at maximum power match and a G_T of 12.84 dB was observed at 10 GHz. A simultaneous 36.9 dBm output power, 12.7 dB

transducer gain and %56.4 drain efficiency is obtained at (2.7+4.4i) Ω source and (18.4+24.0i) Ω load impedances.

4.2 Topology Selection

Targeted performance goals of for this PA design is given in table 4.6.

Specifications	Minimum	Typical	Maximum
Operation Frequency Band	8.5 GHz	-	11 GHz
Small-Signal Gain	23 dB	-	-
Pulsed Mode Output Power	-	41.5 dBm	-
PAE	30	-	-
Gain Compression	-	-	6 dB

Table 4.6: Design specifications of the power amplifier

Single transistor performances of a 8x125 µm HEMT that this design based on are given in the table below.

	Frequency		
	8.5 GHz	**10 GHz**	**11 GHz**
P3dB (dBm)	34.3	34.9	34.7
Large-Signal Gain (dB)	14.7	13.1	12.1

Table 4.7: Power output and gain of the 8x125 µm HEMT (at 3 dB compression) used in design

Note that these results are different from the ones presented in transistor optimization section. This is due to the fact that at the beginning of design, transistor optimization was still in progress, thus the final optimized transistor results were unavailable in the design phase. Hereafter, all presented transistor results will refer to the ones that the design is based on, unless stated otherwise.

To achieve the small-signal goal of 23 dB, a 2 stage design is necessary. Output power target of 41.5 dBm also dictates at least 4 transistors in parallel are

required at the output stage. For the driver stage, it is possible to employ a single transistor, resulting in a power drive ratio of 1:4. However, driver stage in this configuration may be driven to too much compression, affecting the maximum compression budget for the output stage. On the other hand, using 2 transistors at the driver stage helps with the overall gain compression of the amplifier at the cost of efficiency, as 1:2 power drive ratio will not compress the driver stage significantly. Therefore, these two possible topologies are investigated in more detail with MMIC power simulations.

MMIC power simulations are performed in MATLAB environment, using our own tool developed to process raw data of Vector Network Analyzer (VNA) based transistor load-pull measurements. This MMIC simulation tool applies curve fitting on the load plane to interpolate between the measured load-pull data points. Also a virtual source pull technique dubbed "magic source pull" is implemented to characterize device behaviour for all source impedance space [34]. Tool takes the amplifier topology, matching network losses and impedances presented to transistors as its inputs, and generates power sweep simulations for the overall MMIC and individual amplifier stages. Power simulation of the MMIC with 2:4 topology at 10 GHz is presented in Fig. 4.8 and power sweep simulations of 1st and 2nd stages can be seen in Fig. 4.9a and Fig. 4.9b.

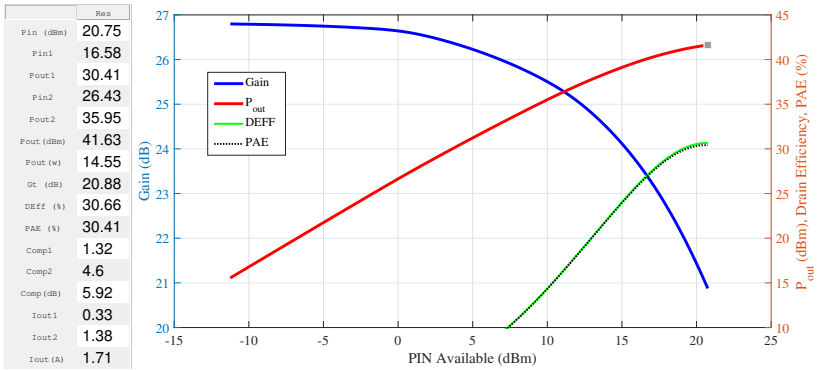
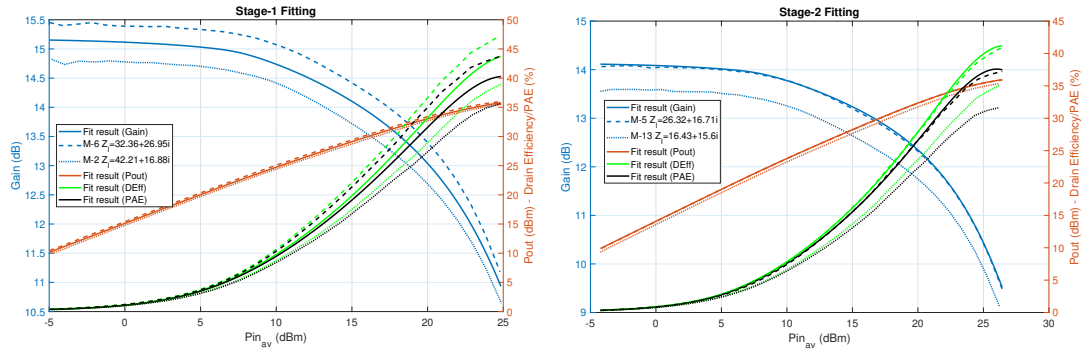


Figure 4.8: Power sweep simulation of 2 stage MMIC with 2:4 topology at 10 GHz

Fig. 4.8 shows that under 5.92 dB gain compression (denoted as *Comp (dB)*), 1st stage only goes into 1.32 dB compression (*Comp1*), while the output stage gain is compressed by 4.6 dB (*Comp2*). Figure 4.9 shows the accuracy of the

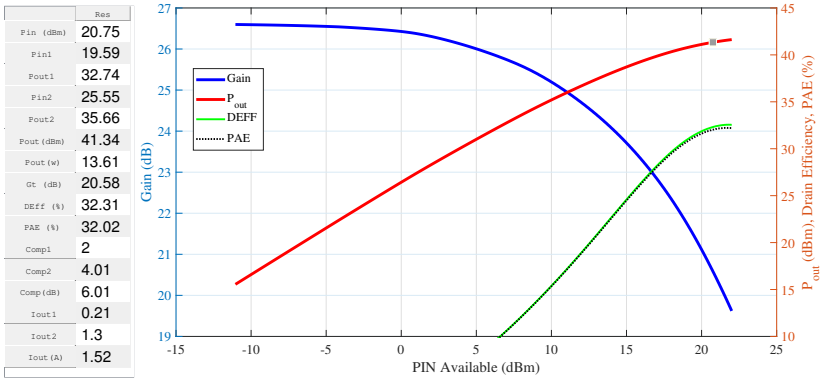


(a) (b)

Figure 4.9: Power sweep fittings for a) 1st and b) 2nd stage transistors and load-pull measurements superposed

curve fitting, in comparison to two neighboring load impedances, which ensures the accuracy of MMIC simulation under given input conditions (source&load impedances and network losses). This topology offers 41.63 dBm output power under 5.92 dB compression, satisfying the design targets.

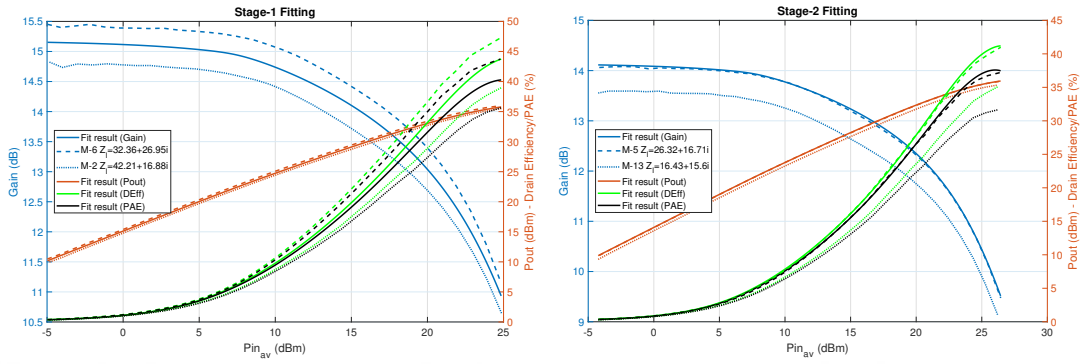
Alternative 1:4 topology is also simulated in the same way and the results are presented in Fig. 4.10.



	Res
Pin (dBm)	20.75
Pin1	19.59
Pout1	32.74
Pin2	25.55
Pout2	35.66
Pout(dBm)	41.34
Pout(w)	13.61
Gt (dB)	20.58
DEff (%)	32.31
PAE (%)	32.02
Comp1	2
Comp2	4.01
Comp(dB)	6.01
Iout1	0.21
Iout2	1.3
Iout(A)	1.52

Figure 4.10: Power sweep simulation of 2 stage MMIC with 1:4 topology at 10 GHz

Power simulation results of 1:4 topology reveal that despite the boost in efficiency, output power offered by this topology falls just short of design specifications. While this simulation is based on assumptions of load and source



(a) (b)

Figure 4.11: Power sweep fittings for a) 1st and b) 2nd stage transistors and load-pull measurements superposed

impedances that will be presented to devices as well as assumed matching network losses, thus is not definitive; it gives a relative idea about the expected results from the specific topologies.

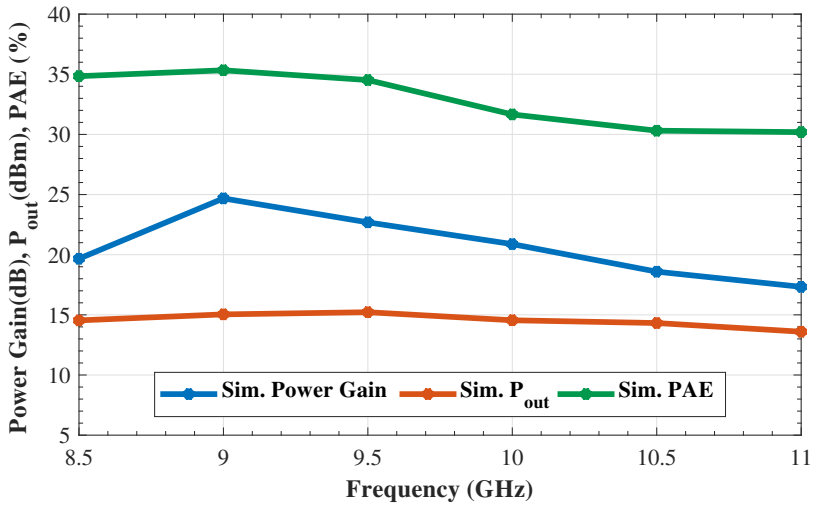


Figure 4.12: Power simulation results at 6 dB compression for 2:4 topology in 8.5 GHz - 11 GHz band

Based on this analysis, amplifier design is commenced with 2:4 topology due to its better prospects to deliver specified output power under limited gain compression. Power sweep simulations performed for 2:4 topology at 6 dB compression across the band yield the results presented in Fig. 4.12.

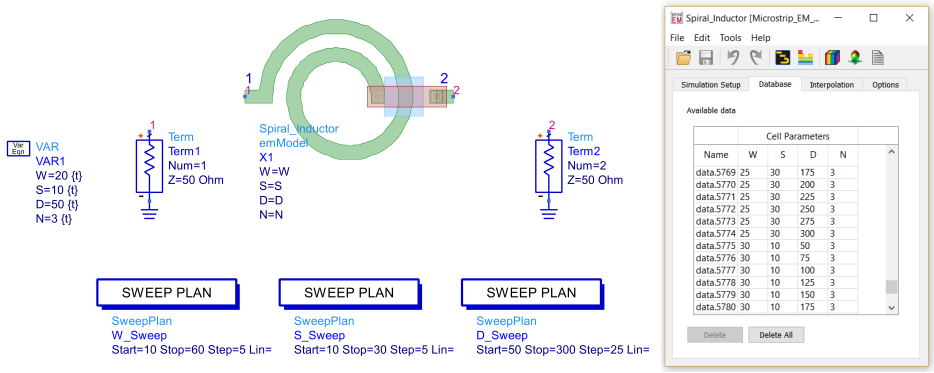
4.3 Passive Component EM Model Library

Behaviour of passive circuit elements substantially deviate from their low frequency lumped models as the frequency increases. To simulate high frequency response of on-chip passive elements, either analytical lumped-element equivalent circuit models for distributed components have to be developed, or these distributed structures require to be simulated in EM field solvers.

While it is faster and computationally easier to work with analytical lumped-element equivalent circuit models of passive elements, it is particularly difficult to obtain accurate, broadband and scalable models that hold for wide range of layout parameters. On the other hand, despite its flexibility and better accuracy, performing EM simulations for every layout part causes layout design process to be cumbersome and slow.

To overcome this problem and benefit from the advantages of these two approaches; table based models of microstrip components has been created where parametric layouts of all the circuit components are swept across a range of common parameter values and EM simulated beforehand (Fig. 4.13a).

Simulation results corresponding to these nested sweeps are kept at ADS *emModel* tables and recalled when needed (Fig. 4.13b).



(a) Nested parameter sweep schematic of inductor EM model

(b) EM model data table of the inductor

Figure 4.13: Schematic and EM model data table view of spiral inductor

Any data that falls between the simulated parameter values can be interpolated. This is considered to be a better approach than depending on analytical models, since the analytical models are essentially derived from EM analysis by curve fitting them to an equation. Typically, the equation is too simplistic to include all the details at high frequency that the EM simulation can capture.

EM simulation substrate stack (Fig. 4.14) in ADS for the 100 µm thick microstrip process is optimized based on the DC and RF measurements of passive test structures and process data.

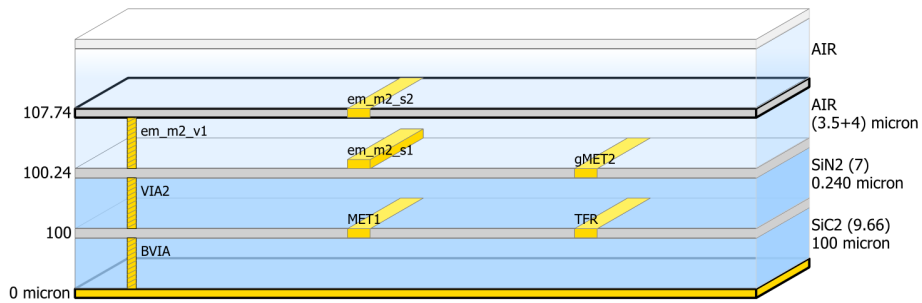


Figure 4.14: EM substrate stack used in ADS

Conductivities of 1st (thin) metal (*MET1*) and 2nd (thick) metal (*em_m2_s1*) layers are 3.4×10^7 S/m and 3.7×10^7 S/m respectively. Sheet resistance of thin film resistor layer (*TFR*) is 30 Ω/□. Metal-insulator-metal (MIM) capacitance density between the 1st and 2nd metal layers is about 258 pF/mm^2. Dielectric loss tangents for capacitor nitride layer (*SiN2*) and Silicon Carbide base layer (*SiC2*) are 0.001 and 0.03 respectively.

To demonstrate the high frequency behaviour of on-chip spiral inductors and the accuracy of the EM models in predicting them; measurement results of a fabricated spiral inductor that corresponds to 600 pH (seen in the layout in Fig. 4.15) are compared (in Fig. 4.16) with its EM model and an ideal lumped inductor.

Smith Chart Fig. 4.16b illustrates that spiral inductor quickly deviates from the ideal inductor behaviour as the frequency increases; which is captured by the EM model fairly accurately, together with the increase in effective inductance and the resonance around 38 GHz.

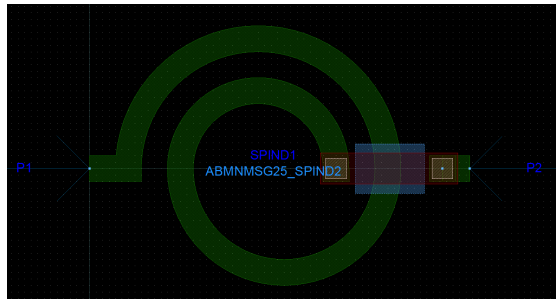
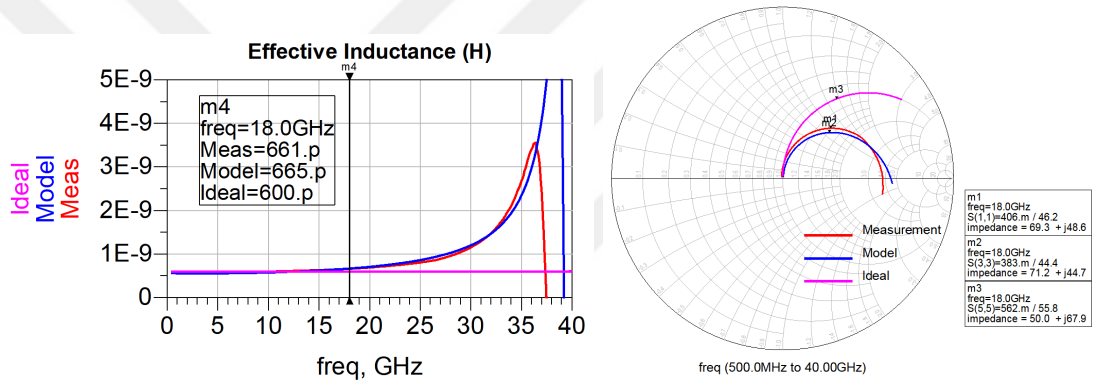


Figure 4.15: Layout of the on-chip spiral inductor that correspond to 600 pH



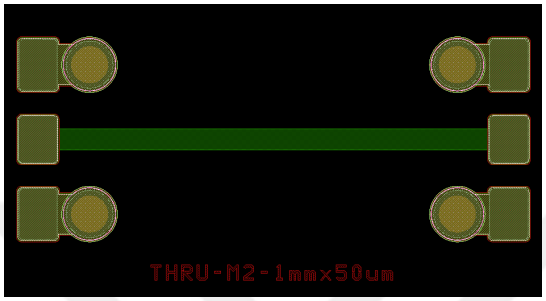
(a) Effective inductance comparison

(b) Frequency response of inductors in Smith Chart

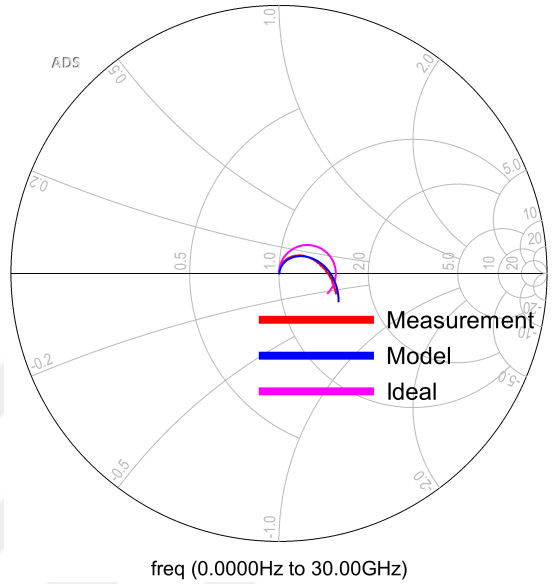
Figure 4.16: Comparison of inductor measurement and simulation results with ideal inductor response

As for the accuracy of distributed element simulations, measurement and EM model simulation results of a 50 µm wide and 1 mm long line (Fig. 4.17a), corresponding to a 62 Ω transmission line of 45° electrical length at 12 GHz are presented in Fig. 4.17b.

Fig. 4.17b shows that EM model representation of transmission lines are also fairly accurate up to *Ka*-band frequencies.



(a) Layout of the microstrip transmission line



(b) Frequency response comparison of measured, modeled and ideal TLs in Smith Chart

Figure 4.17: Comparison of transmission line measurement and simulation results with ideal TL response

4.4 Stability

Preventing unwanted oscillations in amplifiers is a vital aspect of the design cycle. Circuits become more complex from the stability analysis perspective as multiple transistors are used either as cascaded or in parallel configuration; leading to many possible cases that may satisfy oscillation conditions.

Especially in power amplifiers, stability analysis becomes more critical than small-signal amplifiers. Since transistor characteristics change under large-signal regime and pulse operation modes, conventional small-signal stability analysis is not sufficient to ensure unconditional stability of the amplifier [35]. In addition to the standard even-mode tests, necessary precautions against odd-mode and parametric oscillations should also be taken.

In this design, small-signal even-mode stability is ensured by checking the μ factors of individual cascaded stages. Instead of designing stability networks

based on a single S-parameter measurement, multiple S-parameter measurements of the same type of transistor are used to account for different operation&bias conditions, fabrication variations and also to improve stability against parametric oscillations [35].

For odd-mode stability tests, we implement the method proposed by Freitag [36] by calculating impedances and admittances at the inputs and outputs of all active devices for all odd excitation modes to see whether they satisfy oscillation conditions.

To ensure unconditional stability in and out of the band, resistive losses need to be introduced by adding series or shunt stability networks to the circuit. However as the full design develops, loss contribution from these networks can be reduced or these networks can be removed altogether as the losses coming from the practical implementation of the layout help to stabilize the network.

A two step approach is followed in stabilization, where transistors are initially stabilized before matching network design with the addition of a stability unit cell, improving even-mode stability to a certain degree; and then after the full layout design of matching and bias networks are completed, extra stability networks (that don't affect matching at the operation frequencies) are added to gate bias lines to compliment even-mode stability and provide extra suppression against parametric oscillations of the amplifier stages.

4.4.1 Even-Mode Stability

In the even-mode stability analysis, μ factors of the two port networks are considered, since they better indicate relative level of stability, a larger value meaning greater device stability.

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta(S_{11}^*)| + |S_{21}S_{12}|} > 1 \tag{4.5}$$

$$\mu' = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta(S_{22}^*)| + |S_{21}S_{12}|} > 1 \tag{4.6}$$

where Δ is defined as:

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{4.7}$$

Stability (μ factor) and MAG of a single 8x125 µm HEMT can be seen in Fig. 4.18.

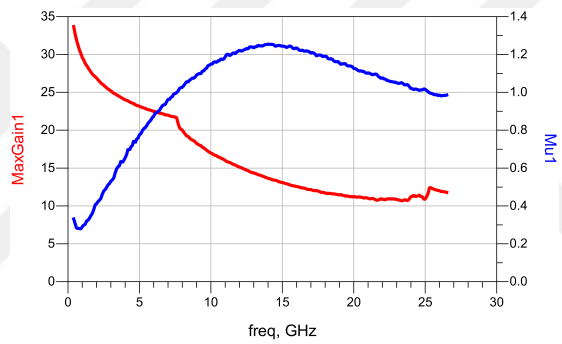


Figure 4.18: Stability and MAG of a 8x125 µm HEMT before stabilization

As the first step of even mode stabilization, a parallel RC circuit added in series (Fig. 4.19) just before the transistor gate feed. Resistor and capacitor values of the stability cell are tuned in such a way to impact the MAG in band minimally and improve out-of-band stability (especially in low frequencies) until μ and μ' are greater than approximately 0.9 throughout the frequency spectrum. Transistors are not unconditionally stabilized at this point, as the loss contribution that will come from realized matching and bias networks will also increase the stability. Layout of this stability cell is implemented symmetrically to create less asymmetry for RF signal propagation between gate fingers.

A single μ factor analysis should be a sufficient indicator of unconditional stability for all passive loads presented to a two port network under nominal small-signal conditions. However, stability behaviour of transistors change under different bias (different voltages and quiescent drain currents, CW vs. pulsed operation) and temperature conditions. Also, transistors performances vary on a single wafer, as well as among the different fabrication runs. To account for

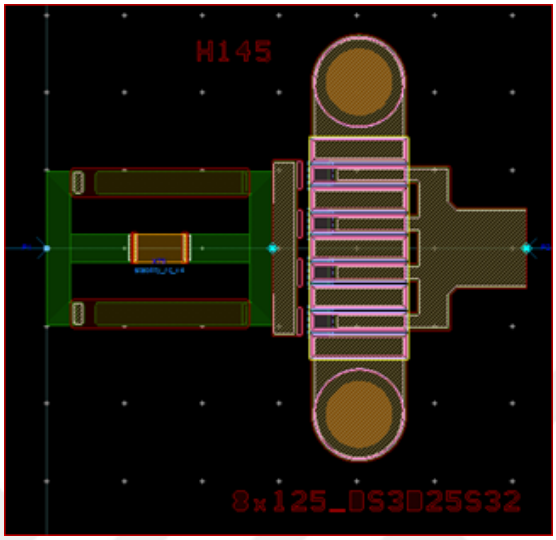


Figure 4.19: Layout of the transistor with input stability cell

such variations, batch S-parameter simulations encompassing a range of devices and operation conditions are performed for even-mode stability analysis using the *Data Access Component (DAC)* tool of ADS (Fig. 4.21).

Next step of device stabilization is implemented after the design of matching and bias networks are completed. Even-mode stabilities of individual amplifier stages partitioned as in the Fig. 4.20 are analyzed. Extra stability elements are added to gate bias lines to improve stability until both two port networks are unconditionally stable (Fig. 4.21).

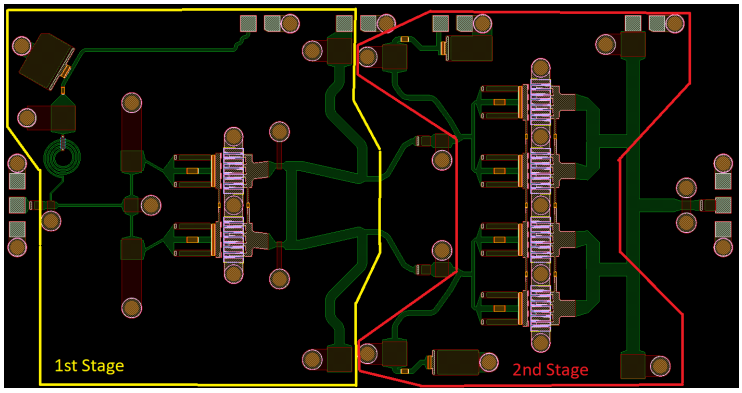
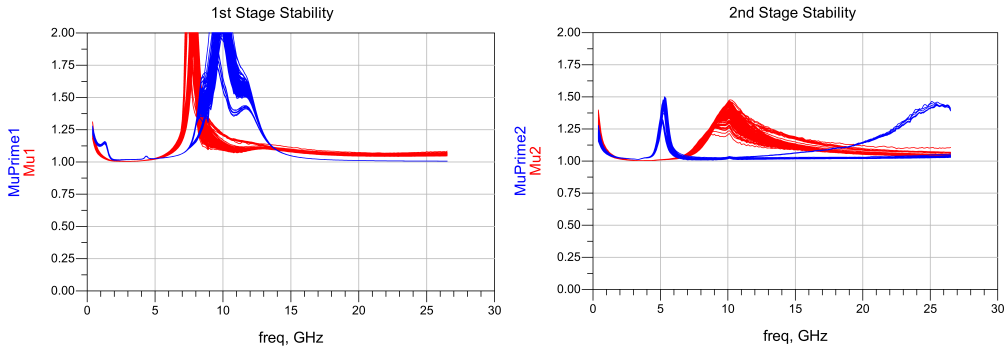


Figure 4.20: Layout partitioning of 1st and 2nd stages in even-mode stability tests

Addition of these extra elements do not interfere with impedance matching in



(a) 1st stage μ stability factors (b) 2nd stage μ stability factors

Figure 4.21: Even-mode stability results of both stages

the operation frequency band, since they are added after the RF choke inductors and RF grounding capacitors in the bias lines and remain in the DC portion of the circuit. Overall stability circuit topology is in line with the scheme suggested for suppressing parametric oscillations [35] and is expected to improve stability against unpredicted low frequency oscillations.

4.4.2 Odd-Mode Stability

Amplifier stages where a number of transistors are used in parallel configuration are designed to work in even-mode operation, where all transistors are assumed to be excited with an RF signal of the same phase and amplitude. However transistors can have slight variations in g_m and gate threshold voltages which, when biased with the same gate voltage, results in different quiescent drain currents between transistors. In addition to that, in the realized layout, individual matching networks of each transistor will present slightly different load and source impedances. These differences in transistor performances may create conditions for odd-mode or differential-mode excitations. Combined with high transistor gain and finite device isolation (reverse transmission), these conditions may lead to odd-mode oscillations through the feedback loops existing between parallel transistors. Therefore, amplifier designs consisting of multiple parallel transistors have to be checked for odd-mode stability using appropriate techniques.

In this design, we have implemented (Fig. 4.22) Freitag's method of odd mode stability analysis. Impedances and admittances at the inputs and outputs of all active devices (for all odd excitation modes) are calculated. Negative impedances or admittances at the input and output nodes of the devices are undesirable since they may fuel instabilities [36]. Full criteria for the onset of a stable oscillation are a subset of this condition [37].

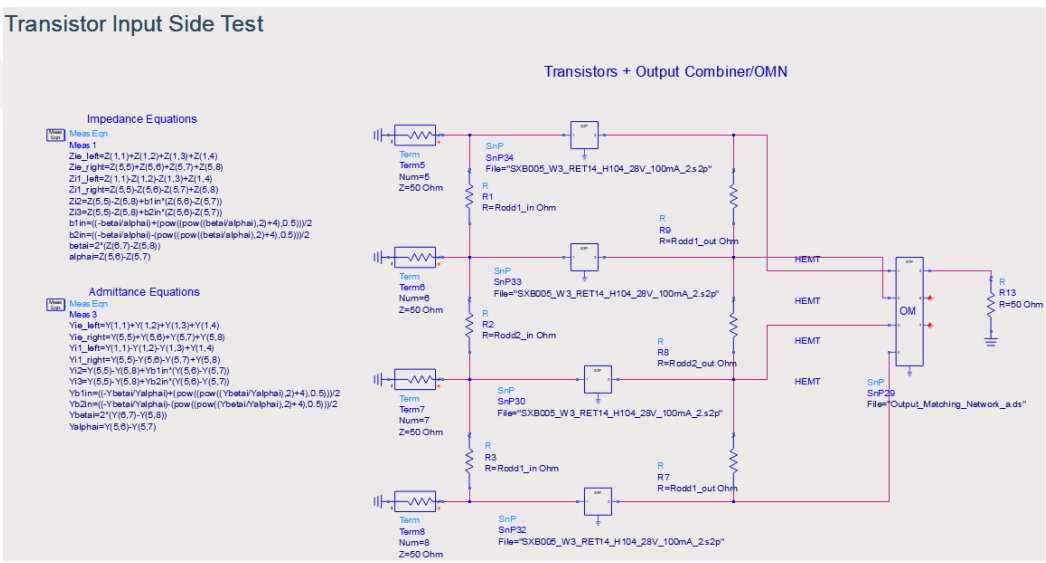


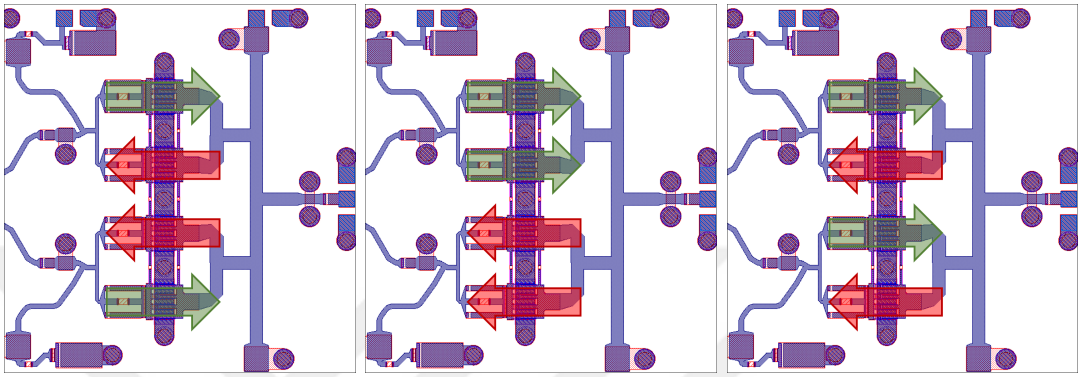
Figure 4.22: One of the ADS schematics for calculating odd-mode impedances and admittances at the input and output of 2nd stage transistors for odd-mode stabilization

All three odd oscillation modes that a 4-branch network can support (namely *[+,-,-,+]*, *[+,+,-,-]* and *[+,-,+,-]*) are considered in calculations (Fig. 4.23).

Respective impedance and admittance values are analyzed and necessary odd-mode suppression resistors (Fig. 4.24) are added between gate and drain feeds of transistors.

Results before and after the odd-mode stabilization are presented in the figures (Fig. 4.25, Fig. 4.26 and Fig. 4.27) below. To account for transistor variations and for robustness, phase perturbations are introduced. Stability is preserved even under a phase imbalance of 10° between branches.

Without any odd-mode suppression resistors between the transistors at power



(a) Odd Mode #1 configuration, ([+,-,-,+])

(b) Odd Mode #2 configuration, ([+,+,-,-])

(c) Odd Mode #3 configuration, ([+,-,+,-])

Figure 4.23: Schematic representations of odd excitation modes

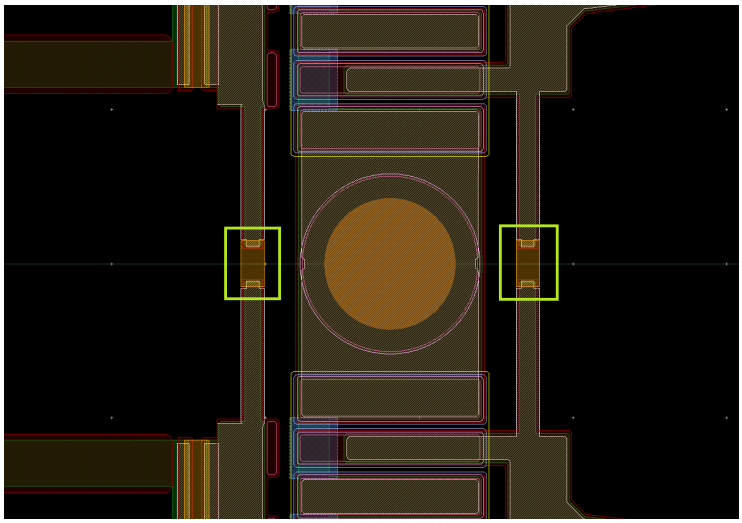


Figure 4.24: Highlighted odd-mode suppression resistors between the gate and drain manifolds of the HEMTs

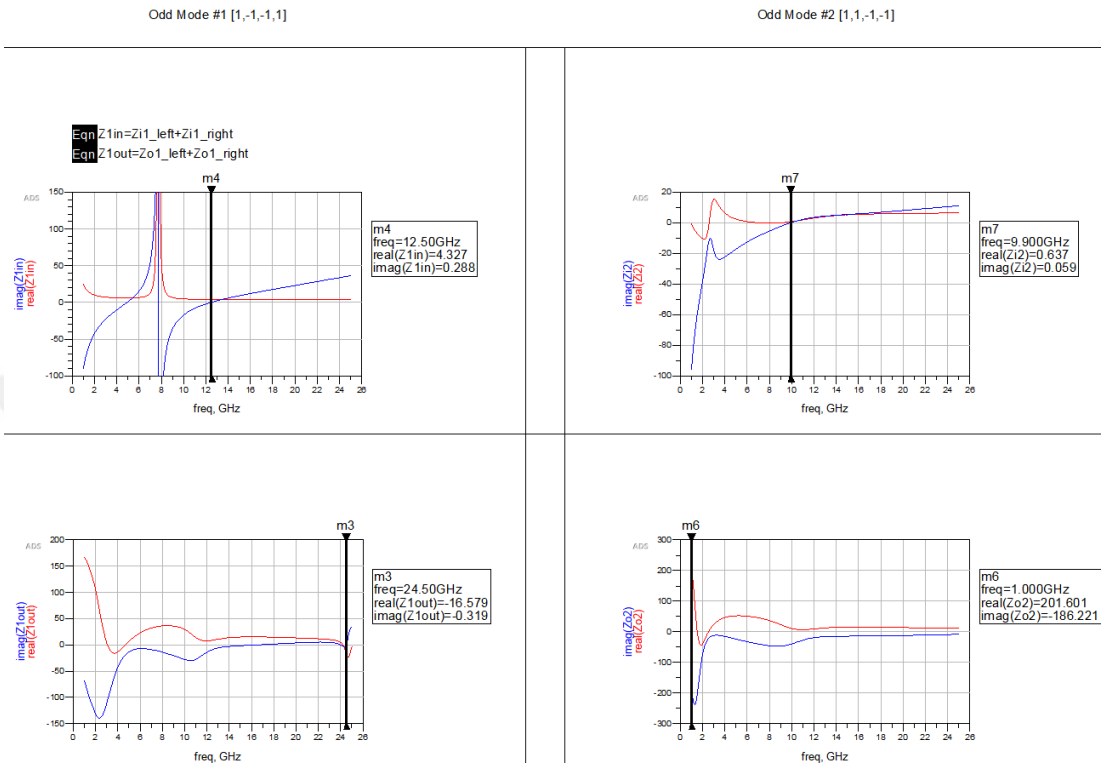


Figure 4.25: Odd-mode impedances calculated at the input and output of 2nd stage transistors before odd-mode stabilization

stage, there seems to be an instability around 24.5 GHz and a dangerously close situation around 9.9 GHz, as can be seen in the Fig. 4.25.

When the odd-mode suppression resistors are added, conditions for the onset of odd-mode oscillations are not satisfied anymore, and the stability margin is improved. Complete list of impedances and admittances after the addition of odd-mode resistors can be seen in the Fig. 4.26 and Fig. 4.27 below.

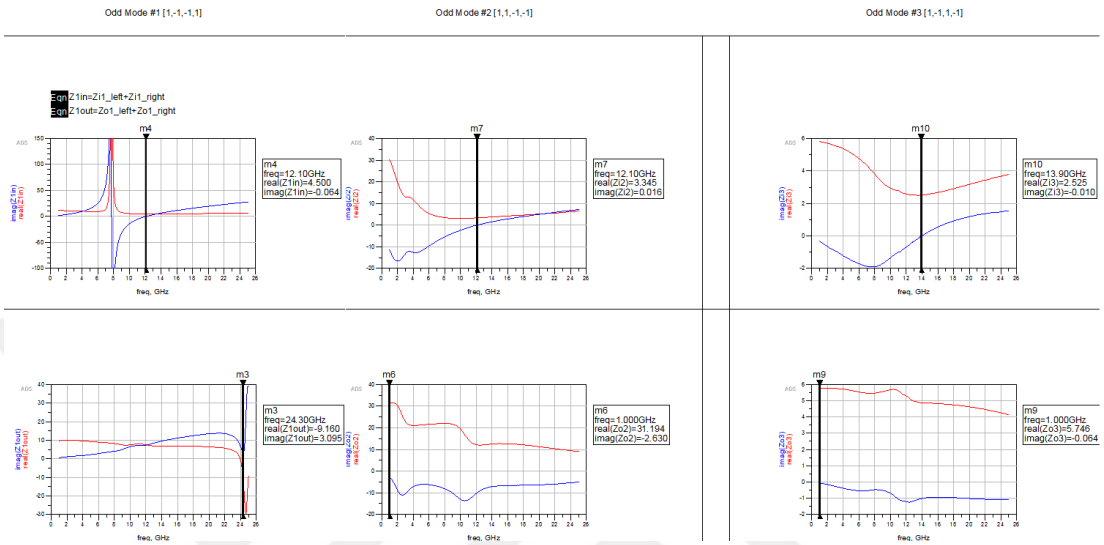


Figure 4.26: Odd-mode impedances calculated at the input and output of 2nd stage transistors after odd-mode stabilization

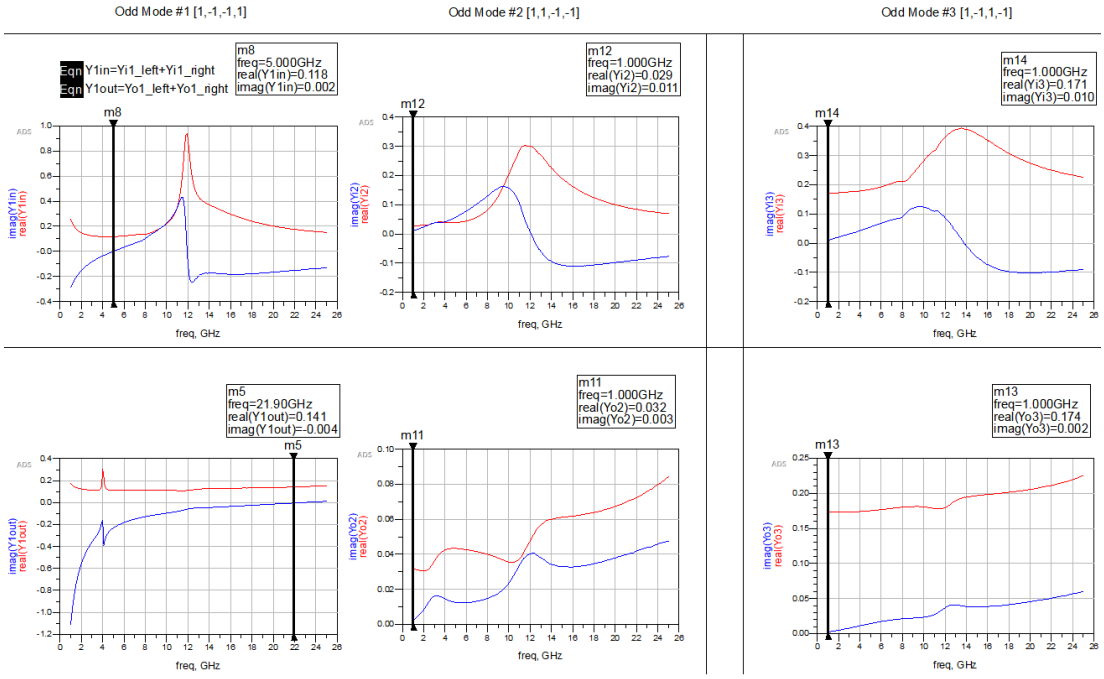
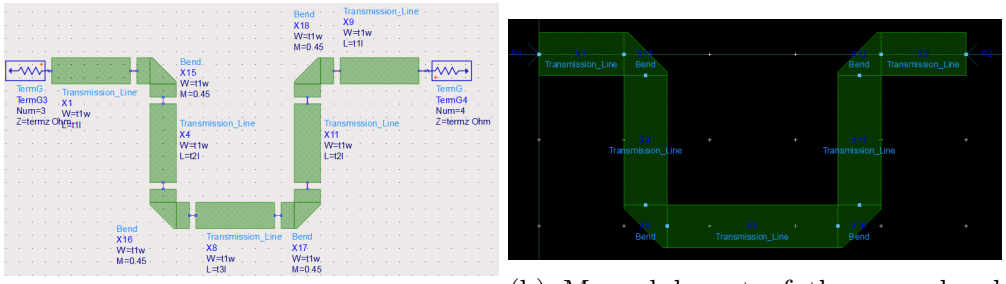


Figure 4.27: Odd-mode admittances calculated at the input and output of 2nd stage transistors after odd-mode stabilization

4.5 Bias and Matching Networks

Design of bias and RF matching networks start with lumped components and ideal transmission lines on schematic level. Purpose of this design phase is to quickly investigate a number of topologies and find suitable ones, considering the matching accuracy, bandwidth, loss and approximate die area circuits will occupy when realized. After this phase of design, circuits are implemented and tuned using the EM models of passive circuit elements. EM component models give a more realistic idea about the final performance of design

Schematic simulations and EM models however, have few shortcomings in predicting the behaviour of merged and tightly packed layouts. EM simulation results of components when simulated individually, may differ from the ones that are used in the actual merged layout. Despite their solid performance in most topologies, models deviate from the full (merged) layout results in situations where there are various discontinuities (such as meandered transmission lines, bends, tee/cross junctions, etc.), especially when there is only a small distance between the discontinuities. One example situation is the meandered line topology examined in the figures below. When the distance between the microstrip bends fall below approximately 200 µm (which is two times the substrate thickness) results of EM models start to deviate from the EM simulation results of the full layout.



(a) Meandered line schematic created with EM models

(b) Merged layout of the meandered line

Figure 4.28: Schematic and merged layout views of a meandered microstrip transmission line

Another difference we encounter is when there are nearby components that are within the coupling distance of the existing components. This is also connected

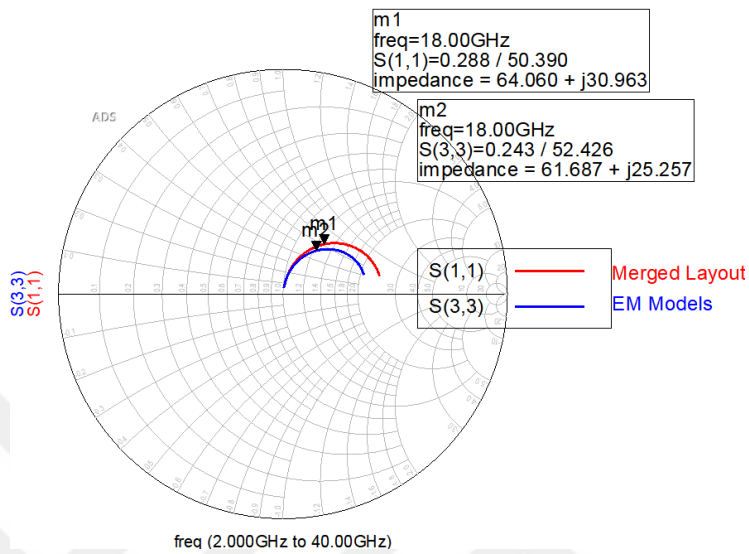


Figure 4.29: Frequency responses of schematic simulation vs. merged layout of a meandered transmission line structure

to the asymmetry problem encountered in matching circuits which is explained in more detail in the output matching section below. Models, of course, fail to simulate such effects and seemingly symmetric branches present different impedances to the transistors.

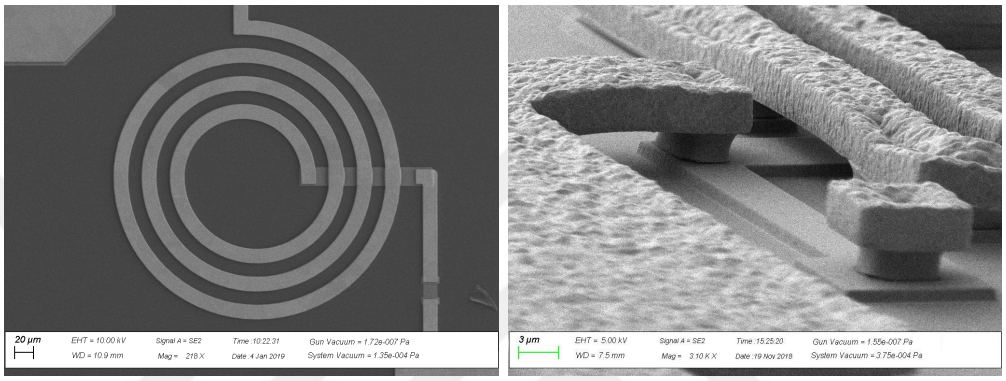
Therefore, as the final step of layout design process, fully merged layouts of matching networks are constructed as parametric cells and layout parameters are optimized towards design goals based on EM simulations.

4.5.1 Gate and Drain Bias Networks

It is necessary to have sufficient isolation between the DC bias ports and the rest of the amplifier circuit. Any changes beyond the DC pads should not affect RF circuit, and RF signal should not leak through the DC ports. Having a significant RF suppression in DC bias paths is also beneficial for bias loop stability. Ideally, this is achieved with a series *RF choke* inductor and a set of shunt RF grounding capacitors of various sizes, forming a low pass filter.

However, due to their relatively big sizes and current carrying limitations, it

is not always possible to use inductors in bias feeds. Current carrying capacity of inductors are significantly less than a transmission line of the same line width, since at the metal-metal crossovers of inductor turns all the current flows through the thin metal layer at the air-bridge underpass (Fig. 4.30).



(a) Top view of an on-chip spiral inductor

(b) Angled close-up of another inductor's air-bridges at metal cross overs

Figure 4.30: SEM images of on-chip inductors

Therefore, DC biases of transistor drain sides, where a single 1 mm transistor can draw up to 400 mA current, are fed through transmission lines (Fig. 4.31). RF grounding capacitors of certain dimensions are added to these lines to provide sufficient RF isolation at operation frequencies.

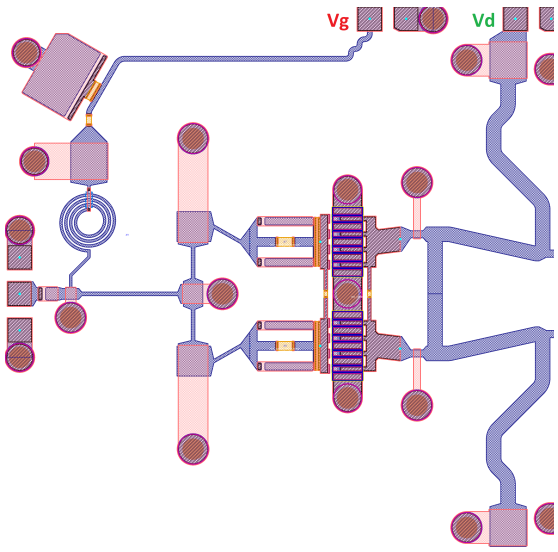
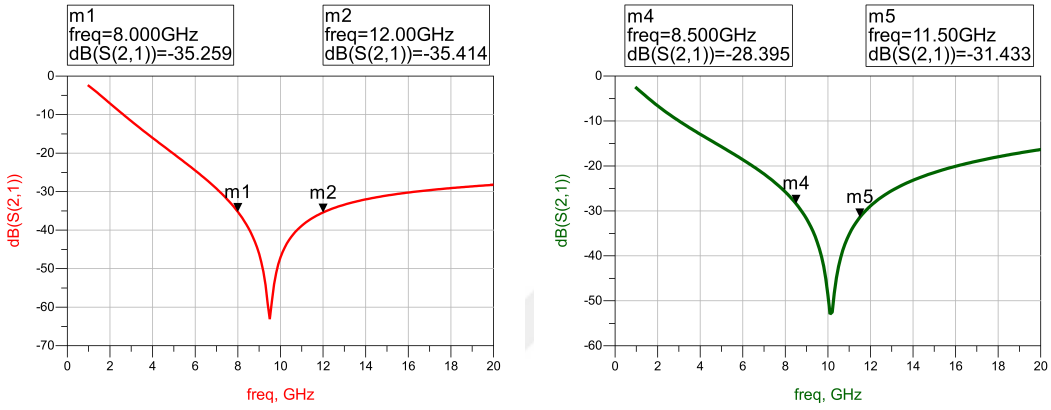


Figure 4.31: Layout view of the 1st stage gate and drain bias networks

Isolation of gate and drain bias lines are given in Fig. 4.32.



(a) (b)

Figure 4.32: RF isolations of a) 1st stage gate and b) drain bias networks

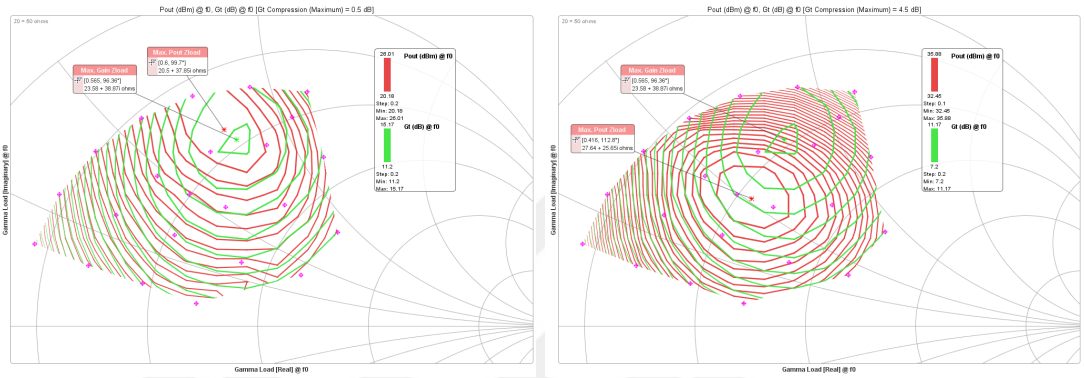
1st stage gate bias line presents a very high impedance in band, thus have negligible affect on matching. Whereas 2nd stage gate bias line and drain bias lines are integrated into matching networks, acting as shorted transmission line stubs.

4.5.2 Output Matching

Output matching networks are arguably the most crucial parts of power amplifier designs. Load impedances presented to output stage transistors directly affect amplifier power output and efficiency figures. Therefore, extensive effort is required to optimize output matching in such a way to provide ideal load impedances to transistors and eliminate any asymmetry between the branches while maintaining a low net insertion loss for minimum dissipation of valuable output power.

Although the maximum output power and maximum gain corresponds to the same goal in small-signal regime, under large-signal operation these two become separate parameters. Load impedance that provides highest gain diverges from the maximum output power impedance.

Therefore, there has to be a trade-off between gain, output power and efficiency of the device in output matching design. This phenomenon can be observed in the load-pull contours presented below.



(a) (b)

Figure 4.33: P_{out} (red) and G_T (green) contours of the 8x125 µm HEMT under a) 0.5 dB and b) 4.5 dB G_T compression

In low input powers (Fig. 4.33a), two set of contours (P_{out}, and transducer power gain (G_T)) concentrate around the same impedance. Whereas two goals begin to diverge as G_T compression increases (Fig. 4.33b) and device enters large-signal operation region. As an implication of this, obtaining low output reflections (via matching to maximum gain impedance/small-signal conjugate matching) and matching for maximum output power are contradictory goals, which is reflected in the usually poor $|S_{22}|$ figures of conventional power amplifiers.

Cluster matching technique has been used in output matching design, for combining output power of transistors, as well as presenting optimum output impedances to the transistors. In this method, transistors and output matching network are effectively used as active power combiners, avoiding a significant amount of extra passive circuitry for power combining. Layout of the design output matching network can be seen in Fig. 4.34a.

Load-pull contours of an 8x125 µm HEMT at the start of the frequency band (8.5 GHz) (Fig. 4.36a), mid-band (10 GHz) (Fig. 4.35), and at the end of the band (11 GHz) (Fig. 4.36b) are presented below.

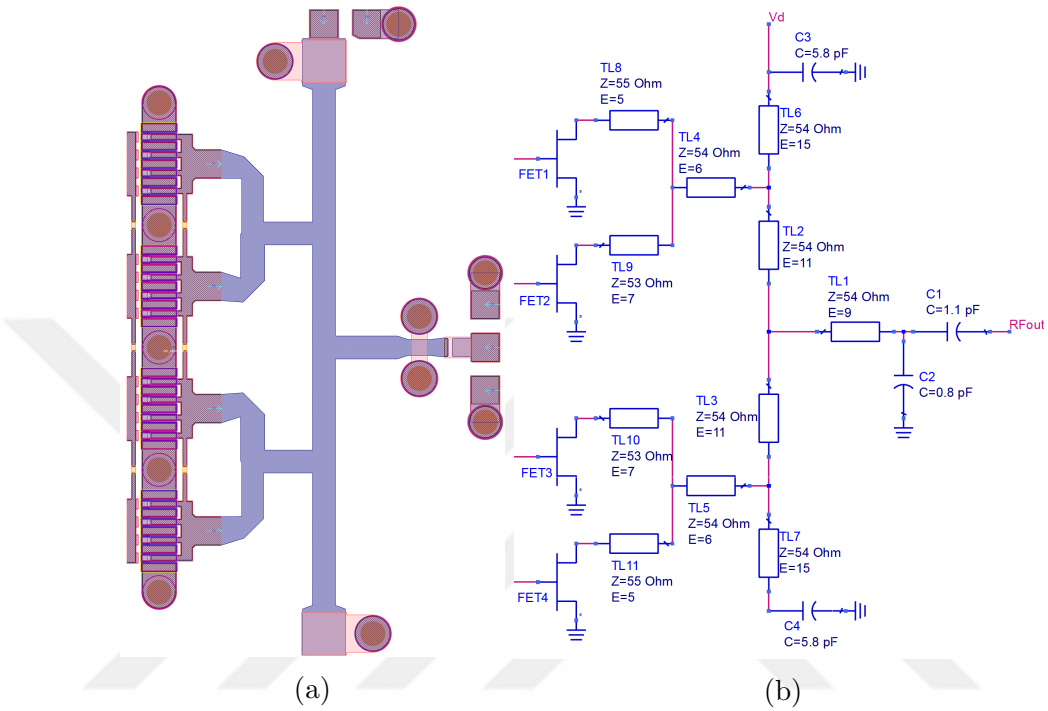


Figure 4.34: Layout (a) and schematic (b) view of the 2nd stage transistors and OMN (TL electrical lengths in schematic view are @10GHz)

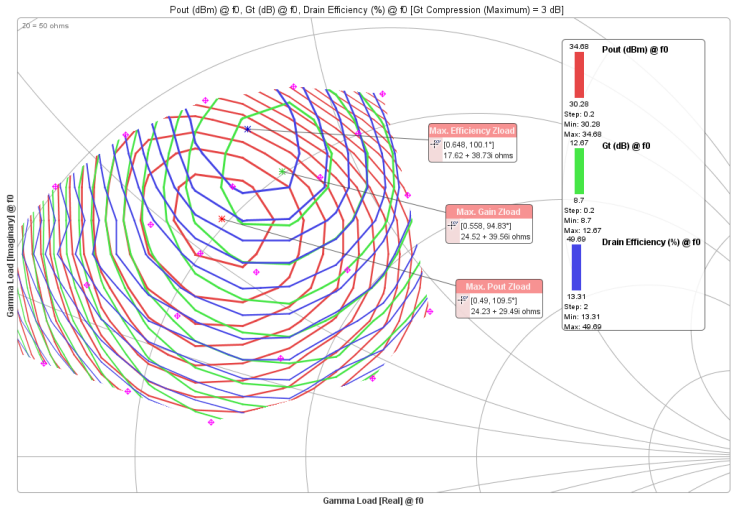
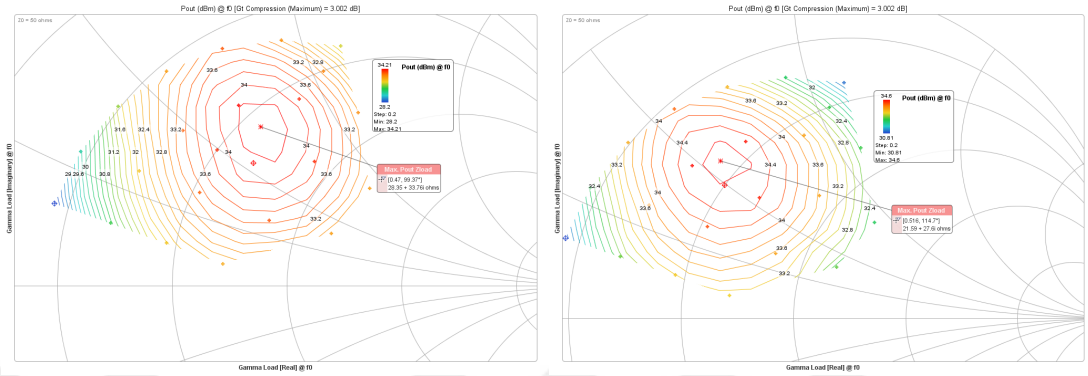


Figure 4.35: P_{out} (red), transducer gain (green) and drain efficiency (blue) contours of the 8x125 µm HEMT at 3 dB compression at 10 GHz



(a) (b)

Figure 4.36: P_{out} contours of the 8x125 µm HEMT at a) 8.5 GHz and b) 11 GHz at 3 dB compression

Load impedances presented to output stage transistors by the OMN are calculated using the EM simulation of the merged OMN layout (Fig. 4.37 and Table 4.8). Note that 2nd stage load impedances achieved by the output matching network are quite close to ideal load-pull impedances.

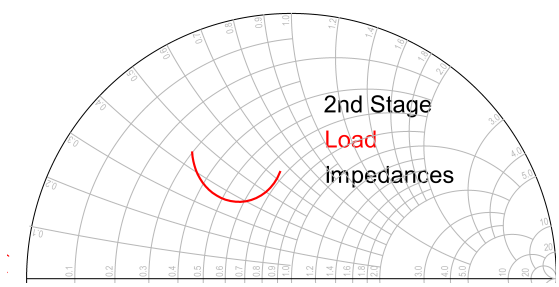


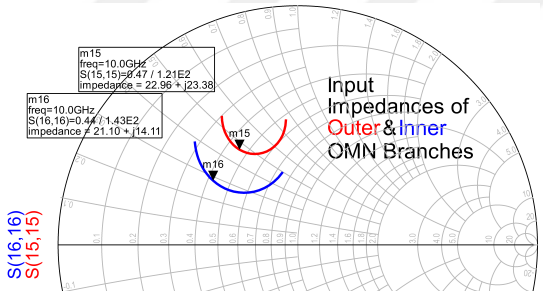
Figure 4.37: Load impedances presented to output stage transistors between 8.5 GHz - 11 GHz

It is important to preserve the phase and amplitude balance between OMN and ISMN branches to ensure output stage HEMTs are driven with equal magnitude and phase. Any deviation from this balance deteriorates even-mode operation conditions of transistors and out-of-phase power addition results in less than designed output power. However, layout symmetry does not ensure electrical symmetry, and seemingly identical RF paths may present different impedances and phases to different branches of the OMN. Impedances and phases of the innermost and outermost branches are calculated (Fig. 4.38) and layout asymmetries introduced in OMN (Fig. 4.34a) to minimize the differences between branches.

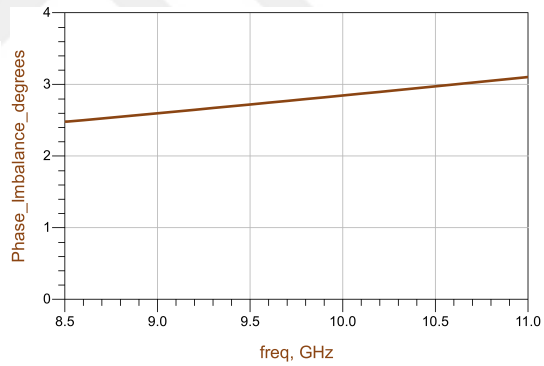
Freq. (GHz)	2nd Stage Zload
8.5	33.5+j32.2
9	33.2+j23.5
9.5	28.0+j18.7
10	22.5+j18.1
10.5	18.1+j19.8
11	15.0+j22.5

Table 4.8: 2nd stage load impedances presented by OMN

Fig. 4.38a shows the load impedances presented to output stage transistors at the outermost and the innermost branches. Fig. 4.38b shows the phase difference between the OMN branches, which is deemed sufficiently low to have any significant impact on power output.



(a) Impedances presented to inner and outer branches



(b) Phase difference between branches in degrees

Figure 4.38: Impedance and phase asymmetry between OMN branches at 8.5 GHz - 11 GHz band

Another criterion for matching network performance is the *net insertion loss* caused by the resistive and dielectric losses in the propagation media. Maximum available gain (MAG) of the OMN is calculated to eliminate mismatch losses and only calculate the RF propagation losses, which is a measure of how much of the valuable transistor output power will be dissipated during the output power combining. Fig. 4.39 shows the net insertion loss of OMN in the operation frequency band.

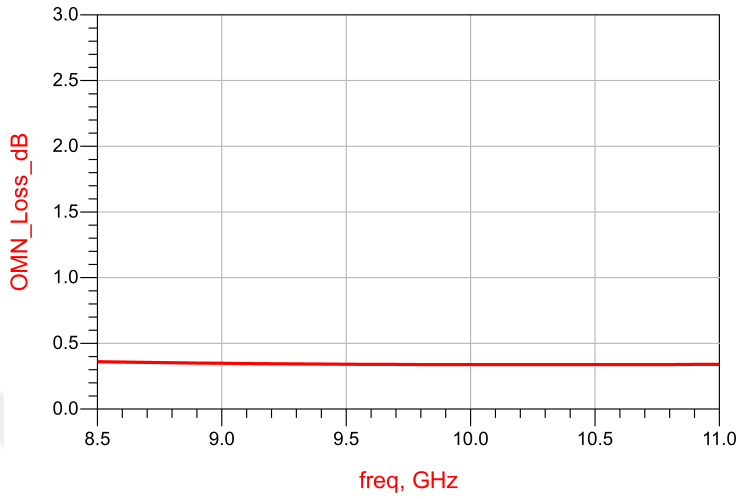


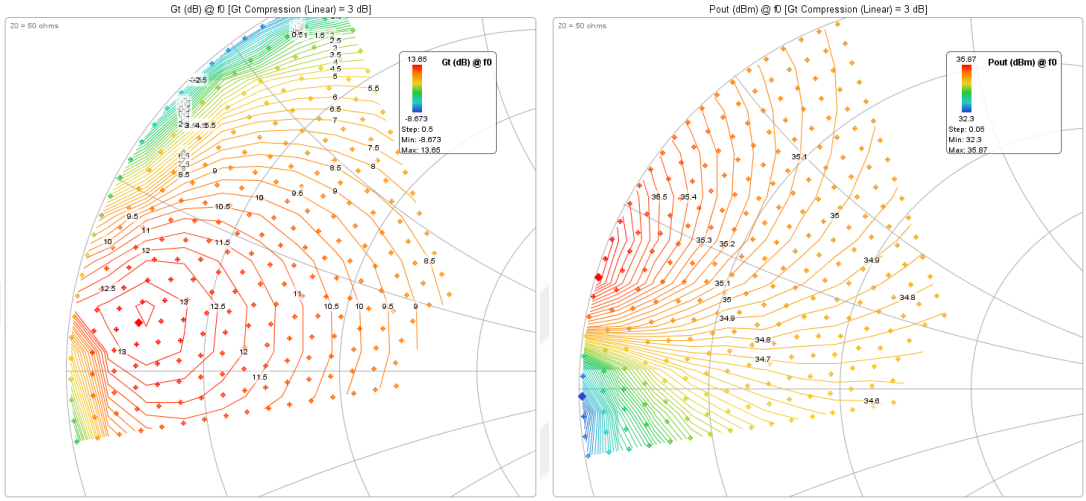
Figure 4.39: Net insertion loss of output matching network at 8.5 GHz to 11 GHz band in dB scale

4.5.3 Interstage Matching

Interstage matching is the section where output stage input impedances are matched to driver stage load impedances. Since the driver stage is required to supply sufficiently high power to the output stage, driver stage itself needs to be compressed. Therefore, drive stage of the HPA is also designed for large-signal operation using the load-pull data. In addition to that, source impedances of output stage HEMTs have an important effect on the gain and power output of transistors. Source-pull contours demonstrating this trade-off on the input side of transistors are presented in Fig. 4.40.

Schematic (Fig. 4.41) and layout (Fig. 4.42) views of the designed interstage matching network are given in figures below.

ISMN is symmetrical with respect to X-axis. First stage drain bias is shared via the transmission line that connects two halfs of the circuit, which is part of the matching network and acts as an open stub under even-mode excitation. Output stage DC gate biases supplied through the odd-mode suppression resistors to all transistors. Since the gate currents are typically on the order of few µA even under large input powers, DC voltage drop on these resistors is negligible.



(a) Transducer gain contours (b) Output power contours

Figure 4.40: Source-pull contours of an 8x125 µm HEMT at 3 dB compression at 9.5 GHz

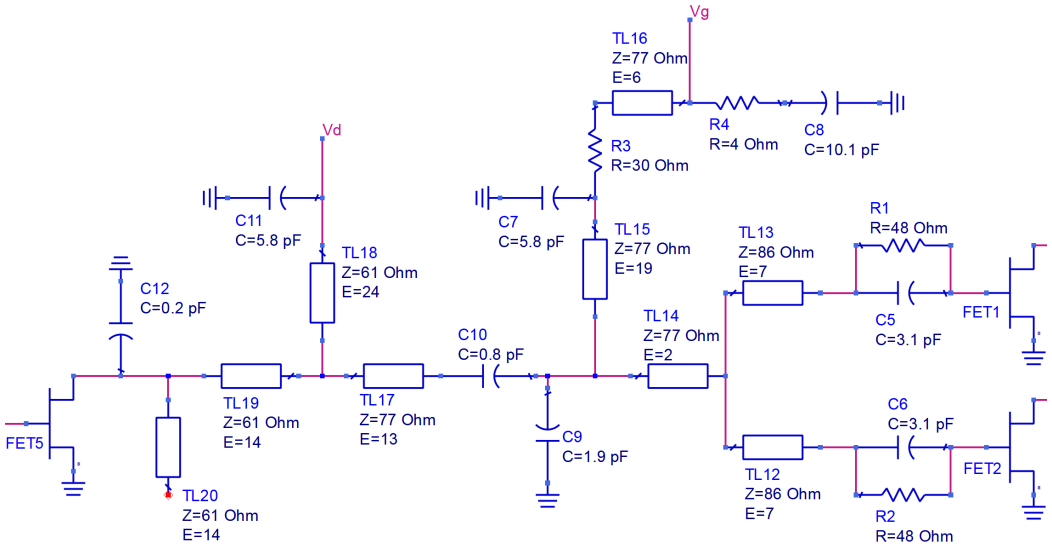


Figure 4.41: Schematic view of top half of the interstage matching network (TL electrical lengths are given @10GHz)

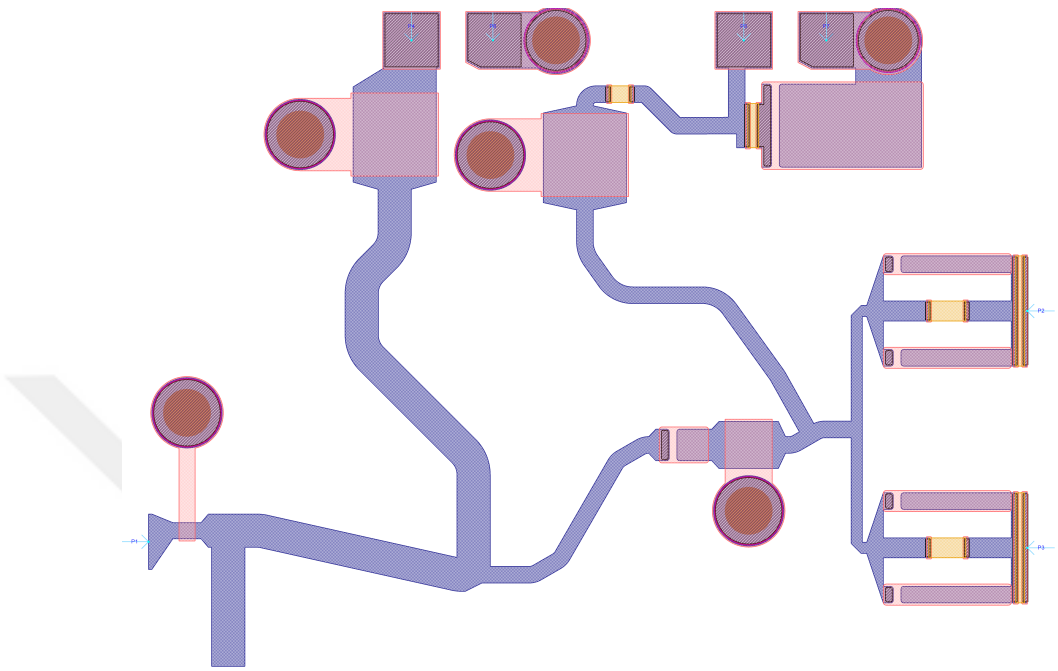


Figure 4.42: Layout view of top half of the interstage matching network

Even-mode impedances presented to 2nd stage sources (Fig. 4.43a) and the 1st stage loads (Fig. 4.43b) are presented in the Smith Chart and the Table: 4.9.

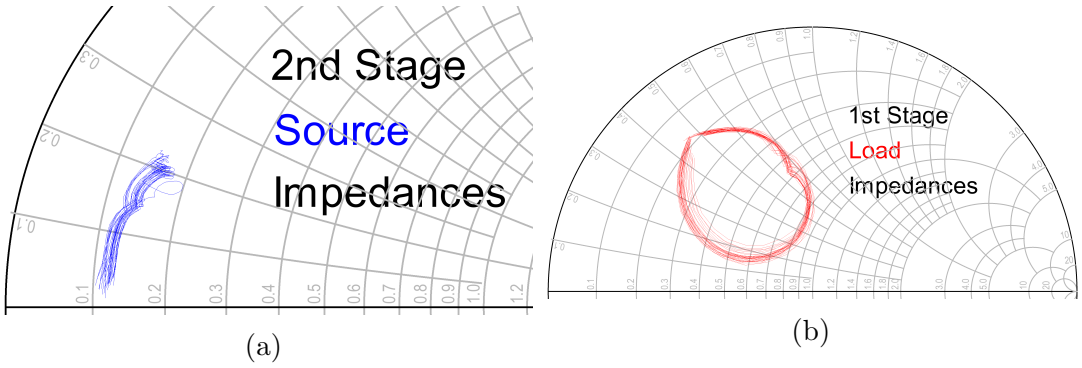


Figure 4.43: Output stage source (a) and driver stage load (b) impedances at 8.5 GHz - 11 GHz band

When considered with regards to the source-pull contours presented above (Fig. 4.40), 2nd stage source impedances, which are crucial for the power output and gain of the amplifier, are within the desirable region of the Smith Chart. In spite of the slight deviation from optimum load impedance areas of Fig. 4.36, 1st stage load impedances are still close to the high power area of the load-pull

Freq. (GHz)	2nd Stage Zsource	1st Stage Zload
8.5	5.1+j1.4	8.6+j22.4
9	5.7+j5.1	13.9+j30.8
9.5	6.6+j7.5	22.7+j34.7
10	7.7+j10.0	39.8+j25.6
10.5	8.6+j10.3	24.2+j11.1
11	7.6+j10.1	11.6+j21.6

Table 4.9: 1st stage load and 2nd stage source impedances presented by ISMN

contours, sufficient to provide necessary RF drive to the output stage.

Net insertion loss of the interstage matching network, together with the OMN losses are given in Fig. 4.44.

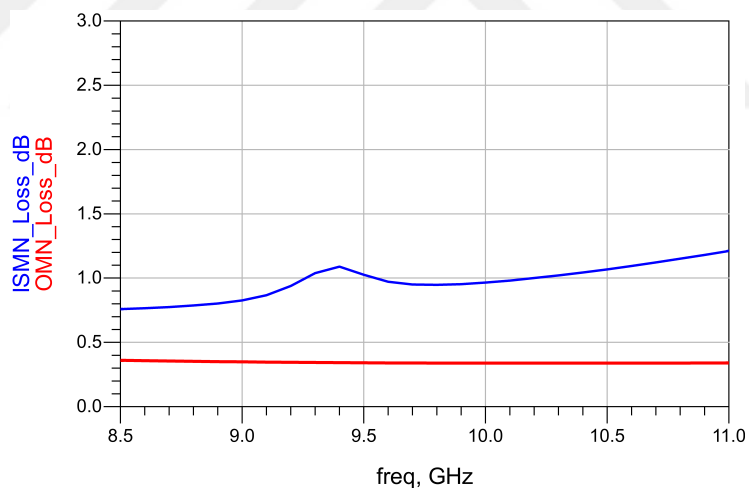


Figure 4.44: Net insertion losses of interstage and output matching networks at 8.5 GHz to 11 GHz band in dB scale

4.5.4 Input Matching

Two criteria are considered in the input matching network design: driver stage source impedances, and the input return loss of the overall amplifier. Schematic (Fig. 4.45) and layout (Fig. 4.46) views of the input matching network are shown in figures below.

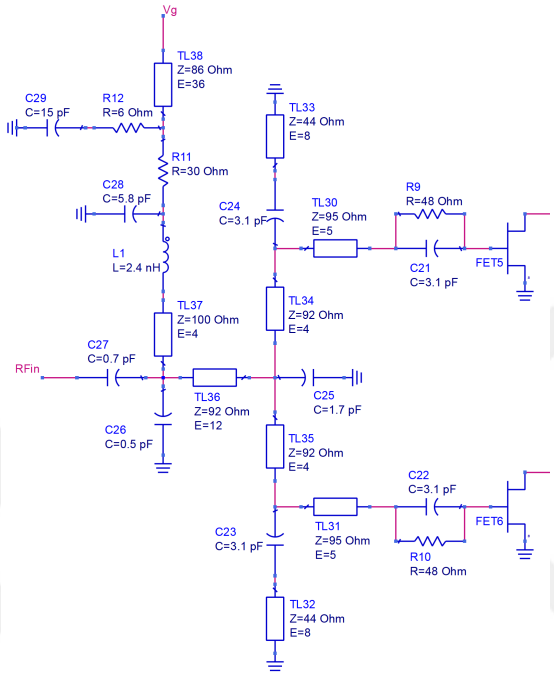


Figure 4.45: Schematic view of the input matching network (TL electrical lengths are defined @10GHz)

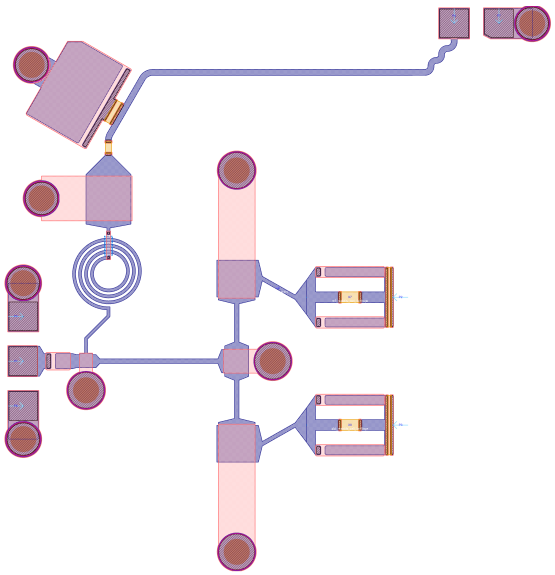


Figure 4.46: Layout view of the input matching network

Source impedances presented to 1st stage transistors at 8.5 GHz to 11 GHz band can be seen in Fig. 4.47 and Table 4.10.

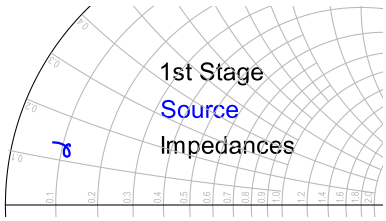
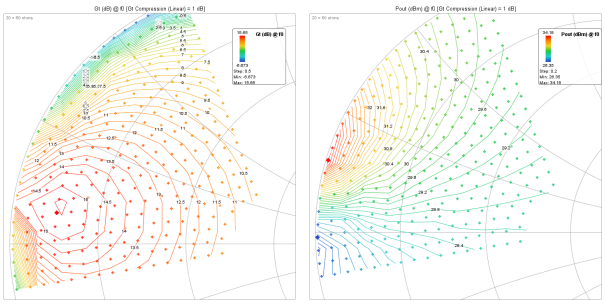


Figure 4.47: Source impedances presented to 1st stage transistors

Freq. (GHz)	1st Stage Zsource	1st Stage Zload
8.5	3.9+j6.7	8.6+j22.4
9	5.8+j6.3	13.9+j30.8
9.5	5.7+j5.5	22.7+j34.7
10	5.3+j6.3	39.8+j25.6
10.5	5.5+j6.8	24.2+j11.1
11	5.8+j6.8	11.6+j21.6

Table 4.10: Load and source impedances presented to 1st stage transistors

Impedances presented to the sources of driver stage transistors are between the areas of maximum transducer gain and maximum power contours in the source-pull graphs at 1 dB compression point presented in Fig. 4.48a and Fig. 4.48b below.



(a) Transducer gain contours

(b) Output power contours

Figure 4.48: Calculated source-pull contours of an 8x125 µm HEMT at 1 dB compression at 9.5 GHz

Output power requirements of the driver stage is achievable without any significant compression, even under small-signal input matching. Thus the driver

stage transistors' source impedances are less important than that of output stage transistors' in terms of output power; thus, a small-signal conjugate matching approach can also be followed in IMN design.

Small-signal simulations of the two stage amplifier performed using S-parameter measurement data of 30 transistors from 3 different wafers are presented in Fig. 4.49.

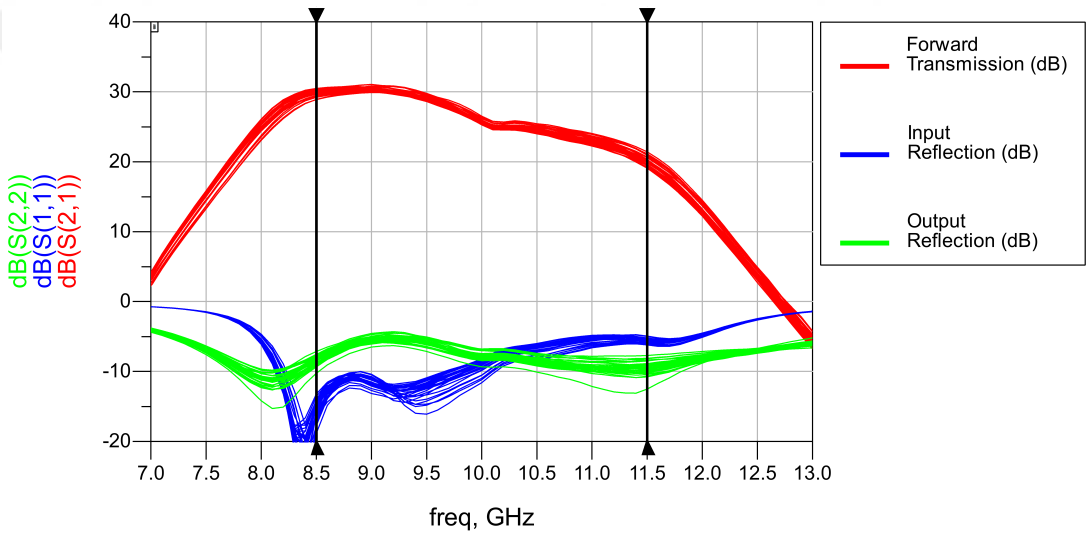


Figure 4.49: Small-signal simulation results of the design, performed using S-parameter data of 30 HEMTs

In these simulations, more than 20 dB gain with +/- 5dB variation is obtained throughout the 8.5 GHz - 11.5 GHz frequency band. Simulated input and output reflection losses are better than 5dB.

Overall schematic of the finished design is given in Fig. 4.50 and the corresponding circuit layout can be seen in Fig. 4.51.

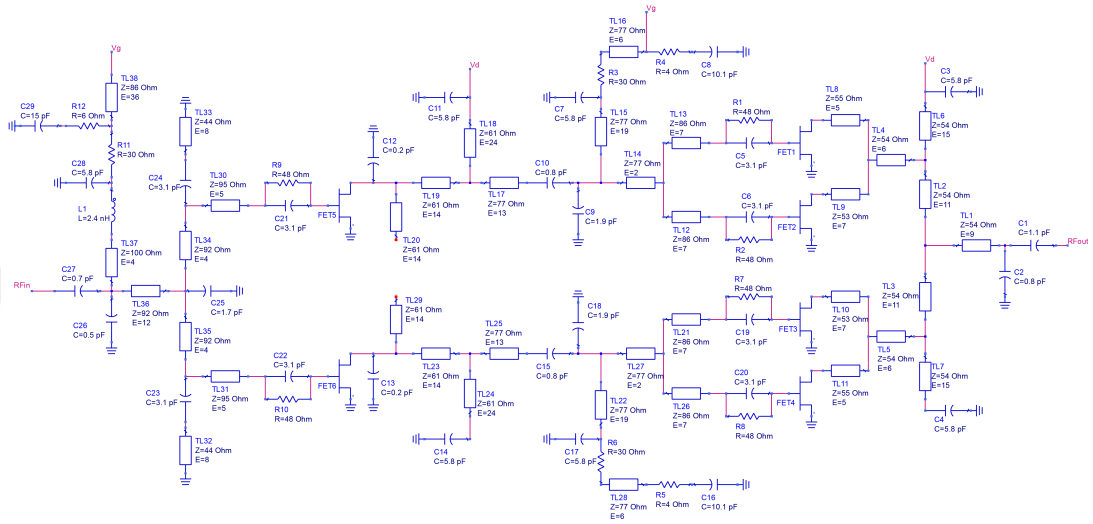


Figure 4.50: Schematic view of the finished design (given TL electrical lengths are @10GHz)

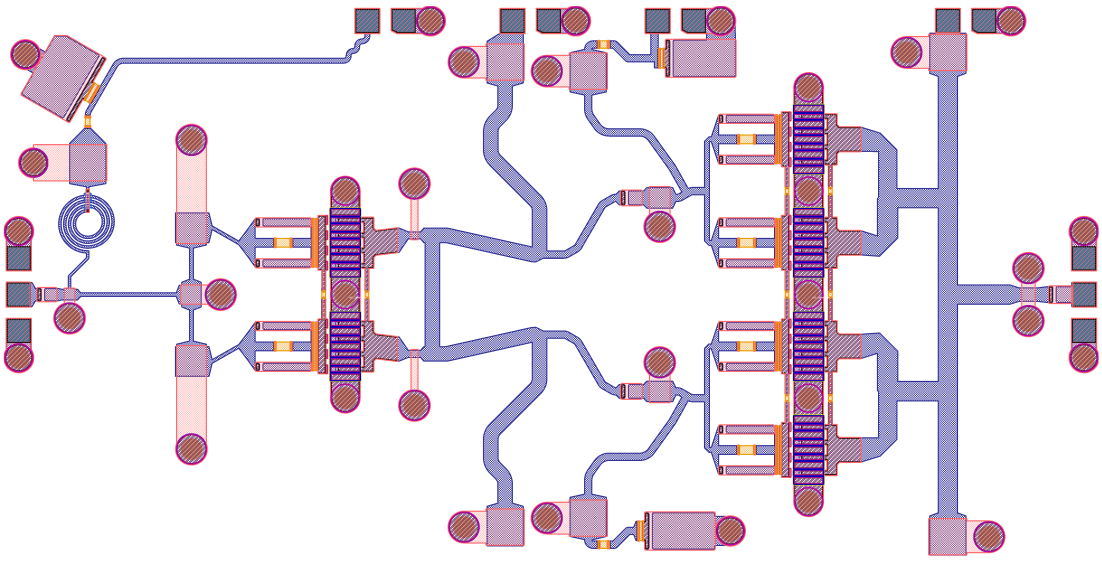


Figure 4.51: Layout view of the finished design

Chapter 5

Measurement Results and Analyses

5.1 Measurement Setup

On-wafer S-parameter measurements and large-signal power measurements are performed on fabricated PAs. SEM image of a fabricated MMIC is seen in Fig. 5.1. Overall MMIC size is 4.3 mm by 2.3 mm, with total die area of 9.9 mm^2

On-wafer small-signal measurements are taken under CW operation at room temperature in the RF measurement setup mentioned in the Chapter 3.

Large-signal characterizations of MMICs are performed in Vector Network Analyzer based load-pull system described in the Chapter 3. In the on-wafer load-pull setup, a source and load impedance of 50 Ω is presented to MMIC in all measurement frequencies. P_{in} available from 50 Ω source and P_{in} delivered to the 50 Ω load are measured via incident and reflected power waves. Current consumption of the amplifier is monitored for all input power levels. Corresponding output power, compression, large-signal gain and efficiency values are calculated accordingly.

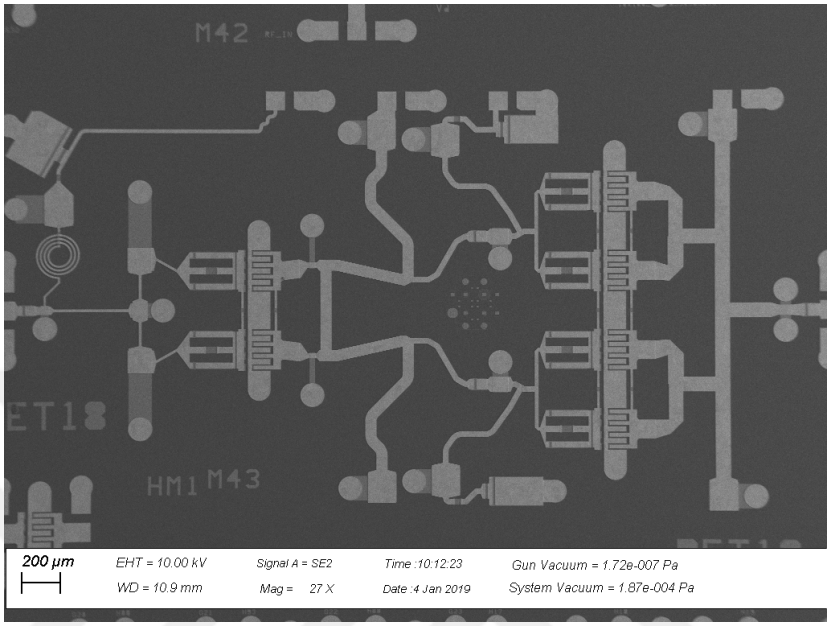


Figure 5.1: SEM view of a fabricated MMIC

5.2 Measurement Results

5.2.1 Small-Signal Measurements

Small-signal measurements of 25 fabricated MMICs are presented in Fig. 5.2.

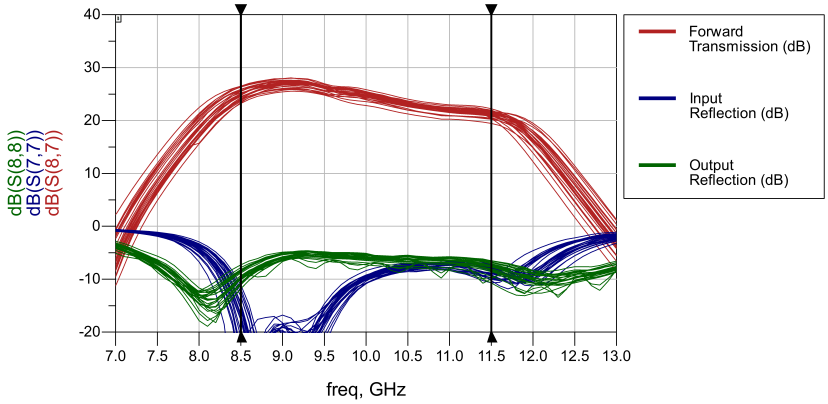


Figure 5.2: S-parameter measurement results of the fabricated 25 MMICs

Small-signal simulations of MMIC performed using the measured S-parameters of several transistors (biased at $100\,\mathrm{mA\,mm^{-1}}$ I_{Dq}) located across the same wafer,

are also shown in lighter tones on top of the MMIC measurement results in Fig. 5.3.

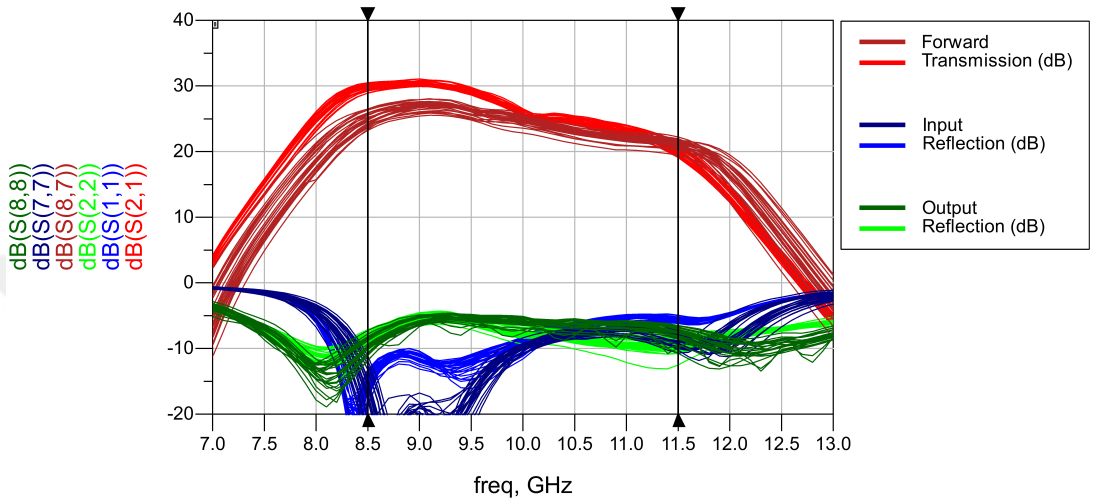


Figure 5.3: S-parameter measurements (darker tones) and simulation results (lighter tones) superposed

Measurement results and simulations are in fairly good agreement. The spread in simulation results gives an idea about the expected variation in MMIC measurements due to the transistor performance variations. The rest of the uncertainty stems from mainly three reasons: finite accuracy of EM substrate model and simulations; slight changes in the capacitance density of fabrication; and non-ideal operating conditions of transistors. On this third point, it's important to note that DC biases are fed through only one side of the MMIC during measurements, which causes slightly uneven gate voltages across the parallel transistors due to multiple resistors on the path. Adding to inherent differences in transistor threshold voltages, this may result in different quiescent drain currents, hence different transistor RF performances.

5.2.2 Power Sweep Measurements

On-wafer power measurements of MMICs are performed at room temperature under pulsed operation conditions, with a pulse width of 100 µs and 6% duty cycle. MMICs are biased at 28V V_{DS} with gate voltages set for 100 mA mm^{-1}

I_{Dq}. Measurements are repeated from 8.5 GHz to 11 GHz with 0.5 GHz steps.

Available input powers presented to MMICs are increased until they are driven to more than 6 dB compression. Power gain, output power and PAE results of these measurements are demonstrated in Fig 5.4.

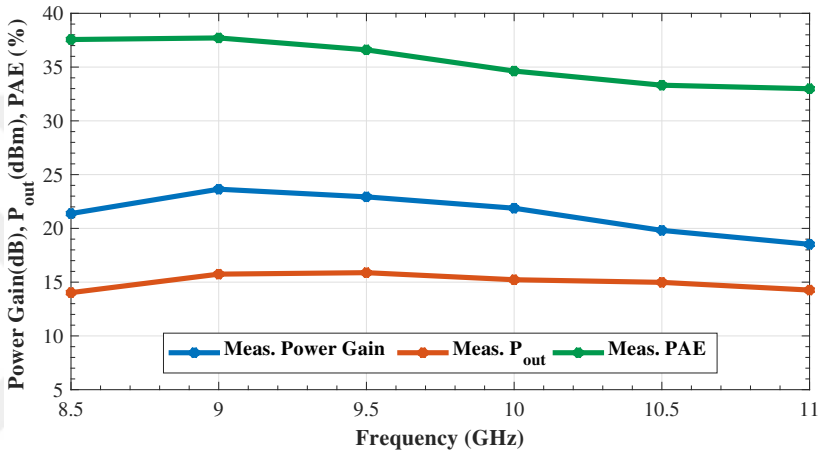


Figure 5.4: Output power, large-signal gain and PAE results of a fabricated MMIC at 8.5 GHz - 11 GHz band at 6 dB compression

The same results are also presented in tabulated form in Table 5.1.

	Frequency (GHz)					
	8.5	**9**	**9.5**	**10**	**10.5**	**11**
Pout (Watts)	14.0	15.7	15.9	15.2	15.0	14.3
Power Gain (dB)	21.4	23.6	22.9	21.9	19.8	18.5
PAE (%)	37.6	37.7	36.6	34.6	33.3	33.0

Table 5.1: Table of power measurement results of a fabricated MMIC at 8.5 GHz - 11 GHz band at 6 dB gain compression

Typical results of these power sweep measurements at 8.5 GHz, 10 GHz and 11 GHz where G_T and P_{out} are plotted versus available input power are presented in figures below.

Power sweeps corresponding to measurements of 5 different MMICs are drawn on top of each other to give a better idea about the order of performance variations in fabricated MMICs.

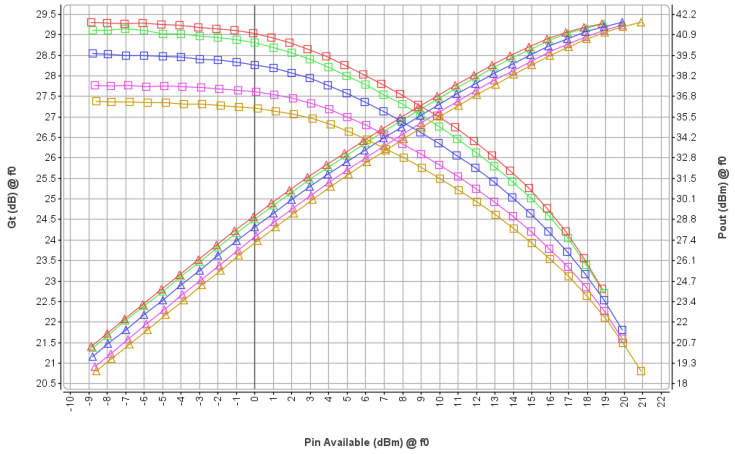


Figure 5.5: Power sweep measurements of MMICs at 8.5 GHz

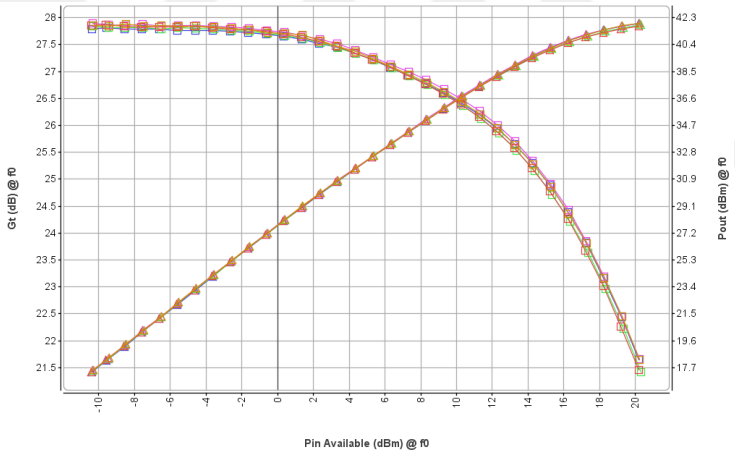


Figure 5.6: Power sweep measurements of MMICs at 10 GHz

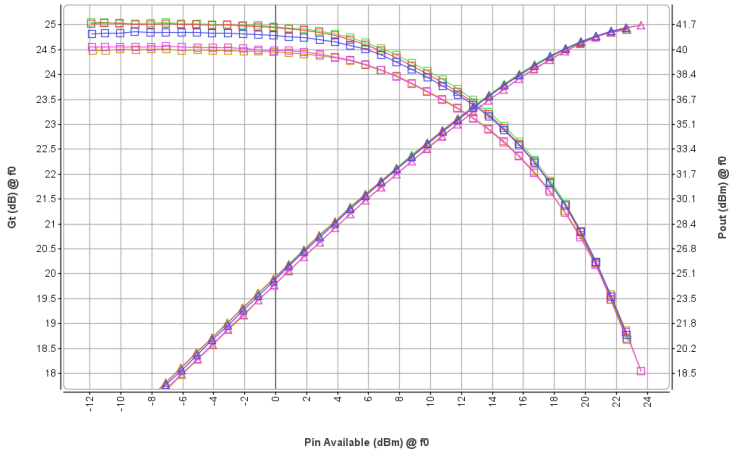


Figure 5.7: Power sweep measurements of MMICs at 11 GHz

Measurement results of a fabricated MMIC are compared with initial power simulations in Fig. 5.8.

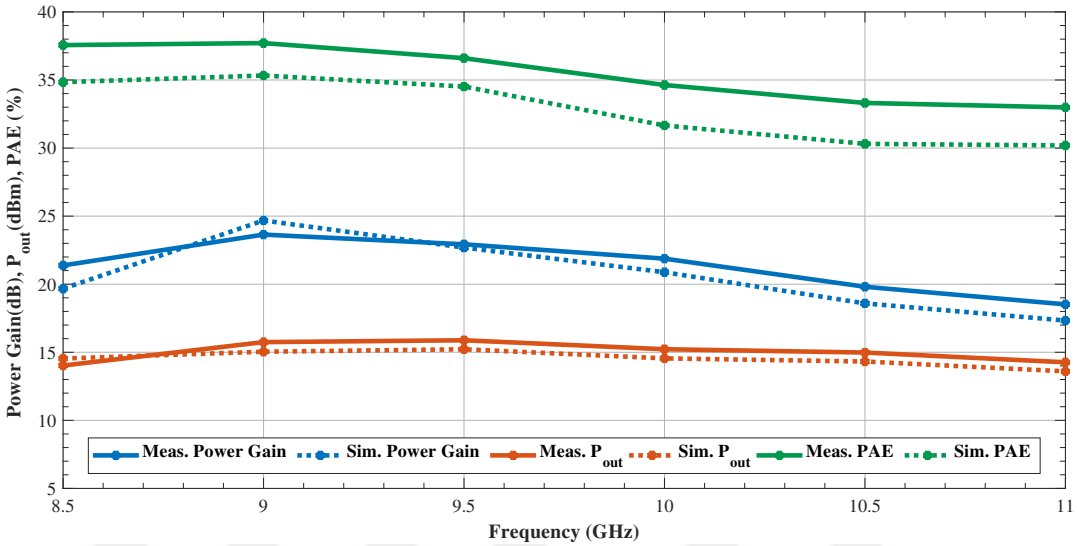


Figure 5.8: Comparison of large-signal measurements and power simulation results of a MMIC

Large-signal measurement results are close to the predictions based on the power simulation algorithm. It's important to note that this simulation assumes ideal even-mode operation of identically performing devices, which is not the case with amplifiers with multiple parallel transistors. On top of that, this approach does not account for the change in impedances seen by devices under large-signal drive. Also impedances at harmonics are not accounted for in this calculations, which will inevitably affect output power capacity of devices. Despite these uncertainties, implemented MMIC power simulation algorithm, based on transistor load-pull data and small-signal circuit analysis, is successful in predicting the trends in output power, gain and efficiency values, as well as providing a rough estimate for them.

5.3 Discussions and Future Work

Measured small-signal gains of MMICs are higher than 23 dB for most of the MMICs in the small-signal operation band of 8.5 GHz to 11.5 GHz, which corresponds to a 30% fractional bandwidth around 10 GHz. Achieved bandwidth is wider than the initial design specification of 8.5 GHz - 11 GHz band. Input and output return losses, despite variations among different MMICs are all better than 5 dB throughout the band.

Fabricated MMICs achieve more than 14 Watts of P_{6dB} in the measured frequency band of 8.5 GHz to 11 GHz, with power added efficiencies greater than 33% at all frequencies, which satisfy the design goals.

The chosen 2:4 topology with 1:2 power drive ratio provide some advantage over the 1:4 topology in power output since the driver stage is not compressed as much. However one major drawback of this configuration is the trade-off in efficiency, since efficiency in class AB operation increases with the compression. Driver stage operates in lower efficiency compression regime, as seen in the power simulation graph (Fig. 4.8). Modifying the design with a smaller driver stage gate periphery will drive the 1st stage transistors into compression, with the benefit of increased power efficiency.

In-band input and output reflections of some of the measured MMICs can go as high as to -5 dB, which is sub-optimal. While the output reflections are largely determined by the maximum output power matching according to load-pull impedances, it is possible to optimize input matching network for small-signal $|S_{11}|$. $|S_{11}|$ and $|S_{22}|$ performances can also be improved by external circuit modifications on PCB after bonding/packaging steps, with the help of discrete matching elements. Alternatively, using this MMIC in a balanced amplifier topology will enhance input and output return losses significantly.

As future work, current amplifier topology will be modified around the new optimized transistor results with around per$-$mode = symbol5 $\mathrm{W\,mm^{-1}}$ power densities in X-band. Also the driver stage gate periphery will be shrinked by

using smaller transistors in 1st stage to boost the small-signal gain and large-signal efficiency of the amplifier. Inter-stage matching circuit will be optimized with the goal of achieving better gain flatness throughout the band.

Although there is much room for improvement, these results are on par with some of the current commercial products in X-band from well known suppliers such as MACOM's MAAP-015036 (8.5-10.5 GHz) [13] and UMS's CHA8611-99F (8.5-11 GHz) [14] bare die power amplifiers in terms of gain and output power, while providing a broader small-signal operation band of 8.5 GHz to 11.5 GHz.

	Operation Band (GHz)	**Output Power (Watt)**	**Power Gain (dB)**	**Gain Comp. (dB)**	**Chip Dimensions (mm×mm)**
NANOTAM X-Band HPA	8.5 - 11	>14.0	18.5	6	4.3×2.3
MACOM MAAP-015036	8.5 - 10.5	>15	17	N/A	4.4×3.6
UMS CHA8611-99F	8.5 - 11	>16	15	9	4.4×2.6

Table 5.2: Performance comparison of measured MMIC results with commercial counterparts

Chapter 6

Conclusion

Microwave power amplifiers are essential components of many modern communication and radar systems. Gallium Nitride based High Electron Mobility Transistors are being utilized increasingly to satisfy growing demands for higher RF output power at microwave frequencies. Monolithic Microwave Integrated Circuit technology allows for compact implementation of power amplifier circuits with high performance, high reliability and low cost. Therefore, X-band MMIC power amplifiers are widely studied in academic, as well as commercial circles.

In this work, we have described design, fabrication and characterization procedure of an X-band microstrip MMIC power amplifier using the 0.25 µm GaN on SiC process of Bilkent University NANOTAM. Fabrication process is briefly demonstrated, transistor and MMIC characterization procedure is explained, study of transistor performance optimizations for X-band applications demonstrated and PA MMIC design process is described in detail. Finally, small-signal and power measurement results of the fabricated PA MMICs are presented and the results are compared to similar commercial products.

With die sizes smaller than 4.3 mm by 2.3 mm, fabricated MMICs operate at 8.5 - 11.5 GHz band with 24 dB small-signal gain. More than 13.5 W (41.3 dBm)

output power (P_{6dB}) and 31 - 38 % power-added efficiency are achieved throughout the 8.5 - 11 GHz band in pulsed mode on-wafer measurements. Although power output and gain results of bare die are comparable to some current commercial counterparts; design can be reiterated in future according to optimized transistor results and few aspects of design can be modified to further improve efficiency and small-signal performance.

Bibliography

[1] J. L. Walker, *Handbook of RF and Microwave Power Amplifiers*. Cambridge University Press, 2011.

[2] C. Costrini, M. Calori, A. Cetronio, C. Lanzieri, S. Lavanga, M. Peroni, E. Limiti, A. Serino, G. Ghione, and G. Melone, "A 20 Watt micro-strip X-band AlGaN/GaN HPA MMIC for advanced radar applications," in *2008 38th European Microwave Conference*, pp. 1433–1436, Oct 2008.

[3] D. Resca, A. Raffo, S. D. Falco, F. Scappaviva, V. Vadala, and G. Vannini, "X-band GaN power amplifier for future generation SAR systems," *IEEE Microw. Wirel. Compon. Lett.*, vol. 24, pp. 266–268, Apr. 2014.

[4] E. Ersoy, C. Meliani, S. Chevtchenko, P. Kurpas, M. Matalla, and W. Heinrich, "A high-gain X-band GaN-MMIC power amplifier," in *Proc. IEEE German Microw. Conf.*, (Ilmenau, Germany), pp. 1–4, Mar. 2012.

[5] R. Giofre, P. Colantonio, and F. Giannini, "X-band MMIC GaN power amplifier for SAR systems," *Microw. Opt. Technol. Lett.*, vol. 55, pp. 2611–2616, Nov. 2013.

[6] A. M. Couturier, N. Poitrenaud, V. Serru, R. Dionisio, J. J. Fontecavc, and M. Camiade, "50% high efficiency X-band GaN MMIC amplifier for space applications," in *2018 48th European Microwave Conference (EuMC)*, pp. 352–355, Sep. 2018.

[7] Y. S. Noh and I. B. Yom, "A 16 Watt X-band GaN high power amplifier MMIC for phased array applications," in *Proc. Int. Conf. Microw. Technol.*, (Beijing, China), pp. 979–981, June 2016.

[8] D. Shin, I. Yom, and D. Kim, "X-band GaN MMIC power amplifier for the SSPA of a SAR system," in *2017 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, pp. 93–95, Aug 2017.

[9] D. Sardin, T. Reveyrand, and Z. Popović, "X-band 10W MMIC high-gain power amplifier with up to 60% PAE," in *2014 44th European Microwave Conference*, pp. 1337–1340, Oct 2014.

[10] R. Quay, F. van Raay, J. Kuhn, R. Kiefer, P. Waltereit, M. Zorcic, M. Musser, W. Bronner, M. Dammann, M. Seelmann-Eggebert, M. Schlechtweg, M. Mikulla, O. Ambacher, J. Thorpe, K. Riepe, F. van Rijs, M. Saad, L. Harm, and T. Rodle, "Efficient AlGaN/GaN HEMT power amplifiers," in *2008 European Microwave Integrated Circuit Conference*, pp. 87–90, Oct 2008.

[11] J. Kuhn, F. van Raay, R. Quay, R. Kiefer, T. Maier, R. Stibal, M. Mikulla, M. Seelmann-Eggebert, W. Bronner, M. Schlechtweg, O. Ambacher, and M. Thumm, "Design of highly-efficient GaN X-band-power-amplifier MMICs," in *2009 IEEE MTT-S International Microwave Symposium Digest*, pp. 661–664, June 2009.

[12] O. Memioglu, A. Karakuzulu, A. Gundel, F. Kocer, and O. A. Civi, "Design and implementation of an encapsulated GaN X-band power amplifier family," in *2018 13th European Microwave Integrated Circuits Conference (EuMIC)*, pp. 89–92, Sep. 2018.

[13] MACOM, *Power Amplifier, 15 W 8.5 - 10.5 GHz*, 4 2013. Rev. V1.

[14] UMS, *18 W X-Band High Power Amplifier GaN Monolithic Microwave IC*, 2 2017.

[15] S. Oliver, "Optimize a power scheme for these transient times," September 2014. [Online; posted 30-September-2014].

[16] "GaN to grow at 9% CAGR to over 18% of RF device market by 2020," June 2014. [Online; posted June-2014].

[17] W. Bi, H. Kuo, P. Ku, and B. Shen, *Handbook of GaN Semiconductor Materials and Devices*. Series in Optics and Optoelectronics, CRC Press, 2017.

[18] F. Medjdoub, *Gallium Nitride (GaN): Physics, Devices, and Technology*. Devices, Circuits, and Systems, Taylor & Francis, 2015.

[19] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-based RF power devices and amplifiers," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 287–305, 2008.

[20] N. R. Council *et al.*, *Materials for High-Temperature Semiconductor Devices*. National Academies Press, 1995.

[21] S. Keller, S. Heikman, L. Shen, I. Smorchkova, S. DenBaars, and U. Mishra, "GaN–GaN junctions with ultrathin AlN interlayers: Expanding heterojunction design," *Applied Physics Letters*, vol. 80, no. 23, pp. 4387–4389, 2002.

[22] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, J. F. Sevic, and N. O. Sokal, "Power amplifiers and transmitters for RF and microwave," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 814–826, 2002.

[23] S. Marsh, *Practical MMIC Design*. Artech House Inc, 2006.

[24] G. Crupi and D. Schreurs, *Microwave De-Embedding: From Theory to Applications*. Academic Press, 2013.

[25] S. C. Cripps, *Advanced Techniques in RF Power Amplifier Design*. Artech House, 2002.

[26] "Microwave Office Measurement Catalog: Maximum Available Gain: GMax."

[27] R. Gilmore and L. Besser, *Practical RF Circuit Design for Modern Wireless Systems: Active Circuits and Systems*, vol. 2. Artech House, 2003.

[28] J. Li, S. Cai, G. Pan, Y. Chen, C. Wen, and K. Wang, "High breakdown voltage GaN HFET with field plate," *Electronics Letters*, vol. 37, no. 3, pp. 196–197, 2001.

[29] N.-Q. Zhang, S. Keller, G. Parish, S. Heikman, S. DenBaars, and U. Mishra, "High breakdown GaN HEMT with overlapping gate structure," *IEEE Electron Device Letters*, vol. 21, no. 9, pp. 421–423, 2000.

[30] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "Suppression of dynamic on-resistance increase and gate charge measurements in high-voltage GaN-HEMTs with optimized field-plate structure," *IEEE Transactions on Electron Devices*, vol. 54, no. 8, pp. 1825–1830, 2007.

[31] A. Wakejima, K. Ota, T. Nakayama, Y. Ando, Y. Okamoto, H. Miyamoto, S. Kamiya, and A. Suzuki, "Observation of cross-sectional electric field for GaN-based field effect transistor with field-modulating plate," *Applied Physics Letters*, vol. 90, no. 21, p. 213504, 2007.

[32] S. Sque, "High-voltage GaN-HEMT devices, simulation and modelling," *ESSDERC 2013 (NXP Semiconductors)*, 2013.

[33] A. Toprak, S. Osmanoğlu, M. Öztürk, D. Yılmaz, Ö. Cengiz, Ö. Şen, B. Bütün, Ş. Özcan, and E. Özbay, "Effect of gate structures on the DC and RF performance of AlGaN/GaN HEMTs," *Semiconductor Science and Technology*, vol. 33, no. 12, p. 125017, 2018.

[34] T. Gasseling, E. Gatard, C. Charbonniaud, and A. Xiong, "Assets of source pull for NVNA based load pull measurements," in *79th ARFTG Microwave Measurement Conference*, pp. 1–5, June 2012.

[35] I. Bahl, *Fundamentals of RF and Microwave Transistor Amplifiers*. John Wiley & Sons, 2009.

[36] R. G. Freitag, "A unified analysis of MMIC power amplifier stability," in *Microwave Symposium Digest, 1992., IEEE MTT-S International*, pp. 297–300, IEEE, 1992.

[37] M. Jankowski, E. Limiti, and P. E. Longhi, "Freitag method application to PA stability test," in *2008 Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits*, pp. 149–152, IEEE, Nov. 2008.