DOKUZ EYLÜL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

NOISE IMMUNE FREQUENCY CONTROL LOOP DESIGN FOR RESONANT INVERTERS

by
Salih ÜNSAL

October, 2019
İZMİR

NOISE IMMUNE FREQUENCY CONTROL LOOP DESIGN FOR RESONANT INVERTERS

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M.Sc THESIS EXAMINATION RESULT FORM

We have read the thesis entitled **"NOISE IMMUNE FREQUENCY CONTROL LOOP DESIGN FOR RESONANT INVERTERS"** completed by **SALİH ÜNSAL** under supervision of **PROF. DR. HALDUN KARACA** and we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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NOISE IMMUNE FREQUENCY CONTROL LOOP DESIGN FOR RESONANT INVERTERS

ABSTRACT

Resonant inverters are needed to be driven at load resonant frequency for maximum efficiency and inverter reliability. Load current oscillates with maximum amplitude at resonant frequency in a series resonant inverter. Load acts as a resistive circuit at this frequency. This is important for reliability especially working at high power regime. Because zero crossings of current and voltage waveforms happen at the same instant when circuit is driven at resonant frequency and power semiconductor switches commutates reliably.

Series resonant inverters, phased-locked loops (PLL) for the frequency control purposes of resonant inverters and especially phase detectors are studied in this thesis. Driven of resonant inverters at load resonant frequency by using PLL is told and in addition to classical PLL in a frequency control loop, a novel noise immune phase detector is designed, implemented and tested.

Although the PLL Chip utilized in this study (CD4046) includes a phase detector with rising edge triggered, it is found that this phase detector is not suitable for the purpose due its sensitivity to noise. It may sense additive noise as rising edge erroneously and change the output frequency. In this thesis, a new phase detector apart from the one inside the 4046 chip is tested in the frequency control loop and found more immune to electrical glitches through the experiments. The inverter malfunction problem more often than not come across during the experiments which use phase detector of PLL Chip is disappeared when the new phase detector is used. As a result of work fulfilled, the inverter got become more immune to noise and malfunction problem was disappeared by using the phase detector designed in this thesis.

Keywords: PLL, resonance, phase-locked-loop, phase detector, resonant inverter

REZONANS EVİRGEÇLERİ İÇİN GÜRÜLTÜYE BAĞIŞIKLI FREKANS KONTROL DÖNGÜSÜ TASARIMI

ÖZ

Rezonans evirgeçlerinin maksimum verimle ve güvenli çalışması için yük rezonans frekansında sürülmeleri gerekir. Seri evirgeçte rezonans frekansı yük akımının maksimum genlikte salınım yaptığı frekanstır. Bu frekansta yük indüktans ve kapasitans reaktansları birbirini yok eder ve sadece rezistif bir yük gibi davranır. Bu özellikle yüksek güçlerde çalışırken tranzistörlerin güvenli anahtarlama yapması açısından da önemlidir. Çünkü devre rezonans frekansında sürüldüğünde akım ve gerilim sıfır geçişleri aynı anda olur ve bu anlarda güç yarıiletkeninin karşı karşıya kaldığı elektriksel stres az olur.

Bu tezde rezonans devreleri, frekans kontrolü amaçlı faz kilitlemeli döngüler (PLL) ve özellikle faz dedektörleri incelenmektedir. Rezonans devrelerinin PLL kullanılarak yük rezonans frekansında sürülmesi incelenmekte, frekans kontrol döngüsünde kullanılan klasik PLL'e ek olarak yeni gürültüye dayanıklı faz dedektörü devresi tasarımı, uygulaması ve testi üzerine çalışılmaktadır.

CD4046-PLL entegresinin içindeki faz dedektörü yükselen kenar tetiklemelidir, ancak gürültüye karşı çok duyarlıdır (Tip2 faz dedektörü). Gürültüyü yükselen kenar olarak algılayıp çıkış frekansını değiştirebilir. Frekans yanlış yöne doğru kayar ve faz farkı gittikçe artar. Bu tezde, yanlış çalışma sorununu engellemek için yeni bir faz dedektörü tasarlanmış, test edilmiş, gürültü ve hatalı sinyallere karşı daha dayanıklı olduğu gözlemlenmiştir. Yeni tasarlanan faz dedektörünün kullanıldığı deneylerde oluşmayan hatalı çalışma sorunu, PLL entegresi içindeki faz dedektörü kullanılarak yapılan deneylerde oldukça sık görülmüştür. Devre gürültüye ve faz dedektörü girişindeki hatalı sinyallere karşı daha dayanıklı hale gelmiş ve problem giderilmiştir.

Anahtar kelimeler: PLL, rezonans, faz kilitlemeli döngü, faz dedektörü, rezonans evirgeci

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CHAPTER ONE
INTRODUCTION

Resonant inverters are used in many areas like induction heating. Induction heaters are high power devices, so efficiency and safety are very important. These devices are driven at resonant frequency to increase efficiency and safety. When it is driven at resonant frequency, voltage and current oscillate at the same phase and this provides the highest current and arc does not occur. Because voltage passes through zero at the same time (Sayed, Abo-Elyousr, Abdelbar & El-Zohri, 2018).

Phase-Locked Loop (PLL) can be used for driving a resonant circuit at resonant frequency. PLL has phase detector (PD). It detects phase differences between voltage and current by using PD and converts this data to a DC voltage. It changes the frequency of voltage-controlled oscillator (VCO) by using this voltage. In the ideal case, this system works perfectly. However, there is a malfunction problem in practical usage because of structure of PLL. PD in the PLL is rising edge triggered. This PD can detect a glitch which can occur because of electromagnetic noise and it causes to change of VCO frequency in the opposite direction (Banerjee, 2006).

1.1 Resonant Inverters

Resonant inverts are used to provide AC supply to load from a DC source. This inverter can be used as voltage source inverter or current source inverter (Chéron,1992). It generates and delivers square wave to circuit. Transistor are switched by an alternating voltage. Q1-Q3 and Q2-Q4 turn on and off simultaneously at switching frequency f_s, and f_s should be equal to resonance frequency f_r. Resonant inverter has L-C load that oscillates. It can be switched at zero voltage or zero current time. When fs is equal to fr, zero crossings of current and voltage waveforms happen at the same instant and switching transistors at this time provides minimum electrical stress.

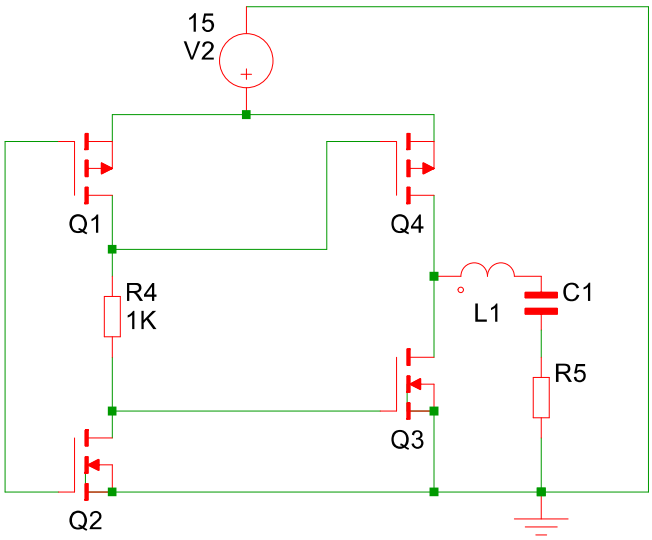

Figure 1.1 A series resonant inverter circuit diagram prototyped and used in experiment. L1 and C1 represents resonant load, and R5 represents load resistance

1.2 Resonant Inverter Application Areas

Induction heating is most known application of resonant inverters. Induction heating is used to heat conducting materials (mostly metals) by generating eddy currents in the base on electromagnetic induction. A conductor material is placed in a heater coil. High frequency alternating current is applied to the coil. This current creates high frequency alternating magnetic field. Rapidly changing magnetic field creates eddy current in the conductive material placed in the coil. Eddy currents flow through the resistance of conducting material and causes heating of material. Induction heating is used in many industrial areas industry and home applications some of those are furnace, welding, cooking, brazing, sealing, plastic injection molding machine. Induction heating provides heating fast and safety (Rapoport& Pleshivtseva, 2006).

Resonant inverters also used in ultrasonic generator, sonar transmitters, fluorescent lighting. Operating at appropriate frequency to the acoustic load is important for ultrasonic and sonar systems. Resonant inverters are used in these systems to match the frequency with load. Also using resonant inverters in fluorescent lighting is provides more efficient systems and reduces losses.

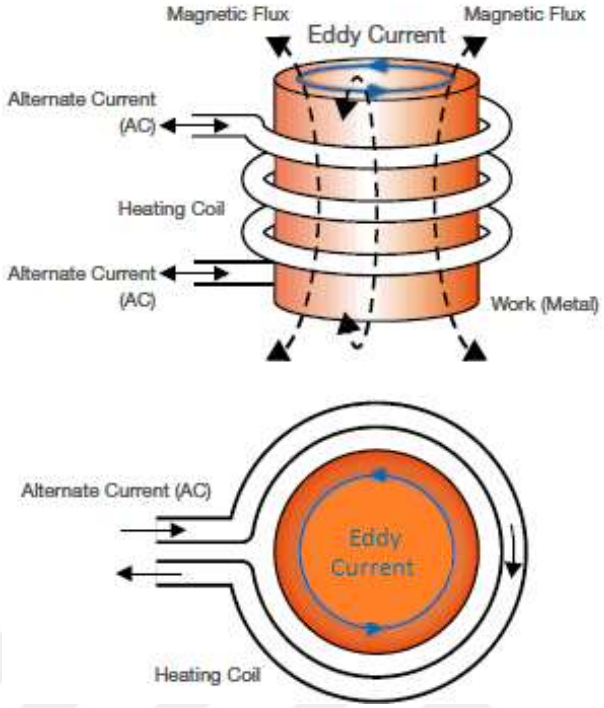

Figure 1.2 Induction heating process working schmes (Avio, n.d.)

1.3 Phase-Locked Loop

PLL circuit provides a system to track another one. PLL circuit generates a synchronous output signal which has same frequency and phase as input signal. PLL idea emerged in early 20th century. It used at analog television receiver in 1930s. First PLL integrated circuit was produced in 1969.

PLL consists of three basic parts; phase detector, loop filter and voltage-controlled oscillator. PLL structure diagram is shown in Figure 1.2. Two inputs signal are connected to phase detector. One of these signals is VCO output signal and the other one is reference signal. Phase detector compares these signal states as logic "1" or "0" and generates square wave pulses in proportion with phase or frequency difference between them by this way. There are kinds of phase detector. Some can detect only phase difference, and some can detect both phase and frequency differences.

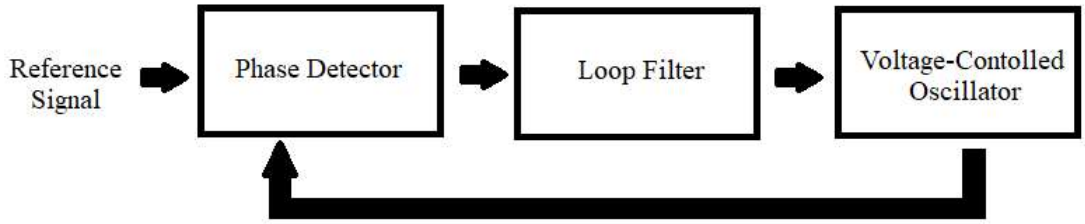

Figure 1.3 PLL basic structure

Second basic part of PLL is loop filter. Loop filter is a low-pass filter and it contains a resistor and a capacitor. The square wave signal generated by phase detector reaches to loop filter. A DC level voltage is generated in loop filter by using appropriate capacitor and resistor values this DC signal drives the voltage-controlled oscillator.

Voltage-controlled oscillator is the last part of PLL. It generates a square wave voltage whose frequency changes between its maximum and minimum limits. These limits are defined by connected capacitors and resistors. It is sensitive to voltage and its operating frequency is defined by a DC voltage. This voltage is generated by the loop filter.

CHAPTER TWO
LOAD RESONANT INVERTERS

2.1 Resonant Frequency

Resonance means oscillating of a system with maximum amplitude at a defined frequency. RLC circuits contain resistor (R), inductor (L), capacitor (C) and shown in . Resistor is an ohmic device, its value (reactance) is constant and independent of frequency. Capacitor and inductor are storage elements. Capacitor stores voltage and inductance stores current. Their reactances have a phase difference of 180° and dependent on frequency.

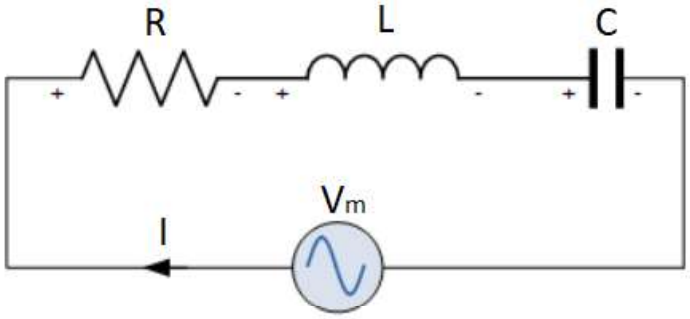

Figure 2.1 Series RLC circuit

Capacitive reactance is;

$$Xc = -\frac{1}{2\pi fC} = -\frac{1}{\omega C} \tag{2.1}$$

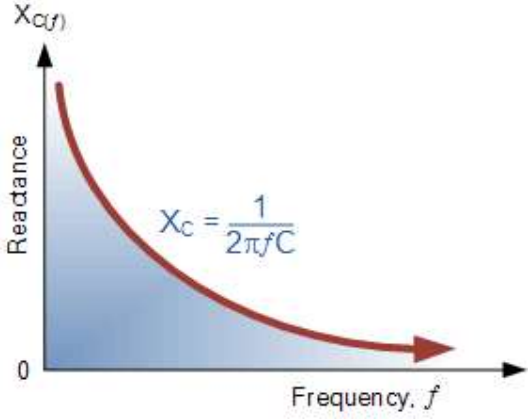

Figure 2.2 Changing of capacitive reactance against frequency (Electroics-tutorials, n.d.)

Inductive reactance is;

$$Xl = 2\pi fL = \omega L \tag{2.2}$$

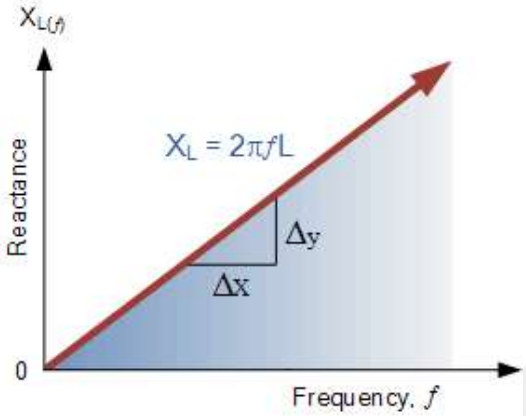

Figure 2.3 Changing of inductive reactance against frequency (Electroics-tutorials, n.d.)

When capacitive reactance is equal to inductive reactance, they neutralize eachother and this reduces the total reactance. By this way, current oscillates with maximum current. Equation (2.1) and (2.2) is used to define resonance frequency.

$$Xc = \mathrm{Xl} \tag{2.3}$$

$$\frac{1}{2\pi fC} = 2\pi fL \tag{2.4}$$

$$f = \frac{1}{2\pi\sqrt{\mathrm{LC}}} \tag{2.5}$$

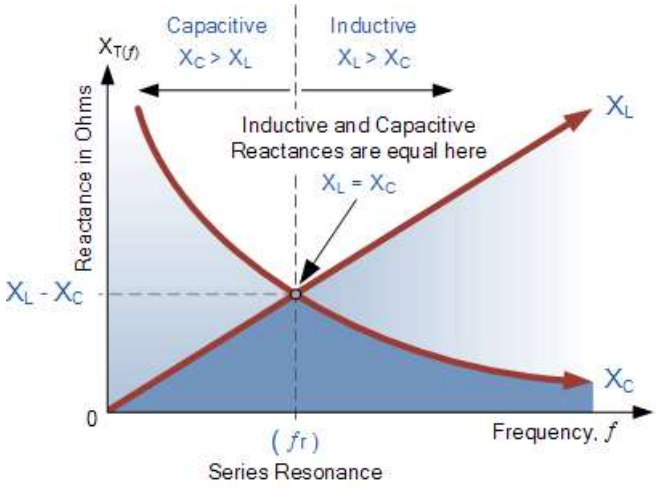

Figure 2.4 Representation of resonance frequency on graph (Electronics-tutorials, n.d.)

Xc: Capacitive reactance

Xl: Inductive reactance

C: Capacitance

L: Inductance

f: Frequency

2.2 Load Tracking Loops of Resonant inverters

Resonant inverters should be driven at the resonant frequency. This frequency can change because of internal and external. Every change in resonance frequency should be detected and driver frequency should be set at this frequency. There is a relation between driving frequency and phase difference. When driving frequency is equal to resonance frequency, phase difference disappears, and current and voltage signals become in the same phase.

System works based on phase difference detection. Current and voltage signals are observed continuously by the system to detect phase difference. PFD generates square wave pulses in proportion with phase difference. These pulses are converted to DC voltage after low-pass filter. This DC voltage drives VCO. When driving frequency is equal to resonance frequency, phase detector stops to generate pulses, and VCO sets the frequency. This system can sense every change in resonant load and sets VCO frequency to resonance frequency. Basic load tracking loop structure of resonant inverter are shown in Figure 2.1.

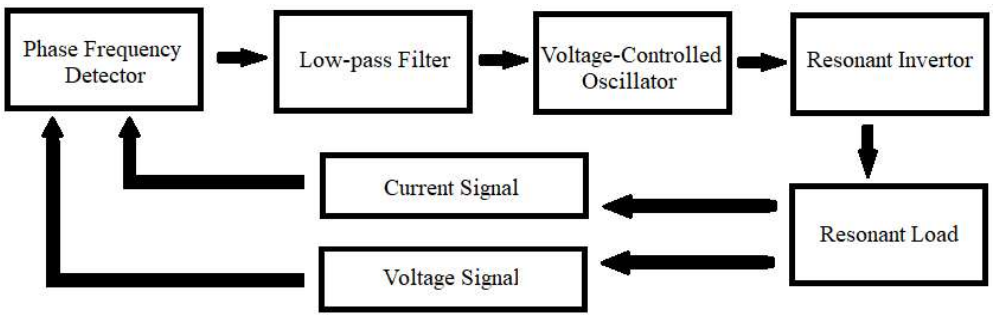

Figure 2.5 Structure of load tracking loop of resonant inverter

CHAPTER THREE
PHASE DETECTORS IN RESONANCE TRACKING LOOP

3.1 Multiplier Type Phase detectors

Multiplier type phase detectors works like a XOR gate. It compares states of two input signal and generates an output signal dependent on inputs. If inputs have the same state (high or low), output is low and if inputs have different states output is low. This operation can give an information about phase difference, but it does not show which signal is leading and which is lagging. Its typical output and output characteristic is shown in Figure 3.1 and Figure 3.2.

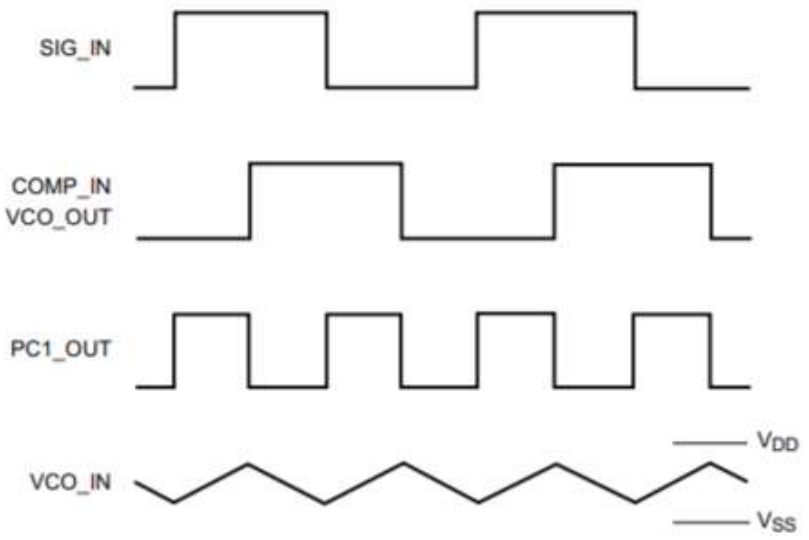

Figure 3.1 Typical output of multiplier type phase detector (Nexperia, 2016)

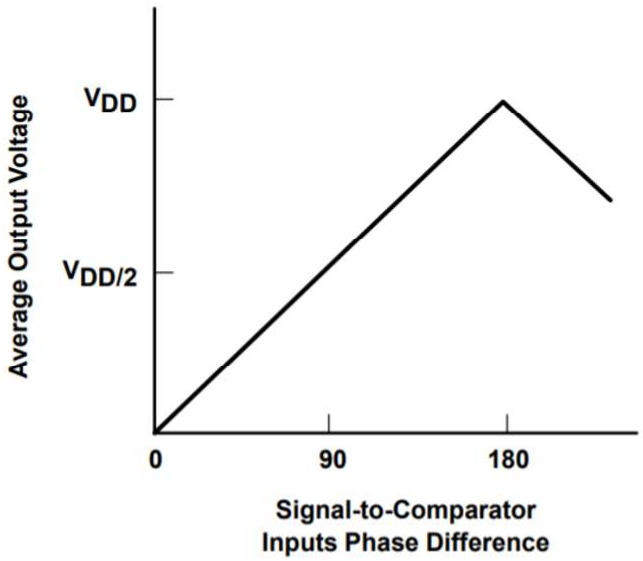

Figure 3.2 Multiplier type phase detector characteristic (Nexperia, 2016)

3.2 PFD Phase Frequency Detectors

Phase frequency detector (PFD) has more complex structure than multiplier type phase detector. Output of PFD depends not only on phase differences between inputs, also depends on frequency difference. PFD is positive edge triggered. As seen on Figure 3.3, PFD contains 2 D-type flip-flops control gating and 3-state output stage.

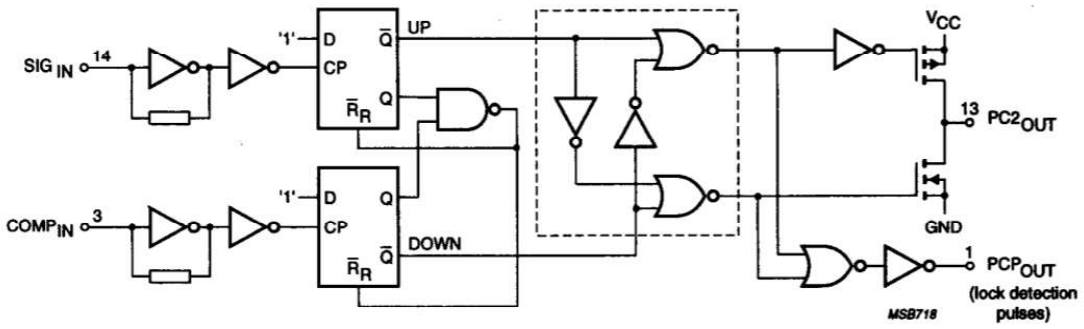

Figure 3.3 Circuit diagram of PFD (Philips, 1995)

If rising edge of SIGN IN comes earlier (positive phase difference), PFD output goes to high from high impedance during phase difference and then turn into high impedance. If rising edge of COMP IN comes earlier (negative phase difference), PFD output goes to low from high impedance during phase difference and then turn

into high impedance again. Low-pass filter is applied to PFD output and phase difference information is converted to a DC level voltage. This operation is shown in Figure 3.4.

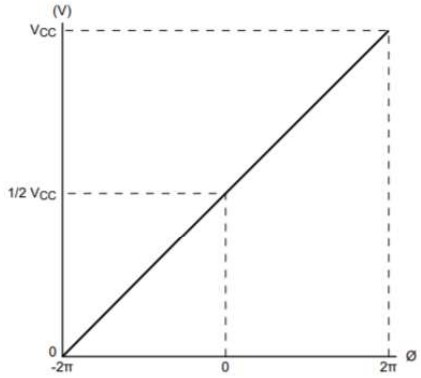

Figure 3.4 PFD characteristic (Nexperia, 2019)

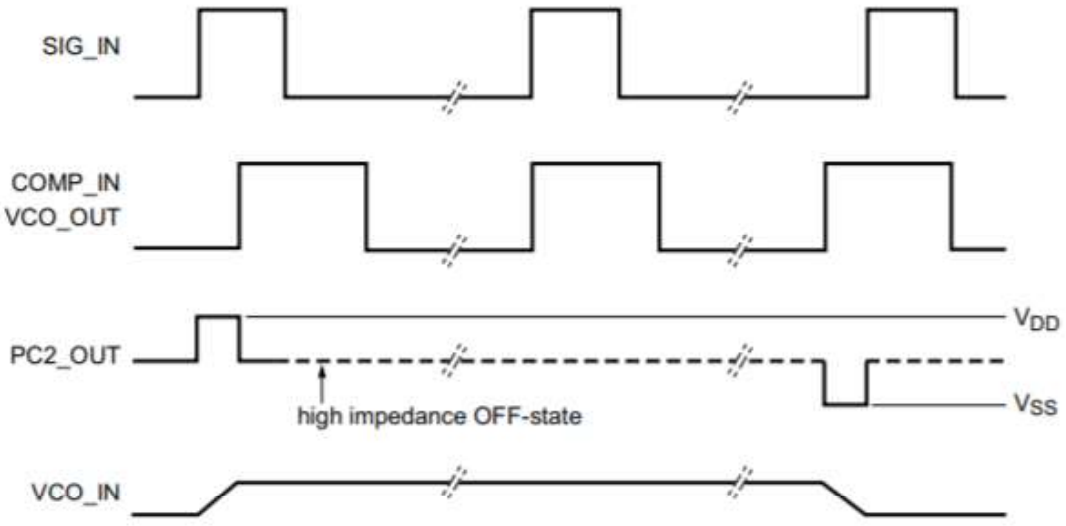

Figure 3.5 Typical output of PFD (Nexperia, 2016)

PFD behavior is shown in Figure 3.6 in detail. This circuit operation is like an UP-DOWN counter. SIG IN makes it up count and COMP IN makes it down count. Also, this operation is shown in Figure 3.7 basically.

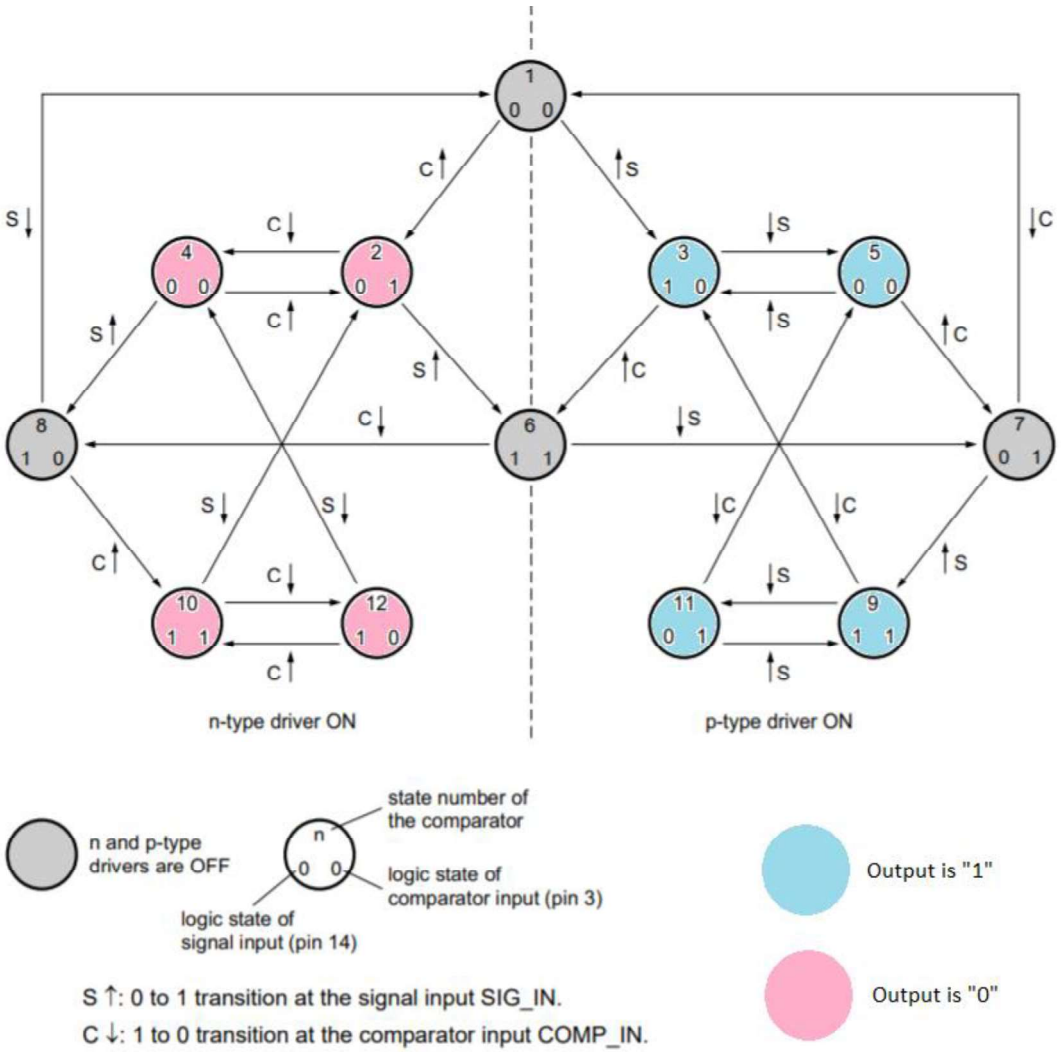

Figure 3.6 Full operation diagram of PFD (Nexperia, 2016)

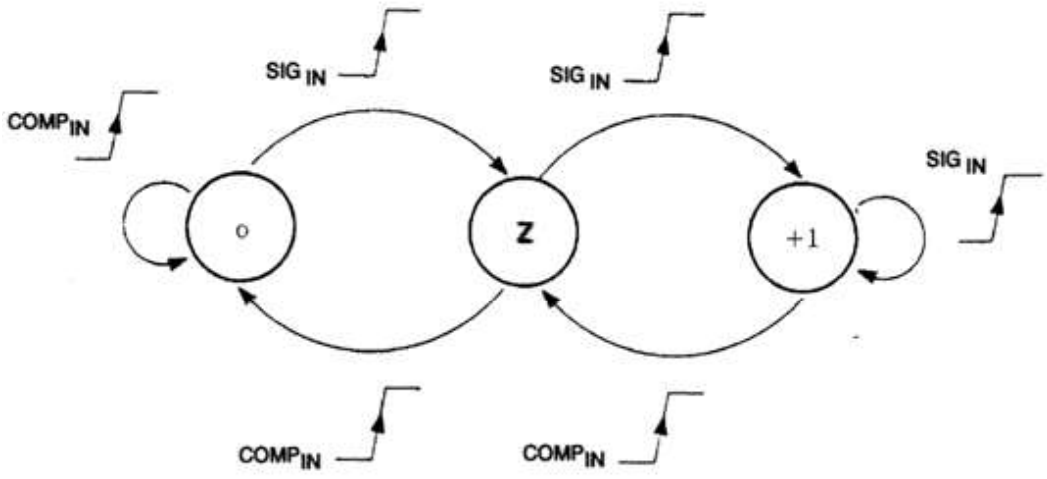

Figure 3.7 Basic operation diagram of PFD (Best, 2003)

Also, PFD detects frequency differences between inputs. This operation is similar with detecting phase difference. When inputs have different frequencies, PFD output goes HIGH or LOW from high impedance. If SIG IN has higher frequency, this means rising edge of COMP IN comes later and output goes to high. If COMP IN has higher frequency, this means rising edge of SIG IN comes later and output goes to low. This operation is shown in Figure 3.8.

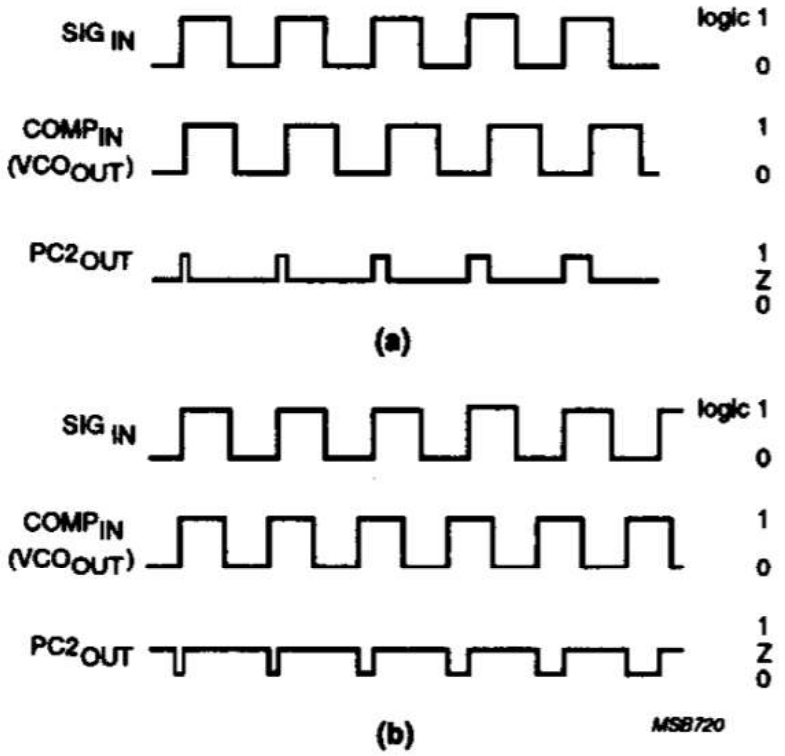

Figure 3.8 Output of PFD according to phase difference. a) SIG IN leads to COMP IN. b) SIG IN lags to COMP IN (Philips, 1995)

3.3 Malfunction Problem with the PFD

When zero phase difference occur between two inputs of PFD, zero error output would occur at output. However, anomalous behavior is observed with PFD under two conditions. it frequently fails to lock to frequency when first stat up, and glitches can cause to break the lock and force the frequency to go maximum or minimum. These glitches can be because of interference.

Output-phase error characteristic of PFD is double-valued, and it is shown in Figure 3.9. In that figure, solid lines are true characteristic and dashed lines are wrong characteristic. This double-values property causes the erratic behavior when PFD is used in a tuned-circuit frequency discriminator. When the PFD starts up, initial phase between two inputs those are voltage and current signals are random. So, PFD selects operation point random and there are two options; upper branches and lower branches of output voltage vs. phase difference characteristic (Karaca, 2001). This selection happens when the first rising edge of inputs signals occurs.

Assume that phase difference θ(0) between voltage and current signals is 90° as initial condition. If PFD choses upper branch of characteristic, it goes to θ=0° and frequency lock occurs correctly. If PFD choses lower branch of characteristic, its acts like phase error is -270° and it goes to θ=2π. However, phase difference of voltage and current signals can not change more than 180° from initial condition. Because if phase difference is 180°, LF output is logic "1" and it makes VCO to operate at maximum frequency. If phase difference between inputs is -180°, LF output is logic "0" and it makes VCO to operate at minimum frequency. Therefore, PFD tries to reach 2π, but it can never reach. So, it can only reach one of VCO limits (maximum or minimum).

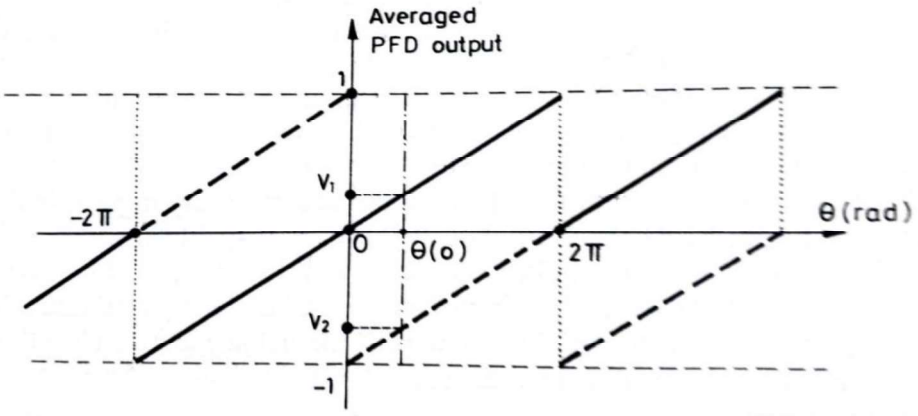

Figure 3.9 The double-valued PFD characteristics, straight line is true, dashed line is false (Karaca, 2001)

Another erratic behavior occurs with glitch that is created by interference or switching speed. PFD in HC4046 integrated circuit is very sensitive to noise because

there is D-type flip-flops at its output, and they require signal-to-noise ratio is higher than 30 dB for operating correctly. If Signal-to-noise ratio is lower, this causes similar erratic behavior.

> Slow rising or falling edges of the SIG IN or COMP IN signals may have small transient around the input switching level of the self-biasing input amplifiers. To avoid 2π phase errors due to these transients, it is recommended to edges of the comparator input signals have a slop of at least 0.5/μs and are monotonically rising or falling. The point requires particular attention, if small AC signals are capacitively coupled via SIG IN to self-biasing input amplifiers. (Philips, 1995, p.21)

These glitches occurred by interference or transient trigger flip-flops with wrong rising edges. PFD cannot distinguish these wrong triggers from real one. Therefore, there is a jump occurs in phase difference. OFD output gets reversed and this makes VCO to change frequency in wrong direction. In Figure 3.10 and Figure 3.11, a wrong rising edge on COMP IN triggers PFD at wrong time. This causes PFD to produce completely wrong output signal. These erratic PFD output signal causes to VCO change frequency in wrong direction. Finally, Frequency reaches maximum or minimum limit of VCO. Also, this phase jump can cause PFD to chose wrong branch in characteristic and 2π phase error occurs again. As a result, VCO reaches to maximum or minimum limit because of glitches.

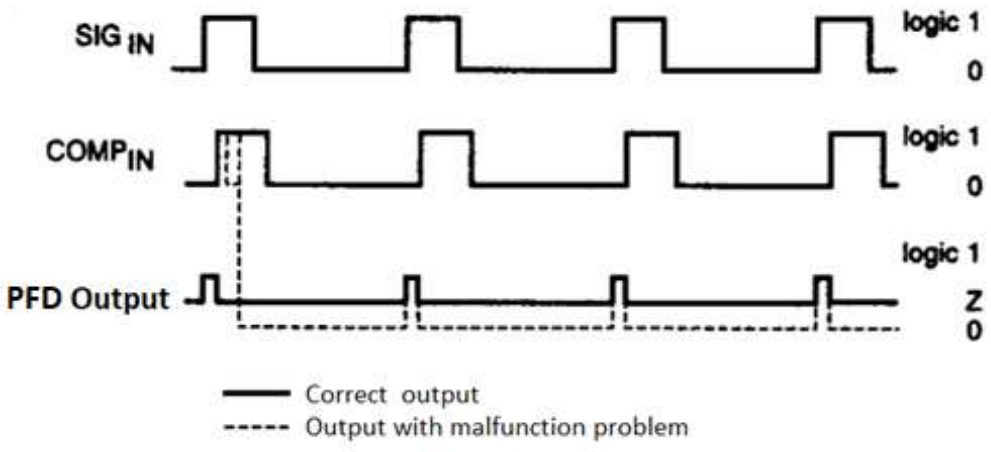

Figure 3.10 effect of negative glitch (Philips, 1995)

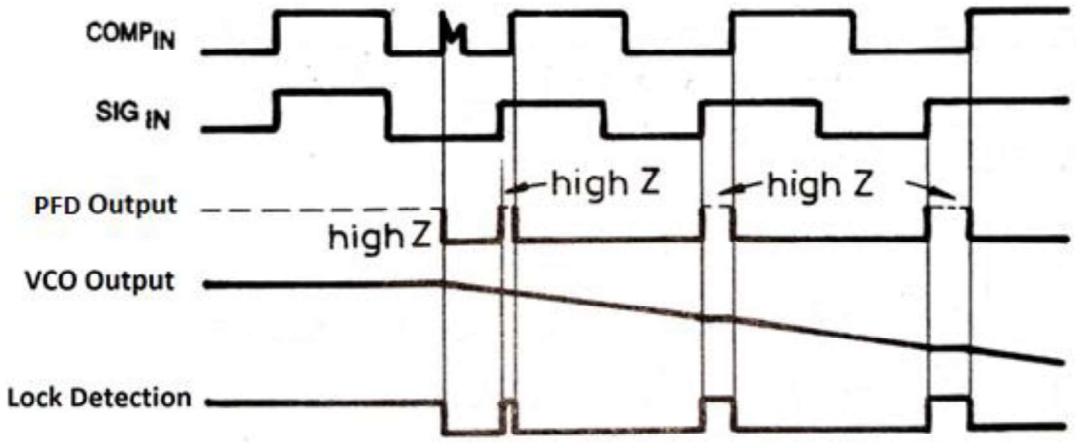

Figure 3.11 Malfunction occurrence triggered by a glitch on comp in waveform (Karaca, 2001)

When two inputs of VCO have different frequencies, phase difference increases or decreases in time that shown in Figure 3.12. After several cycle, phase difference gets higher than 2π or gets lower than -2π. This is called as "cycle slip". Due to PFD characteristic is periodic with 2π, frequency gets a chance to lock every 2π change in phase difference. However, when it is used to tune frequency of load resonant inverters, two inputs of PFD those are voltage and current signals always have the same frequency. So, cycle slip never occurs. There is a additional circuit is needed to provide PFD to work correctly.

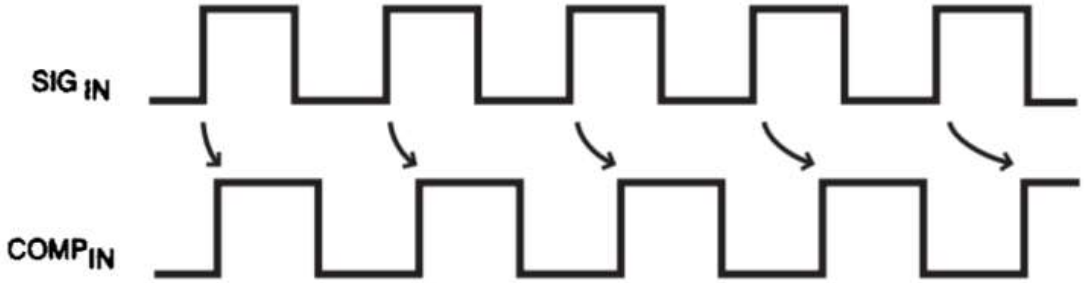

Figure 3.12 Representation of cycle slip (Perrott, 2005)

CHAPTER FOUR
A NEW PFD CIRCUIT WITHOUT MALFUNCTION

Old PFD circuit (Figure 3.3) resets flip-flops when both outputs of flip-flops are equal to logic "1". However, when the glitch occurs at one of inputs, the flip-flop output that connected to this input, gets "1" at the wrong time. This causes flip-flops to set and reset at wrong time. LF is applied to this incorrect output of PFD so, VCO is driven by incorrect DC level voltage. Finally, frequency of VCO changes in wrong direction.

After malfunction problem was observed, it is decided to design a novel PFD. Novel PFD should have a spare resetting circuit to avoid erratic behavior. NOR gates U5 and U7 in Figure 4.1 is placed and both resetting circuits (existing and spare) are connected to it as inputs. Both circuits can reset flip-flops by this way. When both inputs of PFD get HIGH, spare resetting circuit (This circuit contains inverters U2 and U13, and NOR gate U3) resets flip-flops. This inputs also make flip-flops output "1" and this already resets flip-flops. In the normal operation, two resetting circuits makes the same thing. However, when a glitch occurs and flip-flop outputs get wrong, this situation can never be fixed because of memory of flip-flop. In this situation, spare resetting circuit provides to reset the flip-flops and circuit turn into normal operation at next cycle. New designed circuit is shown in Figure 4.1.

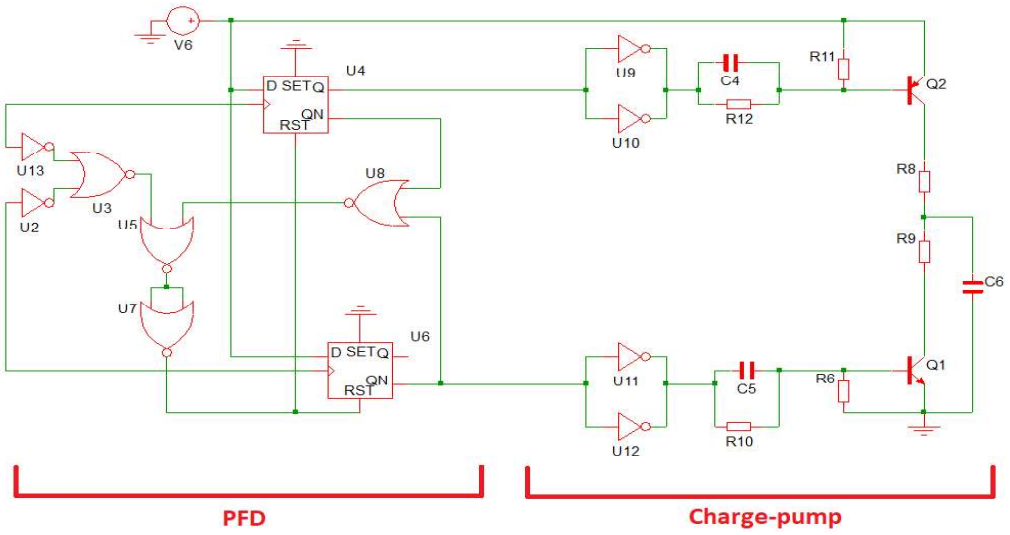

Figure 4.1 Schematic of new designed phase frequency detector with transistorized charge-pump

Full circuit diagram is shown in figure 4.2. In this diagram, PFD and charge-pump are placed at left side, CD4046 integrated circuit is at middle and it is only used as VCO. Load resonant inverter is placed at right top, and comparator circuit that is used to generate square wave signal with current signal is at right bottom. Current signal obtained by observing voltage wave form over R5 resistor.

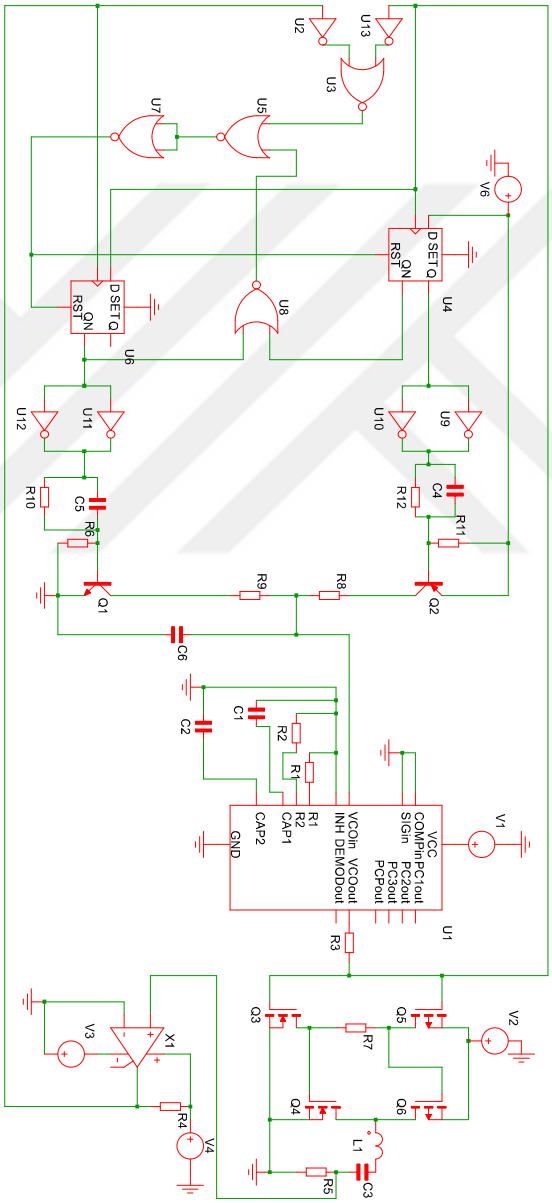

Figure 4.2 Full schematic of load resonant inverter with newly designed charge-pump PFD

CHAPTER FIVE
REALIZING A PROTOTYPE RESONANT INVERTER AND TEST RESULTS

5.1 Realizing of Circuit

First implementation of circuit was built on breadboard (Figure 5.1). PLL, transistors, and other integrated circuits was tested first. Also, needed capacitor, inductor and resistor values was calculated, provided and tested. After making sure that all elements have appropriate properties, first implementation of circuit was realized. Current signal was converted to square wave signal by Using LM311 integrated circuit. This IC is a comparator circuit. It compares input signal and reference signal and makes output logic "1" for situations that input signal is higher than reference voltage and makes output "0" for vice versa.

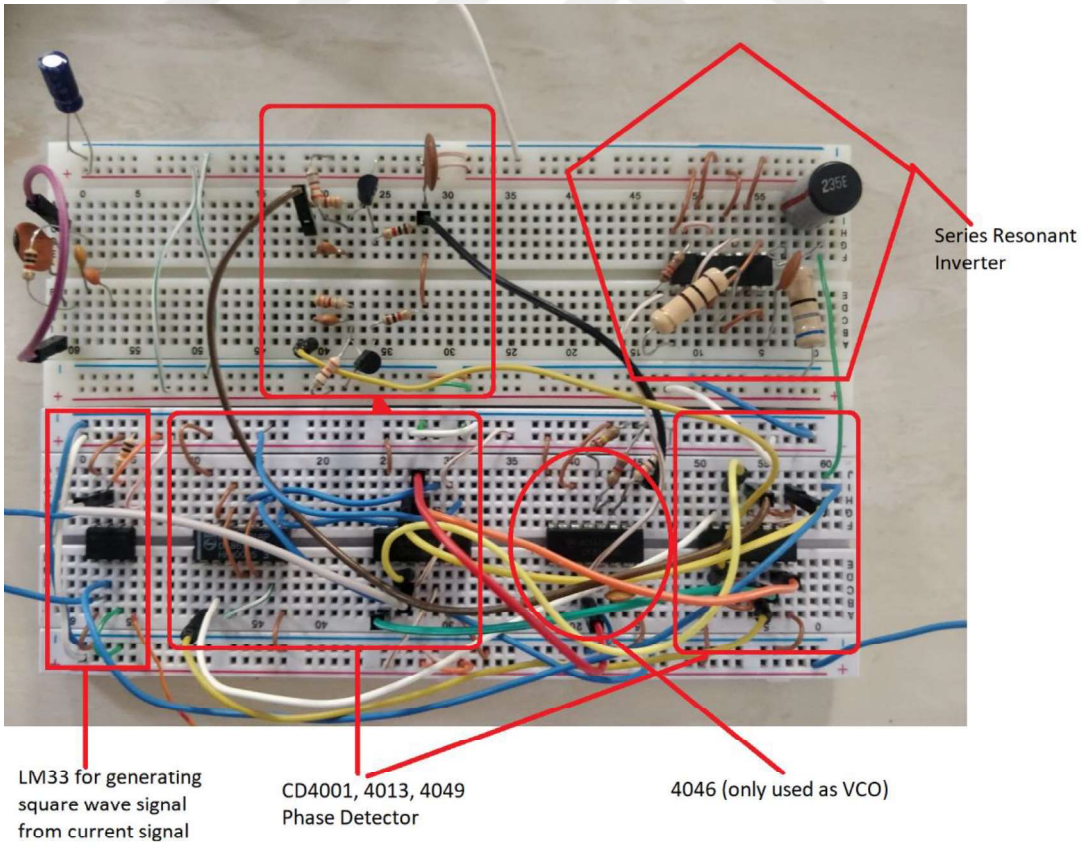

Figure 5.1 Implemented circuit on breadboard (Personal archive, 2019)

First of all, circuit was implemented by using PFD which is already available in HC4046 integrated circuit. The malfunction problem was observed too often at this step. VCO frequency was directly going to upper or lower operating limits at first start up directly. Also, while circuit was working correctly, VCO frequency jumped to upper or lower limits suddenly. Four measuring points (A, B, C, D) are shown in figure 5.2. Voltage and current signals of phase difference condition is shown in Figure 5.3. After this observation, novel designed circuit was implemented.

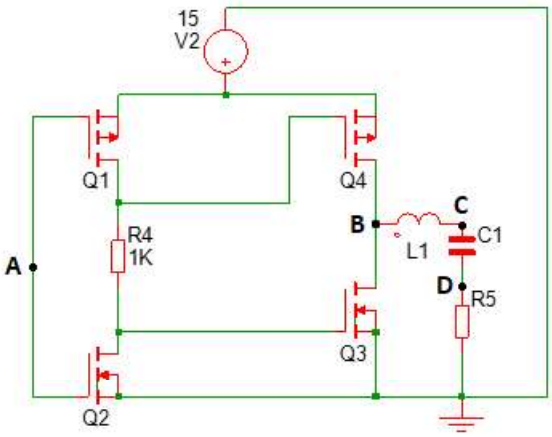

Figure 5.2 A series resonant inverter circuit diagram prototyped and used in experiment

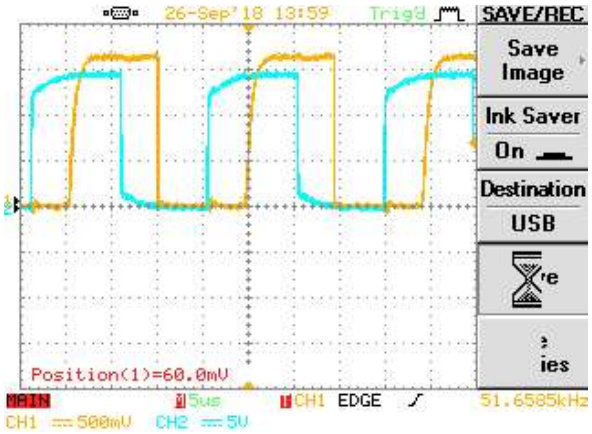

Figure 5.3 Phase difference between current and voltage when fs>fr. Yellow waveform represents current waveform at point D after converted a square wave, and blue one is voltage signal that drives the inverter at point A

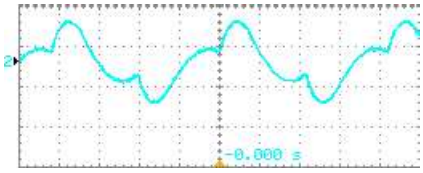

Figure 5.4 Current wave form observed at point D for the case fs>fr

Circuit was implemented on breadboard. There was a problem in circuit operation, and it was not working properly. Circuit was locking to different frequency from resonance frequency. After some observations and measurements, the cause of problem was observed. Capacitor voltage (Vc) in the loop filter was not true. There was a relation between Vc and correct value of capacitor voltage (Vc') that was

$$Vc + Vc' = Vcc \tag{5.1}$$

This problem was fixed by replacing inputs of PFD circuit. Another important problem was about MOSFETs. MOSFETs used in resonant inverter was burning easily even very low voltage because inverter was drawing high current by its nature. These MOSFETs changed with IRFD series power MOSFET. Warming and burning problem was eliminated by this way. After all tests and measurements PCB (Figure 5.4) was designed for designed circuit.

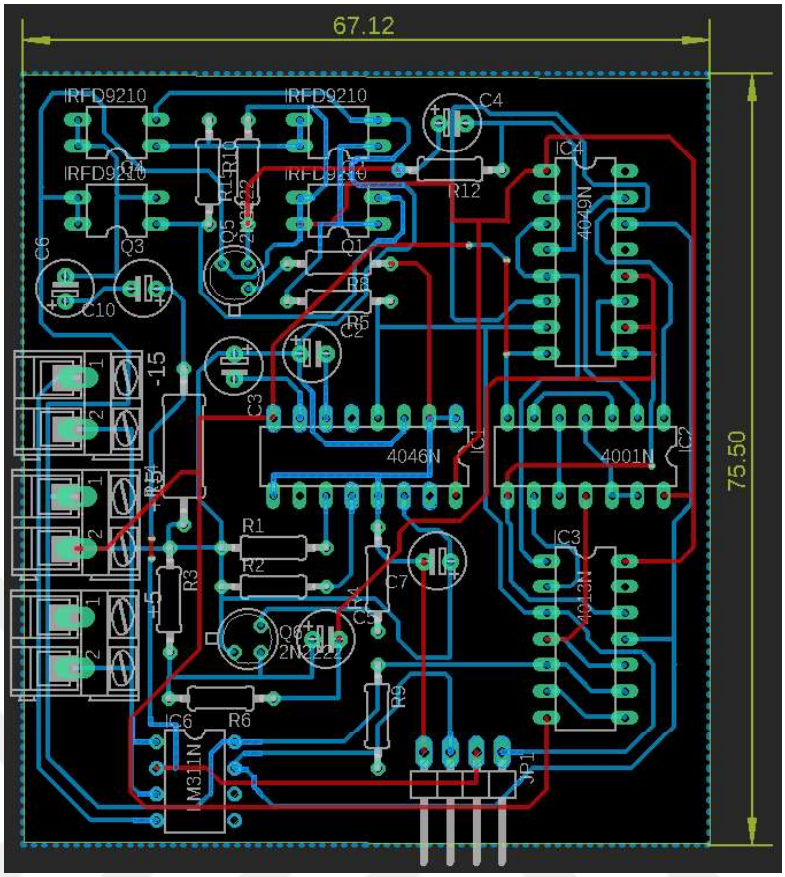

Figure 5.5 PCB of load resonant inverter implemented

5.2 Test Results

After implementation of circuit different tests and measurements were applied. A transistor was connected between capacitor in loop filter and ground. This transistor was triggered by an external source periodically and charging of capacitor was observed. It was observed that capacitor was charging every cycle of input signals step by step. These steps had different width in both time and voltage domains that shown in Figure 5.6 and Figure 5.7. At the beginning, capacitor voltage is zero and this voltage is applied to VCO input. VCO begins to oscillate at its minimum limit frequency. After first start up circuit, capacitor is starting to charge. Its voltage increases and so VCO frequency increases gets closer to resonant frequency. This increasing in frequency causes the capacitor voltage to charge with small steps.

Figure 5.6 Charging capacitor waveform in loop filter during tuning process

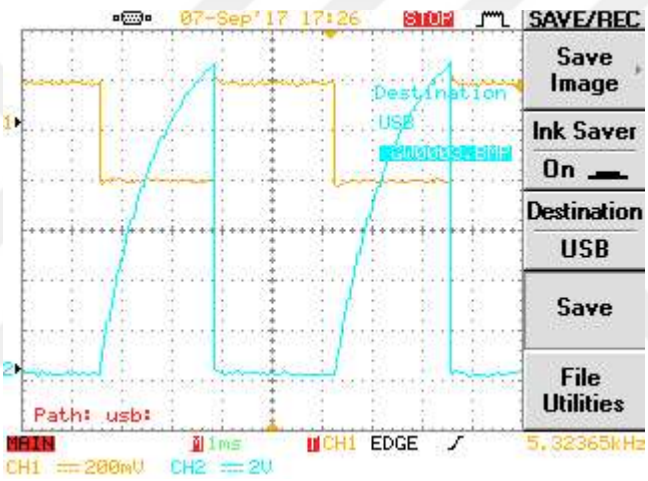

Figure 5.7 Blue one is charging capacitor waveform in loop filter, and yellow one is periodic external signal that makes capacitor voltage to discharge via a transistor

After comparator is applied to current signal, it is converted to a square wave signal that is shown in Figure 5.8. This square wave signal is applied to PFD with voltage signal and rising edges triggered PFD. Finally, VCO Frequency was set to resonance frequency. Voltage and current signal at resonance frequency are shown in Figure 5.9, Figure 5.10 and Figure 5.11.

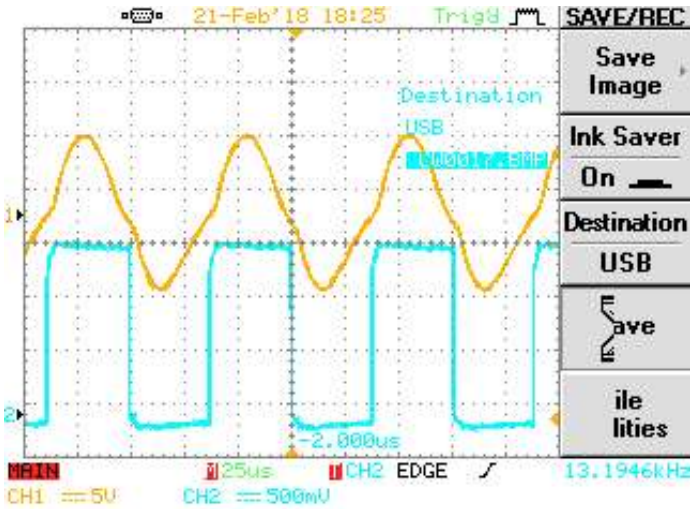

Figure 5.8 Current waveforms at point D before and after comparator when fs=fr. Yellow one is original current waveform, and blue one is obtained after applying comparator

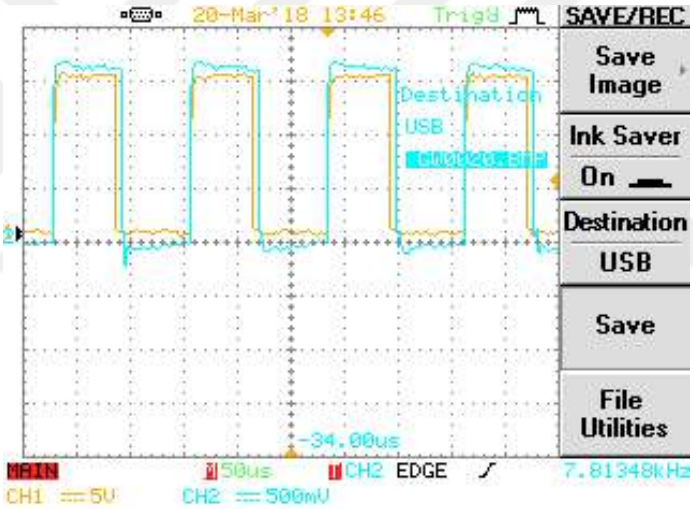

Figure 5.9 Current and voltage waveforms at point D when fs=fr. Yellow one is current signal that is comparator applied, and blue one is voltage signal that drives inverter

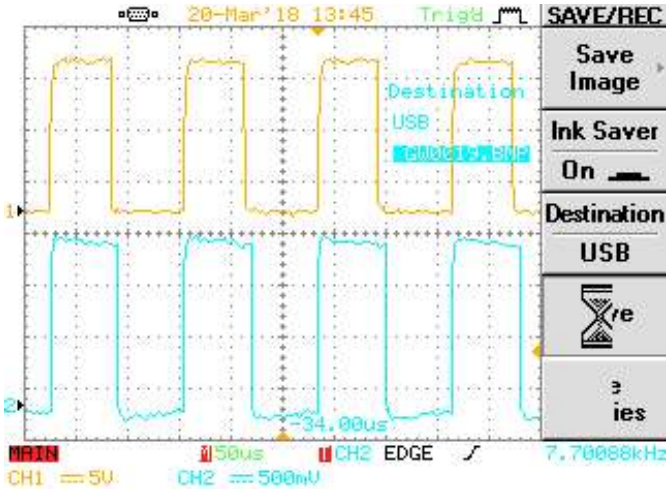

Figure 5.10 Current and voltage waveforms at point D when fs=fr. Yellow one is current signal that is comparator applied, and blue one is voltage signal that drives inverter

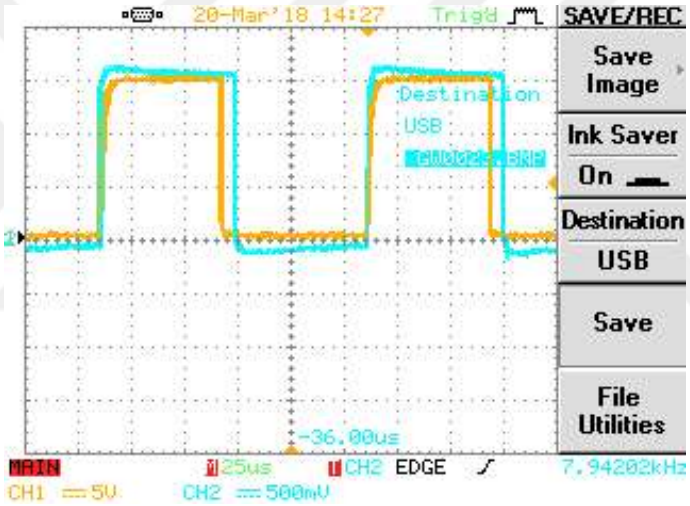

Figure 5.10 Current and voltage waveforms at point D when fs=fr. Yellow one is current signal that is comparator applied, and blue one is voltage signal that drives inverter

Voltage waveforms over resonant load are shown in figure 5.12, 5.13, 5.14, and measuring points are shown in figure 5.2.

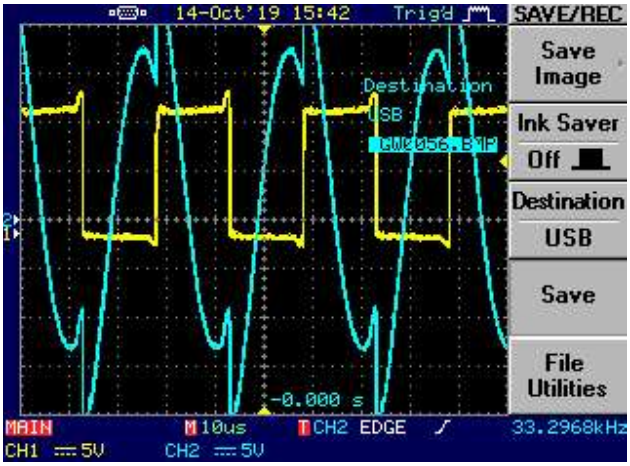

Figure 5.11 Voltage waveforms over resonant load. Blue one is voltage waveform over inductor (at point B), and yellow one is voltage waveform over capacitor (at point C)

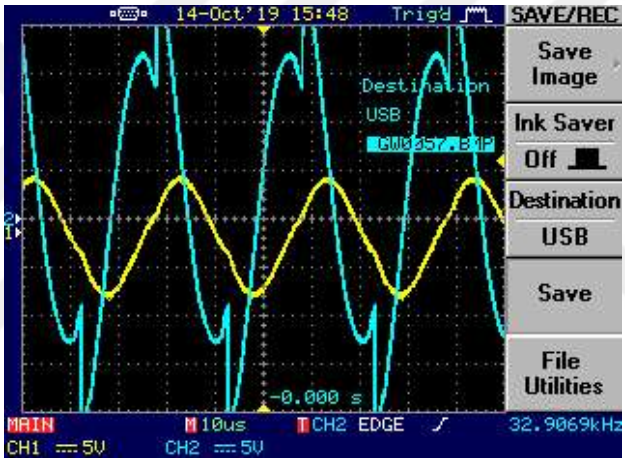

Figure 5.12 Voltage waveforms over resonant load. Blue one is voltage waveform over inductor (at point B), and yellow one is voltage waveform over resistor (at point D)

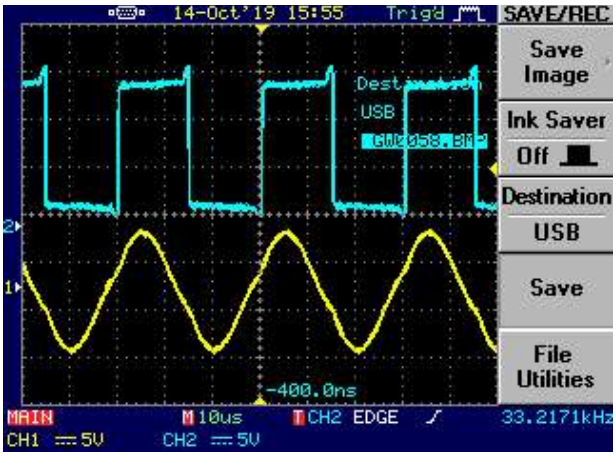

Figure 5.13 Voltage waveforms over resonant load. Blue one is voltage waveform over capacitor (at point C), and yellow one is voltage waveform over resistor (at point D)

CHAPTER SIX
CONCLUSION

In this thesis; resonant inverters, PLL and phase detectors was studied. A malfunction problem with PLL operation in load tracking loop of resonant inverter was observed. Malfunction problem causes to lose lock state in the loop. After investigation and measurements, root cause of the malfunction problem was found out. A glitch that is caused by interference or switching speed is defined as cause of this problem. Solutions was investigated to eliminate effect of the glitch.

Cause of problem was determined as a glitch occurred in input signals of phase frequency detector. Phase frequency detector has rising edge triggered D-type flip-flops and it provides a memory. When a glitch causes a wrong rising edge, it disrupts the phase lock and makes frequency jump to maximum or minimum limit. A novel phase frequency detector was designed to eliminate the malfunction problem. This circuit has a second reset circuit. This circuit works dependent of current and voltage signals directly instead of flip-flops output. This situation provides to reset flip-flops and eliminate effect of the glitch.

Two circuit was constructed. One is constructed with phase frequency detector that exists in PLL chip CD4046 and new designed phase frequency detector was used in the other one. The malfunction problem was observed in first circuit that uses phase frequency detector in CD4046 too often. It is found that this phase detector is not suitable for the purpose due its sensitivity to noise. In the second circuit, the new phase detector, is tested in the frequency control loop and found more immune to electrical glitches through the experiments. Resonant inverter tested under different conditions which are different resonance frequencies and different start up conditions. The malfunction problem that observed with phase detector inside the PLL chip CD4046 was not observed when new designed circuit was used.

Novel designed phase frequency detector circuit can be included into CD4046 integrated circuit in the future or it can be used as external circuit to eliminate

problem for now. Adding new circuit and new components may cause to increase of cost. However, when we compare cost with advantages, new designed circuit provides more advantages and efficiency, and these makes new circuit preferable

As a result of work fulfilled, the resonant inverter is got become more immune to noise and malfunction problem was disappeared by using the phase detector designed in this thesis.

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APPENDICES

Symbols and Abbreviations

C: Capacitor

R: Resistor

L: Inductor

Xc: Capacitive reactance

Xl: Inductive reactance

f: Frequency

ω: Angular Frequency

VCO: Voltage-Controlled Oscillator

PFD: Phase Frequency Detector

PD: Phase Detector

LF: Loop Filter

LPF: Low-Pass Filter

PCB: Printed Circuit Board

IC: Integrated Circuit

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

Xc: Capacitive reactance

Xl: Inductive reactance