HIGH PERFORMANCE ELECTRONICS BASED ON ALIGNED ARRAYS OF SINGLE WALLED CARBON NANOTUBES

BY

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B.S., Middle East Technical University, 2001
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DISSERTATION

Submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy in Physics
in the Graduate College of the
University of Illinois at Urbana-Champaign, 2007

Urbana, Illinois

ABSTRACT

This dissertation describes a new approach for generating large area homogenous parallel array of single walled carbon nanotubes. The approach uses guided growth, by chemical vapor deposition (CVD), of SWNTs on single crystal quartz substrates. The anisotropic interaction associated with lattice structure of the quartz between SWNT and quartz surface guides SWNT during the deposition process. We have optimized CVD conditions that can produce arrays of individual single walled carbon nanotubes in horizontal configurations with perfect linear shapes, to within experimental uncertainties, and with levels of alignment >99.9%. We took the method one step further by printing these SWNT arrays on unusual substrate such as plastic. Using the developed printing technique, we can fabricate multilayer superstructures of single-walled carbon nanotubes (SWNTs) on a wide range of substrates.

In order to understand charge transport through SWNT networks, we studied the scaling behaviours SWNT transistors by systematically varying degrees of alignment and coverage in transistors with a range of channel lengths and orientations perpendicular and parallel to the direction of alignment. We have modelled our experimental results using a first principles stick-percolation based transport model which provides a simple framework to interpret the sometimes counter-intuitive transport parameters measured in these devices.

We have used dense, perfectly aligned arrays of long, perfectly linear SWNTs as an effective thin film semiconductor suitable for integration into transistors and other classes of electronic devices. These types of devices show excellent electric performance with mobilities and scaled transconductances approaching ~2,000 $cm^2\ V^{-1}\ s^{-1}$ and ~3,000 $S\ m^{-1}$, respectively. MOS and CMOS logic gates and mechanically flexible transistors on plastic were also demonstrated. Finally we have studied the high frequency performance of transistors that use aligned SWNT arrays. For the first time we have observed power gain from SWNT transistors. This achievement allows us to build all of the key functions of analog electronics, including resonant antennas, fixed RF amplifiers, RF mixers and audio amplifiers. Combining these components we have built the first carbon nanotube radio. These results represent important first steps to practical implementation of SWNTs in high speed analog circuits.

To my wife and daughter

ACKNOWLEDGMENTS

I would like express my deepest gratitude to my academic advisor, Prof. John A. Rogers, throughout my Ph. D. program at University of Illinois at Urbana-Champaign (UIUC). These sentences can not explain my acknowledgment for his support and guidance. He is a perfect teacher and mentor. I have always tried to learn his clear scientific thinking. I am proud to be his student and I am happy that I can keep this honor all my life.

I am very lucky to have Prof. Alexey Bezryadin, Prof. Karl Hess, Prof. Taekjip Ha, Prof. Nadya Mason and Prof. Ivan Petrov in my thesis committee. Their, advice are key ingredients for this dissertation.

I want to tell my gratitude to our collaborators Prof. Moonsub Shim, Prof. M. Alam and Prof. Slava Rotkin and Ninad Pimparkar. I would like to thank Dr. Hong Zhang, Dr Aaron Pesetski and Dr. James Baumgardner for their help and contributions for RF experiments.

I am indebted to Dr. Dahl-Young Khang, Dr. Seong Jun Kang, Taner Ozel, and the undergraduate student who helped me to carry this work forward. Their contributions are very valuable for the thesis. I want to thank all current and former members of the Rogers group for making high standard scientific environment.

Finally, I dedicate this dissertation to my wife and daughter.

This material is based upon work supported by the National Science Foundation under grant NIRT-0403489 and the U.S. Department of Energy, Division of Materials Sciences under Award No. DEFG02-91ER45439, through the Frederick Seitz MRL and Center for Microanalysis of Materials at the University of Illinois at Urbana-Champaign.

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CHAPTER 1 INTRODUCTION

The main goal of my doctoral research is to develop a new approach for generating large area homogenous parallel array of single walled carbon nanotubes (SWNT) and integration of these arrays for high performance thin film type electronic devices. The scope of the research ranges from the fundamental scientific understanding of the technique and device operation to fabrication of high speed devices on both flexible and rigid substrates.

Macroelectronics is a new kind of emerging technology which is aiming to generate large scale consumable electronics on unconventional substrates such as plastics, paper etc... Flexible displays, electronic textile, electronic tag, large area photovoltaics are some of the possible applications of macroelectronics. The idea behind the new technology is to use low cost semiconducting materials to fabricate large area electronics with decent performance. Large area electronics requires very cost effective materials and processes, therefore the main trend of macroelectronics is based on low cost polymer based electronics which is knows as polytronics (1). Conjugated polymers, oligomers and other small molecules have been tested as a thin film semiconductor. However electronic performance of these materials is very poor because of the small grain size and week intermolecular interactions. Typical filed effect mobility of these materials is less than 1 cm^2/Vs. Researchers are exploring new alternative materials which have good electronic properties together with ability to be processed on unconventional substrate in a cost effective way. Organic crystals, amorphous silicon, nanostructured inorganic semiconductors are some of the promising candidates for macroelectronics. The review article (2) provides an extensive summary of recent developments in this field.

The high carrier mobilities (~10000cm^2/Vs) of single-walled carbon nanotubes (SWNT) make them interesting for possible applications in nanoelectronics (3-8), and together with the ability to deposit the tubes onto plastics substrates make them attractive for macroelectronics applications. Recent studies (8-14) demonstrate that SWNT network can be used as a semiconducting film for thin film transistors. Figure 1.1 shows scanning electron micrograph of SWNT random network. Although individual SWNT has very high carrier mobilities (~10000cm^2/Vs), ensemble behaviour of the tubes in a

random network provides much lower mobilities (~50cm^2/Vs). Tube-tube junction resistance and screening between the tubes limit the charge transport in the network and reduces the performance of SWNT random networks. Figure 1.2 shows layout of back gated SWNT TFT. In order to achieve intrinsic performance of SWNTs, placing them into regular linear arrays is required. Densely packed, perfectly aligned horizontal arrays of non-overlapping, linear SWNTs as an effective thin film electronic material has the potential to avoid these problems.

1.1 Carbon Nanotubes

Carbon nanotubes (CNTs) are one of the allotropes of carbon. Basically CNTs are graphene sheets rolled into a cylinder. Depending of number of layer in the tube, they are named as single-walled (SWNT) or multi-walled (MWNT). All of the carbon atoms in carbon nanotube has sp^2 bond. Sp^2 bond, which is stronger than sp^3 bond, provides mechanical stability of the carbon nanotube in a cylindrical shape. The diameter of the tubes is ranging from 0.5nm to hundreds nanometers and the length of the tubes could be as long as centimeters. Electronic properties of the CNTs are very attractive for many applications ranging from nanolectronics (8), sensors (14-16), optoelectronic devices (17) to transparent conductors (18) and thin film electronics (19-21).

Chirality and diameter of the SWNT are two key parameters that determine electronic property of the tube. Chiral vector can be defined as

$$C_h = na_1 + ma_2 \quad (1)$$

where a_1 and a_2 unit vectors of hexagonal lattice and n and m are the integer numbers. Figure 1.3 shows four example of SWNT with different chrality. Figure 1.3a and b show metallic SWNTs and c and d show semiconducting SWNTs. The basic band structure of SWNT can be derived using the dispersion relation of graphene. Because of cylindrical geometry, SWNTs have periodic boundary conditions which can be written as

$$\vec{C}_h . \vec{k} = 2\pi j \quad (2)$$

Where j is an integer and k is the wave vector of the electrons. Figure 1.4 shows the band diagram of (3,3) metallic SWNT and (4,2) semiconducting SWNT, derived from the graphene dispersion relation .

As most of the organic semiconductors, semiconducting SWNTs show p-type conduction. Since electrons in SWNTs are fermions with velocity of $v_0=8\ 10^5$ *m/s* (23), the band structure of SWNT can be calculated using the dispersion relation for relativistic fermions which is written as

$$E(k) = \pm\sqrt{(m^*\upsilon_0{}^2)^2 + (\hbar k\upsilon_0)^2} \tag{3}$$

Where m^* is the effective mass, v_0 is the velocity and k is the wavevector of the electrons. The effective mass of the electrons are inversely proportional with the diameter of the SWNT and can be written as (23)

$$m^* = \pm\frac{2\hbar}{3d\nu_0} \tag{4}$$

Where *d* is the diameter of the tube. Zhou et al. (24) derived the highest carrier mobility of SWNT from these equations as

$$\mu_{peak} = 0.32\frac{e\tau_0}{m^*} \propto d^2 \tag{5}$$

In the diffusive regimes, the field effect mobility of SWNTs has quadratic diameter dependence.

It has been almost two decays since the discovery of carbon nanotubes by Sumio Iijma in 1991, however the major issues about the synthesis and assembly of SWNT still remains as a challenge. Several methods have been developed to grow carbon nanotubes. Electrical discharge, laser vaporization, HIPCO (High-Pressure CO Conversion) and chemical vapor depositions (CVD) are the most commonly used techniques for SWNT synthesis. For our experiments, we have used CVD technique. Figure 1.5 shows the CVD setup and its schematics. We typically used methane gas or ethanol as a carbon source. At growth temperatures (~900C), hydrocarbons decompose and start to precipitate on the catalyst nanoparticles. Transition metals (Fe, Ni, Co) are generally used as a catalyst, however very recently Takagi *et al.* (25) showed that different metal nanoparticles such as gold, silver or copper can also catalyst SWNT growth. The details of the CVD process are given in the previous chapters.

1.2 Assembly of SWNTs

Different methods have been developed to assemble SWNTs and it is still a hot topic. I will summaries some of these techniques. Figure 1.6 illustrates some of these techniques.

Solution casting: This techniques uses dispersed SWNT solution and assemble them by solution casting or dip coating on substrates (26-28). Some degree of alignment can be obtained due to the shear forces associated with fluid flows. This technique can used large area depositions.

Controlled Flocculation: SWNT can be deposited on selective areas by controlling the specific interactions between nanotubes, ligands or surfaces (29). Methanol added to a surfactant-stabilized SWNT solution initiated the deposition of SWNT. Confining the SWNT solution in microfluidics channels, can provide depositions on narrow line geometry.

Directed self assembly: This technique is based on affinity difference of SWNTs on polar or nonpolar surfaces. SWNTs have higher affinity on polar surfaces. Self assemble monolayers (SAM) can be pattered into small features by using nanolithography tools. SWNT can be localized in to sub-100nm by controlling the affinity of the surface (30).

Electric filed assistant growth: This method is an *in situ* technique that use external electric filed to guide SWNTs during the growth process. Strong electric fields (1V/μm) can induce a dipole moment on the tube. Electric field induces large aligning torque on the tube (31,32). This technique requires predefined high temperature stable electrodes on the growth substrate.

Gas Flow: Gas flow during the deposition process can induce some degree of alignment. Different versions of this technique have been tested. Very recently Jin et al. (33) reported that mechanism behind the gas flow induce alignment is the buoyancy effect. Temperature difference between substrate and feeding gas provides convection flow which can lift the catalyst and drag it along the sample. Even very small gas flows (1sccm) can produce very long (1cm) SWNT arrays.

Epitaxy: Epitaxy is a growth technique that uses a crystalline substrate as a seed to grow high quality crystalline film. In today's technology, epitaxy is the most common technique to grow high quality crystals such as gallium nitrate, gallium arsenate. Similar

methods have been used to grow nanowires on inorganic crystals such as mica, Al2O3, KCl exc... (34-37). For these types of growth process, inorganic crystals provide a template which produces anisotropic intermolecular forces that can guide nanowire growth. Similar types of anisotropic arrangements have been observed for SWNTs. Song et. al. (38) reported directional growth of SWNT on a-plane and r-plane of sapphire crystal. Independently Ago et al. (39) reported guided growth on R, M, and A planes of sapphire crystal. Figure 1.7 shows their results. They claim that the preferential growth is related with the anisotropic arrangement of Al atoms on the crystal surface.

Graphoepitaxy: Graphoepitaxy is a type of epitaxy technique that uses surface relief structure to initiate the crystallization. This technique has been used to grow SWNTs on sapphire (Al_2O_3) surface (40,41). Figure 1.8 shows the flow chart of the graphoepitaxy growth of SWNT. Surface relief structures have been formed by annealing the sapphire crystal.

This thesis reports a novel technique to fabricate large-scale, high-density, aligned arrays of SWNTs using chemical vapor deposition on standard low-cost, commercially available, single-crystal quartz substrates. This technique offers a very simple, low cost route to bottom up self assemble SWNT which is very difficult or impossible with other recent techniques. The linear arrangement of SWNTs provides us a very good platform to build a thin film type transistor with very high performance.

1.3 Construction of the Thesis

Chapter 1 provides the outline of the thesis and provides background information about thins film electronics and single walled carbon nanotubes.

Chapter 2 describes a convenient process for generating large scale, horizontally aligned arrays of pristine, single walled carbon nanotubes (SWNTs). The approach uses guided growth, by chemical vapor deposition (CVD), of SWNTs on miscut single crystal quartz substrates. We have studied the growth parameters such as CVD conditions and the morphology of the quartz, and their effects on the density and alignment of these tubes. We have also demonstrated the thin film transistors that use aligned SWNTs as semiconducting film.

Chapter 3 reports chemical vapor deposition of SWNT from pattered catalyst on quartz crystal surface. Nearly perfectly aligned, high-coverage arrays of SWNTs can be generated in this manner. We have studied different aspects of the technique. High-coverage random networks of SWNTs can also be created in the same growth step, with good spatial alignment and electrical interfaces to the aligned arrays. Tubes with these geometries are ideally suited to applications in thin-film electronic devices. We demonstrate this possibility through the construction of thin-film-type transistors in which the random networks form the source and drain electrodes and the aligned arrays form the channel.

Chapter 4 reports optimized chemical vapor deposition growth procedures that can produce arrays of individual single walled carbon nanotubes in horizontal configurations with perfect linear shapes, to within experimental uncertainties, and with levels of alignment >99.9%. This process also enables simultaneous growth of random networks of SWNT integrated with the arrays, in complex layouts. The electrical properties of thin film type transistors formed with SWNTs grown in this fashion approach expectations based on the intrinsic properties of the pristine, individual SWNTs. Furthermore we have studied SWNT growth on different quartz surfaces. These types of results reveal the important aspects of the alignment mechanism.

In Chapter 5, gate modulated transport through partially aligned films of single walled carbon nanotubes (SWNTs) in thin film type transistor structures are studied experimentally and theoretically. Measurements are reported on SWNTs grown by chemical vapour deposition with systematically varying degrees of alignment and coverage in transistors with a range of channel lengths and orientations perpendicular and parallel to the direction of alignment. A first principles stick-percolation based transport model provides a quantitative framework to interpret transport parameters measured in these devices.

In Chapter 6, we report the use of dense, perfectly aligned arrays of long, perfectly linear SWNTs as an effective thin film semiconductor suitable for integration into transistors and other classes of electronic devices. The large numbers of SWNTs enable excellent device level performance characteristics and good device-to-device uniformity, even with SWNTs that are electronically heterogeneous. Measurements on *p*- and *n*-

channel transistors that involve as many as ~2,100 SWNTs reveal mobilities and scaled transconductances approaching ~1,000 $cm^2\ V^{-1}\ s^{-1}$ and ~3,000 $S\ m^{-1}$, respectively, and currents of ~1 A in devices with interdigitated electrodes. We have also demonstrated PMOS and CMOS logic gates using these types of devices.

In Chapter 7, we developed a technique to print aligned SWNT on different substrates such as high-k thin dielectrics on silicon wafers, transparent plates of glass, cylindrical tubes and other curved surfaces, and thin, flexible sheets of plastic. The approach involves guided growth of SWNTs on crystalline and amorphous substrates followed by sequential, multiple step transfer of the resulting collections of tubes to target substrates.

Chapter 8 reports the high frequency applications of SWNT arrays generated by guided growth on quartz crystal surface. We have implemented dense SWNT arrays to yield radio frequency (RF) SWNT analog electronic devices, such as narrow band amplifiers operating in the VHF frequency band with gains as high as 14 dB. As a demonstration, we fabricated nanotube transistor radios, in which SWNT devices provide all of the key functions, including resonant antennas, fixed RF amplifiers, RF mixers and audio amplifiers. These results represent important first steps to practical implementation of SWNTs in high speed analog circuits.

Chapter 9 provides some routes to improve developed techniques and new application of the aligned SWNT arrays. Modeling results predicts that the tube density can be improved by order of magnitude. Controlling the catalyst particles may improve the tube density. We will discuss the possible techniques to deposit regular array of nanoparticle for carbon nanotube growth. In this chapter we will also introduce a new approach to eliminate metallic SWNT using the differences in optical absorption between these two types of SWNTs. The method is based on ablation of individual single-walled carbon nanotubes by use of intense picosecond laser pulses. Linearly polarized pulses ablate only those tubes that are oriented substantially along the polarization direction. Detailed examples highlight essential aspects of the approach and some features of the underlying physics that governs the process.

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1.5 Figures

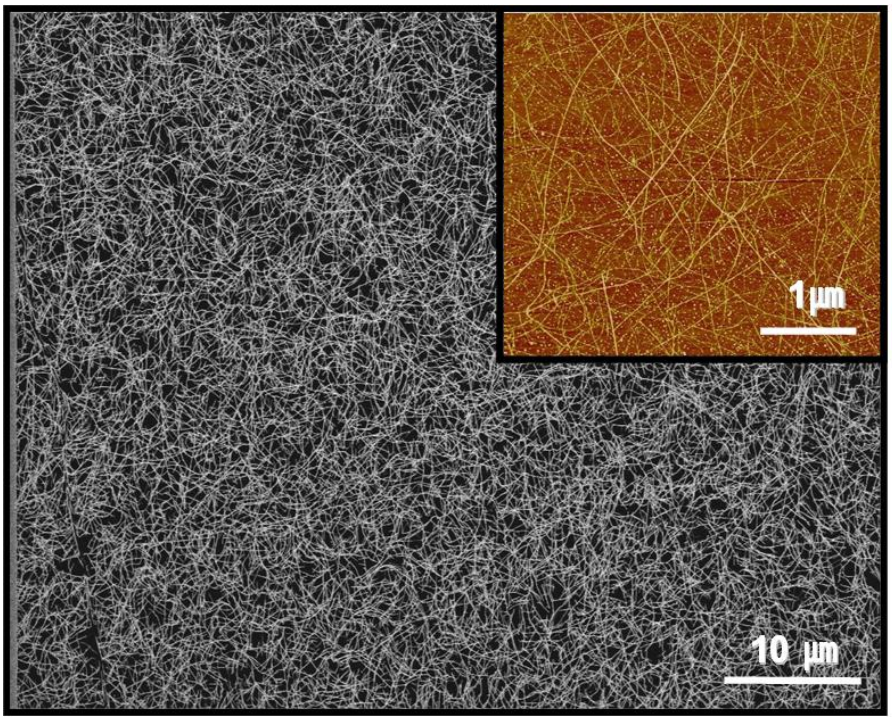

Figure 1.1 SEM and AFM (inset) image of SWNT random network.

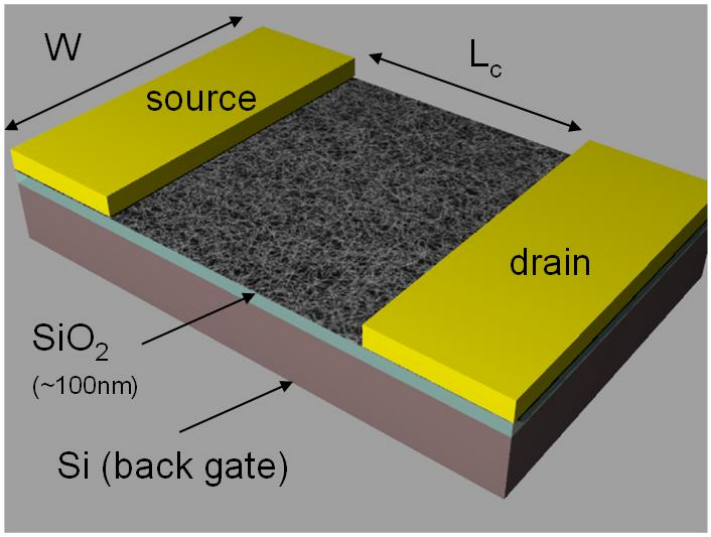

Figure 1.2 Layout of back gated thin film transistor that use SWNT network as a semiconducting film.

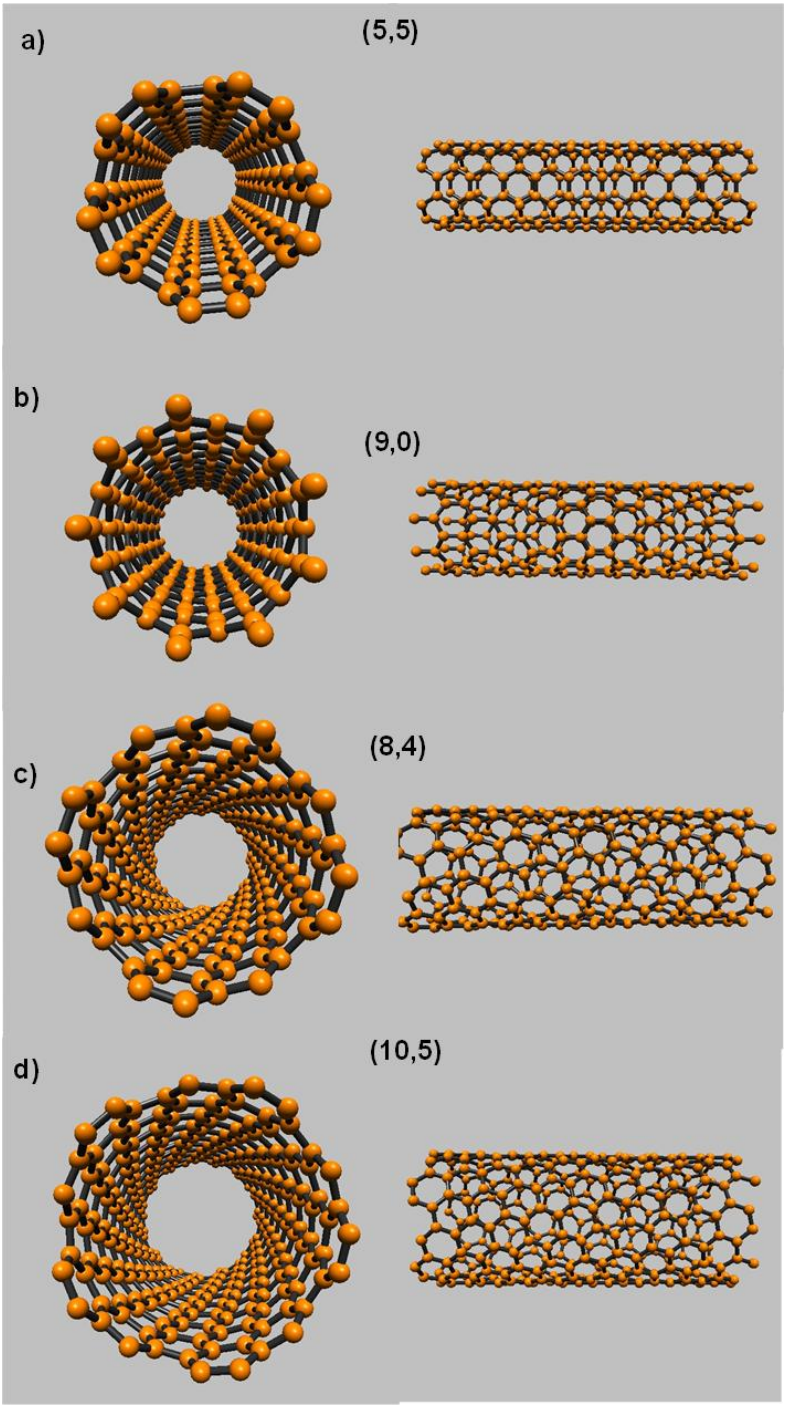

Figure 1.3 SWNTs with different chiral vector. (a-b) show metallic SWNT and (c-d) show semiconducting SWNT.

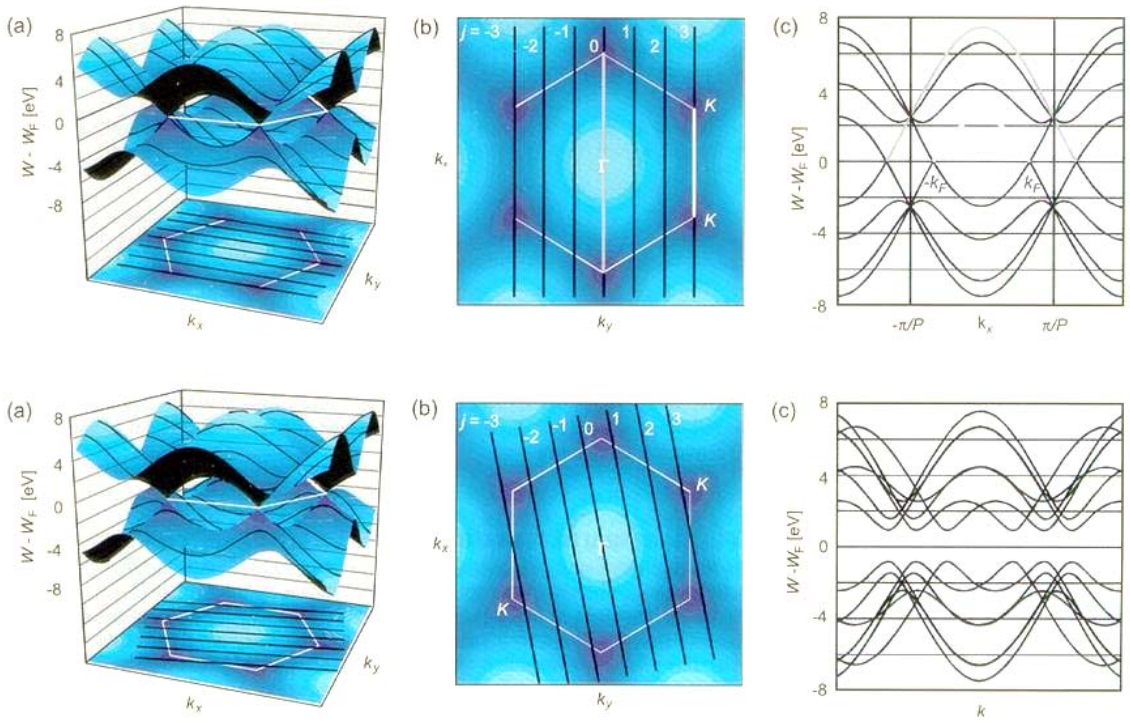

Figure 1.4 Dispersion relation of graphene superimposed with the allowed wavevector of (3,3) (first row) and (4,2) (second row) SWNTs. (Figure is taken from reference 22)

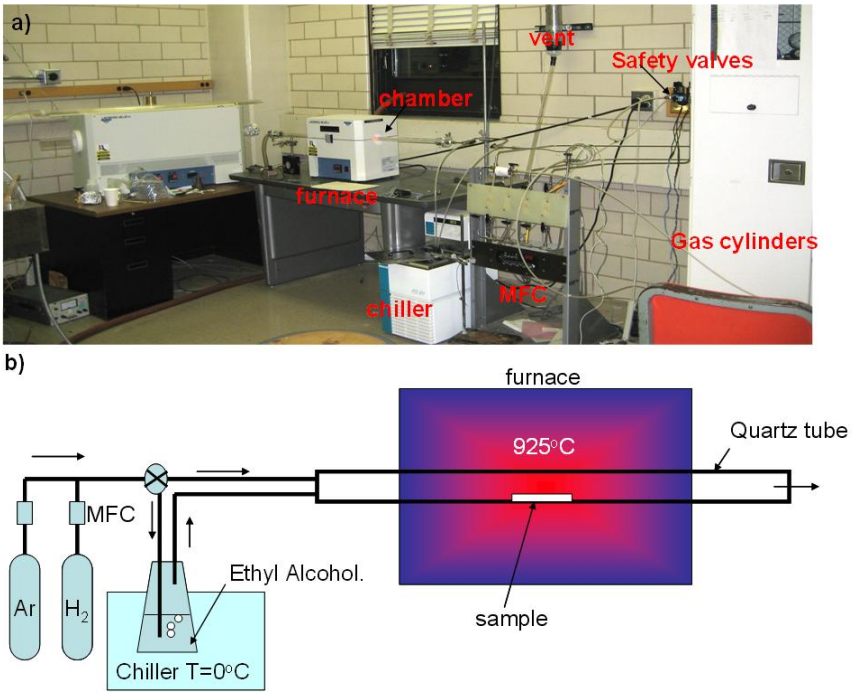

Figure 1.5 Chemical vapor deposition setup for SWNT growth.

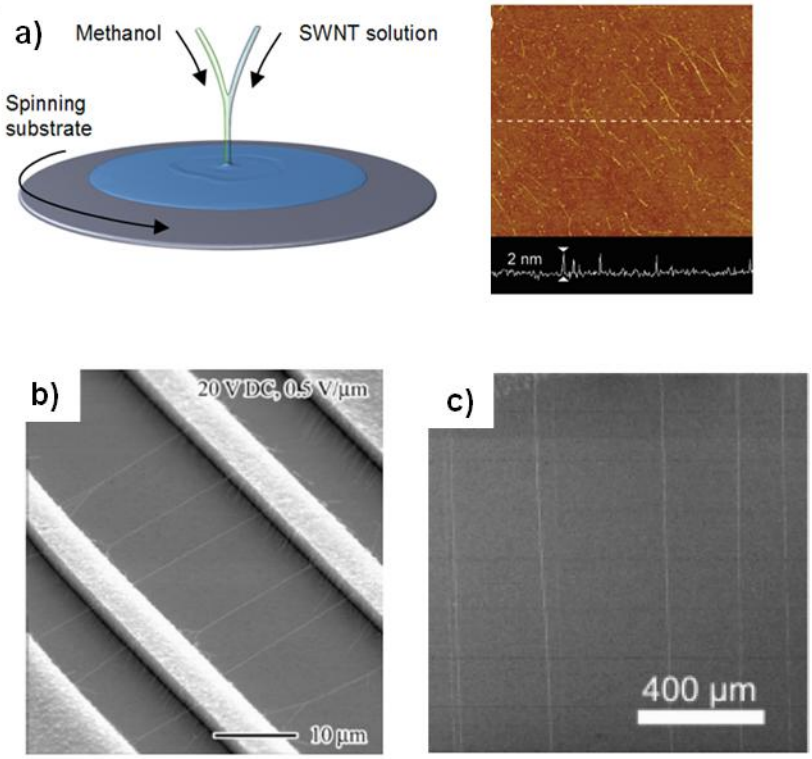

Figure 1.6 Three different techniques that can produce aligned SWNTs, a) spin casting (24), b) electric field assistant alignment (31), c) gas flow assistant alignment (33)

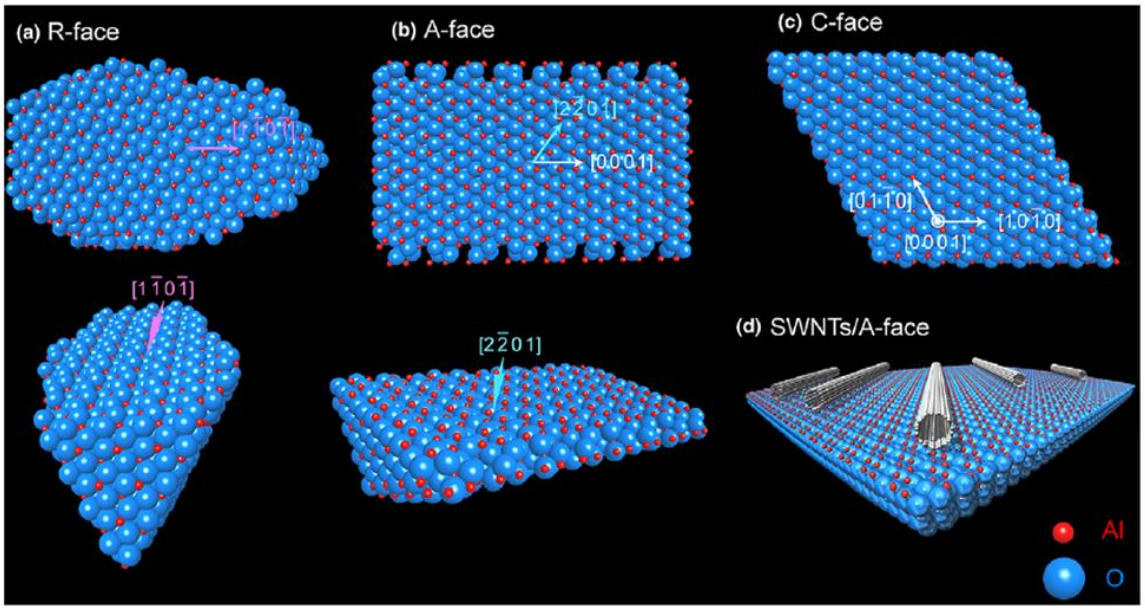

Figure 1.7 Guided growth of SWNTs on different sapphire surfaces. (Taken from ref. 36)

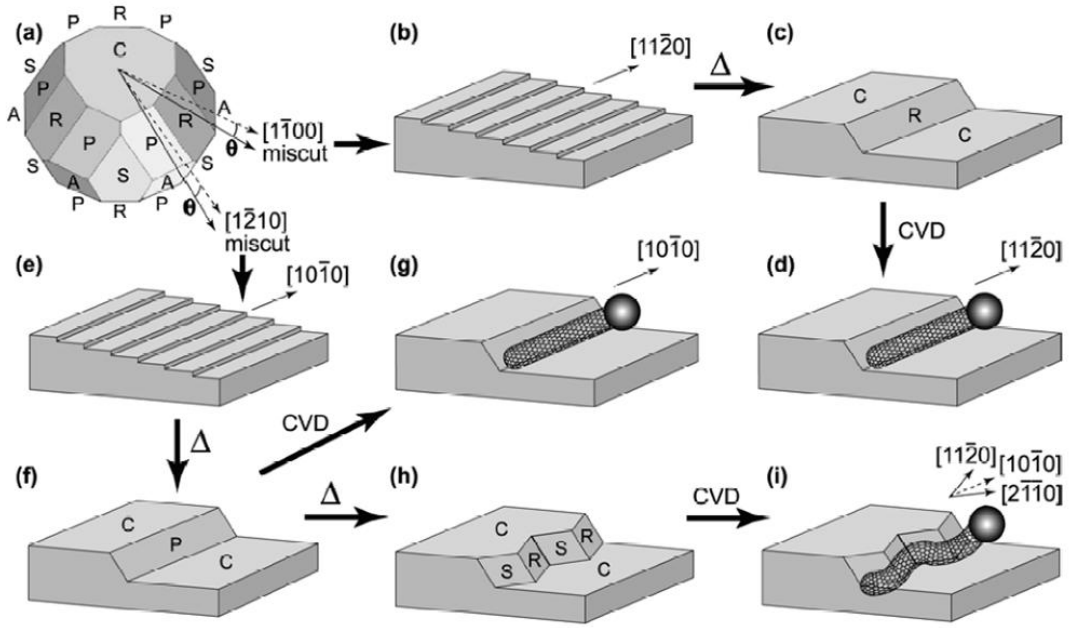

Figure 1.8 Flow chart of carbon nanotube graphoepitaxy by miscut of C-plane sapphire (taken from ref. 38)

CHAPTER 2 GUIDED GROWTH OF SINGLE WALLED CARBON NANOTUBES

This chapter was published as "Guided Growth of Large Scale, Horizontally Aligned Single Walled Carbon Nanotubes and Their Use in Thin Film Transistors, **C. Kocabas,** S.-H. Hur, A. Gaur, M. Meitl, M. Shim and J.A. Rogers, *Small 1(11), 1110-1116 (2005)* " Reproduced with permissions from the journal.

2.1 Introduction

The high mobilities of single-walled carbon nanotubes (SWNT) make them interesting for possible applications in nanoelectronics (1-5). These electronic properties together with the ability to deposit the tubes onto plastics and other unusual device substrates make them also well suited for use in large scale distributed electronics for steerable antenna arrays, flexible displays and other systems. Recent work indicates that random networks of SWNTs can form effective semiconductor layers for thin film transistor (TFT) type devices (6-11). The device mobilities that have been achieved with these networks are, however, still far below the intrinsic tube mobilities inferred from measurements of transistors that incorporate an individual tube (or small number of tubes) spanning the gap between the source and drain electrodes. The resistance at the many tube-tube contacts that are inherent in the networks may limit charge transport. Large scale aligned arrays of SWNTs avoid this problem, thereby offering the possibility to exceed the device mobilities that can be achieved in the networks.

Some degree of alignment can be obtained by casting SWNTs from solution (12-15), but dense arrays formed in this fashion usually involve large numbers of overlapping tubes. In addition, transistors that use solution deposited tubes typically have properties that are inferior to those built with tubes grown directly on the device substrate by, for example, chemical vapor deposition (CVD). Arrays of SWNTs can be generated from random networks, formed by CVD growth or solution deposition, via orientation selective ablation with linearly polarized laser pulses (16). This process has the advantage that it does not rely on chemistries or solvents that can alter the properties of the tubes; it is, however, an inherently destructive process. Electric field assisted growth

(17,18), fast heating (19) can produce aligned array of SWNTs. High density arrays that cover large areas have not, however, been demonstrated with these techniques; device implementations have also not been described. Recently, Ismach et. al. (20) reported a new method of atomic step templated growth of aligned SWNTs miscut sapphire crystals. Song et. al. (21) reported directional growth of SWNT on a-plane and r-plane of sapphire crystal, apparently unrelated to atomic steps. In the following, we show that large scale, high density aligned arrays of SWNTs can be generated by guided CVD growth on standard, low cost commercially available single crystal quartz substrates (22). It describes the nature of these arrays and the dependence of their characteristics (degree of alignment, tube diameter distribution and coverage) on the growth conditions. These data suggest that the alignment mechanism on quartz may have some similarities to that on sapphire (20). We also present the use of these large scale arrays as effective semiconductor 'thin films' for TFTs. The effective device mobilities (up to 125 cm^2V/s) are substantially higher than those that we have been able to achieve in random networks of SWNTs grown using similar techniques (~50 cm^2V/s) (5-10). The results indicate that low cost quartz substrates can be used to generate high quality aligned arrays of SWNTs for a range of applications in electronics and sensing.

2.2 Methods and Materials

Figure 2.1a shows atomic force microscope (AFM) images of SWNTs grown on SiO_2/Si using the procedures described in experimental section. The random networks observed in this case are similar to those that we previously used in thin film type transistors (10). The distributions of the tubes on quartz (Figure 2.1b) involve aligned arrays and few tube-tube crossings; they are much different than those observed on amorphous substrates, including SiO_2 and fused quartz. Figure 2.1c and Figure 2.1d present histograms of the tube orientations and diameters for the region of the substrate shown in Figure 2.1b, respectively. The AFM images are consistent with tubes that are mainly individual single-walled with diameter 1±0.5 nm. The structures with diameters larger than 2 nm could be small bundles. The diameter distribution is similar to those of tubes grown on SiO_2/Si. Conventional CVD growth procedures are most well established for use with SiO_2/Si substrates. We grew tubes on this type of substrate to serve as a

comparison for results on AT-cut quartz (22). We used ferritin catalyst (Aldrich) diluted by deionized water at a volumetric ratio of 1:200 cast onto the substrate, followed by heating at 900 ^{o}C for 10 min to oxidize the catalyst. After oxidization, the sample was cooled to room temperature. Heating to 900°C in a hydrogen environment reduced the catalyst. Purging with hydrogen at 900°C for 1 min and then flowing methane (2500 standard cubic centimeters per minute (sccm)) and hydrogen (75 sccm) at 900°C for 10 min led to the growth of SWNTs. We placed the quartz substrates on polished Si wafers in the growth chamber to enhance the homogeneity of the temperature distribution on their surfaces. Following growth, the samples were cooled slowly (< 5 ^{o} C/min) to avoid cracking in the quartz.

2.3 Results and Discussion

Figure 2.2a shows schematically a quartz crystal (trigonal symmetry) and the orientation of a Y-cut wafer. Most of the results illustrated in this paper use the AT-cut, which is a type of rotated Y-cut that has a cut angle of 35^0 15'. This type of wafer is used often in surface acoustic wave devices, microbalances and resonators. We observed similar tube distributions occur on quartz with slightly different Y-cut angles such as 36^0 or 38^0. Figure 2b shows a cross section of the quartz wafer and the $01\bar{1}$ atomic planes. The wafers have some degree of miscut with respect to these planes. This miscut can lead to steps on the surface, as shown schematically in Figure 2.2c. These types of steps have been observed directly on other quartz planes (23, 24). It is likely that similar steps exist on the Y-cut wafers, although we are unaware of similar direct measurements of them. We did not observe these steps in AFM images of the as-received wafers due, possibly, to the small distances between them. Nevertheless, long thermal annealing (7 hours, 900 C) generated, in some cases, steps spaced sufficiently far apart to allow imaging by AFM, as illustrated in Figure 2.2d.

The alignment of tubes grown on these substrates is always parallel to the direction of the features in Figure 2.2d. It is independent of the direction of gas flow, for the growth conditions explored here. Figure 2.3a shows a collection of well aligned tubes. The inset shows that the tubes are not perfectly straight; they have shapes that are similar to those observed in the step edges of Figure 2.2d. Figure 2.3a and b show that the tubes

also occasionally exhibit large, abrupt changes in their alignment. The shapes of these 'kinks' are similar to those in step edges that are often observed in quartz and other single crystal substrates such as Al_2O_3 (25), MgO (26), $MgAl_2O_4$ (27) that have some small degree of miscut. Figure 2.3c presents an AFM image and a scatter plot of orientation versus diameter appears in Figure 2.3d. Small diameter tubes (<1.5 nm) are mainly aligned; as the tube diameter increases above this value, the degree of orientation decreases. The degree of alignment is also influenced by annealing of the quartz before tube growth. Figure 2.4a-c show results obtained with substrates annealed at 900^0C for 10 min., 4 hours and 7 hours. Increasing the annealing time, which may increase degree of order in the crystal lattice near the surface as well as the lengths and order of the steps (23), improves the alignment.

To further characterize the aligned tubes, we measured Raman spectra (microRaman setup with a HeNe laser at 632 nm) of individual tubes in the arrays. Our spectrometer (Jobin-Yvon confocal) used a 100X microscope objective to focus a HeNe excitation laser (632 nm wavelength; ~1μm spot size; $5x10^5$ W/cm^2 power density) and to collect the backscattered Raman signal through a 50 μm pinhole. Figure 2.5a shows the Raman spectrum of tangential mode of single SWNT for various orientations of the linear polarization direction of the excitation laser. The one dimensional nature of carbon nanotubes gives rise to highly anisotropic optical properties (16, 28, 29). Figure 2.5b shows the dependence of the Raman signal on orientation. The data are accurately described with a $\sim\cos^2(\alpha)$ functional form, where α is the angle between the polarization of incident light and tube axis. The radial breathing mode (RBM) could not be measured because of the intense Raman signal from the single crystal quartz substrate. Thin film consists of aligned array of SWNT shows high optical anisotropy which could find some application for optical devises (30). In all other respects, the tubes on quartz have Raman signatures that are similar to those grown on SiO_2/Si. This spectroscopic information and the growth studies summarized in Figure 2.3 and Figure 2.4 are consistent with an alignment mechanism that relies on energetically favorable van der Waals interactions of the tubes and/or catalyst particles with the SiO_2 lattice along certain crystallographic directions and/or with the step edges (or micro/nanofacets). Additional work is required to determine the details of the process.

High performance TFTs and other devices benefit from closely packed aligned arrays of SWNTs. The coverage can be controlled by changing the concentration of the catalyst particles. Figure 2.6a-c show AFM images of SWNTs grown with different density of catalyst (2000, 100 and 20 times dilution, respectively). With the growth conditions used here, there is a trade-off between coverage and alignment. In particular, the degree of alignment decreases with an increasing number of large tubes and bundles, both of which tend to form at high coverage. Figure 2.6d-f show large areas imaged by SEM. For low densities (~1 tube/micron), nearly perfect alignment can be achieved. The distributions of the lengths of the tubes appear as insets in Figure 2.6d and Figure 2.6e. Generally, as the coverage increases, the average length of the tubes decreases. For the lowest densities, the average tube length can be ~100 μm. Figure 2.7a-c shows SEM images for the highest coverage (>10 tubes/μm) that we can currently achieve reliably. The large area images illustrate the remarkable homogeneity of these aligned, sub-monolayer coatings of SWNTs.

To demonstrate one possible application of these arrays, we built TFTs by first fabricating source/drain contacts of Ti/Au (3 nm and 25 nm thicknesses) on the SWNTs by electron beam evaporation followed by liftoff of a layer of photolithographically patterned resist (Shipley 1805). A layer of epoxy (SU-8; 1.6 μm thick) spin cast and photopatterned on top of this structure formed a dielectric layer for a gate electrode (25 nm thick Au) deposited by electron beam evaporation through a shadow mask. Figure 2.8a-b show SEM images of devices with channels aligned parallel and perpendicular to the direction of the aligned tubes. Figure 2.8c shows transfer characteristics collected from devices similar to those shown in Figure 2.8a,b, but with much longer channel lengths (100 μm). The measurement results clearly show the expected anisotropic response. In the perpendicular configuration, the residual current is due to a small network effect generated by the small number of unaligned tubes. The effective device mobility is given by $\mu_d = \frac{\partial I_D}{\partial V_G}\frac{L}{WCV_D}$ where I_D is the drain current, V_G is the gate voltage, L is the channel length, W is the channel width, and V_D is drain voltage. We estimate the gate capacitance C, to be $2.3\ 10^{-5}$ F/m^2 from the relation $C = \frac{\varepsilon\varepsilon_0}{t}$ where ε is

the dielectric constant of the gate dielectric SU-8 (4.0), εo is the vacuum permittivity, and t is the thickness of gate dielectric. For the parallel configuration, the device mobilities (evaluated in the linear regime, using standard procedures) can reach ~125 cm^2V/s, at channel lengths of 10 μm. This value is obtained with aligned SWNT arrays that have ~10 tubes/μm. A simple geometrical calculation yields a 'per tube' mobility of ~9000 cm^2V/s, which is comparable to that often observed in pristine single tube devices. It is possible that increases in the coverage of the aligned SWNT arrays will lead to improved device mobilities. Achieving this goal is a central focus of our current work. (We note that short channel lengths yield low on/off ratios, due to the presence of metallic SWNTs that span the source/drain gap. These tubes can be selectively eliminated through electrical breakdown or chemical functionalization (10,31))

2.4 Conclusions

In summary, this paper shows that Y-cut single crystal quartz can be used to generate over large areas, well aligned, densely packed, horizontal arrays of pristine SWNTs. Although additional work is required to understand more fully the detailed growth mechanisms, many of the features of the arrays and their dependence on growth conditions are consistent with either alignment along step edges or micro/nanofacets on the surface of the quartz or preferential interactions along certain directions associated with the quartz lattice. A step edge alignment process recently described for miscut α-Al_2O_3 (19) and a preferred interaction process for α-Al_2O_3 without miscut (20) may both be related to the effects that we observe here. The low cost and commercial availability of Y-cut quartz and the ability to grow dense arrays of tubes represent attractive features of the approach introduced here. The format of these arrays (i.e. lying horizontally on a flat substrate) allows easy integration into devices, as demonstrated by high performance TFTs. We believe that these types of arrays and the means for growing them will be valuable for a range of emerging applications that use large collections of SWNTs.

2.5 References

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2.6 Figures

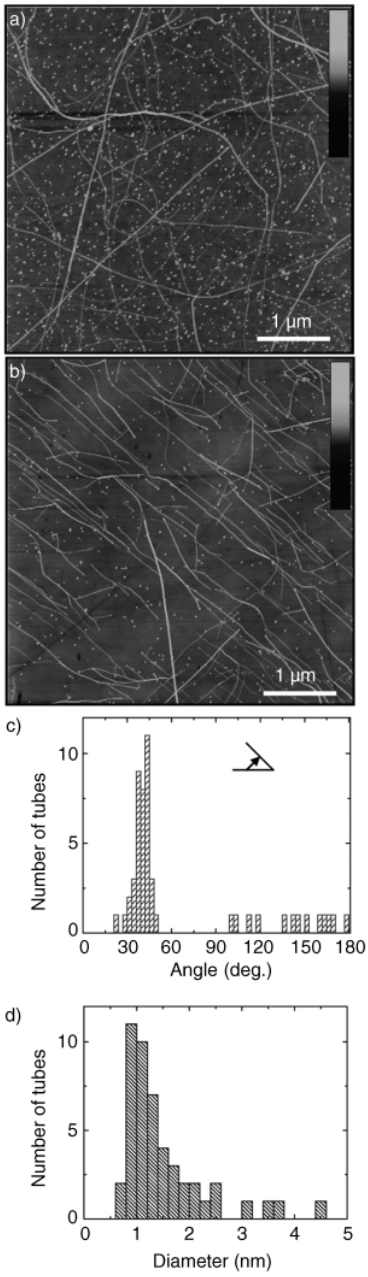

Figure 2.1 AFM images of random (a) and aligned (b) SWNTs grown on SiO_2 and single crystal quartz, respectively. Histogram of the orientation (c), and diameter (d) of the aligned SWNTs. These data suggest that most of the aligned tubes are individual tubes. In (a-b) the color bar represents 10 nm height.

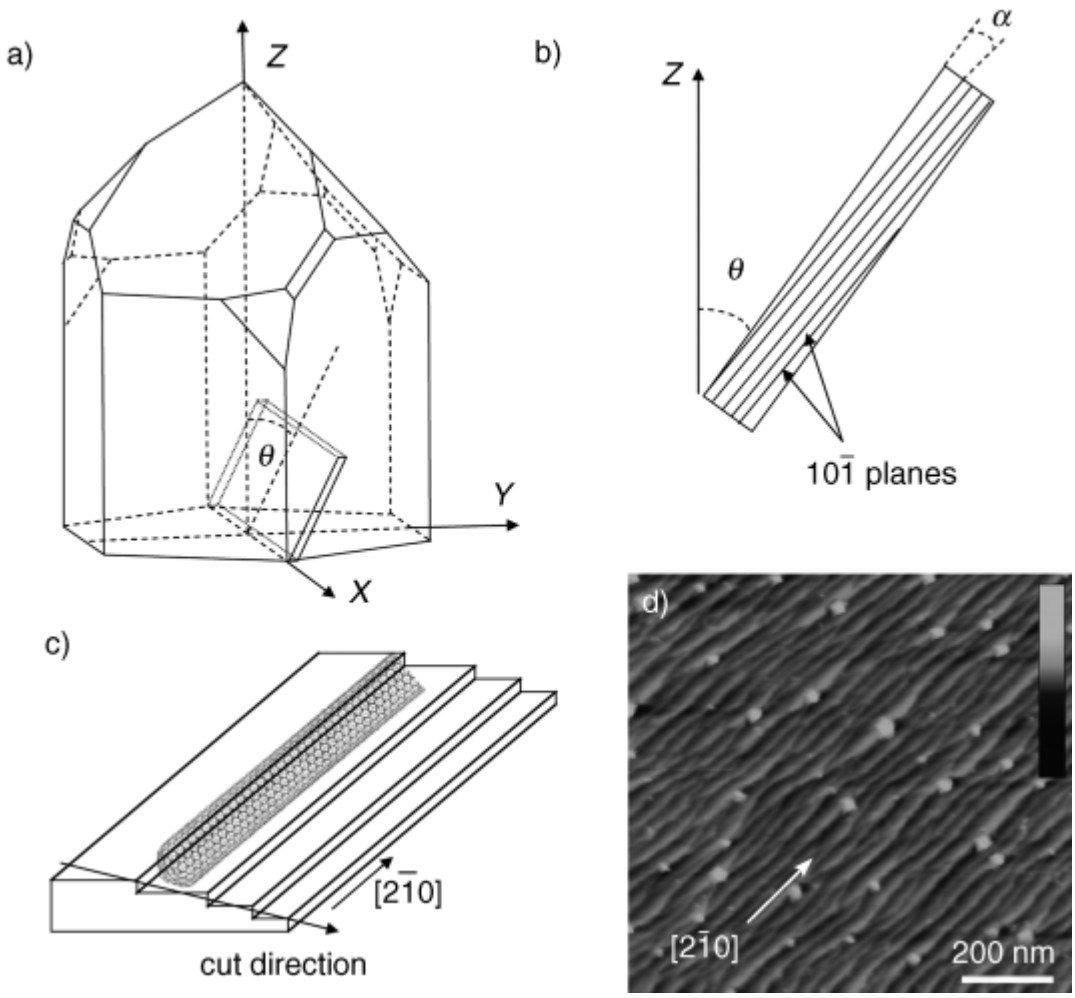

Figure 2.2 (a) Schematic illustration of the crystallographic planes in right handed α-quartz and the orientation of a Y-cut wafer. (b) Cross section of an AT-cut quartz wafer and $0\bar{1}\bar{1}$ planes. The mis-cut angle is 2^0 58'. (c) Schematic illustration of atomic steps and alignment direction on the surface. (d) AFM image of terraced surface structures after thermal annealing. The steps in this case are 0.7 to 1 nm high with 30 to 35 nm spacing. The small particles are ferritin catalyst. The color bar represents 5 nm height.

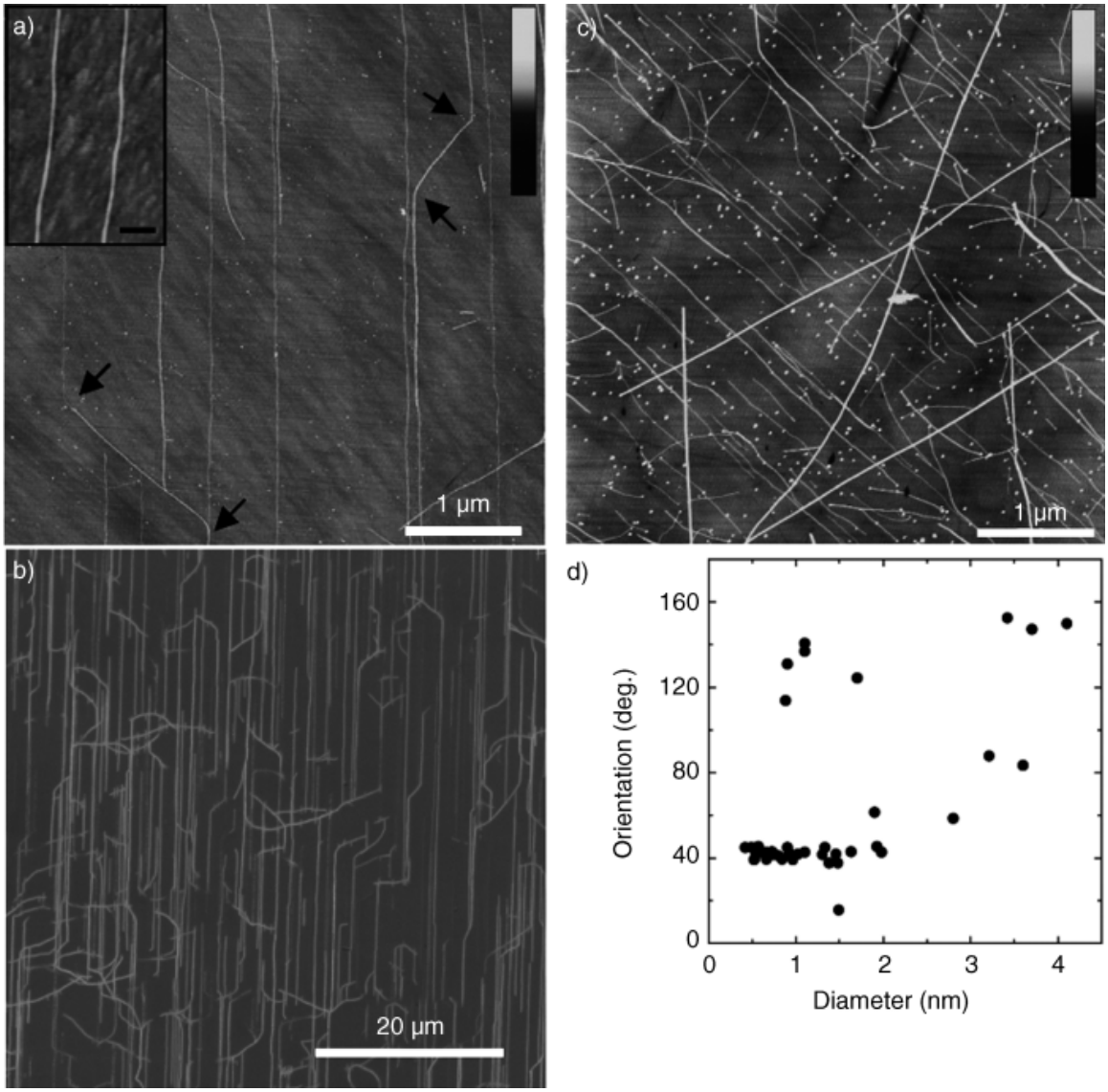

Figure 2.3 (a) AFM images of SWNTs grown on single crystal quartz substrates. The inset shows a high magnification view of a pair of tubes (scale bar is 75nm). Arrows in the main frame highlight 'kinks' in the tubes. (b) Large area SEM image of aligned tubes. (c) AFM image of aligned and unaligned SWNTs. (d) Scatter plot of the tube orientation versus the tube diameter. Large diameter (>1.5 nm) tubes (which may be small bundles) are more likely to be unaligned than small diameter (< 1.5 nm) ones. In (a-c) the color bar represents 10 nm height

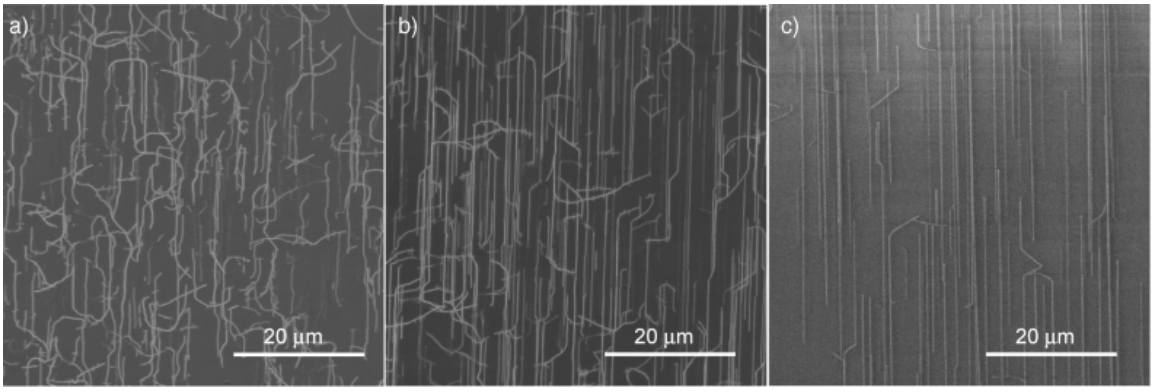

Figure 2.4 SEM images of SWNTs grown on quartz annealed at 900 C for different times. (a) 10 min. (b) 4 hours, (c) 7 hours.

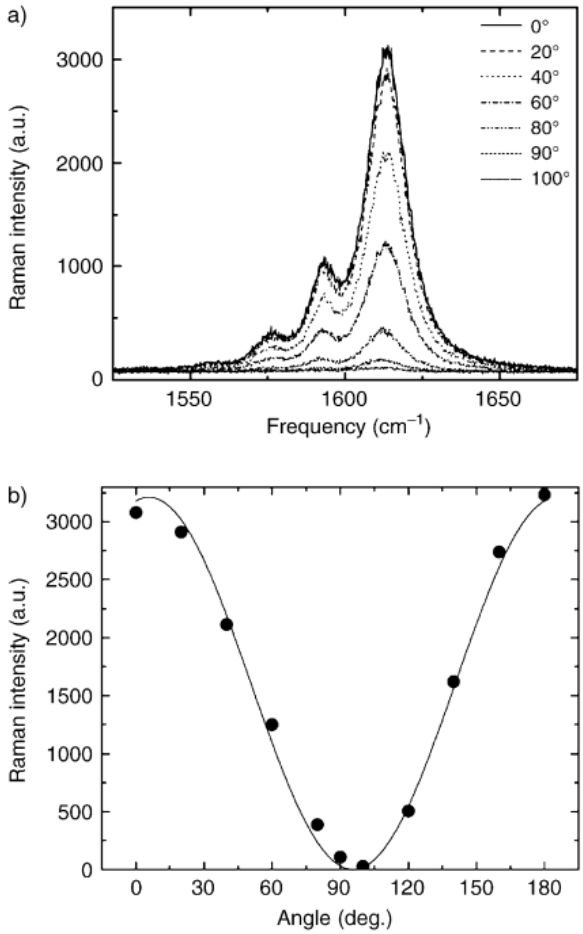

Figure 2.5 (a) Raman spectra of the tangential mode (G line) of an individual SWNT for various angles, between the polarization of incident laser beam and the tube axis. (b) Angular dependence of the Raman intensity at 1614 cm^{-1}. The solid line corresponds to a

$\cos^2(\alpha)$ form. The Raman signal reaches a maximum when the laser beam is polarized along the tube.

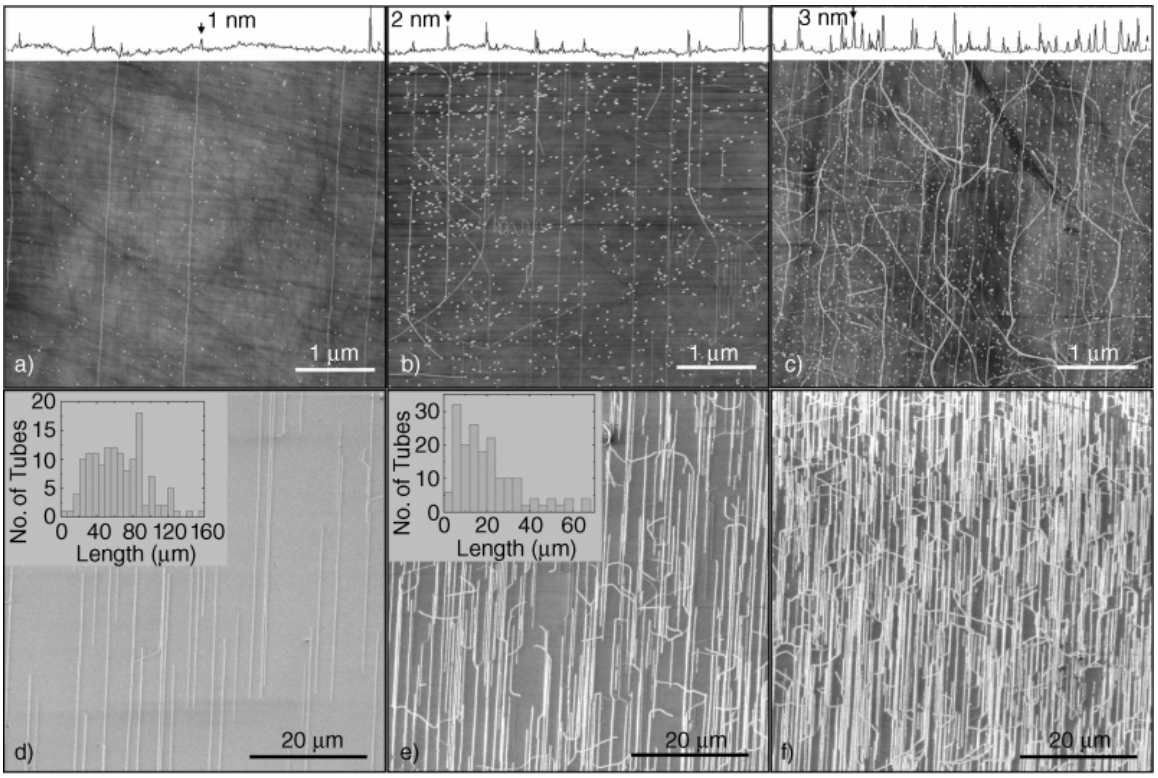

Figure 2.6 AFM images of aligned SWNTs grown on single crystal quartz substrates using different densities of catalyst particles (a-c). Large area SEM images of tubes grown in this fashion (d-f). These results indicate a decreasing degree of alignment with increasing tube density.

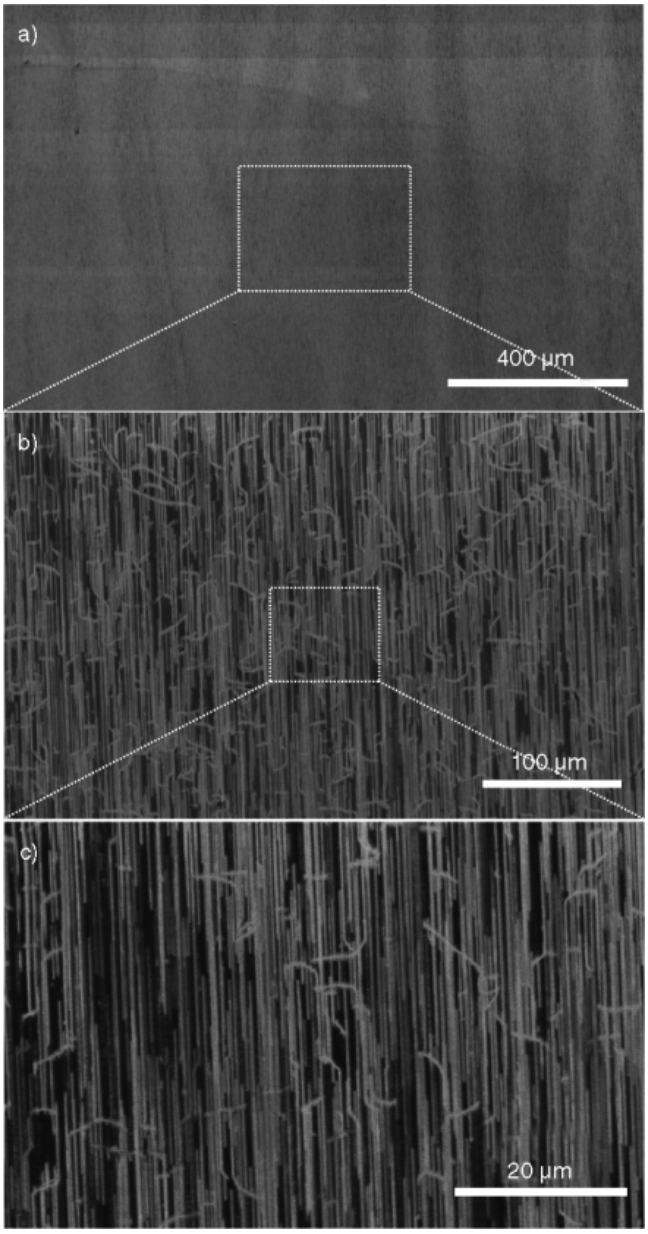

Figure 2.7 (a-c) SEM images of high density aligned tubes for different magnification. These images show that aligned SWNT are homogenous over large areas.

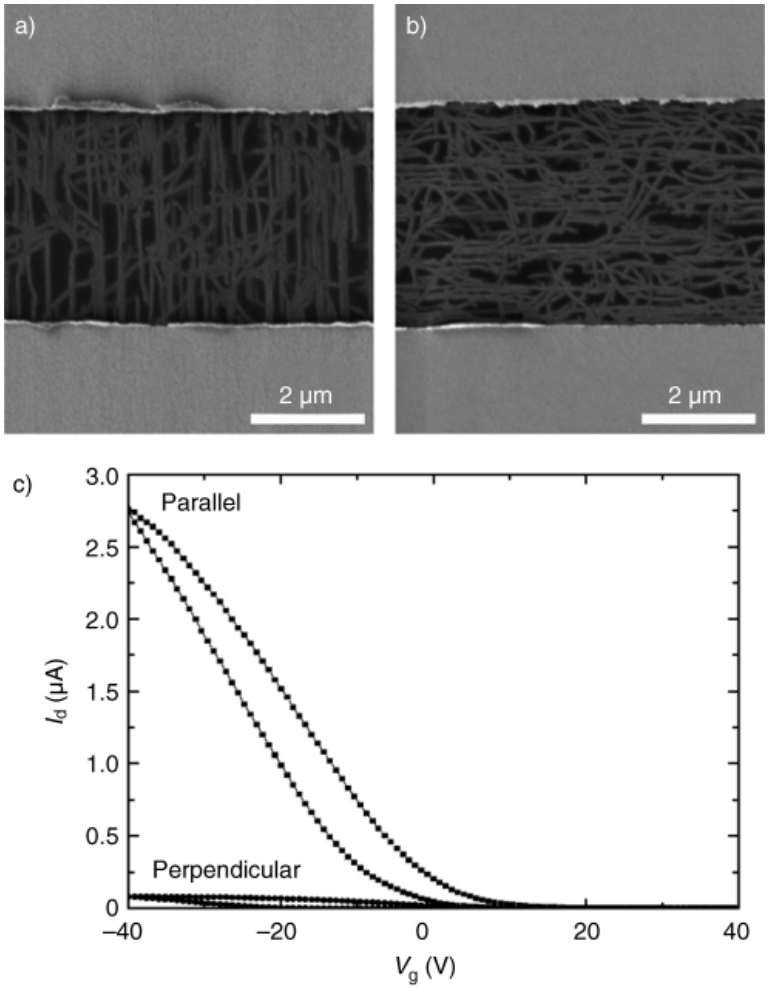

Figure 2.8 (a-b) SEM images of channel regions of TFT devices that have their channels (5 μm channel lengths) aligned parallel and perpendicular to the orientation of the aligned SWNTs, respectively. (c) Current/voltage response of thin film transistors with 100 μm channel length and 250 μm channel width, oriented parallel and perpendicular to the direction of alignment in arrays of SWNTs. The bias voltage V_D is 0.5 V. The aligned SWNTs behave like a highly anisotropic thin film. Device mobilities as high as 125 cm^2/Vs, corresponding to 'per tube' mobilities of ~9000 cm^2/Vs, can be observed in devices of this type.

CHAPTER 3 PATTERNED CATALYST TECHNIQUE

This chapter was published as "Spatially Selective Guided Growth of High Coverage Arrays and Random Networks of Single Walled Carbon Nanotubes and Their Integration into Electronic Devices **Coskun Kocabas,** Moonsub Shim and John A. Rogers, *J. Am. Chem. Soc. , 128, 4540 (2006).*

3.1 Introduction

Thin films of single-walled carbon nanotubes (SWNTs) can provide semiconducting and/or conducting components of passive and active (e.g. transistors) electronic devices (1-4). Potential applications range from large area, mechanically flexible systems, where semiconducting SWNT films could provide advantages over conventional small molecule or polymer semiconductors, to high performance devices, where they could provide alternatives to large grained polysilicon or even single crystal silicon. For the former class of application, random networks of SWNT might offer sufficient performance. For the latter, densely packed aligned arrays of SWNT are preferred. Forming such arrays, patterning their coverage and, possibly, interfacing them with SWNT networks represent significant experimental challenges. Modest degrees of alignment and coverage can be achieved by controlled deposition of SWNTs from solution suspensions (5, 6) or by specialized growth methods (7,8). A new technique for generating arrays uses chemical vapor deposition (CVD) of SWNTs on single crystal substrates of sapphire (9,10) or quartz (11). Optimized CVD growth on quartz can yield well aligned arrays over large areas and with coverages up to 1 SWNTs/micron. The coverage can be increased beyond this level, but only at the expense of degraded alignment, due possibly to detrimental effects of interactions between growing SWNTs and unreacted catalyst particles. We report here a method that avoids these problems by spatially patterning the catalyst. The strategy yields perfectly aligned, high coverage arrays of SWNTs, in well defined geometries; it can also, in the same growth step, produce dense, random networks of SWNTs self-aligned and electrically interfaced to

these arrays. The geometries of these SWNT films enable their easy integration into high performance, planar device.

3.2 Materials and Method

Figure 3.1 illustrates the experimental approach. The susbtrates were ST-cut quartz obtained from Hoffman Materials Inc. and subsequently annealed for 8 hours at 900^0 C in air. Deep ultraviolet photolithography defined openings (e.g. two square regions as in Figure 3.1) in 400 nm thick polymethylmethacrylate (PMMA) photoresist (MicroChem, 495PMMA). Spin casting ferritin diluted 1:20 (v/v) with deionized water deposited catalyst on the PMMA and the exposed regions of the quartz. Washing with acetone, isopropyl alcohol and DI water removed the PMMA and produced a bare quartz substrate with catalyst located in regions corresponding to the patterned openings in the PMMA. The ferritin was sufficiently well adhered to the quartz that most or all of it remained during the steps to remove the PMMA. The deposition conditions (i.e. catalyst concentrations and spin speeds) defined the number of catalyst per unit area in these regions. (The deposition conditions will lead to some degree of non-uniformity in the distribution of catalyst within the patterned regions.) Heating the substrate at 900 ^{o}C for 10 min oxidized the catalyst. Cooling to room temperature and then heating to 900 ^{o}C in a hydrogen environment reduced the catalyst. Purging with hydrogen at 900 ^{o}C for 1 min and then introducing a flow of methane (2500 standard cubic centimeters per minute (sccm)) and hydrogen (75 sccm) at 900 ^{o}C for 10 min led to the growth of SWNTs. High density random networks of SWNTs formed in the regions of the catalyst, which is present at high coverage for the cases examined here. Nearly perfectly aligned SWNT emerged from these regions along directions of preferred growth on the quartz, as illustrated schematically in Figure 3.1 and described in more detail below. Preferential growth drection is along [2-1-10] crystographic direction of single cystal quartz [11].

3.3 Results and Discussion

Figure 3.2 presents scanning electron and atomic force micrographs (SEMs and AFMs, respectively) of representative results. In the regions with catalyst, the SWNTs (diameters in the range between 0.5 and 3 nm) adopt a nearly random network geometry, consistent with our previous results with uniformly deposited catalyst at comparable

coverages. (Supporting Information) The low degree of alignment in this case is likely due to adverse effects of unreacted catalyst particles (~90% of the catalyst does not react to form SWNTs) that coat the growth surface. In the absence of these particles, the SWNTs prefer to grow in an aligned geometry. The results of growth with patterned catalyst, as illustrated in Figure 3.2, are consistent with this expectation. In particular, nearly perfectly aligned, high coverage arrays of SWNTs emerge, at angles along the preferred growth direction, from the edges of random networks in the patterned regions. Figure 3.2(a) provides an SEM image of an edge (dashed line) between a region of the substrate with (top) and without (bottom) catalyst. This effect can be exploited to obtain large area, high coverage aligned arrays of tubes: stripes of high coverage regions of ferritin are patterned with orientations perpendicular to the SWNT growth direction. Figure 3.2(b-d) illustrate the results of this approach. These levels of coverage (~4 SWNT/micron) and alignment (99% of the SWNTs between the catalyst stripes lie within ~1 degree of the preferred growth direction) significantly exceeded those that we were able to obtain with unpatterned catalyst. Figure 3.3 illustrates the density scaling of SWNT array. Tube density can be changed by controlling catalyst concentration and/or growth conditions which affect the catalyst yield.

Patterned catalyst on quartz substrates also enables formation, in a single step, of high coverage random networks of SWNTs self-aligned with, and electrically interfaced to, the arrays. Such arrangements of SWNTs are important for classes of transistors and other devices that use networks and arrays for the conducting and semiconducting elements, respectively. Figure 3.4 presents SEMs that illustrate this type of growth capability, in which aligned SWNTs bridge the gap between large pads of random networks. Relatively few SWNTs emerge from edges of the pads that lie along the direction of preferred growth (Figure 3.4(d)), consistent with a strong driving force for alignment. Figure 3.5 shows some SEM images with catalyst pattern oriented at a shallow angle relative to the preferred growth direction. Even more geometrically elaborate structures of aligned and network SWNTs are possible. Figure 3.6 demonstrates aligned SWNTs grown from more complex catalyst pattern. .

To demonstrate the possibility of using such arrangements of SWNTs for transistors, we deposited 1 μm thick layer of a photo-definable benzocyclobutene (BCB,

Dow Chemical) on top of SWNTs in geometries similar to those in Figure 3.4 to form a gate dielectric, followed by 2/50 nm of Ti/Au to form a gate electrode. The resulting devices behave like transistors in which the networks form the source/drain electrodes and the arrays form the channel, when the gate electrode overlaps only the channel region. Figure 3.4(e) shows transfer of characteristics for devices with channel lengths and widths of 100 and 200 μm, respectively; the gates in these cases overlap both the channel and parts of the network electrodes (Vd= 5 V). Because metallic SWNTs are present, the ratios of on and off currents are less than 10 (black curve in Figure 3.4 (e)). High on/off ration ~1000 can be obtained using low density SWNT electrode (red curve in Figure 3.4(e) and curves in in Figure 3.4(f), although in this case gate modulation of the network based electrodes contribute to the response. Selective removal of metallic tubes in the channel, by procedures such as electrical burnout or chemical functionalization, can be used to improve these types of devices.

3.4 Conclusion

In summary, this chapter introduces new capabilities for creating arrangements of SWNTs that could be useful for application in thin film electronics. These techniques complement other reported approaches, and may facilitate the use of SWNTs in practical devices

3.5 References

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3.6 Figures

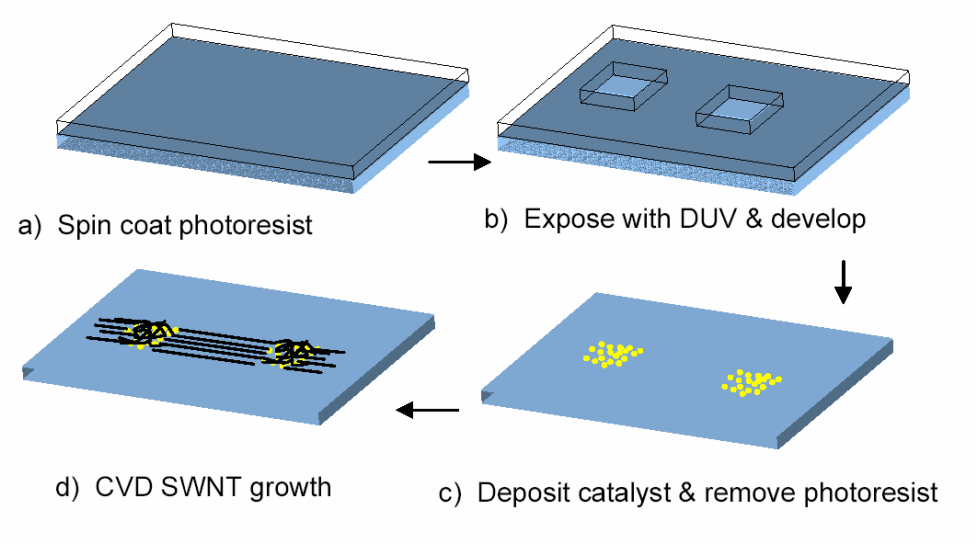

Figure 3.1 Schematic illustration of the steps for generating self aligned patterns of dense arrays and random networks of single walled carbon nanotubes. The approach uses CVD growth on ST cut single crystal quartz with patterned ferritin catalyst. Preferential growth direction is along [2-1-10] crystographic driection.

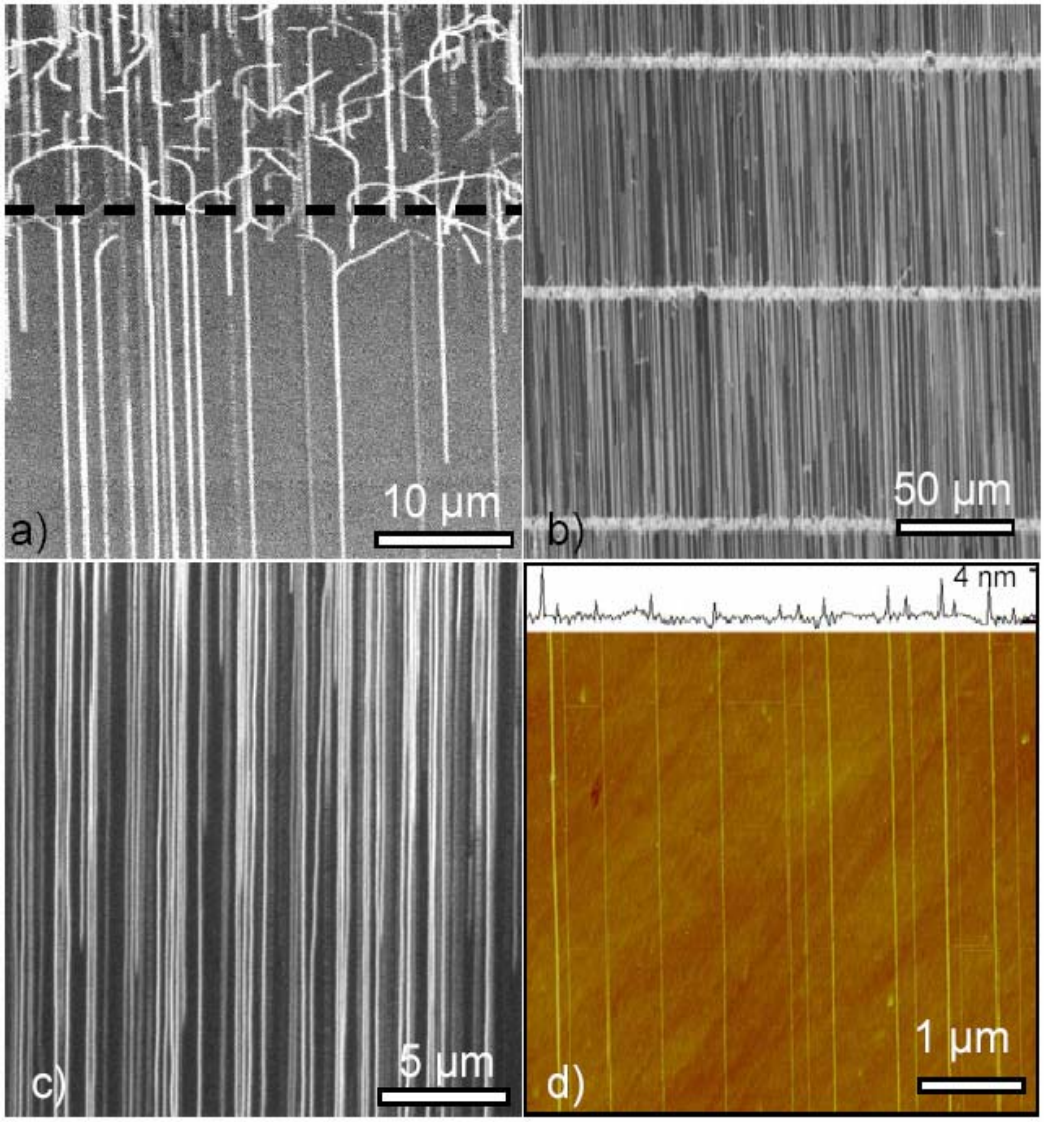

Figure 3.2 Images of SWNTs grown using patterned ferritin catalysts on ST-cut quartz substrates. a) SEM collected near an edge (dashed black line) between a region with (top) and without (bottom) catalyst. b) Nearly perfectly aligned arrays of SWNT with high coverage formed using patterned stripes of catalyst oriented perpendicular to the preferred growth direction. c), d) SEM and AFM images, respectively, of aligned tubes from this same substrate.

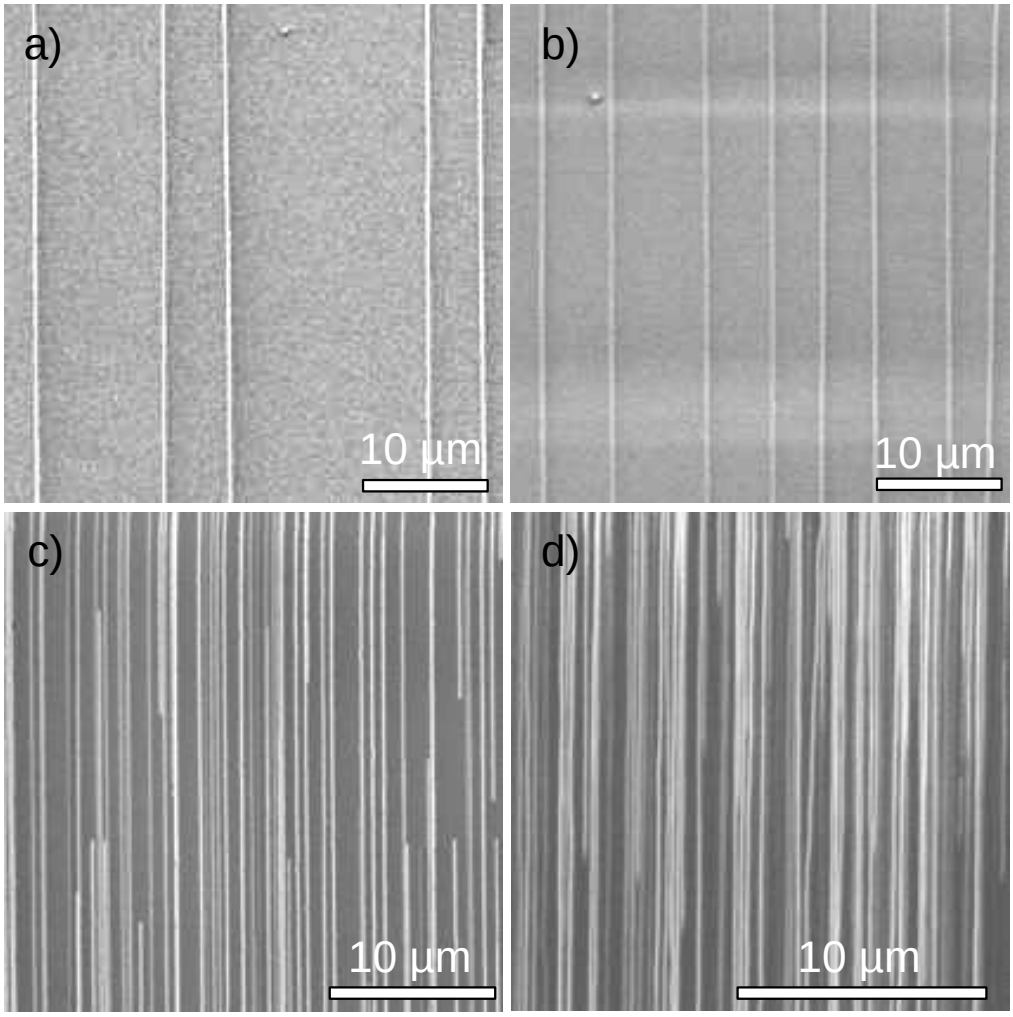

Figure 3.3 SEM images of aligned SWNTs grown on quartz substrates by use of patterned ferritin catalysts. These images were collected away from the regions of catalyst for cases of low (a), moderate (b), high (c) and very high (d) concentrations of catalyst. In this case, unlike the case of unpatterned catalyst, the degree of alignment does not depend (or depends only very weakly) on the coverage of the catalyst or the SWNTs.

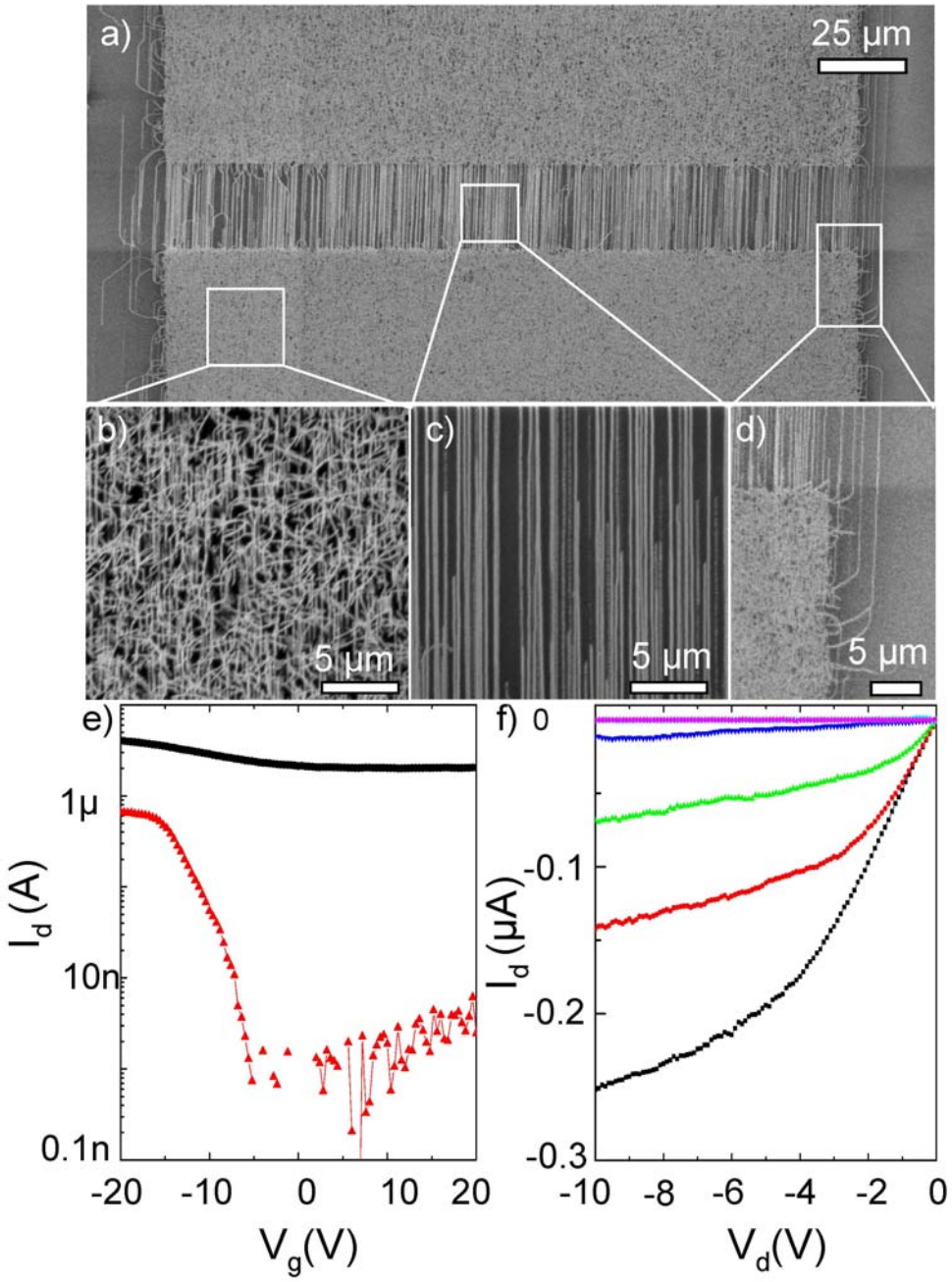

Figure 3.4 SEM images of SWNT grown using catalyst particles patterned in two square regions to form an arrangement of SWNTs suitable for use in a thin film type transistor. a) SWNT network 'electrodes' connected by a 'channel' of aligned SWNTs. b), (c) Electrode and channel regions, respectively. d) Corner of an electrode illustrating the preferential growth. Transfer (e) and output (f) characteristics of transistors that use

random networks of SWNTs as the source and drain electrodes and aligned arrays of SWNTs as the semiconducting channel. Vg: -20 to 0 V from the bottom.

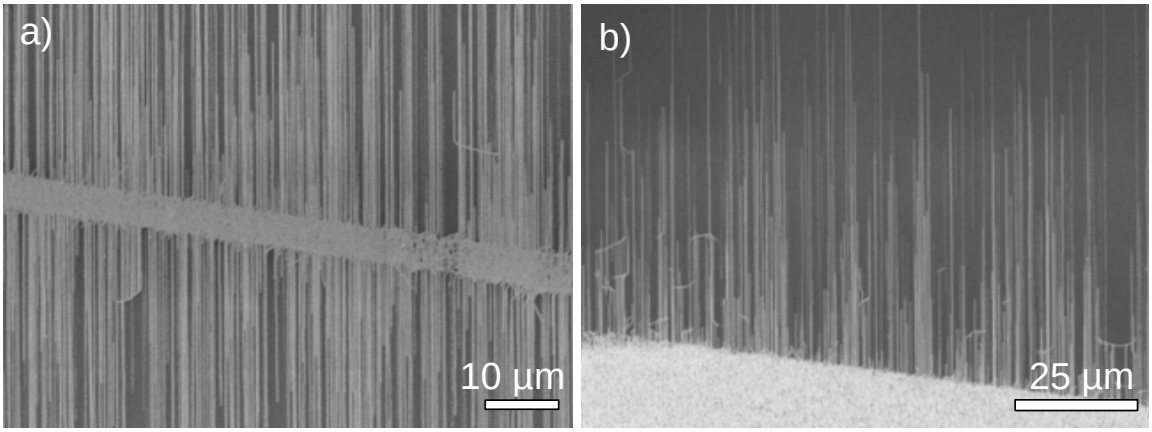

Figure 3.5 SEM image of SWNTs grown on a quartz substrate using a stripe pattern of ferritin catalyst oriented at a shallow angle relative to the preferred growth direction. The SWNTs emerge from the patterned catalyst with orientations along this preferred direction.

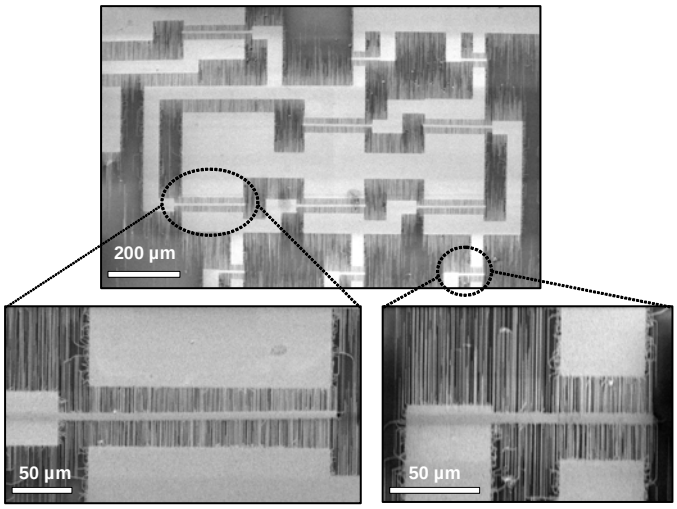

Figure 3.6 SEM images of a complex arrangement of random networks and aligned arrays of SWNTs, formed by using patterned ferritin catalyst and CVD growth on a quartz substrate. The bright white regions correspond to high coverage random networks of SWNTs.

CHAPTER 4 OPTIMIZED SYNTHESIS OF ALIGNED ARRAYS OF SWNT

Significant portion of this chapter is submitted for publication in *J. Phys. Chem. B* as "Improved Synthesis of Aligned Arrays of Single Walled Carbon Nanotubes and Their Implementation in Thin Film Type Transistors **Coskun Kocabas**, Seong Jun Kang, Taner Ozel, Moonsub Shim, John A. Rogers*"*. Reproduced (or 'Reproduced in part') with permission from *J. Phys. Chem. B*, in press (or 'submitted for publication'). Unpublished work copyright 2007 American Chemical Society.

4.1 Introduction

Benchmarking studies of the transport properties of semiconducting single walled carbon nanotubes (SWNTs) indicate certain important advantages compared to single crystal silicon in both bulk wafer and nanowire structural forms (1-3). These findings together with promising demonstrations of SWNTs as active elements in sensors (4-6), optoelectronic devices (7), transparent conductors (8) and thin film electronics (9-12) create interest in the development of scalable means for integrating SWNTs into devices, circuits and systems (13-21). One strategy involves the formation of effective conducting or semiconducting thin films that consist of random networks (9,22) or well aligned arrays of SWNTs (23-26). The large number of SWNTs that are active in devices (e.g. transistors) formed with such 'films' enables high current outputs, with statistical averaging effects that provide good device-to-device uniformity in properties even with SWNTs that are electronically heterogeneous (17). The aligned arrays have advantages compared to the random networks because they avoid percolation transport pathways (11,12,27), unusual scaling of device properties (28), tube/tube junction resistances and other features that might be undesirable for many applications (29). Achieving the ideal configuration of perfectly aligned horizontal arrays of perfectly linear SWNTs at high but sub-monolayer densities, as measured by the number of SWNTs per micron, represents a significant experimental challenge. Nevertheless, methods that use guided chemical vapor deposition (CVD) growth of SWNTs on certain types of single crystal substrates (22-26) appear promising, particularly when implemented with strategically designed patterns of catalyst (24). This paper presents a range of results on SWNT arrays formed using optimized implementations of procedures of this type, as well as the electrical and

scaling properties of thin film transistor devices that are constructed with them. The extremely high quality of the arrays, the ease with which they can be integrated into devices and the excellent performance that can be achieved suggest that these approaches have the potential to provide a realistic pathway to SWNT based electronics and optoelectronics, sensors and other systems.

4.2 Methods and Materials

For growth of the arrays, we start with recently reported procedures that use CVD of SWNTs on thermally annealed quartz substrates. The basic alignment mechanism in this system is thought to involve preferential growth along step edges (30) and/or along certain crystallographic directions due to orientationally anisotropic interaction energies between the tubes and the quartz (26). When the catalyst is uniformly distributed on the substrate at moderately low densities (i.e.~10 particles/μm^2), the growth can yield extremely linear, well aligned and long tubes but at low densities (~ 0.2 SWNT / μm)(23). Many applications, however, demand much higher densities, preferably approaching a full monolayer. (Multilayer arrangements can frustrate field effect current modulation in thin film transistors.) Increasing the catalyst density increases the tube density, but with reductions in the average tube length, degree of alignment and linearity in the shape (24). These effects are thought to be due to unwanted interactions between unreacted catalyst particles and growing SWNTs. Patterning the catalyst into strategic locations (e.g. stripes oriented perpendicular to the preferred growth direction) avoids this problem and provides a means for increasing the SWNT coverage while maintaining the alignment, length and linear geometries (24).

This chapter introduces important improvements in this basic approach, including optimized annealing conditions for the quartz, processing methods that eliminate residue from the substrate surfaces, high density catalyst stripes formed from evaporated sub-monolayer films of iron, ethanol for the feed gas, and well controlled temperature of the substrate. These procedures yield arrays of SWNT with levels of perfection that are orders of magnitude better than previously reported results (23-26), with coverages that are also substantially higher.

4.2.1 Optimized Growth Process

Figure 4.1(a-b) shows scanning electron microscope (SEM) images of representative aligned arrays of SWNTs grown using these optimized approaches. The substrate was a ST-cut single crystal quartz wafer (31), annealed in air at 900 ^{o}C for 8 hours prior to growth. Isolated lines of catalyst on quartz were prepared by photolithographically patterning iron deposited by physical vapor deposition. In particular, the catalyst consisted of an ultrathin film (0.1-0.2 nm) of Fe uniformly deposited by electron beam evaporation (Temescal BJD1800) onto a photolithographically patterned layer of photoresist (AZ5214) on the quartz. After removing the photoresist with acetone and stripper (AZ Kwik stripper), samples were annealed at 900 ^{o}C for 1.5 h to form isolated FeO nanoparticles. The widths and spacings of the stripes patterned by photolithography that defined the spatial extent of these nanoparticles were 10 μm and 100 μm, respectively. The chemical vapor deposition process began with flushing the chamber with a high flow rate of Ar (3000 sccm) for 2 min and then heating the furnace to 925 ^{o}C while flowing H_2 (300 sccm). After stabilizing the temperature, flows of both H_2 and Ar were set to 8 sccm. Growth of SWNTs occurred by passing these gases through an ethanol bubbler held a 0 ^{o}C in a water bath chiller prior to entry into the chamber. Growth was terminated after 20 min, and the chamber was then cooled in H_2 and Ar flow. We estimate the growth rate of aligned SWNT formed in this manner to be between 0.5-2.5 μm/sec, consistent with previous reports for unaligned SWNTs grown by CVD on amorphous substrates (32,33).

4.2.2 Characterization of SWNT Array

As shown in Figure 4.1a-b, the degree of alignment and linearity in the SWNT arrays can be extremely high. In particular, the percentage alignment, as measured using the total summed lengths of SWNT segments oriented along the preferred growth direction and of those oriented along any other direction, is reproducibly >99.9%. The degree of linearity is also exceptionally high, as illustrated in Figure 1a-b. For a typical tube shown in Figure 4.1c, for example, the maximum spatial deviation from a perfectly linear shape is ~ 5 nm along lengths of ~5 μm. This level of deviation is comparable to the uncertainty in determining the location of a tube by fitting the convolved height

profile obtained with our atomic force microscope (AFM; DimensionV, Digital Ins.) equipped with a standard tip (radius of curvature ~20 nm). Figure 4.1d shows an AFM image of catalyst particles form from 0.2nm evaporated iron film. Based on AFM measurements in the regions of the catalyst, the average size of the iron oxide nanoparticles is 1.8nm, as indicated in the histogram of Figure 4.1e presents the distribution of tube diameters, evaluated by AFM. The mean (~1.2 nm) and the range of diameters (0.4 to 4 nm) is similar compared to SWNTs grown using conventional CVD approaches. The degree of alignment and linearity do not depend on diameter, for this range. The average densities of the arrays can be as high as 5-10 SWNT/ μm. Figure 4.2 provides more information about the SWNT array. The growth process reported here provides very repeatable results. Figure 4.3 shows different magnification SEM micrograph of SWNT arrays from 5 different samples grown at the same time. The variation of the tube density from sample to sample is likely due to the position inside the CVD chamber.

The average tube density is typically around 5-10 SWNT/ μm. At some areas, the tube density could be as high as 50 SWNT/ μm. Figure 4.4 shows an AFM image of SWNTs separated by a distance of ~15nm. These results suggest that uniform densities at this level, and perhaps higher, are possible, with suitable optimization. Increasing the thickness of the Fe catalyst film, the flow rate of the ethanol and other procedures designed to increase the density further typically lead to the formation of bundles and growth vertically, out of the plane of the substrate in the regions of the catalyst. Further work, and perhaps different strategies, will be required to improve the densities to values substantially higher than those introduced here. The separation distance between the lines of catalyst limits the lengths of the SWNTs in the arrays of Figure 4.1. Growth from an isolated catalyst line reveals the length distribution when the growth is not limited by structures on the substrate. Figure 4.5 shows some results. The average length is ~300 μm, with some tubes that are as long as 1 mm. We observed that several factors influence the length. First, photoresist residue and high flow rates result in amorphous carbon formation and the early termination of growth. Second, growth temperatures (925-930 ^{o}C) that are somewhat higher than those reported previously, improves substantially the yield (i.e. the density) as well as the lengths. Third, cooling the ethanol

bubbler (0 ^{o}C) reduces the vapor pressure of ethanol and allows improved control over its concentration in the chamber, thereby enabling the prevention of amorphous carbon formation.

4.2.3 Growing Millimeter Long SWNT

There are couples of mechanisms for growth termination. Depending on tip or base growth, termination mechanism could be different. The growth mechanism with Fe catalyst on quartz is not known clearly. If we assume that it is base-growth, SWNT should overcome the van der Waals forces between the tube and substrate. When tubes reaches a critical length, driving force of the growth can not overcome the van der Waals forces as a result growth will be terminated. Interestingly most of the tubes stop growing around the same length (~200-300 μm). This can be an evidence for base-growth. If we assume the growth is tip-growth, termination mechanism should be related with the activation of the catalyst particles. Amorphous carbon formation on the catalyst can stop the growth. The life time of the active catalyst determines the length of the tube.

The long lengths and the relatively large separations between the ends of long tubes like those in Figure 4.5 allow Raman spectroscopy to be performed on individual aligned tubes in the array. Such information can provide valuable insights into the uniformity of the dimensions and chirality of a single tube along its length. The measurements used a confocal instrument (Jobin–Yvon) and a 100X microscope objective to focus the excitation laser (He-Ne, 632 nm wavelength; ~1 μm spot size; $5x10^5$ W/cm^2 power density). The backscattered Raman signal was collected through a 50-μm pinhole. Figure 4.5(c) shows results of a single point measurement on a typical SWNT. The two Raman peaks around 127 cm^{-1} and 205 cm^{-1} are due to quartz. The peak at 144 cm^{-1} is the radial breading mode (RBM) of the SWNT, which is related to the diameter of the tube. Figure 4.5(d) presents the frequency of the RBM as a function of position along the length of this tube. The results indicate a position independent value of 144 ± 0.5 cm^{-1} for the 50 μm length examined here. The variation in frequency is within the spectral resolution of the spectrometer is (~0.5 cm^{-1}). These data suggest that the diameter (~1.7nm) of the tubes in the arrays, for the cases that we examined, do not change during the growth process, consistent also with AFM measurements.

Isolated lines of catalyst provide SWNT layouts convenient for studies such as those described above. The ability to define the locations and spatial layouts of the catalyst sites into other geometries can be important for applications that require unusual arrangements of aligned tubes, or the integration of these aligned tubes with random networks of tubes. Figure 4.6 shows SEM images of some representative examples, including 'wavy' line patterns (Figure 4.6a), arrays of disks (Figure 4.6b), and complex circuit-like structures (Figure 4.6c). The bright white regions correspond to high coverage random networks of SWNTs that grow in the areas where catalyst is present. These networks have densities ~100 SWNT / μm and sheet resistances of ~250 Ω/sq, suitable for use as transparent, tube-based interconnects between the aligned arrays of SWNTs. The results of Figure 4.6b and Figure 4.6c also illustrate clearly that the direction of gas flow is unimportant in determining the alignment in this process: aligned tubes grow equally well in directions that are different by 180 degrees.

4.2.4 Crystal Structure of Quartz

In this section I will report control experiments which provide some inside about the alignment mechanism. First of all, I will introduce the crystal structure of quartz. Quartz, the crystal form of silica (SiO2), is one of the most abundant mineral in Earth. Quartz has rhombohedral crystal system which three fold symmetry along c axis [0001]. Figure 4.7 shows the structure of quartz. The unit cell parameters of quartz are a=4.91Å and c=5.4 Å. The average Si-O bond length and Si-O-Si linking angle are 1.607Å and 144.4^{o}, respectively (34). Quartz has high temperature polymorph known as cristobalite or β-quartz. β-quartz has 6 fold symmetry around c axis [0001] and it has center of symmetry. α-quartz transforms to β-quartz after 573^{o}C at atmospheric pressure(35,36). More detailed information about α and β-quartz can be found in reference 4.

Quartz crystal can be described as three dimensional polymer of tetrahedral (SiO_4) by sharing the corner oxygen atoms (Figure 4.8). Quartz has tendency to form fiber along polar axis (36). The polar axis of quartz is along [1 1 -2 0] direction which is also known as the main axis of quartz. There are three identical polar axis on the basal plane. Along this direction there are chains of Si-O-Si linkages. The Si-O bond is a covalent bond with effective charge of 2e for Si and –e for O (33,37). Therefore electric dipole moment of Si-O bond is around 3.84 Debye.

Contact angle of water on a surface can be measured from the angle between liquid and gas phase at the point where solid liquid and gas meet. Contact angle of water on a surface depends on the surface and interface energy and also about the surface termination. Figure 4.9 shows the schematics of the contact angle setup. Quartz surface has very high affinity to water molecules. The high water affinity is originated from hydrophilic surface silanol groups –Si-(OH)-Si(OH). Heating the quartz above 300^{o}C removes hydrogen and forms siloxane groups Si-O-Si (39). When quartz surface is exposed to air, a monolayer of water molecules form on the surface. We have tested three different surface treatment techniques to change the surface chemistry of the quartz.

First one is annealing at high temperature (900^{o}C). As received quartz wafers has hydrophobic surface with contact angle of ~10^{o}. After high temperature annealing, surface become hydrophobic and contact angle increases to 50^{o}. The degree of alignment is also influenced by annealing of the quartz before tube growth. Figure 2.4a-c show results obtained with substrates annealed at 900^{0}C for 10 min., 4 hours and 7 hours. As received quartz wafers were polished using mechanical and chemical processes. These process induces thin (<1nm) amorphous layer of SiO_2. High temperature annealing can recover the quartz surface. Figure 4.11 shows cross sectional TEM images of unannealed and annealed quartz surface. Thin amorphous layer can be seen on unannealed quartz surface, and this amorhous layer disappears after high temperature annealing.

Second technique is reactive ion etching with oxygen plasma. Oxygen plasma can effect the quartz surface by changing the surface termination to silanol groups –Si-(OH)-Si(OH) or by damaging the crystal structure of quartz resulting in a thin amorphous SiO2 layer. RIE treatment changes the hydrophobic surface (θ_c=50^{o}) to hydrophilic surface(θ_c=10^{o}). Figure 4.12 shows SEM images of SWNT grown on quartz surface after exposing RIE. During RIE process, some area on the surface is protected by pattered photoresist. Aligned SWNTs that enter the RIE exposed area lose alignment and grow in random directions. The SWNTs regain their alignment after emerging on the other side of the unexposed area.

Third technique is the ozone treatment using a UV lamp. Similar to the RIE, after ozone treatment, quartz surface will be terminated with silanol groups which makes the surface hydrophilic (θ_c=10^{o}). Figure 4.13 shows the SWNT grown on quartz surfaces

threaded with ozone . It is clearly seen that the degree of alignment is very poor after the ozone treatment. These observations are consistent with other reports (37- 39) and can be explained by surface termination mechanism.

The degree of alignment depends on the surface quality and cleanness of the quartz surface. Contamination or coating on the surface affects the alignment. To illustrate this effect, we grew SWNT on quartz with a patterned layer of amorphous SiO_2 (~2 nm thickness) deposited by electron beam evaporation. Figure 4.14 shows schematic illustrations of this system, together with SEM views of SWNTs grown on this type of substrate. Aligned SWNTs that enter the SiO_2 coated area lose alignment and grow in random directions. The SWNTs regain their alignment after emerging on the other side of the uncoated area. Some of the SWNT (Figure 4.14c) stop at the interface of SiO_2 pattern, perhaps due to the small surface relief associated with this layer. These observations suggest that the SWNTs grown while in intimate contact with the quartz, which is quite different than the growth mechanisms typically observed on amorphous substrates.

4.2.5 Rearrangement of SWNT on Quartz Surface

In general, we do not observe affects of gas flow on SWNT alignment. Nevertheless, in rare instances near the very edge of the sample, gas flow can be important, perhaps due to high peak flow rates associated with turbulence in these regions. In these cases, the interplay between gas flow and quartz induced alignment occurs. When the SWNT touches the quartz surface, it orients along the [2-1-10] direction. Figure 6a shows different configurations of the SWNTs on quartz surface. The SWNT along the blue arrow (shows X-axis) is aligned due to SWNT-lattice interaction and the SWNT along the red arrow (indicating the flow direction) is aligned because of gas flow. The result is an unusual zigzag shape (Figure 4.15b, Figure 4.15c).

4.2.6 Growing SWNT on Different Quartz Surfaces

Studies of SWNT growth on quartz substrates with different cuts can provide additional insights into the alignment mechanisms. Quartz crystal has a hexagonal crystal structure, which belongs to rhombohedral crystal system. The alignment direction [2-1-10] is known as the main axis (X axis) of quartz. The basal plane (0001), has three

fold symmetry. We examined growth on three different quartz surfaces; Y-cut (0010), Z-cut (0001) and X-cut (2-1-10), each of which has a different orientation with respect to the alignment axis. Figure 4.16a-Figure 4.16 c show top views of a space filling model of Y-cut (0010), Z-cut (0001) and X-cut (2-1-10) quartz, respectively. Figure 4.16d-Figure 4.16f show the orientation of wafers with respect to main crystal axis. Scanning electron micrographs of SWNT grown on these wafers are shown in Figure 4.16g-Figure 4.16i. On Y-cut substrates, we observed alignment of SWNTs along X-axis (Figure 4.16g), consistent with other results presented here and previously. On Z-cut wafers, which has three fold symmetry, we observed three alignment directions, along three identical X-axis (Figure 4.16h). On the other hand, on X-cut wafer, we did not observe any alignment (Figure 4.16). These observations indicate that SWNT prefer [2-1-10] direction. Strong anisotropic interaction is likely due to the arrangement of Si and O atoms. It is important to note that the piezoelectric effect in quartz is also observed along the X-axis.

4.2.7 Top Gated Thin Film Transistor on SWNT

One area of application for arrays such as these is in electronics. To explore these possibilities, we fabricated top gated transistors that use the aligned SWNT arrays for the semiconducting channel, using recently reported procedures (46) but with different materials for the gate dielectrics, as discussed subsequently. For the device examples in Figure 4.17, the fabrication began with growth of aligned SWNTs using 10 μm wide catalyst lines separated by 100 μm. Photolithography (AZ 5124) followed by uniform electron beam evaporation of Ti (1 nm), Pd (25 nm) and removal of the resist defined source and drain electrodes, with the gaps between them aligned to the parts of the susbtrates that do not include the patterned catalyst lines. After another photolithography step to protect the region between these electrodes, O_2 reactive ion etching (200 mTorr, 100 W) removed all of the exposed SWNTs to yield electrically isolated the devices. A hydrogen silsesquioxane (HSQ, Fox-12; Dow Corning) formed the gate dielectric. Spin coating (6000 rpm, 30 s) a precursor to this material and then baking (220 ^{o}C for 10 min) created a uniform, 80 nm thick nano-porous layer. An advantage of HSQ is its excellent ability to conform to and planarize the underlying topography associated with the tubes

and the source and drain electrodes. Even very thin ~30 nm layers could be used effectively. The gate electrode (Ti, 1 nm; Au, 25 nm) was defined on top of the HSQ by photolithography and liftoff. Figure 4.17(a) gives a schematic illustration of a device. Figure 8(b) shows the atomic structure of the dielectric and its integration with a SWNT. Imaging by SEM before depositing the gate dielectric and gate reveals the layout of the channel region of the device, as illustrated in Figure 4.17c). The variation in source/drain current (I_d) as a function of gate voltage (V_g) at a source/drain bias (V_d) of 0.5 V appears in Figure 8(d) for a device with 5 μm and 200 μm channel length (L_c) and width (W), respectively. The density of the array is ~5 SWNT/μm. This device, then, involves the parallel operation of ~1000 individual SWNTs. The large output currents (i.e. mA) are consistent with this device design. The moderate ratio of currents in the on and off states results from the large numbers (~300) of metallic tubes that span the source and drain electrodes. The hysteresis observed in Figure 4.17(d) is characteristic of nanotube devices that operate at gate voltages larger than ~5 V. The hysteresis with the HSQ material, notably, is smaller, at comparable gate fields, than that observed with other materials. The reason for low hysteresis could be related to the porosity of HSQ materials and high curing temperature (220^{o}C). The detailed mechanisms for hysteresis in nanotube devices have been studied by other groups (41), and remains a topic of current research

Figure 4.18 shows additional data from devices of this type. In particular, Figure 4.18(a) and (b) show the scaling of device properties with channel length (L_c). As expected, both the on and off currents (I_{on} and I_{off}, respectively) increase with decreasing channel length. The rate of increase is slightly less, however, than a $1/L_c$ scaling, likely due to the increasing relative role of contacts with decreasing L_c.

4.2.8 Field Effect Mobility of SWNT Array

The linear regime mobilities can be calculated in several different ways. We define the effective field-effect mobility of the TFT device as

$$\mu_d = \frac{L}{V_d C W} \cdot \frac{dI}{dV_g} \qquad (1)$$

where C is the capacitance *per unit area*. The simplest method approximates C as that of a uniform parallel plate capacitor. This estimate has been used in the past in thin

film type SWNT devices (42,43), but it is valid only when the average spacing between adjacent tubes is significantly smaller than the thickness of the gate dielectric. Figure 4.18(d) shows the results of such calculations. We refer to this quantity as the thin film, or device, mobility(40). (Since the effects of contacts are ignored completely in the above expression, the apparent mobility decreases with decreasing channel length.) A more rigorous definition of the mobility relies on explicit calculation of the capacitance coupling between the gate and the array of tubes, including the effects of fringing fields and electrostatic screening. The capacitance can be derived analytically for a uniformly spaced array of SWNTs by a variety of methods(40,42). An approach that uses classical electrostatics with image charge techniques and is applied to the case that the dielectric constant of the gate dielectric is similar to that of the substrate (geometry in Figure 4.17), yields the following expression for the total capacitance per unit area of the SWNT array (40,42):

$$C_{tot} = \frac{Q}{V} = \frac{N\rho}{V} \frac{2\pi\varepsilon_0\varepsilon_r N}{\ln\left(\frac{\sinh(\pi(2t+r)/\Delta L)}{\sinh(\pi r/\Delta L)}\right)} \qquad (2)$$

Where Q is the total charge per unit area of the array, ρ is the linear charge density along a single SWNT in the array, V is the potential difference between a SWNT in the array and the gate electrode, N is the total number of tubes per unit length, ΔL is the distance between the tubes ($\Delta L = 1/N$) in the array, t is the gate dielectric thickness ε_0 is the permittivity of free space, ε_r is the dielectric constant of the gate dielectric and r is the tube diameter. In the limiting cases of low and high densities, Eq. (2) yields expressions consistent with a parallel plate ($C_p = \underset{\Delta L \to 0}{Lim} C_{tot} = \frac{\varepsilon\varepsilon_0}{t}$) and with a single tube ($C_s = \underset{\Delta L \to \infty}{Lim} \frac{C_{tot}}{N} = \frac{2\pi\varepsilon_0\varepsilon_r}{\ln\left(\frac{(2t+r)}{r}\right)}$), respectively, consistent with other reports (40,42,43).

The metallic SWNTs in the array contribute to the device capacitance, but these tubes cannot be modulated with the gate field. The metallic tube capacitance represents a type of intrinsic parasitic capacitance, which can be only by eliminating the metallic tubes and

not, for example, by optimizing the device layout. For mobility calculation we consider two different cases. In the first, since only semiconducting tubes can be modulated by the gate, we include only the capacitance of the semiconducting tubes ($C=N_s.\rho/V$ where N_s is the number of semiconducting tubes per unit length). The mobility calculated with Eq. (1) and this rigorous value of the device capacitance yields a value that is equal to the average single tube mobility. In the second case, we include capacitance contributions from both the metallic and the semiconducting tubes, such that the mobility is equal to 2/3 of single tube mobility. Figure 4.18d shows scaling of the calculated mobility using different capacitance value. The per tube mobilities (~2000 cm^2/Vs) of the semiconducting SWNT inferred from these measurements are in the same range as independent measurements on devices that incorporate individual tubes[17]. Finite element modeling (FEM) reproduces these limits as well as the functional variations between them. Figure 4.18(d) shows the results of mobilities computed with Eq. (1). The values are systematically higher than those estimated with the parallel plate model, as expected. Figure 4.19(a) shows the calculated field distribution and electric filed lines using Eq. (2). Figure 4.19(b) presents the calculated capacitance as a function of dielectric thickness, derived with Eq. (2) and FEM simulation.

4.2.9 All Carbon Nanotube TFT on Flexible Substrate

In addition to devices, such as these, that use SWNTs for the channel, it is possible to combine random networks with aligned arrays to produce all-tube devices. Such designs can yield optically transparent devices with the ability for integration on flexible plastic substrates, for possible applications in flexible heads-up displays and other systems. This type of nanotube approach to transparent thin film transistors could complement recently reported strategies that use inorganic semiconducting and conducting oxides (44). The fabrication for devices presented here began with the patterning of thin (<0.5nm) Fe catalyst into shapes that define the source and drain electrodes, on a quartz substrate. The optimized CVD techniques described previously yielded collections of SWNTs in layouts, qualitatively similar to those shown in Figure 4, from these catalyst patterns. Dense, random networks and aligned arrays of SWNT formed in the areas coated and uncoated with catalyst, respectively. Aligned SWNTs that

emerge from the catalyst areas to grow along the preferred direction on the quartz to connect two random networks. Figure 4.20(a) and Figure 4.20(b) show SEM and AFM images of the networks and arrays, respectively. Transfer printing (45,46) these structures onto thin plastic substrates (PET) coated with layers of indium tin oxide (100 nm; ITO) as the gate electrode and Polyamid (1 μm, polyamic acid, Aldrich) as the gate dielectric formed the final device. The dense random networks of SWNTs serve as the source and drain electrodes. Figure 4.20(c), Figure 4.20(d) provide optical images and schematic illustrations of the final device. Probing these devices by physically contacting the source, drain and gate electrodes using conventional probe tips, reveals their electrical properties (Figure 4.20(e). These devices show mobilities as high as ~240 cm^2/Vs), computed using the parallel plate models for C. The large hysteresis is characteristic of high operationg voltages and thick dielectrics. The relatively high sheet resistances (~250 Ω/sq) of the source and drain electrodes contributes to device resistance and reductions in apparent mobility with channel length.

4.3 Conclusion

In summary, in this chapter, we demonstrate an optimized, reliable CVD process capable of producing large scale arrays of SWNT that offer levels of perfection in alignment and linearity that are orders of magnitude better than previously reported results. Thin film transistors that use these arrays show device level performance that approaches values expected based on the intrinsic properties of the SWNTs, with good device to device uniformity. The array geometry greatly simplifies the integration of SWNT into complex circuits for a range of other applications such as light emitting diodes, photodetectors, chemical sensors, nanoelectromechanical oscillators, and electrically or thermally conductive elements.

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4.5 Figures

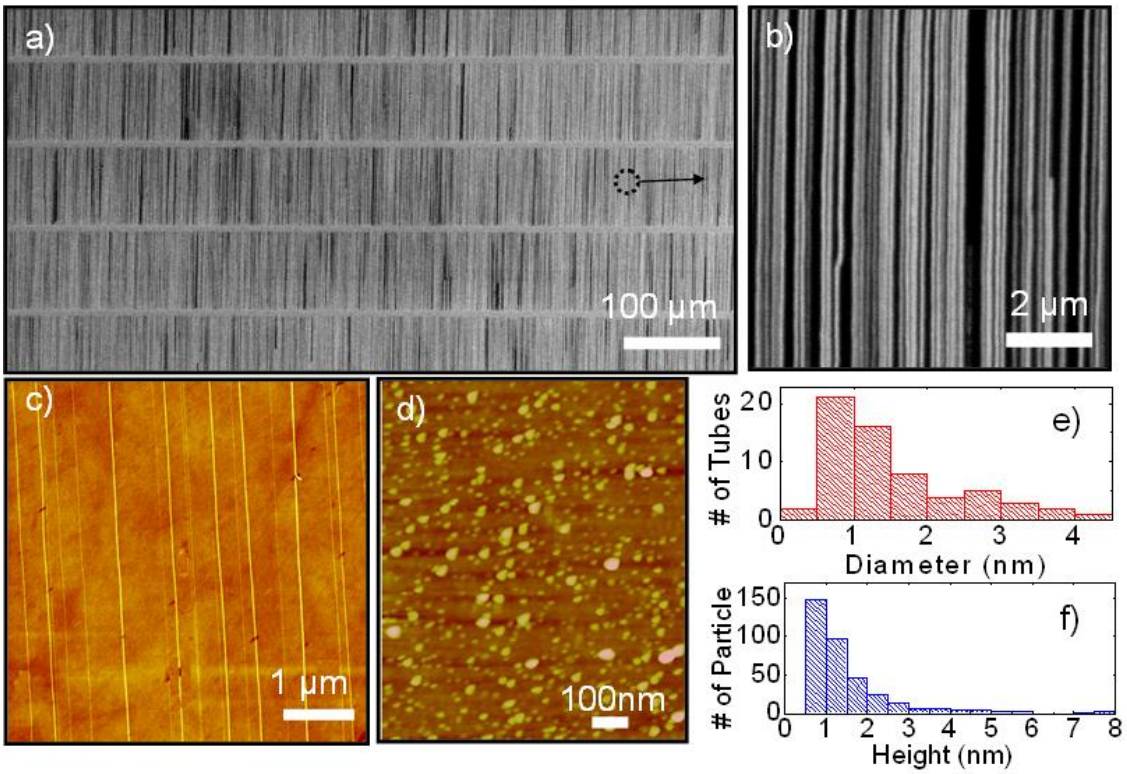


Figure 4.1 (a-b) Scanning electron microscope images of aligned SWNT arrays collected at different magnifications. The tube density is ~5 SWNT/µm. The bright regions in (a) correspond to random networks of SWNT that form near the Fe catalyst that exists in these locations. (c) Atomic force microscope (AFM) images of selected SWNTs in these arrays. (d) AFM images of iron oxide catalyst particle after 1.5 hour annealing process.

Distribution of diameters of SWNTs in the arrays (e), and catalyst particles (f) measured by AFM. The average diameter is ~1.2 nm for SWNT and 1.8 nm for catalyst particles.

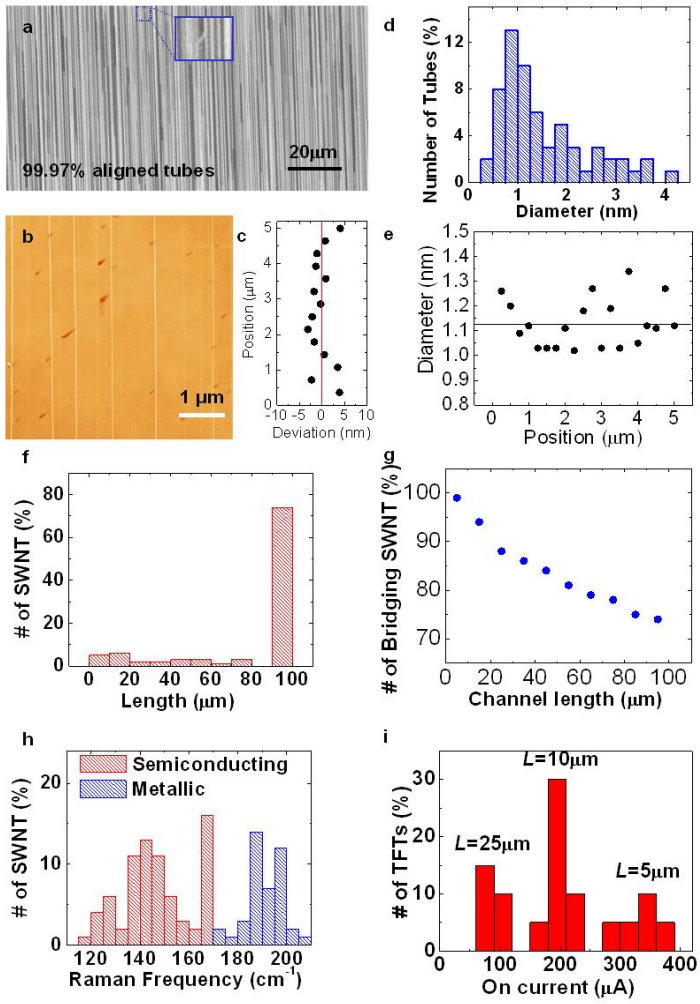


Figure 4.2 a, SEM image of an array of SWNTs. The inset shows the single, small segment of a misaligned tube that exists in this entire area. **b,** AFM image of an array of SWNTs showing excellent parallelism. **c,** Plot of deviation in the position of a SWNT as a function of position along its length, measured relative to a perfect linear shape. **d,** Distribution of SWNT diameters measured from an array like that shown in **a**. **e,** Diameters of SWNT measured as a function of position across an array. **f,** Distribution of SWNT lengths in an array similar to that shown in Fig. 1a of the main text. **g,** Measured numbers of SWNTs that bridge the gap between source and drain electrodes spaced by some distance (i.e. the channel length). **h,** Distribution of radial breathing

mode frequencies as measured by Raman scattering. **i,** Measured on currents in transistors (TFTs) with different channel lengths (*L*).

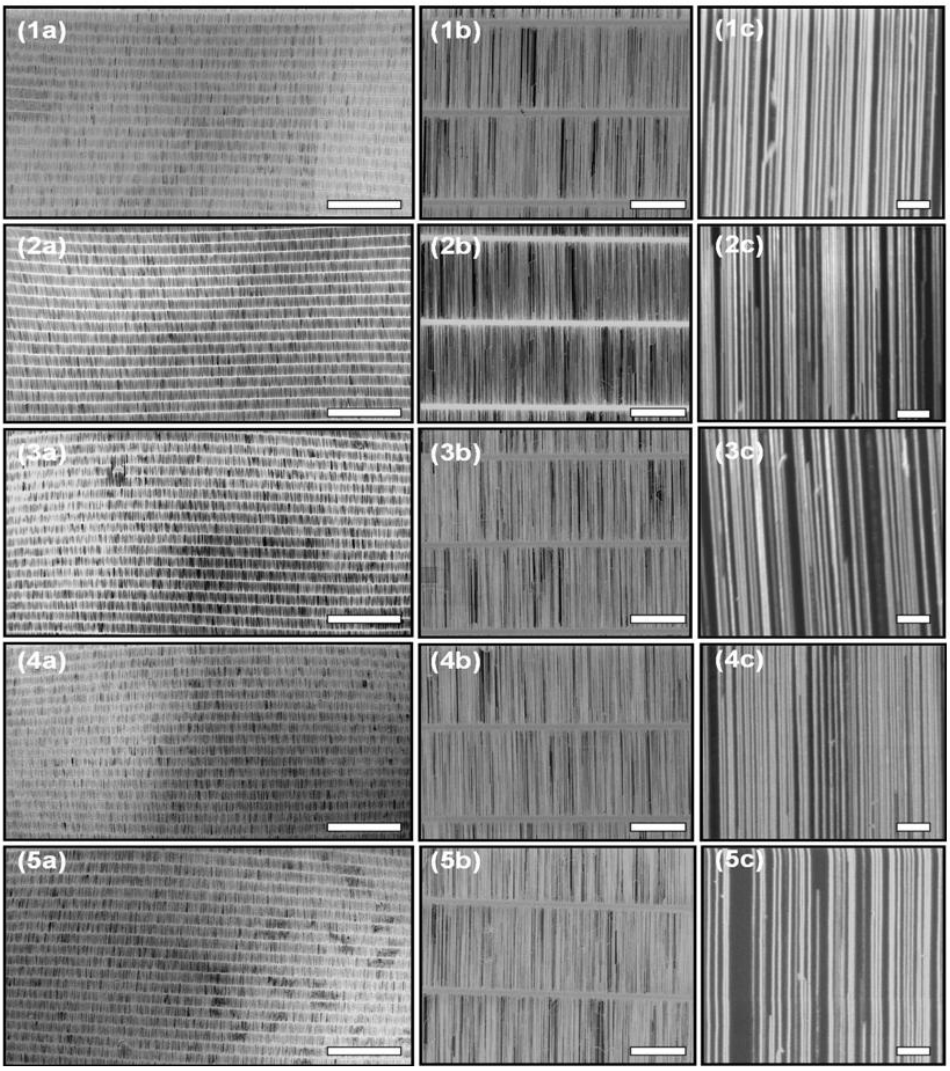


Figure 4.3 Growth yield for nanotube arrays. 5 substrates with Fe catalyst were prepared and were grown at the same time using CVD.

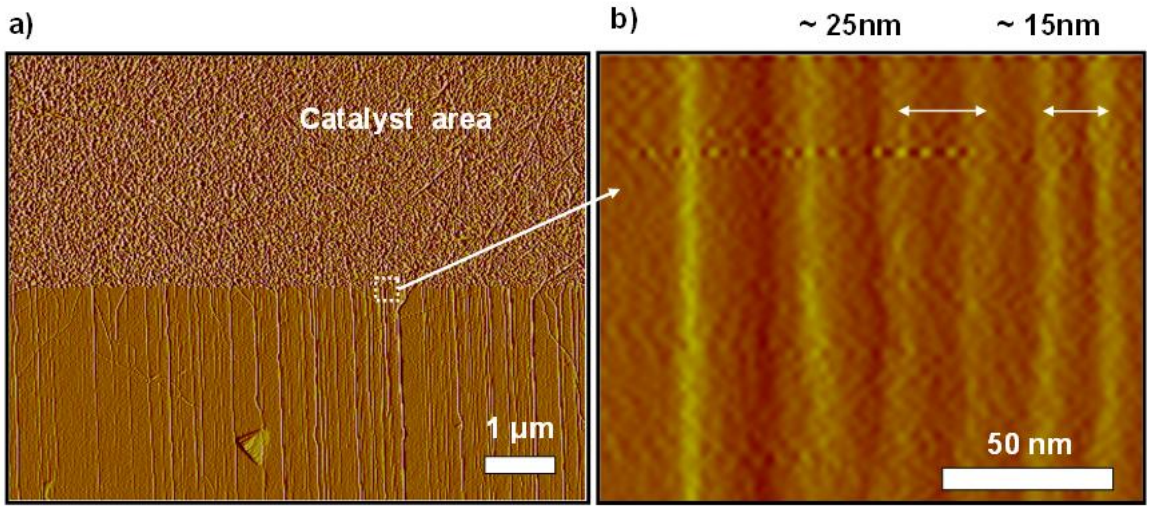


Figure 4.4 a) Atomic force microscope (AFM) image of a dense array of SWNTs emerging from a region of patterned catalyst. b) High resolution AFM image of a high density region in this array. The shortest distance between two SWNT, as measured in this fashion, is ~ 25 nm. In this area, the local tube density can be as high as 40-50 SWNT/µm.

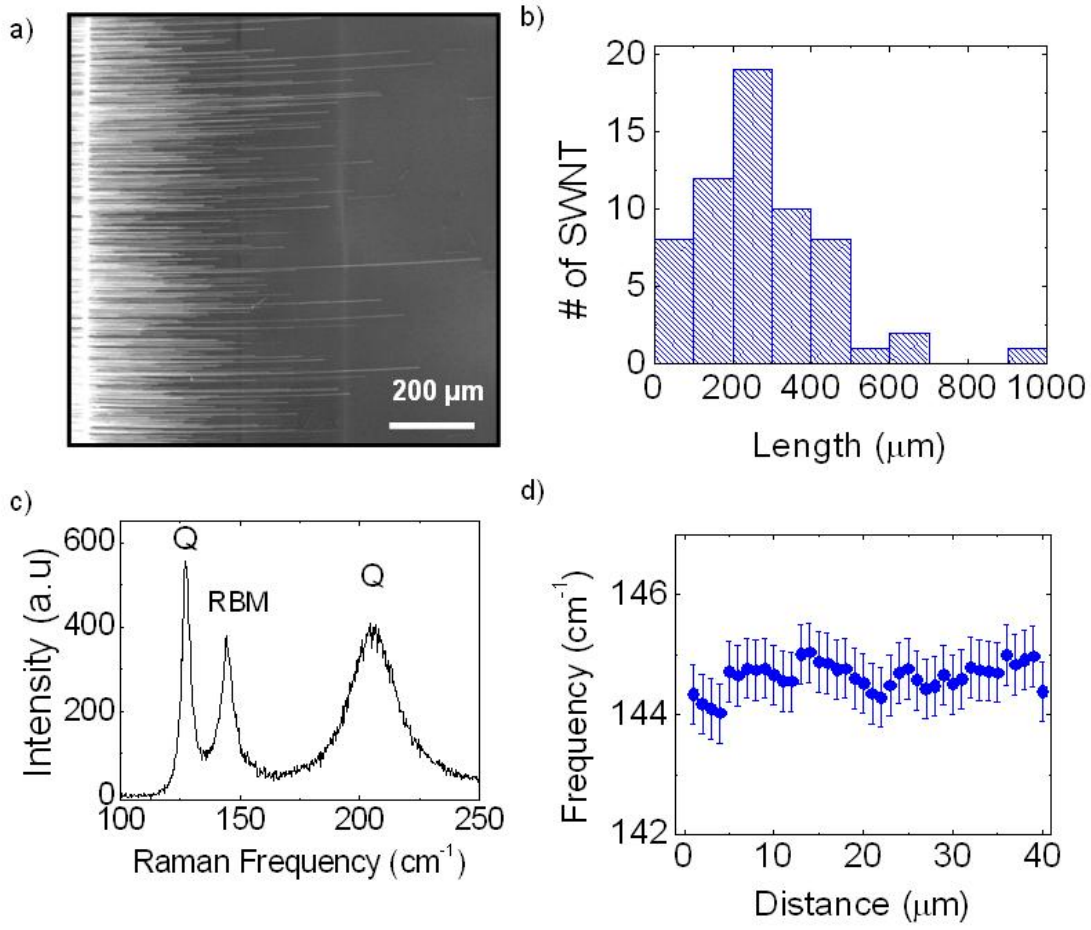


Figure 4.5 (a) Scanning electron microscope image of SWNTs grown from a patterned line of Fe catalyst (vertical, bright stripe on the left side of this image). (b) Histogram of the lengths of SWNTs shown in (a). The longest tube is ~1 mm, and the average length is ~300 µm. (c) Raman spectrum of an individual SWNT from the array shown in (a), collected using a confocal spectrometer. The peaks labeled "Q" at ~127 cm^{-1} and ~205 cm^{-1} are associated with the quartz substrate. The radial breathing mode (RBM) of the SWNT is at ~144.5 cm^{-1}. (d) Frequency of the RBM of a SWNT as a function of position along its length. The frequency is constant to within the uncertainty of the measurement (±0.5 cm^{-1}), for this 50 µm long segment.

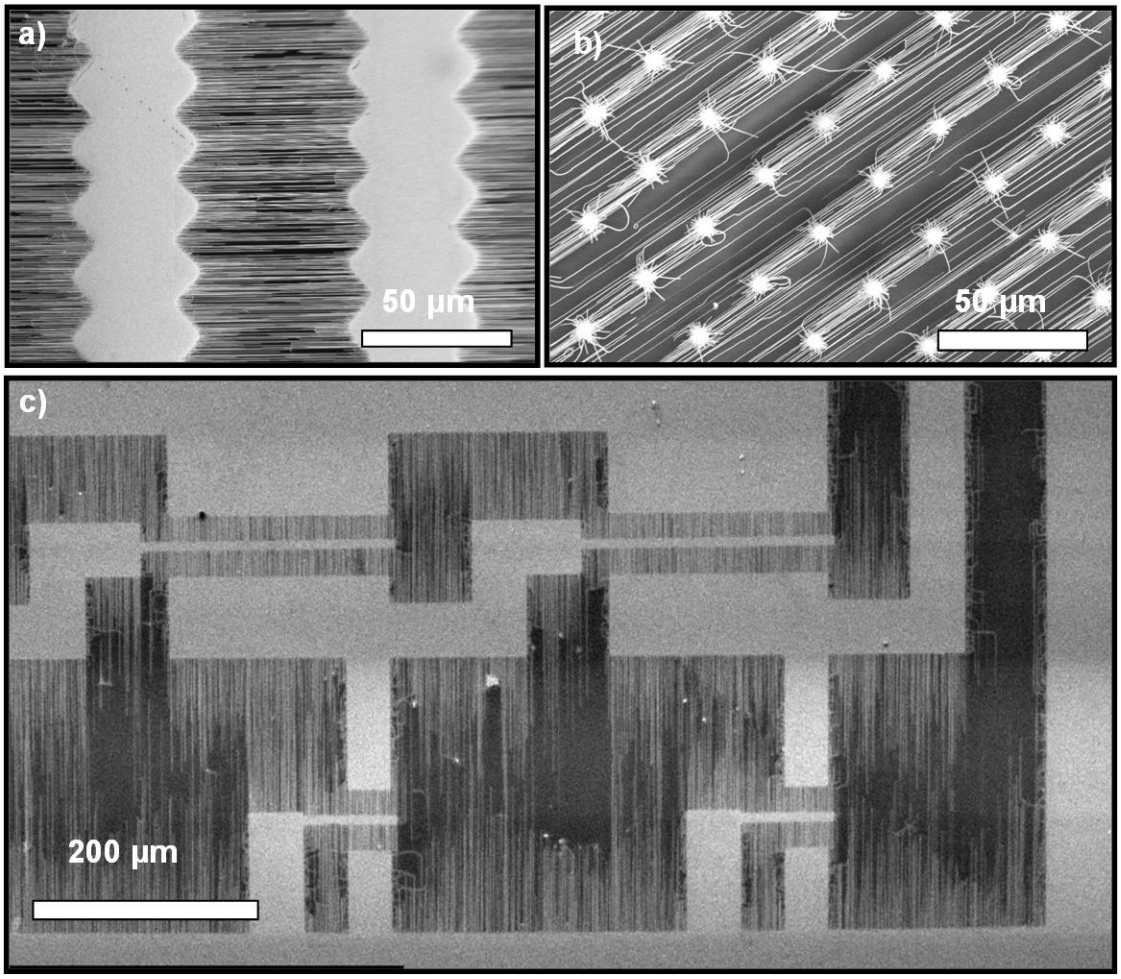


Figure 4.6 Aligned arrays of SWNT grown from catalysts particles patterned into different geometries, including (a) wavy lines, (b) circles (2 **µ**m diameters separated by 25 µm) and (c) a complex circuit-like pattern.

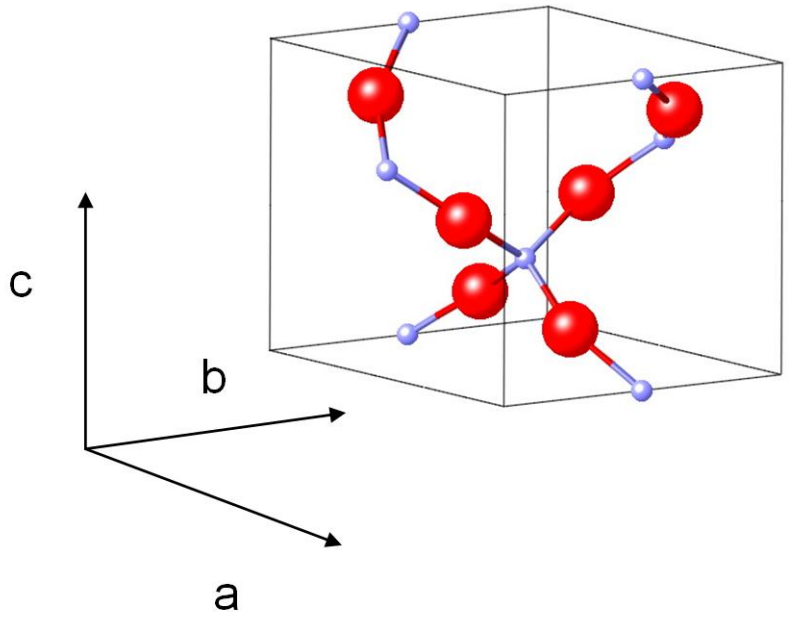


Figure 4.7 The unit cell of quartz crystal, Red and blue spheres represent oxygen and silicon atoms.

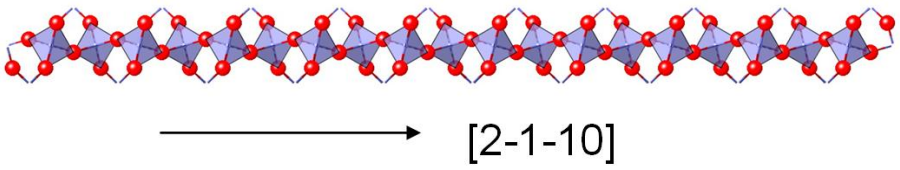


Figure 4.8 Chain of tetrahedral structures (Si_2O_4) connected by the corner oxygen.

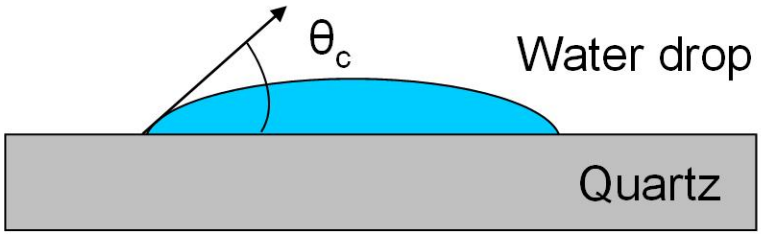


Figure 4.9 Contact angle of water on quartz surface.

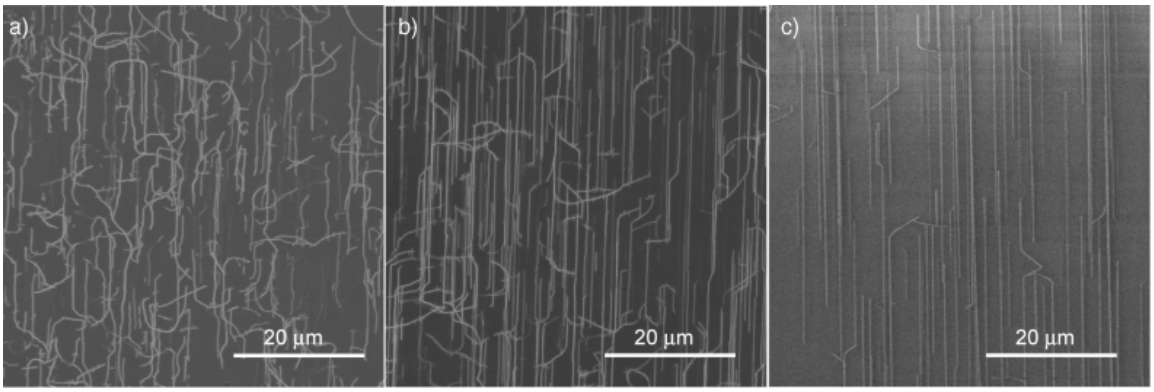


Figure 4.10 SEM images of SWNTs grown on quartz annealed at 900 ^{o}C for different times. (a) 10 min. (b) 4 hours, (c) 7 hours.

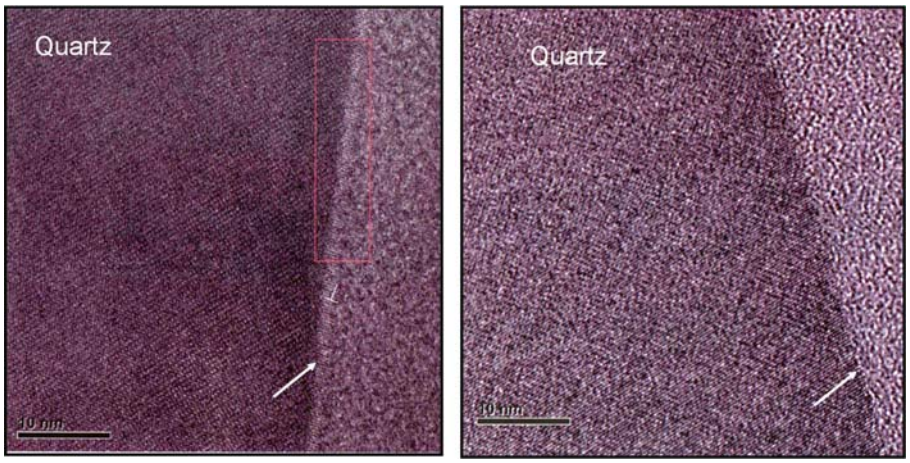


Figure 4.11 Cross-sectional Transmision electron micrographs of unannealed (a) and annealed (b) quartz surface. Very thin amorphous layer of SiO2 can be seen on the top surface of unannealed quartz. (TEM images were taken by Prof. Jian-Min Zuo)

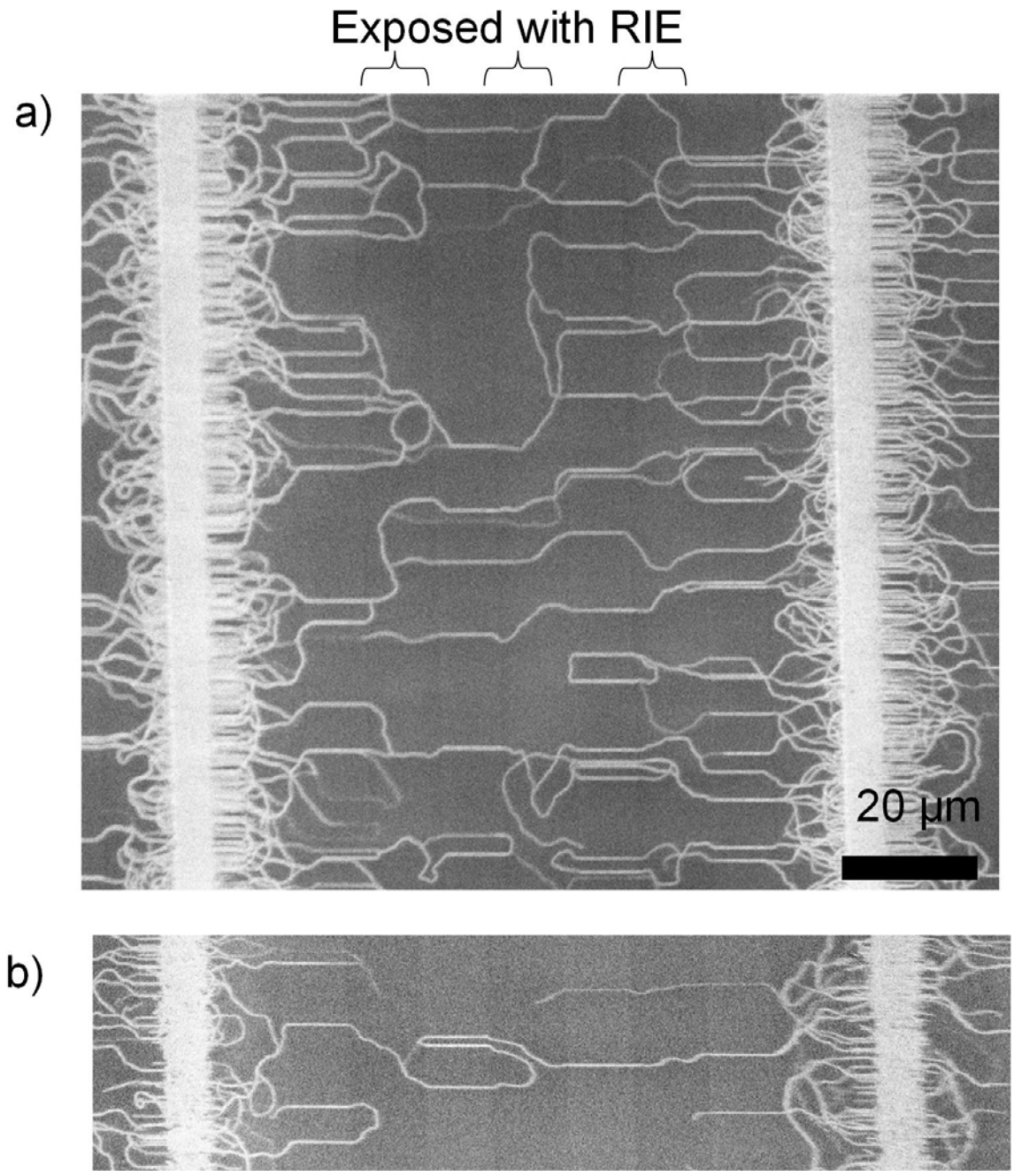


Figure 4.12 SEM images of SWNTs grown on quartz substrate which is selectively exposed by oxygen plasma.

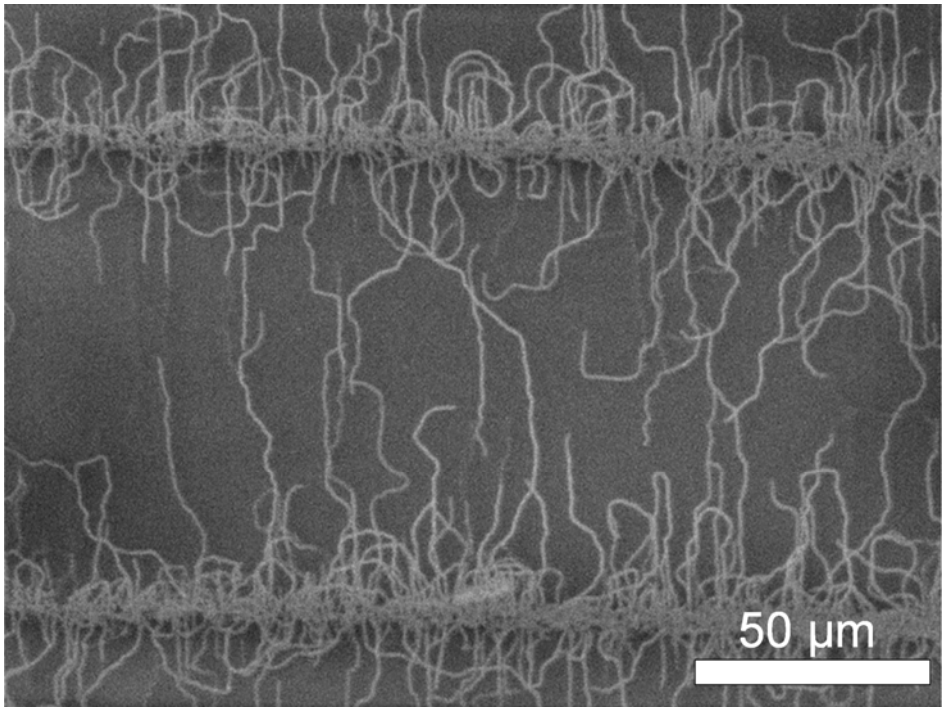


Figure 4.13 SEM images of SWNTs grown on quartz substrate which is exposed by ozone.

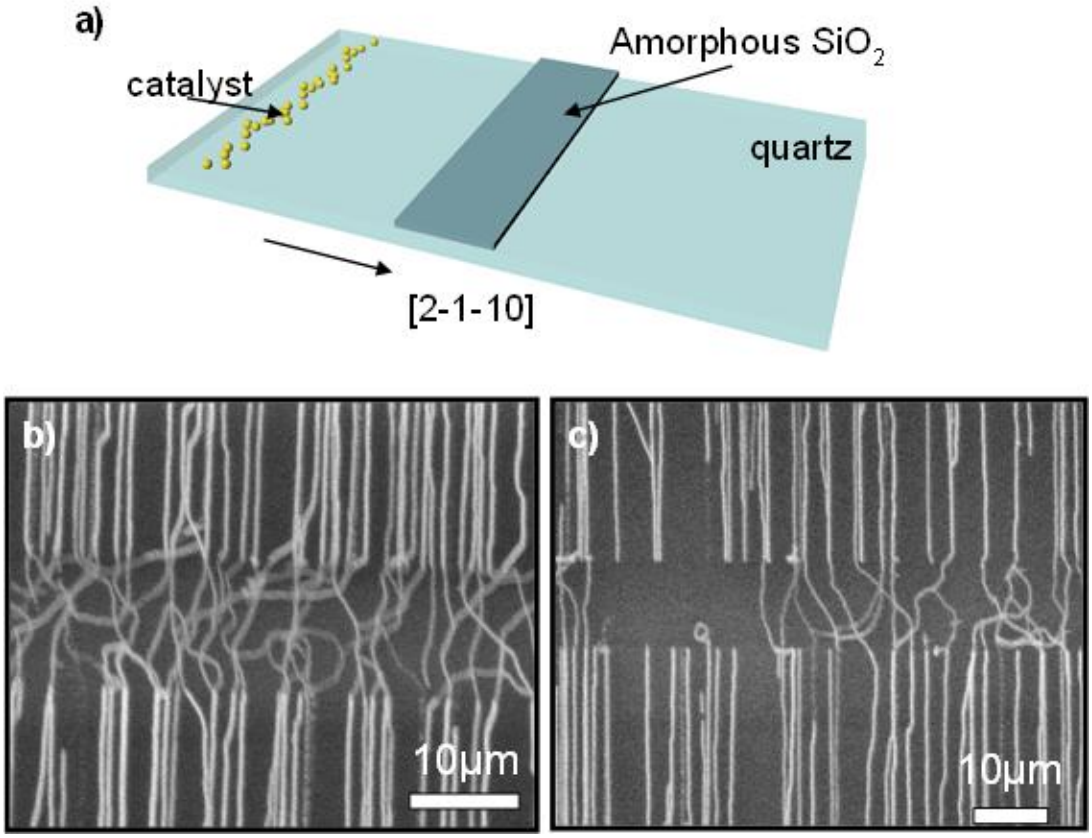


Figure 4.14 (a) Schematic illustration of the geometry of quartz with a 2 nm thick patterned stripe of amorphous SiO_2. (b,c) SEM images of SWNTs grown on this substrate.

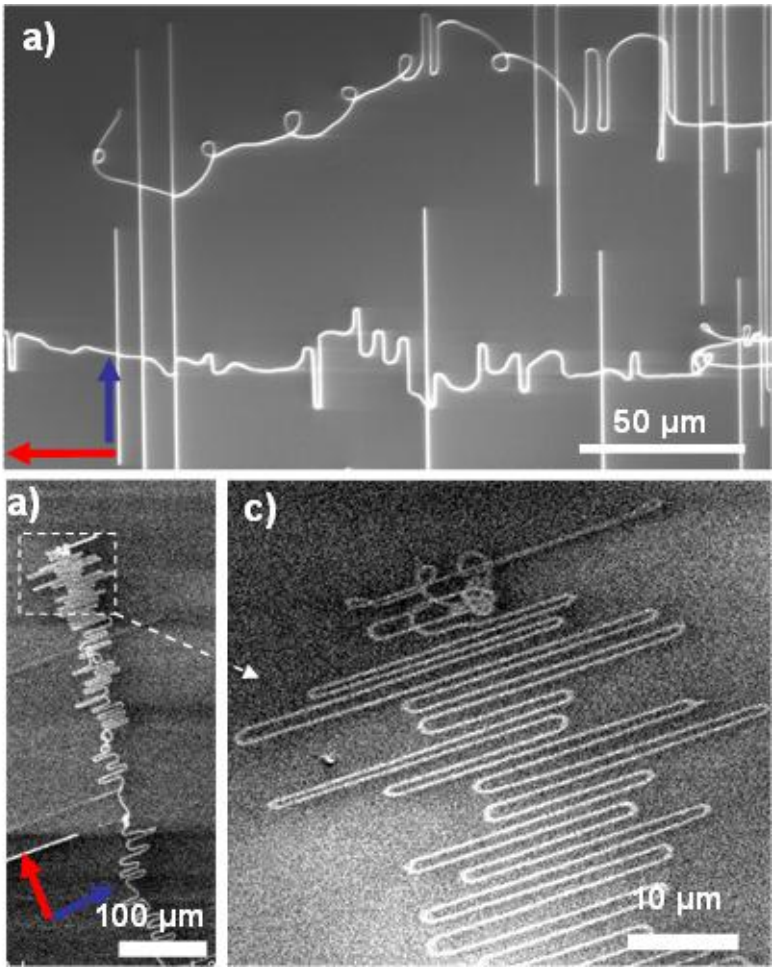


Figure 4.15 (a) Scanning electron microscope (SEM) image of an SWNT formed into an unusual shape due to the combined effects of alignment due to the quartz surface (blue arrow indicates X-axis) and to gas flow (red arrow direction). (b) Large area and zoomed (c) SEM image of a zigzag shaped SWNT.

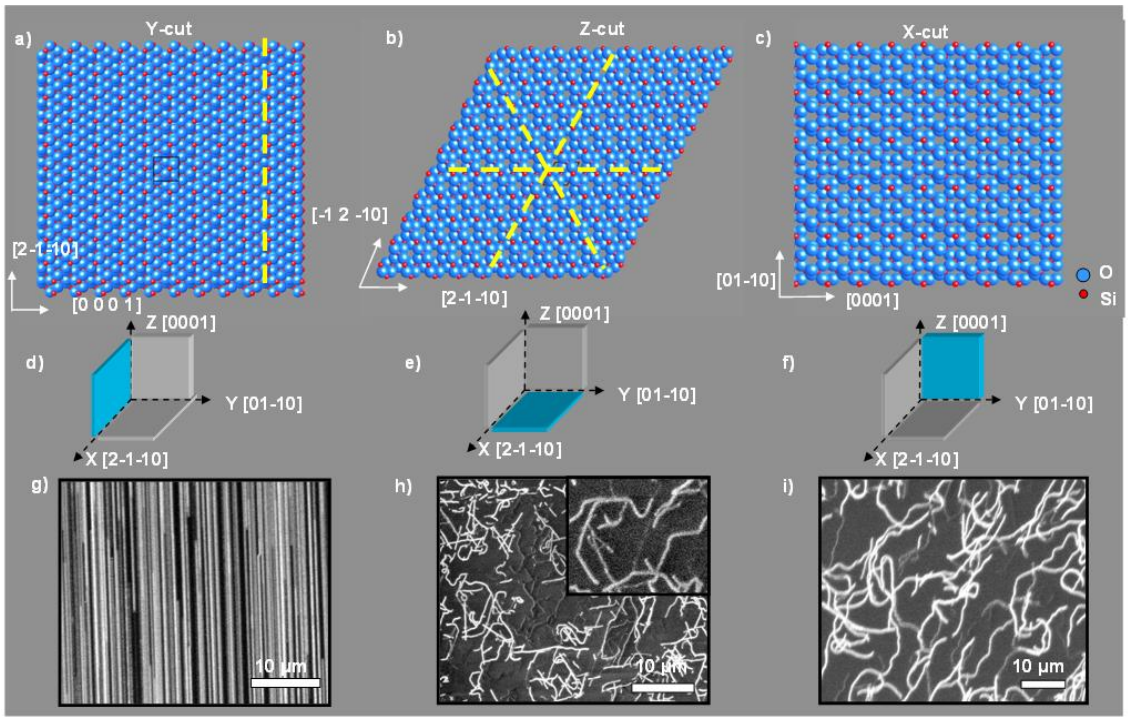


Figure 4.16 Space filling model of Y-cut (a), Z-cut (b) and X-cut (c) quartz surfaces. The insets show the orientation of the quartz surface with respect to main axis of quartz. (d-f) Scanning electron microscope (SEM) images of SWNTs grown on Y, Z, X cut quartz wafers, respectively. The Y-cut provides high degree of alignment along [2-1-10] direction; Z-cut provides 3 fold symmetric alignment (inset in e shows a high magnification SEM image); X-cut does not provide any alignment.

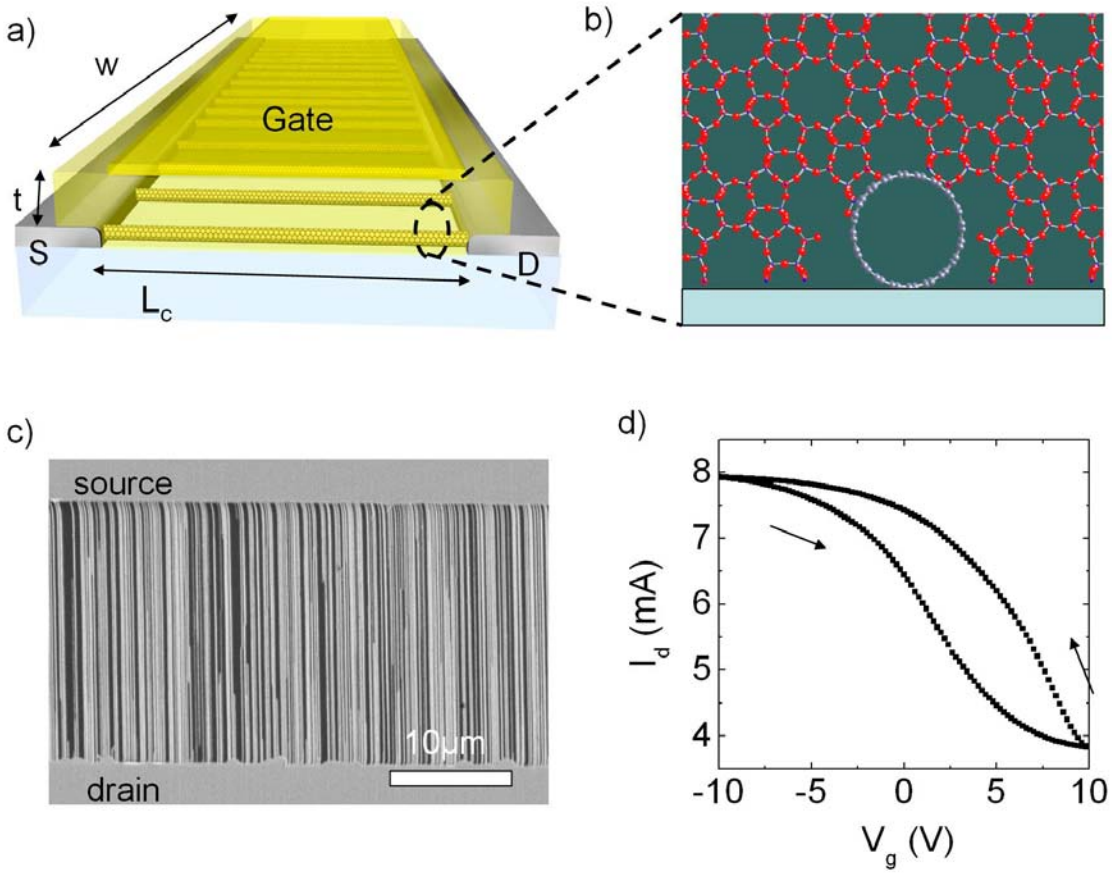


Figure 4.17 (a) Schematic illustration of the geometry of a thin film type transistor that uses aligned SWNTs as the semiconducting channel. (b) Atomic structure of a silsesquioxane gate dielectric coating a SWNT on a substrate. (c) Scanning electron microscope image of the channel region of a device like the one illustrated in (a). The bright regions at the top and bottom of this image are the source and drain electrodes. (d) Source/drain current (I_d) as a function of gate voltage (V_g) at a source/drain bias of 1 V. Arrows indicates the sweeping direction of gate voltages.

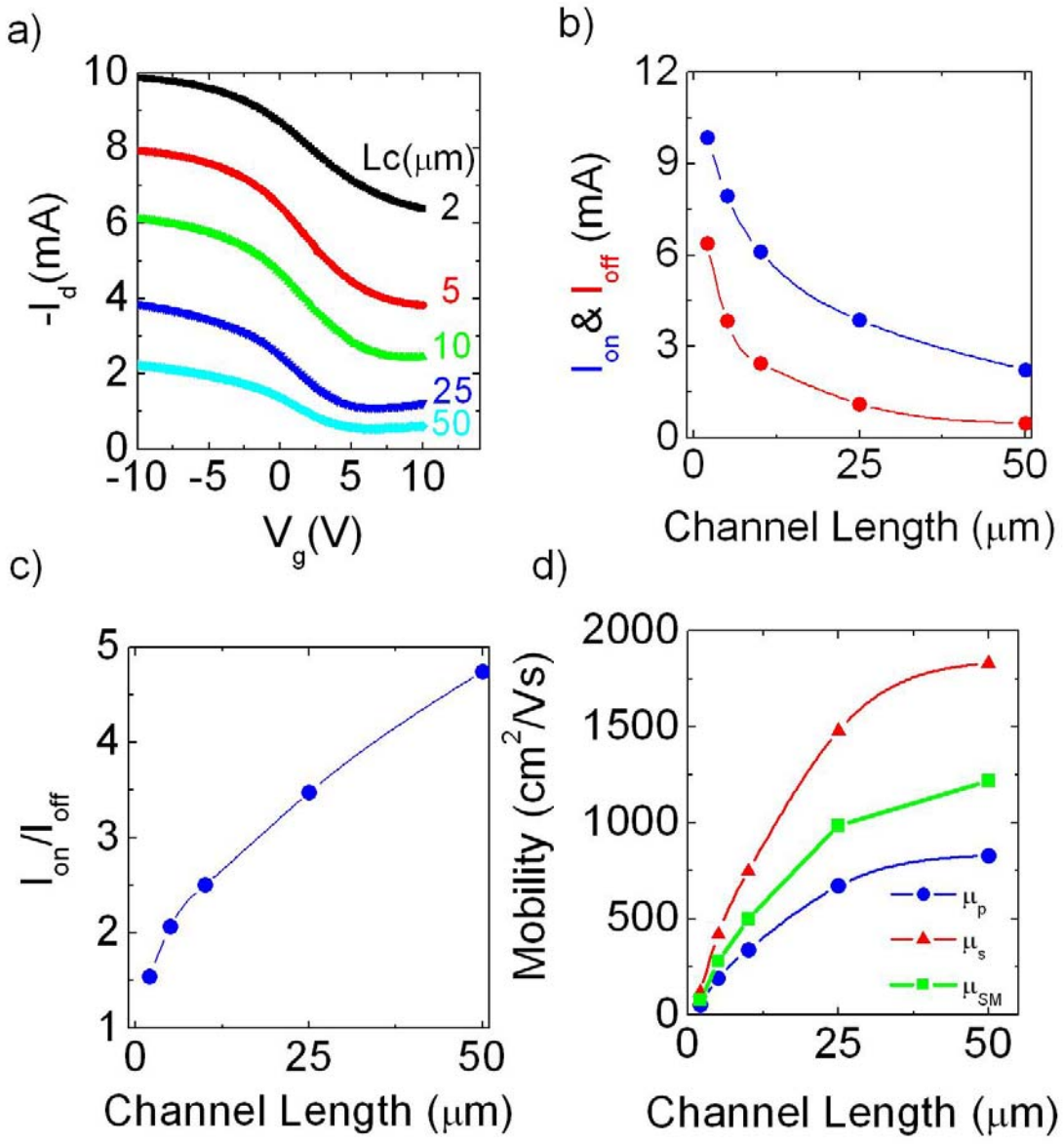


Figure 4.18 (a) Transfer characteristics measured from thin film transistors that use SWNT arrays, with channel widths of 200 μm and channel lengths (L_c) between 2 and 50 μm. (b) On current and off current (I_{on} and I_{off}, respectively) as a function of channel length. (c) Channel length dependence of on/off ratio. (d) Apparent mobility calculated by using a parallel plate model for the capacitance (μ_p) and rigorous calculations of the device capacitance taking into account only semiconducting tubes (μ_S) and both metallic and semiconducting tubes (μ_{SM}).

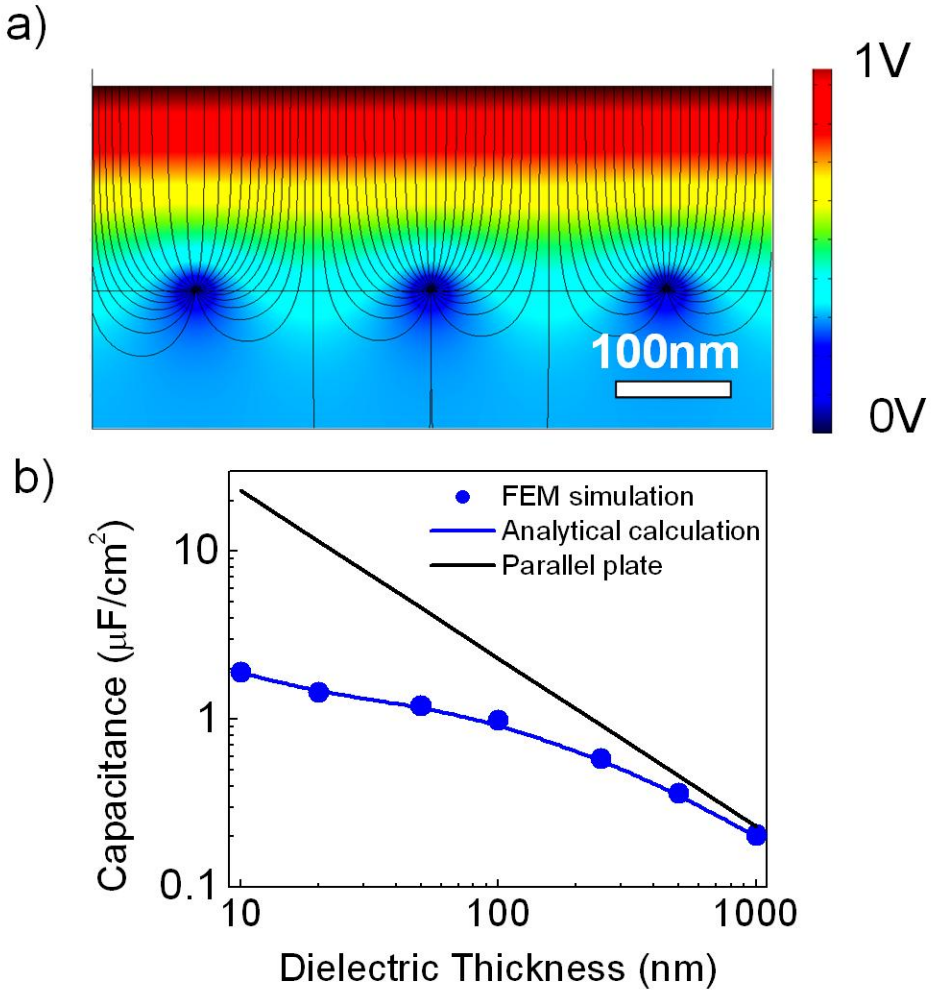


Figure 4.19 (a) Field distribution of a SWNT array calculated by finite element modeling. The distance between the tubes is assumed to be constant. Y-axis is scaled by 2. (b) Calculated capacitance for arrays with the tube density of 5 SWNT/μm.

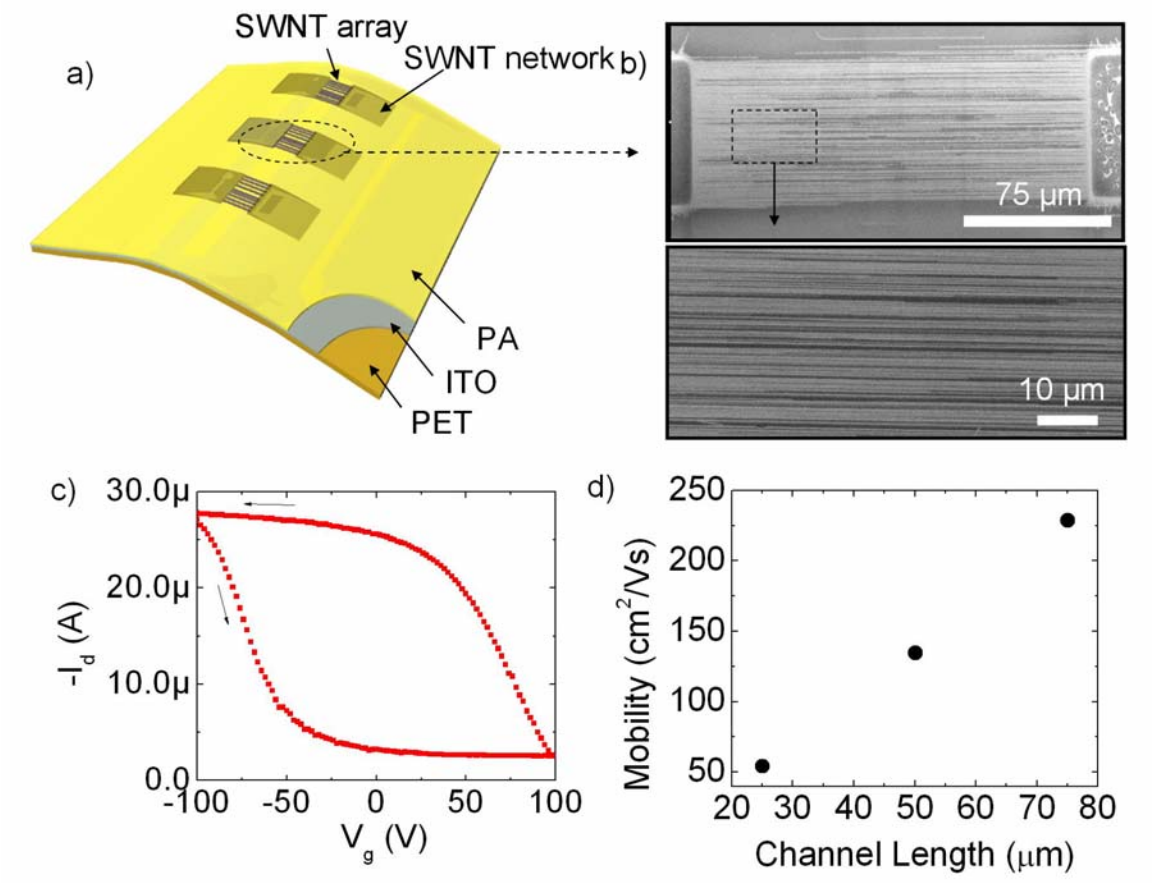


Figure 4.20 (a) Schematic geometry of TFT on ITO coated PET substrate. (b) SEM images of TFTs that use aligned arrays of SWNT as an active semiconductor and dense SWNT network as an source and drain electrode. (d) Transfer characteristics of the TFT as a function of gate voltage. d) Channel length dependence of calculated field effect mobility.

CHAPTER 5 CHARGE TRANSPORT THROUGH SWNT THIN FILMS

This chapter was published as "Experimental and Theoretical Studies of Transport Through Large Scale, Partially Aligned Arrays of Single Walled Carbon Nanotubes in Thin Film Type Transistors **Coskun Kocabas**, Ninad V. Pimparkar, Ozlem Yesilyurt, Seong Jun Kang, M. Alam, John A. Rogers *Nano Letters, 7, 1195-1202 (2007)* " Reproduced (or 'Reproduced in part') with permission from Nano Letters. Copyright 2007 American Chemical Society.

5.1 Introduction

Thin films of single-walled carbon nanotubes (SWNTs) represent a class of electronic material that can serve as high-performance semiconducting and/or conducting layers in thin film type field effect transistors (TFT) and other devices(1-8). The favorable statistics of such films may provide a route to practical tube based electronics systems by obviating the need for precise control over the properties or positions of individual SWNTs. The films can consist of any arrangement of tubes, from random networks to perfectly aligned arrays typically in coverages that correspond to somewhat less or somewhat more than a monolayer (appropriate for maximum gate control). In such network TFTs, tube-tube contact resistances have detrimental effects on the overall transistor performance. Reducing or eliminating such tube-tube contacts can improve the performance. This goal can be achieved by designing the devices such that (i) the SWNTs are sufficiently long (length L_S) to directly bridge the source/drain electrodes (channel length L_C) and (ii) the SWNT are configured into dense, aligned arrays that avoid tube-tube overlaps. Generating well aligned arrays with near-monolayer coverage represents a considerable experimental challenge. Some promising methods rely on chemical vapor deposition growth guided by favorable van der Waals and/or step edge interactions between the tubes and the underlying substrate (quartz or sapphire)(9-11). When implemented with annealed substrates, moderate catalyst concentrations and optimized growth conditions, well aligned arrays at reasonably high coverage are possible(12). Even in these cases, however, some degree of misalignment exists, which tends to increase with increasing tube coverage. The influence of even a small number of

misaligned tubes on transport can be significant, since such tubes can intersect and thereby establish electrical contacts to many other aligned tubes.

Predictive knowledge of the physics of percolative transport through such partially aligned heterogeneous (one-third of the tubes are metallic) arrays, therefore, is a prerequisite to interpret and optimize the electrical performance of these thin films. The system involves, in general, a combination of (i) transport from one electrode to another through individual tubes that bridge the source/drain electrodes, and (ii) percolation type transport in an anisotropic tube network. The length and coverage of the tubes and the orientation and length of the transistor channel (L_C) determine the relative contributions of these two pathways to overall transport in a particular device. Effects of anisotropy in the percolation through purely conductive networks has been studied in structured metal films(13) and carbon nanotube/polymer composites(14). The present report examines a different type of anisotropic network, which involves both gate modulated percolation and direct transport in transistor structures. This particular problem, which is of paramount importance to the implementation of SWNTs as active layers in thin film electronic systems, as well as the more general case of gate modulated percolation transport in heterogeneous anisotropic networks (i.e. one with both metallic and semiconducting elements), has not been studied before. The results presented here include experimental and theoretical studies of transport and scaling properties of transistors that use sub-monolayer films of SWNTs with systematically varying degrees of alignment and coverage, from low coverage well aligned films to high coverage partially aligned ones. Good agreement between measurement and theory validates the key aspects of the model, and reveals new routes to improve the transport properties of the films.

5.2 Methods

Figure 5.1 shows scanning electron micrographs (SEMs) of SWNT films typical of those studied here. These samples were grown by conventional chemical vapor deposition on ST cut quartz substrates (12) using spin cast ferritin catalysts. Before the growth, the quartz wafers were annealed for 8 hours at 900^0 C in air and cleaned with acetone, isopropyl alcohol and deionized water. The annealing conditions, the catalyst

concentrations and the growth conditions determine the coverage and alignment of SWNTs in the resulting films. By varying these parameters, we could achieve films ranging from well to moderately aligned, and from low (*~0.1%*) to high (*~2%*), in terms of the percentage of the surface covered by SWNTs. For the cases studied here, we used four different films (Figure 5.1a,Figure 5.1d) with degrees of alignment, defined primarily by the catalyst concentrations. Solutions of the catalyst (ferritin, Aldrich, diluted with DI water) with concentrations of 0.1 mg/ml, 0.2 mg/ml, 0.76 mg/ml or 3.8 mg/ml, were placed on the quartz substrate and after waiting 1 min, a few methanol droplets were added. The substrate was then rotated at 3000 rpm for 30 sec using a spin coater, followed by thorough rinsing with methanol. Heating at 900 °C for 10 min oxidized the catalyst. Cooling to room temperature and then heating to 900 °C in a hydrogen environment reduced the catalyst. Purging with hydrogen at 900 °C for 1 min and then introducing a flow of methane (2500 standard cubic centimeters per minute (sccm)) and hydrogen (75 sccm) at 900 °C for 10 min led to the growth of SWNTs. The diameters of the tubes in all cases are between 1 and 3 nm, as determined by atomic force microscopy (9) with some trend toward larger diameter tubes (or small bundles) with increasing coverage. Past studies of SWNTs grown by CVD with ferritin catalysts indicate that roughly one third of the tubes are metallic and two thirds are semiconducting (15). The ratio of numbers of semiconductor to metallic tubes was evaluated directly by electrical burning of single or a few tubes devices and counting the metallic and semiconducting tubes individually. Details of the experiments are given in Supporting Information. The histogram plots summarize the distributions of tube lengths (L_S) and orientations (θ), as determined from image analysis of the SEMs. The orientations of the tubes often change at one or both of their ends. The reported values of θ correspond to segments of tubes that have a single orientation, as observed in the field of view. Similarly, the values of L_S correspond to the lengths of these tube segments. The average tube lengths, $< L_S >$, were determined by the arithmetic mean of the measured L_S values; the lengths for films 1-4 were *40, 22, 6* and *5* μm, respectively. The degree of alignment can be defined in terms of an anisotropy parameter, R, where $R=L_{//}/L_{\perp} = \sum_{i=1}^{N}\left|L_{S,i}\cos\theta_i\right| \Big/ \sum_{i=1}^{N}\left|L_{S,i}\sin\theta_i\right|$. Films 1-4 have R = *21.4, 6.5, 6.0*, and *2.9*, respectively.

These growth procedures yield strong correlations between the coverage, the tube length and the degree of anisotropy. We also note that while the approaches presented here require quartz substrates, the anisotropic networks can be transferred to other substrates, including thin, flexible plastic sheets (16).

We constructed top gate transistors in which the films (films 1-4, as illustrated in Figure 5.1) serve as the semiconductor layer. The fabrication began with growth of the films on quartz, followed by definition of source and drain electrodes of Ti/Pd (1 nm / 25 nm; deposited by electron beam evaporation) by photolithography and liftoff. A spin cast layer of a photocurable epoxy (MicroChem, SU8-2) with thickness ~1.3 μm provided a gate dielectric with dielectric constant of ε_r=4.0, and per unit area capacitance of 2.8 nF/cm^2. We chose a thick polymer for the present studies for three reasons: (1) these materials enable simple, high yield fabrication of devices with very low gate leakage, (2) the polymers, unlike many of the thin high capacitance inorganic materials that have been explored in single tube devices, do not alter the electronic properties of the tubes, and (3) the gate coupling to the tubes can be approximated by a parallel plate model for the capacitance (i..e the tube-tube separations are, in most cases, small compared to the thickness of the gate dielectric). Thinner dielectrics, are desirable for device performance, but are not important for the present studies. Photolithography and liftoff defined a gate electrode on top of this dielectric, aligned to the channel and also overlapping parts of the source/drain electrodes. Openings in the dielectric formed by photolithographic patterning provided electrical probing access to the source and drain. We used these procedures to fabricate the transistors with channel lengths of L_C = *5, 10, 25, 50* and *100 μm* all with widths of W = *250 μm*. Figure 5.2 shows the device geometry. The channels were oriented either parallel or perpendicular to the preferred direction for tube alignment. For each device, currents between source and drain were measured at a bias (V_{sd}) of *0.5 V* while sweeping the gate (V_g) between *-40 V* and *40 V*. In all cases the current to the gate was less than *100 nA*.

5.3 Results and Discussion

5.3.1 Anisotropic SWNT Network Thin Film Transistors

To analyze the transport characteristics of these films, we consider the scaling behavior of 'ON' and 'OFF' currents, I_{on} and I_{off}, as a function of channel length L_C. The ON current is measured at $V_{sd} = 0.5\ V$ and $V_g = -40\ V$; the OFF current corresponds to the minimum current observed for the range of gate voltages between $-40\ V$ and $40\ V$, with $V_{sd} = 0.5\ V$. (The slight ambipolar response of the transistors motivates the use of such a definition for I_{off}.) Although the transistors exhibited some hysteresis, as is typical for devices of this type, the current values, I_{on} and I_{off}, which form the focus of this paper, remain robust, independent of direction or history of applied voltages to the gate. Figure 5.2e shows a typical device response and channel length dependence. A total of 80 devices were measured for each of the films 1-4: 40 with the channel along the preferred alignment direction and 40 with orientations perpendicular to it for five different channel lengths, $L_C = 5, 10, 25, 50$ and $100\ \mu m$.

Figure 5.3 illustrates a representative set of different devices that were studied. The layouts of the tubes have correlated levels of coverage, alignment and tube length, for the growth procedures used here. (Recent reports describe growth strategies that eliminate some of these correlations(17). At low coverage, extremely high degrees of alignments and long tube lengths result, leading to many tubes that bridge the source and drain electrodes, with almost no tube-tube overlaps. This configuration leads to large ON currents, but also large OFF currents due to the presence of the metallic tubes. At high coverage, the alignment can be poor and the tubes are short; this configuration leads to percolation transport pathways and high on/off ratios due to the small chance of bridging tubes or purely metallic current pathways. Similar but different types of considerations lead to different behaviors with different channel orientations. Figure 5.3c and Figure 5.3d show devices with same tube coverage but different channel orientations. Lower ON currents and higher on/off ratios are observed for perpendicular orientation (Figure 5.3f) compared to the parallel orientation. Measurements of this type provide a means to quantify the level of electrical anisotropy in the network, in terms of the ratio of ON currents measured in the parallel and perpendicular directions. Figure 5.3g shows the

calculated current anisotropy, $A = I_{\parallel}/I_{\perp}$, evaluated in the on state, of aligned, dense partially aligned and random network cases. The highest anisotropy occurs, as expected, in the aligned devices. Increasing tube coverage tends to lower the anisotropy. In cases that involve some level of percolation transport pathways, the ON current anisotropy decreases with increasing channel length. Completely random network grown, for example on amorphous SiO_2, does not provide any anisotropic conduction.

A review of the measured electrical characteristics for aligned (Figure 5.1a, Figure 5.1a), partially aligned (Figure 5.1c, Figure 5.4b) and dense partially aligned (Figure 5.1d, Figure 5.4c) networks shows that, analogous to classical transistors, I_{on} and I_{off} decrease with increasing L_C. The corresponding insets show samples of randomly generated networks. Unlike classical transistors, however, the (channel-length) scaling exponents of I_{on} and I_{off}, are significantly different(7,18). This anomaly is highlighted in the ratio of I_{on}/I_{off} $(= R_I)$ which, instead of remaining constant (as would be expected for classical transistors), increases with L_C. Moreover, the rate at which R_I increases with L_C increases with decreasing coverage. Finally, one anticipates the I_{on} and I_{off} to individually approach zero for perfectly aligned network as $L_C \rightarrow L_S$, yet remarkably both currents remain finite even with $L_C >> L_S$. These three counter-intuitive transport characteristics of aligned tubes indicate that classical 'top-down' mobility-based models are no longer adequate and that a 'bottom-up'(18) treatment of transport based on stick-percolation models is required.

5.3.2 Stick-percolation Model of SWNT Network

We construct a numerical stick-percolation model for this system by randomly populating a 2D grid by sticks of length (L_S) and orientation (θ) with probability density function (PDF) consistent with experimental conditions (Figure 5.1). One third of the generated tubes are metallic and the remaining two-third are semiconducting (the results are not too sensitive to the precise fraction of metallic tubes between 1/3 and 1/4,). Since, L_C and L_S are much larger than the phonon mean free path, contact resistances are not important and linear-response transport (small V_{sd} and constant V_g obviates the need to solve the Poisson equation) within *individual stick segments* of this anisotropic stick-network system is well described by drift-diffusion theory (7,19-21). The low bias drift-

diffusion equation, $J = q\mu n\, d\varphi/ds$, when combined with current continuity equation, $dJ/ds = 0$, gives the non-dimensional potential φ_i along tube i as

$$d^2\varphi_i/ds^2 - c_{ij}(\varphi_i - \varphi_j) = 0. \quad (1)$$

Here, s is the length along the tube and $c_{ij} = G_0/G_1$ is the dimensionless charge-transfer coefficient between tubes i and j at their intersection point, and G_0 (~0.1 e^2/h)[22] and $G_1 (= qn\mu/\Delta x$ (7)) is mutual and self conductance of the tubes. Here, n is carrier density, μ is mobility and Δx is grid spacing. The network contains both metallic and semiconducting tubes. I_{on} is computed by assigning G_1(metal) ~ G_1(semi), while I_{off} is compute by setting G_1(semi) =10^{-4} × G_1(metal) (23). G_1(metal) is assumed to be relatively insensitive to V_g. Hundreds of such samples are constructed to accurately reflect the PDF of length and anisotropy distribution in Figure 5.1 and the average of these currents is compared to the measured data.

5.3.3 Completely Random Stick Network

Before we use our stick-percolation model to interpret the three counterintuitive features of anisotropic network discussed above and shown in Figure 5.4, let us first analyze the simpler case of ON current dependence on L_C for the completely random stick network (7). As is well known, in a classical 2D film conductor the current will simply be inversely proportional to L_C i.e. $I_{on} \sim k / L_C$ which is ohm's law. Here, k is a material-specific constant. However, stick networks are non-classical 2D conductor and satisfy the finite size scaling relationship (24,25)

$$I_{on} \sim \frac{k}{L_S}\left(\frac{L_S}{L_C}\right)^m \quad (2)$$

where, the current exponent m is universal constant that depends *only* on the normalized coverage *($\rho_S L_S^2$, ρ_S is the number of SWNT in unit area and Ls is the length of SWNT)* and the anisotropy of the tubes. For example, for completely random network (24) and at coverage much higher than the percolation threshold ($\rho_S L_S^2 >> 4.236^2/\pi$) (26), most of the sticks in the network are connected and take part in conduction as shown in Figure 5.5a. Therefore, the high coverage network behaves as a 2D conductor and $m \sim 1$ i.e. $I_{on} \sim k / L_C$ (Figure 5.5c, red circles is experiment and red line is simulations), which is

again Ohm's law. But for a random network with coverage *at/near* percolation threshold ($\rho_S L_S^2 \sim 4.236^2/\pi$) all the sticks are not connected to source and drain and there are many islands or pools of unconnected sticks. These pools of sticks form new percolating paths as L_C is reduced – effectively increasing the width of the channel and increasing the current exponent to $m = 1.9$ (7,24) i. e. $I_{on} \sim (k / L_S)(L_S / L_C)^{1.9}$. For example, the intermediate coverage network (density above the percolation threshold, but still low compared to the dense network) shown in Figure 5.5b, has a current exponent of m = 1.4. The dotted lines show the current paths in each device. The ON current scaling appears in Figure 5.5c (blue squares). Figure 5.5d shows the current exponent (m) vs. coverage, where the symbols represent the two curves in Figure 5.5c. Devices with high coverage and long channel length ($L_C >> L_S$) approach the macroscopic device limit (classical ohmic behavior) (5,27). Here, the random networks with high coverage (Figure 5.5a, $\rho_S L_S^2 \sim$ 20-40) and low coverage (Figure 5.5b, $\rho_S L_S^2 \sim$ 5-10) were grown on SiO_2 (100 nm)/Si where Si forms a back gate.

Next, let us look at the second puzzle of on/off ratio: The scaling of the on/off ratio, R_I, for random networks, shown in Figure 5.5e, in the high (red circles) and low (blue squares) coverage cases provides additional insights. Note that approximately one-third of the tubes are metallic and two-third are semiconducting. In the 'ON' state, the total (metallic plus semiconducting) tube coverage $\rho_S L_S^2$ determines the experimental current exponent m_{on} as discussed earlier. On the other hand, the effective coverage of the network at 'OFF' state is $\sim \rho_S L_S^2/3$ (only metallic tubes conduct) with the current exponent being m_{off}. Since m scales inversely as $\rho_S L_S^2$ (Figure 5.5d), $m_{on} < m_{off}$. Since $R_I \equiv \frac{I_{on}}{I_{off}} \sim \left(\frac{1}{L_C}\right)^{m_{on}} \Big/ \left(\frac{1}{L_C}\right)^{m_{off}} = \left(\frac{1}{L_C}\right)^{m_{on}-m_{off}}$, therefore R_I increases with the exponent $m_{on} - m_{off}$ as a function of L_C. Moreover, the model predicts that the R_I vs. L_C increases more rapidly for lower coverage network. This is a consequence of rapidly changing exponent, m, at lower coverage vs. relatively constant m at higher coverage (compare red circles to blue squares in Figure 5.5e).

5.3.4 Anisotropic Stick Network

The analysis of ON current (I_{on}), OFF current (I_{off}). and on/off ratio (R_I) for anisotropic networks (Figure 5.4) is qualitatively similar the random networks (Figure 5.5). In fact, the basic explanations of the first two nonintuitive features of an anisotropic network, i.e. (a) non-classical scaling of ON current and OFF current scaling and (b) increase in R_I with L_C Figure 5.4, are exactly the same as that that the features shown in Figure 5.5 (just discussed above). However, *quantitatively* there are significant differences: First note that the high coverage anisotropic networks show exponents (~1) that are similar to the random network (Red circles in Figure 5.4 b and c and in Figure 5.5c) . The results are completely different for the lower coverage cases. Because of the tradeoff between tube coverage, tube length and orientation associated with the growth process, the current exponents can change drastically. The stick percolation model described above can be employed to explain the behavior of these anisotropic networks and the simulations (lines) agree with the experiments (symbols) well as shown in Figure 5.4. Each simulation point of Figure 5.4 and Figure 5.5 reflects the average solution of ~200 statistical samples. The current exponents for aligned (Figure 5.1a and Figure 5.4a), partially aligned (Figure 5.1c and Figure 5.4b) and dense partially aligned (Figure 5.1d and Figure 5.4c) networks for $I_{on,}$ I_{off} and on/off ratio are given by m_{on} = 1.7, ~1, ~1, m_{off} = 4.8, 2.78, 1.53 and $m_{on} - m_{off}$ = -3.1, -1.78, -0.53, respectively. Although some expected scaling of current exponents and current outputs can be observed through comparisons between device types, each network case must be analyzed separately due to correlations between tube length, tube alignment and coverage. For the anisotropic networks, low coverage provides low on/off ratios and high coverage provides on/off ratios similar to random networks. In the former cases, spanning tubes dominate transport, such that the on/off ratio is nearly constant (<10) up to channel length of 50 μm. Intermediate tube coverage provides the highest on/off ratio. All types of networks yields lower limit on the on/off ratio given by $1+2G_1(semi)/G_1(metal) \sim 3$ (assuming equal conductance in 'ON' state) as $L_C \rightarrow 0$, where all the tubes bridge S/D directly irrespective of alignment (Figure 5.4 and Figure 5.5e).

The stick percolation approach also highlights the importance of misalignment in dictating long-channel transistor performance and resolves the third dilemma so as to why the currents do not drop to zero as L_C approaches L_S. In Figure 5.1(a), the degree of misalignment appears negligible. Had this been the case, I_{on} and I_{off} would have dropped dramatically as $L_C \rightarrow L_S$, because the percolation threshold for perfectly aligned system approaches infinity ($\rho_{perc} \rightarrow \infty$). Yet, the I_{on} and I_{off} current show no dramatic change as L_C approaches L_S. This is because a very small number of short misaligned tubes can bridge the (otherwise unconnected) longer tubes and dramatically reduce ρ_{perc} to finite values. Misalignment also reduces the variations in current output with orientation of the channel relative to the preferred direction of tube alignment. In the long channel limit ($L_C > L_S$), this anisotropy can be extremely high, since the absence of spanning tubes in the perfectly aligned case yields zero current output (in both the ON and OFF states). For short channels ($L_C < L_S$), the degree of anisotropy is moderate, with current ratios in the range of $\pi/2$ for the perfectly aligned and isotropic cases.

5.3.5 Determination of Percentage of Metallic and Semiconducting SWNT

Electrical characterization of SWNT is the best way to figure out the metallic and semiconducting percentage. Therefore we have fabricated back gated field effect transistors using aligned SWNT. Aligned SWNTs were grown on quartz wafers using the same growth process described in the paper and then transferred on highly doped Si wafers (with 100 nm SiO2) using a transfer technique (30). Figure 5.6 shows the device layout and an SEM image of single tube device. We counted the number of metallic and semiconducting SWNT using electrical burning process, similar to that described before (31). In this procedure, the number of tubes can be counted from the sharp current drops on the IV curve. Figure 5.7 shows the transfer curves for semiconducting (a,b) and metallic (c,d) SWNT before and after the electrical burning. We measure the transfer curves before and after the burning process. We tested 50 such devices in this manner. From the data, we counted 86 SWNTs, 56 of which showed semiconducting behavior and 30 of which showed metallic behavior. The ratio, then, is ~1.9. The similar results have been reported previously by different groups who used the similar growth technique (31-34).

5.3.6 Derivation of Non-dimensional Potential along Tube

The equation is derived from Drift-Diffusion Equation

$$J = q\mu\, n\frac{dV}{dx} + qD\ \frac{dn}{dx} \qquad (1)$$

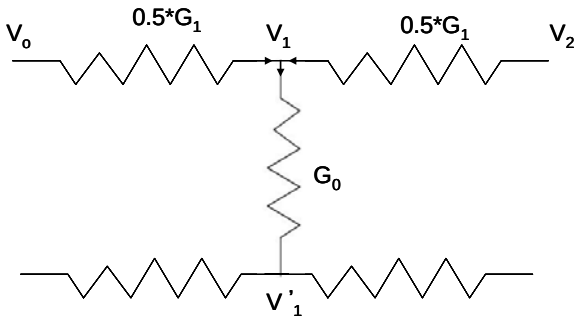
and Carrier Continuity Equation

$$\frac{1}{q}\frac{dJ}{dx} = 0\,. \quad (2)$$

For linear voltage-current regime (gate voltage V_g=constant and drain voltage V_{sd} ~ small), the carrier concentration is uniform across the channel, therefore one need not solve the Poisson equation explicitly. Since the channel length is several microns long, contact resistance is unimportant and scattering dominated drift-diffusion theory apply. However, in the linear response regime, the diffusion term is negligible compared to the drift term in Eq. (1), therefore Eqs. (1) and (2) can be combined to obtain

$$q\mu n\frac{d^2V}{dx} = 0 \ \Rightarrow \sigma\frac{d^2V}{dx^2} = 0 \qquad (3)$$

where V is the potential and σ is the conductivity. Eq. (3) applies to transport in isolated tubes. To understand the modification of Eq. (3) for intersecting tubes, consider the following derivation. When two tubes intersect each other, the tube resistance and the contact resistance can be represented by the circuit below.



The respective voltages are shown in the figure above. Using Kirchoff's law, voltage drop-equation can be written as:

$(V_0 - V_1) \times \frac{G_1}{2} + (V_2 - V_1) \times \frac{G_1}{2} = (V_1 - V_1^{'}) \times G_0$, which can be rearranged as:

$$\frac{V_0 - 2V_1 + V_2}{2\Delta x^2} = (V_1 - V_1^{'}) \times \frac{G_0}{G_1 \Delta x^2}$$

$$\Delta x^2 \frac{d^2V}{dx^2}\bigg|_1 = C_{ij}(V_1 - V_1^{'}) \text{ where } c_{ij} = \frac{G_0}{G_1}$$

Now for two intersecting tubes i and j, the above equation takes following form (Kirchoff's law):

$$\frac{d^2V_i}{dx^2} - c_{ij}(V_i - V_j) = 0 \ ; \ c_{ij} = \frac{G_0}{G_1}$$

where V_i and V_j are the potentials of the tube i and j at the point of intersection, $G_0(\sim \frac{0.1e^2}{h})$ is the contact-conductance between the tubes and $G_1(\sim {}^{qn_{1D}\mu}\!/_{\Delta x})$ is the conductance of the tube. Here n_{1D} is the carrier density of tubes and $\Delta x(\sim 1e^{-6} cm)$ is the grid spacing. We find $c_{ij} \sim 50.0$ from the above calculations. Our simulations for nanotubes are reported for this value of c_{ij}. This equation can be written in non-dimensional form as:

$$\frac{d^2\phi_i}{ds^2} - c_{ij}(\phi_i - \phi_j) = 0$$

where s = x / Δx and ϕ is the non-dimensional voltage.

5.3.7 Effect of Variation of Metallic Tube Ratio

We used simulations to provide additional evidence that the fractions of metallic and semiconducting CNTs are close to 1/3 and 2/3, respectively. Figure 5.8 shows I_{on}, I_{off} and on/off ratio for four different values of f_M. I_{on} is not sensitive to f_M but the simulated I_{off} and on/off ratio match closely to the experimental results (symbols) only for f_M close to 1/3 and 1/4. The simulation results for f_M = 1/2 and 1/9 do not match experiment, suggesting that the fraction of metallic CNTs is close to 1/3. The values of f_M chosen for the simulations here are in the range of measured values by using electrical burning method.

5.4 Conclusion

A related finding is that our results imply that for transistors with $L_C > L_S$, perfect alignment is not optimal and would actually carry less current than slightly nonaligned systems. In this case, percolation dominates and high on/off ratios are possible even with a significant population of metallic tubes. On the other hand, short channel transistors ($L_C < L_S$), which are necessary for high performance technologies, have low on/off ratios, which reflect roughly the relative numbers of metallic and semiconducting tubes. In this regime, an approach for removing the effects of the metallic tubes might be necessary to produce acceptable devices (2,28,29). These and other predictions based on these models provide insights into methods to optimize SWNT films for various applications in electronics.

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5.6 Figures

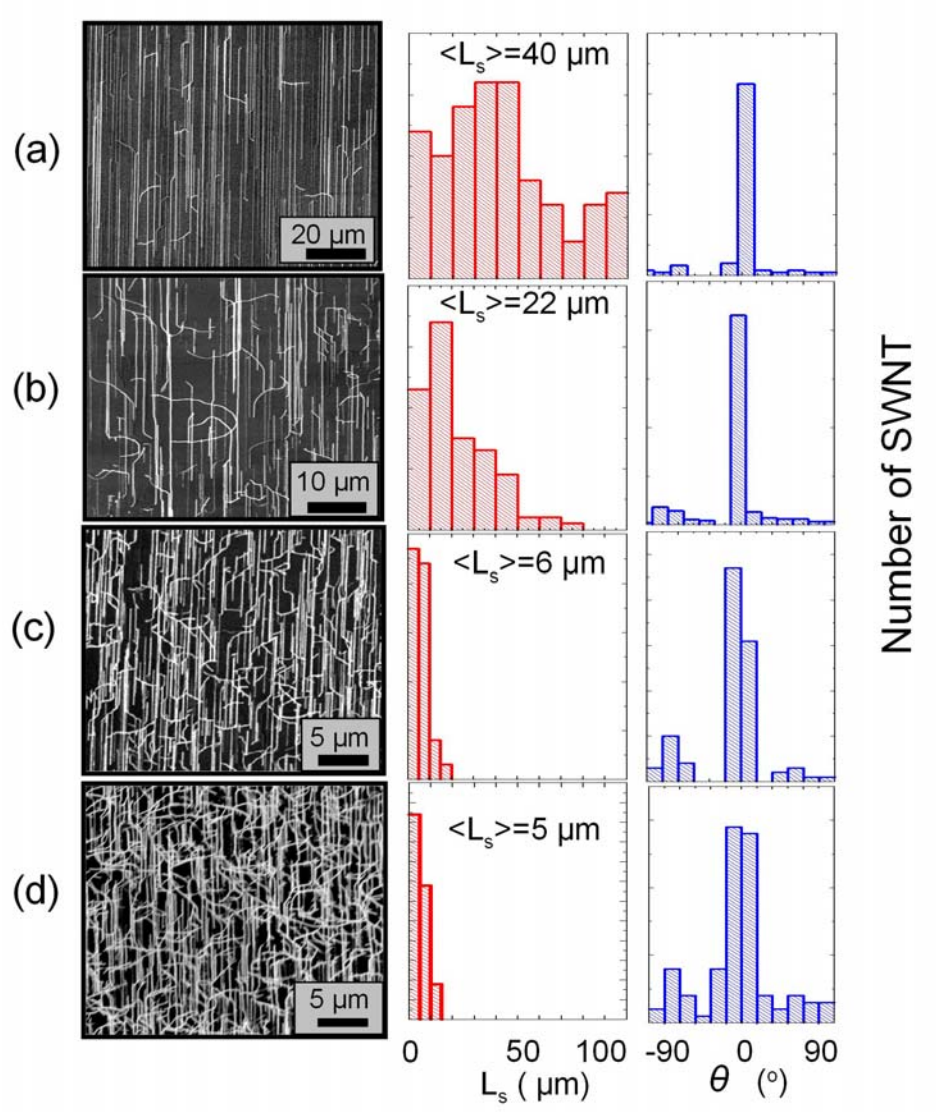

Figure 5.1 Scanning electron micrographs (SEMs) and statistical information on the four types of films of single walled carbon nanotubes that were studied. The films range from well aligned, low coverage (a) to partially aligned, high coverage (d) cases. The histogram plots show data for the tube length, L_s, and tube orientation, θ, determined from image analysis of the SEMs. The SWNTs in all cases have diameters between 1 and 3 nm.

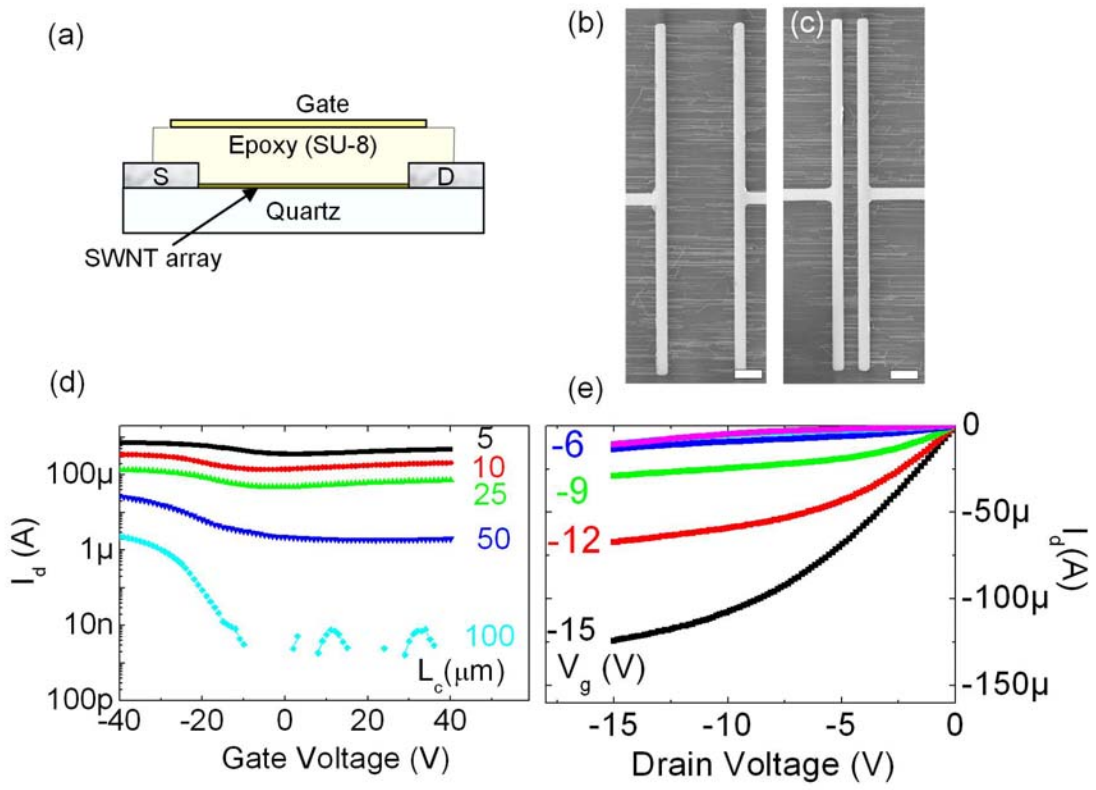

Figure 5.2 Device layout of thin film transistors fabricated on SWNT. (b) SEM images of S/D electrodes with SWNTs. Scale bar is 10 µm (c) Typical data collected from representative devices that reveal scaling properties of transport as a function of transistor channel length, L_C of 5, 10, 25, 50 and 100 µm, and output characteristics for 100 µm channel length (d).

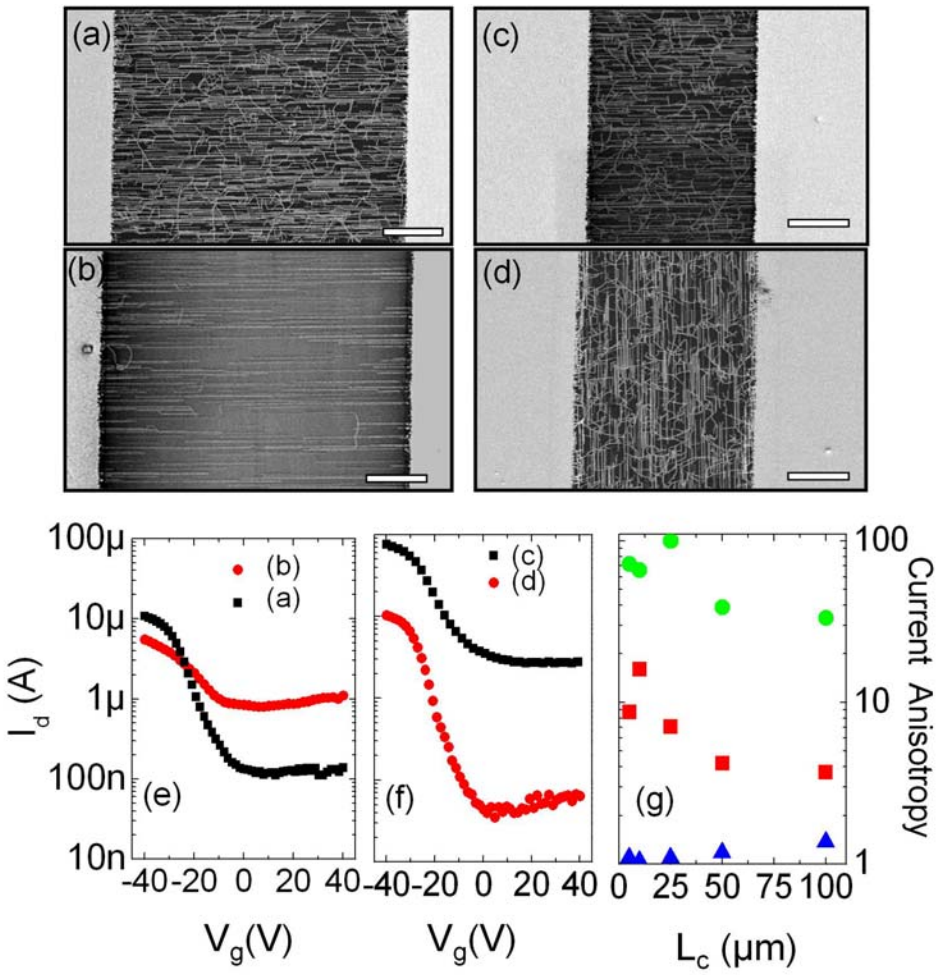

Figure 5.3 Scanning electron micrographs (SEMs) of transistors with channel lengths of 50 µm (a, b) and 25 µm (c, d) with different channel orientations and degrees of alignment and coverage. The scale bars are 10 µm. (e) Transfer curves of two devices with different tube coverage and the same channel length (L_c= 50 µm). (f) Transfer curves of devices with channels oriented parallel (\\, black) and perpendicular (⊥, red) to the alignment direction. (g) Channel length dependence of ON current anisotropy ($I_{\parallel}/I_{\perp}$) for aligned (green), dense partially aligned (red) and random network (blue).

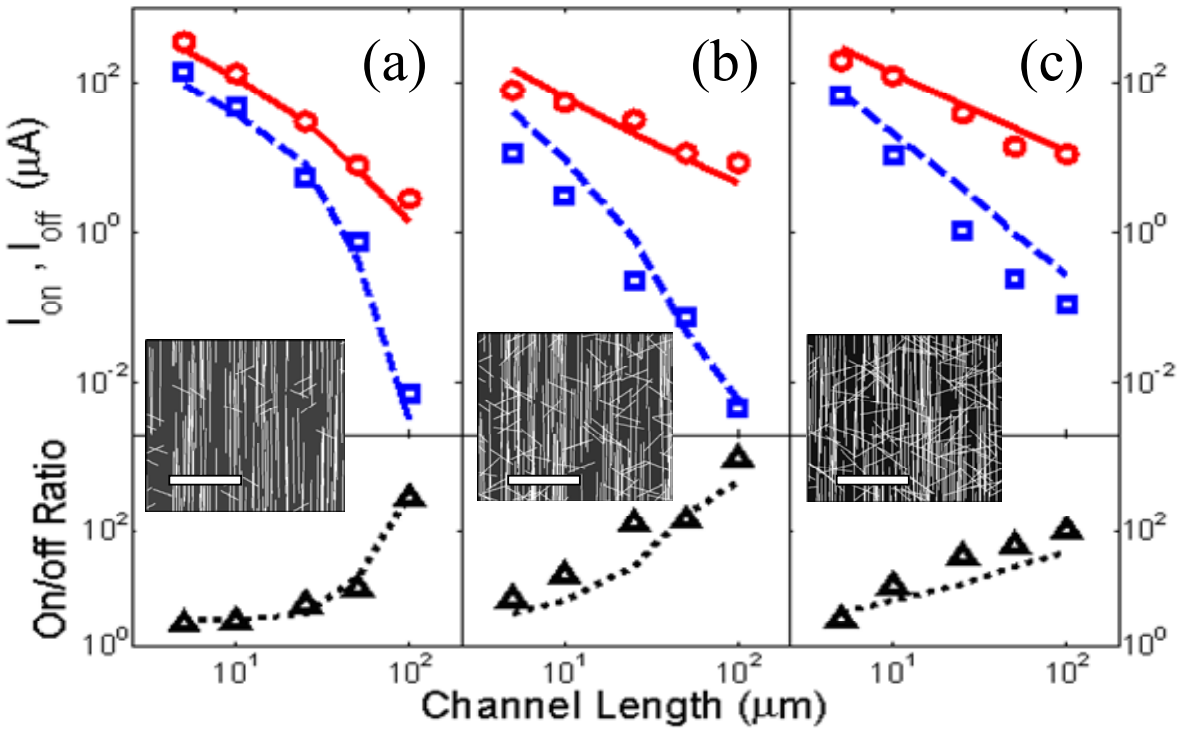

Figure 5.4 ON current I_{on}, OFF current I_{off}, and on/off ratio for (a) aligned, (b) partially aligned and (c) dense partially aligned networks corresponding to Figure 5.1 (a), (c), and (d), respectively, where the symbols show experimental and lines show simulation results. The current exponents, m_R (Eq. 1) for (a), (b), and (c) are given by, m_{on} = 1.7, ~1, and ~1, m_{off} = 4.8, 2.78, and 1.53, and the exponents for the on/off ratio = -3.1, -1.78, -0.53, respectively. The insets show the simulated networks with scale bar = 10 μm.

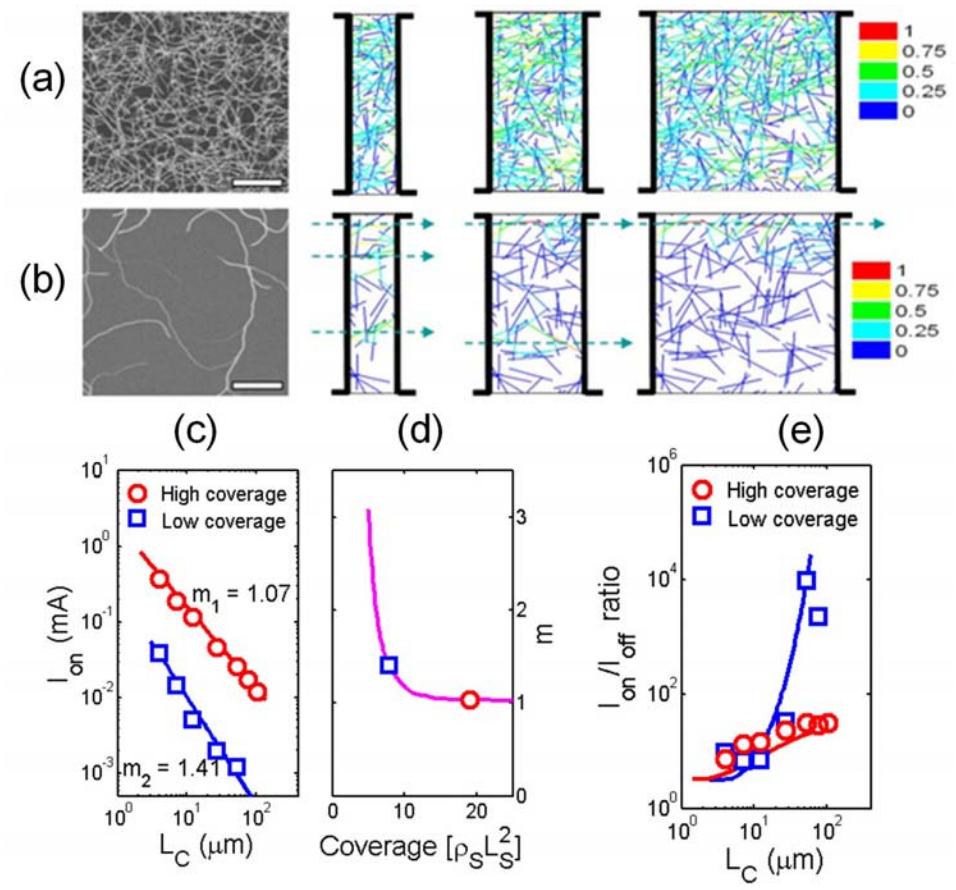

Figure 5.5 SEM images (scale bar is 5 μm) and simulated normalized current distribution for network with high (a) and low (b) coverage for L_C = 4, 8, 16 μm, respectively. The dotted arrows in show the current paths (c) Experimental (symbols) and simulated (lines) ON current (I_{on}) vs. channel length (L_C) for high (red circles, $\rho_S L_S^2 \sim 20$) and low (blue squares $\rho_S L_S^2 \sim 8$) coverage completely random network with current exponent $m_1 = 1.07$, and $m_2 = 1.41$, respectively. (d) Simulated current exponent (m) for random networks with coverage ($\rho_S L_S^2$) decreases monotonically with increasing $\rho_S L_S^2$ approaching the classical limit of m = 1 for higher coverage. The points indicated correspond to high (red circle) and low (blue square) coverage curves in c. (e) I_{on}/I_{off} ratio vs. channel length (L_C) for same coverage increases with L_C and the rate of increase is more for lower coverage.

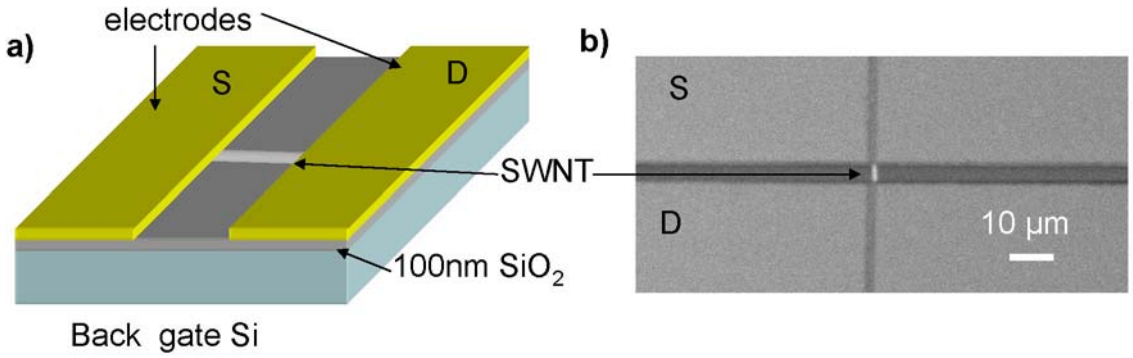

Figure 5.6 (a) Schematics of back gated SWNT field effect transistor, (b) SEM image of one of tested devices.

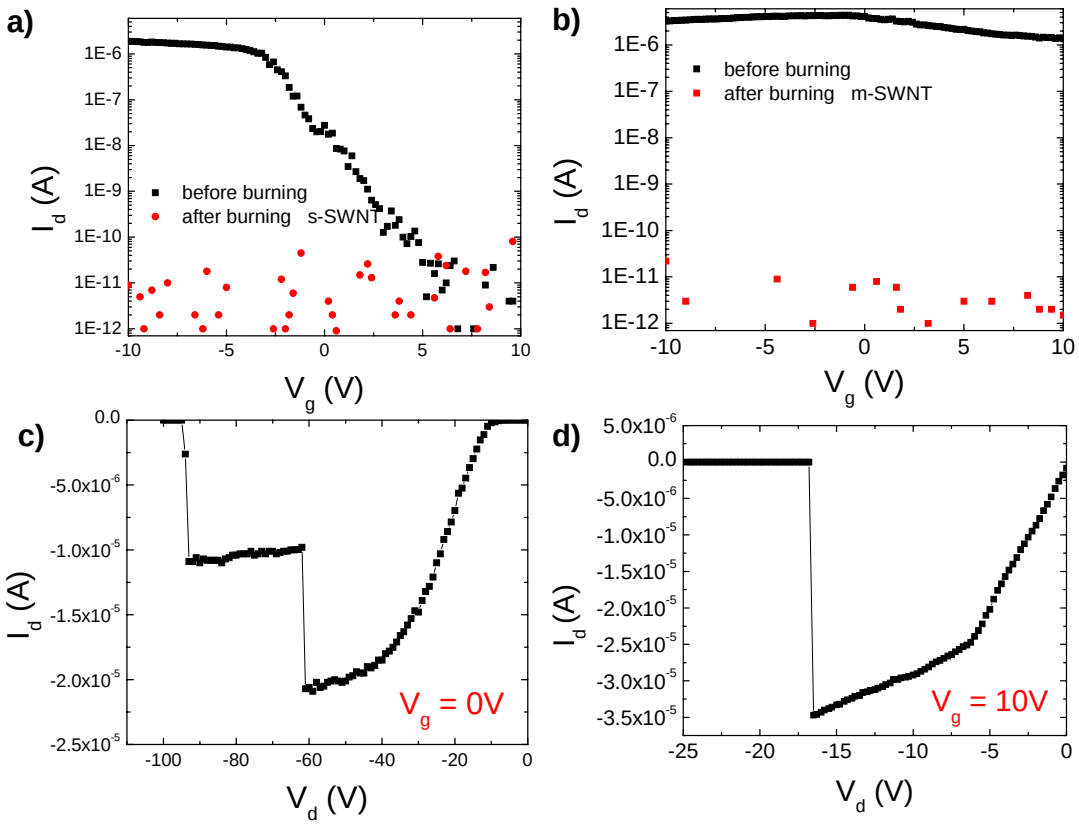

Figure 5.7 (a,b) Transfer curves for semiconducting and metallic SWNT . (c) electrical burning of two semiconducting and (d) one metallic SWNT. The number of tubes can be counted from the sharp current drops.

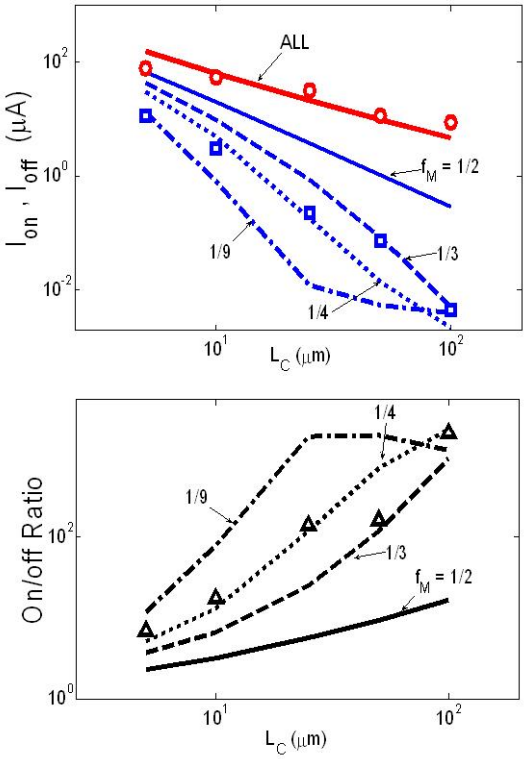

Figure 5.8 On current I_{on}, off current I_{off}, and on/off ratio for partially aligned networks corresponding to Fig 3 (b) in the paper, where the symbols show experimental and lines show simulation. The 4 lines correspond to metallic tube fraction of f_M = ½ (solid), 1/3 (dashed), ¼ (dotted) and 1/9 (dash-dot) as indicated. The simulation curves for I_{on} are overlapping.

CHAPTER 6 HIGH PERFORMANCE THIN FILM ELECTRONICS

This section was published as "High Performance Electronics Based on Perfectly Aligned Arrays of Single Walled Carbon Nanotubes Seong Jun Kang, **Coskun Kocabas** (equal contribution), Taner Ozel, Moonsub Shim, Ninad Pimparkar, Ashraf Alam, Slava Rotkin, John A. Rogers, *Nature Nanotechnology 2,* 230-236 (2007)" Reproduced with permissions from the journal. Copyright 2007, Nature Publishing Group

6.1 Introduction

Fundamental studies of charge transport through individual single walled carbon nanotubes (SWNTs) reveal remarkable room temperature properties, including mobilities more than ten times larger than silicon, current carrying capacities as high as 10^9 A cm^{-2} and ideal subthreshold characteristics in single tube transistors (1-4). The implications of these behaviors could be significant for many applications in electronics, optoelectronics, sensing and other areas (5-9). Devices that use single SWNTs as functional elements might not, however, form a realistic basis for these technologies, due in part to their low current outputs and small active areas. More important, integration of single tube devices into scalable integrated circuits requires a solution to the very difficult problem of synthesizing and accurately positioning large numbers of individual, electrically homogeneous tubes with linear geometries. The use of densely packed, perfectly aligned horizontal arrays of non-overlapping, linear SWNTs as an effective thin film electronic material has the potential to avoid these problems while retaining the attractive properties of the individual tubes. The multiple, parallel transport pathways in these arrays provide large current outputs and active areas, together with statistical averaging effects that lead to small device-to-device variations in properties, even with tubes that individually have widely different transport characteristics. Although theoretical work has examined some of the anticipated electrical properties of such arrays (10, 11), experimental results are lacking (12-14), due to difficulties associated with generating dense, large scale, aligned SWNTs at the extremely high degrees of alignment and linearity needed to avoid percolating transport pathways, tube/tube overlap junctions, electrostatic screening effects and non-ideal electrical properties (15-17). This paper presents high performance

p- and *n*-channel transistors and unipolar and complementary logic gates that use perfectly aligned arrays of long, pristine, individual SWNTs with perfectly linear geometries. The excellent properties of the devices derive directly from a complete absence, to within experimental uncertainties, of any defects in the arrays, as defined by tubes or segments of tubes that are misaligned or have non-linear shapes. This level of perfection represents several orders of magnitude improvement over previous results (12, 18-20). Analysis of measurements on these devices using rigorous models of the capacitance coupling of the arrays to the gate electrodes reveal device level properties that approach those of pristine individual tubes. These features together with the ability of these devices to provide both *p*- and *n*-type operation and CMOS circuit designs and their compatibility with a range of substrates suggest that these approaches have some promise for realistic SWNT based electronic and optoelectronic technologies.

6.2 Results and Discussion

6.2.1 Fabrication of Nanotube Arrays and Devices

Figure 6.1 shows scanning electron microscope (SEM) images of representative arrays of SWNTs, SEM images and schematics of their integration into transistors and some electrical properties. Chemical vapor deposition (CVD) on ST (Stable Temperature) cut quartz wafers using patterned stripes of iron catalyst and methane feed gas forms arrays of individual SWNTs with average diameters of ~1 nm, lengths of up to 300 μm, and densities (*D*) as high as ~5 SWNTs μm^{-1}. More than 99.9% of the SWNTs lie along the $[2,\bar{1},\bar{1},0]$ direction of the quartz, to within <0.01 degree, with perfectly linear configurations, to within the measurement resolution of an atomic force microscope[12]. This nearly ideal layout, especially as obtained at high *D*, is critically important to the device results presented here, and represents a significant improvement over previously reported results.(18-20) The simplest method to integrate these arrays into transistors begins with photolithography to define source and drain electrodes (Ti; 1 nm / Pd; 20 nm) on the SWNT/quartz substrates in regions between the catalyst stripes. Etching SWNTs outside of the channel region, spin casting a uniform epoxy gate dielectric (1.5 μm; SU8, Microchem Corp.) and photolithographically defining top gate

electrodes (Ti; 1 nm / Au; 20 nm) aligned to the channel regions yields arrays of electrically isolated transistors. Figure 6.1b and Figure 6.1c shows schematic illustrations and images. We formed devices in this manner with channel lengths (L) between 5 and 50 μm, all with widths (W) of 200 μm. For these geometries, each device incorporates ~1,000 perfectly linear, parallel SWNTs in the channel, most (e.g. >80%, even for L = 50 μm) of which span the source/drain electrodes. This large number of active tubes per device provides high current outputs and good statistics for uniform, reproducible properties. Figure 6.1d presents measurements that show a ~10% standard deviation in source/drain currents, I_D, measured in more than one hundred two-terminal test structures (source/drain voltage, V_D = 10 V; L = 5 μm; W = 200 μm). We observe high yields both for growing the arrays and for building devices that incorporate them.

Figure 6.1e shows typical transfer characteristics measured from a set of devices. The responses indicate *p*-channel behavior, consistent with observations in single tube devices that use similar materials and designs. The large current outputs are consistent with the high channel conductance provided by the multiple tubes. These currents vary approximately linearly with the channel length, indicating diffusive transport, with ratios of the on to off currents in a range (between ~2.3 and ~5) consistent with the relative populations of metallic and semiconducting SWNTs. Resistances of the semiconducting tubes in their 'on' state (i.e. biased to gate voltages, V_G, of -50 V), are 36 +/- 10 $k\Omega\mu m^{-1}$ for L = 50 μm, where the effects of contacts are least significant. Single tube device results, computed using reported diameter dependent resistances (1) and diameter distributions measured from these arrays, yield a resistance of ~21 $k\Omega\mu m^{-1}$. Similar calculations for the metallic tubes in these devices yield higher and lower resistances in the low and high bias regimes, respectively, than the best single tube device measurements (14, 21-23).

6.2.2 Capacitance Coupling and Mobility Calculation

The low on state resistances of the semiconducting tubes yield excellent device level transistor properties. Figure 6.1f presents linear regime device mobilities as a function of channel length, computed from the transfer curves, the physical widths of the

source/drain electrodes (W = 200 μm), and a parallel plate model for the capacitance, C, according to $\mu_{dev} = \frac{L}{WC}\frac{1}{V_D}\frac{\partial I_D}{\partial V_G}$. These mobilities are as high as ~1100 cm^2 V^{-1} s^{-1} for L > 25 μm, decreasing with L, likely due to effects of contacts(1,24,25) that are not considered explicitly in these calculations. The validity of this simple parallel plate model for the capacitance can be explored through measurements and calculations for devices with different D. Figure 6.2a and Figure 6.1b present SEM images of SWNT arrays with D between ~0.2 SWNTs μm^{-1} and ~5 SWNTs μm^{-1}, obtained by controlling the growth conditions. The responses of devices built with these arrays and with single tubes are similar to those in Figure 6.1. The influence of fringing fields and partial electrostatic screening by the tubes on the capacitance, C, are important in this range of tube spacings and gate dielectric thickness (1.5 μm)(10, 11). Figure 6.2c and Figure 6.2d present results of calculations that include these effects, the quantum nature of the tubes and their intrinsic capacitance for D = 5 SWNTs μm^{-1}, where screening is dominant, and 0.2 SWNTs μm^{-1}, where it is small. In the former regime, the calculated C differs, only by ~10%, from that determined by a simple parallel plate model. In the latter case, the capacitance coupling to each individual tube is nearly the same as that for isolated tubes.

Such models enable calculations of the average per tube mobilities, which we denote as $< \mu_t >$, according to $< \mu_t >= \frac{L}{WC_t D_s}\frac{1}{V_D}\frac{\partial I_D}{\partial V_G}$ where C_t is the capacitance per unit length for a semiconducting tube in the array (computed using D), and D_s is the density of semiconducting tubes that span the channel. For L = 50 μm and D = 5 SWNTs μm^{-1}, $< \mu_t >$ ~2,200 ± 130 cm^2 V^{-1} s^{-1}, if we assume that ~2/3 of the SWNTs in the channel are semiconducting and that ~80% of them span the source and drain electrodes. As with the device mobility, the per tube mobility (as computed in a manner that does not account for the contacts) decreases with channel length (e.g. ~570 cm^2 V^{-1} s^{-1}, L = 5 μm), which is qualitatively consistent with expectations based on reports on single tube devices (1,24-26). Averaging the diameter dependent mobilities inferred from single tube devices[1], weighted by the measured distribution of tube diameters in the arrays, yields ~3,000 cm^2 V^{-1} s^{-1} if we assume that most of the 3-4 nm tubes are small bundles (~4,300 cm^2 V^{-1} s^{-1}

without this assumption). This value is only somewhat higher than the results determined from measurements on the array devices. An analysis of per tube mobilities in devices with various tube densities at L = 10 μm, where the effects of contacts are significant, yields $< \mu_t > \sim 800 \pm 100$ cm^2 V^{-1} s^{-1}, with a negligible systematic dependence on D. Similar mobility values are observed in single tube devices.

6.2.3 High Performance Nanotube Array Devices

Although the devices of Figure 6.1 and Figure 6.2 have high mobilities, their on/off ratios are modest, due to the presence of metallic tubes, and their transconductances are low, due to the use of low capacitance gate dielectrics. The on/off ratios can be improved by destroying the metallic tubes in a breakdown procedure that involves slowly increasing V_D, while holding V_G at a large positive value (Figure 6.3a) in a manner similar to previous demonstrations on random network and multiwalled nanotube devices (15, 27). To implement this procedure, the SWNT arrays were first transferred, with high yields, onto a substrate of epoxy (150 nm) / SiO_2 (100 nm) / Si, using an adaptation of previously reported techniques(28-30). The epoxy / SiO_2 bilayer and Si provided the gate dielectric and gate, respectively, in a backgate geometry that leaves the SWNTs exposed to air to facilitate the breakdown process. Transfer curves in Figure 6.3a, collected before and after this process for a typical case D = 4 SWNTs μm^{-1}, (L = 12 μm, W = 200 μm, V_D = -0.5V), demonstrate that the on/off ratios can be increased by four orders of magnitude, or more, in this manner. Figure 6.3b shows full current/voltage characteristics recorded after breakdown. The response is consistent with a well-behaved device (i.e. saturated and linear current outputs for $V_D >> V_G$ and $V_D << V_G$, respectively), offering large current output even with low operating voltages (selected to avoid hysteresis) and low capacitance dielectrics used here. The differences in threshold voltages observed in Figure 6.3a and Figure 6.3b result from hysteresis that occurs at the high voltages associated with measurements in Figure 6.3a. Increasing the capacitance of the gate dielectric improves the transconductance and eliminates the hysteresis. These aspects, as implemented in devices described in the following, also increase the voltage gain by more than an order of magnitude. In addition, extremely high current outputs can be obtained in this manner, especially in devices that use

interdigitated source and drain electrodes to increase W. Figure 6.3c and Figure 6.3d show images and electrical responses of such a device that uses an array of SWNTs (D = 7 SWNTs μm^{-1}) transferred onto a substrate of HfO_2 (10 nm) / Si where the HfO_2 serves as the gate dielectric and the Si provides the gate. In such a device, each SWNT in the array is active at multiple separate segments along its length, similar to related demonstrations in single tube systems (31). For this device, the output current reaches ~ 1 A at V_G = -2 V and V_D = -5 V, as illustrated in Figure 6.3d. The transconductance (g_m) computed using an effective width (W_{eff}) defined by the summed widths of the SWNTs that are active in the device, in a manner analogous to similar analyses of single tube devices(31), can also be high in such devices. Figure 6.3e shows results from devices that use slightly lower tube densities (D = 2 SWNTs μm^{-1}), non-interdigitated electrodes and various channel lengths. The peak values of transconductances scaled in this manner are ~800 S m^{-1} (at V_D = -0.5 V, L = 7 μm) with HfO_2 (10 nm) dielectrics and up to ~3,000 S m^{-1} (at V_D = -0.5 V, L = 5 μm) with polymer electrolyte gating (32).

6.2.4 Transfer Printing of Aligned SWNTs

The transfer process used for these devices also enables integration onto unusual substrates, including flexible plastics. As an example, Figure 6.3f and Figure 6.3g show an image and electrical characteristics of devices (D = 3 SWNTs μm^{-1}) on a sheet of poly(ethylene terephthalate) (180 μm), where polyimide (1.6 μm) and indium tin oxide (150 nm) provide the gate dielectric and gate, respectively, with L = 27 μm and W = 200 μm. The linear regime mobility, computed using a parallel plate approximation for the capacitance, is ~480 $cm^2 V^{-1} s^{-1}$. The inset of Figure 6.3g shows the normalized mobility as a function of bending induced strain (ε) for bending down to radii of curvature of 0.4 cm. At higher values of strain, the devices fail due to fracture of the gate electrode.

Many of the exceptional electrical properties can be obtained, at once, in suitably designed devices. Figure 6.4 provides optical micrographs and electrical measurements of such devices, formed on quartz growth substrates in top gate geometries similar those of devices of Figure 6.1 and Figure 6.2, but with high capacitance dielectrics and with

split gate electrodes aligned to the transistor channel to avoid parasitic overlap capacitances for high speed operation. The dielectric consists of a bilayer of HfO_2 (~10 nm) deposited by atomic layer deposition, on top of a layer of benzocylobutene (BCB, ~20 nm) spin cast on the SWNTs. Figure 6.4a-c show several devices that use arrays with D = 7 SWNTs μm^{-1}. The design enables high speed (radio frequency, RF) operation, and provides electrode pad layouts in the ground-signal-ground configuration to facilitate RF probing. The mobilities can be computed using the parallel plate model for the capacitance or using rigorous calculations similar to those for $< \mu_t >$ but which also include capacitance contributions from the metallic tubes. Figure 6.4d shows the results, along with the average per tube mobility, from measurements on 15 devices. The high mobilities and scaling behaviors are quantitatively similar to those of devices in Figure 6.1 The on resistances of the semiconducting tubes are also similar, ~40 $k\Omega\mu m^{-1}$. The current outputs are high, they scale linearly with W, and in an expected manner with L. Figure 6.4e and f show these results. The high capacitance gate dielectrics lead to transconductances scaled by W_{eff} as high as ~2900 S m^{-1}, as shown in Figure 6.4g. Behaviors in the upper end of the range for all of these properties are achieved in devices with L = 4 μm and W = 600 μm where, for example, the mobility, scaled transconductance and current output are 400 +/- 50 cm^2 V^{-1} s^{-1}, (using the parallel plate capacitance, ~160 nF/cm^2) ~3000 S m^{-1} and 8 mA, respectively. The mobility is 800 +/- 100 cm^2 V^{-1} s^{-1} when evaluated using the rigorous models for the capacitance (~70 nF/cm^2). These devices also have a strong potential for high speed operation. Measurements using a network analyzer (Agilent E5062A) indicate small signal gain up to frequencies (f_T) approaching 0.5 GHz, evaluated without any de-embedding.

6.2.5 Complementary Devices and Logic Gates

As illustrated in Figure 6.5a-c, coating the devices with polyethyleneimine (PEI) (15, 33) enables *n*-channel operation, similar to observations in single tube devices.(33) These results provide straightforward means to form complementary and unipolar logic gates (i.e. inverters), and other circuit elements. Figure 6.5d shows a PMOS inverter that uses an SWNT array based *p*-channel transistor (response shown in Figure 6.5b) as the drive and an array of SWNTs, partially processed by electrical breakdown, as the load.

Combining *n*- and *p*-channel devices yields CMOS inverters, as illustrated in Figure 6.5e. The gains observed in the PMOS and CMOS inverters were 2.75 and 1.8, respectively, as measured at V_{DD} = 5V for the PMOS device and V_{DD} = ±2 V for the CMOS device. Taken together, these and the other results presented in this paper indicate a scalable path to SWNT based thin film electronics, with high performance capabilities. Initial applications might be envisioned in areas that require unusual substrates (e.g. plastics), such as flexible displays or conformal structural health monitors, or optical transparency, such as heads-up displays and certain security devices. The high performance attributes combined with the possibility of direct integration with silicon also creates interest in the possible use of nanotube array devices with Si CMOS for enhanced operation (e.g. power handling capabilities, linear response or high speed operation). The array geometry should also be useful for a range of other applications, which currently exist only in the form of single tube demonstrations. Examples include light emitting diodes, photodetectors, chemical sensors, nanoelectromechanical oscillators, and electrically or thermally conductive elements. These and other related systems appear promising for future study.

6.3 Methods

6.3.1 Growth of Perfectly Aligned Arrays of Long, Linear SWNTs

Chemical vapor deposition (CVD) procedures were used to grow SWNTs on ST cut quartz wafers (Hoffman Inc.) that were annealed at 900° C in air for 8 hours. The first step of the growth process involved photolithography to open lines (W = 10 μm and L = 1 cm) in a layer of photoresist (AZ 5214) on the quartz followed by electron beam evaporation (3×10^{-6} Torr; Temescal CV-8) of Fe (Kurt J. Lesker Co.; 99.95%) to a nominal thickness of <0.5 nm. Lifting off the photoresist with acetone left a pattern of Fe lines. Annealing the Fe at 550° C in air formed isolated iron oxide nanoparticles with diameters near ~1 nm. The particles served as the catalytic seeds for CVD growth of the SWNTs. Purging with hydrogen at 900°C for 5 min and then introducing a flow of methane (1900 standard cubic centimeters per minute (sccm)) and hydrogen (300 sccm) at 900 °C for 1 hour led to the growth of SWNTs.

6.3.2 Fabrication of Top and Bottom Gate Transistors

To make top gate transistors on the quartz growth substrates, Ti (1 nm)/Pd (20 nm) (electron beam evaporated at $3x10^{-6}$ Torr; Temescal CV-8) source/drain electrodes were formed by photolithography and lift-off. For device isolation, these electrodes and the channel region were covered with photoresist, the exposed tubes were removed by reactive ion etching (50 mTorr, 20 sccm O_2, 30 watt, 30 sec), and then the resist was washed away with acetone. A spin cast layer of a photodefinable epoxy (SU8-2, Microchem Corp.) formed the gate dielectric. On top of this layer, we defined the gate (Ti (1 nm)/Au (20 nm)) using photolithography and lift-off. Reactive ion etching through the epoxy, using a layer of photoresist as a mask, created openings to enable probing of the source and drain electrodes. For the high performance devices of Figure 6.4, spin casting and atomic layer deposition techniques defined high capacitance bilayer dielectrics of BCB and HfO_2. In addition, gate electrodes with widths comparable to the channel length provided low overlap capacitances for high speed operation. The electrodes layouts match probing configurations for high speed measurements with a network analyzer.

For bottom gate devices, the SWNT arrays were transferred from quartz onto other substrates. To pick up the aligned tubes, a 100 nm layer of Au was first deposited on the nanotubes/quartz by electron beam evaporation ($3x10^{-6}$ Torr, 0.1 nm sec^{-1}; Temescal CV-8). On top of this Au layer, a film of polyimide (polyamic acid, Aldrich) was spin coated at 3000 rpm for 30 seconds and cured at 110 °C for 2 minutes. Physically peeling away the PI/Au/SWNT film lifted the tubes off of the quartz with nearly 100% transfer efficiency. Placing this film on the receiving substrate (SiO_2 / Si) coated with an adhesive layer of SU8-2 (150 nm) and then etching away the PI by reactive ion etching (150 mTorr, 20 sccm O_2, 150 watt 35 min) left the Au/SWNTs film on the substrate. Photolithography and etching of the Au (Au-TFA, Transene Co.) defined Au source and drain electrodes. In the final step of the fabrication, SWNTs outside of the channel regions were removed by reactive ion etching to isolate the devices.

6.3.3 Polymer Electrolyte and HfO_2 Gate Dielectrics

To achieve high transconductances, we used high capacitance gate dielectrics consisting of either 10 nm HfO_2 or a polymer electrolyte. The electrolytes were made by directly dissolving $LiClO_4*3H_2O$ in poly(ethylene oxide) (PEO, M_n = 550) or in polyethylenimine (PEI, M_n = 800) in air at room temperature with 2.4:1 and 1:1 polymer to salt weight ratios, respectively. The electrolytes were injected into a polydimethylsiloxane (PDMS) fluidic channel laminated over aligned arrays of SWNTs on quartz substrates with source/drain electrodes defined according to the previously described procedures. In these devices, gate voltages were applied through a silver wire dipped in the electrolyte. The HfO_2 was prepared on a doped silicon substrate by atomic layer deposition (ALD) (Savannah 100, Cambridge NanoTech Inc.) using H_2O and $Hf(NMe_2)_4$ (99.99+%, Aldrich) and a substrate temperature of 150 C. SWNT arrays were transferred onto the HfO_2 using procedures described above, but without the adhesive layer. Photolithography and etching defined Au electrodes for source and drain.

6.3.4 Fabrication of N-type Transistors, CMOS and PMOS Logic Gates

Spin coating layers of PEI (M_n = 800, Aldrich.) on the top of the nanotubes switches the operation of the transistors from unipolar *p*-channel to unipolar *n*-channel. To form these coatings, PEI was first dissolved in methanol with a volume concentration of 1:5. Spin casting the PEI directly onto the SWNTs at 2000 rpm for 30 seconds created the coatings. Heating at 50 C for 10 hours gave *n*-channel TFTs. Suitable interconnection of such devices can yield logic gates of various types. For PMOS inverters, one transistor served as a resistor load, while the other served as the drive. CMOS inverters were formed with uncoated p-channel devices and PEI coated n-channel devices.

6.4 References

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6.5 Figures

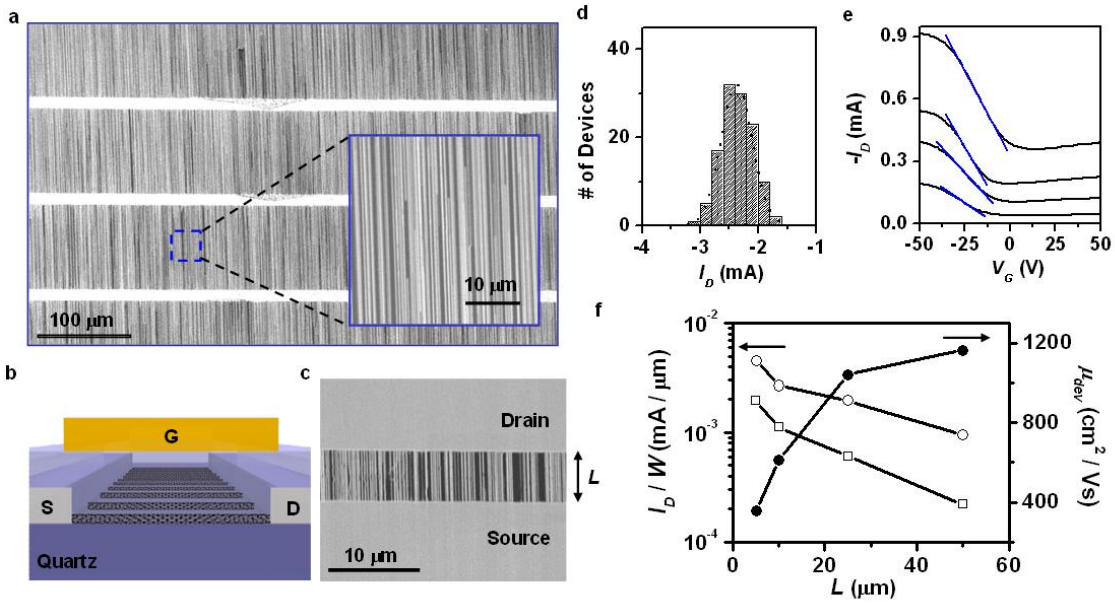

Figure 6.1 a, Scanning electron microscope (SEM) image of a pattern of perfectly aligned, perfectly linear SWNTs formed by chemical vapor deposition growth on a quartz substrate. The bright horizontal stripes correspond to the regions of iron catalyst. The inset provides a magnified view. These arrays contain ~5 SWNTs μm^{-1}. **b,** Schematic illustration of the layout of a type of transistor that incorporates these aligned SWNTs as the semiconductor. The device uses source, drain and gate electrodes and a dielectric layer formed sequentially on top of the SWNTs on quartz. **c,** SEM image of the channel region of such a device. The distance between the source and drain electrodes defines the channel length (L). **d,** Output currents (I_D) measured on more than one hundred two terminal test structures using electrodes with widths, W, of 200 μm and separated by distances (i.e. channel lengths), L, of 7 μm, evaluated with an applied potential, V_D, of 10 V. **e,** Transfer curves (i.e. I_D as a function of gate voltage, V_G) measured from transistors with L = 5, 10, 25, and 50 μm, from top to bottom, and W = 200 μm at V_D = -0.5 V. Blue lines show the linear regions of the transfer curves. These devices used polymer gate dielectrics, with thickness of ~1.5 μm. **f,** Width normalized on and off currents (open circles and squares, respectively) and linear regime device mobilities (solid circles; μ_{dev}) as a function of L.

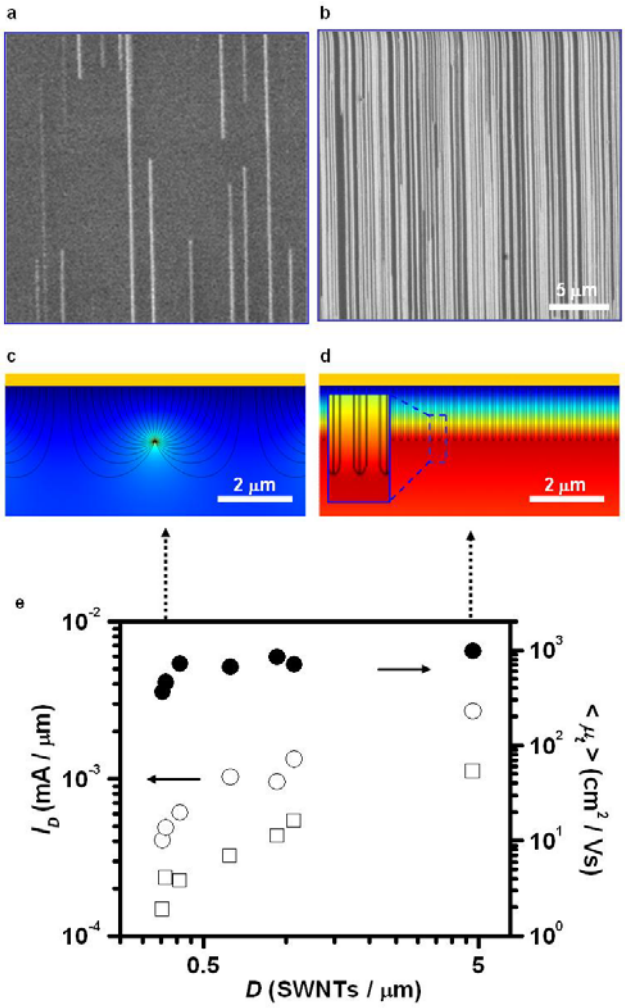

Figure 6.2 a, Scanning electron microscope (SEM) images of an array of aligned SWNTs with ~0.2 SWNTs μm^{-1} and **b,** with ~5 SWNTs μm^{-1}. **c,** Color contour plots and electric field lines for the computed electrostatic coupling of a gate electrode (top yellow plate) through a dielectric layer to an array of SWNTs with low density (i.e. average spacing between the SWNTs is larger than the gate dielectric) and **d,** with high density (i.e. average spacing between the SWNTs is smaller than the gate dielectric). The former and latter results show field distributions that are similar to those associated with an isolated tube and a parallel plate, respectively. **e,** Width normalized on and off currents (open circles and squares, respectively) measured in transistors built with arrays of SWNTs with different densities, *D*. The thickness of the gate dielectric was ~1.5 μm.

The plot also shows the average per tube mobilities (solid circles; $< \mu_t >$) computed from transfer curves measured from these devices.

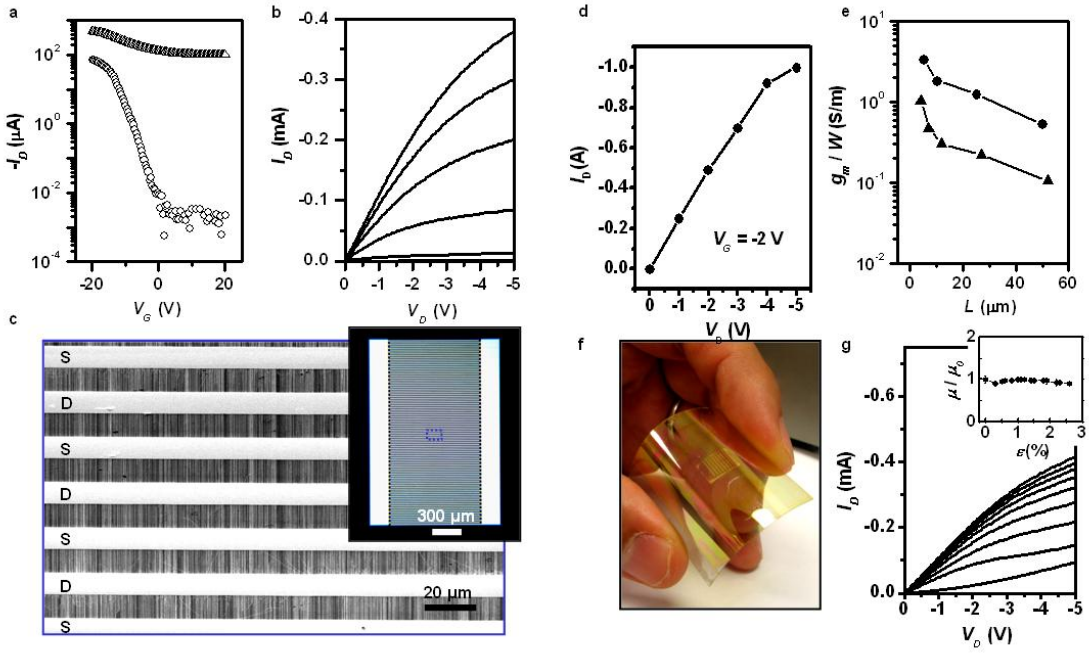

Figure 6.3 **a,** Transfer curves from a transistor (L = 12 μm, W = 200 μm) that uses aligned arrays of SWNTs (D = 4 SWNTs μm^{-1}) transferred from the quartz growth substrate to a doped silicon substrate with a bilayer dielectric of epoxy (150 nm) / SiO_2 (100 nm). The data correspond to measurements on the device before (open triangles) and after (open circles) an electrical breakdown process that eliminates metallic transport pathways from source to drain. This process improves the on/off ratio by a factor of more than 10,000. **b,** Full current-voltage characteristics of the same device, measured after breakdown, illustrating a well behaved response. The gate voltage varies from -5 V to 5 V (top to bottom). **c,** Optical (inset) and scanning electron microscope (SEM) images of a transistor that uses interdigitated source and drain electrodes, in a bottom gate configuration with a gate dielectric of HfO_2 (10 nm) on a substrate and gate of Si. The width and length of the channel are 93 mm and 10 μm, respectively. The box indicated by the dashed blue lines in the optical image inset delineates the region shown in the SEM image. **d,** Output current (I_D) as a function of V_D at V_G = - 2 V, for the device shown in part c. High on currents (up to ~1 A) can be obtained. **e,** Transconductance per unit effective width (g_m / W_{eff}) as a function of channel length (L), for devices (D = 2

SWNTs μm^{-1}) that use a polymer electrolyte gate (solid circles; V_D = -0.5 V) and a 10 nm HfO_2 (solid triangles; V_D = -0.5 V) gate dielectric, respectively. **f,** Optical image of an array of SWNT transistors with D = 3 SWNTs μm^{-1}, on a flexible plastic substrate (PET), and L = 27 μm and W = 200 μm. **g,** Current voltage characteristics of a typical device. The gate voltage varies from -20 V to 20 V (top to bottom). The linear regime field effect mobility was ~480 cm^2 V^{-1} s^{-1}, representing the highest *p* channel mobility reported for a device on plastic. The inset shows the variation of the normalized mobility as a function of bending induced strain, down to a radius of curvature of 0.4 cm. Beyond this degree of bending, failure occurs due to fracture of the gate electrode.

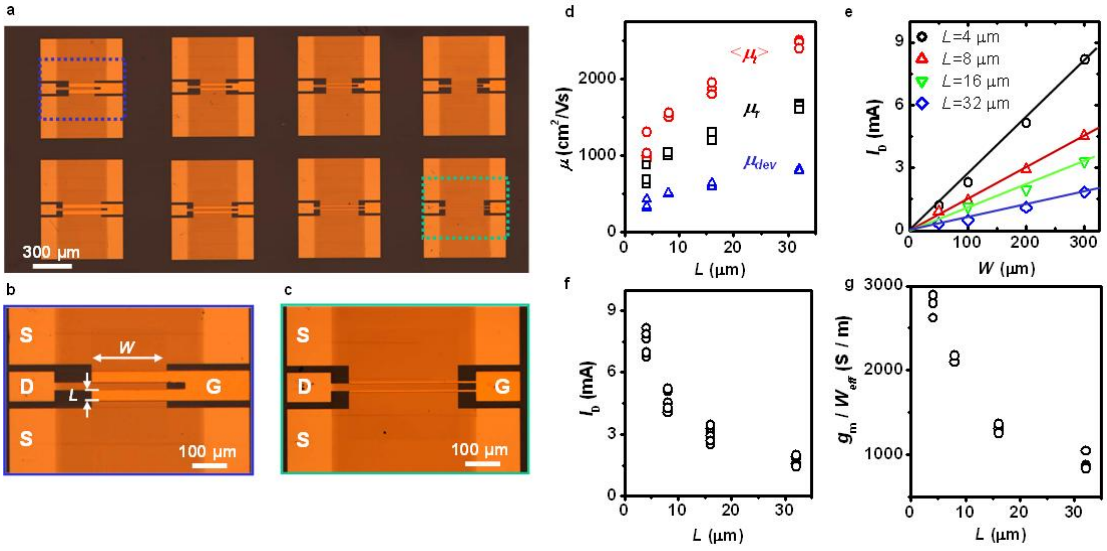

Figure 6.4 a, Optical micrograph showing an array of eight transistors that use SWNT arrays for the semiconductor, the quartz growth wafer as the substrate, high capacitance bilayer gate dielectrics of BCB (20 nm) / HfO_2 (10 nm) and split gate electrodes aligned to the channels of the devices. **b**, Optical micrograph of a device with L = 32 μm and W = 200 μm, corresponding to the box indicated by the dashed blue line in the left portion of part **a**. **c**, Optical micrograph of a device with L = 4 μm and W = 300 μm, corresponding to the box indicated by the dashed green line in the right portion of part **a**. **d**, Mobilities computed using parallel plate (μ_{dev}, blue triangles) and rigorous (μ_r, black squares) models for the capacitance coupling between the gate electrode and the SWNT

arrays. The plot also shows the average per tube mobilities (<μ_t>, red circles). **e**, Output currents, I_D (V_D = -1 and V_G = -1 V), for devices with L = 4, 8, 16 and 32 μm at W = 50, 100, 200 and 300 μm. **f**, Output currents, I_D (V_D = -1 and V_G = -1 V), for 18 devices with L between 4 and 32 μm. g, Scaled transconductances (g_m / W_{eff}) for 15 devices with L between 4 and 32 μm.

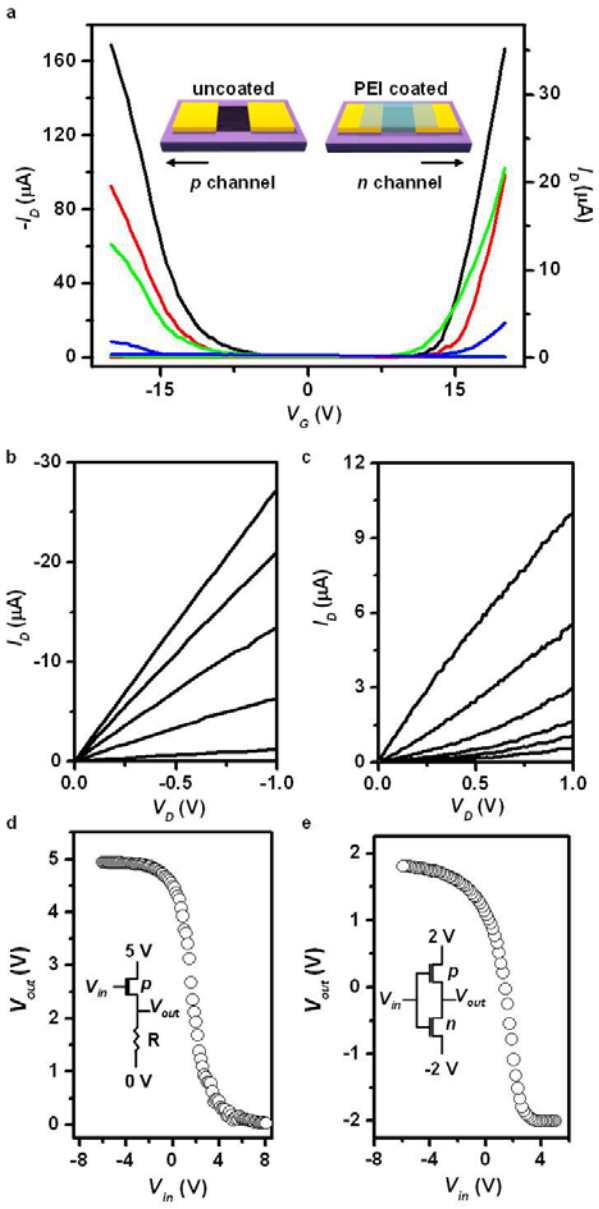

Figure 6.5 a, Transfer curves of *p*- and *n*-channel transistors that use aligned arrays of as fabricated and PEI coated arrays of SWNTs, respectively. All devices were processed

using electrical breakdown to achieve high on/off ratios. In the case of the *n*-channel devices, this process was performed before PEI coating. (L = 4 μm (black), L = 7 μm (red), L = 12 μm (green), L = 27 μm (blue), V_D = -0.5V) b, Current-voltage response of a typical *p* channel device in a regime of small V_D. (V_G = 5V ~ -5V) c, Similar results from an *n* channel device. (V_G = 0V ~ 5V) d, Transfer curve from a PMOS inverter that uses a SWNT array transistor for the drive, and a two terminal device with SWNT arrays for the resistive load. The gain of the PMOS inverter is 2.75. The inset provides a circuit schematic. e, Similar information for a CMOS inverter that combines *p*- and *n*-channel SWNT array transistors. The gain of the CMOS inverter is 1.8

CHAPTER 7 TRANSFER PRINTING OF SWNT ARRAYS

This chapter is submitted for publication in Nano Letters as "Printed Multilayer Superstructures of Aligned Single-Walled Carbon Nanotubes for Electronic Applications Seong Jun Kang, **Coskun Kocabas**, Hoon-Sik Kim, Qing Cao, Matthew A. Meitl, Dahl-Young Khang, John A. Rogers". Reproduced (or 'Reproduced in part') with permission from Nano Letters, in press (or 'submitted for publication'). Unpublished work copyright 2007 American Chemical Society.

7.1 Introduction

Single-walled carbon nanotubes (SWNTs) might represent an interesting semiconductor material for electronic applications, as suggested by the high current-carrying capacities, ideal subthreshold behavior and high field effect mobilities that can be achieved in single tube devices (1-3). Although devices of this type can be used to achieve representative demonstrations in electronics, optoelectronics, sensing and other areas, their integration into a scalable technology poses many significant challenges (4-8) One approach to avoid these difficulties relies on collections of tubes, either as random, sub-monolayer networks (9-11) or, preferably, horizontally aligned arrays (12-16), as effective thin film type semiconductors. Films based on arrays can, in fact, be used to form transistors and simple circuits (i.e. logic gates) with reproducible, device level characteristics that approach expectations based on some of the best single tube devices (12). Certain applications, however, require collections and layouts of tubes that are more complex than simple aligned arrays or random networks. Synthetic approaches for such configurations, sometimes in multilayer layouts, are therefore of some interest. Recent reports show that methods based on gas flow (17) and electrospinning (18) and electric fields (19,20) can provide some useful capabilities. Drawbacks include some combination of moderate to low densities, uncertain uniformity and electrical properties, and complex fabrication processes. In this paper, we present a strategy that involves the guided growth of aligned arrays, random networks and complex combinations of arrays and networks of SWNTs, followed by physical transfer of these tubes, in multiple, sequential steps, to target substrates. This approach enables the formation of large scale

multilayer superstructures of complex layouts of SWNTs on substrates ranging from silicon wafers, to flat and curved glass plates to thin plastic sheets. Electrical measurements illustrate some of the properties of several layouts of tubes formed in this manner.

7.2 Methods and Materials

The first step of the process, which is illustrated in its entirety in Figure 7.1, involves the growth of collections of SWNTs, typically at coverages somewhat less than a monolayer. We used recently reported chemical vapor deposition (CVD) growth techniques with patterned and unpatterned catalyst on either single crystal quartz substrates for aligned arrays and random networks (12-14) or amorphous SiO_2/Si for random networks (21). The catalyst consisted of solution cast ferritin (Aldrich; diluted in DI water with concentration 4.25 mg/ml) for the random networks and sub-monolayers of iron (<0.5 nm) deposited by electron beam evaporation for the aligned arrays. Photolithographic techniques were used to define patterns of both types of catalyst, using procedures described elsewhere (12, 14). For all cases, the CVD growth used a flow of argon (10 sccm) and hydrogen (10 sccm) through an ethanol bubbler and a temperature of 925 °C. By combined control of the catalyst layout, the substrate type and the growth conditions, configurations of tubes ranging from random networks, to perfectly aligned arrays and anything in between, as well as integrated layouts of electrically connected random networks and aligned arrays in various geometries, are possible (12-15).

7.2.1 Transfer Printing of Aligned SWNT Arrays

The transfer process moves these collections of tubes from the growth substrate to another surface, without changing their coverage, geometry or other properties of their layouts. The general strategy involves first the deposition of a thin layer of solid material, which we refer to as the ‘carrier’, on top of the SWNTs. Next, a kinetically controlled printing process (22) with a soft, elastomeric stamp, peels this film from the growth substrate, and delivers it to a target substrate. Etching the layers off of the tubes completes the process. The materials for the carrier film are critically important; they must (i) effectively encapsulate the exposed parts of the SWNTs to enable their efficient removal from the growth substrate, (ii) provide a mechanically strong structural element

for peel-back, and (iii) remove easily from the SWNTs after transfer in a manner that does not degrade the properties of the SWNTs. We find that a bilayer of Au and either polyimide (PI) or polyvinyl alcohol (PVA) provides all of these required characteristics. The polymer provides physical toughness for clean separation. The metal can be removed from the SWNTs, by wet chemical etching, without significantly altering their properties or layouts. These selections, together with the kinetically controlled printing approach, which obviates the need for an etching step to lift off the SWNTs from their growth substrate, represent important differences between the transfer techniques described here and those previously reported (21). These differences lead to the ability to manipulate SWNT arrays, integrated arrays and networks as well as multilayer stacks in ways that were previously impossible, to enable the types of layouts presented here.

Figure 7.1 schematically illustrates the transfer process. The first step involved deposition of a thin layer of Au (~100 nm) by electron beam evaporation (3×10^{-6} torr; Temescal CV-8) onto the SWNTs. Spin casting (3000 rpm for 30 s) formed a partially cured film of polyamic acid (PI; polyamic acid, Aldrich) on top of this Au layer; heating at 110 °C for 2 mins removed the solvent and partially cured the PI. A flat slab of poly(dimethylsiloxane) (PDMS; Sylgard 184, Dow Corning) elastomer provided the stamp. Placing this stamp in conformal contact with the PI/Au/SWNTs/substrate, and then quickly peeling it away lifts the film of PI/Au/SWNTs off of the substrate, and leaves it van der Waals adhered to the surface of the stamp (Figure 7.1c). The stamp with the layers of PI/Au/SWNTs was then placed on a receiving substrate. Slowly peeling back the PDMS leaves the PI/Au/SWNT on this receiving substrate, thereby completing the transfer. The PI/Au carrier was removed by oxygen reactive ion etching (150 mtorr, 20 sccm O_2, 150 W, 35 mins) to eliminate the PI, followed by wet etching with a commercial solution (Au-TFA, Transene) to eliminate the Au. The process with PVA is similar, except that the PVA is dried 70 °C for 30 mins (instead of cured) after spin casting (speed, time, thickness) from a deionized (DI) water solution. The PVA can be removed by 10 min rinsing with DI water.

Figure 7.2a shows a scanning electron microscope (SEM) image of arrays of SWNTs grown on quartz and transferred to 100 nm SiO_2/Si. The inset provides an SEM image of the SWNT arrays on the growth substrate, collected before the transfer process.

The bright stripes in these images correspond to the regions of patterned iron catalyst, where dense random networks of SWNTs form. As the SWNTs emerge from these regions onto the bare quartz, they align with the $[2\bar{1}\bar{1}0]$ direction. (13) Figure 7.2b, c and Figure 7.2d, e show high magnification SEM images of the SWNTs arrays on quartz before transfer and after transfer to a thin (10 nm) layer of HfO_2 substrate on Si, respectively. As indicated by these images, the density, alignment, linearity and other features of the SWNT arrays are unaltered by the process. The atomic force microscope (AFM) image in Figure 7.2a shows nanotube arrays after transfer on 100 nm SiO_2/Si and a short exposure to H_2O_2: H_2SO_4 = 2:1, to eliminate residual byproducts from RIE of the PI. This image indicates that only a small amount of residue remains, such that the arrays of SWNTs can be seen clearly. Improvements in the processing might lead to even smaller residue, for applications that are critically sensitive.

This same procedure is compatible with random networks and other layouts of tubes. For example, patterning the catalyst into complex shapes on quartz leads to random networks of SWNTs in these regions, and aligned arrays in the other regions. Figure 7.3a and 3b show an example where the catalyst is in the geometry of a ring oscillator. The bright areas correspond to dense networks of tubes; these regions are interconnected by aligned arrays. Figure 7.3c and d present the same type of structure after transfer to SiO_2(100 nm)/Si. The efficiency in this case is similar to the simpler structures of aligned arrays. The same procedures can be used with other substrates, provided that they are sufficiently smooth to receive the Au/PI/SWNT layer. Figure 7.4a and 4c show, as examples, SWNTs arrays transferred to the curved surface of a glass tube and a thin sheet of plastic (Kapton, DuPont). These results suggest that high quality SWNT arrays can be integrated with wide ranging classes of substrates, important for imaging systems, flexible electronics and other applications.

7.2.2 Multilayer Superstructures of SWNTs

An important aspect of the approach is its ability to transfer tubes onto substrates that already support tubes can yield well-defined multilayer superstructures of SWNTs. For example, bilayer crossbar arrays can be formed by transferring an aligned array on top of another array, with a rotation of ninety degrees, as shown in Figure 7.5a. The

bright crossed lines correspond to the regions of catalyst in the two arrays. Figure 7.5b illustrates that crossbar arrays of SWNT, in the form of square mesh structures, exist inside each box defined by these catalyst lines. Transfer of random networks onto aligned arrays produces bilayer structures (Figure 7.5c and Figure 7.5d) with levels of in-plane anisotropy that can be defined by controlling the coverages of the random network and aligned array components. Similar procedures can be repeated to yield additional layers. For example, two transfer steps onto a target substrate with aligned arrays, using rotation angles of 60 degrees forms trilayer, triangular mesh structures, as shown in Figure 7.5e and Figure 7.5f.

7.2.3 Transparent Conductors and Field Effect Transistors

An obvious potential area of application of these structures of SWNTs is in electronics, either as field effect transistors, transparent conductors or related elements. For these and other applications, the ability to pattern electrodes, dielectrics and other materials by photolithography is important. We found that even in these multilayer configurations, the SWNTs are sufficiently adherent to the substrate to allow for spin casting of photoresist, patterned exposure, development and resist removal in a lift-off process that defines metal electrodes without substantially altering the coverage or arrangements of the SWNTs. To demonstrate this capability and to evaluate electrical properties of a representative multilayer SWNT structures, we formed collections of electrodes on the aligned arrays (a), the bilayer crossbar layouts (b) and the random networks (c) as shown in Figure 7.6. In this process, photolithography defined openings in a spin cast layer of photoresist (AZ 5214; 1.6 μm at 3000 rpm, Clariant). Blanket deposition of a bilayer of Ti (1nm)/Pd (20nm) by electron beam evaporation (3×10^{-6} torr; Temescal CV-8) followed by removal of the resist with acetone defined the electrodes. The geometry consisted of arrays of devices, each with four pads, either 40 × 40 or 20 × 20 μm in size, separated by 60 μm. To isolate these devices, the region between the electrodes was first protected by a patterned layer of photoresist (AZ 5214; 1.6 μm at 3000 rpm, Clariant) aligned to the devices. Reactive ion etching (50 mtorr, 20 sccm O_2, 100 watt, 30 sec) then removed the exposed SWNTs, and a rinse in acetone washed away the remaining resist. Figure 6 presents images of the types of devices that were

investigated. Current-voltage characteristics were measured in each case with various probing combinations using different pairs of electrodes (E1, E2, E3 and E4). As shown in Figure 7.7(a), the device with aligned arrays showed extremely strong anisotropy in the properties. In particular, current flowed only between electrodes E2 and E4; other probing combinations revealed currents at the noise limit of our setup. In the case of other devices (Figure 7.6 (b) and (c)), current was observed between all pairs of electrodes, due to the possibility of percolation pathways associated with tube/tube junctions. Using a definition of the anisotropy (A) according to

$$A = \left| \frac{I_x - I_y}{I_x + I_y} \right| \quad (1)$$

I_x is the current between E2 and E4, while I_y is the current between E1 and E3. We find that the aligned arrays have A = 1 (Figure 7.6(a)), the crossbar layouts have A = 0.04 (Figure 7.6 (b), which has a 105 tubes in x-direction while 85 tubes in y-direction), and the single layer random networks have A = 0.01 (Fig. 6 (c)). Moreover, if we change the number of tubes in each direction of crossbar layout, we can obtain various films with different anisotropy factors. For example, we obtained A= 0.14 (47 tubes in x-direction and 91 tubes in y-direction) and A= 0.08 (75 tubes in x-direction and 116 tubes in y-direction). These results demonstrate some flexibility in the levels of anisotropy that can be engineered into films of SWNTs by use of transfer approaches. Such layouts could be useful for various applications in chemical sensing, transparent electronics, light emitting devices, logic circuits and memory cells.

Next, we used these types of devices to determine, using the four-point probe method (Van der Pauw formula) (23), sheet resistances from the measured resistances between pairs of electrodes for crossbar arrays with different densities of tube/tube junctions, D. In particular, constant current was applied to E1 and E2 (and, separately, E2-E3, E3-E4 and E4-E1), while the voltage was measured between E3 and E4 (and, separately, E4-E1, E1-E2 and E2-E3). Sheet resistance of the film can be written (24) as $R_s = C(\lambda)R$, where $C(\lambda)$ is a correction coefficient, and λ is the ratio of contact length to total length of the boundary of the sheet.

$$e^{-\pi R_{vertical}/R} + e^{-\pi R_{horizontal}/R} = 1 \quad (2)$$

$$R_{vertical} = \frac{R_{E1-E2,E3-E4} + R_{E3-E4,E1-E2}}{2} \quad (3)$$

$$R_{horizontal} = \frac{R_{E2-E3,E4-E1} + R_{E4-E1,E2-E3}}{2} \quad (4)$$

$$R_{E1-E2,E3-E4} = \frac{V_{E3-E4}}{I_{E1-E2}} \quad (5)$$

Here, vertical and horizontal refer to the $\hat{x} + \hat{y}$ and $\hat{x} - \hat{y}$ directions, respectively. For the device geometry shown in Figure 7.7b, λ ~0.7 which provides correction coefficient of ~5. Figure 7.7(b) shows the results. The sheet resistances varied from ~66.5 kΩ/sq at *D*= ~1.4 juntions/μm^2 to ~31.5 kΩ/sq at *D*= ~7.7 juntions/μm^2. The sheet resistance of the random network in Figure 7.6 (c) is ~585 kΩ/sq at *D*= ~10 juntions/μm^2. The silicon substrate was grounded during the measurement. The two-terminal (E2-E4) resistance of the aligned nanotube film (Fig. 6a) is ~50 kΩ (surface coverage: ~0.5 %), while the value is ~495 kΩ for the random network nanotube film as shown in Figure 7.6c (surface coverage: ~1.1 %).

7.2.4 Conclusion

In summary, we developed a method for transferring and combining collections of SWNTs in a wide variety of formats ranging from random networks to perfectly aligned arrays, and integrated versions of these geometries. We demonstrated SWNTs arrays, formed by guided growth on single crystal quartz substrates, to other surfaces, including glass, plastic and high k films, without substantially altering the alignment or coverage of the SWNTs. Simple structures, including transparent conductors, demonstrate the electrical functionality of single and multilayer SWNT layouts. These results might be of interest for various applications of SWNTs in electronics, optoelectronics, sensors and nanomechanical systems.

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7.4 Figures

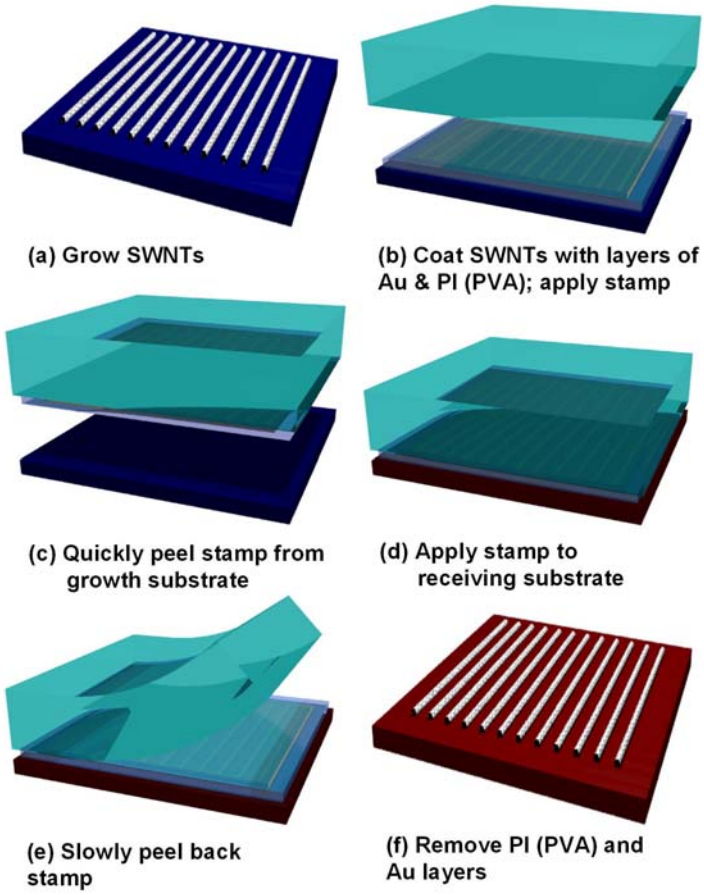

Figure 7.1 Schematic illustration of a printing-like process for transferring well defined collections of SWNTs from a growth substrate to a receiving substrate. The process consists of several steps, beginning with patterned growth of SWNTs (aligned arrays in this case) on a substrate (quartz in this case) by chemical vapor deposition (a), followed by deposition of a bilayer of Au/polymer (either polyimide, PI, or polyvinyl alcohol, PVA) as a 'carrier' film (b) and removal of the resulting SWNT/Au/polymer layer with an elastomeric stamp (c). Applying the stamp to a receiving substrate (d) and slowing peeling back the stamp leaves the SWNT/Au/polymer on the receiver (e). Finally, removing the polymer and Au by etching completes the process (f).

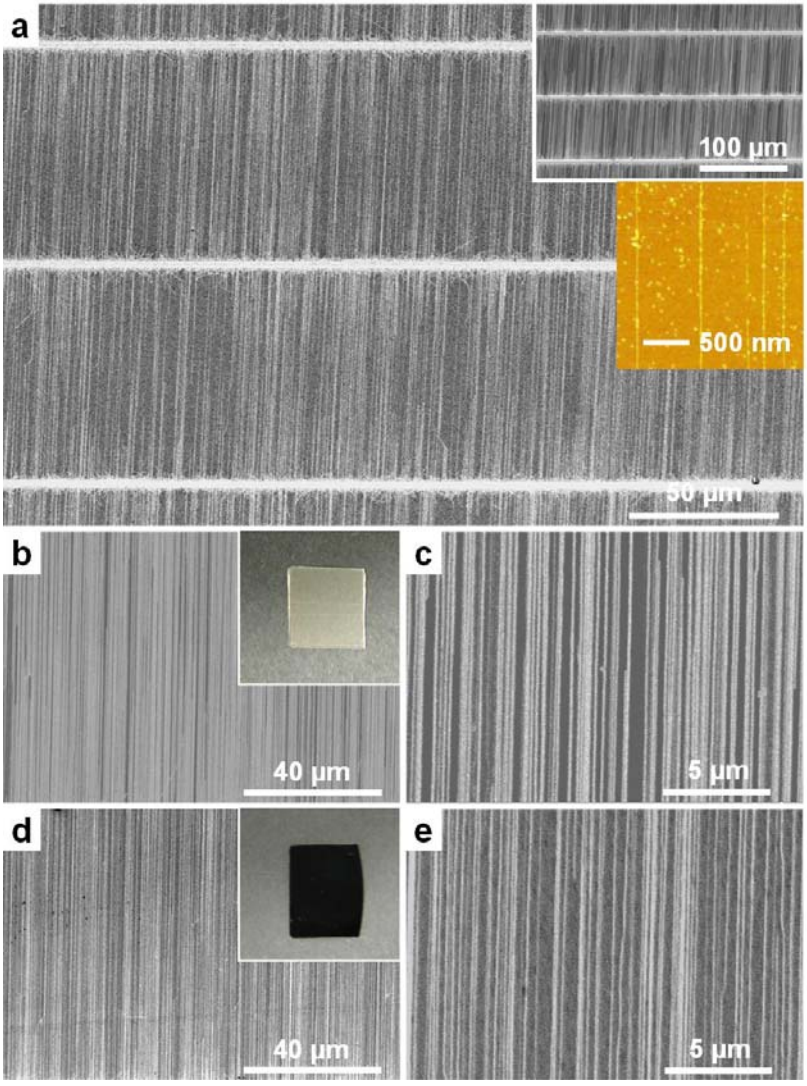

Figure 7.2(a) Scanning electron micrographs (SEMs) of aligned arrays of SWNTs transferred to a substrate of SiO_2 (100 nm)/Si. The inset shows an image of the SWNTs on quartz growth substrate before transfer. The inset atomic force micrograph shows SWNTs on SiO_2 (100 nm)/Si after transfer. (b), (c) SEMs of arrays of SWNTs on a quartz growth substrate. (d), (e) SEMs of arrays of SWNTs transferred to a receiving substrate of HfO_2 (10 nm)/Si. These images indicate that the alignment and density of the arrays are not changed substantially by the transfer process.

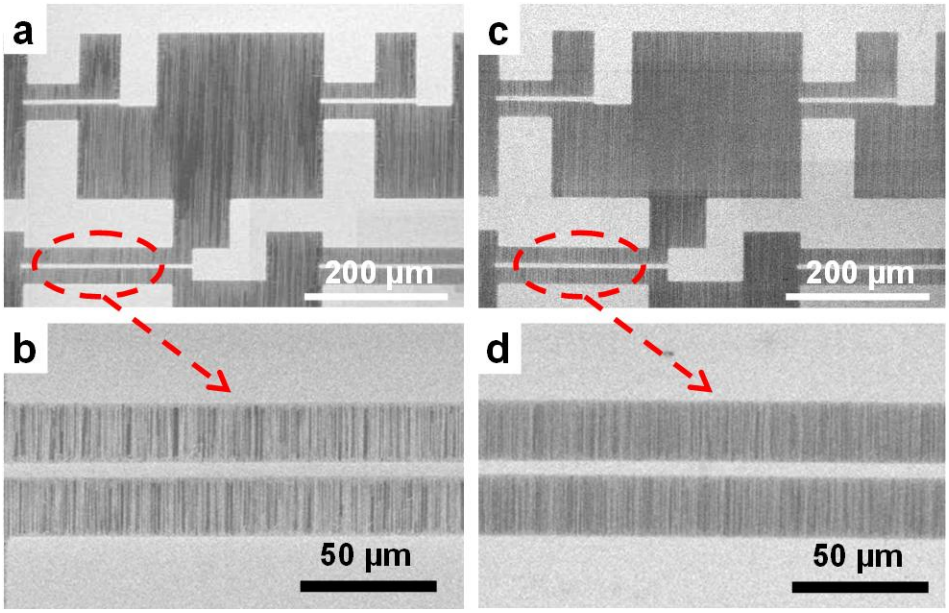

Figure 7.3 Scanning electron micrographs (SEMs) of complex patterns of dense, random networks of SWNTs (bright regions) interconnected by aligned arrays of SWNTs, as grown on quartz (a), (b), and transferred to SiO_2(100 nm)/Si (c), (d).

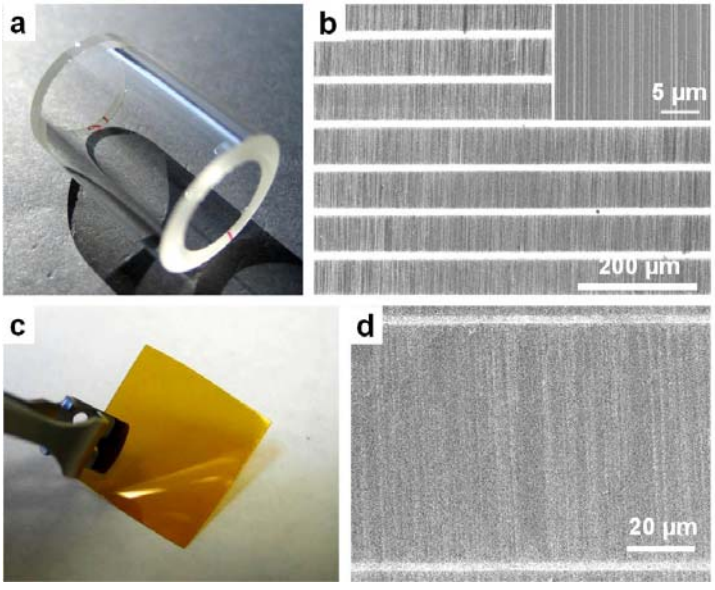

Figure 7.4 Optical image (a) and scanning electron micrograph (SEM) (b) of aligned arrays of SWNTs transferred from a quartz growth substrate to the surface of a glass cylinder. The inset in (b) provides a high magnification view. Optical image (c) and

scanning electron micrograph (SEM) (d) of aligned arrays of SWNTs transferred from a quartz growth substrate to a thin sheet of polyimide (Kapton).

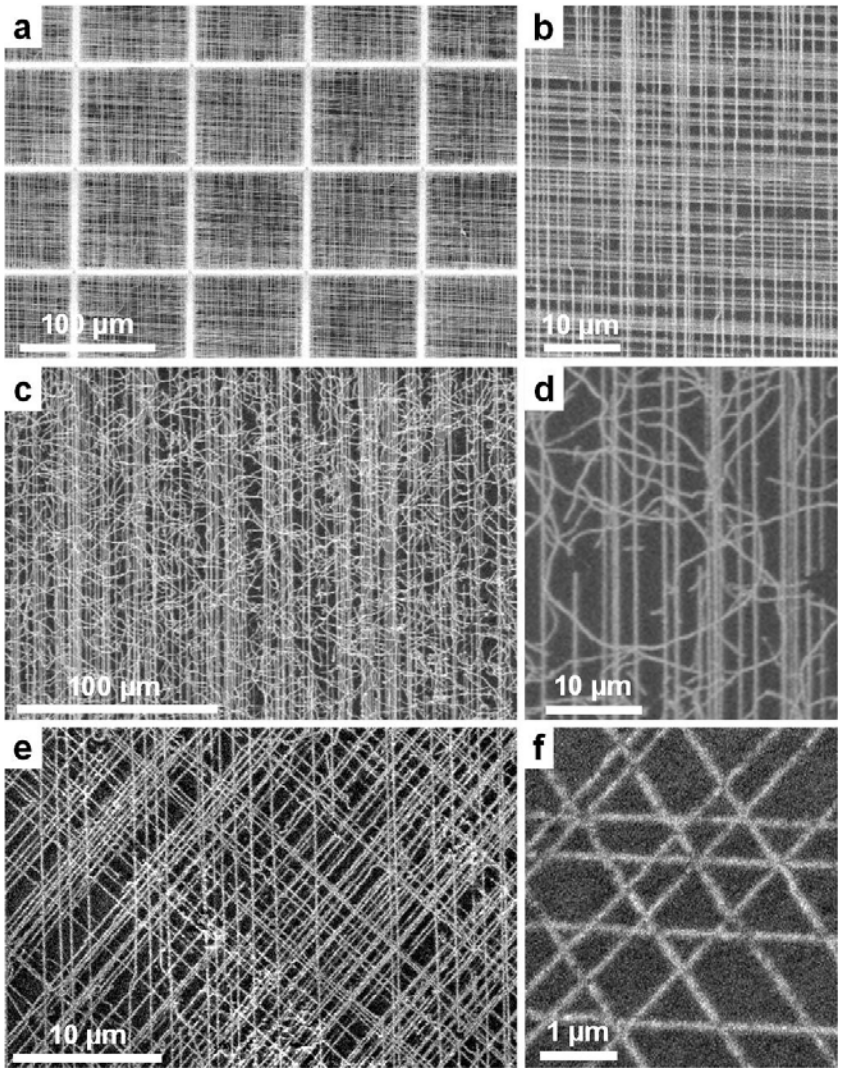

Figure 7.5 Scanning electron micrographs of various types of multilayer stacks of SWNTs formed by transfer. (a), (b) SWNTs in the geometry of crossbar arrays formed by a transfer process. (c), (d) SWNTs in the geometry of a triangle lattice, formed by a two-step transfer process. (e), (f) Random network of SWNTs transferred on top of an aligned array.

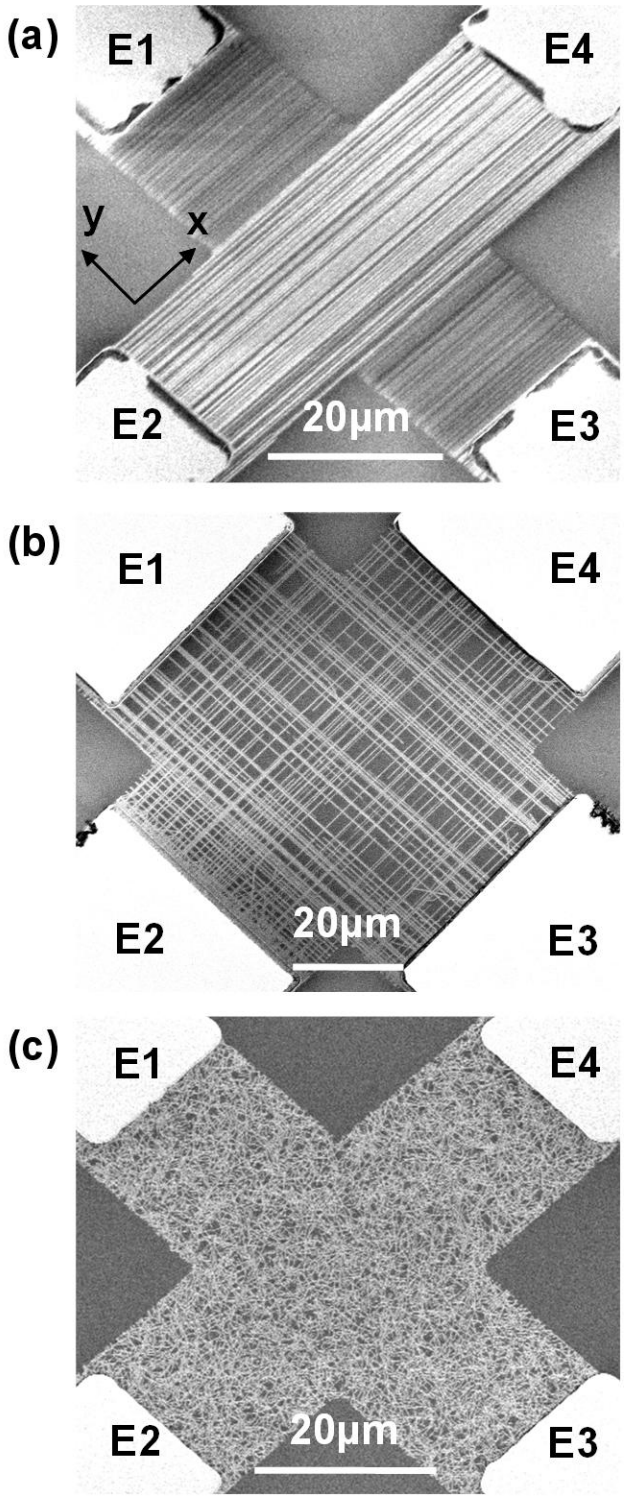

Figure 7.6 Scanning electron micrographs (SEMs) of four terminal test structures formed on SWNTs with different layouts, including (a) aligned arrays, (b) crossbars and (c) random networks.

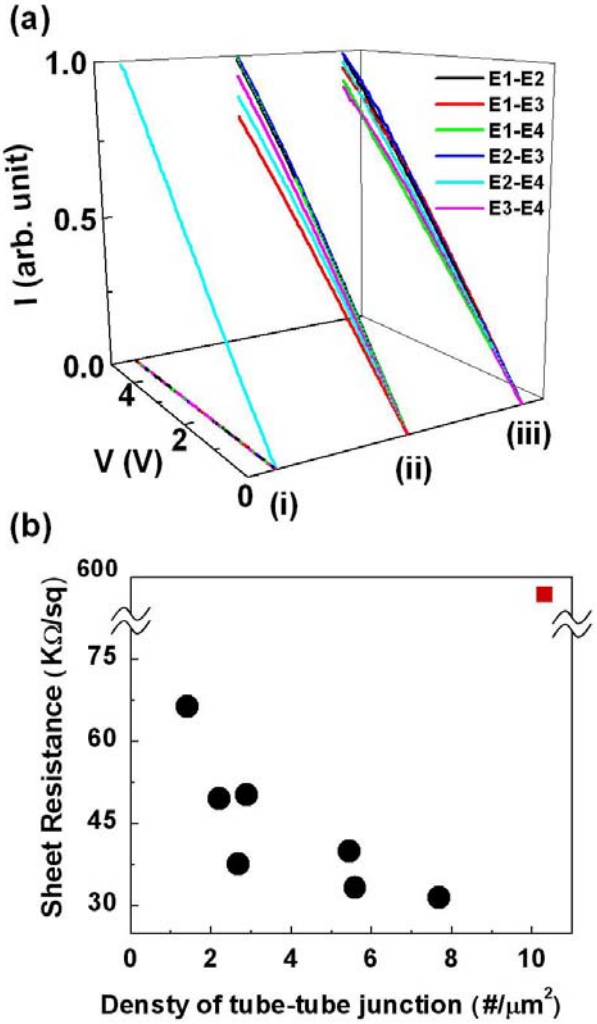

Figure 7.7 (a) Electrical measurements on different types of 'films' of SWNT generated by growth and transfer, including aligned arrays (i), crossbars (ii) and random networks (iii), with various four terminal probing combinations (E1-E2, E1-E3, E1-E4, E2-E3, E2-E4, E3-E4). The graph shows current (I), voltage (V) response that indicate linear, metallic response, with levels of anisotropy that reflect the underlying anisotropy of the SWNT arrangements in the films. Part (b) shows sheet resistances of crossbar layouts of SWNTs (black symbols) as a function of the density of tube-tube junctions. The red square corresponds to the case of a random network of SWNTs.

CHAPTER 8 HIGH FREQUENCY OPERATION OF SWNT TRANSISTORS

This chapter is submitted for publication in Science as "Carbon Nanotube Transistor Radios, **Coskun Kocabas**, Hoon-sik Kim, Tony Banks ,John A. Rogers, A. Pesetski, J. Baumgardner, S. Krishnaswami and H. Zhang"

8.1 Introduction

The invention of the transistor in 1947 represents the birth of the electronics age (*1*). The full scope of application possibilities began to emerge to the general public a few years later when researchers developed approaches to overcome the many scientific and technical challenges to implementing transistors in low cost, handheld radios (*2,3*). More advanced analog circuit systems and, ultimately, digital logic applications followed, thereby expanded the reach of transistors to virtually every form of modern technology. Although single walled carbon nanotubes (SWNTs) have many remarkable properties, transistors based on them must go through a similar development sequence if they are to achieve important roles in advanced electronics. The high level of difficulty associated with this development is empirically clear from the history of the field. More than ten years of worldwide research, beginning with the discovery of nanotubes, has failed, for example, to yield realistic demonstrations of even basic systems that provide power gain in the radio frequency (RF) range. This paper describes some progress in the area of SWNT based RF analog electronics, including carbon nanotube power amplifiers that operate in the VHF frequency band. These results, together with integration of this technology in transistor radios that use nanotube devices for resonant antennas, fixed RF amplifiers, RF mixers and audio amplifiers, might represent important steps in the development of SWNTs for RF electronics and other related applications.

The promise of SWNTs for electronics derives from their high mobilities and current carrying capacities (*4,5*), together with their low intrinsic capacitances (*6*). Transistors and small scale, simple digital logic devices that rely on individual SWNTs confirm this promise (*7-9*), through benchmarking studies conducted at low frequencies against single crystal silicon (*10*). Scalable integration of SWNTs into digital circuits is challenging, although recent work with assembled individual tubes as active elements, or

relatively dense, horizontally aligned arrays of tubes as thin film type semiconductors both show some promise (*11-18*). Nevertheless, the development of SWNTs for a digital electronics technology that could compete with silicon is daunting. Analog electronics (*19-21*), by contrast, represents a different and less well explored area of application of SWNTs. While these systems have many of the same challenges associated with digital circuits, their meaningful implementation can occur at comparatively lower levels of integration density and in layouts that can better exploit the exceptional electronic and thermal properties of the SWNTs. Recent reports show some measurements of intrinsic high speed operation in individual nanotube devices, but without the sorts of layouts or performance that would be needed for realistic applications(*20,22-24*). In particular, a critical part of an analog electronic circuit is the power amplifier, which converts small input signals to relatively high power outputs suitable for further processing. The ability to achieve power gain at high frequencies with 50 Ω termination is essential for applications in RF communication devices, global positioning systems (GPS), radar modules and others. This paper presents direct measurements of RF power gain for narrow band amplifiers based on transistors that use horizontally aligned arrays of SWNTs as semiconductor thin films. The ability of these devices to drive standard 50 Ω termination systems leads to their straightforward use in analog electronics. Nanotube transistor radios in which nanotube devices provide all of the key functions demonstrate an important example of this capability.

8.2 Method and Materials

For these systems, we developed advanced versions of basic layouts that we reported recently (*11*). In particular, horizontally aligned arrays of SWNTs with extremely linear configurations and high levels of alignment occupy the channel regions of transistor devices, where they act collectively as an effective thin film type semiconductor. Each of the several thousand SWNTs in a device provides an electrically continuous and independent pathway for charge transport. To achieve RF performance, we developed device designs that provide both high capacitance gate dielectrics (C_g), and low parasitic overlap capacitances (C_{gd}), with low resistance electrodes and probing pads. The electrodes define short gate lengths (L_g, down to 750 nm), precisely aligned to the

source, drain (Ti:1 nm, Pd: 10 nm, Au: 300 nm for source and drain; Ti:10 nm, Au:300 nm for gate), created either by electron beam (ebeam) lithography (Raith, eLine) or by contact mode photolithography (MJB8, Karl Suss). The alignment procedures provided an accuracy of ~50 nm and ~500 nm for the former and latter processes, respectively, as determined by the measured layouts of the electrodes. The lengths of the gate electrodes fabricated by ebeam lithography were somewhat smaller (~100 nm) than the lengths of the channels (i.e. the separations between the source and drain electrodes). The gate dielectrics consisted either of a bilayer of HfO_2 (~10 nm) deposited by atomic layer deposition, on top of a layer of benzocylobutene (BCB, ~20 nm Dow Chemical) spin cast on the SWNTs or a single layer of a HfO_2 (~50 nm) deposited by electron beam evaporation ($3x10^{-5}$ Torr; Temescal CV-8) directly onto the SWNTs. The thin film capacitance of the former and latter types of dielectrics were ~160 nF/cm^2 and ~210 nF/cm^2, respectively. Figure 8.1A shows schematic illustrations of the device layouts, together with scanning electron (Figure 8.1B) and optical (Figure 8.1C) micrographs. The arrays of SWNTs had average densities of >5 SWNT/μm, with peak values as high as ~25 SWNT/μm, in nearly ideal parallel, linear layouts, where >95% of the tubes span the source and drain electrodes and there are no tube/tube crossings or overlapping tubes. These devices and the performance enabled by them represent major technical advances over previous results (*11*). Figure 8.1D shows direct-current (DC) measurements of a representative device fabricated by ebeam lithography with an Hf_2O dielectric, L_g = 0.75 μm and a channel width (W) of 600 μm. In this example, g_m is as high as ~ 17 mS at a drain bias of -1 V and gate bias of -0.5 V. The device is capable of current outputs up to several tens of mA. The relatively low ratio of the currents in the on and off states results from the sizable populations (~1/3) of metallic SWNTs in the channel. Although such low on/off ratios would preclude applications in digital logic, they can be acceptable in analog RF systems where the devices operate in a narrow range of voltages around a fixed bias point.

8.2.1 Chemical Vapor Deposition of the Arrays of SWNTs

The growth of the arrays of SWNTs was accomplished by chemical vapour deposition growth on quartz. The process starts with cleaning of an ST-cut single crystal

quartz wafers and then annealing them in air at 900 ^{o}C for 8 h. 0.1-0.2 nm thick Fe film was deposited by electron beam evaporation (Temescal BJD1800, evaporation rate of 0.1 A/s) onto a photolithographically (standard UV photolithography) patterned layer of photoresist (AZ5214) on the quartz. Photoresist and photoresist residue were cleaned by acetone and stripper (AZ Kwik), respectively. In order to form isolated iron oxide nanoparticles, the samples were then annealed at 900 ^{o}C for 1.5 h. The SWNT growth process began with flushing the chamber with a flow of Ar (3000 sccm) for 2 min and then heating the furnace to 925 ^{o}C while flowing H_2 (300 sccm). Ethanol vapour is used as a carbon source by passing gases (8 sccm. H_2 and 8 sccm. Ar) through an ethanol bubbler held a 0 ^{o}C in a water bath chiller. Growth was terminated after 20 min, and the chamber was then cooled in H_2 and Ar flow. After the growth scanning electron micrograph (Raith e-LiNE) of the SWNTs were taken with 1KV acceleration voltage (Fig. S1).

8.2.2 Transistor Fabrication

Long channel length devices: We have used standard UV photolithography to fabricate devices for long channel (2μm to 32 μm) length. The fabrication process for long channel length devices began with fabrication of source/drain electrodes on SWNT array by UV photolithography (MJB8, Karl Suss) using AZ5214 photoresist. Metal for the source and drain electrodes (Ti:1nm, Pd:30nm) was deposited by e-beam evaporation (Temescal BJD1800; base pressure of 2e-6 torr). Lift-off was accomplished by rinsing in acetone for 10 min, and followed by rinsing with isopropanol and deionized water. Oxygen reactive ion etching (200 mT, 20 sccm. O_2 flow, 100W RF power,) removed SWNTs outside of the channel region which was protected by a patterned layer of photoresist (AZ5214). Spin casting 2% BCB (20nm) and atomic layer deposition of HfO_2 (10 nm) defined high capacitance bilayer dielectrics. Gate metal (Ti:2nm,Au:30nm. ebeam evaporation Temescal BJD1800; base pressure of 2e-6 torr) is defined top of the dielectric by UV photolithography. After defining the gate metal, dielectric on the source/drain contact pads was removed by etching with concentrated HF acid.

Short channel length devices: The fabrication of short channel length devices (0.75nm-2 μm) with these arrays of SWNT began with spin coating of a layer (400 nm) of electron

beam (e-beam) resist (495PMMA-A6, Microchem) at 2000 rpm for 30 s on the SWNT/quartz. The samples were then baked on a hot plate at 220 ^{o}C for 2 min. To avoid charging during electron beam (e-beam) writing process, a uniform layer of Al (12 nm) was deposited by e-beam evaporation (Temescal BJD1800; base pressure of 2e-6 torr) onto the resist. The source-drain pattern was the defined with an e-beam lithography tool (Raith e-LiNE) using an accelerating voltage of 10 KV and a current dose of 140 μC/cm^2. After writing, the Al was removed with an KOH etching solution; the PMMA was developed by immersion in a solution of a 1:3 part solution of MIBK and IPA, for 45 s. Metal for the source and drain electrodes (Ti:1nm, Pd: 10nm, Au: 300nm) was deposited by e-beam evaporation (Temescal BJD1800; base pressure of 2e-6 torr). Lift-off was accomplished by rinsing in acetone for 10 min, and followed by rinsing with isopropanol and deionized water. Oxygen reactive ion etching (200 mT, 20 sccm. O_2 flow, 100W RF power,) removed SWNTs outside of the channel region which was protected by a patterned layer of photoresist (AZ5214). The gate dielectric (50nm HfO_2) was deposited by e-beam evaporation (Temescal BJD1800, base pressure is 2e-5 Torr.). After dielectric deposition, the gate pattern was defined by a second e-beam lithography step, using process conditions similar to those used for the source-drain layer. The gate electrode was aligned (± 50nm precision) to source and drain using previously patterned alignment markers. After defining the gate metal, the HfO_2 on the source/drain contact pads was removed by etching with concentrated HF acid.

8.3 Results and Discussion

The large values of g_m together with small C_g, $C_{gd,}$ lead to devices with good performance in the RF range. Figure 8.2A and 2B show two port S-parameter data (symbols) for a device with W=300 μm and L_g=4 μm and an HfO_2/BCB dielectric, for frequencies between 10 MHz and 10 GHz. Modeling results (solid lines) using a small signal equivalent circuit (Figure 8.2B inset) with transconductance of g_m = 9.7 mS a small signal shunt resistance of R_0 = 220 Ω, a gate-drain capacitance of C_{gd} = 1.9 pF, and a drain resistance of R_d = 120 Ω, yields S parameters that match experimental results to within 1 dB over the 10 MHz to 1 GHz frequency range. The values of R_d and C_{gd} are close to expectations based on the device geometry and materials. The product of g_m and

R_0 is ~2, consistent with a device that has ~68% semiconducting nanotubes, if we assume that the conductance per tube of the metallic nanotubes is equal to the maximum transconductance per tube of the semiconducting nanotubes, a result that we find to be true empirically in our measurements of single SWNT devices (*11,20*). Figure 8.2C shows a plot of current gain ($|H_{21}|^2$) and maximum available gain (G_{max}) as a function of frequency for this device with W=100 μm and L_g=4 μm and an HfO_2/BCB dielectric. The extracted cutoff frequencies for current gain (f_T) and power gain (f_{max}) are ~2.5 GHz and ~1.1 GHz, respectively.

The scaling of these quantities with L_g, shown in Figure 8.2D, provides additional insights. For diffusive transport, the intrinsic transconductance should be proportional to L_g^{-1}, whereas measurements show a weaker dependence on L_g. This difference arises from an effective transconductance, as extracted from the current-voltage curves, that is a function not only of the intrinsic transconductance, but also of the shunt resistance, R_0, associated with the metallic nanotubes, which is directly proportional to L_g. Figure 8.2D shows the variation of f_T and f_{max} with L_g for photolithographically defined devices with bilayer dielectric, W=300 μm and L_g between 2 μm to 32 μm. We find empirically, that f_T scales as L_g^{-1} while f_{max} scales as approximately $L_g^{-0.5}$. The former scaling is relatively easy to understand, because f_T is proportional to g_m/C_{gd}, g_m is proportional to L_g^{-1} and C_{gd} is dominated by parasitic capacitance resulting from fringing fields, making this quantity essentially independent of L_g. (At frequencies near f_T, the capacitive reactance is much smaller than R_0 and dominates the device behavior.) The behavior of f_{max}, which can also be written as $f_{\max} = \dfrac{f_T}{2\sqrt{(R_g + R_s)g_m + 2\pi R_g C_{gd} f_T}}$, is substantially more complicated, since the maximum available power gain (G_{max}) for a transistor is (*25*)

$$G_{\max} = \left| \frac{S_{21}}{S_{12}} \right|, K < 1 \quad or \quad \left| \frac{S_{21}}{S_{12}} \left(K - \sqrt{K^2 - 1} \right) \right|, \; K > 1, \tag{1}$$

where the stability factor, K, is given by

$$K = \frac{1 + \left|S_{11}S_{22} - S_{12}S_{21}\right|^2 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2}{2\left|S_{12}S_{21}\right|} \quad (2)$$

Simulations based on the small signal model in which g_m scales as L_g^{-1} and R_0 is proportional to L_g predict a nontrivial behavior for f_{max} that is consistent with, but not exactly the same as, a proportionality to $L_g^{-0.5}$.

These devices are capable of producing power gain when the input and output are properly impedance matched, thereby providing the opportunity to build amplifiers that operate in the VHF range. Figure 8.3A shows a schematic illustration of the measurement system for a narrowband amplifier, where a series inductor enables impedance matching. The inductor combines with the C_{gd} to form a resonator, stepping up the voltage on the input to a SWNT transistor that has a bilayer dielectric, W=300 μm and L_g=4 μm. These amplifiers provided power gains of 1 to 14 dB into a standard 50 Ω load for frequencies up to 125 MHz. Figure 8.3B shows the power gain as a function of frequency for four different amplifiers. Modeling results (line in Figure 8.3B), using the same values that reproduce the S parameters as discussed for Figure 8.2A and 2B, indicate that an additional ~5 dB of gain could be obtained by properly impedance matching the output.

We fabricated nanotube radios using these types of amplifiers and other SWNT transistor components to demonstrate several of the most important elements of analog electronics (Figure 8.4A). Substrates with devices formed according to procedures described previously were diced into chips, each containing three SWNT transistors, and then wire bonded into a conventional ceramic DIP packages. Figure 8.4B and Figure 8.4C show the constructed circuit and packed devices. The radio uses an autoheterodyne receiver design consisting of four capacitatively coupled stages: an active resonant antenna, two fixed RF amplifiers, and an audio amplifier, all based on SWNT devices. The active resonant antenna used a magnetic dipole antenna formed from 33 loops of wire on a 6" diameter form, in parallel with a variable capacitor and the gate-drain capacitance of a SWNT transistor. An LC tank circuit steps up the voltage by factor of ~30, and also increases impedance. A SWNT transistor serves as a buffer to convert this high-impedance signal back to ~377 Ω. Tuning was accomplished with the active

resonant antenna, which provided a quality factor, Q, of ~50 and a gain of ~30 dB. For the purpose of testing, the antenna was designed to resonate at 1090 kHz, corresponding to a local radio station in the Baltimore, MD area. The two RF amplifiers were constructed according to designs shown in Figure 8.3. The first RF amplifier provided a further +20 dB of gain at the resonant frequency. An LC tank circuit (with 440 μH inductor and 48 pF capacitor), stepped up the voltage to enable impedance matching. The second RF amplifier performed the dual function of providing gain and demodulating the signal. Biasing the gate voltage of the second amplifier slightly above the maximum gain point created a large second harmonic in the amplifier output. Applying the amplitude modulated input signal to this non-linear amplifier produced a demodulated audio frequency signal with a conversion (mixer) gain of +8 dB. The audio amplifier design was similar to that of the RF amplifiers except the input was coupled with a transformer to produce audio frequency gain. Three SWNT transistors were connected in parallel to convert high impedance to 80 Ω. The audio amplifier provides another +20 dB of gain suitable for driving, directly, a standard 16 Ω speaker. Additional 2.5 dB gain can be achieved by final matching transformer. An audio recording of a traffic report picked up by a nanotube radio is given in the Supporting Online Materials; a power spectrum of this output, which is dominated by frequencies in the range of the human voice, appears in Figure 8.4C.

8.4 Conclusion

The results described here represent important first steps toward the implementation of SNWT materials in high speed analog electronics, in a manner that appears to have favourable scaling characteristics. Hundreds of devices, interconnected into desired planar layouts on quartz or even transferred to silicon are possible, thereby opening up the possibility of achieving systems with significantly more complex functionality. Straightforward downscaling of the dimensions of the types of devices introduced here should enable further improvements in performance. These possibilities, as well as strategies to improve the density of the SWNTs in the arrays, are promising directions for future research.

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26. This material is based upon work supported by the National Science Foundation under grant NIRT-0403489 and the U.S. Department of Energy, Division of Materials Sciences under Award No. DEFG02-91ER45439, through the Frederick Seitz MRL and Center for Microanalysis of Materials at the University of Illinois at Urbana-Champaign.

8.6 Figures

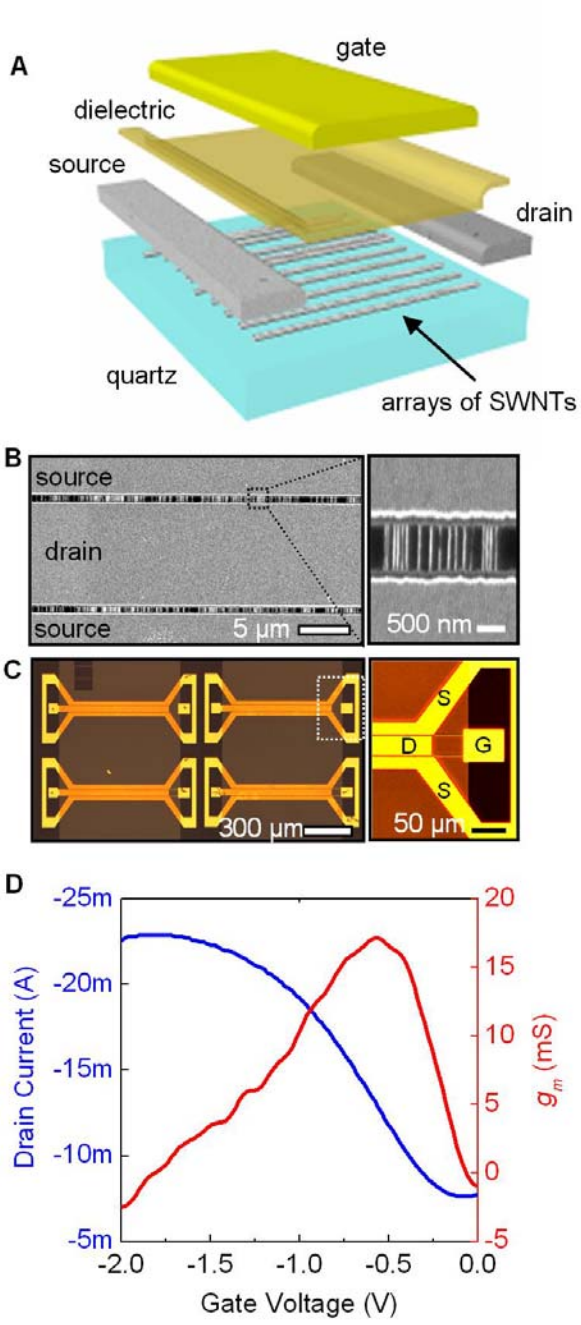

Figure 8.1 (A) Schematic exploded view of a radio frequency (RF) transistor that uses parallel, aligned arrays of single walled carbon nanotubes (SWNTs) for the semiconductor. The critical design aspects include, (1) aligned source, drain and gate electrodes to eliminate parasitic capacitance, (2) short gate lengths and high capacitance gate dielectrics to maximize the transconductance, and (3) low resistance leads and

contact pads. **(B)** Optical micrograph of an array of devices on a quartz wafer. The inset provides a magnified view. **(C)** Scanning electron micrograph of source/drain electrode pairs with bridging arrays of SWNTs. The average density of SWNTs is ~5 SWNT/μm. The insets provide magnified views. The devices used split gate layouts with probing pads in a ground-signal-ground configuration suitable for direct probing with a vector network analyzer. **(D)** Transfer characteristics of a representative device with channel length and width of ~0.75 μm, and 600 μm, respectively, formed by electron beam lithography. The red and blue curves show the dependence of the transconductance (g_m) and drain current on gate voltage, both measured at a source/drain bias of -1 V.

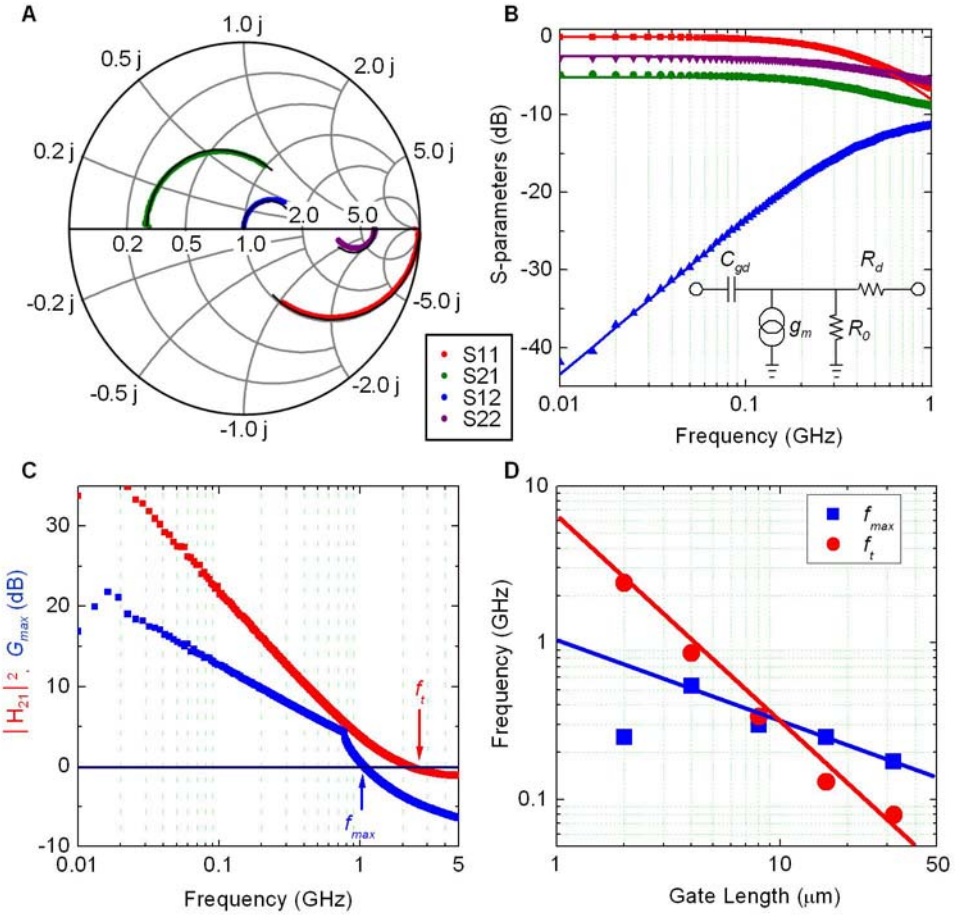

Figure 8.2 **(A,B)** Smith chart and amplitude plot of measured (symbols) and simulated (lines) two port *S* parameters for a device with channel length and width of 4 mm and 300

μm, respectively. **(C)** Current gain ($|H_{21}|^2$) and maximum available power gain (G_{max}) as a function of frequency for the device, showing f_T ~2.5 GHz and f_{max} ~ 1.1 GHz. **(A)** Plot of f_T and f_{max} for devices (channel widths of 300 μm) with different gate lengths.

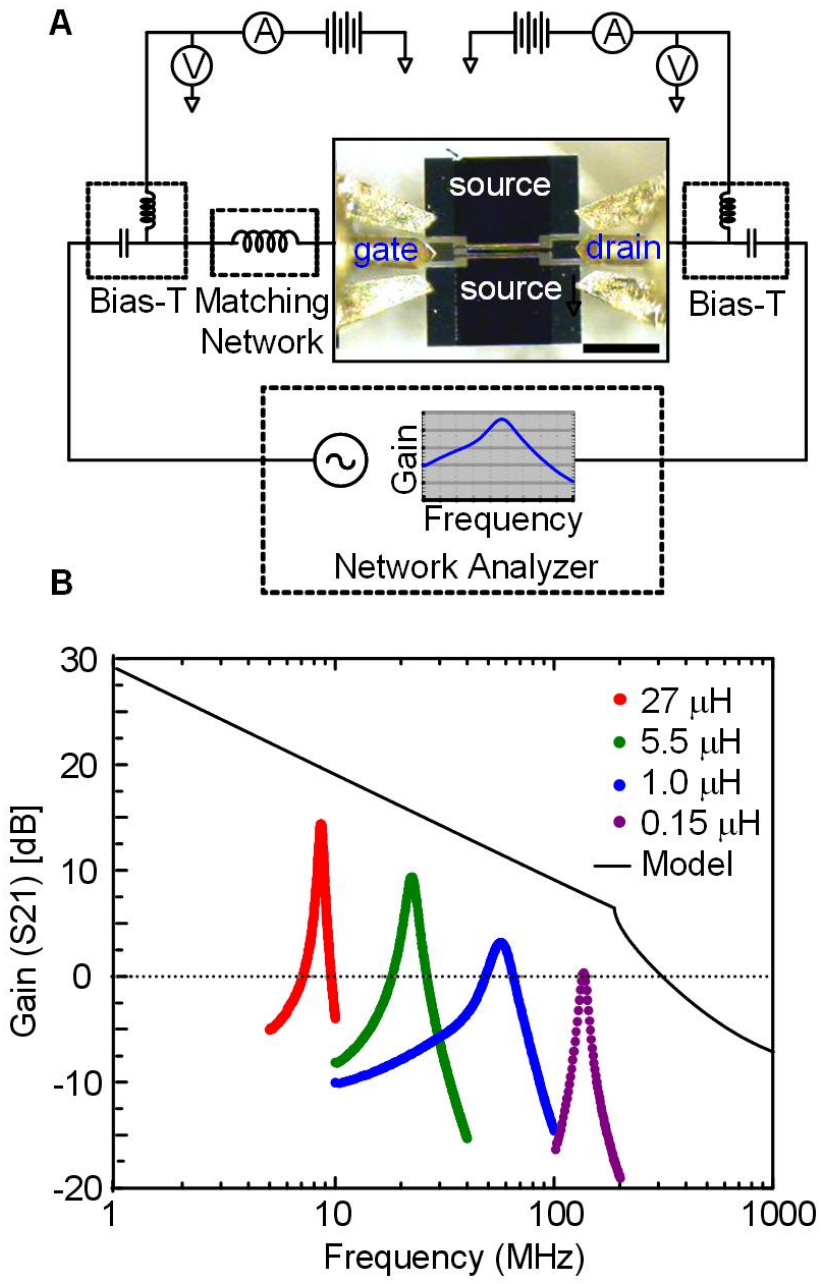

Figure 8.3 (A) Circuit schematic for an SWNT based RF amplifier, with an illustration of the measurement system. Scale bar is 300 μm. **(B)** Plot of theoretical maximum stable

gain calculated from S parameter data (line) and measured S_{21} data for narrow band amplifiers (symbols) with different matching inductors.

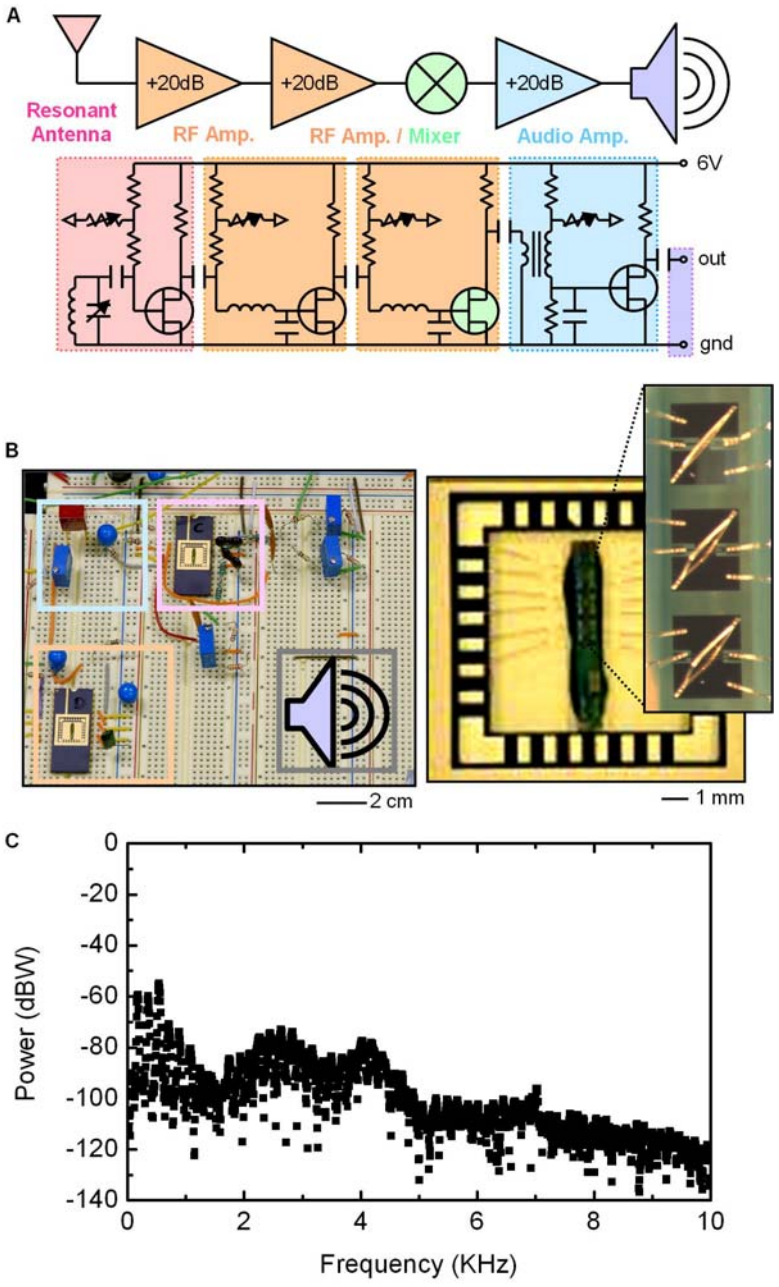

Figure 8.4 (A) Block and circuit diagrams of a radio that uses SWNT transistors for the resonant antenna, two fixed RF amplifiers, an RF mixer and an audio amplifier. **(B)** Image of the radio, with magnified views of SWNT transistors wire bonded into DIP

packages. **(C)** Power spectrum of the radio output measured across a 16 Ω load, recorded during a commercial broadcast of a traffic report.

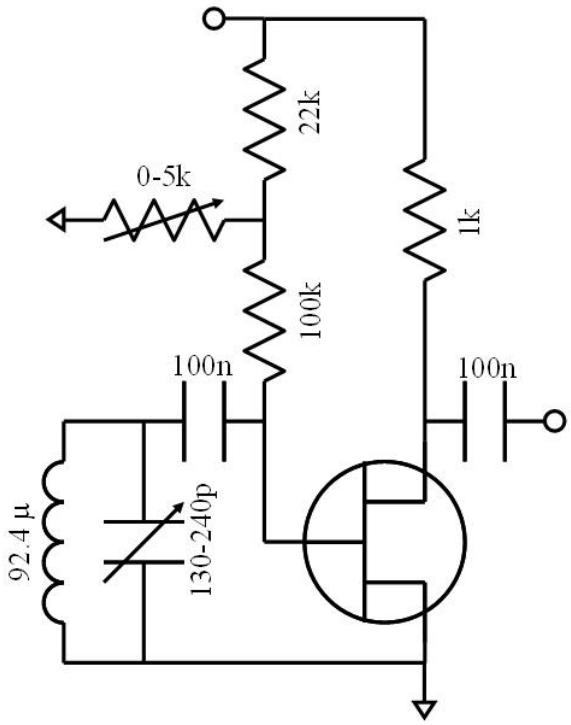

Figure 8.5 Circuit diagram for the active resonant antenna. The antenna consists of a LC tank circuit with a resonance frequency of 1.09 MHz. This circuit is capacitatively coupled to the gate of a SWNT transistor that functions as a buffer to convert the high-impedance signal back to ~377 Ω. The output impedance is adjusted with a 1 kΩ resistor. The gate bias of the device is adjusted to achieve highest transconductance with a variable resistor (0-5 kΩ).

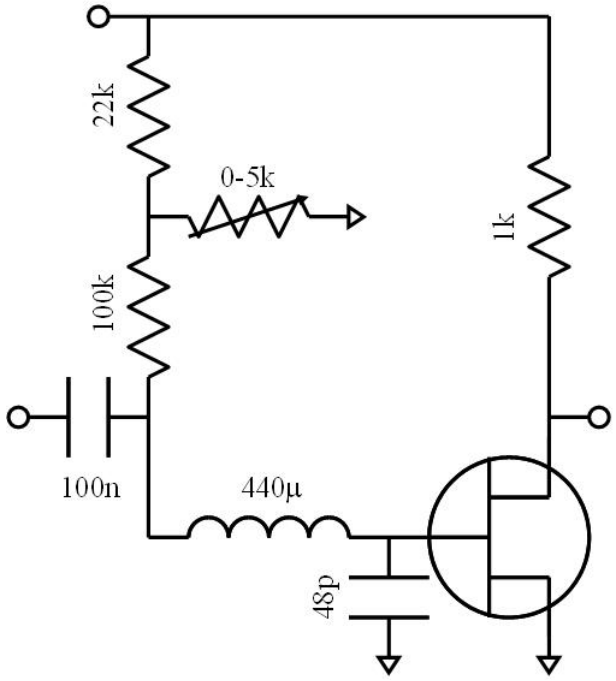

Figure 8.6 Circuit diagram for the narrow band amplifier. The input of the amplifier is capacitatively coupled to the output of resonant antenna. The LC tank circuit steps up the voltage by factor of ~30, and matches the low impedance input and high impedance of a SWNT transistor at the resonant frequency with a 10 kHz bandwidth. The total capacitance of the tank circuit has three components: 2 pF from the transistor (C_{gs}), 13 pF from package and 33 pF added with a separate capacitor. The transistor converts the high impedance signal back to 377 Ω. This amplifier provides 20 dB gain at the resonant frequency.

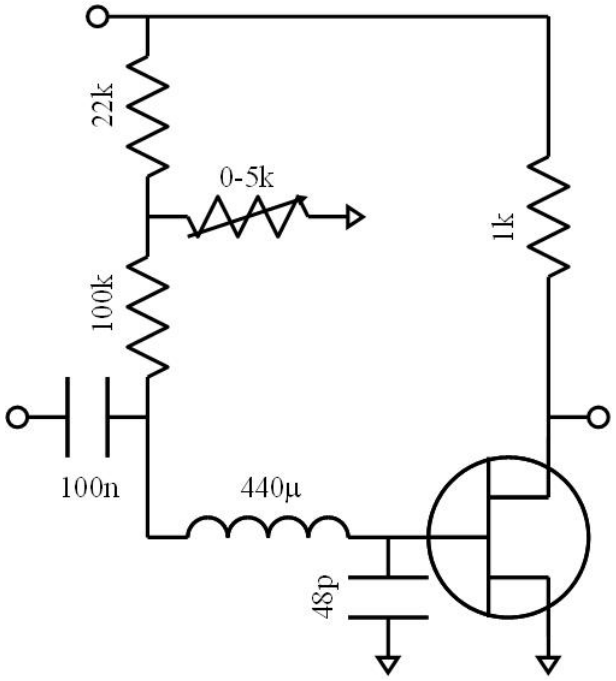

Figure 8.7 Circuit diagram for the active mixer. The operation of the mixer is similar to the narrow band amplifier but serves a dual function: providing 20 dB gain for the carrier signal, and demodulating the signal. The mixing is achieved by biasing the gate voltage to a nonlinear point slightly above the maximum gain point. The conversion gain of the mixer is 8 dB.

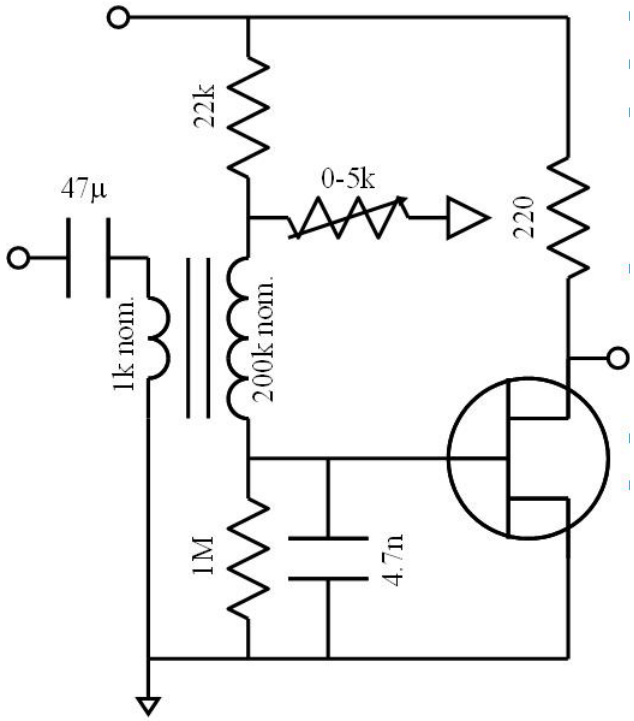

Figure 8.8 Circuit diagram for the audio amplifier. An audio amplifier provides 20 dB gain for frequencies between 300 Hz to 20 kHz. A transformer is used to step up the voltage by 10 times. To achieve 80Ω output impedance, three SWNT transistors are connected in parallel. A 16 Ω headphone is directly connected to the drain of the SWNT devices.

CHAPTER 9 OUTLOOK AND FUTURE DIRECTIONS

As a conclusion we have develop a new approach for generating large area homogenous parallel array of single walled carbon nanotubes. The approach uses guided growth, by chemical vapor deposition (CVD), of SWNTs on single crystal quartz substrates. The anisotropic interaction associated with lattice structure of the quartz between SWNT and quartz surface guides SWNT during the deposition process. We have optimized CVD conditions that can produce arrays of individual single walled carbon nanotubes in horizontal configurations with perfect linear shapes, to within experimental uncertainties, and with levels of alignment >99.9%. We took the method one step further by printing these SWNT arrays on unusual substrate such as plastic. Using the developed printing technique, we can fabricate multilayer superstructures of single-walled carbon nanotubes (SWNTs) configured in horizontally aligned arrays, random networks and complex geometries of arrays and networks, on a wide range of substrates.

The aligned SWNT arrays, networks and multilayer structure provide effective semiconducting film suitable for electronic devices. In order to understand charge transport through SWNT films, we studied the scaling behaviour of SWNT transistors by systematically varying the degrees of alignment and coverage in transistors with a range of channel lengths and orientations perpendicular and parallel to the direction of alignment. We have modelled our experimental results using a first principles stick-percolation based transport model which provides a simple, framework to interpret the sometimes counter-intuitive transport parameters measured in these devices.

We have used dense, perfectly aligned arrays of long, perfectly linear SWNTs as an effective thin film semiconductor suitable for integration into transistors and other classes of electronic devices. These types of devices show excellent electric performance with mobilities and scaled transconductances approaching ~1,000 $cm^2\ V^{-1}\ s^{-1}$ and ~3,000 $S\ m^{-1}$, respectively. MOS and CMOS logic gates and mechanically flexible transistors on plastic were also demonstrated. Finally, we have studied the high frequency performance of transistors that use aligned SWNT arrays. For the first time we have observed power gain

from SWNT transistors. This achievement allows us to build all of the key functions of analog electronics, including resonant antennas, fixed RF amplifiers, RF mixers and audio amplifiers. Combining these components we have built the first carbon nanotube radio. These results represent important first steps to practical implementation of SWNTs in high speed analog circuits.

9.1 Improvement of the Growth Technique

The developed growth technique can produce long (~1mm), straight ($\pm 1^{o}$), dense (~10 SWNT/μm) SWNT arrays. Tube density is the critical parameter for high performance electronic devices. Theoretical expectations based on the growth mechanism, predict that the tube density can be improved by an order of magnitudes. 100 SWNT/μm or even higher tube densities could be possible. In this section I will summaries the ideas, which are our current research topics, to improve the density. The key parameter of the growth is deposition of the catalyst particles. Currently we do not have much controllability on the catalyst deposition. Extensive research on deposition of catalyst particles shows that pattered thin iron film (~0.2nm) is the best choice to achieve higher densities. Annealing of this film results formation of nanoparticles with random distribution in size and location. We believe that more controllability on particle size and location will improve the growth yield. Along this point we proposed two approaches to control the catalyst deposition. The process for generating such arrangements of nanoparticles will involve imprint lithography followed by angled evaporation of Fe, liftoff and then thermal annealing to generate particles with diameters of 1-2 nm. A staggered arrangement of such particles will achieve lateral separations of adjacent SWNT that are much smaller (<10 nm) than the resolution of the lithography (~50 nm).

9.2 Some Applications and on Going Work

Thin film electronics is only one of the applications of aligned SWNTs. SWNT has been used for different applications such as biological or chemical sensors, light emission devices etc... Using regular aligned SWNT arrays definitely simplify the fabrication process and it will increase the throughput of such devices. Using aligned SWNT arrays as a sensor could be the most trivial application. Figure 9.2 shows proposed sensor geometry that use aligned SWNT as a sensing element. Aligned SWNT arrays allow us to

fabricate high density sensors. Integration with microfluidic devices could open a fruitful research topic.

9.3 Elimination of Metallic SWNT with Selective Laser Ablation

The growth procedures described in the thesis yields high density arrays of SWNT, but with ~1/3 metallic tubes. Eliminating these tubes, each one of which creates electrical shorts in transistors built with these arrays, is a critically important part of the process. Here we propose the use of scanning, resonant laser ablation to eliminate selectively the metallic tubes without affecting the semiconducting tubes. Our previous results show the ability to destroy, in an orientationally selective fashion, SWNTs on substrates. (See Section 9.3.1) The proposed strategy will extend this work to include wavelength selective ablation of the metallic tubes. This approach exploits the different optical absorption properties of metallic and semiconducting SWNTs. The first optical transitions of metallic SWNTs, associated with their Van Hove singularities, lie in a range of wavelengths between 400 and 600 nm. These features are distinct from transitions associated with semiconducting SWNT between 800-1600nm. We propose, then, that pulsed lasers with wavelengths tunable between 400-600 nm will provide a means to ablate selectively the metallic tubes. Figure 9.3 illustrates this process, in a schematic fashion. This technique, unlike chemical or solution based methods to separate metallic tubes, has the advantage that it can be applied directly to the aligned arrays, without chemical contamination of the substrate or tubes. This method is well suited to application with the perfectly aligned array geometries and can be easily extended to large areas such as full wafer scale using systems that might resemble, for example, the laser based systems that are used for manufacturing polysilicon thin film electronics.

9.3.1 Laser Ablation of SWNTs

This section was published as "Aligned arrays of Single-Walled carbon Nanotubes Generated from Random Networks by Orientationally Selective Laser Ablation, **C. Kocabas**, M.A. Meitl, A. Gaur, M. Shim and J.A. Rogers, *Nano Letters, 4(12), 2421-2426 (2004).* " Reproduced (or 'Reproduced in part') with permission from JACS. Copyright 2007 American Chemical Society.

In this section we will introduce a new approach to eliminate metallic SWNT using the differences in optical absorption between these two types of SWNTs. The method is based ablation of individual single-walled carbon nanotubes by use of intense picosecond laser pulses. Linearly polarized pulses ablate only those tubes that are oriented substantially along the polarization direction. When applied to random submonolayer networks of tubes on solid supports, this procedure can produce collections of aligned tubes oriented perpendicular to the polarization direction. Detailed examples highlight essential aspects of the approach and some features of the underlying physics that governs the process.

The remarkable characteristics of single-walled carbon nanotubes (SWNT) make them interesting electronic materials for applications in electrical and optical sensors, nanoelectronic devices, and in new classes of systems that involve large area flexible circuits, also known as macroelectronics. In the latter class of device, parallel arrays or random networks of tubes act as effective semiconductor layers for high performance thin film type transistors.(1-5) In many cases, these devices can benefit from collections of tubes that have narrow distributions of orientations. Past work shows that certain solution deposition techniques can yield aligned tubes.(6-9) Directed growth methods can also produce some preferred orientation.(10-14) This paper provides an approach that separates completely the steps of growth and deposition from those of alignment. It involves exposing unaligned random networks of SWNTs to high intensity, linearly polarized laser pulses to ablate selectively tubes that lie along the polarization direction. In this manner, the laser ablation creates, from an orientationally disordered collection of SWNTs, well aligned tubes oriented in a direction that is perpendicular to the polarization. The paper begins by describing the setup and the laser sources. A variety of ablation results provides insights into the capabilities of the method and the underlying physics. Thin film transistors made using collections of SWNTs exposed to linearly polarized light show behavior that depends strongly on the orientation of the channel with respect to the polarization direction. This type of process might be useful for generating well-controlled arrays of SWNTs suitable for applications in optics,(15) sensors,(16) and electronics(5).

Figure 9.4 illustrates the experimental setup. The light source is an optical parametric oscillator (Euroscan picosecond OPO) that produces trains of pulses with 3 μm wavelength. Other wavelengths are possible; we also demonstrated ablation, for example, at 1064 nm and at 532 nm. The duration of the pulses is 10 ps. They are each separated in time by 10 ns and they occur in 1 μs long bursts at a repetition rate of 25 Hz. The energy per pulse is ~24 μJ, which corresponds to an average power of 60 mW. A CaF lens with 75 mm focal length focuses the laser to a spot with a diameter of 100 μm on the sample. The sample itself consists of a collection of SWNTs grown on a quartz substrate by chemical vapor deposition (CVD). Quartz was chosen to avoid absorption of the laser light by the substrate. For the CVD growth, we used ferritin catalyst (Aldrich) diluted by deionized water at a volumetric ratio of 1:200 cast onto the quartz wafer. Immediately placing this substrate into a quartz tube furnace at 900 ^{o}C for 2 min followed by purging with hydrogen gas at 900 ^{o}C for 1 min and then flowing methane (500 standard cubic centimeters per minute (sccm)) and hydrogen (75 sccm) at 900 ^{o}C for 10 min grows the SWNTs. The density of tubes for the experiments described here is between 2 and 5 per square micron, with diameters between 1 and 5 nm and lengths in the range of 5-10 μm. SWNTs grown in this manner appear on the substrate with the entire range of possible orientations. A motorized sample mount provides a means to scan the laser spot over the surface of the sample in a controlled manner.

Figure 9.4b shows a schematic illustration of linearly polarized light incident on a SWNT. The symbol E represents the polarization direction. Since SWNTs have deeply subwavelength and highly anisotropic dimensions, their interaction with light strongly depends on the orientation of electric field with respect to their orientation. In particular, optical absorption is much stronger for light polarized along the tube axis than it is for light polarized perpendicular to this axis. Recent work describes models for the physics behind this anisotropy.(17-20) One can qualitatively understand the effect by analogy to absorption anisotropy in metal wires that have subwavelength widths. As a result, the total absorption is proportional to the square of the projection of the electric field onto the long axis of the tube. For laser pulses with sufficiently high intensity and short pulse duration, it is possible for this absorbed light to destroy the tubes through an ablation process. The strong dependence of the absorption cross section on orientation induces a

similar dependence in the threshold for ablation. We exploit this effect to generate aligned tubes from random networks.

Figure 9.5 shows AFM images of SWNTs exposed to laser pulses with different intensities above ablation threshold, with fixed exposure time of 100 ms. The ablated tubes appear in these AFMs as discontinuous lines or dots that lie along the positions of tubes that existed before laser exposure. (Dots present even at low intensities are due to ferritin catalyst particles.) This structural deformation is different for different exposure intensities. At low intensities, the tubes become discontinuous with small breaks (as observed by AFM) that appear along the lengths of the tubes. As the power increases the structural deformation becomes more pronounced and these breaks evolve into isolated dots. Figure 9.6 shows results from ablation of an array of parallel SWNTs that have diameters between 1 and 5 nm. Even with the laser power tuned near the ablation threshold, we did not observe a significant dependence of the ablation on the diameter or on the electronic properties (i.e., semiconducting or metallic). Similarly aligned tubes tended to ablate in a nonspecific manner at comparable thresholds. The morphologies of the ablated tubes have some similarities to those of SWNTs that are heated above 350 ^{o}C in air. Although these similarities do not provide sufficient information to draw firm conclusions on the details of the ablation process, they are consistent with ablation that has some thermal origins. Extrapolations from recent work suggest that the temperature rise in the tubes in our experiments could easily exceed 500 ^{o}C. The time constant for diffusion of heat from the tubes to the underlying substrate is on the order of ~40 ps.(21) It is therefore likely that cumulative heating from successive pulses in the train (pulse to pulse separation of 10 ns) is insignificant and that ablation can occur in a single pulse. The makeup of the material that remains after ablation is unknown, but it likely consists, at least in part, of amorphous carbon. Additional experiments are required to understand fully these and other aspects. This paper focuses, instead, on some operational features of the process and means to use it to generate aligned tube arrays for transistor applications.

Figure 9.7a and b shows results obtained with orthogonal linear polarizations; Figure 4c shows the case for circularly polarized light (10 μJ pulses with 300 ps duration and repetition rate of 10 kHz at 1064 nm, focused to a spot with 10 μm diameter). The insets at the bottom left illustrate the polarization states. The first two frames illustrate

clearly that only tubes aligned along the polarization direction are ablated by the laser. The circularly polarized light destroys all tubes, independent of orientation, as expected due to the lack of dependence of the absorption on orientation in this case. By controlling the polarization of the laser we can select the ablation direction to generate tube arrays with well-defined orientation.

Additional aspects of the ablation process can be understood from careful examination of the effects on individual or small numbers of SWNTs. Figure 9.5 presents AFM images of a representative set of results. Figure 9.8a shows the intersection of an ablated tube with two orthogonally aligned tubes that remain unablated. To within the resolution of the AFM, the orthogonal tubes survive without any significant structural deformation due to the ablation of the tube that previously directly crossed them (on top or beneath). Theoretical studies suggest that such crossing tubes interact only with weak dispersion forces and that the contact areas at the crossing regions are small. As a result, the resistance to heat flow from one tube to another is expected to be large.(22) The results of Figure 9.8a are qualitatively consistent with that conclusion. Figure 9.8b shows an AFM image of a ring-shaped SWNT ablated with linearly polarized pulses. The parts of this ring that have tangents parallel to the polarization direction are ablated, while the other parts remain unaffected. The results show that individual nanotubes can be structured by laser ablation. This observation is somewhat surprising if the ablation process is fundamentally thermal, since SWNTs are known to have extremely high thermal conductivities. It might be understood, however, based on the combined effects of efficient heat flow to the substrate and a sharp threshold for thermal ablation. If we assume that the time for flow of heat to the substrate has a characteristic time scale of 40 ps, then the diffusion length is ~200 nm if we assume that the diffusivity of the tubes is ~10 cm^2/s. Figure 9.8c shows another AFM image of a ring-shaped SWNT exposed to circularly polarized laser pulses. Here, the entire ring is ablated, as expected based on the lack of dependence of absorption with orientation, in this case. An image of a long curved SWNT after ablation appears in Figure 9.8d. Ablation ceases, apparently abruptly, beyond a certain angular mismatch between the tube axis and the polarization direction. Taken together, these AFM images illustrate the high precision in control of SWNT shapes and orientations that is possible with laser ablation.

As an application example, we used this technique to fabricate thin film transistors that incorporate an aligned collection of SWNTs as an effective semiconductor layer, by starting with an orientationally disordered network. Figure 9.9a shows an AFM image of channel region of a completed device with 6 μm channel length. The source and drain are illustrated as colorized regions at the top and bottom of this image. The film of SWNTs was grown on a quartz substrate in the manner previously described and then exposed with linearly polarized laser pulses to destroy tubes along the polarization direction. Figure 9.9b shows a magnified AFM image of the channel region. Directionally ablated tubes can be seen clearly. Source/drain contacts of Ti/Au (3 and 25 nm thicknesses) were fabricated on the exposed film by liftoff with a poly(methyl methacrylate) (PMMA) resist patterned by deep ultraviolet photolithography. A 1 μm thick PMMA layer spin cast on top of this structure formed a dielectric for the Au gate electrode that was deposited through a shadow mask. Figure 9.9c shows an optical micrograph of an array of devices (top) and a schematic illustration of the device geometry (bottom). Figure 9.9d presents the transfer characteristics of typical devices that have their channels aligned parallel and perpendicular to the direction of the aligned tubes. The results clearly show the expected anisotropic response. The currents in the perpendicular device are about 1 μA or less; the gate leakage is less than a few nA in both cases. The inset in Figure 9.9d shows the scaling of the on current in the case of a series of devices with the parallel orientation. The current depends linearly on the channel width, as expected for devices that use uniform thin films of semiconductors and that are decoupled well from one another. (This latter feature is due at least partly to poor conductivity through the film in the perpendicular direction.) The observation of large currents in the parallel devices is consistent not only with orientationally selective burning, but it also reveals additional information concerning ablation at tube/tube crossings (e.g., Figure 9.8a). For the SWNT arrays used in these devices, nearly all of the unablated tubes have at least one crossing point with an ablated tube. If the ablation destroyed both tubes at this crossing point, then the electrical continuity of the unablated tube would be degraded or eliminated. Our electrical measurements are consistent only with relatively minor (from an electrical standpoint) or no degradation.

In summary, this section introduces a ablation of SWNTs with intense laser pulses. This method could be used to generate anisotropic SWNT nmetwork from a random network. Thin film transistors built with such laser processed tubes show good performance and the expected orientational anisotropy. This tool may be valuable for a range of device applications. The basic mechanisms of the ablation and the nature of the products of this process represent topics for future research.

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9.5 Figures

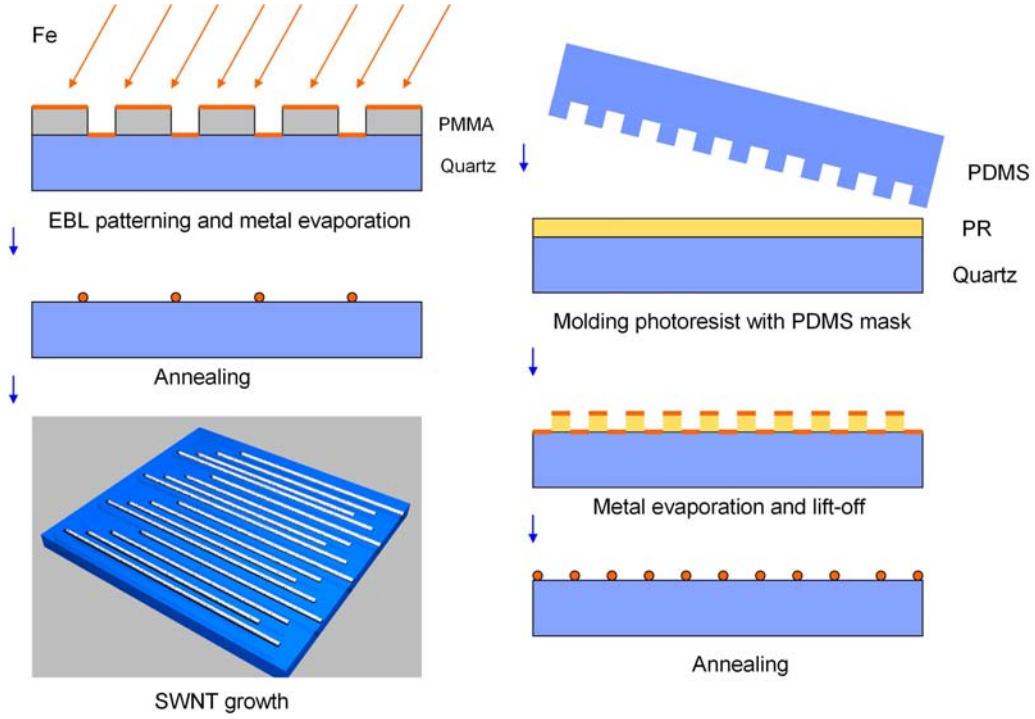

Figure 9.1 Strategy for achieving ultrahigh density, perfectly aligned arrays of SWNTs, by guided growth on quartz using lithographically defined iron nanoparticle catalysts.

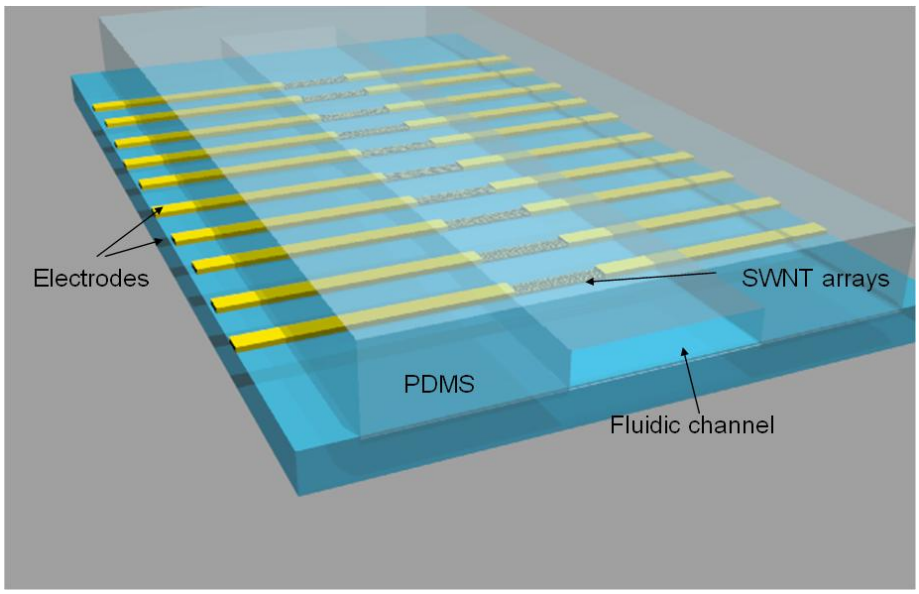

Figure 9.2 Proposed SWNT sensor geometry. SWNT array devices integrated with a microfluidic channel could provide nice platform for high throughput sensing application.

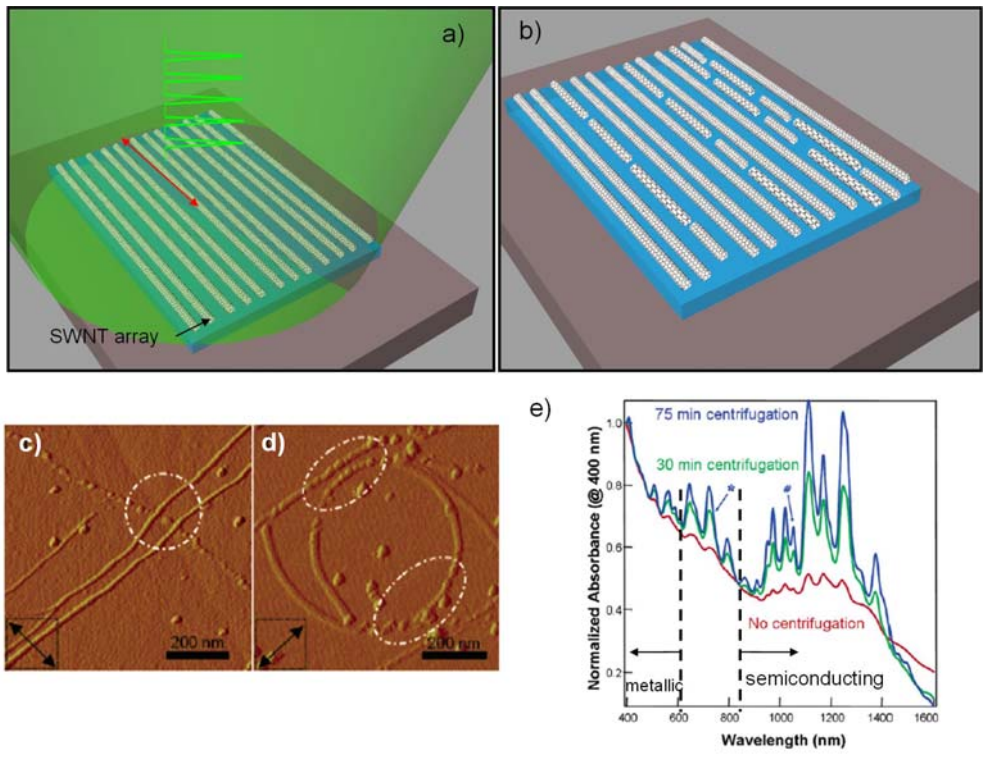

Figure 9.3 (a,b) Strategy for elimination of metallic tubes by selective laser ablation, (c,d) shows AFM images of burned and unburned SWNT with different polarization.

(e) shows measured absorption spectra for SWNT (from Nano Letters, 3, 1549) metallic and semiconducting absorption bands are shown by arrows.

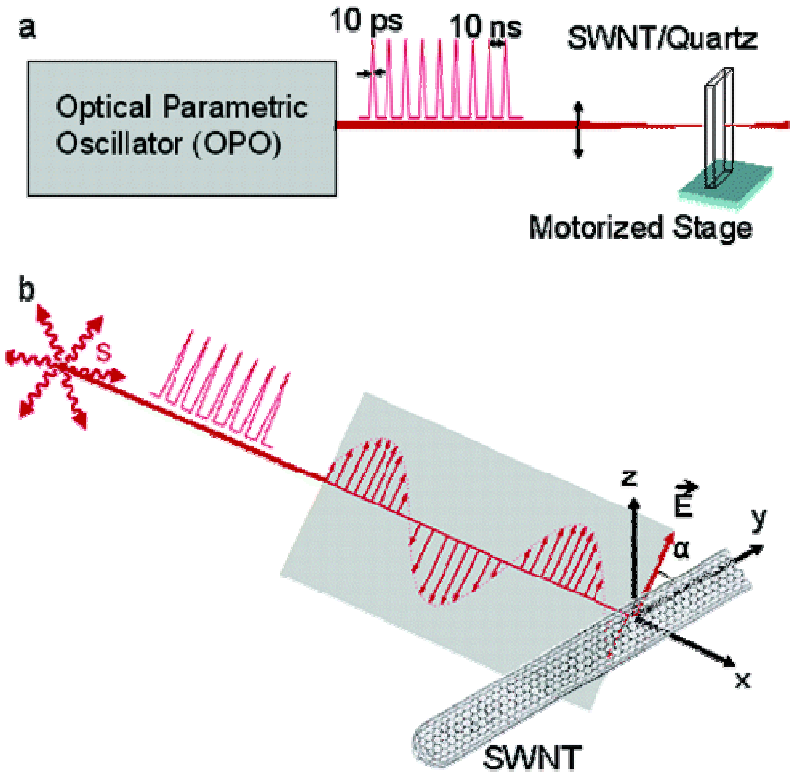

Figure 9.4 a) Experimental setup and schematic illustration of direction selective laser ablation of single-walled carbon nanotubes (SWNTs). (b) Illustration of linearly polarized light (E gives the polarization direction) oriented at an angle, α, a relative to the long axis of a SWNT.

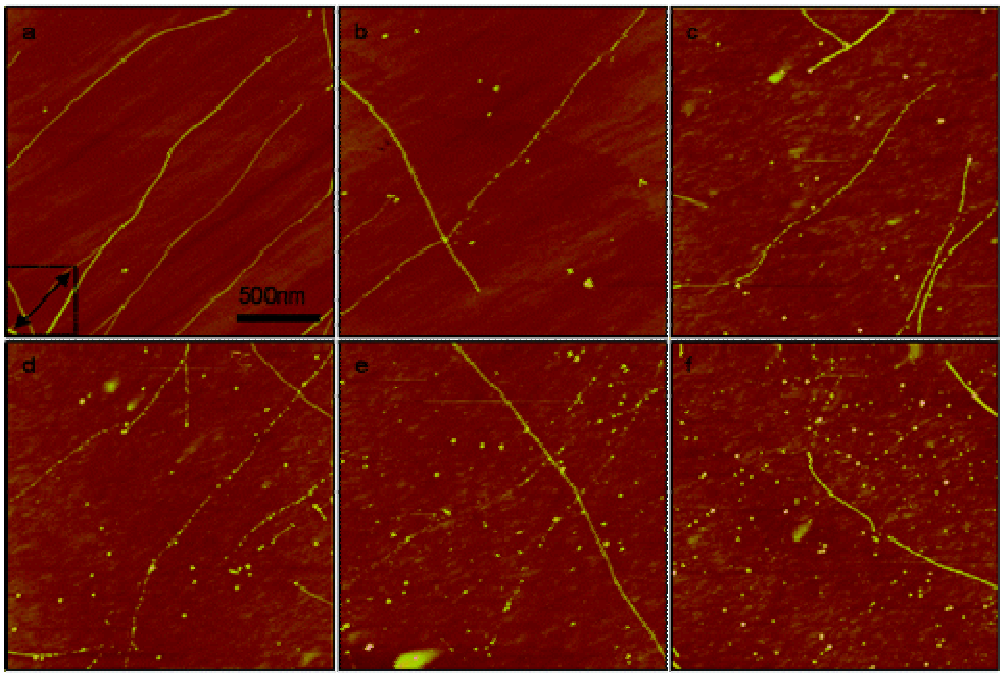

Figure 9.5 Series of AFM images of SWNTs exposed to laser pulses with different peak powers: (a) unexposed, (b) 13 MW/mm^2, (c) 27 MW/mm^2, (d) 40 MW/mm^2, (e) 53 MW/mm^2, and (f) 80 MW/mm^2. These data indicate that the threshold for ablation, as determined by morphological changes observable by AFM, is roughly 13 MW/mm^2

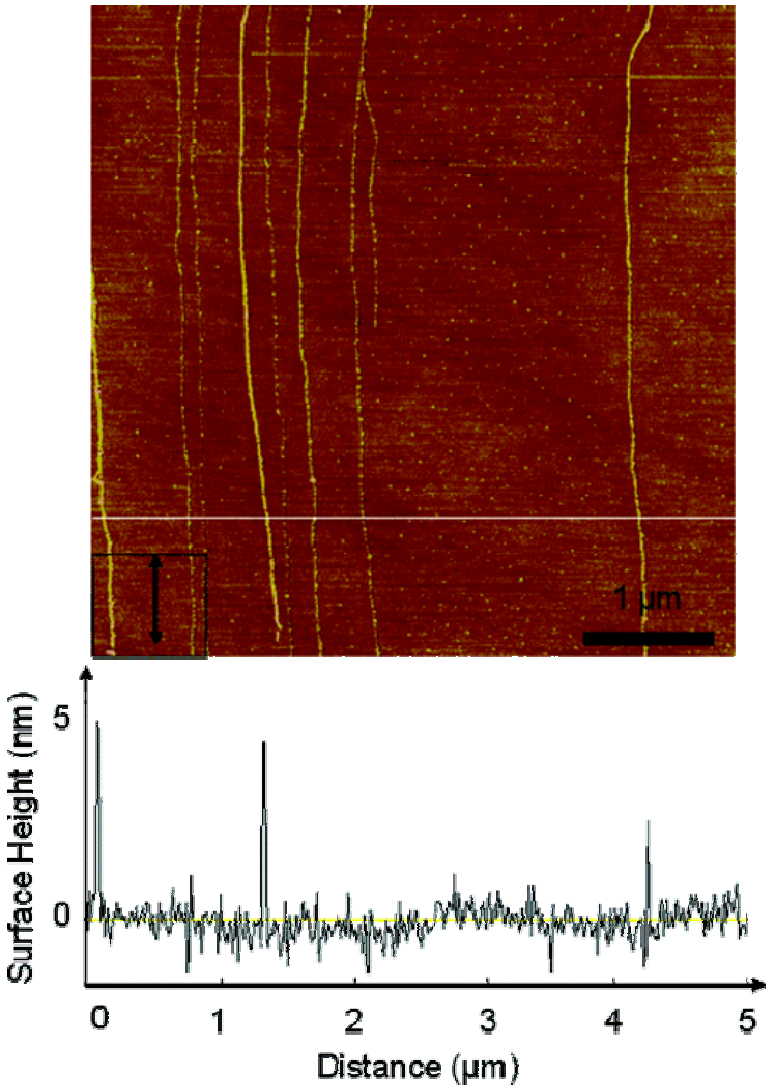

Figure 9.6 AFM image (top) and line scan (bottom) of an array of parallel SWNTs that have different diameters, between 1 and 5 nm. Inset shows the polarization direction of the laser. These data indicate that the laser can ablate tubes with a range of diameters. The ablation thresholds are comparable for the range of diameters studied.

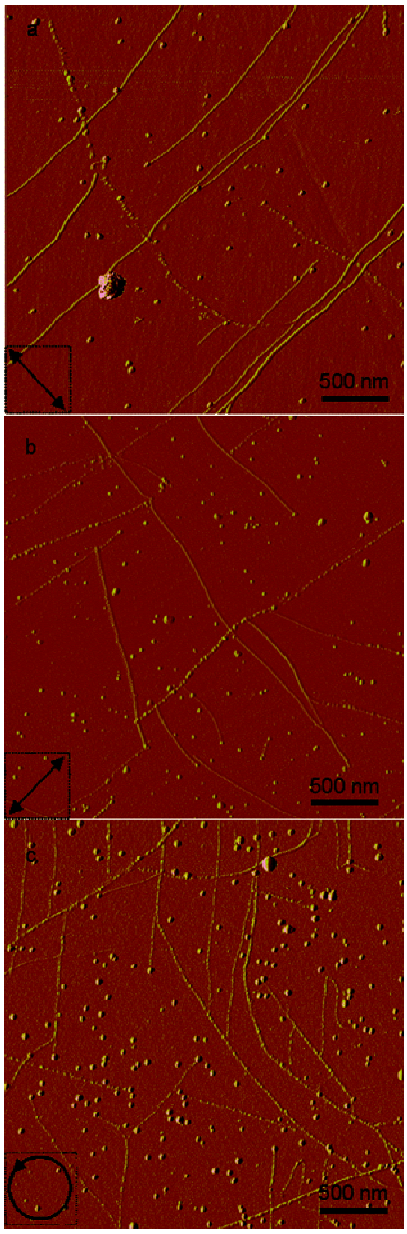

Figure 9.7 AFM images of SWNTs after exposure to intense laser pulses with linear polarization. The double headed arrows in the lower right portions of these images illustrate the polarization direction. The laser ablates only those tubes that are oriented substantially parallel to the polarization direction.

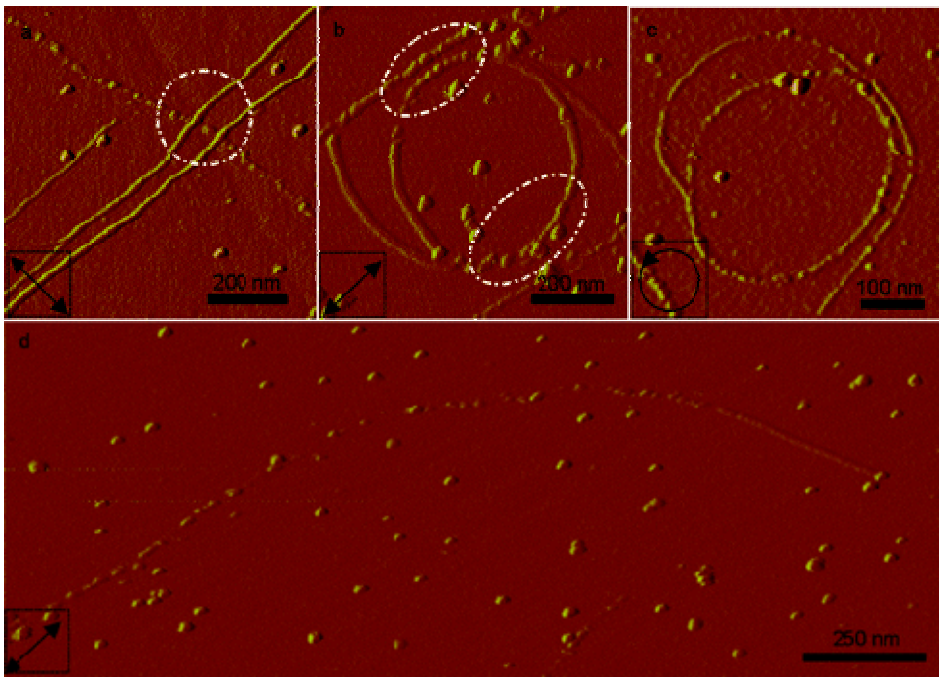

Figure 9.8 AFM images of different effects of laser ablation on collections of SWNTs. (a) Image that highlights the ability to ablate a SWNT without substantially affecting orthogonally aligned SWNTs that overlap with it. (b) Image of the results of ablating a semicircular SWNT with linearly polarized light; only the sides that are parallel to the polarization direction are ablated. (c) Image of a similar semicircular SWNT ablated with circular polarized light; in this case the entire length of the SWNT is ablated. (d) Image of a long curved SWNT in which only the segment that lies along the direction of linear polarization is ablated. In all frames the schematic illustrations in the lower left indicate the state of polarization; dotted white circles highlight the important parts of the images. These results provide important insights into the ablation process and the apparently small role that thermal diffusion plays in it.

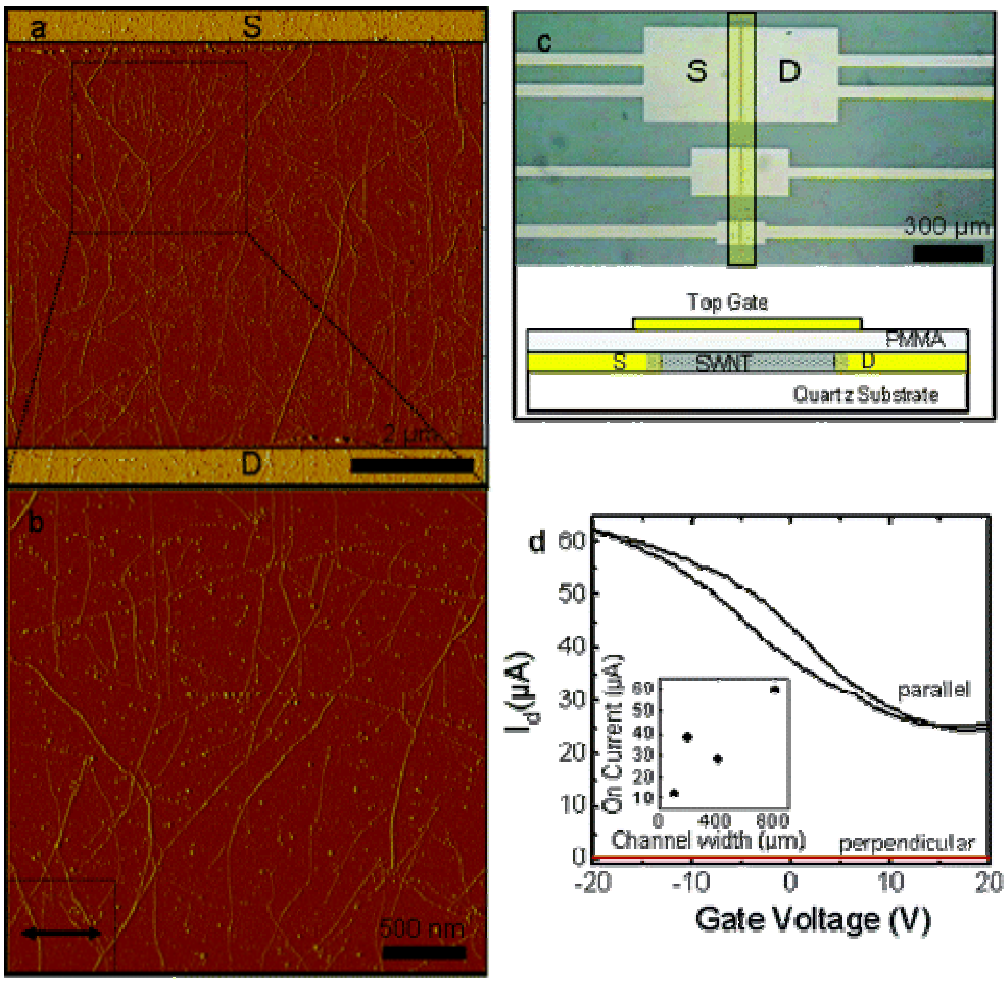

Figure 9.9 Field effect transistor that uses a collection SWNTs, some of which have been destroyed by laser ablation. (a) AFM image of the channel of a typical device; the source and drain electrodes are at the top and the bottom. The distance between them is 6 μm. (b) Magnified view of part of the channel region of the device. The inset in the bottom left illustrates the direction of linear polarization of the light used to selectively ablate some of the tubes. (c) Optical image of an array of devices (top) and schematic illustration of the device geometry (bottom). These transistors use a 1 μm thick layer of PMMA deposited onto the tubes as a gate dielectric. (d) Current/voltage response of devices that have channels oriented parallel (black) and perpendicular (red) to the polarization direction of the linearly polarized laser pulses used for ablation. These data show clearly that the laser destroys SWNTs that lie along the polarization direction.

CURRICULUM VITAE

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1. PERSONAL INFORMATION

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2. ACADEMIC DEGREES

- PhD Physics , University of Illinois Urbana Champaign, 2003-2007
- M.S. Physics, Bilkent University (Ankara Turkey) 2001-2003
- B.S. Physics, Middle East Technical University (Ankara Turkey) 1996-2001

3. ACADEMIC SCORES

- B.S. GPA 3.78/4.00
- M.S. GPA 3.86/4.00
- PhD. GPA 3.89/4.00

4. EXPERIENCE

2006 summer internship (Motorola, Tempe, Arizona)

Worked on the design and fabrication of carbon nanotube based high speed electronic devices.

2003-present (University of Illinois Urbana-Champaign, Illinois)

Developed a new technique to grow high density aligned array of single walled carbon nanotubes. Working on the physics and application of aligned SWNT arrays for macro electronics.

2001-2003 (Bilkent University, Ankara Turkey)

Developed novel integrated optical sensors for scanning probe microscopies. Analyzed the design criteria for high sensitive compact optical sensors for massively parallel arrays of atomic force microscopes.

1999-2001 (Middle East technical University, Ankara, Turkey)

Performed low temperature experiments to probe the anharmonic effects of phonon-phonon coupling in layered crystals. Concentrated on temperature dependent Raman spectroscopy of GaS and GaSe and binary compound GaSxSe1-x. Wrote all the data acquisition and analysis programs using Labview programming package.

5. HONORS, AWARDS

• METU Science Foundation Scholarship 1996-2001

• TUBITAK Science Scholarship 1996-2001

• Full scholarship awarded by Bilkent University, Turkey 2001-2003

6. PUBLICATIONS

20) Molecular Scale Buckling Mechanics in Individual, Aligned Single-Wall Carbon Nanotubes on Elastomeric Substrates

Dahl-Young Khang, Jianliang Xiao, **Coskun Kocabas,** Scott Maclaren, Tony Banks, Hanqing Jiang, Yonggang Y. Huang, and John A. Rogers

Submitted to Nature Nanotechnology,

19) Carbon Nanotube Transistor Radios

Coskun Kocabas, Hoon-sik Kim, Tony Banks ,John A. Rogers, A. Pesetski, J. Baumgardner, S. Krishnaswami and H. Zhang

Submitted to Science

18) Printed Multilayer Superstructures of Aligned Single-Walled Carbon Nanotubes for Electronic Applications

Seong Jun Kang, **Coskun Kocabas**, Hoon-Sik Kim, Qing Cao, Matthew A. Meitl, Dahl-Young Khang, John A. Rogers

Submitted to Nano Letters

17) Improved Synthesis of Aligned Arrays of Single Walled Carbon Nanotubes and Their Implementation in Thin Film Type Transistors

Coskun Kocabas, Seong Jun Kang, Taner Ozel, Moonsub Shim, John A. Rogers,

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16) Limits of Performance Gain of Aligned CNT over Randomized Network: Theoretical Predictions and Experimental Validation,

N. Pimparkar, **C. Kocabas,** S. J. Kang, J. Rogers and M. A. Alam,

"Electron Device Letters 28, , 593-595 (2007).

15) High Performance Electronics Based on Perfectly Aligned Arrays of Single Walled Carbon Nanotubes

Seong Jun Kang, **Coskun Kocabas** (equal contribution), Taner Ozel, Moonsub Shim, Ninad Pimparkar, Ashraf Alam, Slava Rotkin, John A. Rogers

Nature Nanotechnology 2, 230-236 (2007).

14) Experimental and Theoretical Studies of Transport Through Large Scale, Partially Aligned Arrays of Single Walled Carbon Nanotubes in Thin Film Type Transistors

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13) Gate Capacitance Coupling of Single-Walled Carbon Nanotube Thin-film Transistors

Q. Cao, M. Xia, **C. Kocabas**, M. Shim and J.A. Rogers, S.V. Rotkin,

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12) Spatially Selective Guided Growth of High Coverage Arrays and Random Networks of Single Walled Carbon Nanotubes and Their Integration into Electronic Devices

Coskun Kocabas, Moonsub Shim and John A. Rogers,

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11) Guided Growth of Large Scale, Horizontally Aligned Single Walled Carbon Nanotubes and Their Use in Thin Film Transistors,

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10) Printed Thin Film Transistors and Complementary Logic Gates That Use Polymer Coated Single Walled Carbon Nanotube Networks,

S.H. Hur, **C. Kocabas,** A. Gaur, O.O. Park, M. Shim and J.A. Rogers,

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9) Nanotransfer printing by use of noncovalent surface forces: Applications to thin-film transistors that use single-walled carbon nanotube networks and semiconducting polymers,

S.-H. Hur, D.-Y. Khang, **C. Kocabas,** and J.A. Rogers,

Applied Physics Letters 85(23), 5730-5732 (2004).

8) p-channel, n-channel Thin Film Transistors and p-n Diodes Based on Single Wall Carbon nanotube Networks,

Y. Zhou, A. Gaur, S.-H. Hur, **C. Kocabas**, M.A. Meitl, M. Shim and J.A. Rogers

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7) Aligned arrays of Single-Walled carbon Nanotubes Generated from Random Networks by Orientationally Selective Laser Ablation,

C. Kocabas, M.A. Meitl, A. Gaur, M. Shim and J.A. Rogers,

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6) Prism Coupling Technique Investigation of Elasto-optical Properties of Thin Polymer Films,

F. Ay, A. Kocabas, **C. Kocabas,** A. Aydinli, S. Agan,

Journal of Applied Physics , 96 (2004), 7147

5) Design and Analysis of an Integrated Optical Sensor for Scanning Force Microscopies

C. Kocabas, A. Aydinli

IEEE Sensors Journal, 5, (2005) 411

4) Integrated Micro-Ring Resonator Displacement Sensor For Scanning Probe Microscopies

I. Kiyat, **C. Kocabas**, A. Aydinli

J. Micromech. Microeng. 14 (2004) 374

3) Temperature-dependent Raman scattering spectra of ε-GaSe layered crystals,

N. Gasanly, A. Aydinli, **C. Kocabas**

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2) Anhamonicity of zone-center phonons: Raman scattering spectra of GaSe0.5S0.5 layered crystal,

N. Gasanly, A. Aydinli, **C. Kocabas**

Physica Scripta 65 (2002) 534-538.

1) Temperature dependence of first-order Raman scattering in GaS layered crystals,

N. Gasanly, A. Aydinli, **C. Kocabas**

Solid State Communications 116 (2001) 147-151.

7. PATENTS

2) Method of Making Spatially Aligned Nanotubes and Nanotube Arrays,

Pending patent,

GWS ref. 25-06; OTM ref.TF06027 (filled 3 March 2006)

Coskun Kocabas, Seong Jun Khang, Moonsub Shim, John A. Rogers

1) Integrated Optical Displacement Sensors for Scanning Probe Microscopies

The Patent Cooperation Treaty

PCT International Application No: PCT/TR03/05 (filed 18 June 2003)

Atilla Aydinli , Coskun Kocabas

8. EXPERIMENTAL EXPERIENCE

- Raman Spectroscopy,
- Photoluminescence spectroscopy
- Micro-Raman Spectroscopy
- Clean Room (Class 100,1000)
- Data Acquisition Systems

9. COMPUTATIONAL EXPERIENCE

- Finite Element Analysis Method (ANSYS, Femlab)
- Beam Propagation Method (BeamProp)
- Programming (Pascal, MATLAB, Matematica)

• Molecular Dynamic Simulation (Cerius2)

10. TEACHING EXPERIENCE

• PHYS 101 Laboratory, Teaching assistance, Bilkent University, Ankara Turkey) Fall 2001

•PHYS 580, Experimental Methods in Applied Physics, Teaching assistance, Bilkent University, Ankara Turkey) Spring 2002

• PHYS 415 Optics Laboratory, Teaching assistance, Bilkent University, Ankara Turkey, Fall 2002

• PHYS 486 Quantum Physics I, Teaching assistance, University of Illinois Urbana Champaign, Fall 2003

• PHYS 580 , Quantum Mechanics I, Teaching assistance, University of Illinois Urbana Champaign) Spring 2004

11. EMPLOYMENT HISTORY

• 2006 summer: Internship at Motorola Embedded Research Lab, Tempe Arizona

• 2004-2006: Research Assistant, University of Illinois, Urbana Champaign, Department of Physics

• 2003-2004: Teaching Assistant, University of Illinois, Urbana Champaign, Department of Physics

• 2001-2003: Research Assistant, Bilkent University, Department. of Physics

• 2001-2003: Teaching Assistant, Bilkent University, Department of Physics