ÇUKUROVA UNIVERSITY
INSTITUTE OF NATURAL AND APPLIED SCIENCES

PhD THESIS

Adnan TAN

DESIGN AND IMPLEMENTATION OF A SHUNT HYBRID ACTIVE POWER FILTER

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

ADANA, 2015

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We certify that the thesis titled above was reviewed and approved for the award of degree of the Doctor of Philosophy by the board of jury on 27/11/2015.

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This PhD Thesis is written at the Department of Institute of Natural And Applied Sciences of Çukurova University.
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ABSTRACT

PhD THESIS

DESIGN AND IMPLEMENTATION OF A SHUNT HYBRID ACTIVE POWER FILTER

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Year: 2015, Pages: 232
Jury : Prof. Dr. Mehmet TÜMAY
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This thesis presents the controller development, the power circuit design and the experimental studies for Shunt Hybrid Active Power Filter (SHAPF). In this thesis work, a novel control method is proposed for SHAPF. Thanks to the proposed control method, SHAPF provides a dynamic compensation for the current harmonics and reactive power demands of the loads with the adaptive dc link voltage. In the proposed control method, a novel individual harmonic elimination based feedback control method is applied with using Synchronous Reference Frame (SRF) method in order to improve the harmonic compensation performance. In addition, an adaptive dc link voltage reference calculation method which is dependent on the reactive power demand and the harmonic current level of the load is applied to decrease the losses of SHAPF. In the scope of this thesis work, SHAPF prototype is designed to compensate the low order dominant current harmonics of six pulse rectifiers up to 15A and the reactive power in the range of 10kVAr±30%. The effective performance of the proposed controller and the designed power and electronic control circuits for SHAPF in the steady-state and the dynamic conditions of is verified with the experimental results.

Key Words: Harmonic Compensation, Reactive Power Compensation, Passive Filters, Active Power Filters (APF), Hybrid Active Power Filters (HAPF).

ÖZ

DOKTORA TEZİ

ŞÖNT MELEZ AKTİF GÜÇ FİLTRESİNİN TASARIMI VE GERÇEKLEŞTİRİLMESİ

Adnan TAN

ÇUKUROVA ÜNİVERSİTESİ
FEN BİLİMLERİ ENSTİTÜSÜ
ELEKTRİK – ELEKTRONİK MÜHENDİSLİĞİ ANABİLİM DALI

Danışman : Prof. Dr. Mehmet TÜMAY
İkinci Danışman : Doç Dr. K. Çağatay BAYINDIR
Yıl: 2015, Sayfa: 232
Jüri : Prof. Dr. Mehmet TÜMAY
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Bu tez, Şönt Melez Aktif Güç Filtresi (ŞMAGF) için kontrolcü geliştirme çalışmalarını, güç devresi tasarımı çalışmalarını ve deneysel çalışmaları sunmaktadır. Bu tez çalışmasında ŞMAGF için yeni bir kontrol yöntemi önerilmiştir. Önerilen kontrol yöntemi sayesinde ŞMAGF, adaptif DA bağ gerilim ile yüklerin akım harmonikleri ve reaktif güç talepleri için dinamik kompanzasyon sağlamaktadır. Önerilen kontrol yönteminde, ŞMAGF' nin harmonik kompanzasyon performansının iyileştirilmesi için Senkron Referans Düzlem (SRD) yöntemi kullanılarak ayrık harmonik elemeli geri beslemeli kontrol yöntemi uygulanmıştır. Buna ek olarak, ŞMAGF' nin kontrolcüsünde sistemin kayıplarını düşürmek için yükün reaktif güç talebi ve akım harmoniği seviyesine bağımlı adaptif DA bağ referans hesaplama yöntemi uygulanmıştır. Tez kapsamında tasarımı yapılan ŞMAGF, 15A' e kadar altı darbeli doğrultucuların ürettiği düşük frekanslı harmoniklerin ve 10kVAr±%30 aralığındaki reaktif güç değişimlerinin kompanzasyonunu sağlayabilecek şekilde tasarlanmıştır. ŞMAGF için önerilen kontrol yönteminin ve tasarlanan güç ve elektronik kontrol sisteminin dinamik ve kararlı durumdaki etkili performansları deneysel sonuçlar ile doğrulanmıştır.

Anahtar Kelimeler: Harmonik Kompanzasyonu, Reaktif Güç Kompanzasyonu, Pasif Filtreler, Aktif Güç Filtreleri (AGF), Melez Aktif Güç Filtreleri (MAGF).

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude to my supervisor Prof. Dr. Mehmet TÜMAY and my co-supervisor Assoc. Prof. Dr. K. Çağatay BAYINDIR ¸ not only for their guidance, criticism, encouragements and insight throughout this research but also for their continuous confidence in me, and their unforgettable and valuable contributions to my career.

I would like to thank Prof. Dr. M. Salih MAMİŞ and Assist. Prof. Dr. M. Uğraş. CUMA for their suggestions and comments in my thesis progress committee.

I wish to express my special thanks to Dr. Alper TERCİYANLI and İlker YILMAZ for sharing their knowledge and experience on electrical power quality and active power filters.

I am also grateful to Assoc. Prof. Dr. Ahmet TEKE and Tahsin KÖROĞLU for their support.

This thesis is a part of the research project entitled as "Design and Implementation of a Hybrid Unified Power Quality Conditioner (UPQC-H) with a DC-DC Boosting Converter at the DC Link" (Project Number: 112R028) which is supported with Scientific and Technological Research Projects Funding Program by Engineering Research Group of Scientific and Technological Research Council of Turkey. I would like to acknowledge to Engineering Research Group of Scientific and Technological Research Council of Turkey for their full financial support.

Finally, I would like to express my deepest gratitude to my family for their patience, encouragement and continuous morale support.

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LIST OF ABBREVIATIONS

AC	: Alternating Current
ADC	: Analog to Digital Converter
APF	: Active Power Filter
CENELEC	: European Committee for Electrotechnical Standardization
CSC	: Current Source Converter
DC	: Direct Current
DSP	: Digital Signal Processor
EHV	: Extra High Voltage
EMRA	: Republic of Turkey Energy Market Regulatory Authority
GPIO	: General Purpose Input-Output
HAPF	: Hybrid Active power Filter
HPF	: High Pass Filter
HV	: High Voltage
IEC	: International Electrotechnical Commission
IET	: The Institution of Engineering and Technology
IEEE	: The Institute of Electrical and Electronics Engineers
IGBT	: Insulated Gate Bipolar Transistor
IHD	: Individual Harmonic Distortion
LPF	: Low Pass Filter
LV	: Low Voltage
MCU	: Microcontroller Unit
MOSFET	: Metal Oxide Semiconductor Field Effect Transistor
MV	: Medium Voltage
PCB	: Printed Circuit Board
PCC	: Point of Common Coupling
PF	: Passive Filter
PI	: Proportional Integral
PLL	: Phase Locked Loop
PQ	: Power Quality

PWM	: Pulse Width Modulation
RMS	: Root Mean Square
SHAPF	: Shunt Hybrid Active Power Filter
SRF	: Synchronous Reference Frame
SVPWM	: Space Vector Pulse Width Modulation
TCR	: Thyristor Controlled Reactor
TDD	: Total Demand Distortion
THD	: Total Harmonic Distortion
UPQC	: Unified Power Quality Conditioner
VSC	: Voltage Source Converter
3P3W	: Three Phase Three Wire
3P4W	: Three Phase Four Wire

1. INTRODUCTION

The significant increase in demand for electrical energy and the rapid change in characteristics of electrical loads with developments in technology lead electrical power quality and electrical energy efficiency issues to become more remarkable in recent years. Electrical power quality (PQ) is a considerable issue that concerns and effects the entire levels of generation, transmission and distribution of electricity and end-user loads. PQ problems can be defined as any problem occurred in amplitude, frequency and waveform of voltage and current that causes misoperation and failure of equipment connected to power systems and end user loads (Dugan et al., 2002).

Harmonics are the most encountered PQ problem in electrical power systems. Additionally, the severity and the ratio of harmonics are continuously increasing in electrical power systems because of the increase of power electronics based loads. Advances in power electronics technology lead to change the characteristics of loads distinctly. Power electronics based loads such as motor drivers, electronic balast based illumination devices, uninterruptable power supplies and welding machines etc. have nonlinear load characteristic. Even though these nonlinear loads provide an efficiency in electrical energy utilization, they are main sources of harmonics. In addition to harmonics, reactive power which is not directly defined as PQ problem in related standards causes PQ problems such as undervoltages, overvoltages and voltage fluctuations. Hence, reactive power should also be taken into account as an important issue.

In order to overcome the harmonics phenomenon, passive filter (PF) and active power filter (APF) compensation systems are developed. PFs are commonly preferred because of the low installation cost and satisfying the reactive power requirements of nonlinear loads while filtering harmonics (Fujita and Akagi, 1991). However, the drawbacks and the limited performance of PFs lead the development of APFs (Das, 2004; Akagi, 2005). APFs present an excellent performance in harmonic and reactive power compensation with compared to PFs but the cost of APFs increases extremely with increasing compensation capacity. To overcome this contradiction, hybrid APF (HAPF) topologies formed from the combination of PF and APF are developed in

order to provide the compensation requirements of dominant harmonics and reactive power demand of nonlinear loads with passive filters and decrease the ratings and also costs of APF.

The different HAPF topologies are proposed in the past two decades. Shunt hybrid active power filter (SHAPF) topology is one of the latest HAPF topology which is formed from directly series connection of PF and voltage source converter (VSC). In this topology, PF compensates a part of harmonics related to the tuning frequency and it can meet a significant part of reactive power demand of load whereas VSC part of SHAPF improves the filtering performance of PF and presents effective harmonic compensation performance (Fujita and Akagi, 1991). Moreover, VSC can keep PF from resonance conditions. This topology presents remarkable advantages especially in high power and/or high voltage applications with reduced converter ratings, a reduced converter size and an increased converter efficiency.

1.1. General Overview of Harmonics

1.1.1. Definition of Harmonics

Harmonics are defined as sinusoidal voltages or currents having frequencies that are integer multiples of the fundamental frequency of supply system (IEC, 1990; IEEE, 2009). The main sources of harmonic currents are nonlinear loads. On the other hand, the nonlinear loads cause waveform distortions on not only current waveforms but also voltage waveforms. Voltage harmonics generally arise indirectly from current harmonics which cause voltage drops on system impedances. These distorted current and voltage cause the flow of harmonic currents in the ac power system that can cause interference with other equipment (IEEE, 1992).

The nonlinear loads act as current sources which supply harmonic current to the electrical power systems. The electrical power systems are designed to operate with linear loads. The equipment that form the infrastructure of electrical power systems such as generators, power transformers and transmission and distribution lines show linear characteristics and they are represented as series and/or parallel connections of

resistors, inductors and capacitors. Furthermore, other indispensable part of electrical power systems are the reactive power compensation systems which are generally formed from large capacitor banks. When nonlinear loads are connected to the electrical power systems which consists of series and/or parallel connections of resistors, inductors and capacitors, the resonance phenomenon which cause the excessive magnification of voltage and current harmonics may occur in a point of network.

The effects of harmonics change depend on the susceptibility of loads or the power system (IEEE, 1992). The effects of harmonics on equipment can be classified as short term effects and long term effects. Short term effects are instantaneous effects that generally cause failure, malfunctions or downgraded performance of equipment through the displacement of zero-crossing point of voltage waveform. Power converters and electronic devices are the most susceptible devices exposed to short time effects of harmonics. Long term effects are related with mainly additional thermal losses and overheating in cables, transformers, motors, capacitors, etc. These problems cause excessive aging or even damage in equipment (IEC, 2002).

In order to diminish the effects of harmonics and improve the electrical power quality in electrical power systems, the prominent institutes and commissions such as the Institute of Electrical and Electronics Engineers (IEEE), the European Committee for Electrotechnical Standardization (CENELEC) and the International Electrotechnical Commission (IEC) have published standards, guides and technical reports. The foremost standards, guides and technical reports regarding harmonics are presented in Appendix A. These publications specify the descriptions, the limitations, the measurement techniques and the control of harmonic voltages and currents.

In order to determine the amount of harmonic distortion in non-sinusoidal voltage or current waveforms and set the limits for harmonic levels, several indices such as individual harmonic distortion (IHD), total harmonic distortion (THD) and total demand distortion (TDD) are defined in related standards. IHD defines the percentage of the root mean square (rms) value of individual harmonic component to the rms value of the fundamental component. IHD is used for either harmonic voltages or currents as given in Eq. 1.1.

$$IHD_V = \frac{V_h}{V_1}$$
$$IHD_I = \frac{I_h}{I_1} \quad (1.1)$$

where h is the harmonic order, $h=2, 3, 4...$

THD is also used for either voltage or current harmonics and defined as the percentage of the rms value of the harmonic components to the rms value of the fundamental component as given in Eq. 1.2. This index is used to measure the deviation of a periodic waveform containing harmonics from a perfect sine wave (Chang et al., 1998). The harmonic voltage limitations are specified with using IHD and THD indices in related standards. IEEE Std. 519-1992 offers voltage distortion limits to the utilities for low voltage (LV), medium voltage (MV), high voltage (HV) and extra high voltage (EHV) levels (IEEE, 1992). IEC 61000-2-2 and IEC 61000-2-12 present harmonic voltage compatibility levels for LV and MV levels, respectively (IEC, 2002; IEC, 2003). In addition, IEC 61000-3-6 presents harmonic voltage planning levels for MV, HV and EHV levels (IEC, 2008). EN50160 presents harmonic voltage limits for LV and MV levels which show major similarity with related IEC standards (CENELEC, 2010). When the standards related with voltage harmonic limits are compared, IEEE recommends constant limits for the individual voltage harmonics whereas the limit values of individual voltage harmonics decrease with frequency in IEC and CENELEC standards (Halpin, 2005).

$$THD_V = \frac{\sqrt{\sum_{h=2} V_h^2}}{V_1}.100\%$$
$$THD_I = \frac{\sqrt{\sum_{h=2} I_h^2}}{I_1}.100\% \quad (1.2)$$

Even though IHD and THD indices are used to specify the harmonic voltage limits, using of these indices to define harmonic current limits can be misleading under

certain circumstances. For instance, the high power equipment may draw highly distorted current when they are operating with light loads. Although they have high current THD during the light loading conditions, the effect of these distorted current on power system is negligible because the magnitudes of harmonic currents are low (Dugan et al., 2002). In order to overcome this situation, IEC and IEEE presents different approaches.

IEC published IEC 61000-3-2, IEC 61000-3-4 and IEC 61000-3-12 for harmonic current limits in only LV levels. In these publications of IEC, an equipment based classification is presented with respect to input currents and limit values are evaluated with THD and IHD indices. IEC 61000-3-2 introduces harmonic current limits for the equipment with input current below 16A. In the scope of this standard, the equipment are divided into four categories named through Class A to D and different harmonic current emission limits are defined for each category (IEC, 2014). IEC 61000-3-4 presents harmonic current limits for the equipment with input current higher than 16A. However, this technical report is valid for the equipment drawing more than 75A after IEC 61000-3-12 which introduces limits for the equipment with input current higher than 16A and below than 75A have been published. Both IEC 61000-3-4 and IEC 61000-3-12 takes different approach than IEC 61000-3-2 for the evaluation of harmonic current limits. IEC 61000-3-4 and IEC 61000-3-12 introduces the harmonic limits with respect to the ratio of the load impedance to the supply impedance available at the point of common coupling (PCC) (IEC, 1998; IEC, 2011).

IEEE Std. 519-1992 recommends a similar approach with IEC 61000-3-4 and IEC 61000-3-12 for the limitation of harmonic currents in LV, MV, HV and EHV levels. In this approach, harmonic current limits are evaluated with respect to the size of the load and the capacity of the power system to which the load is connected. This is determined with the ratio of the short-circuit current available at PCC, to the maximum fundamental load current. In IEEE Std. 519-1992, TDD is recommended for harmonic current distortion instead of THD. TDD is defined as the percentage of the rms value of the current harmonic components to the rms value of the maximum load (demand) current fundamental component, I_L drawn from PCC as given in Eq. 1.3. Individual harmonic current limits are evaluated with using the percentage of the

rms value of individual harmonic current to the maximum rms value of fundamental load current.

$$TDD = \frac{\sqrt{\sum_{h=2} I_h^2}}{I_L}.100\% \tag{1.3}$$

In Turkey, the Turkish Republic Energy Market Regulatory Authority (EMRA) has published several regulations regarding the limits of harmonic voltages and currents for the transmission and distribution companies and their customers. The harmonic limits for transmission company and their customers have introduced in Electricity Market Law (EMRA, 2015). In this regulation, the planning limit levels and the compatibility limit levels for harmonic voltages are defined for transmission voltage levels and also harmonic current limits are specified for the transmission system customers and the distribution system customers directly connected to transmission levels. The limits of harmonic voltages and currents for distribution companies and their customers are introduced in Regulation on Service Quality In Electricity Distribution and Retail Sale (EMRA, 2013). In the both of these regulations, the presented limit values are almost equivalent to those in IEC 61000-2-2, IEC 61000-2-12, IEC 61000-3-6, IEEE Std. 519-1992 and EN50160.

1.1.2. Harmonic Mitigation Techniques

To suppress harmonic pollution in electrical power system, there are two main approaches. The first approach is the improvement of equipment design for minimizing harmonic current production and the second approach is the use of compensation systems for nonlinear loads. In the first approach, effective input filters and/or circuit topologies such as phase multiplying rectifiers and PWM rectifiers are commonly applied in the equipment design to reduce the harmonic currents drawn from power system. However, this approach causes increase in the cost, the size and the complexity of the equipment. In the second approach, the harmonic pollution in

the power system is controlled by the harmonic compensation methods. The most common harmonic compensation methods are passive filters (PF), active power filters (APF) and hybrid active power filters (HAPF) consisting of PFs and APF. These compensation systems are introduced in following sections.

1.1.2.1. Passive Filters

PFs formed from the combinations of capacitors, inductors, and/or resistors have been used to control harmonic pollution in power systems for a long time. PFs are mainly classified into series PF and shunt PF. The series PFs are connected in series between power system and nonlinear loads to suppress harmonic currents by performing high impedance at tuned frequency. The sizes and also costs of series PFs increase with the load power capacity because they must be capable of carrying a full rated load current. Therefore, the series PFs are not preferred in many of applications. Shunt PFs are the most preferred PF type because they meet the reactive power requirements of nonlinear loads while filtering the harmonics. The shunt PFs are connected in parallel with nonlinear loads and they provide low-impedance paths for harmonic frequencies, thus resulting in absorbing the dominant harmonic currents of the loads. The most common shunt PF filter types are single tuned PFs, high pass PFs and C-Type PFs shown in Figure 1.1.

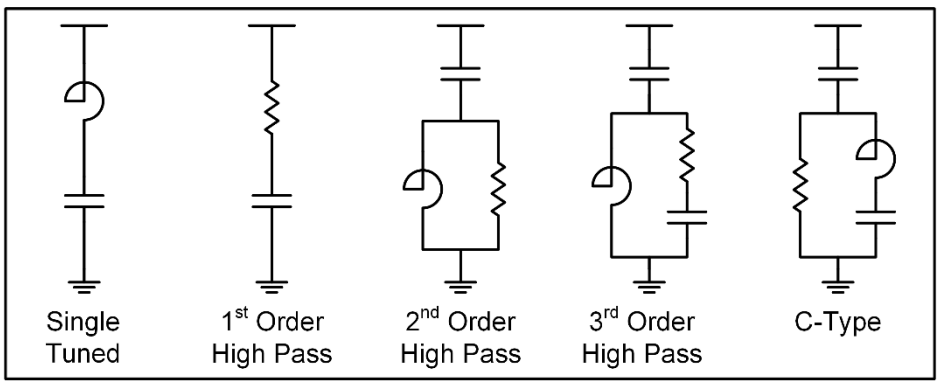


Figure 1.1. Most common passive filter types

Single tuned PFs also named as band-pass PFs or notch PFs are the most commonly used type of the shunt passive filters. Single tuned PF is tuned to a specific frequency to present low impedance for a particular harmonic current. This type of filter is the most economical type and is frequently sufficient for the many applications (Dugan et al., 1996). High pass PFs also named as damped PFs provide low impedance for a wide spectrum of harmonics. However, the high pass PFs have high losses and require high reactive power capacity for effective harmonic filtering. Because of these, they are generally designed in low power ratings to damp the high order harmonics (Arrillaga, 1985). The C-type PF which is also a type of damped filter has similar filtering performance with the high pass PFs. C-type PFs present significant advantage in fundamental frequency losses. Thus, C-type PFs can be tuned to low order harmonics between 2^{nd} and 6^{th} order harmonics with high power ratings and they are generally used in arc furnace and HVDC compensation systems (Nassif et al., 2009).

PFs have several advantages in the low installation cost, the simplicity of power circuit and meeting the reactive power requirements of nonlinear loads while filtering the harmonics. Besides the advantages of PFs, they have significant drawbacks as listed below (Fujita et al., 1991; Das, 2004);

- The power system impedance affects directly the filtering performance of PFs. The filtering performance of PFs weakens in the stiff power system whose short circuit power is in high levels. Moreover, it is difficult to anticipate the changes in the power system impedance in the design stage.
- The resonance issue is one of the prominent limitations of PFs. Parallel resonance may be formed between a source and a PF and causes amplification of harmonic currents on both the source side and PFs at specific frequencies below the tuned frequency of PFs. Moreover, PFs may fall into series resonance with a source that causes excessive harmonic currents flowing into the PFs.
- PFs cannot provide adaptation for changing power system conditions. Once installed, neither the tuned frequency nor the size of PF can be changed without changing the values of PF components.

- The aging, overloading and temperature can change the values of components in PF so these effects may cause a detuning in PF tuned frequency which must be considered in the design stage.

1.1.2.2. Active Power Filters

The drawbacks and the limited harmonic filtering performance of PFs lead the invention of APFs. The basic operating principle of APFs was originally introduced by Sasaki and Machida (1971) and the power circuit concept of APF was firstly developed by Gyugyi and Strycula (1976) in 1970s. However, APFs become technologically and economically feasible as a superior harmonic compensation system in early 1990s thanks to the developments in the power semiconductor device, microprocessor and sensor technologies (Akagi, 2005; Özkaya, 2007). In last two decades, various control methods and power circuit topologies have been applied in literature in order to improve the performance and efficiency of APFs. These achievements have played significant role in development of modern APFs which can not only achieve harmonic and reactive power compensation but also solve the various type power quality problems such as unbalanced loading, voltage fluctuation and flicker.

APFs can be mainly classified into shunt (parallel) APFs, series APFs, the combination of both series and shunt APFs named as unified power quality conditioner (UPQC). The shunt APF is connected in parallel with nonlinear load as shown in Figure 1.2 and acts as a controlled current source. The basic operating principle of shunt APF is to detect the harmonic currents in distorted load current and inject the reverse of harmonic currents to the power system so that the harmonic currents are eliminated from the supply current. The series APF is connected in series between the power system and load by using an injection transformer as shown in Figure 1.3. The main operating principle of series APF is to inject a harmonic voltage in series with the line to suppress the harmonic currents. Series APF act as a harmonic isolator and shows high impedance to harmonic currents. The main drawback of series APF is that all rated load current flows through its power circuit. This situation increases the

current ratings and losses. Additionally, it must be particularly protected against the short circuit faults. UPQC is formed by connecting the series APF and the shunt APF back to back using the same DC link as shown in Figure 1.4. UPQC is a state of art in the power quality compensation systems which presents a complete solution for all power quality problems. Its main drawbacks are the complexity of control systems and the high cost due to the power circuit.

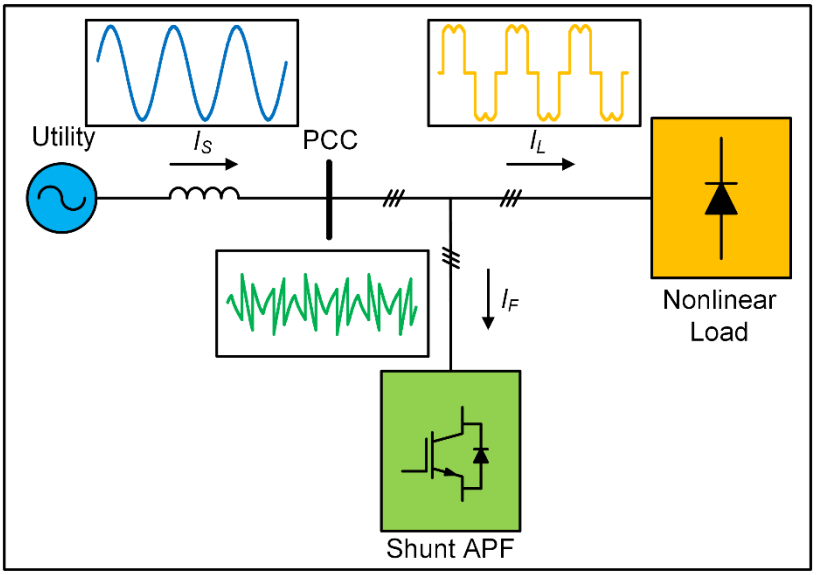


Figure 1.2. Block diagram of Shunt APF

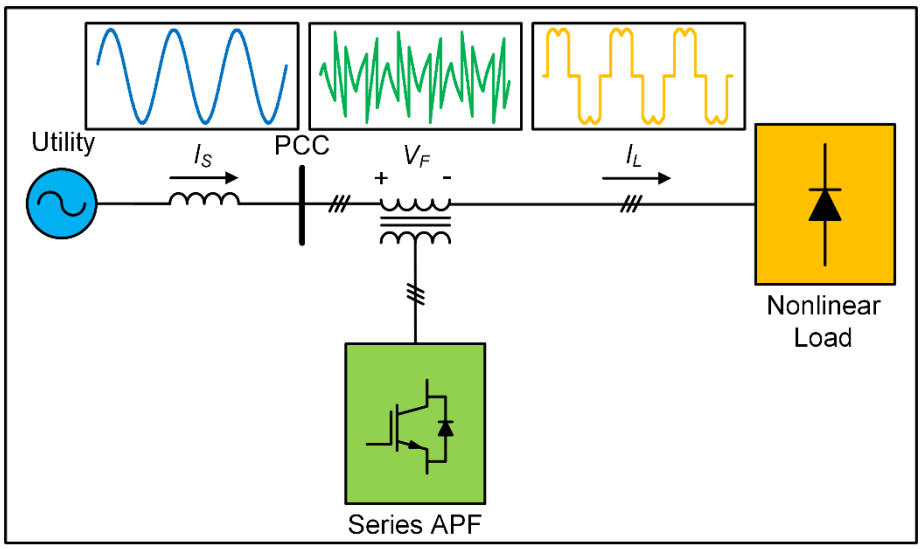


Figure 1.3. Block diagram of Series APF

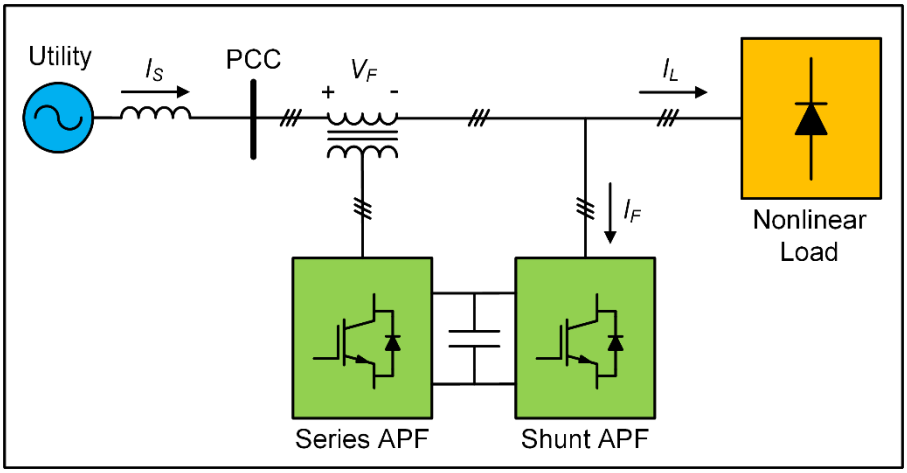


Figure 1.4. Block diagram of UPQC

The shunt APF is the most preferred power circuit topology in either the research studies or the practical applications. The power circuit of shunt APFs is realized using voltage source converter (VSC) or current source converter (CSC). The VSC based APF is formed from interface filter, VSC and dc link capacitor as shown in Figure 1.5. In VSC-APF, the dc link capacitors are used as energy storage devices that supply or absorb the required energy for the compensation of harmonics and reactive power and anti-parallel diodes are used with switching power devices in VSC for allowing reverse current flow. The CSC based APF is formed from LC interface filter, CSC and dc link reactor as shown in Figure 1.6. In CSC-APF, the dc link reactor is used as energy storage device to supply or absorb the necessary energy for the compensation and series connected diodes are used with switching devices to maintain the reverse voltage blocking capability. CSC based APF has advantages in fast and superior performance in ac current control, and inherent short circuit protection (Terciyanlı, 2010). On the other hand, CSC based APF has high initial cost, high losses and large covered area per unit power because of the bulky dc link reactor whereas VSC based APF offers advantages in high efficiency, smaller size and the low initial costs (Akagi, 2005; Routimo et al., 2007). Because of these, the studies in the literature are focused on VSC based APF and they are commonly preferred in the most of practical applications.

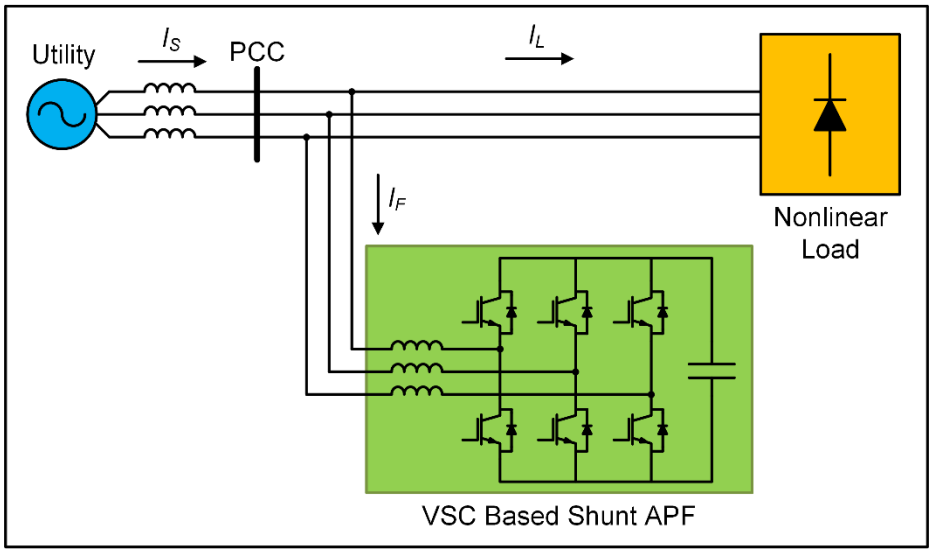


Figure 1.5. Power circuit diagram of VSC based Shunt APF

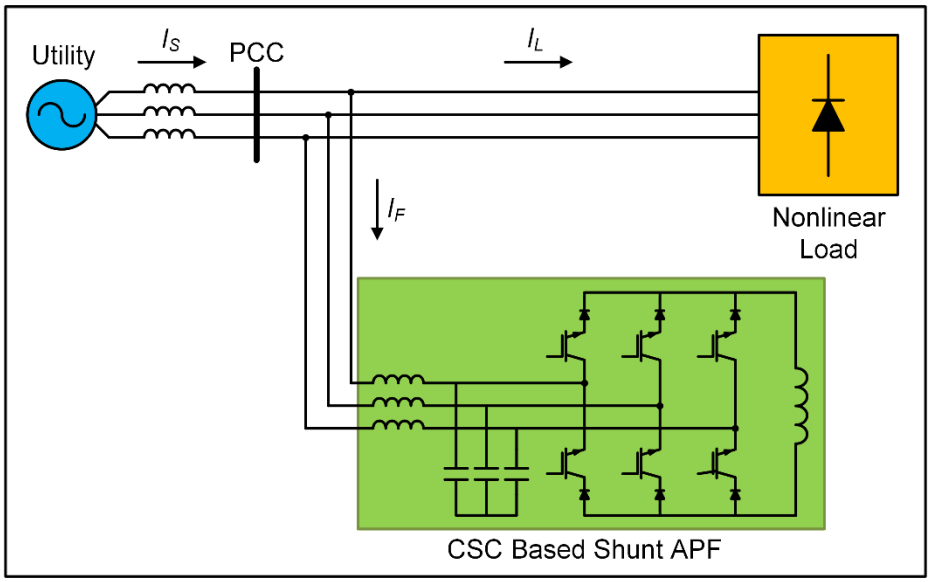


Figure 1.6. Power circuit diagram of CSC based Shunt APF

In order to compensate harmonic pollution, the shunt APFs can be located in single phase, three phase three wire (3P3W) and three phase four wire (three phase with neutral conductor - 3P4W) power systems. The high power industrial nonlinear loads are connected to 3P3W power systems, so that 3P3W VSC based shunt APFs as illustrated in Figure 1.5 are applied to compensate current harmonics in 3P3W power systems. The residential and the commercial single phase nonlinear loads are commonly fed from 3P4W low voltage distribution systems. These single phase

nonlinear loads generate triplen harmonics and unbalance loading problem which cause excessive current flow from neutral wire. In order to compensate harmonics and unbalance current problems of single phase loads, 3P4W shunt APF topologies are utilized. The most common 3P4W VSC based shunt APF topologies as shown in Figure 1.7 and 1.8 are three leg converter with split capacitor topology and four leg converter topology. In the three leg converter with split capacitor topology, the neutral wire is connected to the midpoint of dc link of APF. The main advantage of this topology is less number of power semiconductor devices and gate drivers. On the other hand, the dc link capacitor voltages must be balanced with controller and neutral current cannot be controlled independently with split capacitor topology. In the four leg converter topology, the neutral wire is connected to fourth leg of converter. This topology takes advantages in no need of dc link voltage balancing control, independent control of neutral current from phase currents and lower dc link voltage by the help of increasing modulation index to the over modulation region with injecting third-order harmonic component in reference voltages. The main drawback of four leg topology is the high number of power semiconductor and gate drivers (Pettersson, 2009).

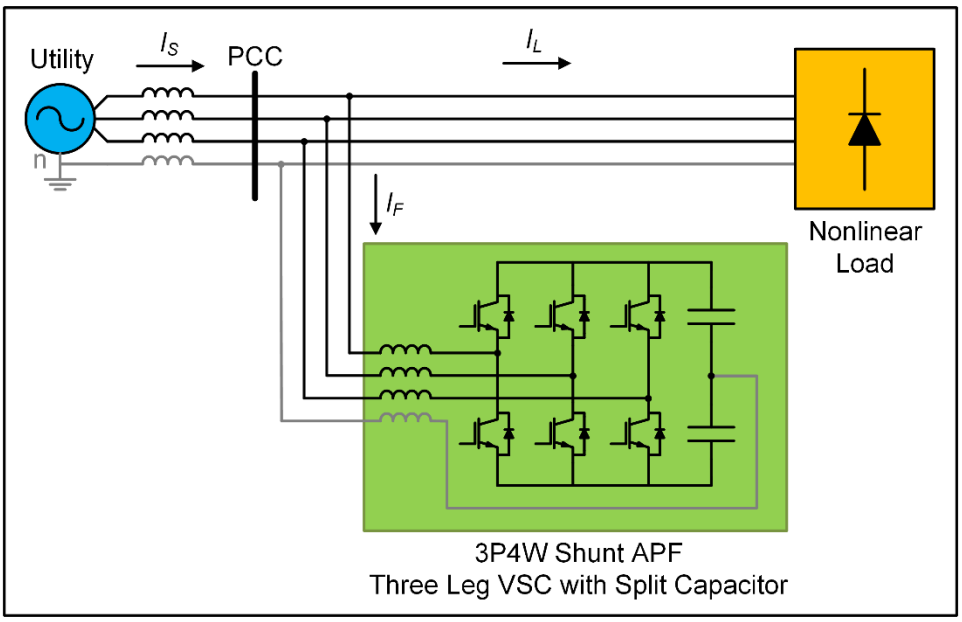


Figure 1.7. Power circuit diagram of 3P4W Shunt APF - Three leg VSC with split capacitor topology

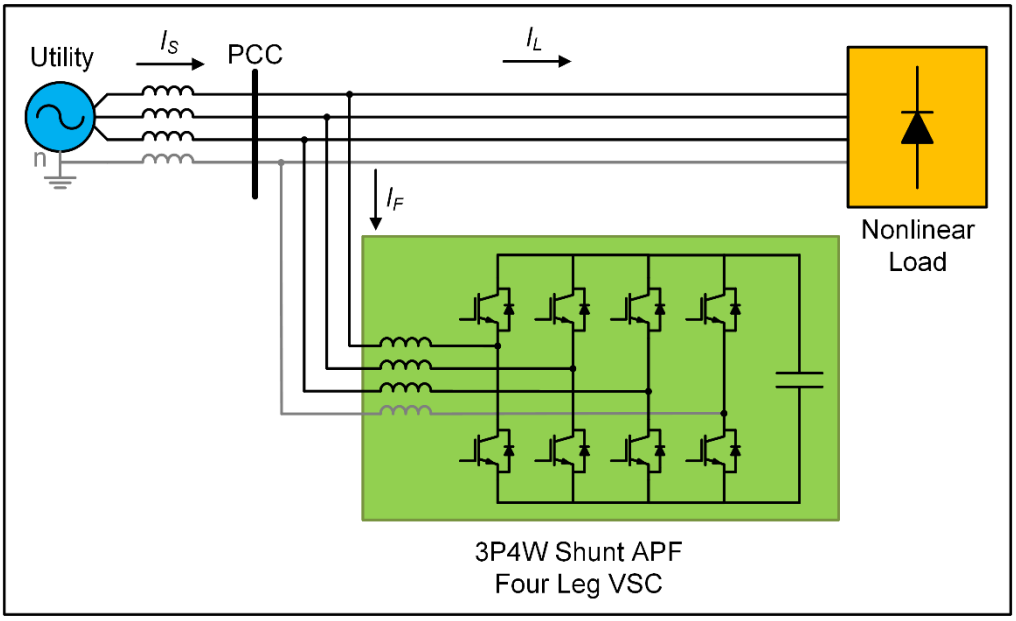


Figure 1.8. Power circuit diagram of 3P4W Shunt APF - Four leg VSC topology

1.1.2.3. Hybrid Active Power Filters

APFs are superior compensation systems for harmonics and reactive power compensation but, the cost of APF increases seriously with increasing power ratings. To overcome this contradiction, various hybrid APF (HAPF) topologies formed from the combination of PFs and APF are presented in order to provide the compensation requirements of dominant harmonics and the reactive power demand of the nonlinear loads with PFs and decrease the ratings and also the costs of APF.

There are several HAPF topologies proposed in literature. The most popular HAPF topologies are illustrated in Figure 1.9. In Figure 1.9(a), shunt APF is combined with shunt PF. This topology can be utilized from one or more shunt PF branches to compensate the major part of the reactive power and the dominant harmonics of load so that the ratings of shunt APF can be reduced by compensating only high order harmonics with the remaining part of low order harmonics and reactive power. The HAPF topology in Figure 1.9(b) consists of series APF and shunt PF. In this topology, series APF acts as harmonic isolator and increases the filtering performance of PF by showing high impedance to harmonic currents. The rating of series APF is decreased because series APF injects lower magnitude voltage for the compensation of harmonic

currents by the help of PF. The drawbacks of series active power filter limit the utilization of this topology. The latest popular HAPF topology that APF is connected with shunt PF in series is illustrated in Figure 1.9(c) and 1.9(d). In the early studies of this topology, APF is connected in series with coupling transformer and ripple filter as presented in Figure 1.9(c). However, it is shown in latest studies that APF can be connected directly series to PF in low voltage and certain level high voltage applications as demonstrated in Figure 1.9(d). This transformerless topology is named as shunt HAPF (SHAPF) in literature.

SHAPF which is the main concern of this thesis presents significant advantages. In this topology, PF capacitor holds fundamental supply voltage on its terminals so that APF keeps only the necessary dc link voltage for the compensation of harmonics. Thus, the voltage ratings, switching losses, converter size and also cost of APF are reduced. The details of SHAPF topology is presented in following chapters.

1.2. Motivation for the Thesis

Nowadays, nonlinear loads that are the main source of harmonics constitute the major part of loads connected to the transmission and distribution power systems and the harmonic pollution and their effects in power systems are increasing with the increasing number of these nonlinear loads. The compensation of harmonics with reactive power is one of the most challenging issues in the distribution systems. The conventional compensation methods based on PFs do not present sufficient performance in most cases for the compensation of harmonics and reactive power, when they are compared with APFs. APFs have an excellent performance in the harmonic filtering and dynamic compensation of reactive power.

APFs have been studied by the researchers and the engineers over thirty years in literature and it has taken place as a commercial product in market for over ten years. However, the increasing number and the changing characteristics of nonlinear loads have been revealing newer problems so that the researchers have a continuing interest on new power circuit topologies and new control methods of APF to maintain an effective compensation performance with lower cost and higher efficiency.

The most important obstacle in front of the conventional APF is the significantly increasing cost with the increasing compensation power capacity. In order to solve this drawback of APFs, the researchers focus on HAPF topologies which are the combination of APF and PFs in recent years. SHAPF topology have been become a favorite HAPF topology because of the inherent advantages. Its topology presents a lower voltage rating for VSC and also a lower switching loss than the conventional APF. Thus, it presents an improved-performance and a cost-effective solution to the compensation of dominant harmonics and reactive power in power systems. These advantages maintain recently a significant interest on SHAPF in literature which leads to improve its compensation performance and efficiency.

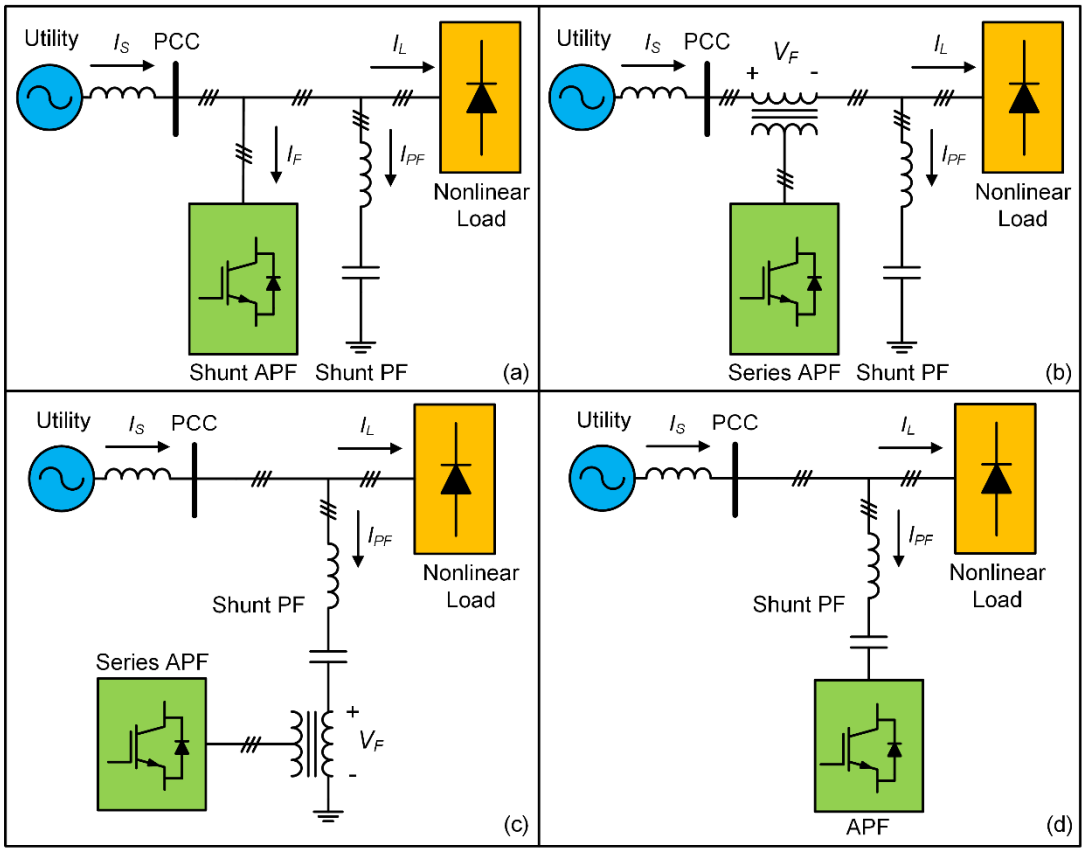


Figure 1.9. HAPF topologies
(a) Shunt APF and Shunt PF topology (b) Series APF and Shunt PF topology
(c) APF Series with Shunt PF topology (d) SHAPF topology

1.3. Scope of the Thesis

The work in this thesis consists of design, control and implementation of SHAPF. In the scope of this thesis, a laboratory prototype of 3P3W SHAPF is designed and implemented to compensate the dominant harmonic currents up to 15A and the variable reactive power demand in the range of 10kVAr±%30 of a load group installed in laboratory, which consists of three phase bridge rectifiers and inductive loads.

Synchronous reference frame (SRF) based controller is proposed in order to compensate the harmonic currents and the reactive power of the load group. In the controller, the dc link voltage level of SHAPF is instantaneously adjusted with respect to the reactive power requirements of load in order to decrease the switching losses and achieve power savings in low load conditions. The design approach of SHAPF power circuit which consists of single tuned PF and VSC is presented in detail. The verification of power circuit design and the dynamic and the steady state performance of the controller are investigated with both the simulation studies performed using MATLAB/Simulink and the experimental results.

1.4. Contributions of the Thesis

This thesis work makes following original contributions to the research and application area of SHAPF;

- An individual harmonic elimination based feedback controller is proposed for SHAPF in order to improve the harmonic compensation performance.
- The dynamic compensation of a variable reactive power demand is realized with the proposed controller of SHAPF and the performance of system is investigated with wide range changes in the reactive power demand of load.
- The dc link voltage level of SHAPF is instantaneously adjusted related to current harmonics and reactive power requirements of load by the proposed controller in order to decrease the switching losses and achieve power savings in low loading conditions.

- A detailed design approach based on theoretical analysis and simulation studies is presented for SHAPF.
- The proposed controller and design approach of SHAPF are verified by experimental results.

1.5. Outline of the Thesis

The rest of the thesis is organized as follows;

- In Chapter 2, a comprehensive literature review on SHAPF is presented. SHAPF studies in literature are classified according to their topologies. Moreover, the significant controller approaches related to SHAPF topology are classified.
- In Chapter 3, the basic circuit configuration and operating principles of SHAPF are presented. The conventional control methods of SHAPF are introduced. The general scheme of the proposed controller is described and the main parts of SRF based control scheme applied in this thesis are presented in detail.
- In Chapter 4, design and implementation of SHAPF are presented. Firstly, design requirements of laboratory prototype of SHAPF are specified. According to design specifications, design of single tuned PF, VSC and dc link performed with theoretical and simulation studies are presented. Additionally, the design and implementation of digital signal processor (DSP) based electronic control system applied to SHAPF prototype is also presented.
- In Chapter 5, the experimental results of SHAPF prototype is presented providing comprehensive case studies. The proposed controller and design approach of SHAPF is verified with experimental results. The harmonic current and reactive power compensation performance of SHAPF is demonstrated with detailed experimental results.
- In Chapter 6, general conclusions of this thesis work are given. A summary of the obtained results in this thesis work is presented. The key contributions are

highlighted. In addition, proposals of future work based on this thesis work are mentioned.

2. LITERATURE SURVEY ON SHAPF

In the literature survey of SHAPF, the databases of popular journal and conference publications such as IEEE, IET and Elsevier-Science Direct are investigated and a wide literature survey study is presented. In this literature survey, publications related with SHAPF are classified according to their topologies and controllers.

2.1. Topology Based Classification

The fundamentals of SHAPF topology was firstly introduced by Fujita and Akagi (1991). In this study, a new HAPF topology was proposed by deriving from the conventional HAPF topology formed from series APF and shunt PFs. In this topology, APF is connected in series with shunt PF using coupling transformer and interface filter as shown in Figure 2.1. This HAPF topology shows the similar compensation characteristic with the conventional HAPF formed from series APF and shunt PF. In proposed topology, APF acts as series connected resistance between source side and load in harmonic frequencies so, APF isolates harmonic currents by improving the filtering characteristics of PFs. Thanks to this HAPF topology, a significant reduction in voltage ratings of APF and the main drawback of series APF caused by flowing all rated load current through its power circuit is removed (Fujita and Akagi, 1991; Bhattacharya et al., 1997; Fujita et al., 2000; Po-Tai et al., 2000).

In following studies, the proposed HAPF topology in Fujita and Akagi (1991) was improved with connecting inverter of APF directly to shunt PF without using ripple filter and coupling transformer as shown in Figure 2.2 (Srianthumrong and Akagi, 2003). Due to the high impedance characteristic of shunt PF in switching frequencies, PF attenuates switching ripples with high ratio and usage of ripple filter is not necessary (Srianthumrong and Akagi, 2003). Moreover, this improved topology can be directly connected to the certain voltage levels without using coupling transformers by the help of series connection. In (Srianthumrong and Akagi, 2003) and (Inzunza and Akagi, 2005), it is verified by down-scaled low voltage experimental

studies that SHAPF formed from two level three leg VSC can be directly connected to 3.3kV and 6.6kV voltage levels without coupling transformers. This improved HAPF topology has been named as SHAPF in subsequent studies.

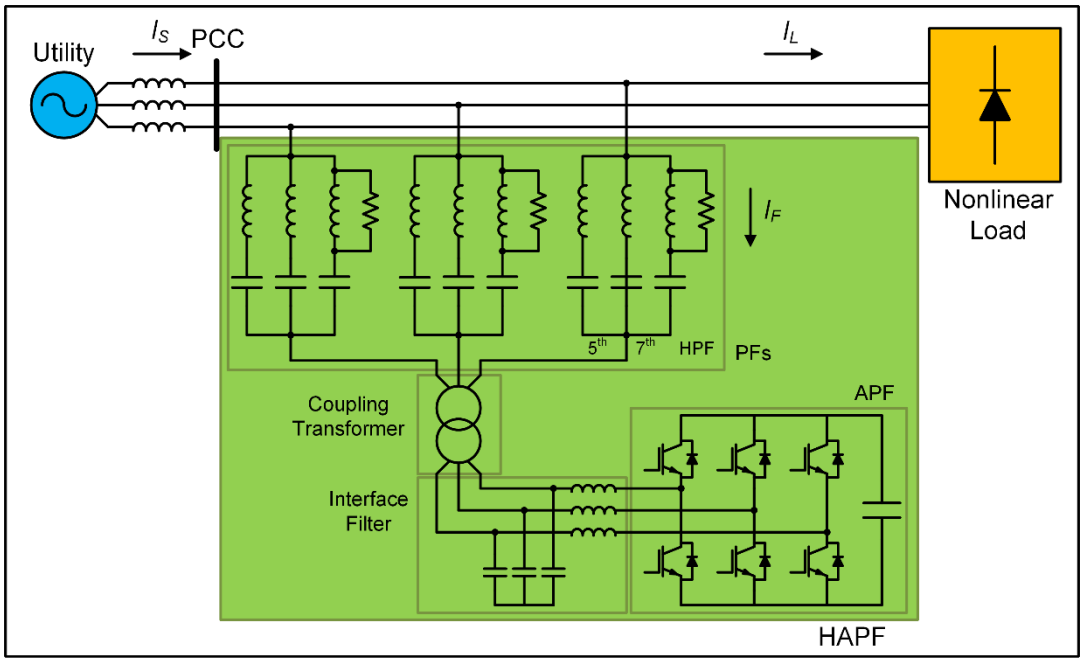


Figure 2.1. Power circuit diagram of HAPF topology introduced by Fujita and Akagi (1991)

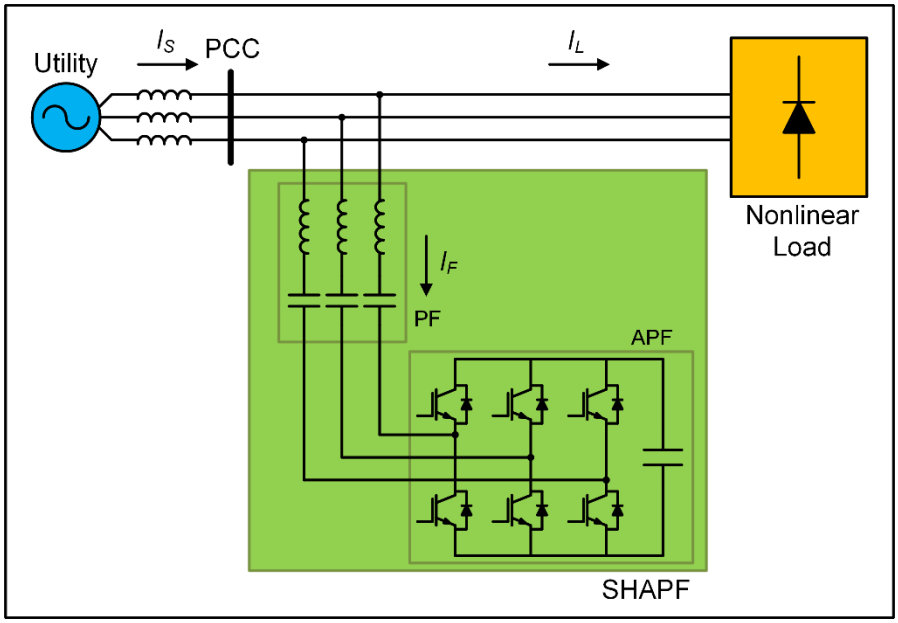


Figure 2.2. Power circuit diagram of SHAPF topology

The 3P4W SHAPF studies in literature have investigated the effect of the neutral reactor on ratings of SHAPF. In conventional three phase four wire APF topologies, the neutral reactor is only used for damping the switching ripples. However, the neutral reactor in 3P4W SHAPF topology can provide additional benefits during the compensation of zero sequence harmonic currents if the neutral reactor is tuned with the components of PF to the most dominant zero sequence harmonic frequency. By the help of this configuration, the majority of zero sequence harmonics can be filtered by PF and neutral reactor combination so SHAPF can compensate zero sequence harmonic currents by generating reduced voltage on ac side. Thus, the voltage rating of SHAPF converter can be decreased additionally by using the neutral reactor in 3P4W systems. In Lam et al. (2012), the neutral reactor is used in split capacitor three phase four wire topology as shown in Figure 2.3. In this topology, the filtering characteristic of PF and neutral reactor combination is provided during the operation of inverter of SHAPF. In Rodriguez et al. (2009), the neutral wire is connected to the positive or negative dc side of inverter with neutral reactor as depicted in Figure 2.4. By the help of this connection, it is not necessary to use balancing control for dc link capacitors in this topology. Furthermore, both positive-negative sequence and zero sequence harmonics can be filtered when the converter of SHAPF is not operating. Only disadvantage of this topology is that the PF capacitor of SHAPF holds the half of the dc link voltage across it terminals so the voltage rating of PF capacitor is increased.

With today's power electronics semiconductor technology, SHAPFs formed from two level VSCs can be directly connected to around 10kV voltage levels. In order to maintain harmonic compensation in higher voltage levels, multilevel VSCs can be utilized for SHAPF topology. There are several multilevel VSC based SHAPF studies in literature. In these studies, diode clamped multilevel VSC based SHAPF topology shown in Figure 2.5 is preferred.

In the study carried out by Akagi and Hatada (2009) and Wiroj et al. (2007), three level diode clamped VSC consisting of 1200V IGBTs was utilized for the connection of SHAPF to 6.6kV voltage level without coupling transformer. In Akagi and Isozaki (2012), the same SHAPF topology was connected to 33kV voltage level

with coupling transformer. Another considerable point seen in the diode clamped multilevel studies is voltage balancing control of dc link capacitors. In the study carried out by Akagi and Hatada (2009), voltage balancing of DC link capacitors was achieved by zero sequence current control of converter and this problem was solved with connecting reactors between midpoint of capacitors and ac line for each phase.

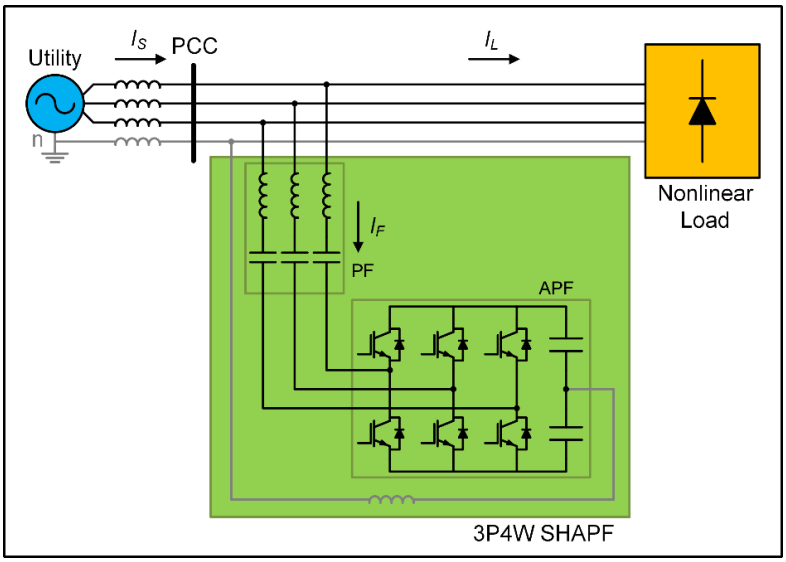


Figure 2.3. Power circuit diagram of 3P4W SHAPF - Split capacitor topology

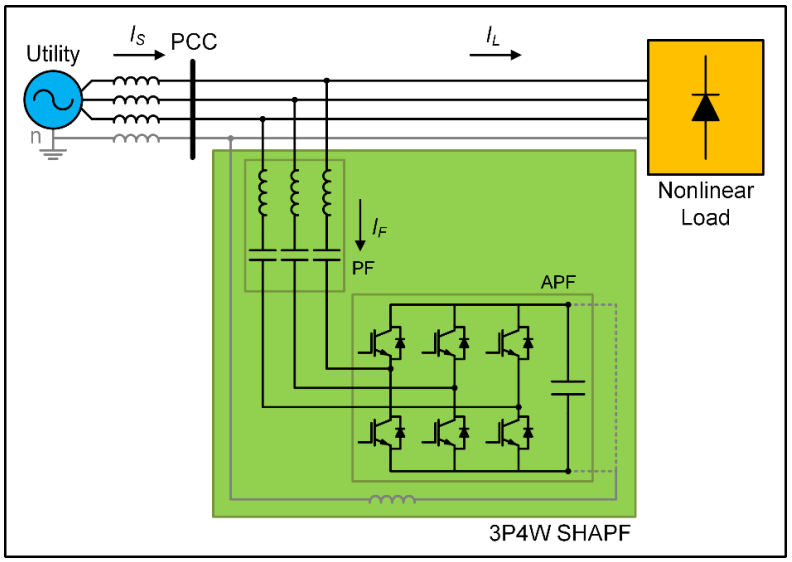


Figure 2.4. Power circuit diagram of 3P4W SHAPF - Neutral wire connected to the positive or negative DC side of VSC

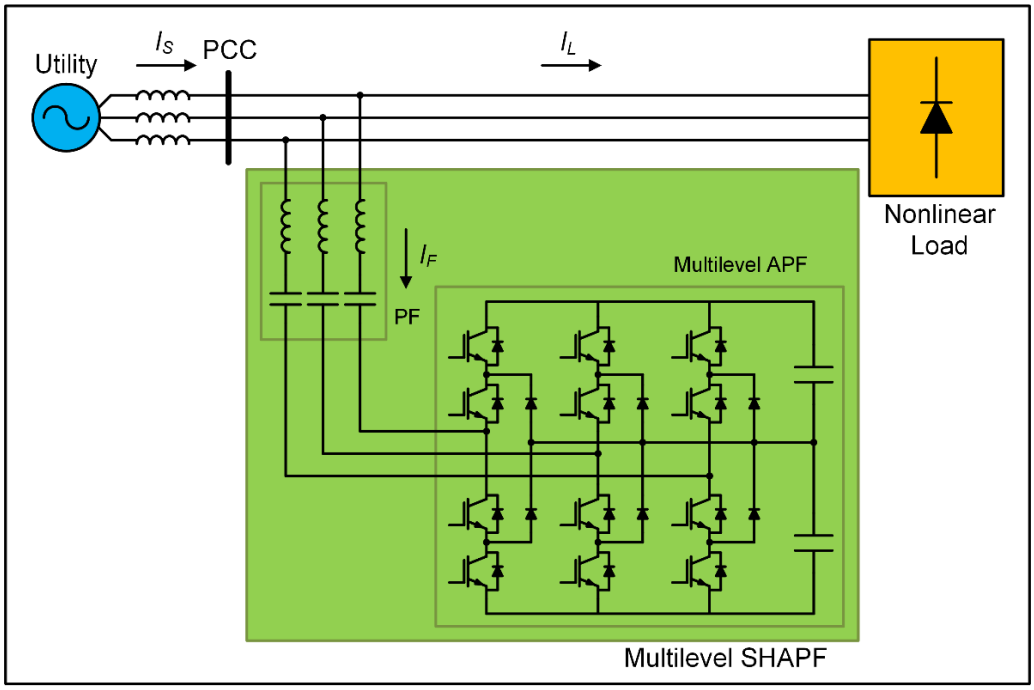


Figure 2.5. Power circuit diagram of SHAPF with three level diode clamped multilevel converter topology

In literature, various passive filter topologies and connection types are applied in SHAPF topology. Among these studies, two SHAPF topologies come into prominence. These are midpoint connected SHAPF topology shown in Figure 2.6 and injection type SHAPF shown in Figure 2.7.

Midpoint connected SHAPF topology is investigated in Herman and Papic (2012), Busarello et al. (2012) and Wu et al. (2012). In this topology, the converter of SHAPF is connected to the midpoint of passive filter reactor and capacitor. By the help of this connection fundamental reactive current of passive filter does not flow from the converter of SHAPF so the current rating of converter is decreased in addition to voltage rating. However, the studies in literature using this topology does not give details about the active power flow for establishing DC link voltage, switching ripple attenuation and fundamental reactive current and harmonic current sharing between passive filter and converter.

The prototype of injection type SHAPF topology was implemented in industrial application to compensate harmonic and reactive power demand of a copper mill at 10kV voltage level in China (An et al., 2009; An et al., 2009; An et al., 2009;

An et al., 2010; Shuai et al., 2011; Zhao et al., 2011; Zhikang et al., 2011). This topology is derived by dividing PF capacitor into two capacitor in midpoint topology and the converter of SHAPF is connected to the midpoint of the divided PF capacitors as shown in Figure 2.7. In this topology the resonance frequency of PF reactor and series connected capacitor is set to fundamental frequency. By the help of series resonance circuit, there is not any voltage seen in fundamental frequency across the terminals of converter and there is not any fundamental current flown through the converter of injection type SHAPF. Thus, the current rating of converter is considerably decreased in addition to voltage rating. On the other hand, this resonance circuit prevents the dc link voltage control of injection type SHAPF because if the converter generates voltage at fundamental frequency in the output, it causes excessive high currents in the series resonant circuit. Thus, dc link voltage of injection type SHAPF is maintained by auxiliary rectifier circuit as shown in Figure 2.7. Another problem caused by this topology is that the reference signal of injection type SHAPF control method should not contain fundamental frequency signals as the same causes in DC link voltage control. Because of these, high level control methods should be applied in the controller of Injection Type SHAPF.

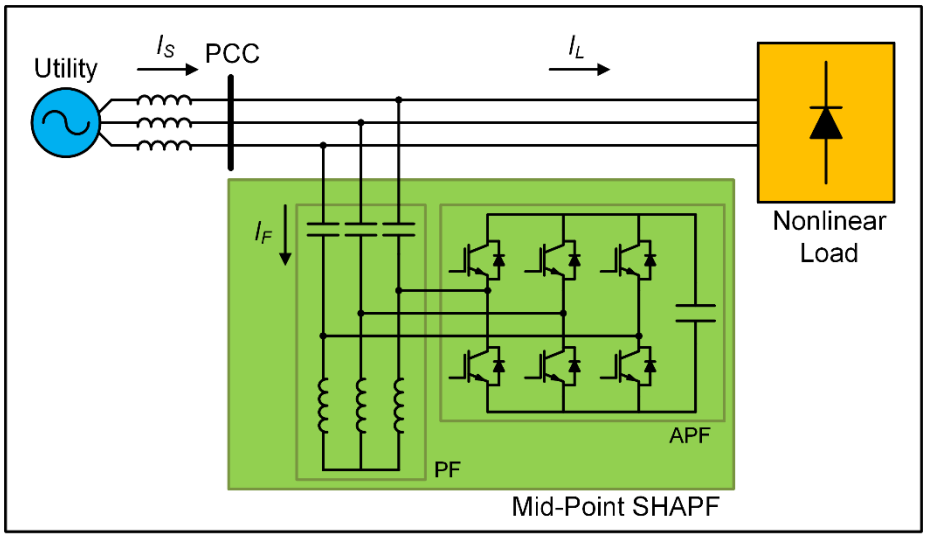


Figure 2.6. Power circuit diagram of mid-point SHAPF topology

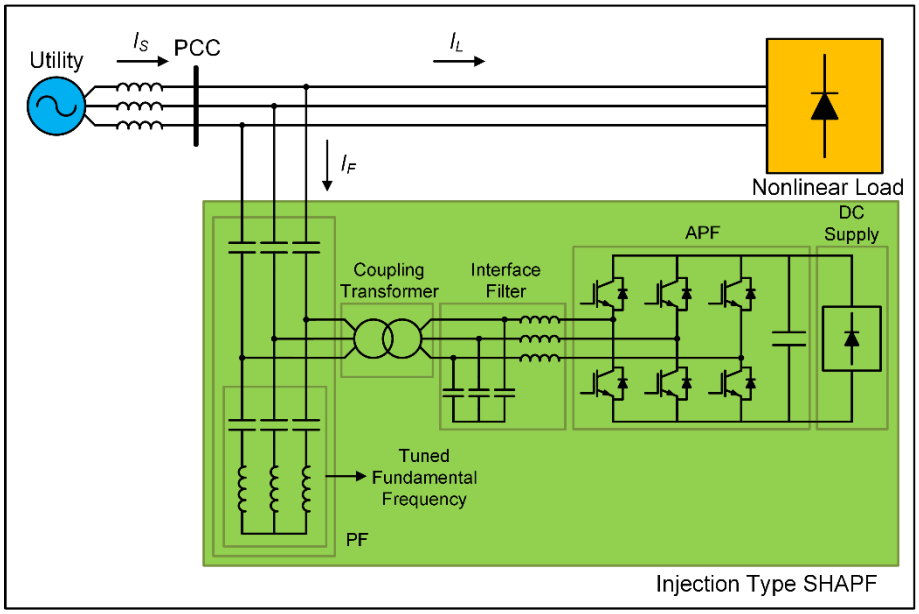


Figure 2.7. Power circuit diagram of injection type SHAPF topology

SHAPF topology is mainly proposed for the compensation of harmonics by improving the filtering characteristic of PF with APF and the compensation of constant reactive power demand with PF. However, the reactive power demand shows variation in power systems and PF can not solve the compensation of variable reactive power demand with fixed power capacity. In order to maintain dynamic reactive power compensation with SHAPF, two approaches are proposed in literature. The first approach is to provide dynamic reactive power compensation with the converter of SHAPF by means of the controller. The details of this approach are introduced under the following heading. The second approach is to improve the power circuit topology of SHAPF with new components and/or devices.

There have recently been two studies related with the second approach in literature. In these studies, the dynamic reactive power compensation is provided by combining SHAPF topology with Thyristor Controller Reactor (TCR). In Rahmani et al. (2014), TCR is connected parallel with PF capacitor of SHAPF as shown in Figure 2.8 and in An et al. (2012), TCR is combined with Injection Type SHAPF by connecting TCR directly to power system as shown in Figure 2.9. Both of these topologies presents wide reactive power compensation capability. However, additonal TCR system increase the cost and complexity of overall system.

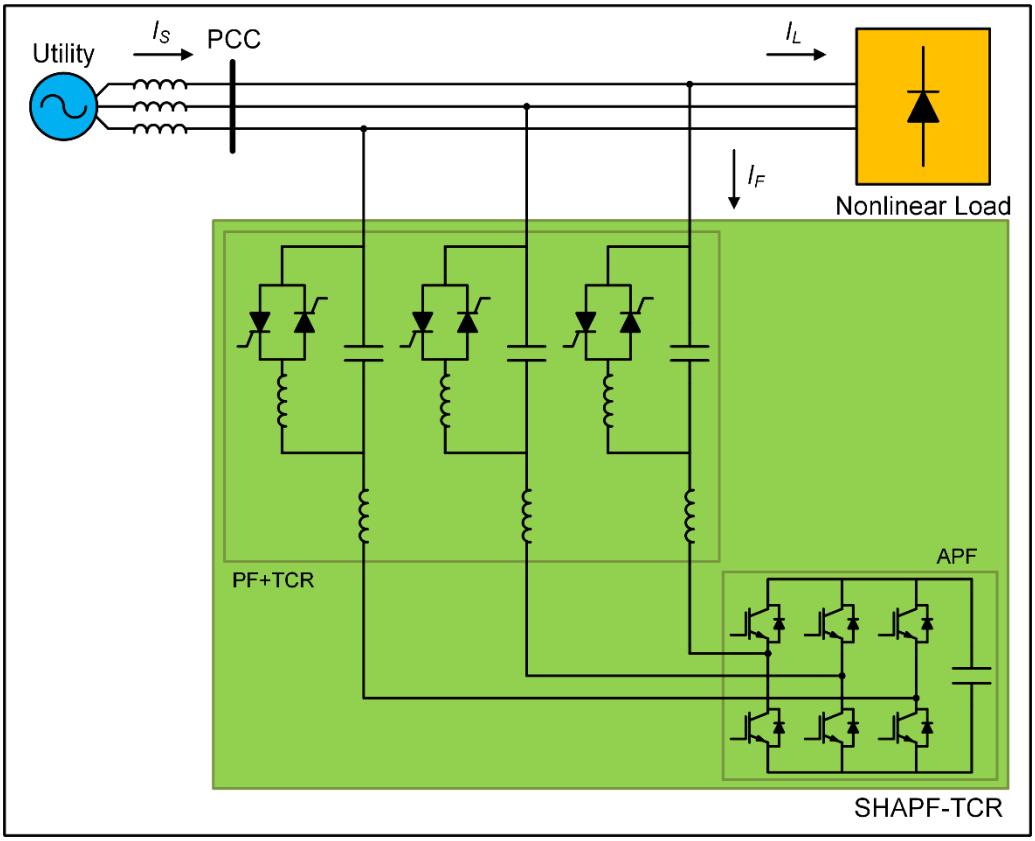


Figure 2.8. Power circuit diagram of SHAPF-TCR topology

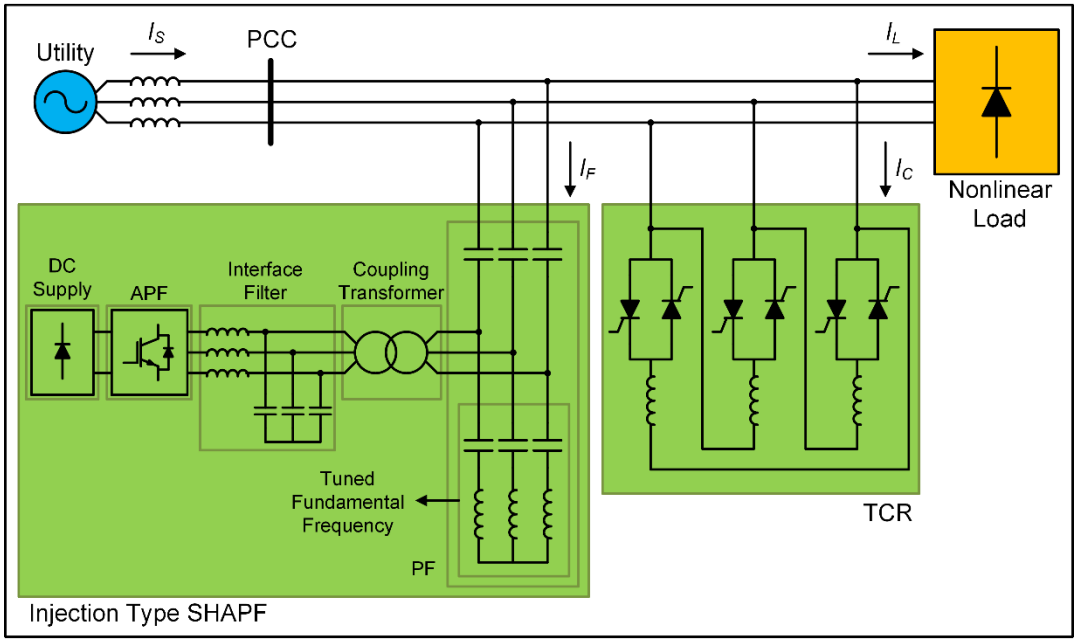


Figure 2.9. Power circuit diagram of Injection Type SHAPF and TCR combination

2.2. Controller Based Classification

The controller design has a significant impact on the compensation performance and stability of SHAPF so that various control methods are proposed to improve the performance of SHAPF in literature. The reference generation is one of the most important part of controller. In SHAPF studies, synchronous reference frame (SRF) is used as conventional reference generation method in the most of the studies in literature (Fujita and Akagi, 1991; Bhattacharya et al., 1997; Fujita et al., 2000; Bhattacharya, 2003; Srianthumrong and Akagi, 2003; Akagi, 2005; Inzunza and Akagi, 2005; Wiroj et al., 2007; Wiroj et al., 2007; Akagi and Hatada, 2009; Akagi and Isozaki, 2012). Additionally, PQ Theory (Chi-Seng et al., 2012; Lam et al., 2012), Fast Fourier Transform (FFT) (Wai-Hei et al., 2013), band pass filters (Rodriguez et al., 2009), resonant filters (Herman et al., 2014) and neural network based methods (Yang et al., 2011) are used for reference generation in the controller of SHAPF. Even though the proportional and proportional-integral controllers present sufficient performances in most cases for the current and voltage controllers of SHAPF, high level control methods such as nonlinear control techniques (Rahmani et al., 2009; Hamadi et al., 2013), Lyapunov Function based controller (Rahmani et al., 2012), sliding mode control (Hamadi et al., 2010), fuzzy logic control (An et al., 2009) and deatbeat control (Yang et al., 2011) are applied in order to improve the performance of SHAPF.

Several control approaches related with the conventional SHAPF topology come into prominent in literature. These important control approaches are determined and classified regarding the control strategies and the features of controllers. Three main topics come forward when the proposed controllers of SHAPF in literature are classified. These topics are harmonic detection methods, dynamic reactive power compensation feature and variable dc link voltage feature being dependent to the amount of harmonics and reactive power. The details of these classification are presented in following sections.

Classification According to Harmonic Detection Methods

Several harmonic detection approaches are introduced in literature for the operation of SHAPF. These are load current detection, supply current detection, supply voltage detection, SHAPF current detection and PF voltage detection. These methods have a direct effect on compensation characteristic of SHAPF. The load and supply current detection methods are preferred for SHAPFs which are installed close to nonlinear loads to filter harmonic currents. On the other hand, the supply voltage detection, SHAPF current detection and PF voltage detection methods are preferred for SHAPFs which are placed to power systems by the electric utilities in order to suppress harmonics (Akagi, 1996; Akagi, 2000).

The supply current detection method is accepted as conventional control method for the compensation of harmonic currents of nonlinear loads in many of studies (Akagi, 2005; Lam and Wong, 2014). In this approach, the required inverter output reference voltage is calculated by source side harmonics. In order to calculate exact voltage reference, source voltage and the impedance of LC passive filter must be taken into account but, the second order characteristics of LC passive filter and the dependence of source voltage make the design of controller complicated. The studies in literature, Fujita and Akagi (1991), Srianthumrong and Akagi (2003), Akagi (2005), Wiroj et al. (2007), Wiroj et al. (2007), Akagi and Hatada (2009), Bhattacharya et al. (1997), Po-Tai et al. (2000) and Rodriguez et al. (2009) propose a linear proportional controller instead of using source voltage and the impedance of LC passive filter in order to calculate output voltage reference of inverter. This model has sufficient performance in narrow frequency band harmonics and under the ideal supply voltage. In wide frequency band harmonic compensation, the linear proportional gain does not present sufficient performance and supply voltage harmonics can affect the performance of SHAPF seriously (Lam and Wong, 2014).

In several studies in literature; Hamadi et al. (2010), Rahmani et al. (2012), Hamadi et al. (2013), Rahmani et al. (2013), Lam et al. (2012), Chi-Seng et al. (2012) and Chi-Seng et al. (2014), the load current detection method is applied for the compensation of harmonic currents of nonlinear loads. In this approach, APF part is

operated as current source. Although supply voltage has no dominant effect on control loop of load current detection method, step response changes increases complexity of controller because of the second order characteristics of LC passive filter.

In order to suppress harmonic voltages in power systems, supply voltage detection, SHAPF current detection and PF voltage detection methods are investigated in Fujita et al. (2000) and Inzunza and Akagi (2005). Both of these methods are compared in Fujita et al. (2000) and it is shown with theoretical analysis that both of three method presents sufficient damping performance. SHAPF current detection method is preferred in Fujita et al. (2000) because of the effective harmonic detection accuracy compared to the other methods while the direct current control scheme with supply voltage detection method is applied to SHAPF in Inzunza and Akagi (2005).

Classification According to Dynamic Reactive Power Compensation Feature

SHAPF can compensate a complete or a part of fixed reactive power demand of loads with PF. However, the reactive power demands are variable in many applications and this variable reactive power demands are able to be compensated dynamically using voltage source converter of SHAPF. The dynamic reactive power compensation feature causes a contradiction to the efficiency of topology. In order to provide dynamic reactive power compensation with voltage source converter of SHAPF, the dc link voltage of converter must be increased to higher levels because of the impedance of passive filter. This condition is against to the reason of arising SHAPF topology which presents lower switching loss and relatively smaller size in converter with low dc link voltage. Therefore, only fixed reactive power compensation ability of passive filter part of SHAPF is emphasized and the dynamic reactive power compensation feature is not investigated in the significant number of studies. However, the dynamic reactive power compensation feature is investigated with comprehensive case studies in Chi-Seng et al. (2012), Wai-Hei et al. (2013) and Chi-Seng et al. (2014). These references state that the dynamic reactive power compensation in the certain range around the reactive power capacity of passive filter can be feasible for SHAPF with low dc link voltage increase.

Classification According to Variable DC Link Voltage Feature Being Dependent to the Amount of Harmonics and Reactive Power

SHAPF topology presents a comparatively low dc link voltage for the compensation of harmonics and reactive power. The dc link voltage level of SHAPF should be calculated relative to the maximum amount current harmonics and/or reactive power which can be compensated by SHAPF. For the variable load conditions, the dc link voltage level determined relative to the maximum load conditions can cause inefficiency in the SHAPF topology.

The variable dc link voltage is firstly applied in Po-Tai et al. (2000). In this study, dc link voltage is adaptively changed according to the current harmonic level. In Chi-Seng et al. (2012) and Wai-Hei et al. (2013), the dc link voltage of SHAPF is adaptively changed according to the dynamic reactive power compensation requirements of load. Chi-Seng et al. (2012) investigates only the reactive power compensation feature and Wai-Hei et al. (2013) presents both harmonic and reactive power compensation performance of SHAPF with variable dc link voltage which is changed by reactive power compensation requirements of load. Finally, Chi-Seng et al. (2014) uses both harmonic and reactive power compensation requirements of load in order to calculate variable dc link voltage. In this study, the current harmonic and reactive power compensation performance is investigated in detail with small step load changes.

3. OPERATING PRINCIPLES AND CONTROL OF SHAPF

3.1. Basic Circuit Configuration

The power circuit topology of SHAPF is mainly formed from single tuned PF connected series with APF, which consists of VSC and dc link capacitor bank as shown in Figure 3.1. In conventional APF topology, the dc link voltage must be kept higher than the peak value of supply voltage in order to control the active and reactive power flow and injecting harmonic currents to grid. However, in SHAPF, the capacitor of PF topology holds the fundamental supply voltage across its terminals so that APF keeps required voltage on dc link only for the harmonic compensation. Thus, the voltage ratings of VSC and dc link are significantly reduced by the series connection of PF and APF in SHAPF topology. By means of this advantage, low voltage power switching devices and dc link capacitors can be used and the size and the cost of APF can be reduced. Additionally, the switching losses in APF are considerably decreased thanks to the low voltage stress on power switching devices.

Single tuned PF is generally tuned to low order harmonic frequencies. It filters a part of dominant harmonic currents of load at tuned frequency and supplies capacitive reactive power for the reactive power demand of load. Additionally, PF attenuates the switching ripples currents of APF so that it removes the additional switching ripple filter requirement. VSC is the main part of SHAPF that generates voltage across its terminals to compensate harmonics and other power quality problems.

VSC improves the harmonic filtering characteristic of PF in SHAPF by creating harmonic isolation between load and power system. The switching devices used in VSC should be selected according to the power ratings of SHAPF. The most common switching devices used in VSCs are MOSFETs and IGBTs. MOSFETs are suitable for low power low voltage applications with low power and high switching frequency capabilities. On the other hand, IGBTs are appropriate for high power and high voltage applications with high power handling capabilities.

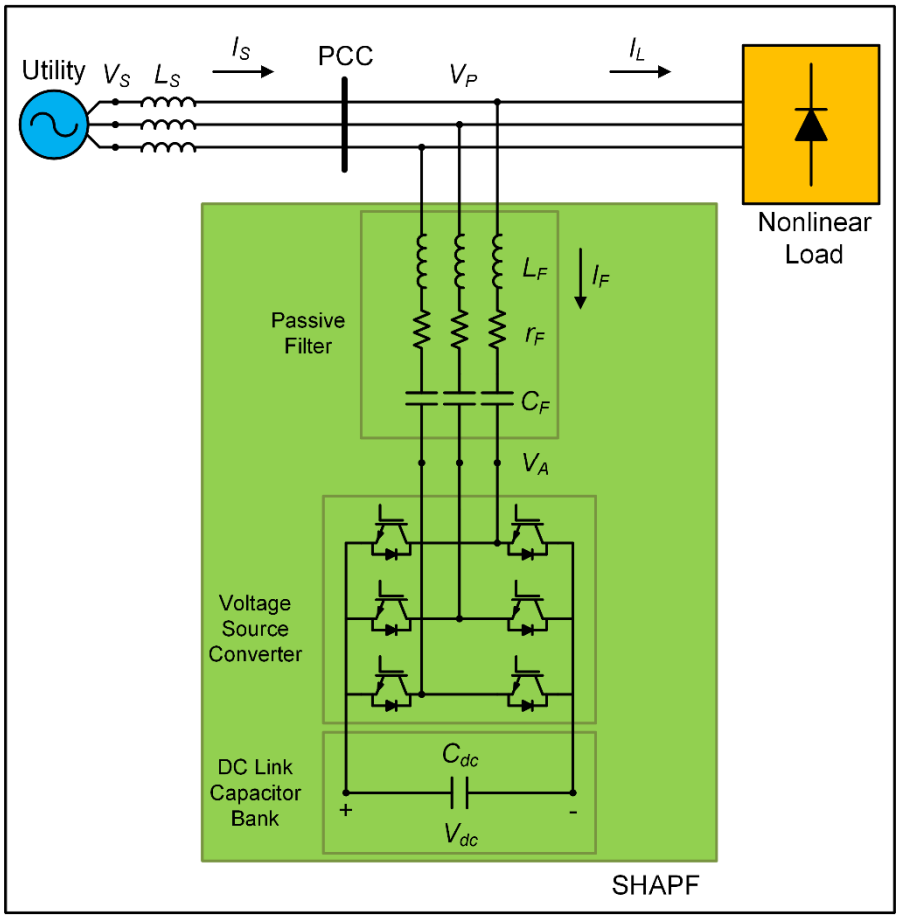


Figure 3.1. Power circuit configuration of SHAPF

The dc link capacitor bank is used as energy storage device that holds the required energy for the compensation of harmonics and/or other power quality problems. VSC of SHAPF can realize the compensation ability by supplying reactive energy to dc link and/or consuming reactive energy from dc link instantaneously. Thus, an additional dc supply is not necessary for the compensation requirements of SHAPF. The only active power requirement of SHAPF is for its power circuit losses and this can be provided by the dc link voltage controller of SHAPF which is introduced in following section.

3.2. Operating Principles of SHAPF

3.2.1. Harmonic Compensation Principles

Harmonic compensation strategies are changed with respect to harmonic detection methods of controllers which have direct effect on the compensation characteristic of SHAPF. The proposed harmonic detection methods for SHAPF in literature are as follows (Akagi, 2000; Fujita et al., 2000);

- Load Current Detection: $I_F = - I_{Lh}$
- Supply Current Detection: $V_A = G(s).I_{Sh}$
- Supply Voltage Detection: $V_A = G(s).V_h$
- SHAPF Current Detection: $V_A = G(s).I_{Fh}$
- PF Voltage Detection: $V_A = G(s).V_{PFh}$

The load and supply current detection methods are suitable for SHAPFs that are installed near the nonlinear loads to compensate harmonics and prevent the flow of harmonics through power system. The supply voltage detection, SHAPF current detection and PF voltage detection methods are suitable for SHAPFs placed in distribution systems by the electric utilities in order to suppress voltage harmonics in supply voltage (Akagi, 2000).

The load current detection method is based on feedforward control strategy. In this detection method, APF part act as a negative impedance that provide a shunt short circuit path for harmonic currents. The direct current control method should be applied in control method to ensure the reverse flow of harmonic load currents through SHAPF. The source current detection method is based on a feedback control strategy. In this method, APF part is operated with a current controlled voltage source which acts as high series impedance between the supply and the load to isolate harmonic currents. This detection method is usually implemented with indirect current control method. The supply voltage detection, SHAPF current detection and PF voltage detection methods are also based on feedback control strategy. In these detection

methods, SHAPF act as a low impedance which controls harmonic current flow in power system to suppress harmonic voltages (Akagi, 1996; Akagi, 2000; Bhattacharya, 2003).

In order to compensate harmonic currents generated by loads, the supply current detection method and load current detection method are applied for SHAPF in literature. The supply current detection method is regarded as the conventional control method of SHAPF due to the basic control scheme and the sufficient compensation performance.

3.2.1.1. Analysis of SHAPF with Supply Current Detection Method

This compensation strategy is introduced by Fujita and Akagi (1991). In this compensation strategy, APF part of SHAPF is operated a voltage source depended to source current harmonics which acts as a harmonic isolator between the source and the load to improve the filtering characteristic of PF. This compensation strategy of SHAPF can be explained with single line equivalent circuit of SHAPF shown in Figure 3.2(a). APF is assumed as an ideal controllable voltage source which generates compensation voltage V_A. The load is represented as ideal current source which generates load currents I_{Lh} in a wide harmonic spectrum. Utility is represented as an ideal voltage source with a series inductive impedance Z_S.

The voltage of APF, V_{Ah} based on supply current is given as;

$$V_A = G_S(s)G_R(s)G_{VSC}(s)I_{Sh} \tag{3.1}$$

where $G_S(s)$ is the transfer function of the controller that furnish the compensation voltage, V_{Ah} with using supply current harmonics I_{Sh}. The use of proportional controller, $G_S(s) = K$ is the common tendency to prevent phase delays in the reference generation if the detection of supply harmonics is realized by fundamental component extraction methods. $G_R(s)$ is the transfer function of harmonic reference detection method. It is generally assumed as zero gain in fundamental

frequency $|G_R(s)|_f = 0$ and unity gain in harmonic frequencies $|G_R(s)|_h = 1$ with including delay. $G_{VSC}(s)$ is the transfer function of VSC which can be modelled as a first order delay function with unity gain in general applications (Bhattacharya, 2003). In order to investigate the compensation characteristic of supply current detection method, $G_R(s)$ and $G_{VSC}(s)$ are assumed as unity gain. Therefore, Eq. 3.1 is simplified as;

$$V_A = KI_{Sh} \tag{3.2}$$

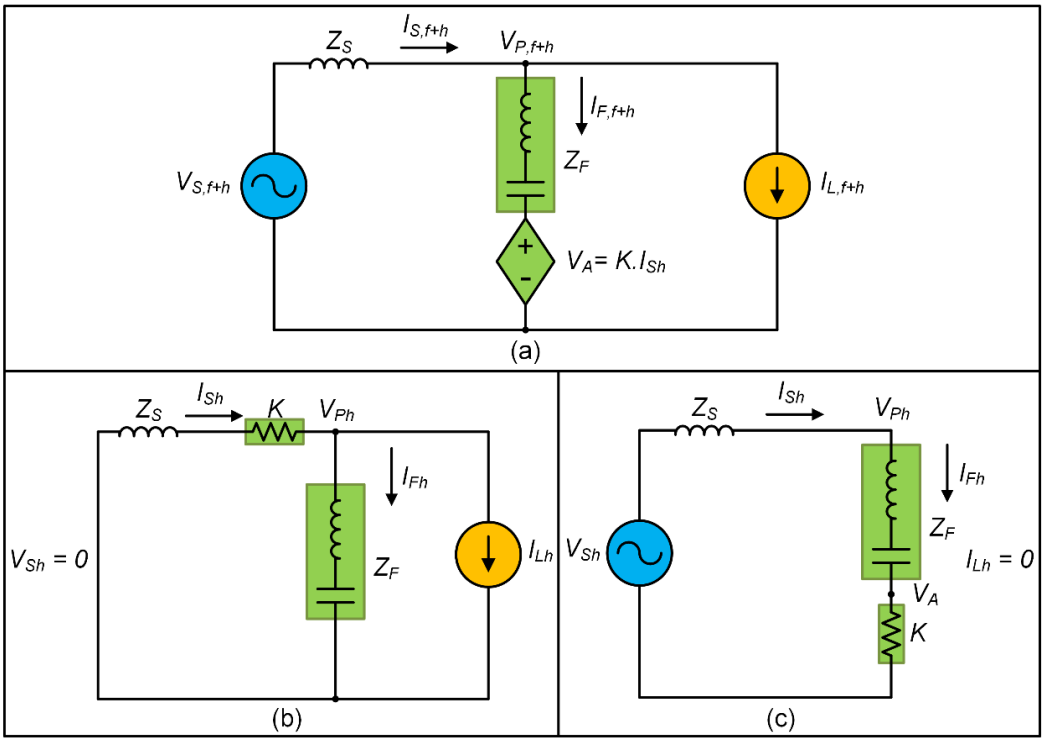


Figure 3.2. Equivalent circuits of SHAPF for supply current detection method
(a) Equivalent circuit of SHAPF
(b) Equivalent circuit of SHAPF for I_{Lh}
(c) Equivalent circuit of SHAPF for V_{Sh}

If the equivalent circuit in Figure 3.2(a) is analyzed for harmonic frequencies, the following equations are obtained for I_{Sh}, V_{Ph}, and V_{Ah}.;

$$I_{Sh} = \frac{Z_F I_{Lh}}{Z_S + Z_F + K} + \frac{V_{Sh}}{Z_S + Z_F + K} \tag{3.3}$$

$$V_{Ph} = -\frac{Z_S Z_F I_{Lh}}{Z_S + Z_F + K} + \frac{(Z_F + K) V_{Sh}}{Z_S + Z_F + K} \tag{3.4}$$

$$V_{Ah} = \frac{K Z_F I_{Lh}}{Z_S + Z_F + K} + \frac{K V_{Sh}}{Z_S + Z_F + K} \tag{3.5}$$

The system characteristic can be analyzed in terms of load current harmonics and supply voltage harmonics. The system characteristic regarding load current harmonics can be analyzed by assuming that the supply is pure sinusoidal ($V_{Sh}=0$). Eqs. 3.3 and 3.4 with considering $V_{Sh}=0$ show that APF acts as a pure resistor with the proportional controller gain, K as shown in Figure 3.2(b) to damp parallel resonance between Z_S and Z_F and increase the filtering performance of PF. If the system characteristic is analyzed in the presence of supply voltage harmonics by assuming there is no load harmonics ($I_{Lh}=0$), it is shown from Eqs. 3.3 and 3.4 that APF acts again as a pure resistor K series with PF as illustrated in Figure 3.2(c) to suppress series resonance caused by voltage harmonics and keep PF from overloading (Fujita and Akagi, 1991).

The filtering characteristic of SHAPF for load harmonic currents is demonstrated in Figure 3.3. When K is equal to 0, APF has no effect and PF is used standalone with the load. In this case, PF eliminates a part of the load harmonic currents around its tuning frequency f_c but, it has no considerable filtering effect in other harmonic frequencies. Moreover, the load harmonic currents cause parallel resonance at f_r which is below the tuning frequency of PF. With the increasing values of K, APF improves the filtering characteristic of PF and prevent the parallel resonance as shown in Figure 3.3. The damping characteristic of SHAPF for source harmonic currents caused by source voltage harmonics are demonstrated in Figure 3.4. In the case that K is equal to 0, source harmonic voltages cause the amplification of source harmonic currents because of the series resonance. For the higher values of K, the series resonance caused by source harmonic voltages can be damped by APF as shown in Figure 3.4.

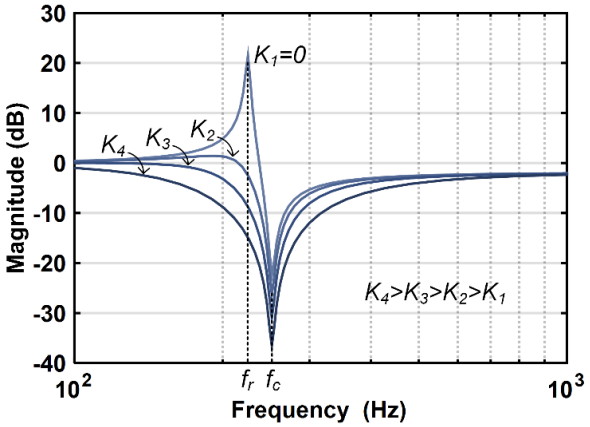


Figure 3.3. Filtering characteristic for I_{Lh}

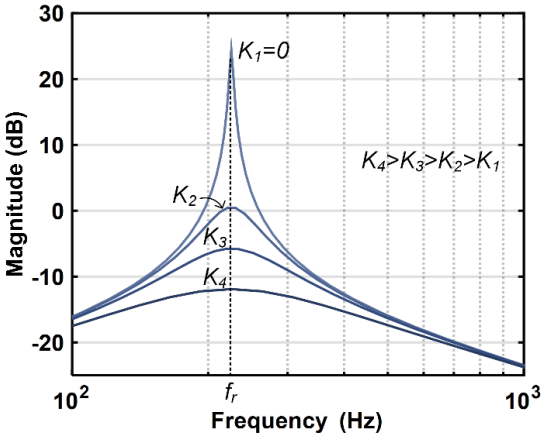


Figure 3.4. Harmonic damping characteristic for V_{Sh}

Assuming that $K>>|Z_S|$ and $K>>|Z_F|$, Eqs. 3.3, 3.4 and 3.5 are derived as;

$$I_{Sh} = 0 \tag{3.6}$$

$$V_{Ph} = V_{Sh} \tag{3.7}$$

$$V_{Ah} = Z_F I_{Lh} + V_{Sh} \tag{3.8}$$

Eqs. 3.6, 3.7 and 3.8 show that the ideal filtering characteristic can be obtained if K approaches to infinity. However it may not be possible to increase the gain as expected because of the delays in controller and the phase errors caused by the

measurement circuitry. The excessive increase of K can cause also stability problem in the controller so, K should be limited to certain values (Fujita and Akagi, 1991; Srianthumrong and Akagi, 2003).

3.2.1.2. Analysis of SHAPF with Load Current Detection Method

In this compensation strategy, APF part of SHAPF is operated as a current source depended on load harmonic currents as shown in the equivalent circuit given in Figure 3.5(a). APF is assumed as an ideal controllable current source which acts a variable negative impedance, Z_A is used to improve the filtering characteristic of PF by decreasing the equivalent impedance in harmonic frequencies as illustrated in Figure 3.5(b) (Bhattacharya, 2003).

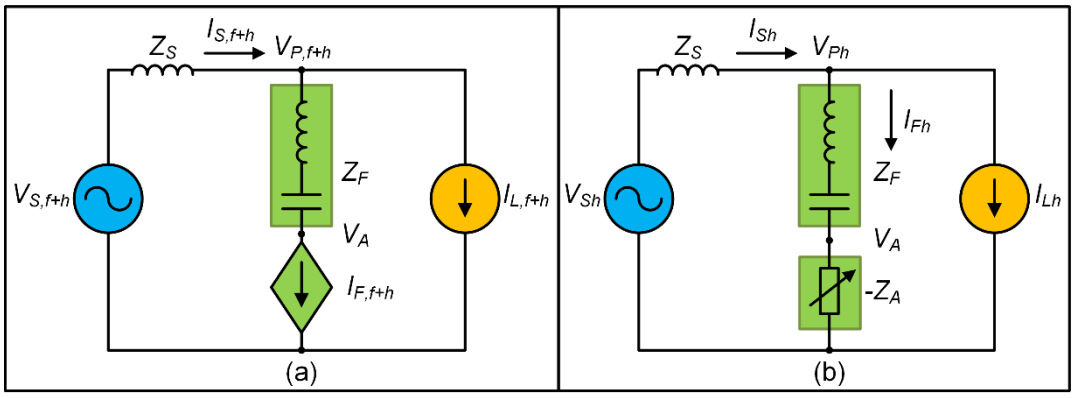


Figure 3.5. Equivalent circuits of SHAPF for supply current detection method

Z_A is dependent on load harmonic currents as given in Eq. 3.9 on the assumption of ideal harmonic detection method and ideal VSC. $G_L(s)$ is the transfer function of the controller in this equation

$$Z_A = G_L(s) I_{Lh} \tag{3.9}$$

If the equivalent circuit in Figure 3.5(b) is analyzed, the following equations are extracted for I_{Sh}, V_{Ph}, and $V_{Ah.}$;

$$I_{Sh} = \frac{(Z_F - Z_A) I_{Lh}}{Z_S + Z_F - Z_A} + \frac{V_{Sh}}{Z_S + Z_F - Z_A} \tag{3.10}$$

$$V_{Ph} = -\frac{(Z_F - Z_A) Z_S I_{Lh}}{Z_S + Z_F - Z_A} + \frac{(Z_F - Z_A) V_{Sh}}{Z_S + Z_F - Z_A} \tag{3.11}$$

$$V_A = -\frac{Z_A Z_F I_{Lh}}{Z_S + Z_F - Z_A} - \frac{Z_A V_{Sh}}{Z_S + Z_F - Z_A} \tag{3.12}$$

Eqs. 3.10, 3.11 and 3.12 show that the load current harmonic detection method can show similar harmonic filtering and resonance damping characteristic with the source current harmonic detection method in appropriate values of Z_A. Therefore, it is important that Z_A cannot be used as a simple resistor in this case. If the system characteristic is investigated in terms of load current harmonics, Z_A should have equal impedance value with Z_F in load current harmonic frequencies to achieve an effective harmonic current filtering. On the other hand, the value of Z_A should have larger than Z_F and Z_S in resonance frequencies to suppress the parallel resonance. If the system characteristic is investigated in terms of source voltage harmonics, Z_A should show again large value in voltage harmonic frequencies to keep PF from series resonance and prevent overloading of PF.

3.2.2. Reactive Power Compensation Principles

SHAPF is a type of a shunt compensator such as static synchronous compensator (STATCOM) or APF which can control capacitive or inductive output current independent of the ac system voltage. SHAPF has an inherent reactive power compensation ability thanks to PF. Although PF can provide fixed reactive power compensation, SHAPF can achieve dynamic reactive power compensation in certain power limits around the capacity of PF with sustaining its efficiency. Before introducing the reactive power compensation principles of SHAPF, the general reactive power compensation principles of shunt compensator are presented firstly.

The simplified equivalent circuit diagram of VSC based shunt compensator connected to the power system is demonstrated in Figure 3.6.

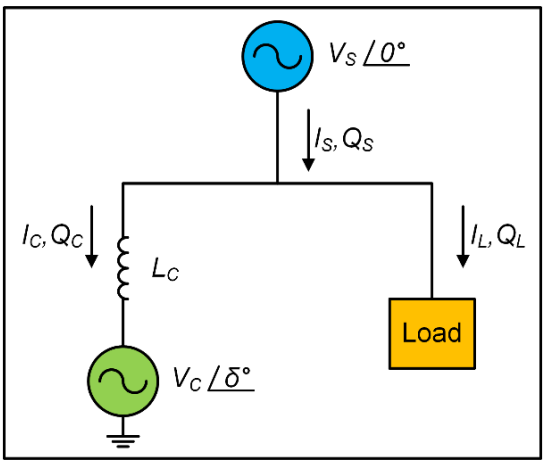


Figure 3.6. Simplified equivalent circuit of shunt compensator

If the power system and the compensator are assumed as lossless systems, the compensator controls the reactive power flow by generating voltage when V_C is in phase with supply voltage, V_S ($\delta = 0°$). Then, the reactive power supplied or consumed by the compensator is derived for lossless system as;

$$Q_C = V_S \frac{(V_S - V_C)}{X_C} \tag{3.13}$$

where X_C is the reactance of interface filter of compensator. It is shown in Eq. 3.13 that the reactive power control of compensator is maintained with the magnitude of the terminal voltage of compensator. Thus,

1) In the case of $V_C > V_S$, the current drawn by compensator, I_C leads V_S so that the capacitive reactive power is supplied to the power system and the compensator is operated in capacitive mode.
2) In the case of $V_C < V_S$, the current drawn by compensator, I_C lags V_S so that the inductive reactive power is drawn from the power system and the compensator is operated in inductive mode.

3) In the case of $V_C = V_S$, the reactive power generated by the compensator is equal to zero.

These capacitive and inductive operation modes of compensator are demonstrated with phasor diagrams and waveforms in Figure 3.7 for lossless system.

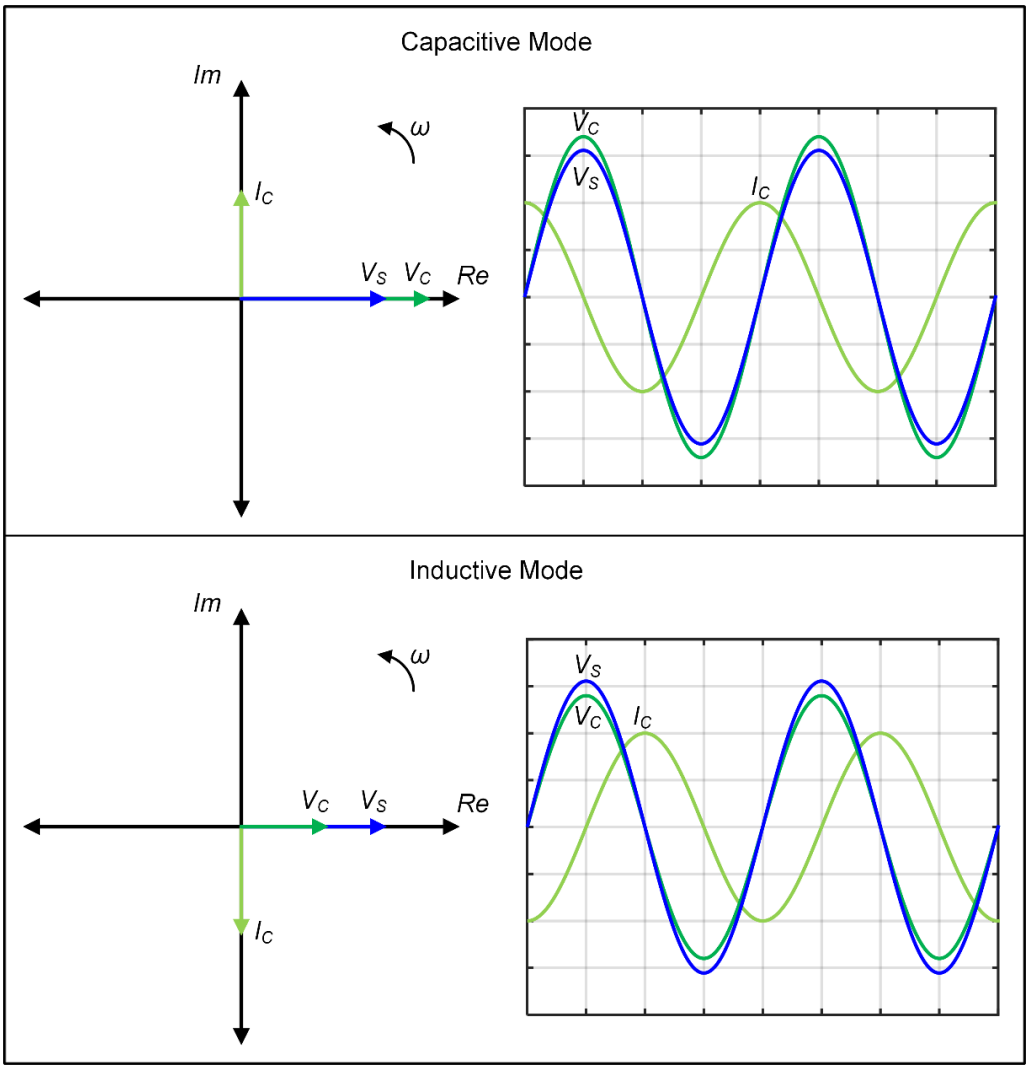


Figure 3.7. Phasor diagrams and waveforms of shunt compensator

In order to generate pure sinusoidal voltage in fundamental frequency by VSC based compensator, pulse width modulation (PWM) techniques are applied in control systems (Çetin, 2007). The rms value of fundamental component phase voltage, V_{Cphf} generated by two level VSC with PWM is defined as in Eq. 3.14;

$$V_{Cph_f} = m_a \frac{V_{dc}}{2\sqrt{2}} \tag{3.14}$$

where m_a is modulation index of PWM technique and V_{dc} is dc link voltage of VSC. It is shown from Eq 3.14 that voltage and also reactive power generated by the VSC based compensated is dependent to m_a and V_{dc}. Therefore, it can be concluded that reactive power absorbed or delivered by the compensator can be controlled by one of the following techniques (Çetin, 2007);

1) Variable modulation index m_a with constant V_{dc}
2) Variable V_{dc} with constant m_a
3) A combination of (1) and (2)

When these techniques are compared, the constant dc link voltage with variable modulation index scheme presents fast dynamic response in variable load conditions whereas the dynamic response of the variable dc link voltage with constant modulation index scheme is directly related with the inductance of interface filter and the capacitance of dc link. On the other hand, the variable dc link voltage with constant modulation index scheme maintains efficient operation in low capacitive power compensation requirements with low dc link voltage levels.

When the reactive power flow control of SHAPF is investigated, the presence of PF causes differences in the operation of APF so, SHAPF differs from the conventional shunt compensator in the reactive power flow control. The simplified equivalent circuit diagram of SHAPF connected to the power system is demonstrated in Figure 3.8.

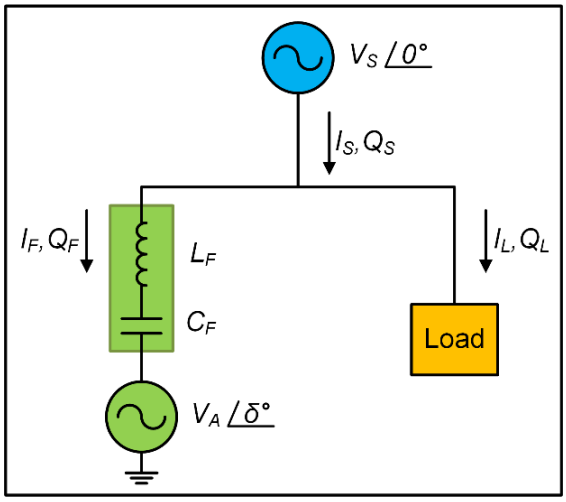


Figure 3.8. Simplified equivalent circuit of SHAPF

Again assuming the power system and SHAPF as lossless systems, APF part of SHAPF controls the reactive power flow with generating voltage, V_A in phase or 180° phase shift with V_S. Then, the reactive power supplied or consumed by SHAPF is derived for lossless system as;

$$Q_F = V_S \frac{(V_S - V_A)}{X_F} = Q_{PF} - \frac{V_S V_A}{X_F} \tag{3.15}$$

where Q_{PF} is the reactive power of PF, X_F is the reactance of PF and δ is the phase angle of APF terminal voltage, V_A which should be 0° or 180° for the reactive power flow control. Because of the capacitive reactance of PF, the reactive power flow control of SHAPF can be adjusted by magnitude and phase angle of V_A with following modes;

1) If $V_A = 0$, the reactive power generated by SHAPF is equal to Q_{PF} so the capacitive reactive power is supplied to the power system and SHAPF is operated in capacitive mode.
2) If $V_S > V_A > 0$ and V_A is in phase with V_S ($\delta = 0°$), APF part is operated in inductive mode and the reactive power generated by SHAPF is lower than Q_{PF}

but, capacitive reactive power is still being drawn from the power system and SHAPF have been operated in capacitive mode.

3) If $V_A > V_S$ and V_A is in phase with V_S ($\delta = 0°$), the current drawn by SHAPF, I_F lags V_S so that the inductive reactive power is drawn from the power system. Both APF part and SHAPF are operated in inductive mode.
4) If $V_A > 0$ and V_A is in 180° phase with V_S ($\delta = 180°$), APF part is operated in capacitive mode and the reactive power generated by SHAPF is higher than Q_{PF}. Therefore, SHAPF is operated in capacitive mode.
5) If $V_A = V_S$ and V_A is in phase with V_S ($\delta = 0°$), the reactive power generated by SHAPF is equal to zero.

SHAPF presents advantage in VSC and dc link voltage rating of APF. In order to provide conditions in 3rd and 5th modes, the dc link voltage of APF should be above two times of the peak value of V_S in linear modulation region. Thus, these modes does not comply with the invention reasons of SHAPF and they are not feasible technically and economically for SHAPF. Also, the value of V_A should be kept in certain levels for 2nd and 4th modes because of the same manners explained for 3rd and 5th cases. The operation modes explained in 1st, 2nd and 4th modes are illustrated with phasor diagrams and waveforms in Figure 3.9 for lossless system. It can be summarized that SHAPF is suitable for dynamic reactive power compensation in certain levels around the reactive power capacity of PF.

In the practical applications, the internal resistance of the output filters and VSC should be taken into account. However, the internal resistance value of the output filters is generally in the low values compared to the compensation power of the system so that the control of the compensator can be achieved by assuming the compensators as lossless systems.

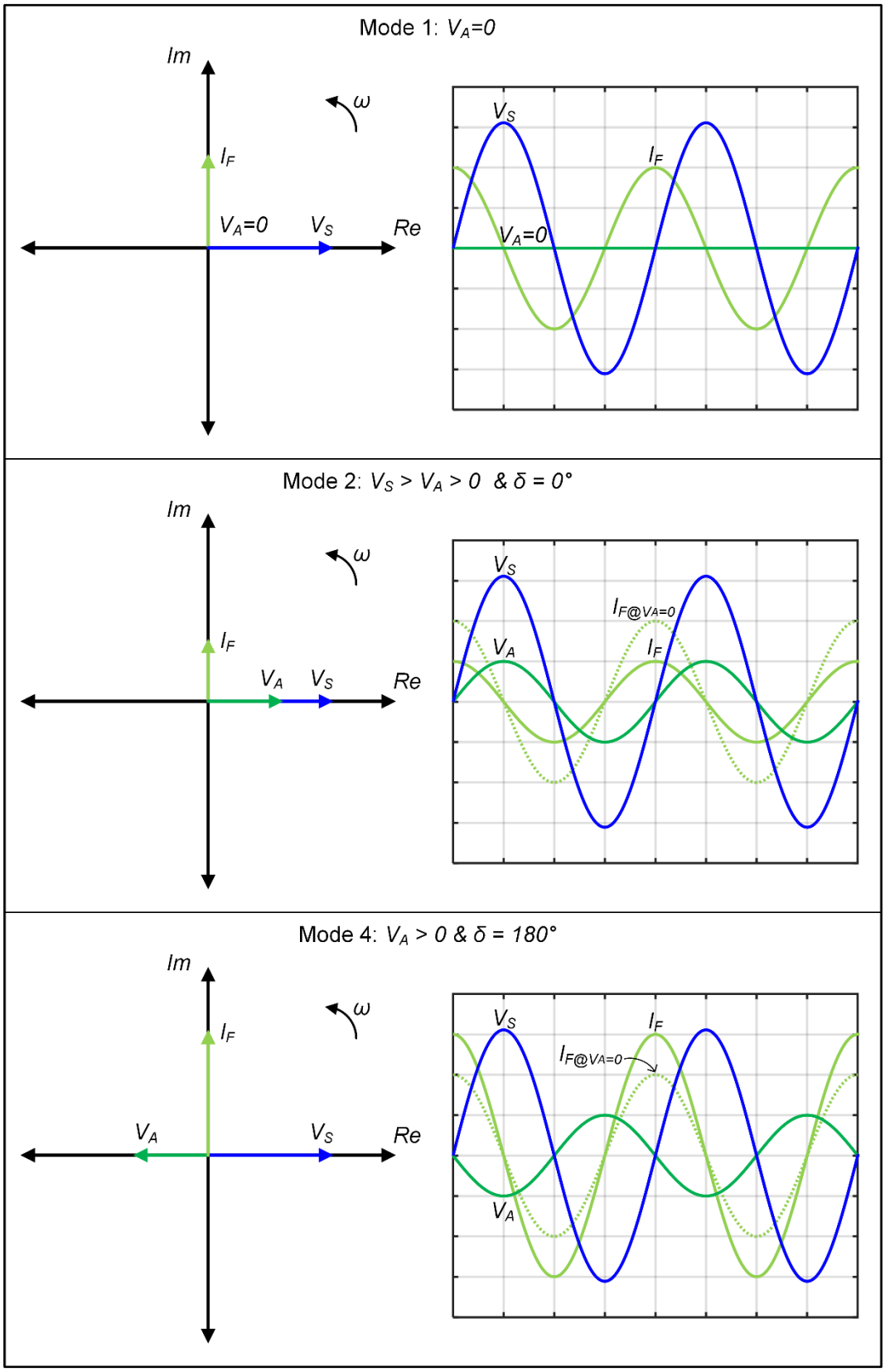


Figure 3.9. Phasor diagrams and waveforms of SHAPF

3.2.3. Fundamentals of SHAPF Controller

As considered previous section, SHAPF is a type of shunt compensator and the fundamental control scheme of SHAPF show significant similarity with the controllers of shunt compensators. The simplified control block diagram of shunt compensators is demonstrated in Figure 3.10. Mainly, the controller of shunt compensator can be divided into four main parts. These are reference generation, dc link voltage controller, current controller and gate signal generation. In the reference generation part, harmonic, reactive and/or unbalance reference currents are calculated according to the compensation requirements of shunt compensator. The dc link voltage controller is necessary for providing and keeping the required dc link voltage in constant level to achieve compensation. Current controller and gate signal generation method provide the generation of required compensation currents accurately.

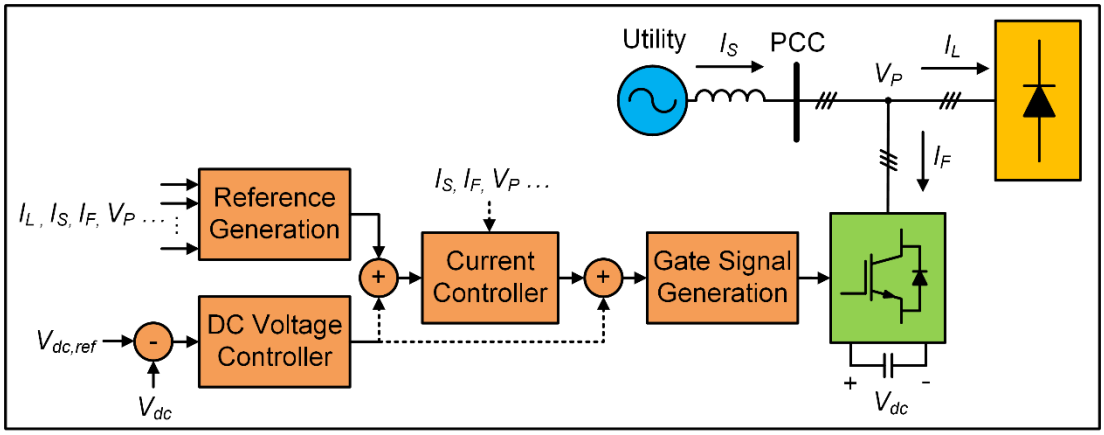


Figure 3.10. Simplified control diagram of shunt compensators

3.2.3.1. Reference Generation Methods

Reference generation methods have significant importance in the compensator performance. Especially in order to achieve effective harmonic compensation, the reference harmonic currents should be calculated fast and accurately. Moreover, the calculation complexity of harmonic extraction methods should be low for the efficient use of electronic control system resources of compensators. In order to extract

harmonics, reactive components and unbalance components, different techniques are presented in literature. These techniques are generally classified into time domain methods and frequency domain methods.

The time domain methods offer increased speed and fewer calculations compared to the frequency-domain methods. PQ Theory and SRF methods are the most popular time domain harmonic extraction methods. Both of these methods need voltage and current measurements. These methods suffer from non-sinusoidal and unbalanced supply voltage which directly affects the performances of these methods. In literature, various improvements are proposed to increase the performance of PQ theory and SRF methods in non-sinusoidal and unbalanced supply voltage conditions. Additionally, selective harmonic extraction can be achieved by the help of PLL in SRF method.

The most common frequency based methods are Fourier based methods and wavelet method. The limitations of the frequency domain approaches are that the designer has to consider the effect of aliasing. The antialiasing filter which is required to be very accurate can be used for the filtering of aliases. The accuracy of antialiasing filter is directly affects the certainty of the calculation. Moreover, sampling instant and zero crossing of fundamental are required to be synchronized. Otherwise, phase estimation will be erroneous by this process. If number of samples is not a power of two, then zero padding is required. In addition, this method of analysis is very susceptible to noise and transients (Asiminoaei et al., 2007; Bhattacharya et al., 2009).

SRF method has come into prominence with its simplicity, performance and stability. Because of these, it is one of the most preferred reference generation method in APF studies. SRF method is introduced below in detail.

SRF Method

SRF method is based on dq rotating frame transformation which represents three phase voltage and/or current signals as a space vector in rotating frame to simplify the three phase circuit calculations. In the case of pure sinusoidal and balanced three phase voltage and/or current signals, three phase ac signals are

transformed into two dc quantities. In order to understand the basics of dq rotating frame transformation, it can be useful to introduce αβ stationary frame transformation. The αβ stationary frame transformation represents three phase signals as a space vector rotating with angular velocity, θ in stationary frame. With this transformation, three phase ac signals are transformed into real (α) and imaginary (β) ac signals. The geometrical representation of three phase abc frame and αβ stationary frame is illustrated in Figure 3.11. The mathematical representation of αβ stationary frame transformation is given in Eq. 3.16. The αβ stationary frame transformation is also named as Clarke Transformation. The αβ stationary frame representation of three phase signals can be obtained with the transformation given in Eq. 3.17. The αβ stationary frame signals can be converted to abc frame with using inverse transformation given in Eq. 3.18. C used in transformation matrices is the transformation constant. If C is selected 2/3, the magnitude of α and β quantities will be equal to magnitude of three phase quantities. However if C is selected $\sqrt{2/3}$, power invariant form of expression will be obtained.

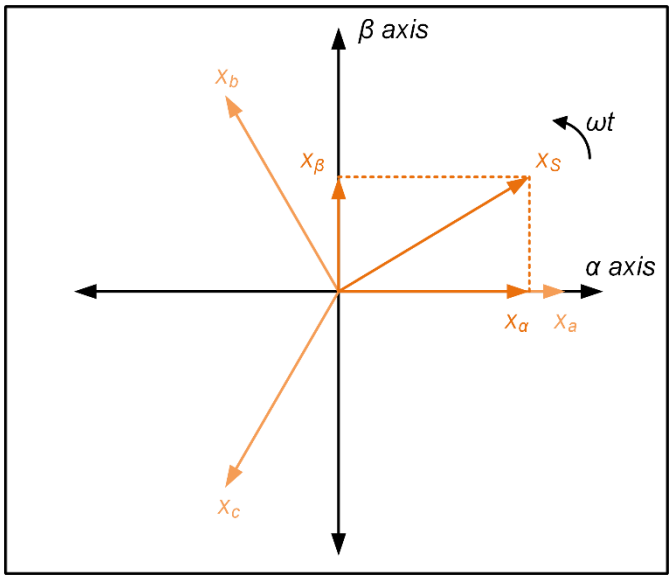


Figure 3.11. Geometrical representation of three phase abc frame and αβ stationary frame

$$x_S = x_\alpha + jx_\beta = \left(x_a + x_b e^{j\frac{2\pi}{3}} + x_c e^{-j\frac{2\pi}{3}} \right) \tag{3.16}$$

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = C \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{3.17}$$

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \frac{1}{C} \begin{bmatrix} \frac{2}{3} & 0 & \frac{2}{3} \\ -\frac{1}{3} & \frac{\sqrt{3}}{3} & \frac{2}{3} \\ -\frac{1}{3} & \frac{\sqrt{3}}{3} & \frac{2}{3} \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} \tag{3.18}$$

The dq rotating frame can be realized by rotating the stationary frame with angular velocity of three phase signals as illustrated in Figure 3.12. Therefore, the ac quantities in stationary frame becomes dc quantities in rotating frame. The mathematical representation of the rotation of stationary frame is obtained by multiplying α and β quantities with $e^{-j\theta}$ as given in Eq. 3.19. The dq rotating frame transformation is also named as Park Transformation. In the scope of this thesis work reference signals are generated with sinus based signals so the dq rotating frame transformation are achieved by assuming that the rotating frame is aligned 90° behind α axis. Therefore, Eq. 3.19 can be modified for sinus based reference signals as in Eq. 3.20. According to Eq. 3.20, the dq rotating frame representation of αβ can be obtained with the transformation given in Eq. 3.21. The three phase ac signals can be directly transformed into magnitude invariant dq frame variables with matrix given in Eq. 3.22. Inverse transformation for dq frame to abc frame, dq frame to αβ frame and αβ frame to abc frame can be obtained with transformation matrices given in Eqs. 3.23 and 3.24 respectively.

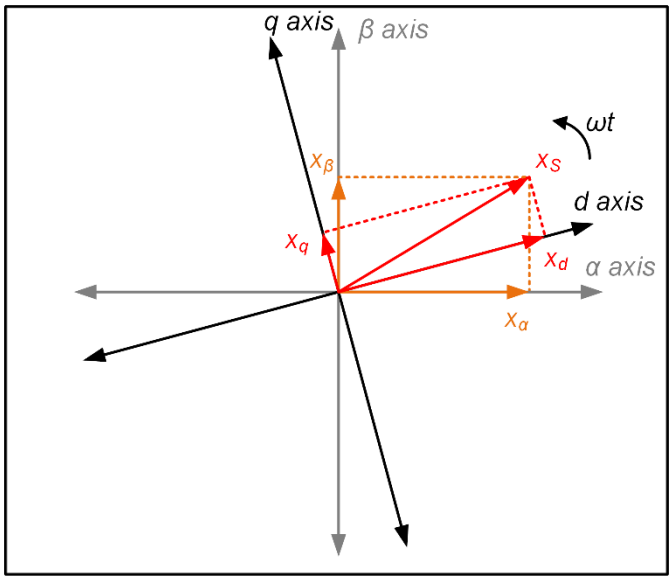


Figure 3.12. Geometrical representation of αβ stationary and dq rotating frames

$$x_S = x_d + jx_q = \left(x_\alpha + jx_\beta\right)e^{-j\omega t} = \left(x_a + x_b e^{j\frac{2\pi}{3}} + x_c e^{-j\frac{2\pi}{3}}\right)e^{-j\omega t} \tag{3.19}$$

$$x_S = x_d + jx_q = \left(x_\alpha + jx_\beta\right)e^{-j\left(\omega t - \frac{\pi}{2}\right)} = \left(x_a + x_b e^{j\frac{2\pi}{3}} + x_c e^{-j\frac{2\pi}{3}}\right)e^{-j\left(\omega t - \frac{\pi}{2}\right)} \tag{3.20}$$

$$\begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} = \begin{bmatrix} \sin(\omega t) & -\cos(\omega t) & 0 \\ \cos(\omega t) & \sin(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} \tag{3.21}$$

$$\begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{3.22}$$

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = \begin{bmatrix} \sin(\omega t) & \cos(\omega t) & 0 \\ -\cos(\omega t) & \sin(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} \tag{3.23}$$

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \begin{bmatrix} \sin(\omega t) & \cos(\omega t) & 1 \\ \sin(\omega t - \frac{2\pi}{3}) & \cos(\omega t - \frac{2\pi}{3}) & 1 \\ \sin(\omega t + \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} \tag{3.24}$$

In SRF method, active and reactive components of three phase currents, harmonic components of three phase signals and unbalance components of three phase signals can be extracted. Assume that three phase voltage and current signals are balanced and pure sinusoidal signals as given in Eq. 3.25. When SRF method is applied to three phase current signals with rotating dq frame by the fundamental phase information of three phase voltages, $\omega_1 t$ three phase current signals are transformed into dc quantities as show in Eq. 3.26. The zero component is equal to zero because of the three phase balanced current signals. Due to the rotation of dq frame with $\omega_1 t$, d component gives the active component of fundamental current and q component gives the reactive component of fundamental current.

$$\begin{aligned} v_a &= \hat{V}_1 \sin(\omega_1 t) \\ v_b &= \hat{V}_1 \sin(\omega_1 t - \frac{2\pi}{3}) \\ v_c &= \hat{V}_1 \sin(\omega_1 t + \frac{2\pi}{3}) \end{aligned} \tag{3.25}$$

$$\begin{aligned} i_a &= \hat{I}_1 \sin(\omega_1 t + \phi_1) \\ i_b &= \hat{I}_1 \sin(\omega_1 t - \frac{2\pi}{3} + \phi_1) \\ i_c &= \hat{I}_1 \sin(\omega_1 t + \frac{2\pi}{3} + \phi_1) \end{aligned}$$

$$\begin{aligned} i_d &= \hat{I}_1 \cos(\phi_1) \\ i_q &= \hat{I}_1 \sin(\phi_1) \\ i_0 &= 0 \end{aligned} \tag{3.26}$$

If three phase currents that consist of 3rd, 5th and 7th harmonics as given in Eq. 3.27 are transformed into dq frame, d and q components of three phase currents consist dc and ac components and zero component appears as given in Eq. 3.28. The fundamental current component is again transformed into dc quantities. The value of 3rd harmonic currents is equal to zero in d and q components and they are seen only in zero component. 5th and 7th harmonic currents are transformed into ac quantities on d and q components. 5th harmonic component is in negative sequence and 7th harmonic component is in positive sequence. Since the dq frame is rotated in the direction of positive sequence, 5th and 7th harmonic components have 6th harmonic angular frequencies in dq frame.

$$\begin{aligned} i_a &= \hat{I}_1 \sin(\omega_1 t + \phi_1) + \hat{I}_3 \sin(3\omega_1 t + \phi_3) + \hat{I}_5 \sin(5\omega_1 t + \phi_5) + \hat{I}_7 \sin(7\omega_1 t + \phi_7) \\ i_b &= \hat{I}_1 \sin(\omega_1 t - \frac{2\pi}{3} + \phi_1) + \hat{I}_3 \sin(3\omega_1 t + \phi_3) + \hat{I}_5 \sin(5\omega_1 t + \frac{2\pi}{3} + \phi_5) + \hat{I}_7 \sin(7\omega_1 t - \frac{2\pi}{3} + \phi_7) \\ i_c &= \hat{I}_1 \sin(\omega_1 t + \frac{2\pi}{3} + \phi_1) + \hat{I}_3 \sin(3\omega_1 t + \phi_3) + \hat{I}_5 \sin(5\omega_1 t - \frac{2\pi}{3} + \phi_5) + \hat{I}_7 \sin(7\omega_1 t + \frac{2\pi}{3} + \phi_7) \end{aligned} \tag{3.27}$$

$$\begin{aligned} i_d &= \hat{I}_1 \cos(\phi_1) - \hat{I}_5 \cos(6\omega_1 + \phi_5) + \hat{I}_7 \cos(6\omega_1 + \phi_7) \\ i_q &= \hat{I}_1 \sin(\phi_1) + \hat{I}_5 \sin(6\omega_1 + \phi_5) + \hat{I}_7 \sin(6\omega_1 + \phi_7) \\ i_0 &= \hat{I}_3 \sin(3\omega_1 t + \phi_3) \end{aligned} \tag{3.28}$$

If three phase currents that consist of positive, negative and zero sequence fundamental components as given in Eq. 3.29 are transformed into dq frame, positive sequence current component again transformed into dc d and q quantities, negative sequence current component transformed into ac d and q quantities whose frequency is equal to two times of fundamental angular frequency and zero sequence current

components appears in zero component of dq transformation as given in Eq. 3.30. If dq frame is rotated in the negative direction of phase angle information, this time, negative sequence fundamental components are transformed into dc d and q quantities and positive sequence harmonics are transformed into ac d and q quantities with two times of fundamental angular frequency.

$$\begin{aligned} i_a &= \hat{I}_p \sin(\omega_1 t + \phi_1) + \hat{I}_n \sin(\omega_1 t + \phi_n) + \hat{I}_z \sin(\omega_1 t + \phi_z) \\ i_b &= \hat{I}_p \sin(\omega_1 t - \frac{2\pi}{3} + \phi_1) + \hat{I}_n \sin(\omega_1 t + \frac{2\pi}{3} + \phi_n) + \hat{I}_z \sin(\omega_1 t + \phi_z) \\ i_c &= \hat{I}_p \sin(\omega_1 t + \frac{2\pi}{3} + \phi_1) + \hat{I}_n \sin(\omega_1 t - \frac{2\pi}{3} + \phi_n) + \hat{I}_z \sin(\omega_1 t + \phi_z) \end{aligned} \quad (3.29)$$

$$\begin{aligned} i_d &= \hat{I}_p \cos(\phi_1) - \hat{I}_n \cos(2\omega_1 + \phi_n) \\ i_q &= \hat{I}_p \sin(\phi_1) + \hat{I}_n \sin(2\omega_1 + \phi_n) \\ i_0 &= \hat{I}_z \sin(\omega_1 t + \phi_z) \end{aligned} \quad (3.30)$$

The performance of SRF method is directly depended on phase angle information. Phase angle information should be obtained by PLL methods. Harmonics, unbalance and noise in three phase signals can affect the accuracy of phase angle information obtained by PLL methods. Thus, the necessary attention must be given in the selection of PLL methods for the performance of SRF method.

Harmonic Current Extraction using Synchronous Fundamental Reference Frame

The block diagram of harmonic current extraction using synchronous fundamental reference frame is demonstrated in Figure 3.13. The fundamental current components become into dc d and q quantities and harmonic current components become into ac d and q quantities when the three phase currents consisting harmonics are transformed into dq reference frame with rotating dq frame by the fundamental phase information θ. The ac components can be decoupled from dc component with using high pass filter. However high pass filter may cause large phase angle error in

ac components so reference currents will not in phase with actual harmonic currents. In order to solve this problem, high pass filter can be applied with decoupling dc component with low pass filter and extracting dc component from non-filtered signal to get ac component. The dc component output of low pass filter has no phase shift so, this method does not cause phase shift problem on ac harmonic components (Asiminoaei et al., 2007). After ac d and q components are separated, they can be converted into three phase signals by applying inverse transformation so that harmonic currents are extracted.

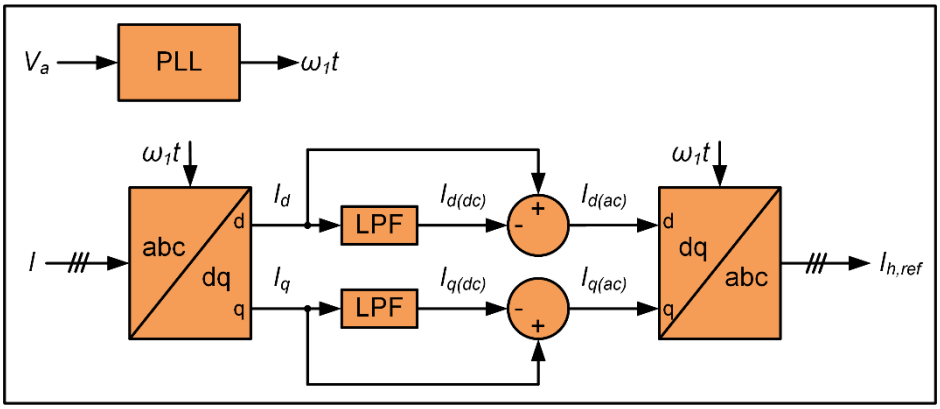


Figure 3.13. Harmonic current extraction with synchronous fundamental reference frame

Harmonic Current Extraction using Synchronous Individual Harmonic Reference Frame

The individual harmonics can be extracted using SRF method with rotating dq reference frame in the angular frequency of harmonic components. If the dq reference frame is rotated with the angular frequency of a harmonic component by considering the rotation direction of harmonic components, this harmonic component becomes dc d and q quantities and, the fundamental and other harmonic components become ac quantities. Therefore, the required dc harmonic component can be decoupled from ac components with using low pass filters without any phase and gain errors. Finally dc component can be transformed into three phase signals with inverse transformation.

The block diagram of individual harmonic current extraction using SRF is demonstrated in Figure 3.14 for 5th and 7th harmonics. In most of general conditions, 5th harmonics are negative sequence and 7th harmonics are positive sequence. Therefore, the dq reference frame is rotating with the angular frequency of $-5\omega_1$ for 5th harmonics and $7\omega_1$ for 7th harmonics, in order to convert 5th and 7th harmonics to dc components in dq frame. These dc components are extracted with low pass filters and transformed into three phase signals with inverse transformations.

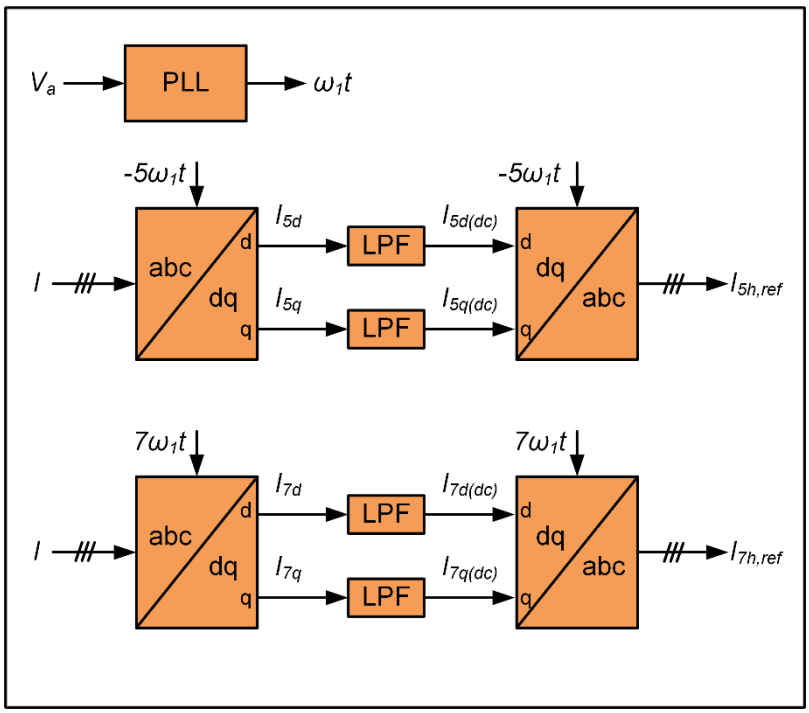


Figure 3.14. Harmonic current extraction using synchronous individual harmonic reference frame

3.2.3.2. DC Link Voltage Controller

The dc link capacitors are used as energy storage device in the shunt compensators. The shunt compensators eliminate harmonics and/or other power quality problems by supplying reactive energy to dc link and/or consuming reactive energy from dc link so, additional dc supply is not required. The only active power requirement of the compensator is for losses of its power circuit. The various dc link

voltage control methods are applied to the shunt compensators in literature. These controller methods are Proportional-Integral (PI), Fuzzy Logic, Artificial Neural Network controller, Adaptive Controllers and etc. PI based dc link control method shows sufficient performance in many applications. The block diagram of PI based dc link voltage control is presented in Figure 3.15.

In dc link controller, the measured dc link voltage is subtracted from dc link reference voltage and error between reference and actual dc link voltage is obtained. This error signal is applied to controller and the control signal is taken from output of controller. This control signal can be used as a current component, voltage component and/or active power component according to the control strategy.

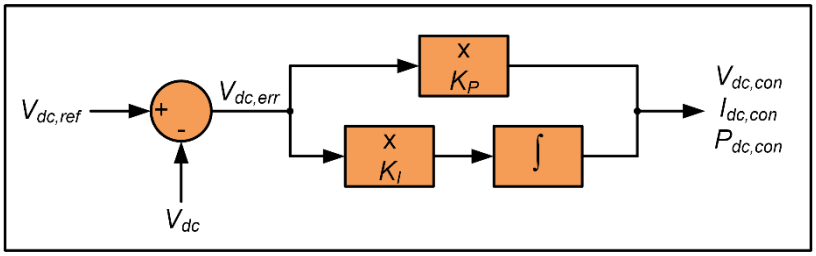


Figure 3.15. PI based dc link voltage control

3.2.3.3. Current Controller

Even though the performance and accuracy of reference generation methods have significant importance on the performance of the shunt compensators, the current controller which is responsible for generating currents in a desired waveform to provide effective compensation is the backbone of the shunt compensators. According to the feedback loop, two different current control scheme named as direct current control (DCC) and indirect current control (ICC) can be applied to the controller of shunt compensators.

In DCC scheme, the reference signals are generated for the injected current of shunt compensator in order to compensate target disturbance variables such as, harmonics, reactive power, unbalance etc. The injected current of shunt compensator is used to provide feedback loop for current control. The simplified block diagram of DCC scheme is demonstrated in Figure 3.16(a). The injected current of compensator

is subtracted from the reference current to obtain an error signal. The error signal is applied as input to the current controller. Then, the current controller generates control signal for generating the switching signals. DCC control scheme provides a feedforward control in terms of the compensation strategy.

In ICC scheme, the generated reference signals are the desired waveforms or values of target compensated variables such as supply voltages, supply currents and supply reactive power. The target compensated variables are used as feedback signal in this control scheme. The simplified block diagram of ICC scheme is demonstrated in Figure 3.16(b). The compensated variable is subtracted from reference signal and to obtain an error signal. The error signal is applied as input to the current controller for the generation of control signal. The control signal is applied to gate signal generation block to generate switching signals. The output voltage and current of compensator are not used in ICC control loop so it is not required to measure these signals. ICC scheme provides a feedback control in terms of the compensation strategy.

In both direct and indirect current control methods, various current controllers are investigated in literature. These are proportional controller, proportional – integral controller, proportional resonant controller, fuzzy controller, artificial neutral network based controller and etc.

3.2.3.4. Gate Signal Generation Methods

Gate signal generation which is also accepted as a part of current controller is responsible for the generation of gate signals of power electronic semiconductors to provide the generation of required compensation currents accurately. A large variety of gate signal generation methods have been introduced for VSCs in literature. Hysteresis pulse width modulation (PWM), carrier based PWM and space vector PWM (SVPWM) methods are the most common gate signal generation methods for the VSC based shunt compensators.

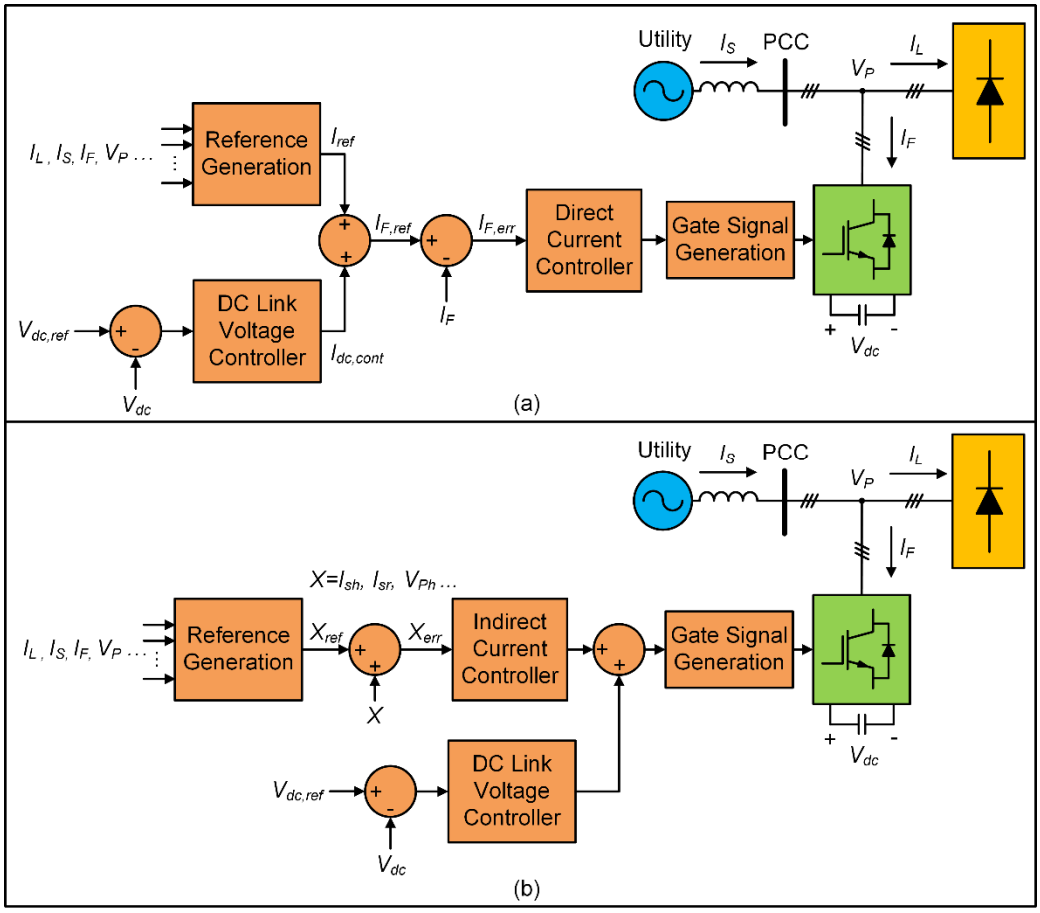


Figure 3.16. Generalized block diagram of current control methods
(a) Direct current control method (b) Indirect current control method

Hysteresis PWM method also named as hysteresis current controller is a type of ON-OFF current controllers. The main operating principle of this method is to keep error signal between reference and feedback signals in certain levels with using hysteresis band. The block diagram of hysteresis PWM method for three phase VSC is shown in Figure 3.17. The operating principles of hysteresis PWM method for one phase of three phase bridge VSC is demonstrated by the waveforms in Figure 3.18. If the error signal reaches to the upper limit of heresies band, the upper switch is turned off and the lower switch is turned on. If the error signal reaches to the lower limit of heresies band, the upper switch is turned on and the lower switch is turned off. If the error signal remains in the hysteresis band, the positions of switches are preserved. Hysteresis PWM method is easy to implement and presents excellent dynamic performance. However, the switching frequency of this method does not remain

constant and varies along with the current waveform. Moreover the switching frequency is dependent to hysteresis band limits. When the limits are decreased, the switching frequency is increased and vice versa. In order to obtain a sufficient waveform quality, the limits must be set under certain values. Especially switching frequency excessively increases in the low values of reference signals. This condition may result in excessive heat generation of VSC (Holtz, 1992; Mohan and Undeland, 2007; Özkaya, 2007).

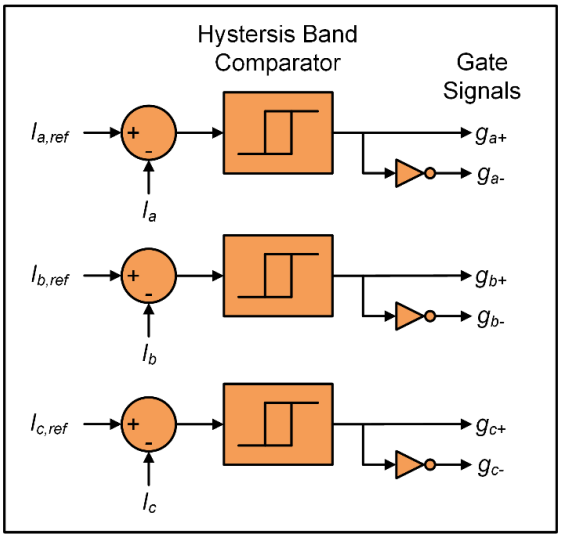


Figure 3.17. Block diagram of Hysteresis PWM method for three phase VSC

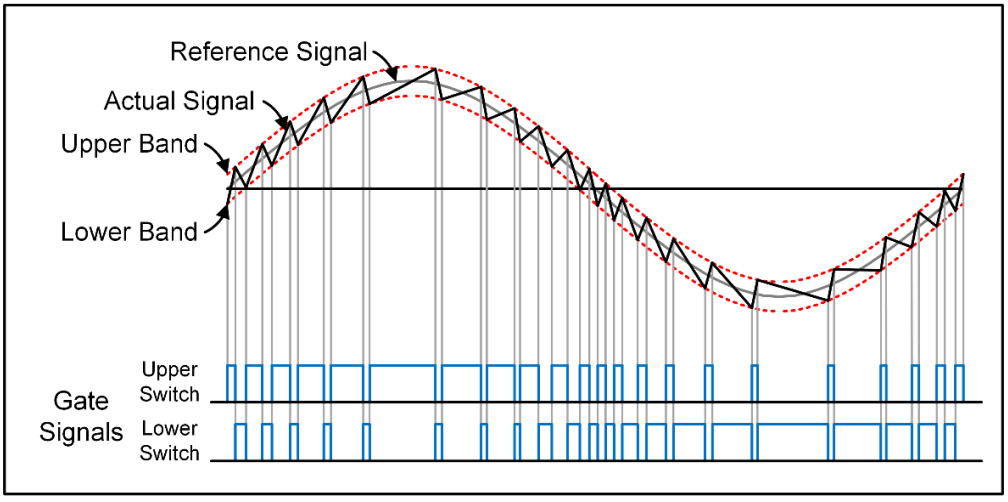


Figure 3.18. Operating principle waveforms of Hysteresis PWM

The carrier based PWM is the most widely used gate signal generation method in the controller of shunt compensators. The major advantage is to have a fixed switching frequency. In the carrier based PWM, the control signal is modulated with carrier signal in order to generate the switching signals of power semiconductors. The carrier signal can be selected as a saw-tooth or a triangular wave. Triangular waveform is generally used in VSC based applications due to the providing high quality output waveform. The switching frequency is the same with the frequency of carrier signal. The block diagram of carrier based PWM method is shown in Figure 3.19 for one leg of VSC. The output voltage/current of VSC is controlled by the duration of switching states of power semiconductors. The duration of switching state is determined by comparing the magnitudes of control signal and carrier signals as shown in Figure 3.20. The gate signals change their states in the intersection of reference and carrier signals (Holtz, 1994; Hava et al., 1998).

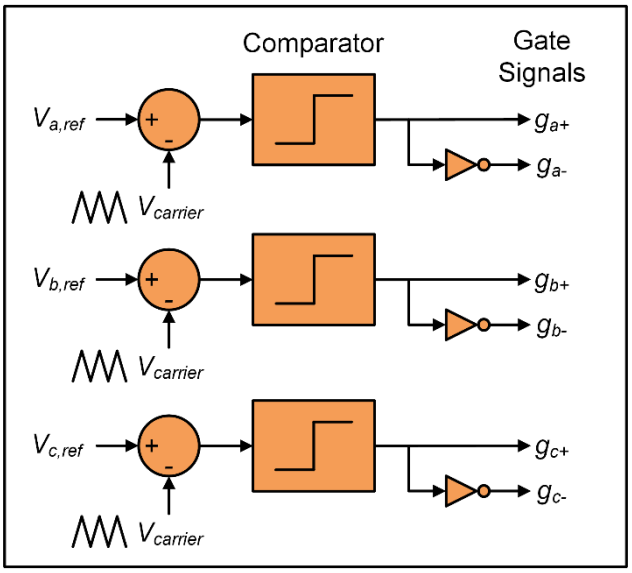


Figure 3.19. Block diagram of Carrier Based PWM method for three phase VSC

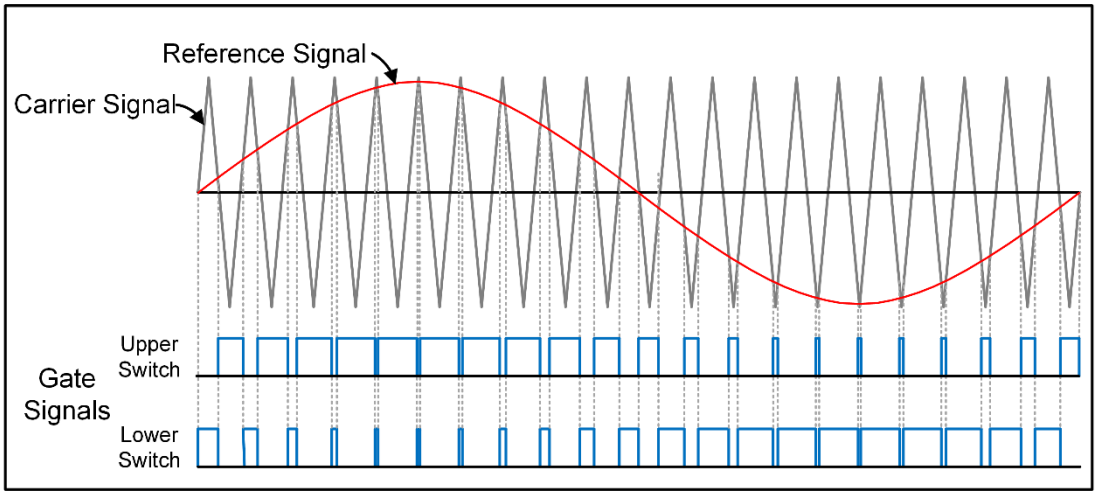


Figure 3.20. Operating principle waveforms of Carrier Based PWM

SVPWM is based on the mathematical calculation of switching periods of each switch in VSC according to the magnitude and the angle of reference vector in each sampling time. SVPWM has significant advantages in dc link voltage utilization and output waveform quality (van der Broeck et al., 1988; Keliang and Danwei, 2002). In the scope of this thesis work, SVPWM is used for gate signal generation in the proposed controller of SHAPF. This method is introduced in the following section comprehensively.

SVPWM Method:

SVPWM uses state space vectors to create switching signals so the reference voltage in abc frame should be converted a normalized reference space vector in αβ reference frame. This reference vector is used for determining the switching sequence vectors of VSC and their operation periods to generate reference voltage at the output of VSC (Holtz, 1994; Pinheiro et al., 2002). The power circuit topology of three phase three leg bridge VSC is given in Figure 3.21. In this VSC topology, there are 8 possible switching patterns except on and off states of switches on the same leg at the same time. These 8 switching pattern forms 8 switching vectors in αβ reference frame. These switching vectors and normalized output voltages in abc and αβ frames are given in

Table 3.1. The switching state vectors in αβ coordinates forms 6 regions which is named as sector as demonstrated in Figure 3.22.

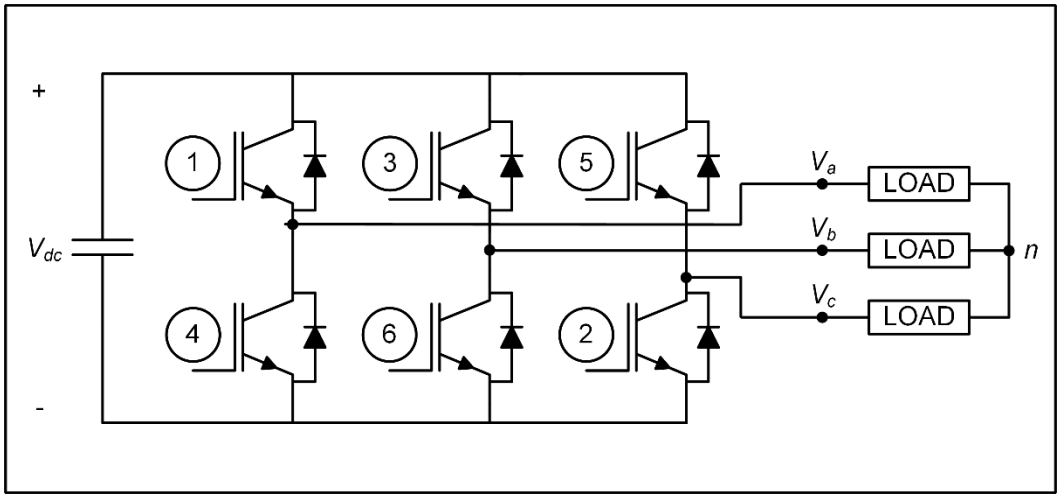


Figure 3.21. Power circuit diagram of three phase three leg bridge VSC

Table 3.1. Switching states of three phase VSC

Vectors	Switching States			Normalized Output Phase Voltages $V_{x,n}=V_x/V_{dc}$			Normalized Output Line Voltages $V_{xy,n}=V_{xy}/V_{dc}$			Normalized αβ0 Voltages $V_{x,n}=V_x/V_{dc}$	
	S_1	S_3	S_5	$V_{a,n}$	$V_{b,n}$	$V_{c,n}$	$V_{ab,n}$	$V_{bc,n}$	$V_{ca,n}$	$V_{\alpha,n}$	$V_{\beta,n}$
V_0	0	0	0	0	0	0	0	0	0	0	0
V_1	1	0	0	2/3	-1/3	-1/3	1	0	-1	2/3	0
V_2	1	1	0	1/3	1/3	-2/3	0	1	-1	1/3	$1/\sqrt{3}$
V_3	0	1	0	-1/3	2/3	-1/3	-1	1	0	-1/3	$1/\sqrt{3}$
V_4	0	1	1	-2/3	1/3	1/3	-1	0	1	-2/3	0
V_5	0	0	1	-1/3	-1/3	2/3	0	-1	1	-1/3	$-1/\sqrt{3}$
V_6	1	0	1	1/3	-2/3	1/3	1	-1	0	1/3	$-1/\sqrt{3}$
V_7	1	1	1	0	0	0	0	0	0	0	0

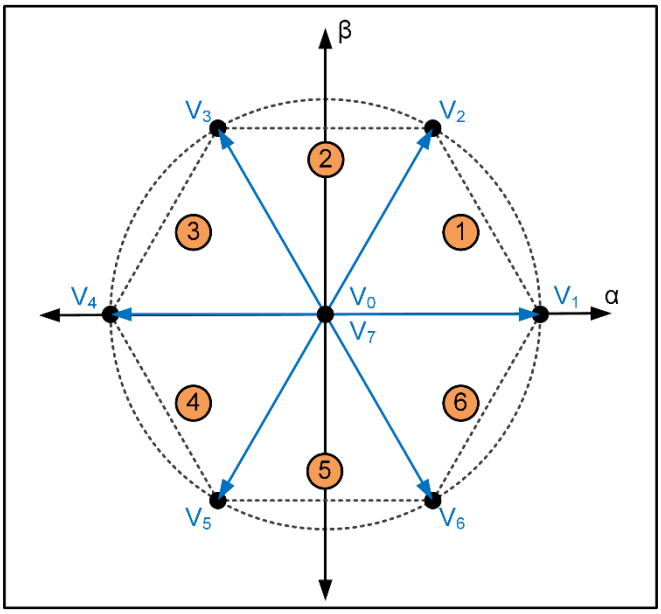


Figure 3.22. Switching state vectors in αβ coordinates

SVPWM method is performed with 3 main steps;

Step 1:

In the first step, the reference voltages in abc frame are transformed to reference voltages in αβ frame with Eq. 3.31. These reference voltages in αβ frame is normalized according to dc link voltage with Eq. 3.32. The rotation angle of reference space vector, θ are calculated with Eq. 3.33.

$$\begin{bmatrix} V_{\alpha,ref} \\ V_{\beta,ref} \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{\sqrt{3}}{3} & -\frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} V_{a,ref} \\ V_{b,ref} \\ V_{c,ref} \end{bmatrix} \tag{3.31}$$

$$\begin{aligned} V_{\alpha,norm} &= \frac{V_{\alpha,ref}}{V_{dc}} \\ V_{\beta,norm} &= \frac{V_{\beta,ref}}{V_{dc}} \end{aligned} \tag{3.32}$$

$$\theta = \tan^{-1}\frac{V_\beta}{V_\alpha} \tag{3.33}$$

Step 2:

In the second step, the sector in which the reference space vector exists is firstly determined with using the rotation angle of reference vector, θ. Then, the operation period of each switching state vector in this sector is calculated in order to create reference voltage at the output of inverter during one sampling period. The operation period calculations of switching state vectors in Sector 1 is given in Eqs. 34-38. The calculations of other sectors are given in Appendix B.

$$T_s V_{ref,norm} = T_1 V_1 + T_2 V_2 + T_0 V_0 + T_7 V_7 \tag{3.34}$$

$$T_s \begin{bmatrix} V_{\alpha,norm} \\ V_{\beta,norm} \end{bmatrix} = T_1 \begin{bmatrix} 2/3 \\ 0 \end{bmatrix} + T_2 \begin{bmatrix} 1/3 \\ 1/\sqrt{3} \end{bmatrix} + T_0 \begin{bmatrix} 0 \\ 0 \end{bmatrix} + T_7 \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{3.35}$$

$$T_1 = \frac{3}{2} T_s V_{\alpha,norm} - \frac{\sqrt{3}}{2} T_s V_{\beta,norm} \tag{3.36}$$

$$T_2 = \sqrt{3} T_s V_{\beta,norm} \tag{3.37}$$

$$T_0 = T_7 = \frac{T_s - T_1 - T_2}{2} \tag{3.38}$$

Step 3:

In the third step, the switching signals of each switch are generated according to the switching periods and the switching sequences. The switching sequence directly effects the quality of output voltage and the switching frequency of VSC (Pinheiro et al., 2002). The symmetrical switching sequence is the one most preferred method because of the low harmonic distortion of output voltage (Neacsu, 2001; Kumar et al.,

2010) The symmetrical switching sequence of three phase three leg VSC is presented for each sector in Table 3.2. The pulse pattern of symmetrical switching sequence is illustrated for Sector 1 in Figure 3.23. The pulse patterns of all sectors are presented in Appendix B.

Table 3.2. Symmetrical switching sequence of three phase three leg VSC

Sector 1	V_0 - V_1 - V_2 - V_7 - V_7 - V_2 - V_1 - V_0
Sector 2	V_0 - V_3 - V_2 - V_7 - V_7 - V_2 - V_3 - V_0
Sector 3	V_0 - V_3 - V_4 - V_7 - V_7 - V_4 - V_3 - V_0
Sector 4	V_0 - V_5 - V_4 - V_7 - V_7 - V_4 - V_5 - V_0
Sector 5	V_0 - V_5 - V_6 - V_7 - V_7 - V_6 - V_5 - V_0
Sector 6	V_0 - V_1 - V_6 - V_7 - V_7 - V_6 - V_1 - V_0

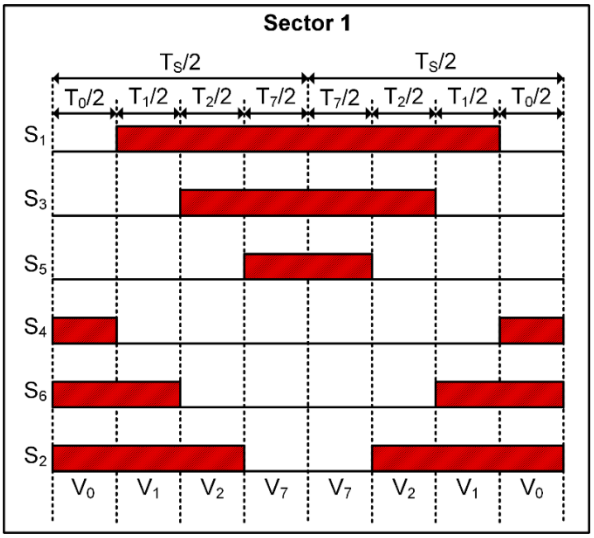


Figure 3.23. Pulse pattern of symmetrical switching sequence for Sector 1

3.3. Conventional Controller Methods of SHAPF

SHAPF is firstly proposed with the supply side harmonic detection based feedback controller by Fujita and Akagi (1991). This feedback controller approach is accepted in the following studies as a conventional controller method for SHAPF. The block diagram of the supply side harmonic detection based feedback controller by Fujita and Akagi (1991) is introduced in Figure 3.24. In this early study, the PQ theory is used for the harmonic extraction method. The supply current harmonics are

extracted with calculating the instantaneous active power, p and the instantaneous reactive power, q using the three phase supply voltage and current signals. The fundamental components of source currents are transformed into dc power quantities, $\bar{p}$ and $\bar{q}$. The harmonic components of the source currents are transformed into ac power quantities $\tilde{p}$ and $\tilde{q}$. The ac power components are separated using first order high pass filters.

In dc link controller, the measured dc link voltage is subtracted from dc link reference voltage to obtain the error signal. The error signal is applied to controller to generate control signal. This control signal is added to the ac reactive power component, $\tilde{q}$. If VSC part of SHAPF generates a fundamental output voltage in phase with the fundamental leading current of PF, the active power flow is achieved. This active power flow generated by the fundamental voltage in phase with PF current can supply the dc link capacitor. Thus, the dc link control of SHAPF is achieved with the reactive power component instead of the active power component (Fujita and Akagi, 1991; Srianthumrong and Akagi, 2003).

The ac power quantities with the dc link control signal are transformed into three phase current references using the inverse calculation of PQ theory. These reference currents are multiplied with the proportional feedback gain, K to generate the voltage reference to PWM method.

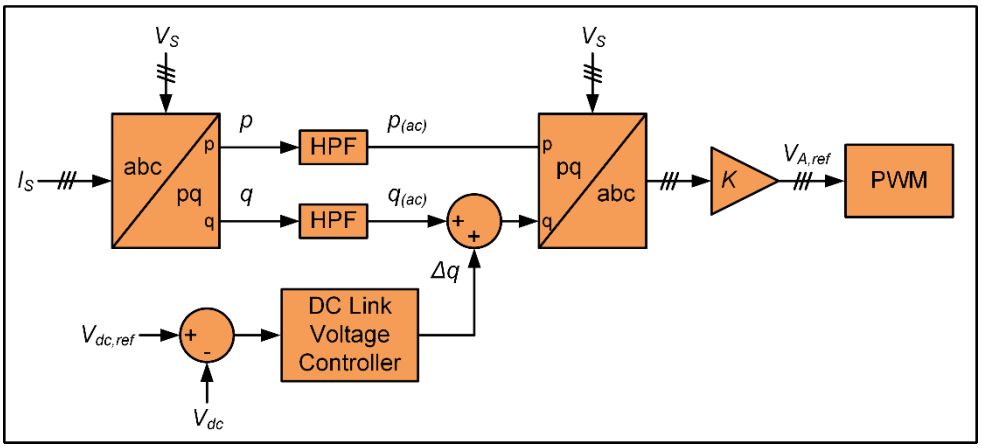


Figure 3.24. Block diagram of conventional feedback controller

In the further studies, the cut-off frequency of PF is selected to 7th harmonic frequency in order to compensate the high order current harmonics of three phase rectifiers with lower dc link voltage and smaller PF reactor than the SHAPF whose PF is tuned to 5th harmonic frequency (Srianthumrong and Akagi, 2003; Akagi, 2005; Wiroj et al., 2007; Akagi and Hatada, 2009). However, this configuration of PF reduce the performance of SHAPF in the compensation of 5th current harmonics which is the most dominant harmonic of the three phase rectifiers. In order to solve this problem, the feedback + 5th harmonic feedforward controller shown in Figure 3.25 is introduced by Srianthumrong and Akagi (2003). In this controller, a feedforward loop is added to the conventional feedback controller in order to improve the filtering performance of SHAPF in the 5th current harmonic. SRF method is preferred for the extraction of current harmonics. The feedback controller uses the synchronous fundamental reference frame for the extraction of current harmonics. The feedforward controller uses the synchronous individual harmonic reference frame for the extraction of 5th current harmonics. In the harmonic extraction methods, first order high pass and low pass filters are used.

The main idea of the feedforward controller is to make PF absorb all amount of the 5th harmonic current by generating the required compensation voltage at the terminals of VSC (Srianthumrong and Akagi, 2003). In order to achieve this objective, the 5th current harmonics are extracted using the load current. The required compensation voltage of the 5th current harmonic is calculated using the 5th load current harmonic and the impedance of PF in 5th harmonic frequency.

The impedance of PF on the dq frame which is rotating in the fundamental angular frequency, ω_1 and in the 5th harmonic angular frequency are given in Eqs. 3.39 and 3.40 as (Srianthumrong and Akagi, 2003);

$$Z_F(s) = R_F + sL_F + \frac{1}{sC_F} \tag{3.39}$$

$$Z_{F_{dq5}}(s) = R_F + \left(s + j\omega_5\right)L_F + \frac{1}{\left(s + j\omega_5\right)C_F} \tag{3.40}$$

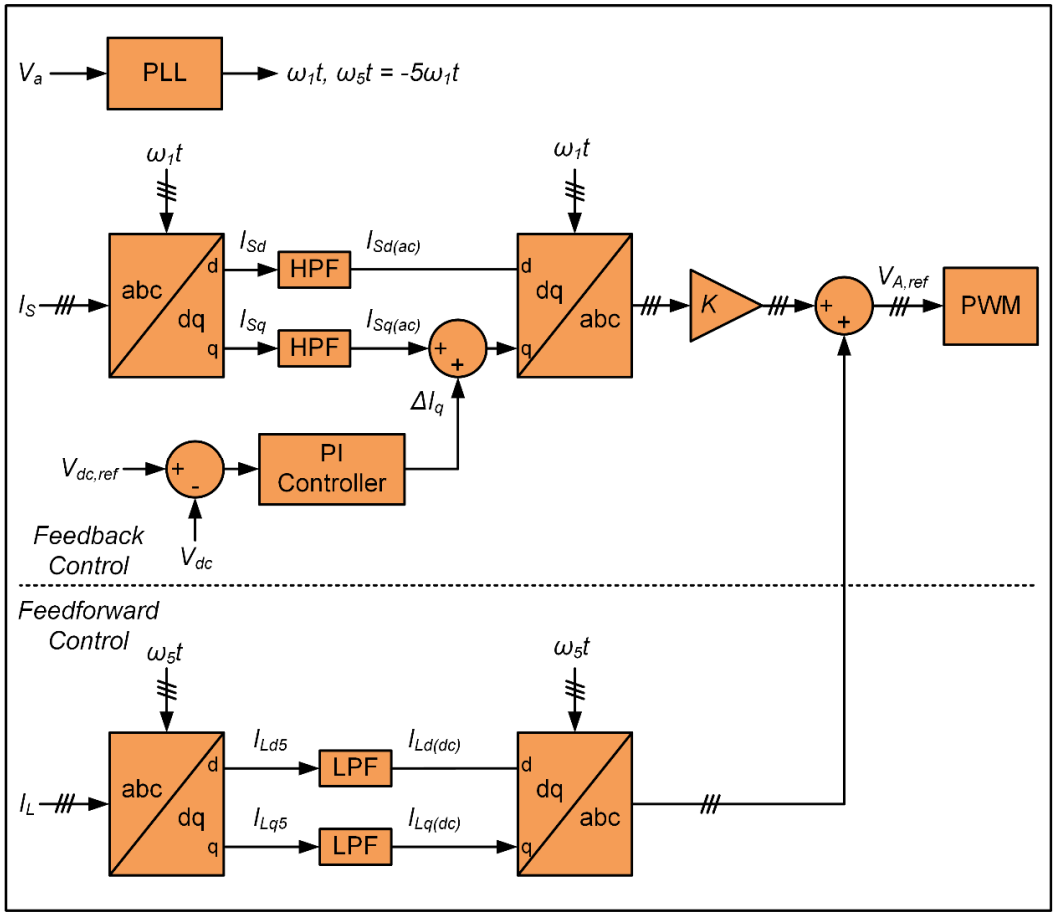


Figure 3.25. Block diagram of feedback + 5th harmonic feedforward controller

For the steady state condition, the impedance of PF is equal to as (Srianthumrong and Akagi, 2003);

$$Z_{F_{dq5}}(0) = R_F + j\omega_5 L_F + \frac{1}{j\omega_5 C_F} \tag{3.41}$$

The d and q components of the required compensation voltage for the 5th current harmonic is calculated with Eqs. 3.42 and 3.43 as (Srianthumrong and Akagi, 2003);

$$V^*_{dq5} = \left(R_F + j\left(\omega_5 L_F - \frac{1}{\omega_5 C_F} \right) \right) \bar{i}_{L_{dq5}} \tag{3.42}$$

$$\begin{bmatrix} V_{d5}^{*} \\ V_{q5}^{*} \end{bmatrix} = \begin{bmatrix} R_F & -\omega_5 L_F + \dfrac{1}{\omega_5 C_F} \\ \omega_5 L_F - \dfrac{1}{\omega_5 C_F} & R_F \end{bmatrix} \begin{bmatrix} \bar{i}_{L_{d5}} \\ \bar{i}_{L_{q5}} \end{bmatrix} \tag{3.43}$$

The filtering characteristic SHAPF with the conventional feedback controller and the feedback plus 5th harmonic feedforward controller are given in Eqs. 3.44 and 3.45, respectively (Srianthumrong and Akagi, 2003).

$$\frac{I_{Sh}(s)}{I_{Lh}(s)} = \frac{Z_F(s)}{Z_S(s) + Z_F(s) + KD_{FB}(s)} \tag{3.44}$$

$$\frac{I_{Sh}(s)}{I_{Lh}(s)} = \frac{Z_F(s) - Z_{F_{dq5}}(s) D_{FF}(s)}{Z_S(s) + Z_F(s) + KD_{FB}(s)} \tag{3.45}$$

where

$$D_{FB} = \frac{s - j\omega_1}{s - j\omega_1 + \omega_c} \tag{3.46}$$

$$D_{FF} = \frac{\omega_c}{s - j\omega_5 + \omega_c} \tag{3.47}$$

D_{FB} is the transfer function of the harmonic extraction method in the feedback control and D_{FF} is the transfer function of the harmonic extraction method in the feedforward method. ω_c is the angular cutoff frequency of low pass or high pass filter in the harmonic extraction method. ω_1 is the fundamental angular frequency and ω_5 is the 5th harmonic angular harmonic frequency. Note that, ω_5 is equal to $-5\omega_1$ because 5th harmonic component is in negative sequence.

The positive and negative sequence filtering characteristic of SHAPF which has 7th harmonic tuned PF is demonstrated with the conventional feedback controller

and the feedback + 5th harmonic feedforward controller in Figure 3.26. As previously stated in Section 3.2.1.1, when the feedback gain, *K* is equal to zero, PF performs a limited filtering performance and causes harmonic amplification under its cut-off frequency. When *K* is larger than 0, SHAPF prevents the resonance phenomenon of PF shows an effective filtering characteristic around the cut-off frequency of PF. However, SHAPF cannot perform adequate filtering performance in the most dominant 5th harmonic frequency. Moreover, the filtering performance of the feedback controller is limited in the high frequency dominant harmonics. When the filtering characteristic of SHAPF with the feedback +5th harmonic feedforward controller is investigated, the feedback +5th harmonic feedforward controller shows the almost same positive sequence filtering characteristic with the conventional feedback controller but, the feedforward controller significantly improves the filtering characteristic of SHAPF in the 5th harmonic negative sequence component (Srianthumrong and Akagi, 2003; Wiroj et al., 2007).

The filtering performance of the conventional feedback controller is depending on the feedback gain, *K*. The increase of *K* increases the filtering performance of the feedback controller but, the excessive increase of *K* causes stability problems because of the delays in the controller and the phase errors in the measurement circuitries. Theoretically, the 5th harmonic current feedforward loop presents a significant filtering performance in the most dominant 5th current harmonic for SHAPF with PF tuned to 7th harmonic frequency. However, in practical situations, the delays in the controller, the phase errors of the measurements circuitries, the tolerance values of PF components and the voltage harmonics has considerable effect on the performance of the feedforward controller. The effect of the delays in the controller, the phase errors of the measurements circuitries and the tolerance values of PF components can be minimized with the preliminary measurements and the adjustments in the controller, but the effect of voltage harmonics can only be determined with a real time harmonic determination during the operation of SHAPF. However, the effect of voltage harmonics can be only prevented with the ability of the controller. The feedforward controller has not any ability to overcome the effect of voltage harmonics. The compensation performance of the feedback controller is affected severely even if the

voltage harmonics will exist in low magnitudes. The feedback control loop can theoretically show a successful suppression for the effect of the voltage harmonics with the increasing value of *K*. However, this performance of the feedback control loop is limited in practical applications because of the stability problems caused by the high values of *K*.

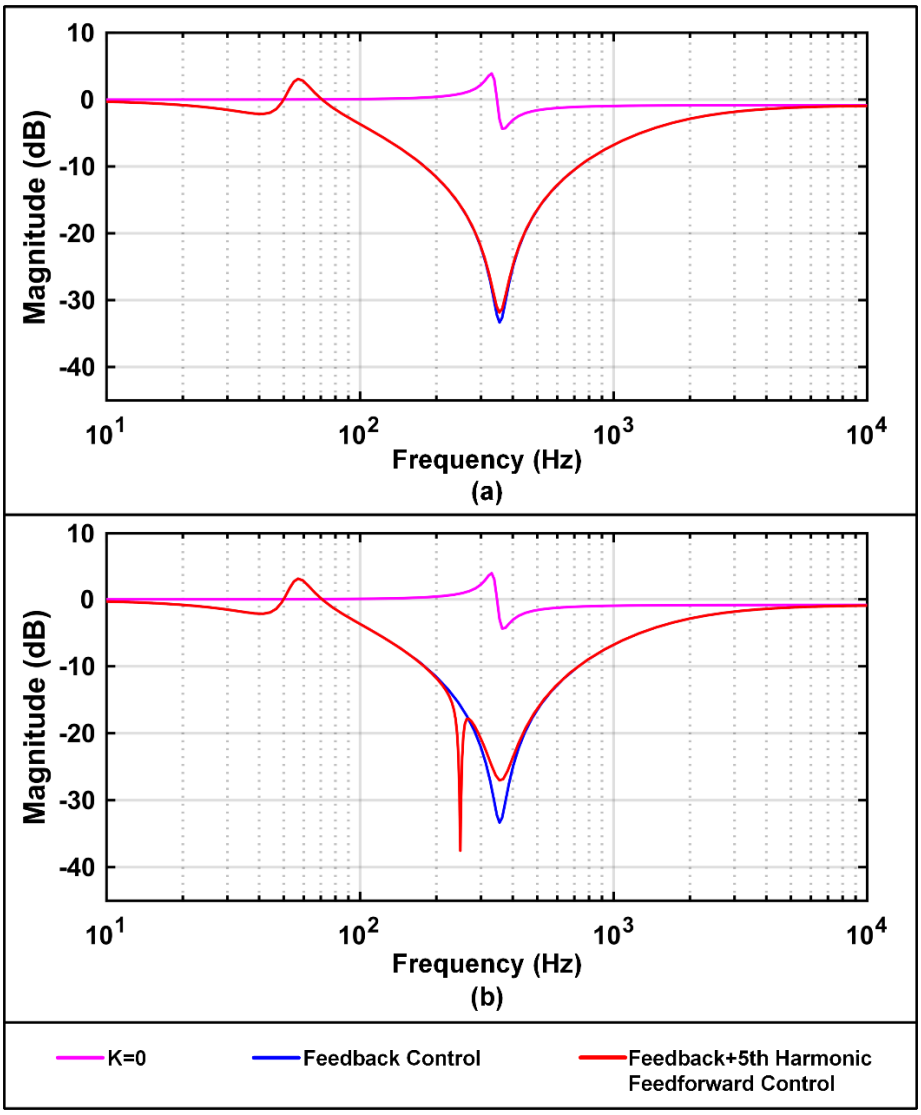


Figure 3.26. Filtering characteristic of conventional control methods
(a) Positive sequence filtering characteristic
(b) Negative sequence filtering characteristic

3.4. Proposed Control Method for Dynamic Harmonic and Reactive Power Compensation with Adaptive DC Link Voltage

The SRF based proposed control method of SHAPF can achieve the dynamic harmonic and reactive compensation with adaptive dc link voltage. The generalized block diagram of the proposed control method is shown in Figure 3.27. The proposed controller is formed from the harmonic compensation controller, the reactive power compensation controller, the adaptive dc link voltage reference calculation, the dc link voltage controller and SVPWM.

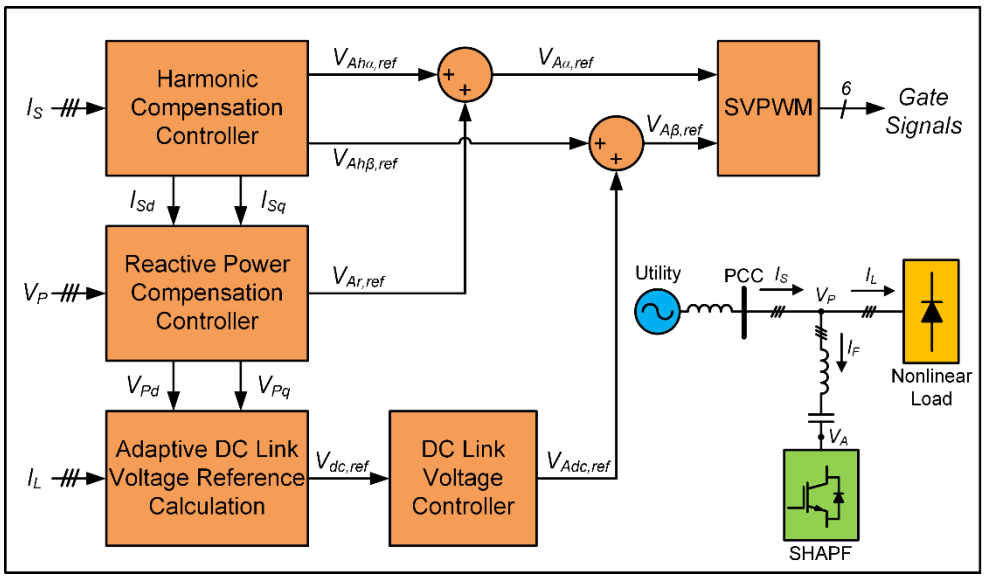


Figure 3.27. Generalized block diagram of proposed controller for SHAPF

In the harmonic compensation controller, a novel individual harmonic elimination based control method is applied for the compensation of harmonics for the effective harmonic compensation of three phase rectifiers. In the reactive power compensation controller, the supply side reactive power detection based feedback controller is realized. The adaptive dc link voltage reference calculation method calculates the dc link reference voltage of SHAPF according to the load reactive power and the load current harmonics levels. The dc link voltage controller sets the calculated dc link reference voltage on the dc link of SHAPF. Finally, SVPWM generates the gates signals for the VSC of SHAPF. In the proposed controller, SRF method is used

for the harmonic, reactive power and dc link reference and feedback signal calculations.

The main parts of the proposed controller are presented in the following sections in detail. SVPWM method is introduced in the previous section so that it is not mentioned again in this section.

3.4.1.1. Harmonic Compensation Controller

In the harmonic compensation controller of the proposed control method, a novel individual harmonic elimination based feedback control method is applied in order to increase the compensation performance of SHAPF. The detailed block diagram of individual harmonic elimination based control method is presented in Figure 3.28. In this control method, the conventional feedback controller is improved with the feedback loops which are applied for individual current harmonics with using PI controllers. The individual current harmonics are extracted up to 25th harmonics from the supply current with using synchronous individual harmonic reference frame. In the SRF based harmonic extraction methods, the first order low pass filters are used. The extracted d and q components of individual current harmonics are applied to PI controllers separately. The PI controllers generate the d and q components of the reference voltage required for the compensation of individual harmonics with Eqs. 3.48 and 3.49 as,

$$V_{Ahdn,ref} = K_{pn} I_{Sdn} + K_{in} I_{Sdn} \frac{1}{s} \tag{3.48}$$

$$V_{Ahqn,ref} = K_{pn} I_{Sqn} + K_{in} I_{Sqn} \frac{1}{s} \tag{3.49}$$

where $n = 6p \mp 1 \quad p = 1, 2, 3, 4$

The reference voltages in dq reference frame are transformed into αβ reference frame. Finally, the reference voltages for the compensation of individual current harmonics are summed with the reference voltage generated by the conventional feedback controller to generate the reference voltage for the compensation of current harmonics.

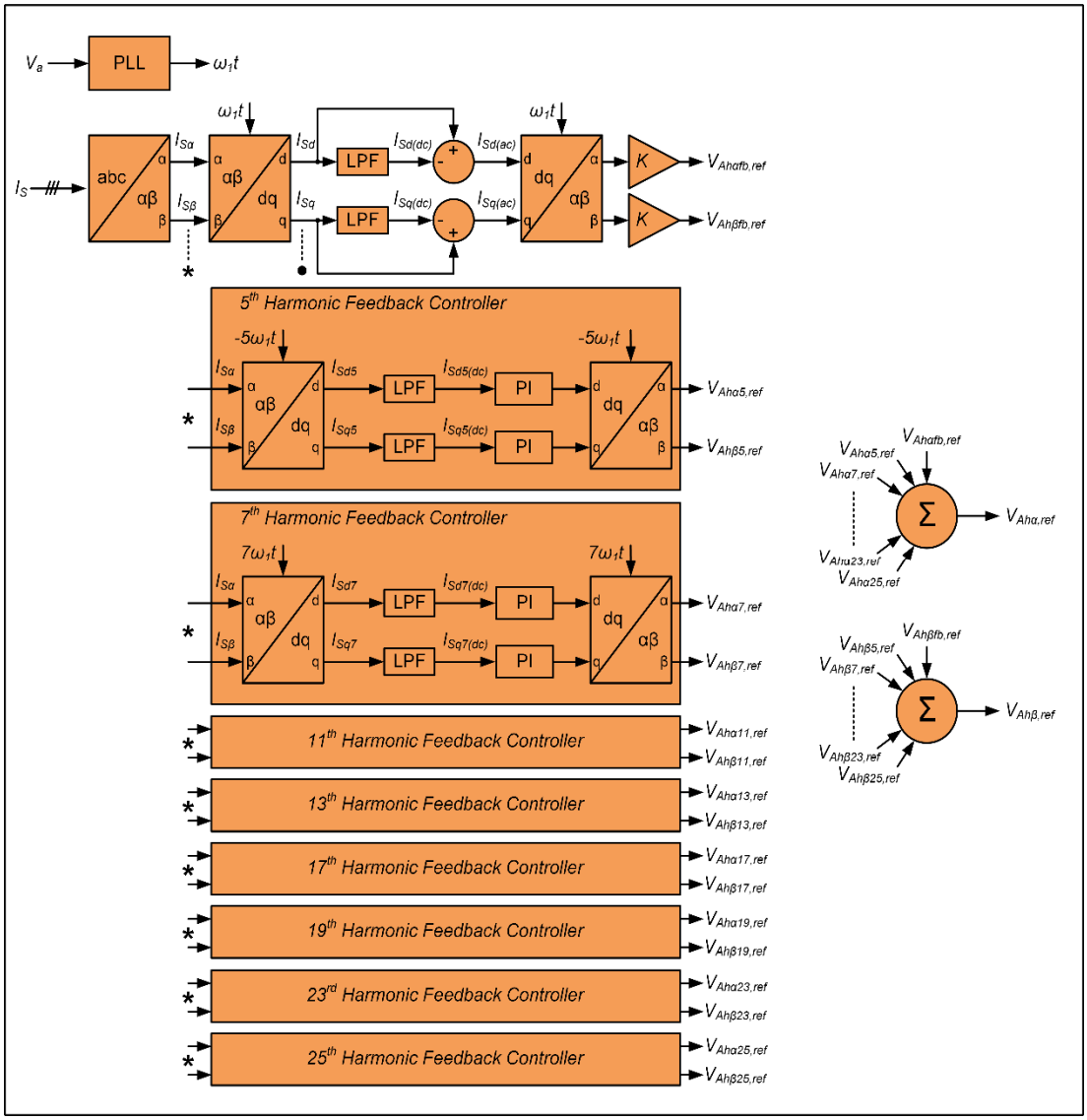


Figure 3.28. Block diagram of individual harmonic elimination based feedback controller

The filtering characteristic of SHAPF with the individual harmonic elimination based feedback controller can be analyzed with Eq. 3.50. D_{FB} is the transfer function of the harmonic extraction method in the conventional feedback control loop and it is given in Eq. 3.46. D_{IH} given in Eq. 3.51 is the transfer function of harmonic extraction method in the individual harmonic elimination feedback loops. Note that, ω_{6p-1} is equal to $-(6p-1)\omega_1$ because the harmonics in the angular frequency of ω_{6p-1} is in the negative sequence and ω_{6p+1} is equal to $(6p+1)\omega_1$ because the harmonics in the angular frequency of ω_{6p+1} is in the positive sequence.

$$\frac{I_{Sh}(s)}{I_{Lh}(s)} = \frac{Z_F(s)}{Z_S(s) + Z_F(s) + KD_{FB}(s) + \sum_{p=1}^{4}\left[\left(K_{pdn} + \frac{K_{idn}}{s} + j\left(K_{pq(6p\pm1)} + \frac{K_{iqn}}{s}\right)\right)D_{IHn}(s)\right]} \tag{3.50}$$

where

$$D_{IHn}(s) = \frac{\omega_c}{s - j\omega_n + \omega_c} \tag{3.51}$$

$$n = 6p \mp 1 \quad p = 1,2,3,4$$

The positive and negative sequence filtering characteristic of SHAPF which has 7th harmonic tuned PF is demonstrated with the individual harmonic elimination based feedback controller in Figure 3.26. The proposed harmonic compensation method shows an excellent filtering performance in the positive and negative individual harmonics compared to the conventional feedback harmonic controller. The proposed harmonic controller has almost the same effective filtering range in the positive sequence with the conventional feedback controller but the effective filtering range of the proposed controller in the negative sequence is narrower than the conventional feedback control method. However, this filtering characteristic of the proposed harmonic controller does not affect the performance of SHAPF in the compensation of the characteristic harmonics of the three phase rectifiers.

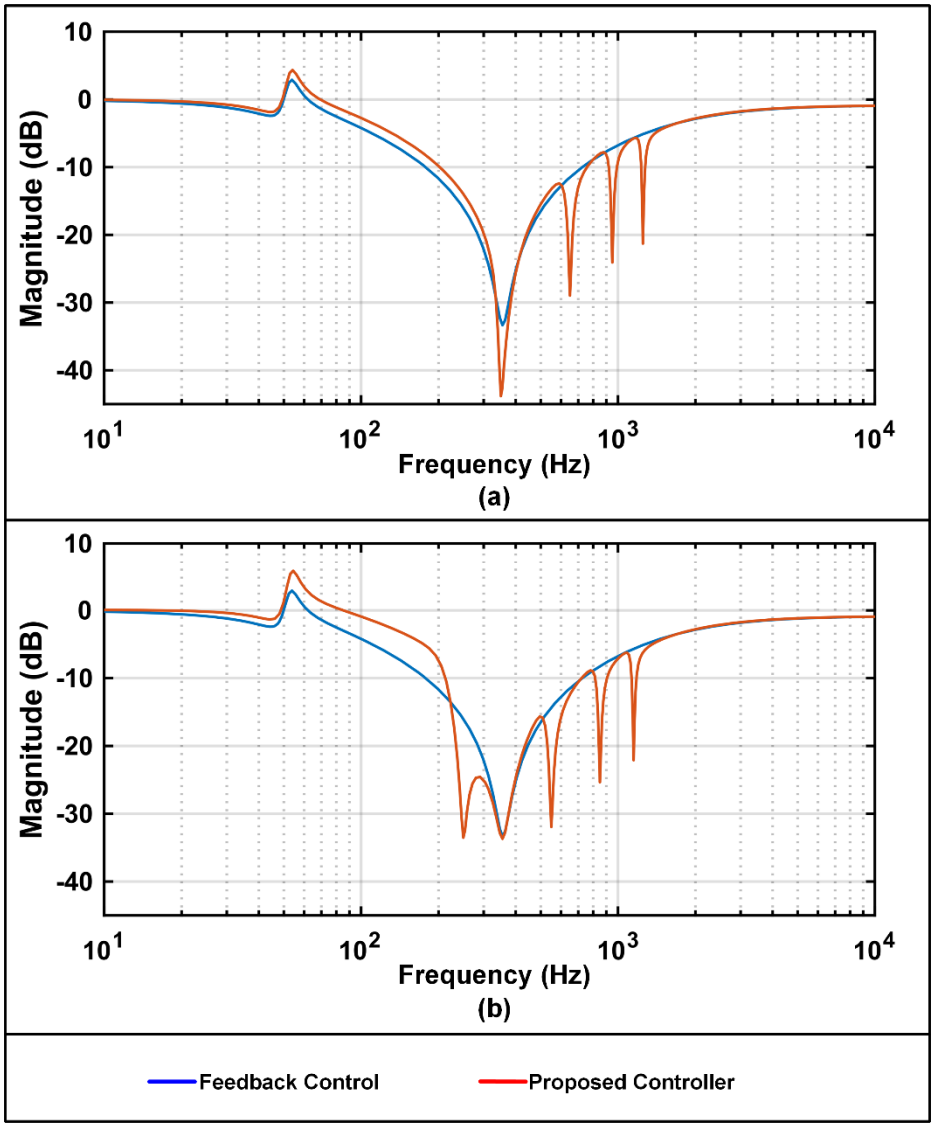


Figure 3.29. Filtering characteristic of individual harmonic elimination based feedback controller
(a) Positive sequence filtering characteristic
(b) Negative sequence filtering characteristic

Although the proposed harmonic controller shown an effective compensation characteristic in the individual current harmonics, the same filtering characteristic can be also achieved theoretically with the feedback plus feedforward controllers. However, the proposed controller shows its influence in the existence of the disturbances such as the delays in the controller, the phase errors in the measurements circuitry, the tolerance values of PF components and the voltage harmonics. The effect of these disturbances on the conventional feedback and the feedback + feedforward

controllers are discussed in the previous section. In the proposed controller, the effect of these disturbances can be effectively suppressed with the help of PI controllers used in each d and q components of the individual harmonics.

3.4.1.2. Reactive Power Compensation Controller

The dynamic reactive power compensation of SHAPF is performed with the supply side reactive power feedback control approach. In this control approach, the reactive power is determined with the supply side measurements and a voltage reference signal is generated with the indirect control scheme for the compensation reactive power. SHAPF achieves the reactive power flow by injecting currents 90° phase shift with phase voltages as defined in Section 3.4.1.2.

The block diagram of the reactive power compensation controller of the proposed control approach is presented in Figure 3.30. In this controller, the supply side instantaneous reactive power is calculated with using Eq. 3.52. The reactive power caused by the fundamental components of supply voltage and current transformed into dc power quantity, $q_{S(dc)}$ and the reactive power caused by the harmonics are transformed into ac power quantity, $q_{S(ac)}$. The ac reactive power component is in the responsibility of the harmonic compensation controller. The reactive power compensation controller is responsible from the elimination of the dc reactive power component.

$$q_S = q_{S(dc)} + q_{S(ac)} = \frac{3}{2}\left(V_{Pq} I_{Sd} - V_{Pd} I_{Sq}\right) \tag{3.52}$$

The dc reactive power component is extracted with using a first order low pass filter and applied to PI controller as an error signal in order to determine the magnitude of VSC output reference voltage for the compensation the reactive power in the dq domain. In order to achieve dynamic reactive power compensation, VSC of SHAPF must generate a fundamental frequency voltage which is in the same phase with grid

voltage. Therefore, voltage reference signal should be applied as d component into the dq to αβ transformation.

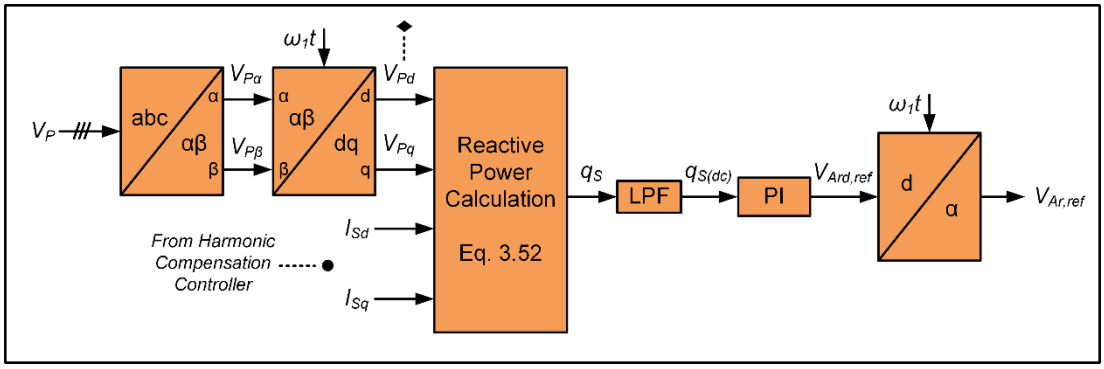


Figure 3.30. Reactive power compensation controller

3.4.1.3. Adaptive DC Link Voltage Reference Calculation

In order to decrease switching losses and maintain energy efficiency in SHAPF topology, the required dc link voltage can be calculated and set instantaneously according to the harmonic current level and the reactive power compensation requirements of the load. The block diagram of the adaptive dc link voltage calculation method is introduced in Figure 3.31.

In this calculation method, the load side instantaneous reactive power is calculated with using Eq. 3.53. The reactive power demand of the load caused by the fundamental components transformed into dc power quantity, $q_{L(dc)}$ and the reactive power caused by the harmonics are transformed into ac power quantity, $q_{L(ac)}$. The dc reactive power component is extracted with using a first order low pass filter.

$$q_L = q_{L(dc)} + q_{L(ac)} = \frac{3}{2}\left(V_{Pq} I_{Ld} - V_{Pd} I_{Lq}\right) \tag{3.53}$$

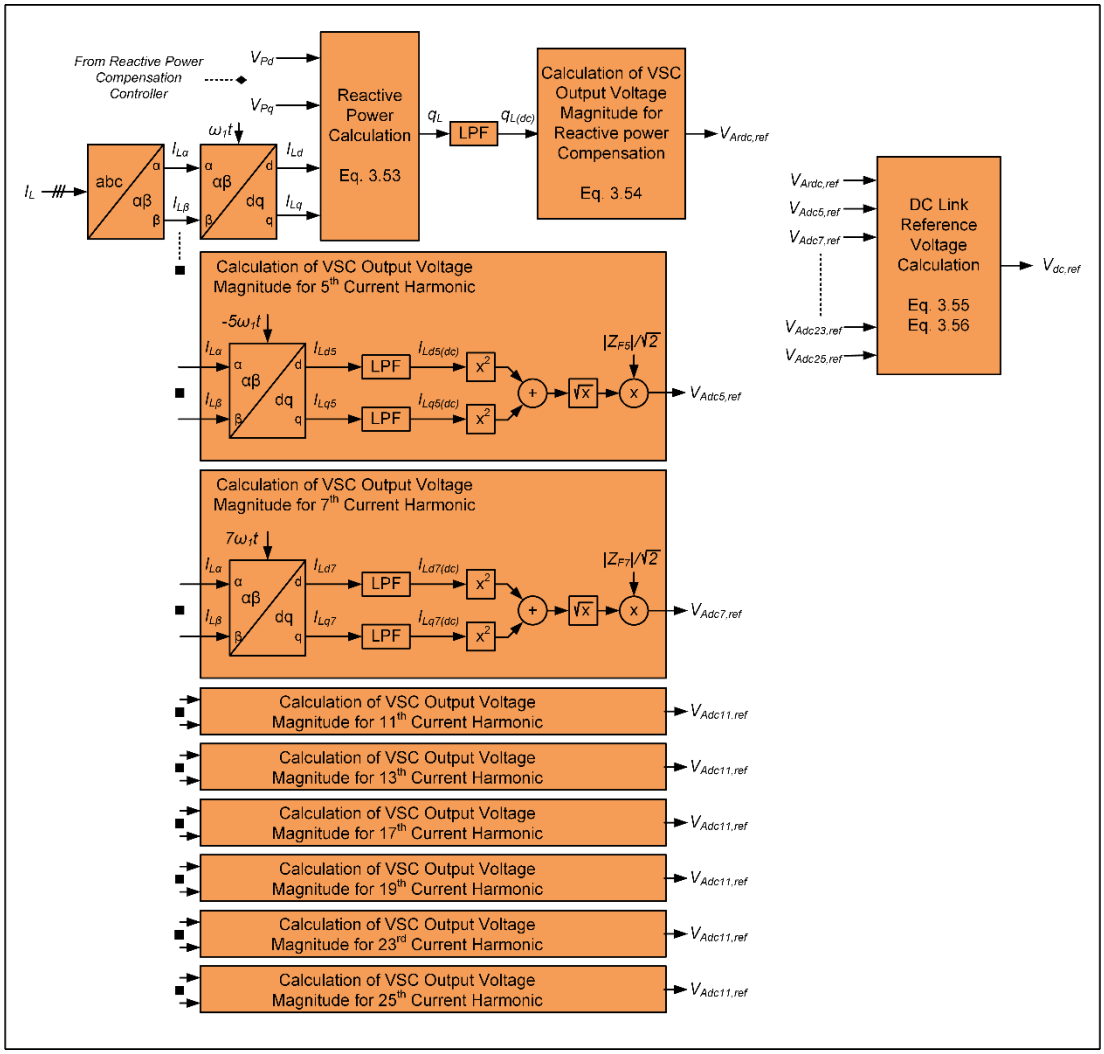


Figure 3.31. Block diagram of adaptive dc link voltage calculation method

The required output phase voltage for the dynamic reactive power compensation, V_{Ar} is calculated by Eq. 3.54 (Chi-Seng et al., 2012; Wai-Hei et al., 2013). In this equation, V_P gives the phase voltage at the PCC and X_{pf} gives the reactance of the passive filter.

$$V_{A_r} = V_P \left| 1 - \frac{q_{L(dc)} X_{pf}}{3V_P^2} \right| \tag{3.54}$$

The rms value of the required VSC output voltage for the compensation of each individual load current harmonic, V_{Ahn} can be calculated with using the rms value of

each load current harmonic and the PF impedance in each individual harmonic frequency. The dominant load current harmonics of the three phase rectifiers up to 25th harmonics are extracted with using synchronous individual harmonic reference frame method. The squares of each d and q components of load current harmonics are calculated and the magnitude of the load current harmonics are calculated. In order to calculate the rms value of VSC output voltage for the compensation of each current harmonics, the load current magnitude is divided by √2 and multiplied with the impedance of PF in the harmonic frequencies.

The VSC output voltage of SHAPF is given in Eq. 3.8 for the ideal harmonic compensation characteristic. With using Eq. 3.8, the minimum required rms value of VSC output phase voltage, V_{Amin} can be determined by Eq. 3.55 for the harmonic and reactive power compensation of SHAPF. In this equation, V_{Ar} gives the required output phase voltage for the reactive power compensation, V_{Ahn} gives the required output phase voltage for the compensation of each individual harmonic current and V_{Pm} is the supply voltage harmonic which should be generated by VSC to prevent the resonance conditions.

$$V_{A_{\min}} = \sqrt{V_{A_r}^2 + \sum_{n=6p\pm1} V_{A_{hn}}^2 + \sum_{m} V_{P_m}^2} \tag{3.55}$$

In order to determine the magnitude of supply voltage harmonics, additional harmonic extraction method should be applied. This situation causes the increase of the complexity and computational load of the controller algorithm. However, in the most of cases, the magnitude of the reference voltage for the current harmonics are quite higher than the supply voltage harmonics so the voltage harmonics can be neglected in Eq. 3.55. But conversely, if the voltage harmonics in the supply voltage reaches to significant levels, the certain voltage harmonic levels can be determined with the preliminary voltage harmonic measurements for the calculation of the rms value of VSC output voltage. In the controller of SHAPF prototype realized in the scope of this thesis work, the voltage harmonic are neglected in the rms value of VSC output voltage calculations.

Finally, the dc link reference voltage calculation can be performed using the rms value of VSC output voltage of SHAPF by Eq. 3.56. U_{PWM} is the utilization factor of PWM method for three phase three leg converter. Its value is $1/(2\sqrt{2})$ for Carrier based PWM method and $1/\sqrt{6}$ for SVPWM method. K_{dc} is the dc link increase factor which is related with the crest factor of the VSC output reference voltage of SHAPF.

$$V_{dc,ref} = K_{dc} \frac{1}{U_{PWM}} V_{A_{\min}} \tag{3.56}$$

In PWM methods, the output voltage of converter whose waveform is pure sinusoidal and crest factor is equal $\sqrt{2}$ is associated with the utilization factor of PWM method and the dc link voltage. However in APF applications, the output voltage of converter contains predominantly voltage harmonics. In the presence of harmonics, the crest factor of a voltage or current signal can be significantly higher than the crest factor of pure sinusoidal waveform. Thus, the dc link voltage level of APF calculated with only the utilization factor of PWM method and the output voltage of converter is not adequate to meet the compensation requirements. In this condition, the controller of APF enforce the PWM method to operate highly in the over modulation region. This situation can cause performance degradation and stability problems. In order to solve this problem in APF applications, the dc link voltage can be increased with respect to the peak value of the output reference voltage. Although this solution provides a dc link voltage level for the compensation requirements of APF, this may cause an excessive increase of the dc link voltage and it may not be an efficient solution to this problem. In APF applications, PWM methods can operate up to the certain levels of the over modulation regions to provide the desired compensation performance. Thus, it will be appropriate for the dc link voltage level to select an optimum dc link voltage increase factor, K_{dc} which can provide the required compensation performance in the maximum load conditions.

The adaptive dc link voltage level specification of the proposed control method makes the selection of K_{dc} more challenging than the constant dc link operation. In the different load conditions, SHAPF provides the required compensation with different

VSC output reference voltage and dc link voltage level. Moreover, the crest factor changes with respect to the magnitudes and the phase angles of the fundamental and the harmonic components in a waveform so that the crest factor of VSC output reference voltage may change according to the different compensation situations.

In the scope of this thesis, the realized SHAPF prototype can compensate the low order dominant current harmonics of six pulse rectifiers up to 15A and the reactive power in the range of 10kVAr±30%. In order to determine the value of K_{dc}, the VSC output reference voltage waveform of SHAPF prototype is investigated with the simulation studies for the different loading conditions in the determined compensation range. Finally, the value of K_{dc} has been chosen 1.3 for SHAPF prototype to provide an effective compensation in all cases of the determined compensation range

3.4.1.4. DC Link Voltage Controller

The dc link voltage level control of SHAPF is performed by controlling active power flow from utility. This is achieved by generating voltage in phase with passive filter leading current at the output of VSC. If VSC generates voltage that has 90° leading phase shift with grid voltage, SHAPF consumes active power form utility and the dc link will be charged up. If VSC generates voltage that has 90° lagging phase shift with grid voltage, SHAPF supplies active power to utility and the dc link will be discharged.

The block diagram of the dc link controller is shown in Figure 3.32. In the dc link control of SHAPF, the error voltage between the dc link reference voltage and the measured dc link voltage is firstly calculated. The measured dc link voltage is filtered using a first order low pass filter in order to separate the ripples on the dc link voltage. The error voltage is applied to PI controller. PI controller generates the reference output voltage of VSC in the dq domain for the control of the dc link voltage. Inverse transformation from dq domain to αβ domain is realized with using the reference output signal obtained from PI controller as q component to achieve in 90° leading or lagging phase shift with grid voltage.

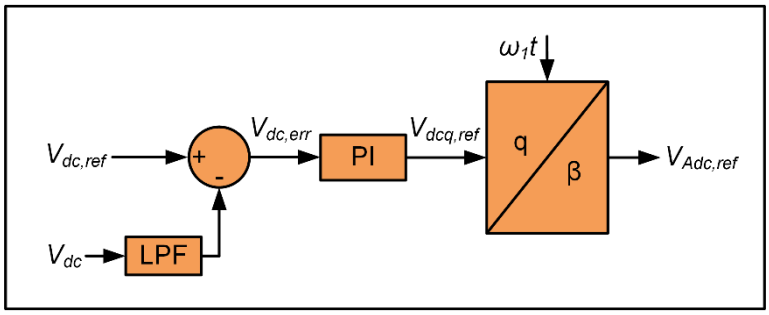


Figure 3.32. Block diagram of dc link voltage control

4. DESIGN AND IMPLEMENTATION OF SHAPF

4.1. Introduction

In the scope of this thesis work, a laboratory prototype of SHAPF is designed and implemented for the compensation of harmonic currents and reactive power in three phase three wire (3P3W) electrical power systems. The implementation studies of SHAPF prototype is realized in Power Electronics Research Laboratory of Çukurova University Electrical and Electronics Engineering Department.

SHAPF prototype can simultaneously compensate the dominant current harmonics of three phase six pulse rectifiers up to 15A, and meet the dynamic reactive power demand in the range of 10kVAr±30% in 400V supply voltage. Additionally SHAPF can control dc link voltage level according to the reactive power requirements of loads to increase the efficiency of system in low compensation power conditions. The design of the prototype system is performed regarding the requirements of industrial systems. Thus, the design approach presented for low power scale SHAPF prototype can be applied to high power systems successfully.

The theoretical design studies of SHAPF are supported by the simulation model of SHAPF prototype realized in MATLAB/Simulink. The power circuit design specifications of SHAPF prototype are determined and verified using the results of simulation study.

SHAPF system is mainly divided into two parts as, power circuit and electronic control system. In the following sections, the design specifications of SHAPF power circuit, the design of SHAPF power components and the design of SHAPF electronic control system are introduced.

4.2. Power Circuit Design Specifications of SHAPF

SHAPF prototype can compensate the dominant harmonics of three phase six pulse rectifier up to 25^{th} harmonics with the rated current of 15A. The individual harmonic current compensation ratings of SHAPF are determined according to the

harmonic characteristic of the capacitive loaded six pulse rectifier which is the most common three phase nonlinear load configuration in distribution systems. The rectifiers are commonly utilized with smoothing reactors to decrease their harmonic contents. The inductance value of smoothing reactors are selected in range of 1% and 5% of rectifier impedance seen from power system. In Table 4.1, the harmonic load characteristic of three phase capacitive loaded rectifier is presented for the different values of smoothing reactors. The individual harmonic current ratings of SHAPF are extracted using the harmonic percentages of three phase rectifier with the smoothing reactor in value of 1% as given in Table 4.2. The design values for individual harmonic compensation current are approved as given in Table 4.2.

Table 4.1. Harmonic load characteristic of three phase capacitive loaded rectifier

Harmonic Order	Smoothing Reactor Percentages		
	1%	2%	3%
Fun.	100%	100%	100%
5^{th}	63.5%	44.6%	35%
7^{th}	38.5%	20.1%	10%
11^{th}	8.2%	8%	6.9%
13^{th}	8.1%	4.5%	3%
17^{th}	4%	3.6%	2.8%
19^{th}	3.3%	2%	1.8%
23^{rd}	2.4%	2%	1.3%
25^{th}	1.85%	1.3%	1.2%
THD	75.5%	50.1%	37.4%
The results are taken from the supply current spectrum of 5kW capacitive loaded three phase six pulse rectifier (Load Resistance 50Ω, Load Capacitance 2200μF)			

SHAPF prototype also compensates reactive power in the range of 10kVAr±30%. As mentioned in the previous sections, PF part provides static capacitive reactive power capacity and dynamic range of reactive power compensation can be controlled with APF part. In addition, APF part set the dc link voltage level with respect to its reactive power injection requirements. In order to realize efficient operation with SHAPF prototype, the main part of reactive power compensation

capacity should be supplied with PF and dynamic changes around the reactive power capacity of PF should be controlled with APF part. Thus, the capacitive reactive power rating of PF should be kept around 10kVAr and the reactive power compensation capacity of APF should control reactive power up to ±3kVAr with regarding the load conditions. The power circuit design specifications of SHAPF prototype are summarized in Table 4.3.

Table 4.2. Harmonic current ratings of SHAPF

	Percentage Values According to Tot. Rated Harmonic Compensation Current	Calculated Harmonic Compensation Current Values	Design Values for Individual Harmonic Compensation Currents
Tot.	100%	15A	-
5^{th}	84.23%	12.63A	13A
7^{th}	51.06%	7.66A	8A
11^{th}	10.87%	1.63A	2A
13^{th}	10.74%	1.61A	2A
17^{th}	5.30%	0.79A	1A
19^{th}	4.37%	0.65A	1A
23^{rd}	3.18%	0.47A	0.5A
25^{th}	2.45%	0.36A	0.5A

Table 4.3. Power circuit design specifications of SHAPF prototype

Specifications	Rating
Nominal Grid Voltage	400V
Harmonic Compensation Total Rated Current	15A
Individual Harmonic Compensation Rated Currents	See Table 4.2.
Reactive Power Compensation Rating	10kVAr±30%.
Reactive Power Rating of PF	10kVAr
Maximum Value of DC Link Voltage of APF	As low as possible

4.3. Power Circuit Design of SHAPF

4.3.1. Design of PF

In the design specifications, it is stated that the capacitive reactive power rating of SHAPF should be selected as 10kVAr for the efficiency of the system. Another important specification of PF is cut-off frequency which directly affects the filtering performance of system and the dc link voltage ratings of APF. SHAPF prototype is designed for the compensation dominant harmonics of three phase rectifiers. It is known and also shown from Table 4.1 that three phase rectifiers dominantly generates 5^{th} and 7^{th} harmonic currents. Because of these, the cut-off frequency should be selected near the frequencies of 5^{th} and 7^{th} harmonics.

At first sight, the selection of 5^{th} harmonic frequency for the cut-off frequency of PF may be proper for the effective compensation of the most dominant harmonics. However, 5^{th} harmonic PF has poorer filtering performance in 11^{th}, 13^{th} and higher frequency harmonics than 7^{th} harmonic PF. Moreover, the required output voltage of APF is higher with 5^{th} harmonic PF than 7^{th} harmonic PF for the compensation of 11^{th}, 13^{th} and higher frequency harmonics. Therefore, this situation affects not only the output voltage but also the dc link voltage of APF. Furthermore, the size and also cost of 7^{th} harmonic PF reactor are lower than 5^{th} harmonic PF reactor (Srianthumrong and Akagi, 2003; Wiroj et al., 2007).

The impedance characteristics of 10kVAr PFs tuned to 5^{th} and 7^{th} harmonic frequencies are demonstrated in Figure 4.1 It is shown from Figure 4.1 that 7^{th} harmonic PF presents more effective filtering performance than 5^{th} harmonic PF. The required APF output voltage for the compensation of harmonic currents in the values of design specifications of SHAPF is presented in Table 4.4 for ideal grid conditions. It is shown that APF generates over 50% more output voltage in SHAPF with 5^{th} harmonic PF in order to inject harmonic current values denoted in the design specifications. Thus, the cut of frequency of PF in SHAPF prototype is selected 350Hz. The design specifications of PF is summarized in Table 4.5.

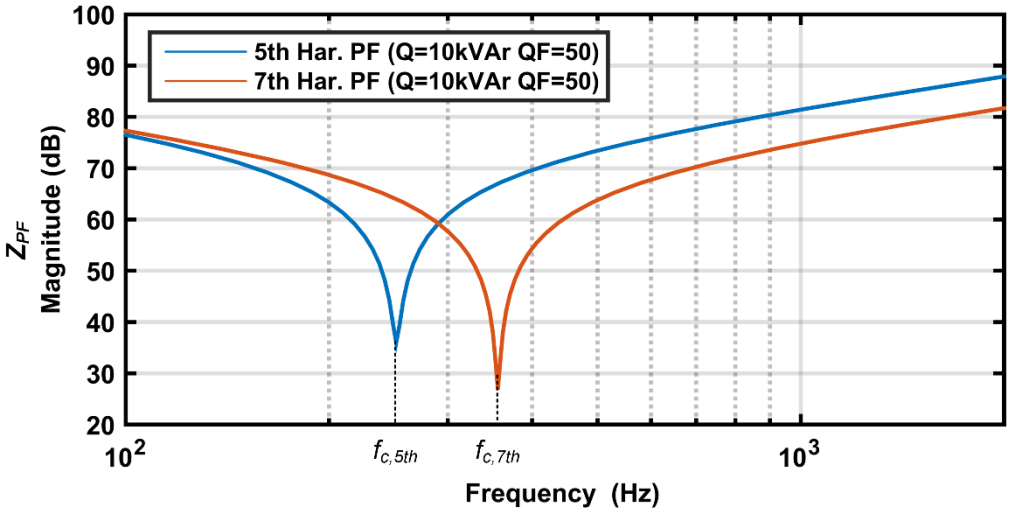


Figure 4.1. Impedance characteristics of 5th and 7th harmonic PFs

Table 4.4. Required APF output voltage for compensation of harmonic currents

	Design Values for Individual Harmonic Compensation Currents	APF Output Voltage for with 5th Harmonic PF for Individual Harmonics	APF Output Voltage for with 7th Harmonic PF for Individual Harmonics
5th	13A	0V	21.6
7th	8A	17.3V	0V
11th	2A	11.1V	4.1V
13th	2A	14.1V	5.9V
17th	1A	9.9 V	4.5V
19th	1A	11.2V	5.2V
23rd	0.5A	6.9V	3.3V
25th	0.5A	7.6V	3.6V
Total Output Voltage of APF		30.8V	24.3V

The calculations in this table are evaluated with 10kVAr PF whose QF is infinity and ideal supply conditions.

Table 4.5. Design specifications of PF

Specifications	Rating
Nominal Grid Voltage	400V
Nominal Grid Frequency	50Hz
Rated Capacitive Reactive Power	10kVAr
Tuned Frequency of PF, f_c	350Hz

The design calculations of PF are as follows. The harmonic factor of PF is calculated with Eq. 4.1 as;

$$p = \left(\frac{f_1}{f_c} \right)^2 .100\% \tag{4.1}$$

$$p = \left(\frac{50}{350} \right)^2 .100\% = 2.04\%$$

The capacitance value of PF is determined with Eq. 4.2 as;

$$C_F = \frac{Q_F}{2\pi f_1 V_{S_1}^2}(1-p) \tag{4.2}$$

$$C_F = \frac{10.10^3}{2x\pi x50x400^2}(1-0.0204) \cong 203\mu F$$

Because PF have been used series with VSC of APF and SHAPF has high harmonic compensation current ratings, the standard ac reactive power compensation capacitors are not suitable for SHAPF applications. Instead of these, film capacitors can be preferred with high voltage and current ratings. From the standard catalog values of the film capacitor manufacturers, the capacitance value of PF is determined 200μF.

The inductance value of PF reactor is calculated from Eq. 4.3 as;

$$L_F = \frac{1}{(2\pi f_c)^2 C_F} \tag{4.3}$$

$$L_{PF} = \frac{1}{(2x\pi x350)^2 200.10^{-6}} = 1.033mH \cong 1mH$$

The quality factor of PF, *QF* should be as high as possible for the effective filtering performance of system. In the worst case condition, the value of *QF* should be minimum 20. Then, the equivalent resistance of PF is calculated from Eq. 4.4 as;

$$QF = \frac{2\pi f_c L_F}{R_F} \tag{4.4}$$

$$R_F \leq \frac{2x\pi x350x1x10^{-3}}{20} \cong 0.11\Omega$$

The impedance and the filtering characteristic of PF with calculated values are demonstrated in Figure 4.2 and 4.3, respectively. According to determined capacitance and inductance values of PF, the passive filter rated capacitive reactive power is evaluated from Eqs. 4.5 and 4.6 by neglecting R_F as follows;

$$Z_F = \left| 2\pi f_1 L_F - \frac{1}{2\pi f_1 C_F} \right| \tag{4.5}$$

$$Z_F = \left| \left(2x\pi x50x1x10^{-3} \right) - \frac{1}{2x\pi x50x200x10^{-6}} \right| = 15.6\Omega$$

$$Q_F = \frac{V_{S_1}^2}{Z_F} \tag{4.6}$$

$$Q_F = \frac{400^2}{15.6} \cong 10.25kVAr$$

With these inductance and capacitance values, PF supplies 10.25kVAr capacitive reactive power. In order to satisfy the design requirements of SHAPF, APF part must supply 2.75kVAr capacitive reactive power and 3.25kVAr inductive reactive power.

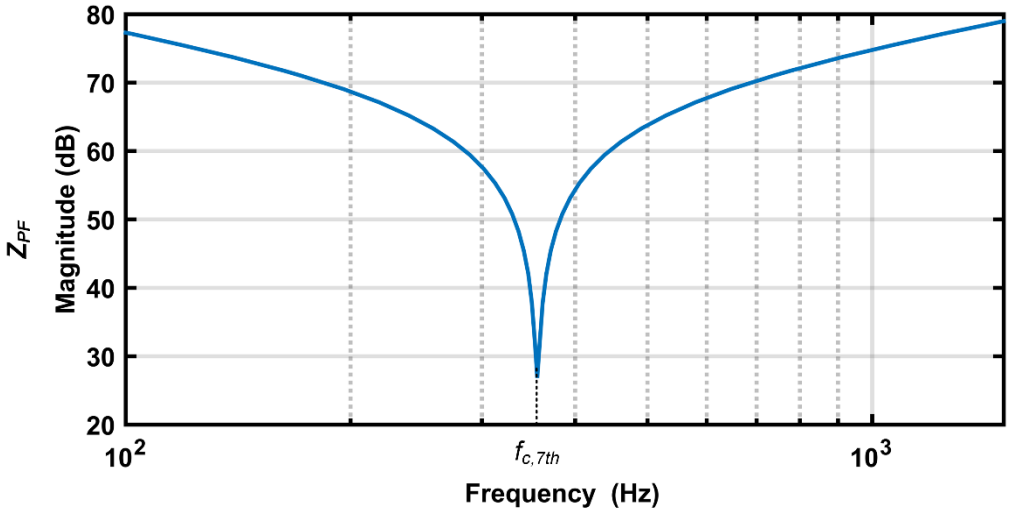


Figure 4.2. Impedance characteristic of PF with calculated values

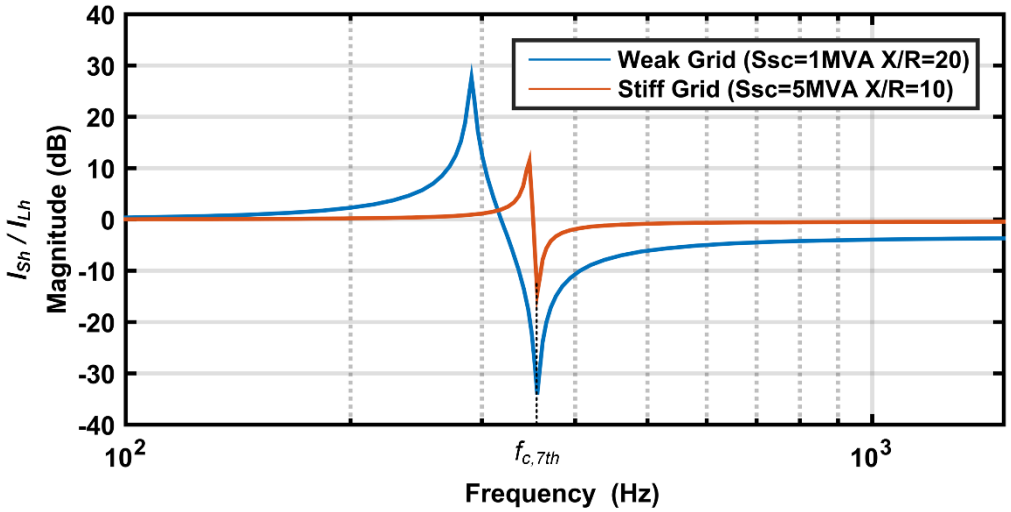


Figure 4.3. Filtering characteristic of PF with calculated values

The fundamental current of PF in standalone operation and in operation with APF is calculated from Eqs. 4.7 and 4.8, respectively.

$$I_{F_1} = \frac{V_{S_1}}{\sqrt{3}Z_F} \tag{4.7}$$

$$I_{F_1} = \frac{400}{\sqrt{3}x15.6} \cong 14.8A$$

$$I_{F_1} = \frac{Q_{SHAPF,\max}}{\sqrt{3}V_{S_1}} \tag{4.8}$$

$$I_{F_1} = \frac{13.10^3}{\sqrt{3}x400} \cong 18.76A$$

Both the fundamental reactive current and harmonic currents flow through PF and APF. Thus the current rating of PF and also SHAPF is calculated with Eq. 4.9. The design values for individual harmonic compensation currents are used for the magnitudes of harmonic currents in Eq. 4.9.

$$I_F = \sqrt{\sum_{h=1} I_{F_h}^2} \tag{4.9}$$

$$I_F = \sqrt{18.76^2 + 13^2 + 8^2 + 2^2 + 2^2 + 1^2 + 1^2 + 0.5^2 + 0.5^2} \cong 24.4A$$

The fundamental phase voltage across the capacitor of PF in standalone operation of PF and in operation of PF with APF is calculated from Eqs. 4.10 and 4.11, respectively.

$$V_{Cp_1} = \frac{V_{S_1}}{\sqrt{3}\left(1-p\right)} \tag{4.10}$$

$$V_{Cp_1} = \frac{400}{\sqrt{3}\left(1-0.0204\right)} \cong 235.7V$$

$$V_{Cp_1} = \frac{Q_{SHAPF,\max}}{\sqrt{3}V_{S_1}} Z_C \tag{4.11}$$

$$V_{Cp_1} = \frac{13x10^3}{\sqrt{3}x400} x \frac{1}{2x\pi x50x200x10^{-6}} \cong 298.6V$$

In addition to the fundamental voltage seen across the capacitor of PF, a voltage drop is formed across the terminals of PF and also PF capacitor because of the harmonic compensation current of SHAPF. The total rms voltage seen across the terminals of PF capacitor is calculated from Eq. 4.12. The design values for individual harmonic compensation currents are used for the magnitudes of harmonic currents in Eq. 4.12.

$$V_{Cp} = \sum_{h=1} I_{F_h} Z_{C_h} \tag{4.12}$$

$$\begin{aligned} V_{Cp} = {} & 18.76x \frac{1}{2x\pi x50x200x10^{-6}} + 13x \frac{1}{2x\pi x250x200x10^{-6}} \\ & + 8x \frac{1}{2x\pi x350x200x10^{-6}} + 2x \frac{1}{2x\pi x550x200x10^{-6}} \\ & + 2x \frac{1}{2x\pi x650x200x10^{-6}} + 1x \frac{1}{2x\pi x850x200x10^{-6}} \\ & + 1x \frac{1}{2x\pi x950x200x10^{-6}} + 0.5x \frac{1}{2x\pi x1150x200x10^{-6}} \\ & + 0.5x \frac{1}{2x\pi x1250x200x10^{-6}} \cong 304V \end{aligned}$$

As a result, the capacitance value of passive filter capacitor is selected 200μF, the minimum rms voltage rating of PF capacitor is calculated 304V, the inductance value of passive filter reactor is determined 1mH and the minimum rms current rating of passive filter capacitor and reactor are calculated 24.4A. The voltage and current ratings of PF should be at least 10% higher than the calculated values for safety operation by considering the resonance, overvoltage and overloading conditions. In order to meet capacitor ratings, GP84 series power electronic capacitors of Ducati Energia is selected for SHAPF prototype. The reactor is produced by a domestic

manufacturer as single phase reactors with 50A rms current rating. The details of technical specifications of PF reactor and capacitor are presented in Table 4.6.

Table 4.6. Technical specifications of PF reactor and capacitor

PF Reactor	Type: Single Phase Lamination Plate Thickness: 0.5mm Inductance Value: 1mH Tolerance: 3% Rated Current: 50A Insulation Voltage: 2.5kV Temperature Class: Class F
PF Capacitor	Brand-Model: Ducati Energia-GP 84 Series Type: Single phase, Film Capacitor Capacitance Value: 200uF Tolerance: 5% Rated RMS Voltage: 450V Rated DC Voltage:825V Rated AC Voltage: 630V Max. Rated Current: 70A Surge Voltage: 1800V Surge Current: 5.7kA

4.3.2. Design of VSC

The design of VSC is divided into four main parts as, the design of dc link capacitor bank, the selection of power semiconductors, the design of heatsink and finally the design of dc laminated busbar and power stage layout. Today's power semiconductor technology assures VSC design of SHAPF prototype with specified power ratings using the transistor integrated circuit package based IGBTs or MOSFETs such as TO-220 and TO-247 packages. However, one of the main aims of the laboratory prototype implementation is to realize a low scale model of high power SHAPF system. Thus, the design of VSC is realized with IGBT power modules and laminated busbar for further studies.

4.3.2.1. Design of DC Link Capacitor Bank

The dc link capacitors hold the required energy for the compensation of harmonics and the reactive power. The dc link voltage level of VSC, dc link ripple current and the capacitance value of dc link capacitor bank are three important parameters for the design of dc link capacitor bank. The dc link voltage level and current ripple are directly proportional to the output compensation voltage and current of VSC, respectively. The dc link capacitance value affects the ripple voltage on dc link voltage level with respect to the transferred compensation energy and it has significant effect on the compensation performance of SHAPF.

The minimum required rms value of output phase voltage of VSC, V_{Amin} can be determined by Eqs. 3.54 and 3.55 as clarified in Section 3.4.1.3. The reactive power output of SHAPF, Q_F is changed in the range of 10kVAr±30% and the fundamental frequency impedance of PF is calculated from Eq. 4.5 as 15.6Ω. The output voltage of APF can be calculated from Eq. 3.54 for the edge values of reactive power compensation rating of SHAPF as;

$$V_{A_r} = \frac{400}{\sqrt{3}}\left|1 - \frac{13x10^3 x15.6}{400^2}\right| \cong 62V$$

$$V_{A_r} = \frac{400}{\sqrt{3}}\left|1 - \frac{7x10^3 x15.6}{400^2}\right| \cong 73.2V$$

It is shown from the calculations that VSC requires higher output voltage for the compensation of 7kVAr reactive power than 13kVAr reactive power in the normal operating voltage levels because of 10.25kVAr reactive power rating of PF. The point paid attention about this issue is that the reactive power capacity is depended on the PCC voltage and PCC voltage can be varied in band of 10% of its rated value during normal operation condition of supply. This condition causes the increase of output voltage ratings of VSC for the reactive power compensation specifications. For instance, if PCC voltage decreases to near to 360V, PF supplies approximately

8.3kVAr. APF must provide the maximum reactive power compensation rating of 13kVAr so APF must generate nearly 118V to supply 13kVAr reactive power by SHAPF at 360V level. Conversely, if PCC voltage increases to near to 440V, PF supplies approximately 12.4kVAr. VSC must provide the minimum reactive power compensation rating of 7kVAr so VSC must generate nearly 110V to supply 7kVAr reactive power by SHAPF at 440V level. By the help of example given for the variations of PCC voltage, the minimum value of VSC output should be taken 118V for the worst case reactive power compensation conditions.

The required output voltage for the compensation of harmonic currents, V_{Ahn} can be calculated using the impedance values calculated for PF in Section 4.3.1 and taking the determined design values for individual harmonic compensation currents instead of load harmonic currents. Thus, the minimum value of VSC output voltage for the compensation of harmonic current design values is calculated as 30.8V.

The final term V_{Pm} in Eq. 3.55 is the most challenging parameter due to its unpredictable nature. In order to determine the minimum dc link voltage level requirement for the worst case compensation scenario, the values of V_{Pm} are decided by taking the upper harmonic limit voltages determined in EN50160 standard for LV systems. The harmonic voltages are regarding for only odd harmonics up to 13^{th}. The triplen harmonics are not taken into account because SHAPF prototype is developed for 3P3W systems. The minimum required output phase voltages for the reactive power compensation V_{Ar}, the compensation of each individual harmonic current, V_{Ahn} and the voltage harmonics, V_{Pm} are presented in Table 4.7 and the minimum required rms value of VSC output phase voltage, V_{Amin} is calculated from Eq. 3.55 as 125.8V.

Table 4.7. Minimum required VSC output voltage ratings for worst case conditions

	Design Values for Individual Har. Comp. Cur.	Min. Required APF Output Vol. for Reac. Comp.	Min. Required APF Output Vol. for Har. Comp.	Min. Required APF Output Vol. Caused by Har. Vol.	Min. Tot. Output Vol. for Fun. Comp. and Harmonics
Fun.	-	118V	-	-	118V
5th	13A	-	21.6V	V_{Sph}x6%=13.8V	35.4V
7th	8A	-	1V	V_{Sph}x5%=11.5V	12.5V
11th	2A	-	4.1V	V_{Sph}x3.5%=8V	12.1V
13th	2A	-	5.8V	V_{Sph}x3%=7V	12.8V
17th	1A	-	4.5V	-	4.5V
19th	1A	-	5.2V	-	5.2V
23rd	0.5A	-	3.3V	-	3.3V
25th	0.5A	-	3.6V	-	3.6V
		Min. Required Output Phase Voltage of APF, V_{Amin}			≈ 125.8V

The minimum dc link voltage level of SHAPF is calculated from Eq. 3.56. As stated in Section 3.4.1.3, the increase factor, K_{dc} in Eq. 3.56 is determined as 1.3 and the utilization factor of PWM method, U_{PWM} is taken $1/\sqrt{6}$ for SVPWM method. The minimum dc link voltage level of SHAPF is calculated as 400V in the following equation for the worst case operation conditions. The design specification of capacitor bank voltage level should be higher than 400V for the safety operation.

$$V_{dc_{\min}} = 1.3x\sqrt{6}x125.8 \cong 400V$$

The dc link voltage and current consist of dc and ac components as denoted in Eqs. 4.13 and 4.14 as;

$$v_{dc}(t) = V_{dc} + \tilde{v}_{dc}(t) \tag{4.13}$$

$$i_{dc}(t) = I_{dc} + \tilde{i}_{dc}(t) \tag{4.14}$$

The dc link capacitor current of APF can be determined with using instantaneous power balance equation given in Eq.4.15 as (Thomas et al., 1998);

$$v_{dc}(t)i_{dc}(t) = p_{ac}(t) \tag{4.15}$$

Also the ac side instantaneous power consists of dc and ac components as shown in Eq. 4.16.

$$p_{ac}(t) = P_{ac} + \tilde{p}_{ac}(t) \tag{4.16}$$

However, the ac side average power of APF, P_{ac} can be assumed as zero because the power loss of APF is considerably lower than its power rating. Thus, the ac side instantaneous power of APF also can be represented by Eq. 4.17 as;

$$\tilde{p}_{ac}(t) \approx v_{A_a}(t)i_{F_a}(t) + v_{A_b}(t)i_{F_b}(t) + v_{A_c}(t)i_{F_c}(t) \approx \sum_n P_n \cos(n\omega t + \phi_n) \tag{4.17}$$

Moreover, the dc component of dc link current can be assumed as zero because the power loss of APF is considerably low compared to its power rating. Also, the ac component of dc link can be neglected because its amplitude is very small compared with the dc component. Thus, the ac component of dc link current can be represented in Eq. 4.18 as (Jou et al., 1994);

$$\tilde{i}_{dc}(t) \approx \frac{\tilde{p}_{ac}(t)}{V_{dc}} \tag{4.18}$$

The dc link ripple current of SHAPF prototype is investigated and analyzed with the help of simulation studies. The waveform of dc link current taken from the simulation studies is presented in Figure 4.4 while SHAPF is providing the full harmonic and reactive power compensation at rated voltage conditions. It is shown from Figure 4.4 that the peak value of dc link current ripple reaches nearby 83A. The

rms value of ripple current seen in Figure 4.4 is calculated as 15.8A. The minimum rms and ripple value of dc link current which is required for the dc link capacitor bank ratings and life time calculations should be taken as 17.5A and 92A with increasing the value obtained in simulation results to approximately 10% of its value for the overload situations.

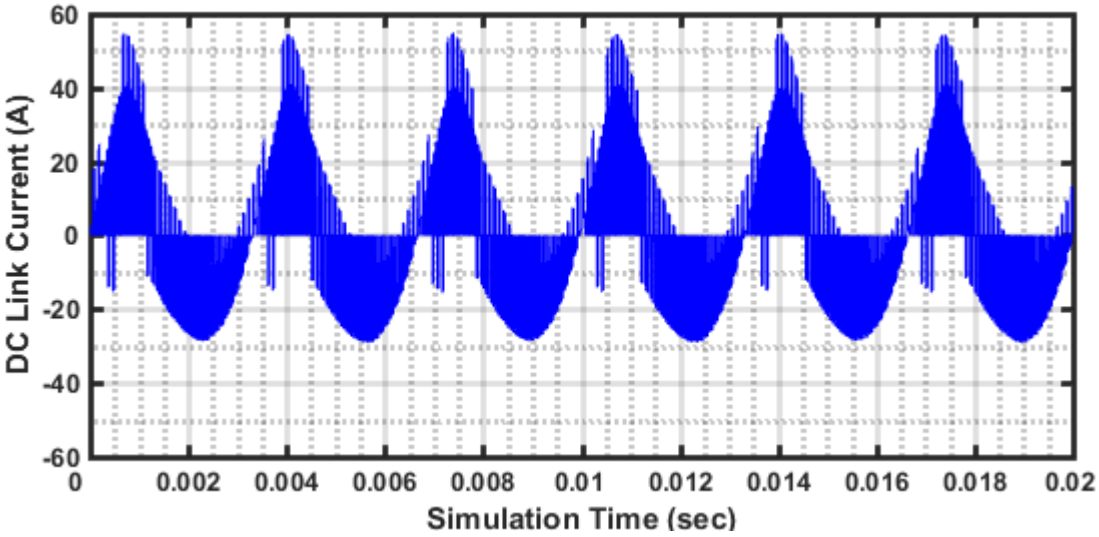


Figure 4.4. DC link current waveform

The dc link ripple voltage depends on the dc link capacitance and dc link current ripple as given in Eq. 4.19 as;

$$\tilde{v}_{dc}(t) = \frac{1}{C_{dc}} \int_0^t \tilde{i}_{dc}(t) dt \tag{4.19}$$

The dc link voltage ripple is important for the waveform quality at the output of APF so that the peak to peak ripple of dc link voltage should be kept under 10% of the average dc link voltage. The dc link ripple voltage must be set under certain limits by setting the capacitance value. With combining Eqs. 4.17, 4.18 and 4.19, the ripple voltage of dc link capacitor is approximately calculated by Eq. 4.20 as (Jou et al., 1994);

$$\tilde{v}_{dc}(t) \approx \frac{1}{V_{dc}C_{dc}} \sum_{n} \frac{P_n}{n\omega} \sin(n\omega t + \phi_n) \tag{4.20}$$

With using Eq. 4.20, the dc link capacitor value can be obtained for three phase APF by Eq. 4.21 as;

$$C_{dc} \approx \frac{\sqrt{2}}{\Delta\tilde{v}_{dc}V_{dc}} \sqrt{\sum_{k=0}^{\infty}\sum_{j=0}^{\infty}\left(\frac{V_{a_k}I_{a_j} + V_{b_k}I_{b_j} + V_{c_k}I_{c_j}}{(k+j)\omega}\right)^2} \tag{4.21}$$

In SHAPF prototype, the dc link voltage is varied in wide range because of the dynamic reactive power compensation specification. This situation complicates the determination of dc link capacitance value. In Table 4.8, the dc link capacitance values of APF are calculated for different supply operating voltage values with different compensation cases. The compensation cases consist of only harmonic compensation cases, harmonic and reactive power compensation cases and harmonic and reactive power compensation cases with existing supply harmonics. The capacitance values are calculated using Eqs. 4.9, 4.10, 4.12 and 4.21. In the calculations, the values of harmonic currents are taken from the design specifications given in Table 4.2, the supply voltage harmonic values are taken from Table 4.7. The output voltage values of APF are calculated with Eq. 4.9 and 4.10. The minimum dc link values are calculated for SVPWM technique from Eq. 4.12. The magnitude of dc link ripple voltage in Eq. 4.21 is taken 3% of the dc link voltage.

It is shown in Table 4.8 that the calculated capacitance value for APF varies in large ratios related with the required dc link voltage and the compensation current. The reactive power compensation current in fundamental frequency has dominant effect on dc link capacitance value. According to the calculated dc link capacitance values, the minimum capacitance value of the dc link capacitor bank should be taken 4.56mF to obtain sufficient performance in worst case conditions.

Another important issue related with the design of dc link capacitor bank is the minimization of dc link inductance. Switching operation of power semiconductors, the

turn-off operation can cause high voltage spikes across collector emitter voltage of power semiconductors because of the inductance of current commutation loop. The dc link inductance which is mainly formed from the inductance of dc side connection wires or busbars with the equivalent series inductance (ESL) of dc link capacitors is the remarkable part of the commutation loop inductance. Thus, the ESL value of dc link capacitors should be as low as possible. Other important parameter of dc link capacitors is the equivalent series resistance (ESR). Its value must be as low as possible for the dc link losses. The determined electrical specifications for dc link capacitor bank of APF is summarized in Table 4.9.

In order to create dc link capacitor bank, film capacitors are one of the best candidates with their electrical specifications. The high capacitance, voltage and current ratings can decrease the size of dc link capacitor bank. On the other hand their costs are significantly higher than aluminum electrolytic capacitors which is the other conventional capacitor type for the design of dc link capacitor banks. As a result of product search performed for the film and aluminum electrolytic capacitors of different manufacturers, it is decided to use aluminum electrolytic capacitors because of their low costs and short delivery times.

In order to satisfy the electrical specifications of the dc link capacitor bank presented in Table 4.9, 3300µF 450V aluminum electrolytic capacitor, B43564A5338M from EPCOS is chosen. The technical specifications of the chosen capacitor are given in Table 4.10. 8 pieces of 3300µF 450V capacitors are used in dc link capacitor bank to form four parallel branch with connecting two of each in series as shown in Figure 4.5. The electrical specifications of the designed capacitor bank is given in Table 4.11. The capacitance value of dc link capacitor bank has been kept higher than the calculated value to ensure the dc link voltage ripple in certain limits for unexpected conditions. The dc link voltage of capacitor bank has been chosen 900V for using VSC in the future laboratory studies.

Table 4.8. Calculated dc link capacitance values

Cases	Har. Comp. Current Val.	Reac. Power Comp.	Supply Vol. Har.	Min DC Link Vol.	DC Link Vol. Ripple	Calculated Cap.Value
Case 1 - Only Har. Comp.@ 400V	See Table 4.2	Q_{PF}	-	77V	3%	2.76mF
Case 2 - Har. & Reac. Power. Comp. @ 400V	See Table 4.2	7kVAr	-	244V	3%	1.78mF
Case 3 - Har. & Reac. Power. Comp. @ 400V	See Table 4.2	13kVAr	-	214V	3%	3.46mF
Case 4 - Har. & Reac. Power. Comp. with Existence of Vol .Har. @ 400V	See Table 4.2	7kVAr	See Table 4.7	268V	3%	1.50mF
Case 5 – Har. & Reac. Power. Comp. with Existence of Vol .Har. @ 400V	See Table 4.2	13kVAr	See Table 4.7	241V	3%	2.78mF
Case 6 - Only Har. Comp. @ 360V	See Table 4.2	Q_{PF}	-	175V	3%	3.62mF
Case 7 - Har. & Reac. Power. Comp. @ 360V	See Table 4.2	7kVAr	-	128V	3%	3.20mF
Case 8 - Har. & Reac. Power. Comp. @ 360V	See Table 4.2	13kVAr	-	385V	3%	2.22mF
Case 9 - Har. & Reac. Power. Comp. with Existence of Vol .Har. @ 360V	See Table 4.2	7kVAr	See Table 4.7	169V	3%	1.19mF
Case 10 - Har. & Reac. Power. Comp. with Existence of Vol .Har. @ 360V	See Table 4.2	13kVAr	See Table 4.7	400V	3%	2.06mF
Case 11 - Only Har. Comp.@ 440V	See Table 4.2	Q_{PF}	-	158V	3%	3.26mF
Case 12 - Har. & Reac. Power. Comp. @ 440V	See Table 4.2	7kVAr	-	359V	3%	1.15mF
Case 13 - Har. & Reac. Power. Comp. @ 440V	See Table 4.2	13kVAr	-	87V	3%	4.56mF
Case 14 - Har. & Reac. Power. Comp. with Existence of Vol .Har. @ 440V	See Table 4.2	7kVAr	See Table 4.7	376V	3%	1.06mF
Case 15 - Har. & Reac. Power. Comp. with Existence of Vol .Har. @ 440V	See Table 4.2	13kVAr	See Table 4.7	140V	3%	2.18mF

Table 4.9. Determined electrical specifications for dc link capacitor bank

Capacitance Value	≥4.56mF
Rated DC Voltage	≥400V
Rated Ripple Current	≥92A
ESL Value	As low as possible
ESR Value	As low as possible

Table 4.10. Technical specifications of the chosen dc link capacitor

Manufacturer	EPCOS
Product No	B43564A5338M
Capacitance Value	3300µF
Rated DC Voltage	450V
Rated Ripple Current	19A
Maximum Ripple Current	32A
ESL Value	20nH
ESR Value	50mΩ

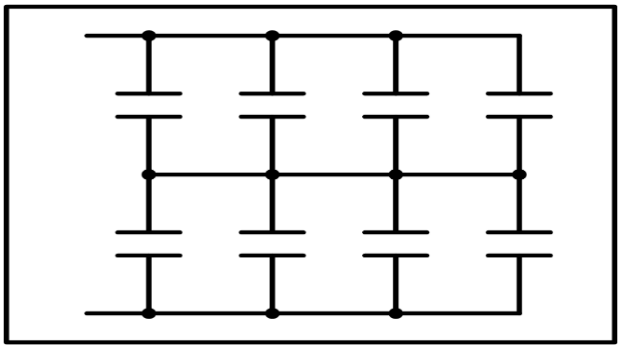


Figure 4.5. DC link capacitor bank connection diagram

Table 4.11. Electrical specifications of the designed dc link capacitor bank

Equivalent Capacitance Value	6.6mF
Total Rated DC Voltage	900V
Total Rated Ripple Current	76A
Total Maximum Ripple Current	128A
Equivalent ESL Value	10nH
Equivalent ESR Value	25mΩ

4.3.2.2. Selection of Power Semiconductors

In previous sections, the minimum dc link voltage value is determined as 400V and the minimum rms value of phase current is calculated 24.4A for the worst case situations. The voltage and current waveforms of power switch taken from the simulation results for the rated design specifications of Case 3 in Table 4.8 are given in Figure 4.6.

The minimum collector-emitter voltage and collector current of power semiconductors should be 400V and 60A with respect to theoretical calculations and simulation results. The switching frequency has been chosen 10kHz for the effective modulation of harmonic reference voltages up to 25^{th} harmonics. The possible power semiconductor candidates for these specifications are IGBT power modules whose collector-emitter voltage ratings are 600V and 1200V. The collector emitter voltage and collector current of IGBT modules has been chosen 1200V and 100A respectively for using VSC in the future laboratory studies. The screw terminal modules have been preferred instead of solder pin modules for easy mounting and demounting. The investigated candidate 1200V 100A IGBT module products are listed with key technical specifications in Table 4.12. These products have been compared in terms of their conduction and switching losses, costs and lead time. SKM100GB12T4 from Semikron has been chosen because of the lower cost and shorter lead time than the other products. The detailed technical specifications of SKM100GB12T4 IGBT Module are presented in Appendix C.

In order to generate switching signals of IGBTs, gate drivers are required. There are a wide range product portfolio for gate drivers. Instead of simple gate drive integrated circuit products, advanced gate drive systems which have advanced specifications such as top and bottom signal interlock, deadband generation, short circuit protection and soft turn-off. Thus, SKYPER PRO 32 R from Semikron has been chosen to generate gate drive signals for SKM100GB12T4 modules by considering cost and lead time of gate drive products. The detailed technical specifications of SKYPER PRO 32 R are presented in Appendix C.

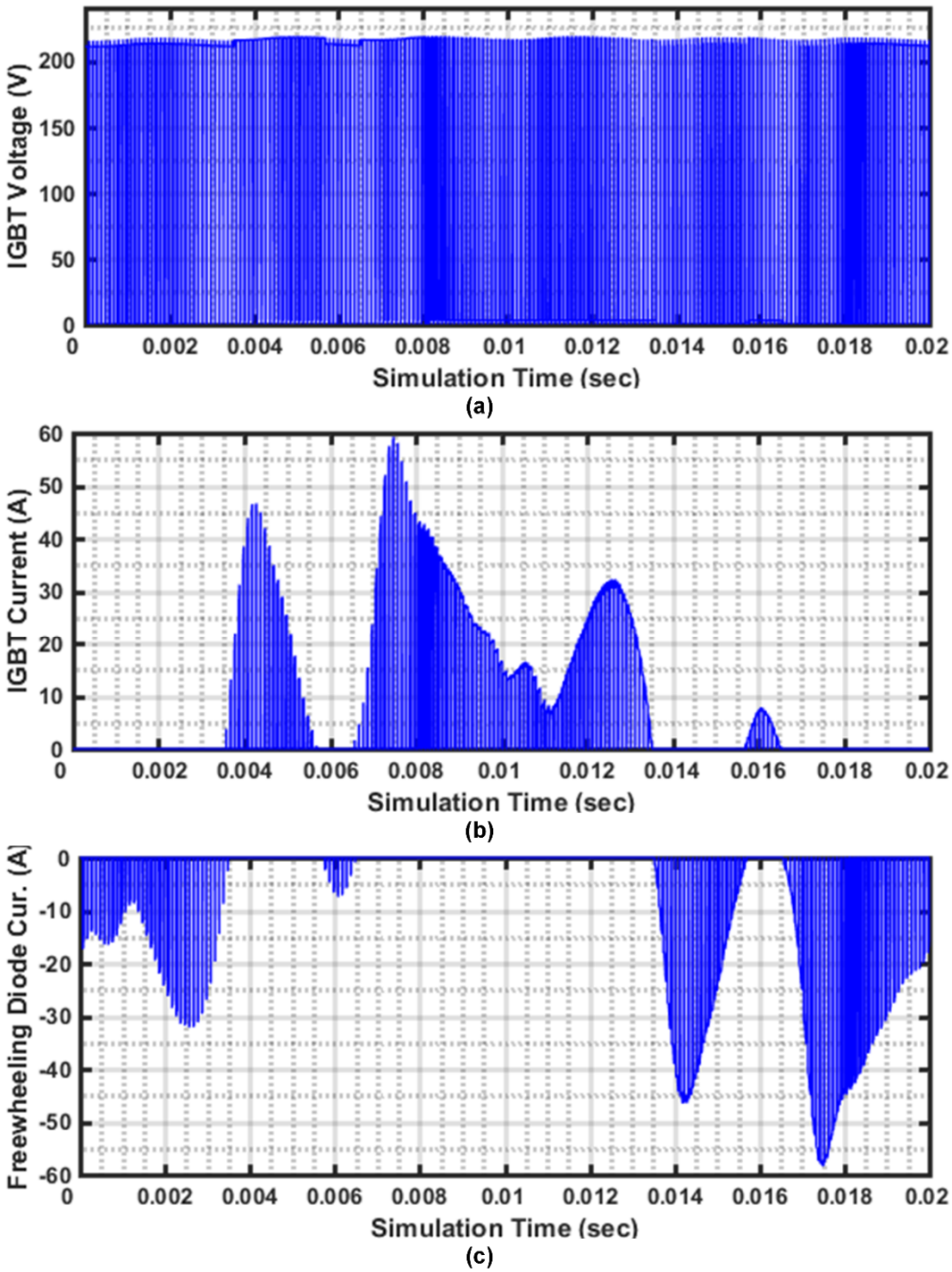


Figure 4.6. Voltage and current waveforms of power switch taken from simulation results
(a) Switch voltage (b) Switch current (c) Freewheeling diode current

Table 4.12. Technical specifications of candidate IGBT module products

Manufacturer Product No	Switch Config.	V_{CES} (V)	I_{Cnom} (A)	$V_{CE(SAT)}$ (V)	E_{ON} (mJ)	E_{OFF} (mJ)	E_R (mJ)
SEMIKRON SKM100GB12T4	Half Bridge	1200	100	2.2	15	10.2	5.9
SEMIKRON SKM100GB12V	Half Bridge	1200	100	2.2	10.7	8.7	5.7
SEMIKRON SEMiX101GD12Vs	Six Pack	1200	100	2.2	12.9	11.4	7.7
SEMIKRON SEMiX151GD126HDs	Six Pack	1200	100	2	12	14	11.5
INFINEON FF100R12RT4	Half Bridge	1200	100	2.1	10.5	10	7
INFINEON FF100R12KS4	Half Bridge	1200	100	3.85	9.5	7.7	5.5
INFINEON FS100R12PT4	Six Pack	1200	100	2.1	10.5	9.3	8
FUJI ELECTRIC 2MBI100VA-120-50	Half Bridge	1200	100	2.25	7	9	8.7
POWEREX CM100DY-24A	Half Bridge	1200	100	2.4	3.5	10	2.5
POWEREX CM100DY-24NF	Half Bridge	1200	100	2	5	13	-

4.3.2.3. Selection of Heat Sink

In order to perform the selection of appropriate heat sink for VSCs, the power loss and thermal calculations of power semiconductors in VSC should be accomplished. The first step is the power loss calculation of power semiconductors to estimate the junction temperature for thermal calculations. The total power dissipation of power semiconductors are divided into conduction and switching losses as given in Eq. 4.24 as;

$$P_{tot} = P_{cond} + P_{sw} \tag{4.22}$$

The power semiconductors in VSCs should be formed from power switching device with freewheeling diode for the proper operation. In SHAPF prototype, it has been decided that IGBTs with freewheeling diodes have been used as power

semiconductors of VSC. The conduction losses of IGBT with freewheeling diode can be calculated for each of IGBT and freewheeling diode with Eqs. 4.23 and 4.24 respectively as (ABB, 2015; Electric, 2015; Semikron, 2015);

$$P_{cond,IGBT} = \frac{1}{T}\int_0^T (V_{CE0} i_C(t) + i_C^2(t) r_{CE}) dt \tag{4.23}$$

$$P_{cond,DIODE} = \frac{1}{T}\int_0^T (V_{F0} i_F(t) + i_F^2(t) r_F) dt \tag{4.24}$$

In order to calculate conduction losses, the empirical formulations have been proposed for conventional applications in the application notes of power semiconductor manufacturers (ABB, 2015; Fuji-Electric, 2015; Semikron, 2015). By estimating the average collector current of IGBT and forward current of freewheeling diode, the conduction losses of them can be easily calculated from Eqs. 4.25 and 4.26 respectively.

$$P_{cond,IGBT} = V_{CE0} i_{C,avg}^2 + i_{C,avg}^2 r_{CE} \tag{4.25}$$

$$P_{cond,DIODE} = V_{F0} i_{F,avg}^2 + i_{F,avg}^2 r_F \tag{4.26}$$

The switching losses of power semiconductors are the sum of turn-on energy, E_{ON} and turn-off energy, E_{OFF}. The switching power loss of IGBTs can be calculated from Eq. 4.27 as;

$$P_{sw,IGBT} = \left(E_{ON} + E_{OFF}\right) f_{sw} \tag{4.27}$$

The turn-on energy of the anti-parallel diodes can be neglected because of the low forward recovery energies of the fast anti-parallel diodes (Semikron, 2015). Only

the reverse recovery energy, E_{RR} is applied for the switching power loss of freewheeling diodes as follows;

$$P_{sw,DIODE} = E_{RR} f_{sw} \tag{4.28}$$

The power losses of one IGBT with freewheeling diode of SKM100GB12T4 used in SHAPF prototype are presented in Table 4.13 for different supply operating voltage values with different compensation cases. In order to calculate the conduction losses of IGBT and freewheeling diode, the average value of IGBT collector current, I_C and the average value of freewheeling diode forward current, I_F are calculated using the simulation results of SHAPF prototype obtained from MATLAB-Simulink. The collector emitter saturation voltage of IGBT, $V_{CE(sat)}$ and the forward voltage of freewheeling diode, V_F have been determined using related characteristic curves in the datasheet of SKM100GB12T4 according to the average values of I_C and I_F. The switching losses calculations have been performed by using the chosen switching frequency of 10kHz. The gate turn-on resistance, R_{Gon} and the gate turn-off resistance, R_{Goff} have been chosen 10Ω for SKM100GB12T4. E_{ON} and E_{OFF} values of IGBT given in the datasheet of SKM100GB12T4 have been scaled for switching loss calculations with respect to the operation values of V_{CE} and I_{CE}, and the chosen values of R_{Gon} and R_{Goff}. Additionally, E_{RR} value of freewheeling diode have been scaled with respect to the operation values of V_F and I_F. It is shown in Table 4.13 that the total power loss of one IGBT with freewheeling diode in SHAPF prototype can reach 136.1W. The total power loss of VSC can reach 816.5W. By considering overloading conditions, 10% safety margin is added to the maximum power losses of IGBT and freewheeling diode so that the maximum power losses of IGBT and freewheeling diode are taken for thermal loss calculations as 128.2W and 21.6W respectively.

Table 4.13. Thermal power losses of SHAPF prototype in different cases

Cases	Total Power Losses (W)			
	IGBT	Diode	IGBT + Diode	VSC
Case 1 - Only Har. Comp.@ 400V *Max. Har. Comp. Current Val.: See Table 4.2* *Approximate Reactive Power Comp Rating: Qpf* *Max. Supply Harmonic Voltage : -*	25.3	7.8	33.1	198.6
Case 2 - Har. & Reac. Power. Comp. @ 400V *Max. Har. Comp. Current Val.: See Table 4.2* *Approximate Reactive Power Comp Rating: 7kVAr* *Max. Supply Harmonic Voltage : -*	71.4	12.4	83.8	502.6
Case 3 - Har. & Reac. Power. Comp. @ 400V *Max. Har. Comp. Current Val.: See Table 4.2* *Approximate Reactive Power Comp Rating: 13kVAr* *Max. Supply Harmonic Voltage : -*	64.1	12.7	76.8	460.8
Case 4 - Har. & Reac. Power. Comp. with Exsistance of Vol .Har. @ 400V *Max. Har. Comp. Current Val.: See Table 4.2* *Approximate Reactive Power Comp Rating: 7kVAr* *Max. Supply Harmonic Voltage : - See Table 4.7*	78.2	13.4	91.5	549.1
Case 5 - Har. & Reac. Power. Comp. with Exsistance of Vol .Har. @ 400V *Max. Har. Comp. Current Val.: See Table 4.2* *Approximate Reactive Power Comp Rating: 13kVAr* *Max. Supply Harmonic Voltage : - See Table 4.7*	71.8	13.8	85.6	513.5
Case 6 - Only Har. Comp.@ 360V *Max. Har. Comp. Current Val.: See Table 4.2* *Approximate Reactive Power Comp Rating: Qpf* *Max. Supply Harmonic Voltage : -*	52.5	10.7	63.2	379.0
Case 7 - Har. & Reac. Power. Comp. @ 360V *Max. Har. Comp. Current Val.: See Table 4.2* *Approximate Reactive Power Comp Rating: 7kVAr* *Max. Supply Harmonic Voltage : -*	39.2	8.9	48.1	288.6
Case 8 - Har. & Reac. Power. Comp. @ 360V *Max. Har. Comp. Current Val.: See Table 4.2* *Approximate Reactive Power Comp Rating: 13kVAr* *Max. Supply Harmonic Voltage : -*	112.2	18.9	131.1	786.3

Table 4.13. Thermal power losses of SHAPF prototype in different cases (cont.)

Cases	Total Power Losses (W)			
	IGBT	Diode	IGBT + Diode	VSC
Case 9 - Har. & Reac. Power. Comp. with Exsistance of Vol .Har. @ 360V *Max. Har. Comp. Current Val.: See Table 4.2* *Approximate Reactive Power Comp Rating: 7kVAr* *Max. Supply Harmonic Voltage : - See Table 4.7*	50.8	10.4	61.2	367
Case 10 - Har. & Reac. Power. Comp. with Exsistance of Vol .Har. @ 360V *Max. Har. Comp. Current Val.: See Table 4.2* *Approximate Reactive Power Comp Rating: 13kVAr* *Max. Supply Harmonic Voltage : - See Table 4.7*	116.5	19.6	136.1	816.5
Case 11 - Only Har. Comp.@ 440V *Max. Har. Comp. Current Val.: See Table 4.2Approximate Reactive Power Comp Rating: Qpf* *Max. Supply Harmonic Voltage : -*	48.1	10.7	58.8	352.7
Case 12 - Har. & Reac. Power. Comp. @ 440V *Max. Har. Comp. Current Val.: See Table 4.2* *Approximate Reactive Power Comp Rating: 7kVAr* *Max. Supply Harmonic Voltage : -*	103.4	16.1	119.5	717.2
Case 13 - Har. & Reac. Power. Comp. @ 440V *Max. Har. Comp. Current Val.: See Table 4.2* *Approximate Reactive Power Comp Rating: 13kVAr* *Max. Supply Harmonic Voltage : -*	28.3	8.4	36.7	220.3
Case 14 - Har. & Reac. Power. Comp. with Exsistance of Vol .Har. @ 440V *Max. Har. Comp. Current Val.: See Table 4.2* *Approximate Reactive Power Comp Rating: 7kVAr* *Max. Supply Harmonic Voltage : - See Table 4.7*	108.3	16.9	125.3	751.7
Case 15 - Har. & Reac. Power. Comp. with Exsistance of Vol .Har. @ 440V *Max. Har. Comp. Current Val.: See Table 4.2* *Approximate Reactive Power Comp Rating: 13kVAr* *Max. Supply Harmonic Voltage : - See Table 4.7*	43.3	10.3	53.5	321.2

Three SKM100GB12T4 IGBT modules have been used for VSC of SHAPF prototype. The thermal calculations have been performed by considering that these three modules have been mounted on one common heatsink. In order to determine heatsink specifications, the thermal model of VSC with heatsink shown in Figure 4.7 can be used. The thermal resistance values of SKM100GB12T4 IGBT module are given in Table 4.14.

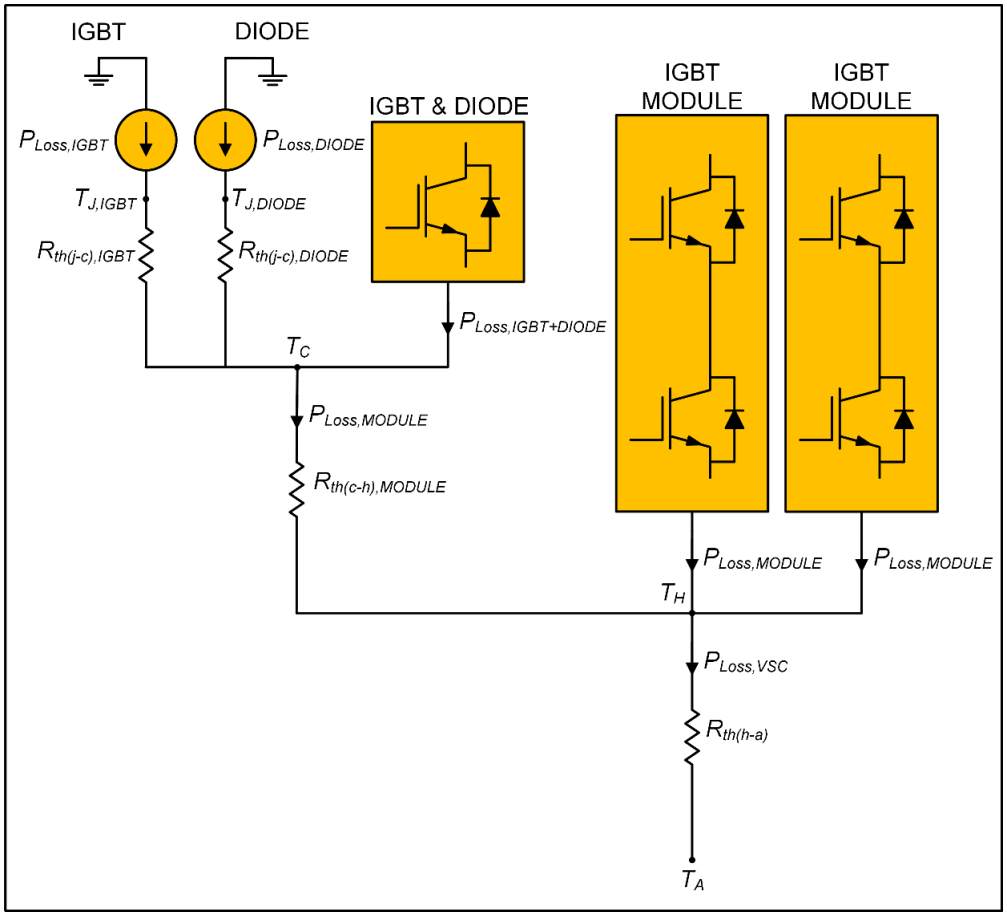


Figure 4.7. Thermal model of three phase VSC

Table 4.14. Thermal resistance values of SKM100GB12T4 IGBT module (Semikron, 2013)

Thermal Resistance	Value
IGBT Junction to Case Thermal Resistance ($R_{th(j-c),IGBT}$)	0.27 °C/W
Diode Junction to Case Thermal Resistance ($R_{th(j-c),Diode}$)	0.48 °C/W
Module Case to Heatsink Thermal Resistance ($R_{th(c-h)}$)	0.05 °C/W

The junction temperature, T_J of SKM100GB12T4 should not exceed 150°C for the safe operation of module. In order to select a proper heatsink for SHAPF prototype, the heatsink to ambient thermal resistance of heatsink is calculated from Eq. 4.29 as (Çetin, 2007);

$$R_{ha} = \frac{T_J - T_A - R_{th(c-h)} P_{MODULE} - \max\left(P_{Loss,IGBT} R_{th(j-c),IGBT}, P_{Loss,DIODE} R_{th(j-c),DIODE}\right)}{P_{Loss,VSC}} \quad (4.29)$$

By assuming T_J is equal to 150°C and T_A is equal to 40°C, the maximum value of heatsink thermal resistance is calculated as 0.067 C/W. This thermal resistance specification of heatsink have been satisfied with using P3-300 heatsink model from Semikron. The natural air cooing thermal resistance of P3-300 is 0.24 C/W for three IGBT module. The thermal resistance of P3-300 can be decreased to 0.06 C/W for three IGBT module by forced air cooling with the air flow rate of 10m/s. This air flow rate have been obtained with mounting axial fan on the chosen heatsink.

4.3.2.4. Design of DC Link Busbar and Power Stage Layout

The fast switching behavior of IGBTs cause the high instantaneous rate in current over time (*di/dt*) at turn-off operation. Due to the inductance of the current commutation loop, *di/dt* value results in high voltage spike across the collector -emitter terminals of IGBT. Therefore, the inductance of the current commutation loop should be kept under certain limits. The inductance of the current commutation loop is mainly formed from the internal inductance of IGBTs, the equivalent series inductance of dc link capacitors and the inductance of dc link connection wires or busbars. In today's technology, the internal inductance of IGBTs and the equivalent series inductance of dc link capacitors can be manufactured in low levels so the inductance of dc link connections become a decisive parameter of the commutation loop inductance. The laminated busbar systems are the state of art for dc link connections of the high power

systems. The laminated busbar systems connect the entire power system together and achieves the lowest possible dc link commutation loop inductance (Allocco, 1998).

The low inductance laminated busbar design can be achieved with using following design criterions (Beukes et al., 1997; Caponet et al., 2002; Çetin, 2007);

- The surface area of busbars should be as large as possible.
- The distance between busbars should be as small as possible.
- The thickness of busbars should be as small as possible.
- The length of current flow path should be as short as possible.
- The current flow distribution on busbars should be as uniform as possible.
- The current frequency should be as high as possible.

Because of the shapes of busbars and the connection holes on them, the laminated busbar systems do not have uniform models. The certain electrical specifications of laminated busbar systems can be determined by complex computer based numerical analysis methods. However, the approximate electrical specifications can be calculated by neglected connection holes and assuming the shape of busbars uniform. A laminated busbar system formed from two uniform shape busbar is demonstrated in Figure 4.8. In Figure 4.8, *t* denotes the thickness of busbar, *w* denotes the width of busbars, *l* is the length of busbar along current flow path and *d* denotes the distance between busbars.

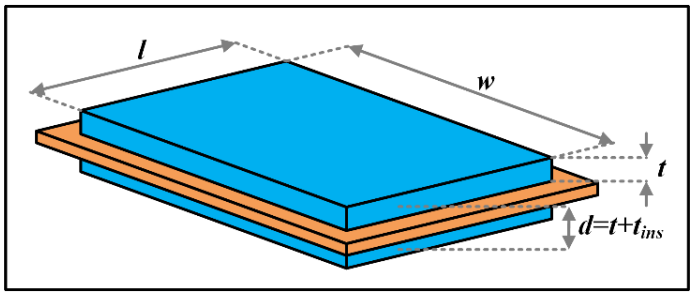


Figure 4.8. Representation of a laminated busbar system

The inductance of laminated busbar system consists of self-inductance and mutual inductance. The self-inductance which is a result of flux linkages within a conductor is frequency dependent due to the skin and proximity effects. The self-inductance of laminated busbar system shown in Figure 4.8 can be calculated with Eq. 4.30 as (Caponet et al., 2002);

$$L_s = \frac{\mu_0 \mu_r}{8\pi} l \ (H) \tag{4.30}$$

where

μ_0 is the magnetic permeability of free space

μ_r is the relative magnetic permeability of material

The mutual inductance can be defined as a flux linkage per unit current with one conductor to another. It is dependent to the geometry of conductors. By assuming $d<<2t$, $d<<t+w$ and $t<<w$, the mutual inductance between busbars can be calculated with Eq.4.35 as (Caponet et al., 2002);

$$L_m = 2\mu_0 \mu_r \frac{t.l}{\pi\left(t+w\right)} \ (H) \tag{4.31}$$

The total inductance is equal to sum of self and mutual inductances as;

$$L_t = L_s + L_m \tag{4.32}$$

The capacitance of laminated busbar system is dependent on the type and thickness of dielectric material and the surface area of busbars. It can be calculated with Eq. 4.33 as (Caponet et al., 2002);

$$C = \varepsilon_0 \varepsilon_r \frac{w.l}{t_{ins}} \ (F) \tag{4.33}$$

where

ε_0 is the permittivity of free space

ε_r is the relative permittivity of material

The dc resistance of laminated busbar system can be calculated from Eq. 4.34 as (Caponet et al., 2002);

$$R_{dc} = \rho \frac{2.l}{w.t} \ (\Omega) \tag{4.34}$$

where

ρ is the specific electrical resistance of material

In the high frequency operations, the skin depth, δ should be considered for the resistance calculations. The skin depth can be calculated from Eq. 4.35 as;

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0}} \ (m) \tag{4.35}$$

The ac resistance of laminated busbar system can be calculated for $t>2\delta$ from Eq. 4.36 as (Caponet et al., 2002);

$$R_{ac} = \rho \frac{4.l}{w.\delta} \ (\Omega) \tag{4.36}$$

The current carrying capacity of conductor is related with geometry of conductor, the power loss dissipated through resistance of conductor and the allowable operating temperature. In the practical design considerations, the minimum current carrying capacities of conductors are assumed as $2A/mm^2$ for copper conductors and $1A/mm^2$ for aluminum conductors. The skin effect should be taken in consideration for the high frequency ac operations.

In order to provide the connections of the dc link capacitor bank and VSC in SHAPF prototype, the laminated busbar system have been designed with three busbars as demonstrated in Figure 4.9. These busbars are named as positive busbar, negative busbar and midpoint busbar. The positive busbar provides the connection between positive side of VSC and dc link capacitor bank. Similarly, the negative busbar provides the connection between the negative side of VSC and the capacitors of dc link capacitor bank. The midpoint busbar provides the series connection between each parallel branch of the dc link capacitor bank and connects the midpoints of parallel branches together.

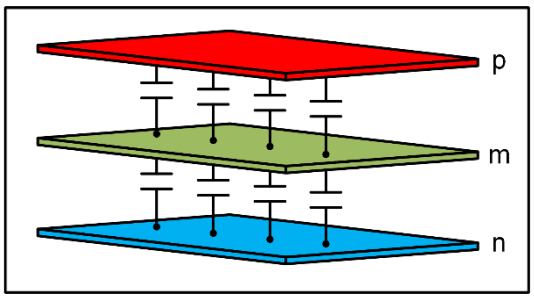


Figure 4.9. Demonstration of dc link capacitor bank of SHAPF prototype with laminated busbars

In ideal conditions, the electrical potential between any two points of midpoint busbar is equal to zero so the midpoint busbar is an equipotential surface through which a current does not flow and its impedance is equal to zero. In practical situations, there is negligible flow because of the capacitance tolerances of the dc link capacitors. Thus, the midpoint busbar can be assumed as equipotential surface and its impedance can be assumed as zero. In the design studies of dc link busbar of SHAPF prototype, the laminated busbar design of SHAPF prototype is performed according to the calculations of two busbar system shown in Figure 4.8. By assuming the middle busbar has no mutual inductance, the positive busbar has been placed to the top of the busbars, the negative busbar has been placed to the middle of the busbars and the midpoint busbar is the bottom of the busbars as demonstrated in Figure 4.10 to minimize the inductance of laminated busbar system of SHAPF prototype.

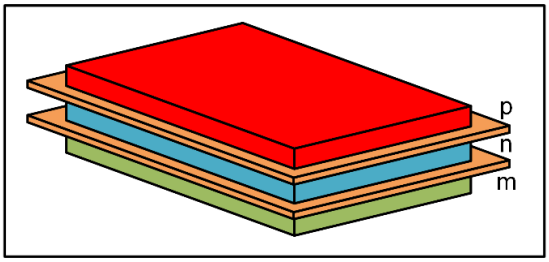


Figure 4.10. Layout of busbars in laminated busbar system of SHAPF prototype

The power stage layout and the laminated busbar design of SHAPF prototype have been performed with a computer aided design (CAD) program. The ac busbars are also designed with laminated busbar system to ensure the safety and reliable ac connections for VSC. The top views of the power stage layout of SHAPF prototype and the designed laminated busbar system are shown in Figure 4.11. The designed laminated busbar system of SHAPF prototype has been implemented using aluminum plate instead of copper plate because of the low cost and the high resistant to corrosion and oxidation specifications of the aluminum material. The thickness of aluminum plate is chosen 2mm for the implementation of busbars. The insulation between busbars is achieved with using Trivoltherm series aramid paper from Krempel which has 0.36mm thickness.

The geometrical specifications and the calculated inductance values of the designed laminated busbar are given in Table 4.15. The total inductance of the dc link current commutation loop is calculated as given in Table 4.16.

Table 4.15. Laminated busbar specifications of SHAPF prototype

Busbar Specifications	**Values**
Busbar Width (w)	360mm
Busbar length (l)	280mm
Busbar Thickness (t)	2mm
Insulator Thickness (d)	0.36mm
Relative Magnetic permeability of Busbar Material (μ_r)	Aluminum $\mu_r = 1.000022$
Self-Inductance Value (L_s)	14nH
Mutual Inductance Value (L_m)	1.24nH
Total Inductance Value ($L_t = L_s + L_m$)	15.24nH

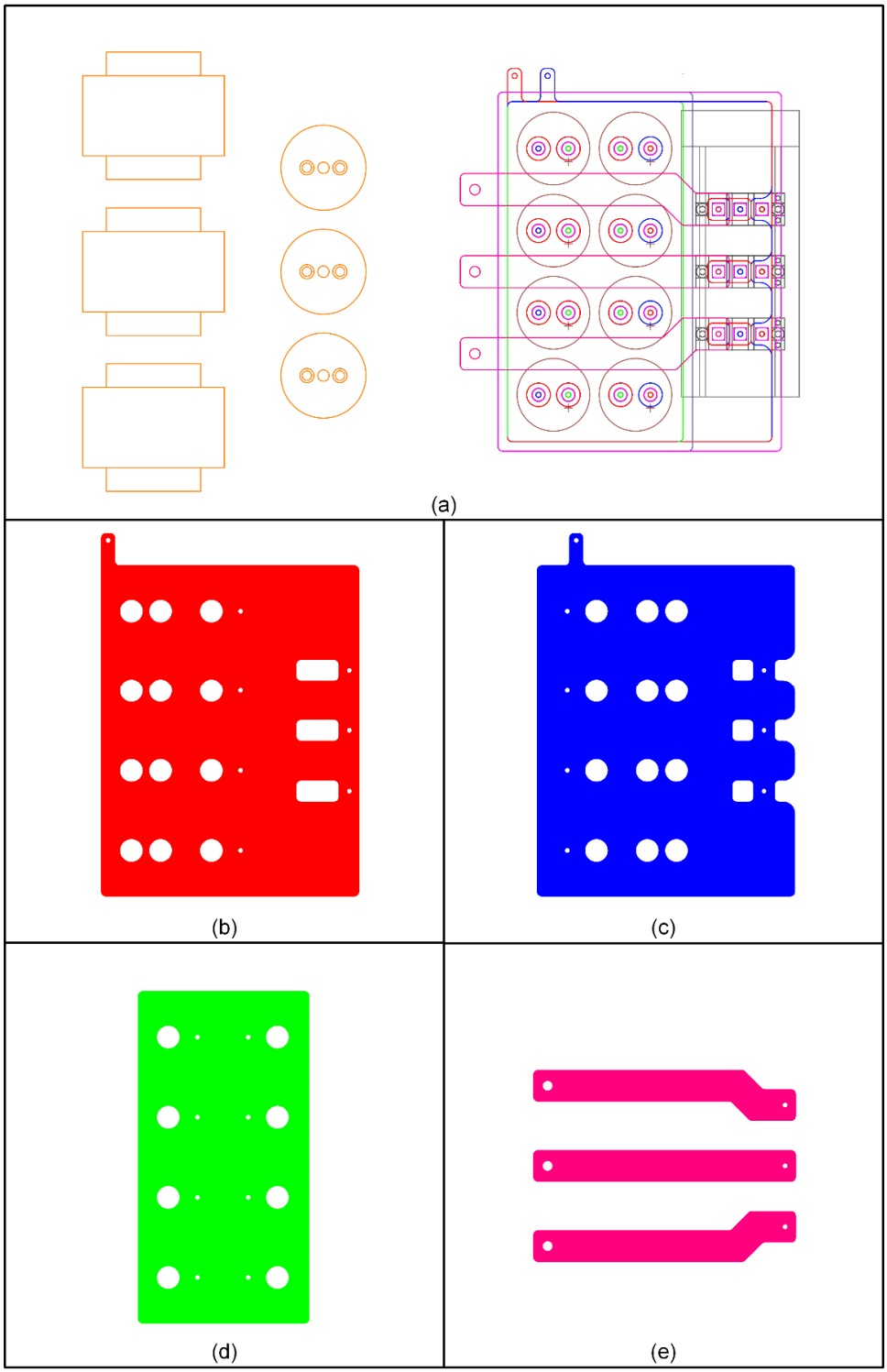


Figure 4.11. Power stage and laminated busbar system layout of SHAPF prototype
(a) Power stage layout (b) Positive busbar layout (c) Negative busbar layout
(d) Midpoint busbar layout (e) AC busbars layout

Table 4.16. Inductance calculation of dc link current commutation loop

Total Inductance of Laminated Busbar	15.24nH
Total ESL of DC link Capacitor Bank (2 Series Capacitor in 4 Parallel Branch)	20nH
Internal Inductance of IGBT Modules	30nH
Inductance of Mounting Connections (Screw, Washer, Spacer, etc.)	≈20nH
Total Inductance of DC Link Current Commutation Loop	85.24nH

The maximum magnitude of voltage spike on V_{CE} of IGBT can be calculated using dc link commutation inductance, the maximum turn-off current, the minimum turn-off time and the maximum value of V_{dc} as given in Eq. 4.37. The turn-off current waveforms of IGBTs in SHAPF prototype is investigated with simulation studies. It is observed from the simulation results that the turn-off currents of IGBTs can reach 80A in transient conditions. The minimum turn-off time has been determined 200ns for SKM100GB12T4 and the chosen gate turn- off resistor. The maximum dc link voltage is determined 400V in Section 4.3.2.1. Therefore, the maximum magnitude of voltage spike on IGBTs of SHAPF prototype is calculated 434V. The calculated magnitude for voltages spike is far below V_{CE} of SKM100GB12T4 IGBT modules. Thus, it is not necessary to use snubber circuits in VSC of SHAPF prototype.

$$V_{CEp} = V_{dc} - L_t \frac{\Delta i_{C,turn-off}}{\Delta t} \tag{4.37}$$

$$V_{CEp} = 400 + 85.24x10^{-9} \frac{80}{200x10^{-9}} \cong 434V$$

4.4. Design of Electronic Control System

4.4.1. General Design Considerations

The performance and operation safety of SHAPF prototype directly depends on the electronic control system. The required voltage and currents signals for the controller of SHAPF must be measured in high accuracy and the gate signals must be generated in high resolution to achieve the best compensation and efficiency performance. In addition, the electronic control system must have protection function for the safety operation of SHAPF prototype. Moreover, isolated digital input/output (I/O) circuits should exist in the electronic control system for the external control-command signals.

The block diagram of SHAPF prototype's electronic control system is demonstrated in Figure 4.12. The main parts of the electronic control system are digital signal processor (DSP) based microcontroller unit (MCU), measurement circuits, analog protection and fault detection circuits, digital I/O circuits, firing circuits and isolated digital I/O circuits.

The DSP based MCU can be assumed as the heart of the electronic control system. Although single DSPs have higher performance than DSP based MCUs in market, DSP based MCUs present great advantage in the simplification of electronic control system design with their peripherals such as, analog to digital converter (ADC) and pulse with modulation (PWM) units.

The electronic control system of SHAPF prototype should measure 10 voltage and current signals including dc link voltage, 3 supply voltages, 3 source currents and 3 SHAPF currents for the controller. The measurement circuits make signal conditioning of the measured signals for ADC of MCU. The measurement circuits should be designed with high accuracy sensors and precision amplifiers for the performance of SHAPF prototype.

The analog protection circuits are required for the secondary protection of SHAPF prototype in addition to the software protection realized by MCU. The fault detection circuits are required to latch fault signals obtained from analog protection

circuits, MCU and firing circuits, and generated trip signal to stop the operation of system.

The digital I/O circuits are required for the level transition between MCU logic voltage level and the logic voltage level of electronic control system. The most of the high performance MCU's logic voltage level is 3.3V or below than this level. The electronic control system should be nearby the power circuit of SHAPF prototype to transmit the switching signal with the lowest distance. The switching of power devices in SHAPF prototype can cause electromagnetic interference (EMI) problems which effect the operation of electronic control system. EMI problems such as noise or voltage glitches can be formed on the logic signals which have long traces along printed circuit board (PCB). In 5V logic voltage level, logic high and logic low voltage levels have wider voltage band than 3.3V or below voltage levels. Thus, logic level is selected 5V, in order to increase noise immunity of electronic control system.

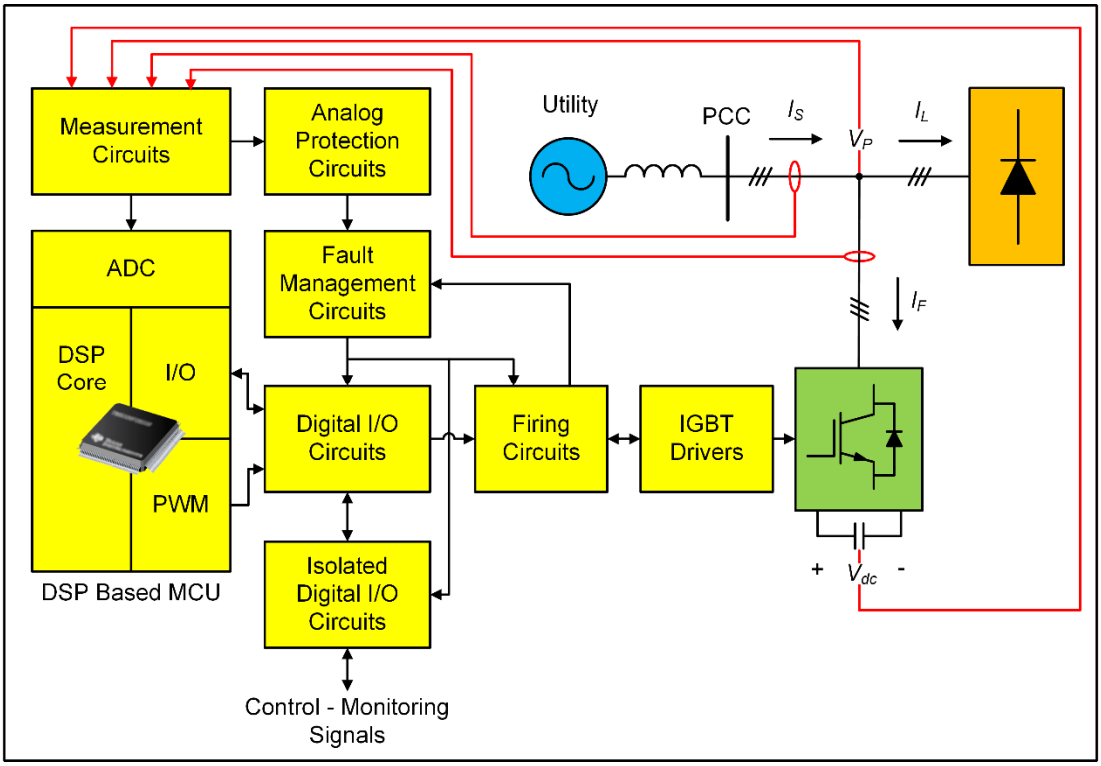


Figure 4.12. Block diagram of electronic control system

The firing circuit transmits the switching signals to IGBT drivers and receive the fault signals of IGBT drivers. The chosen IGBT drivers have 15V logic voltage level so that the firing circuits should provide voltage level transition between 5V logic voltage level of electronic card system and 15V logic voltage level of IGBT drivers.

The isolated digital I/O circuits are used to perform voltage level transition and isolation between 24V control and monitoring signals and 5V logic signals of electronic control system.

The details of electronic control system is introduced in following sections.

4.4.2. Selection of Digital Signal Processor Based Microcontroller Unit

The DSP based MCU which will be used in the electronic control system of SHAPF prototype should provide following key requirements;

- The operating cycle rate of MCU should allow to realize the controller operation of SHAPF prototype including ADC conversion process, control algorithm, protection software and switching signal generation lower than 100μs for real time operation.
- MCU should contain high performance peripheral modules. Especially, the technical specifications of ADC and PWM modules should ensure the real time operation of MCU for SHAPF prototype.
- MCU should contain hardware mathematical calculation units such as floating point unit in order to shorten the operating cycle of mathematical calculations in the control algorithm of SHAPF prototype.
- MCU should support the real time debugging specifications with emulators in order to observe the controller algorithm of SHAPF prototype.
- MCU should have adequate memory for the controller software and the required data of SHAPF prototype.
- MCU should have software support with optimized mathematical and peripheral libraries.

The base technical specifications in Table 4.17 have been determined for the selection of DSP based MCU. By considering these specifications, the product portfolios of leading DSP based MCU manufacturers such as Texas Instrument, Analog Devices, STM Electronics have been investigated. Finally, TMS320F28335 Delfino Series DSP based MCU of Texas Instrument is chosen due to being preferred in many power electronics applications and wide library and application note resource support. The technical specifications TMS320F28335 are given in APPENDIX D (Texas-Instruments, 2015).

Table 4.17. Technical specifications for selection of DSP based MCU

CPU Specifications	
Clock Frequency	≥ 100MHz
Cycle Time	≤ 10ns
Floating Point Unit	Yes
Memory Specifications	
RAM	≥ 32KB
Flash Memory	≥ 128KB
ADC Specifications	
Channel Number	≥ 10
Resolution	≥ 10bit
Sample Rate	≥ 10MSPS
Conversion Time	≤ 100ns
PWM Specifications	
Channel Number	≥ 6
Resolution	≥ 12bit

Instead of IC package versions, the control card version of TMS320F28335 which has DIMM 100 connection interface has been chosen for the electronic control system of SHAPF prototype. The control card version of TMS320F38335 contains auxiliary circuitries for peripheral modules, boot options and emulator connections. Thanks to the control card version of TMS320F38335, the development process of electronic control system have been simplified and shortened.

4.4.3. Design of Measurement Circuits

In SHAPF prototype, 10 power circuit signals including dc link voltage, 3 grid voltages, 3 supply side currents and 3 SHAPF currents should be measured for the control and protection algorithms. The measurement circuits are responsible from the signal conditioning of power circuit voltage and current signals for ADC inputs of the chosen MCU.

The power circuit signals are transformed into measurement signals by voltage and current sensors. Voltage and current sensors are the most important part of the measurement circuit because their sensitivities and accuracies directly affect the performance of SHAPF prototype. Another important parameter for sensors are the measurement frequency bandwidth. In order to compensate harmonic currents in sufficient performance, especially current sensors should perform the measurement of high frequency components. By considering these requirements, LV 25-P voltage sensor from LEM and CTF-50A current sensor from MULTIMIC have been selected for the measurement circuits. The detailed technical specifications of the chosen sensors are presented in Appendix E.

The block diagram of dc link voltage measurement circuit is given in Figure 4.13. The dc link voltage measurement circuit is mainly formed from voltage sensor, non-inverting amplifier and ADC driver circuit which consists of a voltage follower and RC low pass filter. The dc link voltage measurement range is determined as 0-500V. LV25-P sensor operates with respect to current measurement principle. The measured voltage is converted to current quantity by the primary side resistor, R_P. This current proportional to the measured voltage is transformed into secondary current with the transformation ratio of sensor. The secondary side current is transformed into a single ended signal with connecting a measurement resistor, R_M. This voltage signal is conditioned with non-inverting amplifier to 0-3V ADC input range of the chosen MCU. The voltage follower in ADC driver circuit provides a low impedance source to charge the sample capacitor in ADC. RC filter provides immunity to noise. Resistor restricts the charge current of sample capacitor and capacitor helps to improve signal stability at the input of ADC (Texas-Instruments, 2008).

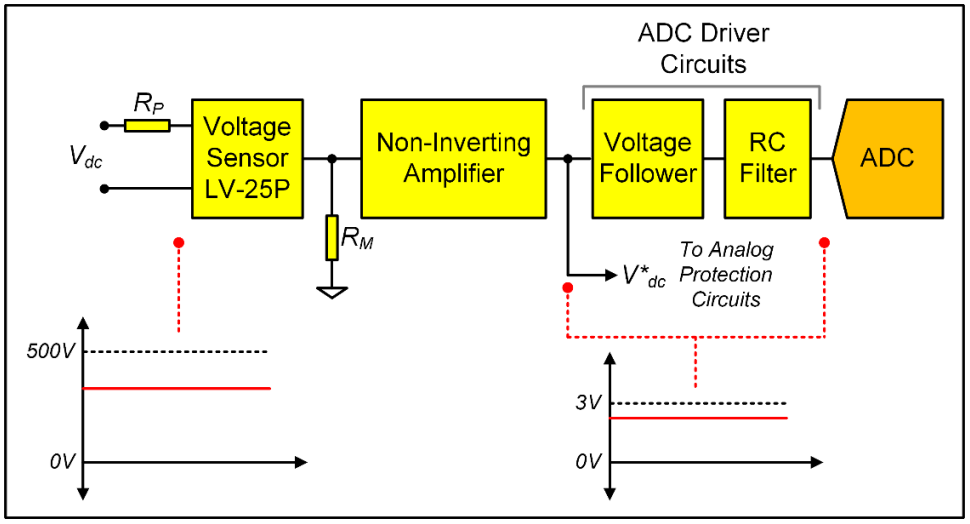


Figure 4.13. Block diagram of dc link voltage measurement circuit

The grid voltage measurement circuits whose block diagram is given in Figure 4.14 show similarity in large ratio with dc link measurement circuit except non-inverting summing amplifier and offset voltage circuit. The measuring range of grid voltage signals are determined as ±370V peak. The grid voltage signals are bipolar signals and the measurement range of the chosen MCU's ADC is in unipolar range. Therefore, the bipolar input signals should be conditioned to 0-3V input range of ADC with gain adjustment and offset adding. The grid voltage measurement signal is adjusted in the range of ±1.5V peak with non-inverting amplifier. The non-inverting summing amplifier adds the measurement signal obtained from non-inverting amplifier with 1.5V offset voltage, V_{OFF} generated from the offset voltage circuit to obtain unipolar ADC input voltage. The offset voltage circuit consists of 1.5V precision voltage reference and voltage follower.

The source side current and SHAPF current measurement circuits have same design logic with voltage measurement circuits due to being bipolar current signals. However, the chosen current sensor, CTF-50A is a type of ferrite core current transformer and its output is differential ended current signal. Because of these, the current measurement circuit whose block diagram is shown in Figure 4.15 is mainly formed from differential amplifier, inverting amplifier, non-inverting summing amplifier with offset signal and ADC driver circuit. The measurement range of source side current and SHAPF current is selected ±70A peak. The output current of current

sensor is converted to differential ended voltage signal on measurement resistors. The gain adjustment of measurement signal is performed with differential and inverting amplifiers. At the output of inverting amplifier, ±70A peak current signal is conditioned to ±1.5V peak. In order to condition ±1.5V peak measurement signal to 0-3V ADC input signal, 1.5V offset signal is added by non-inverting summing amplifier. Finally, ADC driver circuit transmits the conditioned measurement signal to ADC.

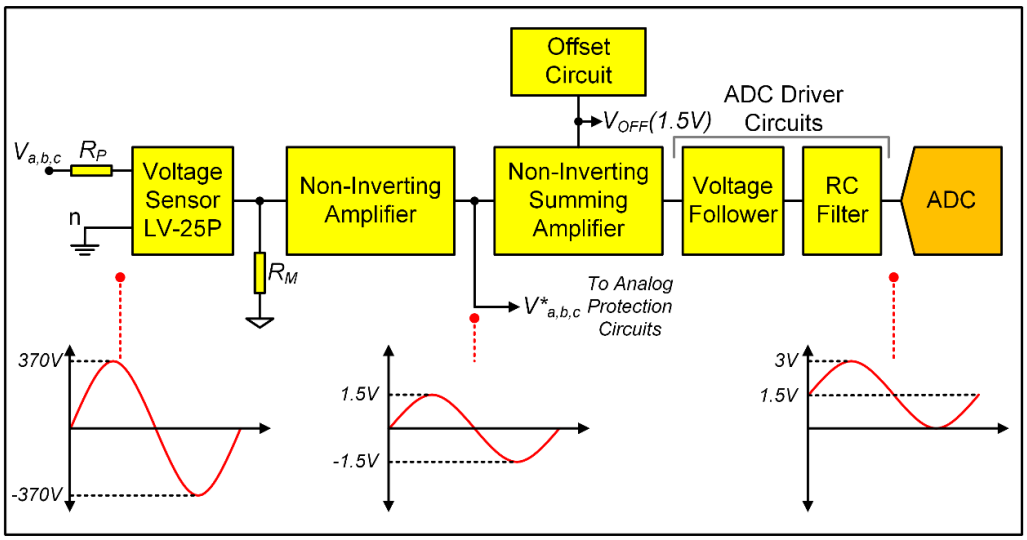


Figure 4.14. Block diagram of grid voltage measurement circuit

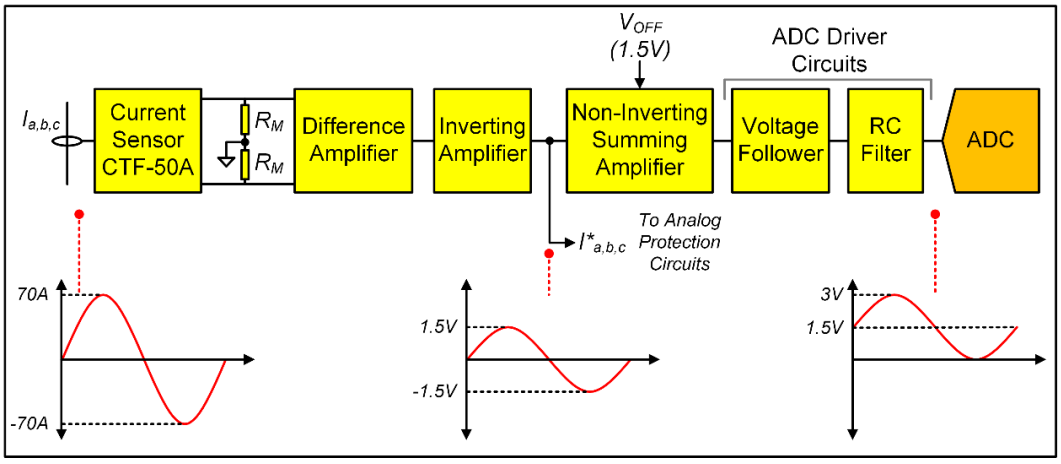


Figure 4.15. Block diagram of supply and SHAPF current measurement circuits

4.4.4. Design of Analog Protection and Fault Management Circuits

Analog protection circuits are used to provide a secondary protection for the possible transient and overvoltage/over current problems in dc link voltage, grid voltage and SHAPF current in addition to the software protection performed by MCU. The block diagrams of analog protection circuits for dc link voltage and for grid voltages and SHAPF currents are given in Figure 4.16. The analog protection circuits are mainly formed from a fault voltage level circuit and comparator. The fault voltage level circuit consists of simple resistive voltage divider circuit with trimmer potentiometers. Additionally a precision rectifier is used in analog protection circuits of grid voltages and SHAPF currents for the rectification of ac signals to catch-up over voltages and/or over currents in negative cycles of the measured signals immediately. In the electronic control system of SHAPF prototype, fault signals are generated with negative logic. Analog protection circuits generate a negative logic pulse signal to fault detection circuits in the output of comparators if the peak value of measured signals exceed the fault set voltage levels. Analog protection circuits of dc link voltage and grid voltages take the measured signals from the output non-inverting amplifier in voltage measurement circuits. Analog protection circuits of SHAPF currents take the measured signals from the output of the inverting amplifier in current measurement circuits.

Fault management circuits control the fault logic of electronic control system. They have three main functions. These are latching of the fault signals coming from analog protection circuits, MCU and firing circuits, resetting of the latched fault signals if the fault signals are removed and generating trip signal to stop the operation of SHAPF power circuit. The block diagram of fault management circuits is presented in Figure 4.17. They are mainly formed from fault latch and reset circuits and trip signal generation circuits. The fault latch and reset circuits are used for each of fault signals. The operation logic of fault latch and reset circuits is provided with a NAND logic gate and negative logic RS Latch IC. In order to indicate fault signals, a LED with resistor is connected to output of RS Latch IC. Trip signal generation circuits

consist of AND logic gates to generate trip signals with using the fault signals taken from each of fault latch circuits.

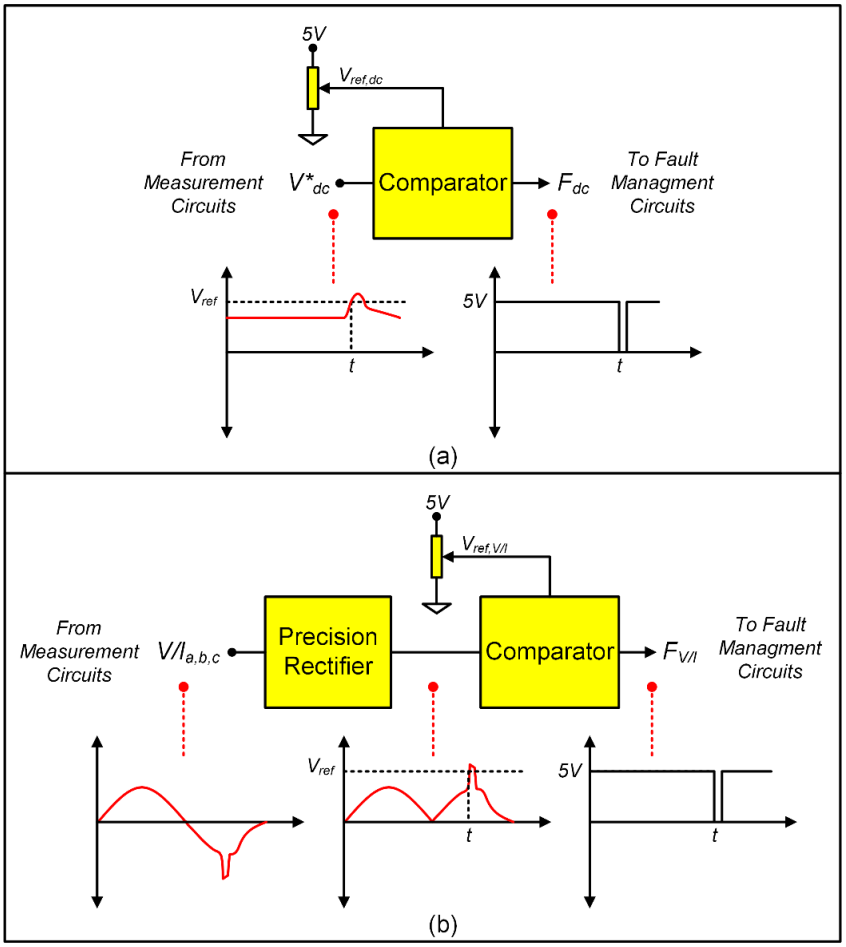


Figure 4.16. Block diagrams of analog protection circuits
(a) DC link voltage protection circuit
(b) Grid voltage and SHAPF current protection circuits

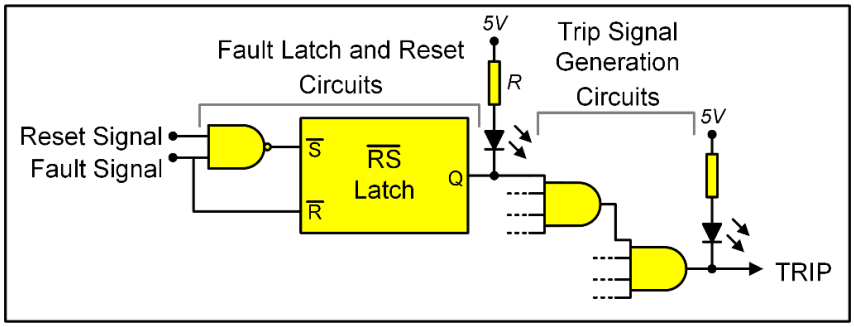


Figure 4.17. Block diagram of fault management circuits

4.4.5. Design of Digital I/O Circuits

Electronic control system of SHAPF prototype has different digital I/O voltage levels for MCU, the digital circuits on electronic control system and, the external control and signals. The block diagram of digital I/O circuits for voltage level transition of input and output signals between MCU and digital circuits of electronic control system are illustrated in Figure 4.18. It is shown from Figure 4.18 that the voltage level transitions between 3.3V digital I/O voltage level of MCU and 5V digital I/O voltage level of the digital circuits are provided with using bus transceiver ICs. The bus transceiver ICs can translate the voltage level below 10ns propagation time which has negligible effect on electronic control system.

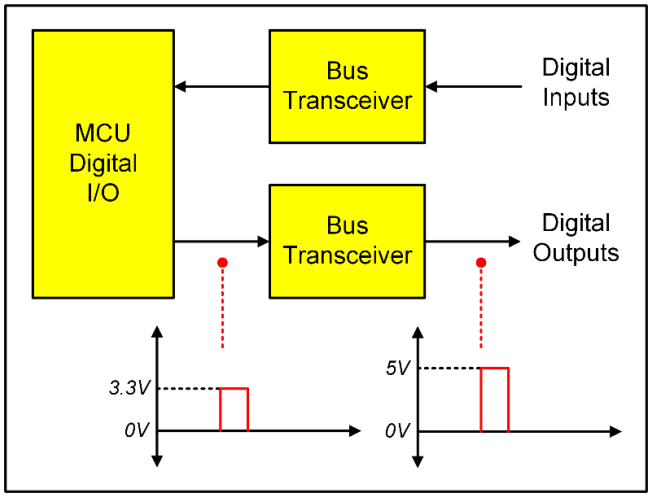


Figure 4.18. Block diagram of digital I/O circuits

The voltage level transition between the digital circuits and the external control-command signals are realized with isolation to protect electronic control system from the possible external faults on control-command signals. The block diagram of digital I/O circuits for voltage level transition of input and output signals between the command-control circuits and digital circuits of electronic control system are illustrated in Figure 4.19. The voltage level transition between 24V digital I/O voltage level of control-command signals and 5V digital I/O voltage level of the digital circuits are provided using optocouplers for the isolation between two circuits. The

current rating of the most of the optocoupler ICs are below under 100mA. In order to drive relays or contactors with 24V output signals of electronic control system, a power amplifier realized with a single bipolar junction transistor is connected to output of each optocoupler. In order to observe 24V input and output signals on electronic control system, LED indicator circuits are used for all 24V input and output signals.

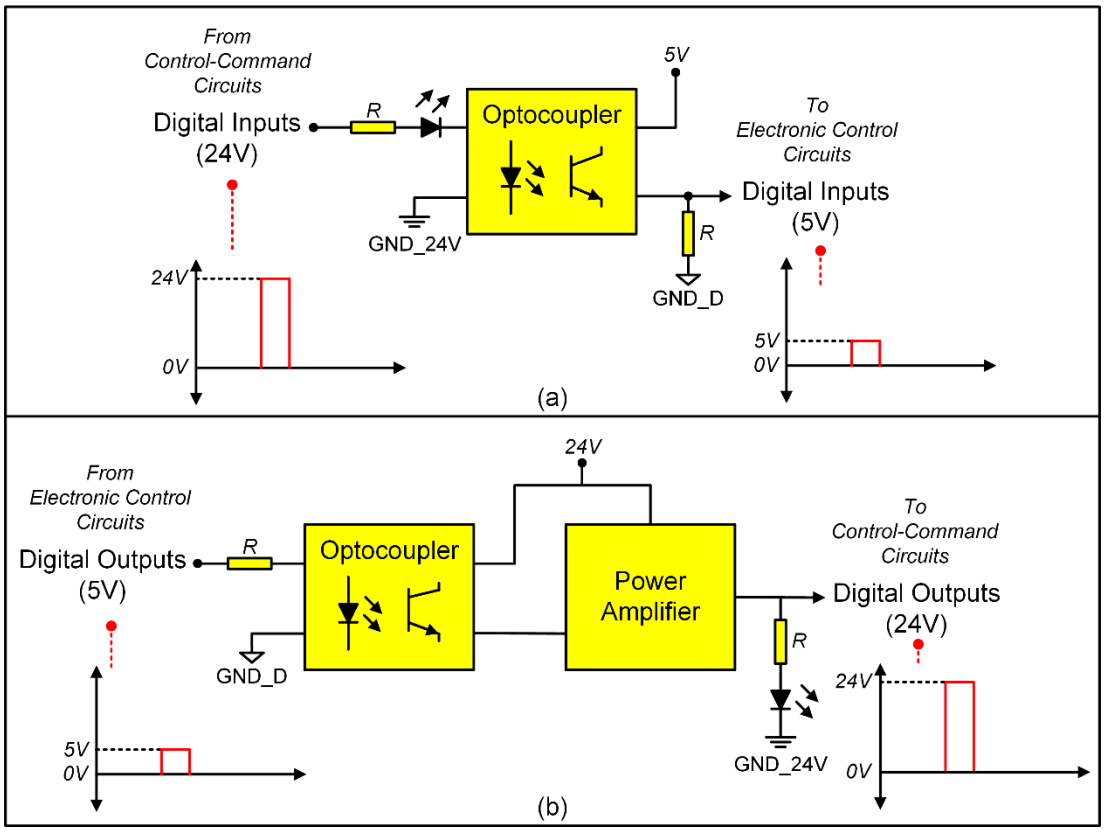


Figure 4.19. Block diagram of isolated digital I/O circuits
(a) Isolated digital input circuits
(b) Isolated digital output circuits

4.4.6. Design of Firing Circuits

The main functions of firing circuits are to transmit PWM signals by shifting the voltage level of signals from 5V to 15V and receiving the fault signals of IGBT driver by decreasing the voltage level of fault signal of IGBT driver from 15V to 5V. Additionally, IGBT driver and electronic control system are supplied from the same power supply and they share the same ground. In order to prevent ground loop

problems between IGBT driver and electronic control system, firing circuits perform isolation between two systems.

The block diagram of firing circuit for one leg of VSC is introduced in Figure 4.20. In the turn-on, turn-off and trip procedures of SHAPF prototype, VSC part should maintain a star point for PF by turning on upper or lower IGBTs of VSC. Otherwise, the dc link capacitor bank of VSC is instantaneously charged near to the peak value of grid line voltage over freewheeling diodes of IGBT modules. This problem can be solved with the software of MCU. However, it has been decided to control the switching of IGBTs in the turn-on, turn-off and trip procedures with the hardware for the safe operation of SHAPF prototype. In order to prevent this problem, switching control circuit is designed using logic gates. The switching control circuit turns on the top IGBTs and turns-on the bottom IGBTs of VSC to create star point when "PWM_RUN" signal is low logic and "TRIP" signal is high logic (no trip exists) or "TRIP" signal is low logic (trip exists). PWM signals generated by MCU are transmitted to IGBT drivers only if "PWM_RUN" signal is high logic and "TRIP" signal is high logic (no trip exists). "PWM_RUN" signal is generated by MCU and "TRIP" signal is generated by fault management circuits. The voltage level transmission of PWM signals from 5V to 15V is performed with using isolated MOSFET driver ICs instead of conventional optocouplers because of their low transmission propagation times. In order to provide the isolation between electronic control system and IGBT drivers, the output side of isolated MOSFET driver is supplied with additional isolated 15V power supply.

The fault receiving circuit is formed from a comparator and an optocoupler. The comparator is used to show high impedance load to IGBT driver because the fault signal is generated over a resistor on IGBT driver board. High speed CMOS optocoupler is chosen for the fault receiving circuit to decrease the propagation time of fault signal.

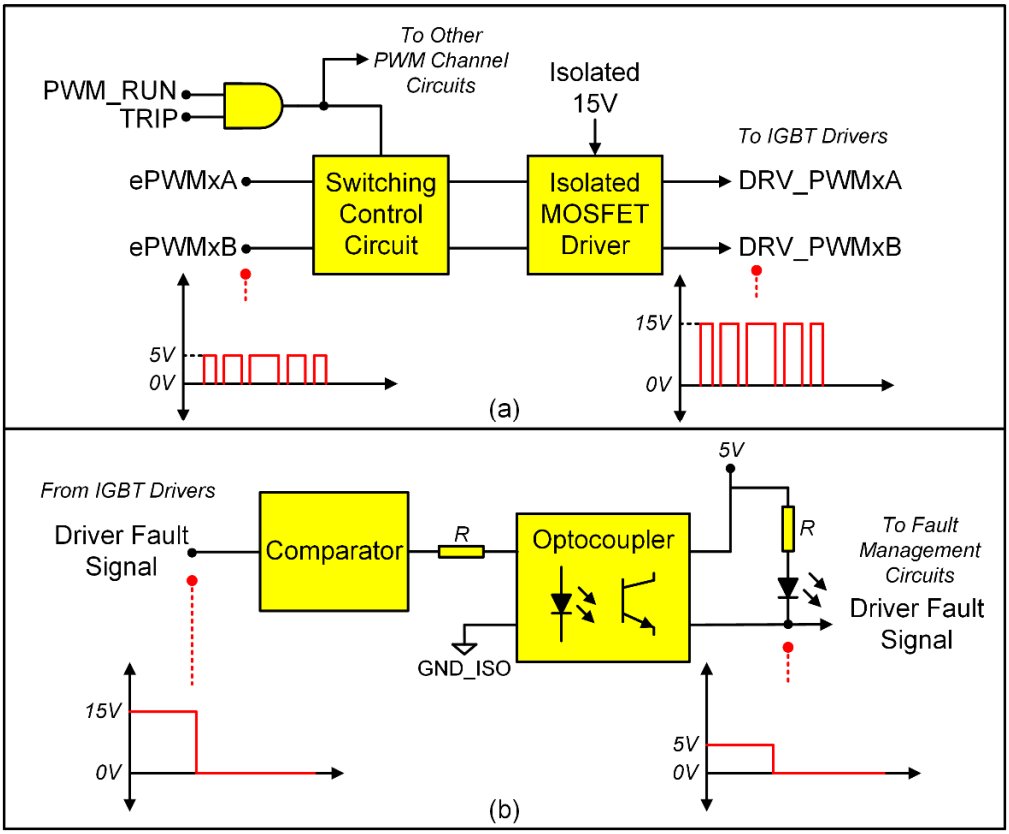


Figure 4.20. Block diagram of firing circuits
(a) Firing circuits for PWM signals
(b) Fault receiving circuits for IGBT driver

4.4.7. PCB Design of Electronic Control System

The electronic control system of SHAPF prototype is realized with two PCB named as “Control Board” and “Firing Board”. Control Board consists of DSP based MCU, measurement circuits, analog protection circuits, fault management circuit and digital I/O circuits. Firing Board consists only firing circuits.

PCB design of Control and Firing Boards have been performed with using Altium Designer software tool. The 2-D layout view and 3-D model of Control and Firing Boards obtained from PCB design software are shown in Figure 4.21(a)-(d). The designed electronic control system formed from Control and Firing Boards are presented in Figure 4.21(e). Control and Firing Boards are designed with two layers using surface mount technology.

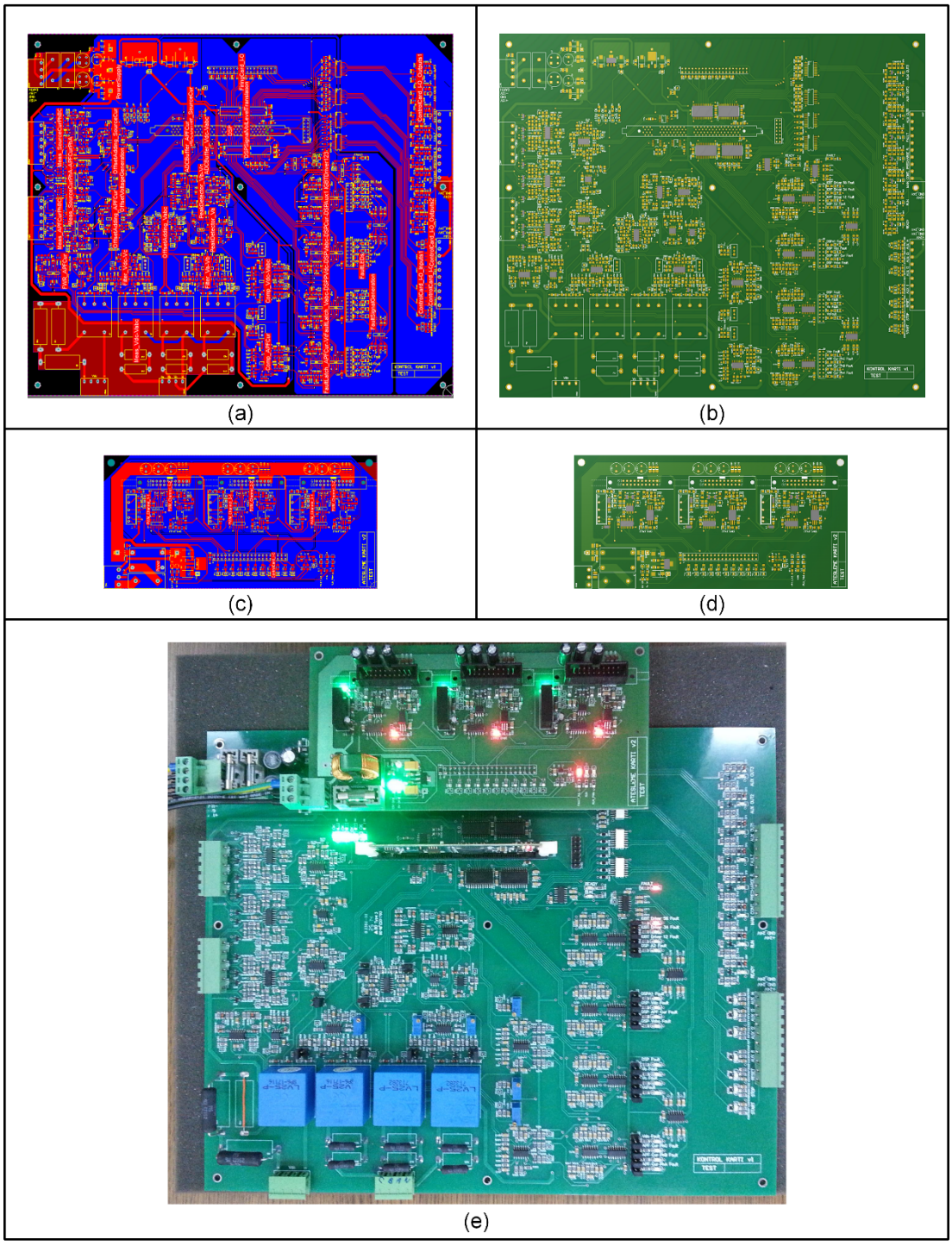


Figure 4.21. PCB design and implementation of electronic control system
(a) 2D layout of control board (b) 3D layout of control board
(c) 2D layout of firing board (b) 3D layout of firing board
(e) Picture of electronic control system

4.5. Hardware Implementation of SHAPF Prototype

The hardware implementation of SHAPF prototype is realized in Power Electronics Research Laboratory of Çukurova University Electrical and Electronics Engineering Department. After the components of power circuit and electronic control system had been supplied with respect to specifications obtained from the design studies, the hardware implementation of SHAPF prototype was performed applying following steps;

- The electronic control system of SHAPF was installed by soldering the electronic components.
- The function tests of electronic control system were performed.
- The mechanical and electrical installation of SHAPF power circuit were performed.
- The function tests of SHAPF power circuit were performed.

The detailed three phase power circuit drawing is presented in Figure 4.22. SHAPF prototype is connected to grid using a three phase disconnector with 40A blade fuses for the protection of power circuit. In order to start-up of SHAPF prototype a 40A three phase power contactor is used at the input of SHAPF power circuit. A 10A three phase power contactor with three 2.2Ω 50W resistors is connected parallel to the main contactor in order to limit the inrush current of PF during the start-up of system. The discharge of dc link capacitor bank is realized using series connected two 1kΩ 50W resistors with 6A relay.

SHAPF prototype has been installed on a metal sheet with dimensions of 130cmx90cm. The top view and side view pictures of SHAPF prototype are presented in Figure 4.23 by indicating the main components.

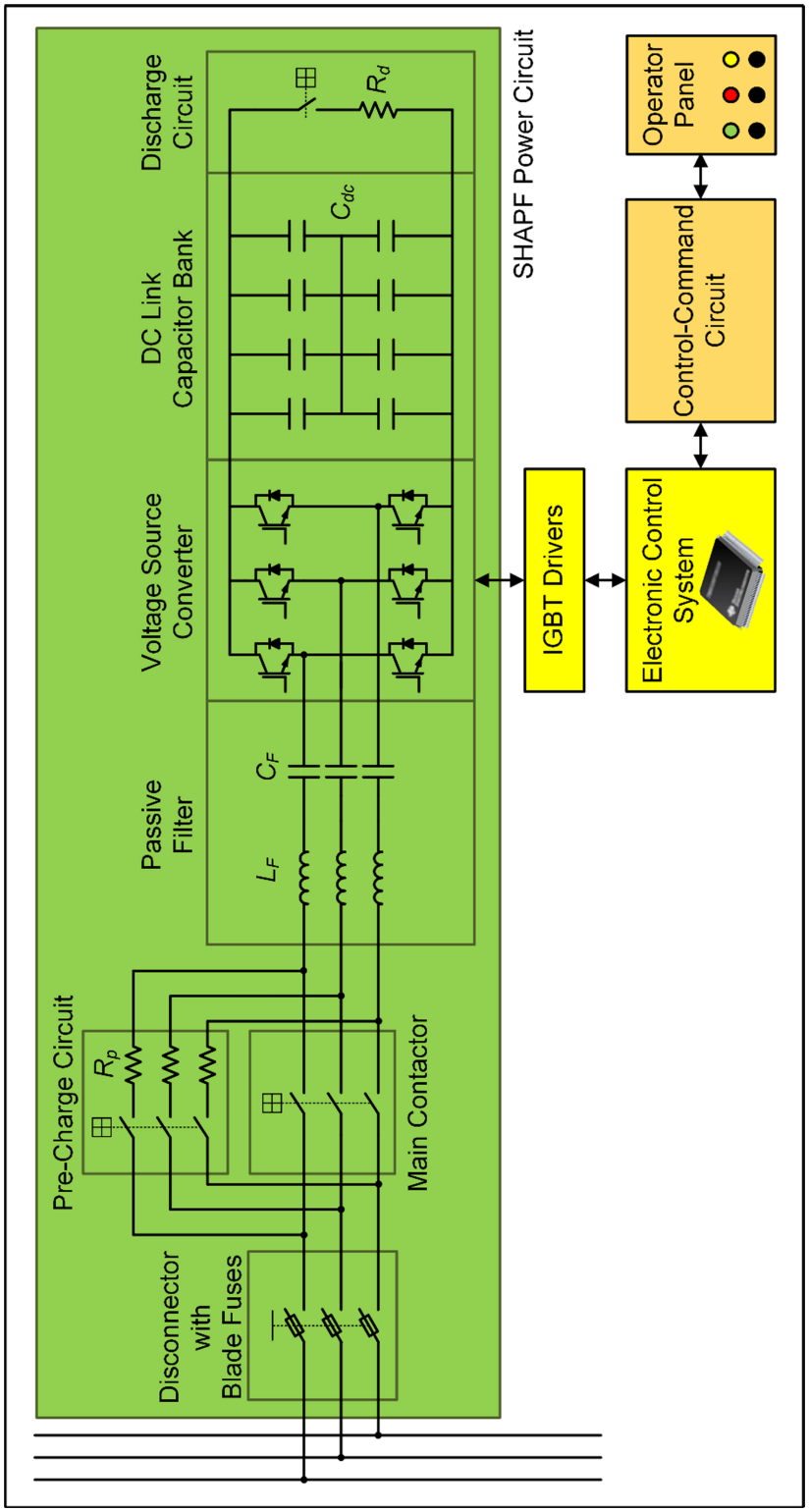
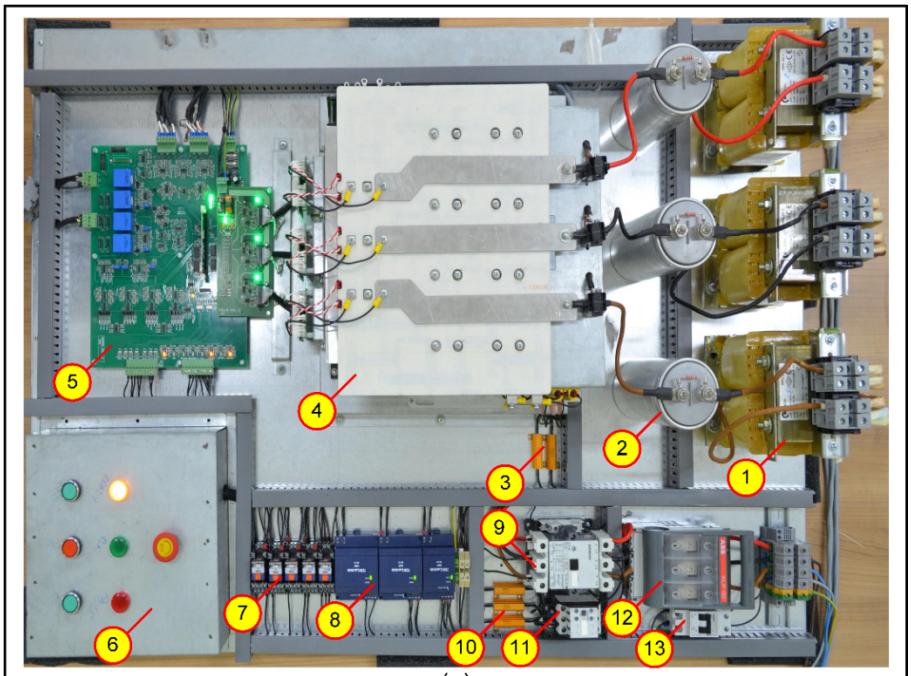
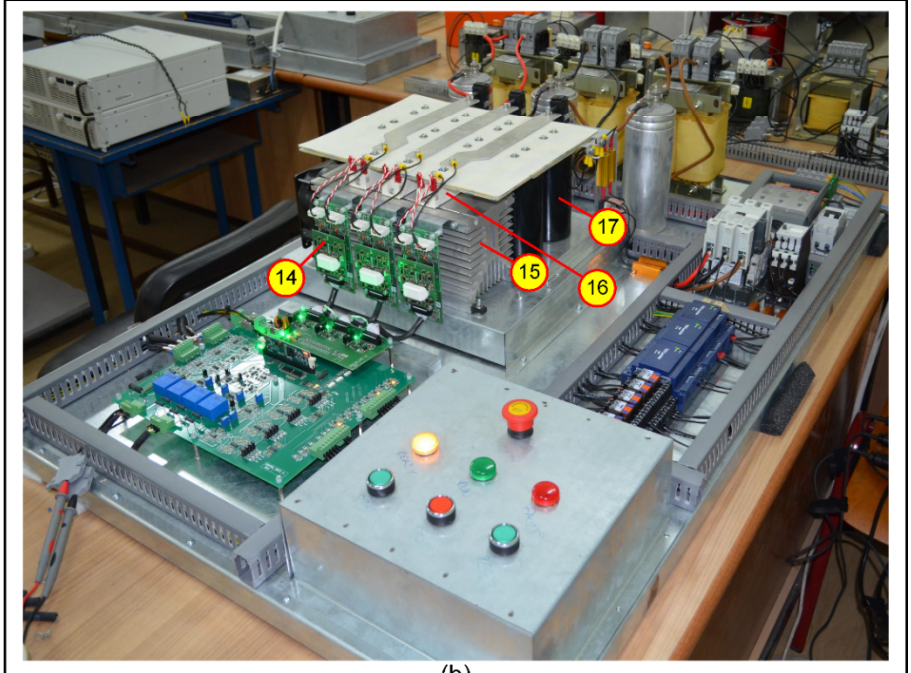


Figure 4.22. Three phase power circuit diagram of SHAPF prototype



(a)



(b)

1. PF Reactor	10. Precharge Resistors
2. PF Capacitor	11. Precharge Contactor
3. Discharge Resistors	12. Disconnector with Blade Fuses
4. DC Link Laminated Busbar System	13. Automatic Fuse of Control System
5. Electronic Control System	14. IGBT Driver
6. Command-Control Interface	15. Heat Sink
7. Command-Control Circuit Relays	16. IGBT Module
8. Power Supplies of Electronic Control System	17. DC Link Capacitor Bank
9. Main Contactor	

Figure 4.23. Pictures of SHAPF prototype
(a) Top view (b) Side view

4.6. Development of Embedded System Software

The embedded system software of SHAPF prototype is developed with Code Composer Studio (CCS) development software tool of Texas Instrument in C programming language. The embedded system software of SHAPF constitutively consists of the main function and the interrupt function. In the main function, the configuration of CPU and peripheral units and initial values of global variables are assigned. The interrupt function consists of the code of SHAPF main control algorithm and operational functions such as, start-stop functions, protection functions, trip functions etc. In the software of SHAPF prototype, PWM interrupt of TMS320F28335 is preferred for the interrupt function.

The flowchart of the main function of SHAPF prototype is given in Figure 4.24. In the main function, the following configurations are performed for TMS320F28335;

- CPU clock speed is set 150MHz with the configuration of PLL.
- The clock signals of peripheral modules are activated.
- The clock speed of ADC is set to 25MHz.
- Input, output and PWM pins of GPIO are configured.
- Peripheral interrupt vector is configured for PWM interrupt function.
- Flash memory is prepared to use.
- ADC module is configured in “Simultaneous Cascade” mode.
- The sample hold window time of ADC module is set to 200ns.
- ePWM modules are configured as,
    - ePWM1 is configured as master module and ePWM2 and ePWM3 are slave modules which are synchronized with respect to ePWM1.
    - ePWM1 generates interrupt in every 100μs and start ADC conversion.
    - ePWM1, ePWM2 and ePWM3 modules are configured to generate switching signals at 10kHz.

In the final step of main function, TMS320F28335 is kept in infinite loop and waited for interrupt function of ePWM1 module.

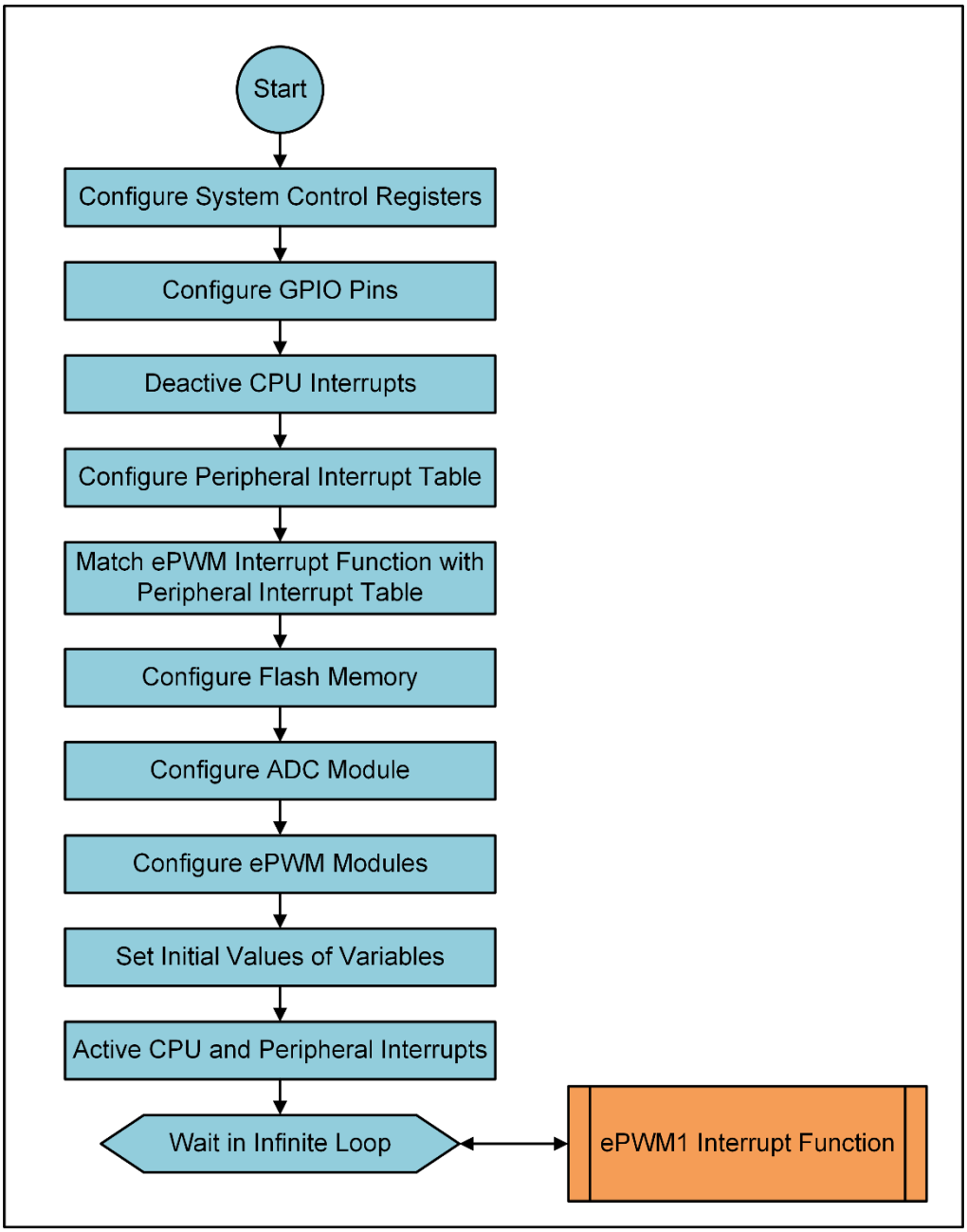


Figure 4.24. Flow chart of main program

When the counter value of ePWM1 timer is equal to zero in every 100µs, the interrupt signal of ePWM1 is generated to start the interrupt function and ADC conversion. The interrupt function controls the whole operation of SHAPF prototype. The flowchart of interrupt function which shows the main steps of program flow is presented in Appendix F.

5. EXPERIMENTAL RESULTS

5.1. Overview of Experimental Studies

The experimental studies of SHAPF prototype are performed in the Power Electronics Research Laboratory of Çukurova University Electrical and Electronics Engineering Department. In order to experience the functions and performance of SHAPF prototype, a load group which consists of nonlinear and inductive loads is set up.

The power circuit diagram and the photography of the experimental set-up are introduced in Figure 5.1 and 5.2, respectively. The load group is formed from 3 pieces 5kW three phase bridge rectifiers with smoothing reactors. The three phase rectifiers are designed highly capacitive loaded in order to increase the magnitude of low frequency dominant harmonics. The inductive load group is formed with 5 steps as; 2 steps 1kVAr loads, 2 steps 2kVAr loads and 1 step 5kVAr loads. The specifications of load group are summarized in Table 5.1.

During the experimental studies, the experimental waveforms are captured with Tektronix MSO3034 oscilloscope. The PQ measurements are done with Fluke 1760 power quality analyzer which is fully compatible with IEC 61000-4-30. The voltage, current and power measurements are recorded with 200ms averages and the harmonic measurements are recorded with 3s averages. The power and harmonic measurements are presented using the measurement analysis program of Fluke 1760. In order to show simultaneous power and harmonic measurements, single phase measurements are recorded with Fluke 1760 from supply, load and SHAPF sides by taking Phase A as reference. Three phase power demonstrations are done with taking the three times of the power measurements of Phase A.

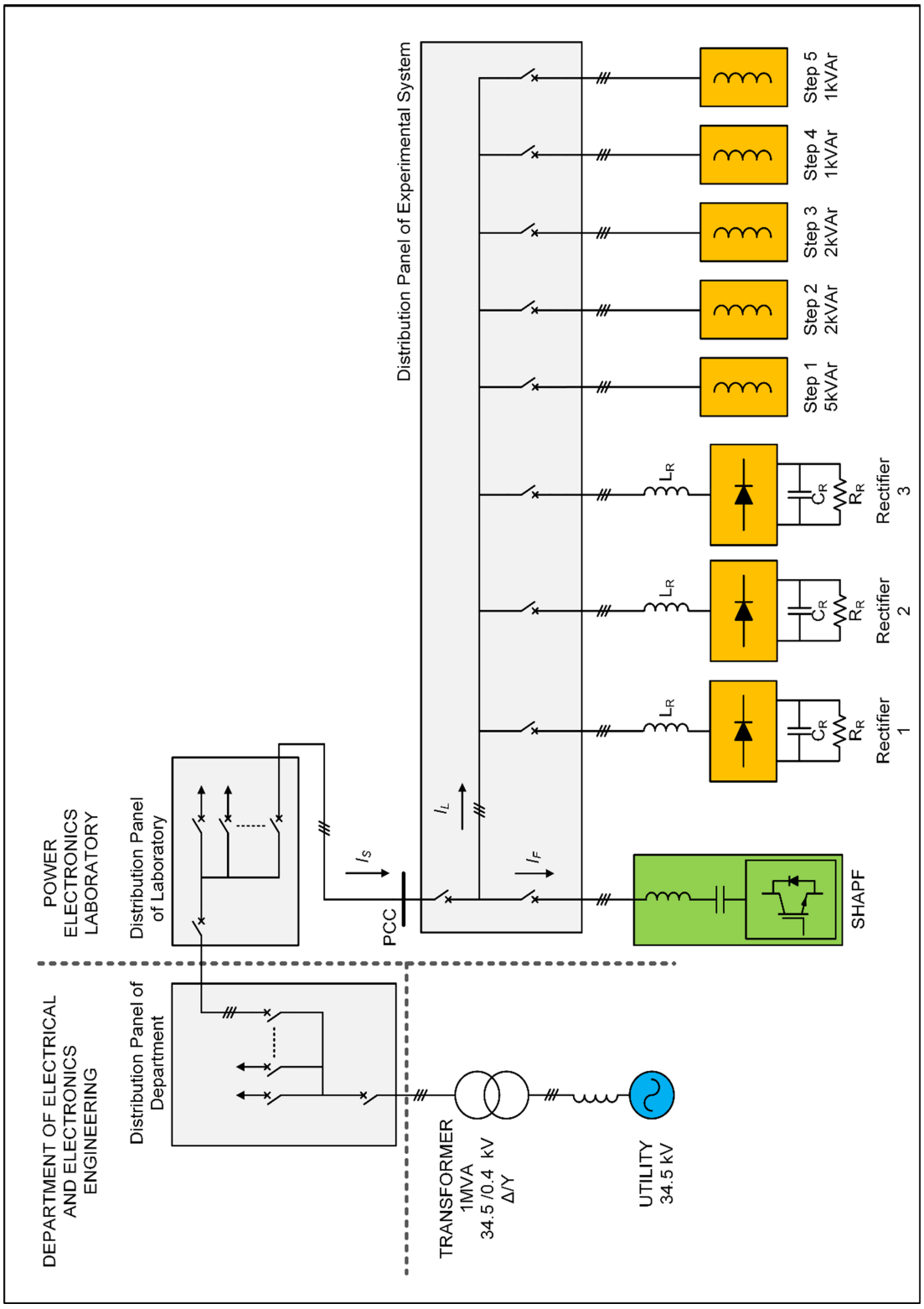


Figure 5.1. Power circuit diagram of experimental diagram

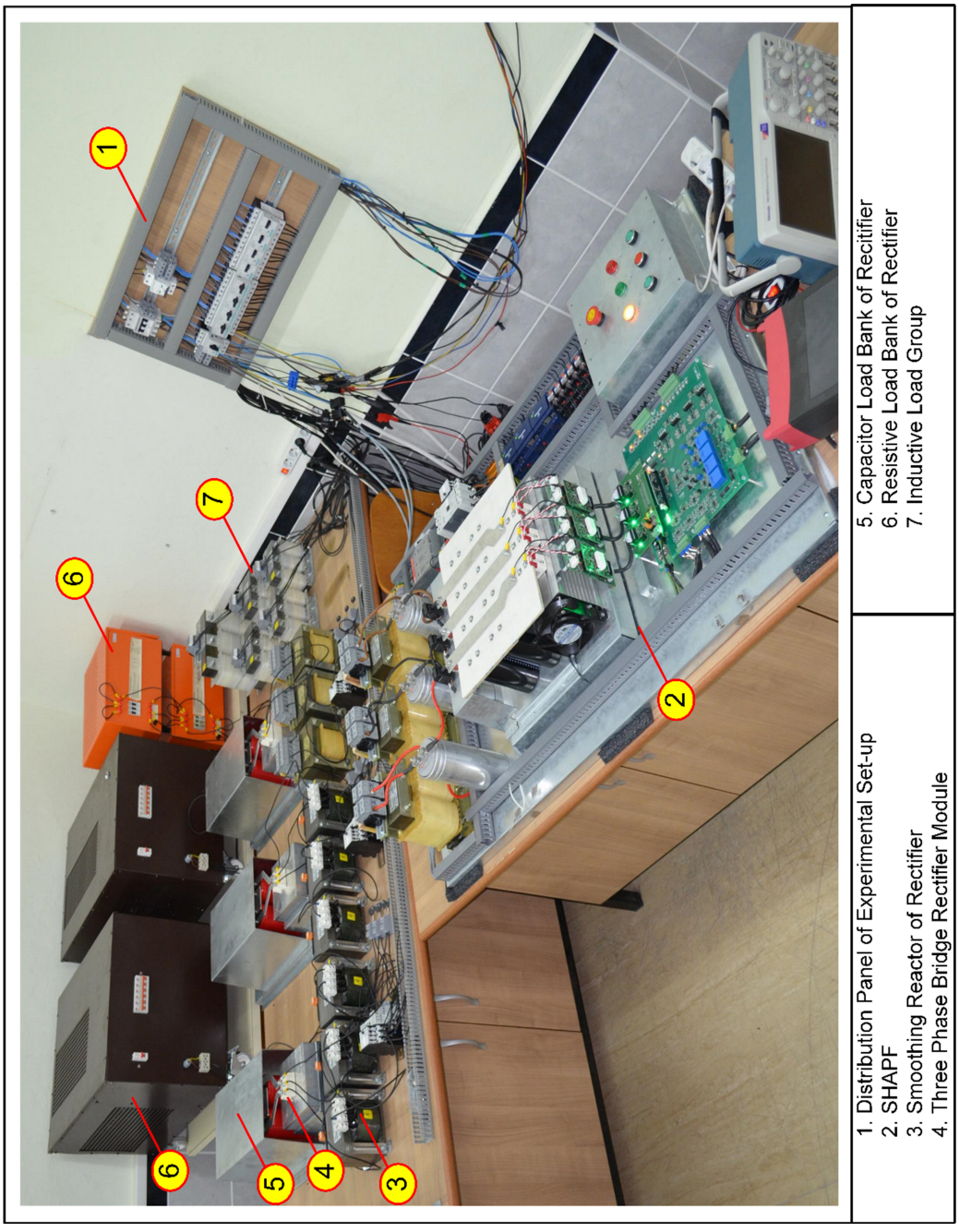


Figure 5.2. Picture of experimental set-up

Table 5.1. Power circuit specifications of experimental load group

Three Phase Bridge Rectifiers	
DC Load Resistor (R_R)	50Ω
DC Load Capacitor (C_R)	2200μF
Smoothing Reactor (L_R)	2mH
Inductive Loads - 11kVAr with 5 Steps	
Step 1	5kVAr
Step 2-3	2kVAr
Step 4-5	1kVAr

The source voltage waveform and the waveforms of the load group current are presented in Figure 5.3 when all rectifiers and inductive loads of the load group are turned on. The active and reactive power trend of the load group are shown in Figure 5.4 and 5.5. The current THD trend and the current harmonic spectrum of the load group are given in Figure 5.6 and 5.7. During the PQ measurements of this case, the supply voltage changes around 218V. It is shown from the experimental waveforms that the current waveform of the load group is considerably distorted. The load group draws nearly 16kW active power and 13.5kVAr reactive power. The current THD of load group is around 41%. And it is seen from the current harmonic spectrum that the load group draws 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonics intensively. With this load group, the performance of SHAPF prototype can be tested under close to its full compensation ratings.

The performance of SHAPF prototype is investigated with the comprehensive experimental case studies which are presented in the following sections. Firstly, the start-up of SHAPF prototype is examined. Secondly, the performance of the proposed individual harmonic elimination based feedback harmonic control method is investigated with constant dc link voltage by comparing with conventional methods. Finally, the performance of the proposed controller which achieves the dynamic harmonic and reactive power compensation with adaptive dc link voltage is presented.

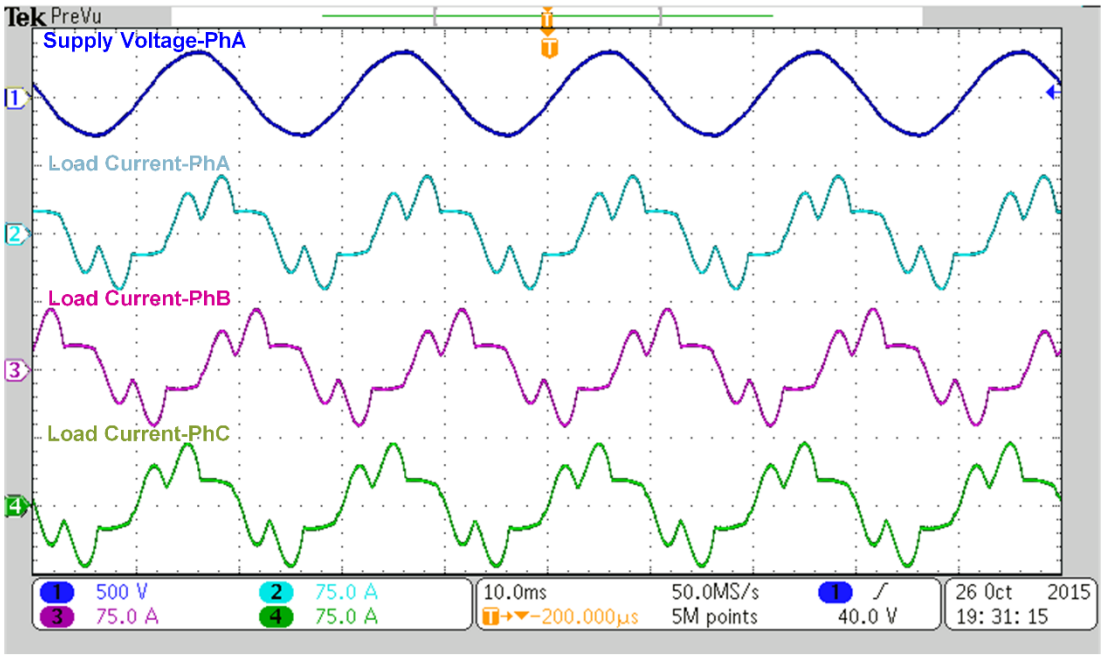


Figure 5.3. Supply voltage and load group current waveforms

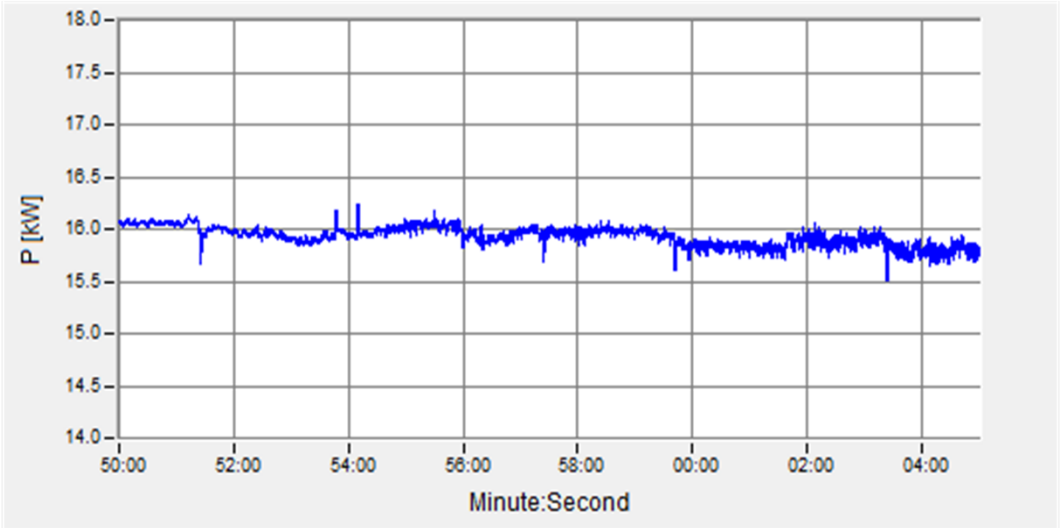


Figure 5.4. Active power trend of load group

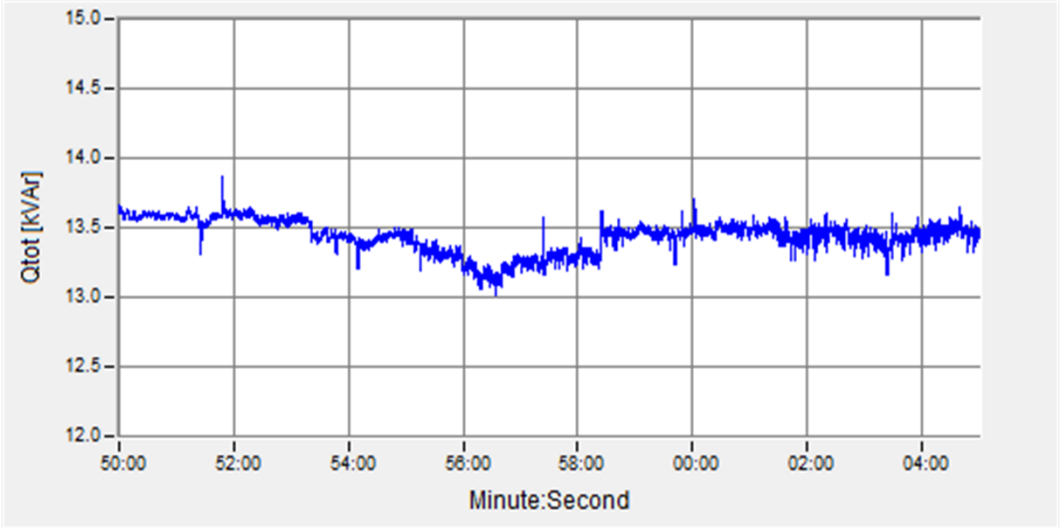


Figure 5.5. Reactive power trend of load group

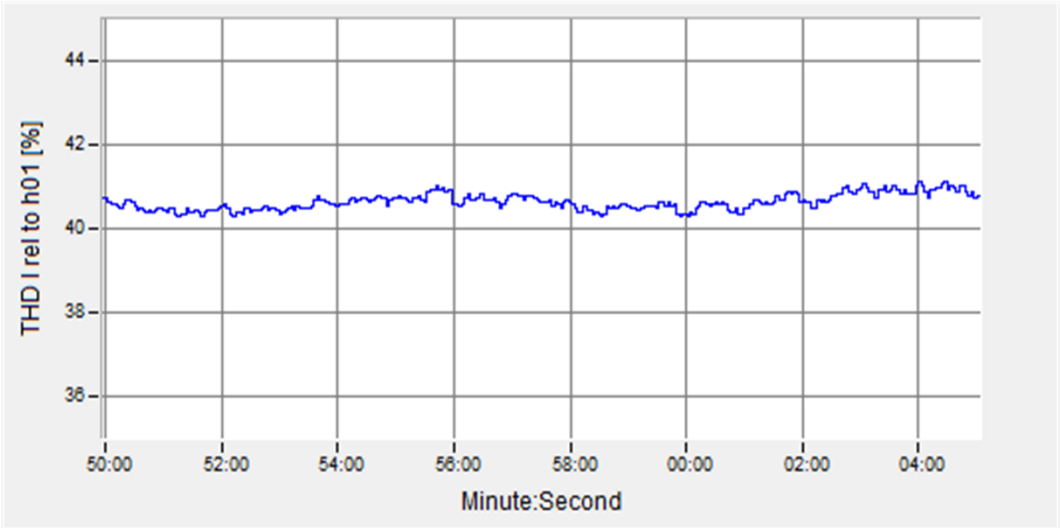


Figure 5.6. THD trend of load group current

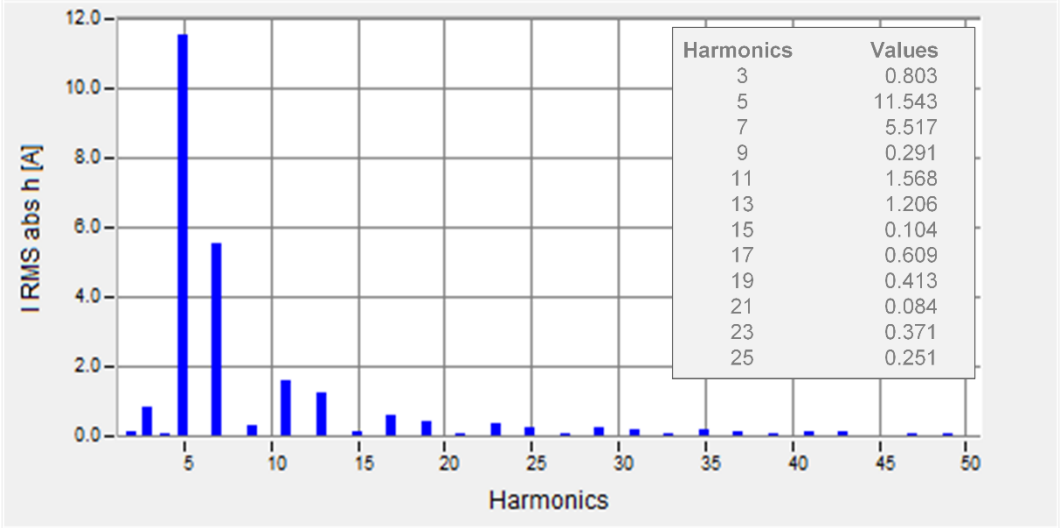


Figure 5.7. Harmonic spectrum of load group current

5.2. Investigation of Start-up

In this part of the experimental results, the start-up of SHAPF prototype is investigated. SHAPF prototype is started-up by following procedure. In this procedure, firstly PF is turned on with pre-charge resistor by closing the pre-charge contactor when the start signal arrives. After 0.2s later, the main contactor is closed and the pre-charge circuit is bypassed and PF is connected to the supply directly with the load. After 0.2s later than the closing of the main contactor, the pre-charge contactor is opened. During the start-up of PF, IGBTs in the bottom leg of VSC are turned on to maintain star point to PF. After 1s later than the closing of the main contactor, the dc link voltage controller is started up and sets the dc link voltage to the reference voltage level. Finally, after 3s later than the start of the dc link voltage controller, the harmonic and reactive power compensation controllers are started and the start-up procedure of SHAPF prototype is completed.

The start-up of SHAPF prototype is investigated with following cases;

- Case 1: The Inrush Current of PF
- Case 2: The Standalone Operation of PF with Load Group
- Case 3: The Start-up of SHAPF Controllers

5.2.1. Case 1: The Inrush Current of PF

In this case the effect of the pre-charge circuit is investigated. The inrush current of capacitors can exceed 10 times of its nominal current value. This inrush current can cause undesired problems such as; fuse trips, contactor failures and notches on supply voltage. Additionally, the inrush current of PF flows through VSC in SHAPF topology because of the series connection of PF and VSC. Thus, the excessive inrush current can damage IGBTs in VSC.

In Figure 5.8, the start-up current waveforms of PF without pre-charge circuit are presented. The inrush current of PF reaches 150A and oscillates nearly one period. This excessive inrush currents cause a severe waveform distortion in the supply voltage.

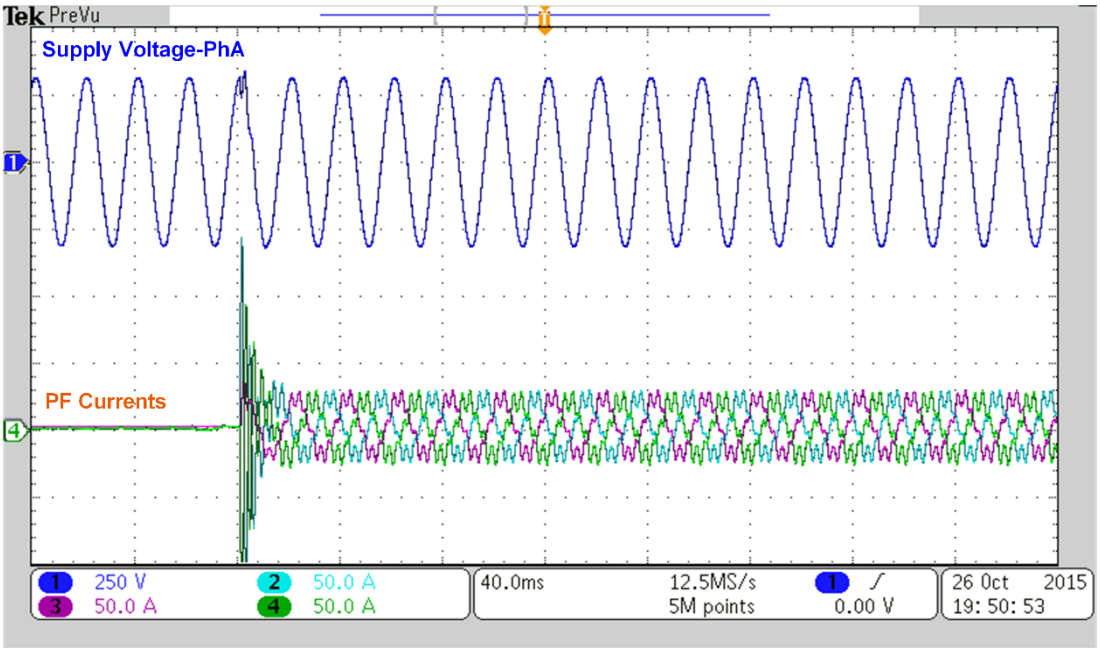


Figure 5.8. Start-up current waveforms of PF without pre-charge circuit

In Figure 5.9, the start-up current waveforms of PF with pre-charge circuit are presented. With the help of 3.3Ω pre-charge resistors, the inrush current of PF is limited under 70A. It is shown from Figure 5.9 that PF is firstly turned on with the pre-charge circuit and the inrush current reaches only 50A approximately. After 0.2s later,

the main contactor is closed and PF are connected to the supply directly without excessive inrush current. Moreover, this soft start-up of PF with pre-charge circuit does not cause any waveform distortion on the supply voltage.

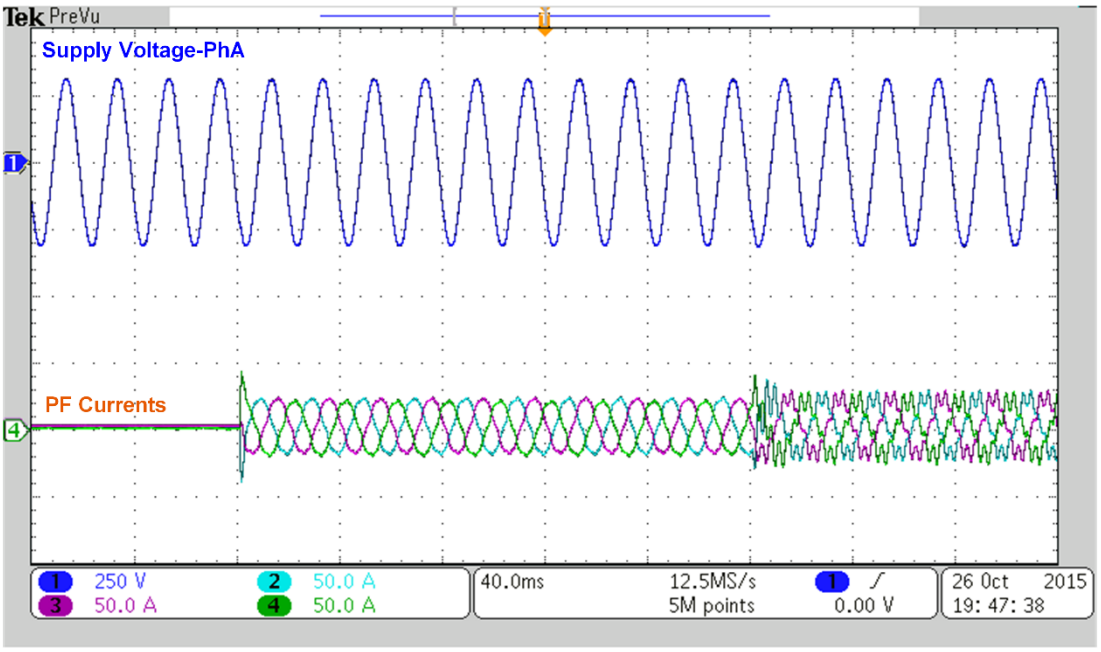


Figure 5.9. Start-up current waveforms of PF with pre-charge circuit

5.2.2. Case 2: Standalone Operation of PF with Load Group

In this case, the standalone harmonic filtering and reactive power compensation performance of PF filter is presented. During the standalone operation, all nonlinear loads and inductive loads in the load group are turned on. The supply voltage and source load and PF current waveforms are presented in Figure 5.10. The reactive power trends of supply, load and PF is given in Figure 5.11. The supply voltage THD trend and harmonic spectrum are given in Figure 5.12 and 5.13, respectively. The supply and load THD trends, the supply harmonic spectrum and the load current harmonic spectrum are given in Figure 5.14, 5.15 and 5.16, respectively.

During the PQ measurements of this case, the supply voltage changes around 213.6V. The load group demands around 12.7kVAr. PF supplies nearly 8.9kVAr reactive power at this voltage level and compensates the significant part of the load

group reactive power. When the harmonic compensation performance of PF is investigated from the experimental results, PF filters nearly 15% of 5th harmonic, about %10 of 11th and 13th harmonics, lower than %10 of higher frequency harmonics. Besides this poor harmonic filtering performance of PF, it causes an amplification in the 7th harmonic frequency which is the cut-off frequency of PF. When the harmonic spectrums of supply and load currents are investigated, it is shown that the 7th harmonics in the load current increases up to %13 at the supply current. It is seen from the supply voltage, supply current and load current harmonic spectrums that PF causes a series resonance in the power system and the 7th harmonic currents of the neighbor loads in the power system flow through to PF instead of the supply. Even though, PF provides a harmonic filtering in low ratios, the supply current THD increases from 37.9% up to 43.4% because of the high amount of amplification in 7th harmonic and the decrease of the fundamental component cause by the reactive power compensation.

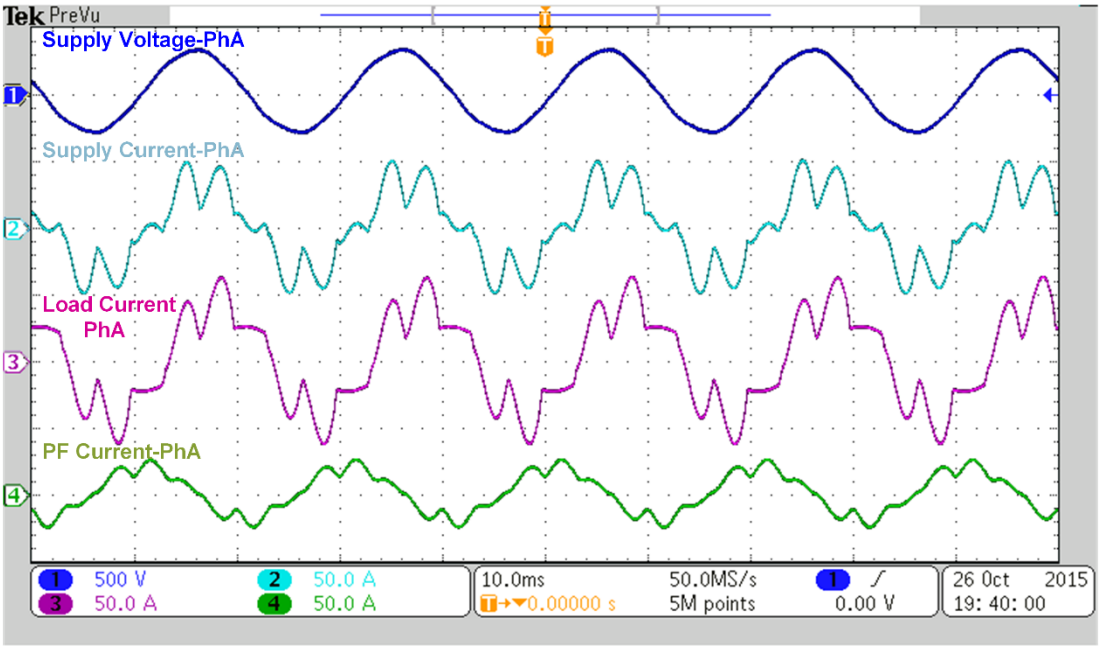


Figure 5.10. Supply voltage and current waveforms during the operation of PF with load group

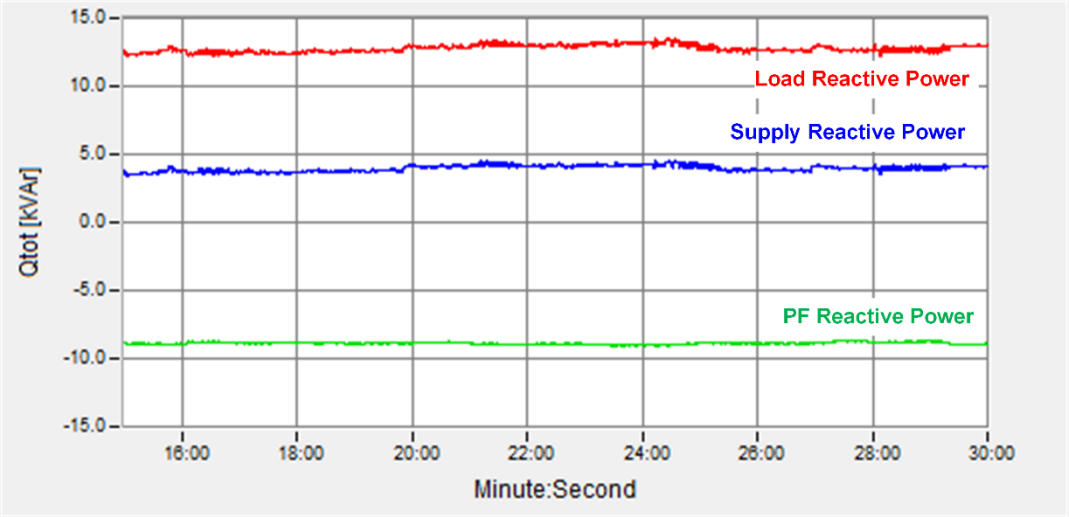


Figure 5.11. Reactive power trends during the operation of PF with load group

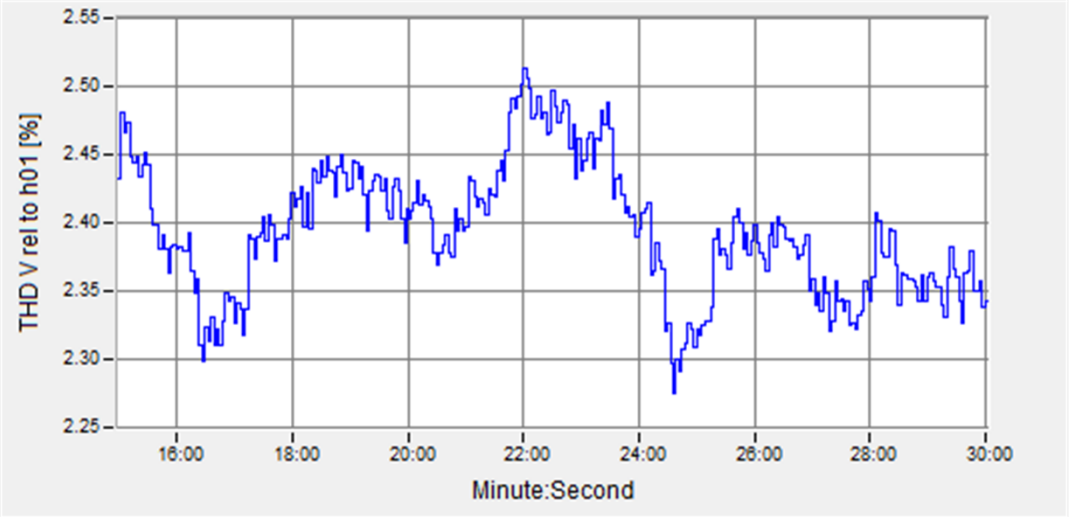


Figure 5.12. Supply voltage THD trend during the operation of PF with load group

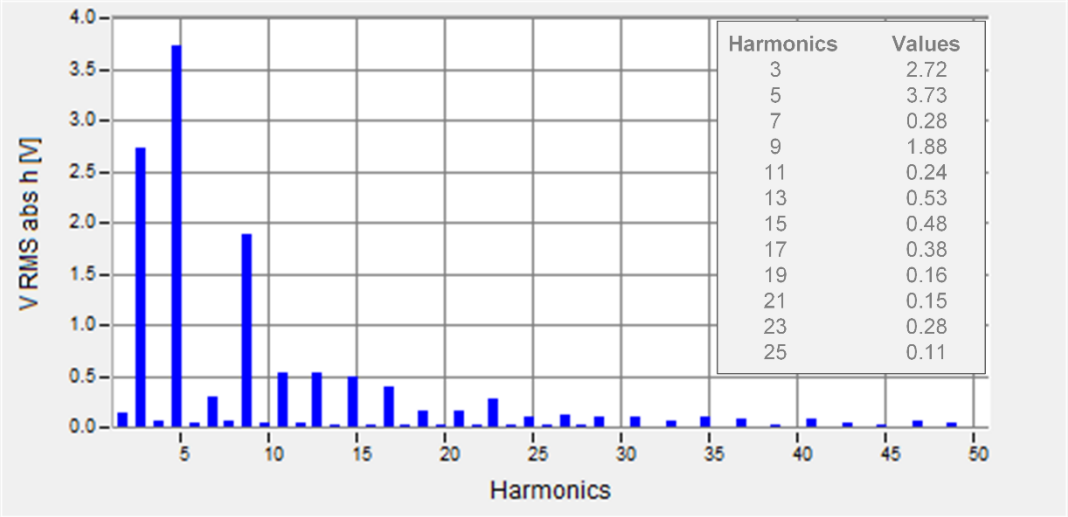


Figure 5.13. Supply voltage harmonic spectrum during the operation of PF with load group

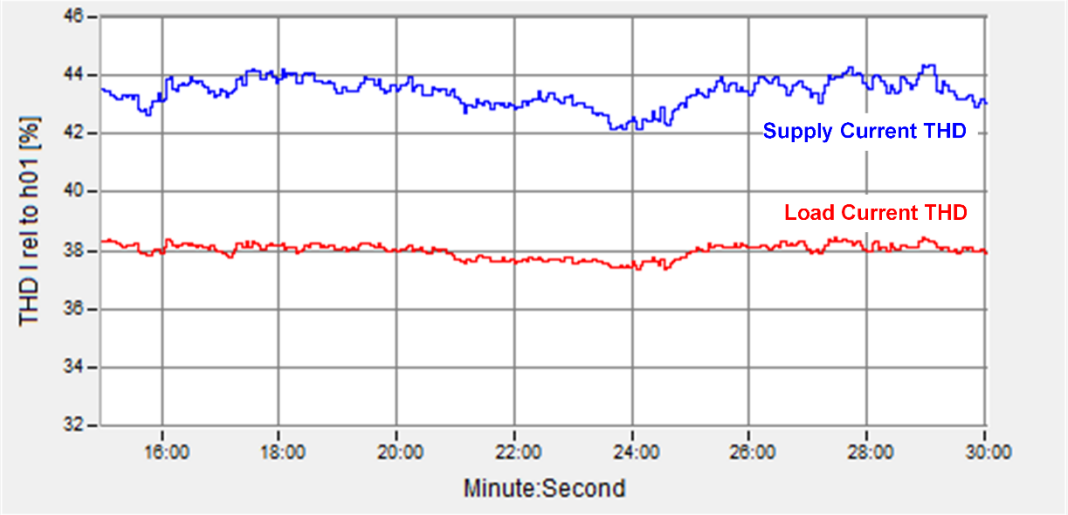


Figure 5.14. Current THD trends during the operation of PF with load group

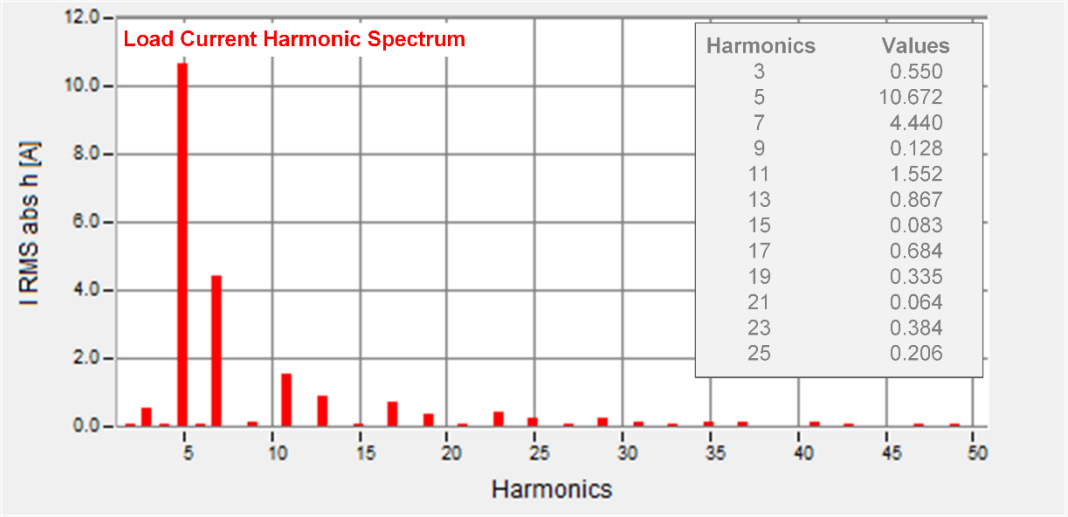


Figure 5.15. Load current harmonic spectrum during the operation of PF with load group

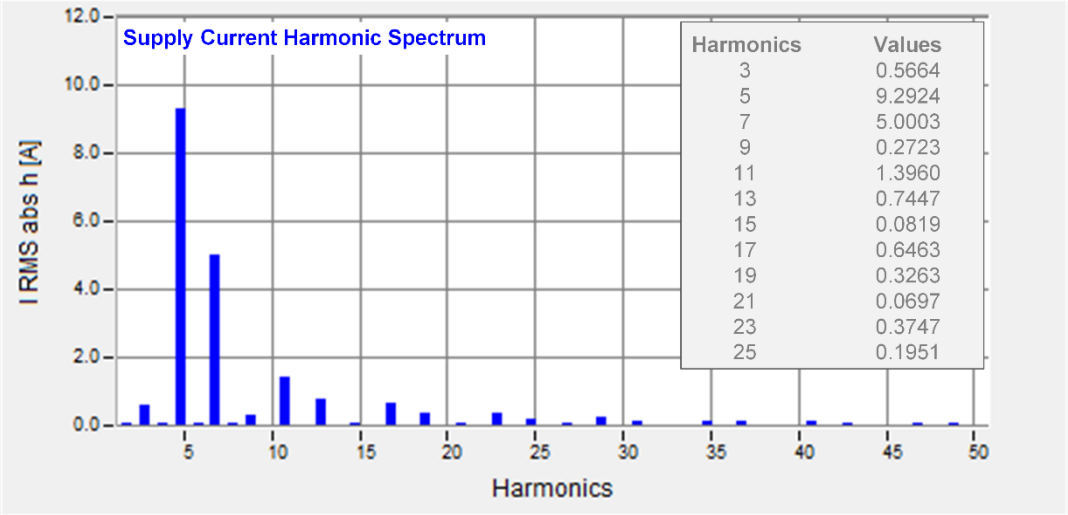


Figure 5.16. Supply current harmonic spectrum during the operation of PF with load group

5.2.3. Case 3: Start-up of SHAPF Controllers

In this case, the start-up of the proposed SHAPF controller method are introduced with the experimental results. The proposed control method is started up with the dc link controller. The dc link controller is firstly set the dc link voltage level to the reference value generated by the adaptive dc link voltage reference generation method. In Figure 5.17, the start-up of the dc link voltage controller is presented with

supply voltage and current, SHAPF current and dc link voltage waveforms. During the start-up presented in Figure 5.17, all nonlinear loads and all steps of linear loads are turned on and the load group demands around 13kVAr. The adaptive dc link reference generation method calculates the dc link voltage reference value 295V for the harmonic and reactive power compensation of SHAPF. After the start of the dc link voltage controller, the controller have set the dc link voltage level to the reference value of 295V under 300ms with under 10% overshoot.

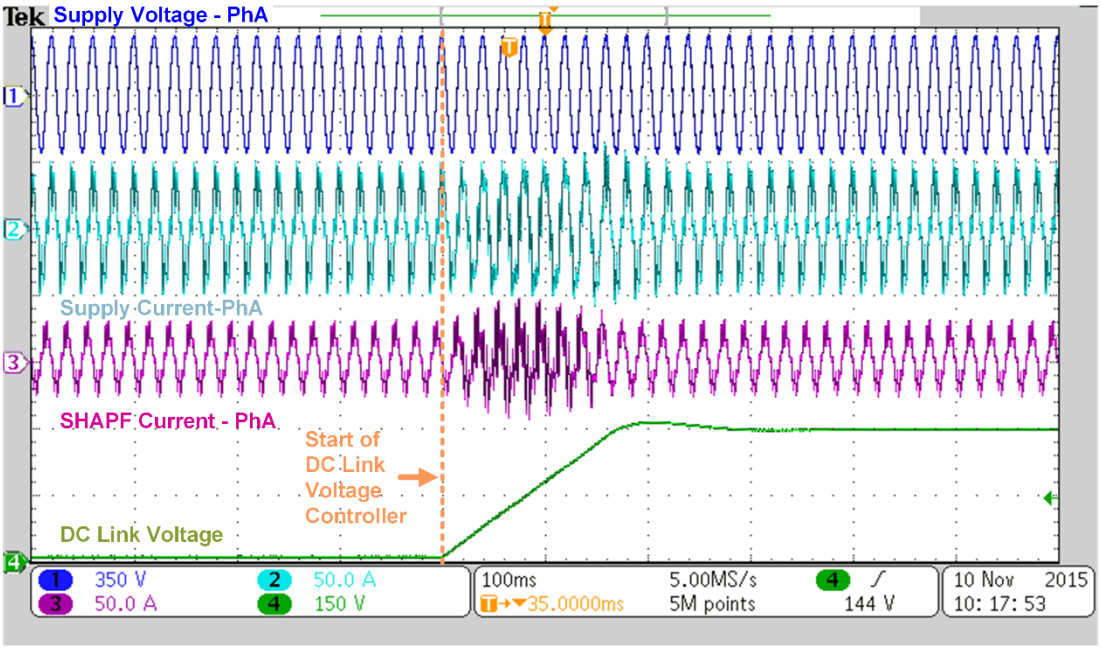


Figure 5.17. Supply voltage, supply current SHAPF current and dc link voltage waveforms during the start-up of dc link voltage controller

After the start-up of the dc link voltage controller, SHAPF is ready to start the compensation. The start-up of the harmonic and reactive power compensation is presented with the waveforms of supply voltage and current, SHAPF current and dc link waveforms in Figure 5.18. It is seen in the experimental waveforms that the start-up of the compensation controllers causes an oscillation on dc link voltage but this oscillation is suppressed by the dc link voltage controller under 100ms with 2% overshoot. SHAPF operates nearly at the full compensation rating and the dc link voltage ripple is held under 6V – 2% in the steady state operation of SHAPF prototype. SHAPF prototype can provide the full harmonic and reactive power compensation

requirements under 100ms after the start-up of the compensation controllers. In the steady state condition after the start-up of the harmonic and reactive power compensation controllers, SHAPF prototype decreases the THD of the supply current 42% to under 3.8% and compensates 13.1kVAr reactive power of load by decreasing the supply reactive power in the range of ±100VAr. The detailed compensation performance investigation of SHAPF prototype is presented in the following sections.

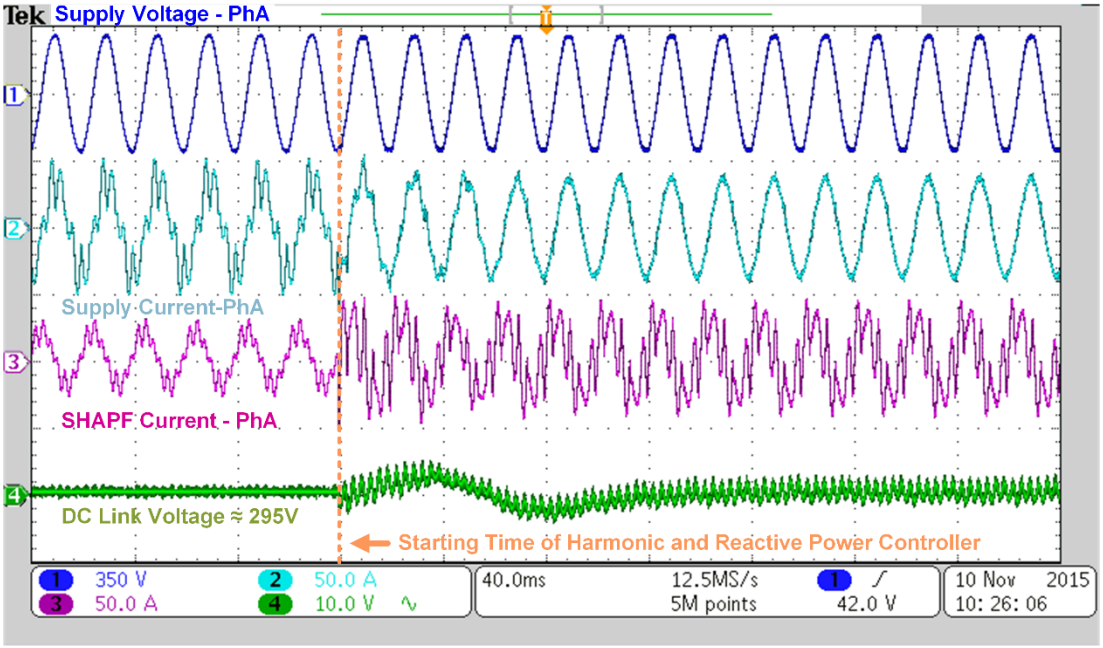


Figure 5.18. Supply voltage, supply current, SHAPF current and dc link voltage waveforms during the start-up of the compensation controllers

5.2.4. Summary

In this section of the experimental results, the each step of the start-up operation of SHAPF prototype is investigated with detailed experimental results. The experimental results of the start-up operation of SHAPF prototype are summarized with following statements;

- The necessity of pre-charge circuit is observed with the experimental results. The inrush current of PF is limited under 70A with the designed pre-charge circuitry.

- The compensation performance of PF in standalone operation is investigated in detail. The harmonic and reactive power compensation performances of PF are summarized in Table 5.2 when all rectifiers and all steps of the load group are turned on. PF compensates the significant part of the reactive power of the load group but it shows inadequate harmonic filtering performance. Moreover, PF causes resonance problem in the power system at 7^{th} harmonic frequency.

Table 5.2. Summary of PF compensation performance during the standalone operation

Parameters	Load Side	Supply Side
Reactive Power	12.8kVAr	3.9kVAr
Fundamental Current	30.9A	24.7A
5^{th} Current Harmonic	10.67A	9.29A
7^{th} Current Harmonic	4.44A	5.00A
11^{th} Current Harmonic	1.55A	1.39A
13^{th} Current Harmonic	0.86A	0.74A
17^{th} Current Harmonic	0.68A	0.64A
19^{th} Current Harmonic	0.33A	0.32A
23^{th} Current Harmonic	0.38A	0.37A
25^{th} Current Harmonic	0.20A	0.19A
THD	37.9%	43.4%

- The start-up of the proposed controller is presented in detailed waveforms. The dc link voltage controller can set the dc link voltage reference value of 295V which is calculated by the adaptive dc link voltage reference generation method for the full compensation requirements of the load group under 300ms with under 10% overshoot.
- The start-up of harmonic and reactive power compensation controllers is tested approximately at the full compensation ratings. After the start-up of the compensation controllers, SHAPF prototype can provide the full harmonic and reactive power compensation requirements under 100ms. The start-up of the compensation controllers causes an oscillation in the dc link voltage but this oscillation is controlled with the dc link controller under 100ms with 2% overshoot. The dc link ripple is held under 6V – 2% in the steady state operation of SHAPF prototype which is below than the design criteria of 3%.

5.3. Harmonic Performance Comparison of Proposed Controller with Conventional Controllers

In this section of the experimental results, the performance of the proposed individual harmonic elimination based feedback controller (Figure 3.24) is investigated by comparing with the conventional feedback controller (Figure 3.25) and feedback+5th harmonic feedforward controller (Figure 3.28).

In order to compare the performance of harmonic compensation controllers on equal terms;

- All nonlinear loads and inductive loads of the load group have been turned on.
- The reactive power compensation controller and adaptive dc link reference calculation method of the proposed controller method are disabled. SHAPF supplies constant reactive power with only the capacitive reactive capacity of PF.
- The dc link voltage level is set to 100V.
- The feedback gain, *K* is set to 10 in all of three controllers.

In this section, the experimental results of the conventional harmonic controllers and the proposed harmonic controller are presented with the following cases.

5.3.1. Case 1: Harmonic Compensation Performance of Conventional Feedback Controller

In this case, the harmonic compensation performance of the conventional feedback controller (Figure 3.24) presented in Section 3.3 is investigated. The supply voltage and current waveforms are shown in Figure 5.19. The supply, load and SHAPF currents and the dc link voltage waveforms are given in Figure 5.20. The supply and load current THD trends, the load current harmonic spectrum and the supply current harmonic spectrum are presented in Figure 5.21, 5.22 and 5.23, respectively.

The harmonic compensation performance of conventional feedback harmonic controller is clearly shown from waveforms and harmonic spectrum. This method provides a considerable harmonic filtering performance in low order dominant harmonics with compensating 84.4% of 5^{th} harmonic, 93.6% of 7^{th} harmonic, 64.7% of 11^{th} harmonic and 60.8% of 13^{th} harmonic of the load current. Although the conventional feedback control method provides a certain performance in the low order harmonic frequencies, the magnitude of 5^{th} harmonic in the supply current still remains in a high level because of the 7^{th} harmonic tuning frequency of PF. In 17^{th} and 19^{th} harmonic currents, SHAPF prototype shows insufficient performance with this conventional compensation method. Moreover, SHAPF prototype causes amplification in 23^{rd} and 25^{th} harmonics because of the feedback gain, K of the conventional controller and the phase error in the measurement. At the certain level of K, the feedback controller starts a contradiction between the performance and the stability of system. The increase of K increases the harmonic filtering performance of system up to a certain value. However, the excessive increase of K causes instability problems such as an amplification in high order harmonics after a certain level of K. With the selected K value of the controller, SHAPF prototype maintains the minimum THD value of supply current harmonic despite of the handled amplification in high order harmonics. SHAPF prototype decreases the supply current THD from nearly 40.6% to 9.36% with this conventional method.

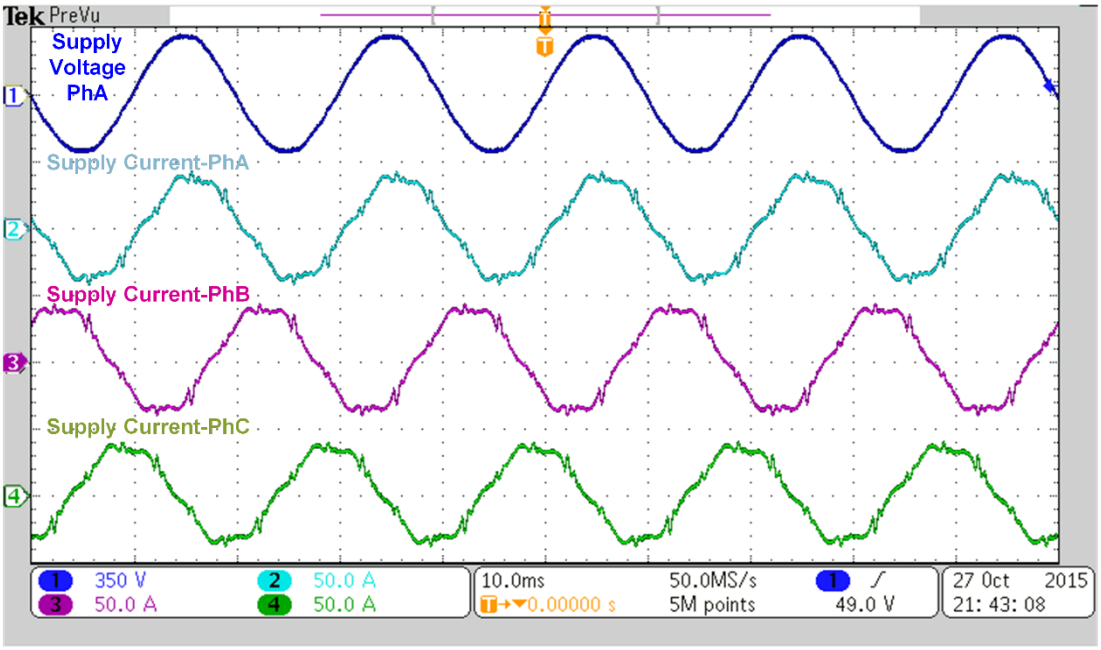


Figure 5.19. Supply voltage and current waveforms during the operation of conventional FB harmonic controller

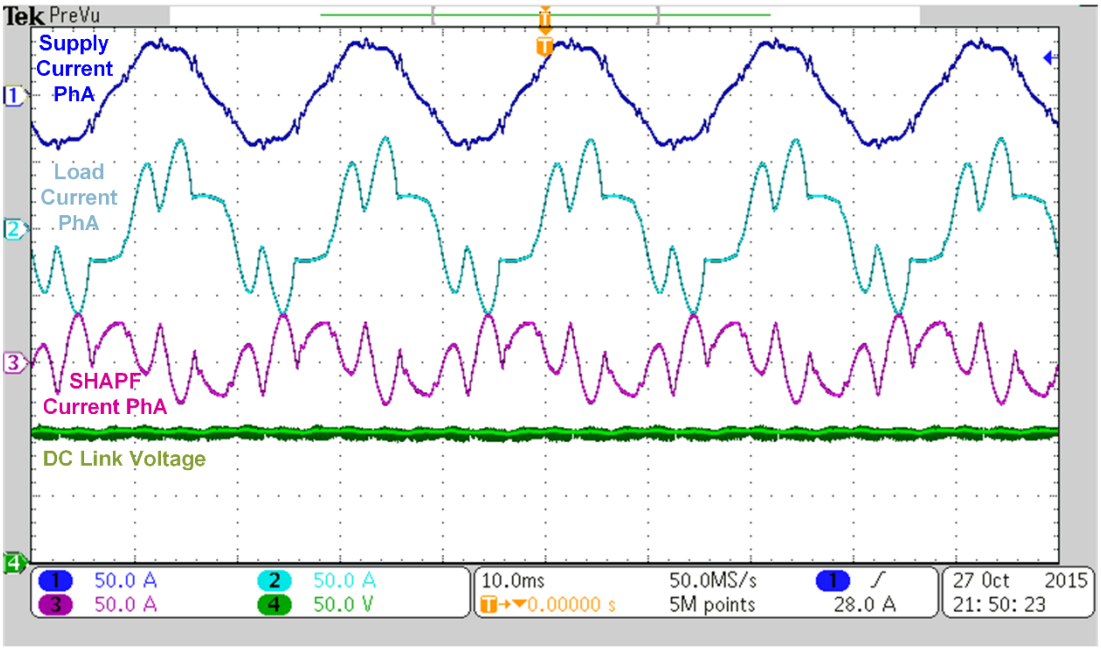


Figure 5.20. Current and dc link voltage waveforms during the operation of conventional FB harmonic controller

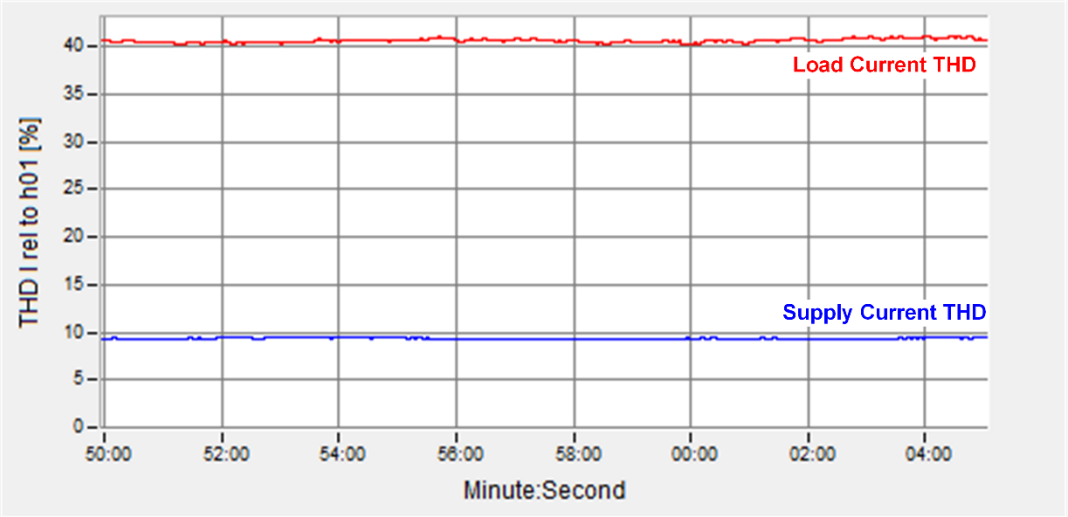


Figure 5.21. Supply and load current THD trend during the operation of conventional FB harmonic controller

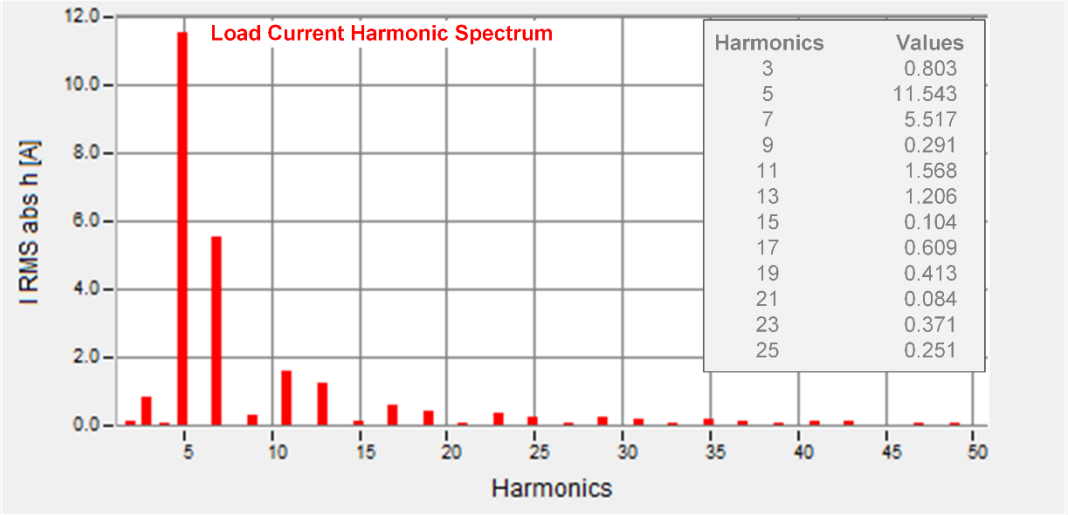


Figure 5.22. Load current harmonic spectrum during the operation of conventional FB harmonic controller

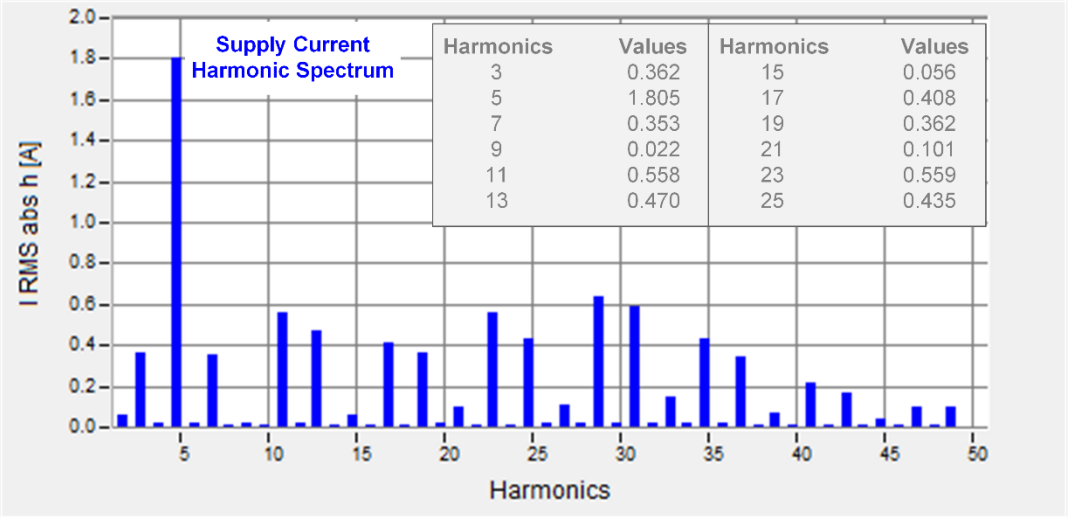


Figure 5.23. Supply current harmonic spectrum during the operation of conventional FB harmonic controller

5.3.2. Case 2: Harmonic Compensation Performance of Conventional Feedback + 5th Harmonic Feedforward Controller

Because of the insufficient 5th harmonic compensation performance of the conventional feedback controller, an additional feedforward loop is added to the conventional feedback controllers in early studies. In this case, the harmonic compensation performance of this additional 5th harmonic feedforward control loop (Figure 3.25) presented in Section 3.3 is investigated.

The supply voltage and current waveforms are shown in Figure 5.24. The supply, load and SHAPF currents and the dc link voltage waveforms are given in Figure 5.25. The supply voltage harmonic spectrum, the supply and load current THD trends, the load current harmonic spectrum and the supply current harmonic spectrum are presented in Figure 5.26, 5.27, 5.28 and 5.29, respectively.

It is shown from the experimental results that the feedforward loop increases the 5th harmonic filtering performance of SHAPF prototype from approximately 84.4% to 92.7%. The feedback+5th harmonic feedforward controller shows the similar harmonic filtering performance with the conventional feedback controller for other harmonic frequencies as expected. With the effect of feedforward loop, SHAPF prototype decreases the supply current THD around to 7.19%.

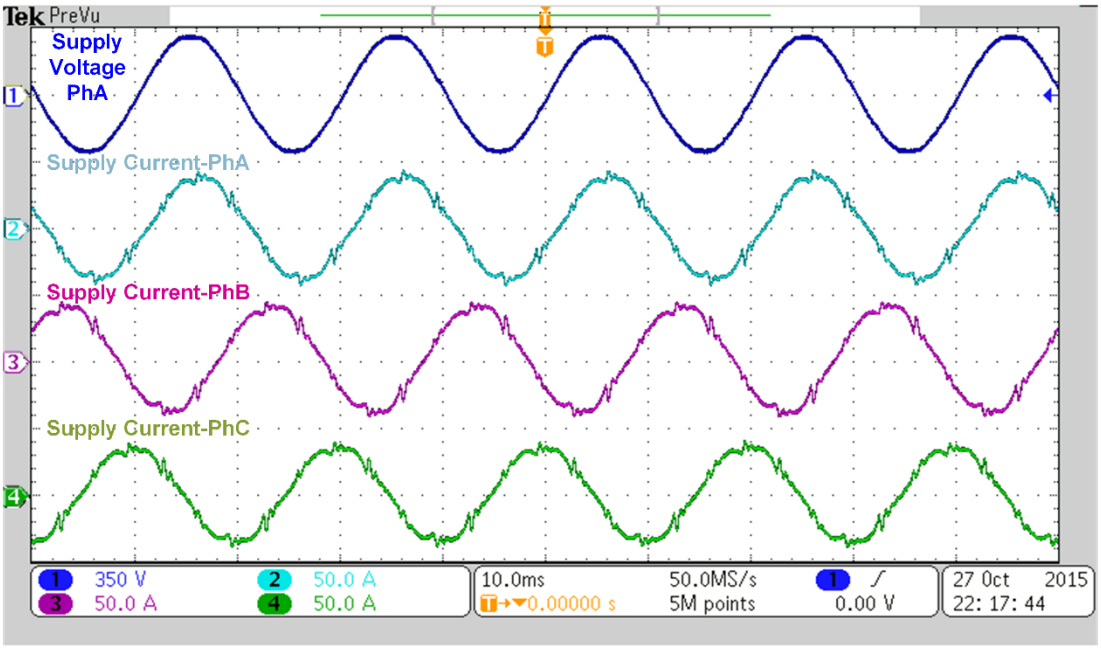


Figure 5.24. Supply voltage and current waveforms during the operation of conventional FB + 5th harmonic FF harmonic controller

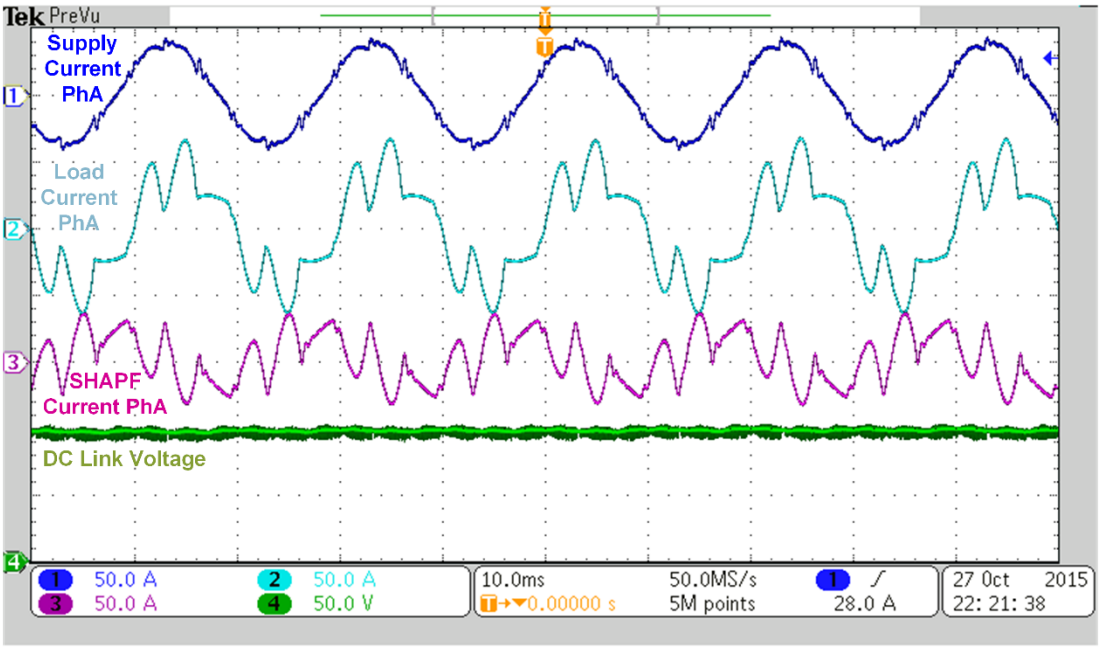


Figure 5.25. Current and dc link voltage waveforms during the operation of conventional FB + 5th harmonic FF harmonic controller

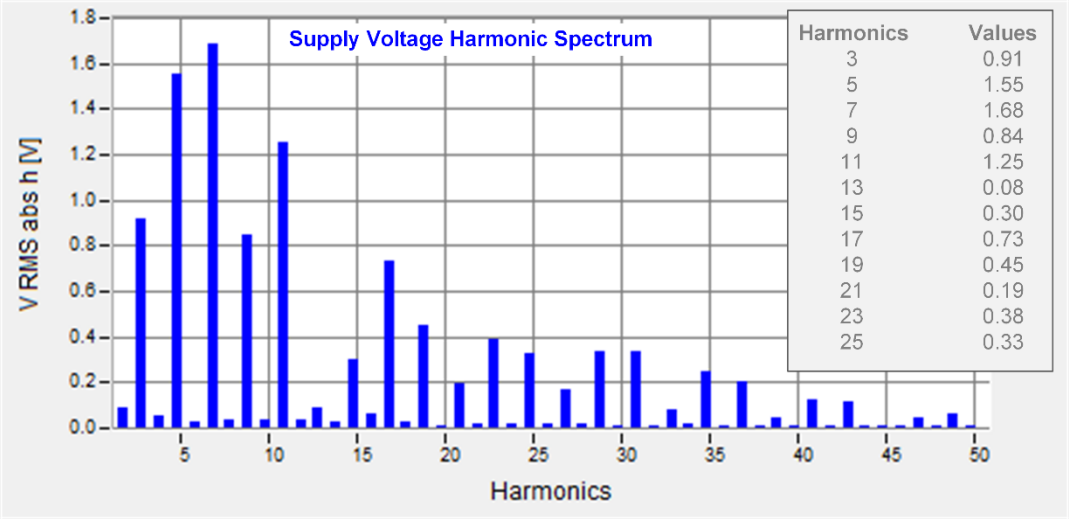


Figure 5.26. Supply voltage harmonic spectrum during the operation of conventional FB + 5th harmonic FF harmonic controller

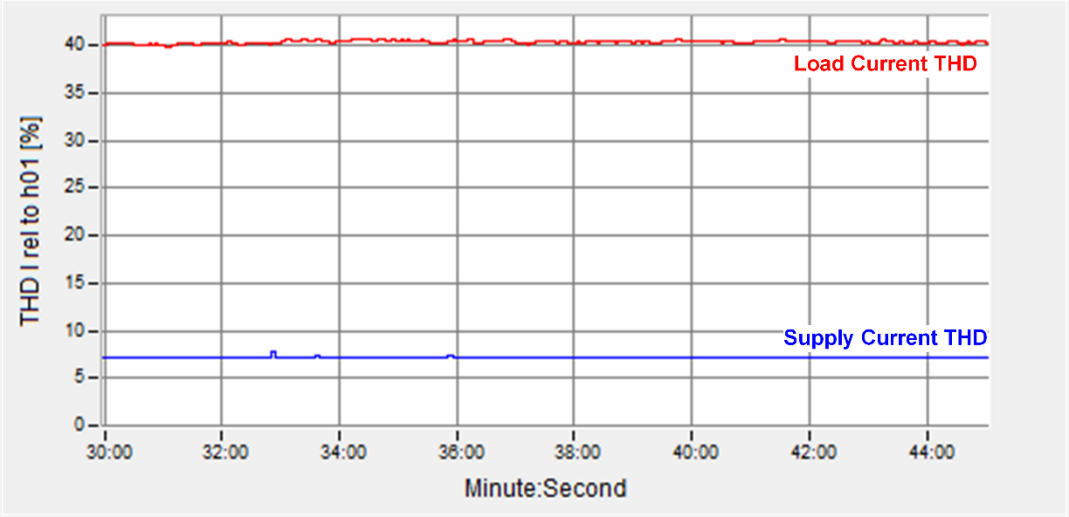


Figure 5.27. Supply and load current THD trend during the operation of conventional FB + 5th harmonic FF harmonic controller

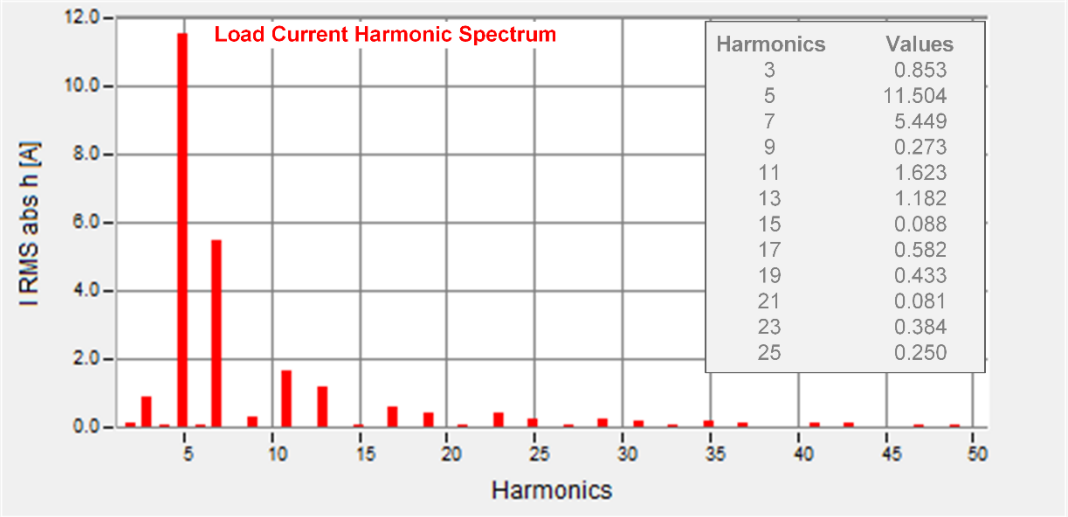


Figure 5.28. Load current harmonic spectrum during the operation of conventional FB + 5th harmonic FF harmonic controller

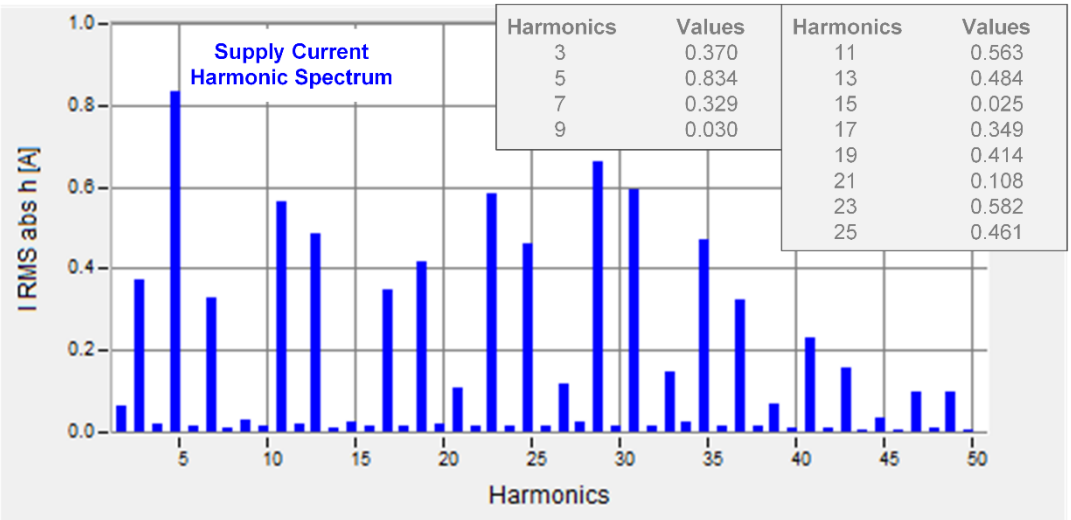


Figure 5.29. Supply current harmonic spectrum during the operation of conventional FB + 5th harmonic FF harmonic controller

Although this control approach shows a sufficient harmonic filtering performance, the effect of the feedforward loop does not show the expected performance on the 5th current harmonic. It is shown from the supply current harmonic spectrum in Figure 5.26 that the average value of the 5th harmonic in the supply current is 0.83A. There may be three main reasons of this undesired performance of the feedforward loop. The one of these reasons is the tolerance values of PF filter components. This causes an error in the calculation of voltage reference in the

feedforward loop. However, this problem is minimized by obtaining the actual values of PF components with the measurements. The second reason is the phase error of the 5^{th} load current harmonic in the current measurement circuitry. This problem is also compensated with in the dq transformation of feedforward control loop. The third reason which is the challenging one is the voltage harmonic in the supply voltage. The 5^{th} harmonic impedance of PF is 1.66Ω which is quite low so that the 5^{th} harmonic in the supply voltage can cause a performance degradation even if it exists in low magnitudes. In the feedback+5^{th} harmonic feedforward controller, the feedforward loop has no effect on the supply voltage harmonics because it only generates a required compensation voltage reference signal with using the load current harmonic and the PF impedance. On the other hand, the effect of the voltage harmonics can be eliminated with the increasing value of the feedback gain, *K* of the feedback loop as mentioned in theoretical calculations given in Section 3.2.1.1. However, the increase of *K* causes instability problems as discussed in the previous case so, the feedback controller shows a limited performance on the suppressing the effect of voltage harmonics. The voltage harmonic should be detected and added to voltage reference of SHAPF for the solution of this problem but it increases the complexity and also the computation load of the control.

It is shown from Figure 5.23 that the 5^{th} harmonic average value of the supply voltage is 1.55V during the PQ measurements of this case. Even though this value of the supply harmonics seems as low, it can cause a remarkable effect with respect to phase angle difference between the supply voltage harmonic and the reference voltage generated by the controller.

5.3.3. Case 3: Harmonic Compensation Performance of Proposed Individual Harmonic Elimination Based Feedback Controller

In this case, the harmonic compensation performance of the proposed individual harmonic compensation controller is presented. In order to compare the performance of the proposed individual harmonic elimination based feedback controller with the conventional controllers on equal terms, the reactive power

compensation controller and the adaptive dc link reference generation method of the proposed controller method are disabled and the dc link reference value is set to 100V.

The supply voltage and current waveforms are shown in Figure 5.30. The supply, load and SHAPF currents and the dc link voltage waveforms are given in Figure 5.31. The supply voltage harmonic spectrum, the supply and load current THD trends, the load current harmonic spectrum and the supply current harmonic spectrum are presented in Figure 5.32, 5.33, 5.34 and 5.35, respectively.

It is shown from the experimental results that SHAPF prototype holds the average values of dominant harmonics of the load group up to 25th harmonic under 0.1A with the proposed harmonic compensation controller. The proposed controller provides a much better filtering performance than the conventional methods. It decreases the supply current THD from 41.2% to 3.44%. Moreover the amplification of 23rd and 25th harmonics in supply current is taken under control and an effective filtering performance is provided close to 90% in these harmonics.

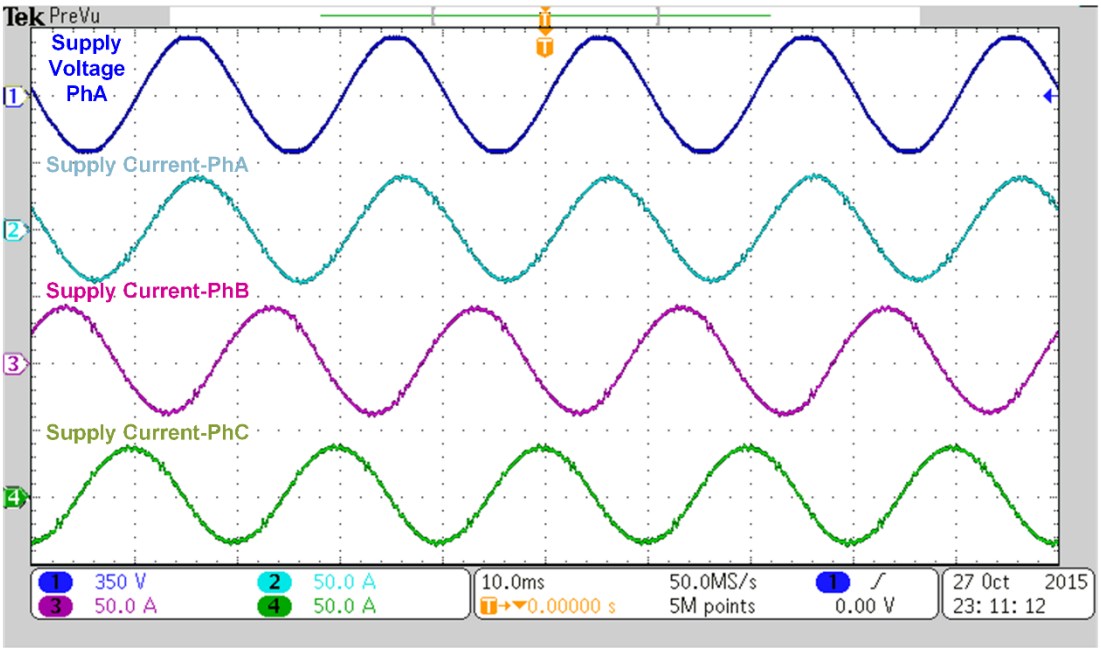


Figure 5.30. Supply voltage and current waveforms during the operation of proposed individual harmonic based FB controller

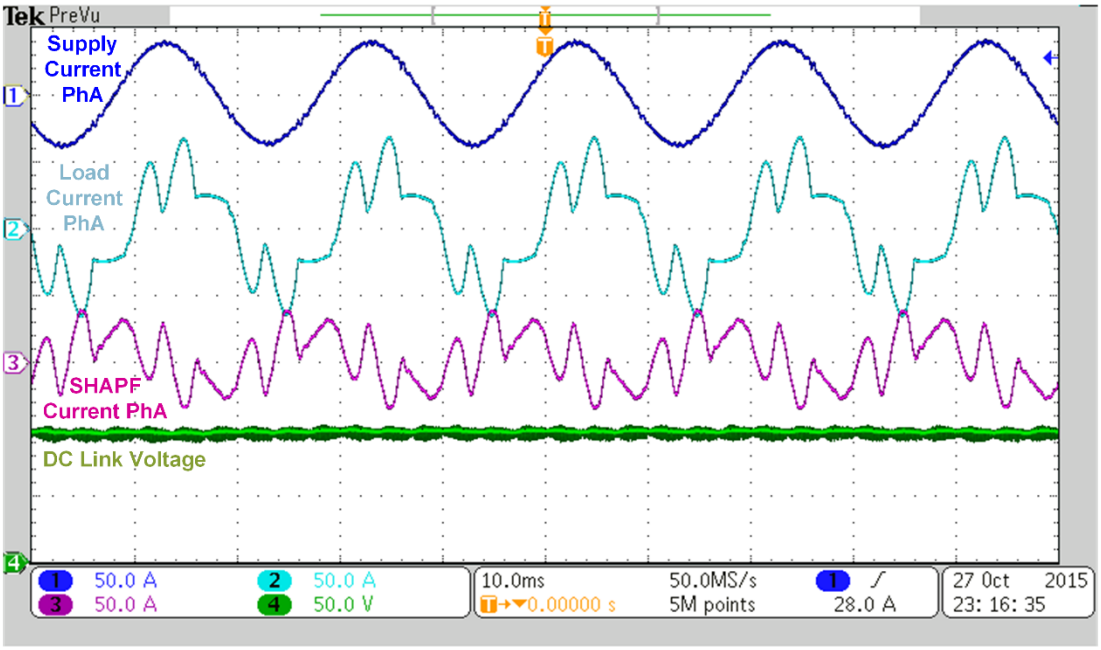


Figure 5.31. Current and dc link voltage waveforms during the operation of proposed individual harmonic based FB controller

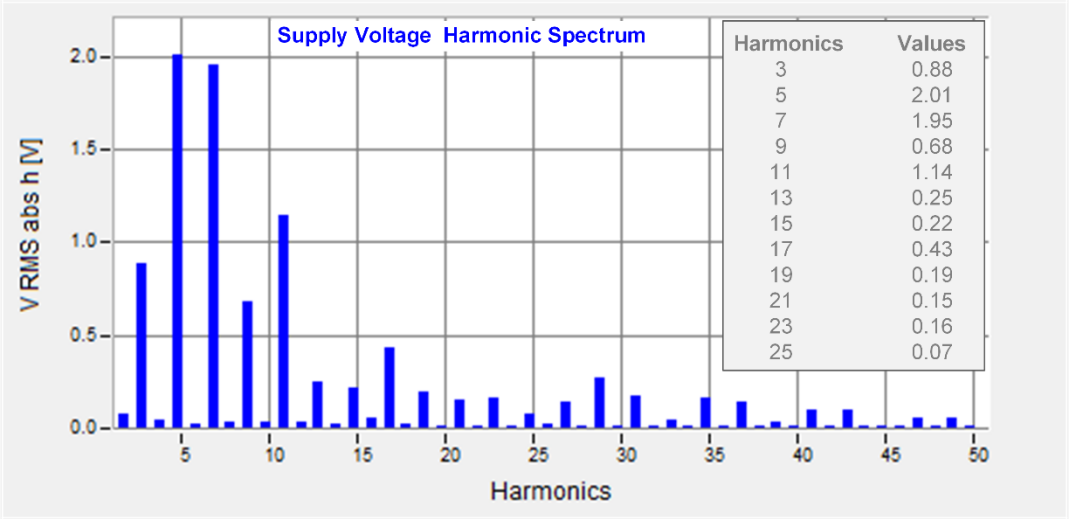


Figure 5.32. Supply voltage harmonic spectrum during the operation of proposed individual harmonic based FB controller

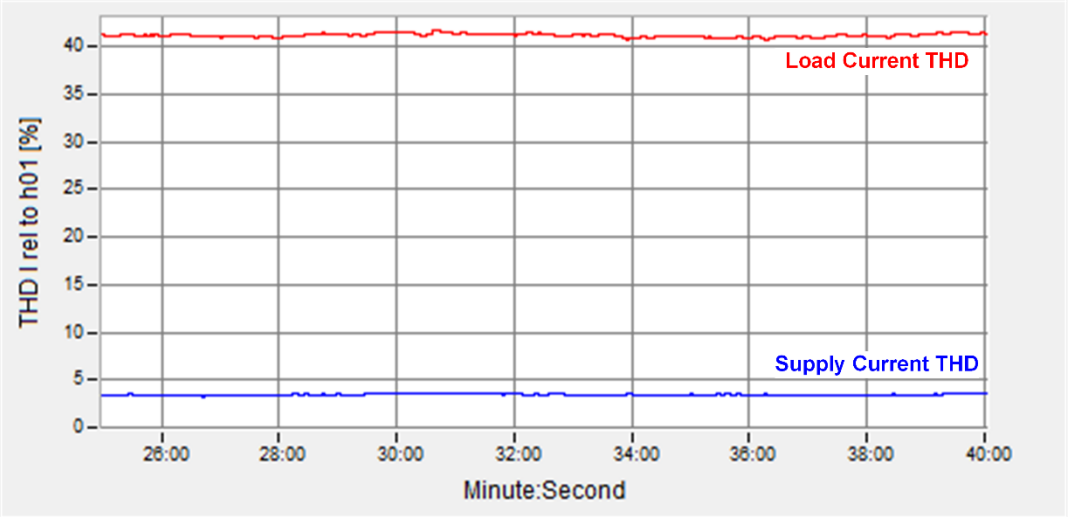


Figure 5.33. Supply and load current THD trend during the operation of proposed individual harmonic based FB controller

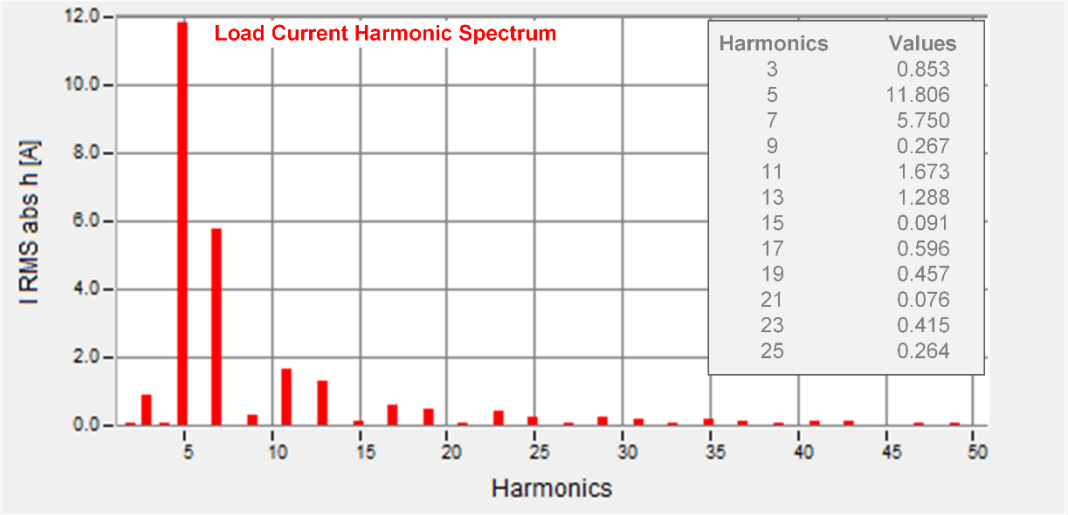


Figure 5.34. Load current harmonic spectrum during the operation of proposed individual harmonic based FB controller

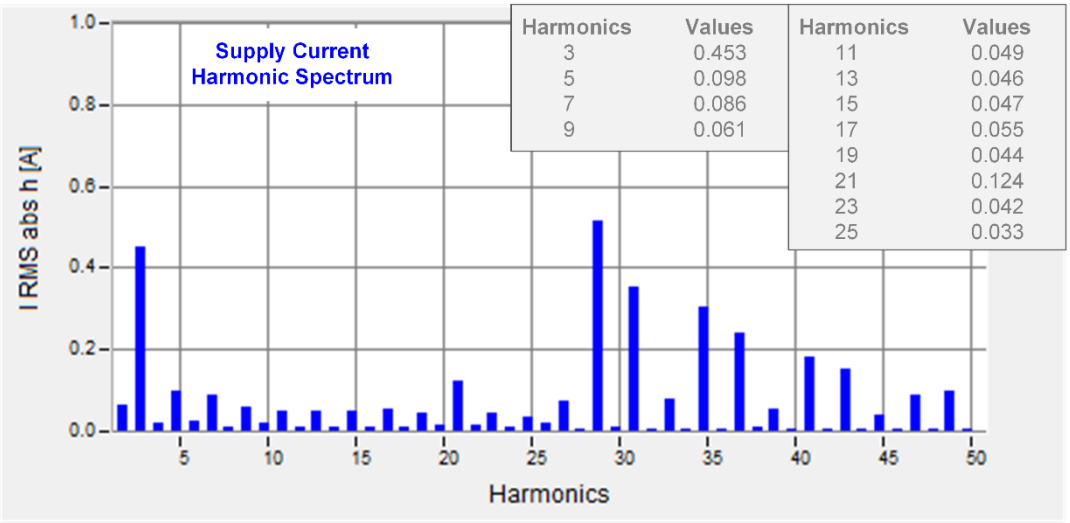


Figure 5.35. Supply current harmonic spectrum during the operation of proposed individual harmonic based FB controller

In this proposed harmonic compensation method, PI controllers are used in each d and q components of each individual harmonics up to 25th harmonic. PI controllers set a reference voltage for the d and q components of each individual harmonics in order to minimize the harmonics in the supply currents. Thus, the disturbance caused by the tolerance values of PF components, the phase errors in the measurements and the presence of voltage harmonics in the supply voltage are suppressed by PI controllers as shown in the experimental results.

5.3.4. Summary

In this section, the harmonic compensation performance of the proposed individual harmonic compensation method is compared with the conventional feedback harmonic controller and feedback + 5th harmonic feedforward controller on the equal terms.

The experimental harmonic compensation performance of SHAPF prototype with the conventional controllers and the proposed harmonic compensation controller is summarized in Table 5.3. It is obviously shown in the performance summary table that SHAPF shows an excellent harmonic compensation performance with the

proposed control method and the performance of the proposed method has much better performance than the conventional control methods.

Table 5.3. Summary of SHAPF prototype performance with the conventional controllers and the proposed harmonic compensation controller

	Feedback Controller			Feedback+5th Harmonic Feedforward Controller			Proposed Controller		
	I_L	I_S	Fil. Rate	I_L	I_S	Fil. Rate	I_L	I_S	Fil. Rate
Fun.	32A	26.1A	-	32.1A	26.1A	-	32.4A	26.3A	-
5th	11.54A	1.80A	84.4%	11.5A	0.83A	92.7%	11.8A	0.098A	99.1%
7th	5.51A	1.35A	93.6%	5.44A	0.33A	93.9%	5.75A	0.086A	98.5%
11th	1.56A	0.55A	64.7%	1.62A	0.56A	65.4%	1.67A	0.049A	97.0%
13th	1.20A	0.47A	60.8%	1.18A	0.48A	59.3%	1.28A	0.046A	96.4%
17th	0.61A	0.40A	34.4%	0.58A	0.35A	39.6%	0.59A	0.055A	90.6%
19th	0.41A	0.36A	12.2%	0.43A	0.41A	4.65%	0.45A	0.044A	90.2%
23th	0.37A	0.56A	-	0.38A	0.58A	-	0.41A	0.042A	89.7%
25th	0.25A	0.43A	-	0.25A	0.46A	-	0.26A	0.033A	87.3%
THD	40.6%	9.36%	-	40.4%	7.19%	-	41.2%	3.44%	-

The comparison study of the conventional control methods and the proposed method presented in this section is summarized with following statements;

- The performance of the conventional feedback controller is directly proportional to the value of the feedback gain, *K*. According to the theoretical analysis, if the value of *K* goes to the infinity, SHAPF eliminates all of the load current harmonics at the supply side. However, the increase of *K* is limited to a certain level in the real implementation because of the delays of reference generation methods, the delays in the switching operation, the phase errors of the measurement circuitries and etc. Particularly, the phase errors of high order harmonics in the measurements cause the instability after a certain level of *K*. The phase errors of harmonics can be compensated in the controller with the individual harmonic detection methods but unfortunately, it cannot be compensated with the fundamental extraction based harmonic detection methods used in the conventional feedback method. This situation is observed

in the experimental results of SHAPF prototype with the conventional feedback controller. It is shown in the experimental results that SHAPF prototype shows maximum harmonic filtering performance in low order harmonics and ensures the minimum source current THD with the selected *K* value. Nevertheless, this value of *K* causes instability in the compensation of high order harmonics with the amplification of 23^{rd} and 25^{th} current harmonics in the source side. Although the conventional feedback control method presents a remarkable compensation performance in the low order dominant harmonics, this performance may be insufficient for many applications. Especially, the conventional feedback control method cannot show effective performance in the most dominant 5^{th} current harmonic, because of the cut-off frequency of PF.

- The feedback + 5^{th} harmonic feedforward controller is proposed to improve the performance of the conventional feedback controller in 5^{th} current harmonic. Although this feedforward approach improves the filtering performance of SHAPF in the 5^{th} current harmonic, the experimental results are far away from the theoretical performance of this approach. The tolerance of PF components, the phase error in the measurement of 5^{th} current harmonic and the existence of the voltage harmonics are the main obstacles on the expected performance of the feedforward loop. The tolerance of PF components and the phase error in the measurements can be compensated with the preliminary measurements and making settings on the controller. However, the effect of voltage harmonics is directly related with the capability of the controller. The feedforward controller has not any ability to reducing the effect of voltage harmonics. The feedback controller can theoretically perform a successful suppression for the effect of voltage harmonics with the increasing value of the feedback gain of controller. Nonetheless, the increasing value of the feedback gain causes stability problems in practical applications so that the feedback control loop presents a limited performance in the avoidance of the performance degradation caused by the voltage harmonics.

- In the proposed individual harmonic elimination based feedback controller, PI controllers are added to each d and q components of individual harmonics in order to increase the performance of SHAPF prototype. Thanks to PI controllers used in the proposed controller, SHAPF prototype are not affected from the tolerance values of PF components, the phase errors in the measurements and the presence of voltage harmonics in the supply voltage. It is shown from the experimental results that SHAPF presents an excellent performance in the compensation of the dominant harmonics of the six pulse rectifier up to 25^{th} harmonics when it is compared with the conventional feedback and feedback+5^{th} harmonic feedforward controllers.

5.4. Dynamic Harmonic and Reactive Power Compensation with Adaptive DC Link Voltage

In this section of the experimental results, the performance of SHAPF prototype with the proposed controller which can perform dynamic harmonic and reactive power compensation with adaptive dc link voltage is investigated. The performance of SHAPF prototype is presented with two detailed case studies as;

- Case 1: Capacitive Operation of VSC
- Case 2: Inductive Operation of VSC

During the dynamic harmonic and reactive power compensation of the load group, the dc link voltage reference generation method of the proposed controller calculates the reference dc link voltage adaptively to the harmonic and the reactive power compensation requirements of the load. The dc link voltage controller sets the dc link voltage to this reference value in order to decrease the losses of SHAPF in low power compensation states.

5.4.1. Case 1: Capacitive Operation of VSC

In this case, the performance of SHAPF prototype is investigated in the capacitive operation of VSC. If the inductive reactive power of the load is higher than the reactive power capacity of PF, VSC is operated in the capacitive mode to supply the reactive power demand of the load. In order to investigate the steady state and dynamic performance of SHAPF prototype in the capacitive operation of VSC, the three different load state is formed with the load group. The states of the load group applied in this case are presented in Table 5.4.

Table 5.4. Load states in the capacitive mode operation of VSC

State No	Switched-On Loads in Load Group	
1	Rectifiers:	Inductive Loads:
	Rectifier 1	Step 1 - 5kVAr
	Rectifier 2	Step 2 - 2kVAr
	Rectifier 3	Step 3 - 2kVAr
		Step 4 - 1kVAr
2	Rectifiers:	Inductive Loads:
	Rectifier 1	Step 1 - 5kVAr
	Rectifier 2	Step 2 - 2kVAr
		Step 4 - 1kVAr
3	Rectifiers:	Inductive Loads:
	Rectifier 1	Step 1 - 5kVAr
	Rectifier 2	Step 2 - 2kVAr
	Rectifier 3	Step 3 - 2kVAr

The active and reactive power trends of the supply, load and SHAPF prototype during the capacitive mode operation of VSC are presented in Figures 5.36 and 5.37 respectively. The supply and the load current THD trends are introduced in Figure 5.38. The load states are demonstrated in the figures of active and reactive power and current THD trends.

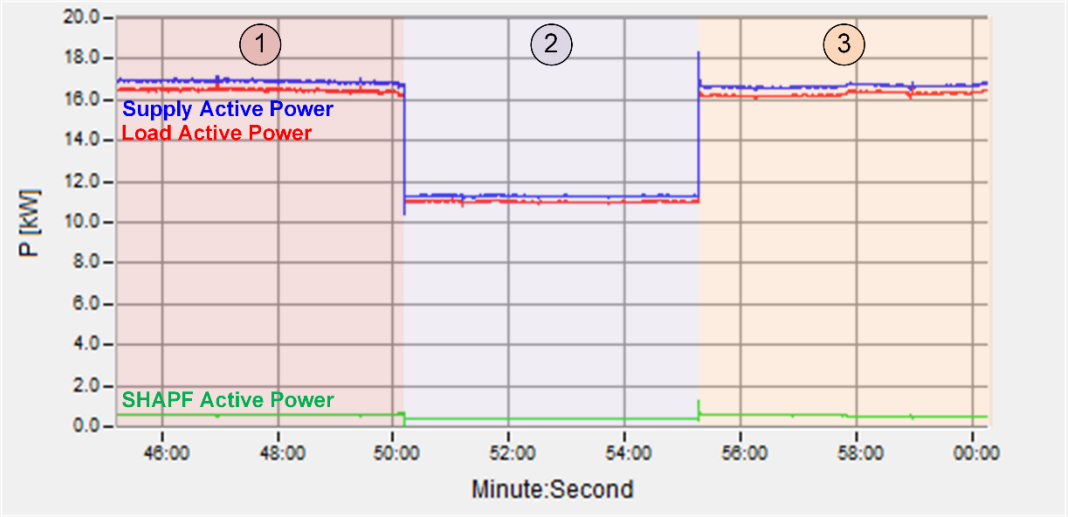


Figure 5.36. Active power trends of supply, load and SHAPF during the capacitive mode operation

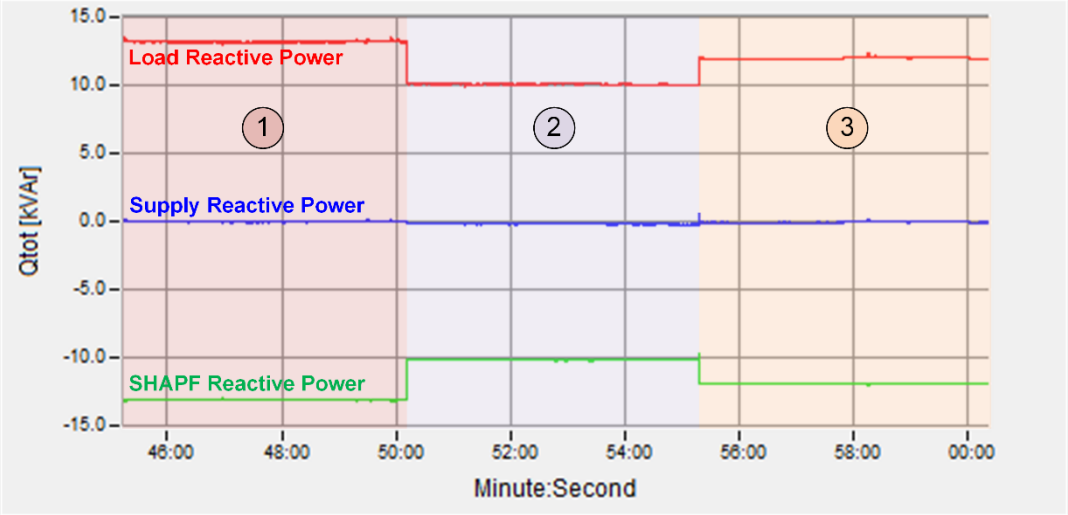


Figure 5.37. Reactive power trends of supply, load and SHAPF during the capacitive mode operation

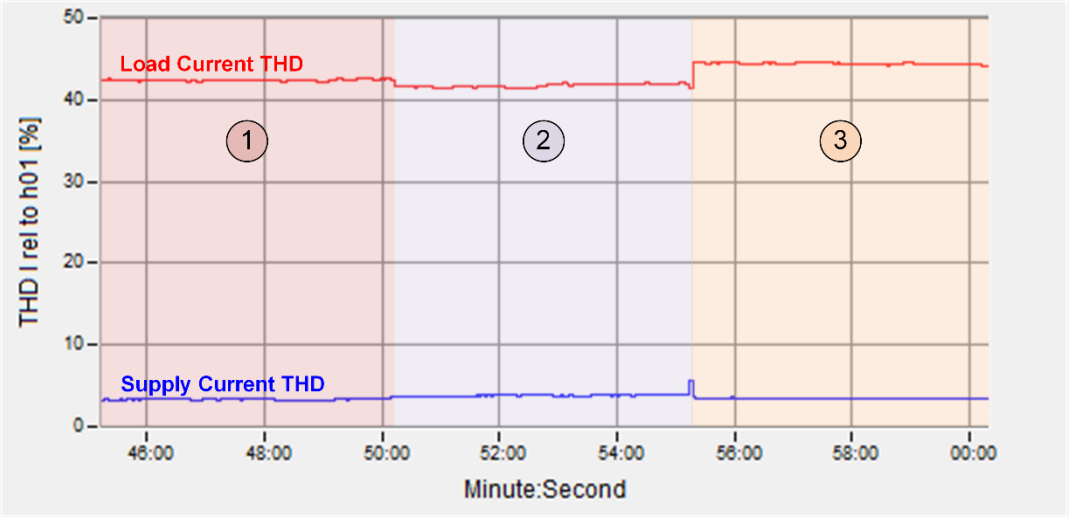


Figure 5.38. THD trends of supply and load currents during the capacitive mode operation

The supply voltage and the current waveforms and the supply, the load and SHAPF currents and the dc link voltage waveforms during the 1st state are presented in Figures 5.39 and 5.40, respectively. The load and supply current harmonic spectrum during the 1st state are given in Figure 5.41 and 5.42, respectively. In this state, the average active power and the reactive power of the load group are 16.3kW and 13.1kVAr at 221.7V supply voltage. The rms value of dominant current harmonics and the current THD of the load group are nearly 13.2A and 42.4%. The PF part of SHAPF supplies close to 9.45kVAr capacitive reactive power at 221.7V supply voltage. The dc link voltage of VSC is determined and set to 295V by the dc link reference voltage calculation method and the dc link voltage controller to compensate 13.2A current harmonics and the remaining 3.65kVAr inductive reactive power of the load group. SHAPF decreases the supply current THD from 42.4% to 3.31% and keeps the supply reactive power between ±100VAr in the steady state operation.

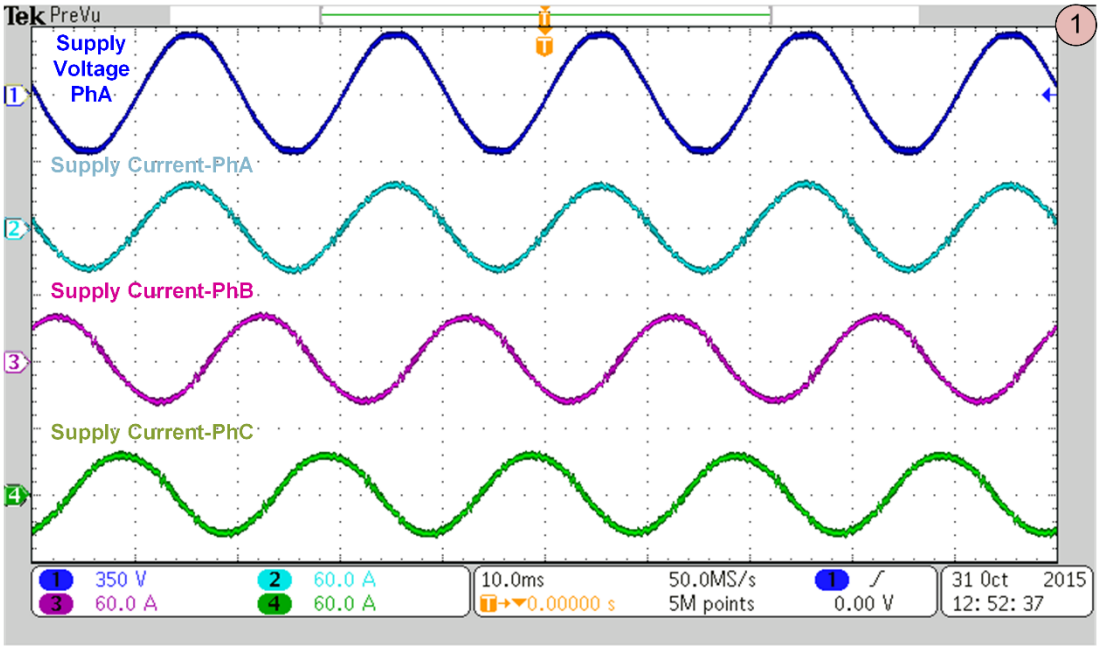


Figure 5.39. Supply voltage and current waveforms during the 1st state of capacitive mode operation

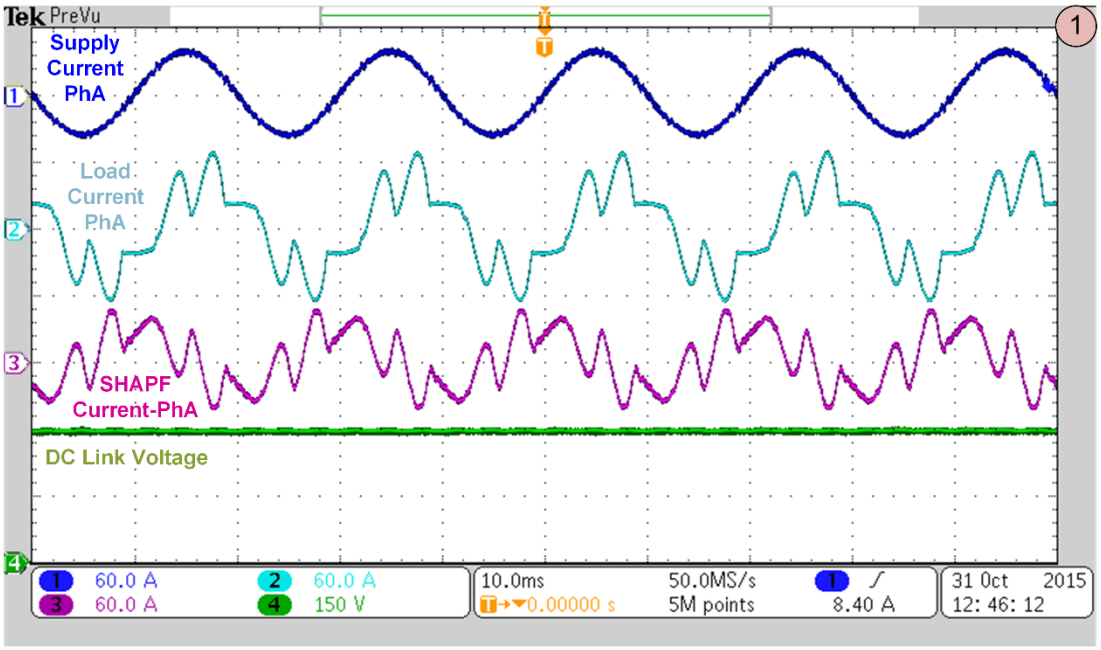


Figure 5.40. Supply current, load current, SHAPF current and dc link voltage waveforms during the 1st state of capacitive mode operation

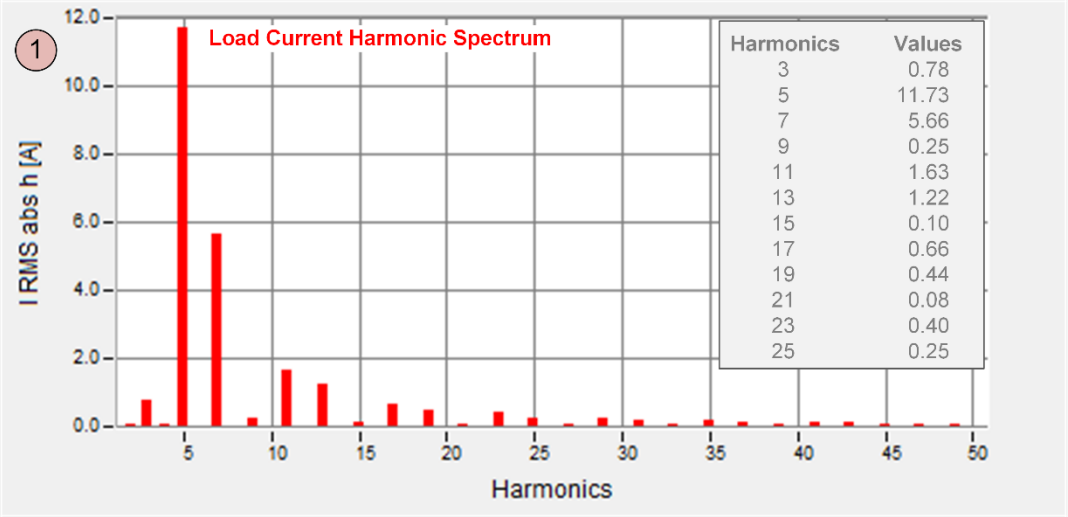


Figure 5.41. Load current harmonic spectrum during the 1st state of capacitive mode operation

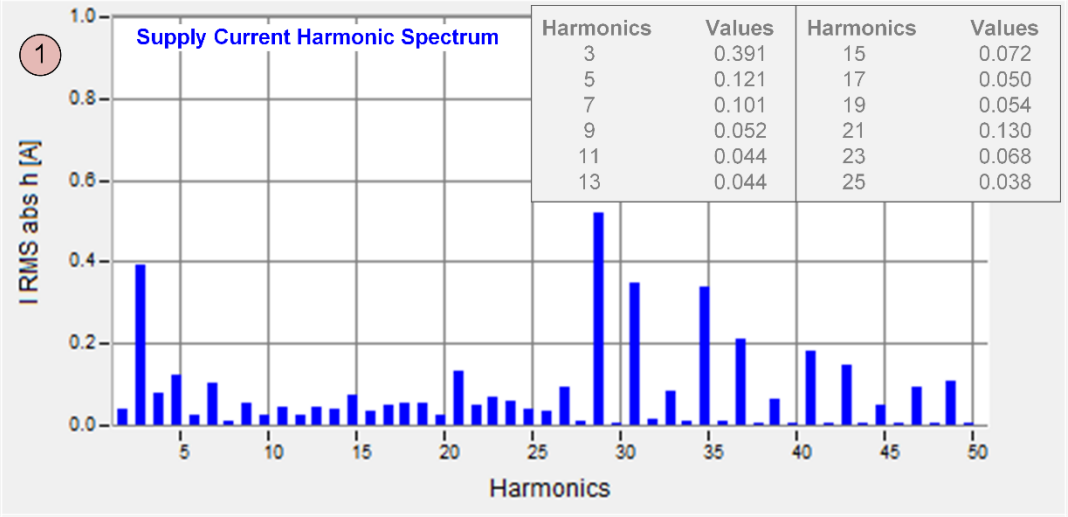


Figure 5.42. Supply current harmonic spectrum during the 1st state of capacitive mode operation

In Figure 5.43, the supply current, the load current, SHAPF current and the dc link voltage waveforms during the load change from the 1st state to 2nd state are given. The supply voltage and the current waveforms and the supply, the load and SHAPF currents and the dc link voltage waveforms during the 2nd state are presented in Figures 5.44 and 5.45, respectively. The load and supply current harmonic spectrum during the 2nd state are given in Figure 5.46 and 5.47, respectively. In the 2nd state, the active power and the reactive power of the load group decreases to 11kW and 10.1kVAr at

around 223.5V supply voltage. The rms value of the dominant load group current harmonics decreases to 9.13A and the current THD of the load group is about 41.7%. The PF part of SHAPF supplies the capacitive reactive power of 9.6kVAr at 223.5V supply and only 0.5kVAr remains for the compensation of VSC. In order to compensate the current harmonics of 9.13A and the remaining reactive power of 0.5kVAr, the required dc link voltage of VSC is calculated as 90V. During the load transition from the 1st state to 2nd state, SHAPF discharges the dc link voltage from 295V to 90V under 300ms with 20% overshoot to decrease the losses. In this load state, SHAPF decreases the supply current THD to 3.8% and keeps the supply reactive power between ±100VAr.

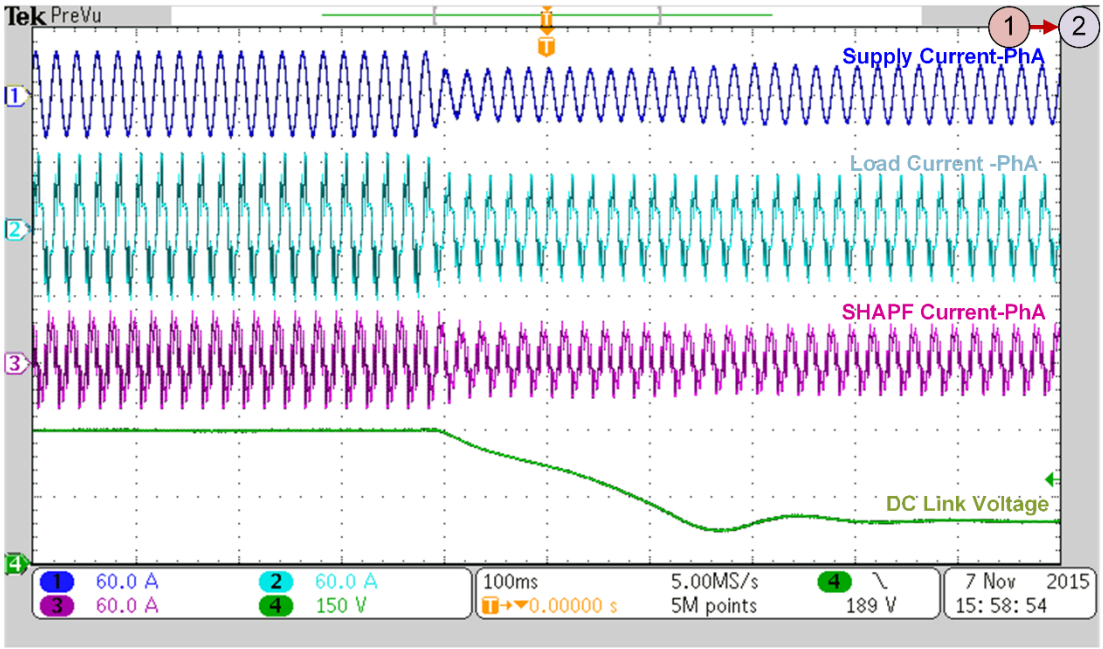


Figure 5.43. Supply current, load current, SHAPF current and dc link voltage waveforms during the transition from 1st state to 2nd state of capacitive mode operation

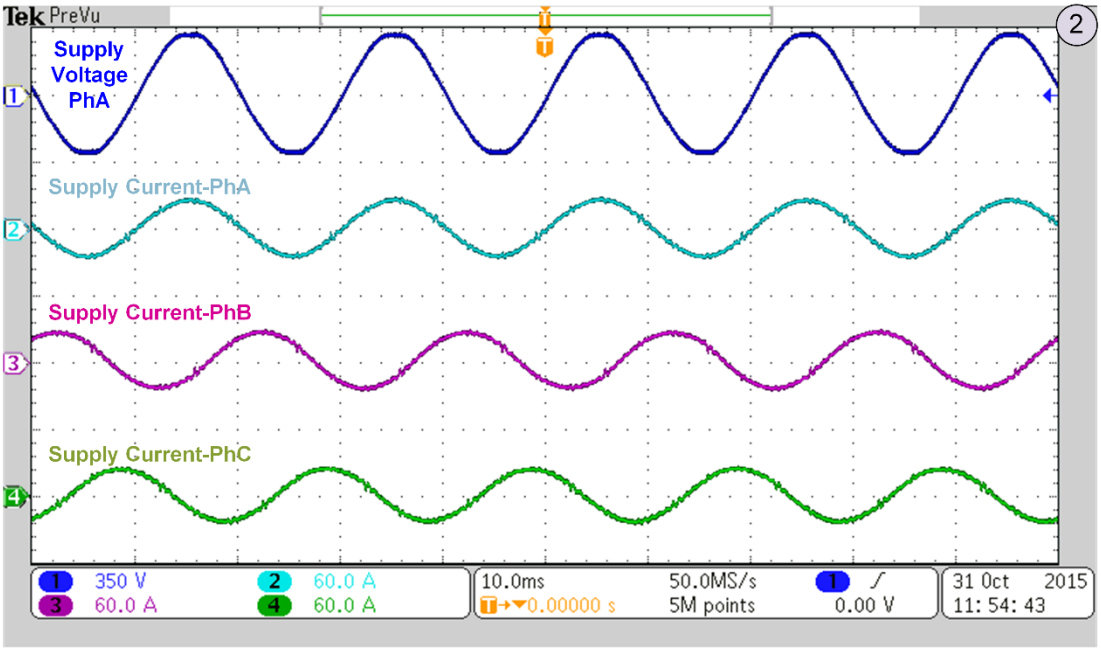


Figure 5.44. Supply voltage and current waveforms during the 2nd state of capacitive mode operation

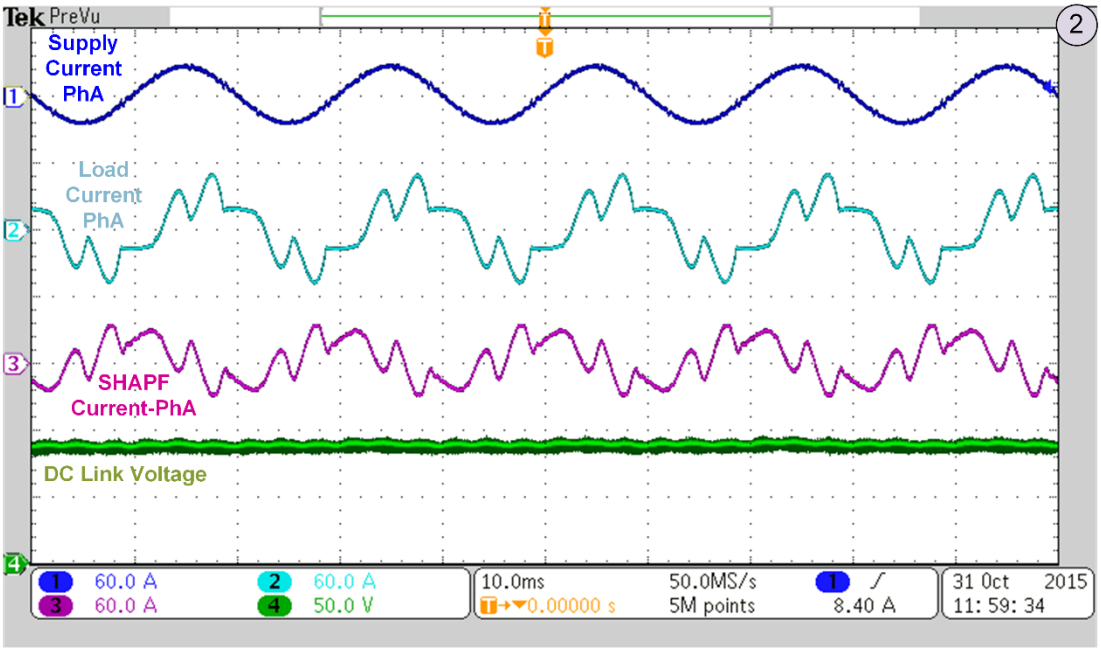


Figure 5.45. Supply current, load current, SHAPF current and dc link voltage waveforms during the 2nd state of capacitive mode operation

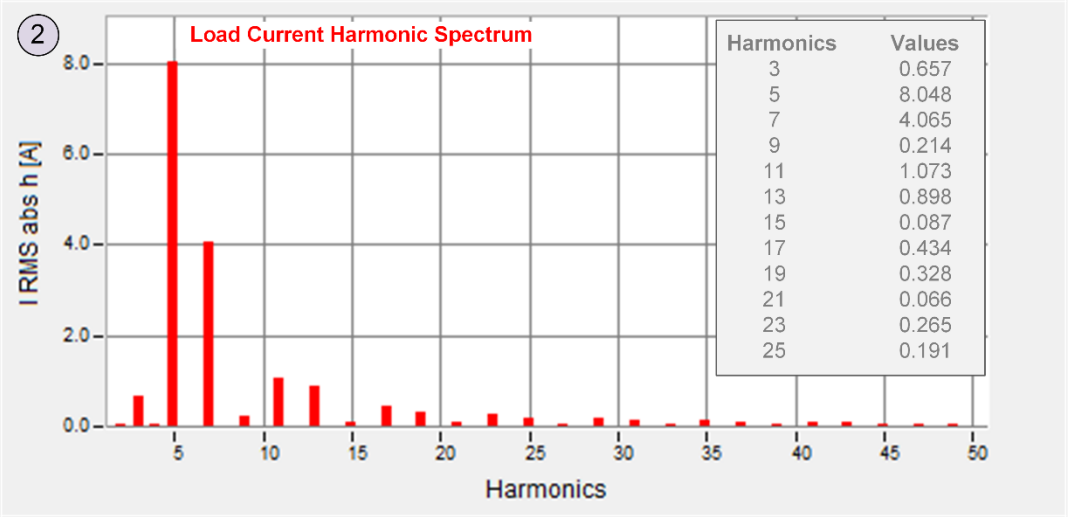


Figure 5.46. Load current harmonic spectrum during the 2nd state of capacitive mode operation

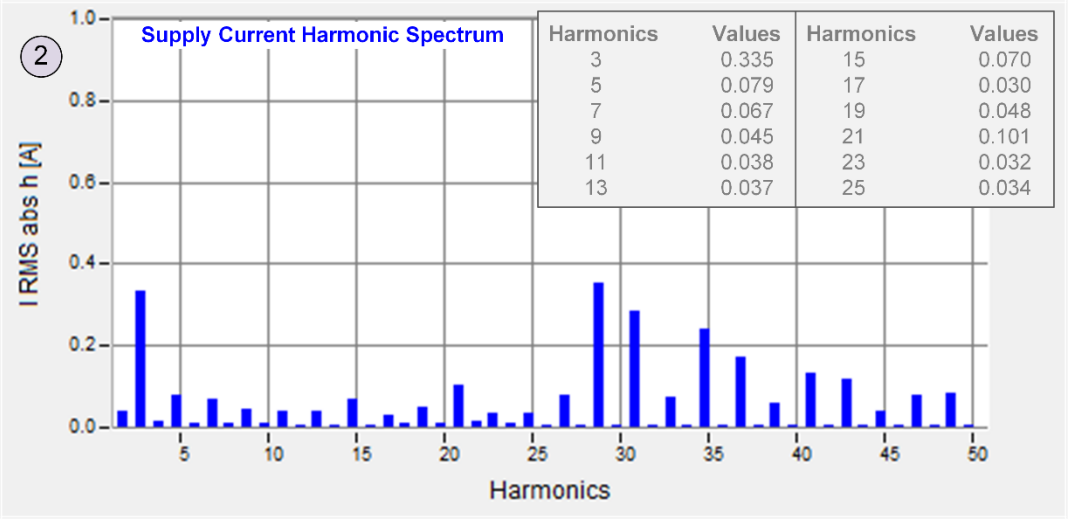


Figure 5.47. Supply current harmonic spectrum during the 2nd state of capacitive mode operation

In Figure 5.48, the supply current, the load current, SHAPF current and the dc link voltage waveforms during the load change from the 2nd state to 3rd state are given. The supply voltage and the current waveforms and the supply, the load and SHAPF currents and the dc link voltage waveforms during the 3rd state are presented in Figures 5.49 and 5.50, respectively. The load and supply current harmonic spectrum during the 3rd state are given in Figure 5.51 and 5.52, respectively. In the 3rd state, the active power and the reactive power of the load group increases to 16.2kW and 11.9kVAr at

around 221.3V supply voltage. The rms value of current harmonics and the current THD of the load group increases to 13.4A and is 44.4%. The PF part of SHAPF supplies approximately 9.42kVAr capacitive reactive power at 221.3V supply voltage and VSC compensates the remaining reactive power of 2.48kVAr. In order to compensate the current harmonic and the reactive power of the load group in the 3rd state, the required dc link voltage of is determined as 215V for VSC. During the load transition from the 2nd state to 3rd state, the dc link voltage of SHAPF is increased from 90V to 215V under 200ms with 10% overshoot to perform the harmonic and reactive power compensation of the load group. In addition, SHAPF shows a stable dynamic response against the high inrush current of the load group during the load transition. In this load state, SHAPF decreases the supply current THD from 44.4% to under 3.44% and keeps the supply reactive power between ±100VAr.

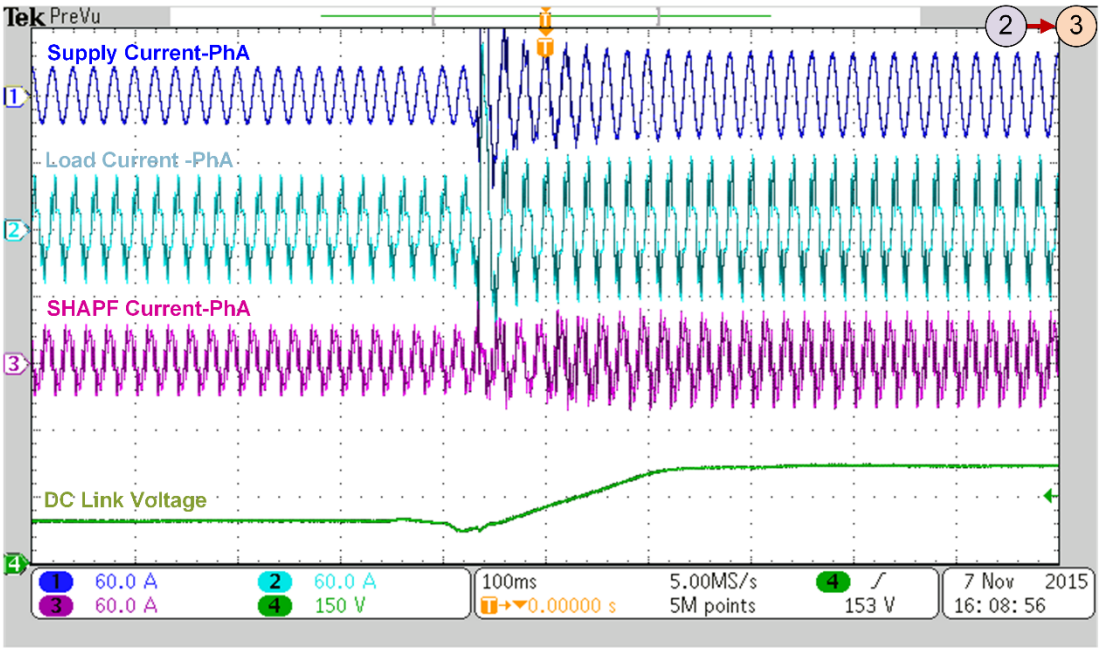


Figure 5.48. Supply current, load current, SHAPF current and dc link voltage waveforms during the transition from 2nd state to 3rd state of capacitive mode operation

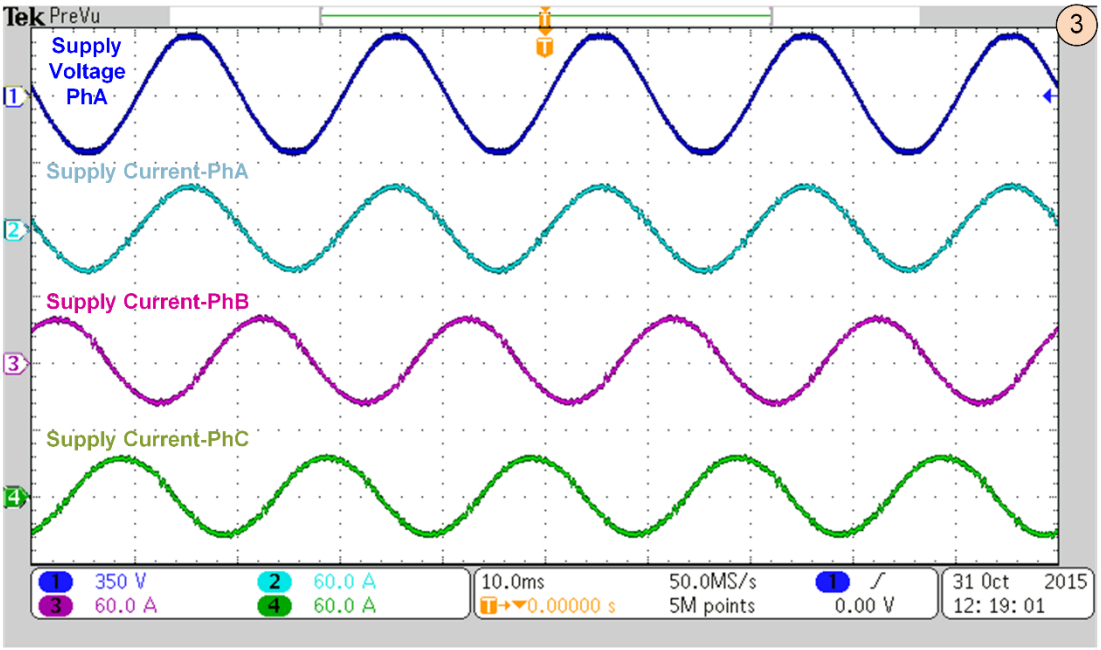


Figure 5.49. Supply voltage and current waveforms during the 3rd state of capacitive mode operation

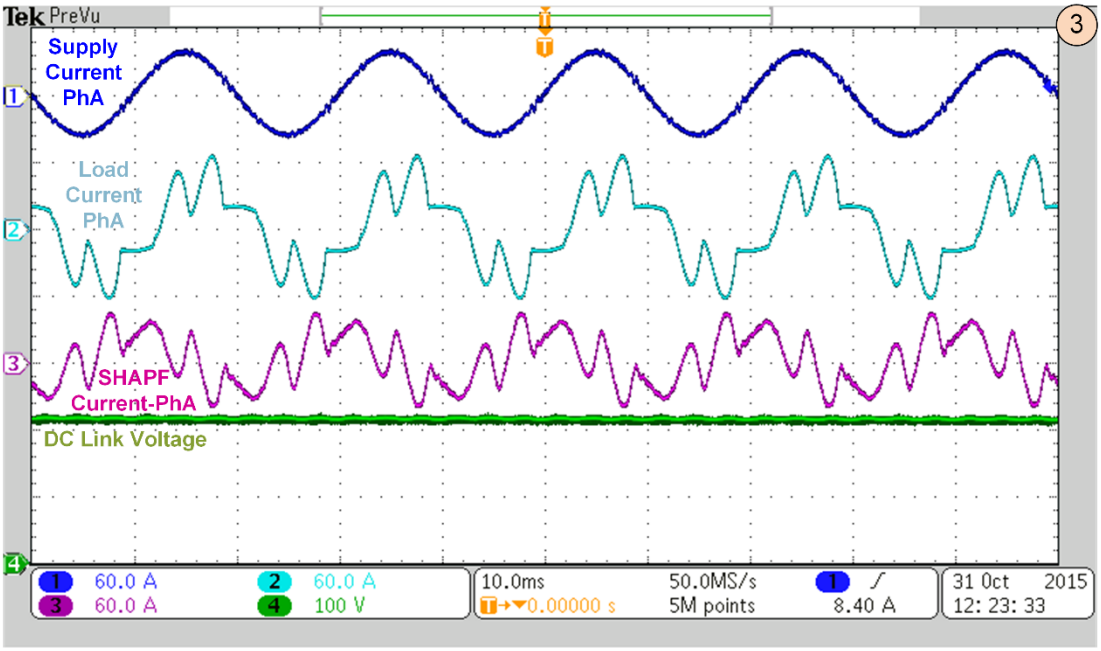


Figure 5.50. Supply current, load current, SHAPF current and dc link voltage waveforms during the 3rd state of capacitive mode operation

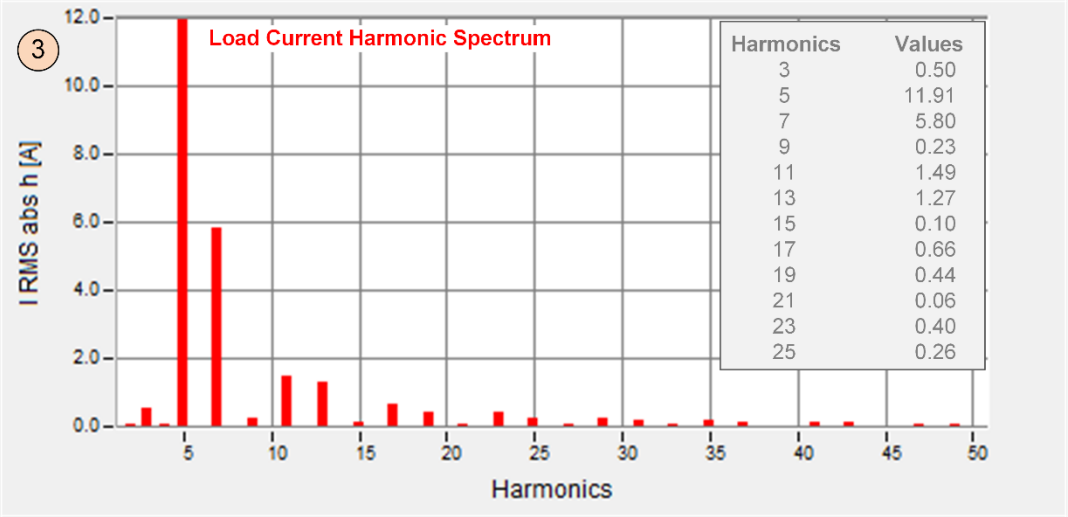


Figure 5.51. Load current harmonic spectrum during the 3rd state of capacitive mode operation

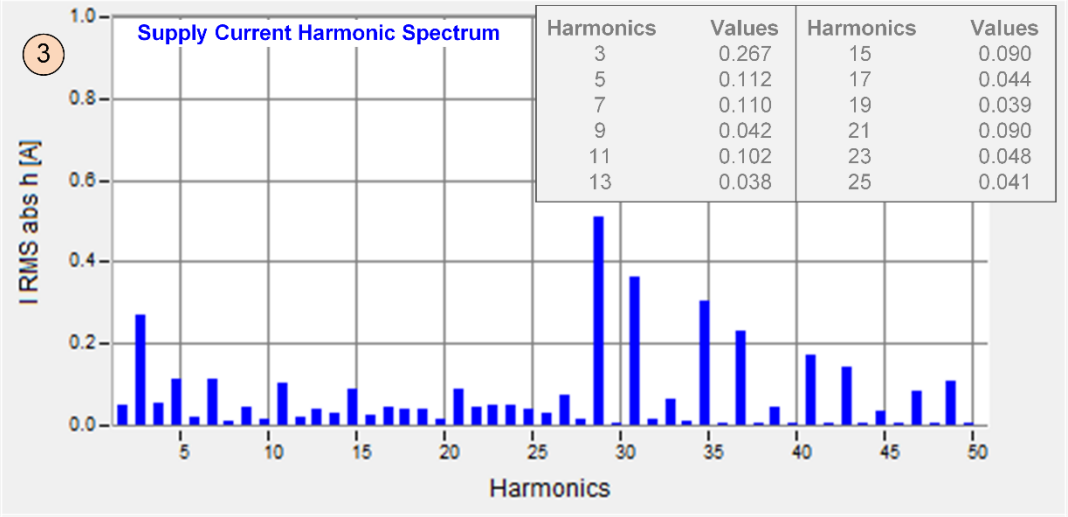


Figure 5.52. Supply current harmonic spectrum during the 3rd state of capacitive mode operation

5.4.2. Case 2: Inductive Operation of VSC

In this case, the dynamic harmonic and reactive power compensation performance of SHAPF prototype is investigated when the inductive reactive power compensation requirements of load group is lower than the reactive power capacity of PF. In this case, PF causes overcompensation and VSC must be operated in inductive mode with adaptive dc link voltage in order to supply the reactive power requirements

of the load group. In order to investigate the steady state and dynamic performance of SHAPF prototype in inductive operation of VSC, the three different load state is formed with the load group as in the capacitive mode operation case. The states of the load group applied in this case are presented in Table 5.5.

Table 5.5. Load states in the inductive mode operation of VSC

State No	Switched-On Loads in Load Group	
1	Rectifiers:	Inductive Loads:
	Rectifier 1	Step 2 - 2kVAr
		Step 3 - 2kVAr
		Step 4 - 1kVAr
		Step 5 - 1kVAr
2	Rectifiers:	Inductive Loads:
	Rectifier 1	Step 2 - 2kVAr
	Rectifier 2	Step 3 - 2kVAr
		Step 4 - 1kVAr
		Step 5 - 1kVAr
3	Rectifiers:	Inductive Loads:
	Rectifier 1	Step 2 - 2kVAr
	Rectifier 2	Step 4 - 1kVAr
	Rectifier 3	Step 5 - 1kVAr

The active and reactive power trends of the supply, load and SHAPF prototype during the inductive mode operation of VSC are presented in Figures 5.53 and 5.54, respectively. The supply and the load current THD trends are introduced in Figure 5.55. The load states are demonstrated in the figures of active and reactive power and current THD trends.

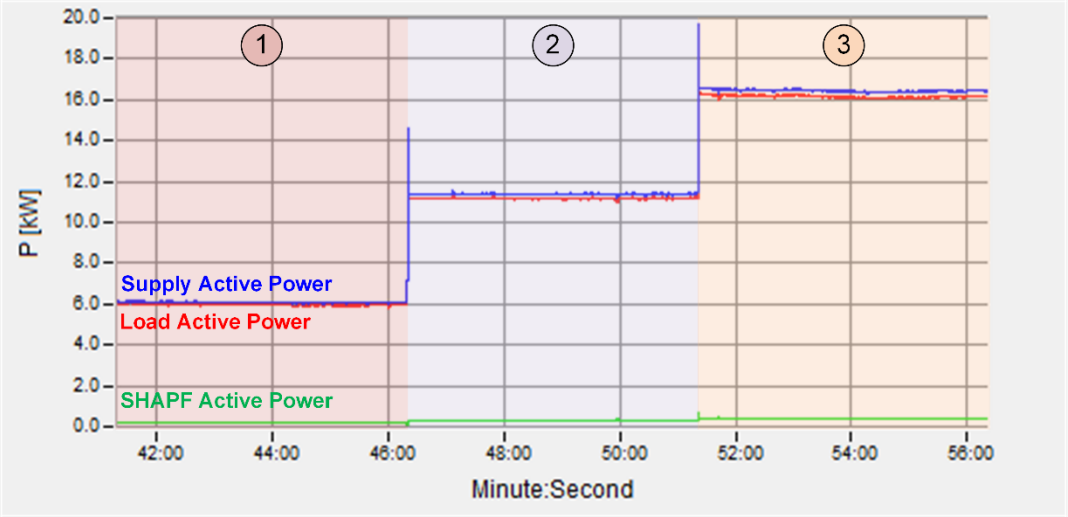


Figure 5.53. Active power trends of supply, load and SHAPF during the inductive mode operation

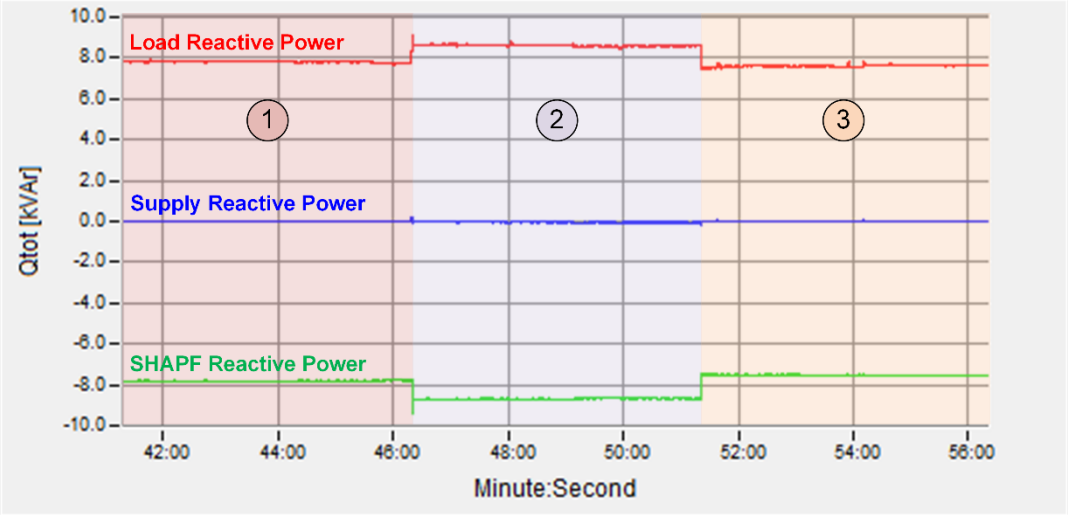


Figure 5.54. Reactive power trends of supply, load and SHAPF during the inductive mode operation

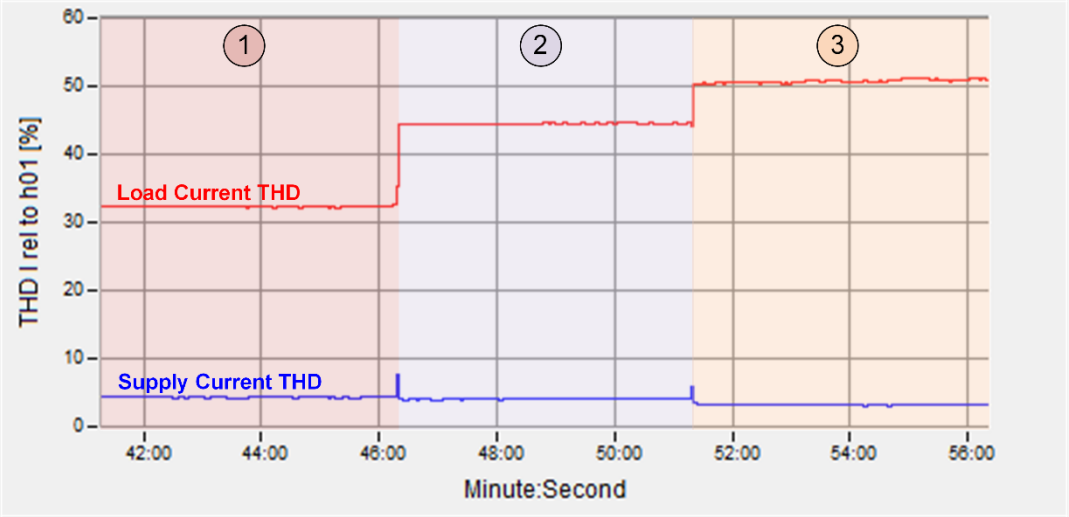


Figure 5.55. THD trends of supply and load currents during the inductive mode operation

The supply voltage and the current waveforms and the supply, the load and SHAPF currents and the dc link voltage waveforms during the 1st state are presented in Figures 5.56 and 5.57, respectively. The load and supply current harmonic spectrum during the 1st state are given in Figure 5.58 and 5.59, respectively. In the 1st state, the active power and the reactive power of the load group are 5.9kW and 7.8kVAr under 226.5V supply voltage. The rms value of dominant load current harmonics and the current THD of the load group are nearly 4.61A and 32.3%. PF supplies close to 9.9kVArkVAr capacitive reactive power. The dc link voltage of VSC is calculated and set to 153V by the proposed controller to compensate the current harmonics and the reactive power of the load group. VSC supplies the inductive reactive power of 2.1kVAr to prevent over compensation of PF and maintain the reactive power compensation requirements of the load. SHAPF decreases the supply current THD from 32.3% to 4.3% and keeps the supply reactive power between ±100VAr.

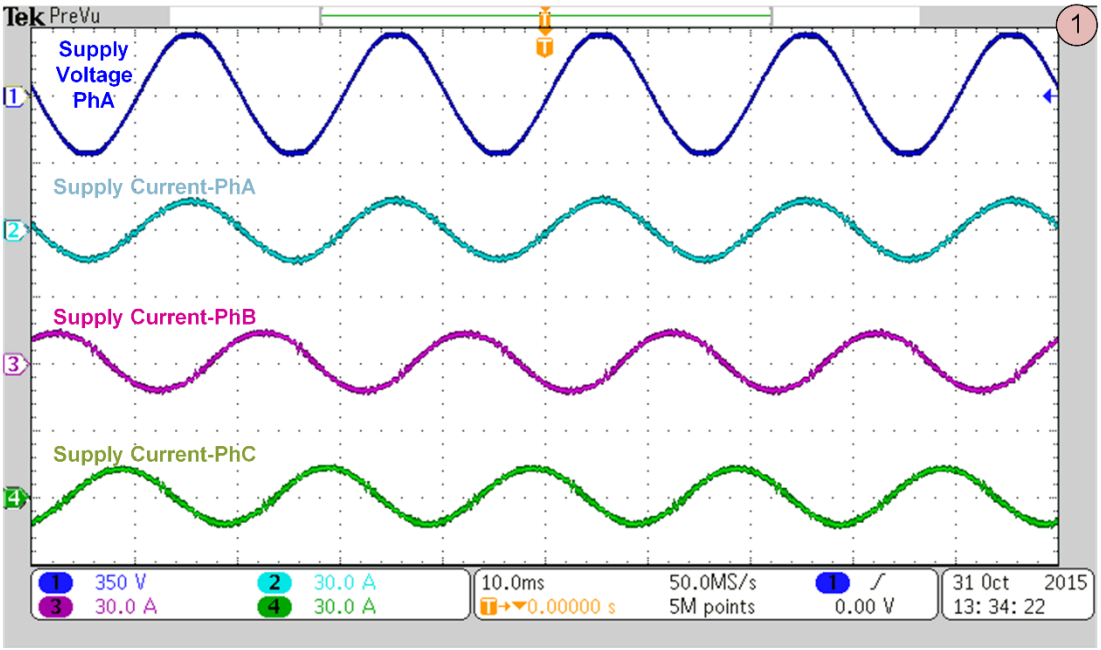


Figure 5.56. Supply voltage and current waveforms during the 1st state of inductive mode operation

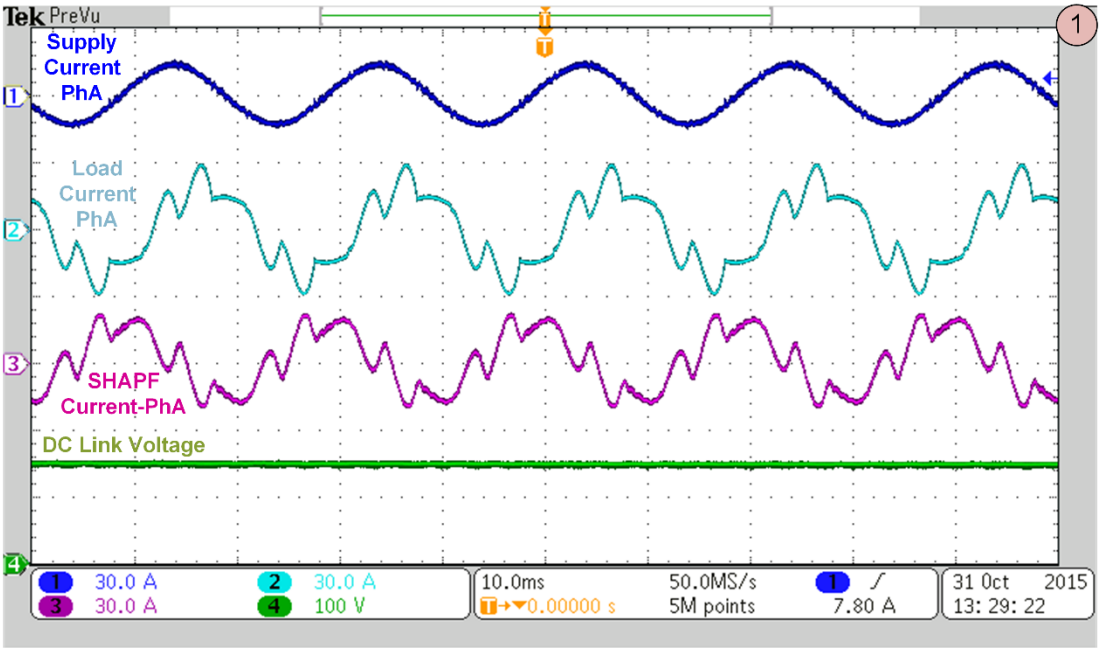


Figure 5.57. Supply current, load current, SHAPF current and dc link voltage waveforms during the 1st state of inductive mode operation

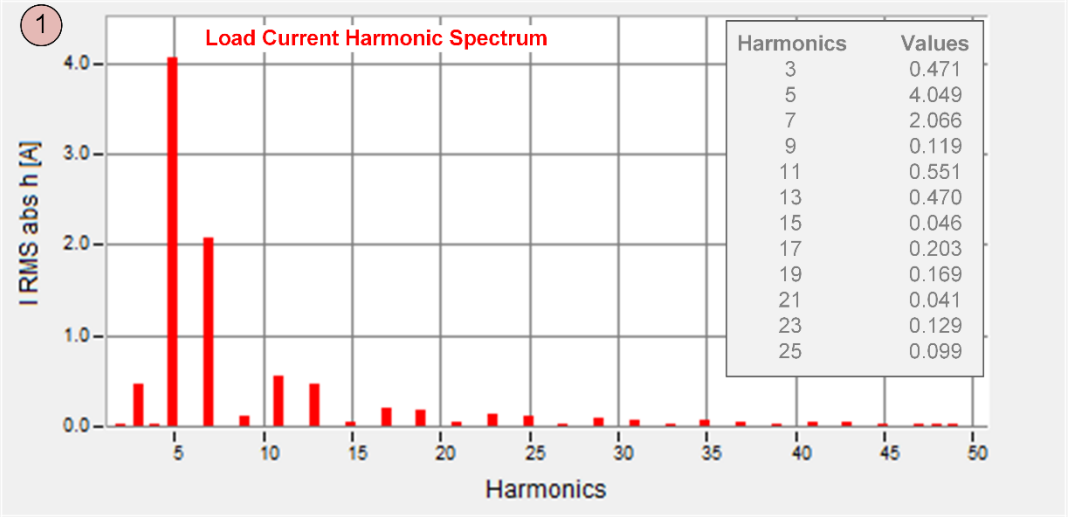


Figure 5.58. Load current harmonic spectrum during the 1st state of inductive mode operation

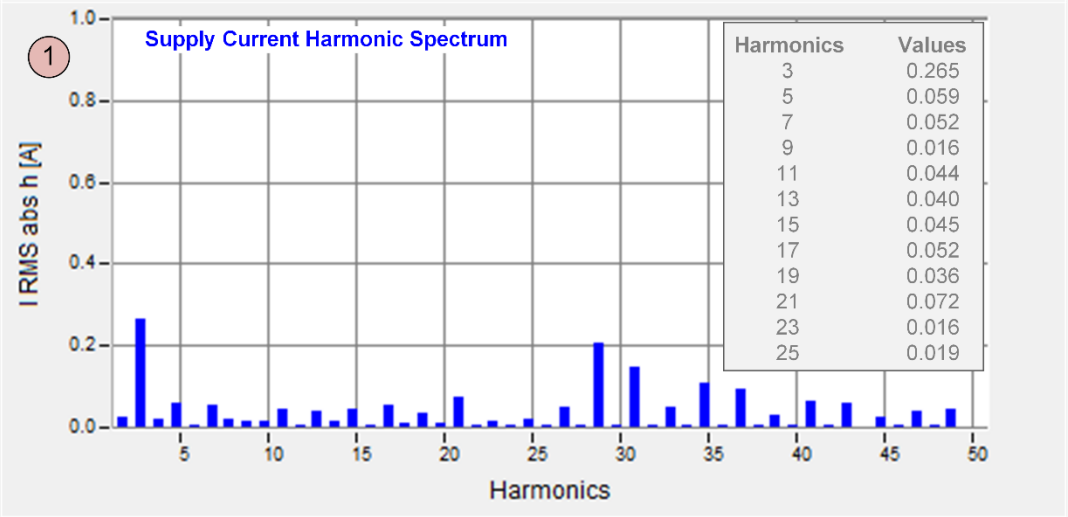


Figure 5.59. Supply current harmonic spectrum during the 1st state of inductive mode operation

In Figure 5.60, the supply current, the load current, SHAPF current and the dc link voltage waveforms during the load change from the 1st state to 2nd state are given. The supply voltage and the current waveforms and the supply, the load and SHAPF currents and the dc link voltage waveforms during the 2nd state are presented in Figures 5.61 and 5.62, respectively. The load and supply current harmonic spectrum during the 2nd state are given in Figure 5.63 and 5.64, respectively. In the 2nd state, the active power and the reactive power of the load group increases to 11.1kW and 8.6kVAr

when the supply voltage is 223.7V. The rms value of the dominant load group current harmonics increases to 9.19A and the current THD of the load group is about 44.5%. PF supplies the capacitive reactive power of 9.6kVAr. The required dc link voltage of VSC is calculated to be 105V. During the load transition from the 1st state to 2nd state, SHAPF discharges the dc link voltage from 153V to 50V under 150ms with 5% overshoot to increase the efficiency. In addition, the high inrush current of the load group during the load transition does not affect the dynamic response of SHAPF. VSC supplies the inductive reactive power of 1kVAr to prevent over compensation of PF and maintain the reactive power compensation requirements of the load. SHAPF decreases the supply current THD from 44.5% to 4.1% and holds the supply reactive power between ±100VAr.

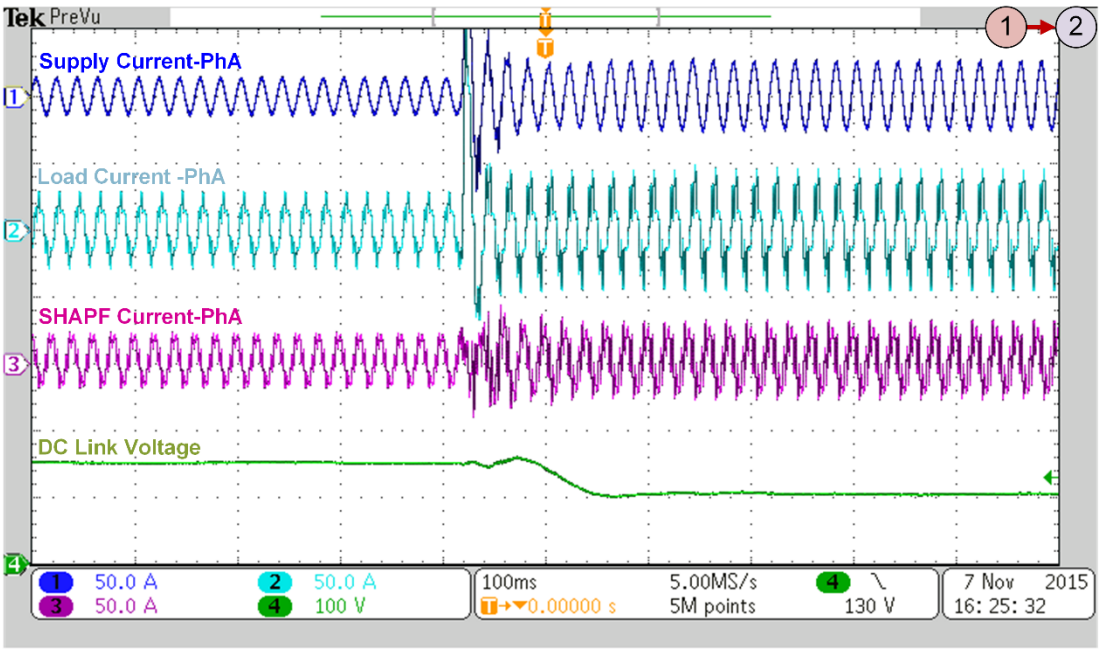


Figure 5.60. Supply current, load current, SHAPF current and dc link voltage waveforms during the transition from 1st state to 2nd state of inductive mode operation

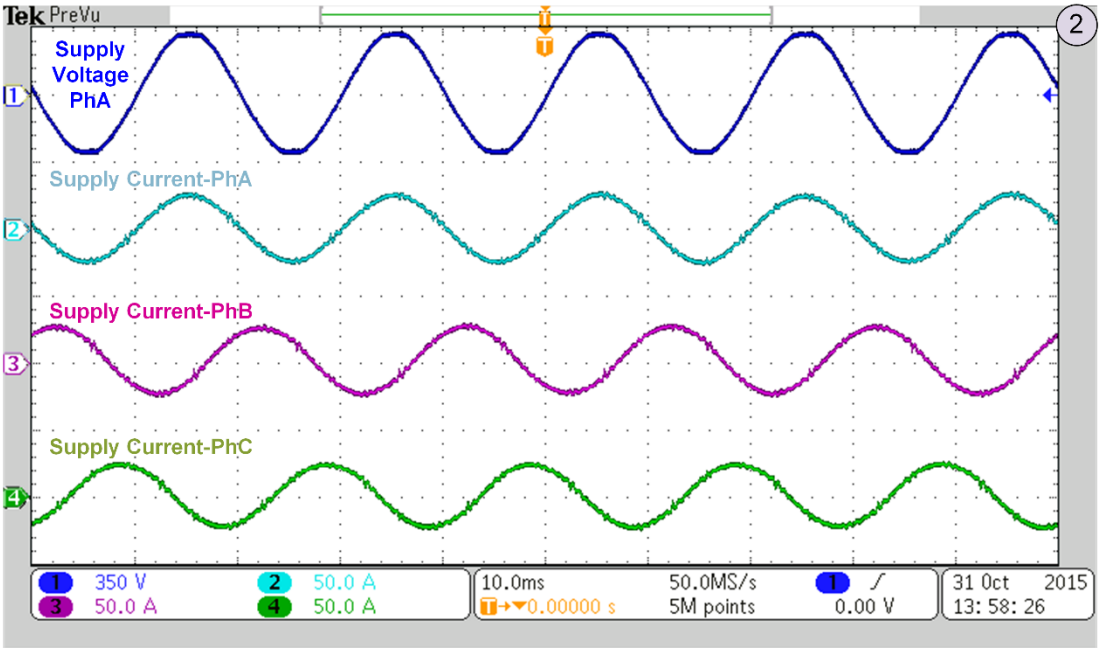


Figure 5.61. Supply voltage and current waveforms during the 2nd state of inductive mode operation

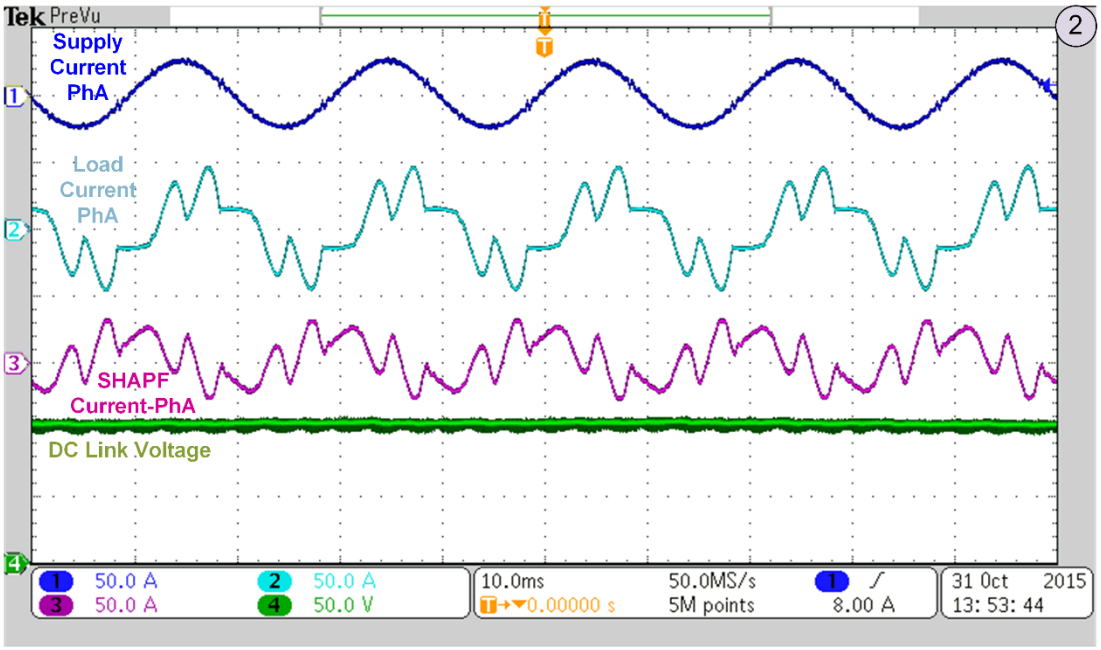


Figure 5.62. Supply current, load current, SHAPF current and dc link voltage waveforms during the 2nd state of inductive mode operation

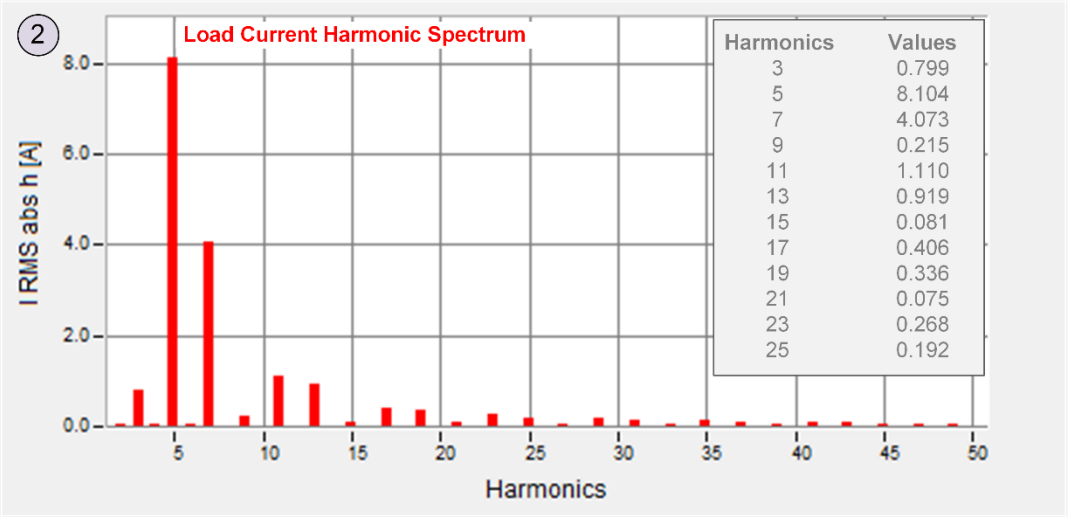


Figure 5.63. Load current harmonic spectrum during the 2nd state of inductive mode operation

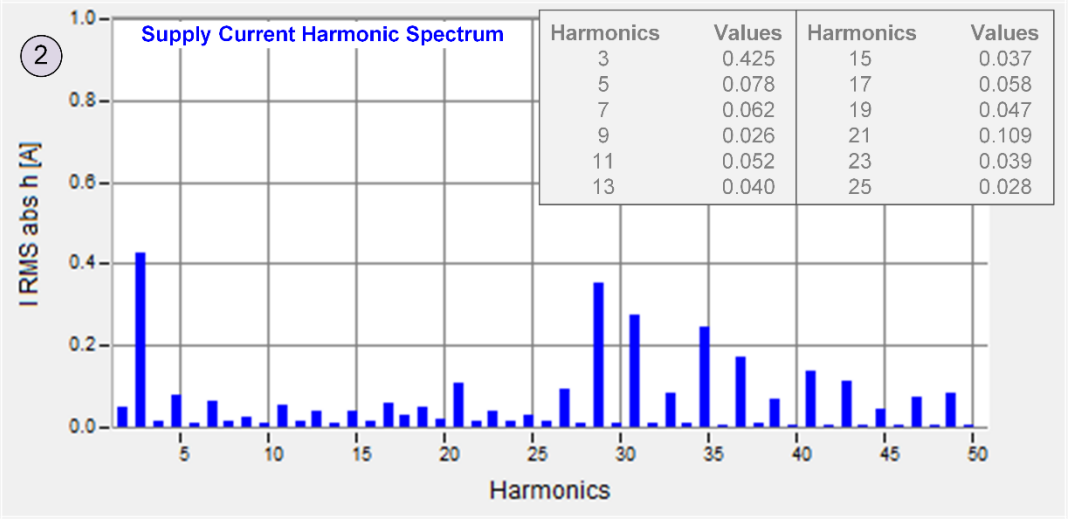


Figure 5.64. Supply current harmonic spectrum during the 2nd state of inductive mode operation

The supply current, the load current, SHAPF current and the dc link voltage waveforms during the load change from the 2nd state to 3rd state are given in Figure 5.65. The supply voltage and the current waveforms and the supply, the load and SHAPF currents and the dc link voltage waveforms during the 3rd state are presented in Figures 5.66 and 5.67, respectively. The load and supply current harmonic spectrum during the 3rd state are given in Figure 5.68 and 5.69, respectively. In this state, the reactive power of load group is decreased but the current harmonics of the load group

is increased. The active and reactive power of the load group are 16.1kW and 7.6kVAr at around 221.9V supply voltage. The rms value of the dominant load group current harmonics is 11.7A and the current THD of the load group is about 50.7%. PF supplies the capacitive reactive power of 9.47kVAr. The dc link voltage of VSC is determined and set to 186V by the proposed controller to compensate the current harmonics and the reactive power of the load group. Although the reactive power of load in this case has nearly the same value with the reactive power in the 1st case, the dc link voltage in this case is considerably higher than the 1st case because of the increase of the harmonic currents. During the load transition from the 1st state to 2nd state, SHAPF charges the dc link voltage from 105V to 186V under 200ms with 10% overshoot to decrease the losses. As in the previous load state changes, the high inrush current of the load group during the load transition does not affect the dynamic response of SHAPF. VSC supplies the inductive reactive power of 1.87kVAr to prevent over compensation of PF and maintain the reactive power compensation requirements of the load. SHAPF decreases the supply current THD from 44.5% to 4.1% and holds the supply reactive power between ±100VAr.

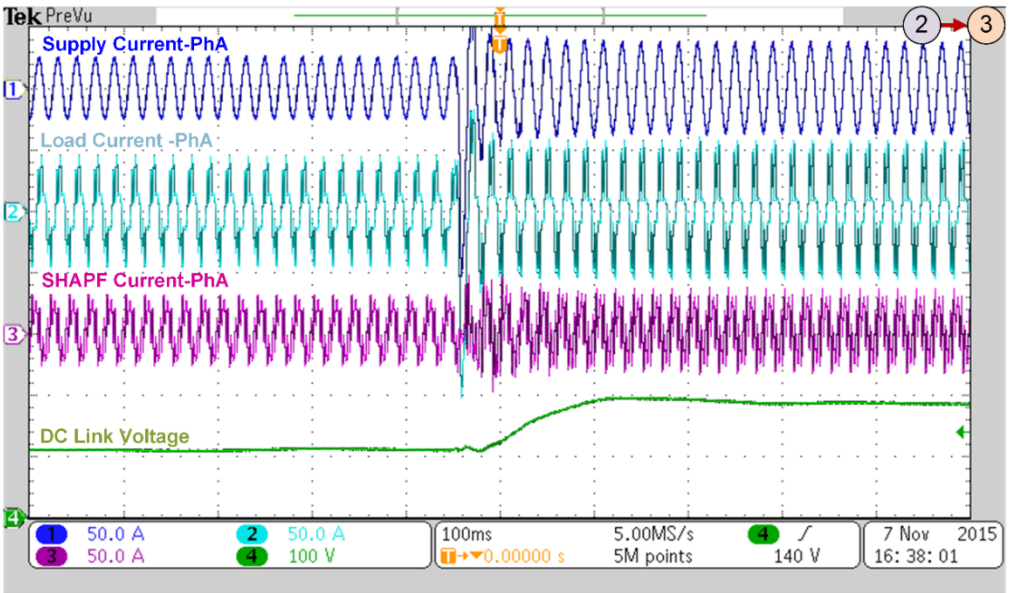


Figure 5.65. Supply, load and SHAPF currents and dc link voltage waveforms during the transition from 2nd state to 3rd state of inductive mode operation

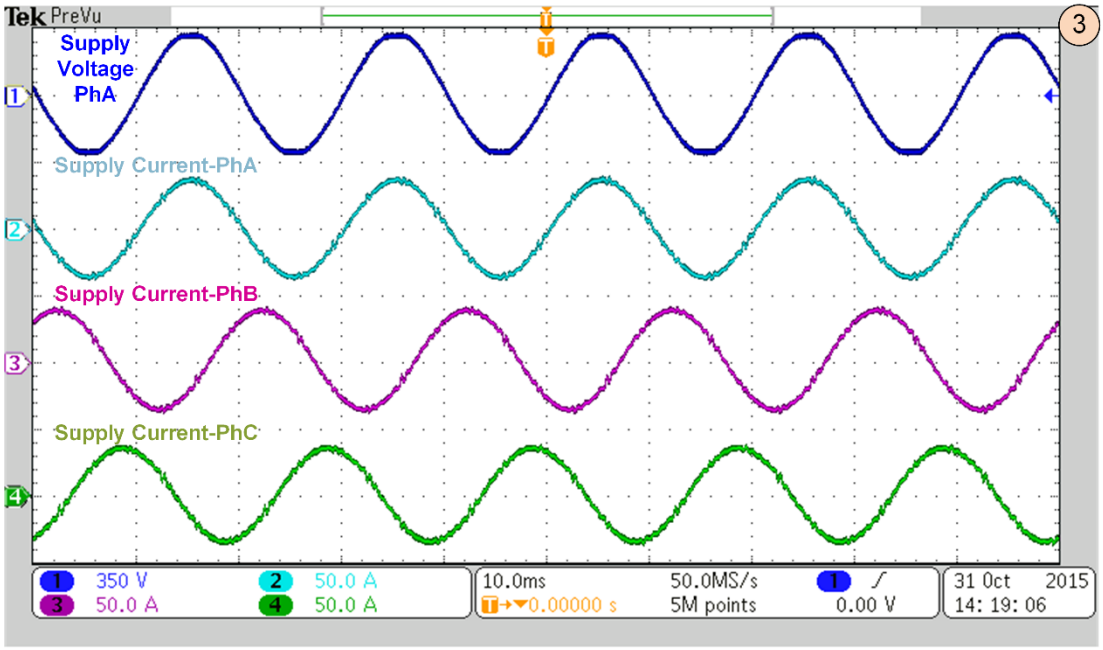


Figure 5.66. Supply voltage and current waveforms during the 3rd state of inductive mode operation

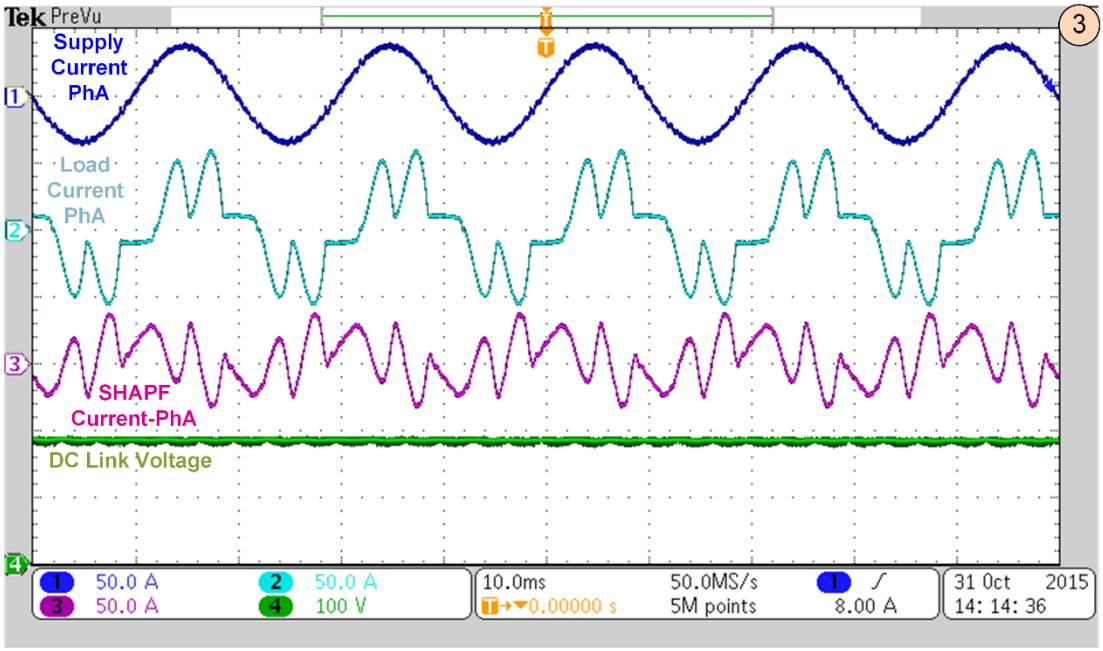


Figure 5.67. Supply current, load current, SHAPF current and dc link voltage waveforms during the 3rd state of inductive mode operation

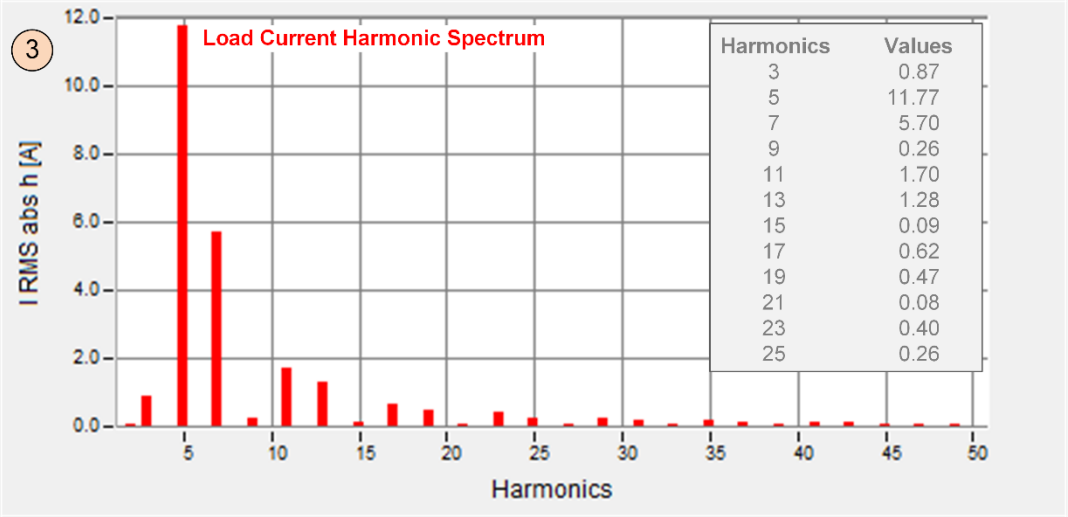


Figure 5.68. Load current harmonic spectrum during the 3rd state of inductive mode operation

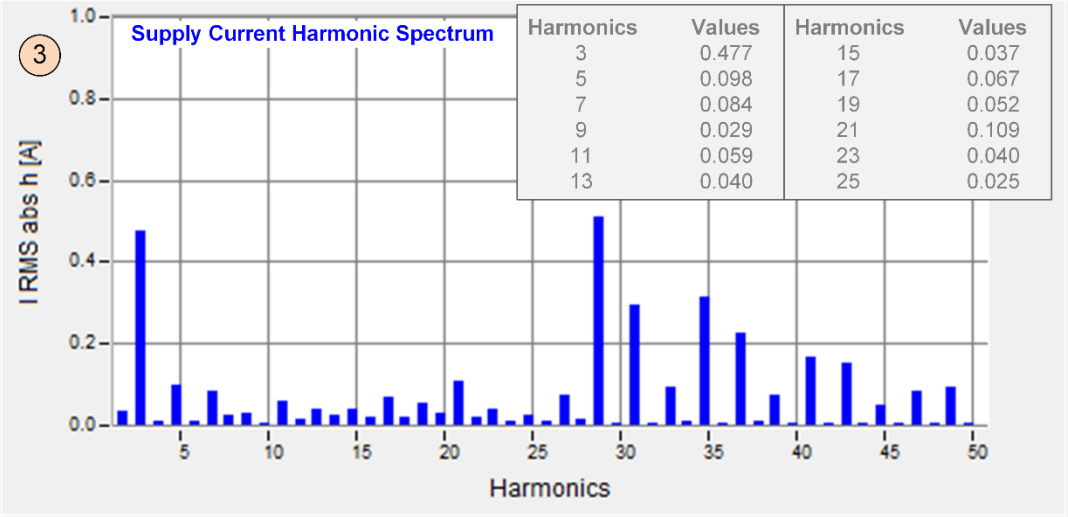


Figure 5.69. Supply current harmonic spectrum during the 3rd state of inductive mode operation

5.4.3. Summary

In this section of the experimental results, the performance of dynamic harmonic and reactive compensation with adaptive dc link voltage is investigated with two extended cases. The cases are presented according to the capacitive and inductive operation modes of VSC part. In the first case, the inductive reactive power demand of the load group is set higher than the reactive power compensation capacity of PF so

VSC operates in capacitive mode to supply the reactive power demand of the load group. In the second case, the inductive power demand of the load group is held under the reactive power capacity of PF. In this situation, PF causes over compensation and VSC operates in inductive mode in order to balance the reactive power demand of the load group. The performance of SHAPF with the proposed controller is presented with three load states in both of two cases. The steady state results are presented for each load state. In addition, the dynamic performance between the load states changes are introduced with detailed waveforms. The experimental results of the capacitive and inductive operation cases are summarized with the average values in Tables 5.6 and 5.7, respectively.

Table 5.6. Summary of experimental results during the capacitive operation cases

	State 1		State 2		State 3	
	Load	Supply	Load	Supply	Load	Supply
Supply Voltage	221.7V		223.5V		221.3V	
Active Power	16.3kW	16.9kW	11kW	11.4kW	16.2kW	16.7kW
Reactive Power	13.1kVAr	-23VAr	10.1kVAr	-45VAr	11.9kVAr	-39VAr
Fun. Current	31.6A	25.4A	22.2A	16.85A	30.3A	25.1A
5^{th} Cur. Har.	11.73A	0.12A	8.04A	0.07A	11.9A	0.11A
7^{th} Cur. Har.	5.66A	0.10A	4.06A	0.06A	5.80A	0.11A
11^{th} Cur. Har.	1.63A	0.04A	1.07A	0.03A	1.49A	0.10A
13^{th} Cur. Har.	1.22A	0.04A	0.89A	0.03A	1.27A	0.03A
17^{th} Cur. Har.	0.66A	0.05A	0.43A	0.03A	0.66A	0.04A
19^{th} Cur. Har.	0.44A	0.05A	0.32A	0.04A	0.44A	0.04A
23^{th} Cur. Har.	0.40A	0.06A	0.26A	0.03A	0.40A	0.05A
25^{th} Cur. Har.	0.25A	0.03A	0.19A	0.03A	0.26A	0.04A
Current THD	42.4%	3.31%	41.7%	3.81%	44.4%	3.44%
Tot. RMS Value of Dominant Load Cur. Har. up to 25^{th} Har.	13.2A		9.13A		13.4A	
Approximate Reac. Power Supplied by VSC	-3.65kVAr		-0.5kVAr		-2.48kVAr	
DC Link Vol. of SHAPF	295V		90V		215V	

Table 5.7. Summary of experimental results during the inductive operation cases

	State 1		State 2		State 3	
	Load	Supply	Load	Supply	Load	Supply
Supply Voltage	226.5V		223.7V		221.9V	
Active Power	5.9kW	6.2kW	11.1kW	11.4kW	16.1kW	16.4kW
Reactive Power	7.8kVAr	-40VAr	8.6kVAr	-45VAr	7.6kVAr	-10.2VAr
Fun. Current	14.4A	8.95A	20.9A	16.9A	26.8A	24.7A
5^{th} Cur. Har.	4.05A	0.06A	8.10A	0.08A	11.77A	0.10A
7^{th} Cur. Har.	2.06A	0.05A	4.07A	0.06A	5.70A	0.08A
11^{th} Cur. Har.	0.55A	0.04A	1.11A	0.05A	1.70A	0.06A
13^{th} Cur. Har.	0.47A	0.04A	0.92A	0.04A	1.28A	0.04A
17^{th} Cur. Har.	0.20A	0.05A	0.40A	0.06A	0.62A	0.06A
19^{th} Cur. Har.	0.17A	0.03A	0.33A	0.04A	0.47A	0.05A
23^{th} Cur. Har.	0.13A	0.01A	0.27A	0.04A	0.40A	0.04A
25^{th} Cur. Har.	0.10A	0.02A	0.19A	0.03A	0.26A	0.02A
Current THD	32.3%	4.3%	44.5%	4.1%	50.7%	3.15%
Tot. RMS Value of Dominant Load Cur. Har. up to 25^{th} Har.	4.61A		9.19A		13.28A	
Approximate Reac. Power Supplied by VSC	2.1kVAr		1kVAr		1.87kVAr	
DC Link Vol. of SHAPF	153V		105V		186V	

The experimental results presented in this section are summarized with the following statements;

- The experimental results show that SHAPF prototype provides a superior performance in the compensation of current harmonics and reactive power with the proposed controller. In all states of each cases, SHAPF prototype keeps the current harmonic THD under 4.5% and the reactive power between ±100VAr levels in the supply side. Moreover, the dc link voltage level of SHAPF is adaptively changed according to the harmonic and reactive power requirements of the load group with the proposed controller.
- The dc link reference voltage calculation method determines the necessary dc link voltage for the harmonic and reactive power compensation requirements. The calculated dc link reference value is set by the dc link voltage controller.

It is shown from the experimental results that the dc link voltage of SHAPF prototype is changed with respect to the harmonic and reactive power levels of the load group.

- Even though SHAPF topology provides a low voltage rating and a low losses for VSC than the conventional Shunt APFs, the adaptive dc link voltage specification presents an additional efficiency for the losses of SHAPF. The switching losses of VSCs are directly proportional with their dc link voltage levels. The adaptive dc link voltage calculation method with the dc link voltage controller changes the dc link voltage according to the current harmonic and the reactive power compensation requirements. By the help of this ability, only the required voltage is held on the dc link of VSC for the compensation so, the switching loss of VSC is decreased considerably in the low power compensation requirements. This specification is obviously seen in the states of the capacitive and the inductive operation cases.
- The dynamic performance of SHAPF is clearly presented with the experimental waveforms during the load state transitions in each case. It is shown from the experimental results that the dynamic response speed of SHAPF is related with the dc link charging or discharging duration in the step response changes of the load current harmonics or reactive power. The dc link charging and discharging time of SHAPF depends on the value of the dc link capacitor bank, PI controller parameters of dc link voltage controller and the impedance of PF. The dc link capacitor bank is designed according to reactive power and current harmonic compensation specifications. PI controller parameters are optimized to maintain the maximum speed with minimum overshoot and oscillation in the step changes in the load. PF parameters are selected for the reactive power compensation range of SHAPF prototype. In high power systems, the impedance of PF can be decreased and the dynamic response of SHAPF can be accelerated. The slow variations in the current harmonics and reactive power of the load can easily be handled with a small value variation of the dc link voltage by the proposed control method so these variations do not affect the compensation performance of SHAPF prototype.

6. CONCLUSIONS AND FUTURE WORK

Nowadays, the load profiles in electrical systems show nonlinear characteristics. These nonlinear loads are the common source of the one of severe PQ problem named as harmonics. Harmonics are the one of the most encountered PQ phenomenon in electrical systems. In addition to harmonics, reactive power flow is another serious problem in electrical systems. Reactive power which is not defined as a PQ phenomenon gives rise to other PQ problems so the reactive power flow in electrical systems should be kept under control. The compensation of harmonics with reactive power is a challenging issue for today's complex electrical distribution and transmission systems. In early compensation systems, PFs were commonly preferred for the compensation of harmonics and reactive power. Although conventional passive filtering methods maintain high reactive power capacity in low costs, they do not show adequate performances in the compensation of harmonics. In addition to the inadequate harmonic compensation performance, overcompensation and resonance problems are other main drawbacks of PFs. On the other hand, APFs presents superior compensation performance for the harmonics and the reactive power. However, the initial costs of APFs increase seriously with increasing power ratings. The cost drawback of APFs leads the use of APFs with PFs which is named as HAPFs in order to decrease the power ratings and also costs of APFs. SHAPF topology formed from the series connection of PF and APF comes into prominence with its low ratings, high efficiency and low cost of APF.

In this thesis work, SHAPF prototype system is designed and implemented at low voltage level in order to compensate the low order dominant current harmonics of six pulse rectifiers up to 15A and the reactive power in the range of 10kVAr±30%. In order to maintain these compensation performance, a novel control method which achieves the dynamic harmonic and reactive power compensation with adaptive dc link voltage level is proposed for SHAPF. In the controller of SHAPF, SRF method is applied for the harmonic, reactive power and dc link reference and feedback signal calculations. The individual harmonic elimination based feedback harmonic compensation method is applied for the harmonic compensation controller. With the

help of proposed method, the harmonic compensation performance of SHAPF becomes immune to voltage harmonics, the delays in the controller, the phase errors caused by the measurements circuits and the tolerance values of PF components. Therefore, SHAPF can show an effective harmonic filtering performance for the dominant harmonic of three phase rectifiers. By the help of the proposed control method, the dc link voltage level of SHAPF is determined adaptively with respect to the load current harmonics and the load reactive power demand. Therefore, only the required voltage level is kept on the dc link voltage for the compensation and the switching losses of VSC is decreased in the low power compensation operations.

The comprehensive power circuit design approach is presented for SHAPF prototype in this thesis work. According to the design specifications of prototype system, the design of PF and VSC are performed with using the theoretical calculations and the simulation studies performed in MATLAB/Simulink. An electronic control system is developed for SHAPF prototype in the scope of this thesis work. In the design studies of the electronic control system, the selection of DSP based MCU, the design of electronic circuits and the PCB design of the electronic control system are achieved. The prototype system is completed with the hardware implementation studies of the power circuit and the electronic control system and the embedded software development studies.

The performance of SHAPF is investigated with experimental studies performed in Power Electronics Research Laboratory of Çukurova University Electrical and Electronics Engineering Department. In order to examine the dynamic and steady state performance of prototype system, a test load group which consists of 3 pieces 5kW capacitive loaded rectifier and 5 step 11kVAr inductive load group is set. The performance of SHAPF prototype is proved with the extensive experimental case studies.

In the first section of the experimental results, the start-up of prototype is investigated. In this case, the requirement of pre-charge circuit is discussed. The reactive power compensation capacity, the harmonic filtering performance and the resonance problem of PF are investigated. Moreover, the start-up of SHAPF controllers is presented.

In the second section of the experimental results, the harmonic compensation performance of proposed individual harmonic compensation based feedback control method is compared with conventional feedback controller and feedback plus feedforward controller. In this case, the dynamic reactive power compensation ability of controller and the adaptive dc link voltage controller is turned off and dc link is set to a constant voltage level in order to compare the performance of conventional and proposed control method under the same conditions.

It is reported in the literature that the conventional feedback controller provides an intensive filtering performance in only a narrow bandwidth around the tuned frequency of PF. In this thesis work, PF of prototype system is tuned to 7^{th} harmonic frequency to maintain optimum harmonic compensation performance in high frequency harmonics with lower dc link voltage requirements as stated in literature. The compensation performance of the conventional controller is seen with the experimental results that this method presents sufficient performance only at the tuned 7^{th} harmonic frequency of PF and a poor compensation performance in other dominant harmonics.

In the conventional feedback plus feedforward controller, a feedforward control loop is added to compensate 5^{th} current harmonic more effectively because of the inadequate compensation performance of feedback controller caused by the 7^{th} harmonic tuned frequency of PF. Feedforward controller calculates the required reference voltage for the compensation of 5^{th} current harmonic. The reference voltage of feedforward loop is calculated with extracting the 5^{th} harmonic current from load current and multiplying the current harmonic by the impedance value of PF. Therefore, the performance of this method directly depends on the accuracy of PF impedance value so the tolerance values have important effect on the compensation performance. In addition, the harmonic voltages are a significant disturbance for the harmonic compensation controller. Conventional feedback controller has limited immunity to the harmonic voltages so the calculated reference voltage does not ensure the effective compensation of harmonic frequency to which the feedforward loop is applied in the presence of voltage harmonics. When the experimental results of the feedback plus feedforward controller are investigated, the effect of feedforward loop on 5^{th} current

harmonic is obviously shown but the performance of controller is not at the desired level.

In the proposed individual harmonic elimination based feedback controller, the feedback control loops are added to conventional feedback controller for each dominant harmonic frequency with using the PI controllers. The PI controllers generate the d and q components of voltage reference signals in order to minimize the current harmonics at the source side. By the help of PI controllers, the controller have high immunity to the voltage harmonics and the impedance value of PF has no effect in the controller performance in contrast to the conventional feedback plus feedforward controller. When the experimental result of the proposed controller is investigated, SHAPF prototype has been able to compensate the dominant current harmonics of 3 pieces 5kW six pulse rectifier superiorly. SHAPF prototype has held the average values of supply side dominant current harmonics of rectifier up to 25^{th} harmonics under 0.1A. Thus, the harmonic compensation performance of the proposed control method is proved with the comparative experimental results.

In the third section of the experimental results, the performance of the proposed controller which achieves the dynamic harmonic and reactive power compensation with adaptive dc link voltage are presented. In the operation of SHAPF prototype, VSC of SHAPF can be operated in both capacitive and inductive modes according to the reactive power demand of load group. When the load group demands higher reactive power than the reactive power rating of PF, VSC is operated in the capacitive operation mode to compensate the reactive demand of load group. Conversely, if the load group demands lower reactive power than the reactive power rating of PF, VSC is operated in the inductive operation mode to decrease the reactive power rating of SHAPF under the reactive power capacity of PF. The performance of the proposed controller is examined in both capacitive and inductive mode operation cases of VSC with three load states for each. In the experimental results, the steady state and the dynamic performances of SHAPF prototype are reported. It is shown from the experimental results that SHAPF prototype has calculated and set the required dc link voltage accurately with respect to load conditions. SHAPF prototype has kept the supply side current THD under 4.5% in all of three states of both cases with providing the average

values of supply side dominant current harmonics of 3 pieces 5kW six pulse rectifier up to 25th harmonics under 0.15A. Additionally, it keeps the reactive power of supply side in the range of ±100VAr in all of three states of both cases. When the dynamic response of SHAPF prototype during the load state changes is investigated, the prototype system have supplied the full harmonic and reactive power compensation requirements under 300ms for the step changes of the load group in all of three states of both cases. The outstanding steady state and dynamic performances of SHAPF prototype have been verified with these extensive case studies.

The major conclusions of this thesis work can be summarized with the following list;

- A SHAPF prototype system is designed and implemented at 400V level in order to compensate the low order dominant current harmonics of six pulse rectifiers up to 15A and the reactive power in the range of 10kVAr±30%.
- A novel control method which achieves the dynamic harmonic and reactive power compensation with adaptive dc link voltage level is developed for SHAPF. By the help of this control method, only the required dc link voltage is held to decrease the switching losses of VSC in the low power compensation demands.
- In the harmonic compensation part of the proposed controller, an individual harmonic elimination based feedback control method is applied in order to increase the harmonic compensation performance of SHAPF prototype system.
- A detailed power circuit design procedure is presented for SHAPF prototype.
- The success of proposed controller and the designed power circuit is verified with the comprehensive experimental results.

As a future work, the following research studies will be performed;

- The dc link voltage level of SHAPF should be increased to certain level above the calculated dc link voltage calculated from the rms value of desired VSC output voltage and the utilization factor of PWM method because of the high

crest factor of the desired output voltage of VSC in the certain compensation states of SHAPF. This required increase of dc link voltage varies according to the different compensation states. In the scope of this thesis work, the increase rate of dc link voltage is determined according to the worst case conditions. However, this increase rate causes inefficiency in low crest factor conditions. Because of these, an adaptive estimation method will be applied for the increase rate of dc link to increase the efficiency of SHAPF.

- The performance of SHAPF prototype will be investigated with the load side reference generation and direct current control approach.
- In order to increase the dynamic response of SHAPF prototype system, different reference generation methods or control methods will be applied.
- With using advanced switching modulation techniques, the effective switching frequency of SHAPF can be decreased for the efficiency of system.
- The proposed design procedure and the infrastructure of SHAPF prototype will be used to develop 3P4W compensation systems or the high power systems for the real applications.

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APPENDIX A: STANDARDS, GUIDES AND TECHNICAL REPORTS REGARDING HARMONICS

Table A.1. Standards, Guides and Technical Reports Regarding Harmonics

Commissions / Institute	Code / Number	Title
IEEE	519-1992	Recommended practices and requirements for harmonic control in electrical power systems
IEEE	1159-2009	Recommended practice on monitoring electrical power quality
CENELEC	EN50160	Voltage characteristics of electricity supplied by public distribution systems
IEC	61000-1-4	Historical rationale for the limitation of power-frequency conducted harmonic current emissions from equipment in the frequency range up to 9 kHz – Technical Report
IEC	61000-2-1	Description of the environment - Electromagnetic environment for low-frequency conducted disturbances and signaling in public power supply systems
IEC	61000-2-2	Compatibility levels for low-frequency conducted disturbances and signaling in power supply systems
IEC	61000-2-3	Description of the environment – Radiated and non-network-frequency-related conducted disturbances
IEC	61000-2-4	Compatibility levels in industrial plants for low-frequency conducted disturbances
IEC	61000-2-6	Assessment of the emission levels in the power supply of industrial plants as regards low-frequency conducted disturbances
IEC	61000-2-12	Compatibility levels for low-frequency conducted disturbances and signaling in public medium-voltage power supply systems – Basic EMS publication
IEC	61000-3-2	Limits for harmonic current emissions (equipment input current≤ 16 A per phase)
IEC	61000-3-4	Limitation of emission of harmonic currents in low-voltage power supply systems for equipment with rated current greater than 16 A
IEC	61000-3-6	Assessment of emission limits for distorting loads in MV and HV power systems
IEC	61000-3-9	Limits for interharmonic current emissions (equipment with input current≤ 16 A per phase and prone to produce interharmonics by design) – Technical report
IEC	61000-3-10	Emission limits in the frequency range 2 to 9 kHz (equipment with input current≤ 16 A per phase) – Technical report
IEC	61000-3-12	Limits for harmonic currents produced by equipment connected to public low-voltage systems with input current≤ 75 A per phase and subject to restricted connection
IEC	61000-4-7	General guide on harmonic distortion and interharmonics measurement and instrumentation, for power supply systems and equipment connected thereto
IEC	61000-4-13	Harmonics and interharmonics including mains signaling at a.c. power port, low frequency immunity test
IEC	61000-4-30	Measurements of power quality parameters
IEC	61000-4-31	Measurements in the frequency range 2 kHz to 9 kHz

APPENDIX B: OPERATION PERIOD CALCULATIONS OF SWITCHING STATE VECTORS AND PULSE PATTERNS OF ALL SECTORS SYMMETRICAL SWITCHING SEQUENCE IN SVPWM METHOD

The operation period calculations of switching state vectors are as follows;

Sector 1:

$$T_s V_{ref,norm} = T_1 V_1 + T_2 V_2 + T_0 V_0 + T_7 V_7$$

$$T_s \begin{bmatrix} V_{\alpha,norm} \\ V_{\beta,norm} \end{bmatrix} = T_1 \begin{bmatrix} 2/3 \\ 0 \end{bmatrix} + T_2 \begin{bmatrix} 1/3 \\ 1/\sqrt{3} \end{bmatrix} + T_0 \begin{bmatrix} 0 \\ 0 \end{bmatrix} + T_7 \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$T_s\, V_{\alpha,norm} = \frac{2}{3} T_1 + \frac{1}{3} T_2 + 0T_0 + 0T_7$$

$$T_s\, V_{\beta,norm} = 0T_1 + \frac{1}{\sqrt{3}} T_2 + 0T_0 + 0T_7$$

$$T_1 = \frac{3}{2} T_s\, V_{\alpha,norm} - \frac{\sqrt{3}}{2} T_s\, V_{\beta,norm}$$

$$T_2 = \sqrt{3} T_s\, V_{\beta,norm}$$

$$T_0 = T_7 = \frac{T_s - T_1 - T_2}{2}$$

Sector 2:

$$T_s V_{ref,norm} = T_2 V_2 + T_3 V_3 + T_0 V_0 + T_7 V_7$$

$$T_s \begin{bmatrix} V_{\alpha,norm} \\ V_{\beta,norm} \end{bmatrix} = T_2 \begin{bmatrix} 1/3 \\ 1/\sqrt{3} \end{bmatrix} + T_3 \begin{bmatrix} -1/3 \\ 1/\sqrt{3} \end{bmatrix} + T_0 \begin{bmatrix} 0 \\ 0 \end{bmatrix} + T_7 \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$T_s\, V_{\alpha,norm} = \frac{1}{3} T_2 - \frac{1}{3} T_3 + 0T_0 + 0T_7$$

$$T_s\, V_{\beta,norm} = \frac{1}{\sqrt{3}} T_2 + \frac{1}{\sqrt{3}} T_3 + 0T_0 + 0T_7$$

$$T_2 = \frac{3}{2} T_s\, V_{\alpha,norm} + \frac{\sqrt{3}}{2} T_s\, V_{\beta,norm}$$

$$T_3 = -\frac{3}{2} T_s\, V_{\alpha,norm} + \frac{\sqrt{3}}{2} T_s\, V_{\beta,norm}$$

$$T_0 = T_7 = \frac{T_s - T_2 - T_3}{2}$$

Sector 3:

$$T_s V_{ref,norm} = T_3 V_3 + T_4 V_4 + T_0 V_0 + T_7 V_7$$

$$T_s \begin{bmatrix} V_{\alpha,norm} \\ V_{\beta,norm} \end{bmatrix} = T_3 \begin{bmatrix} -1/3 \\ 1/\sqrt{3} \end{bmatrix} + T_4 \begin{bmatrix} -2/3 \\ 0 \end{bmatrix} + T_0 \begin{bmatrix} 0 \\ 0 \end{bmatrix} + T_7 \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$T_s\, V_{\alpha,norm} = -\frac{1}{3} T_3 - \frac{2}{3} T_4 + 0T_0 + 0T_7$$

$$T_s\, V_{\beta,norm} = \frac{1}{\sqrt{3}} T_3 + 0T_4 + 0T_0 + 0T_7$$

$$T_3 = \sqrt{3} T_s\, V_{\beta,norm}$$

$$T_4 = -\frac{3}{2} T_s\, V_{\alpha,norm} - \frac{\sqrt{3}}{2} T_s\, V_{\beta,norm}$$

$$T_0 = T_7 = \frac{T_s - T_3 - T_4}{2}$$

Sector 4:

$$T_s V_{ref,norm} = T_4 V_4 + T_5 V_5 + T_0 V_0 + T_7 V_7$$

$$T_s \begin{bmatrix} V_{\alpha,norm} \\ V_{\beta,norm} \end{bmatrix} = T_4 \begin{bmatrix} -2/3 \\ 0 \end{bmatrix} + T_5 \begin{bmatrix} -1/3 \\ -1/\sqrt{3} \end{bmatrix} + T_0 \begin{bmatrix} 0 \\ 0 \end{bmatrix} + T_7 \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$T_s\, V_{\alpha,norm} = -\frac{2}{3} T_4 - \frac{1}{3} T_5 + 0T_0 + 0T_7$$

$$T_s\, V_{\beta,norm} = 0T_4 - \frac{1}{\sqrt{3}} T_5 + 0T_0 + 0T_7$$

$$T_4 = -\frac{3}{2} T_s\, V_{\alpha,norm} + \frac{\sqrt{3}}{2} T_s\, V_{\beta,norm}$$

$$T_5 = -\sqrt{3} T_s\, V_{\beta,norm}$$

$$T_0 = T_7 = \frac{T_s - T_4 - T_5}{2}$$

Sector 5:

$$T_s V_{ref,norm} = T_5 V_5 + T_6 V_6 + T_0 V_0 + T_7 V_7$$

$$T_s \begin{bmatrix} V_{\alpha,norm} \\ V_{\beta,norm} \end{bmatrix} = T_5 \begin{bmatrix} -1/3 \\ -1/\sqrt{3} \end{bmatrix} + T_6 \begin{bmatrix} 1/3 \\ -1/\sqrt{3} \end{bmatrix} + T_0 \begin{bmatrix} 0 \\ 0 \end{bmatrix} + T_7 \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$T_s \, V_{\alpha,norm} = -\frac{1}{3} T_5 + \frac{1}{3} T_6 + 0T_0 + 0T_7$$

$$T_s \, V_{\beta,norm} = -\frac{1}{\sqrt{3}} T_5 - \frac{1}{\sqrt{3}} T_6 + 0T_0 + 0T_7$$

$$T_5 = -\frac{3}{2} T_s \, V_{\alpha,norm} - \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm}$$

$$T_6 = \frac{3}{2} T_s \, V_{\alpha,norm} - \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm}$$

$$T_0 = T_7 = \frac{T_s - T_5 - T_6}{2}$$

Sector 6:

$$T_s V_{ref,norm} = T_6 V_6 + T_1 V_1 + T_0 V_0 + T_7 V_7$$

$$T_s \begin{bmatrix} V_{\alpha,norm} \\ V_{\beta,norm} \end{bmatrix} = T_6 \begin{bmatrix} 1/3 \\ -1/\sqrt{3} \end{bmatrix} + T_1 \begin{bmatrix} 2/3 \\ 0 \end{bmatrix} + T_0 \begin{bmatrix} 0 \\ 0 \end{bmatrix} + T_7 \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$T_s \, V_{\alpha,norm} = \frac{1}{3} T_6 + \frac{2}{3} T_1 + 0T_0 + 0T_7$$

$$T_s \, V_{\beta,norm} = -\frac{1}{\sqrt{3}} T_6 + 0T_1 + 0T_0 + 0T_7$$

$$T_6 = -\sqrt{3} T_s \, V_{\beta,norm}$$

$$T_1 = \frac{3}{2} T_s \, V_{\alpha,norm} + \frac{\sqrt{3}}{2} T_s \, V_{\beta,norm}$$

$$T_0 = T_7 = \frac{T_s - T_6 - T_1}{2}$$

The pulse patterns of symmetrical switching sequences are given in Figure B.1 for all sectors.

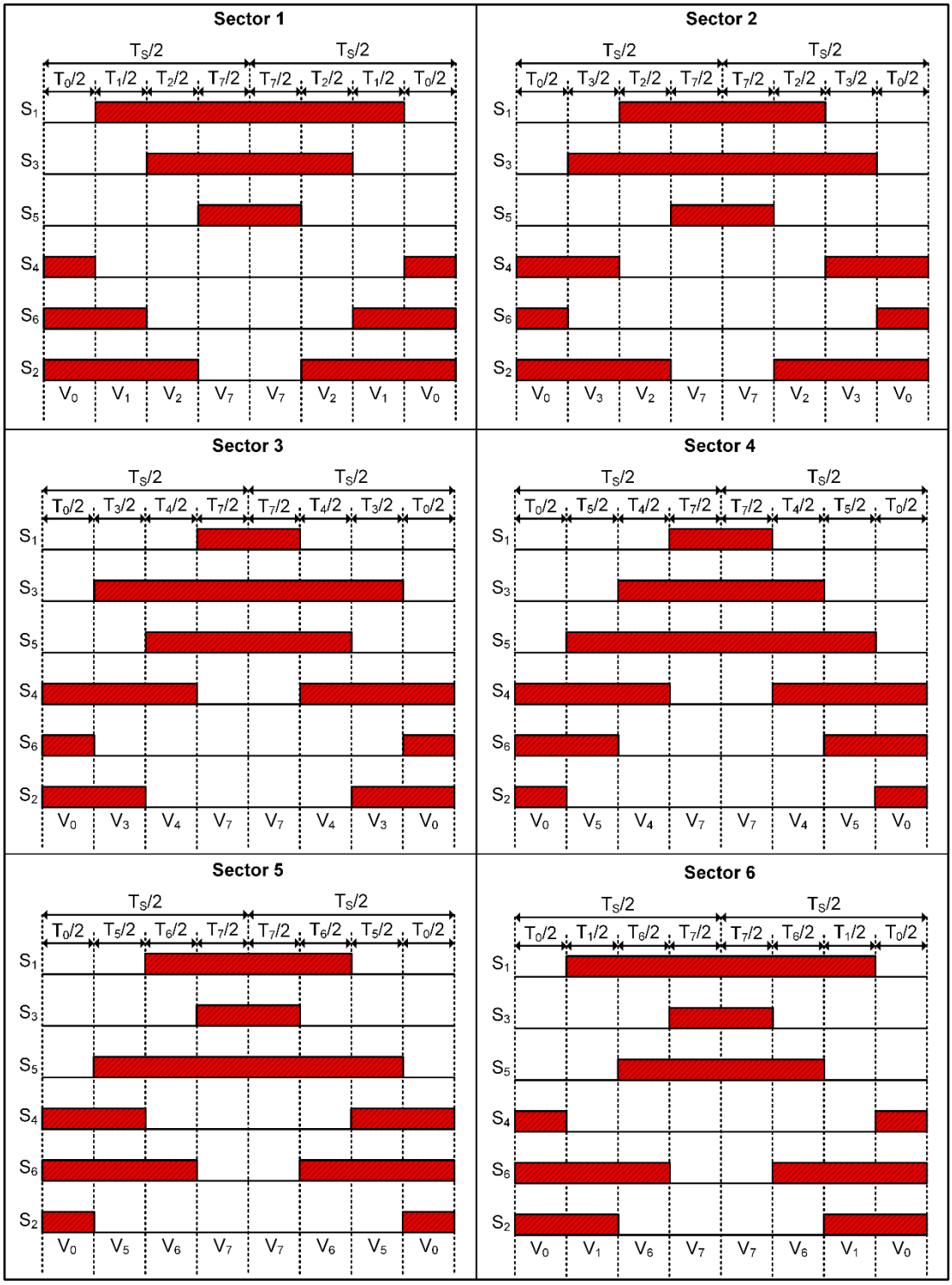

Figure B.1. Pulse pattern of symmetrical switching sequences of SVPWM

APPENDIX C: TECHNICAL SPECIFICATIONS OF IGBT MODULE AND IGBT DRIVER

Table C.1. Technical specifications of Semikron SKM100GB12T4 (Semikron, 2013)

Man.	**SEMIKRON**				
No	**SKM100GB12T4**				
					
V_{CES}	T_J= 25°C			1200V	
I_C	T_C=25°C T_J= 175°C			160A	
	T_C=80°C T_J= 175°C			123A	
I_{Cnom}	100A				
I_{CM}	300A				
			min	**typ**	**max**
$V_{CE(sat)}$	ChipLev. V_{GE}=15V I_C=150A	T_J=25°C	-	1.8V	2.05V
		T_J=150°C	-	2.2V	2.4V
I_{CES}	V_{GE}=0V V_{CE}=1200V		-		1mA
R_G	Internal		-	7.5Ω	-
Q_G	-		-	565nC	-
$t_{d(on)}$	V_{CC}=600V I_C=150A V_{GE}=±15V R_{Gon}=1Ω Inductive Load	T_J=25°C	-	-	-
		T_J=150°C	-	165nsec	-
t_r		T_J=25°C	-	-	-
		T_J=150°C	-	47nsec	
E_{on}		T_J=25°C	-	-	-
		T_J=150°C	-	15mJ	-
$t_{d(off)}$		T_J=25°C	-	-	-
		T_J=150°C	-	400nsec	-
t_f		T_J=25°C	-	-	-
		T_J=150°C	-	75nsec	-
E_{off}		T_J=25°C	-	-	-
		T_J=150°C	-	10.2mJ	-
V_F	At chip V_{GE}=0V I_F=150A	T_J=25°C	-	2.2V	2.52V
		T_J=150°C	-	2.15V	2.47V
E_{rr}	I_F = 150A di_F/dt = 3100 /µs V_R = 600V V_{GE} = -15V	T_J=25°C	-	-	-
		T_J=150°C	-	5.9mJ	-

Table C.2. Technical specifications of Semikron SKYPER 32 PRO R (Semikron, 2007)

Man.	**SEMIKRON**		
No	**SKYPER 32PRO R**		
			
Specifications	• Two output channels • Integrated potential free power supply • Under voltage protection prim/sec • Drive interlock top / bottom • Dynamic short circuit protection • Halt status with failure management • External failure input (sec.) • Soft turn-off		
V_{CEmax}	1700V		
I_{outmax}	15A		
f_{max}	50kHz		
V_{dcmax}	1200Vdc		
V_{isol}	4000V		
$R_{Gon\ min}$	1.5Ω		
$R_{Goff\ min}$	1.5Ω		
Q_{out}/pulse	6.3uC		
	min	**typ**	**max**
V_s	14.4V	15V	15.6V
$I_{Snoload}$	80mA	-	-
I_{Smax}	-	-	500mA
V_{IH}	-	15V	-
V_{IL}	-	0V	-
V_{Gon}	-	(+)15V	-
V_{Goff}	-	(-)7V	-
$t_{d(on)}$	-	1.2us	-
$t_{d(off)}$	-	1.2us	-
$t_{r(out)}$	-	-	-
$t_{f(out)}$	-	-	-
t_{TD}	0us	-	4.3us

APPENDIX D: TECHNICAL SPECIFICATIONS OF MCU BASED DSP

Table D.1. Technical Specifications of TMS320F28335 (Texas-Instruments, 2015)

Clock Rate	150MHz
Instruction cycle	6.67 ns
Floating-point Unit	Yes
3.3-V on-chip flash (16-bit word)	256K
Single-access RAM (SARAM) (16-bit word)	34K
Boot ROM (8K x 16)	1K
Code security	Yes
Boot ROM (8K x 16)	Yes
16/32-bit External Interface (XINTF)	Yes
6-channel Direct Memory Access (DMA)	Yes
PWM outputs	ePWM1/2/3/4/5/6
HRPWM channels	ePWM1A/2A/3A/4A/5A/6A
32-bit Capture inputs	eCAP1/2/3/4/5/6
32-bit QEP channels	eQEP1/2
Watchdog timer	Yes
ADC Resolution	12 Bit
ADC No. of channels	16
ADC Sampling Rate	12.5 MSPS
ADC Conversion time	80 ns
32-Bit CPU timers	3
Multichannel Buffered Serial Port (McBSP)/SPI	2 (A/B)
Serial Peripheral Interface (SPI)	1
Serial Communications Interface (SCI)	3 (A/B/C)
Enhanced Controller Area Network (eCAN)	2 (A/B)
Inter-Integrated Circuit (I2C)	1
General Purpose I/O pins (shared)	88
External interrupts	8

APPENDIX E: TECHNICAL SPECIFICATIONS OF VOLTAGE AND CURRENT SENSORS

Table E.1. Technical specifications of LEM LV 25-P (LEM, 2012)

	Electrical data		
$\mathbf{I}_{PN}$	Primary nominal r.m.s. current	10 mA	
$\mathbf{I}_{P}$	Primary current, measuring range	0 .. ± 14 mA	
$\mathbf{R}_{M}$	Measuring resistance	$\mathbf{R}_{M}$ min	$\mathbf{R}_{M}$ max
	with ± 12 V		
	@ ± 10 mA max	30	190 W
	@ ± 14 mA max	30	100 W
	with ± 15 V		
	@ ± 10 mA max	100	350 W
	@ ± 14 mA max	100	190 W
$\mathbf{I}_{SN}$	Secondary nominal r.m.s. current	25 mA	
$\mathbf{K}_{N}$	Conversion ratio	2500 : 1000	
$\mathbf{V}_{C}$	Supply voltage (± 5 %)	± 12 .. 15 V	
$\mathbf{I}_{C}$	Current consumption	10 (@± 15 V)+ $\mathbf{I}_{S}$ mA	
Vd	R.m.s. voltage for AC isolation test 1), 50 Hz, 1 mn	2.5 kV	
	Accuracy - Dynamic performance data		
$\mathbf{X}_{G}$	Overall Accuracy @ $\mathbf{I}_{PN}$, $\mathbf{T}_{A}$= 25°C		
	@ ± 12 .. 15 V	± 0.9 %	
	@ ± 15 V (± 5 %)	± 0.8 %	
$\mathbf{e}_{L}$	Linearity	< 0.2 %	
$\mathbf{I}_{O}$	Offset current @ $\mathbf{I}_{P}$ = 0, $\mathbf{T}_{A}$ = 25°C	± 0.15 mA	
$\mathbf{I}_{OT}$	Thermal drift of $\mathbf{I}_{O}$	0°C .. + 25°C	± 0.06 ± 0.25 mA
		25°C .. + 70°C	± 0.10 ± 0.35 mA
$\mathbf{t}_{r}$	Response time @ 90 % of $\mathbf{V}_{P}$ max	40 µs	

Table E.2. Technical specifications of Multimic CTF 50A (Multimic, 2015)

Insulation Resistance	More than 100MΩ by 500V insulation tester (between output terminal and outer case)
Open Circuit Protection	7.5V
Operational Temperature	-10～50 ℃, less than 80%RH Without condensation
Standard	Compliant with RoHS directive
Output Example	AC16.6mA±1% (50A)
Dimension/Weight	26(W)×23(D)×48(H)mm /Approx. 45gs.
Material of Outer Case	P.P. (Flame rating:compliant with UL-94V-O)
Material of Core	Ferrite
Applicable Current	AC 0.1～50Arms
Max. Input Current	100Arms continuous
Output characteristic	Refer to the drawing
Phase Accuracy	-1.4°±0.5°(50A)
CT Inside Diameter	10mm×9.5mm
Nominal CT Ratio	3000：1
Applicable Frequency	10Hz～5kHz
Max. Circuit Voltage	Less than AC600V for insulated cable
Withstanding Voltage	AC 2200V/1 minute (between output terminal and outer case)

APPENDIX F: FLOW CHART OF INTERRUPT FUNCTION

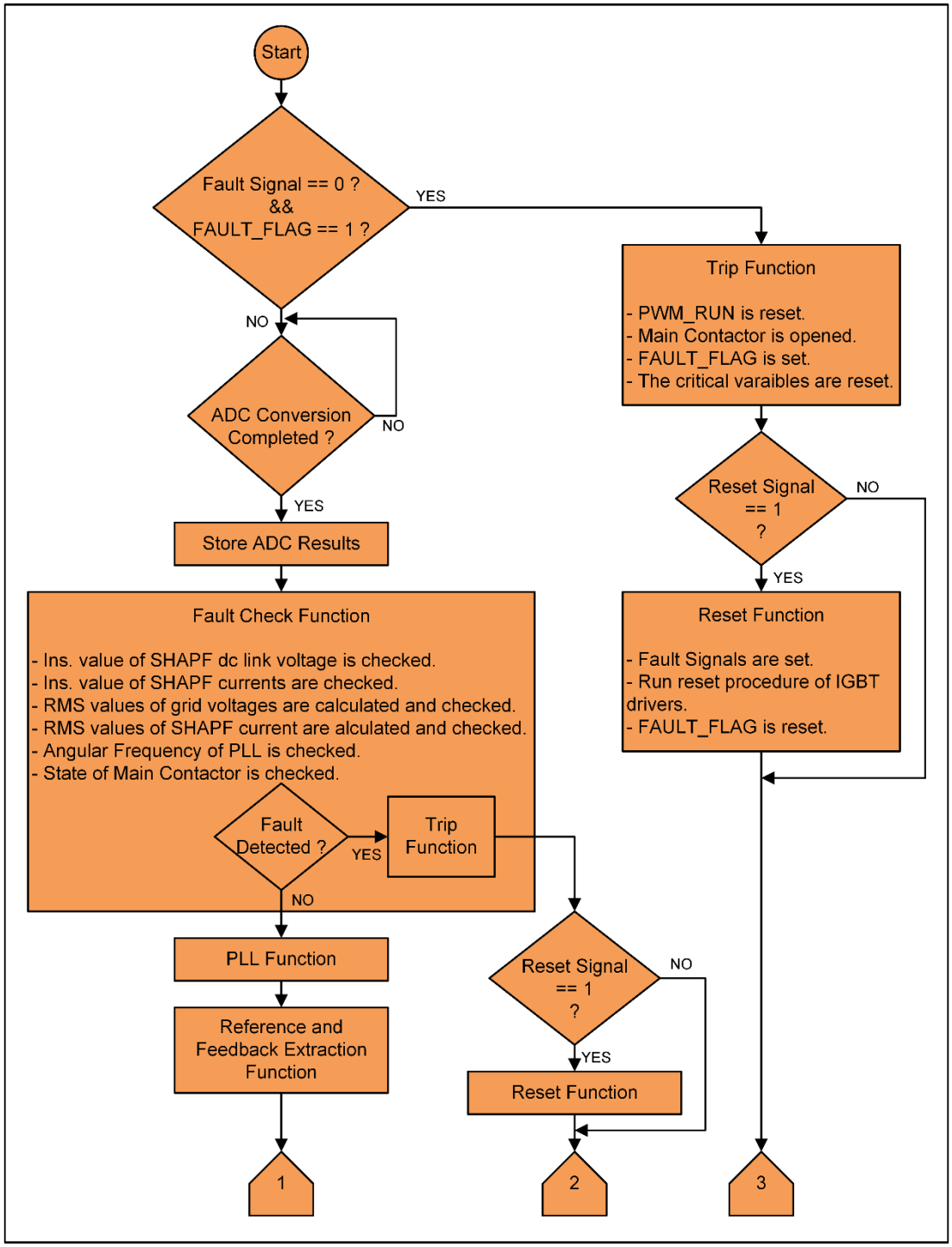

Figure F.1. Flow chart of interrupt function - Part 1

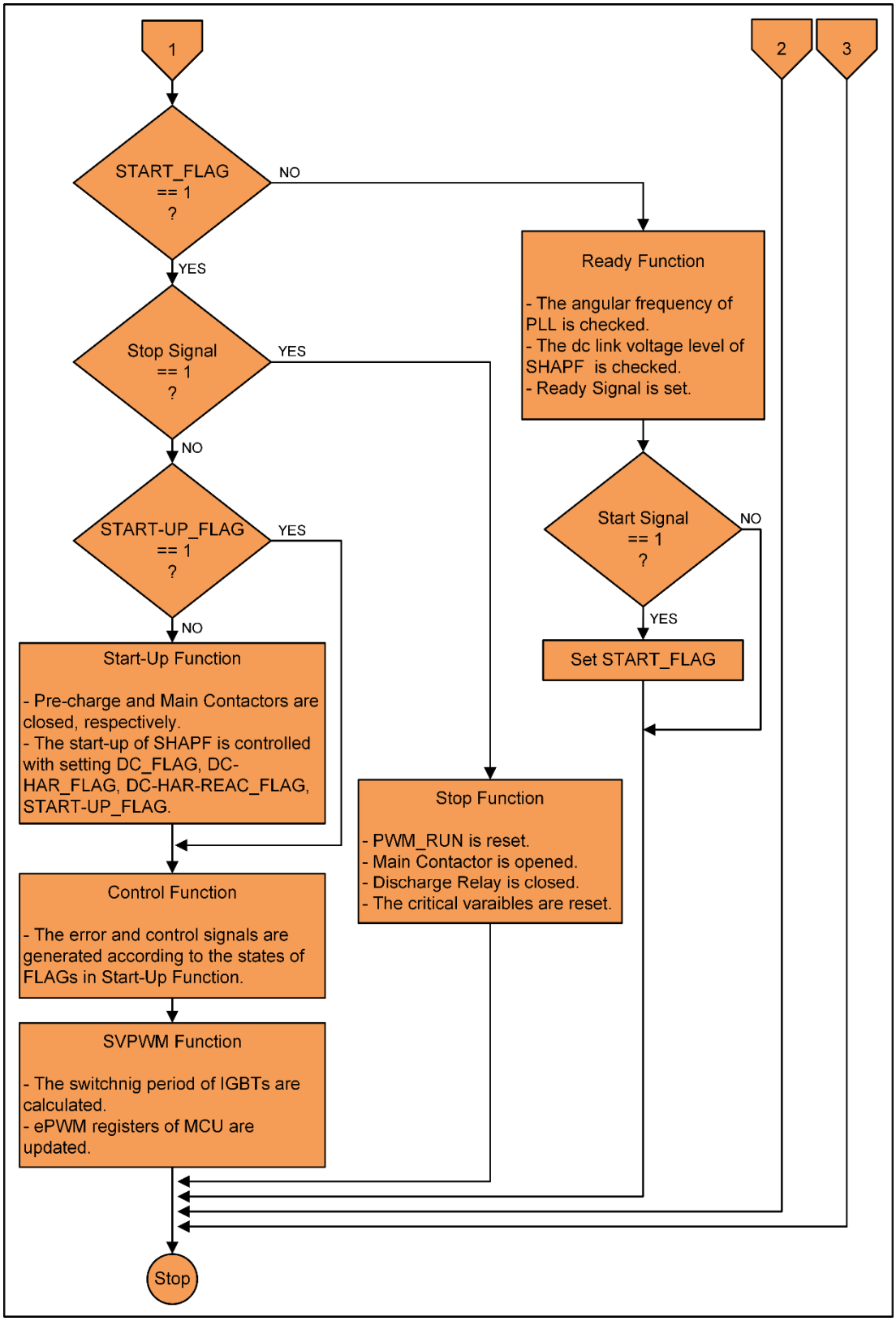

Figure F.2. Flow chart of interrupt function - Part 2