

DESIGN AND IMPLEMENTATION OF THREE-LEVEL SIC INTERLEAVED
BOOST CONVERTERS FOR A GRID CONNECTED MULTI-STRING PV
INVERTER

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

OGÜN ALTUN

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2023

Approval of the thesis:

**DESIGN AND IMPLEMENTATION OF THREE-LEVEL SIC
INTERLEAVED BOOST CONVERTERS FOR A GRID CONNECTED
MULTI-STRING PV INVERTER**

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ABSTRACT

DESIGN AND IMPLEMENTATION OF THREE-LEVEL SIC INTERLEAVED BOOST CONVERTERS FOR A GRID CONNECTED MULTI-STRING PV INVERTER

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September 2023, 112 pages

The popularity of solar power, which is an endless energy source for the world, increased in recent years. Developments in solar cells ensure higher efficiency at lower costs. Moreover, the advancements in power electronics also increased their popularity. In this thesis, the design of a 20 kW three-level boost converter is investigated. The designed converter is used for 1500 V multi-string photovoltaic inverters, which is the new trend in photovoltaic systems. The converter design is optimized so that the power conversion efficiency is higher than 99% for all conditions. The designed converter then implemented and verified experimentally. With the help of silicon carbide semiconductor devices, 80 kHz switching frequency is achieved. The implemented prototype is able to convert the input voltage of 850 - 1300 V to 1300 V at the output with the efficiency of 99.2% for worst case. The control algorithm provides maximum power point operation and balances the output capacitors even if the capacitor loads are not identical. The second design is implemented for multi-string operation where eight parallel converter is placed. For multi-input single output parallel converters, conventional interleaving does not result in the best operation. Hence, a novel algorithm is presented to find the optimum interleaving phase angle in order to minimize

the capacitor current. Experimentally it is shown that proposed algorithm reduces the capacitor losses by 20% which extend the life-time of the capacitors and hence the designed converter.

Keywords: Multi-string inverter, PV inverter, multi-level converter, silicon carbide, interleaving, capacitor current minimization



ÖZ

ŞEBEKE BAĞLANTILI ÇOKLU DİZİ FV EVİRİCİLER İÇİN ÜÇ SEVİYELİ SİC FAZ KAYDIRMALI BOOST DÖNÜŞTÜRÜCÜLERİN TASARIMI VE GERÇEKLEŞTİRİLMESİ

Altun, Oğün

Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü

Tez Yöneticisi: Doç. Dr. Ozan Keysan

Eylül 2023 , 112 sayfa

Dünya için sonsuz bir enerji kaynağı olan güneş enerjisinin popülaritesi son yıllarda artmıştır. Güneş hücrelerindeki gelişmeler, daha düşük maliyetlerle daha yüksek verim sağlamaktadır. Ayrıca güç elektroniğindeki gelişmeler de popülaritesi arttırmıştır. Bu tezde, 20 kW gücünde üç seviyeli bir yükseltici dönüştürücünün tasarımı incelenmiştir. Tasarlanan dönüştürücü, fotovoltaik sistemlerde yeni trend olan 1500 V çok dizili invertörlerde kullanılmaktadır. Dönüştürücü tasarımı, güç dönüşüm verimliliği tüm koşullar için %99'dan yüksek olacak şekilde optimize edilmiştir. Tasarlanan dönüştürücü daha sonra gerçekleştirilmiş ve deneysel olarak doğrulanmıştır. Silisyum karbür yarıiletkenlerin yardımıyla 80 kHz anahtarlama frekansına ulaşılmıştır. Gerçekleştirilen prototip, en kötü durumda %99.2 verimlilikle 850 - 1300 V giriş gerilimini çıkışta 1300 V'a dönüştürebilmektedir. Kontrol algoritması maksimum güç noktası operasyonunu sağlama ve kapasitör yükleri aynı olmasa bile çıkış kapasitörlerini dengeleme amacıyla kullanılır. İkinci tasarım, sekiz paralel dönüştürücünün yerleştirildiği çok dizili çalışma için uygulanmıştır. Çok girişli, tek çıkışlı paralel

dönüştürücüler için, geleneksel serpiştirme en iyi çalışmayı sağlamaz. Bu nedenle, kapasitör akımını en aza indirmek amacıyla en uygun serpiştirme faz açısını bulmak için yeni bir algoritma sunulmuştur. Önerilen algoritmanın kapasitör kayıplarını %20 oranında azalttığı, böylece kapasitörlerin ömrünü uzattığı ve tasarlanan dönüştürücüyü iyileştirdiği deneysel olarak gösterilmiştir.

Anahtar Kelimeler: Çok dizili evirici, FV evirici, çok seviyeli dönüştürücü, silisyum karbür, serpiştirme, kondansatör akım minimizasyonu





To my lovely family...

ACKNOWLEDGMENTS

First, I would like to express my sincere gratitude to Assoc. Prof. Dr. Ozan Keysan for his mentorship, guidance, and endless support. This thesis would not be possible without his expertise and encouragement.

I would also like to thank dear committee members: Assist. Prof. Dr. Emine Bostancı Özkan, Assoc. Prof. Dr. Murat Göl, Prof. Dr. Mehmet Timur Aydemir and Assist. Prof. Dr. Erhan Demirok for helping me to improve my thesis work.

I want to thank ODTÜ-GÜNAM for their generous funding support for the project to which this thesis belongs. I would like to extend my appreciation to TÜBİTAK-MAM researchers for their assistance and collaboration in the project's development.

I wish to express my deepest thanks to my friends and colleagues. I am grateful to Öztürk Şahin Alemdar, Enes Ayaz, Göktuğ Tonay, Özgür Gülsuna, Nail Tosun, Yunus Çay and Mohammad Derogarian for their support in the design and laboratory works. Without their assistance and dedication, this thesis would not have been completed. Moreover, I would like to thank everyone in METU PowerLab for creating an enjoyable atmosphere within the team.

I am also thankful to TÜBİTAK, the Scientific and Technological Research Council of Türkiye, for granting me their M.S studies scholarship, BİDEB 2210.

I am grateful to my flatmate, Umut Çağrı Işılak, for his support and understanding during the countless late nights I spent working on this thesis. I am also grateful to my friends Alperen Dinçel, Ayla Mollalar, Betül Şerefolu, Harun Bütün, Deniz Dinç, Dilşat Yiğit Bilgen, Gamze Yılmaz, İrem Canbolat, Kaan Aksoy, Nurcan Özşahin, Onur Bilgen and Deniz Yıldız. Their presence made this journey much more bearable.

I owe a special thanks to Zeynep Bilge Bakanoğlu, whose love, support, and encouragement played a significant role in the completion of this thesis.

Lastly and most importantly, I am deeply thankful to my parents, Özer and Gülmine, and my dear sister, Elis, for their lifelong support. I thank them for always being my unwavering foundation.



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LIST OF ABBREVIATIONS

ANPC	Active neutral point clamp
AC	Alternating current
CM	Common mode
DC	Direct current
GaN	Gallium nitride
MOSFET	Metal oxide semiconductor field effect transistor
MPP	Maximum power point
MPPT	Maximum power point tracking
NPC	Neutral point clamp
P&O	Perturb and observe
PV	Photovoltaic
PCB	Printed circuit board
RMS	Root mean square
SiC	Silicon carbide
3L-BC	Three-level boost converter
WBG	Wide band-gap



CHAPTER 1

INTRODUCTION

Today most of the electrical energy is generated using fossil fuels which increases carbon emission and results in global warming [1]. International Energy Agency suggests the zero-emission policy in electrical energy generation until 2040 [2]. In line with these policies, the use of renewable energy in electricity generation is increasing with the guidance of governments. The share of renewable energy in the global market has increased from 25% to 30% from 2017 to 2022 [2].

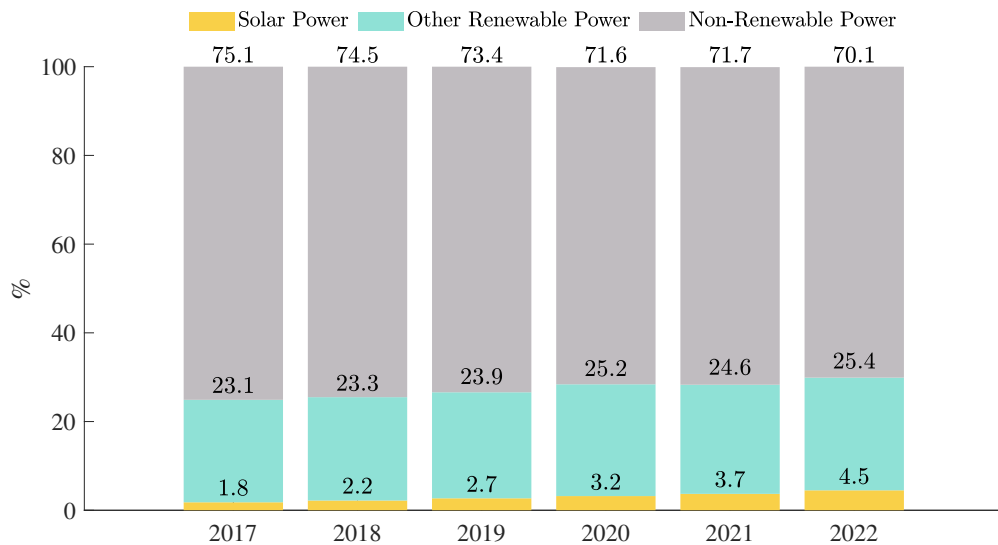


Figure 1.1: Market share of global power

Among all renewable energy sources, solar energy is the fastest-growing in recent years. Thanks to the decrease in the cost of photovoltaic (PV) systems, more attention is gathered by the power generation industry [3]. In 2022, 66% of the installed renewable energy capacity was composed of solar power plants [4]. Based on the pro-

jections, the installed capacity of photovoltaic plants will exceed the coal by 2027 [5].

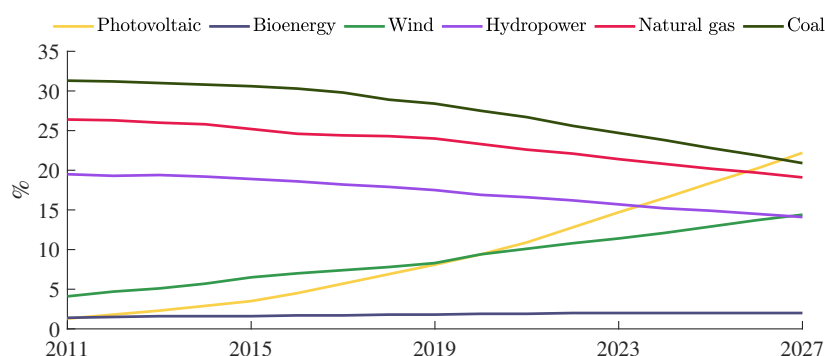


Figure 1.2: Installed capacity of different electricity generation sources

The main reason behind the growth of PV systems is the reduced cost. According to International Renewable Energy Agency, the levelized cost of the electricity of PV systems decreased to \$ 0.11/kWh in 2020, which was \$ 0.34/kWh in 2010 [6]. Another reason for this interest is that its availability in various sizes and places. Apart from other renewable energy sources such as wind and bioenergy, solar plants can be installed also in urban settlements. Higher electricity prices enhance the use of rooftop PV constructions and contribute to the growth of PV market share. Furthermore, utility-scale PV farms are also popular. The installation place of PV panels determines the power level and power electronics topologies.

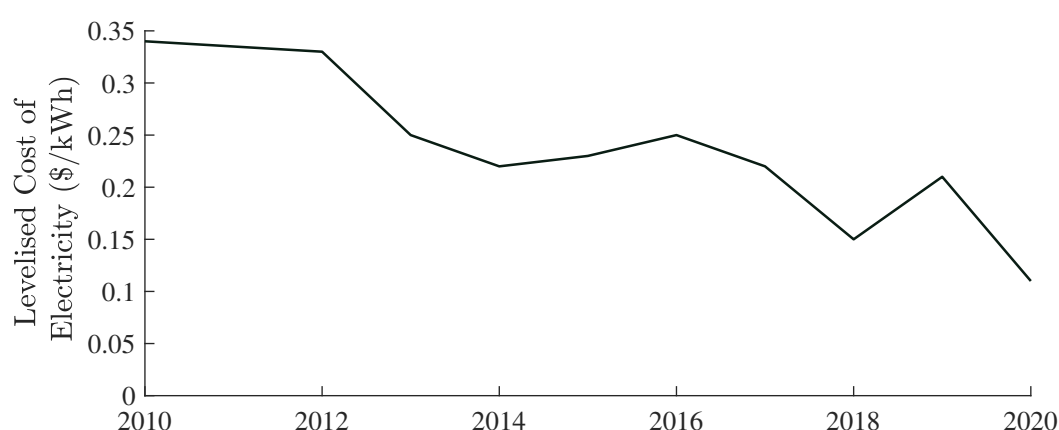


Figure 1.3: Change of the levelized cost of the electricity of PV systems

1.1 Main Types of PV Inverters

PV panels generate direct current (DC) at the output. The output voltage is processed by a power electronics circuit to match the load requirements. The load can be an individual device or the alternating current (AC) grid. Different PV inverter types are utilized in solar applications, as shown in Fig. 1.4.

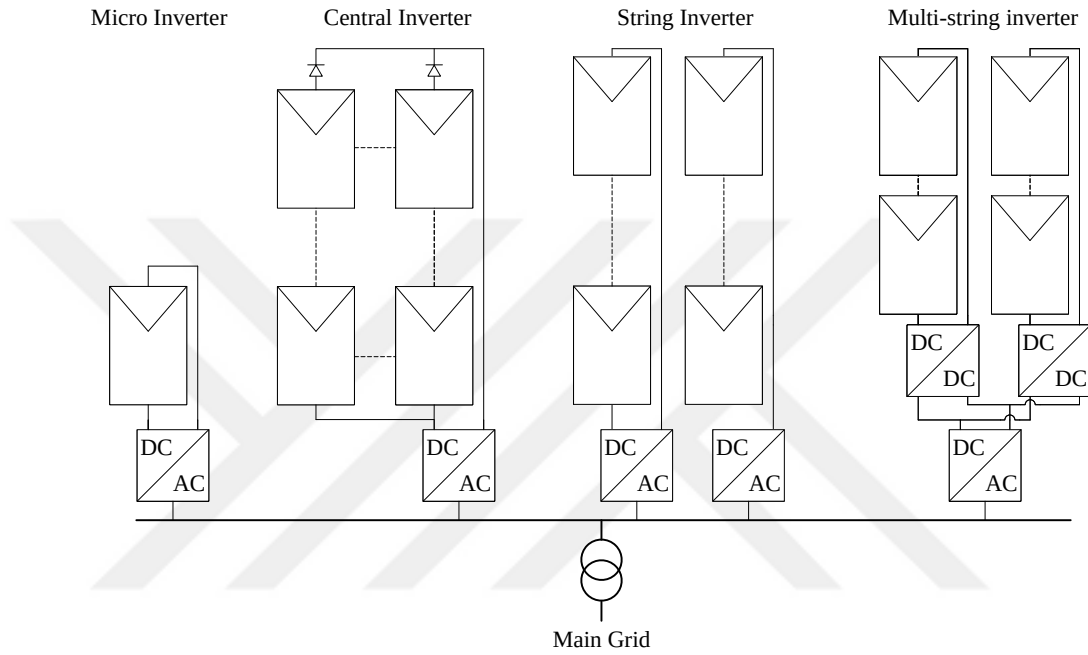


Figure 1.4: Grid-connected PV inverter types

- The micro-inverters are used in low-power PV systems. Each individual inverter is mounted on a single PV panel [7]. This connection allows each solar panel to operate independently. Panel-level DC to AC conversion provides panel-level optimization. If a single panel is shaded in a PV power plant, the remaining panels are not affected, thanks to independent connection. The main drawback of micro inverters is the higher initial cost. The need for an inverter for each PV panel increases the installation cost. Hence, it is not suitable to build a solar power farm. Instead, household usage is much preferable.
- Central inverters are large-scale inverters designed to handle high-power demand. A number of PV panels are connected in series to have a PV string.

Then, PV strings are paralleled to increase the power level. Constructed PV panel structure is connected to a single DC/AC conversion unit, and power is transferred to the grid [8]. Single power electronics circuit for a huge number of PV panels provides a cost-effective solution. However, as opposed to micro inverters, only system-level optimization is possible. Controlling the PV arrays as a whole, the maximum power of each PV panel is not guaranteed. In addition, a failure in the system may result in a complete shutdown resulting in significant energy lost.

- String inverters are the inverter types present between the micro inverters and central inverters. Medium-sized power generation is provided by this inverter type. Different than central inverters, each PV string constructed by a series connection of PV panels is directly connected to DC to AC converter [3]. This provides string-level power control. The power of each string can be maximized independently. Additionally, if a failure happens in a string, the remaining modules can still operate and transfer power to the grid.
- The last type is the multi-string PV inverter which combines the advantages of central and string inverters. Multiple PV strings are connected to increase the power level. Different than central inverters, this time, each string is connected to a DC/DC converter [3]. Instead of PV strings, DC/DC converters are paralleled, and a DC link is constructed. Then, DC to AC conversion establishes the grid connection. The use of DC/DC converters provides string-level power control. Failures in PV strings can be fixed by disconnecting a string instead of total shutdown. These advantages make this inverter type the market leader in recent years [9]. The market share increased to 61% in 2019, which was 37% in 2015.

1.2 1500 V Trend in PV Systems

The voltage and current of a PV string can be determined by changing panel size, PV cells in panels, and the number of PV panels in the string. However, some voltage levels have become popular in the PV industry. This way, devices that are compatible with each other can be easily used. Voltage level of a PV system is identified as the

maximum voltage that can be obtained by a PV string. Nowadays, 1500 V strings and 1500 V string inverters are the new trends in the market, and most industrial company develops compatible products. By increasing the maximum voltage level to 1500 V from the previous voltage standard of 1000 V, the current levels of the systems decrease to reach the same power. Decreasing the current level helps to decrease losses. Additionally, decreasing current may result in a decrease in the used copper, which results in cost-effective PV systems.

Developments in the 1500V PV systems are followed by researches in different subjects. In [10], 1000V and 1500V PV systems are compared in terms of installation requirements. The reduction of the array cabling and combiner boxes is reported by this voltage transition. Reliability and safety updates that need to be completed for 1500 V systems are discussed in [11]. The change of voltage also brings the studies in converter topologies. In [12], the design of a three-level inverter is presented for 1500V PV systems. [13] compares the multilevel DC/DC converters and emphasizes the advantages of wide band-gap (WBG) devices in 1500 V PV structures.

1.3 Wide Band-Gap Semiconductors

In a power converter, the requirements are high efficiency and high power density, which means less volume and low cost. Wide band-gap devices provide high efficiency and high power density requirements. Although WBG devices are more expensive than the silicon-based counterparts, the advances in semiconductor technology reduced the cost and commercialized the gallium nitride (GaN) and silicon carbide (SiC) devices. The commercial SiC schottky barrier diodes have been used since 2001 [14]. The SiC MOSFETs at different voltage and current levels also became available in the following years [15].

The higher breakdown voltage of WBG semiconductor technology made thinner wafer used power devices possible to be used in high voltage applications [16]. Especially the SiC devices can reach very high voltages in reasonable sizes. The devices with thinner semiconductors provide low channel resistance and decrease conduction losses. The smaller semiconductor area also decreases the gate area and the gate

charge, which eventually makes WBG devices achieve high switching speeds. Consequently, WBG devices are subject to low switching losses and can reach switching frequencies (up to hundreds of kHz) that silicon counterparts cannot operate [17]. Increasing the frequency of the power converter downsizes the filtering elements like inductors and capacitors. Moreover, thanks to their lower losses, it is possible to use lower-volume cooling apparatus. All in all, the overall volume and weight of the converters can be minimized thanks to the use of WBG devices.

Another important criterion for semiconductor devices is the thermal performance. The thermal conductivity of SiC is two times higher than the silicon [18]. Hence, the generated loss can be easily removed. Moreover, as noted in [19], the SiC devices can be operational at extremely high temperatures (up to 450°C.) However, this is not applicable with regular plastic packages. Yet, the junction temperature of SiC devices in plastic packages can be increased to 175°C as mentioned in device datasheets. The silicon devices, however, can reach 125°C [20]. At high ambient temperatures, like PV systems operating under sunlight, it is advantageous to use SiC devices.

In short, WBG devices (especially SiC) provide great opportunities to PV systems where temperature is critical and high voltage levels are present. In the literature use of SiC in PV systems is studied in many papers [13, 16, 21, 22]. In addition to academic papers, industrial companies also benefit from SiC devices and produce efficient and power-dense products [23, 24].

1.4 Motivation of the Thesis

In this thesis design of the three-level boost converters (3L-BC) is investigated for a grid connected multi-string PV inverter. The multi-string PV inverters hold a large share in PV industry. The new 1500 V trend in PV systems improves system performance. The designed converter is planned to be used as the DC/DC stage in "Design of the 1500 V PV string inverter" project which is funded by TÜBİTAK 1004 research program. The DC/AC stage is designed by TÜBİTAK MAM researchers and out of scope of this thesis.

The design of converter is accomplished to reach efficiency above 99% for the rated

operating conditions. SiC semiconductor devices are analyzed for the loss and efficiency performance, and device selection is discussed with the switching frequency optimization. The magnetic design of the boost inductor is performed so that it is suitable for power ratings and efficiency requirements. The designed converter is implemented and tested under different conditions. The issues on the implementation stage is discussed and possible suggestions are proposed to improve the design. Afterward, the new layout design of parallel converters are presented with the improvements. The effect of interleaving of converters is on the output capacitor current is studied. Conventional interleaving method is improved and a new algorithm is suggested to find phase shift of parallel converters. Thanks to proposed algorithm, it is experimentally shown that capacitor losses can be decreased by 20% compared to conventional methods.

1.5 Outline of Thesis and Contributions

Chapter 2 mainly analyzes the multi-string inverter topology. Firstly, the I-V characteristic of PV systems is discussed, and the requirements of the DC/DC and DC/AC stages are presented. Then, commercial multi-string inverter topologies are compared. The design decisions are discussed. Power and voltage levels are specified. Then, the requirements of DC/DC converters are stated. Afterward, DC/DC converter topologies are studied with their advantages and disadvantages. Finally, the maximum power point algorithms are presented and compared.

In Chapter 3, the analytical design of the 3L-BC is investigated. First, the operation principle of the converter is studied. Circuit waveforms of different switching schemes are observed. The semiconductor selections are discussed based on the voltage-current ratings and loss comparisons. The inductor design decisions are justified with loss comparisons. The last component is the output capacitor which is selected based on the voltage and current ratings. Then, the common mode leakage current analysis is performed for switching schemes. Cooling system requirements are described, and thermal design results are given for worst-case analysis. At the end, control of the converter is presented.

Chapter 4 focuses on the implementation and the experimental results of the prototype design. The specifications of the built prototype printed circuit board are discussed. Then, a series of experimental results are conducted and compared with the analytical expectations. The inductor design is first verified. Common mode leakage current measurements are presented for different configurations. At rated voltage, the semiconductor device voltage waveforms are observed with input and output waveforms. Then, calorimetric loss and efficiency measurements are introduced. Moreover, the thermal performances of the critical components are observed by thermal images. Lastly, the control algorithms are experimentally verified. The verifications and the significant outcomes are concluded.

In Chapter 5, the design of the eight-parallel 3L-BC is presented. The experimental results provide the rated operations of the converters. Then, a novel method is explained to minimize the DC-link capacitor current, which is based on harmonic analysis. The proposed method is compared with the literature. The harmonic analysis derivations are introduced and compared. Finally, the method is verified by parallel operation of DC-DC converters.

Chapter 6 concludes thesis and evaluates the design outcomes. Possible improvements and the future work are discussed.

CHAPTER 2

OPERATION AND DESIGN CONSIDERATIONS OF MULTI-STRING PV INVERTER

The previous chapter discusses the popularity of PV power generation and compares different PV inverter types. Multi-string inverters have a significant market share thanks to mentioned advantages. In this chapter, design decisions will be evaluated for the multi-string inverter. Firstly, the I-V characteristics of a PV panel will be investigated. Then, the structure of a multi-string inverter will be presented. Duties of DC/DC and DC/AC stages will be given. The commercially available multi-string inverters will be compared, and the design parameters will be specified. Then, different topologies will be analyzed and compared for the DC/DC stage.

2.1 PV Characteristics and Multi-String Inverter Operation Principles

The power that a PV panel can generate depends on several factors. Firstly, the output voltage of a PV panel is directly related to the current drawn. Moreover, the solar irradiation and the temperature of the PV cells change the I-V characteristics of the panel [25]. In Fig. 2.1, a sample I-V characteristics of the PV panel is presented. As the current of the panel increases, its terminal voltage decreases. The voltage where there is no panel current is named open-circuit voltage (V_{oc}). The maximum current that a panel can supply is the short-circuit current (I_{sc}), which is obtained if panel terminals are short-circuited. The panel power diminishes at those boundaries, and the maximum power point (MPP) of a PV panel places between them. As shown in the figure, panel current is directly related to solar irradiance. Additionally, the temperature of the PV cells determines the voltage, and higher voltages can be obtained

at lower temperatures. Hence, the MPP of a PV panel changes throughout the day according to ambient conditions. In order to maximize the generated power, maximum power point tracking (MPPT) algorithms are utilized.

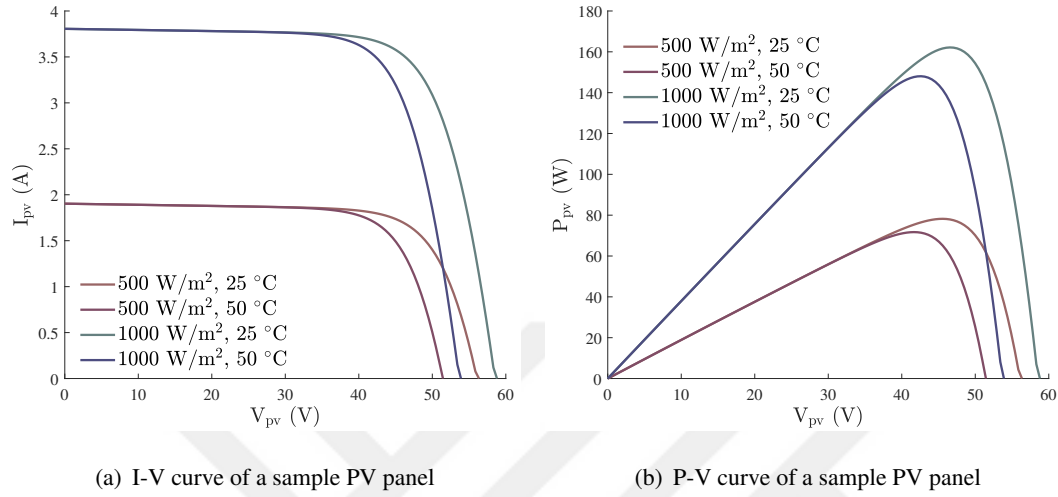


Figure 2.1: PV panel characteristics at different temperatures and irradiance

In Fig. 2.2, the overall block diagram of the multi-string inverter topology is presented. Several PV panels are connected in series, and a PV string is constructed. PV string is connected to a DC/DC converter. This string and DC/DC converter structure are paralleled according to the power level of the converter. A DC-link is constructed at the output of the DC/DC converters. Then, DC to AC power conversion is accomplished. Although the DC/DC and DC/AC stages work in accordance, the function of each stage can be summarized as follows. The DC/DC converters are responsible for the MPP operation of each string [26]. Based on the algorithm and control technique, PV panel voltage is kept at MPP voltage (V_{mpp}). The duty of the DC/AC converter is to keep the DC-link voltage constant and transfer the power coming from the DC/DC converters to the grid. Hence, each stage is critical in a string inverter topology. In [27], the contribution of the DC/DC stage is evaluated in comparison with the topologies that do not employ an intermediate DC/DC stage. DC/DC converters increase the PV panels' operation voltage range and the system's flexibility.

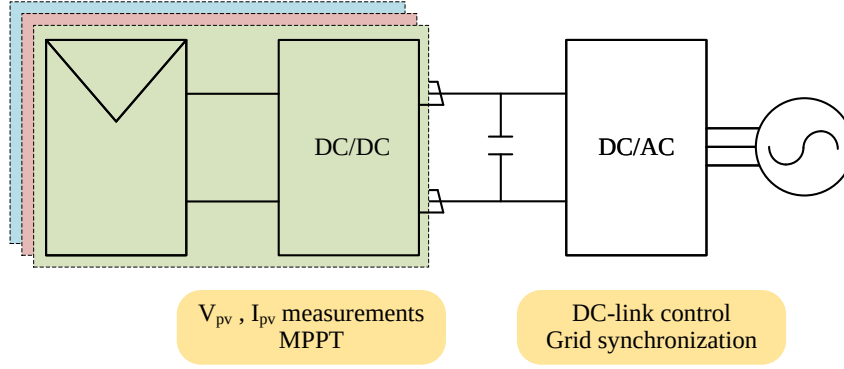


Figure 2.2: Multi-string inverter operation diagram

2.2 Specifications of Commercially Available Multi-String Inverters

As declared in Chapter 1, multi-string inverters have the greatest market share in the PV industry. Hence, many solar power plants are constructed and operated by commercial inverters. It was stated that 1500 V PV strings with the related equipment are the trend of new power systems. However, the power level of a string and the number of strings in an inverter is the design criteria. To design a new inverter, it is a good practice to analyze the market-leading products and select power levels accordingly. In Table 2.1, the specifications of the commercial multi-string inverters are presented.

It is shown that there are different power level inverters present and different numbers of string connections are available. All of the example products have either 2 or 3 strings for a DC/DC converter. Hence, it means that the 2 or 3 strings can be paralleled at the DC input. This specification does not affect the power electronics circuit used. However, it gives an idea about the power level of mostly used strings. The power of a single string that can be connected to available products is between 7 kW and 14 kW, but 10 kW is more common. The other selection parameter is the number of MPPT trackers and hence the total power rating. As a design choice, 125 kW rating is targeted. The number of MPPT converters is selected as 8. The number of strings per converter is 2. Hence 7.5-8 kW strings can be paralleled and used in the input. However, to be compatible with the higher power level PV strings, the maximum

Table 2.1: Specifications of commercial multi-string PV inverters

Product	Total Power	Number of MPPT Converters	Number of Strings	Power per String
HUAWEI SUN2000-185KTL-H1	175 kW	9	18	9.7 kW
FIMER PVS-175-TL	175 kW	12	24	7.3 kW
SUNGROW SG250HX	250 kW	12	24	10.4 kW
SUNGROW SG125HX	125 kW	6	12	10.4 kW
GOODWE GW250K-HT	250 kW	12	24	10.4 kW
GOODWE GW250KN-HT	250 kW	6	18	13.9 kW

power rating of the DC/DC converters is selected as 20 kW. This way, by connecting the desired number of strings to inputs, the rated power can be achieved for varying string number and power. Moreover, these specifications allow it to be used with different powered strings at the same time. If some of the strings have higher power due to better sunlight exposure, the remaining ones can operate at lower power, and still, maximum power can be transferred to the grid.

The other common property of these inverters is the output voltage. All products have 800 V at the output side. Hence, the output voltage is going to be 800 V for the designed inverter. Three-phase 800 V output generation requires at least 1130 V DC link if the space vector pulse with modulation is utilized. Not to operate near the unity modulation, a higher DC-link voltage level is preferred.

To decide on the voltage limits of the designed converter, the input side specifications of the same multi-string inverters are investigated and presented in Table 2.2. Moreover, according to sample annual data given in [27], the MPP voltage of a 1500 V rated PV string changes between 850 V and 1200 V in different seasons, which gives an idea about the selection of voltage limits.

Table 2.2: Input voltage specifications of commercial multi-string PV inverters

Product	MPPT Input Voltage Range	Nominal Input Voltage
HUAWEI SUN2000-185KTL-H1	500 V- 1500 V	1080 V
FIMER PVS-175-TL	850 - 1350 V	1100 V
SUNGROW SG250HX	860 - 1300 V	1160 V
SUNGROW SG125HX	860 - 1300 V	1160 V
GOODWE GW250K-HT	500 - 1500 V	1160 V
GOODWE GW250KN-HT	500 - 1500 V	1160 V

Based on the investigations of products and the output voltage requirements, the specifications of the DC/DC converter stage are summarized in Table 2.3. To compete with the commercial products, the aimed DC/DC conversion efficiency is 99% for the specified input voltage range.

Table 2.3: Design specifications of DC/DC converters

Number of DC/DC Converters	8
Number of Input Strings	16
Output Voltage	1300 V
Single Converter Rated Power	20 kW
Maximum Input Current	24 A
MPP Input Voltage Range	850 V - 1300 V
Nominal Input Voltage	1050 V
Efficiency	>99%
Maximum Ambient Temperature	50°C

2.3 DC/DC Converter Topologies

According to the specified parameters in Table 2.3, a voltage-boosting DC/DC converter is required between the PV input and the inverter. The converter should provide MPPT operation and be suitable for the rated power operation. In the literature, there are different types of DC-DC converters studied. Overall, the DC-DC converters are classified as isolated and non-isolated ones.

Isolated converters provide galvanic isolation between the input side and the output side. The voltage transformer used in the circuit ensures electrical separation. Forward, push-pull and bridge converters are the well-known examples. Instead of a transformer, a coupled inductor can also provide isolation, like in a flyback converter. These converters are used in applications where high voltage gain is required. Additionally, applications with strict safety requirements take advantage of galvanic isolation. Generally, in grid-connected implementations, the standards require isolation for increased safety [28]. However, if there is no restriction and no need for a high voltage ratio, the use of magnetic components is not preferred due to the cost and increased weight of the components.

Non-isolated converters are simpler than isolated ones. The input and output are electrically connected, and a transformer or coupled inductor is not required. In simple applications, they provide cost-effective solutions. The well-known examples of non-isolated converters are buck, boost, buck-boost, cuk and sepic converters. The first three require only two switching devices, a single inductor, and a capacitor. The latter two contain additional filtering capacitors and inductors.

As discussed in the previous section, the output of the designed inverter will be connected to 800 V grid. The output is then increased to distribution system voltage levels by line frequency transformers. Hence, additional isolation is not required in the multi-string inverters. To decrease the cost of the device, all of the above-mentioned commercial products use transformerless designs. Hence, the same practice will be utilized in the design. The simplest voltage-step-up converter, boost, and multilevel versions will be analyzed and compared.

The conventional boost converter circuit schematic is given in Fig. 2.3.a. When

switch S is in conduction, the inductor is charged up. When it is off, inductor current flows through to output, and voltage step up is achieved. The number of switching devices is two; the filtering elements are an inductor and a capacitor. Although it is the simplest solution to stepping up the voltage, it becomes disadvantageous when used in high-voltage applications [29]. The switching devices should be capable of blocking the output voltage, which is 1300 V for the designed converter. Additionally, the output capacitor also needs to handle the rated output voltage. Since these voltage levels are more specialized, as the voltage level increases, the number of available devices decreases, and the cost increases. The available insulated-gate bipolar transistors (IGBT) can provide the required voltage levels. However, high switching frequencies are not applicable to them. Hence, the filtering equipment becomes larger, which increases the cost size and weight. Therefore, multilevel converters are studied in the literature as an alternative to the conventional converters.

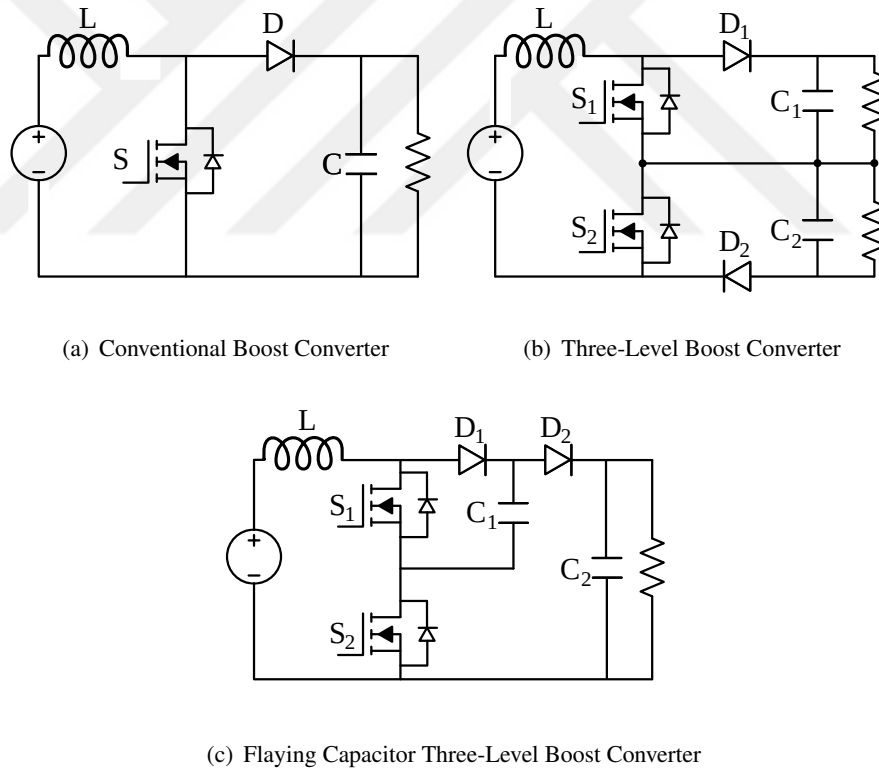


Figure 2.3: Boost converter types

In Fig. 2.3.b and 2.3.c, two multilevel boost converters are presented, namely three-level boost converter (3L-BC) [30] and flying capacitor three-level boost con-

verter (FC-BC) [31]. For an N-level converter, the required voltage is divided by the N-1 devices [32]. Hence, lower voltage rated switching devices can be utilized. As the number of levels increases, the required voltage rating of semiconductor devices decreases. On the contrary, the number of devices and passive components increases, which makes the circuit more complex. Additionally, the overall cost of the system may start to increase after some point. For a 1300 V rated converter, it is now easier to find switching devices at 650 V. Hence three level systems are suitable and beneficial for 1500 V PV systems [13].

In 3L-BC topology, two series-connected capacitors are present at the output. Hence, each one is rated at half of the output voltage. The switching devices then need to block only half of the output voltage. This property is ensured in FC-BC by using C_1 capacitance, which is named as flying capacitor. This capacitance is charged up to half of the output voltage, and the voltages of devices are set accordingly [29]. However, the second capacitance C_2 is rated at the full output voltage. The most significant difference between 3L-BC and FC-BC is the connection to the midpoint of the load. Similar to DC/DC converters, three level designs are popular in DC/AC stage. Neutral point clamp (NPC) and active neutral point clamp (ANPC) inverters utilize the midpoint of the DC-link capacitors to create a new voltage level at the grid side [33]. Based on the modulation method used in the inverter, the load of each DC-link capacitor may differ in time, which means the voltages differ from each other. This fact decreases the performance of the DC/AC side. In the literature, 3L-BC is pointed out to solve this problem [34]. By arranging a proper control algorithm, it is shown that the load imbalance of the capacitors is handled, and inverter performance is increased.

2.4 Maximum Power Point Tracking Algorithms

The characteristics of a PV string is explained in Section 2.1, and it is discussed that DC/DC converters are responsible for the MPP operation. In the literature, many MPPT algorithms were developed and compared for different performance factors. There are a few algorithms that keep the voltage of the panel at a constant level. Since the irradiance does not make an important change in the MPP voltage (V_{mpp})

of the panel, constant voltage operation provides the operation close to MPP [35]. V_{mpp} is mostly affected by the temperature; hence, temperature sensor integrated controls are also studied [36]. Additionally, algorithms that mathematically represent the I-V curve of PV panels are investigated in the literature [37, 38]. The drawback of all previous methods is the requirement of panel characterization. Variables should be updated based on the used string. There are also panel-independent MPPT algorithms. Perturb and observe (P&O) and incremental conductance algorithms are the most popular ones, which do not require panel parameters [39].

2.4.1 Perturb and Observe MPPT algorithm

P&O is a simple and widely used MPPT algorithm. The main working principle is perturbing the PV panel's operation point and observing the output power change. The block diagram of the algorithm is shown in Fig. 2.4. Algorithm starts by measuring the PV power at the current operating point and then gradually adjusts the operating point in a certain direction (either increasing or decreasing voltage/current) to observe the corresponding change in power. If the power output increases, the algorithm continues perturbing in the same direction; however, if the power output decreases, it changes direction. Before the algorithm is started, the PV panel voltage is mostly equal to V_{oc} . Then the first change should decrease the panel voltage. When the second measurements are obtained, the algorithm runs in a continuous loop. Panel voltage gradually decreases until it goes below the V_{mpp} . Then, it changes direction. This way, the PV voltage oscillates around the MPP voltage. The oscillation amount depends on the perturbation voltage (ΔV). If ΔV is large, MPP is found in a short time, but oscillation around MPP becomes large. If it is small, the oscillation amount decreases, but reaching the MPP takes a long time. This issue is studied in the literature, and variable ΔV operations are demonstrated to solve the problem[40, 41].

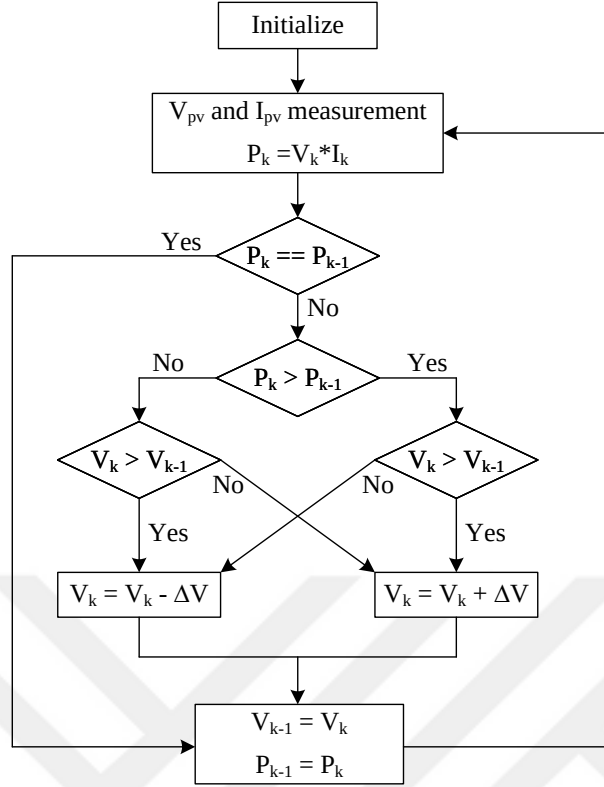


Figure 2.4: Block diagram of the perturb and observe algorithm

2.4.2 Incremental Conductance MPPT algorithm

The incremental conductance algorithm is another well-known and used MPPT algorithm. It is mainly based on the derivative of the PV power with respect to PV voltage which is given in (2.1).

$$\frac{dP}{dV} = \frac{d(IV)}{dV} = I + V \frac{dI}{dV} \quad (2.1)$$

At panel MPP voltage, the derivative is zero. On the left of the MPP, it is positive and becomes negative on the right side of the MPP. The resulting cases are given in (2.2). The conductance (I/V) and the incremental conductance (dI/dV) comparison gives the position of the operation point. Then, the panel is directed to the MPP voltage. Ideally, the algorithm keeps the panel voltage constant during the MPP operation. However, this point may not be found if the voltage step is not well adjusted. Hence,

similar to the P&O algorithm, adaptive methods are required to arrange the step size of the algorithm [42].

$$\begin{aligned}\frac{dI}{dV} &= -\frac{I}{V} \Rightarrow V = V_{mpp} \\ \frac{dI}{dV} &> -\frac{I}{V} \Rightarrow V > V_{mpp} \\ \frac{dI}{dV} &< -\frac{I}{V} \Rightarrow V < V_{mpp}\end{aligned}\tag{2.2}$$

As stated, P&O and incremental conductance are the most used algorithms. They provide the ability to track the MPP efficiently when used with proportional-integral control loops [39]. Due to its simplicity, the P&O MPPT method will be utilized in the design.

2.5 Conclusion

In this chapter, firstly, the characteristic of a panel was analyzed. It was shown that the MPP of a PV panel may change based on environmental conditions. The significance of the multi-string inverter's DC/DC stage was emphasized as the key point for achieving MPP operation, complemented by the DC/AC stage maintaining a constant DC-link voltage. The discussion then shifted to determining the power and voltage ratings of the DC/DC converters based on the commercial products and literature review. The DC/DC stage should be capable of converting input voltages ranging from 850 V to 1300 V to output of 1300 V at a rated power of 20 kW, while targeting a remarkable 99% efficiency during rated power operations. Additionally, comparison of various DC/DC topologies highlighted the advantages inherent to each. Thanks to the lower voltage ratings required, and the connection to the midpoint of the load, 3L-BC will be used in the design of the multi-string PV inverter. The chapter concluded by presenting MPPT algorithms that maintain the panel voltage at its MPP level. Due to its simplicity, the P&O algorithm will be utilized in the design. In the next chapter, the analytical design procedure of the 3L-BC will be studied and the control algorithms will be explained.



CHAPTER 3

DESIGN OF THE THREE-LEVEL BOOST CONVERTER

3.1 Introduction

The previous section presents the overall structure of a string inverter topology and operations of DC-DC and DC-AC stages. The design specifications of the string inverter are discussed. Moreover, the considerations for the selection of three-level boost converter topology are explained.

In this chapter, the design of the converter will be presented. Firstly, the operation of the converter will be investigated with circuit waveforms, and analytical derivations will be given. Then, the selection of the circuit components will be discussed, and loss analysis will be performed. The design will be analyzed for common mode leakage currents. For the losses of the devices, the cooling analysis will be given. Afterward, the control algorithms of the converter will be explained.

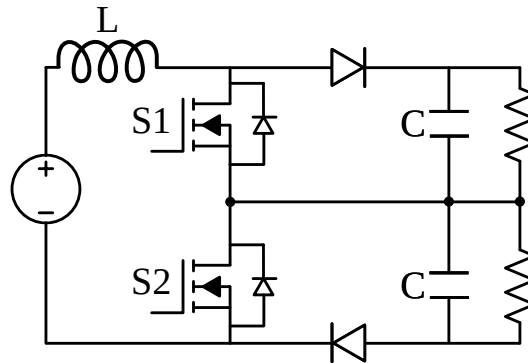


Figure 3.1: 3L-BC circuit schematic

3.2 Operation Principles of 3L-BC

The circuit schematic of 3L-BC is given in Fig. 3.1. Switches S_1 and S_2 can be turned on simultaneously, or a phase shift can be given between the switches. Depending on the duty cycle of switches and phase shift, there are four possible states of the converter which are given in Fig. 3.2. Conducting semiconductors are indicated as short-circuit connections, whereas nonconducting paths are open-circuited.

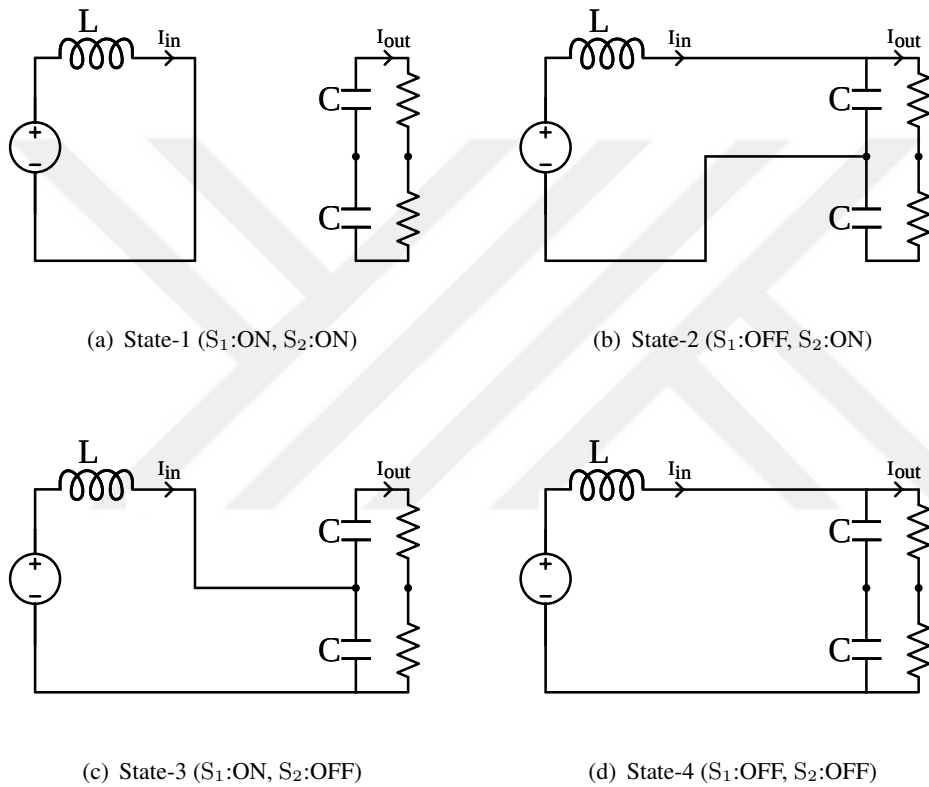


Figure 3.2: States of the 3L-BC for all switch conditions

If the switches are turned on in-phase and duty cycles are identical, 3L-BC operates as a regular boost converter, and the converter alternates between State-1 and State-4. The output voltage (V_o) of the converter is given in (3.1) in terms of input voltage (V_{in}) and duty cycle (d).

$$V_o = \frac{1}{1-d} V_{in} \quad (3.1)$$

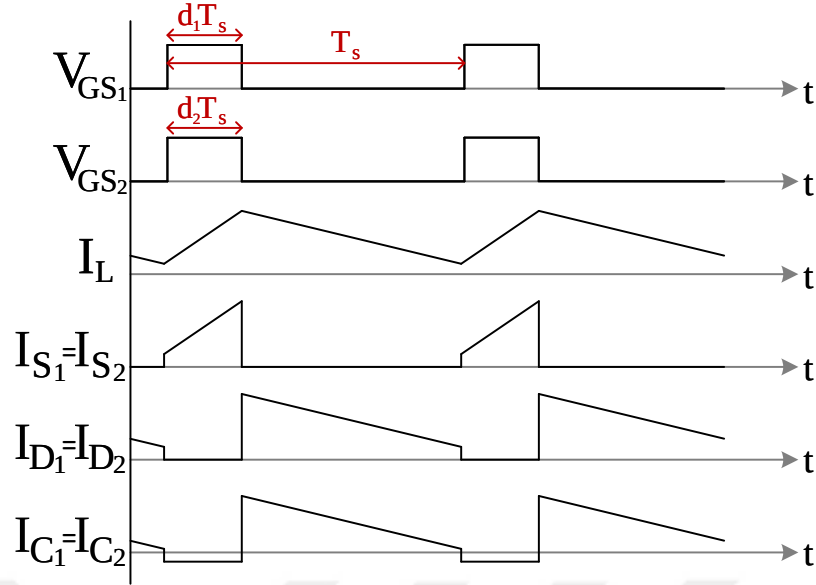


Figure 3.3: 3L-BC in-phase switching waveforms

Switching timings and current waveform of the inductor, switches, diodes, and capacitors are given in Fig. 3.3 for this switching scheme. In this case, the inductor ripple frequency is the same as the switching frequency (f_s). The peak-to-peak current ripple is calculated by (3.2) in terms of input voltage, output voltage, switching frequency, and inductance value (L).

$$\Delta I_L = \frac{V_{in} \left(1 - \frac{V_{in}}{V_o}\right)}{L f_s} \quad (3.2)$$

When the switches are turned on out-of-phase (i.e., with a phase shift of 180°), there are three possible circuit states. If the sum of duty cycles d_1 and d_2 is smaller than 1, possible states are 2, 3, and 4. On the other hand, possible states are 1, 2, and 3 if the sum of duty cycles is larger than 1. The first case is presented in Fig. 3.4 with switching timings and current waveforms of the circuit components. Here, it is important to note that equal-valued capacitors are used at the output to equally share the output voltage. Moreover, the duty cycles of switches are equal ideally. In fact, the duty cycles of switches are adjusted independently to balance the output capacitor voltages caused by nonidealities. Those situations will be examined later

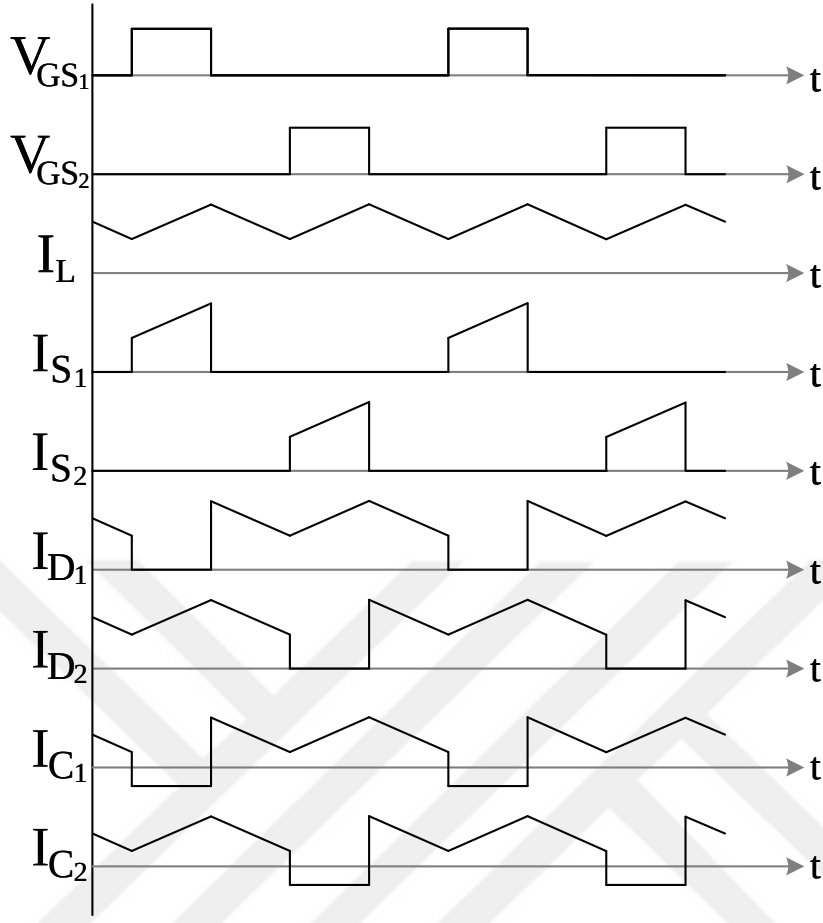


Figure 3.4: 3L-BC out-of-phase switching waveforms ($d_1=d_2<0.5$)

in Section 3.8.2. In the below analysis, an ideal operation is assumed. As shown in Fig. 3.4, the inductor charges up in State-2 and 3 with a voltage of $V_{in} - V_o/2$, whereas discharges in State-4, where inductor voltage is $V_{in} - V_o$. Hence, the voltage transfer ratio of the converter is found using the volt-second balance of the inductor as in (3.3) and (3.4). The resulting transfer ratio becomes the same as a conventional boost converter.

$$(V_{in} - V_o/2)(2d) + (V_{in} - V_o)(1 - 2d) = 0 \quad (3.3)$$

$$V_o = \frac{1}{1-d} V_{in} \quad (3.4)$$

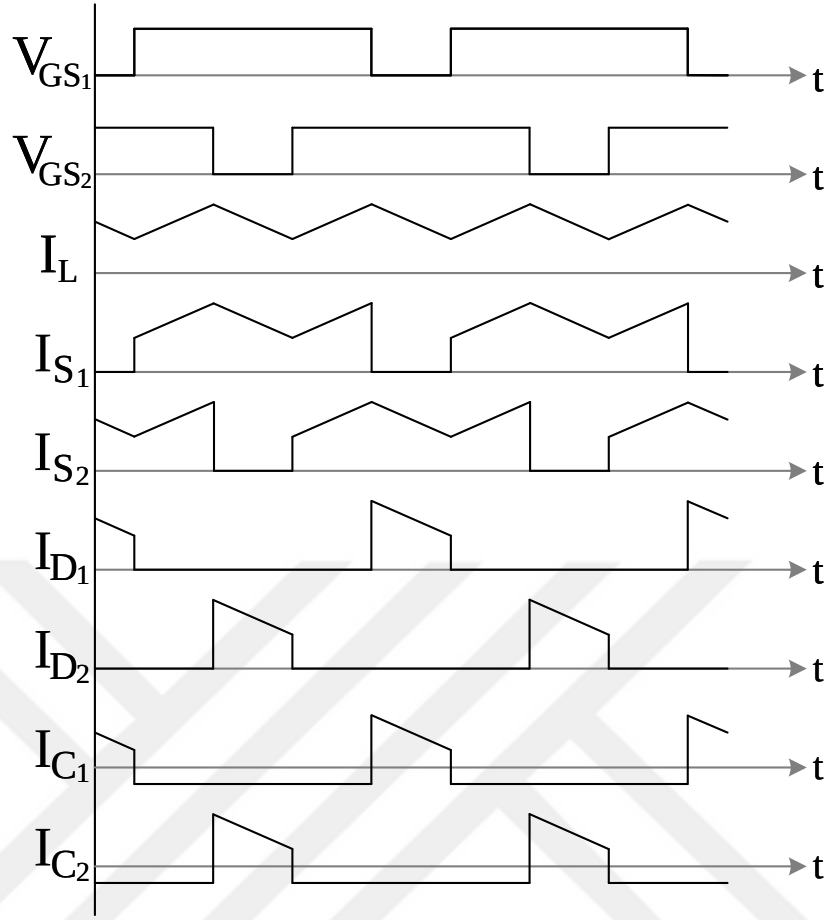


Figure 3.5: 3L-BC out-of-phase switching waveforms ($d_1=d_2>0.5$)

In Fig. 3.5, the second case is represented where d_1 and d_2 are equal and larger than 0.5. The inductor charging state is State-1, and the charging voltage is V_{in} . State-2 and 3 discharge the inductor with a voltage of $V_{in} - V_o/2$ in this case. Volt-second balance is given in (3.5) with timings shown in Fig. 3.5. The resulting voltage transfer ratio is equal to the first case (3.4).

$$(V_{in})(2d - 1) + (V_{in} - V_o/2)(2 - 2d) = 0 \quad (3.5)$$

It can be seen from both inductor current graphs that the effective frequency of the current is doubled due to phase-shifted switching. The peak-to-peak current ripple is calculated by (3.6) for this switching scheme. Assuming a lossless system, the nor-

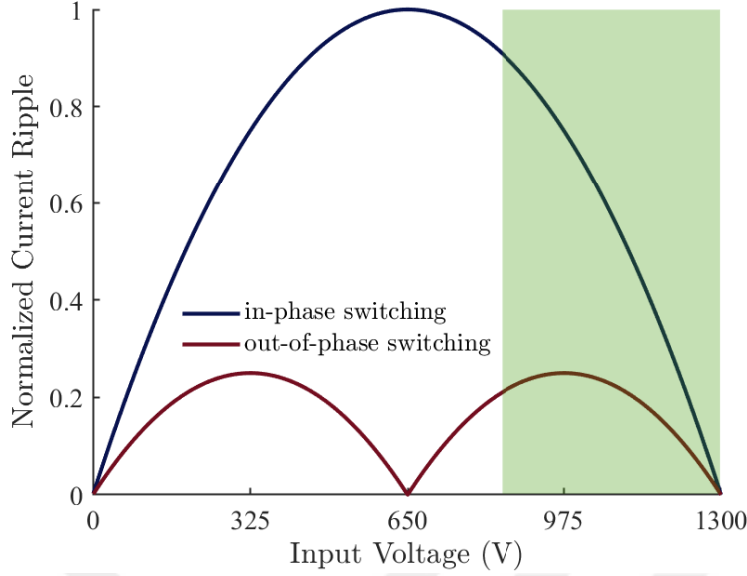


Figure 3.6: Current ripple comparison of switching techniques

malized current ripple comparison of the switching schemes is given in Fig. 3.6. In the comparison, the input voltage is swept from 0 V to 1300 V, which is the rated output voltage. As shown in the figure, out-of-phase switching reduces the current ripple in a significant manner. Moreover, the characteristics of the curves are different. In-phase switching results in maximum ripple at $d = 0.5$, where the input voltage is half of the output voltage. For this condition, out-of-phase eliminates the ripple in the inductor. The maximum current ripple occurs at $d = 0.25$ and $d = 0.75$, which are all smaller than the in-phase switching ripple values.

$$\Delta I_L = \begin{cases} \frac{(2V_{in} - V_o)(1 - V_{in}/V_o)}{2f_s L} & \text{if } V_{in} > 2V_o \\ \frac{(V_o - 2V_{in})(V_{in}/V_o)}{2f_s L} & \text{if } V_{in} < 2V_o \end{cases} \quad (3.6)$$

In Chapter 2, rated operating conditions of the converter were discussed. Each converter should be capable of processing 20 kW of power within the input voltage range of 850-1300 V. For these limitations, the maximum, minimum and nominal operating conditions of the converter are summarized in Table 3.1. For the minimum input voltage of 850 V, maximum duty cycle is required, which is 0.35. The rated operating input voltage range is also marked in the Fig. 3.6. As input voltage increases, the ra-

Table 3.1: Operation limits of the converter

V_{in}	I_{in}	d	Switch Duty	Diode Duty
850 V	23.8 A	0.35	0.35	0.65
1050 V	19.3 A	0.19	0.19	0.81
1300 V	15.5 A	0	0	1

tio of the current ripple for switching techniques diminishes. However, for minimum input voltage operation the ratio increases to 4.25. According to the inductor current ripple analysis, it is reasonable to turn on switches with 180° phase shift.

3.3 Semiconductor Device Selection

The operating principles of the converter are analyzed, and operating conditions are discussed. The next step of designing the converter is the selection of semiconductor devices that can withstand the designed voltage and current levels. As discussed in Section 1.3, SiC semiconductor devices provide high efficiency, and switching frequency can be increased thanks to low switching losses. Hence, SiC MOSFETs and diodes are considered to be used in the design.

The voltage that needs to be blocked by the MOSFETs and diodes is $V_o/2$, which is 650 V. However, voltage spikes occur in the semiconductors at the switching instants due to the inevitable path inductance of the circuits. Hence, the voltage rating of the semiconductors should have a safety margin. In the market, there are 900 V, and 1200 V rated SiC devices available, which can be used in the design of the converter [43].

Semiconductors' maximum average current is 23.8 A, which is the case with minimum input voltage with rated power operation. As the junction temperature increases, the drain-source resistance (R_{DS}) of the MOSFETs and the forward voltage drop of the diodes increase for SiC technology. Hence, the device's current carrying capability weakens. Therefore, the current rating was selected assuming the junction temperature is around 150°C . As stated in Section 1.3, the junction temperature of SiC

devices can be increased to 175°C.

Another important point while choosing the MOSFET is the kelvin source connection. Kelvin source is an additional pin to the regular source pin of the MOSFETs. While the regular source pin is connected to the power loop of the circuit, kelvin source pin is used to provide gate-source turn-on voltage. Kelvin pin is connected to MOSFET die so that the gate loop is minimized with minimum inductance. Hence, MOSFETs with a kelvin source connection can turn on and off faster than MOSFETs that are switched by a regular source connection [44]. So, MOSFETs with kelvin source connection have fewer switching losses and are selected for the design of the converter.

In order to select the optimal semiconductor for the given conditions, a semiconductor device database was constructed. The semiconductors were first filtered based on the voltage and current ratings. The additional checked parameters of the MOSFETs are R_{DS} and E_{OSS} . E_{OSS} is defined as the stored energy in the output capacitance (C_{OSS}) of a MOSFET. Choosing a low R_{DS} MOSFET decreases the conduction losses. Whereas low E_{OSS} generally results in lower switching losses [13]. MOSFETs made up of large semiconductor areas provide low R_{DS} ; however, capacitances become larger, and switching performance worsens. Consequently, there is a trade-off between switching losses and conduction losses. In Fig. 3.7, the R_{DS} - E_{OSS} values of selected SiC MOSFETs are presented. It is shown that lower R_{DS} results in higher E_{OSS} .

Fig. 3.7 shows the preliminary result for MOSFET selection. However, the dominant loss of the converter is not clear and depends on the switching frequency. Hence, the loss analysis was performed for the MOSFETs in the dataset. Conduction loss and switching loss of the MOSFETs are calculated by (3.7) and (3.8), respectively. For calculation of switching loss, turn-on energy (E_{On}) and turn-off energy (E_{Off}) are used which are functions of drain-source voltage (V_{DS}), drain-source current (I_{DS}), gate voltage (V_{GS}), gate resistance (R_G) and junction temperature (T_j). Data-sheet parameters are tabulated, and a look-up table is generated to obtain loss at required conditions.

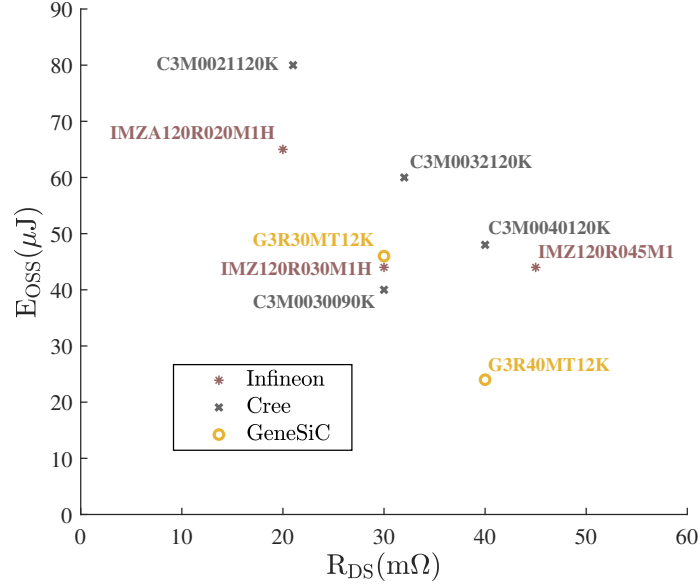


Figure 3.7: R_{DS} and E_{OSS} values of MOSFETs in design database

$$P_{cond,MOSFET} = R_{DS(ON)} I_{DS,rms}^2 \quad (3.7)$$

$$P_{sw,MOSFET} = (E_{On} + E_{Off}) f_{sw} \quad (3.8)$$

For the rated power conditions, conducting interval of the MOSFET increases when the input voltage decreases. This condition also results in maximum input current. Hence MOSFET losses are maximum. In Fig. 3.8, the loss of each MOSFET option is presented for the maximum MOSFET loss condition. The switching frequency is swept from 10 kHz to 120 kHz. As frequency increases, MOSFET losses increase as expected. According to the results, G3R40MT12K, C3M0030090K, and G3R30MT12K are the most suitable options. Among them, G3R40MT12K [45] is the cheapest one and it is selected for the converter design.

The same loss analysis was performed for SiC diode selection. The conduction loss of the diode is calculated as (3.9) where V_f and I_f are forward voltage drop and forward current. Since there is no reverse recovery current in the SiC Schottky diode, the switching loss of it is almost zero. Hence only the conduction loss is considered. The losses of the diode options do not show a significant variation. Hence, the cheapest

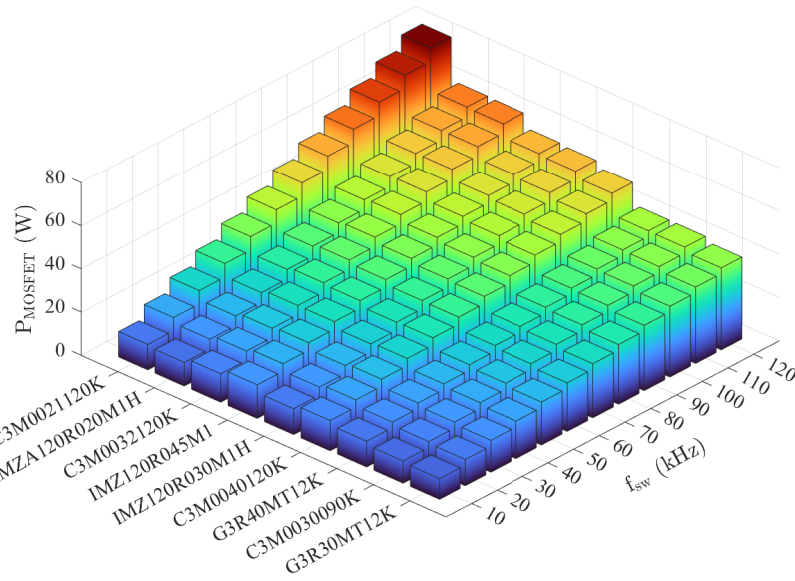


Figure 3.8: Comparison of the loss of MOSFETs for different switching frequencies

IDWD30G120C5 [46] diode is selected to be used in the design. The images of selected devices are presented in Fig. 3.9, and the important device parameters are given in Table 3.2.

$$P_{con, DIODE} = \frac{1}{T_s} \int_0^{T_s} V_f(t) I_f(t) dt \quad (3.9)$$



(a) G3R40MT12K



(b) IDWD30G120C5

Figure 3.9: Images of selected semiconductor devices

The total loss of the selected semiconductor devices is given in Fig. 3.10 for minimum and nominal voltage conditions. As previously explained, maximum MOSFET loss arises at minimum V_{in} case. Diode losses, however, show a small variation since the diode conduction period decreases when the input voltage is at the minimum.

Table 3.2: Parameters of the selected semiconductor devices at 25°C

Part Number	G3R40MT12K	Part Number	IDWD30G120C5
Package	TO-247-4	Package	TO-247-2
$V_{DS(max)}$	1200 V	$V_{r(max)}$	1200 V
I_{DS}	28 A	$I_{f(max)}$	40 A
R_{DS}	40 mΩ	$V_f (I_f = 30 \text{ A})$	1.7 V
$V_{GS(ON)}$	+15 V to +18 V		
$V_{GS(OFF)}$	-5 V to -3 V		

Therefore, the minimum input voltage condition is the limiting factor in designing the converter. By analyzing the losses of semiconductor devices, it is reasonable to choose the switching frequency of 80 kHz. At this frequency, semiconductor losses are half of the allowed loss budget. The other half could have resulted from other losses, such as inductor losses, input filter losses, and other losses that are inevitable in the implementation stage.

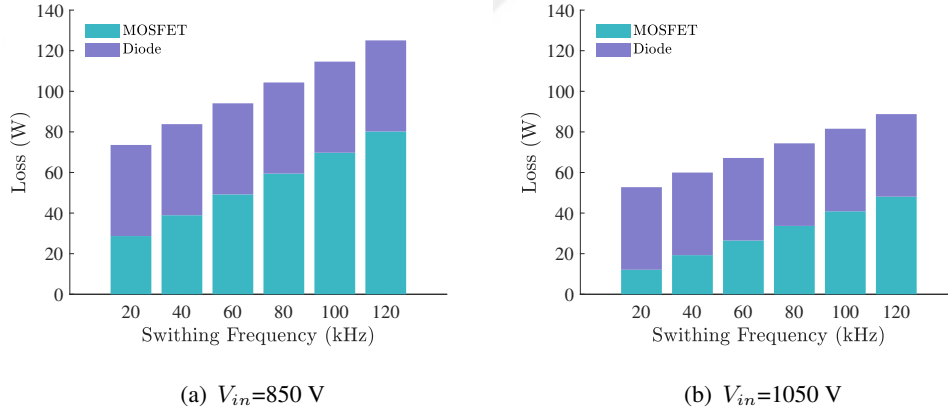


Figure 3.10: Loss analysis of the selected semiconductor devices

3.4 Inductor Design

Another important design point is the inductor of the converter. The three main criteria of the inductor design are mean current, ripple current and ripple frequency, which

are all related to inductor losses. It is also desired to design the inductor at a minimum size and cost. Choosing out-of-phase switching scheme helps to achieve this design goal as the ripple frequency is doubled to 160 kHz, allowing a lower inductance in the circuit.

Losses of an inductor can be analyzed in two parts. Copper loss (P_{cu}) that are produced due to the equivalent resistance of the winding, and core loss (P_{core}) which is generated due to hysteresis characteristic of magnetic materials and eddy currents induced in the core material. Copper loss is found by (3.10) where R_{eqv} is the equivalent winding resistance and $I_{L(RMS)}$ is the RMS of the inductor current. To find the core loss of the inductor, (3.11) can be used, which is well known as the "Steinmetz Equation" [47]. The parameters a , b , and c are material depended and supplied by the core manufacturer.

$$P_{cu} = R_{eqv} I_{L(RMS)}^2 \quad (3.10)$$

$$P_{core} = a f^b \Delta B^c \quad (3.11)$$

As given in (3.11), the loss of the inductor increases with the flux density change (ΔB) in the core material. Hence high current ripple results in more core loss. The current ripple of the three-level boost converter is calculated by (3.6) for out-of-phase switching. Increasing the inductance, the current ripple is decreased, and core loss is reduced. However, inductance increase is ensured by a higher number of turns, which results in higher R_{eqv} and higher copper losses. Thus, an optimal point can be found in the design of the inductor.

Designing the inductor requires the core material and core type selection. There are different core materials used for manufacturing an inductor. Ferrite provides low loss at high-frequency applications. However, the saturation flux density is low and requires an additional air gap. When the saturation point is exceeded, inductance decreases sharply, which may result in damaging the components. Another disadvantage of ferrite is the low operating temperature capability. Ferrite saturation flux density is highly dependent on the temperature; hence high-temperature operation is

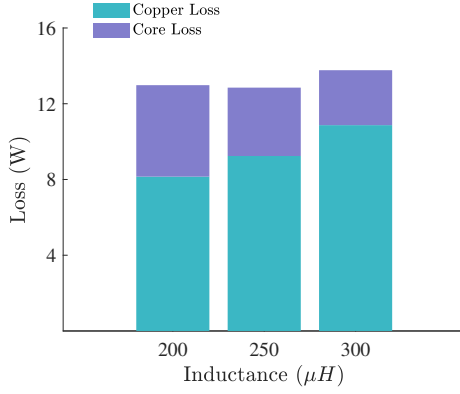
not feasible with ferrite core inductors. Iron powder is another magnetic core material that is produced by placing iron dust in epoxy. It enables high saturation flux density, and temperature dependency is low. However, iron particles placed in the core cause high eddy current losses, which prevents them from being used in high-frequency applications due to higher losses. Another powder core material is sendust [48]. It provides lower core losses compared to iron powder and can be used in high frequencies. Compared to ferrite, higher temperature operation is allowed. Its high saturation flux density and soft saturation behavior allow it to have a reasonable inductance in faulty conditions. For a short-circuit scenario, inductance does not drop out sharply, which provides time to take action. Additionally, as stated in [49], size reduction can be achieved with the distributed air-gap core materials. Considering all, sendust-based magnetic cores are selected to be used in the design. Kool M μ is a sendust core produced by Magnetics Inc and has different shapes and sizes of magnetic cores. Similar to MOSFET selection, a core database was constructed with the available Kool M μ cores, and different designs were compared. The loss analysis of the two most suitable cores is given in Fig. 3.11. The loss analysis was performed in the maximum current scenario, which causes the maximum inductor losses. In the design process, the current density was chosen as 3.4 A/mm², and the copper losses were calculated for the copper temperature of 70°C. Analysis shows that as the inductance increases, core loss decreases thanks to a lower current ripple. However, copper loss increases, as stated before, due to longer wire usage. Based on this analysis, 250 μ H inductance is reasonable for both of the core options. The design parameters of the inductors are given in Table 3.3. The first option is narrower in width and longer in length. Eventually, the fill factor of the first inductor is higher. If additional turns are required due to mismatches in analytical design, it is difficult to place wires in the first toroid, whereas the second one has enough empty space. Therefore, second option will be evaluated and will be investigated in the prototype design.

3.5 Capacitor Selection

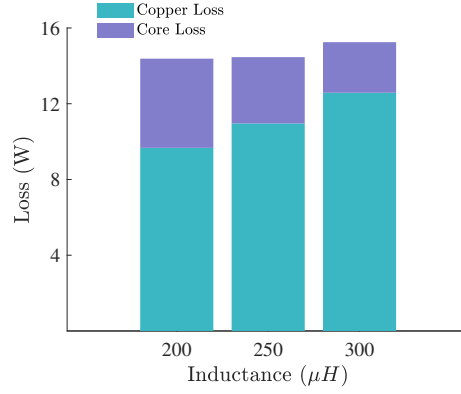
The last stage of the converter design is the output capacitor selection. Different types of capacitors can be used for DC-link applications. In [50], aluminum electrolytic ca-

Table 3.3: Design parameters of boost inductor

Core Part Number	0077776A7	0077100A7
Relative Permeability	40	40
Shape	toroid	toroid
Outer diameter	78 mm	103 mm
Inner diameter	38 mm	56 mm
Height	27 mm	18 mm
Number of turns	51	68
Fill factor	32 %	20 %
Unbiased inductance	351 μH	342 μH
Inductance at $I_L = 23.8 \text{ A}$	250 μH	250 μH



(a) 0077776A7 Kool Mμ-40 Toroid Core



(b) 0077100A7 Kool Mμ-40 Toroid Core

Figure 3.11: Loss Analysis for possible inductor designs ($V_{in} = 850 \text{ V}$, $I_{in} = 23.8 \text{ A}$, $V_o = 1300 \text{ V}$, $f_{sw} = 80 \text{ kHz}$, out-of-phase switching scheme)

pacitors, metalized polypropylene film capacitors, and multi-layer ceramic capacitors are compared in terms of different aspects. It is concluded that metalized polypropylene film capacitors are the most reliable option for high-voltage applications while providing low ESR and a wide operation frequency range. Yet, the highest allowed temperature is not as good as multi-layer ceramic capacitors. It should be paid attention to the allowable temperature rise in the design stage.

Minimizing the output voltage ripple is important for the stable control of the boost

converter and the inverter stage. DC-link voltage fluctuations increase the harmonic content of the output hence reducing the performance. Thus, voltage ripple should be within the desired limited range. The output voltage ripple of the three-level boost converter is found by (3.12), which is independent of the switching strategy.

$$\Delta V_o = \frac{DI_o}{f_{sw}C_{out}} \quad (3.12)$$

Limiting the capacitor voltage ripple to 1 % of the average voltage, 10 μ F capacitance is required at the output. However, another vital criterion while choosing the capacitor is the ripple current. Due to the internal resistance of the capacitors, ripple current results in power loss and heating, which indeed reduces the lifetime. Hence, it should be within the safe range of the selected product. The RMS of each output capacitor current can be expressed as (3.13). As shown in Fig. 3.3, Fig. 3.4, and Fig. 3.5, high-side and low-side capacitor currents are ideally identical. Depending on the I_L , RMS values slightly change due to changes in switching strategy, but the calculation method is valid for all cases.

$$I_{c,RMS} = \sqrt{\frac{1}{T_s} \left(\int_0^{dT_s} (-I_o(t))^2 dt + \int_{dT_s}^{T_s} (I_L(t) - I_o(t))^2 dt \right)} \quad (3.13)$$

When the available capacitors are searched in the market, it is seen that choosing a capacitor just providing the desired voltage ripple may result in unsuitable products in terms of the current RMS. Therefore, higher valued capacitance might be required. Consequently, in the design of this converter, 18 μ F metalized polypropylene film capacitor (C4AQUBW5180A3OJ [51]) was selected to provide the required current level.

3.6 Common Mode Leakage Current Analysis

In PV applications, a common mode (CM) leakage current problem arises due to parasitic capacitances between PV panels and the physical ground. Additionally, the capacitance between the semiconductors and heatsink provides a path to CM currents

and may increase the leakage current. Hence, CM circuit analysis is important while designing the converters. For the common mode analysis of the converter, a similar approach as presented in [52] is performed. Switching nodes of the converter are shown in Fig. 3.12.a and numerated. These node voltages are analyzed referenced to the input ground point. Also, the effect of the position of the boost inductor is analyzed and compared at the end.

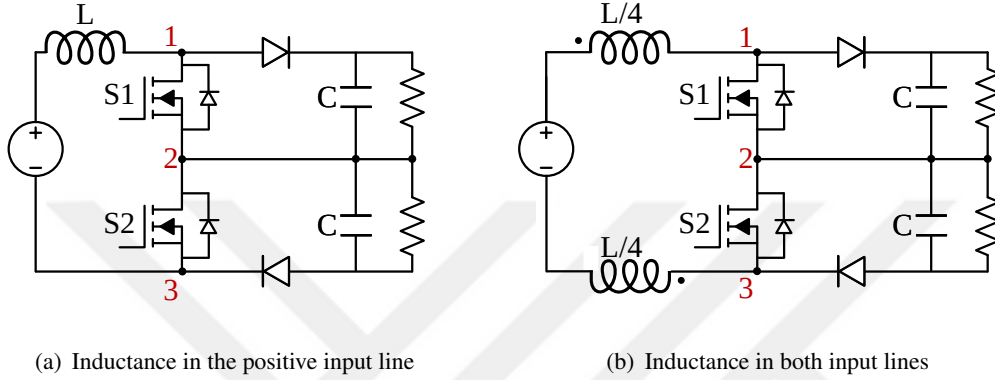
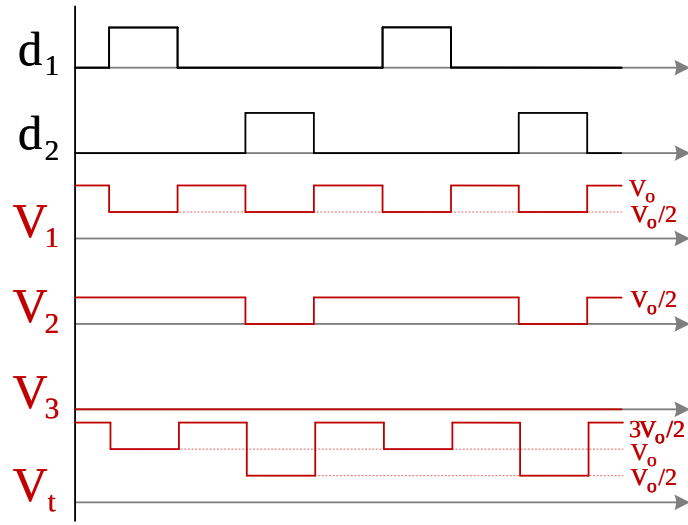


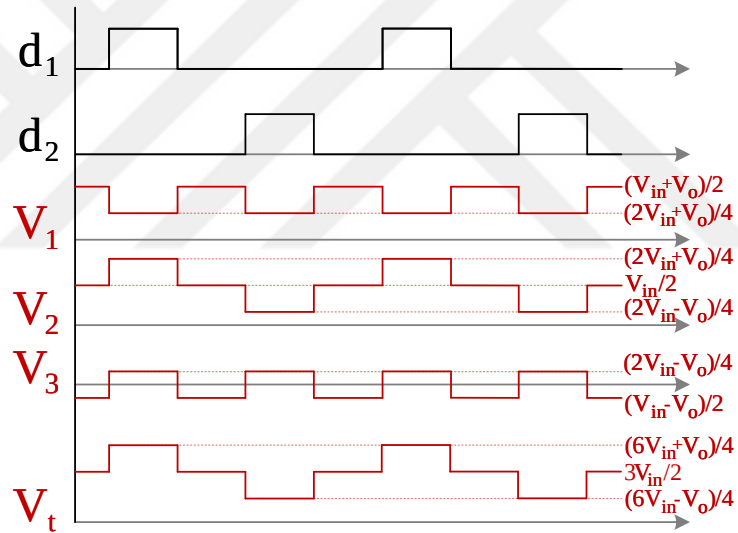
Figure 3.12: Switching nodes of 3L-BC for CM leakage current analysis

3.6.1 Out-of-phase Switching & Inductor on the Positive Line

The switching timings and the node voltages are plotted in Fig. 3.13.a for the out-of-phase switching technique. The inductor is placed on the positive input line as a conventional boost converter. The neutral line is directly connected to node-3. Node-2 switches between $V_o/2$ and ground depending on the conduction status of S_2 . The voltage of node-1 is depended on both S_1 and S_2 . If one of the switches is conducting, node-1 voltage is set to $V_o/2$. Otherwise, it is equal to V_o . The sum of three node voltages (V_t) is also given in the last plot. It is shown that the sum of node voltages changes between $3V_o/2$, V_o and $V_o/2$. Hence, pulsating CM voltage is generated.



(a) Inductance in the positive input line



(b) Inductance in both input lines

Figure 3.13: CM analysis for out-of-phase switching scheme

3.6.2 Out-of-phase Switching & Inductor on the Positive and Neutral Line

In [52, 53], it is shown that dividing the input inductance into two separate windings and connecting to both of the input ports eliminates the CM leakage for a conventional boost converter. The same method is analyzed for the 3L-BC in this part. The circuit

diagram of this configuration is given in Fig. 3.12.b with numerated nodes. In the circuit diagram, the self-inductance of each inductor is $L/4$, and total inductance results in L due to the addition of mutual inductance if the windings are placed on the same core. As shown in Fig. 3.13.b, dividing the inductor results in more balanced voltage generation at the nodes. However, the sum of node voltages is not constant, and it oscillates around $3V_{in}/2$ with an amount of $V_o/4$, which results in nonzero common mode voltage and leakage current. It is seen that connecting the inductor in both of the input lines does not eliminate the CM voltage for 3L-BC. However, since the amplitude of oscillation is decreased, it is expected to have a lower CM current with this condition.

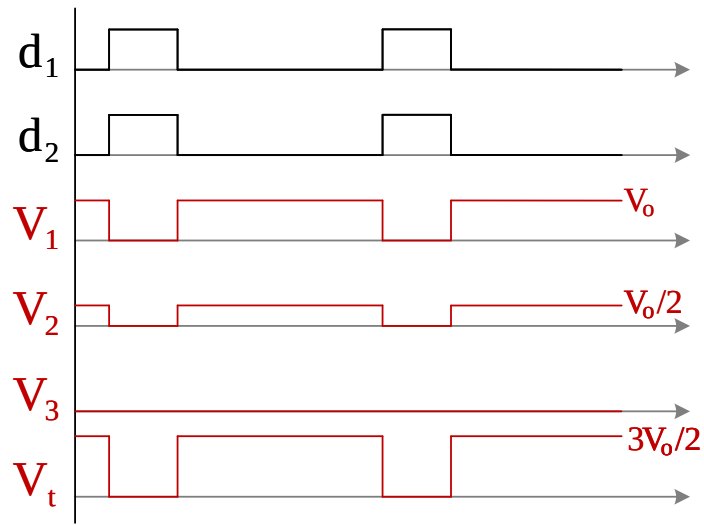
3.6.3 In-phase Switching & Inductor on the Positive Line

It is shown that CM voltage cannot be prevented using out-of-phase switching scheme. In this section, the same analysis is also performed for the in-phase switching technique. The node voltages and their summation is given in Fig. 3.14. This time, node-2 and node-3 voltages are changing simultaneously, where node-3 is directly connected to the ground. V_t is not constant, and CM voltage is generated.

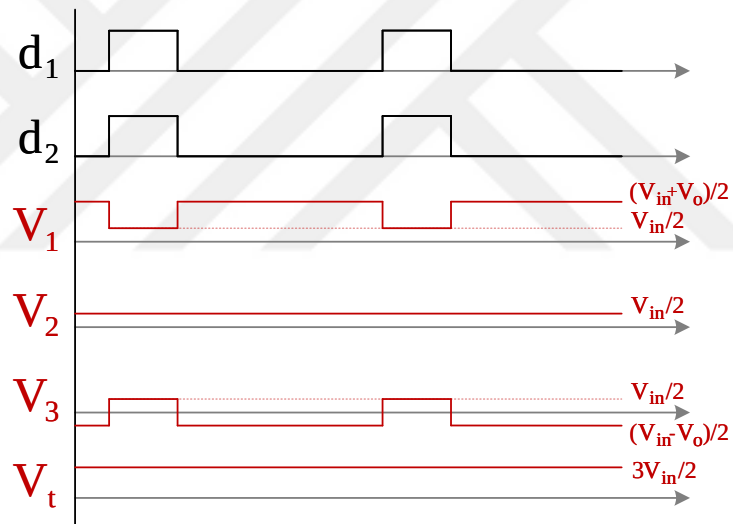
3.6.4 In-phase Switching & Inductor on the Positive and Neutral Line

The last analysis examines connecting the inductor into two lines for in-phase switching. The circuit schematic is given in Fig. 3.12.b. The node voltages are given in Fig. 3.14.b with their summation. Since the sum of the node voltages is constant, the CM leakage current due to switching is eliminated, similar to cases in [52] and [53].

These results show that CM current can be minimized by utilizing in-phase switching and inductors in both of the input lines. However, as shown in the operation principles section, out-of-phase switching performs much better in terms of inductor current ripple. Minimizing the inductor current ripple and hence the loss is important to design a high-efficiency converter. If the same designed inductors are used with in-phase switching scheme, the losses will be higher. The loss analysis with the increased inductor current ripple is given in Fig. 3.15. As expected, losses are almost



(a) Inductance in the positive input line



(b) Inductance in both input lines

Figure 3.14: CM analysis for in-phase switching scheme

doubled compared to out-of-phase switching. Yet, the total loss of the inductor and semiconductors is around 135 W, which is in the acceptable region in terms of loss budget.

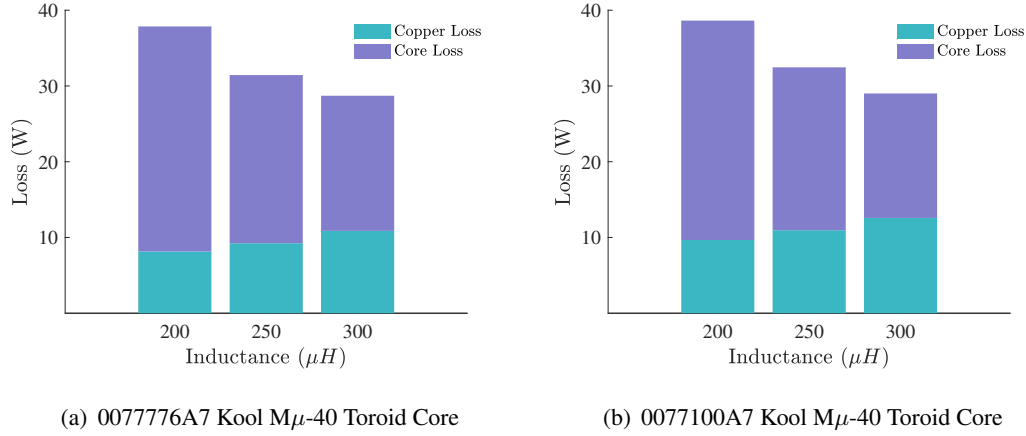


Figure 3.15: Inductor loss analysis for in-phase switching scheme

3.7 Thermal Design

The semiconductor device selection and the worst-case loss analysis were performed in the previous sections. The total losses of the semiconductor devices become 104 W at the maximum current operation. Hence a cooling system is required to safely operate the converter. Lumped circuit analysis is used to build a cooling system, as shown in Fig. 3.16. MOSFET losses (P_{S1} , P_{S2}) and diode losses (P_{D1} , P_{D2}) are modelled as current sources. The thermal resistance between the device junction and case ($R_{th,J-C}$) is given by the manufacturers. The thermal pad resistance ($R_{th,C-HS}$) and the heatsink to ambient resistance ($R_{th,HS-A}$) were selected so that junction temperature is lower than 150°C. The selected thermal pad is appropriate for 1500 V applications.

The maximum loss values and the thermal resistances of the devices are given in Table 3.4. Using only a heatsink could not provide low thermal resistance, so a cooling fan was established. At the maximum loss point, the junction temperature of the MOSFET is calculated as (3.14). The designed structure is capable of handling the heat generated at the ambient temperature of 25°C.

$$T_j = (30W)(0.66^{\circ}C/W + 1.2^{\circ}C/W) + (104W)(0.4^{\circ}C/W) + (25^{\circ}C) = 122.4^{\circ}C \quad (3.14)$$

Table 3.4: Losses and the thermal resistances of the components

Parameter	Value
$P_{S1} = P_{S2}$	30 W
$P_{D1} = P_{D2}$	22 W
$R_{th,J-C(MOSFET)}$	$0.66^{\circ}C/W$
$R_{th,J-C(Diode)}$	$0.5^{\circ}C/W$
$R_{th,C-HS}$	$1.2^{\circ}C/W$
$R_{th,HS-A}$ without fan	$4^{\circ}C/W$
$R_{th,HS-A}$ with fan	$1.6^{\circ}C/W$

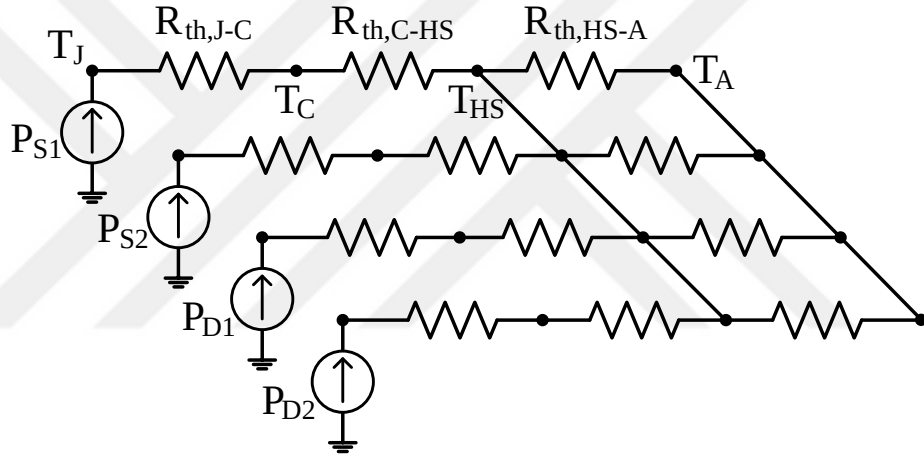


Figure 3.16: Lumped circuit model for thermal analysis

3.8 Controller Design

In the previous sections, the operation principle of the 3L-BC was investigated, and critical component selections were discussed. Further analysis of the control of the converter will be examined in this part. Control of the converter can be detailed in two sections. The first one is PV string voltage control which is important to operate at the maximum power point of the PV string. The second one is the capacitor voltage balance which is required to equally load the capacitors. It must be noted that the

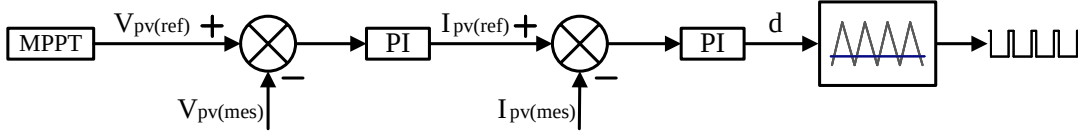


Figure 3.17: PV string voltage control block diagram

control algorithms discussed here are independent of the switching scheme and can be used for both techniques.

3.8.1 PV String Voltage Control

The main structure of the MPPT via the P&O algorithm was explained in Chapter 2. In Fig. 3.17, the block diagram of the string voltage control is shown. First, the MPPT block decides on the PV string voltage. Then, voltage error passes from the PI controller and results in the current reference for the converter input. The current error is used in the second control loop. The output of this loop is the duty cycle value to drive the MOSTEFs. It is compared with the triangular waves and converted to gate drive signals. These cascaded voltage and current control loops settle the PV string voltage based on the reference value coming from the MPPT algorithm while also controlling the PV current.

3.8.2 Output Voltage Balance

As shortly discussed in the operation principles of the converter part, normally, output capacitors equally share the output voltage. However, due to manufacturing tolerances, capacitances may be slightly different. Additionally, unequal conditions occur throughout the implementation, like minor differences in the gate drive paths. Moreover, uneven loads might be drawn as the center point of the output capacitors is connected to the neutral point of the three-level inverter. All in all, output capacitors may not share the voltage equally. In order to equalize the capacitor voltages, two different methods can be performed. The first one is the adjustable phase shift

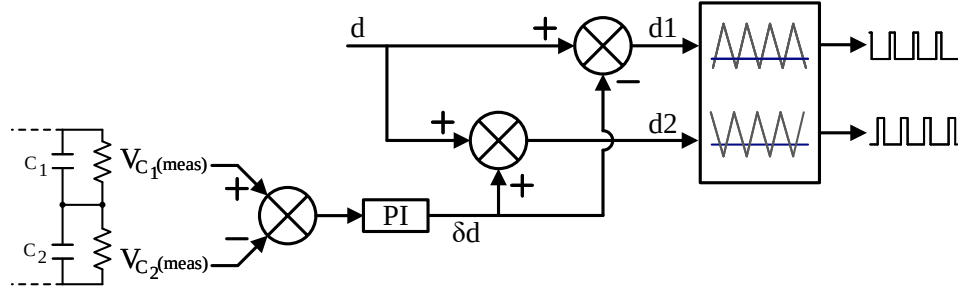


Figure 3.18: Block diagram of output voltage balance controller

between the MOSFET turn-on signals. For this method, instead of 180° phase shift, variable phase shift is applied [54]. Although it is suitable for small voltage differences, the capability of equalizing the voltages is limited. The second method is the unequal duty cycle for switches [34]. If the voltage of the high-side capacitor is lower than the low-side, increasing the high-side duty cycle increases the high-side voltage. Higher levels of voltage differences can be equalized with this approach. For the implementation of this method, the block diagram in Fig. 3.18 is used. The duty cycle command from the panel voltage controller defines the main input-output voltage ratio. The voltage difference of the capacitors is processed by a PI block. The output of the voltage balance controller, δd , is added to or subtracted from the original duty cycle. Required different duty values are found, and respective turn-on signals are generated via triangular wave comparators.

3.9 Conclusion

In this section, 3L-BC topology is analytically investigated with the help of circuit waveforms. The out-of-phase switching technique was shown to be superior to reducing inductor current ripple. Based on the analytical derivations and converter requirements, the operation conditions of the 3L-BC were decided. Then, the selection of semiconductor devices was explained by loss comparison of available devices. For the selected frequency, inductor design and loss analysis was accomplished. The common mode voltage generation was analyzed for different inductor placements and switching techniques. For the calculated losses of semiconductors, thermal analysis

was performed. The selected cooling equipment is able to keep the semiconductor within a safe operating region. Finally, the control algorithms of the converter are explained. All in all, analytical results show successful operation for the designed converter. In the next chapter, experimental verification will be performed, and the measurements will be compared with the analytical calculations.



CHAPTER 4

IMPLEMENTATION AND EXPERIMENTAL VERIFICATION OF THE THREE-LEVEL BOOST CONVERTER

Operational analysis of the 3L-BC was discussed in Chapter 3. In this chapter, firstly, the implementation of the converter will be presented. The considerations for gate driver and printed circuit board designs will be evaluated. Then, several experiments will be investigated to validate the manufactured converter's operation. The inductor parameters were measured, and the current waveform of the inductor was observed. Afterward, CM leakage current was analyzed for different inductor connection options and switching techniques. Then, the rated voltage experiments were conducted. MOSFET and diode voltage waveforms were monitored. The loss measurements were gathered, and thermal performance was investigated with a thermal camera. Finally, the control algorithm was tested for MPPT operation and output capacitor voltage balancing.

4.1 Hardware Design Considerations

In order to verify the operation of the converter, hardware implementation is required. Hence a single-module converter was designed. There are different considerations for the hardware design. These issues will be discussed in the following parts: SiC MOSFET gate driver design and PCB layout design.

4.1.1 SiC MOSFET Gate Driver Design

In order to turn on the MOSFETs, the turn-on signal should be amplified, and gate-source capacitance needs to be charged. Next, it needs to be discharged at the turn-off transition. For fast transition, highly impulsive currents are required. Specialized gate drivers are used to handle these requirements. The basic structure of a gate drive system is given in Fig. 4.1.

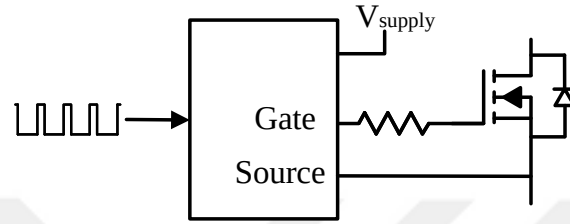


Figure 4.1: Basic gate drive circuitry

Designing the gate drive circuitry comes up with some challenges. First, the gate-drive path inductance should be as small as possible to minimize the oscillations on the gate-source voltage. This challenge is not unique to SiC MOSFETs. However, it might be more vital with the SiC MOSFETs as the switching is faster. To minimize the path inductance, the gate current loop must be minimized. In addition to minimizing path inductance, in [55], it is recommended to add ferrite beads to drive circuits in order to reduce high-frequency noise and ringing.

The other challenge of the drive system is source terminal referenced gate voltage generation. Gate drive integrated circuits are capable of supplying impulsive current. However, the top side switch gate voltage should be referenced to the top side source pin. This can be obtained using bootstrap circuits. However, using isolated supplies and isolating the drive circuitry from the signal paths is much safer for both top and bottom-side MOSFETs.

The last challenge is the false turn-on possibility of the MOSFETs. In a leg configuration of SiC MOSFETs, like in 3L-BC, turning on the top side switch creates a high dV/dt on the drain terminal of the bottom side switch. The miller capacitance (C_{DG}) of the bottom side switch can be charged by the so-called displacement current

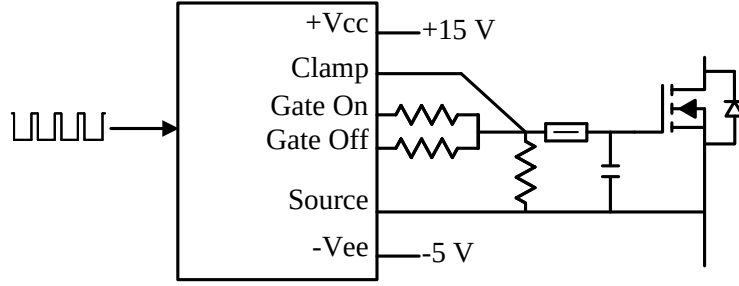


Figure 4.2: Designed gate drive circuitry

resulting from high dV/dt , which eventually may turn on the bottom switch. This is also known as cross-talk, and precautions should be taken as the threshold voltage of SiC MOSFETs is low. Implementing an external gate-source capacitance helps to overcome the problem. However, it increases the switching losses by slowing down the switching process. The other solution is the negative turn-off voltage. Keeping the V_{GS} voltage away from the threshold voltage, false turn-on probability decreases. The last solution is using a driver with Miller clamp capability. When the gate-source voltage decreases beyond a specific level, high current sinking circuitry clamps V_{GS} to the turn-off level via direct connection to the gate terminal. Based on these challenges, the designed gate-drive circuitry is given in Fig. 4.2. All the methods are implemented in the circuitry to safely turn on and off the MOSFETs.

4.1.2 PCB Layout Design

For the hardware implementation of the converter, a PCB design is required. Designed and assembled PCB is shown in 4.3. The width of the PCB is 26 cm, and the length is 30 cm. The detailed PCB design is not the subject of this thesis. The main points that were followed in the design process are given as follows.

- A common mode filter was utilized at the input side of the converter due to CM voltage generated by out-of-phase switching.
- The spacings between the power paths were arranged so that voltage differences do not cause a dielectric breakdown. Minimum spacing values given by the

IPC-2221B standard were obeyed.

- In order to keep path resistances small while maintaining the spacing rules, a 4-layer PCB design was realized.
- Semiconductors were placed as close as possible to minimize the power loop inductance.
- The output capacitance should be placed close to the semiconductors to minimize the layout inductance. In order to minimize the power loop and provide a path to high-frequency harmonics, additional power loop capacitance was added to the circuit.
- Gate drive circuitry was placed as close as possible to the switches.
- Voltage and current measurement circuits were added to the PCB design to accomplish capacitor voltage balancing and MPPT algorithms.
- The overall PCB size is not critical since the board is used for prototype testing. Hence, test points were added wherever possible.
- TI F28379D evaluation board was employed to generate PWM signals based on the control algorithms.
- In addition to PV input, additional 12 V input was used to provide power for integrated circuits, controller, and cooling fan. The other voltage levels were produced by 12 V input.

4.2 Inductor Verification Experiments

The design with 0077100A7 toroid core was first manufactured, and the parameters were measured with GW Instek 101G LCR-meter. In the absence of DC bias, the inductance is $344\ \mu\text{H}$. The DC resistance of the winding was measured as $20\ \text{m}\Omega$ at 25°C . The measurement results are highly matching with the designed values. Then, the converter was tested with a 200 V input voltage to verify the operation. The inductor current waveform was obtained during the tests, which is shown in Fig. 4.4.a. The current waveform is different from the expected regular waveform. The reason

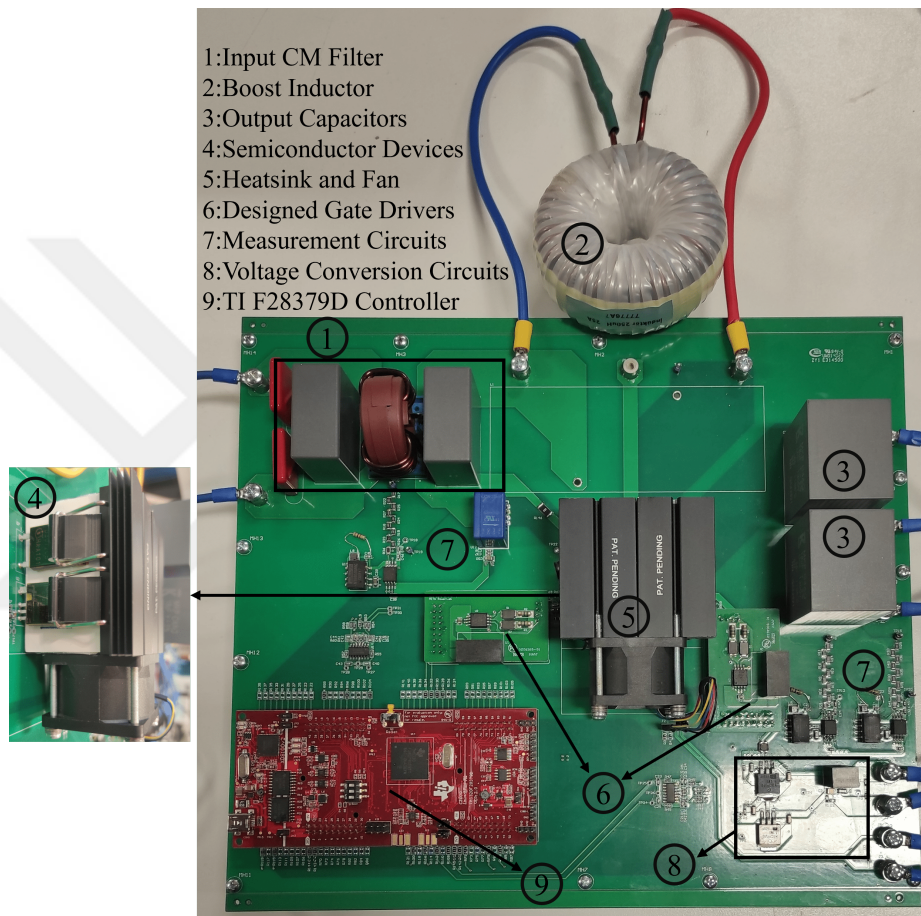


Figure 4.3: 3L-BC prototype PCB design

for having this kind of current was considered to be the capacitance between the windings [56]. The equivalent circuit diagram of this phenomenon is given in Fig. 4.5. The inductor used in the experiment is shown in Fig. 4.6.a. The toroid core was wound with enameled wire by a winding machine. Due to the thin insulating coating, a capacitance exists between the adjacent windings, which results in the waveform given due to resonance. To overcome this problem, the same core was wound by hand using a wire with thick insulating material as shown in Fig. 4.6.b. The same test was conducted using the new inductor, and the resulting current waveform is given in Fig. 4.4.b.

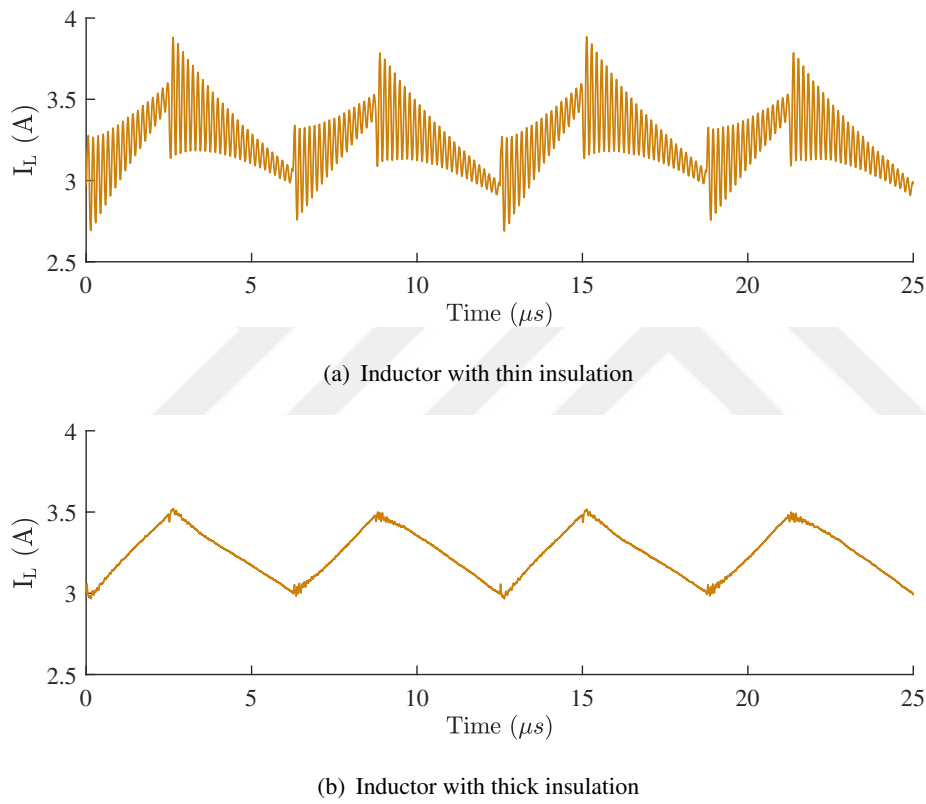


Figure 4.4: Effect of interwinding capacitance on the inductor current

The LCR-meter measurement results of the inductors are presented in Table 4.1. The first manufactured inductor is formed by a designed copper area of 7 mm². However, the second one has a copper area of 4 mm². The wire cross-sectional area, including the insulator thickness, is 12 mm². Due to wider winding, the number of turns is increased to 72 in order to reach the same inductance. Using thicker insulated wire reduced the resonance current, as shown in the waveforms. However, since the cop-

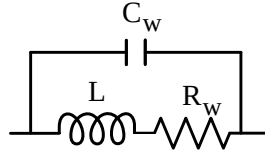


Figure 4.5: Equivalent circuit diagram of a real inductor



(a) Inductor with thin insulation



(b) Inductor with thick insulation

Figure 4.6: Inductors used in the experiment

per area is reduced and the copper length is increased, the resistance of the second inductor doubles the first one. The total copper loss will be higher than the designed loss value. The detailed analysis will be given in the loss measurement section.

Table 4.1: LCR-meter measurement results of inductors

	Inductor with thin insulation	Inductor with thick insulation
Number of turns	68	72
L (no DC bias)	344 μH	340 μH
DCR (25°C)	20 m Ω	40 m Ω

To verify the soft saturation behavior of the inductor, $V_{in} = 850$ V and $V_{out} = 1300$ V operation is analyzed for both in-phase and out-of-phase switching techniques. The input current is set to 21.2 A due to the power rating of the supply. Fig. 4.7 gives the resultant current waveforms. The expected current ripple and measured current ripple values are presented in Table 4.2. The expectations are nearly the same as the measurements. The design by data-sheet parameters provides successful results.

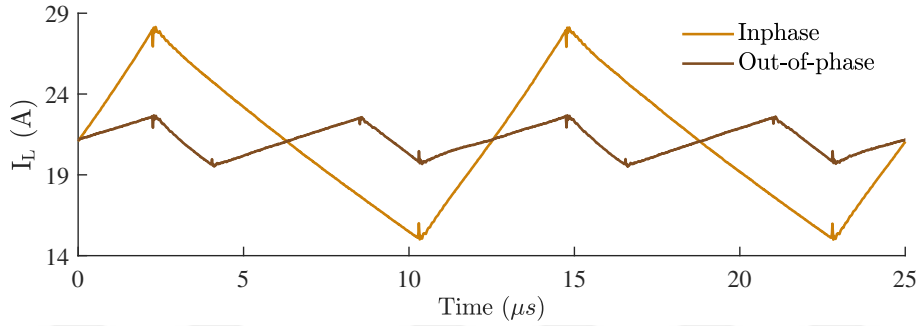


Figure 4.7: Inductor current ripple analysis under 21.2 A DC bias

Table 4.2: Inductor current ripple analysis under DC bias ($I_{L(avg)} = 21.2$ A, $V_{in} = 850$ V, $V_o = 1300$ V)

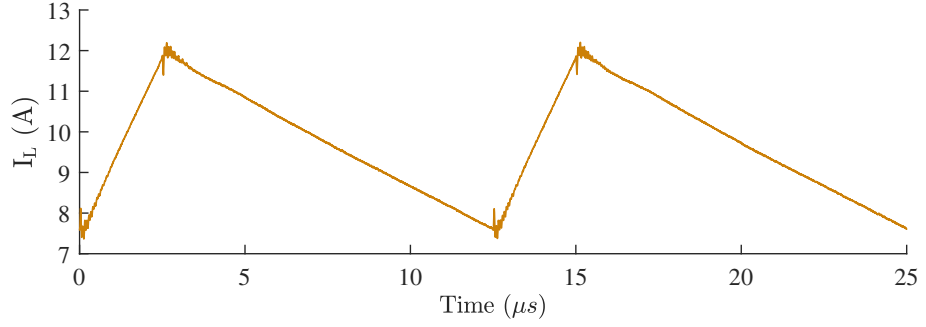
Case	Expected current ripple	Measured current ripple
In-phase switching	13.3 A	13 A
Out-of-phase switching	3.1 A	2.9 A

4.3 Common Mode Current Experiments

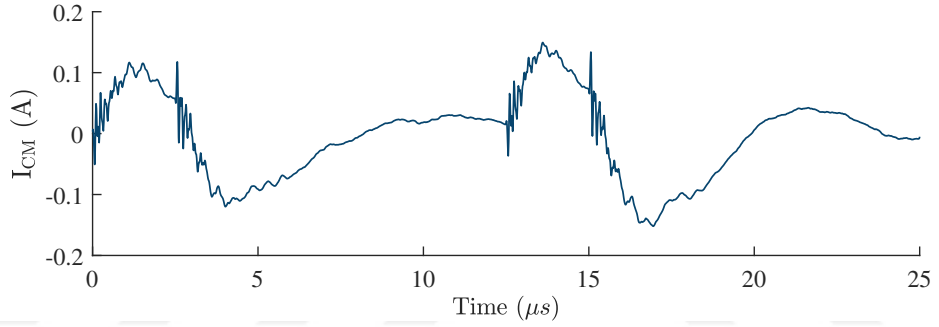
The effect of the position of the boost inductor was analyzed for CM leakage currents in Section 3.6. Additionally, the switching scheme was investigated. In this section, those analyzes were studied by a series of experiments.

The first scenario is in-phase switching with the inductor placed on the positive PV input line. In Fig. 4.8, inductor current and common mode current measurements are shown with MOSFET voltage waveforms. The CM current was measured by placing both input wires in the current probe. The experiment was conducted with 600 V input voltage and a switching frequency of 80 kHz. The duty cycles of the switches

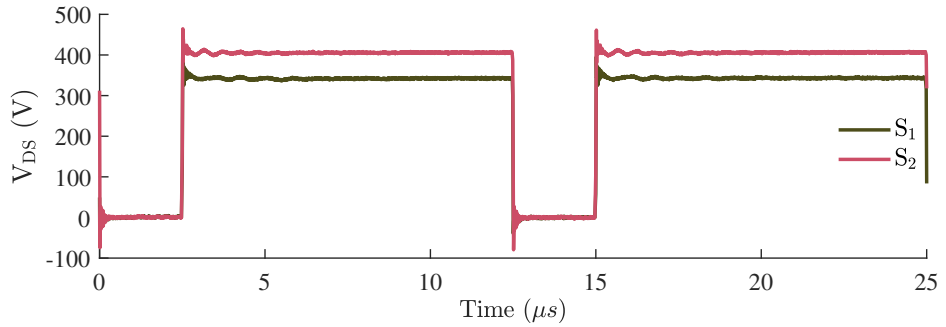
are identical and set to 0.2. As shown in the figure, the dominant harmonic is at switching frequency of 80 kHz. Additionally, there are high-frequency harmonics in common mode current at turn on and turn off instants. In total, the RMS of the CM current is measured as 71 mA.



(a) Inductor current



(b) Common mode leakage current



(c) MOSFET voltages

Figure 4.8: CM leakage investigation with in-phase switching scheme. The inductor is placed in the positive input line.

In the second scenario, the input inductor's position was changed as shown in Fig. 3.12. Half of the windings were placed in the positive input line, and the other half was

placed in the neutral line. The remaining test conditions were kept constant. The result of this case is given in Fig. 4.9. The inductor current is nearly the same as the previous case. The oscillations at the switching instants are much less than in the first scenario. The common mode current is also reduced significantly. The switching frequency harmonic is almost diminished. The magnitudes of the high-frequency harmonics are also decreased. The measured RMS of CM current is 19 mA. The improvement of connecting inductance to both of the inputs is clearly visible.

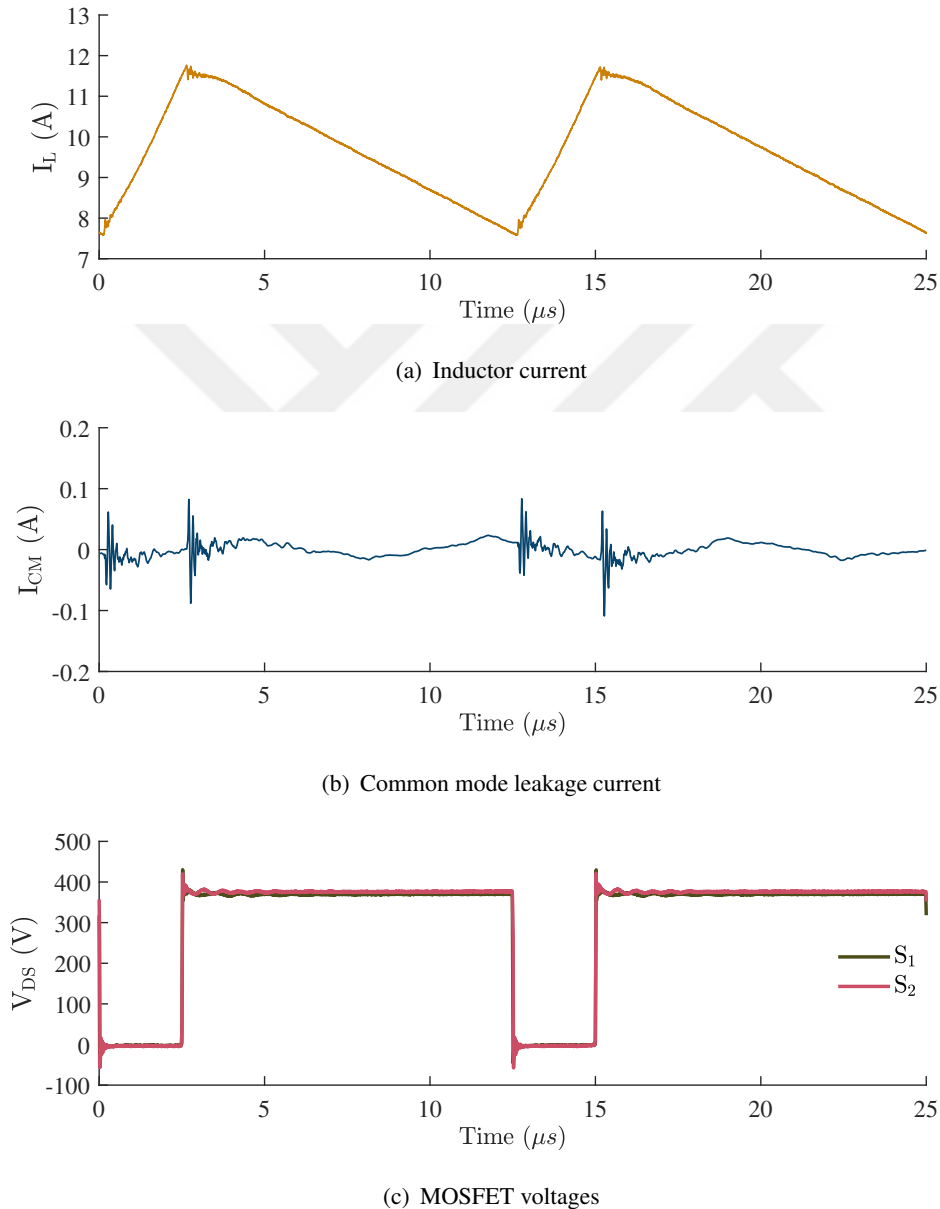


Figure 4.9: CM leakage investigation with in-phase switching scheme. The inductor is placed in both of the input lines.

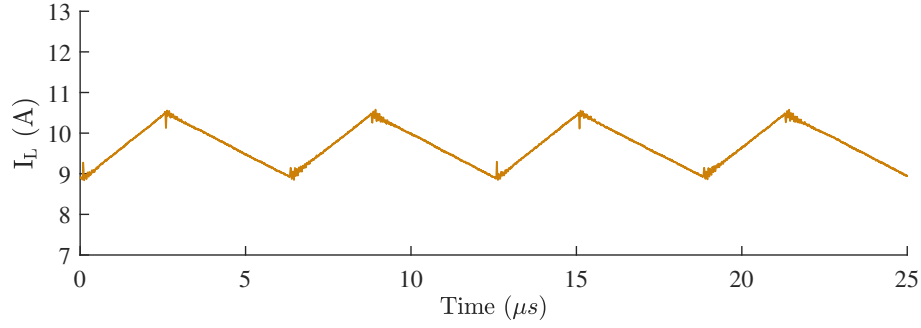
Then the switching scheme was changed so that the phase shift between the turn-on signals is 180° . Again the inductor was connected in the positive input line, and the other parameters were kept the same. Fig. 4.10 shows the inductor current and CM leakage current. Firstly, it is seen that the inductor frequency is doubled, and the ripple decreases. Slight oscillations are also visible at turn-on and off instants. The CM current waveform shows that the high-frequency harmonics are also dominant in addition to 80 kHz current. The RMS of the CM current is 68 mA, which is close to the in-phase switching case. It is difficult to compare the result with the first scenario regarding magnitude and shape.

The last scenario is the out-of-phase switching using inductors at both input lines. Fig. 4.11 shows the resulting current waveforms. As shown in the in-phase switching case, the divided inductor helps to reduce oscillations at switching instants. The shape of the CM current is highly similar to the third case. Its RMS is 61 mA which is also close to the case with the inductor in the positive line. The comparison of the four experiments is presented in Table 4.3.

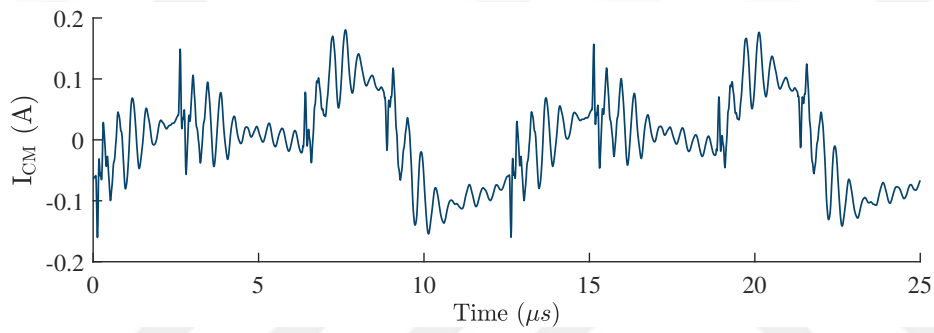
Table 4.3: Comparison of common mode leakage current experiments

	In-phase Switching		Out-of-phase Switching	
	Single Inductor	Divided Inductor	Single Inductor	Divided Inductor
$I_{CM(RMS)}$	71 mA	19 mA	68 mA	61 mA
I_L oscillation	present	reduced	present	reduced
Output Capacitors	unbalanced	balanced	unbalanced	balanced

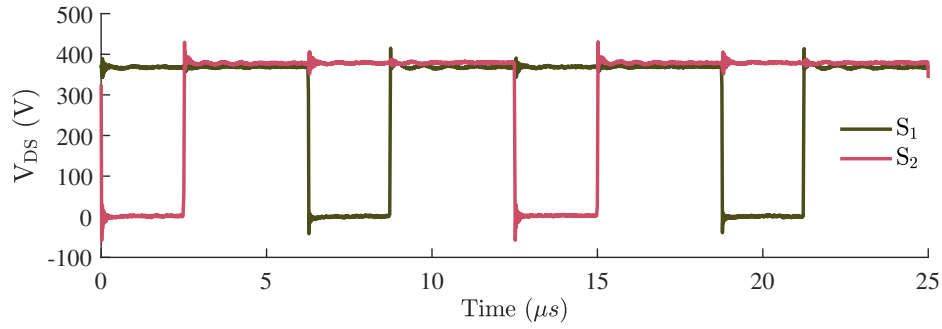
The drain-source voltages of the MOSFETs are given in the last plots of each case. It is shown that switch voltages are not equal unless the inductor is placed on both of the input lines. Dividing the inductor into two parts helps to balance the output capacitors. Otherwise, minor differences in the circuit may lead to huge differences in the output capacitor voltages. Since the windings of two inductors are on the same core, the size and the total number of turns do not change compared to a single-side connection. Hence, connecting the boost inductor to both inputs is always preferable. In the upcoming experiments, this configuration is used.



(a) Inductor current

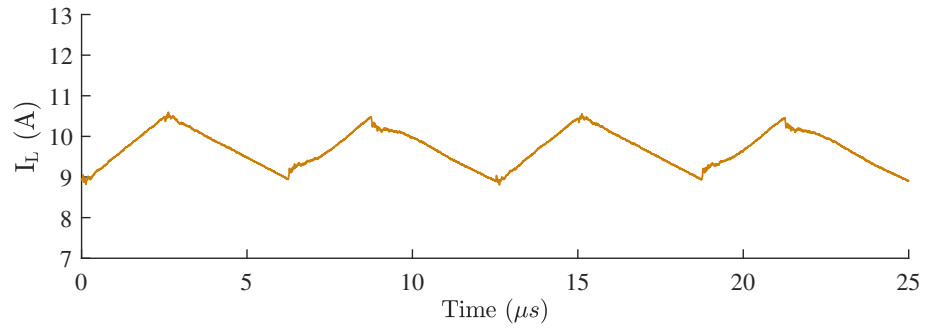


(b) Common mode leakage current

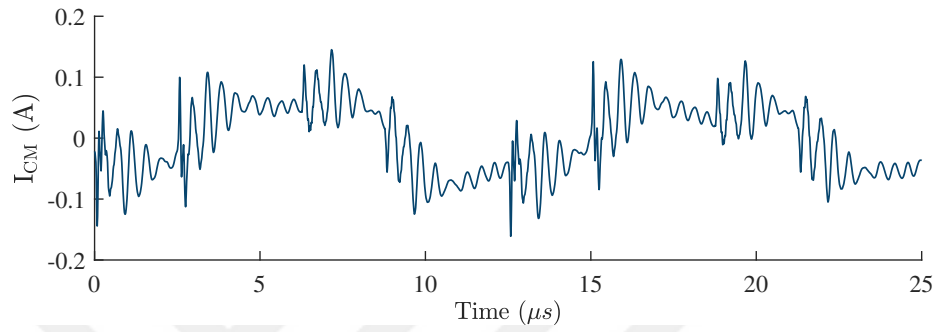


(c) MOSFET voltages

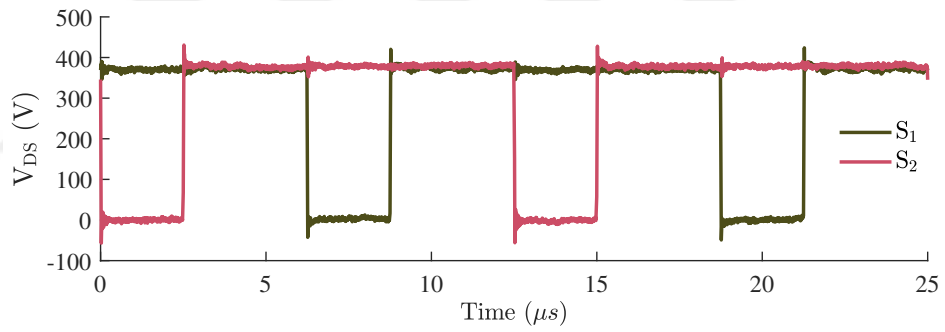
Figure 4.10: CM leakage investigation with out-of-phase switching scheme. The inductor is placed in positive input lines.



(a) Inductor current



(b) Common mode leakage current



(c) MOSFET voltages

Figure 4.11: CM leakage investigation with in-phase switching scheme. The inductor is placed on both of the input lines.

The above analysis proves that in-phase switching is required to minimize the CM leakage current. Yet, it is also clearly seen that the current ripple increases at the cost of reducing the CM leakage current. The thermal performance of the converter and components should be investigated.

4.4 Rated Voltage Experiments

The rated operating conditions of the 3L-BC prototype are studied in this section. The experimental setup is given in Fig. 4.12. The converter was tested with a Chroma 62180H-1800S voltage source at the input. A resistive load bank was connected to the output. Due to the power limit of the available DC voltage source, load resistance was adjusted as $95\ \Omega$, which approximately corresponds to an input power of 18 kW. The experimental data were gathered by Tektronix MSO46 200 MHz oscilloscope. The used current probe is Tektronix TCP015. Voltage measurements were taken with Tektronix THDP0100 differential probes.

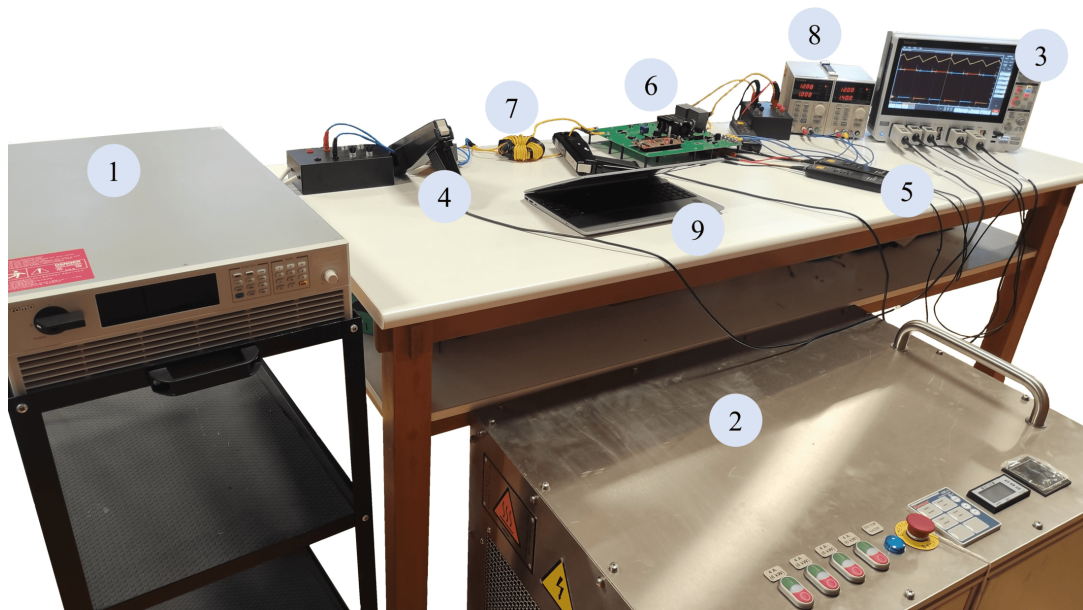


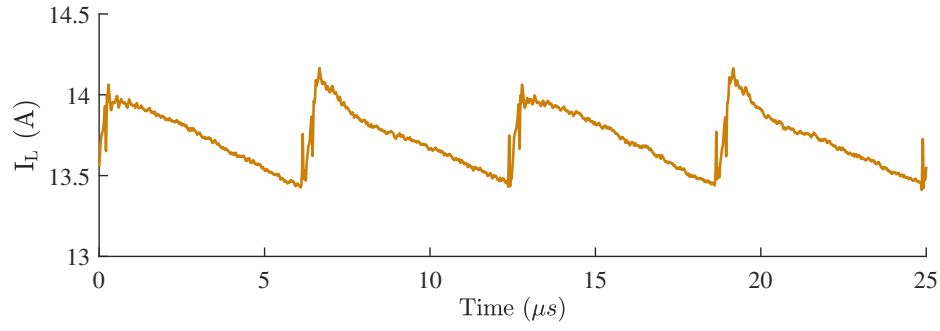
Figure 4.12: Experimental Setup (1: DC supply, 2: resistive load bank, 3: oscilloscope, 4: current probes, 5: voltage probes, 6: designed PCB, 7: boost inductor, 8: 12 V DC supply, 9: computer)

Firstly, the converter is tested with an input of 1275 V which is close to the upper voltage limit. The voltage waveforms of the semiconductor devices are given in Fig. 4.13 with inductor current and output voltage waveforms. The waveforms are given for two switching cycles, and out-of-phase switching technique is utilized. The duty cycles of the switches are set to 0.025 and output voltage nearly reaches to rated voltage. The semiconductor voltages are measured as the half of the output voltage when they are not conducting. At turn-on and turn-off instants, voltage spikes are

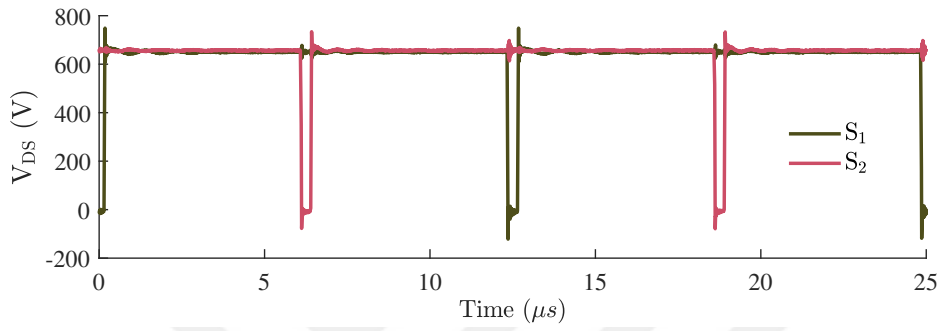
present as expected. The magnitude of the spikes are lower than 750 V and provides safe switching.

The experimental result of the rated input voltage (1050 V) is presented in Fig. 4.14. The duty cycles of the switches are identical and set to 0.2 to reach the rated output voltage, where the analytical duty cycle is 0.19. The semiconductor voltages reach 650 V at steady state. The magnitudes of the voltage oscillations at turn-on and turn-off instants are larger than the case of 1275 V input due to increased current for this case. However, all semiconductor voltages are within the safe operating regions.

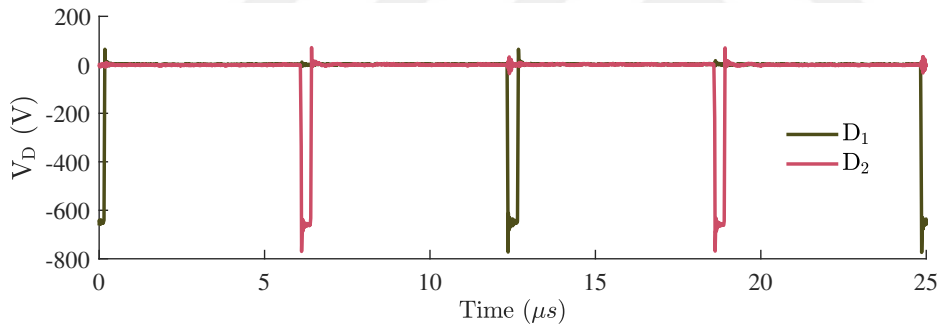
In 4.15, the same waveforms are given for the minimum input voltage condition. Maximum input current is drawn from the supply. Again, the output voltage is set to 1300 V. In Table 3.1, the required duty cycle was calculated as 0.35 for $V_{in} = 850$ V ideally. In the experiment, due to losses in the converter, $d_1 = d_2 = 0.358$ was applied to reach the rated output voltage. Due to minor differences in the components and PCB paths, device voltages slightly differ. The device's off-state voltages are 640 V and 670 V, reaching 777 V and 797 V at transients. The oscillations on the MOSFET and diode voltages are within the limits of the devices.



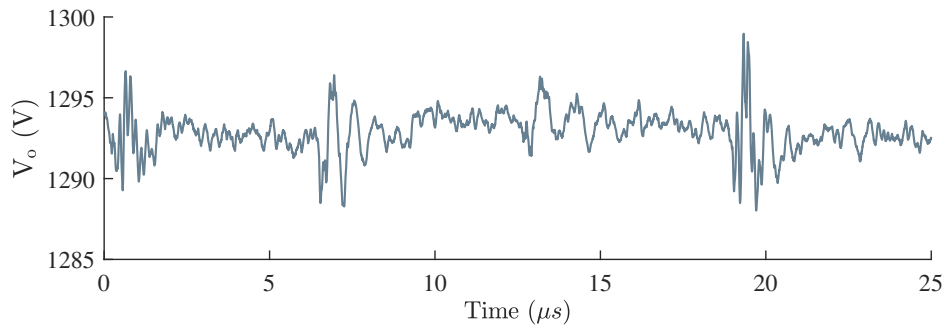
(a) Inductor Current



(b) MOSFET Drain Source Voltage

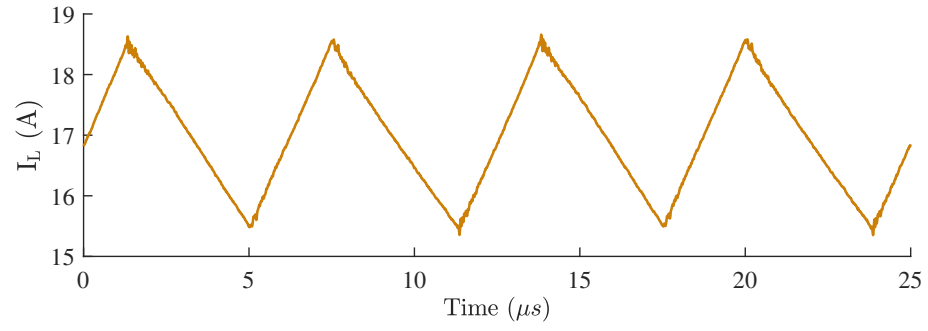


(c) Diode Voltage

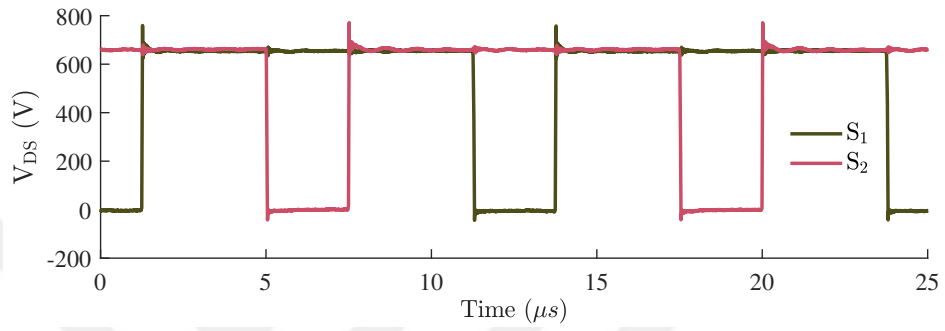


(d) Output Voltage

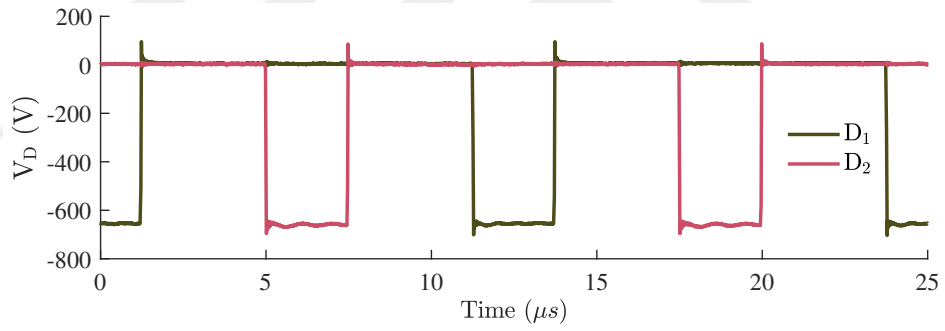
Figure 4.13: Circuit waveforms when $V_{in} = 1275$ V, $d = 0.025$



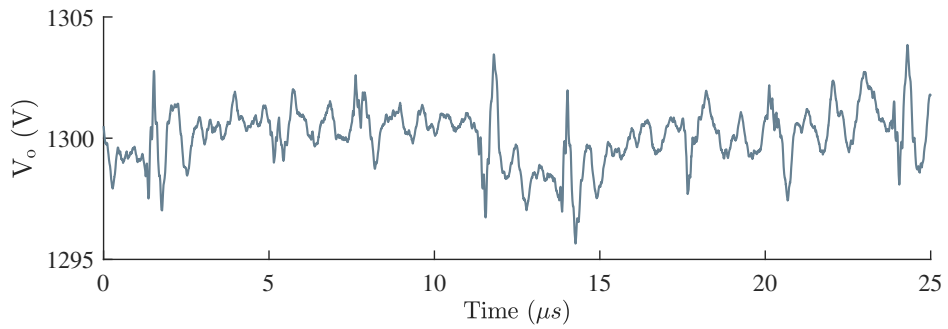
(a) Inductor Current



(b) MOSFET Drain Source Voltage



(c) Diode Voltage



(d) Output Voltage

Figure 4.14: Circuit waveforms when $V_{in} = 1050$ V, $d = 0.2$

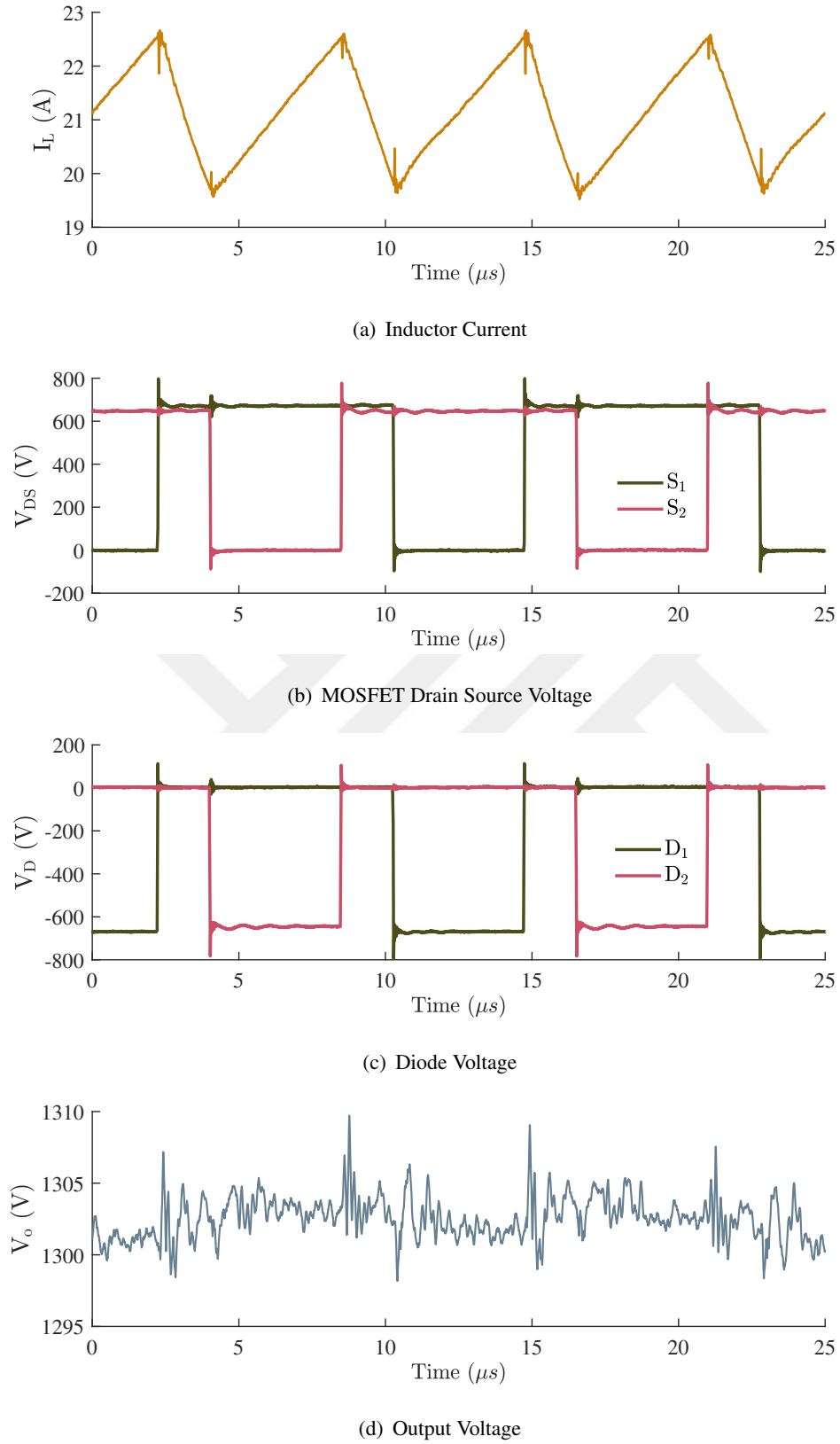


Figure 4.15: Circuit waveforms when $V_{in} = 850$ V, $d = 0.358$

4.5 Loss Measurements and Thermal Performance

The operation of the converter was verified, and different operating conditions were studied in the previous sections. This section presents loss measurements of the CM filter, boost inductor, and semiconductor devices. The efficiency results are compared with the expectations. Moreover, the thermal performance of the components is investigated.



Figure 4.16: Calorimeter setup to measure losses of the components

4.5.1 Loss and Efficiency Measurements

Electrical measurement of the loss and efficiency is extremely challenging in high-efficiency converters because of measurement errors. In this case, calorimetric measurement gives more precise results [57]. As the expected efficiency of the system is larger than 99%, the loss was measured with a calorimeter which is shown in Fig. 4.16. In fact, this method provided to measure the individual losses of the components. The known losses were first generated, and the reference temperature values were gathered. Then, components were individually placed in the calorimeter, and the temperature increase was noted under desired conditions. The losses of the devices were found by interpolating the reference data. The measurements are taken for nominal input voltage and also for the maximum input current condition. The measured losses are given in Table 4.4. In order to measure the individual loss of the CM filter, the relevant part was disconnected and assembled in another PCB. The

semiconductor device losses were measured in total. Since the power rating of the DC supply limits the rated power operation, the loss measurements were taken for 18 kW operation. For the conditions that experiments were conducted, the recalculated loss expectations are also given in Table 4.5 for comparison. The duty cycle values are updated with the experimental required ones. The cross-sectional area of the inductor winding is revised according to the used inductor.

Table 4.4: Loss measurements of devices for 18 kW operation

	In-phase Switching		Out-of-phase Switching	
	$V_{in} = 850 \text{ V}$	$V_{in} = 1050 \text{ V}$	$V_{in} = 850 \text{ V}$	$V_{in} = 1050 \text{ V}$
	$I_{in} = 21.2 \text{ A}$	$I_{in} = 16.9 \text{ A}$	$I_{in} = 21.2 \text{ A}$	$I_{in} = 16.9 \text{ A}$
CM Filter Loss	11 W	8 W	34 W	25 W
Boost Inductor Loss	35 W	19 W	20 W	15 W
Semiconductor Loss	105 W	75 W	105 W	75 W
Total Loss	151 W	102 W	159 W	115 W
Efficiency	99.2 %	99.4 %	99.1 %	99.3 %

Table 4.5: Recalculated losses for 18 kW operation

	In-phase Switching		Out-of-phase Switching	
	$V_{in} = 850 \text{ V}$	$V_{in} = 1050 \text{ V}$	$V_{in} = 850 \text{ V}$	$V_{in} = 1050 \text{ V}$
	$I_{in} = 21.2 \text{ A}$	$I_{in} = 16.9 \text{ A}$	$I_{in} = 21.2 \text{ A}$	$I_{in} = 16.9 \text{ A}$
Boost Inductor Loss	36 W	20 W	18 W	14 W
Semiconductor Loss	89 W	66 W	89 W	66 W

Looking at the loss values of the CM filter in Table 4.4, the first outstanding result is that the values of out-of-phase switching are much greater than in-phase switching. The CM leakage current in out-of-phase switching scheme generates a loss in the filter. In addition, higher input current results in higher losses because of the winding resistance of the filter.

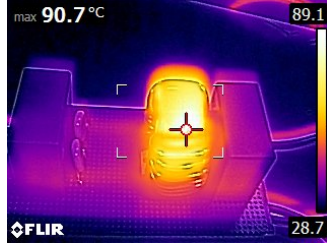
The measured inductor losses are close to expectations given in Table 4.5. Since the

copper area is updated according to the wire used in the inductor, the copper losses can be estimated accurately. Moreover, the DC bias characteristics were verified in Section 4.2. The ripple values are close to expectations; hence the core loss calculations are pretty close to the experimental results.

As expected and calculated in Table 4.5, experimental results show that the 850 V input case is the maximum semiconductor loss condition. The measured losses of the semiconductor devices are approximately 15% greater than the calculated ones, which does not cause an important problem. Overall, the measured efficiency of the converter ensures the requirements for all cases. Yet, the thermal performance of the components should be examined.

4.5.2 CM Filter Thermal Performance

The first considered component is the CM filter for thermal analysis. In Fig. 4.17, the thermal camera images of the CM filter are shown after some operation time. In Fig. 4.17.a, input voltage and current are set to 1050 V and 16.9 A. The output voltage is 1300 V. Out-of-phase switching scheme is applied, and the switching frequency is 80 kHz. The temperature of the filter gradually increased and reached 90.7°C. The rate of temperature increase did not slow down, and the converter was de-energized after 10 minutes. Similarly, the maximum current operation resulted in 94°C after 6 minutes and could not provide safe operation as shown in Fig. 4.17.b. It is clear that the selected filter was not able to work continuously under these circumstances. In Fig. 4.17.c, 1050 V operation is repeated with the in-phase switching scheme. In this case, the maximum temperature of the filter is 38.8°C, and the rate of temperature increase nearly vanished after 10 minutes. The hot spot moved to copper winding from the magnetic core. Thanks to decreased CM leakage current, the CM filter did not heat up to undesirable temperatures. The maximum input current case is shown in Fig. 4.17.d. The copper loss of the CM filter increases; hence the temperature of the filter increases but does not cause a problematic situation. The thermal images of the filter support the loss measurements.



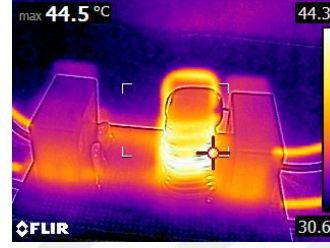
(a) Out-of-phase switching, 16.9 A, after 10 minutes



(b) Out-of-phase switching, 21.2 A, after 6 minutes



(c) In-phase switching, 16.9 A, after 10 minutes

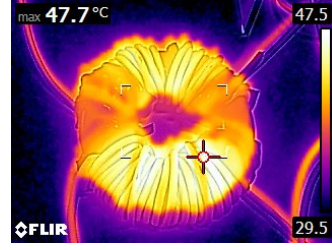


(d) In-phase switching, 21.2 A, after 10 minutes

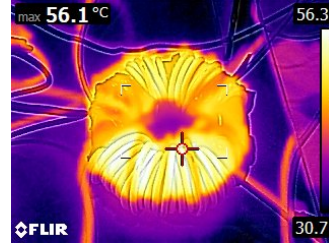
Figure 4.17: Thermal images of the CM filter

4.5.3 Inductor Thermal Performance

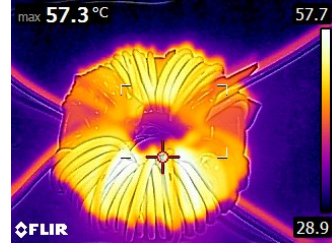
The second investigation item is the inductor. The nominal and minimum voltage operation conditions were tested with both switching techniques. For $V_{in} = 1050$ V case, the thermal images of the inductor are given in Fig. 4.18.a and Fig. 4.18.b for out-of-phase and in-phase switching techniques, respectively. The effect of the switching scheme on the inductor ripple was compared in Fig. 3.6. In-phase switching increases the ripple and losses. The resultant inductor temperature is higher as expected. The images of $V_{in} = 850$ V and $I_{in} = 21.2$ A are given in Fig. 4.18.c and Fig. 4.18.d. The current waveforms of these cases were analyzed in Section 4.2 and given in Fig. 4.7. Since the inductor current is increased, the temperature of the inductor increases for both techniques. The worst case for the inductor is the last case with the largest ripple, and the inductor reached 73.3°C . Applying in-phase switching brought the CM filter temperature to an acceptable level. In return, inductor losses are increased. Nevertheless, the inductor is thermally more stable thanks to the larger volume and can handle the increased losses.



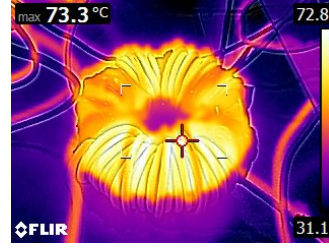
(a) Out-of-phase switching, 16.9 A



(b) In-phase switching, 16.9 A



(c) Out-of-phase switching, 21.2 A



(d) Inphase switching, 21.2 A

Figure 4.18: Thermal images of the boost inductor

4.5.4 Thermal Performance of Semiconductor Devices

In the last test, the thermal performances of the semiconductor devices are examined. Loss measurements show that the maximum loss appears at $V_{in} = 850$ V condition. The thermal image of this operation is given in Fig. 4.19. It is shown that the switching scheme does not change the temperature of the switches as proposed. If the total measured loss of the semiconductors is scaled according to analytical calculations and used to find the case temperature of MOSFET, the created thermal circuit results in 106°C as in (4.1). The thermal image indicates a close value. The thermal resistances might be higher in the constituted cooling system. All tests were performed safely, so thermal improvements are not critical for this prototype.

$$T_c = (30\text{W})(1.2^{\circ}\text{C/W}) + (105\text{W})(0.4^{\circ}\text{C/W}) + (28^{\circ}\text{C}) = 106^{\circ}\text{C} \quad (4.1)$$

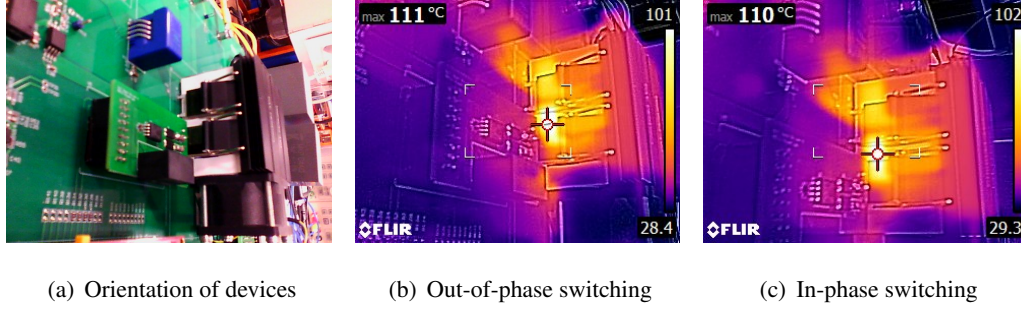


Figure 4.19: Images of semiconductor devices ($V_{in} = 850$ V, $I_{in} = 21.2$ A, $f_s = 80$ kHz)

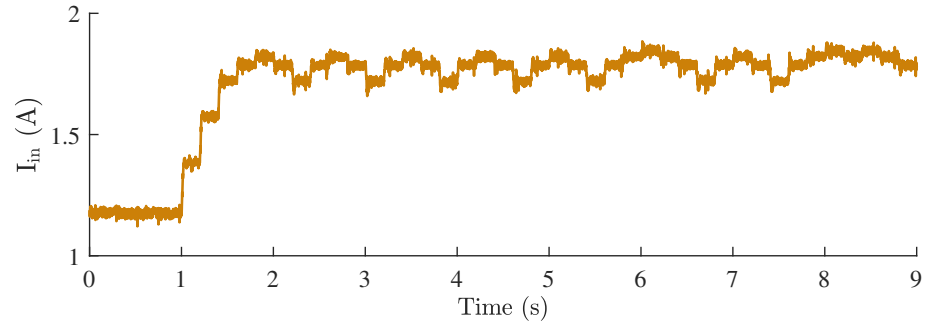
4.6 Maximum Power Point Tracking Algorithm Implementation

As described in the relevant sections, the P&O algorithm is utilized to find the required duty cycle and operate at the maximum power point of the PV string. In Fig. 4.20, the MPPT algorithm test result is given. In order to test the algorithm, Chroma 62180H-1800S PV array simulator was connected to the converter's input. Table 4.6 gives the simulated PV array characteristics. An electrical load was connected to the output and set as a constant voltage source ($V_o = 140$ V). The load behaves like the inverter and keeps the DC-link voltage constant.

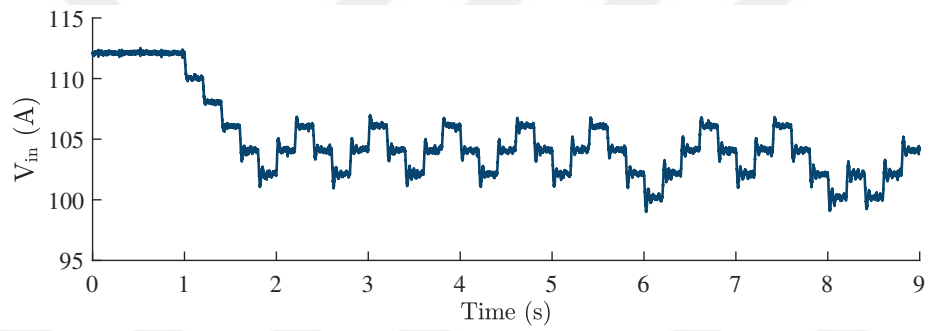
Table 4.6: Simulated PV array characteristics for MPPT algorithm test

V_{oc}	120 V	I_{sc}	2 A
V_{mpp}	104 V	I_{mpp}	1.8 A

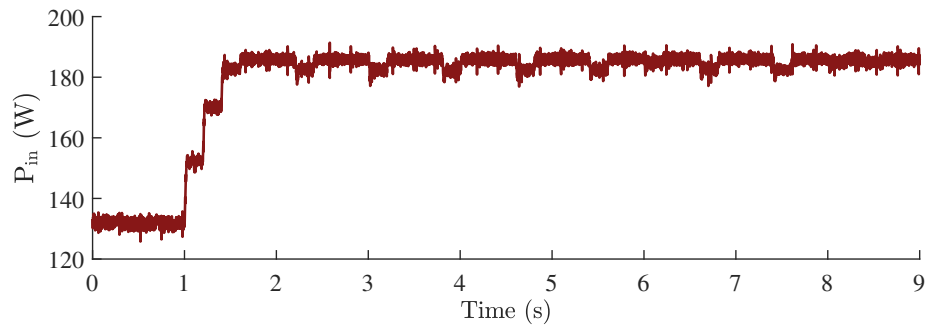
Initially, the converter started at a constant duty cycle and stayed in an idle state. At $t = 1$ s, the MPPT algorithm is enabled. Then the input reference voltage is reduced. The voltage step was set as 2 V in the test. Input voltage continued to decrease since the power increased in the same direction. When the power started to decrease, the PV reference voltage was increased. Once the algorithm reached the maximum power point, it oscillated around it.



(a) Input Current



(b) Input Voltage



(c) Input Power

Figure 4.20: MPPT algorithm test result

4.7 Capacitor Voltage Balance Experiment

In Section 3.8.1, the capacitor voltage balancing algorithm was shown. An experimental setup was built to verify the algorithm, as presented in Fig. 4.21. Two different resistive loads ($R_1 = 1050 \, \Omega$, $R_2 = 1000 \, \Omega$) were connected to each output capacitor in addition to main load resistance ($R_L = 95 \, \Omega$.) The converter's input voltage was set to 500 V. The result of this experiment is shown in Fig. 4.22. Initially, the algorithm is inactive, and capacitor voltages are unequal due to unbalanced loads. At $t = 5 \, \text{ms}$, the algorithm is enabled. Then, the controller updates the duty cycle of switches so that the voltages are equalized. It is seen that voltages are equalized after 2 ms. In Fig. 4.22.a, the inductor current is given for the same time interval. When the algorithm is enabled, changing duty cycles results in oscillation in the current. The oscillation also settles within the 2 ms.

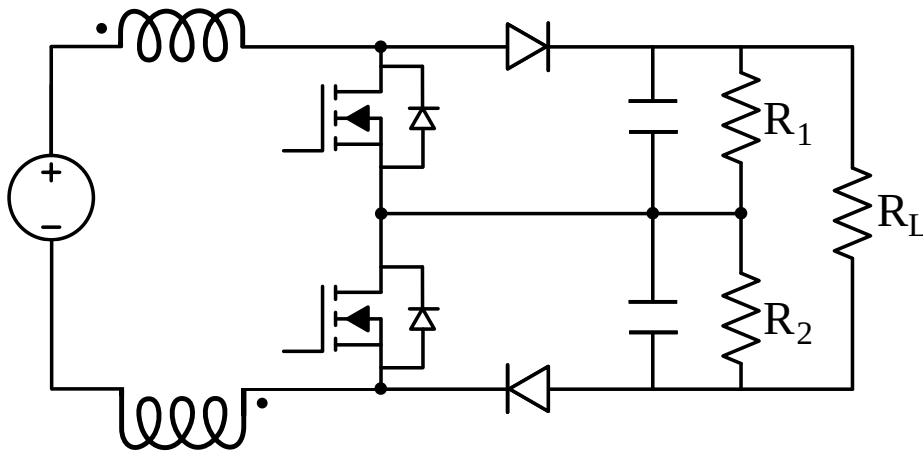
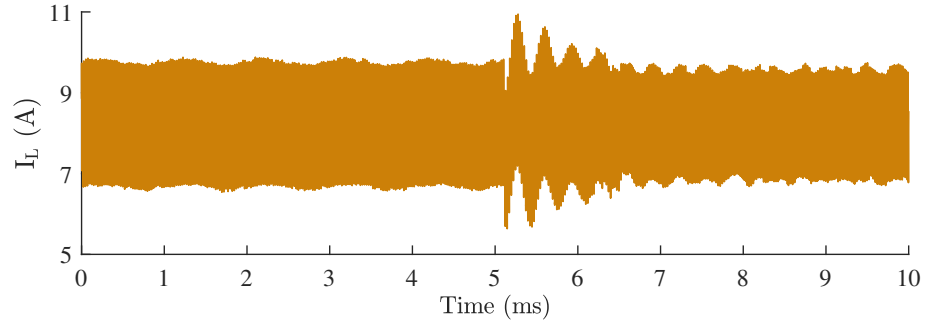
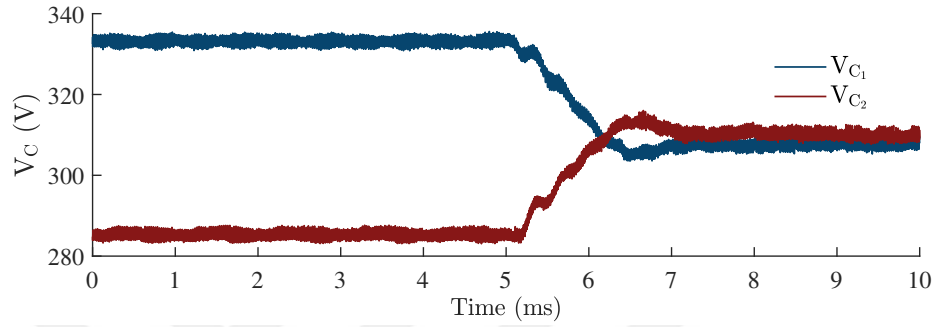


Figure 4.21: Circuit diagram for voltage balance experiment



(a) Inductor Current



(b) Output Capacitor Voltages

Figure 4.22: Performance of voltage balance algorithm

4.8 Conclusion

In this chapter, the implementation of the 3L-BC is presented. Then, different design decisions were evaluated with experimental results. Although the results imply that the designed converter can perform the required tasks, experiments revealed some remarkable outcomes. These can be summarized as follows:

- Inter-winding capacitance plays an important role in high-voltage, high-frequency applications. A new inductor manufacturing should provide low capacitance and desired copper area at the same time.
- Out-of-phase switching results in CM voltage generation. Generated CM voltage creates loss on the CM filter and heats up the filter. The selected filter is not able to work under these conditions. Custom CM filter design may overcome the problem.

- In-phase switching decreases the CM leakage current and lightens the load of CM filter.
- Out-of-phase switching technique provides less ripple and less inductor losses. As the duty-cycle approaches 0.5, the advantage of out-of-phase switching increases.
- Efficiency measurements show that desired efficiency limit is achieved for all switching conditions.
- Analyzing the thermal images and loss measurements, in-phase switching scheme is more applicable.
- In the case of in-phase switching scheme, boost inductor heating might warm up the surroundings. Proper placement should be made.

In accordance with these outcomes, the overall design of the 8-parallel boost converter will be examined in the next chapter.

CHAPTER 5

DESIGN AND INTERLEAVED OPERATION OF 3L-BC FOR MULTI-STRING INVERTER

In Chapter 3, the design of a single 3L-BC was investigated, and component selections are discussed. The performance of the designed converter was verified in Chapter 4. In this chapter, the design of the single converter will be adopted for multi-string inverter. The number of MPP trackers is selected as eight as discussed in Chapter 2. Thus, eight parallel 3L-BC design will be examined in this chapter, and the interleaved operations of the converters will be investigated. A novel algorithm to minimize the DC-link capacitor current ripple will be presented. In the end, the design and the current minimization algorithm is verified with experimental results.

5.1 Multi-String Inverter DC/DC Stage PCB Design

In the previous chapter, it is shown that the designed converter is capable of boosting the input voltage to the desired output voltage. Hence, for the multi-string inverter, the same design will be used with some modifications. The design decisions are given as follows. Note that some of the requirements are specified for the use of the DC/AC stage, which is not the subject of this thesis.

- The selected semiconductors perform the rated voltage operation safely. The measured loss values are close to analytical calculations and within the limits of the loss budget. Hence, the same devices will be used in the new design.
- Although the designed inductor is proved to be sufficient, a higher copper area is preferred to minimize losses. Hence, a new inductor is procured with wider

copper wires in a similar total volume.

- To keep the overall size and weight of the product as small as possible, the size of the DC/DC stage should be minimized.
- The DC/DC converters are paralleled at the output and connected to the DC/AC stage. Thus, the designed PCB should provide the required connection points.
- Cooling will be performed by a heat sink-fan combination, whose selection criteria are based on DC/DC and DC/AC stage requirements. The designed cooling system should provide safe operation for rated conditions under the designed temperature range.
- Each DC/DC converter should be operated at MPP. Hence, input voltage and current are measured for all converters individually.
- A micro-controller is selected so that the MPPT algorithm can be utilized based on the voltage and current measurements.
- In total, 16 PWM signals should be generated for 8 DC/DC converters.

According to the requirements listed above, a new PCB was designed. Firstly, the gate driver was downsized to reach a more compact design, as shown in Fig. 5.1. The used circuitry was kept the same, but the size decreased to 16 mm x 50 mm, whereas the old one was 32 mm x 50 mm.

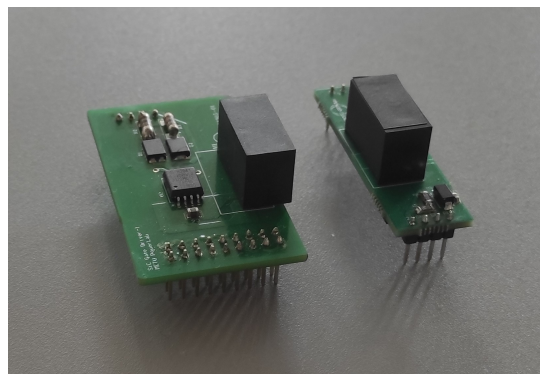


Figure 5.1: Old and renewed gate driver PCBs

Then, the overall PCB was designed to be as small as possible. The design consists of two parts, which are the input filter and the main power board. The input filter is

presented in Fig. 5.2, whose length is 620 mm and width is 130 mm. The length of the main power PCB is 700 mm, and the width is 220 mm, which is shown in Fig. 5.3 as placed on the designed heat sink. The remaining heat sink is allocated for the DC/AC stage. The output capacitors are not shown in the figure and will be placed on the DC/AC stage.

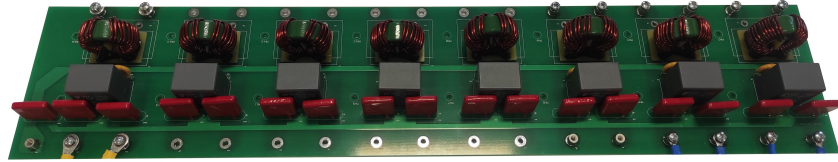


Figure 5.2: Input filter PCB for multi-string inverter

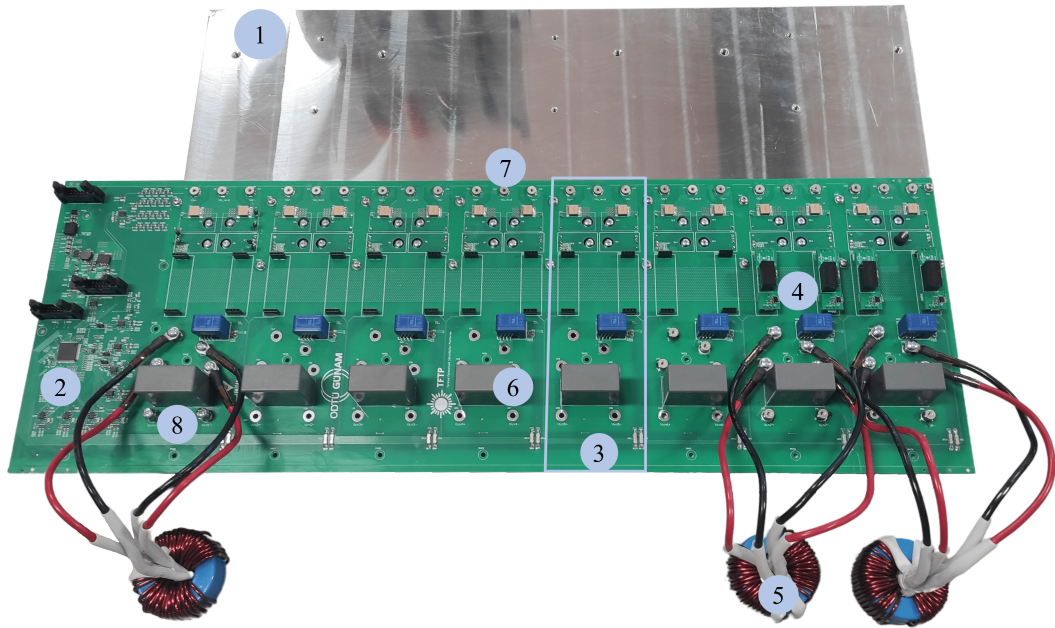


Figure 5.3: New PCB design for multi-string PV inverter. (1: heat sink, 2: controller, 3: one of the paralleled DC/DC converters, 4: gate drivers, 5: boost inductor, 6: input capacitor, 7: output connectors, 8: input connectors)

5.2 Verification of the PCB Design

The operation of the converter was verified with the designed prototype as presented in Chapter 4. However, there are some modifications in the implementation. Especially the layout is designed from scratch. Hence, the new PCB needs verification. Similar to experiments with the first prototype, the new design is tested with Chroma 62180H-1800S DC supply and the resistive load bank. To test the new inductor and PCB, the most stressful operation case is experimented with the maximum input current and the maximum ripple. Input voltage is set to 850 V, and in-phase switching is utilized. In Fig. 5.4, the thermal image of the inductor is shown. It is seen that the temperature of the inductor reaches 55°C, which was 73°C in the same operation with the first inductor, thanks to increased winding copper area. The circuit waveforms of the converters are presented in Fig. 5.5. It is seen that the new layout design is capable of operating at the rated conditions. In the next sections, the parallel operation of the converters will be investigated.

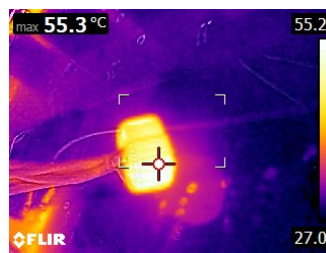
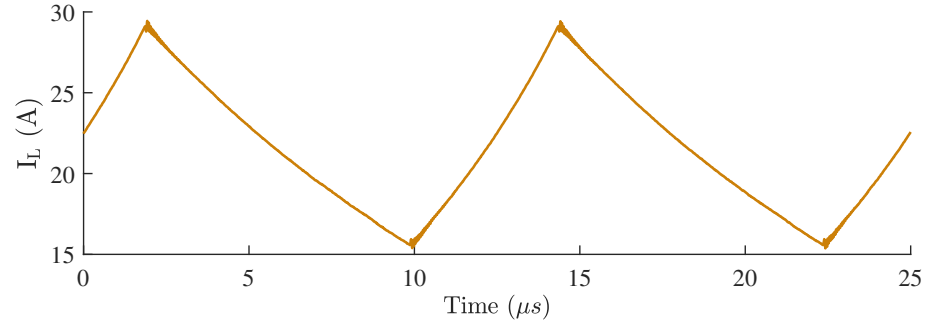
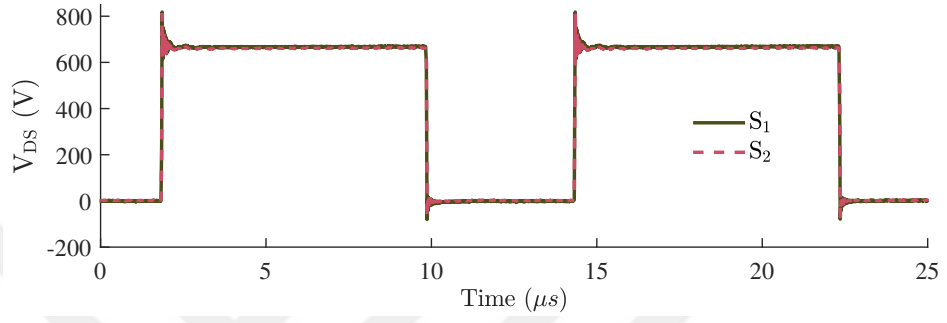


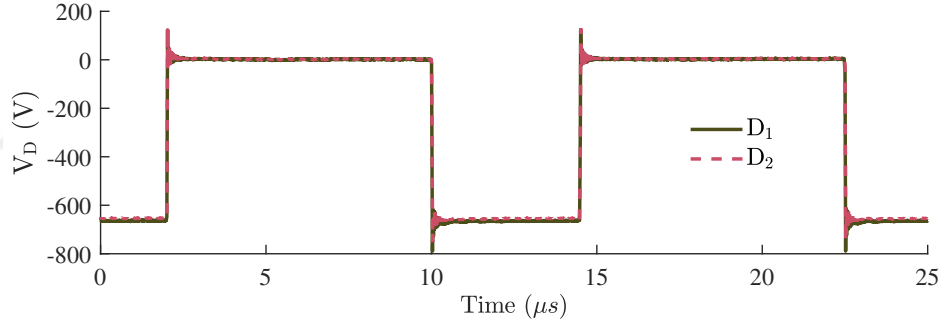
Figure 5.4: Thermal image of the new boost inductor, in-phase switching, 21.2 A



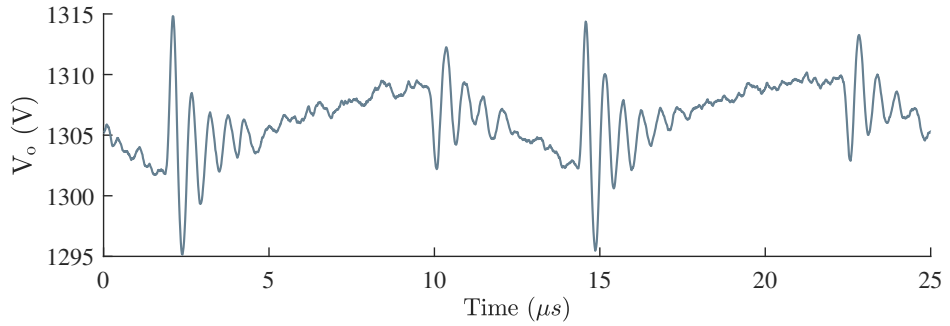
(a) Inductor Current



(b) MOSFET Drain Source Voltage



(c) Diode Voltage



(d) Output Voltage

Figure 5.5: Circuit waveforms of a single DC/DC converter of the multi-string inverter when $V_{in} = 850$ V, $d = 0.358$

5.3 Interleaved DC/DC Converters

Parallel operation of the DC/DC converters has been studied in the literature [58, 59, 60]. In order to decrease the current ratings of the devices and provide fault-tolerant operations, a number of converters are parallel connected in single-input single-output configuration as shown in Fig. 5.6. Additionally, if the converters operate with phase shift, known as interleaving, input and output ripples reduce. Reducing the ripple decreases the size of the filter elements or decreases the losses. In single-input single-output case with N converter modules, the required phase shift between the modules is found by (5.1).

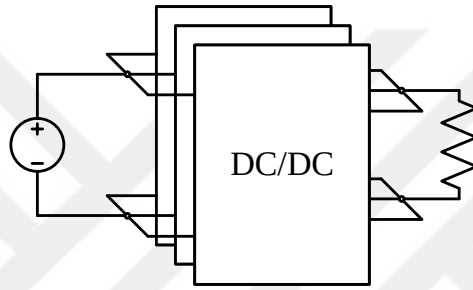


Figure 5.6: Conventional single-input single-output interleaved DC/DC converters

$$\theta = \frac{360^\circ}{N} \quad (5.1)$$

Interleaving of single-input single-output systems is a well-known and applied technique in the literature. However, the interleaved operation of multi-input single-output converters still attracts attention. DC/DC converters in multi-string inverters are investigated in this concept. Due to the placement of the strings, the operating conditions of converters may differ. Additionally, shadowing or aging of the PV strings may lead to different MPP operations. In these cases, conventional methods may not find the optimal phase shift angle. In the literature, the interleaving of converters having different operating conditions is investigated. [61] investigates the single-input single-output buck-boost converters, but inductor tolerances result in asymmetric operations. Harmonic analysis is used to minimize the first harmonic of the output ripple. In [62], single input multiple output DC/DC converters are analyzed. The aim is

to minimize input current ripple by interleaving the asymmetric operated converters. To find the optimal phase shift, harmonic analysis is performed, and a look-up table is generated. Then, the required phase shift is found from the look-up table during the operation. In [63], interleaving phase shift is optimized for asymmetric operated converters under faulty conditions. In the optimization, the selected harmonic minimization method is presented. Similarly, [64] presents the harmonic elimination method for a multi-input series connected output DC/DC converter. To minimize the output current ripple, the first harmonic of each converter module is analyzed, and the required phase angle is calculated. In [65], it is said that minimizing a single harmonic does not result in the best result. Hence, the authors suggest a recursive search method for a multi-string PV inverter application. For the selected phase angle combination, the harmonic analysis is performed by considering the harmonics up to the desired order. Then, the surroundings of the first selected case are searched. In an iterative way, the optimal angles are found. A decentralized interleaving algorithm is presented in [66]. Output voltage ripple minimization is achieved by the decision of each converter, but it requires the ripple measurement for each individual converter. In [67], instead of harmonic analysis, the waveform of the output capacitor is analytically defined, and ripple minimization is investigated. Similarly, the algorithm presented in [68] relies on time domain analysis and is implemented by logic gates. It is used in multi-input single-output buck converters in order to minimize output voltage ripple.

In summary, the interleaving of asymmetric DC/DC converters gathers the attention of researchers. Algorithms commonly rely on harmonic analysis. The ones considering a single harmonic lack of information. On the other hand, including several harmonics increases the computational cost; hence, a direct solution may not be found. In this section, a capacitor current minimization algorithm will be presented that involves the first two harmonics of the capacitor currents. The analysis is based on the current waveform of a three-level boost converter with out-of-phase switching scheme. However, the proposed method is independent of the switching scheme or the converter type. By updating the investigated waveform, the proposed method can be implemented for any type of converter.

5.3.1 Investigation of Harmonic Content of the Capacitor Current

In the 3L-BC topology, there are two capacitors that ideally share the output voltage equally, as discussed before. In the below analysis, the duty cycle of switches is assumed to be the same, and equal voltage of capacitors is provided. Hence, the currents of each capacitor are equal but phase-shifted by 180° due to out-of-phase switching scheme. For the sake of simplicity, analysis, and derivations are given for the top-side capacitor. However, minimizing the top-side capacitor current also minimizes the bottom-side due to equal voltage and duty cycle assumption. In order to analyze the current of the output capacitor, the harmonic spectrum is investigated in this part. The typical capacitor current waveform is given in Fig. 5.7 for a switching period (T_s), where $V_{in} = 850$ V, $V_o = 1300$ V and $P_{in} = 20$ kW. The given waveform is constructed by assuming that the output voltage is constant and the inductor current is perfectly triangular. This assumption is used in different papers [65, 67] and is valid if the output voltage ripple is much smaller than the average output voltage, which is the case in a well-designed converter.

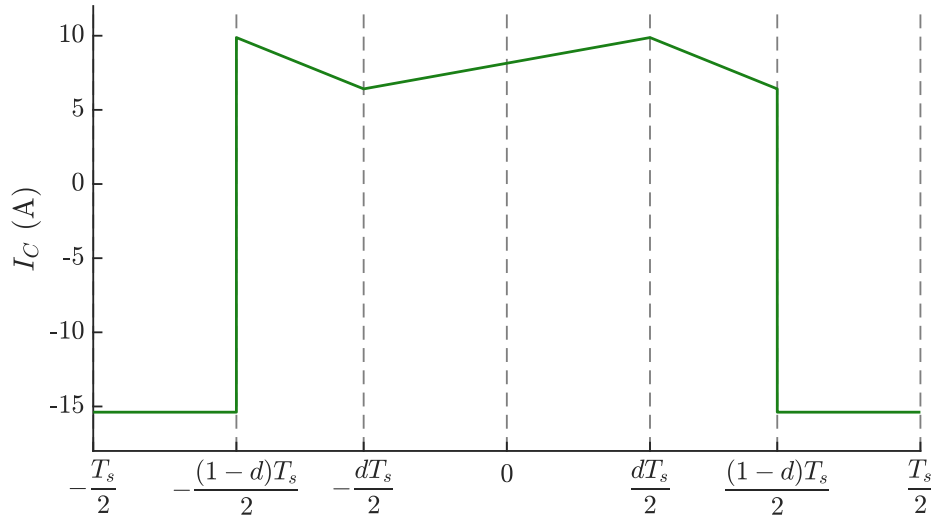


Figure 5.7: Capacitor current waveform ($V_{in} = 850$ V, $V_o = 1300$ V and $P_{in} = 20$ kW)

The capacitor current ($I_c(t)$) can be expressed as the summation of sinusoidal signals with integer multiples of the fundamental frequency as given in (5.2), which is known as the Fourier series expansion. Here, it should be noted that there is no DC component of the current. Hence, the a_0 coefficient is not considered in the equation. The

remaining Fourier coefficients (a_n, b_n) are found by (5.3) and (5.4).

$$I_c(t) = \sum_{n=1}^{\infty} (a_n \cos(2\pi n f_s t) + b_n \sin(2\pi n f_s t)) \quad (5.2)$$

$$a_n = \frac{1}{T_s} \int_{-T_s/2}^{T_s/2} i_c(t) \cos(2\pi n f_s t) dt \quad (5.3)$$

$$b_n = \frac{1}{T_s} \int_{-T_s/2}^{T_s/2} i_c(t) \sin(2\pi n f_s t) dt \quad (5.4)$$

Time domain capacitor current is derived in (5.5) in terms of d, T_s, I_{max}, I_{min} and I_{out} . The time intervals are written explicitly in Fig. 5.7. The current magnitudes are calculated in (5.6), (5.7) and (5.8). All variables used to define $I_c(t)$ can be expressed by the measured values for the MPPT algorithm, which are input voltage, input current, and duty cycle defined by the controller.

$$I_c(t) = \begin{cases} -I_{out} & t_0 < t < t_1 \\ \frac{(t + (1-d)T_s/2)(I_{max} - I_{min})}{(dT_s - T_s/2)} + I_{max} & t_1 < t < t_2 \\ \frac{(t + dT_s/2)(I_{max} - I_{min})}{dT_s} + I_{min} & t_2 < t < t_3 \\ \frac{(t - dT_s/2)(I_{max} - I_{min})}{dT_s - T_s/2} + I_{max} & t_3 < t < t_4 \\ -I_{out} & t_4 < t < t_5 \end{cases} \quad (5.5)$$

$$I_{out} = (1-d)I_{in} \quad (5.6)$$

$$I_{max} = I_{in} + \Delta I_L/2 - I_{out} = dI_{in} + \Delta I_L/2 \quad (5.7)$$

$$I_{min} = I_{in} - \Delta I_L/2 - I_{out} = dI_{in} - \Delta I_L/2 \quad (5.8)$$

Based on the integrations, Fourier series coefficients are given in (5.9) and (5.10).

$$a_n = -\frac{I_{in} \sin(n\pi(d-1))}{(n\pi)} \quad (5.9)$$

$$b_n = -\Delta I_L \frac{\sin(n\pi d) + 2d\sin(n\pi(d-1)) + dn\pi(1-2d)\cos(n\pi(d-1))}{2d^2n^2\pi^2} \quad (5.10)$$

Once the Fourier coefficients are found, $I_c(t)$ can be formulated in terms of current harmonics with magnitudes $|I_n|$ and phases ϕ_n , where $|I_n| = \sqrt{a_n^2 + b_n^2}$ and $\phi_n = \arctan(b_n/a_n)$.

$$I_c(t) = \sum_{n=1}^{\infty} |I_n| \cos(2\pi n f_s t - \phi_n) \quad (5.11)$$

The harmonic content of the above presented current waveform is shown in Fig. 5.8. The most dominant harmonic is at switching frequency as expected. It is also clearly seen that the magnitude of the second harmonic is also significant. In Fig. 5.9, the harmonic content of the case with $V_{in} = 1050$ V is investigated. The dominance of the first harmonic is decreased for this operation. Hence, it is clear that minimizing only the first harmonic does not provide the most effective solution.

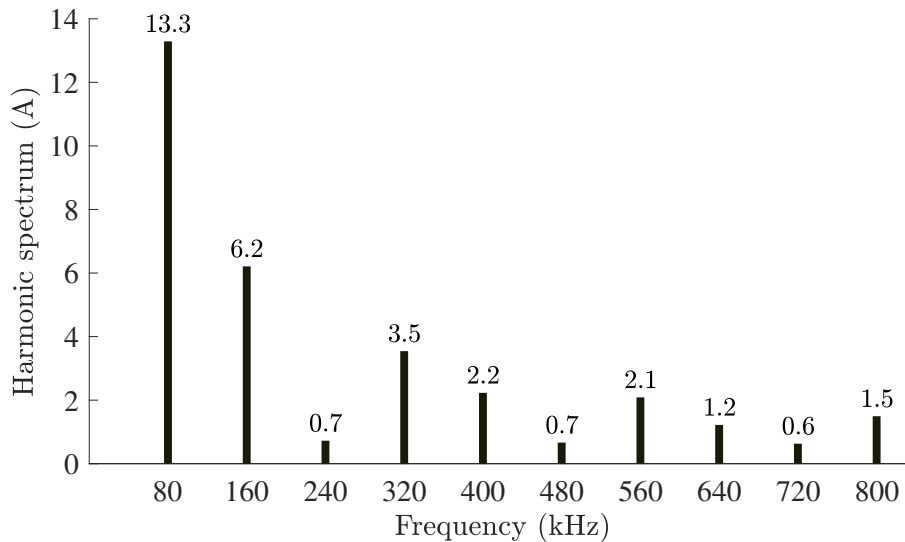


Figure 5.8: Harmonic analysis of the capacitor current, $V_{in} = 850$ V

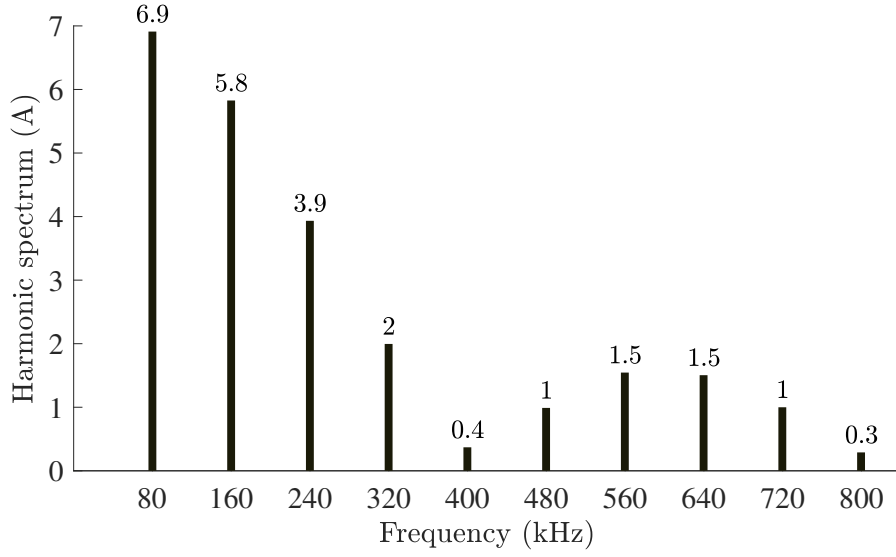


Figure 5.9: Harmonic analysis of the capacitor current, $V_{in} = 1050$ V

5.3.2 Harmonic Current Reduction Analysis

In order to minimize the capacitor current, all of the harmonics should be considered. However, it is not easy to reach an analytical solution in this way. Hence, $|I_c^{(k)}|^2$ is defined as the summation of the square of harmonics up to k^{th} one as in (5.12). In the below analysis, the first two harmonics are minimized. The analysis can be widened for higher harmonics if required by applying the same procedure given in the following equations.

$$|I_c^{(k)}|^2 = \sum_{n=1}^k |I_n|^2 \quad (5.12)$$

5.3.2.1 Interleaving of Two Modules

When two converters are used in the single-input single-output topology, 180° phase shift is applied to minimize the ripple components. However, this might not result in the minimum capacitor current for multi-input single-output topologies. When the operating conditions of converters differ, the optimal point shifts away from 180° . A sample operation is discussed here to see the effect of asymmetric operation. The operating conditions of the converters are given in Table 5.1.

Table 5.1: Sample case for two-module interleaving analysis

Parameter	Value
Output Voltage	1300 V
Module-1 input voltage	1050 V
Module-1 input current	19 A
Module-2 input voltage	1050 V
Module-2 input current	5 A

For this operating condition, the analysis result of $|I_c^{(k)}|^2$ with respect to phase shift angle is given in Fig. 5.10. When all harmonics are considered ($k = \infty$), it is seen that the optimal phase angle moves away from 180° . If only the first harmonic is considered, the required angle is found as 180° . On the other hand, implementing the algorithm with the first two phases, the found phase shift is closer to the optimal required phase.

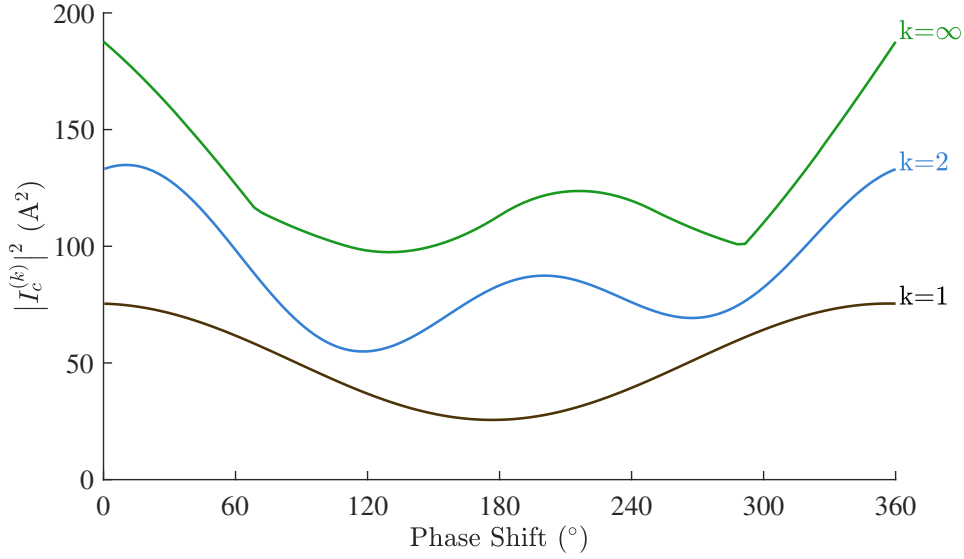


Figure 5.10: $|I_c^{(k)}|^2$ change with respect to phase shift angle for different k values

To examine the sum of the first two harmonic squares, the first and second harmonic of the capacitor current should be computed. Let I_1 denote the first harmonic of the capacitor current, whereas $I_{1,x}$ and $I_{1,y}$ are the contributions of each boost module, named x and y for clarity. Magnitude of I_1 , which is the vector addition of $I_{1,x}$

and $I_{1,y}$, is found in (5.13). Here, θ_i is the initial phase difference of the module harmonics, and θ is the applied phase shift. For the calculation of the second harmonic component, (5.14) is used, where θ_{2i} is the initial phase difference of second harmonic currents. These equations are depicted in Fig. 5.11.

$$|I_1|^2 = |I_{1,x}|^2 + |I_{1,y}|^2 + 2|I_{1,x}||I_{1,y}|\cos(\theta + \theta_i) \quad (5.13)$$

$$|I_2|^2 = |I_{2,x}|^2 + |I_{2,y}|^2 + 2|I_{2,x}||I_{2,y}|\cos(2\theta + \theta_{2i}) \quad (5.14)$$

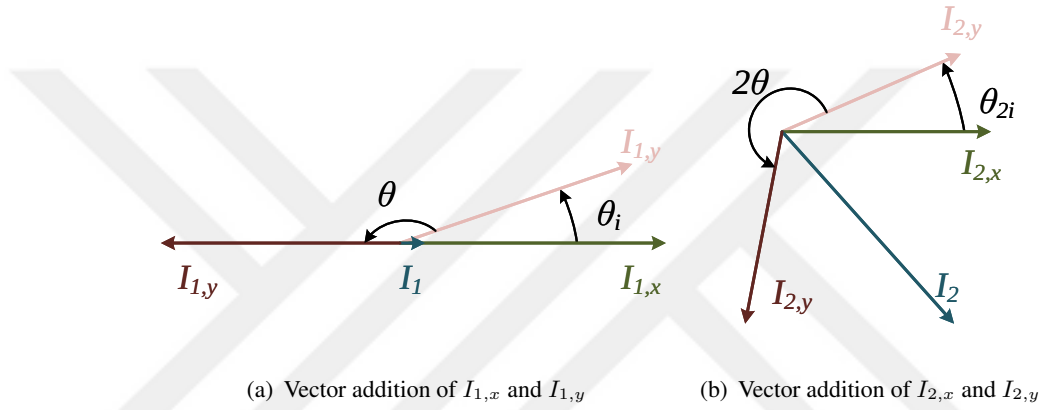


Figure 5.11: Visual representation of the vector addition of current harmonics

To find the minimum point of $|I_1|^2 + |I_2|^2$, derivative operator is used with respect to phase shift angle. However, as shown in (5.15), derivative operation results in $\sin(\theta)$ and $\sin(2\theta)$ terms which are not linear, and a simple solution is not present. Hence, an approximation is useful to find the minimum current phase angle. To make an approximation, the boundaries should be found first.

$$\frac{d(|I_1|^2 + |I_2|^2)}{d\theta} = -2|I_{1,x}||I_{1,y}|\sin(\theta + \theta_i) - 4|I_{2,x}||I_{2,y}|\sin(2\theta + \theta_{2i}) \quad (5.15)$$

In Fig. 5.12, two possible regions are marked for minimum current operation. Those correspond to angles in which one of the harmonics is increasing, but the other is decreasing. Otherwise, the sum of the harmonics is monotonically increasing or decreasing. As shown in Fig. 5.12, the absolute minimum occurs in the region between

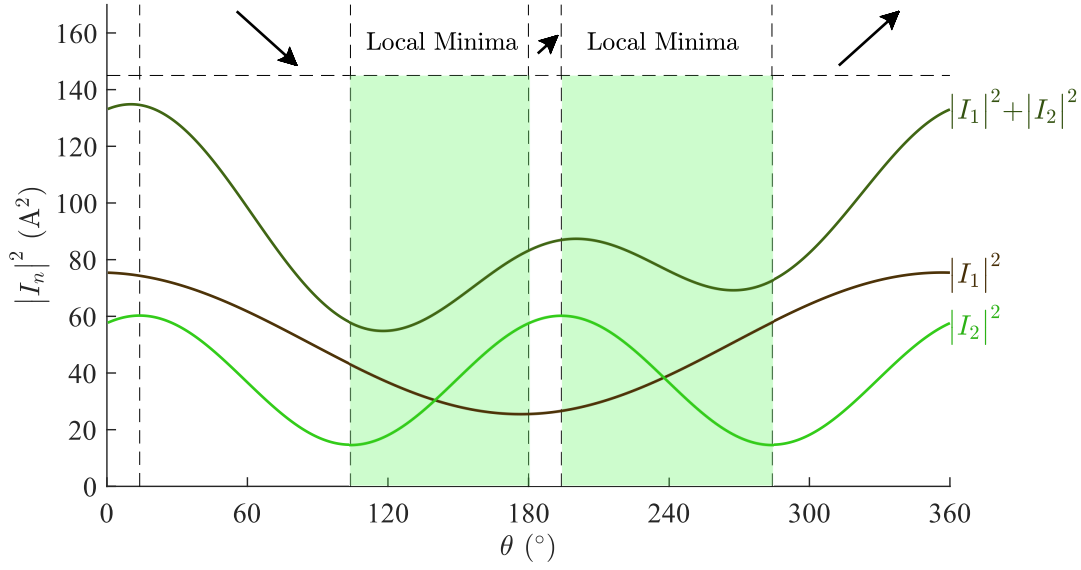


Figure 5.12: Local and absolute minimum points based on the algorithm

the angles minimizing the first and the second harmonics. For the second harmonic minimization, there are two angles, but the one that is closer to the angle minimizing the first harmonic encloses the region.

According to (5.13) and (5.14), first harmonic minimizing phase shift is $\theta_{1,min} = \pi - \theta_i$, and second harmonic minimizing phase shifts are $\theta_{2,min} = (\pi - \theta_{2i})/2$ and $\theta_{2,min} = (3\pi - \theta_{2i})/2$. In the identified interval, approximations can be made based on the shape of the function. Below quadratic equations will be used to approximate $I_1^2(\theta)$ and $I_2^2(\theta)$.

$$I_{1,approx}^2(\theta) = \frac{|I_1(\theta_{2,min})|^2 - |I_1(\theta_{1,min})|^2}{(\theta_{1,min} - \theta_{2,min})^2}(\theta - \theta_{1,min})^2 + |I_1(\theta_{1,min})|^2 \quad (5.16)$$

$$I_{2,approx}^2(\theta) = \frac{|I_2(\theta_{1,min})|^2 - |I_2(\theta_{2,min})|^2}{(\theta_{1,min} - \theta_{2,min})^2}(\theta - \theta_{2,min})^2 + |I_2(\theta_{2,min})|^2 \quad (5.17)$$

Differentiating the sum of (5.16) and (5.17), capacitor current minimizing phase shift is found as given in (5.18). The overall flowchart of the algorithm is presented in Fig. 5.13 as a summary.

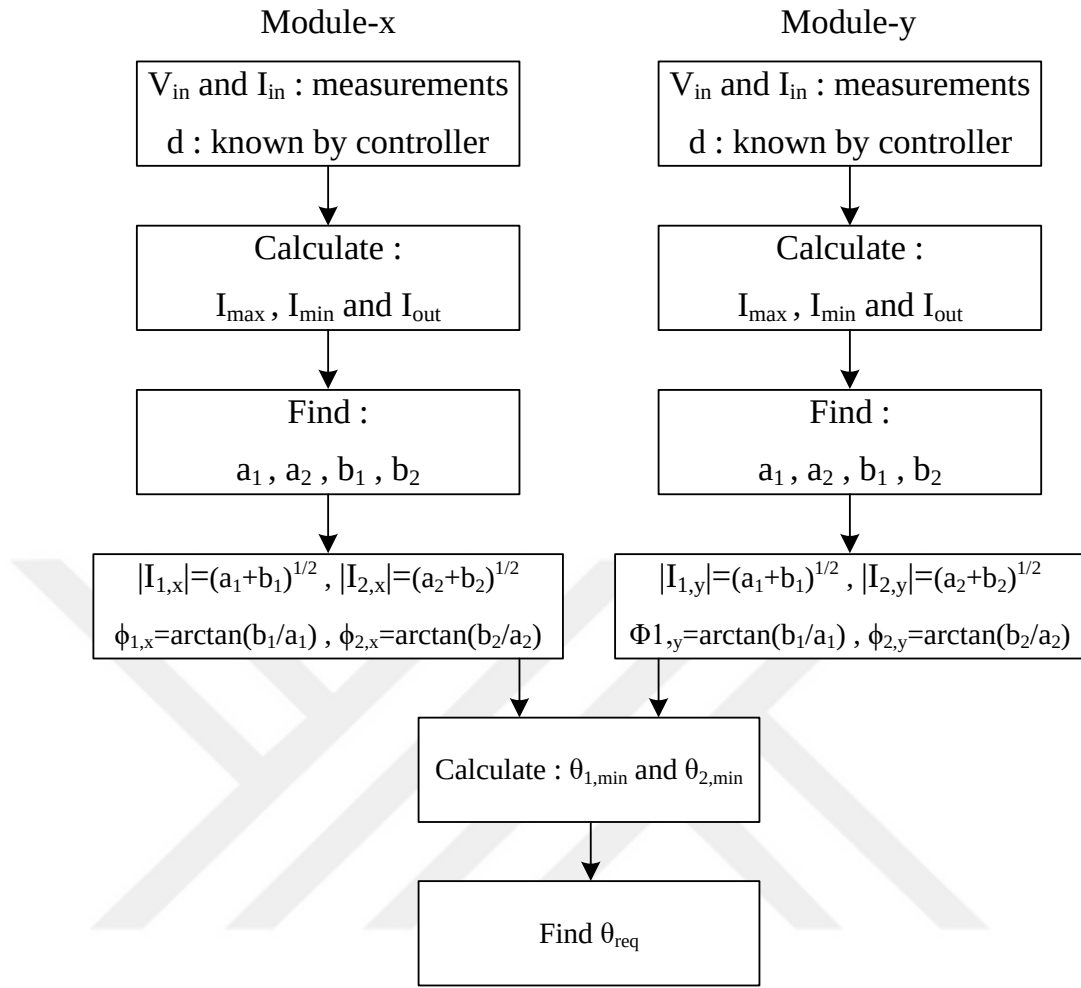


Figure 5.13: Harmonic minimization algorithm flowchart

$$\theta_{req} = \frac{\theta_{2,min}(|I_2(\theta_{1,min})|^2 - |I_2(\theta_{2,min})|^2) + \theta_{1,min}(|I_1(\theta_{2,min})|^2 - |I_1(\theta_{1,min})|^2)}{|I_1(\theta_{2,min})|^2 - |I_1(\theta_{1,min})|^2 + |I_2(\theta_{1,min})|^2 - |I_2(\theta_{2,min})|^2} \quad (5.18)$$

5.3.2.2 Interleaving of Three Modules

When the number of parallel converters is increased to three, a similar analysis can be followed to find the optimum angle that minimizes capacitor current. In Fig. 5.14, different approaches are again compared for a sample operation condition. Fig. 5.14.a

shows the case with $k = \infty$. Here θ_y corresponds to the phase shift of module-y with respect to module-x, and θ_z is the phase difference between module-z and module-x. Fig. 5.14.b is obtained using only the first harmonic of the capacitor current, whereas Fig. 5.14.c demonstrates the case with only the second harmonic. When the first and second harmonics are considered together, the resultant shape is given in Fig. 5.14.d. It is again clearly seen that using only the first harmonic is not well performed. Yet, the first two harmonics nearly overlap with the real capacitor current analysis. To find the total current minimizing angle, the same local minimum points should be found for the first and second harmonics, as explained in the previous part. $|I_1|^2$ and $|I_2|^2$ for three module operation is calculated by vector addition in (5.19) and (5.20) respectively. In the equations, θ_{iy} and θ_{iz} correspond to the initial phase difference of the first harmonic component of the module-y and module-z with respect to module-x. Similarly, θ_{2iy} and θ_{2iz} are the initial phase differences of second harmonics.

$$\begin{aligned}
|I_1|^2 &= |I_{1,x}|^2 + |I_{1,y}|^2 + |I_{1,z}|^2 + 2|I_{1,x}||I_{1,y}|\cos(\theta_y + \theta_{iy}) \\
&\quad + 2|I_{1,x}||I_{1,z}|\cos(\theta_z + \theta_{iz}) + 2|I_{1,y}||I_{1,z}|\cos(\theta_y + \theta_{iy} - \theta_z - \theta_{iz}) \\
|I_2|^2 &= |I_{2,x}|^2 + |I_{2,y}|^2 + |I_{2,z}|^2 + 2|I_{2,x}||I_{2,y}|\cos(2\theta_y + \theta_{2iy}) \\
&\quad + 2|I_{2,x}||I_{2,z}|\cos(2\theta_z + \theta_{2iz}) + 2|I_{2,y}||I_{2,z}|\cos(2\theta_y + \theta_{2iy} - 2\theta_z - \theta_{2iz})
\end{aligned} \tag{5.19}$$

$$\tag{5.20}$$

The local minimum of each harmonic component can be found by partial derivation. Furthermore, minimizing the addition of three vector quantities is simply achieved by forming a triangle if possible. If the vectors do not ensure triangle inequality, the phase shift of two small vectors should be 180° with respect to the largest one [64]. For triangle formation of first harmonic current, $\theta_{1y,min}$ and $\theta_{1z,min}$ are calculated in (5.21) and (5.22). Here, it should be noted that $\theta'_{1y,min} = 2\pi - \theta_{1y,min}$ and $\theta'_{1z,min} = 2\pi - \theta_{1z,min}$ will also minimize the vector addition by forming the symmetric triangle of the first one.

$$\theta_{1y,min} = \arccos\left(\frac{|I_{1,z}|^2 - |I_{1,x}|^2 - |I_{1,y}|^2}{-2|I_{1,x}||I_{1,y}|}\right) + \pi - \theta_{iy} \tag{5.21}$$

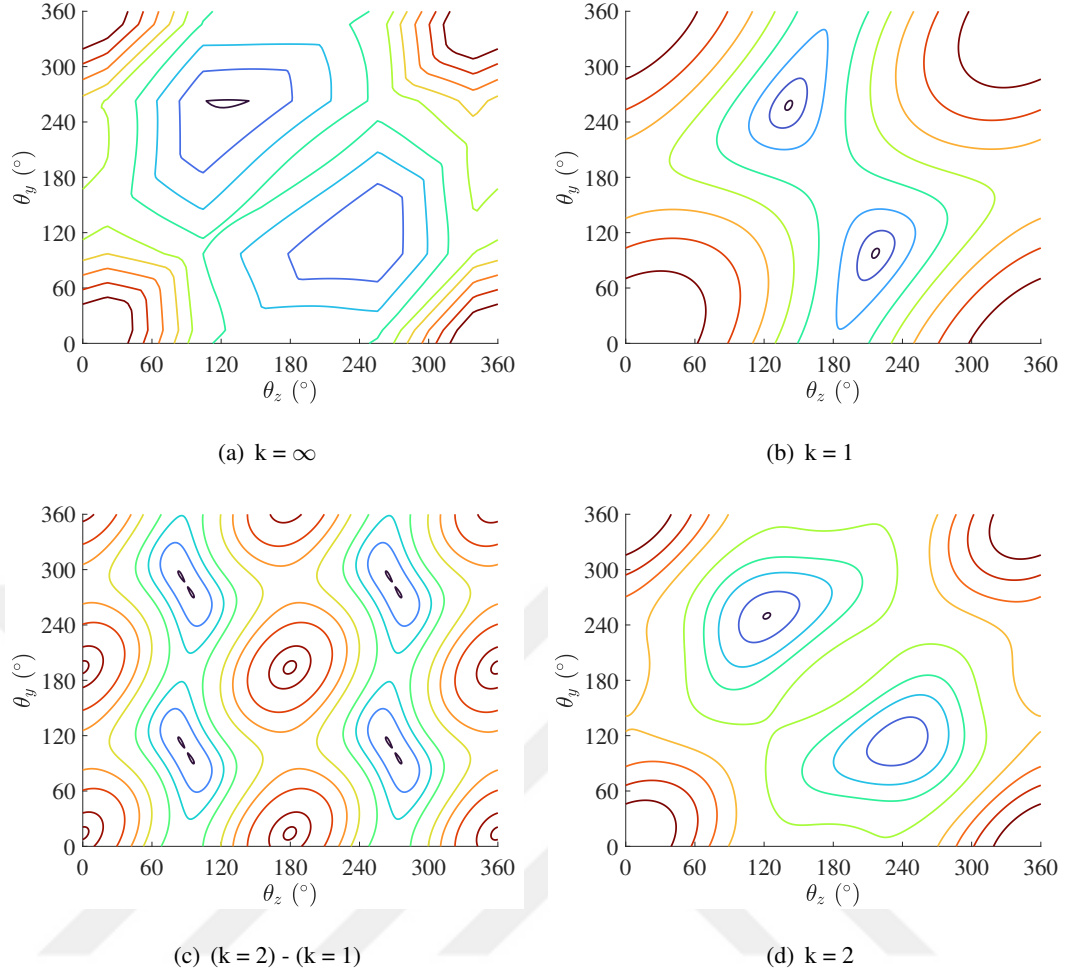


Figure 5.14: Comparison of the harmonic minimization algorithm for different harmonic orders

$$\theta_{1z,min} = \text{acos}\left(\frac{|I_{1,y}|^2 - |I_{1,x}|^2 - |I_{1,z}|^2}{2|I_{1,x}||I_{1,z}|}\right) - \theta_{iz} \quad (5.22)$$

For the second harmonic minimization, (5.23) and (5.24) gives the $\theta_{2y,min}$ and $\theta_{2z,min}$, which are the required phase shifts of module-y and module-z respectively. Similar to the first harmonic analysis, a symmetric triangle can be formed with $\theta'_{2y,min} = \pi - \theta_{2y,min}$ and $\theta'_{2z} = \pi - \theta_{2z,min}$. As also shown in Fig. 5.12, the second harmonic minimizing angle repeats at 180° .

$$\theta_{2y,min} = \frac{\arccos\left(\frac{|I_{2,z}|^2 - |I_{2,x}|^2 - |I_{2,y}|^2}{-2|I_{2,x}||I_{2,y}|}\right) + \pi}{2} - \theta_{2iy} \quad (5.23)$$

$$\theta_{2z,min} = \frac{\arccos\left(\frac{|I_{2,y}|^2 - |I_{2,x}|^2 - |I_{2,z}|^2}{2|I_{2,x}||I_{2,z}|}\right)}{2} - \theta_{2iz} \quad (5.24)$$

In summary, for the first harmonic minimization, there are two possible phase shifts. The number of potential phase shifts is eight for the second harmonic minimization. As two module analysis suggests, absolute minimum occurs around the local minimums, which are closest to each other. To find the absolute maximum, $|I_1|^2$ and $|I_2|^2$ are approximated with similar quadratic functions, however, in three dimensions this time. The approximated functions are given in (5.25) and (5.26), where k_1 and k_2 are the short forms of the multipliers in the equations.

$$\begin{aligned} I_{1,approx}^2(\theta_y, \theta_z) &= \frac{((\theta_y - \theta_{1y,min})^2 + (\theta_z - \theta_{1z,min})^2) |I_1(\theta_{2y,min}, \theta_{2z,min})|^2}{(\theta_{2y,min} - \theta_{1y,min})^2 + (\theta_{2z,min} - \theta_{1z,min})^2} \\ &= k_1((\theta_y - \theta_{1y,min})^2 + (\theta_z - \theta_{1z,min})^2) \end{aligned} \quad (5.25)$$

$$\begin{aligned} I_{2,approx}^2(\theta_y, \theta_z) &= \frac{((\theta_y - \theta_{2y,min})^2 + (\theta_z - \theta_{2z,min})^2) |I_2(\theta_{1y,min}, \theta_{1z,min})|^2}{(\theta_{2y,min} - \theta_{1y,min})^2 + (\theta_{2z,min} - \theta_{1z,min})^2} \\ &= k_2((\theta_y - \theta_{2y,min})^2 + (\theta_z - \theta_{2z,min})^2) \end{aligned} \quad (5.26)$$

In the final step, the minimal point of the sum of these functions is found by partial derivation. The required phase shifts are given in (5.27) and (5.28), which are the weighted averages of the previously found single harmonic minimization angles.

$$\theta_{y,req} = \frac{k_1\theta_{1y,min} + k_2\theta_{2y,min}}{k_1 + k_2} \quad (5.27)$$

$$\theta_{z,req} = \frac{k_1\theta_{1z,min} + k_2\theta_{2z,min}}{k_1 + k_2} \quad (5.28)$$

5.3.3 Experimental Verification of the Harmonic Reduction Algorithm

An experimental setup is built with the designed multi-string DC/DC converter PCB to verify the algorithm. However, the output capacitance of the converter is not present, as previously discussed. Hence, a DC-link capacitor PCB is utilized in the experiment, as shown in Fig. 5.15. The PCB has cutouts for current measurement, for which PEM-CWT rogowski current probe is used. The equipments used in the experiment are shown in Fig. 5.16.

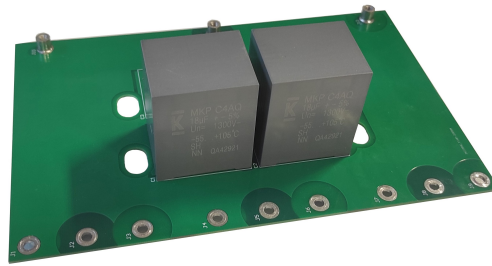


Figure 5.15: DC-link capacitor PCB

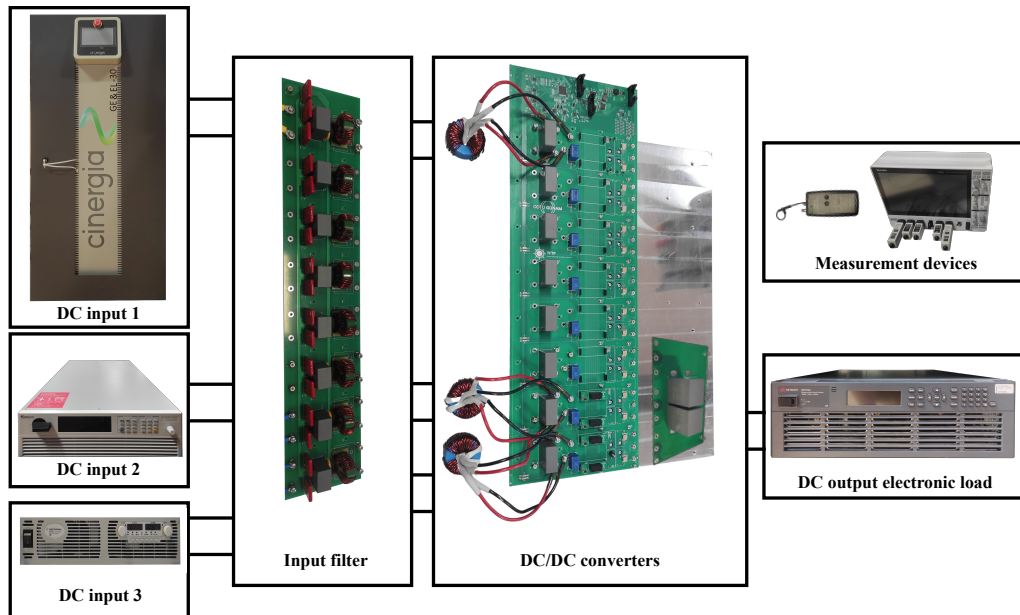


Figure 5.16: Equipmet used in the experimental verification of the interleaved operation

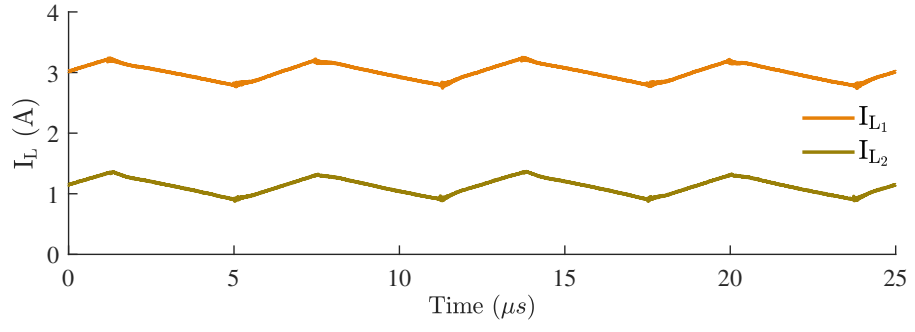
5.3.4 Verification with Two Modules

Firstly the algorithm was verified for interleaving of two DC/DC converters. The operation conditions of the experimental case are presented in Table 5.2. The inductor currents and the output capacitor current are presented in Fig. 5.20 without a phase shift. The shape of the capacitor current is similar to the expected waveform (Fig. 5.7) with the additional ringings. The reason behind the ringings is the layout inductance of the capacitor current path, which can be decreased by placing the capacitor closer to the semiconductor devices. However, to be able to measure the current, such configuration could not be implemented.

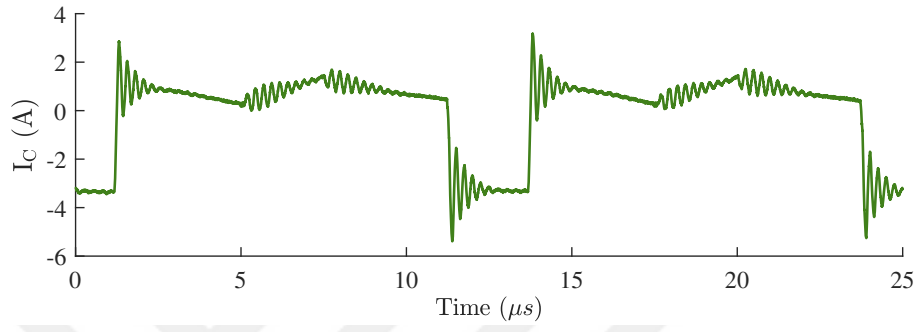
Table 5.2: Operation conditions of the sample experimental scenario

Parameter	Value
Output Voltage	140 V
Module-1 input voltage	115 V
Module-1 input current	2.98 A
Module-1 duty cycle	0.19
Module-2 input voltage	114 V
Module-2 input current	1.13 A
Module-2 duty cycle	0.2

In Fig. 5.18, the experimental result of the $I_{C,rms}$ values are plotted for all phase shift angles. Moreover, the suggestion of the algorithm is marked on the plot. It can be seen that the algorithm performs well and finds the current minimizing angle with a minor error. The current waveform of this case is presented in Fig. 5.19. It should be noted that the ringing of the capacitor current is not modeled analytically. However, the effect of these oscillations is shown in the $I_{C,rms}$ curve. The sudden changes in consecutive angles result from high-frequency oscillations, which can be minimized by decreasing the layout inductance.



(a) Inductor currents



(b) Output capacitor current

Figure 5.17: Circuit waveforms of the interleaved operation (No phase shift applied)

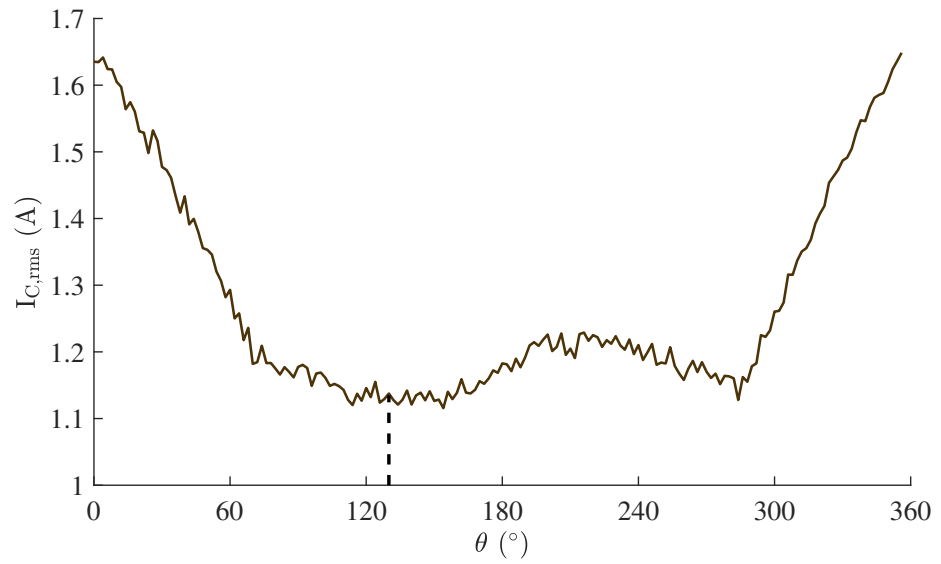


Figure 5.18: Change of $I_{C,rms}$ for different phase shift angles

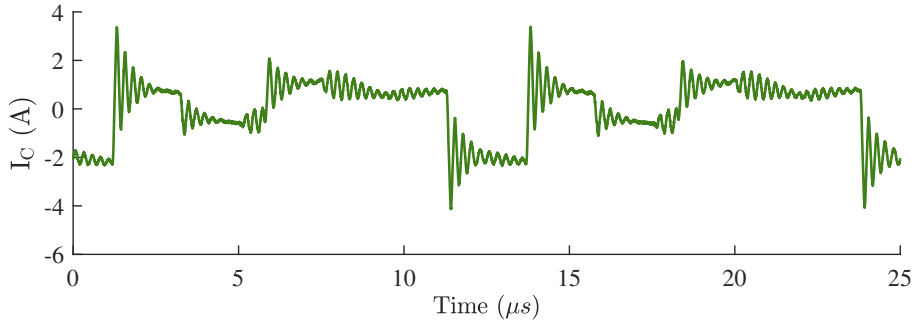


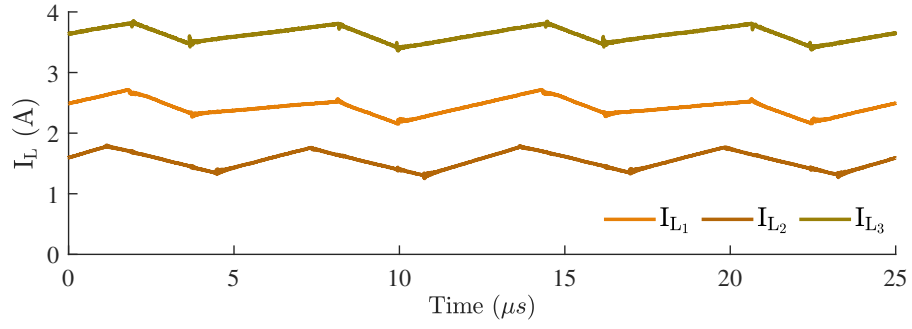
Figure 5.19: Output capacitor current for $\theta = 130^\circ$

5.3.5 Verification with Three Modules

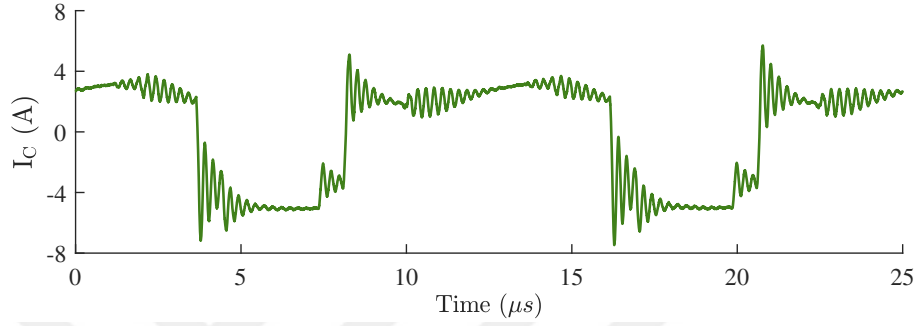
After the verification of the algorithm with the interleaving of two converters, the algorithm was tested with three parallel converters. The operating conditions of the converters are given in Table. 5.3. In Fig. 5.20, the current waveforms of the inductors and the output capacitor are presented when the converters are operated with no phase shift. The RMS of the capacitor current is 3.5 A.

Table 5.3: Operation conditions of the sample experimental scenario for interleaving of three modules

Parameter	Value
Output Voltage	140 V
Module-1 input voltage	92.8 V
Module-1 input current	2.5 A
Module-1 duty cycle	0.35
Module-2 input voltage	109.8 V
Module-2 input current	1.5 A
Module-2 duty cycle	0.23
Module-3 input voltage	91.7 V
Module-3 input current	3.48 A
Module-3 duty cycle	0.36



(a) Inductor currents



(b) Output capacitor current

Figure 5.20: Circuit waveforms of the interleaved operation with three modules (No phase shift applied)

Then, based on the experimental operating conditions, the harmonic minimization algorithm is applied, and required phase shifts are found as $\theta_y = 263^\circ$ and $\theta_z = 133^\circ$. To verify the result, θ_y is kept at 263° and θ_z is swept from 0° to 360° . Similarly, the θ_y is swept in the same range when $\theta_z = 133^\circ$. The results of these experiments are given in Fig. 5.21. In the figure, analytical $|I_c^{(\infty)}|^2$ change is also given for all possible θ_y and θ_z angles in the bottom left plot. The suggested angle pair is marked. The $I_{C,rms}$ values are presented for indicated phase shifts. The results show that the algorithm finds the minimum angle with a minor error of 1 to 2 degrees.

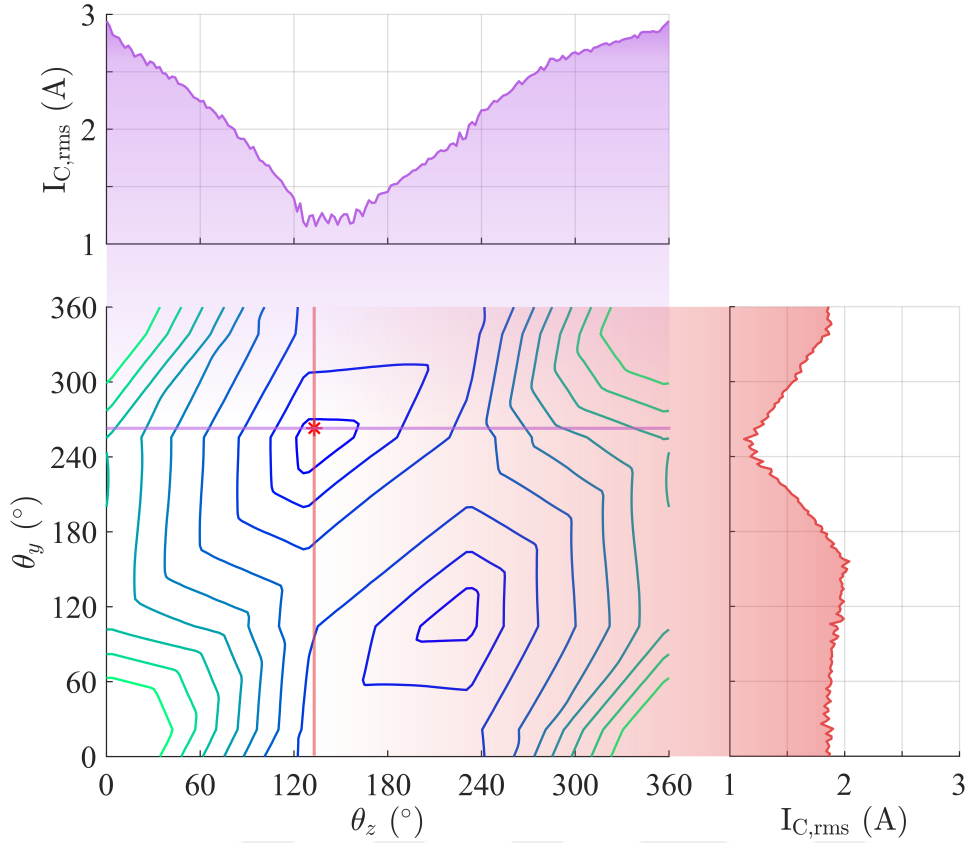
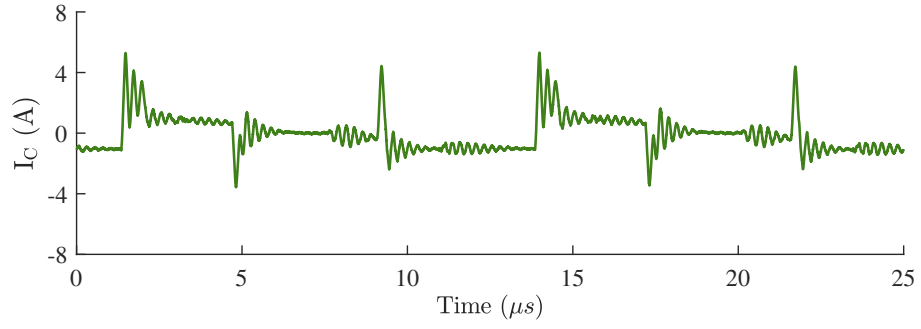


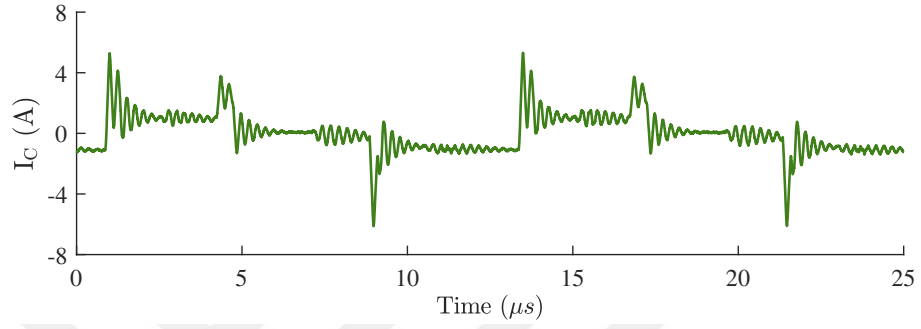
Figure 5.21: Analytical (bottom-left) and experimental (top and bottom-right) change of output capacitor current for three-module operation

Finally, the capacitor current waveform of the algorithm suggestion is observed and compared with conventional interleaving phase shift pairs in Fig. 5.22. All of the current magnitudes are smaller than the case with no phase shift (Fig. 5.20.b) as expected. However, due to the asymmetric conditions of the converters, the current RMS value is not minimized with equal phase shifts. It can be seen that the conventional cases are not equal either. The one closer to the algorithm-suggested phases is smaller than the other one. Yet, the RMS at the suggested point is smaller than both of the conventional cases.

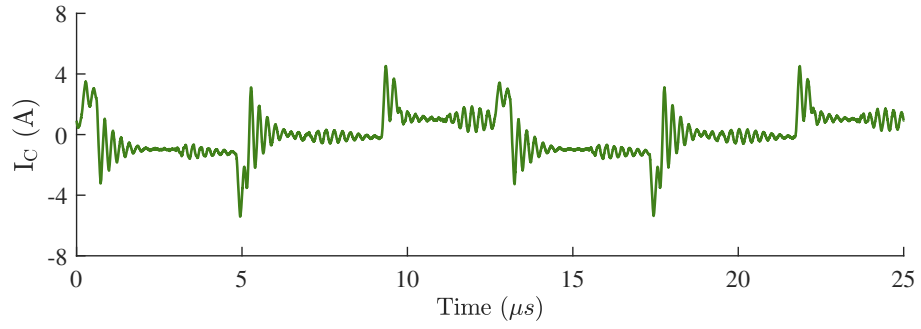
The capacitor current waveforms show the significance of the interleaving of converters. If the converters are operated simultaneously, the output currents are directly added up, and the capacitor current increases. However, when phase shift is applied between the converters, the current magnitude and the RMS start to decrease. In Section 3.5, it is shown that the RMS of the capacitor current plays an important role in



(a) $\theta_y = 263^\circ$ and $\theta_z = 133^\circ$, $I_{C,rms} = 1.15$ A



(b) $\theta_y = 240^\circ$ and $\theta_z = 120^\circ$, $I_{C,rms} = 1.29$ A



(c) $\theta_y = 120^\circ$ and $\theta_z = 240^\circ$, $I_{C,rms} = 1.32$ A

Figure 5.22: Output capacitor current waveforms for three-module interleaving

selecting the proper capacitor. Even though the capacitance value provides the voltage ripple requirement, the current rating might not be suitable. By implementing the interleaving concept, the high current demand of the capacitor can be handled. For the converters that are operated under asymmetric conditions, the proposed algorithm nearly finds the optimum point for the minimum capacitor current. If the algorithm is not used, the capacitor current can be decreased to 1.3 A_{RMS} for the experimental scenario, whereas the algorithm results in 1.15 A_{RMS} . For a tightly designed converter,

the decrease of 20% capacitor loss may result in significant lifetime extension. For example, if the sample experimental conditions are scaled to rated operating conditions, reducing 13 A_{RMS} to 11.5 A_{RMS} would decrease the temperature rise of capacitor to 15°C from 19°C of an adequately selected capacitor with a 15 A current rating [51]. As the temperature of the capacitor increases, the lifetime exponentially decreases. For the sample selected capacitor, the lifetime decreases to one-fourth for 10°C temperature increases. Hence, finding the optimal operation point helps to reduce failures caused by the capacitors.

5.4 Conclusion

In this chapter, the overall design of the multi-string inverter DC/DC stage is presented. A single DC/DC converter module is tested at 18 kW input power, and the circuit waveforms are observed. The new PCB layout is verified by the operation and waveforms under the most stressful conditions. Additionally, the new inductor is analyzed thermally. Lower temperatures are achieved compared to prototype tests presented in Chapter 4. Afterward, the interleaved operation of the DC/DC converters is analyzed for DC-link capacitor current ripple minimization. The conventional interleaving approach does not provide the best operation if the converter operating conditions are not the same. Hence, a new algorithm is presented that tries to minimize the first two harmonics of the capacitor current. The algorithm is verified by experimental results for sample operating conditions. By properly finding the interleaving phase shift, the capacitor current can be minimized, which can reduce the size of the capacitor. Alternatively, the size of the filter can be kept the same, but the losses of the capacitor can be decreased. Decreasing the losses and hence the temperature of a capacitor, its lifetime increases. In the first experimental case, the algorithm reduces the capacitor losses by 50% compared to the non-interleaving case and 10% for the conventional interleaving method. In the second experimental case with the three-module operation, capacitor losses decrease by 90% for the non-interleaving case, whereas the reduction in the losses is 20% compared to the conventional interleaving phases.

CHAPTER 6

CONCLUSIONS

In this thesis, the design of a three-level boost converter is investigated. The designed converter is to be used in the DC/DC stage of a multi-string inverter. The operation of the converter is analyzed analytically, and rated operating conditions are determined. Then, device and switching frequency selections are discussed for the aimed efficiency. Additionally, the control of the converter is analyzed. The designed converter is implemented and verified under different conditions. Then, the verified design is adapted for eight parallel converter operations. A novel interleaving algorithm is suggested to find the optimal phase shift between the converters in order to minimize the capacitor current. It is experimentally shown that proposed algorithm performs better than conventional methods and minimizes the capacitor current.

6.1 Outcomes and Discussions

Firstly, the operation of the 3L-BC is investigated, and it is shown that the MOSFETs and diodes are subject to half of the output voltage. Hence, compared to conventional boost converter, lower voltage-rated devices can be used which reduces the cost. To select the optimum MOSFET and diode, the loss analysis was performed among the SiC devices. The trade-off between the conduction and switching losses of the MOSFETs is examined. Devices with lower R_{DS} suffer from higher E_{OSS} , which results in higher switching losses. Hence, the losses of the available products are compared for different switching frequencies. As loss comparison suggests and having the best price, G3R40MT12K MOSFET is selected for the design. Similarly, the diode is selected by comparing the conduction losses, and IDWD30G120C5 is

selected. Based on the selected devices, the switching frequency of the converter is analyzed, and 80 kHz is selected. For these selections, the analytical semiconductor loss becomes 104 W at worst-case operation. Then, the magnetic design is performed for the inductor based on the calculations of the out-of-phase switching technique. Kool M μ cores, which provide lower losses and higher temperature operations, are compared for different inductor designs. Two of the most suitable options are presented, and the one with more available space for additional windings is selected. The last component of the converter is the output capacitors, whose selection is made according to voltage ripple and RMS current conditions.

For the designed converter, a prototype is implemented, and the operation is verified. The rated voltage operation of the converter is investigated for different input levels. It is shown that selected products are suitable for the operation. The designed PCB provides safe switching, and voltage transients do not cause improper situations. Although the measured losses are slightly higher than the analytical calculations, the efficiency requirement is achieved for all conditions.

In the converter analysis, it is shown that MOSFETs in the topology can be turned on simultaneously or with a 180° phase shift. The phase-shifted operation is superior to decrease the current ripple and the losses in the inductor. However, it is seen that in-phase switching eliminates the common mode voltage generation if the inductor windings are split into positive and neutral input lines. The comparison of the losses of common mode filter and boost inductor shows that in-phase switching results in better efficiency even if the current ripple is higher.

The other important point of the converter is the control algorithms. The voltage of the PV strings should be controlled for maximum power delivery. Hence, P&O MPPT algorithm is utilized to control the input voltage. The designed control loop is experimentally tested with a PV array simulator. The MPP operation is maintained by cascaded voltage and current loops while providing smooth and fast transitions. The second control algorithm is used to balance the output capacitors. Due to inverter modulation, the loads may be unbalanced, which results in unequal voltages in the capacitors. It is shown that capacitors can be balanced by applying uneven duty cycles to the MOSFETs. The required duty cycle difference is found by a PI controller. The

implemented controller provides fast and smooth transitions, and capacitors can be balanced.

Once the operation is verified, the topology is implemented for the eight-parallel converter design. With minor modifications, a more dense PCB layout is designed. According to the results of the experiments conducted by the first design, the boost inductor is renewed. The insulation thickness of the windings is increased so that inter-winding capacitance does not cause resonance. The copper area is kept as desired to decrease the inductor losses and the operating temperature. The new design is verified for rated voltage operation under worst-case operation. Safe operation is maintained, and inductor temperature is decreased as requested.

Then, the parallel operation of the DC/DC converters is investigated. In the literature, interleaving is studied for single input single input converters where the operating conditions of the converters are identical. However, multi-string inverter utilizes multiple PV inputs, which may have different I-V characteristics, and conventional interleaving does not provide optimal operation. Hence, a novel algorithm is presented to find the optimal phase shift between the converters to minimize the DC-link capacitor current, which reduces the capacitor losses and extends the capacitor life-time. Table 6.1 presents the literature comparison for different interleaving algorithms developed for similar asymmetric operations. The interleaving technique is used in different topologies for different reasons. It is seen that harmonic analysis and harmonic elimination is the most common method. However, the analytical solution exists only for the methods that are based on the first harmonic elimination analysis. If higher-order harmonics are also considered, the only way is the iterative solution. On the other hand, the proposed algorithm improves the previous harmonic analysis works and minimizes the first two harmonics where an analytical solution is presented. The proposed algorithm is proved for multi-input single-output three-level boost converters, and the output capacitor current is minimized. It is shown that the capacitor losses can be decreased by 20% compared to conventional interleaving methods, which increases the capacitor life-time.

Table 6.1: Literature comparison for interleaving of DC/DC converters operating in asymmetric conditions

Study	Topology	Aim	Method	Solution
[61]	single-input single-output buck-boost	to reduce output voltage ripple with inductor tolerances	first harmonic elimination	analytical
[62]	Single-input multi-output buck	to reduce input current ripple	first harmonic elimination	look-up table
[63]	Single-input multi-output buck	to reduce input current ripple under faulty conditions	first harmonic elimination	analytical
[64]	multi-input series output ripple buck	to reduce output current ripple	first harmonic elimination	analytical
[65]	multi-input single-output boost	to reduce capacitor current RMS	harmonic minimization up to desired order	iterative
[66]	multi-input single-output buck	to reduce output voltage ripple	first harmonic minimization	iterative measurement
[68]	multi-input single-output buck	to reduce output voltage ripple	time-domain	gate-logic
this study	multi-input single-output three-level boost	to reduce capacitor current RMS	first and second harmonic minimization	analytical

6.2 Possible Improvements and Future Work

In this thesis, the design of the 3L-BC is verified by several experiments. Yet, there are some points that can be further improved.

- The switching frequency of the converter is selected so that half of the total losses are generated by the semiconductor devices. Experimental measurements show that the efficiency of the converter is within the accepted range, and changes between 99.1% and 99.4% based on the operating conditions. However, the switching frequency can be further increased in the designed multi-string parallel-converter system if the converter is investigated with thermal results. This way, the load of filtering elements can be reduced. In the experiments, it is seen that the used cooling system is proper for a single-module operation. However, all of the converters and also the DC/AC stage should be operated under rated power for thermal results. Trying different switching frequencies in the finalized design, optimal frequency can be found.
- The designed converter is verified by experiments conducted with resistive load banks. To model the inverter operation and keep output voltage constant, an electronic load is connected to the output in relevant experiments. The operation of the converter should be verified with the DC/AC stage connected to the output.
- Common mode leakage analysis is performed for different inductor connections and switching schemes. Experimentally shown that used CM filter is not appropriate for out-of-phase switching scheme. A detailed CM analysis can be performed, and a custom CM filter can be designed. The thermal test can be repeated with the custom CM filter. It may be possible to decrease the total loss with the newly designed CM filter and out-of-phase switching scheme.
- The proposed interleaving algorithm is tested with two and three-module operations. The performance of the algorithm should be investigated for eight-module operation and compared with the conventional interleaving algorithm.



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