

A 600W ON-COIL CLASS-E RF POWER AMPLIFIER ARRAY WITH DYNAMIC PHASE CONTROL FOR 3T MRI

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By
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Phase Control for 3T MRI

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We certify that we have read this thesis and that in our opinion it is fully adequate,
in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

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Due to their size and cooling constraints, conventional Magnetic Resonance Imaging (MRI) places radio frequency (RF) amplifiers away from the scanner. These RF amplifiers have relatively low efficiency due to the matching of 50Ω output impedance for means of transmission with cables. Switching Class-E amplifiers on the other hand, by default need a bare RLC network as their load and thus can be directly integrated with the bare unmatched coils and reduce the cost and power losses significantly. This thesis aims to build up on the previous theses' line of work including [1, 2, 3, 4, 5]. Instead of mitigating the symptoms, chronic problems of artifacts have been fixed by focusing on their root causes in the FPGA side of the updated design. The driver has been updated, timing problems have been resolved. FPGA design is also extended to support multi-channel phase control.

A dual channel imaging configuration of on-coil Class-E amplifiers with on-the-fly digital fine phase control is presented for 3T MRI. The system can control the phase with less than 2° granularity (this setting can be fine-tuned down to 0.15°). Without any mechanical intervention with the coil setup, using merely phase control, illuminated slice depth is modulated to three times its base-size during scantime. B1 field maps are also extracted for another setup.

Periodically linear switching (PLS) circuit model of the Class-E amplifier is derived and computed, yielding a simulator with fast and customizable optimization capability. The PLS model is also verified by SPICE and theoretical analysis.

Keywords: MRI, Class-E amplifier, RF amplifiers, Parallel transmit array.

ÖZET

3T MRG İÇİN DİNAMİK FAZ KONTROLÜ ÖZELLİKLİ BOBİN-ÜZERİ 600W E-SINIFI GÜÇ YÜKSELTECİ DİZİSİ

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Manyetik Rezonans Görüntüleme (MRG), radyo frekansı (RF) yükselteçlerini boyutları ve soğutma kısıtlamaları nedeniyle tarayıcıdan uzağa yerleştirir. Bu RF yükselteçleri lineerdir ve kablolarla iletilmeleri için tipik 50Ω çıkış empedansına göre tasarlandıklarından dolayı nispeten düşük verimliliğe sahiptir. Öte yandan E-Sınıfı yükselteçler doğal olarak güç göndermek için RLC devre ağına ihtiyaç duyar ve bu sayede tipik bobinlerle (anahtar kilit uyumu gibi) doğrudan entegre edilebilir ve bu da güç kayıplarını ve maliyeti önemli ölçüde azaltır. Önceki tezlerin [1, 2, 3, 4, 5] üzerine kümülatif ilerleyen bu tezde güncellenen tasarımın FPGA tarafında artefaktlar, kronik sorunların semptomlarını hafifletmek yerine kök nedenlerine odaklanılarak giderildi. Transistör sürücüsü güncellendi, zamanlama sorunları çözüldü. FPGA tasarımı ayrıca çok kanallı faz kontrolünü destekleyecek şekilde genişletildi.

Bobin üstü çift kanallı E-Sınıfı yükselteçler için 3T MRG’de ince ayarlanabilen anlık dijital faz kontrolüne sahip bir tasarım sunulacaktır. Tasarlanan sistem, fazı 2° ’den daha hassas ayarlanabilirlik düzeyinde kontrol edebiliyor. Bobin kurulumuna herhangi bir mekanik müdahale olmaksızın, yalnızca faz kontrolü kullanılarak, görüntülen derinlik, tarama anında taban boyutunun üç katına kadar modüle edildi. B1 manyetik alan haritaları da başka bir deney ile çıkartılmıştır.

E-Sınıfı yükselteçlerin periyodik anahtarlama lineer (PAL) devre modeli türetilmiş ve bilgisayar ortamında hesaplanmıştır. Hızlı ve yüksek uyarlanabilirlikli optimizasyon yeteneğine sahip bir simülatör elde edilmiştir. PAL modeli ayrıca SPICE ve teorik analiz sonuçlarıyla karşılaştırmalı olarak doğrulanmıştır.

Anahtar sözcükler: MRG, E-sınıfı yükselteç, RF yükselteçler, Paralel vericiler.

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Chapter 1

Introduction

Magnetic resonance imaging (MRI) is a noninvasive imaging technique to image anatomy and the physiological processes of the body. MRI uses a powerful magnet in combination with gradient and RF coils. Gradient and RF coils need to be driven by amplifiers. Driving RF amplifiers poses a problem as the proximity of these coils to the strong magnetic field in the MRI bore makes the cooling on them extra challenging and costly. To circumvent this, conventional MRI places the RF amplifiers either in a secondary system room or inside the scanner room, outside the bore. In either case (although cables and cable-induced losses are generally smaller in the latter case), distancing between the amplifier and the body coil requires cabling and additional matching networks to the intrinsic impedance of the cables. Moreover, cable losses introduce additional stress and cost to the system. Class-E amplifier which needs an RLC network as its load simplifies this by removing intermediate matching circuits, which greatly simplifies the job to nothing but placing a switch and a choke inductor on the coil's terminals.

At ultra high field ($>7\text{T}$), transmit array systems (pTx) [6, 7, 8] become the only option due to tightening constraints such as increased attenuation due to decreasing wavelength. One novel design approach uses controlling channel amplitudes and phases in real time to modify the B1 field inside the subject. This proved useful in MR safety applications where we want RF fields to avoid certain

areas with implants. On the other hand, it also proves useful in correcting B1-field non-uniformities in large organs such as the heart [9]. One method to achieve such field modifications is to introduce interchannel phase delays to achieve a “steering” of the B1 field within the subject [10].

Several novel designs using switch-mode on-coil Class-D amplifiers have been proposed [11, 12, 13], and proved highly power efficient. To further reduce the costs and complexity, this thesis proposes Class-E amplifiers (which are basically Class-D amplifiers cut in half at the axis of symmetry). Without any intermediate matching networks, with the coil itself being part of the matching network. This integration, combined with the Class-E topology, further projects to reduce the cost, complexity and area of the design by more than half.

The precursors of this work was started and mostly formed its backbones by [1] for a 100W design with high efficiency using supply modulation. Next, the power output capability is further increased to 300W (at the cost sacrificing some performance at 3T) with a larger transistor by [2]. Furthermore, eliminating the need for supply modulation [3] a purely gate modulated design has also been proposed at 1.5T. Although in the latter, the efficiency takes a hit at high-power outputs, the dynamic range of the amplifier has increased. Finally [4] detailed the optimization with a simplified discrete time numerical model for quad-channel coupled Class-E amplifiers and expanded the concept to (closer to real-life application with coil distancing) a quad-channel imaging under full stress on the amplifiers. Work in [5] further extended the quad-channel numerical model to generalized n-channels and focused on gallium-nitride (GaN) HEMT transistors. In collaboration, also with my help in simplifying the earlier (and faulty) gate driver topology by more than half through the use of a dedicated transistor driver instead of an obsolete half-bridge, the costs have further been decreased while the driver’s performance more than doubled.

The work in this thesis is organized as follows. Chapter 2 will detail the theory of class-E amplifiers, their optimization process, the analytical solution of fields arising from the 2-channel loop setup, and the used B1 field estimation method. In Chapter 3 methods used for B1 field mapping and its modification, updates,

fixes and improvements to the design will be given. In Chapter 4 results using the methods of Chapter 3 and the analysis and comparison with the earlier designs in line of this work will be detailed. In concluding Chapter 5, the complications noted during the design steps and the goals of the future work will be discussed.



Chapter 2

Theory

2.1 The Class-E amplifier

The following section will detail the theoretical analysis in the literature. Simplified design equations will be extracted as the final step used to determine the starting points of tuning of the amplifier.

2.1.1 Background

Proposed by Sokal and Sokal [14], its analysis expanded by Raab [15, 16], Class-E power amplifiers can have theoretical efficiencies up to 100%. As with the simplified switch model, the topology of the Class-E amplifier can be found in Fig. 2.1, The amplifier is composed of a parallel capacitor (C_p or also known in literature as C_1 or C_{sh}), a choke inductor (L_{ch}), a supply voltage (V_{dd}), and a load network which includes a series resonator (L_s - C_s or also known in literature as the pair of L_2 - C_2) and a load resistor (R_L). The main exploit for us here is that our load network in MRI is already an RLC network, with impedances very close to perfect match for a Class-E amplifier with only minor modifications.

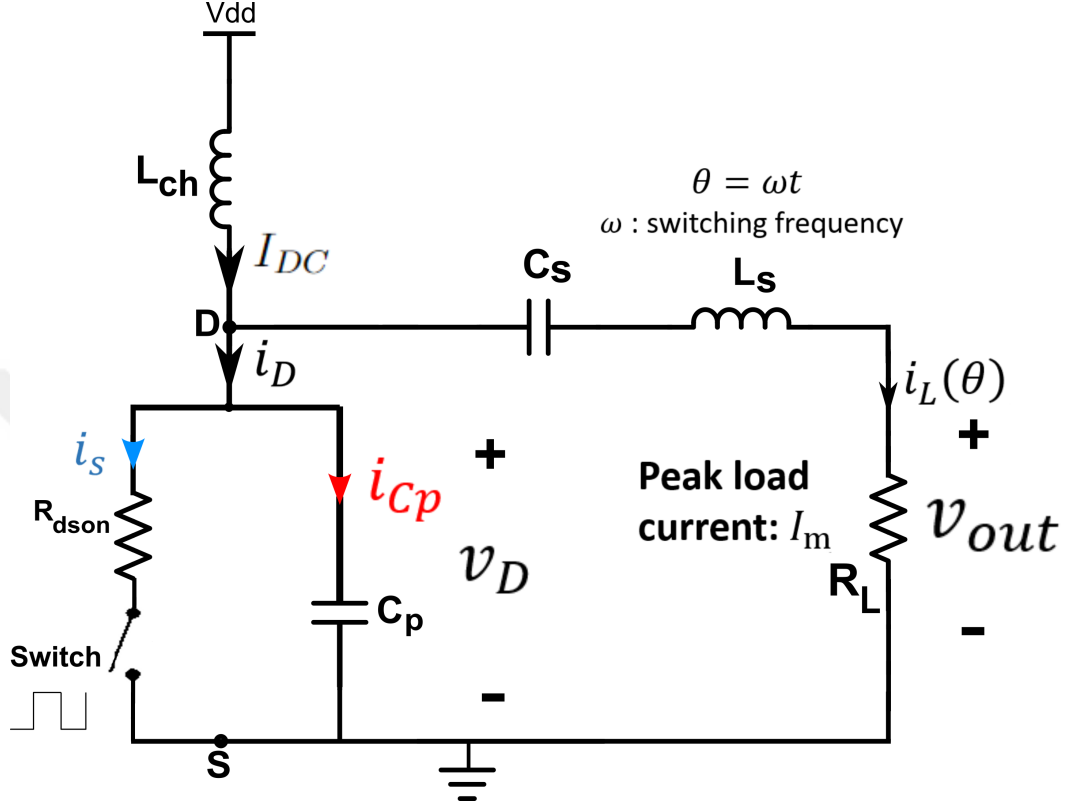


Figure 2.1: Class-E amplifier circuit. The switch is a MOSFET. In this abstraction, the sum of capacitances of switch MOSFET (C_{oss}) and the additive matching parallel capacitor is represented as a single C_p capacitance

We can start by defining a unitless variable representing time, and call it θ ($= \omega t$). For the following analysis of the circuit in Fig 2.1, since they are in parallel, we can use parallel capacitor voltage and switch voltage interchangeably as v_D (named after drain voltage v_D for a typical MOSFET switch). The waveform set of the ideal Class-E amplifier is given in Fig. 2.2. In the steady state assumption for Class-E amplifier operation for a sufficiently large choke inductance, I_{Lch} will converge to a DC value I_{DC} . i_D is defined as the sum of the currents going into C_p and the switch.

$$i_D = i_S + i_{Cp} \quad I_{DC} = i_D(\theta) + i_L(\theta) \quad (2.1)$$

As we will see later, the load current $i_L(\theta)$ can be defined as a sinusoid with amplitude I_m and phase ϕ to hold all boundary conditions.

$$i_L(\theta) = I_m \sin(\theta + \phi) \quad (2.2)$$

Next, the 50% duty ratio case will be detailed below. For the solution, we separate the waveforms into two parts as switch OFF and switch ON and combine them in the middle ($\theta = \pi$) ZVS (for maximum efficiency) and ZVDS (capacitor C_p voltage continuity) boundary conditions. While the switch is OFF, switch current is 0. Combining Eq. 2.1 and Eq. 2.2, we have Eq. 2.3 for i_{Cp} .

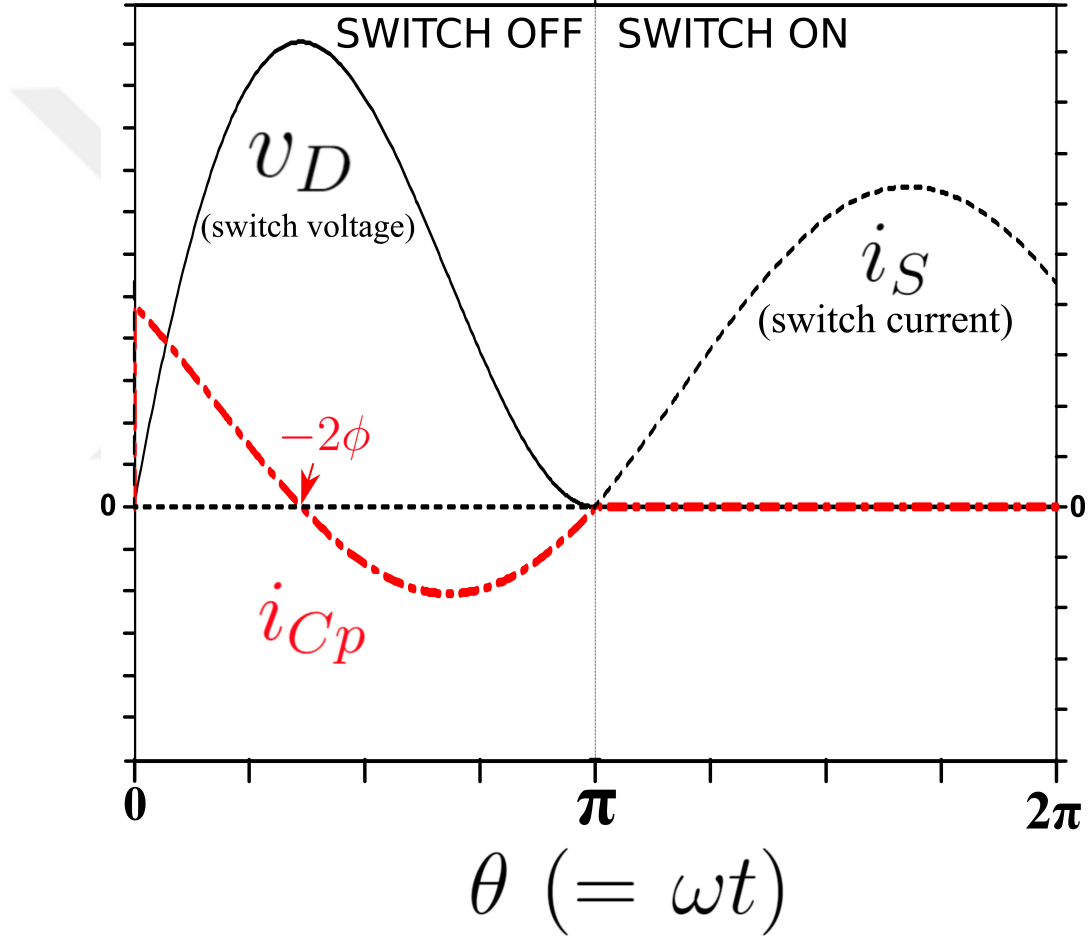


Figure 2.2: The switch voltage (solid), switch current (dashed), and parallel capacitor current (red dash-dot) of an ideal Class-E amplifier

$$i_{Cp}(\theta) = I_{DC} - I_m \sin(\theta + \phi) - 0 \quad : \quad \text{SWITCH OFF} \quad (2.3)$$

While the switch is ON, the switch voltage will stay at zero for the ideal amplifier. As necessitated by load waveform and ZVDS condition, the switch current must follow the path of parallel capacitor current from the first part's Eq. 2.3. For the

ideal amplifier, among these three waveforms only the switch current i_S will be non-zero in this interval:

$$i_S(\theta) = I_{DC} - I_m \sin(\theta + \phi) - 0 \quad : \quad \text{SWITCH ON} \quad (2.4)$$

Continuing the switch OFF case, writing out the parallel capacitor voltage(= $v_{Cp} = v_D$) as the integral of its current we get Eq. 2.5 (For the perfectly ideal Class-E amplifier where $R_{dson} = 0$, the capacitor voltage v_D should start from 0V at $\theta = 0$ and end at 0V at $\theta = \pi$, for 50% duty ratio solution). This means $v_D(0) = 0$ for the ideal Class-E amplifier.

$$v_D(\theta) = v_D(0) + \frac{1}{C_p} \int_0^\theta i_{Cp}(\theta') \frac{1}{\omega} d\theta' \quad (2.5)$$

Plugging Eq. 2.3 into Eq. 2.5, we finally have Eq. 2.8:

$$v_D(\theta) = v_D(0) + \frac{1}{C_p} \int_0^\theta (I_{DC} - I_m \sin(\theta' + \phi)) \frac{1}{\omega} d\theta' \quad (2.6)$$

$$v_D(\theta) = v_D(0) + \frac{1}{\omega C_p} \left\{ I_{DC} \theta' + I_m \cos(\theta' + \phi) \right\} \Big|_{\theta'=0}^{\theta'=\theta} \quad (2.7)$$

$$v_D(\theta) = v_D(0) - \frac{I_m}{\omega C_p} \cos(\phi) + \frac{I_{DC}}{\omega C_p} \theta + \frac{I_m}{\omega C_p} \cos(\theta + \phi) \quad (2.8)$$

Eq. 2.8 denotes the interesting shape of the switch voltage (drain voltage). It has a DC term $v_D(0) - \frac{I_m}{\omega C_p} \cos(\phi)$, a ramp term $\frac{I_{DC}}{\omega C_p} \theta$, and a sinusoidal term $\frac{I_m}{\omega C_p} \cos(\theta + \phi)$. The behavior of these terms at the boundary (verge of switching) will be of interest. For a smooth switching, which is necessary to avoid a singularity in parallel capacitor current (any excess voltage over 0V would have been immensely discharged into $R_{dson} = 0$ -singularity in capacitor current-) v_D must reach zero at the $\theta = 2\pi D$ point (ZVS) which is $\theta = \pi$ for D=50%. Moreover the first derivative of the switch voltage which also characterizes the capacitor current should also be smoothly reaching zero (ZVDS). This is to satisfy a continuous flow of sinusoidal current into the load, since as asserted before in connection with steady state choke current, the switch current and capacitor current combined should be the DC shifted version of the load current.

Applying the ZVS and ZVDS conditions on $v_D(\theta)$ at $\theta = 2\pi D$, we have Eq. 2.9 and 2.10.

$$v_D(\theta) \Big|_{\theta=2\pi D} = 0 = v_D(0) + \frac{2\pi D I_{DC}}{\omega C_p} + \frac{I_m}{\omega C_p} \left(\cos(2\pi D + \phi) - \cos(\phi) \right) \quad (2.9)$$

$$\frac{dv_D(\theta)}{d\theta} \Big|_{\theta=2\pi D} = 0 = \left\{ \frac{I_{DC}}{\omega C_p} - \frac{I_m}{\omega C_p} \sin(\theta + \phi) \right\} \Big|_{2\pi D} = \frac{1}{\omega C_p} \left(I_{DC} - I_m \sin(2\pi D + \phi) \right) \quad (2.10)$$

Subsequently, for $D=50\%$, we have Eq. 2.11 and 2.12 ($\sin(\pi + \phi) = -\sin(\phi)$ and $\cos(\pi + \phi) = -\cos(\phi)$).

$$0 = v_D(0) + \frac{1}{\omega C_p} \left(\pi I_{DC} - 2I_m \cos(\phi) \right) \quad (2.11)$$

$$0 = \left\{ \frac{I_{DC}}{\omega C_p} - \frac{I_m}{\omega C_p} \sin(\theta + \phi) \right\} \Big|_{2\pi D} = \frac{1}{\omega C_p} \left(I_{DC} + I_m \sin(\phi) \right) \quad (2.12)$$

Using Eq. 2.12 irrespective of ideality of switch we have found a distinct relationship between choke current I_{DC} and load sinusoidal current amplitude I_m as Eq. 2.13

$$\frac{I_{DC}}{I_m} = -\sin(\phi) \quad (2.13)$$

Note that angle solution for angle ϕ is negative. Using Eq. 2.13 with we can acquire another additional boundary condition at the end of the cycle $\theta = 2\pi$.

$$i_S(2\pi) = I_{DC} - I_m \sin((2\pi) + \phi) = I_{DC} + I_{DC} = 2I_{DC} \quad (2.14)$$

Moreover, combining Eq. 2.13 with Eq. 2.11 and boundary condition $v_D(0) = v_D(2\pi) = i_S(2\pi)R_{dson} = 2I_{DC}R_{dson}$ (which follows from Eq. 2.14), we get an exact expression for the ratio of $\cos(\phi)$ and $\sin(\phi)$ which gives an exact solution for $\tan(\phi)$ and the angle ϕ itself.

$$-\omega C_p v_D(0) = -\omega C_p 2I_{DC}R_{dson} = \left(\pi(-I_m \sin(\phi)) - 2I_m \cos(\phi) \right) \quad (2.15)$$

$$2\omega C_p R_{dson} \frac{I_{DC}}{I_m} = -2\omega C_p R_{dson} \sin(\phi) = \left(\pi \sin(\phi) + 2 \cos(\phi) \right) \quad (2.16)$$

Rearranging terms

$$\frac{\sin(\phi)}{\cos(\phi)} = \tan(\phi) = -\frac{2}{\pi + 2\omega C_p R_{dson}} \quad (2.17)$$

$$\phi = \arctan \left(- \frac{2}{\pi + 2\omega C_p R_{dson}} \right) \quad (2.18)$$

For the special case of ideal switch with $R_{dson} = 0\Omega$ Eq. 2.18 collapses into its well-known specific value for D=50% case.

$$\phi = \arctan \left(- \frac{2}{\pi} \right) \approx -32.48^\circ \quad (2.19)$$

As for the DC input current to sinusoid output current conversion ratio, following Eq. 2.13 we have Eq. 2.21:

$$-\sin(\phi) = -\sin \left(\arctan \left(- \frac{2}{\pi} \right) \right) = \frac{2}{\sqrt{\pi^2 + 4}} \quad (2.20)$$

$$\frac{I_m}{I_{DC}} = -\operatorname{cosec}(\phi) = \frac{\sqrt{\pi^2 + 4}}{2} \approx 1.862 \quad (2.21)$$

For 50% duty ratio solution, the optimum load angle of the RLC coil load network (ratio of real part of tuned load to its imaginary part) can be found by utilizing in-phase and quadrature (I,Q) component analysis. In (I,Q) domain, dividing the total coil current (load current, as a complex number, written as sum of (I,Q) components) to the total voltage of the branch (drain voltage, again as a complex number representing (I,Q) components), one can find the total coil impedance for this optimum solution. Following the analysis in [17], we have Eq. 2.22 for the optimum-efficiency load angle, and Eq. 2.23 for the optimum-efficiency X_{C_p} reactance for the 50% duty ratio case.

$$Z_{coil} = X_{C_p}(0.1836 + 0.2116j) = R_L + j\omega L_s + \frac{1}{j\omega C_s} \quad (2.22)$$

$$X_{C_p} = \frac{1}{\omega C_p} = \frac{R_L}{0.1836} \quad (2.23)$$

As stated in Eq. 2.23 for a given load resistance direct mapping to the C_p parallel capacitor value. After we calculate C_p , having a fixed L_s of the manufactured coil final step is to adjust C_s value such that Eq. 2.24 is also satisfied.

$$X_{L_s} - X_{C_s} = \omega L_s - \frac{1}{\omega C_s} = \frac{0.2116}{\omega C_p} \quad (2.24)$$

For example, a coil with $R_L \approx 1.22\Omega$ (further away the phantom load, the smaller the real part of load) as in Sec. 3.4.1, will need $C_p \approx 194\text{pF}$ and $Z_{coil} \approx 1.22 + 1.40j\Omega$ coil impedance.

2.1.1.1 Non-Ideal Switch Theory

The extra steps leading to the following equations will be skipped and can be found in [18] for general duty cycles. For a non-ideal switch, at 50% duty ratio the power dissipated on the switch [18] compacts into the form in 2.25.

$$P_{R_{dson}} = 1.37 \frac{R_{dson}}{R_L} P_{out} \quad (2.25)$$

$$\eta = \frac{1}{1 + 1.37 \frac{R_{dson}}{R_L}} 100\% \quad (2.26)$$

In the non-ideal case, angle ϕ becomes dependent on R_{dson} and the shunt capacitor C_1 . As detailed by the theory in [19] we have the following equation for ϕ

$$\phi = \arctan \left(\frac{-2}{\pi + 2\omega R_{dson} C_p} \right) \quad (2.27)$$

which for $R_{dson} = 0$, converges to $\phi = \arctan(\frac{-2}{\pi}) = -32.48^\circ$ ideal case value as expected. It is important to note that for this special ideal case the phase shift ϕ becomes independent of all other circuit components.

For the non-ideal case, voltage and current waveforms of a generic case is given in Fig. 2.3. Examining the waveforms for this tuned case, total current bypassing the load $i_s + i_{C1}$ complement each other and they effectively form a DC up shifted sine wave (unnoticeable ripple for a sufficiently large L_{ch}). This DC shift is still equal to the choke current.

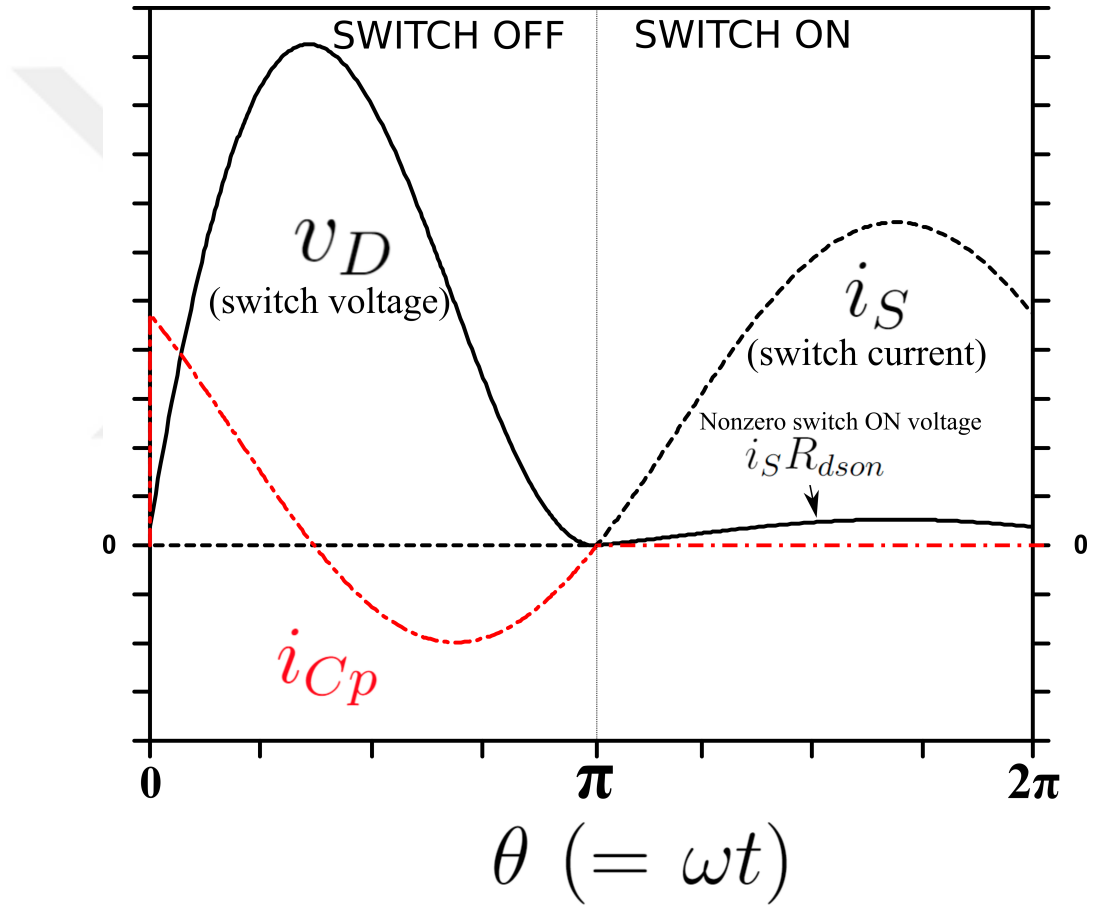


Figure 2.3: Switch voltage (black solid line), switch current (black dashed line), and the parallel capacitor voltage (red dash-dotted line) of the non-ideal Class-E amplifier ($R_{dson} \neq 0$)

2.1.1.2 Summary of The Line of Work up to Now

The diagram of the architecture that has been started by [1], and cumulatively building up until now is summarized in Fig. 2.4, where the coil and the amplifier integration is also depicted. The coil uses distributed capacitors to achieve high quality factors (Q-factors) [20, 21]. The supply modulation block of the original design is given in Fig. 2.5. Specifically, the gate driver block (and its errors) will be investigated under Sec. 2.6 in Fig. 2.11. The transistors (except the introduction of GaN transistors) used and their parameters of interest are summarized in Table 2.1. More details on the system blocks can be found in [1, 2, 3].

Characteristic Parameters	BLF871	BLF573
Bandwidth(MHz)	870	225
Output Power (W)	100	300
Drain-Source On Resistance R_{dson} (m Ω)	210	90
Feedback Capacitance C_{rs} (pF)	1	2.3
Input Capacitance C_{iss} (pF)	95	300
Output Capacitance C_{oss} (pF)	30	103
Maximum V_{DS} (V)	89	110
Threshold Voltage (V)	2	2
Operating Frequency (MHz)	123.24	63.78

Table 2.1: Transistors of interest and their important parameters

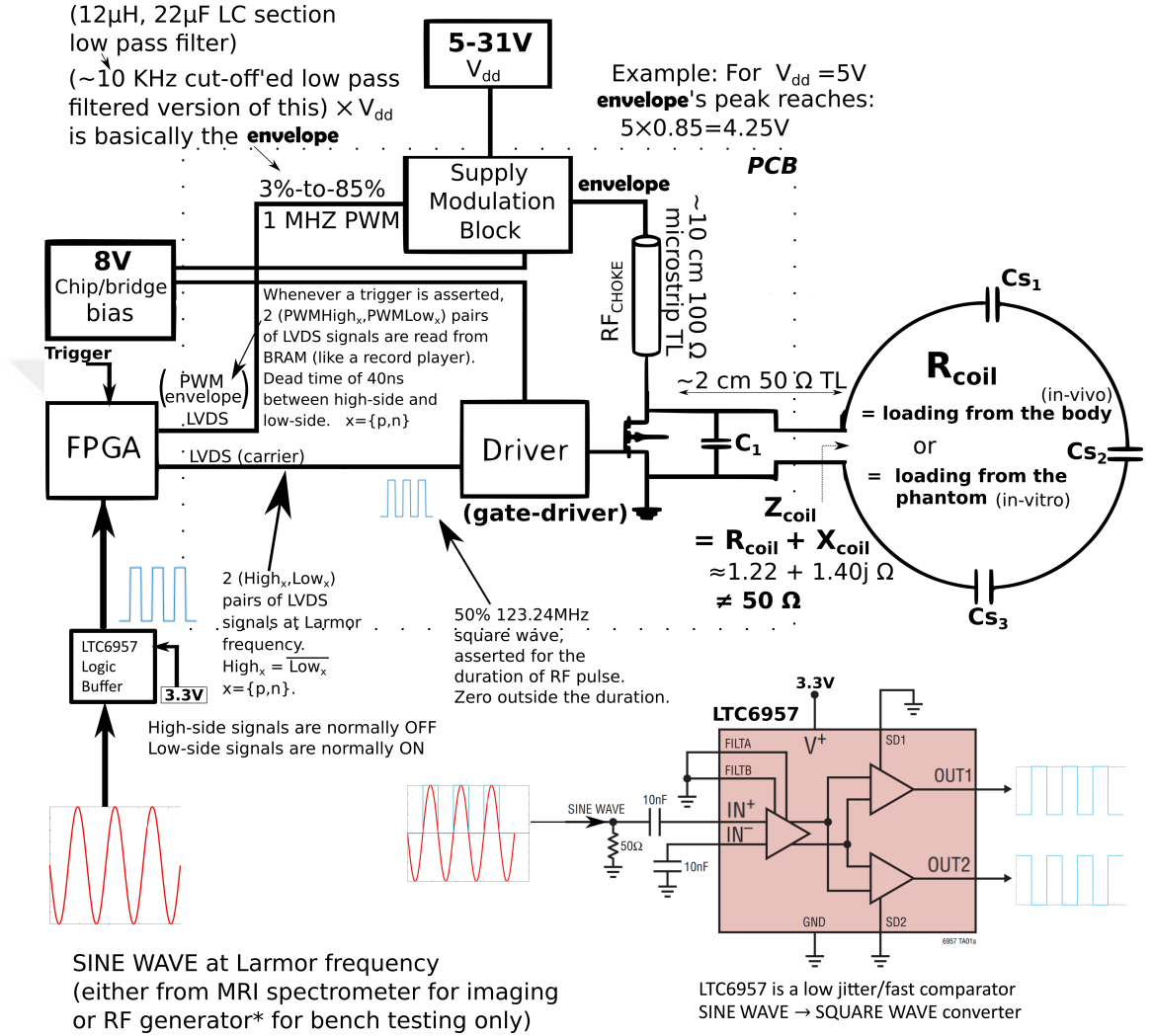


Figure 2.4: Summary of the architecture of the on-coil Class-E amplifier integration into the RF-chain. This is to recall the basic blocks and their functions. Dotted lines represent the edges of the PCB. Main MOSFET was either BLF871 or BLF573 detailed in Table 2.1. The trigger is asserted high and stays high during the RF pulse, and it is either active high (Left-side X9 Port of Siemens 3T TIM TRIO Scanner), or active low (Scimedix 1.5T Scanner) depending on the vendor. Coil impedance value of $1.22 + 1.40j \Omega$ is an example typical coil impedance value valid for the new coil tuned in Fig. 3.3. The transmission line (TL) effect (non-lumped) of ≈ 2 cm 50Ω TL segment from coil edge to amplifier drain will be first discussed here in Sec. 3.4.1. The block of Supply Modulation will further be detailed in Fig. 2.5. The block of gate-driver and its inherent errors will be discussed in Fig. 2.11 (part of the update sections). Up until now, the external RF generator* was not yet integrated as part of MR imaging (heavy artifact presence was noted) and was used only for bench testing. Credits for LTC6957 board diagram: Analog Devices, Inc.

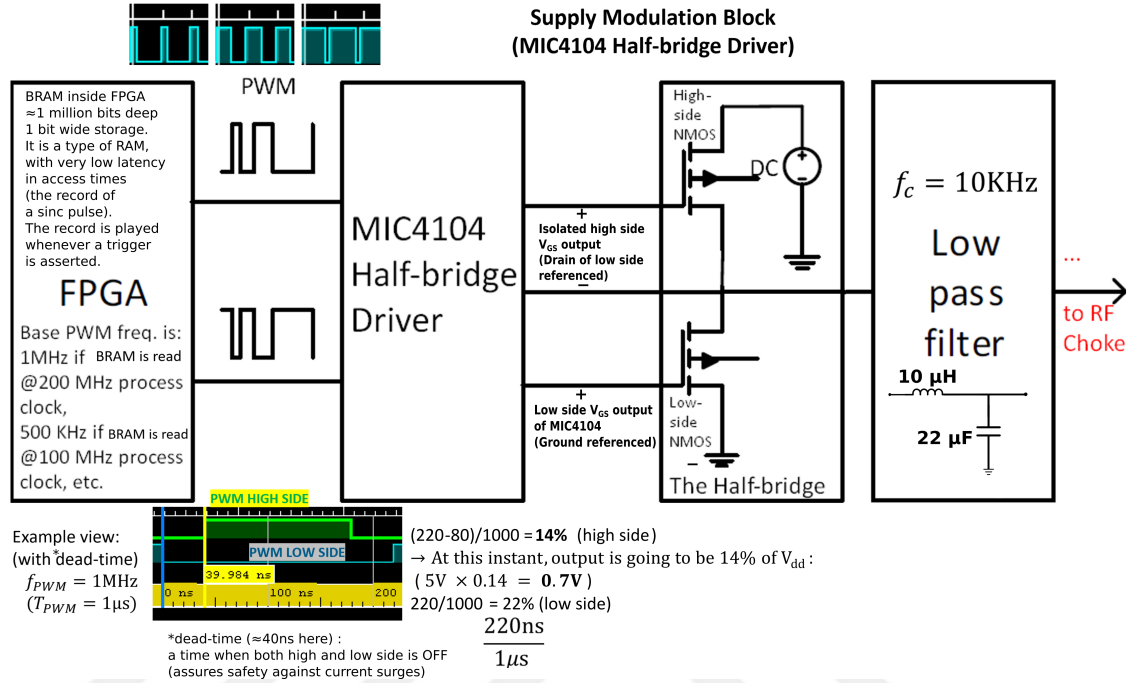


Figure 2.5: Summary of the the supply modulation block diagram for the designs used up to now in the line of this work

2.1.2 Nonlinear Drain Capacitance

Previously on the line leading to this work (summarized in Fig. 2.4), we had modeled the drain capacitance as the parallel combination (sum) of two constant capacitances ($C_1 + C_{oss} = C_p$). Capacitance that the designer externally introduces is modeled as C_1 and the output capacitance (C_{oss}) of the drain of the MOSFET transistor is also modeled as a linear capacitance independent of voltage. But, in general, depending on the operating drain-source voltage, C_{oss} can be heavily voltage dependent [22] (especially near low V_{DS} voltage regime). Quoting the datasheet of the BLF573 (Ampleon, Nijmegen, Netherlands) MOSFET [23], we have the following voltage dependance given in Fig. 2.6. Using this model, we apply a two-term exponential function fit by using MATLAB's (Mathworks, MA, USA) curve fitting toolbox. The result is a reasonable root mean square error (RMSE=10pF). The good thing about having a functional dependance is that, we can than easily employ this data with minimal number of terms in SPICE,

as LTSPICE (LTspice IV, Analog Devices, MA, USA) allows entering nonlinear capacitances by defining the charge (Q) as a function of voltage across its terminals similar to our example case given in Eq. 2.28 (with corresponding constants with units to adjust units).

$$Q = 10^{-12} \times \left(C_1 V - \frac{1.578}{4.06} e^{-4.06V} - \frac{142}{0.1977} e^{-0.1977V} \right) \quad (2.28)$$

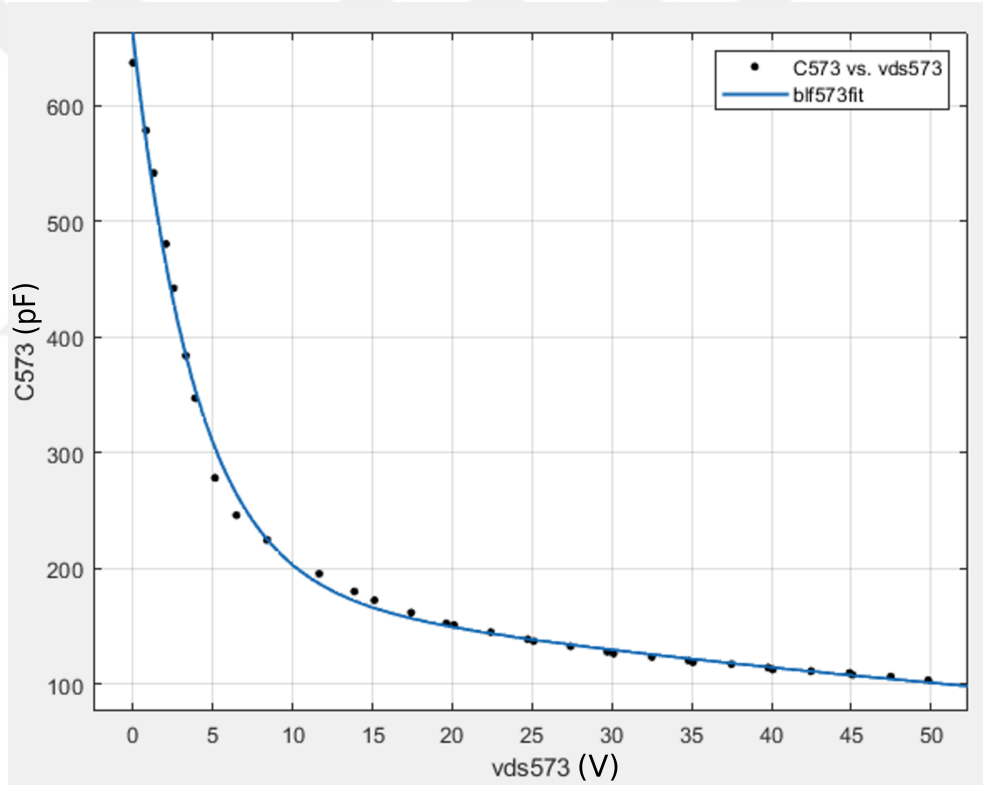


Figure 2.6: (Black dots) Data of C_{oss} output ($C_{ds} + C_{gd}$) capacitance of BLF573 and its two-term exponential curve fit (blue curve) in the range of (0-50V). This fit resulted in a 10pF RMSE error.

2.2 The Periodically Switched (Pseudo-)Linear Model of Non-Ideal Class-E Amplifier

The so-called Augmented Time Invariant Nodal Analysis (Modified Nodal Analysis (MNA)) model of several switching circuits were proposed by Trinchero [24] focusing on periodically switched linear (PSL) circuits focusing on their steady state solutions. This section aims to extend this analysis with limited number of harmonics to the Class-E amplifier shown in Fig. 2.1 for a time varying “sufficiently-smooth” (represented by limited harmonics) model of the switch. The circuit model translated into f -domain prepared for this analysis is given in Fig. 2.7. The case of modeling the Class-E amplifier with limited harmonics of the base switching frequency is of particularly of interest because in real life the switch does not have abrupt changes. By this way we aim to have a fast simulator which also coincides with real life voltage and current waveforms. On the other hand, using this simulator in combination with multivariable optimization, we examined if there exists a better topology of circuits with better custom efficiency and replacing parallel capacitor C_p ’s susceptance with a modified discrete susceptance function that the optimizer converges to.

It is also important here to note that the most efficient solution of the PSL circuit solver will not be the most useful one. Output power should also be monitored. To have also have a decent level of output power while maintaining efficiency, we chose an optimization variable geometrically custom weighting them as described in Eq. 2.29.

$$\text{Opt-var : } opt = P_{out}^{1.2}/P_{in} = \eta \times P_{out}^{0.2} \quad (2.29)$$

PSL circuit solver needs definitions of each element, node voltage, node current with the same limited number of harmonics (N) (with frequency span $-N\omega_0$ to $N\omega_0$, ω_0 being the constant switching frequency of the Class-E amplifier). Under a full frequency span from $-M\omega_0$ to $M\omega_0$ the f -domain analysis collapses to sets of matrix equations that can be quickly dealt with using a computational software (MATLAB (Mathworks, MA, USA) is used here).

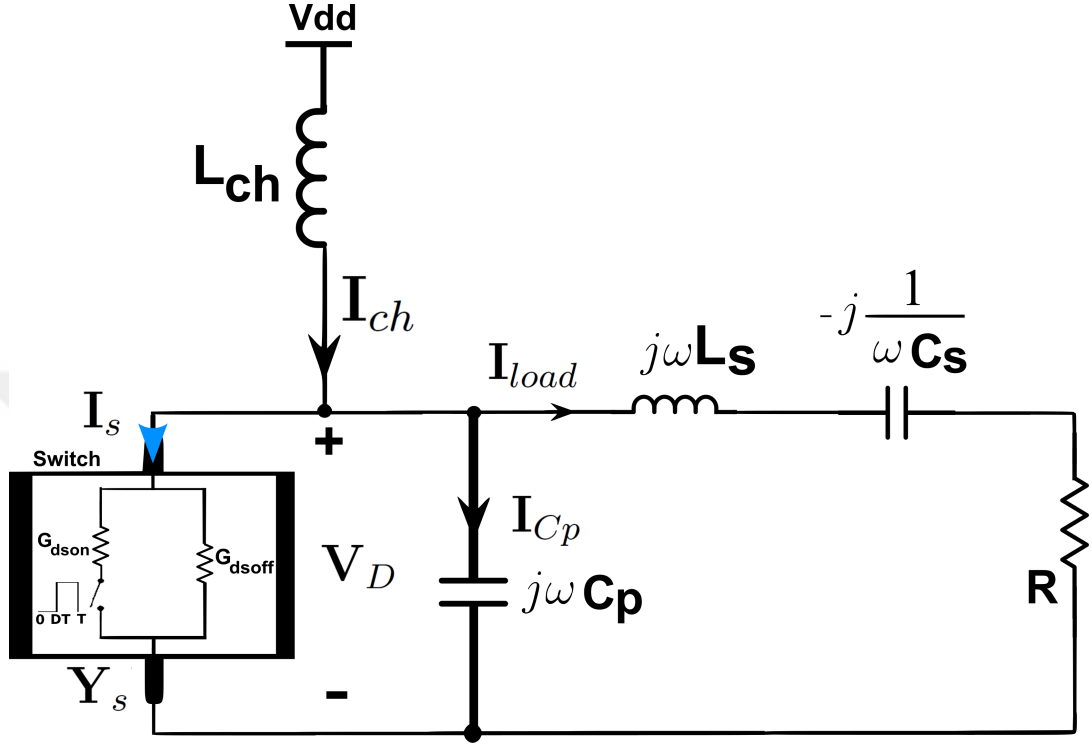


Figure 2.7: The circuit diagram prepared for modified nodal analysis. Linear well-defined elements simply transform into diagonal matrices. To exploit parallel combinations particular elements (such as $\mathbf{Y}_{C_p}$) are quoted with their respective admittances. To relate to common case of switch and being the transistor, switch voltage is referred to as the drain voltage with label V_D

To exploit parallel combination of the branches in the class E amplifier of Fig. 2.1, it is better to look at admittances rather than impedances. Load network's ($R_L - L_s - C_s$), (to which we can also refer as “the coil”) admittance is defined same as their phasor forms, a diagonal matrix as shown in Eq. 2.30. Since there is no inter-frequency interactions for these linear elements their models intuitively come out to be diagonal matrices. For a matrix size of M , a $2M+1$ (always odd-DC component at its isocenter) sized matrix is formed. At the isocenter of the matrices we have the so called DC-term describing the DC behavior of elements or DC component of voltage/currents. For DC analysis with no switching ($M=1$), the matrices turn into numbers describing DC nodal analysis, which also conforms intuition.

$$\mathbf{Y}_{load} = \begin{bmatrix} -M/(j\omega_0 L_s - j\frac{1}{\omega_0 C_s} + R_L) & & \\ & \ddots & \\ & & +M/(j\omega_0 L_s - j\frac{1}{\omega_0 C_s} + R_L) \end{bmatrix} \quad (2.30)$$

The parallel matching capacitor C_p can be defined using again the admittance of it phasor form, another diagonal matrix of a linear element follows in Eq. 2.31

$$\mathbf{Y}_{Cp} = \begin{bmatrix} -M/(-j\frac{1}{\omega_0 C_p}) & & \\ & \ddots & \\ & & +M/(-j\frac{1}{\omega_0 C_p}) \end{bmatrix} \quad (2.31)$$

Apart from these admittances writing the impedance of the choke inductor will also prove useful in this analysis. Again, closely following its phasor form, we have Eq. 2.32 for the choke inductor impedance.

$$\mathbf{Z}_{ch} = \begin{bmatrix} -M(j\omega_0 L_{ch}) & & \\ & \ddots & \\ & & +M(j\omega_0 L_{ch}) \end{bmatrix} \quad (2.32)$$

In this analysis, the most challenging concept to define with limited number of harmonics here is the switch admittance ($\mathbf{Y}_s$). Being both abruptly switching at the midst of the period and being defined with limited harmonics are contradicting each other. In this situation we can increase harmonic content N at the cost of additional computation time. With $N=15$ harmonic frequencies, the synthesized actual time-domain switch resistance is given in Fig. 2.8. The model of the switch arises from a jump between ON ($R_{dson}=100\text{m}\Omega$) and OFF ($R_{dsoff} = 2\text{k}\Omega$) conductance at the edge of the duty cycle. An N term Fourier series expansion of this square wave function yields the harmonic coefficients of the switch. We wanted this to represent an accurate model for the rise and fall behavior of the main LDMOS transistor (BLF573), but the limited number harmonics impacts the behavior significantly. Especially in low resistance region the behavior is critical, where for our case R_{dson} becomes comparable to load resistance value,

whereas for values above $1\text{k}\Omega$, the behavior can be safely ignored (very little impact on SPICE waveforms, since $R_{dson}/R_L \gg 1$). Even then, high to low transition and staying at the constant low resistance value is not completely achieved due to limited harmonic components (bottom of Fig. 2.8).

More generally, the switch admittance matrix $\mathbf{Y}_s$ is defined through an analysis analogous to a Fourier series given in pages 31-33 of [25].

Combining these for the class-E amplifier of Fig. 2.1, we have as the equivalent impedance (Z_{eq}) seen from the choke branch to the bottom as in Eq. 2.33:

$$\mathbf{Z}_{eq} = [\mathbf{Y}_s + \mathbf{Y}_{load} + \mathbf{Y}_{Cp}]^{-1} \quad (2.33)$$

The choke current can also be extracted using V_{dd} supply voltage. V_{dd} supply voltage will effectively be draining down to series combination (sum) of choke impedance $\mathbf{Z}_{ch}$ and the equivalent impedance of Eq. 2.33. Following this step we arrive at Eq. 2.34

$$\mathbf{I}_{ch} = [\mathbf{Z}_{eq} + \mathbf{Z}_{ch}]^{-1} \mathbf{V}_{dd} \quad (2.34)$$

If we matrix multiply the Eq. 2.33's equivalent impedance with choke current we will get the switch (drain) voltage in vector form.

$$\mathbf{V}_D = [\mathbf{Y}_s + \mathbf{Y}_{load} + \mathbf{Y}_{Cp}]^{-1} \mathbf{I}_{ch} = \mathbf{Z}_{eq} \mathbf{I}_{ch} = \mathbf{Z}_{eq} [\mathbf{Z}_{eq} + \mathbf{Z}_{ch}]^{-1} \mathbf{V}_{dd} \quad (2.35)$$

Eq. 2.35 looks similar to the well-known scalar formula of voltage division, instead to be done with matrices and vectors. We can also calculate the expression of switch current in terms of known set of vectors using 2.35. $\mathbf{V}_D$ being the voltage on a switch admittance path of $\mathbf{Y}_s$ the current follows with a simple multiplication.

$$\mathbf{I}_s = \mathbf{Y}_s \mathbf{V}_D = \mathbf{Y}_s \mathbf{Z}_{eq} [\mathbf{Z}_{eq} + \mathbf{Z}_{ch}]^{-1} \mathbf{V}_{dd} \quad (2.36)$$

Similarly, on the branch of parallel capacitor we get Eq. 2.37.

$$\mathbf{I}_{Cp} = \mathbf{Y}_{Cp} \mathbf{V}_D = \mathbf{Y}_{Cp} \mathbf{Z}_{eq} [\mathbf{Z}_{eq} + \mathbf{Z}_{ch}]^{-1} \mathbf{V}_{dd} \quad (2.37)$$

Using this $\mathbf{V}_D$ voltage which is also present on $\mathbf{Y}_{load}$ Load current can then be calculated by finding the current $\mathbf{I}_{load}$ escaping through the path of $\mathbf{Y}_{load}$ load network.

$$\mathbf{I}_{load} = \mathbf{Y}_{load} \mathbf{V}_D = \mathbf{Y}_{load} \mathbf{Z}_{eq} [\mathbf{Z}_{eq} + \mathbf{Z}_{ch}]^{-1} \mathbf{V}_{dd} \quad (2.38)$$

The current $\mathbf{I}_{load}$ can be used to calculate the output power consumed by R_L .

$$P_{out} = \mathbf{I}_{load}^H \mathbf{I}_{load} R_L \quad (2.39)$$

where super script H denotes transpose conjugate operation (Hermitian). For the supplied input power (by the V_{dd}) we can form Eq. 2.40

$$P_{in} = \mathbf{I}_{ch}^H \mathbf{V}_{dd} \quad (2.40)$$

As the final step of substituting $\mathbf{I}_{load}$ in Eq. 2.39 with its solution in Eq. 2.38. And dividing it side by side with Eq. 2.40 we get the compact efficiency expression for a given Class-E amplifier.

$$\eta = P_{out}/P_{in} = \frac{\mathbf{I}_{load}^H \mathbf{I}_{load} R_L}{\mathbf{I}_{ch}^H \mathbf{V}_{dd}} \quad (2.41)$$

which can then be expanded if wanted to by plugging in the value of $\mathbf{I}_{load}$ from Eq. 2.38 and value of $\mathbf{I}_{ch}$ from Eq. 2.34.

$$\eta = \frac{(\mathbf{Y}_{load} \mathbf{Z}_{eq} [\mathbf{Z}_{eq} + \mathbf{Z}_{ch}]^{-1} \mathbf{V}_{dd})^H (\mathbf{Y}_{load} \mathbf{Z}_{eq} [\mathbf{Z}_{eq} + \mathbf{Z}_{ch}]^{-1} \mathbf{V}_{dd}) R_L}{([\mathbf{Z}_{eq} + \mathbf{Z}_{ch}]^{-1} \mathbf{V}_{dd})^H \mathbf{V}_{dd}} \quad (2.42)$$

The target of the above equations has always been to leave the right hand sides full of known quantities for a given Class-E circuit. In the next step of analysis, we can fix some parts of the matrices and force optimization on the remaining parameters. Computational matrix tools such as MATLAB's function optimizers arms us with the ability to optimize full length vectors subject to sets of boundary conditions. Vector optimization of $\mathbf{Y}_p$ for example may lead to some interesting results, and may even suggest better circuit topologies at the cost overheads in circuit complexity.

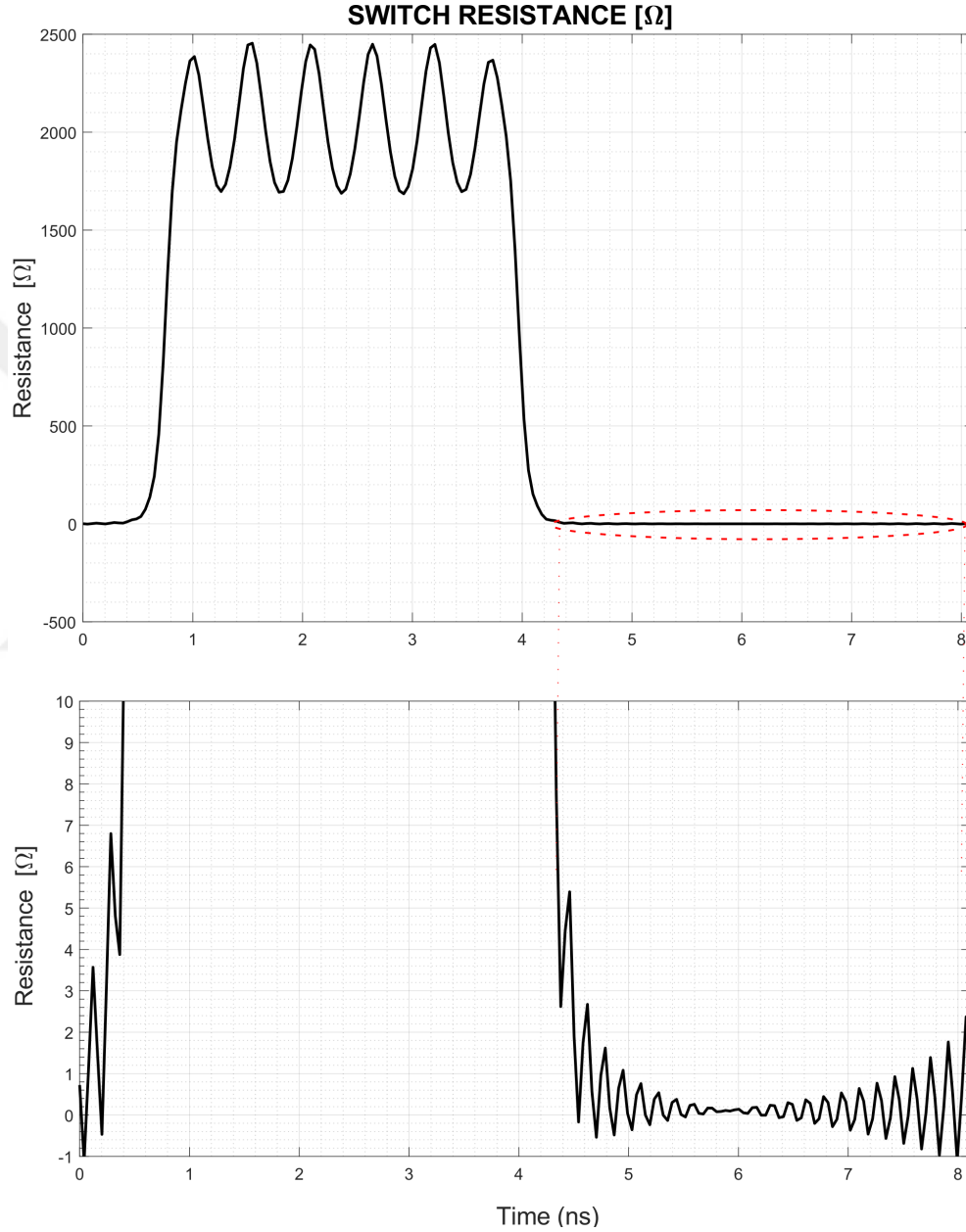


Figure 2.8: PSL circuit model's generated switch resistance model in time domain ($N=15$, $M=50$), a single period ($T \approx 8.11$ ns) for $f_0 = 123.24$ MHz. The Gibbs oscillations are due to finite number of harmonics. Particularly oscillations at lower end is more important (for which y-axis is zoomed at the bottom graph). Due to limited harmonic count, the target 100 mΩ ON resistance is only achieved on average at the OFF-cycle.

2.3 Driver and Supply Modulation

Main focus on updates in the driver and supply modulation aspects was in FPGA (XILINX Inc., KCU105, California, USA) design of Fig. 2.4, which consisted of better utilization of clocking, fixing clock domain crossings and timing errors due to those.

2.3.1 Gate Driver: “Skipping Glitch”, its Artifacts in MRI Image and Theory of its Solution

The skipping glitch for this context can be defined as the system not responding to triggers from time to time, hence skipping some RF pulses when the system vitally needs them. This issue is extremely important because it creates a empty line on the k-space of the readout data which translates to ghosting artifacts (shifted replicas) on the phase encoding axis. As an example the pair representative constant k-space signal with a dent and its Fourier transform can be examined in in Fig. 2.9. This dent clearly creates ghosting effects off the main center frequency (which is DC for the constant signal).

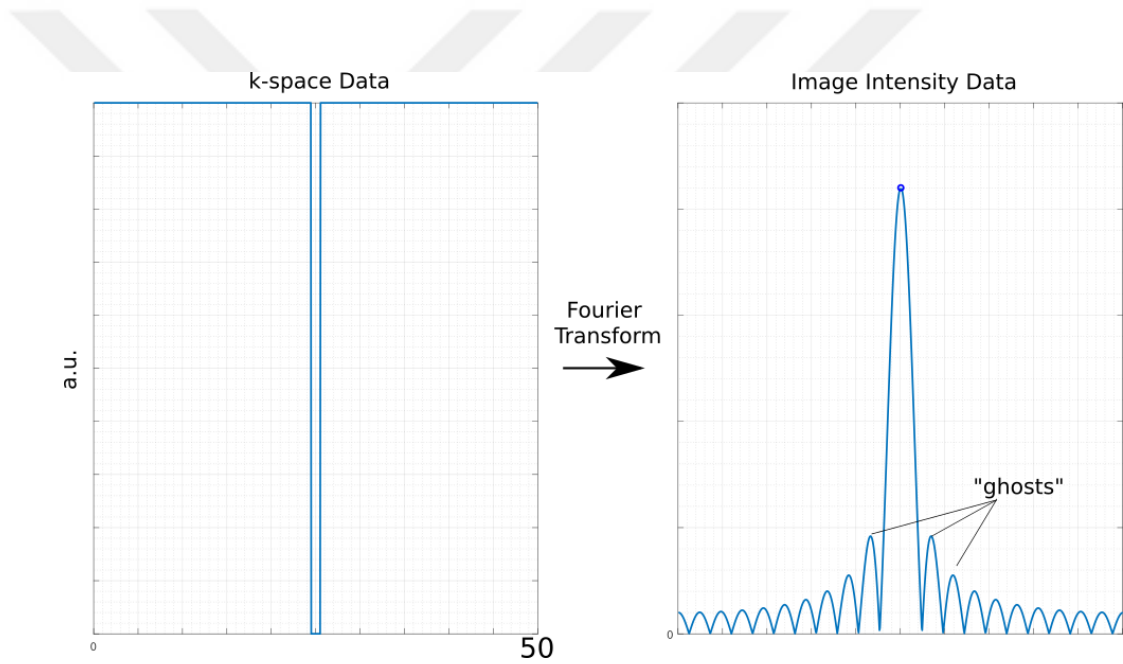


Figure 2.9: Demonstration of 1 missing line out of 50 k-space lines, its effect in the image is ghosting perpendicular to the direction of missing line (Data taken using FFT algorithm with 20 sample upscaling). k_y (phase encoding axis) in our case, for each phase encoded, a line of k_x values are sampled during readout, i.e., k_x data comes in chunks as response to each RF-pulse at each k_y value

2.4 Magnetic Field Analysis of Two Circular Loop Coils

Following the analysis [26] employing off-axis whole space solution to Maxwell's equations for a loop coil set-up shown in Fig. 2.10, we arrive at the following set of Eq. 2.43 and Eq. 2.44 for the magnetic field's axial z and radial ρ components [27], respectively in cylindrical coordinate system (ρ, ϕ, z) . It is important to note that this z -axis of our regular coordinate system in Fig. 2.10 [26] is *not* the direction of the 3 Tesla main MRI field (the bore's axis). For the experiment, the bore's axis is the y -axis and we have two coils loop coils placed at $x = d$ and $x = -d$ (the factor of 2 for convenience in equation terms). Exploiting the symmetry about the y - z plane, at $x = 0$ plane (which will be the sagittal plane), these two coils will excite a B1 field in z -direction at the (B0 field in y -direction), and only the field component inside the x - z plane will matter because of basic MRI principals of torque and precession (y -component cannot rotate the spins and cause a flip angle).

The current in the context of near field can be thought of as a quantity with a phase and magnitude. Hence the phasor notation $\mathbf{I}$ can be put to use for the loop currents. The assumption here is that, since $\lambda \gg D$ (dimensions of our maximum depth of imaging), the retarded vector potential's phase terms can be ignored which makes it purely real in our case of near field. Only the currents will carry the complex phase information (as phasors) due to their rapidly changing nature.

$$B_z = \frac{\mu_0 \mathbf{I}}{2a} \frac{1}{\pi \sqrt{\left(1 + \left(\frac{r}{a}\right)^2 + \left(\frac{z}{a}\right)^2\right)}} \left[\frac{1 - \left(\frac{r}{a}\right)^2 - \left(\frac{z}{a}\right)^2}{\left(1 + \left(\frac{r}{a}\right)^2 + \left(\frac{z}{a}\right)^2 - 4\left(\frac{r}{a}\right)^2\right)} E(k) + K(k) \right] \quad (2.43)$$

$$B_\rho = \frac{\mu_0 \mathbf{I}}{2a} \frac{z/r}{\pi \sqrt{\left(1 + \left(\frac{r}{a}\right)^2 + \left(\frac{z}{a}\right)^2\right)}} \left[\frac{1 + \left(\frac{r}{a}\right)^2 + \left(\frac{z}{a}\right)^2}{\left(1 + \left(\frac{r}{a}\right)^2 + \left(\frac{z}{a}\right)^2 - 4\left(\frac{r}{a}\right)^2\right)} E(k) - K(k) \right] \quad (2.44)$$

where $K(k)$ and $E(k)$ are the complete elliptic integral functions of first and second kind, respectively, and the input k to the elliptic integral functions is

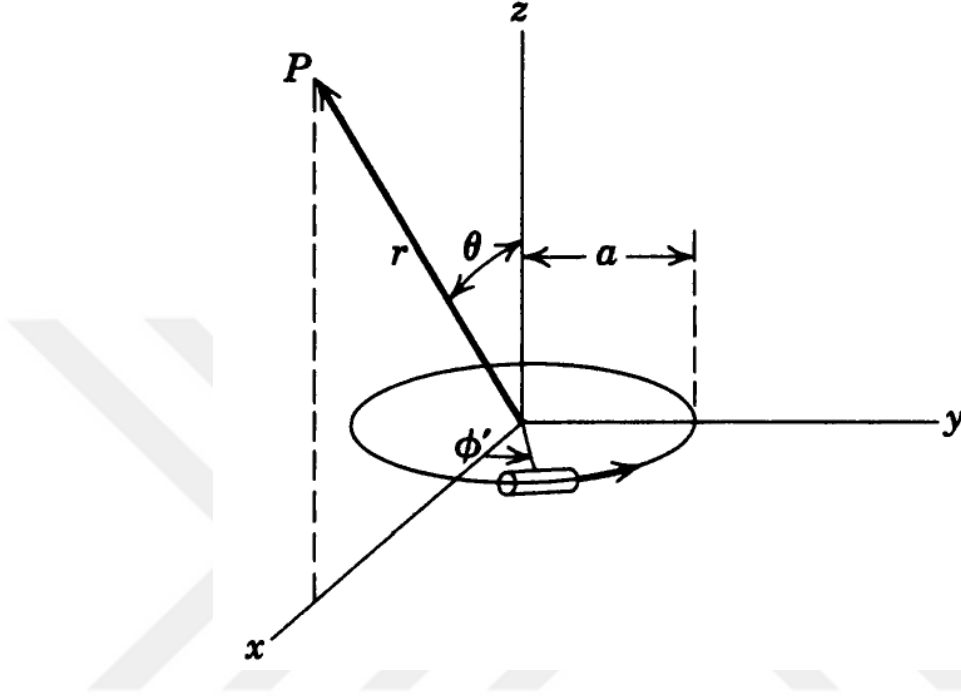


Figure 2.10: Setup modeling the loop coils for the analytical solutions of the magnetic field

defined as in Eq. 2.45.

$$k = \sqrt{\frac{4\left(\frac{r}{a}\right)}{\left(1 + \left(\frac{r}{a}\right)^2 + \left(\frac{z}{a}\right)^2\right)}} \quad (2.45)$$

In MRI, flip angle (α) of the sinc RF-pulse determines the image intensity S . For a sinc pulse, flip angle can be defined as $\alpha = \gamma\tau B_1$ where γ is the gyromagnetic ratio of hydrogen, τ is the duration of the RF sinc pulse and B_1 is the magnitude of the RF-pulse (typically a few μT). The image intensity is directly related to $S \propto \sin(\alpha)$. In the near field solution of two shifted coils on the x - y plane with separation $2d$, we will have the components of the B_1 magnetic field from the left (at $x = -d$) and right (at $x = d$) loop coils adding up in phasor domain. The equation of a shifted coil barely change. The only change will be in the coordinate term r (measuring the distance from the origin of a coil to the point of measurement). r will be substituted by $r_1 = \sqrt{r^2 + d^2}$ and $k(r)$ of Eq. 2.45 will be substituted by $k_1 = k(r_1)$.

$$B_1 = B_{z,total} = |B_{z,left} + B_{z,right}| \quad (2.46)$$

$$B_1 = |\mathbf{I}_{left} + \mathbf{I}_{right}| \frac{\mu_0}{2a} \beta_z(r_1 = \sqrt{r^2 + d^2}, z) \quad (2.47)$$

where the unitless β_z factor contains the spatially dependent scaling term as given in Eq. 2.48:

$$\beta_z(r_1, z) = \frac{1}{\pi \sqrt{\left(1 + \left(\frac{r_1}{a}\right)^2\right)^2 + \left(\frac{z}{a}\right)^2}} \left[\frac{1 - \left(\frac{r_1}{a}\right)^2 - \left(\frac{z}{a}\right)^2}{\left(1 + \left(\frac{r_1}{a}\right)^2\right)^2 + \left(\frac{z}{a}\right)^2 - 4\left(\frac{r_1}{a}\right)} E(k_1) + K(k_1) \right] \quad (2.48)$$

Focusing on the first term of Eq. 2.47 ($|\mathbf{I}_{left} + \mathbf{I}_{right}|$), we see that changing the phase of difference between the currents will have an impact on the overall magnitude of B_1 field excited inside the phantom. Phasors will add up constructively or destructively based on the phase difference between them. Since the wavelength at 123.24 MHz Larmor frequency in air ($\lambda = 2.43$ m) is much larger than the coil dimensions and the dimensions of our phantom (22.4 cm, actual excited region is at most half of this as we will see in results Sec. 4.3), we neglected phase terms resulting from the exact retarded magnetic vector potential solution. It is also important to note that in the experiment, the coils are decoupled ($S_{21} < -40$ dB) using the method of overlap decoupling [28], and thus the theoretical analysis is further simplified by neglecting the terms due to coils exciting each other.

2.5 B1 Mapping Theory: DAM

B1 (the term used short form of B_1^+ in this context) field mapping and its efficiency (measured μT per $\sqrt{W}$ of consumption) are important characteristics describing how good an amplifier is in terms of converting its input power to what really matters as an end product while imaging. A high B1 efficiency is indicates being able to reach a dynamic range of flip angles without the need of sophisticated hardware for cooling in bore which is much more difficult in the presence of high magnetic fields (artifacts/eddy currents/(safety: can't use magnetic elements like motors/fan)).

The challenge here is, being a switch mode amplifier, in converting DC power to AC power, Class-E amplifier suffers from inherent non-linearity. Here we aimed to observe the non-linearity by constraining the amplitude while varying the RF pulse duration. On the next stage duration is kept constant while varying the amplitude to observe the gain compressing (saturation) behavior of the amplifier.

The conventional double angle method (DAM) uses two images with two known flip angles (α and 2α) (typically $\alpha = 60^\circ$ and $2\alpha = 120^\circ$), and dividing their output images to obtain a map of flip angle (and using either one of the images) and B_1 field. Following the analysis in [29] and [30], since the image intensity S (where S stands for signal: the greater the signal the brighter, i.e., more intense the MRI image) for a gradient echo (GE) sequence can be written as in Eq. 2.49

$$S_{GE}(\mathbf{r}) = K p(\mathbf{r}) C(\mathbf{r}) \sin(\alpha(\mathbf{r})) e^{-TE/T_2^*(\mathbf{r})} R(TR, T_1(\mathbf{r}), \alpha(\mathbf{r})) \quad (2.49)$$

where $\mathbf{r}$ is the position vector ($\mathbf{r} = (x, y, z)$), K is a system constant, p is the spin density, C is the coil sensitivity, α is the flip angle, TE is the echo time, TR is the repetition time, and R is the longitudinal relaxation term mainly affected by T_1 -relaxation and flip angle (if T_1 effects are not negligible, the term maximizes when the flip angle equals to the Ernst Angle [31]):

$$R = \frac{1 - e^{-TR/T_1(\mathbf{r})}}{1 - \cos(\alpha(\mathbf{r})) e^{-TR/T_1(\mathbf{r})}} \quad (2.50)$$

Eq. 2.50 denotes that to be able to ignore T_1 effects in the analysis, TR should be kept high enough so that the relaxation term is sufficiently close to unity. Here,

$TR > 5T_1$ is the chosen criteria ($e^{-5} < 0.007$). This will simplify the analysis and will enable us to end up in the well-known compact form of the double angle method. Dividing the two intensities arising from α and 2α side by side and utilizing the trigonometric identity $\sin(2\alpha) = 2\sin(\alpha)\cos(\alpha)$ we have Eq. 2.51.

$$\frac{S_{GE,2\alpha}}{S_{GE,\alpha}} = \frac{\sin(2\alpha)}{\sin(\alpha)} = 2\cos(\alpha) \quad (2.51)$$

What we can do next is to get an expression for α (but need to be careful since arccos function is defined as a 1-to-1 function from $[-1,1]$ to $[0,\pi]$ and its output range ($[0,180^\circ]$) will not be able to cover the full range of possible flip angles. In any case, we need to keep the cyclical nature of $\sin(2\alpha)/\sin\alpha$ function in mind and its $\sin(2\alpha)/\sin\alpha = 1$ intercepts will be of interest.) And then use this expression to plug into the expression of α in terms of B_1 field for the sinc pulses to end up with Eq. 2.54.

$$\alpha(\mathbf{r}) = \frac{1}{2} \arccos\left(\frac{S_{GE,2\alpha}(\mathbf{r})}{S_{GE,\alpha}(\mathbf{r})}\right) = \gamma B_1(\mathbf{r})\tau \quad (2.52)$$

$$B_1(\mathbf{r}) = \frac{1}{2\gamma\tau} \arccos\left(\frac{S_{GE,2\alpha}(\mathbf{r})}{S_{GE,\alpha}(\mathbf{r})}\right) \quad (2.53)$$

To avoid possible non-linear effects when changing voltage to scale B_1 , instead of trying to scale B_1 , it is much a better practice to use the pulse length τ from τ_0 to $2\tau_0$ to obtain the two target flip angles α and 2α and take the images under the same B_1 field condition:

$$B_1(\mathbf{r}) = \frac{1}{2\gamma\tau_0} \arccos\left(\frac{S_{GE,2\alpha,2\tau_0}(\mathbf{r})}{S_{GE,\alpha,\tau_0}(\mathbf{r})}\right) \quad (2.54)$$

DAM can be slow and due to this impractical for in-vivo commercial applications, but it is still kept as the state of the art error-calculative comparison case in the literature [32]. Novel methods also use low TR sequences for double angle B1 mapping on the condition of accounting for so called “T1 correction” [33], i.e., instead of the simpler $\sin(2\alpha)/\sin(\alpha)$ division we must use $\sin(2\alpha)R(2\alpha)/(\sin(\alpha)R(\alpha))$ the full form of the expression. This makes the inverse function not as straightforward as before to express. Computational tools such as Matlab can be used to solve this as a system of equations for each pixel. Parallel computing toolbox, which come in handy in cases of image processing like this, can be employed to make the rendering of B1 maps up to 12 times faster on a 12 threaded CPU.

2.6 Theoretical Update to the Amplifier Design Topology, its Simulation and the Previous Driver's Frequency Response

The gate driver designed by Poni [1] is examined in Fig. 2.11. After also extracting the frequency responsiveness of gate voltage waveform parameters, which is given in Fig. 2.12. The driver uses series resistors and damping circuits composed of capacitors and inductors to cope with ringing in the voltages. This, in turn, combined with the intermediate chips' responses, limits the bandwidth of the driver and gives it a unique frequency response that can be taken a glimpse at in 2.12. But the main problem with it here is not the latter. One can point out that, in its high side portion, the driver lacked one of the most important principles of half bridge driving: using feedback to counterbalance the output gate voltage with a clamped high side switch voltage. A conventional half bridge driver uses two NMOS FETs (high side MOSFET and low side MOSFET) to drive another main NMOS (switch of the Class-E amplifier). On the portion of time when the high side MOSFET is on, the gate voltage of the main MOSFET builds up. This is a direct negative feedback as the source of the high side MOSFET rises, its V_{GS} voltage decreases if left uncompensated. A conventional half bridge driver chip, sees this and accommodates for higher voltages (even higher than V_{dd} in some cases) at the gate of the high side transistor (green marks on Fig. 2.11 [1]). Our earlier design did not have this kind of chip as we could not find candidates of half bridge drivers satisfying the frequency range. This is the part GaN HEMT transistors and their fast drivers comes to rescue. In the next version of the design our group aims to correct this error by using a proper low-side transistor driver (LMG1020 (Texas Instruments, TX, USA)) instead of trying to emulate it. My contribution to this work mainly comprised of suggesting the elimination of bridge driver topology altogether because the Class-E amplifier itself can be thought of as a single low side transistor (high side part is composed of connectivity to V_{dd} via a choke inductor), a single low side transistor driver can do the job.

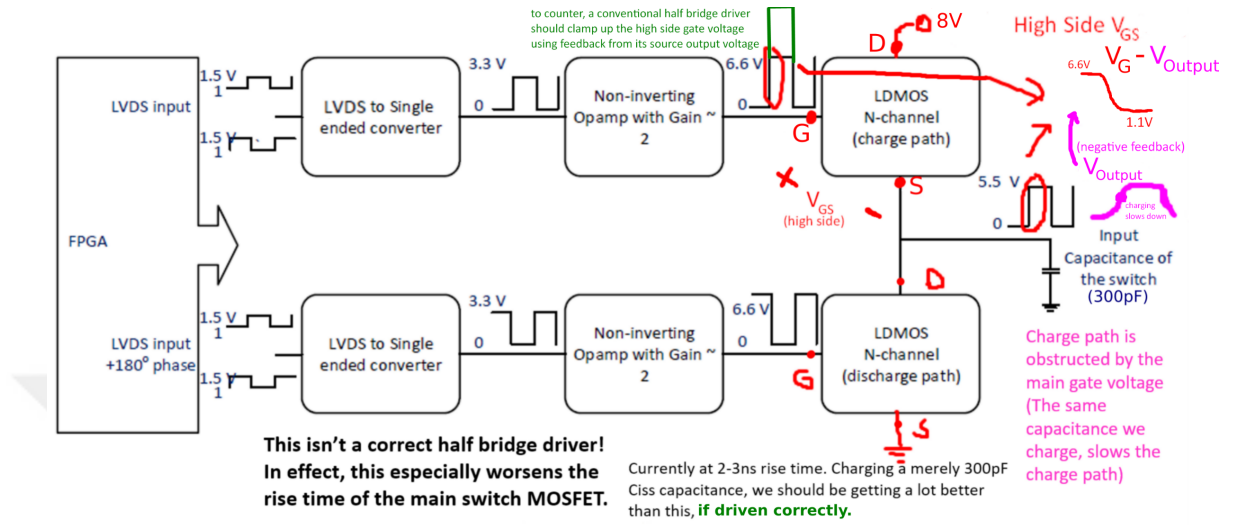


Figure 2.11: Analysis of the gate driver diagram of the earlier design (green: correct high side waveform countering negative feedback)

With the help of new generation fast GaN transistor drivers (LMG1210 and LMG1020), there is actually barely any change in performance using two other transistors to drive one main transistor. Using two other transistors complicates the design requiring each of them to have driver paths and signals and necessitates extra supply voltage levels, which in turn introduce design cost and size overheads. With the help of preliminary simulations I proved the successful integration of a single LMG1020 driver directly driving the main GaN switch. The work will be followed and explained up to manufacturing in Arghiani's thesis [5] as the 4th generation of our on-coil Class-E amplifiers targeting magnetic resonance imaging. In her results, (including the hardware) we will see that the proposed ON voltage for the gate is reached, and rise and fall times of the driver more than halved (i.e., the performance is doubled). The updated design can even now be further overclocked by decreasing the 2Ω anti-oscillatory damping resistors (R1 and R5 in Fig. 3.6 or R9 and R10 in 2.13 or Fig. 3.4 of [5]), at the cost of additional waveform overshoot and undershoot. As the series resistor values gets increase we have the following trend in the rise and all times of the transistor simulated in LTSPICE.

Although the quoted frequency limit of 60MHz can be misleading, because it is

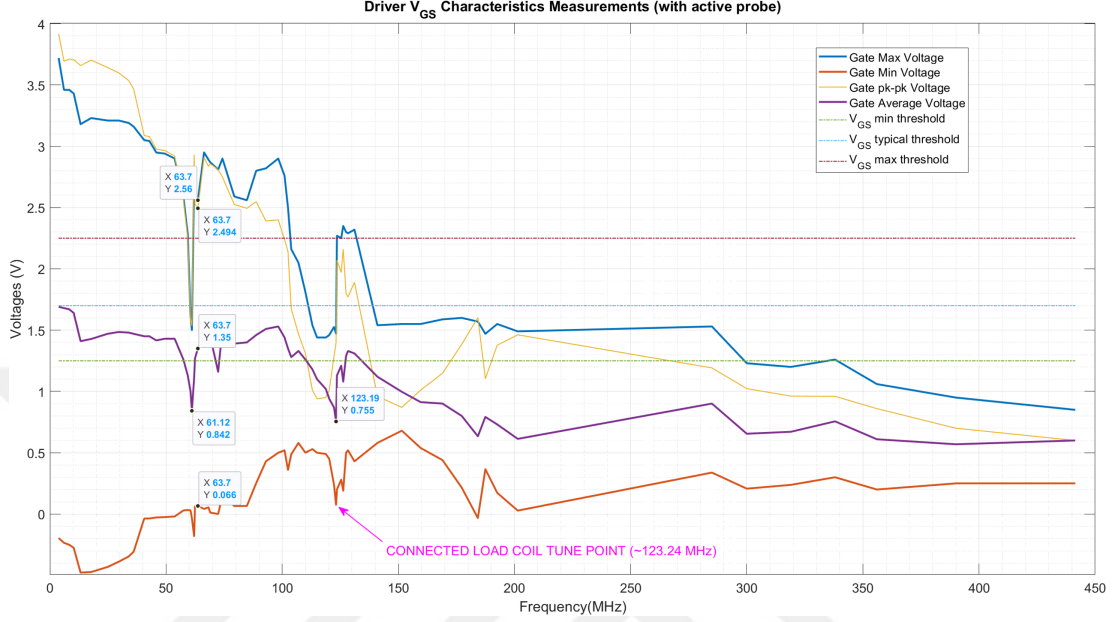


Figure 2.12: Gate voltage waveform's important parameters for a range for drive frequencies of the gate driver

given for 1nF load, LMG1020 [34] advertises capability of 7A peak and 5A source currents. With direct contact under the condition that these aforementioned resistors are zeroed, the rise time of the transistor gate under direct drive condition of the input capacitance of $C_{iss}=75\text{pF}$ [35] EPC2036 GaN can be estimated using Eq. 2.56, employing the source current ($I_{source}=7\text{A}$) parameter and frequency 123.24 MHz ($T=8.11\text{ns}$)

$$\frac{C_{iss}\Delta V}{\Delta t_{rise}} = I_{source} \quad (2.55)$$

$$C_{iss}\Delta V = I_{source}\Delta t_{rise} \quad (2.56)$$

Plugging in the values (where we need a rise to $\Delta V=5\text{V}$ within a time less than 1ns, $C_{iss}=75\text{pF}$) we finally have the numerical value for Δt_{rise} in Eq. 2.58

$$\Delta t_{rise} = \frac{C_{iss}\Delta V}{I_{source}} \quad (2.57)$$

$$\Delta t_{rise} = \frac{75 \times 10^{-12} \times 5 \text{ [Farad Volts]}}{7 \text{ [Coulombs/sec]}} = 53.6 \text{ ps} \quad (2.58)$$

which comfortably satisfy the criteria of at most 1ns rise time. Analogous analysis can be done for fall times, this time using the sink current as the determining factor. In the presence of damping path resistors, the behavior can either be solved

by using the natural exponential solution to the differential equation counterpart of RC with 10% (0.5V) to 90% (4.5V) thresholds, or be simulated in SPICE with readily available models of LMG1020 and EPC2036. The results of such a simulation (Fig. 2.13) covering a stepped range of series resistors are given in Fig. 2.14 . The results are in the order of the theoretical capacitance charge speed equation of 2.58.

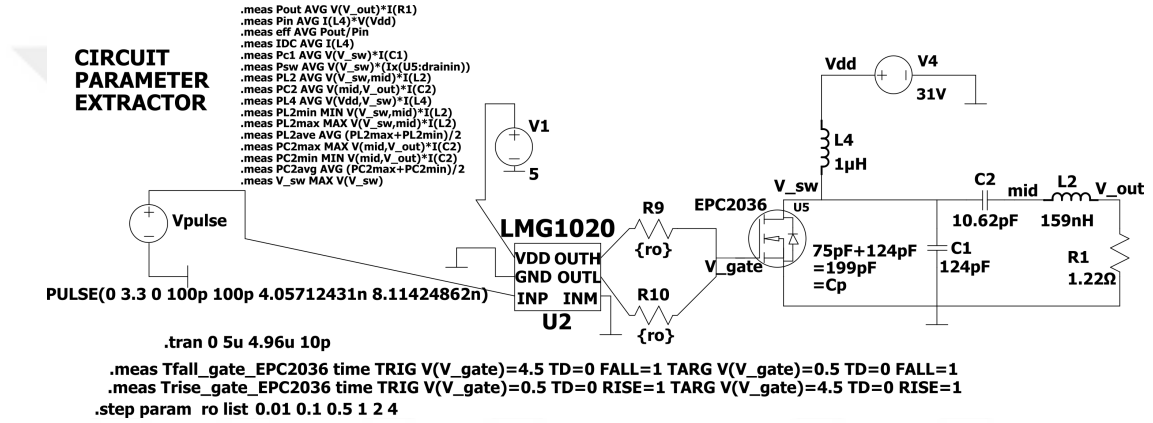


Figure 2.13: Simulated LTSPICE circuit with parameter extractor and sweep capability for theoretical analysis of rise-fall times

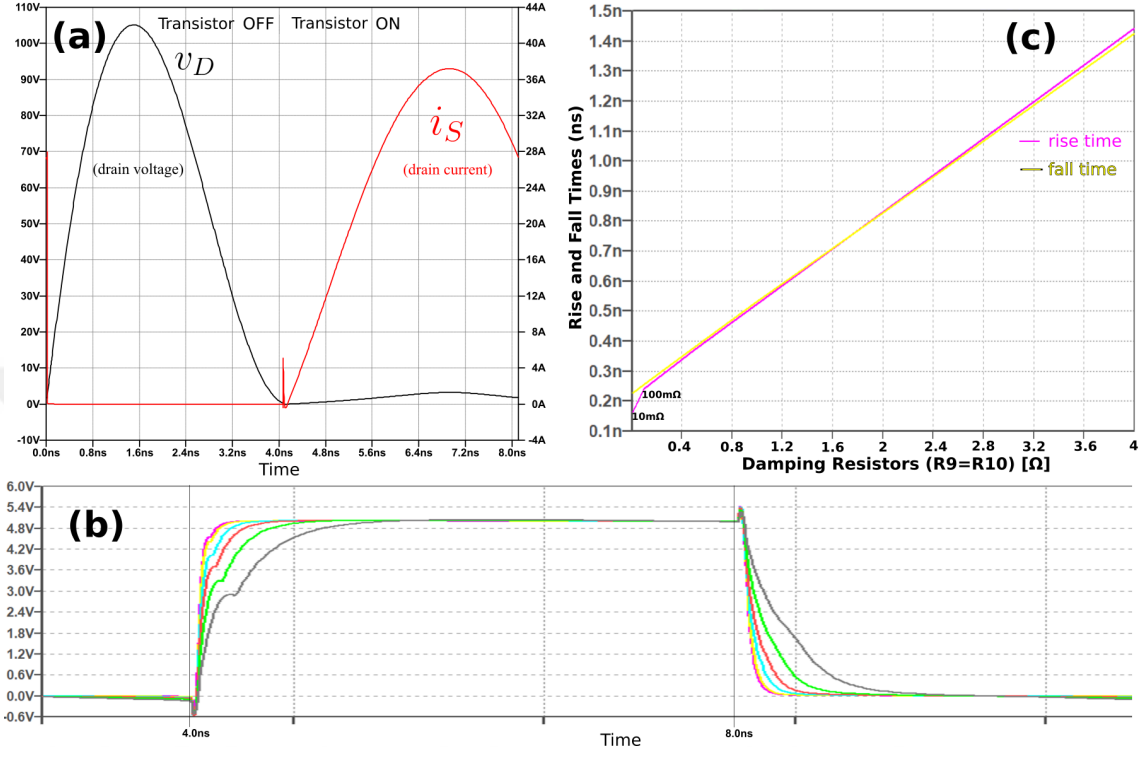


Figure 2.14: (a) Drain voltage and current SPICE simulation of the circuit in Fig. 2.13 for $R_9=R_{10}=10\text{m}\Omega$ - the spike is due to misalignment in tuning latency adjustment in the EPC2036 GaNFET, (b) while stepping parameters, zoomed in version the gate voltage of GaNFET of the same circuit (time axis shifted and zoomed in for better detail), (c) 10%(0.5V), 90%(4.5V) thresholded rise and fall times extracted for the swept values of damping resistors $R_9=R_{10}$

The results of this custom transistor circuit will be given in Table 4.1 for a SPICE comparison case of the switch as the transistor with more realism in its gate driver scheme.

Chapter 3

Methods

3.1 Periodically Switched Linear (PSL) Circuit Simulator Methodology

MATLAB (R2021b, Mathworks, MA, USA) is used for the transcription of the matrix equations of Sec. 2.2 into the computational environment. For $M=50$ and $N=15$, 27610 combinations (251 C_s values and 110 C_p values) of Class-E amplifiers are (for the coil of Fig. 3.3 with the load impedance of the measured case 1.22Ω) simulated using MATLAB's parallel computing toolbox and solutions are recorded for further analysis in terms of maximum efficiency, power, and the opt-var of Eq. 2.29. All of this process took less than 40 seconds on a 12 threaded CPU (12 parallel cluster workers). Example resulting simulation waveform results for the maximum efficiency η , maximum output power P_{out} , and the maximum optimization variable $\text{opt-var} = P_{out}^{0.2}P_{out}/P_{in} = P_{out}^{0.2}\eta$ are particularly examined.

3.2 FPGA Design Methodology

3.2.1 Robust FPGA design: Clearing the Gate Driver Glitches Causing MRI Artifacts

The glitch that was first mentioned in 2.3.1, was due to the system not satisfying the timing constraints. A “flag” signal was generated in a process of 200MHz that ultimately drove the gate modulation clock multiplexer at 123.24 MHz. As this was attempted to be done without timing constraints in mind (no clock domain crossing) the design in this state was failing timing. Up to 10% of the overall asserted RF pulses’ gate driver signals in the pool of asserted RF pulses were missing, while a trigger source requested 80 RF pulses back-to-back within a 1 second time interval. The same was true on a larger time scale. Even at $TR=100ms$ or $TR=1sec$ the system behaved erratically by not responding to RF pulse requests from time to time.

To correct this error, any dependence on processes is completely removed from the path of gate modulation clock signals. In this update, the unblanking of this clock is done using only combinatorial logic elements (as we will see in the corresponding results section) which completely removed the glitching issue.

3.2.2 Supply Modulation: FPGA Update

The block diagram of the early design is given in Fig. 2.4. FPGA generates the necessary pulse width modulation (PWM) signals by reading them out from a set of pre-recorded streams in its block memory. Supply modulation of our design in FPGA was based on a Mealy state machine taking a trigger (unblank) as input whenever the external system needs an RF-pulse. Whenever a trigger is asserted, the state machine goes from IDLE-STATE (blank state) to TX-STATE (transmit RF pulse state) and when the end of the pulse is reached IDLE-STATE takes over [1]. The block RAM initializer coefficient files carry the pulse width modulation

PWM information of the envelope. During initialization, these files are dumped into memory during bitstream programming. The limitation of maximum Block RAM (BRAM) memory depth (1048000 bits $\approx$ 1 million bits), limits the maximum length of the pulses that can be created. The concept of time (duration of pulse) is introduced while these bits are read at a constant bitrate of 200Mbps (process clock). In the previous design, a single BRAM module is initialized to hold both the high side and the low side (40ns dead time in between them to provide safe switching with less dissipation) PWM signals of the RF pulse. Considering this 1 million bit depth limitation combined with 200Mbps read rate, we could get at most 2.5ms of RF pulses (2.5ms high side , 2.5ms low side; total of 5ms; $5\text{ms} \times 200\text{Mbps} = 1 \text{ Million bits}$). In the updated version of the design BRAM are initialized for each of the high and low side bitstream coefficient files. In this state, the system could now support generation of up to 5ms lengths of RF pulses. Moreover, as part of eliminating clock domain crossings, the rather unnecessarily fast 200MHz system clock is also pulled back to default sync clock of 100MHz (from the top scale block design including PCIE and GPIO interfaces), which enabled the design to satisfy timing constraints with minor disadvantages in quantization levels (1MHz PWM signalling is now done at 100 Mbps, which is still 100 fold and will provide 100 quantization levels between 13.5% and 86.5% PWM boundaries).

3.2.3 Dynamic Phase Control On-the-fly

Dynamic phase control is achieved using a dynamic phase shift interface of the Mixed-Mode Clock Manager (MMCM) module [36] of the Kcu105 FPGA. The created top the design schematic can be found in Appendix Sec. A.1. A Mealy State Machine is employed to control the phase and make it approach to a desired input state from a general purpose Input/Output (GPIO) "state register" which is represented by a 9 bit binary number. The GPIO state register is written using the PCIE interface of the FPGA communicating through an AXI interface. For 123.24 MHz (Siemens 3T TIM TRIO (Siemens, Munich, Germany) scanner's Larmor frequency), phases in range 0-708° has been fully covered for the input

range 0-511 (000h to 1FFh). This over coverage is to make the design versatile enough to also cover the range of all phases for 63.78 MHz (for 1.5T Scimedix Scanner (Scimedix Inc., Incheon, South Korea)) operation (0-367°). The phase coverage can be further adjusted by changing the voltage controlled oscillator (VCO) frequency as the phase shifting still occurs in $1/32$ of the full period of the VCO (set $T_{VCO} = 1ns$). For this design, the VCO frequency is configured to 1GHz by applying multiplication and division factors of 10 to a default 100 MHz input. The design also includes forward compatibility by employing DDR4 memory and its control modules, all again communicating through AXI interfaces. In the case of 32 channels (the goal of future work), with its accomodating space, DDR4 memory can be used to store and well-defined and fine-tuned states of phases for all channels.

The Mealy State Machine reads its input from a 10-bit GPIO desired state register (D), compares it with the current state register(C), as long as there is a mismatch ($C < D \rightarrow$ set PSINCDEC set to 1, $C > D \rightarrow$ set PSINCDEC to 0) between the two, it asserts a PSEN bit for one clock cycles and waits 16 clock cycles to guarantee finishing a single shift operation, which shifts (lags) channel 2 with respect to stationary channel 1 by $\frac{T_{VCO}}{32} = 31.25ps$. According to [36], a single shift takes 12 clock cycles and it is deterministic. A 4 clock cycle tolerance is added for system stability and robustness. The 16 clock cycle wait time is assured by raising a flag after overflowing a 4 bit counter. Only after this overflow, the current state register is incremented/decremented. This cycle continues until the current state register and the desired state registers become equal to each other. Upon preliminary post-implementation timing simulations using a subdesign (no testbench is available for PCIE and AXI and will be too cumbersome to write from scratch), for a 100 MHz common process state-machine clock, it is noted that it takes $173\mu s$ to complete a full scale phase shift from 0° to 360°. This delayed response is not critical and well within range to be dynamically adjusted/controlled during a pulse sequence.

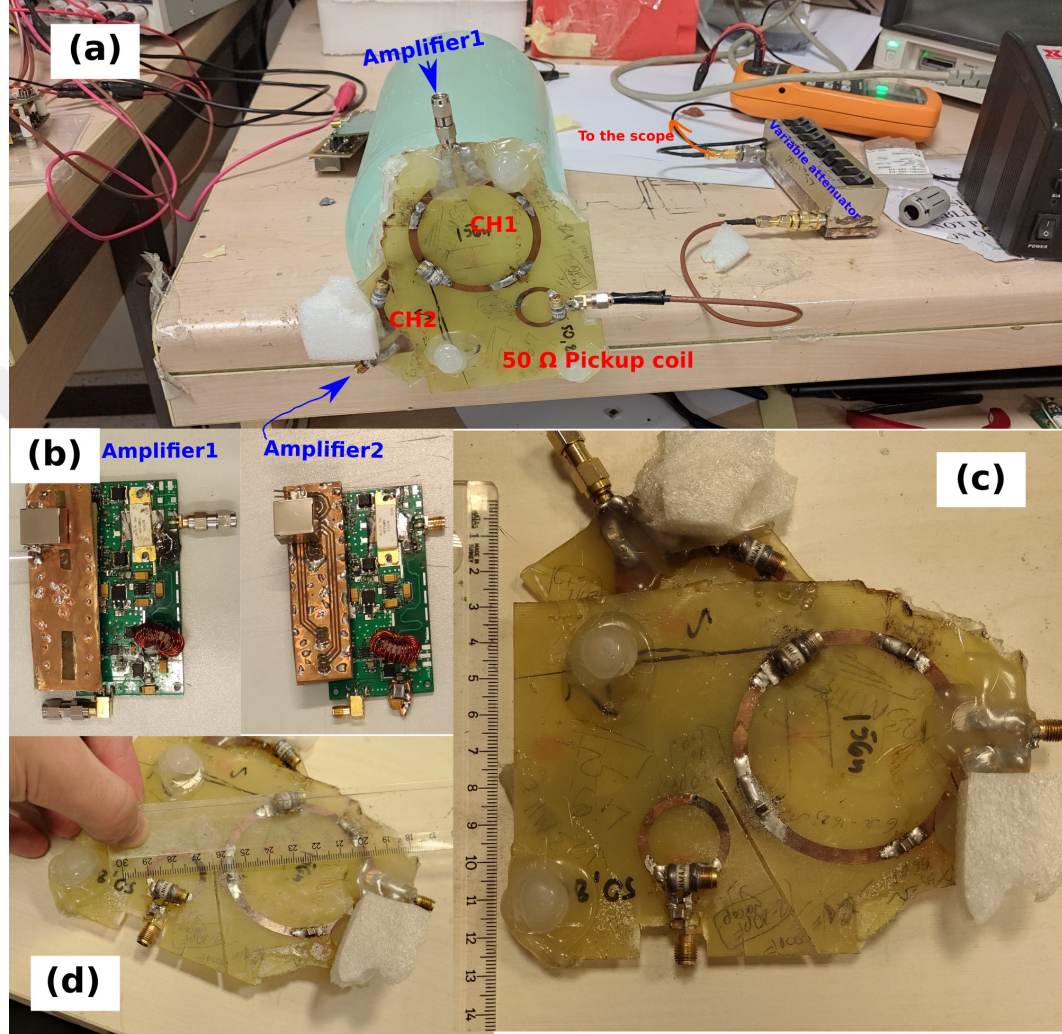


Figure 3.1: Dynamic phase control bench testing set-up (a) Pickup coil and the placement of the channel coils tuned while on phantom (loaded), (b) Amplifier1 and Amplifier2 driving CH1 and CH2 coils, respectively, (c-d) Overlap decoupled coils dimension detailed with a ruler (cm scale)

The setup for bench testing the phase delay control is given in Fig. 3.1. Dimensions of the coils and positions with respect to pickup coils are detailed (kept equal). While the two amplifiers drive their own coils (overlap decoupled), the sum of the responses manifesting the effect phase delays appearing on the pickup coil will be observed. This is expected to be basically a complex vector summation as in Eq. 2.47

3.3 MRI Experiments: Dynamic RF Field Modification with On-Coil Class-E Amplifiers

The main purpose of our study is to have a 32-channel(300W each) 9.6kW array of transmit and receive array of coupled amplifiers. The motivation behind this originates from preliminary simulation studies shown in Arghiani's thesis[5]. It is shown that coupled class-E RF amplifiers will have highly efficient modes of operation at certain phase patterns to the channels.

3.3.1 MRI setup

Two amplifiers driving two overlap-decoupled coils targeting a sagittal slice imaging is sent inside the bore. The set-up and its details are illustrated in Fig. 3.2. The pulse sequence is defined in Pulseseq, with FOV=300mm, τ_{RF} =2ms, TR=100ms, TE=6.8ms, readout duration of 3.2ms, and a matrix size of $N_x \times N_y$ =256×256. For two different phase offsets between the channels (at maximum constructive interference and maximum destructive interference), a single sagittal slice image is taken to demonstrate flip angle modification in the depths of the phantom. The slice is aligned at the center of the phantom and located at the overlapped coils' axis of symmetry.

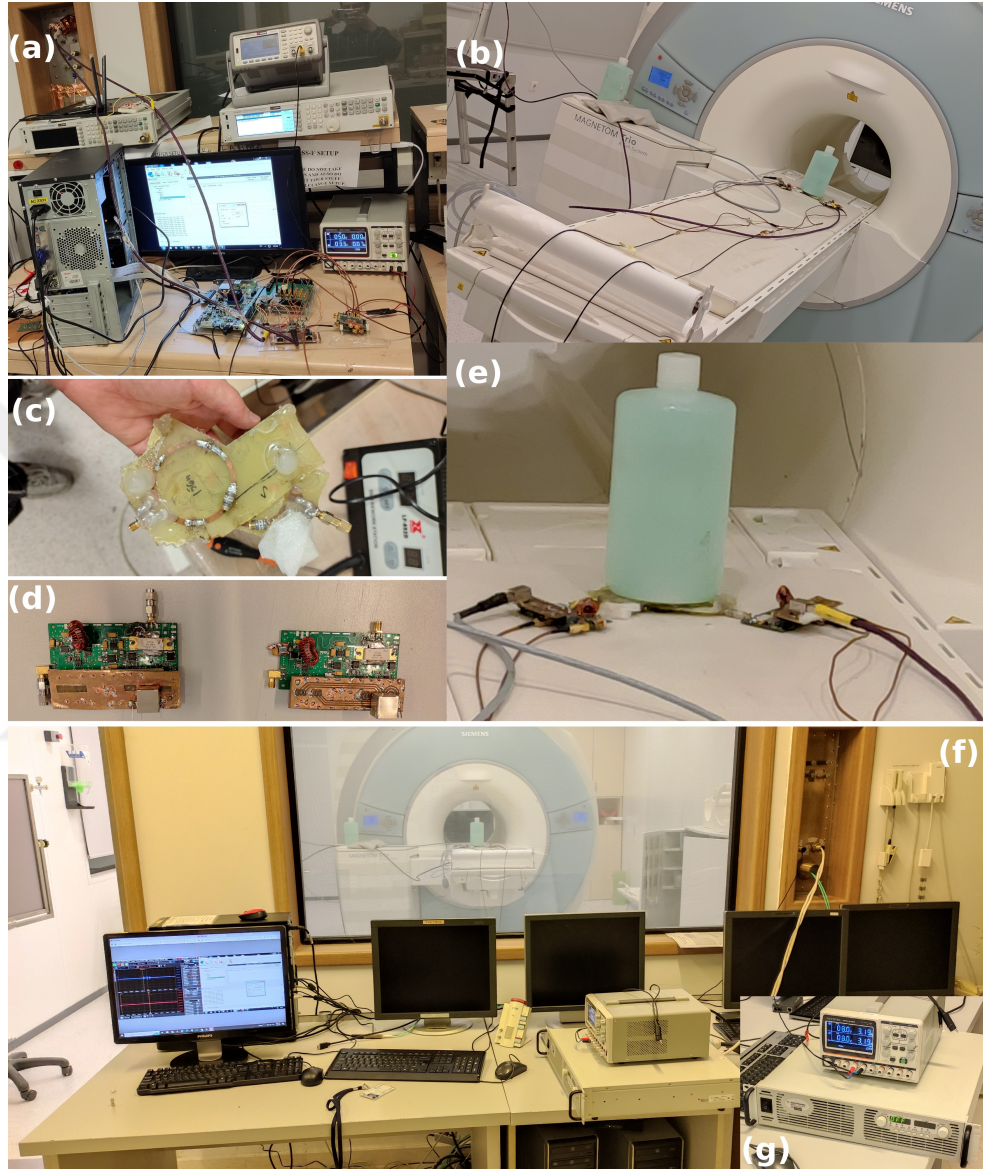


Figure 3.2: Dynamic phase control set-up for MRI imaging (a) FPGA and its PCIE controlling PC, (b) Set-up and cabling in MRI bore room, (c) Overlap decoupled coils, (d) Amplifiers driving the coils, (e) Zoomed-in image of the phantom, coils and the amplifiers inside scanner room, (f) Control room with remote desktop for control of the phase, and DC supplies for the amplifiers, (g) Zoomed-in image of the DC supplies

3.4 MRI Experiments: B1+ Field Mapping with DAM

After solving the glitch issue which creates an line-impulse dents in the k space image, which in turn created ghosts along the horizontal axis, the image data could finally be worked on (Otherwise division between images with artifacts created extremely noisy data). The theory of B1 mapping is given in Sec. 2.5. It is evident from Eq. 2.49 that for a fast gradient echo sequence ($TR < 5T_1$) the need for T_1 data of the subject under test is necessary. Therefore, to have a better idea of where we are in Eq. 2.49, T_1 T_2 and T_2^* maps are extracted for reference. These will be detailed in the sections following the experiment setup.

3.4.1 MRI setup

For the coil, a single loop coil etched on FR4 PCB is used. While loaded with phantom, the coil is initially tuned to optimal Class-E impedance according to the results of Sec. 2.1. The coil is sensitively tuned while loaded with the phantom. For tuning, distributed capacitors are used for better Q-factors and efficiency [20, 21]. While changing the series distributed capacitors, coil input impedance and S-parameters are monitored using Agilent E5061B (Keysight, CA, USA) network analyzer. In this step, it is also important to note that the extra length of transmission line (TL) from the coil port to the drain of the main BLF573 transistor should also be taken into account. This line segment is also marked in Fig. 2.4. Since for the Class-E topology, (without any intermediate matching) we are working with very small impedances far away from the 50Ω origin of the Smith chart, even a small rotational shift (3-5cm of TL $\rightarrow$ 9.4° - 15.6° in FR4 at 123.24 MHz) causes a change in the Class-E load impedance by up to 100% (in terms of load phase and imaginary part; the real part does not vary much, as we mostly stay on on constant resistance circles of 50Ω Smith Chart on the its far left side, while 2cm TL segment is giving a phase shift to the impedance). This is expected as matching and tuning generally get harder as we move away from the Smith Chart's origin. Therefore (missing the transmission line compensation), the final tuned value of output impedance may appear different than Sec. 2.1's load angle results.

For the phantom, a 0.5 gallon (1900mL) 8624186 K2285 standard Siemens phantom with composition $3.75\text{g NiSO}_4 \times 6\text{H}_2\text{O} + 5\text{g NaCl}$ per 1000g of water is used.

For the FPGA RF-pulse frequency input signal, Sec. 3.5's method to get constant amplitude RF from the scanner is used.

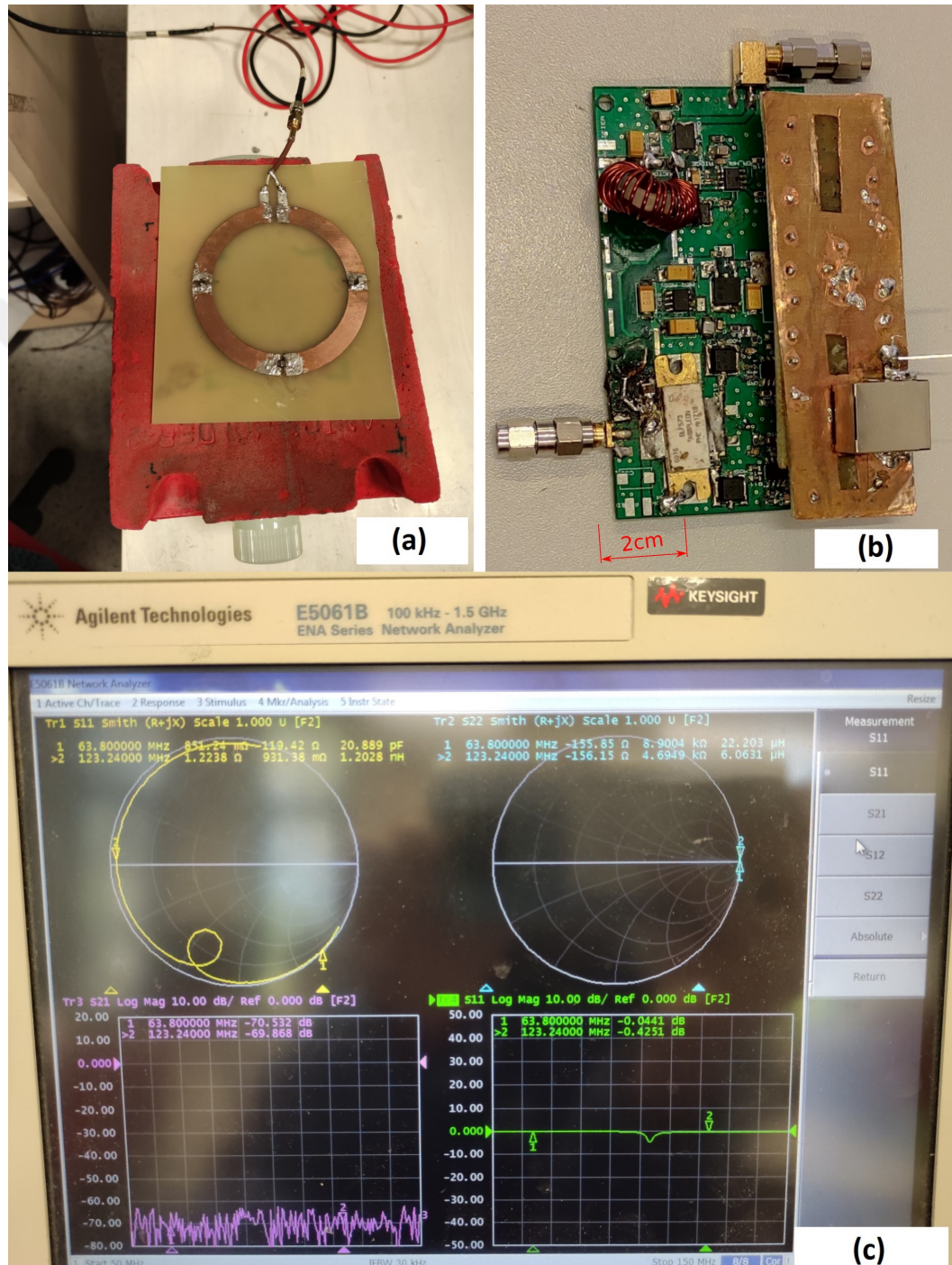


Figure 3.3: Coil tuning and amplifier used for B1 mapping (a) The coil tuned on the phantom (b) The amplifier, (c) Measurement of impedance of the coil (excluding the the 2cm TL path from packaged drain of BLF573 to its SMA connector)

3.4.2 T1 Mapping

For T1 mapping, two spin echo sequences with the same TE (40ms) and two distinct TR parameters (one smaller than the initial guess of T1 (200ms), the other (400ms) larger than that) are employed. The image intensities are then divided to each other to get the T1 weighting. The reason we used spin echo is to get a clear image with the least vulnerability to background noise, as noise in a quotient's denominator can yield the data useless.

3.4.3 T2 Mapping

For T2 mapping, again we exploited the image weighting with two spin echo sequences. Two spin echo sequences with the same TR and two distinct TE parameters (one smaller than T2, one larger than T1) are used. The image intensities are then divided to each other to get the T2 weighting. Common TR value of the images kept sufficiently large as ($TR > 5T_1$) to get high signal values and reduce the effect of noise. Again, the use of spin echo is to eliminate the effect noise as much as possible.

3.4.4 T2* Mapping

In T2* mapping same technique as T2 Mapping is used except with two gradient echo sequences (instead of spin echo) to achieve T2* weighting without the refocusing pulses.

3.5 Replacing MRI Spectrometer with External RF Generator

Pulseseq [37] is used to have full control over the sequence parameters such as the RF-pulse shape (which better be constant amplitude and loss-compensated (high amplitude) since only after after >10m cabling it will be fed to the FPGA after being converted to LVDS logic signals by the LTC6957 (Analog Devices Inc., MA, USA) logic converter board), and RF-spoiling settings. These settings are not straightforward to change in the scanner's own environment. Ease of use in Pulseseq was the main factor in our choice.

3.5.1 Pitfalls of Using Continuous RF generator as Larmor Input: RF Interference at Larmor Frequency

As the following subsections will demonstrate, the main interference source in the experiment set-up is the LTC6957 logic buffer whose outputs feed the FPGA with clock-level information of the MRI's RF pulse frequency. This device should be gated on/off for an interference free imaging when using an external frequency source as the RF-pulse (e.g., the signal generator Keysight Agilent N5171B-501 (Keysight, CA, USA)).

3.5.1.1 Shielding only Solution

The shields of the main MRI Faraday cage and all of the cables in the experiment setup going into the scanner room have been unified. The main contribution was thanks to setting the LVDS RF pulse information carrier CAT7 Ethernet cable's shield unification as shown in Fig. 3.4



Figure 3.4: Unifying LVDS RF pulse information carrier CAT7 ethernet cable's shield with the main MRI scanner room's Faraday cage

3.5.1.2 Gating the RF Generator with RF Pulse Trigger (Unblanking Solution)

The circuit implemented for the purpose of unblanking the RF logic buffer is given in Fig. 3.5. A sensitive NPN BJT (BD675G (Onsemi, AZ, USA)), is used at its base port to detect an active high trigger coming from the trigger source (whenever the scanner needs an RF pulse, this signal is pushed high). Naturally, a level above the $V_{BE-ON} \approx 0.7V$ voltage triggers the BJT. Any level below this voltage is ignored which aims to decrease false detection due to possible

Chapter 4

Results

4.1 PSL Circuit Simulator/Optimizer for Class-E Amplifier Results

Figures 4.1, 4.2 and 4.3 show the results of the 27610 (251 C_s and 110 C_p) combinations of sweep using the fast PSL circuit simulator. The resulting optimal efficiency solution combination of C_s , C_p pairs are in close agreement with the background section of chapter 1. The solution provided a baseline for tuning of Class-E amplifier coil of 3.3.

Despite not being the most efficient case, custom optimization variable provided a decent trade off between output power and efficiency in this model. Compared to most efficient case, only for a loss of 4.5% in efficiency output power showed a 2.5x increase at the output power optimization case. Moreover the optimal point of the optvar design proved closer to theoretical initial guess of Sec. 2.1.1 (194pF initial guess supported by 190pF here). The placement of the custom optimization variable in the C_s – C_p space proved to support a decent lever action between most efficient and most power output states.

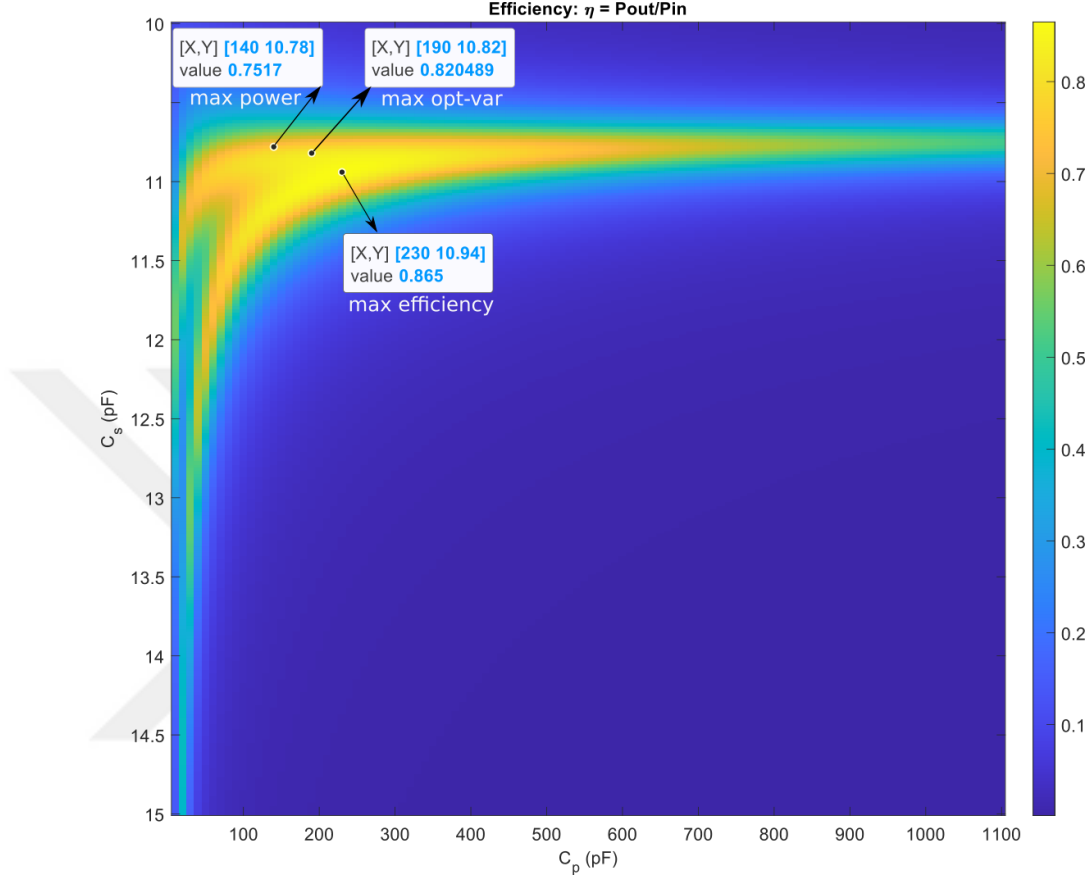


Figure 4.1: Efficiency vs C_s and C_p capacitor values fast scanned using the PSL circuit simulator

The resulting of MATLAB PSL circuit simulator results for the maximum efficiency η , maximum output power P_{out} , and the maximum optimization variable $opt - var = P_{out}^{0.2} P_{out} / P_{in} = P_{out}^{0.2} \eta$ can be found in Fig. 4.4. The translation back to time domain is done using the fast fourier transform (FFT) algorithm (synthesizing the waveform by adding the harmonics described in output $1 \times (2M+1)$ column vectors)

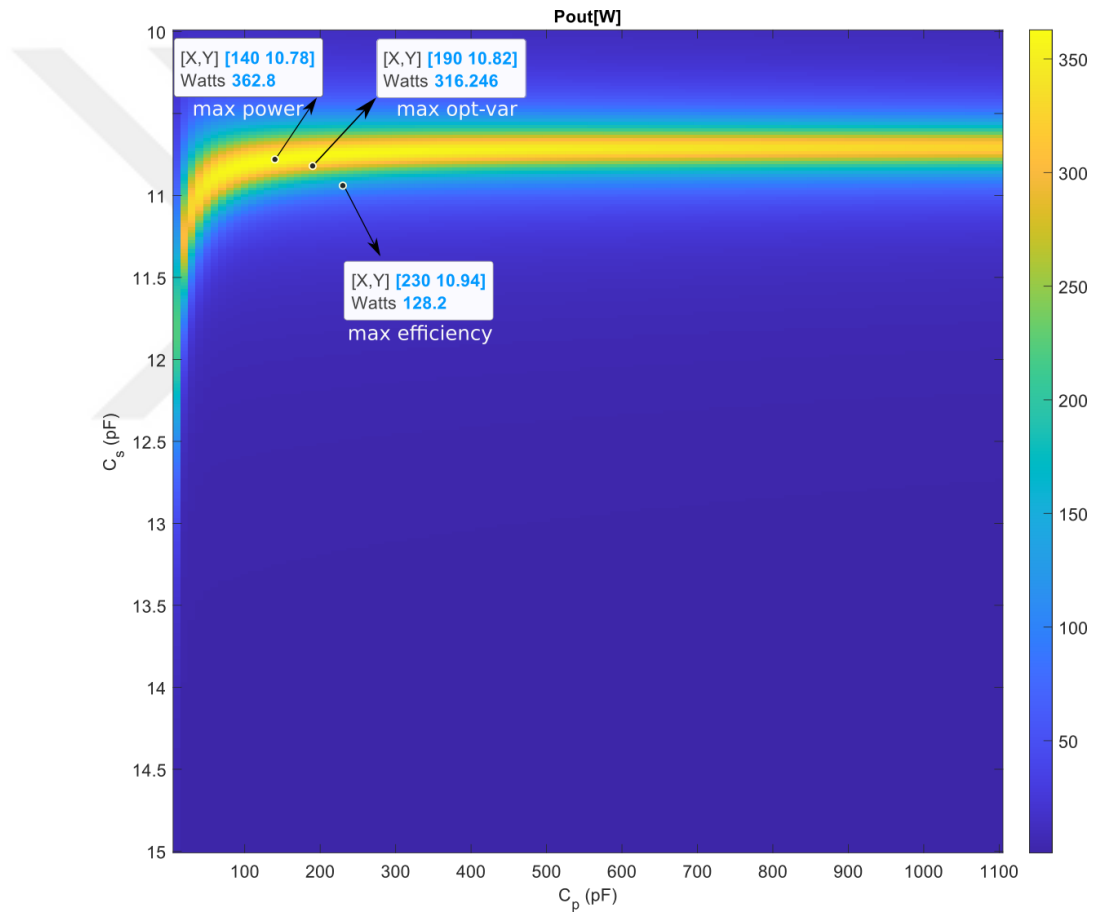


Figure 4.2: Output power vs C_s and C_p capacitor values fast scanned using the PSL circuit simulator

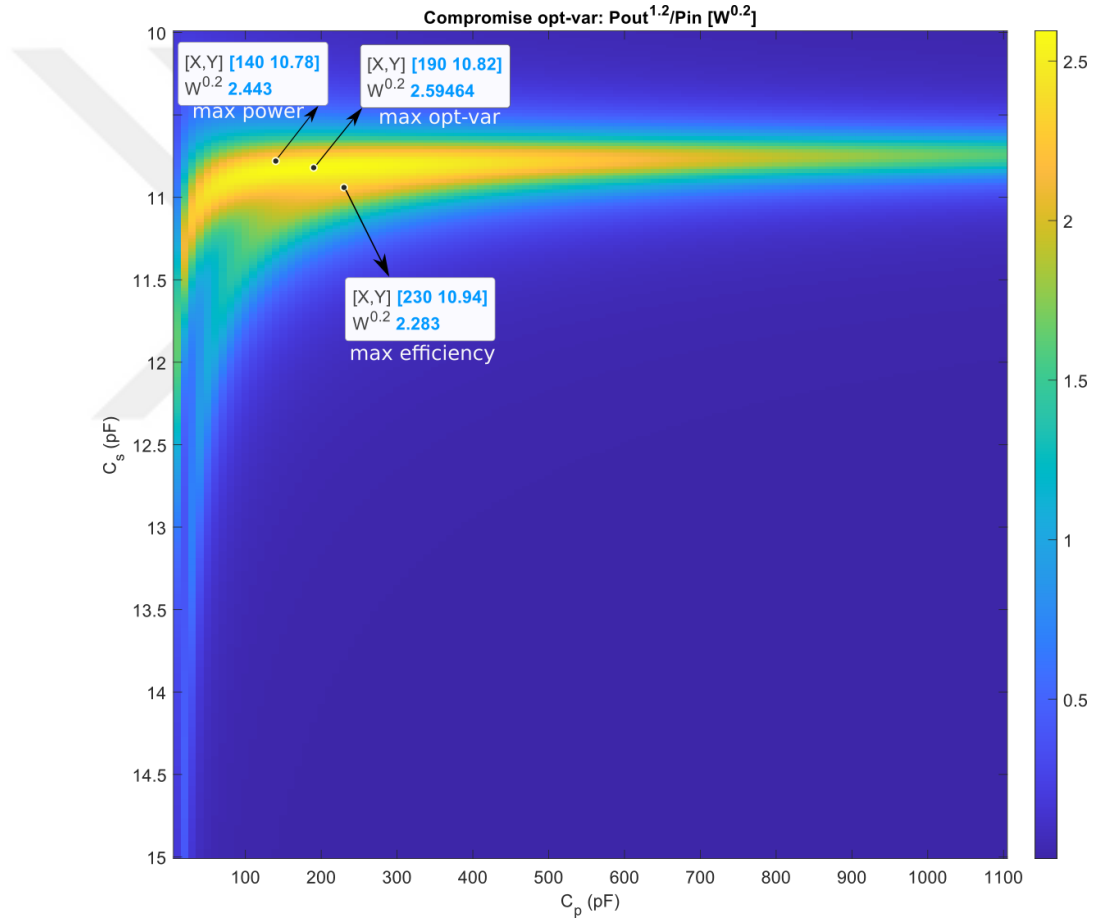


Figure 4.3: Custom optimization variable $P_{out}^{1.2}/P_{in}$ vs C_s and C_p capacitor values fast scanned using the PSL circuit simulator

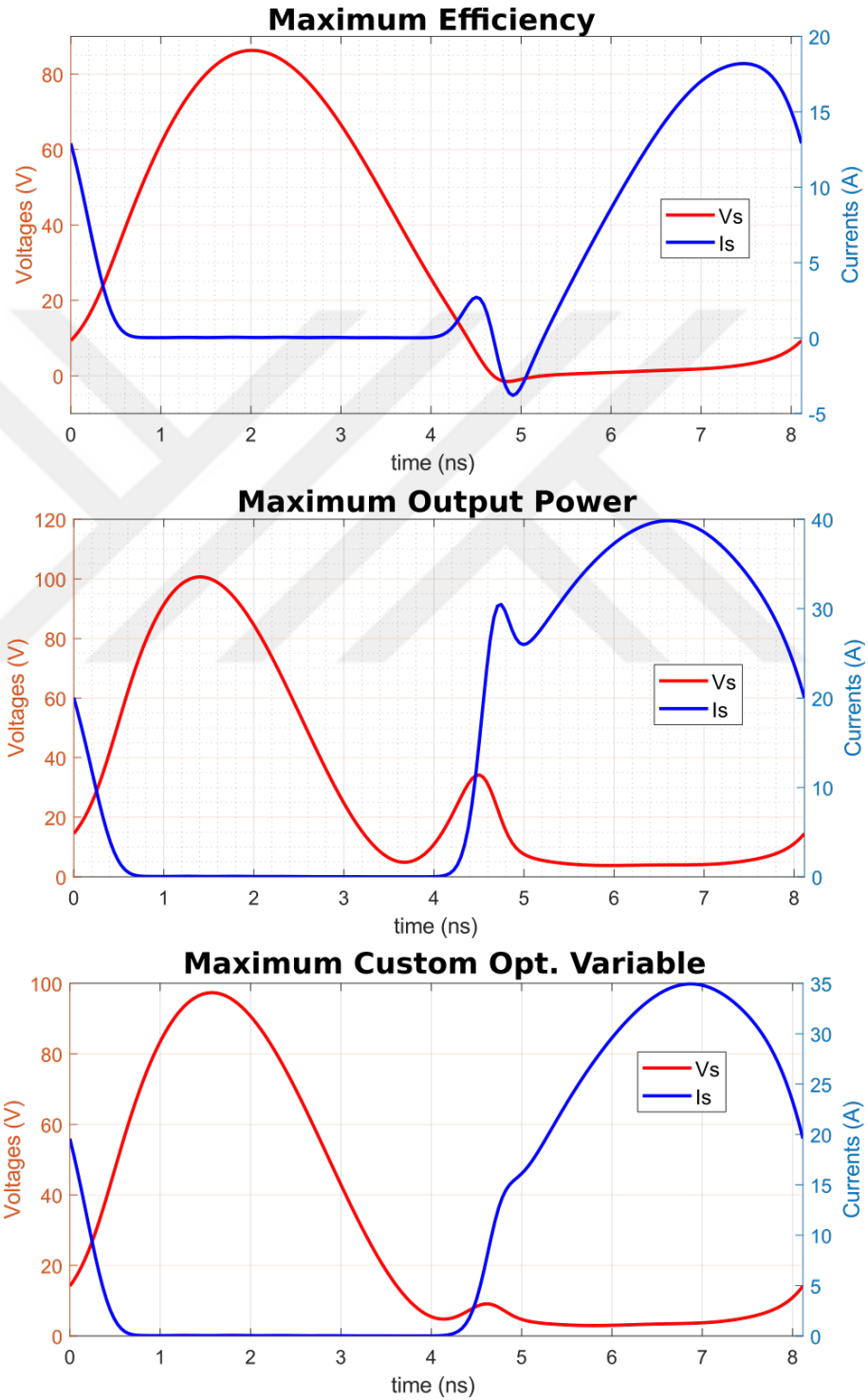


Figure 4.4: Time domain solution results of circuit in switch current and switch voltage using the PSL circuit simulator in MATLAB.

	PSL Circuit Optimizer (MATLAB)			Theory Sec.2.1.1	LTSPICE EPC2036 (realistic)
	Max η	Max P_{out}	Max $\eta P_{out}^{0.2}$	Max η	Max η
C_p (pF)	230	140	190	194	124+75
C_s (pF)	10.94	10.78	10.82	10.83	10.62
η (%)	86.5	75.2	82.0	90.0	80.9
P_{out} [W]	128	363	316	342	366
$\eta P_{out}^{0.2}$ [W ^{0.2}]	2.283	2.443	2.595	2.977	2.634

Table 4.1: Comparison between resulting circuits of 3 different optimization goals ($R_L = 1.22\Omega$, $M = 50$, $N = 15$. Switch Model: $R_{dson} = 100m\Omega$, $R_{dsoff} = 2k\Omega$) $f_0 = 123.24$ MHz. Opt-var = $P_{out}^{1.2}/P_{in} = \eta P_{out}^{0.2}$. Coil inductance: 159nH, $V_{dd}=31V$. Next column is to compare against class-E theory from background equations of Sec. 2.1.1, last column is from the LTSPICE simulation of circuit given in Fig. 2.13 for EPC2036 GaN transistor with realistic driving scheme (with custom SPICE circuit parameter extractor)

The results of the three optimization cases are summarized in Table 4.1. The custom optimization variable draws attention with its close results to the most realistic driver simulation case with the EPC2036 transistor with transient rise and fall time's bearing effect on its continuous transitional behavior between ON-OFF resistances.

One of the conclusive remarks of this optimizer is its speed improvements compared to conventional SPICE based methods. While a single simulation in SPICE would take this amount, here the proposed method leaps forward with over 27000 circuits simulated in the same time interval. SPICE based time domain methods are also restrictive in parallelization of the computation. Iterative time domain methods are heavily single threaded (result of present operation affecting the future chain of events), whereas the PSL circuit simulator is matrix based and can be parallelized much more effectively.

4.2 FPGA Design Results

4.2.1 Before and After the Skipping Glitch: Performance of the Gate Driver

To evaluate the driver's responsiveness, a number of 40 LVDS pulses have been captured over a time interval of 500ms (for a repetition time scenario of $TR=12.5ms$). As illustrated in Fig.4.5 while the previous design missed 2 out of those 40 pulses, the updated design missed none. Furthermore, over a course of 30 seconds the pulse trains have been recorded. The missed pulse count reached over 50 in the previous design compared to new design's perfectly zero miss count.

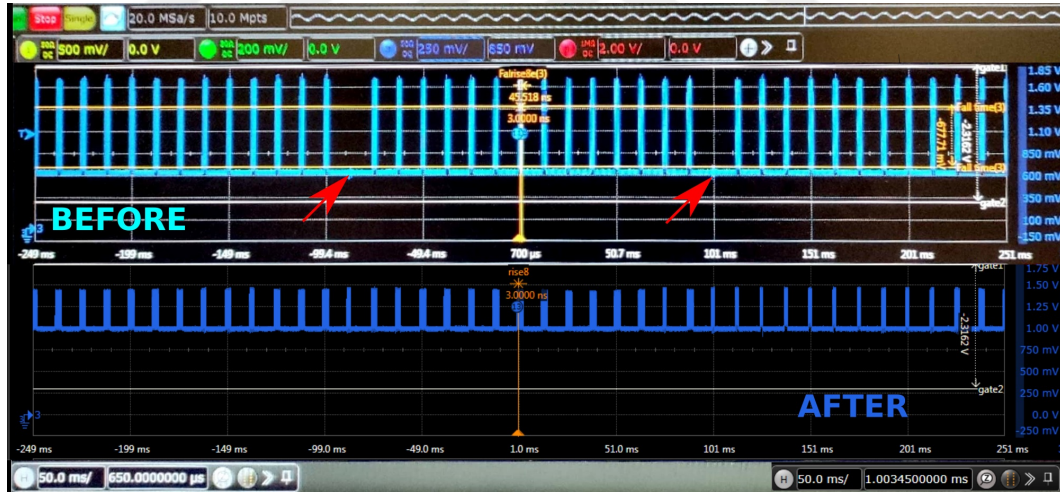


Figure 4.5: LVDS signals of high side gate driver: (top) Previous design which suffers from skipping (marked with red arrows), (bottom) updated design

The effect of ghosting in output images and its removal with this update is shown side-by-side in Fig. 4.6. Another note here is that, although much harder and time consuming, taking MRI images with the glitchy gate driver is also possible (the chance that none of the MRI pulse requests gets missed by the driver.), which was the case for the some of the results in the previous theses [1, 2, 3, 4] results, though, the artifacts in Figures 4.37-40 (especially 4.37, 4.39(a-c) and 4.40(a)) of [4] have clear traces of the pulse skipping glitch.

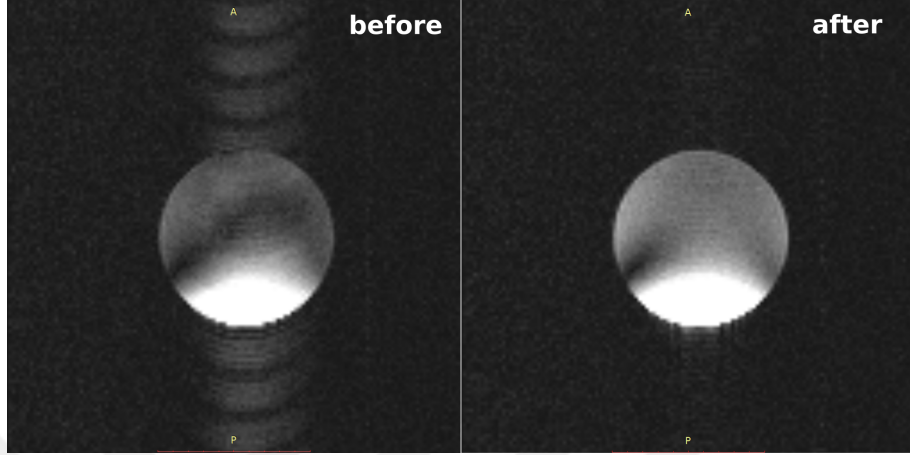


Figure 4.6: MRI images of before and after the FPGA update to the gate driver to solve skipping glitch

Just as we have hypothesized in Chapter 2, the ghosting has one main lobe and saturatingly decreasing amplitude lobes moving away from the centre similar to that of Fig. 2.9. Compared to 1D ghosting of Fig. 2.9, the ghosting manifests itself as 2D replicas of the image along the phase encoding axis (in k_x - k_y space one line of k_x 's is missing at certain value(s) of $k_y = k_{ym_0}$, which results in set of sinc weighted ghosts along y (phase encoding)-axis).

4.2.2 Dynamic Phase Shifting Bench-testing Experiments: Logic Signals and RF Pulse Waveforms

While the phase shift is slowly introduced, resulting LVDS gate driver control signals of the two channels are observed. A 9-bit (0-511) resolution of phase delays in steps of 31.25ps up to 15.97ns is achieved. For the 123.24 MHz case study ($T=8.11$ ns), inter-channel delay results are captured with the DSOS104A (Keysight, CA, USA) oscilloscope. Fig. 4.7 demonstrates a full cycle of phase shifting in channel 2 driver signals with respect to stationary channel 1.

For different phase cases the mutual pickup coil (same distance from each of the coils' isocenter) voltage is also noted for different inputs of phase to observe the interference action. These results are given in Fig. 4.8.

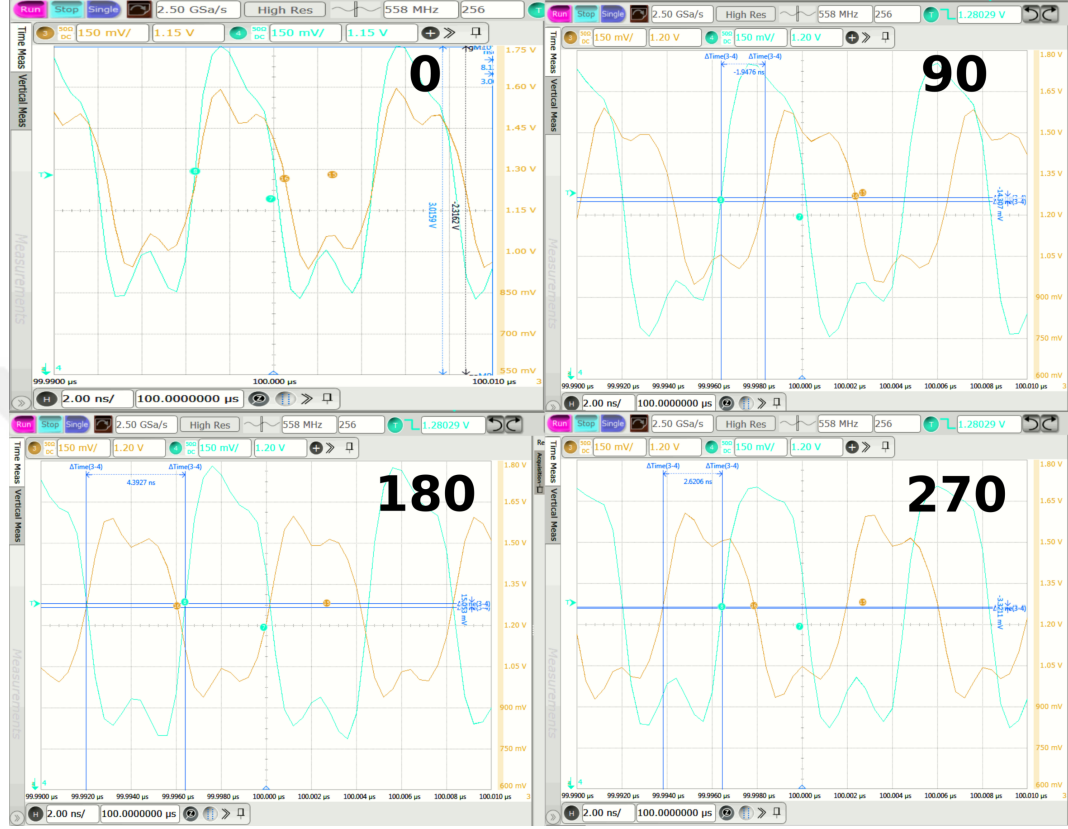


Figure 4.7: LVDS signals of high side driver signals of channel 1 (cyan:stationary) and channel 2 (brown:phase shifting) captured by the scope. With a granularity of 192 steps (00h-C0h:0-192) a phase lag of 270° at channel 2 gate control signals with respect to channel 1 is achieved (1.41° granularity $< 2^\circ$)

It should also be noted that pickup coil samples a different aspect of regions (because of inherently built-in regional averaging due to pick-up pattern of the pickup coil) in space compared to slices captured in MRI (next section).

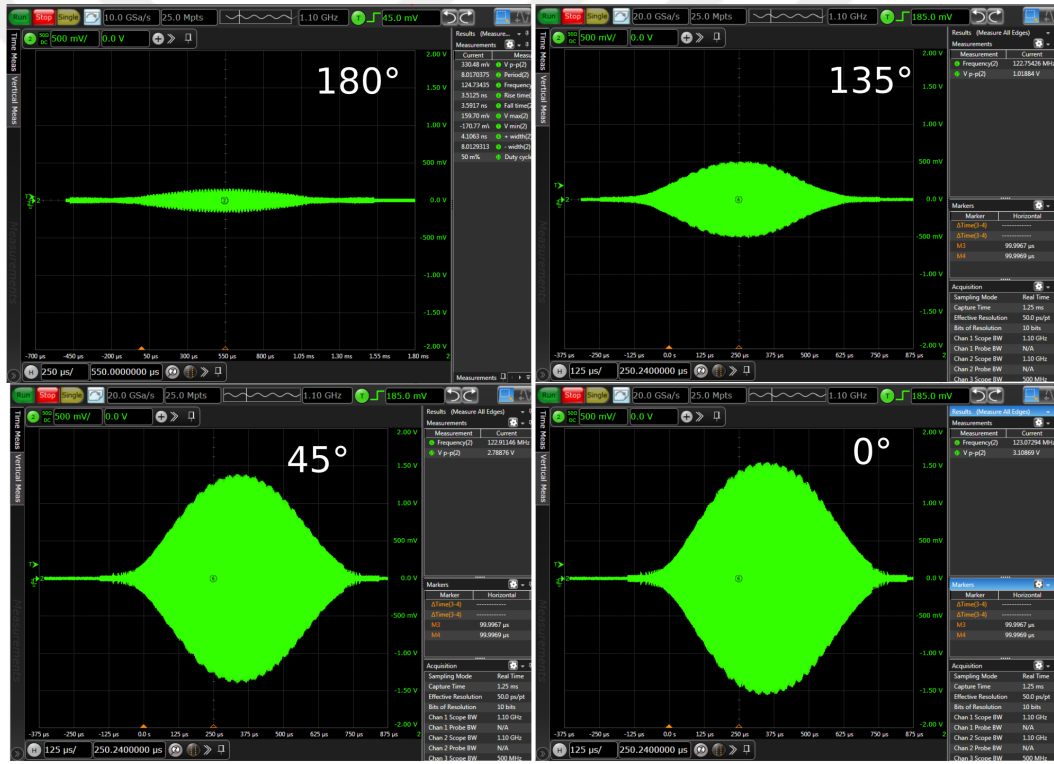


Figure 4.8: Pickup coil probed RF-pulse waveforms for $V_{dd}=5V$, attenuator level=0dB (no attenuation). Under different phase delay inputs outputs effectively summed up on the pickup coil (for the coils of Fig. 3.1)

4.3 MRI Experiment Results: Dynamic RF Field Modification with On-Coil Class E Amplifiers

The resulting images when constructive and destructive interference phases are inputted are shown in Fig. 4.9.

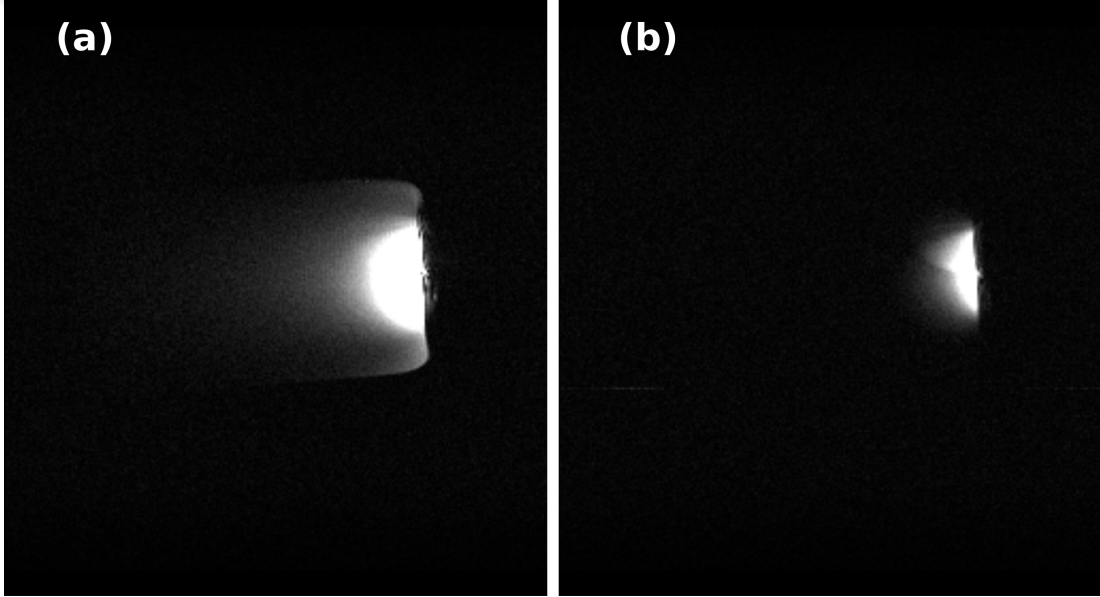


Figure 4.9: Resulting MR images due to (a) constructive, and (b) destructive interference between the channels. (All from the same set-up shown in Fig. 3.2)

The depth of the 90% of peak image intensity moves from 12mm deep in the destructive interference case to 27mm deep in the constructive interference case. Average depth of the 10% of peak image intensity moves from 36mm to 100mm. On top of this low power operation, the amplifier can be placed away from the subject providing more degrees of freedom. While each channel is retaining the 300W output power capability [2] (summation of 600W output capability at tuned phase-shift settings), the power output of the two channel design can be spatially and dynamically modified.

4.4 B1 Field Mapping Results

4.4.1 T1, T2, and T2* Mapping Results

For the standard Siemens 1900mL phantom, division results of the spin echo images and the resulting T1 and T2 maps can be seen in Fig. 4.10. Amongst the two, the most confident (2% variance) results were in T2 mapping with an estimate of $T2 \approx 78\text{ms}$. T1 mapping results showed bias towards the field peak of the TIM TRIO's body coil. For this reason the experiments are repeated for a different orientation of the phantom. T1 estimate stayed within 9% margins of 140ms. T2* estimate on the other hand, showed positive bias towards the edges of the phantom and the experiment again repeated for a different orientation of the phantom. The initial results stayed within 20% margins of $T2^* \approx 40\text{ms}$. The results for the T2* mapping are given in Fig. 4.11. Although the experiment is repeated for different matrix size (reduce to increase SNR) T2* map results had higher standard deviation. There was bias towards the edges of the phantom. One possibility of such phenomenon is the oscillatory edge artifacts, that manifest themselves in an amplified manner when used in image data divisions. Therefore, the inner depths of the phantom produced more reliable data.

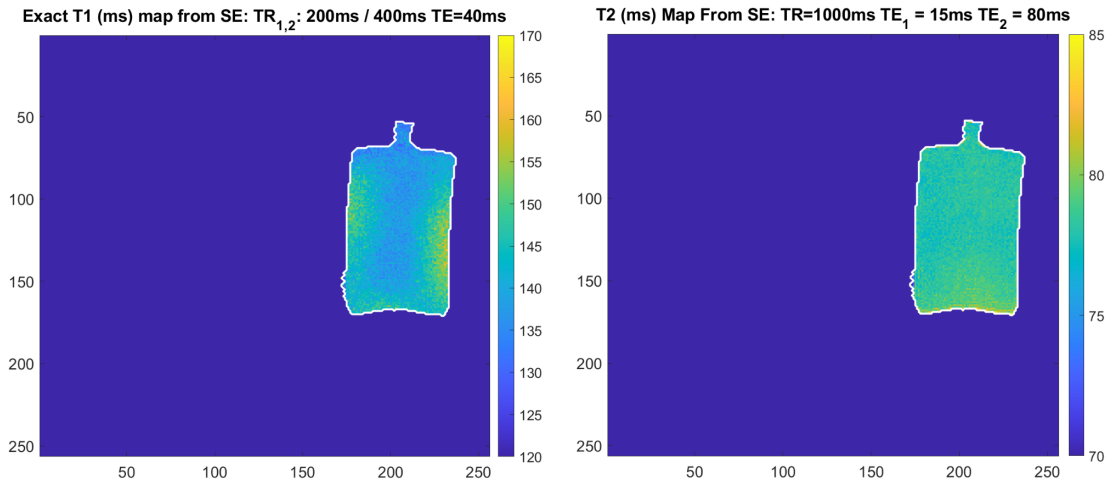


Figure 4.10: T1 and T2 map estimations of the Siemens phantom of set-up of Fig. 3.3

T1 estimate will also be employed in T1 correction equation for short TR

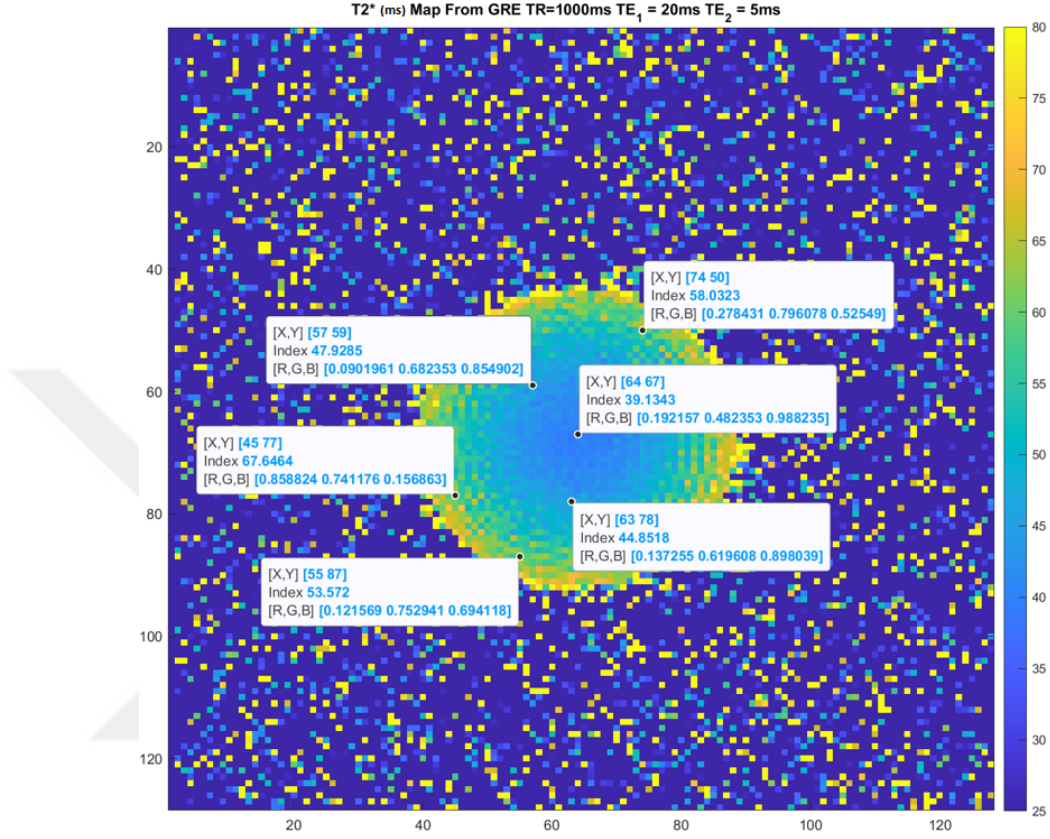


Figure 4.11: T2* map estimation of the Siemens phantom of set-up of Fig. 3.3

B1-mapping estimates of the next section.

4.4.2 B1 Mapping Results

For the loop coil amplifier combination of Fig. 3.3, the estimated flip-angle and B1-maps for the set-up are given in Figures 4.12 and 4.13, respectively.

In Fig. 4.12 the position of the main lobe of field is partially illuminating the phantom.

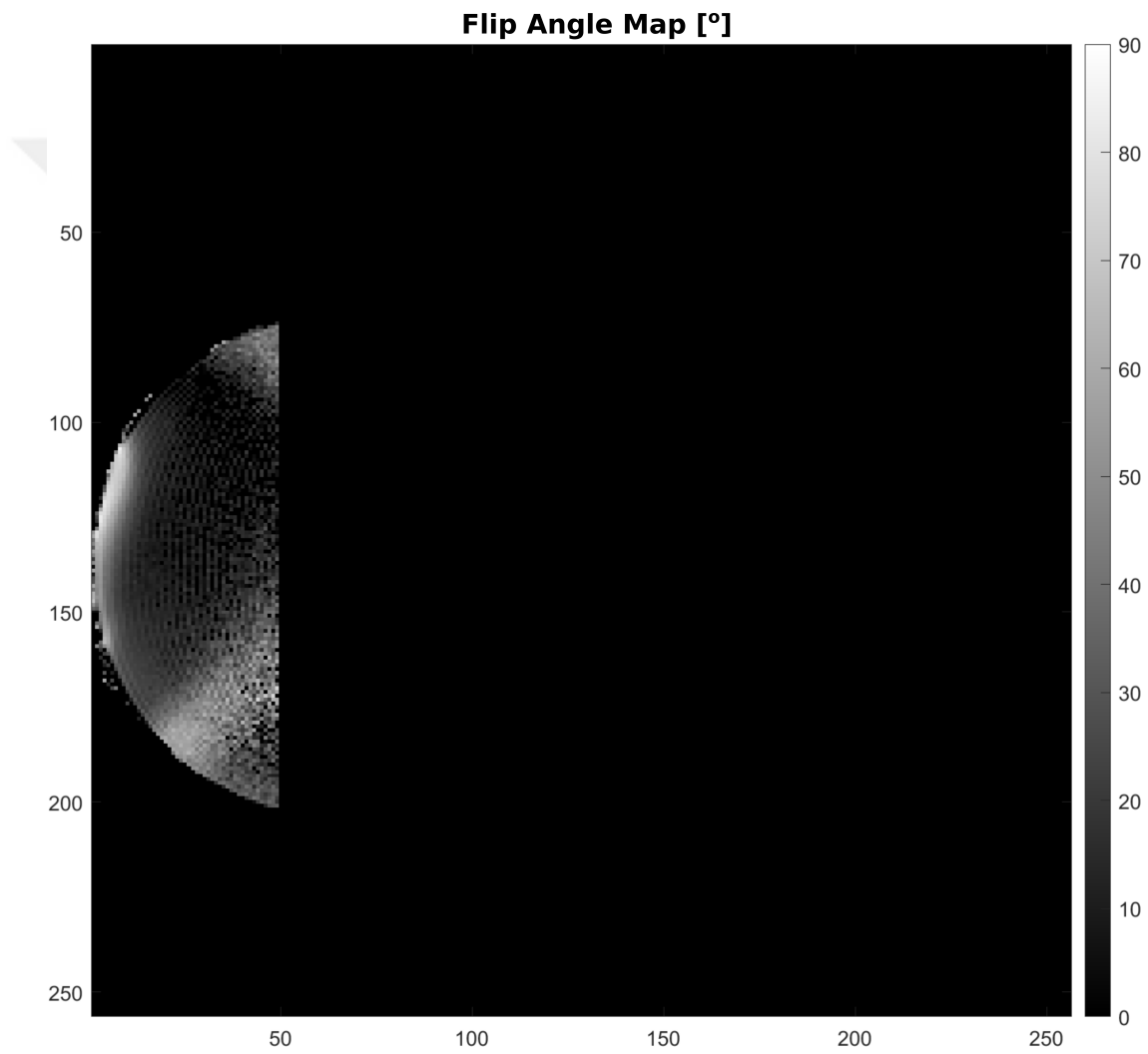


Figure 4.12: T1 corrected flip angle (α) map in units of degrees ($^{\circ}$) at low power operation ($V_{dd}=15V$ $\tau_{RF}=2ms$), using small loop coil of Fig. 3.3

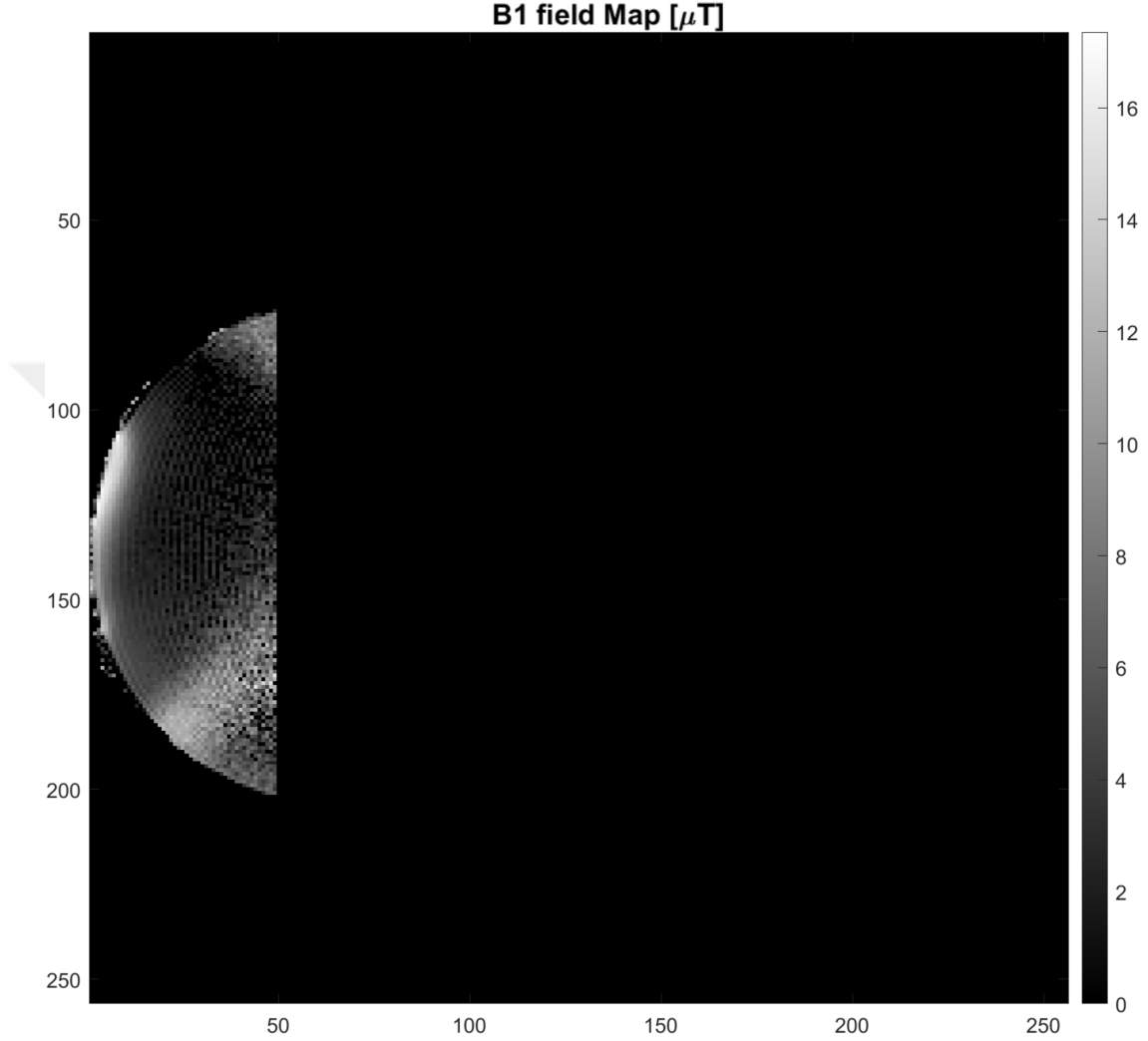


Figure 4.13: T1 corrected B1 field map at low power operation ($V_{dd}=15\text{V}$, $\tau_{RF}=2\text{ms}$), using small loop coil of Fig. 3.3

Note that in Fig. 4.13, the position of the main lobe of field (pixel number: $y \approx 138$) misses the axis of symmetry and is partially illuminating the phantom. That explains why the size of the bright region (most of it illuminating the void space without the phantom) appeared smaller than the case set-up of Fig 3.2, whose phantom is vertical position, its sagittal imaging results are given in Fig. 4.9. The B1 field efficiency is again of the same spatial distribution as B1 and flip angle maps normalized to per $\sqrt{\text{Watt}}$ of the input power. Compared to Fig. 4.13 at $V_{dd}=15\text{V}$ operation, it ranges up to (the peak) $17.4\mu\text{T}/\sqrt{95\text{W}} \approx 1.78\mu\text{T}/\sqrt{\text{W}}$.

4.5 Results of Replacing MRI spectrometer with External RF for Larmor Frequency

4.5.1 Shielding Only Solution

In the case of shielding-only solution, the difference is given in Fig. 4.14.

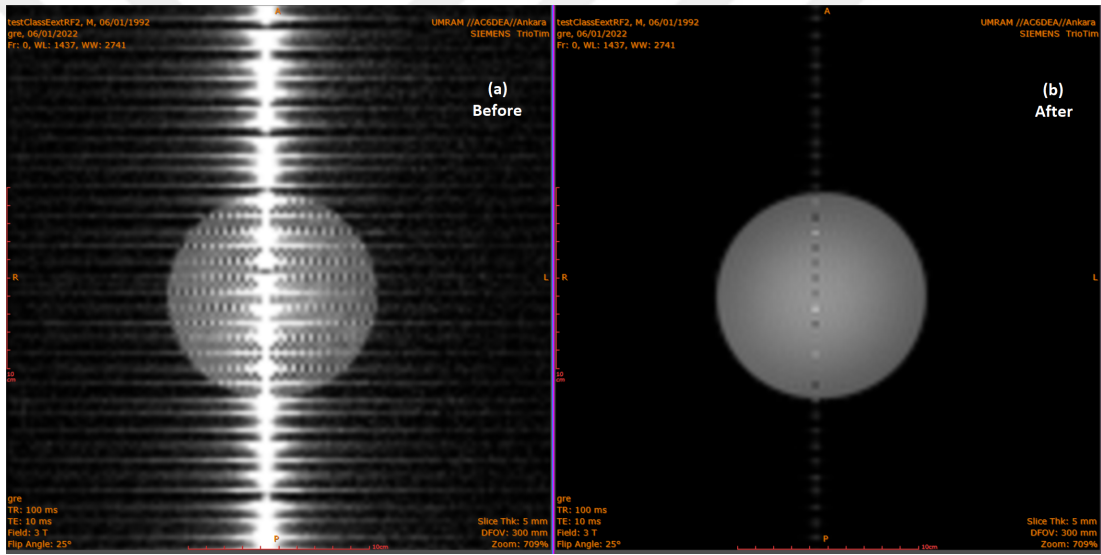


Figure 4.14: Performance of Faraday cage shield unifier solution

Although the performance of such a simple shield connection is remarkable, this was not enough to fully clear the interference. The line interference is still a definite indicator of RF leakage into the scanner room. In the next section RF gating solution will be combined with and the results will be evaluated.

4.5.2 Combination of Shielding and RF Transmit Gating Solution

The gating circuit's resulting output logic signal and the resulting output RF pulse and the BLF573 transistor's drain voltage ($V_{dd}=5V$) is given in Fig. 4.15. In the experiment stage we noted an output pulse peak-to-peak voltage scaling due to a voltage dropout on the output stage PNP transistor. To counter this effect, we increased the initial main supply voltage level to (only in short pulsed mode) 5.9V to guarantee satisfying full scale pulsed operation of the logic buffer.



Figure 4.15: RF gating method signals for a 1.25ms RF pulse from top to bottom: (yellow) 3.2x scaled version of logic buffer output signal, (green) output RF pulse sensed by the pickup coil, (blue) V_{ds} voltage of the Class-E amplifier, (red) Output voltage level feeding the logic buffer

On top of the shielding methods, RF gating circuit is employed. The resulting image comparison is made in Fig. 4.16. In MRI, a straight line of interference denotes a single frequency interference with varying phase. When we changed the RF excitation frequency, this line moved left and right as many pixels according to the the pixel bandwidth of the image .

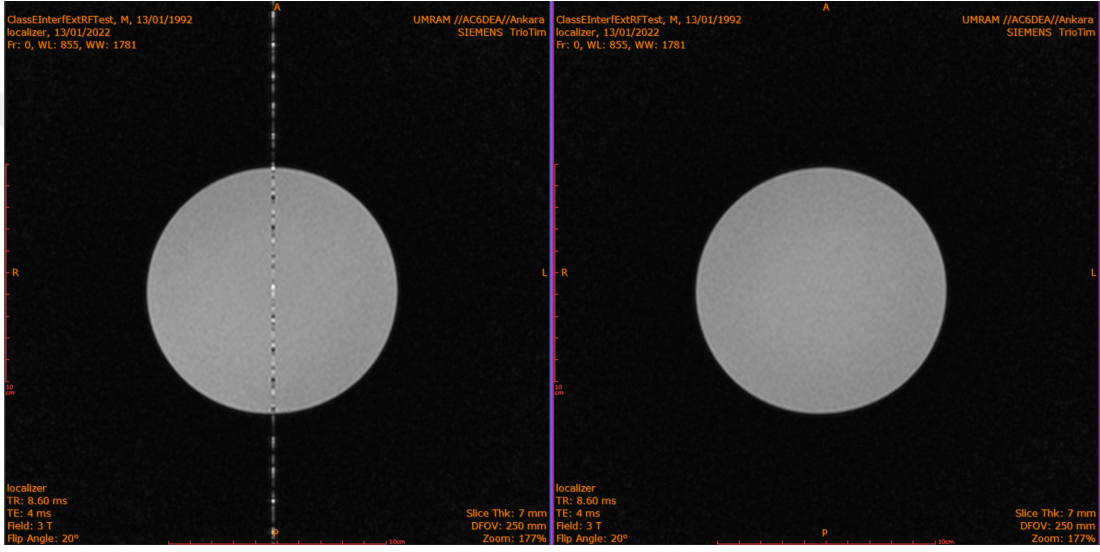


Figure 4.16: Performance of RF gating method solution (left side image: before) (right side image: after)

4.5.3 Final Images After Clearing Interference

For short sequences we managed to get clear slice images. There are artifacts of ghosting visible for rather long sequences (> 10 minutes) as shown in Fig. 4.17. We suspect this artifact is due to the phase drift of the RF generator. This hypothesis is supported by the fact that the drift is expected to be less in a shorter time-span (i.e., as it was the case in our shorter ($TR=100ms$) sequence results of Fig. 4.18).

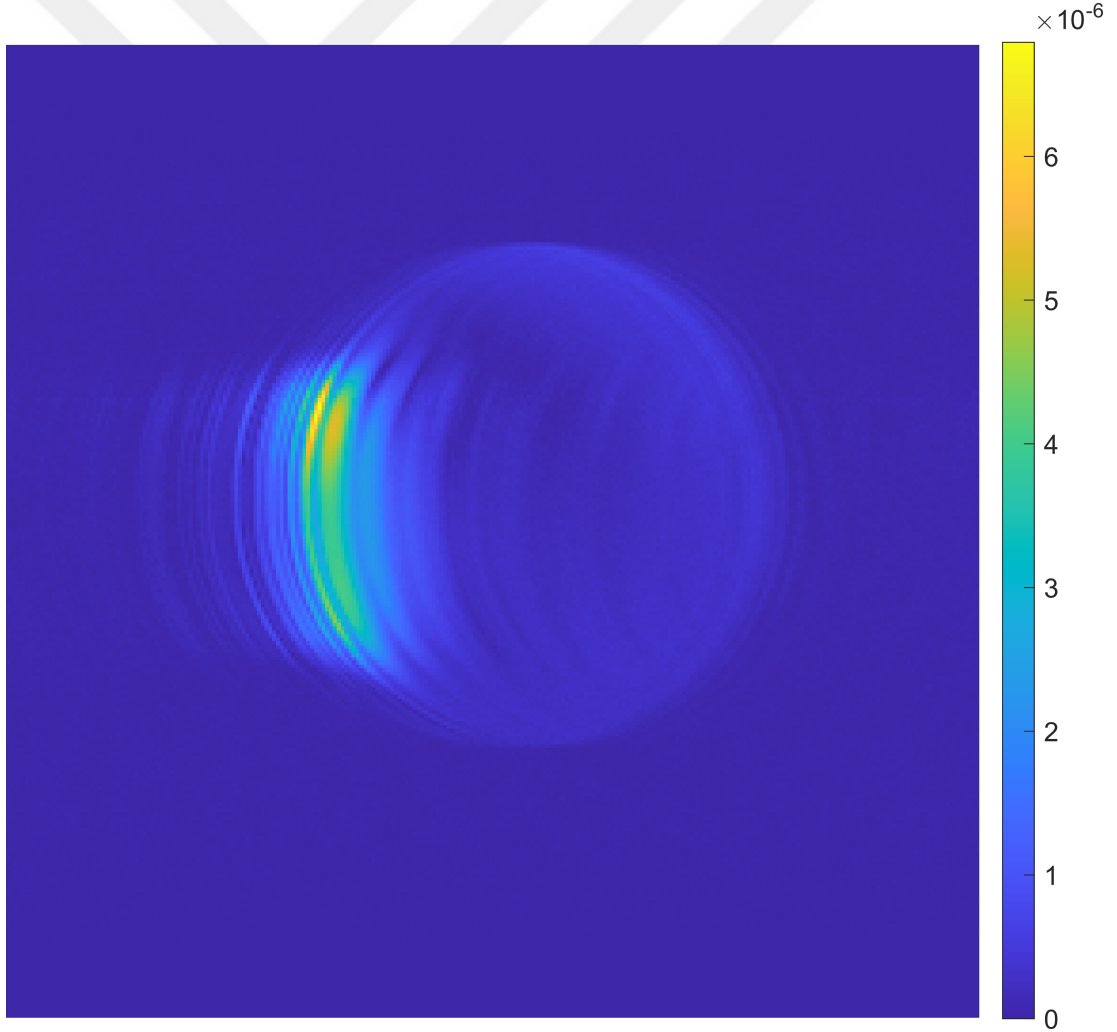


Figure 4.17: Ghosting artifact example while using external RF generator as the RF-pulse frequency input. This was only the case in long sequences ($TR=2000ms$)

Slice selection performance is demonstrated using fruit imaging (of the loquat

fruit) while RF input external frequency is shifted by 110Hz and 1100Hz is shown in Fig. 4.18. As necessitated by the pulse sequence's generated slice selecting z-gradient parameter (33.3 KHz/m) for a 1.1 KHz shift we have approximately $0.033\text{m}=3.3\text{cm}$ shift in the selected slice. Since this distance is almost as large as the radius of the loquat fruit, at the bottom of Fig. 4.18, the slice barely touches the juicy parts of the fruit (mostly its shell) and the signal is smaller, being emitted from a smaller mass of spins (the higher the slice mass (in terms of hydrogen content), the higher the signal). One other reason the signal is smaller there is that the RF coil's transmit pattern favors the middle of the loop coil where the center of the fruit resides.

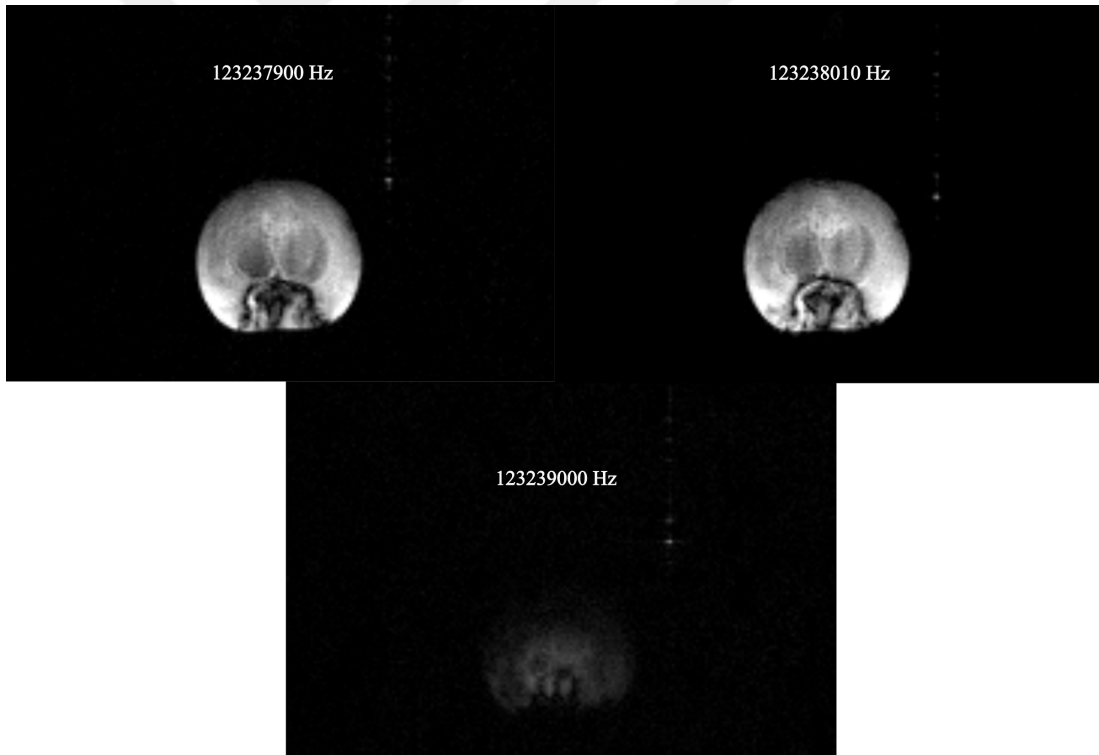


Figure 4.18: Demonstration of slice selection using external RF generator in a fruit (loquat) imaging example

4.6 Nonlinear Transistor Drain Capacitance: LTSPICE Simulation Results

The LTSPICE simulation results case with voltage dependent nonlinear capacitance, and its comparison with constant capacitance case will be detailed. The results are given and compared for the same class-E amplifier topology in 2.1 for coil inductance of $L_s=589.92 \mu\text{H}$, coil tuning capacitance $C_s=2.7565\text{pF}$, load $R_L = 1.614\Omega$, $L_{ch}=5 \mu\text{H}$, $V_{dd}=31\text{V}$, switch on resistance $R_{dson} = 90\text{m}\Omega$, $C_p=135\text{pF}$, and switching frequency $f_0=125 \text{ MHz}$. The waveforms of linear vs. nonlinear (voltage dependent) parallel C_p capacitance cases are given in Fig. 4.19 (for $V_{dd}=31\text{V}$). We note here that the nonlinearity property also interferes with and disturbs the tuning of the amplifier. Although this change may at first appear impactful, there is only a 2% reduction in efficiency. Also, in real-life cases, we rarely see these kinds of capacitor discharge current surges as in the bottom of Fig.4.19 since their equivalent series resistance (ESR) will greatly limit those.

With the nonlinear capacitance of model of Sec. 2.1.2 accounted for, in SPICE simulations in the high-voltage input case ($V_{dd} = 31\text{V}$), the resulting efficiency decreased by 2%, input (+6%) and output (+4%) powers increase, while the power dissipated by the switch increases by 18%. The most notable change was observed in the switch peak voltage, which increased from 107V target in the linear capacitance model to 172V in the nonlinear model. On the low voltage V_{dd} input case (5V) the jump in switch voltage was only from 17.3V to 26.2V. This is expected as at the lower voltage operation of 5V in Fig. 2.6 the higher capacitance slows the voltage change and the peak can now build up to a reduced voltage.

The most notable characteristic change in the shape of the drain voltage is in its overshoot and shrinkage on the time axis. High capacitive regions (marked with circles in Fig. 4.19) tend to suppress voltage levels more, compared to low capacitive parts in the middle parts of the drain voltage. This composes its shrunk shape, while making it shoot up to a higher value at its peak. This particular modeled LTSPICE 2.6 nonlinear capacitance case has a non-ordinary

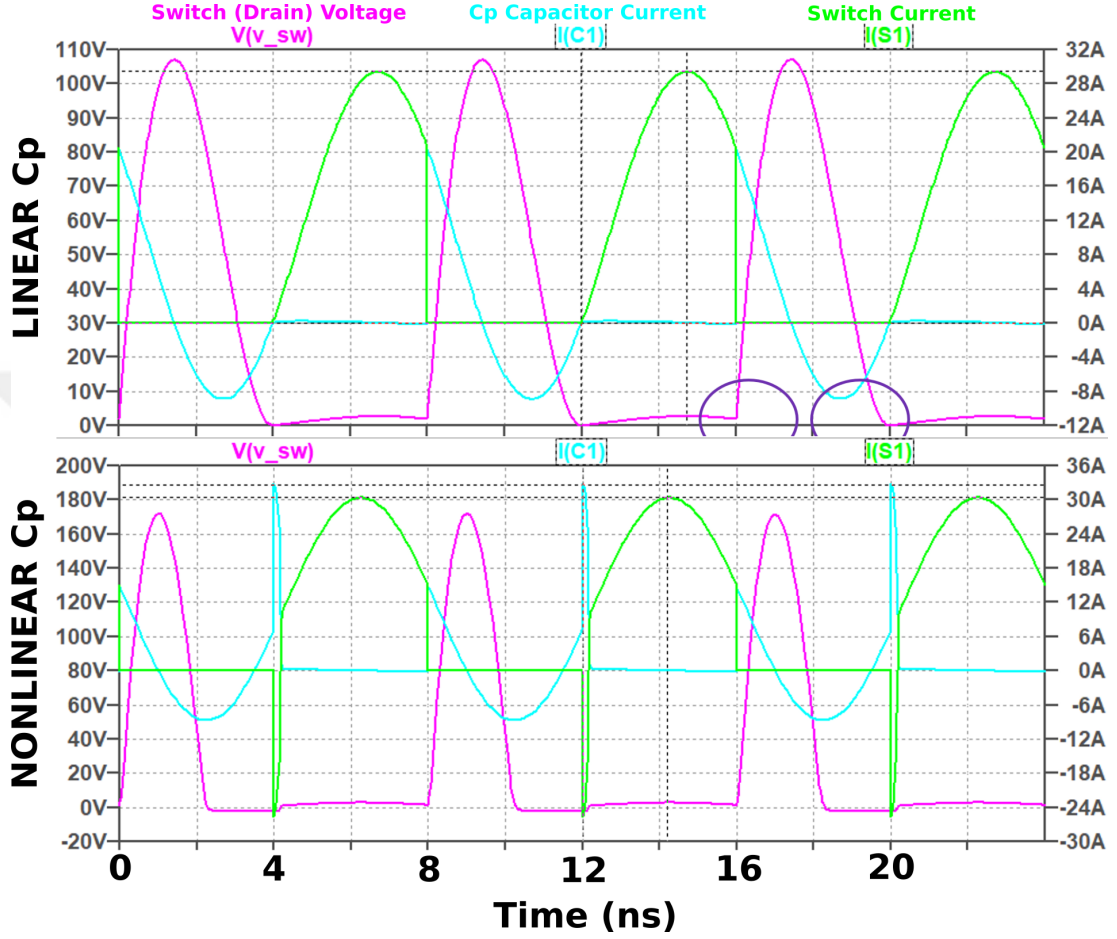


Figure 4.19: (top) Linear C_p capacitance case, (bottom) the same case components are kept the same except adding voltage dependency property of Sec. 2.1.2 to the C_p capacitor.

shape when it comes to its high power output and efficient solution. After some more examination, we saw that this fit is not doing its job properly. As we look at the region beyond 50V data range, we see that the capacitive fit goes all the way down to zero as shown in Fig. 4.20, this is troubling news as such low values of this capacitance is not realistic. We need to look at the fit on a larger data scale. The two-term exponential fit is not enough.

To correct the error shown in Fig. 4.20, the quoted convergence value of the output capacitor is padded at the end of the data vectors. Beyond 50V up until 310V the capacitance is assumed to adopt the constant value of 100pF. The fit also made to include a term with xe^{-kx} type of behavior, as follows in Fig. 4.21.

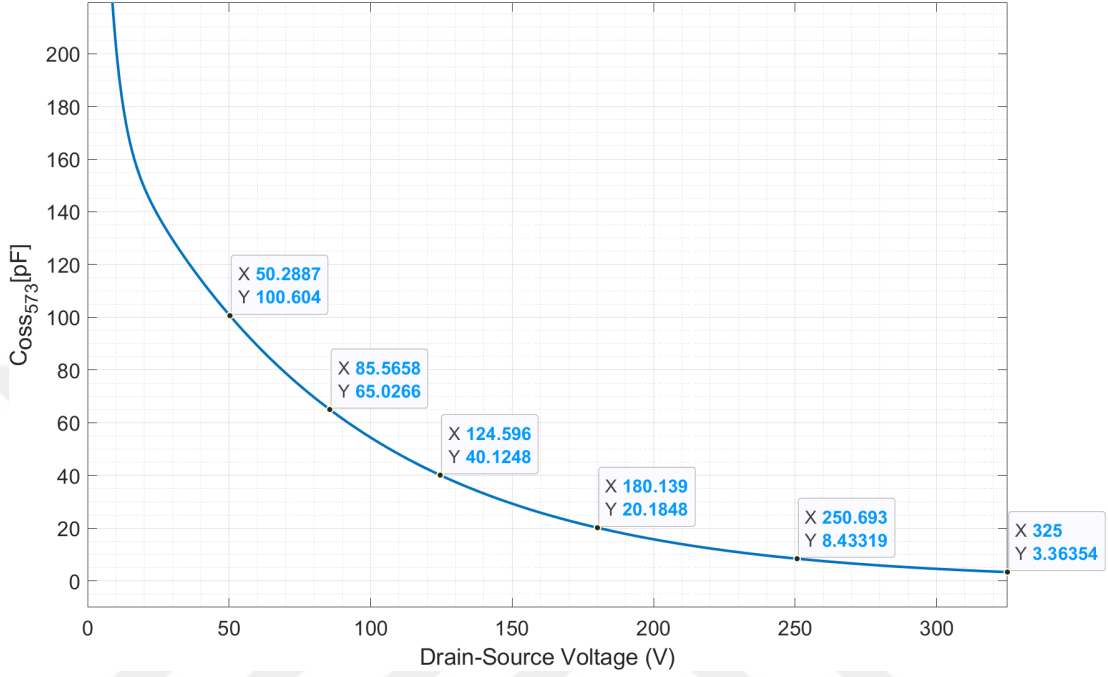


Figure 4.20: Extended look at the limited range (0-50V) (erroneous) curve fit of Sec. 2.1.2. Although the fit was decent within the data range, values beyond the fit-range are extremely unrealistic even ranging down below 20pF.

Table 4.2: Custom 3-term modified fit parameters of Eq. (4.1) Please note that $E=100\text{pF}$ is now actually inclusive and defining the high voltage state converging capacitance

A	B	G	D	E	F	K
424.7	-0.3567	189.3	-0.06978	100	-871.1	-1041

The fit equation translated into the capacitance equation is given as in Eq. 4.1.

$$C(V) = 10^{-12} \times ((E + Ae^{BV} + Ge^{DV} + FVe^{DV}/K) \quad (4.1)$$

where the fit constants A , B , G , D , E , F and K are given in Table 4.2.

The RMSE value of the new fit is 11pF, slightly worse than the first case study of Fig. 2.6, but this time with much better coverage. Integrating Eq. 4.1 with respect to voltage yields Eq. 4.2, which describes the capacitor charge form that can be entered directly into LTSPICE. Notice that any linear term here represents the linear constant capacitance component of the total C_p capacitance of Fig. 2.1.

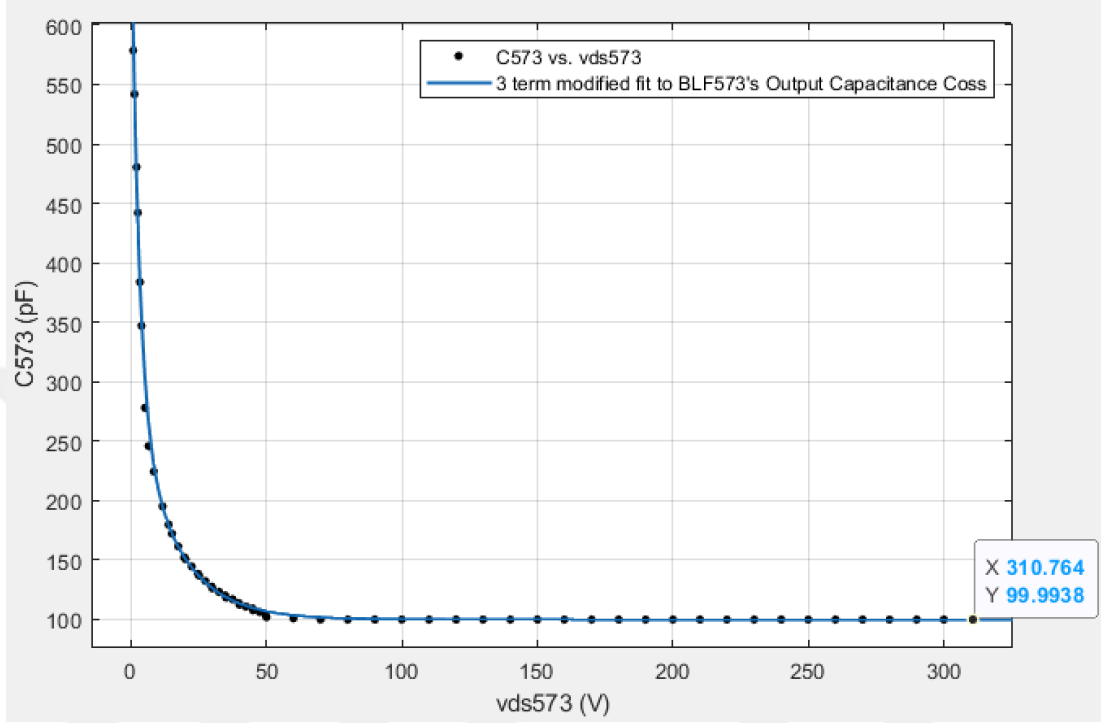


Figure 4.21: New fit also considering the convergence of C_{oss} by employing padded data beyond the scale of datasheet values. The new fit has an RMSE value of 11pF

$$Q(V) = 10^{-12} \times (C_1 V + 100 \times V - 1190 \times e^{-0.3567V} - 0.05769 \times e^{-0.06978V} - 11.99 \times V e^{-0.06978V}) \quad (4.2)$$

where C_1 again represents the externally added capacitance ($C_1 + C_{oss} = C_p$). The final results of the LTSPICE simulations with the corrected model is given in Fig. 4.22.

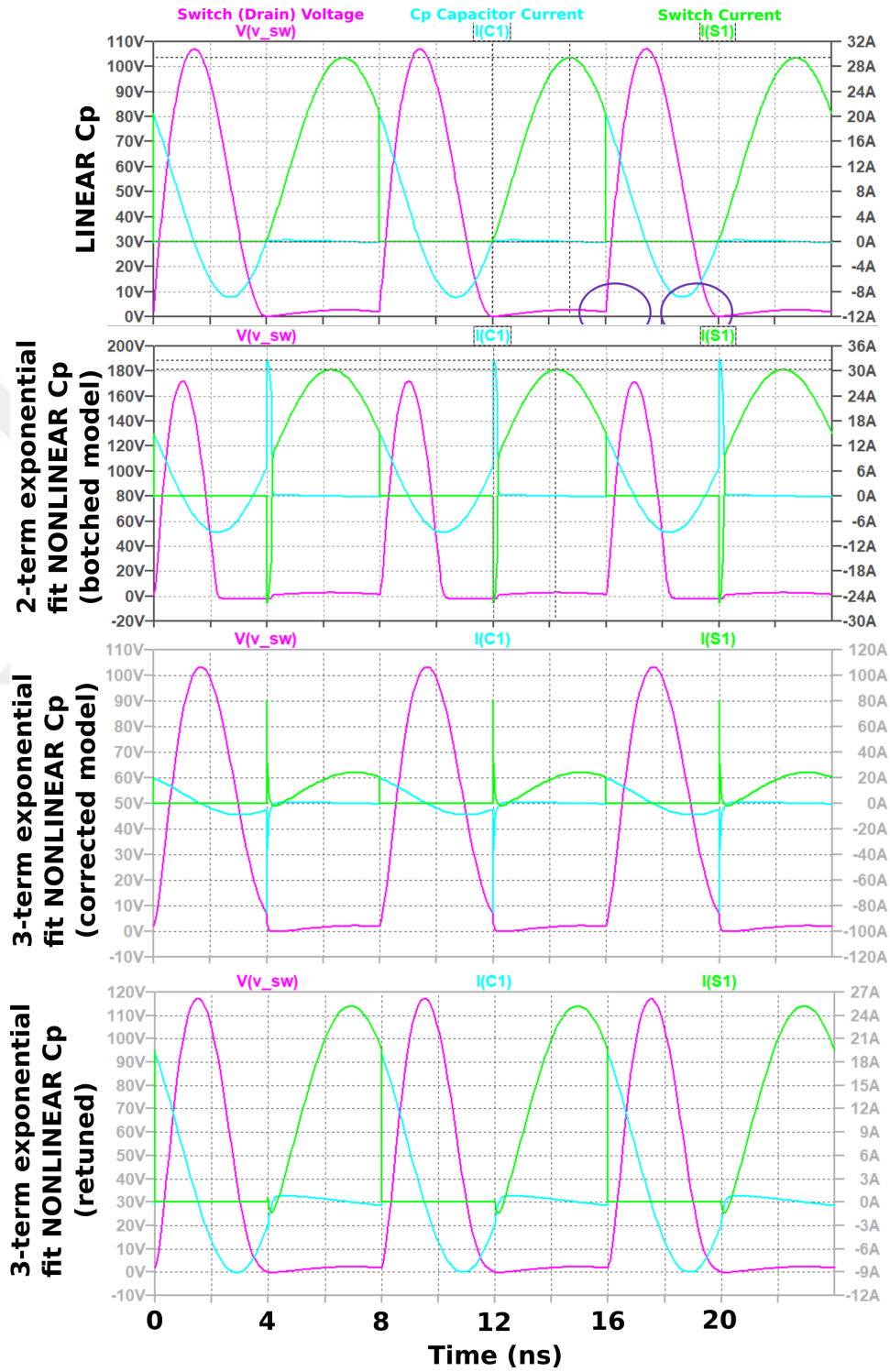


Figure 4.22: Results of new fit in comparison with misleading old fit, the new fit also retuned to very close to original values. In the bottom-most case: The resulting additional capacitance had to be set to 0pF. This showcased the 100pF convergence capacitance taking the entire job of the amplifier's C_p capacitance.

Final results to achieve a re-tuning with the nonlinear capacitance case needed additional (waveforms are very sensitive to the value, hence the detailed significant figures) 0.123% of the base capacitance value of the series C_s compared to the starting design (changed from 2.7565pF to 2.7599pF). The most notable change was in the C_p capacitance which needed no capacitance except the one characteristically inside the BLF573 MOSFET (high voltage the built-in 100pF capacitance of the model took over the job) from 135pF starting value linear case. Thus, the amplifier did not even need an external C_p capacitor. This result can be interpreted as (135pF to 100pF) 26% reduction of linear capacitance component. Unlike the limited-range erroneous model, the corrected model shows that the situation is not that grim. The results are as follows (again, using the SPICE circuit parameter extractor described in 2.13). With the new corrected non-linear voltage dependent capacitance of model of Sec. 2.1.2 accounted for, in SPICE simulations in the high voltage input case ($V_{dd}=31V$), (again, compared to the linear capacitance base case) the resulting efficiency stayed within margin of error, the input (-24%) and the output (-23%) powers decreased significantly. The power dissipated by the switch decreased by 35%. The switch peak voltage jumped from the 108V for the linear capacitance model to 117V in the nonlinear model.

On the low voltage V_{dd} input case (5V), interestingly as expected, the non-linear model lost its initial high voltage tuning point almost completely. The amplifier could not be re-tuned because the switch capacitance was already intrinsic to the transistor, which could not be modified. 100pF base capacitance behavior was completely lost, at low voltage values the drain capacitance started to behave like the far left end of Fig. 4.21. With increased capacitance, which forced a much lower value of X_{C_p} of Eq. 2.23 due to their direct link (0.1836 constant for $D=0.5$), the tuning for the load of 1.614Ω was not possible without changing duty cycle.

One conclusive remark of this section is that the nonlinear C_p case still warns the designer that the switch voltage is actually jumping to a higher value than is initially guessed. Thus, the importance of leaving sufficient tolerance in breakdown voltage-bound designs is stressed. The other remark is that tuning at low

voltage cannot be applied to high voltage operation without making a modifications. The path of this work gains extra importance if we also consider that previous designers [1, 2, 3, 4] in the line of this work heavily depended on tuning at the low voltage case (typically at 5V V_{dd} drive due to the limitation of probe maximum voltage of 20V for N2795A (Keysight, CA, USA)).



Chapter 5

Discussion and Conclusion

About the previous line of designs, the reason we are not reaching a good threshold voltage (and the rise and fall times of the gate voltage appear exaggerated) in Fig. 2.12 is because of the fundamental fault in the gate driver topology [1] of the old design. The reasons for this is given in Sec. 2.6. For example, for the BLF573 transistor to act as its R_{dson} value of $90m\Omega$ it needs voltages well above $(2 + 3.75 = 5.75V$ [23]) its rated threshold voltage given in Table 2.1. Half bridge driving cannot be achieved by merely feeding inverted signals into two series NMOS MOSFETs. For the high side, a conventional half-bridge driver would take rise in the gate voltage (which is the ground of high side) into account and over shoot (up to $>9V$ which is $4V$ above nominal $5V$ gate turn on voltage) the high side NMOS gate preemptively to tackle this negative feedback on the charge path. The previous designs was faulty in this aspect, hence the gate voltage never reached $5.5V$ peak target value[1, 2, 3]. We expect this to increase effective R_{dson} and degrade efficiencies especially at low load cases (high coil to phantom distance) according to Eq. 2.26.

It is also important to have some words about the equivalent series resistance (ESR) of the supply modulation block's parallel reserve charge capacitors. No matter how powerful our supplies are, since there is a long transmission line (≈ 10 m) that has to be travelled by that voltage, during strong RF pulses especially at

high power operation, the amplifier becomes limited by the tantalum capacitors (of $10\mu\text{F}$, and $22\mu\text{F}$ TAJ series [39] (Farnell, Leeds, UK)). These reserve capacitors are non-magnetic and MRI safe but their ESR's are not remarkable. When the low ESR 1nF block capacitor's charge depletes (that can happen at high power draws) this raises a problem. One amplifier suffered from this at high voltages and struggled to keep up. This remains as another type of deficiency to be addressed in the future that might be resolved by updating capacitors with better candidates or using droop compensation methods for amplifiers with or without feedback (theory of [40], counterpart for RF amplifiers).

The course of this work also revealed one of the main pitfalls of failure of our amplifiers. For magnetic evaluation of the amplifier boards (for possible ferromagnetic parts/impurities causing artifacts), MR images while the amplifier inside the bore needs to be taken extra cautiously and only should be done at low flip angles ($< 5^\circ$). It has been revealed that RF pulses of the external scanner causes gate-oxide breakdown in the main MOS transistors. Especially the weaker chain of BLF871 (Ampleon, Nijmegen, Netherlands) transistors are vulnerable. For a typical $10\mu\text{T}$ RF pulse (for large flip angle sequences like spin echo), the electric fields of RF pulse can reach well over ($3 \times 10^8 \times 10 \times 10^{-6} = 3000 \text{ V/m}$) thousand volts per meter. This electric field dumped on the gate oxide of the MOS capacitor (even a few millimeters distancing results in 10s of volts which can be well over its 13V [41] maximum rating of V_{GS} voltage), has high chances of resulting in irreversible failure/breakdown of the oxide, which has been the case for one of the specimens.

Dynamic phase control managed to successfully control the phase with less than 2° granularity (1.41°). This phase shift step can be further tuned down $1/32$ of the period of the voltage controlled oscillator. By utilizing the phase shifting capability, for the near future work, in collaboration with [5], a real-time delay control for the generalized n-channel coupled amplifiers is to be tested. Also, B1 mapping with different orientations and larger coils needs to be addressed. The B1 mapping should also be repeated for different voltage levels to have an idea about how the Class-E amplifier's (being inherently nonlinear) saturation takes its place and to quantify its gain compression. It is of essence to emphasize

that the tuning of coil-integrated Class-E amplifier is load sensitive. Although using the coil as the load network without intermediate matching to 50Ω has its advantages, the body-loading sensitivity also increases. That is why other goals of future work include introducing a feedback control for actively tuning the amplifier. Also, we aim to utilize a feedback control that makes the amplifier operate in a predetermined output power, sensing the output power level to adjust the necessary gate control waveforms. Digital control in this context is of key essence.

The PSL circuit simulator provided fast and realistic results for a wide range of circuits by exploiting the software packages' capabilities in matrix equations and independent parallel computing algorithms. Compared to its iterative counterparts, huge reductions in computation times are achieved. Custom optimization goals should be evaluated with a better translation of the switch model into the computational domain. Future work also aims to better utilize parallelization of computing tools used (for PSL circuit solver or in the rendering of B1 map with T1 correction), which can be further divided into smaller sub-clusters using a graphical processing unit (GPU). This aims to further speed up the result generation and with the speed advantage, the headroom can be expanded for solving a larger array of coupled Class-E amplifiers (with multiple phased switches) using the PSL circuit solver.

Replacing the conventional MRI RF chain's spectrometer with the external generator by sorting out its complications in the process also proved useful as a step towards building one's own low-cost MRI machine (with the Class-E amplifier, FPGA, and the signal generator composing the RF chain).

The end goal of this line of work is the integration of 32-channel (300W each) on-coil Class-E amplifiers under heavily coupled conditions such as driving of the conventional widespread birdcage coil, with modes of operation such that steering of RF power inside the birdcage with digital control is also possible.

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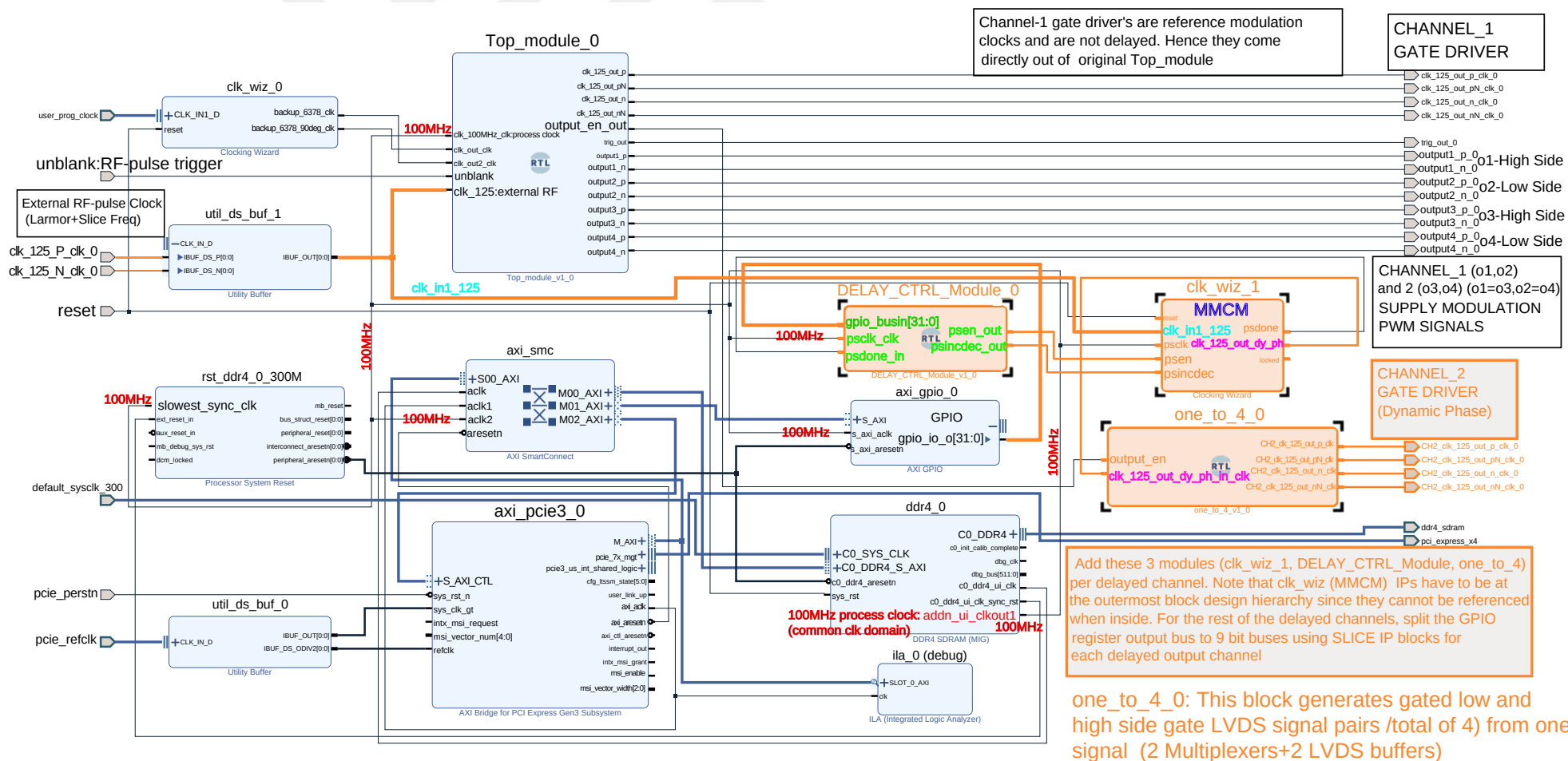


Appendix A

Schematics

A.1 FPGA Design Schematic with Integrated Dynamic Phase Shifting

The schematic is given in the next page. It is also of PDF type and can be zoomed in without loss in resolution.



Important Note: Inputs are always shown on the left sides of each block, outputs are shown on the right

clk_125_out_dy_ph_in_clk is equal to external RF frequency (clk_in1_125). It can be 63.78MHz (1.5T) or 123.24 MHz (3T) or anything else, basically. The same 125 label is kept to show that MMCM does not alter the input frequency, only the phase is altered.