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Millimeter-wave Circuits and Pulse Compression Radar Baseband/Analog Signal Processing Blocks in Silicon Processes

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Mehmet Parlak

Committee in charge:

Professor James F. Buckwalter, Chair
Professor Gert Cauwenberghs
Professor Sadik Esener
Professor Lawrence E. Larson
Professor Gabriel M. Rebeiz

2012

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The dissertation of Mehmet Parlak is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego

2012

DEDICATION

To my parents and sister, Selcuk, Lutfiye and Safak and to my grandmother in heaven, Hatice Oguz.

EPIGRAPH

We must dare to think "unthinkable" thoughts. We must learn to explore all the options and possibilities that confront us in a complex and rapidly changing world. We must learn to welcome and not to fear the voices of dissent. We must dare to think about "unthinkable things" because when things become unthinkable, thinking stops and action becomes mindless.

— J. William Fulbright, March 27, 1964

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ACKNOWLEDGEMENTS

The technological demands arising from the challenges facing society are becoming ever more complex. I believe the complex problems regarding the communication of people all around the world could be solved only if we are able to embed new technologies into the present systems. UC San Diego is highly involved in combining of new and old academic fields into one single discipline and crossing the traditional boundaries between disciplines, as new needs and professions have emerged. I am very thankful to UC San Diego and its community for providing an interdisciplinary environment to their students. A graduate study at UC San Diego in my interest fields enabled me to combine my specializations in the best possible way and helped me bring out my forte to the fore. Electrical and Computer Engineering Department at UC San Diego provided me with very well-maintained state-of-the-art labs and the skills that future engineering leaders have to posses. Possessing a strong academic preparation to back up my ambitions and broad view in applications, I will be able to make significant contributions to the advance of humanity. I also gratefully acknowledge the state-of-the-art labs and financial funds provided by the Center for Wireless Communications (CALIT2) and the counselling help provided by the graduate student advisors, specially acknowledging Robert Rome and Gennie Miranda.

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Lutfiye Parlak always helped me a lot during my hard days. My sister, Dr. Safak Parlak, has always been a book-worm and brought me the joy of reading. She is the sun-shine of our family, inspiring us all. I also sincerely thank my lovely fiancee, princess Shajaira Shizuka Valenzuela, for her great support and devoted love. My thanks also extend to Tufan, Kaan and Fatih. Their friendship has been so valuable to me during my first and last days in San Diego. I thank them a lot for taking care of me and for their invaluable friendship. They were my friends and family in USA. Without my family, this work would have never existed and I would like to express many thanks to them.

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The dissertation author was the primary investigator and author of this material except one conference paper, and co-authors have approved the use of the material for this dissertation.

Mehmet Parlak
La Jolla, CA
September, 2012.

VITA

2001 - 2005	B. S. in Electrical and Electronics Engineering, Middle East Technical University, Ankara, Turkey
2005 - 2006	M. S. in Communications Engineering, Technical University of Munich, Munich, Germany
2006 - 2008	M. S. in Electrical Engineering (Electronic Circuits and Systems), University of California, San Diego, USA
2006 - 2008	Certificate for Business Technology Creation, von-Liebig Center for Entrepreneurism and Technology Advancement, San Diego, USA
2010 - 2012	Certificate for Engineering Leadership, Gordon Engineering Leadership Center, San Diego, USA
2008 - 2012	Ph. D. in Electrical Engineering (Electronic Circuits and Systems), University of California, San Diego, USA

PUBLICATIONS

M. Parlak and J. F. Buckwalter, ”Bidirectional Beamforming with Analog/Baseband Pulse Compression System", SD2012-389 - *Patent submitted via Tech Transfer Office at UCSD*

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ABSTRACT OF THE DISSERTATION

Millimeter-wave Circuits and Pulse Compression Radar Baseband/Analog Signal Processing Blocks in Silicon Processes

by

Mehmet Parlak

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2012

Professor James F. Buckwalter, Chair

The power dissipation and cost of the next generation pulse radar beamforming systems needs to be reduced for the imaging and surveillance sensors. This research work aims at developing and innovating the next generation, mobile hand-held, high performance radar systems for outdoor surveillance applications, i.e. pedestrian detection sensor. Integrating the low cost millimeter-wave (mm-wave) imaging array platforms with advanced analog/baseband signal processing on silicon is proposed for reducing the power dissipation, area, and cost of the next generation radar modules and for the wide deployment of the sensors that are capable of detecting the vehicles and humans with a good range/angle resolution and maximum detection range at the same time. The system concepts of a bidirectional beamforming pulse compression radar system, the

design and measurement results of the bidirectional mm-wave front-end circuits at the front-end and the design and measurement results of a baseband/analog signal processing sub-system and its blocks are presented, although the pulse compression radar is not fully demonstrated. Low noise figure, low power consumption, high linearity and high bandwidth in circuit level is maintained to provide the maximum detection distance, good range and angle resolution for the overall system level.

The analog signal processing system is demonstrated in 90 nm CMOS process. The baseband circuitry is designed as a pulse compression radar system that exhibits the autocorrelation properties of the polyphase codes, maximizes the sensitivity and resolution of a pulse radar system and alleviates speed and resolution requirements of the ADC via an analog correlator while minimizing the power consumption. The baseband circuitry includes a Friis loss tracking VGA for high dynamic range, a correlator /integrator circuit, a comparator, and offset calibration circuits. The different lengths of radar codes are given as inputs to the baseband circuitry chip to find the time of flight.

Next, novel silicon millimeter-wave frequency circuits are implemented to reduce the number of elements in a beamforming front-end, although not specifically designed for the radar system front-end. Bidirectional circuits are motivated by the requirements of scalable microwave and millimeter-wave phased array transceivers. The first bidirectional amplifier in silicon/silicon-germanium is reported to date - a W-band bidirectional cascaded constructive wave amplifier (BCCWA) in a 0.13 μm SiGe BiCMOS technology which operates as either an LNA or PA one at a time. The first phase shifter/variable gain amplifier at W-band in a 0.13 μm SiGe BiCMOS technology is also reported to date. The circuit can operate both as a continuous variable gain amplifier and phase shifter one at a time. The first dual-channel distributed amplifier (DA) is reported to date. The DA is proposed for a highly linear multiple-input receiver front-end and can replace two LNAs at the same time.

Next, millimeter-wave circuits in 45-nm CMOS SOI process are presented. The design and state-of-the-art measurement results of millimeter-wave (Q-band) balanced resistive ring mixer, LNA, and SPDT switch are demonstrated. The results indicate that 45-nm CMOS SOI demonstrates the lowest mixer conversion loss, lowest switch insertion loss, and lowest LNA noise figure compared to other CMOS processes.

Chapter 1

Dissertation Summary

1.1 Dissertation Background

Communication and computing have benefited from CMOS technology scaling improvements. Nanoscale devices on silicon allow low power sub-THz speeds. The other important applications such as imaging could benefit from the scaling of silicon technology. In the near future, effective micro-systems will require hundreds/thousands of electrical, mechanical, biological, optical systems together on the same chip. Exploiting the low cost of silicon technology to realize a dense array of various microsystem designs on a single silicon chip will be essential creating tomorrow's technology. Sensors, specially imaging sensors, are crucial part of these micro systems.

1.1.1 Case Study: Pedestrian Detection Sensor

In 2010, in motor vehicle traffic crashes in the United States, 2.24 million people were injured (pedestrian injuries: 70,000), 32,885 people died (pedestrian deaths: 4,280 - twelve people every day) and the total cost of pedestrian death and injury among children ages 14 and younger is $8.32 billion per year (Safe Kids Worldwide). As accidents at intersections account for about a half of all traffic fatalities, preventive measures are required to avoid collisions involving cars, pedestrians and cyclists.

The low cost, low power, reliable pedestrian detection sensors should be embedded at several locations to sense and image the local surroundings in an intelligent

environment and be benefited in the future environment which is adaptive and responsive to the objects and human beings that occupy it. According to ABI Research, by 2016, the lower costs will play a big part in increasing volumes and push the global pedestrian detection market value to more than £27.2 billion with a growth rate 9.2% CAGR. At present, the pedestrian detection market is not based on the deployment of the sensors on traffic lights due to the cost, battery life and portability of the current sensors however it is only based on the sensors on the vehicles and the market is small-medium, and fragmented. Volvo and Class C Mercedes vehicles already have single camera systems to detect pedestrians and road signs. Other manufacturers like Toyota have also announced that they would soon launch pedestrian detection stereo systems in the market. Small sized start-ups and research institutes are working to develop the technology. However the video sensors on the vehicles limit the speed of the vehicles for pedestrian detection. Volvo's video camera-based pedestrian detection system operates reliably only when new S60 model moves at speeds less than 21 mph. The wide and low cost deployment of pedestrian detection radar sensors is a must however deployment of them around the car is very costly.

To detect the objects in an indoor/outdoor environment, the video camera imaging (optical) sensors, infrared (IR), ultrasound radar based systems are investigated previously [1]. Each have some drawbacks. IR detection has a limited detection range and becomes insensitive in environments with changes in light intensity. Ultrasound sensor power consumption and cost is prohibitive for wide deployment. A traffic surveillance sensor, i.e. a pedestrian detection sensor, based on an optical or infrared camera is not reliable at nighttime, in rain, snow or dense fog. The wide and low cost deployment of pedestrian detection radar sensors is a must however deployment of them around the car is costly. Silicon IC processes make radar chipsets available at low cost and the radar technology will not be subject to such weather conditions. Therefore recent research has been carried out on UWB radar for short-range vehicular applications, doppler radar and vital sign detection [2–11]. However architectures of the UWB systems are not compatible with a communication transceiver and the maximum range of UWB systems are limited. This paper investigates a low cost pulse radar module for a pedestrian detection sensor which is also compatible with a communication transceiver.

Fig. 1.1 presents the case scenario of sensing the pedestrians via a millimeter (mm-wave) radar sensor. The maximum detection range of an object and the range resolution of two objects is dependent on the link budget, transceiver design of the radar beamforming system and the silicon technology available. The advanced radar technology should be capable of detecting humans and cars simultaneously in spite of the fact that human body reflects extremely weak radar signals compared with car body. The case scenario depicts that the low cost and low power radar sensors are deployed as traffic monitoring sensors at every intersection. Pedestrians and bicycles up to 48 meters are detected with high accuracy and with a range resolution of less than 40cm and an angular resolution of 1.2 ° which enables to differentiate every pedestrian and vehicle. Vehicle and pedestrian traffic is monitored and traffic data is sent to the nearby vehicles and/or traffic centers. Radar traffic sensors have a huge potential to be the number one choice for reliable human detection systems which can localize an object through the information provided by direction and time of the radar signal arrival. Direction and time of arrival can be determined through beam-forming and analog signal processing, respectively.

Figure 1.1: Pedestrian and vehicle detection sensor.

1.1.2 An Overview of Mm-wave Imaging Systems

Pedestrian detection being a case scenario, imaging at mm-wave frequencies has recently gained interest for applications ranging from security screening to bio-imaging and spectroscopy. Unlike other regions of the electromagnetic spectrum, mm-wave offers the unique ability to penetrate clothing and other textile materials, enabling

new approaches for weapon and contraband detection. Additionally, the transmission and reflective responses of many materials have distinct features within the mm and sub-mm wave bands, allowing for the possibility of remote material identification. Such systems could potentially detect explosives, poisonous materials, and other chemical threats from several meters away. While the basic building blocks of mm-wave imaging systems are similar to those used in wireless communications (transmitters, receivers, detectors and antennas, etc.), the configurations and requirements for mm-wave imaging are quite different.

Unlike mm-wave communications that wirelessly transmit and receive modulated signal/data, mm-wave imagers detect features of an object based on its radiation, reflection or absorption properties in the mm-wave spectrum. Traditionally mm-wave imagers were implemented in III-V compound semiconductor technologies for their superior noise and high-frequency performance when compared with silicon counterparts. Although a III-V based imaging system offers higher performance, it also has its own limitations including limited integration in forming two-dimensional receiver arrays and excessive power consumption.

The detection of objects based on mm-wave radiation or reflection/absorption can be divided into three separate approaches, each with a unique set of requirements placed on the mm-wave imaging receiver or detector circuitry and its supporting optic as shown in Fig. 1.2.

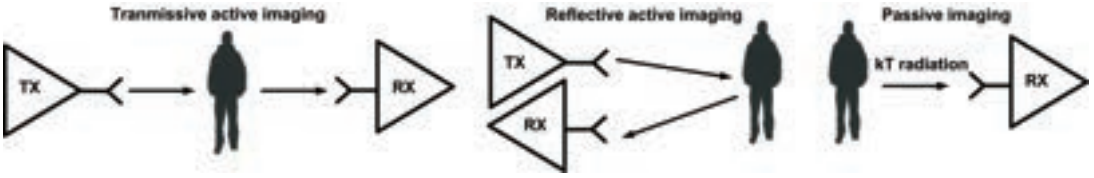

Figure 1.2: Transmissive imaging, reflective active imaging and passive imaging concepts.

Transmissive imaging: A target is placed between a transmitter and receiver. The attenuation or blocking of the target at mm-wave frequencies is then measured at multiple points in space to construct an image. While this is the simplest type of imaging, it inherits a major disadvantage of requiring the system to surround the target for remote security screening and contraband detection.

Reflective active imaging: Most radar systems are examples of reflective active imaging systems. The source of mm-wave illumination (transmitter) is focused into a narrow beam, then the signal is reflected off the surface of a target and returned back to a receiver. This approach is commonly called backscatter or reflective imaging. The reflection coefficient information at different points in space is utilized to create an image. While this is conceptually simple, the signal must travel the path twice (forward and backward) in free-space complicating the link budget.

Passive imaging: It constructs imaging by detecting subject's own blackbody radiation, without the need of mm-wave radiation sources or any compliance to FCC regulations. That can simplify the system and facilitate its wide applications. However, passive imaging is considered to be the most difficult approach in mm-wave imaging systems because it must detect the emitted noise, kT, from the target, where k represents the Boltzmann constant and T represents the absolute temperature measured by Kelvin. While the concept seems relatively simple as compared with communication links, it is actually quite challenging as the temperature variation across a typical scene (contrast ratio) may vary only by a few K. Since scene content varies by such small temperatures a passive mm-wave imager requires <1K in temperature resolution to capture usable images for object detection. One major challenge is that this level of thermal resolution of corresponds to several orders of magnitude lower than the receiver's input referred noise.

1.1.3 An Overview of Silicon Technology

Mm-wave and terahertz applications of SiGe and CMOS circuits have been an active research topic over the past few years. Recent advances in silicon technology, mm-wave integrated circuit/antenna/package design, and beamforming techniques have enabled smaller form factor, lower power consumption and lower cost for the consumer electronics products. While silicon integrated beamforming architectures and phased arrays at millimeter wave frequencies have been demonstrated for automotive radar system, short-distance high-data rate communications, high definition content streaming and satellite systems [12–16], other commercial applications will include sensing, imaging and indoor/outdoor surveillance.

Complementary metal-oxide-semiconductor (CMOS) technology offers an opportunity for dramatic cost and size reduction for beamforming and multiple-input and multiple-output arrays. Integrating the low cost beamformers/arrays with advanced analog signal processing on silicon will provide lower-cost, lower-power millimeter-wave imaging and sensing platforms that require good resolution. Optics, silicon-based antenna arrays and analog signal processing are likely to play a key role towards the wide deployment of future mm-wave sensing systems.

CMOS also offers mixed-signal integration opportunities for concurrent programmability. There have been efforts to realize very-large-scale phased arrays based on CMOS. However, the increased burden on signal processing has not yet been explored in details. The signal processing block has to generate the signals for all transmitters and has to process the signals from all receivers. Therefore, the signal processing burden and the power consumption of the analog-to-digital converter (ADC) increase rapidly. This excessive demand on the signal processing power and the ADC can be a major hurdle to overcome for a radar system. The lack of ADCs with sufficient speed and/or dynamic range constrains many radar designs [17]. Moreover, the speed requirements of an ADC keep increasing because of the modern direct-conversion architectures and high bandwidth waveforms, and the dynamic range requirement of an ADC keeps increasing to detect reduced signal returns in heavy clutter and electronic counter measure environments.

Moreover, for future expansion to mobile applications, a friendly system-on-a-chip (SOC) integration is desirable. Another very important aspect for these applications is low power consumption. In this sense, the design that can be implemented with CMOS technology will be desirable since the digital functionalities can be easily implemented by CMOS. Therefore analog signal processing based systems on silicon over conventional digital signal processing based systems will enable reduction in total system power consumption. A low-power signal processing unit is one of the key enabling technologies for radars.

1.2 Dissertation Motive

As illustrated in Fig. 1.1 and explained in section 1.1.3, the main motive of this research is reducing the power dissipation, area, and cost of the next generation radar modules by integrating the low cost millimeter-wave (mm-wave) imaging array platforms with advanced analog baseband signal processing on silicon. The sensor should be capable of detecting the vehicles and humans with a maximum range of 48 m, range resolution of 40 cm and angle resolution of 1.2° at the same time. Therefore various ways of beamforming circuits and analog signal processing architectures on silicon (SiGe and CMOS technology) suitable for an integrated radar-on-chip system are investigated in this dissertation. Bidirectional bemforming is proposed and motivated by the requirements of scalable microwave and millimeter-wave phased array transceivers. It provides lower power consumption and chip area as compared to other architectures (power matters, especially in portable applications). And powerful analog signal processing on same chip with the mm-wave front-end beamforming circuits is proposed to realize a high performance complete on-chip implementation of radar systems.

Although complete system is not implemented, the high level specifications and block diagram of the pedestrian detection system is illustrated in this dissertation. The bidirectional circuits are designed and implemented in a 0.12 μm SiGe BiCMOS process while analog signal processing circuits are implemented in a 90-nm CMOS mixed-signal/RF low power process.

The mm-wave circuits in other CMOS processes - 45-nm CMOS and 130-nm CMOS - are designed and implemented. The state-of-the-art measurement results are presented. It is demonstrated that 45-nm digital CMOS SOI is an excellent candidate even for mm-wave circuits in addition to its digital, analog and RF integrability in a monolithic system-on-chip (SOC) package. Low loss, high isolation, low-noise and high-power handling circuits are demonstrated.

1.3 Dissertation Organization

In Chapter 1, a case study - pedestrian detection/imaging sensor - has been introduced. An overview of mm-wave imaging systems and silicon technology is explained.

Dissertation motive and organization is introduced.

Chapter 2 presents the background information for beamforming systems and radar architectures. Radar history and concept is explained. Matched filter concept and correlation of radar waveforms via matched filter is introduced. Pulse compression radar and non-coherent integration concepts are briefly explained. The polyphase codes as radar waveforms, their radar ambiguity function and autocorrelation characteristics (range ambiguity, velocity ambiguity, range sidelobes, doppler shift, minimum range etc.) are presented. The motivation of beamforming for radar systems is explained.

Following three chapters (Chapter 3, 4 and 5) are dedicated to describe the system level characterization, baseband analog signal processing and mm-wave front-end of the radar system proposed for pedestrian detection system, respectively.

Chapter 3 proposes the architecture for the pulse compression radar - bidirectional beamforming pulse radar front-end and baseband analog signal processing blocks - to bring the cost and power dissipation of the mobile pulse compression radar (PCR) down. The specifications, maximum and minimum range limitation, resolution limits of the beamforming pulse-compression radar system in silicon are described. The block diagram of the proposed architecture is depicted. The link budget with beamforming, pulse compression, and non-coherent integration in pulse compression radar are illustrated. Front-end and baseband signal processing architectures and their trade-offs are illustrated. The required time-scan and power consumption of the baseband signal processing units is illustrated.

Chapter 4 presents the pulse compression radar analog signal processing blocks which are implemented and fabricated in TSMC 90-nm process. The baseband circuitry includes a two-stage VGA for high dynamic range, a correlator/integrator circuit, a comparator replacing an amplitude detector and ADC, and offset calibration circuits. The chip is wire-bonded on the FR4 printed circuit board and tested with Stratix IV FPGA board to evaluate the system performance for different polyphase codes and their parameters. The differential, 6-bit variable gain amplifier (VGA) preceding in the system is designed to track Friis path loss through rapid change of the VGA gain and reduces the dynamic range on the correlator and ADC. VGA has a gain variation of 52 dB and a low group delay imbalance of only 50 ps over 64 states. The pulse compression radar system

exhibits the autocorrelation properties of the polyphase codes, maximizes the sensitivity and resolution of a pulse radar system and alleviates speed and resolution requirements of the ADC via an analog correlator which replaces the matched filter in a traditional radar architecture.

Chapter 5 presents the novel front-end circuits for low cost, low power active and passive beamforming systems. As the first design, the first bidirectional amplifier in silicon / silicon-germanium is reported to date - bidirectional cascaded constructive wave amplifier (BCCWA). This design is based on the cascaded constructive wave amplifier (CCWA) which uses a transmission line and an active shunt feedback circuit which feeds current back to the input of the quarter-wave transmission line to introduce a small amount of positive feedback to generate gain. For the BCCWA, two feedback amplifiers decide the direction of amplification and only one feedback amplifier operates at a time to provide gain in either the forward and backward direction. The BCCWA is proposed to avoid the insertion losses due to the SPDT switches and decrease the area and power consumption. They are motivated by the requirements of scalable microwave and millimeter-wave phased array transceivers. A W-band BCCWA, which operates as either an LNA or PA, is designed and fabricated in a 0.13 μm SiGe BiCMOS technology. The measured amplifier has a peak gain of 16 dB, a bandwidth of 14.5 GHz at 90 GHz, a noise figure of 11 dB and its output-referred P1dB is 1 dBm at 90 GHz. The circuit occupies an area of 0.47 mm^2, and consumes approximately 32 mA from a 2 V supply. Therefore, it does not impose significant circuit area or power consumption to operate as a bidirectional element.

Next, the first phase shifter/variable gain amplifier at 94 GHz in silicon/silicon-germanium is also reported to date. This design is also based on the cascaded constructive wave amplifier. The CCWA circuit architecture loaded with varactors is used to design a loss-compensated, varactor-loaded transmission line. Analog varactor control introduces a small amount of phase shift and analog feedback amplifier control in the signal path introduces a small amount of gain shift while compensating for the distributed varactor losses. Therefore the circuit can operate both as a continuous variable gain amplifier and phase shifter one at a time. Continuous phase and amplitude control allows phase/gain shift and calibration of the relative phase and gain errors in the

channels of the beamforming systems. More than 65° of continuous phase control and 7 dB gain control (with a maximum gain of 16 dB) one at a time is demonstrated with a power consumption of only 36 mW.

As the third design, although not specifically designed for the radar system front-end, a low-power dual channel distributed amplifier (DA) is implemented to reduce the number of elements in a beamforming front-end. Dual channel DA provides isolation between amplifier channels and is proposed to replace two LNAs at the same time. The DA is biased in moderate inversion to simultaneously obtain low noise figure and high linearity while consuming low power. The dual-channel DA is fabricated in a bulk 0.13μm CMOS process, achieves a forward gain of 9.6 dB and a P_{1dB} of 4.9 dBm, and consumes 18 mW power.

In Chapter 5, mm-wave high performance front-end circuits in 45-nm SOI CMOS process are demonstrated. The design and state-of-the-art measurement results of mm-wave (*Q*-band) SPDT switch, balanced resistive ring mixer and LNA in 45-nm SOI CMOS are presented. The technology provides higher f_t than other CMOS processes and allows the substrate isolation, therefore 45-nm CMOS is an excellent candidate for millimeter-wave low-noise amplifiers and passive circuits - SPDT switches and ring mixers. Electromagnetic simulations are extensively used to model the high frequency behavior of any passive components such as the conventional CPW-line, grounded stubs, inductors, and baluns. The passive resistive I/Q ring mixer demonstrates a conversion loss of 8.35 dB and input P_{1dB} of 4.5 dBm at 43.3 GHz. The gain and phase imbalance of the mixer is minimized using the provided DC pads and is 0.25 dB and 2°, respectively. The record SPDT insertion loss is 1.7 dB at 45 GHz and less than 2.5 dB at 60 GHz with an isolation of greater than 25 dB at 45 GHz. The input P_{1dB} of the switch is 7.1 dBm. The LNA demonstrates a record low noise figure of 2.9 dB at 47 GHz with 18.5 dB of gain and OIP3 of 15.5dBm.

Chapter 6 concludes the dissertation by discussing the next generation base-band/analog signal processing system, topics for future research and a summary of the dissertation with the publications and patents of the author.

Chapter 2

Review of Radar Systems

A millimeter-wave indoor/outdoor surveillance application requires low interference and good angle resolution at low cost therefore radar beamformer sensors can be embedded at several locations to sense, image and learn the local surroundings in an intelligent environment that is adaptive and responsive to the objects and human beings that occupy it, which is defined as "cognitive radar" by Haykin [18]. This millimeter-wave beamformer radar sensor should be a low cost and low power platform based on a silicon CMOS process and will require a dedicated baseband signal processing circuit to generate and detect the radar signal. Analysis of the partitioning of baseband signal processing between the analog and digital domains reveals that the power dissipation of a digital-baseband approach is dominated by the high-resolution, high-speed ADC that is required. The prohibitive performance demands of such an ADC suggests that some analog-baseband signal processing is preferable. It will be shown that the known characteristics of the received radar waveform can be exploited through analog pre-processing elements to alleviate speed and power requirements on the ADC.

This chapter presents the background information for the rest of the dissertation. History on radar, background information on radar waveforms and their properties, pulse compression radar and beamforming for radar systems are introduced. First, radar history and concept is explained in Section 2.1. Next, matched filter concept, correlation of radar waveforms via matched filter, pulse compression radar , polyphase radar codes, radar ambiguity function a nd non-coherent integration are introduced in Section 2.2. The polyphase codes as radar waveforms, their radar ambiguity function and autocor-

relation characteristics (range ambiguity, velocity ambiguity, range sidelobes, doppler shift, minimum range etc.) are presented in Section 2.2.3. The motivation and use of beamforming for radar systems is introduced in Section 2.3. The chapter is concluded in Section 2.4. The relevant papers and patents are summarized in Section 2.5.

2.1 Traditional Radar

As early as 1886, Heinrich Hertz demonstrated the principle of reflective active imaging and showed that radio waves could be reflected from solid objects. Since then, several inventors, scientists, and engineers contributed to the development of radar. German Christian Huelsmeyer was the first to discover the effect of radar in 1904, and the first patent of the detection of objects by radio was issued to him. However radar as we know was invented in 1935 by three British scientists, Sir Robert Watson-Watt, A. F. Wilkins and H. E. Wimperis along with Sir Henry Tizard, who discovered its use putting it to excellent effect in World War 2. It was being tested on December 7, 1941 when the Japanese were attacking Pearl Harbor, but when they saw evidence of a large number of airplanes coming in they thought it was a problem with the radar. The radar was working, the officers just didn't believe it. "We had enough warning to have actually made a difference, but our military officers didn't trust the new technology".

Radar is an active imaging object detection system which uses electromagnetic waves, specifically radio waves, to determine the range, altitude, direction, or speed of both moving and fixed objects such as aircraft, ships, spacecraft, guided missiles, motor vehicles, weather formations, terrain, and even humans. The radar dish, or antenna, transmits pulses of radio waves or microwaves which bounce off any object in their path. The object returns a tiny part of the wave's energy to a dish or antenna which is usually located at the same site as the transmitter. Radar sensor figures of merit include field of view in terms of solid angle and maximum unambiguous range and velocity, as well as angular, range and velocity resolution. Applications of radar sensors include autonomous cruise control (ACC), autonomous landing guidance (ALG), altimetry, air traffic management (ATM), early warning, fire control, forward warning collision sensing (FWCS), ground penetrating radar (GPR), surveillance, and weather forecasting.

Radar sensors are classified by architecture, radar mode, platform, and propagation window.

The key elements of a simple radar system is illustrated in Fig. 2.1. The radar system includes a transmitter, receiver and signal processing blocks. The radar transmits a short pulse of energy that is reflected by objects being examined. The received waveform is a shifted version of the transmitted waveform plus random noise. The radar waveform in time domain and frequency domain is shown in Fig. 2.1. The range resolution of a single pulse is proportional to the pulse width and inversely proportional to the bandwidth, which will be covered in details in Chapter 3.

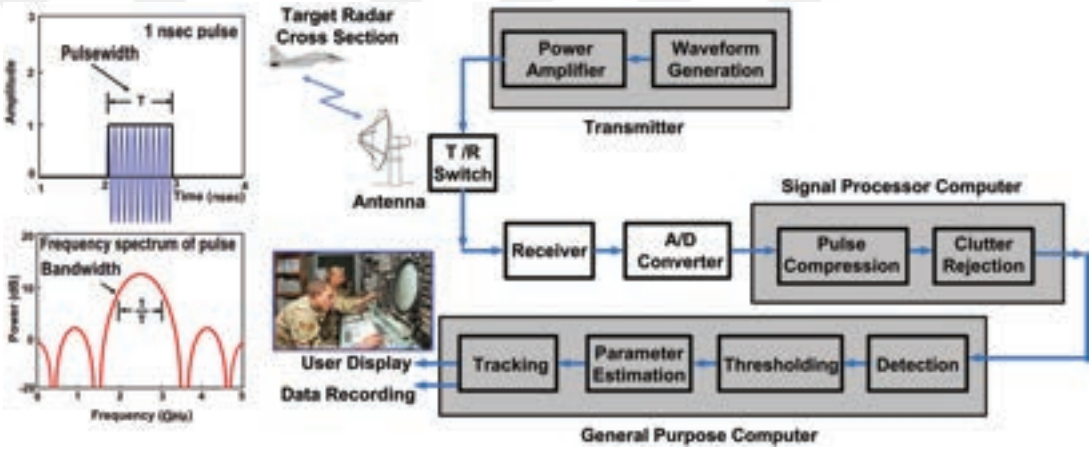

Figure 2.1: Block diagram of a radar system.

2.2 Radar Concepts and Waveforms

Unlike a typical communication system, in radar, certain aspects of the received waveform are known. For instance, in an pulse radar imaging system, a transmitted train of narrow pulses impinges on the objects in the environment. If the reflectiveness of the objects can be assumed to be frequency-independent, to the first order, the received waveform is simply a superposition of delayed and scaled versions of the transmitted waveform. The amplitudes and delays depend on the distances of the reflecting objects, their shapes, sizes, and materials. Therefore detection of a known waveform in a noisy signal is the fundamental problem and the answer to this problem is correlation. Corre-

lation is used to compare the similarity of two signals, the result is a signal that shows this similarity and reaches its maximum at the time when the two signals match best. Therefore correlation can be used to measure the distance of a certain system via time delay.

2.2.1 Matched Filter Concept

A filter whose impulse response is $h(t) = s^*(T-t)$, in which the signal $s(t)$ is assumed to be confined to the time interval $0 \leq t \leq T$ is called a matched filter to the signal $s(t)$ and attains a peak at $t = T$. The response of the MF, $h(t)$, to the arbitrary input signal, $s^i(t)$, at $t = T$ is

$$\begin{aligned} y_{t=T} = \quad & s^i(t) * h(t)|_{t=T} \\ = \quad & \int_{-\infty}^{+\infty} s^i(\tau) h(T-\tau)\, d\tau \\ = \quad & \int_{0}^{T} s^i(\tau) h(T-\tau)\, d\tau \\ = \quad & \int_{0}^{T} s^i(\tau) s^*(\tau)\, d\tau. \end{aligned}$$

It is known that if signal $s(t)$ is corrupted by an additive white Gaussian noise (AWGN) process, the matched filter maximizes the output peak-signal to mean-noise ratio (SNR), and the maximum output SNR is given as $SNR = 2E/N_0$ where $E = \int_0^T |s(t)|^2\, dt$ and $N_0/2$ is the energy of the signal and power spectral density of the noise, respectively. One wants to pass the received radar echo through a filter, whose output will optimize the Signal-to-Noise Ratio (S/N). Matched filter is implemented by "convolving" the reflected echo with the "time reversed" transmit pulse as illustrated in Fig. 2.2. Convolution process first involves to move the digitized pulses by each other in steps. When data overlaps, samples are multiplied and summed up to the output. Therefore, a long pulse compression time [large T with long $s(t)$] can increase the SNR, but it may limit the bandwidth of radar tracking in radar applications, especially with dynamic targets.

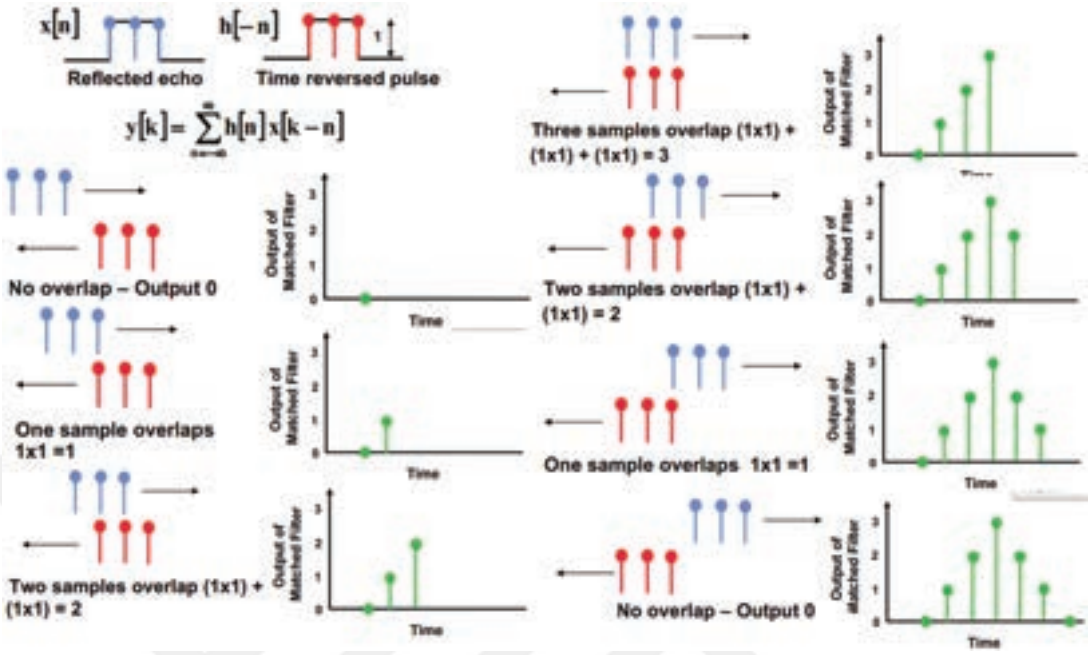

Figure 2.2: Convolution process

Let us consider $s^i(t)$ as a time-shifted replica of $s(t)$ by Δt, i.e. $s^i\ (t)$ = s(t- Δt), and $s_k[n]$ as a sampled and delayed sequence of $s(t)$ by sampling frequency $1/T_s$ and the delay of integer k. In other words

$$s_k[n] = \begin{cases} s((n-k)T_s), & k \le n \le k+N \\ 0 & \text{otherwise} \end{cases}$$

where N is defined as $N = \lfloor T/T_s \rfloor$. If a function $\tilde{y_k}$ is defined as

$$\tilde{y_k} \equiv \mathrm{Re} \int_{-\infty}^{+\infty} s^i(\tau) s_k^*[\lfloor \tau/T_s \rfloor], d\tau, \tag{2.1}$$

and if an integer k can be found such that

$$k = \lfloor (\tau + \Delta t)/T_s) \rfloor - \lfloor \tau/T_s \rfloor \ \approx \lfloor \Delta t/T_s \rfloor \,, \tag{2.2}$$

then

$$\begin{aligned}
\tilde{y_k} &= \int_{\Delta t}^{T+\Delta t} s(\tau - \Delta t) s_k^*[\lfloor \tau / T_s \rfloor] d\tau \\
&= \mathrm{Re} \int_0^T s(\tau) s_k^*[\lfloor (\tau + \Delta t)/T_s \rfloor] d\tau \\
&= \mathrm{Re} \int_0^T s(\tau) s_k^*[\lfloor \tau / T_s \rfloor + k] d\tau \\
&= \mathrm{Re} \int_0^T s(\tau) s^*(\lfloor \tau / T_s \rfloor T_s) d\tau \\
&\approx \mathrm{Re} \int_0^T s(\tau) s_\tau^* d\tau \\
&= \mathrm{Re} \int_0^T |s(t)|^2 \, d\tau \\
&= E
\end{aligned}$$

which is the maximum. Therefore, by finding the maximum of $\tilde{y_k}$ with respect to k, Δt can be estimated from (2.2) with the resolution of T_s. In turn, the target distance can be estimated as $ckT_s/2$ from k.

Furthermore $\tilde{y_k}$ is

$$\begin{aligned}
\tilde{y_k} &= \int_{-\infty}^{+\infty} s^i(\tau) s_k^*[\lfloor \tau / T_s \rfloor] d\tau \\
&= \int_0^T (s_I^i(\tau) s_{k,I}^*[\lfloor \tau / T_s \rfloor] + s_Q^i(\tau) s_{k,Q}^*[\lfloor \tau / T_s \rfloor]) d\tau \\
&= \int_0^T s_I^i(\tau) s_{k,I}^*[\lfloor \tau / T_s \rfloor] d\tau + \int_0^T s_Q^i \tau s_{k,Q}^*[\lfloor \tau / T_s \rfloor] d\tau
\end{aligned}$$

where I and Q denote an in-phase and quadrature-phase component, respectively. Since the analog MF in this work is for radar applications, signal $s(t)$ is already known. Therefore, $s_k[n]$ can be constructed by shifting sampled $s(t)$ by an appropriate amount, and the output can be calculated by the following procedure.

Step 1. Multiply an input signal with $s_k[n]$.

Step 2. Integrate over time $0 \leq t \leq T$.

Step 3. Sample the integrator outputs at time T.

Step 4. Add sampled integrator outputs of the I path and the Q path.

Note that the known sampled sequence $s_k[n]$ of the transmitted signal $s(t)$ is used, but the input signal $s^i(t)$ is not sampled, which precludes the necessity of a high-speed ADC. Moreover, the reference signal shifts instead of the input signal.

Conventional approaches of matched filters use surface acoustic wave (SAW) filters or fast digital convolution processing, but these solutions have significant drawbacks. System-on-a-chip (SOC) integration turns to be difficult, costly and bulky with SAW devices. Fig. 2.3 shows the convolution of the most simple radar waveform, 3-bit Barker code through the tapped delay line, which is a DSP-based pulse compressor or digital finite-impulse response (FIR) filter implementation of a matched filter (MF). The 3-bit Barker code (+ + -) is "time reversed" and (- + +) is applied to the input of the tapped-delay line in order. The inputs are multiplied with the 3-bit Barker code coefficients (+ + -) and summed up to the output. However this implementation consumes significant power and bring complexity. Moreover, for cm-range resolution over meters of range, the gigahertz system bandwidth demands front-end analog-to-digital converters (ADC) with high resolution and high sampling frequency that are beyond current technologies.

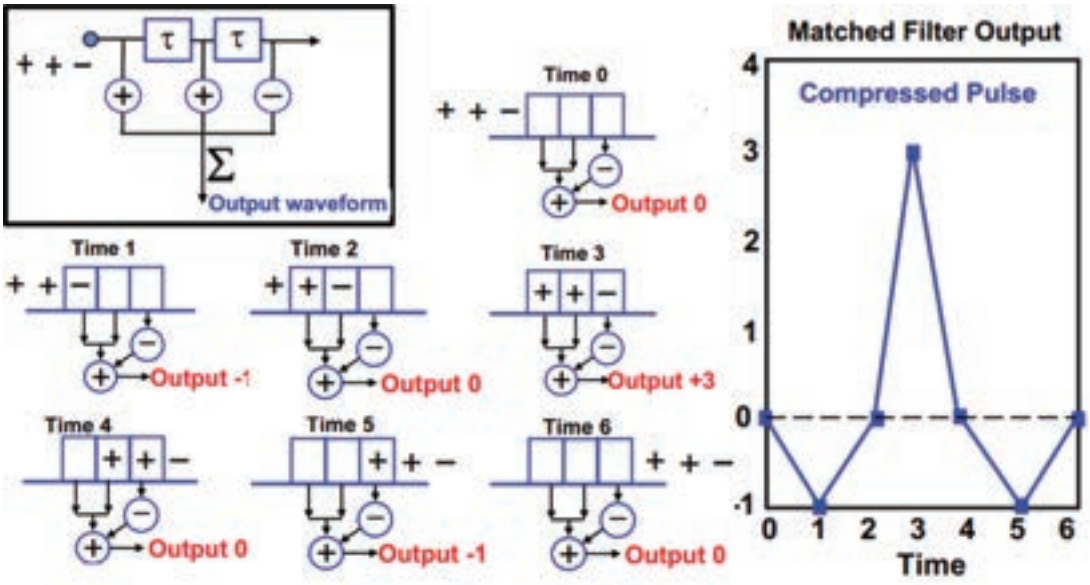

Figure 2.3: Matched filtering the most simple radar waveform, 3-bit Barker code, via FIR filter implementation.

2.2.2 Pulse Compression Radar (PCR)

The pulse radar system should be able to distinguish neighboring objects separated by half the pulse width time $cT/2$. Transmitting narrow radar pulses corresponds to high range resolution. However, it also requires wide receiver bandwidth that desensitizes the receiver through the increased noise bandwidth. With narrow pulse width, higher transmitted peak powers are required to transmit the same energy. However, silicon-based mm-wave PAs often have significant limitations on the peak power. Therefore, this imposes the limitation in range resolution for the system. Therefore, PCR techniques are adopted where a long duration pulse is either frequency or phase modulated to increase the bandwidth without the peak power constraint. Therefore, pulse compression radar is realized using specific PCR codes that transmit high energy through a modulated pulse train that obtains small range resolution corresponding to a short pulse, high-power pulse.

Digital signal processors are typically more flexible and reconfigurable than their analog counterparts as pulse compressors. However, this advantage is not particularly valuable for radar, where the analog signal processing required is a simple matched filter and involves the use of an analog correlator - essentially a multiplier or mixer followed by an integrator. Baseband signal processing in radar involves the correlation of the received and down-converted signal with a delayed version of the transmitted baseband template via the correlator. The correlation is used to compare the similarity of two sets of data and computes a measure of similarity of two input signals as they are shifted by one another. The correlation result reaches a maximum at the time when the two signals match best. If the two signals are identical, this maximum is reached at t = 0 (no delay). If the two signals have similar shapes but one is delayed in time and possibly has noise added to it then correlation is a good method to measure that delay.

As shown in Fig. 2.4 (a), the PCR code - a 7 bit Barker code - is divided into N sub-pulses each having a width of τ. The echo of the PCR signal is received as a weak mm-wave signal and down-converted through a homodyne receiver to the baseband. A baseband signal processing circuit correlates the noisy received baseband echo (in red) with the delayed versions of the transmitted PCR code (template in blue). This implements an analog matched filter to estimate the time of flight of the radar signal. When

two 7-bit Barker codes are aligned, maximum correlation is achieved. In other words, the template 7-bit Barker code signal can be shifted in time until the peak correlation is observed and the corresponding time that is shifted corresponds to the time of flight of the radar signal. As shown in Fig. 2.4 (b), the resultant compressed pulse has a width of 2τ and the range resolution improves by T/τ. Deterministic timing mismatch at the correlator results in a linear decrease in the peak correlator output. When received base-band echo and template are not aligned (less than τ), the degradation from the peak is given by N/M, as shown in Fig. 2.4 (b), where $N = B.T$ is the number of sub-pulses or pulse compression factor, and $M = \tau/\Delta\theta_P$ is the number of resolved phases within one sub-pulse, where θ_P is the phase resolution.

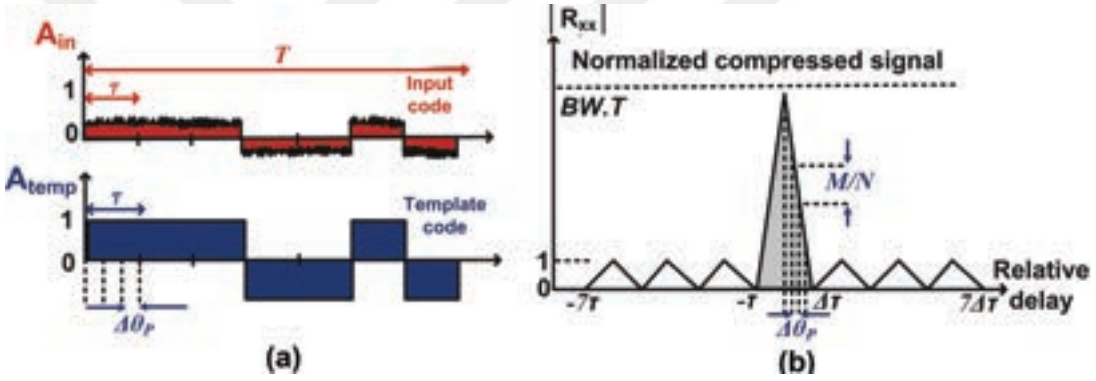

Figure 2.4: (a) The input and template code. (b) The degradation from the peak auto-correlation signal when the input and template code are not aligned.

2.2.3 Polyphase Codes as Radar Waveforms

The use of phase-coded (PC) waveforms helps reduce radio frequency interference (RFI) between adjacent radars and is easily adapted to a communication transceiver. PC waveforms divide the pulse into *N* time segments, referred to as chips, and applies a different phase to each. Binary phase codes modulate chip phase between 0 or π, while other polyphase codes support more levels. The transmitted signal is compressed into the width of sub-pulse by either matched filtering or correlation processing. A special class of PC waveforms called Barker codes are a sequence of *N* values of +1 (0) and -1 (π) and has a maximum autocorrelation sequence which has sidelobes no larger than magnitude of one. Since there are no known Barker codes of length greater than

13 [19], pseudorandom number sequences (PRN) codes generated from cyclic Barker Codes have perfect (and uniform) cyclic autocorrelation sidelobes and can have much longer lengths. Table 2.1 lists several known Barker codes and PRN codes, having a minimum peak sidelobe of one.

Table 2.1: Known Barker Codes with different lengths

Length	Codes
Barker 3	1 1 -1
Barker 5	1 1 1 -1 1
Barker 7	1 1 1 -1 -1 1 -1
Barker 11	1 1 1 -1 -1 -1 1 -1 -1 1 -1
Barker 13	1 1 1 1 1 -1 -1 1 1 -1 1 -1 1
PRN 15	1 -1 -1 -1 1 1 1 1 -1 1 -1 1 1 -1 -1
PRN 31	1 -1 -1 -1 -1 1 -1 1 -1 1 1 1 -1 1 1 -1 -1 -1 1 1 1 1 1 -1 -1 1 1 -1 1 -1 -1

2.2.4 Radar Ambiguity Function

The radar ambiguity function plays a central role in the theory of radar signals. The ambiguity function represents the output of the matched filter, and it describes the interference caused by the range and/or Doppler shift of a target when compared to a reference target of equal RCS. In other words, absolute value of ambiguity function measures the correlation between the signal emitted by the radar transmitter and its echo after reaching a moving target. The response of the matched filter depends on two signal dimensions: delay, t and Doppler frequency, f_d. The ambiguity function evaluated at (τ , f_d) = (0,0) is equal to the matched filter output that is matched perfectly to the signal reflected from the target of interest. In other words, returns from the nominal target are located at the origin of the ambiguity function. Thus, the ambiguity function at nonzero represents returns from some range and Doppler different from those for the nominal target.

As shown in Table 2.1, radar transmit signals are designed and then adaptively

optimized for the radar system performance, such as range, range resolution, radial velocity, or rejection of unwanted object responses. As illustrated in Fig. 2.5, various Barker and PRN codes are given as inputs and their ambiguity functions are plotted to find the radar performance, such as range resolution and radial velocity. Fig. 2.5 also shows the autocorrelation response, which is the radar ambiguity cuts for zero doppler shift. One bit change in the sequence of various Barker and PRN codes increase the sidelobes and degrades range resolution demonstrating that the specific radar waveform sequences are designed very carefully.

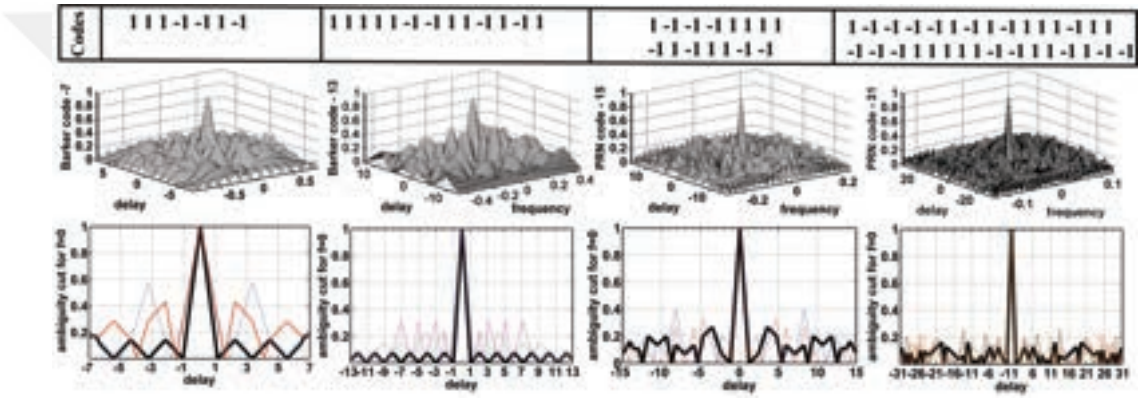

Figure 2.5: Ambiguity functions and cuts for Barker and PRN codes.

Next, range ambiguity, doppler shift, range side-lobes and minimum range descriptions are introduced to familiarize with the several radar waveform characteristics. For instance, a 2 Gb-s, 7-bit Barker code with a PRF of minimum 3 MHz provides a range resolution of 7.5 cm, maximum range of 48 m and minimum range of 1 m, in simple terms.

Range Ambiguity

Range ambiguity occurs if the echo returns after the transmission of the next pulse. After the pulse is transmitted, the radar must wait a sufficient length of time so that echos beyond the maximum range are blocked before the next pulse is emitted. Maximum unambiguous range is $R_u = c/2PRF$ where R_u is the unambiguous range and PRF is the pulse repetition frequency. The 1 Gb-s, 7-bit Barker codes should be separated by 333 ns, i.e. the minimum pulse repetition frequency for this application

should be 3 MHz so that the maximum unambiguous range is far as 48 m.

Doppler Shift

Objects in motion relative to the radar cause the return signal frequency to be frequency shifted. Doppler shift corresponding to the object radial velocity is $f_d = 2v_r/\lambda_o$ where v_r is the object radial velocity, f_d is the object Doppler frequency and λ_o is the transmitted radar signal wavelength. The velocity causing a 1-dB loss at the peak of the autocorrelation is found as 96 km/s (and a doppler frequency is 38.4 MHz) for a 1 Gb-s, 7-bit Barker code. This is much faster than any anticipated objects.

Range Sidelobes

The output of the pulse compressor consists of the compressed pulse accompanied by responses at other times (i.e., at other ranges), called time or range sidelobes. In case there are undesired point objects in the vicinity of an object of interest, ideally the desired object will experience the peak response and the response for the undesired objects should be as low as possible to avoid declaring false detections. One bit change in the pre-defined PCR codes will result in increased sidelobes as illustrated in Fig. 2.5. The sidelobes are 7 times smaller than the pulse compression ratio = 7, for a 1 Gb-s, 7-bit Barker code.

Minimum Range

Whenever a monostatic radar is transmitting, it is blind. When the blind range is calculated for pulse compression radar, the uncompressed pulse width must be used since the radar has to transmit the entire uncompressed pulse before it is able to switch off its power amplifier and listen for reflections. Due to their lengthy uncompressed pulse, pulse compression radars usually have poor blind ranges, which is given as:

$$TOF = 2R/c \geq N\tau = N/B \tag{2.3}$$

where N is the number of sub-pulses, B is the bandwidth and TOF is the time of flight which must be longer than the length of the PCR sequence. The minimum range for a 1

Gb-s, 7-bit Barker code is 1 m.

2.2.5 Non-coherent Integration

When a object is located within the radar beam during a single scan, it may reflect several pulses. The requirements on the EIRP can be relaxed and the radar sensitivity (SNR) can be increased by adding the returns from all pulses returned by a given object during a single scan. This will reduce the power consumption of the PA by alleviating the constraints on the transmitted power and antenna gain. In order to improve the SNR from 0 dB to a threshold of 15dB, multiple pulses are sent, received, correlated and accumulated in digital domain. The process of adding radar returns from many pulses is called radar pulse integration. Accumulation can also be performed in the analog domain to further reduce the ADC sampling rate but places stringent requirements on the droop of analog samples over long periods. This pulse integration method performed after the envelope detector (where the phase relation is destroyed) is called non-coherent or post-detection integration.

If a radar coherently integrates pulses from objects without proper knowledge of the object dynamics it suffers a loss in SNR rather than the expected SNR build up and the requirements of knowing the exact phase of each transmitted pulse as well as maintaining coherency during propagation is very costly and challenging to achieve. Therefore non-coherent integration (post-detection integration) is preferred over the coherent integration although non-coherent integration is less efficient than coherent integration in boosting the SNR.

Non-coherent integration sums the radar returns and divides the sum by the number of returns, n_P. This process reduces the variance of the noise and the variance of the signal plus noise by a factor proportional to n_P, but keeps their mean values as same as shown in Fig. 2.6 (a). Non-coherent integration is beneficial in making a signal easier to detect when the SNR at the input of the processing unit is greater than zero. SNR is boosted with an improvement factor, SNR_{NCI}. When pulses are integrated non-coherently, $SNR_{NCI} = n_P SNR_1$. $SNR_1/(1+SNR_1)$ where SNR_1 is the single pulse SNR and n_P is the number of pulses integrated. The more number of pulses integrated, the more requirements on the EIRP are relaxed.

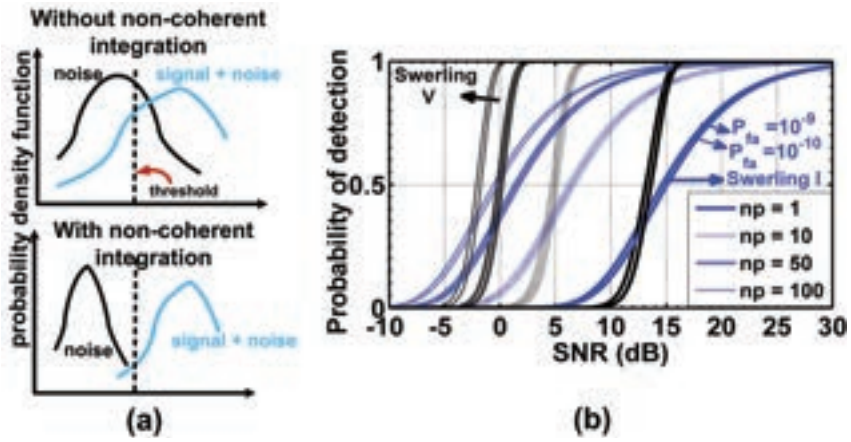

Figure 2.6: (a) Reducing the variance of the noise with non-coherent integration. (b) Boosting the SNR to 20 dB by integrating pulses.

As shown in Fig. 2.6 (b), the 0 dB of SNR at the input of the non-coherent integrator can be boosted to 15-20 dB by integrating approximately 50 returns from Swerling I objects to achieve a detection probability of 0.90 and false alarm probability = 10^{-9} when a single pulse SNR is 0 dB. 1000 returns from Swerling V objects are needed to achieve the same probabilities [20]. Knowledge of object dynamics is not as critical when employing non-coherent integration; nonetheless, object range rate must be estimated so that only the returns from a given object within a specific range bin are integrated. In other words, one must avoid range walk (i.e., avoid having a object cross between adjacent range bins during a single scan).

2.3 Beamforming / Phased Arrays

Beamforming systems/phased arrays is an array of antennas which filters electromagnetic waves in the spatial domain. The signals are received (or transmitted) in desired directions (peaks) by constructive interference between the signals to (or from) each antenna, and simultaneously blocked in undesired directions (nulls) by deconstructive interference. The total effective radiation pattern (scan angle, peaks, nulls, sidelobe levels, beamwidth, etc) of the antenna array is determined by the signal amplitude and phase (time delay) weighting at each antenna. Since the phase and amplitude weighting is done electronically, the beam steering and beam-forming are much

faster than mechanical systems (nearly instantaneous). The beamforming is provided with variable time delays and variable attenuators (or variable gain amplifiers) following (preceding) the antennas, in order to compensate for phase and amplitude difference between the antenna elements so as to have constructive summing in desired directions while having nonconstructive summing in undesired directions.

Research efforts have moved towards large scale integration of phased array transceivers based on silicon/ silicon-germanium (Si/SiGe) processes. Previous work on phased arrays has demonstrated either receive arrays at 6-18 GHz [21, 22], 24 GHz [23, 24], 45 GHz [25], 60 GHz [26, 27] and 77 GHz [26] or transmit arrays at 24 GHz [28], 45 GHz [29], 60 GHz [30], and 77 GHz [31].

The time or phase shifting can be realized in the RF, LO, IF or digital paths of the T/R modules. Shown in Fig. 2.7, the receiver and transmitter with the RF phase shifting topology (all-RF architecture) is shown. RF phase shifting topology has been the most commonly used one since the invention of phased arrays due to high signal-to-interferer ratio (since the beamforming is done in the RF domain before the down-conversion, interferers are rejected before the non-linear mixers), lowest size, lowest power consumption (especially for large number of elements), no need for LO distribution.

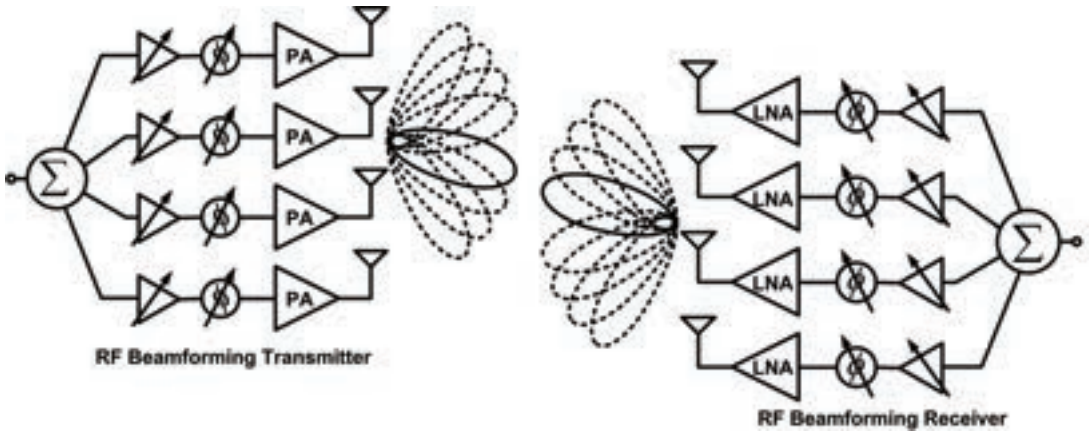

Figure 2.7: RF phase shifting topology for receiver and transmitter.

2.3.1 Beamforming for Radar Systems

While communication systems suggest fully integrated phased array transmitters and receivers at millimeter-wave bands to provide electronic beam control and improve the signal-to-noise ratio, multi-antenna radar systems have to benefit from beamforming. The undesired multipaths or interferences arriving from other directions which can result in false alarms or ghost artifacts as signals return with a misleading time of flight estimation can be rejected with beamforming, forming a directional beam with multiple antennas. In other words, beamforming improves the azimuth and elevation resolution of the pulse radar beamforming system and provides the multipath/jamming immunity. Beamforming provides a high maximum range and low pulse power required for the pulse radar system. The number of the beamforming elements is determined from the desired beamwidth, SNR and beam pattern requirements. Beamforming provides an increase in the transmitted and received power and enhances the signal-to-noise ratio (SNR) of the wireless link. For instance, a 48 channel array implementation provides a steerable beamwidth (angular resolution) of 2.5°. A 48-element phased-array transmitter provides 33.6-dB improvement in EIRP (due to spatial power combining) and a 48-element phased array receiver improves the SNR 16.8 dB higher at the output.

2.4 Conclusion

This chapter presents the background information for the rest of the dissertation. History on radar, background information on radar waveforms and their properties, pulse compression radar, non-coherent integration are introduced. The motivation and use of beamforming for radar systems, polyphase codes as radar waveforms, their radar ambiguity function and autocorrelation characteristics (range ambiguity, velocity ambiguity, range sidelobes, doppler shift, minimum range etc.) are explained.

The conventional approaches of convolution matched filters are bulky, complicated and costly. Instead an analog correlator can accomplish the pulse compression like a matched filters and estimate the time of flight. Pulse compression radar improves the resolution and detection range of the conventional radar systems and an analog signal processing unit achieving the pulse compression is crucial for low power and low

cost radar systems. The specific radar waveform have specific autocorrelations and ambiguity functions, which are highly useful for the time of flight estimation with high resolution.

2.5 Acknowledgement

This chapter has been published in part in the following publications and patents:

1. M. Parlak, M. Matsuo and J. F. Buckwalter, "Analog Signal Processing Architecture for Pulse Compression Radar System in 90nm CMOS", *accepted to IEEE Transactions on Microwave Theory and Techniques*.

2. M. Parlak, M. Matsuo and J. F. Buckwalter, "Bidirectional Circuitry for Millimeter-Wave Pulse Compression Radar", *IEEE International Radar Conference (RadarCon)*, pp. 1062-1067, May 2011.

3- M. Parlak and J. F. Buckwalter, "Bidirectional Beamforming with Analog / Baseband Pulse Compression System", SD2012-389 - *Patent submitted via Tech Transfer Office at UCSD*.

The dissertation author was the primary author of this material.

Chapter 3

Proposed Pulse Compression Radar (PCR) Architecture

This chapter proposes an analog processing circuit for pulse compression radar for use together with a half-duplex, bidirectional beamformer, bringing the cost and power dissipation of the mobile pulse compression radar (PCR) down. In addition to the sensitivity boost, the beamformer and analog processing circuit improves the angle and range resolution of the pulse compression radar, respectively. The specifications and system concepts of the proposed PCR - bidirectional beamforming pulse radar front-end and baseband analog signal processing blocks - are presented. The specifications, resolution limits and maximum range limitation of the beamforming pulse-compression radar system in silicon are described in Section 3.1, 3.2 and 3.3, respectively. Various front-end and baseband PCR architectures, their block diagrams and advantages/disadvantages are shown and explained in Section 3.4. The proposed PCR is presented in Section 3.5. The chapter is concluded in Section 3.6. The relevant papers and patents are summarized in Section 3.7.

3.1 Specifications of Pedestrian Detection System

Fig. 3.1 outlines the maximum and minimum detection range specifications and also range and angle resolution specifications of the pulse compression radar. The range and angle resolution is the ability to distinguish between two neighboring objects on the

same bearing or at the same range, respectively. The specification for minimum and maximum detection range is 1 and 48 m, respectively. The range and angle resolution specifications (i.e. spacing between two pedestrians) are 40 cm and 1 m (1.2° at R_{max} = 48 m), respectively.

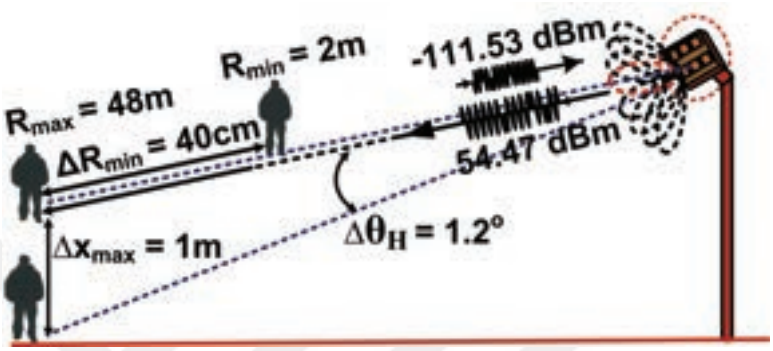

Figure 3.1: Specifications of the pedestrian detection sensor.

3.2 Range and Angle Resolution Limitation of PCR in Silicon

The achievable range resolution, ΔR, of a conventional pulse radar system is determined by the width, T, of the transmitted pulse, the types and sizes of targets, and transceiver specifications. In the first order, the range resolution in the propagation direction is approximately

$$\triangle R = cT/2 = c/2B \tag{3.1}$$

where B is the radar pulse bandwidth and T is the pulse width [32]. To improve the range resolution, the bandwidth of the radar signal should be increased (3.1). To improve the angle resolution, the overall antenna array size, Nd, of the pulse radar system should be increased to boost the antenna directivity and decrease half power beamwidth. However, due to the bandwidth limitations of phased arrays [29] which is shown as

$$\frac{B}{f_o} \leq 0.886 \frac{\lambda_o}{Nd \sin(\theta_a)}, \tag{3.2}$$

the range resolution degrades with the increasing antenna array size and is presented as (substituting (3.2) in the range resolution equation (3.1))

$$\Delta R \geq \frac{N d \sin(\theta_a)}{1.772}, \tag{3.3}$$

where f_o is the center frequency, λ_o is the signal wavelength, θ_a is the beam steering angle, N is the total number of elements, and d is the inter-element spacing of the antenna array.

Neglecting the element factor of the antenna, the angular resolution of the beamformer is determined by the 3-dB half-power beamwidth and is equal to

$$\Delta\theta_H = 102/N\cos(\theta_a). \tag{3.4}$$

The angular resolution as a distance between two targets is $\Delta x = R\,\Delta\theta_H$, where Δx_{max} is determined by the maximum detection range, R_{max}. The range resolution and angular resolution are dependent of each other and the dependency is presented as

$$\frac{\triangle R \triangle x_{max}}{R_{max} d} \geq \tan(\theta_a). \tag{3.5}$$

Fig. 3.2 illustrates the maximum beam steering angle satisfying the range and angle resolution specifications (3-5) with maximum detection distance and radar operating frequency.

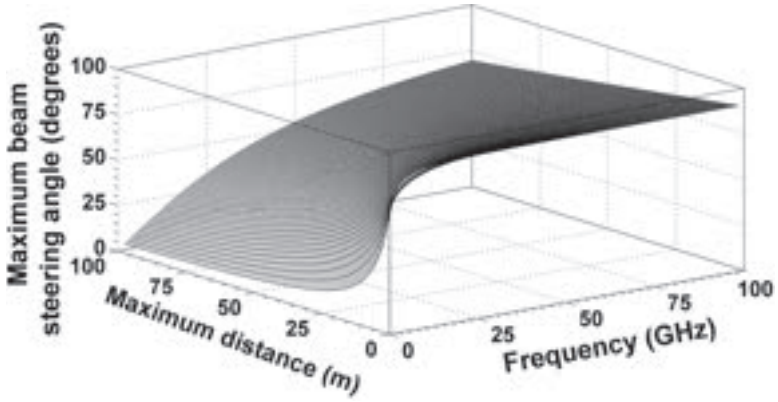

Figure 3.2: Maximum beam steering angle with maximum detection distance and radar operating frequency.

From (3.5), when R_{max} = 48 m and f_o = 60 GHz, $3.34 \geq \tan(\theta_a)$ and the maximum beam steering angle that satisfies both range and angle resolution specifications is θ_a = 73.3°.

The number of the beamforming elements required is determined from the desired resolution specifications for θ_a of 73.3°. From (3.4), the number of elements providing $\Delta\theta_H$ of 1.2° is 252. Therefore a 256 channel array implementation is proposed to provide a worst case angle resolution of 1.16° and a range resolution of 33.94 cm for a maximum steerable beamwidth of θ_a = 70°.

3.3 Maximum Range Limitation of PCR in Silicon

Fig. 3.3 illustrates the block diagram of the overall surveillance system, which includes the 256 channel transmit/receive beamforming front-end unit, the analog signal processing unit composed of the VGA, pulse compressor (correlator and integrator), analog-to-digital converter (ADC), non-coherent pulse integrator and a threshold device.

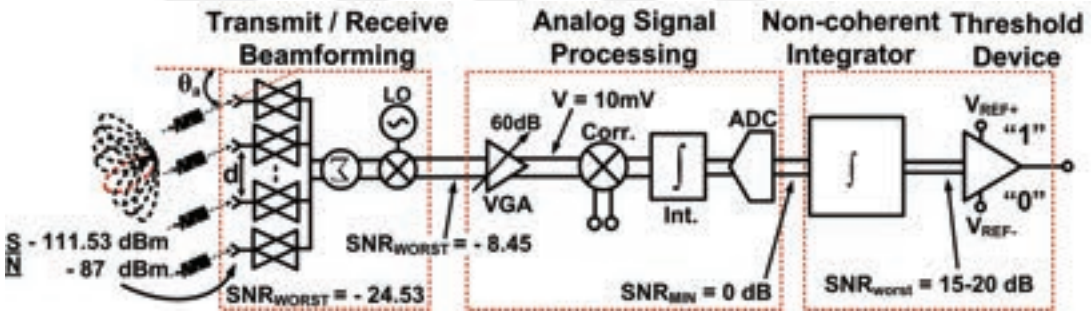

Figure 3.3: Block diagram of a pulse compression radar system for the pedestrian detection sensor.

While meeting the specifications, the system requires the desired signal-to-noise ratio (SNR) at the input of the non-coherent integrator to be 0 dB for reliable non-coherent pulse integration [32] as shown in Fig. 3.3. Therefore the minimum allowable SNR_{MIN} before the non-coherent integration is set to 0 dB at the maximum detection range of 48 meters and SNR_{MIN} equation is presented as

$$SNR_{MIN} = \frac{P_{TX}G_{TX}AF_{TX}G_{RX}AF_{RX}\sigma}{\frac{(4\pi)^3}{\lambda^2}R^4F_{RX}kBT_oL}G_{PCR} \tag{3.6}$$

where P_{TX} is the transmitted power, G_{TX} and G_{RX} are the transmitter and receiver antenna gain, AF_{TX} is the improvement in EIRP and AF_{RX} is the sensitivity boost at the receiver (due to spatial power combining at the transmitter and receiver), λ is the

carrier wavelength, σ is the radar cross section (RCS) of the object, R is the range to the object, F_{RX} is the receiver noise figure, B is the pulse bandwidth, kT_o is 4.10^{-21} J, L is the signal processing and atmospheric losses and G_{PCR} is the pulse compression gain factor. Of these parameters, the range (object distance) and radar cross scattering object-size (RCS) are related directly and independently to the object that we wish to detect and determine the total dynamic-range requirement.

As the range changes from R_{min} (1 m) to R_{max} (48 m), the input at the beamforming unit ranges between -111.53 dBm and -44.29 dBm - a dynamic range of 67.24 dB. The RCS of the largest and smallest objects vary from σ_{min} ($0.01m^2$) to σ_{max} ($1m^2$) resulting in an additional dynamic range of 20 dB. Designing circuits for 87.24 dB of dynamic range is challenging and central to the choice of circuit architecture of the radar system. At the input of the signal processing unit, the VGA needs to be designed to track the Friis path loss of 67.24 dB between R_{min} = 1 m and R_{max} = 48 m and the correlator needs to handle only 20 dB dynamic range due to the RCS of the object. Other challenges are increased transmitted power, increased antenna gain, decreased noise figure, decreased radar system losses, and decreased atmospheric losses for a maximum detection range of 48m. To alleviate the constraints on the transmitted power and beamwidth, beamforming and pulse compression together is an excellent solution to improve the sensitivity and SNR while also allowing for the directional beam to be steered.

As shown in Fig. 3.3, the worst case SNR at the input of beamforming is -24.53 dB for a signal bandwidth of 0.5 GHz. The sensitivity of the system is improved from -79 dBm to -111.53 dBm with 24.08 dB beamforming and 8.45 dB pulse compression boost as Fig. 3.4 illustrates the numerator and denominator of (3.6) for the link budget of the radar system including 256-channel beamforming, pulse compression and non-coherent integration.

A 256-element phased-array transmitter relaxes the requirements on the EIRP and provides 48.16 dB improvement in EIRP (due to spatial power combining) as the 256-element phased array receiver improves the sensitivity 26.84 dB. The requirements on the EIRP and SNR is further relaxed by pulse compression. As shown in Fig. 3.4, when only a 7-bit pulse compression code is used, the effective transmitted power is ideally 8.45 dB relaxed.

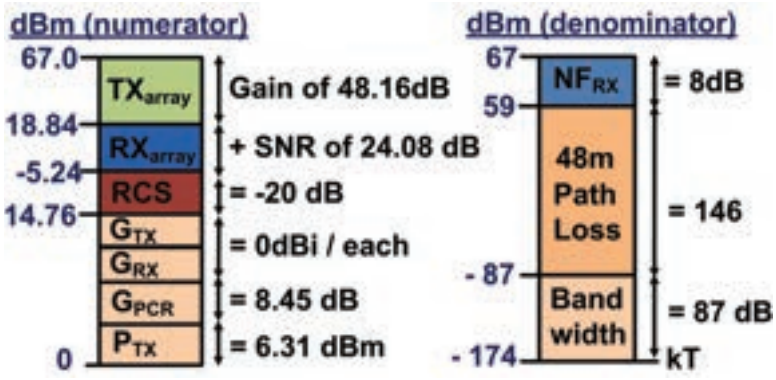

Figure 3.4: Link budget for a radar system with beamforming and pulse compression.

When calculating the range performance of the pulse compression radar, the effective transmitted power is modified and multiplied with the pulse compression ratio = BT as indicated in (3.6). It might appear from (3.6) as though the pulse compression radar is suddenly achieving much greater ranges due to the increase in the effective transmitted power. Unfortunately, the increased effective transmitted power is accounted for by a related increase in S_{min}. S_{min} increases with pulse compression ratio because the bandwidth of the receiver must be wide enough to handle at least the bandwidth, B, of the modulation within the pulse. The main power-related benefit of pulse compression radar is that it is able to achieve the maximum range performance of an equivalent narrow-pulse radar code with a much lower peak power level. When a barker code of length 7 is processed through the correlator, the effective transmitted power increases by $10log_{10}(7)$ = $8.45dB$, as shown in Fig. 3.4. Therefore, the system can reduce its peak power level without losing range performance. As shown in Fig. 3.3, the 0 dB of SNR at the input of the non-coherent integrator can be boosted to a SNR of 15-20 dB by integrating approximately 50 returns from Swerling I objects to achieve a detection probability of 0.90 and false alarm probability = 10^{-9} while a single pulse SNR is 0dB.

3.4 Trade-offs in Front-end and Baseband PCR Architectures

A simple system level architecture and better isolation between transmitter and receiver are main considerations when selecting the front-end of the radar system. Fig. 3.5 (a) depicts the front-ends of radar systems - frequency-modulated continuous-wave (FMCW) radar and pulse radar.

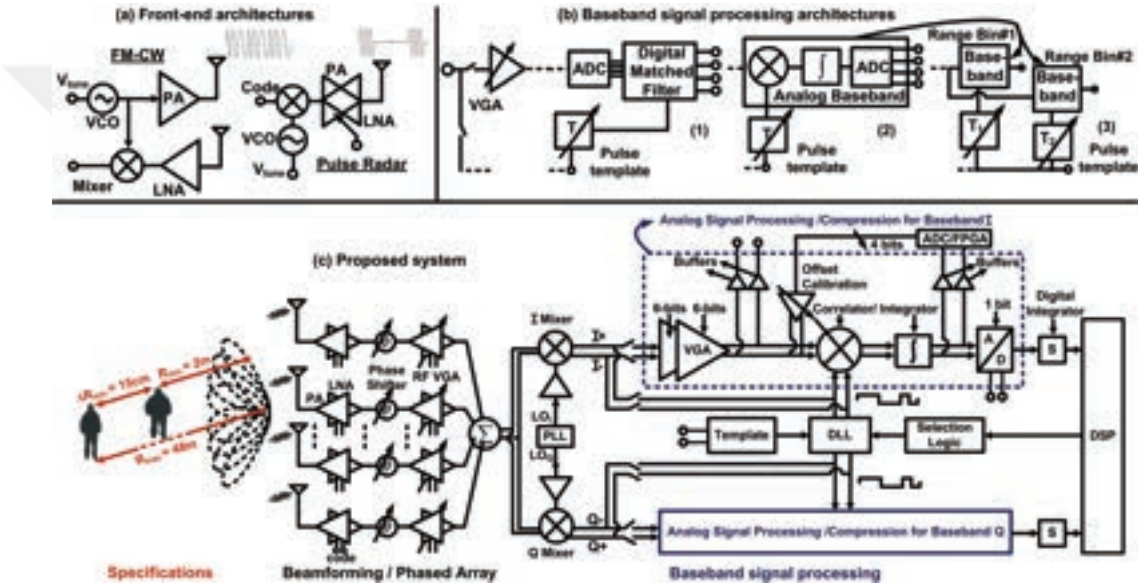

Figure 3.5: (a) Design choices between radar front-end architectures. (b) Design choices between baseband/analog signal processing architectures. (c) Block diagram of the proposed bidirectional front end with the implemented analog signal processing architecture.

While pulse radar transmits a pulse of energy and measures the time of arrival through correlation techniques, FMCW radars continuously vary a carrier frequency to directly compare the transmitted and received frequencies to produce a beat signal. The FMCW resolution is related to how fast and over how wide the FMCW bandwidth it is possible to generate a well-defined chirp. And the frequency sweeping linearity is an important parameter for target range detection. Without adequate isolation between the FMCW transmitter and receiver, the transmit energy leaks into the receiver and limits FMCW for long range detection because the transmit power level must be constrained by the receiver sensitivity. All of these put stringent specification on the on-chip voltage

controlled oscillators and FMCW.

It is necessary for FMCW radars to employ two well-isolated antennas, one for transmitting and one for receiving to allow continuous RF transmission. To use a single antenna for FMCW, a circulator must be introduced to the millimeter-wave front-end. This circulator is a costly discrete element and is not easily integrated. However space limitations in phased arrays generally suggest a single antenna for both transmit and receive. In pulse radars, the time-gated transmit and receive times imply that it is possible for the transmit and receive circuitry to share the same antenna array through T/R switches rather than expensive circulators. Fig. 3.5 (a-2) illustrates the front-end of the new radar architecture which enables to transmit a radar code with different phases and tune the radar code while time-gating the front-end circuits. A single-alone amplifier can be time-gated by the polyphase radar code to enable the power amplifier that transmits a burst of RF energy or low noise amplifier to await the echo.

In Fig. 3.5 (b), three baseband signal processing architecture options are shown. Shown in Fig. 3.5 (b-1), the digital baseband processing performs signal correlation in the digital domain. This provides the most reconfigurable system but demands high-speed, high-resolution ADCs [33]. The ADC precedes the digital matched filter (pulse compressor) and only has to accommodate the pre-compression dynamic range of the signal, which can be a significantly lower requirement. However, the ADC sampling rate must be at least twice the signal bandwidth. In addition, a digital matched filter with the same dynamic range and speed is also required. Shown in Fig. 3.5 (b-2,3), pulse compression and high-speed correlation is performed in analog domain and the speed requirement on the ADC is reduced by a factor equal to the duty cycle - the ADC only needs to sample and digitize the integrated value after each pulse. Overall power consumption is estimated to be over two orders of magnitude lower than the all-digital approach [34]. While the overall scan time in Fig. 3.5 (b-2) is longer than the one in Fig. 3.5 (b-3), the power consumption is the lowest. Shown in Fig. 3.5 (b-3), analog pulse compression is performed in parallel using multiple correlators for different delay values to search for objects at different range-bins.

3.5 Proposed PCR Architecture

The block diagram of the proposed PCR architecture is depicted in Fig. 3.5 (c). The architectures illustrated in Fig. 3.5 (1-b) and (2-b) are proposed at the front-end and back-end, respectively.

The front-end circuitry includes a bidirectional RF-phase shifting beamforming transceiver - a bidirectional RF amplifier that operates as either an LNA or PA [35], a bidirectional circuitry that operates as either an analog phase shifter or VGA [36], a passive phase shifter and a passive mixer which is inherently bidirectional. The radar code time-gates the LNA and PA, which makes this structure appropriate for the PCR system. Following the RF beamformer and mixer, the baseband/analog signal processing architecture is implemented. The baseband circuitry includes a two-stage VGA for high dynamic range, a correlator/integrator circuit, a comparator replacing an amplitude detector and ADC, and offset calibration circuits as shown in Fig. 3.5 (c). Non-coherent integration can be implemented after the comparator and is digitally processed in a microprocessor or FPGA.

For the single correlator analog-baseband approach, to gather data over a maximum detection of 48 m range, it requires 48 m/0.4 m = 120 range bins. For every code transmission from the radar system, different delays are assigned for the template signals of the correlator. In other words, for every signal transmission, one range bin is explored and template is swept once. The angle resolution is specified as a beamwidth of 1.16° as explained in Section 3.1. Assuming the beamformer of the pedestrian sensor system scans for 140°, it requires 140°/1.16° = 121 beam rotations. The detection time can be written as:

$$t_{scan} = \#_{ofrange-bins}.t_{PRP}.\#_{NCI}.\#_{ofrotations}. \tag{3.7}$$

Assuming a 2 Gb-s, 7-bit Barker code with a pulse repetition period of 333 ns - PRF of 300 MHz - is sent via the radar system, the time to scan the maximum detection range - worst case scan time - is 120 x 333 ns x 50 x 121 = 241.758 ms (3.7).

The time on target is given by $\theta_{3dB}/\theta_{scan}$ where θ_a is the 3dB beamwidth and θ_{scan} is the antenna scan rate in degrees per second. For a 2 Gb-s, 7-bit Barker code, time on target is 1.998 ms, therefore the antenna scan rate in degrees per second is

1.16°/1.998 ms = 0.58°/s. In case multiple parallel correlators are used as the analog signal processing units, each single beam scanning takes 50 x 333 ns = 0.0167 ms. And the total time to scan corresponds to 0.0167 ms x 121= 2.02 ms which is 120 times less than the single correlator approach. However the power required for this approach is 120 times more than the single correlator approach.

3.6 Conclusion

This chapter presents the system concepts of the proposed PCR - bidirectional beamforming pulse radar front-end and baseband/analog signal processing blocks - in order to bring the cost and power dissipation of the mobile pulse compression radar (PCR) down. Range resolution of beamforming pulse-compression radar degrades with the increasing array size, therefore medium size beamforming and analog pulse compression are used together to improve the range and angle resolution, maximum detection range, SNR, detection probability and false alarm requirements. The link budget for the radar link and the effect of beamforming, pulse compression and non-coherent integration on the link budget is investigated. After investigating the trade-offs in the front-end and baseband, a PCR architecture is proposed.

3.7 Acknowledgement

This chapter has been published in part in the following publications and patents:

1. M. Parlak, M. Matsuo and J. F. Buckwalter, "Analog Signal Processing Architecture for Pulse Compression Radar System in 90nm CMOS", *accepted to IEEE Transactions on Microwave Theory and Techniques*.

2. M. Parlak, M. Matsuo and J. F. Buckwalter, "Bidirectional Circuitry for Millimeter-Wave Pulse Compression Radar", *IEEE International Radar Conference (RadarCon)*, pp. 1062-1067, May 2011.

3- M. Parlak and J. F. Buckwalter, "Bidirectional Beamforming with Analog / Baseband Pulse Compression System", SD2012-389 - *Patent submitted via Tech Transfer Office at UCSD*.

The dissertation author was the primary author of this material.

Chapter 4

Analog Signal Processing Blocks for Pulse Compression Radar

This chapter presents the system concepts, circuits and measurement results of the baseband/analog signal processing of the pulse radar system presented in Chapter 3 and explained in this Chapter in details.

4.1 Circuit and System Design

The block diagram of the proposed PCR architecture is again shown in Fig. 4.1 for convenience.

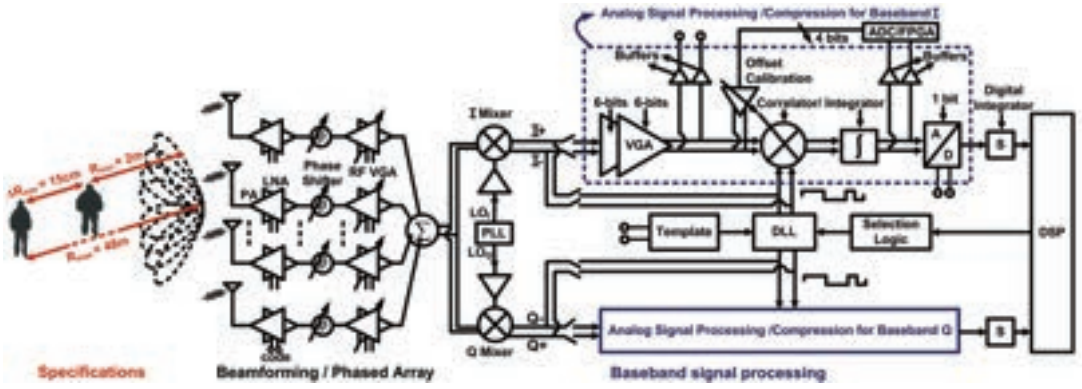

Figure 4.1: Block diagram of the proposed bidirectional pulse radar front end with the implemented analog signal processing architecture.

The front-end circuitry includes a bidirectional RF-phase shifting beamformer - a bidirectional RF amplifier that operates as either an LNA or PA [35], a bidirectional circuitry that operates as either an analog phase shifter or VGA [36], a passive phase shifter and a passive mixer which is inherently bidirectional. The radar code time-gates the LNA and PA, which makes this structure appropriate for the PCR system.

Following the RF beamformer and mixer, the analog signal processing architecture includes a two-stage VGA for high dynamic range, a correlator/integrator circuit, a comparator, and offset calibration circuits. The circuits are demonstrated in Section 4.1.1, Section 4.1.2, Section 4.1.3 and Section 4.1.4, respectively. The measurement results are summarized in Section 4.2. The chapter is concluded in Section 4.3 and the relevant papers and patents are summarized in Section 4.4.

4.1.1 Variable Gain Amplifier

VGAs have been demonstrated with discrete gain steps and digital control [37–39], or continuous gain control [40]. Discrete gain steps can be made through changes in the bias current through the RF transconductor and the changes in the load impedance. However this cause a group delay variation over the bandwidth which distorts the received signal. The current splitting approach provides a constant load and a constant bias current of the input transistor offering low VGA group delay imbalance. This approach tends to suffer from higher noise figure but offers high gain control range and low group delay imbalance compared to the other techniques. Therefore, this design was chosen for implementation.

Reported also in [41], Fig. 4.2 illustrates the schematic of the current splitting VGA topology. The bias current of the input transistor, I_{SS}, is split into two differential amplifiers. The gain variation is achieved by completely steering the bias current of the input transistors (M_i , i = 1...N) to two transistors, M_{iA} and M_{iB} to achieve a discrete-step of variable gain. The transistors M_{iA} are on and off depending on the digital control voltage. When the control voltage V_{i+} is high, the bias current is steered through M_{iA} and the input signal at the gate of M_i is amplified to the output. When V_{i+} is low, the bias current is steered toward M_{iB} amplifying the signal not to the output. The sizes of the input transistor as well as the current steering transistors are binary scaled for N-bit

operation to have the transconductance of each stage g_{m-i} binary scaled,

$$g_{m-i} = K_i(V_{gs} - V_t) = \sqrt{2K_iI_i} = 2^{i+1}\sqrt{2^{-N-1}K_oI_{SS}}, \tag{4.1}$$

where g_{mi} is the transconductance of M_i, K_i is proportional to W_i/L = 2^{i+1} μm / 90nm, I_i = $2^{i-N-2}I_{SS}$ is the bias current through the input transistor, M_i, and $V_{gs} - V_t$ is the overdrive voltage, which is same for each input transistor. The minimum gain of the one stage VGA is defined by the cascode transistor, M_0, which is α times smaller than M_1. The VGA voltage gain and gain variation per stage can be written as

$$A_V = g_{m0}R_d(1 + b_1 + 2\alpha b_2 + ... + 2^{N-1}\alpha b_N), \tag{4.2}$$

$$A_{max-min} = 20log_{10}(1 + (2^N - 1)), \tag{4.3}$$

respectively where g_{m0} is the transconductance of M_0, and b_1-b_N is the binary word for the control voltage V_{s1}-V_{sN}.

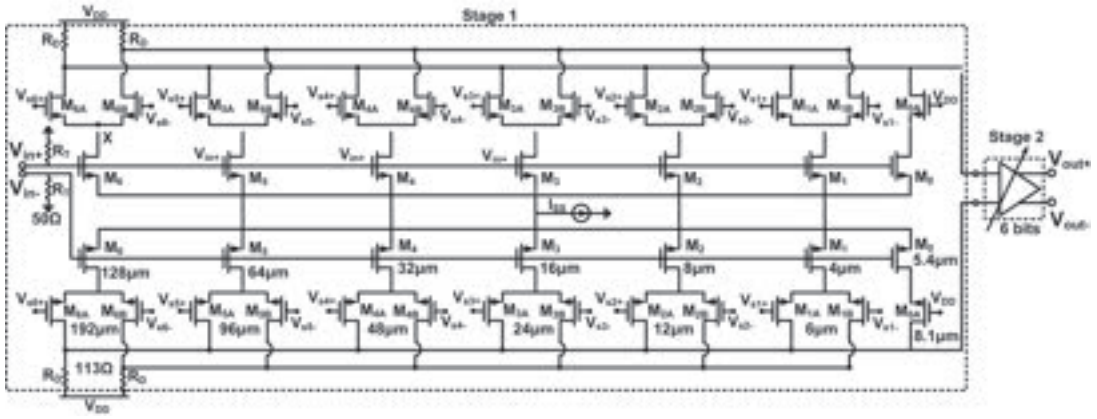

Figure 4.2: Circuit schematic of the variable gain amplifier.

As mentioned in (3.6), the path loss increases quadratically with the range and the VGA gain, G_{VGA}, is introduced such that the output power of the VGA, P_{RX}, is constant as the signal makes a round-trip. As the receiver waits for an echo of the transmitted pulse, the VGA gain compensates the path loss and reduces the dynamic range of the echo after the VGA. To track the Friis loss adaptively and reduce the dynamic range requirements of correlator, two linear-in-magnitude VGA circuits are cascaded with each having 6-bit digital control. To provide the calculated 67.24 dB gain variation (33.62 dB per stage), the number of bits are selected as six (4.3).

Fig. 4.3 (a) illustrates the SPECTRE simulated differential mode gain states of the VGA, A_{DM-DM}. The maximum and minimum gain states provide 19.1 dB gain and 48.1 dB attenuation at 1 GHz, respectively and VGA has a simulated gain range of 67.2 dB. The VGA requires a minimum signal bandwidth of larger than 375 MHz and the sub-pulse width of < 2.67 ns, set by the desired range resolution of ΔR < 40 cm. The simulated VGA exhibits a 3-dB bandwidth of 1.25 GHz to support up to a range resolution of 12 cm as shown in Fig. 4.3 (a). The simulated common mode gain, A_{CM-DM}, is illustrated in Fig. 4.3 (b). For 64 gain states, the common mode rejection is better than 60 dB as illustrated in Fig. 4.3 (c).

The theoretical and simulated VGA gain is compared to the Friis loss. As shown in Fig. 4.3 (d), while the signal penetrates between 1 m and 48 m, the VGA tracks the 67.2 dB Friis path loss within the minimum and maximum detection range (1 and 48 meters) and the simulation follows the theoretical Friis loss curve - G_{VGA} ~ $10log_{10}(R^4)$

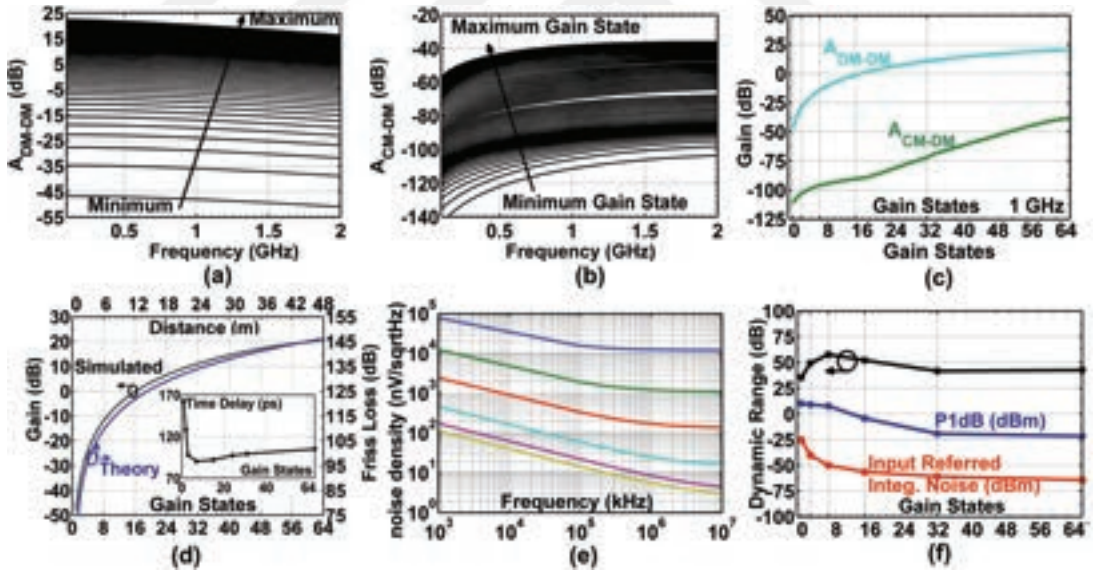

Figure 4.3: (a-c) Simulated differential mode gain, common mode gain and common mode rejection of the VGA for 64 states. (d) Theoretical and simulated Friis loss tracking. (e) Simulated input referred noise and (f) dynamic range.

The bias current variation for the current splitting stage changes the impedance at the common source node of the differential pair (labeled node X in Fig. 4.2), but this does not have much effect on the insertion phase. The output drain capacitance changes slightly due to the bias voltage variation at the gate-drain junction. As the

largest transistors (the higher order bits) are switched into the stage, the capacitance increases and introduces some phase shift. The simulated time delay of the VGA over various gain states is illustrated in Fig. 4.3 (d). The time delay imbalance is only 60 ps between the 64 VGA states.

The dynamic range of the VGA is the ratio of the input referred P1dB compression point to the input-referred noise level. The input referred noise density and integrated noise of the VGA are simulated for the same states as shown in Fig. 4.3 (e-f). The input referred spot noise is 12.6 μV/$\sqrt{Hz}$ and 5.65 nV/$\sqrt{Hz}$ at 1 MHz and input referred integrated noise power is -25 dBm and -64 dBm for minimum and maximum gain states for a noise bandwidth of 1 GHz, respectively. The large signal circuit response is illustrated in Fig. 4.3 (f). P1dB occurs at the input power of 10dBm, 9dBm, 7.5dBm, -4.45dBm, -19dBm, -21.6dBm for 6 various gain states = 1, 3, 7, 15, 31, 63, respectively. The dynamic range is 40-50 dB over 64 gain states.

4.1.2 Offset Calibration Circuits

The offset at the output of the VGA for minimum, mid and maximum gain states is illustrated in Fig. 4.4 (a). Via Monte Carlo simulations, the standard deviation of the offsets at the VGA output is found as 2.37 mV and 23.5 mV for minimum and maximum gain states, respectively. To track the Friis loss adaptively, VGA changes gain for every 2.5 ns (48 m/64 = 0.75 m) assuming a maximum distance of 48m. It is challenging to compensate the offset with a closed loop architecture settling in every 2.5ns.

To compensate the input/output offsets associated with the VGA, a 4-bit offset compensation circuit is introduced. The 4-bit input is provided to the circuit through the look-up table generated through manual calibration. In the manual calibration mode, the circuit output is measured without offset compensation and monitoring the correlator output, the offsets of the VGA are recorded into a look-up table via the analog-to-digital converters (ADCs) in the FPGA. The required values of the 4-bit sequence is then provided to the input of the on-chip offset calibration circuit via the FPGA and VGA and correlator output offset is corrected as shown in Fig. 4.4 (d-e).

As shown in Fig. 4.7 (a), the offset calibration circuit is a current splitting topology, similar to the VGA design. I_{ss} is controlled through an external bias to decide on

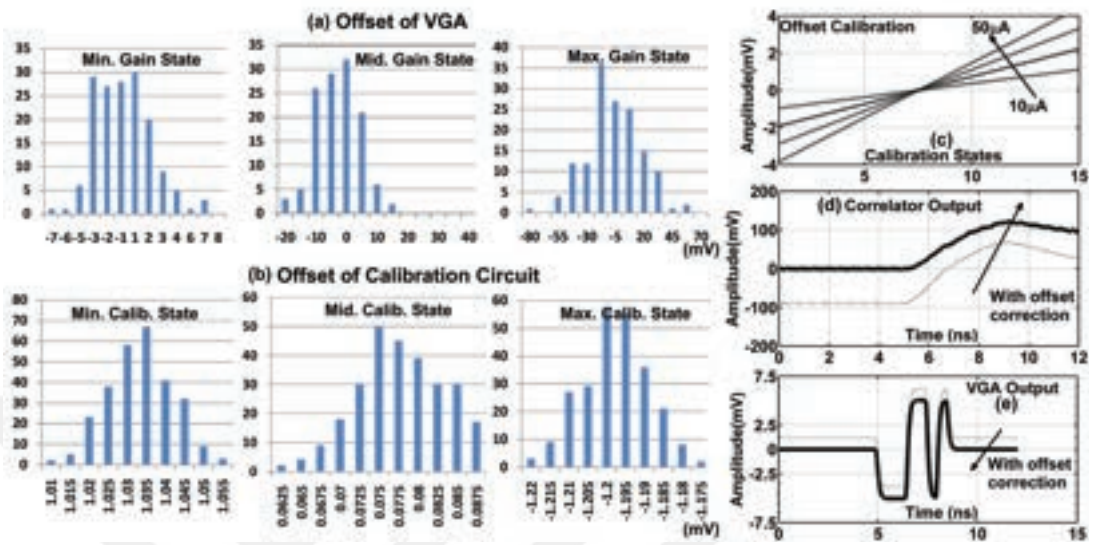

Figure 4.4: (a) Monte Carlo simulations of the offsets at the output of VGA and (b) at the output of the calibration circuit for various gain states. (c) Simulation of the offset correction control with the calibration bias current and (d-e) offset correction at the correlator and VGA output.

the $\pm$ peak value of the offset compensation. The 4-bit offset compensation (16 states) determines the resolution of the calibration as shown in Fig. 4.4 (c). The larger devices exhibit smaller mismatches therefore transistors M_{iA} and M_{iB} have a length of 0.30 μm to minimize the mismatch. As shown in Fig. 4.4 (a-b), the offsets of the calibration circuit are negligible compared to the VGA output offsets. The standard deviation is 10-15 μV for minimum and maximum calibration states, respectively.

4.1.3 Correlator

Fig. 4.7 (b) illustrates the schematic of the correlator and integrator circuits which are combined together as one circuit block. The Friis loss is adaptively compensated by the VGA gain preceding the correlator, therefore the signal swing at the input of the correlator is assumed to be constant, 10 mV. The pre-amplification stage - first stage in the correlator - provides 12 dB gain to boost the signal before the core correlation stage. While M_3 and M_4 provide the amplification, M_5 and M_6 operate as PMOS loads. The common mode feedback is provided via the resistors R_1 and R_2 of 1.5 kΩ

while lowering the gain is avoided.

As shown in Fig. 4.7 (b), following the pre-amplification stage, the correlation is performed at the core correlation stage. The correlator stage is a folded cascode current commuting correlator with cascode PMOS loads, M_{24-27}. PMOS folded cascode provides a low input flicker noise and better slew rate. Transistors M_{14-15} act as current sources, providing a pivot point for folding over the differential-pair output currents. Transistors M_{20-23} act as cascode transistors, pinning the drains of transistors M_{16-17}. The core correlator output is integrated on a capacitor-bank of 1pF - 12 pF to reduce/increase the correlator output charging time and signal level, depending on the speed of the radar code.

Following the core correlation, post amplification is performed to bring the signal to a level and the integrated voltage is compared with a threshold level in the comparator for the signal detection of incoming signal and calculation of the TOF. The integrated voltage is normally sampled by an ADC after each pulse and the shunt switches M_{28-29} resets the correlator at the end of the template pulse transmission for the preparation for the next pulse. The accumulation of multiple signals to achieve higher SNR than 0 dB is performed in the digital domain. Also, a switch M_{32} is added at the post-amplifier to increase/decrease the signal level due to the RCS changes of various objects. All PMOS transistors have source tied to substrate to avoid increased threshold due to body effect.

As illustrated in Fig. 4.5, different lengths of Barker codes are given as inputs and templates to the chip to investigate their effect on the correlation and monitor the correlator output. When the template signal is aligned with the input, and longer Barker codes are provided, the signal level at the output of the correlator increases as illustrated in Fig. 4.5 (a). The correlator output is sampled when the template signal returns to zero, and autocorrelation (zero cut in delay when doppler frequency is zero) of various codes is illustrated in Fig. 4.5 (b). It shows that the simulated results of the circuit exhibit the autocorrelation properties of the Barker codes.

The switch M_{32} increases/decreases the signal level at the output of the correlator depending on the RCS of various objects. Fig. 4.6 (a) illustrates the correlation output when the switch gate control (b_1) is on and off. The capacitor-bank of 1 pF - 12 pF

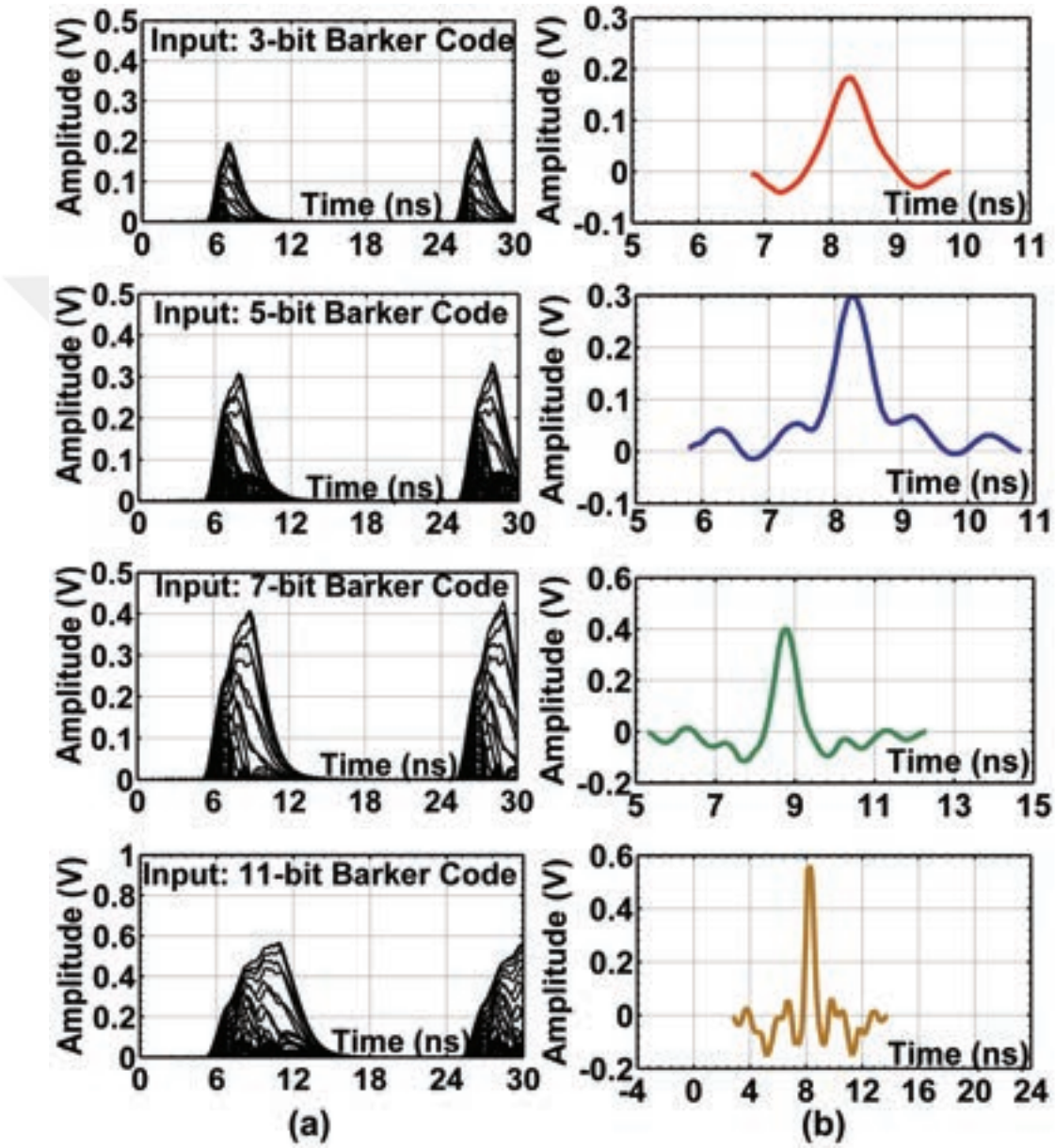

Figure 4.5: (a) Simulation of the correlation of the incoming signal with the aligned and non-aligned templates. (b) Autocorrelation for various Barker codes.

also increases/decreases the correlator output signal level, depending on the speed of the radar code. Fig. 4.6 (b) illustrates the correlation output with different combinations of the correlator bank capacitors.

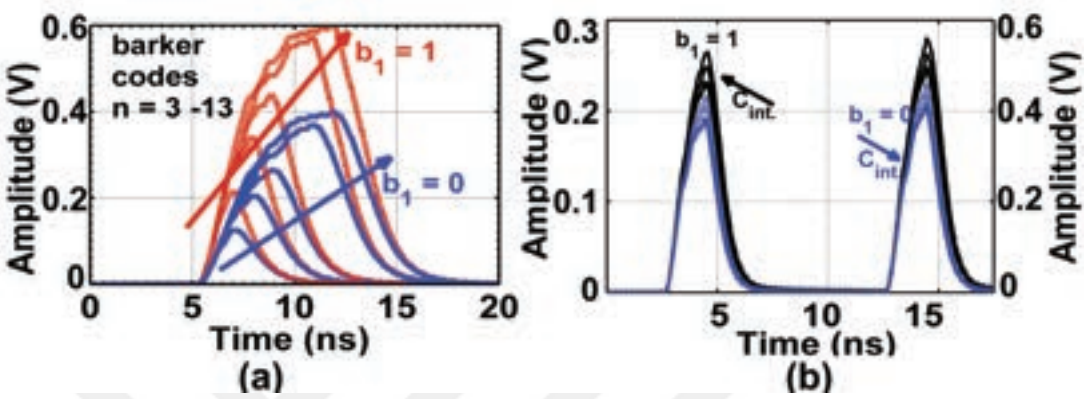

Figure 4.6: (a) Correlation output with the switch control. (b) Correlation output with both varying correlator bank capacitors and switch control.

4.1.4 Comparator

A comparator is designed to provide a one-bit sample of the correlated output. Fig. 4.7 (c) illustrates the schematic of the comparator. The comparator consists of two differential input pairs (M_{3-6}), a regenerative flip-flop (CMOS latch circuit), and a S-R latch. The CMOS latch is composed of an n-channel flip-flop (M_{7-8}) with a pair of n-channel transfer gates (M_{10-11}) for strobing, an n-channel switch (M_9) for resetting, and a p-channel flip-flop (M13, M14) with a pair of p-channel precharge transistors (M_{12-15}). Set (latch) and reset (latch-bar) are the two non-overlapping clocks.

During the reset period, the current flows through the closed resetting switch M_9, which forces the previous two logic state voltages to be equalized. As the input stage settles, a voltage difference is established between nodes A and B and acts as an initial imbalance for the following regeneration time interval. In the meantime, as the n-FET flip-flop is reset, the p-FET flip-flop is also reset by the two closed precharge transistors which charge nodes C and D to the supply voltage. As a result, the CMOS latch is set to the astable high-gain mode. The regeneration is initialized by the opening of switch M12. Since the strobing transistors (M_{10-11}) isolate the n-FET flip-flop from the p-

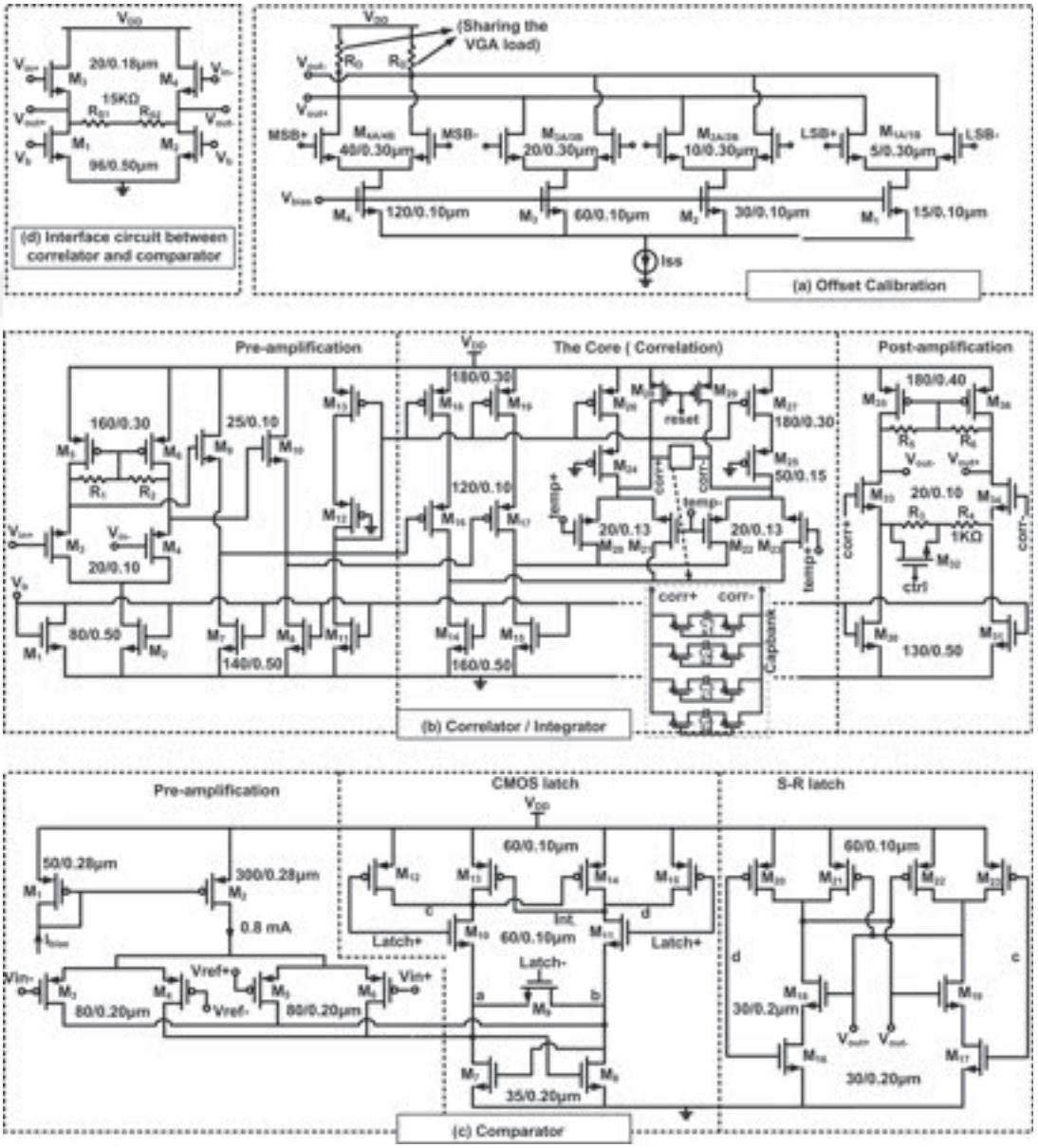

Figure 4.7: (a) Circuit schematic of the offset calibration circuit. (b) Circuit schematic of the correlator and integrator. (c) Circuit schematic of the comparator.

FET flip-flop, the use of two non-overlapping clocks perform the regeneration which is within the short time slot between reset going low and going high when set is low.

The second generation step starts when set goes high and (M_{10-11})are closed. The n-FET flip-flop together with the p-FET flip-flop regenerates the voltage differences between nodes a and b and between nodes c and d. The voltage difference between node c and node d is soon amplified to a voltage swing nearly equal to the power supply voltage. The following S-R latch is driven to full complementary digital output levels at the end of the regenerative mode and remains in the previous state in the reset mode.

As shown in Fig. 4.7 (c), the correlated/integrated signal V_{in} is compared with a reference signal V_{ref} which is externally provided to the chip. When $V_{in} \geq V_{ref}$, the latched comparator employ strong positive feedback for a "regeneration phase" when the clock is high, and have a "reset phase" when the clock is low. If the received echo signal is aligned with the template code, a digital high is observed at the output of the comparator and the time of flight is found.

4.1.5 System Simulation

As shown in Fig. 4.8, a 7-bit Barker code with a sub-pulse width of 0.5 ns is applied at the input of the baseband system and the sensitivity of the correlator to the

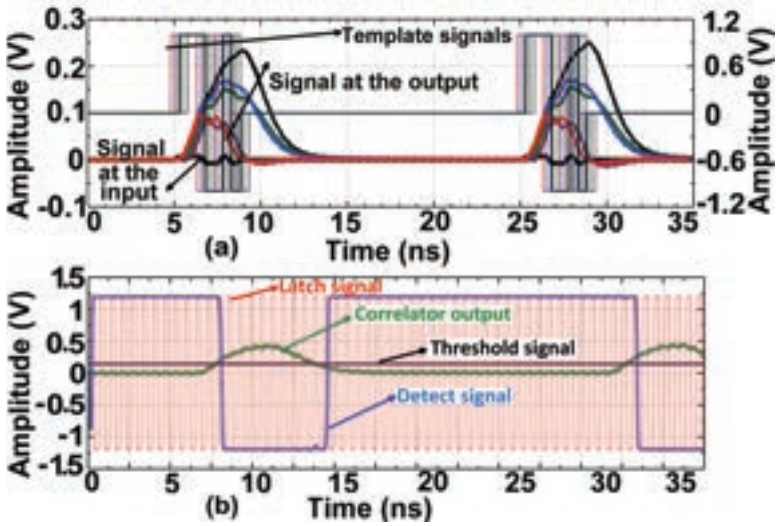

Figure 4.8: (a) Simulation of the correlation of the input signal with the shifted templates in time (b) Illustration of the comparator signals and radar signal detection.

timing alignment between the received signal and the template is simulated. The TOF is 5.7 ns. The template signal is swept between 1.75 ns and 8.75 ns. When the template signal is aligned with the input at 5.7 ns, the maximum correlation voltage is observed.

4.2 Measurement

Fig. 4.9 shows the chip microphotograph of the 90-nm CMOS circuitry and chip-on-board (COB) implementation of the prototype. The chip has an area of only 0.51 mm^2 excluding the pads.

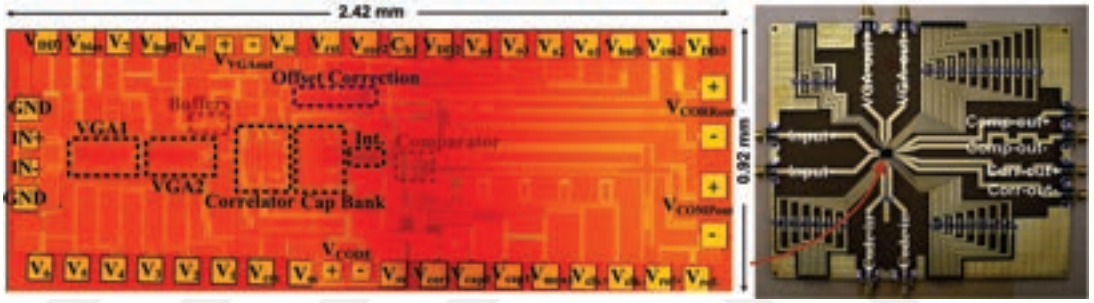

Figure 4.9: The chip microphotograph and chip-on-board (COB) implementation of the prototype.

The proposed baseband circuits are fabricated in TSMC 90-nm CMOS mixed-signal/RF low power process. Nine metal layers are available with the 3.2 μm thick aluminum top metal layer (M9). The silicon chip is epoxied to a grounded island and wire-bonded to a single-layer FR4 printed circuit board. Bondwire coupling is minimized using several ground connections between the RF inputs. The supply is bypassed off-chip with 100 nF capacitors to provide a low impedance. ADS Momentum is used to simulate the transmission lines on the laminate board which has a substrate thickness of 1.57 mm. The dielectric constant of the substrate is 4.3 and the effective dielectric constant is 3.26. The 50 microstrip line has a width of 3 mm (= 0.053 dB/cm). The VGA and monitoring buffers consume 14 mA and 16 mA from a 1.2 V supply. The correlator and monitoring buffers consume 4.1 mA and 13 mA from 1.2 V supply, respectively.

4.2.1 Variable-Gain Amplifier (VGA)

The VGA consumes 14 mA from a 1.2 V supply and has an area of 0.04 mm^2. The *S*-parameters are measured using the Agilent N5242A 4-port network analyzer calibrated with a 4-port E-cal. The A_{CM-DM} and A_{DM-DM} are also monitored through the VGA buffers and illustrated for each of the 64 gain states in Fig. 4.10 (a) and (b), respectively. The maximum gain state provides 19 dB gain and the minimum gain state provides 34 dB of attenuation at 1 GHz , providing a total gain range of 52 dB. The VGA measured 3-dB bandwidth is 800 MHz due to underestimated capacitance. The measured differential mode input return loss and isolation is plotted in Fig. 4.10 (c). Across the 64 different gain states, the input return loss is better than 20 dB and the isolation is better than 40 dB.

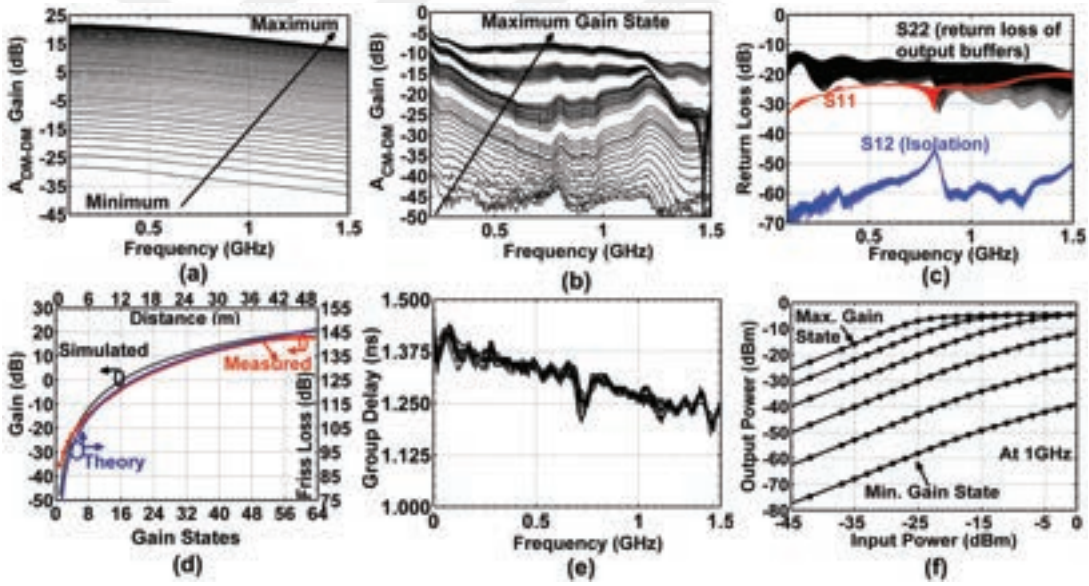

Figure 4.10: (a-c) Measured differential mode gain, common mode gain and return loss. (d) The theoretical, simulation and measurement of the VGA Friis loss tracking. (e) Measured group delay variation and (f) linearity characteristics of the VGA for each of the 64 gain states.

As shown in Fig. 4.10 (d), the measured gain of the VGA tracks the Friis loss within the minimum and maximum detection range very closely (1 and 48 meters). In short distances less than a meter, the VGA is not able to track the Friis loss due to the abrupt changes in the loss.

The group delay variation across gain states of the VGA is important to detect pulse compression codes and is measured over 1.5 GHz as shown in Fig. 4.10 (e). Over the 64 gain states, the measured maximum group delay variation is 50 ps. The largest variation occurs at 800 MHz. The measured input power 1-dB compression, P_{1dB}, at 1 GHz is plotted in Fig. 4.10 (f). P_{1dB} is -26 dBm for the maximum gain state and -15 dBm for the minimum gain state. The saturated output power is -5 dBm for 64 gain states. The overall VGA performance and a comparison with other works is summarized in Table 4.1.

Table 4.1: Comparison to reported VGAs

Ref.	Tech. (μm)	Freq. (MHz)	Gain (dB)	P1dB (dBm)
[42]	0.35	470-870	-17$\sim$16	-
[37]	0.18	65	-22$\sim$32	-
[43]	0.18	32-1050	-52$\sim$43	-48$\sim$-17
[39]	0.18	4-900	-55$\sim$39	-59$\sim$-11
[40]	0.09	2250	-10$\sim$50	-55$\sim$-13
This work [41]	0.09	1250	-29$\sim$23	-26$\sim$-15

4.2.2 VGA, Offset Compensation and Correlator Blocks

The 3-level input signal and template signal is provided with a Stratix IV FPGA and 16-bit, 1 GSps 2channel DA converters on the FPGA board as shown in Fig. 4.11. The commutating transistors in the correlator and VGA input are being driven by the 3-level sequences provided by the FPGA board and DACs on the board. The codes to create the Barker and PRN sequences are written in Quartus environment. To mimic very low level radar returns at the input, external SMA attenuators are used. The analog pulse compressor is tested in various scenarios to evaluate the system performance for different polyphase codes and parameters - number of sub-pulses, period of the sub-pulses and pulse repetition frequencies of the pulse.

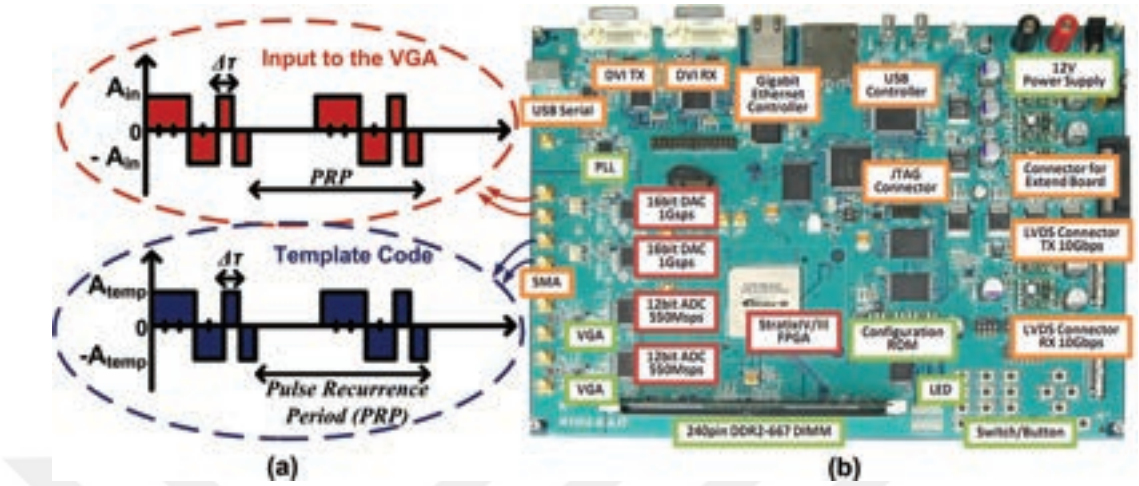

Figure 4.11: (a) The input and template polyphase code parameters and (b) the FPGA used for 3-level waveform creation.

As illustrated in Fig. 4.12, a 3-level template signal (1GB-s 5-bit Barker code) provided with a Stratix IV FPGA is swept in time via the FPGA registers to monitor the correlation output. The correlator output is sampled at the end of each template code and is monitored to create the 5-bit barker code autocorrelation as shown in Fig. 4.12.

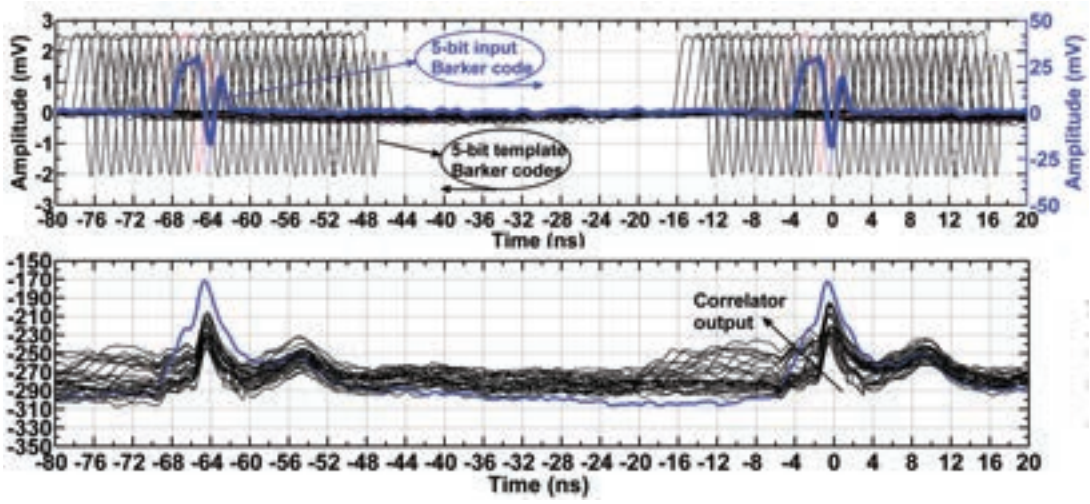

Figure 4.12: Measured correlator output with template signals swept in time.

The correlator output is also monitored with the changing VGA states. For simplicity, the input signal amplitude is kept constant while VGA gains are varied. As illustrated in Fig. 4.13 (a), the increasing VGA gain increases the signal amplitude at

the correlator output, however it brings different offset values at the output, which is compensated with the offset compensation circuit and FPGA.

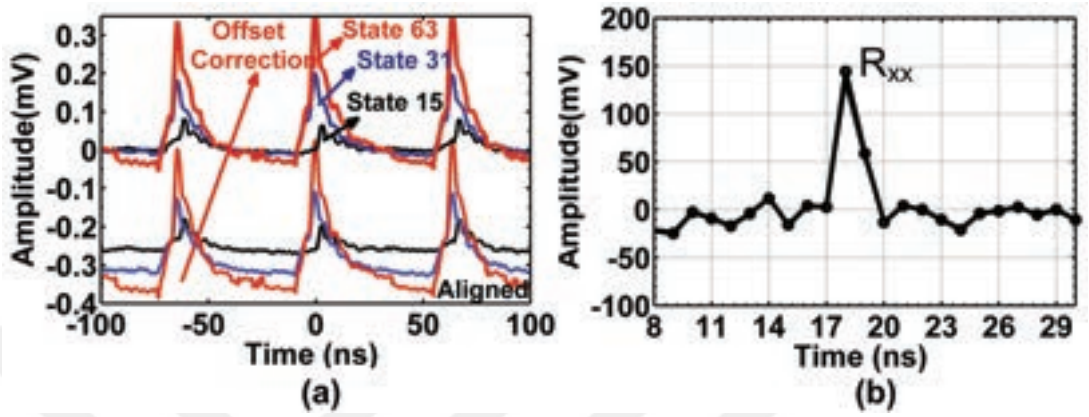

Figure 4.13: (a) Measured VGA gain states in time domain and the offset correction of the corresponding states. (b) Measured autocorrelation for the 1GB-s 5-bit Barker code.

In Fig. 4.13 (b), the measured autocorrelation of the 5-bit Barker code is shown. The alignment occurs for the template corresponding to 18 ns, which determines the TOF of the signal and the distance of the object, 5.4 m. As demonstrated, the sidelobes occur when the template is not aligned with the incoming signal. The only non-ideality is that the side-lobe at 19 ns should have been placed at much lower values than 60 mV to provide the dynamic range required.

4.3 Conclusion

The design and measurement results of a baseband analog signal processing are presented to bring the cost and power dissipation of the mobile pulse compression radar (PCR) down. The implemented analog signal processing circuitry exhibits the autocorrelation properties of the polyphase codes, maximizes the sensitivity and resolution of a pulse radar system and alleviates speed and resolution requirements of the ADC via an analog correlator. The circuitry includes a two-stage variable gain amplifier (VGA) for high dynamic range, a correlator/integrator circuit, a comparator, and offset calibration circuits. The differential, 6-bit VGA is designed to adaptively track the Friis path loss through rapid change of the VGA gain and offset calibration, relaxing the dynamic range

requirements of the correlator. The measured performance shows a VGA gain variation of 52dB and a VGA group delay imbalance of 50 ps over 64 states. The high-speed pulse compression/correlation is performed in analog current domain and the speed requirement on the ADC is reduced by a factor equal to the duty cycle lowering the ADC power consumption. The chip is fabricated in a 90nm process, wire-bonded on the FR4 printed circuit board and tested with a Stratix IV FPGA board to evaluate the system performance for different radar polyphase codes.

4.4 Acknowledgement

This chapter has been published in part in the following publications and patents:

1. M. Parlak, M. Matsuo and J. F. Buckwalter, "Analog Signal Processing Architecture for Pulse Compression Radar System in 90nm CMOS", *accepted to IEEE Transactions on Microwave Theory and Techniques*.

2. M. Parlak, M. Matsuo and J. F. Buckwalter, "A 6-bit Wideband Variable Gain Amplifier with Low Group Delay Variation in 90nm CMOS", *IEEE Topical Meetings on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, pp. 147-150, Jan. 2012.

3. M. Parlak, M. Matsuo and J. F. Buckwalter, "Bidirectional Circuitry for Millimeter-Wave Pulse Compression Radar", *IEEE International Radar Conference (RadarCon)*, pp. 1062-1067, May 2011.

4. M. Parlak and J. F. Buckwalter, "Bidirectional Beamforming with Analog / Baseband Pulse Compression System", SD2012-389 - *Patent submitted via Tech Transfer Office at UCSD*.

The dissertation author was the primary author of this material.

Chapter 5

Bidirectional Circuits for Pulse Compression Radar Beamforming

This chapter presents the silicon mm-wave circuits proposed and implemented to reduce the cost, area and power consumption of the beamforming systems while maintaining low noise figure (NF), power consumption, and high bandwidth. The wide spectrum around the millimeter wave bands, V-band and W-band, offer sufficient bandwidth to allow cm-range resolution for the indoor/outdoor surveillance systems. This chapter specifically investigates the performance of the W-band novel bidirectional circuit elements which are later proposed to place in a bidirectional active phased array transceiver and which can be placed at the front-end of a low power and low cost pulse compression radar (PCR) system. Section 5.1 introduces the motivation for bidirectional beamforming/phased arrays. In Section 5.2, cascaded constructive wave amplifier (CCWA) is introduced. Circuit analysis, simulation, and measurements of the W-band bidirectional amplifier (BCWA) are presented in Section 5.3. Circuit analysis, simulation, and measurements of the bidirectional phase shifter and variable gain amplifier are presented in Section 5.4. Section 5.5 introduces the motivation for passive switched-beam transceivers. Circuit analysis, simulation, and measurements of the dual-channel distributed amplifier for passive switched-beam transceivers are presented in Section 5.6.

5.1 Bidirectional Active Beamforming/Phased Arrays

Bidirectional elements are motivated by the requirements of the scalable multi-antenna systems and mm-wave phased array transceivers to address the size, weight, power, and cost associated with the millimeter-wave circuitry. Bidirectional front-ends functioning in either direction eliminates the microwave switches before and after the low-noise amplifier/power amplifier. Earlier work focused on a GaAs HEMT common gate topology as a bidirectional amplifier but is limited by the difficulty to simultaneously optimize the common gate device for both low-noise and high-power [44]. Further development of this approach was motivated by the need for scalable bidirectional transceiver front-end elements for phased arrays implemented in GaAs [45]. Recent work in silicon has investigated bidirectional front-end elements based on microwave switches before and after the LNA [7]. The disadvantage of this switch is that it contributes loss to the RF signal path which ultimate limits receiver sensitivity as well as reducing PA output power and efficiency. Another recent work on silicon investigates the design of a PALNA (PA-LNA) bidirectional amplifier that uses transmission line matching techniques to isolate the power amplifier and low-noise amplifier under different bias conditions and eliminates the sensitivity penalty of microwave switches at the front-end [46].

Phased array circuits are complicated by linearity concerns and calibration across each receive path. In an RF phase-shifting transceiver, the low-noise amplifier (LNA) should provide a low noise factor and the power amplifier (PA) should provide high efficiency and high signal power. A phase shifter is necessary to steer the beam 360 ° and a variable gain amplifier varies the gain while compensating the loss. The phase shifter and VGAs are placed in both receiver and transmitter channel, increasing the area, cost and power of the system. Calibration circuits are also needed in each RF path to minimize the phase and amplitude mismatch in each channel.

Fig. 5.1 shows the conventional RF beamforming and the proposed bidirectional beamforming front-end. Bidirectional elements - amplifiers, phase shifters, VGAs, calibration circuits and passive mixers - simplify the block diagram of the phased array extensively as shown in Fig. 5.1. Bidirectional front-end has the additional advantage of requiring one amplifier instead of one LNA and PA and one passive mixer rather than

two mixers for the transmit and receive paths. Consequently, the LO distribution is simplified. A digitally controlled phase shifter composed of the cascaded switch elements is inherently bidirectional and can be used to steer the antenna pattern and beam electronically as shown in Fig. 5.1. Following the phase shifter, the bidirectional analog phase shifter and VGA calibration circuit provides continuous phase and amplitude control and allows the calibration of the relative phase and gain errors between channels, incorporating the loss compensation at the same time as shown in Fig. 5.1. The bidirectional phase/gain calibration circuit controls the amplitude and phase of the RF signal in each channel and prevents the increased sidelobe levels, reduced directivity, pointing errors and symbol errors due to the phase and amplitude errors between channels of the phased array systems.

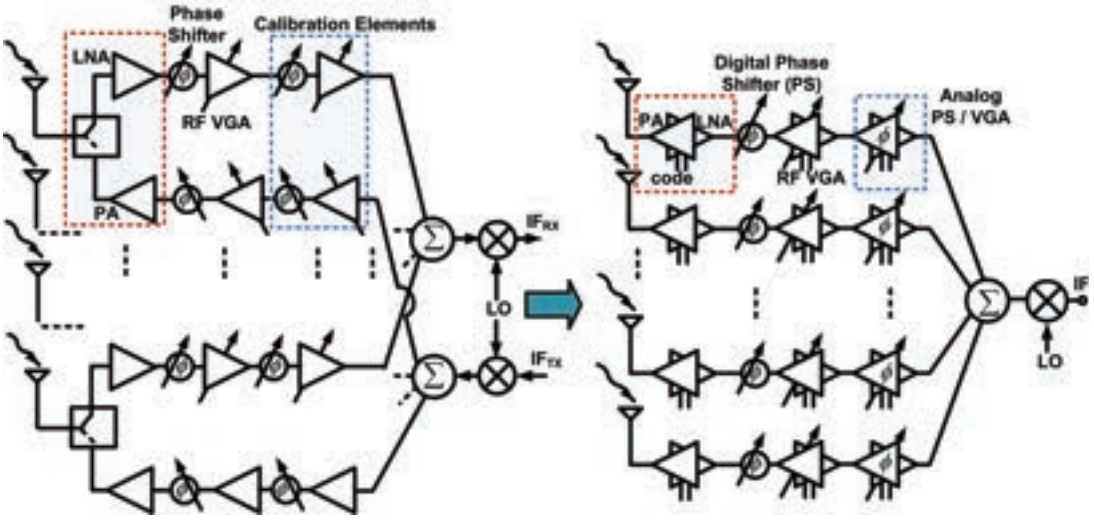

Figure 5.1: Conventional RF phase shifting beamforming transceiver compared to bidirectional RF phase shifting beamforming transceiver.

The *W*-band front-end bidirectional amplifier proposed in this chapter replaces both the LNA and PA in an conventional phased array channel at the same time. Similarly, the bidirectional *W*-band analog phase shifter/VGA replaces the calibration circuits. Both bidirectional amplifier and phase shifter/VGA performance can be tuned adaptively to change the gain, noise figure, output power or linearity of the front-end circuit.

5.2 Cascaded Constructive Wave Amplifier

The bidirectional circuits implemented is based on the cascaded constructive wave amplifier (CCWA) which consists of identical traveling wave amplifier stages [47]. The constructive wave amplifier uses a transmission line and an active shunt feedback circuit which feeds current back to the input of the quarter-wave transmission line to introduce a small amount of positive feedback to generate gain as shown in Fig. 5.2. CCWA gain and noise figure measurement results are presented in [47] and are also illustrated in Fig. 5.2.

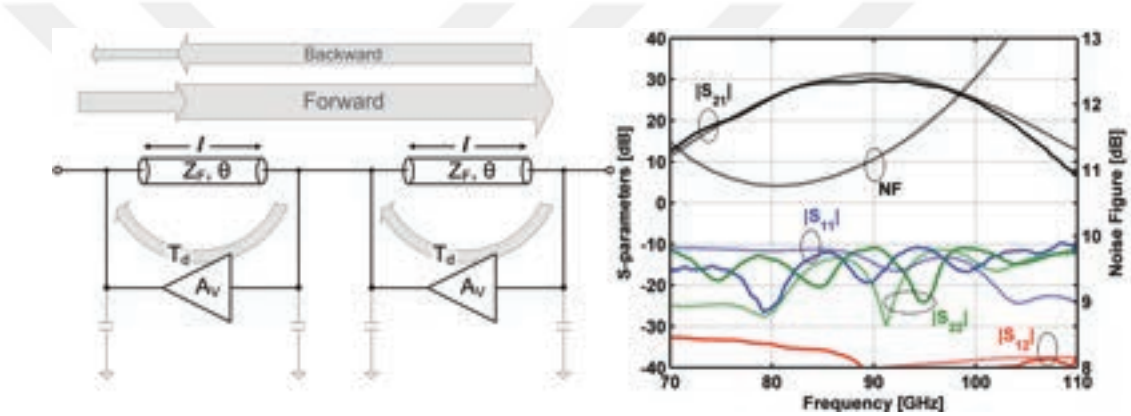

Figure 5.2: Cascaded constructive wave amplifier (CCWA) model and measured results.

5.3 W-Band Bidirectional Amplifier

Switches based on highly-scaled silicon devices tend to introduce high-loss, around 4 dB at *W*-band in highly scaled CMOS processes. This insertion loss comes at a substantial cost to the noise figure and output power of the system. A switch also limits the minimum range in radar systems since a reflected pulse will not be received during the transmit pulse and subsequent receiver recovery time due to the switch settling time. A recovery time of 3 ns corresponds to a minimum range of 0.9 m. Instead a bidirectional amplifier that switches between low-noise amplification and power amplification with a parallel control is proposed to avoid these insertion losses and minimize the recovery time. The alternatives to conventional architectures, switchless half-duplex transceivers, are presented in Section 5.1. PALNA and bidirectional constructive cas-

caded travelling wave amplifier (BCCWA) implementations replacing the conventional architectures are shown in Fig. 5.3. While the BCCWA eliminates the need for an antenna switch, it also requires only one mixer, i.e a passive mixer which is bidirectional inherently. Therefore bidirectional amplifier architecture lets the designer electronically select forward or backward wave amplification and independently optimize for RX/TX.

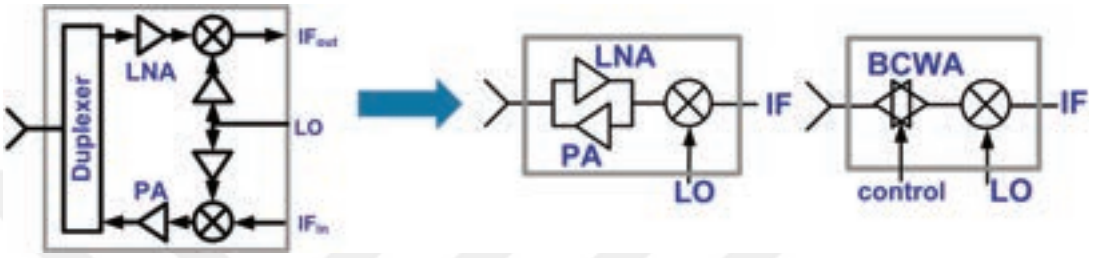

Figure 5.3: Conventional half-duplex transceivers and switchless half-duplex transceivers - PALNA and BCCWA architectures.

Previously, PALNAs are designed with various architectures in various process as shown in Fig. 5.4. When PA and LNA are connected in anti-parallel, operating in either transmit or receive mode, the base biasing of the PA and LNA circuits is alternated. Design issues related to ensuring matching under transmit and receive conditions occur.

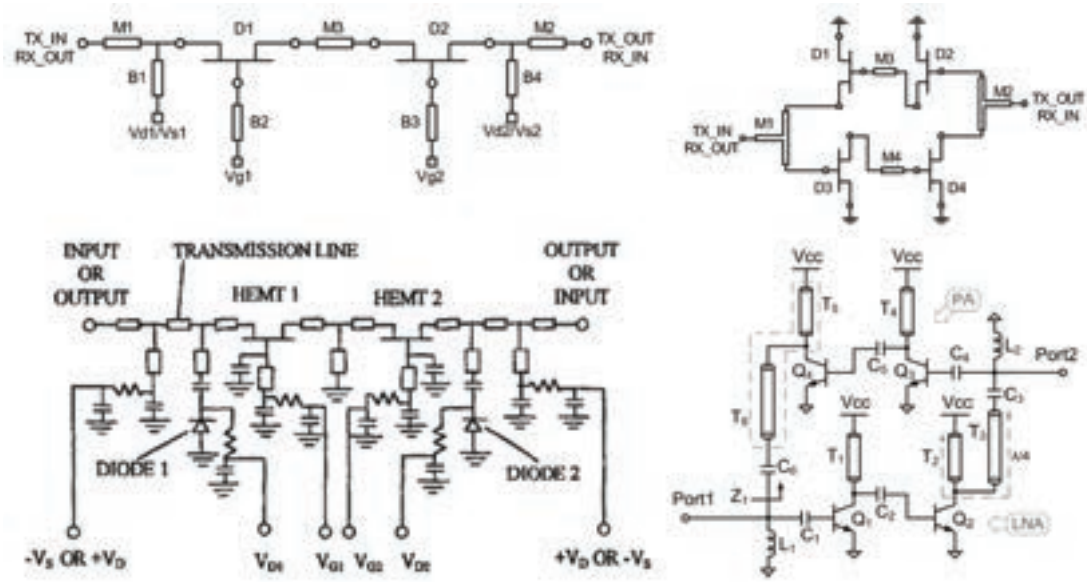

Figure 5.4: Previously reported bidirectional architectures.

5.3.1 Circuit Design

The bidirectional amplifier architecture is based on the recently demonstrated CCWA and consists of identical traveling wave amplifier stages. The prior work, CCWA, incorporated only one feedback amplifier to amplify the traveling wave in only one direction [47]. Here, we demonstrate a bidirectional constructive wave amplifier (BCCWA) circuit incorporating two anti-parallel feedback amplifiers which are modeled as a transconductance, g_m and which are modulated by the traveling wave at the output of the stage as shown in Fig. 5.5 (a).

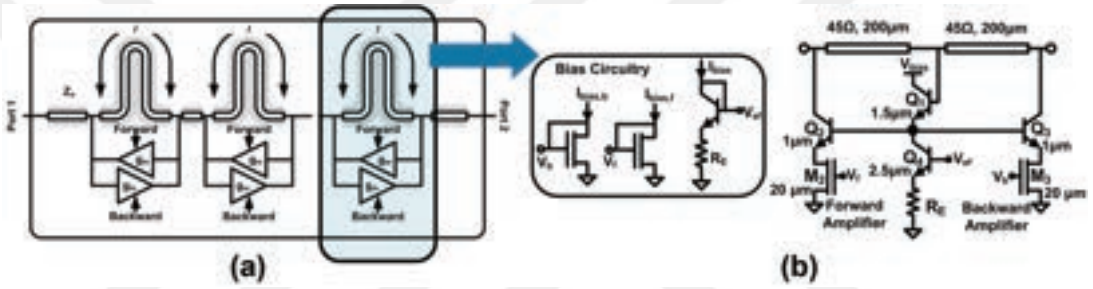

Figure 5.5: (a) Block diagram of the proposed BCCWA and (b) circuit schematic of one stage.

Fig. 5.5 (b) illustrates the schematic for a single bidirectional constructive wave amplifier stage in the silicon-germanium process as well as common biasing circuits. The circuit implementation consists of ten identical cascaded bidirectional amplifier stages. Each stage has an emitter follower, Q_1, and current source consisting of Q_4 and R_E. The emitter width of Q_1 is 1.5 μm. The emitter follower feeds the signal to both the forward and backward amplifiers consisting of HBTs, Q_2 and Q_3, and NMOS transistors, M_2 and M_3, respectively. The NMOS devices are biased in the triode region to provide a voltage controlled degeneration resistance for the common emitter HBTs. Two separate current mirrors are provided to bias the gate of M_2 and M_3 independently from an off-chip current source for testing. The proposed approach requires long transmission lines to distribute the forward and backward amplifiers but reduces parasitic loading from the active devices by distributing these amplifiers. Each transmission line is implemented as a shielded microstrip to prevent interstage coupling and is 200 μm long. The characteristic impedance of the transmission line is 45 Ω for improved input

and output return losses. As shown in Fig. 5.6, only one of the feedback amplifiers operates at a time which obviates the need for a switch between the LNA and the PA. The green line in Fig. 5.6 shows the paths which are active in either forward (LNA) or backward (PA) amplification mode.

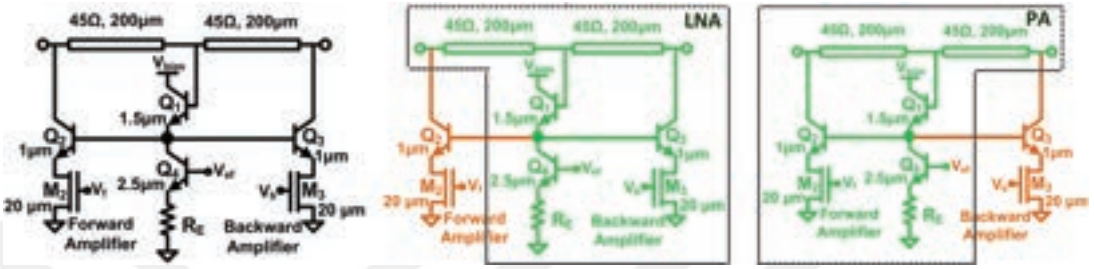

Figure 5.6: The paths which are active in either forward (LNA) or backward (PA) amplification mode.

The small-signal model is illustrated in Fig. 5.7 (a). The local feedback at each stage injects current into the traveling wave at the input of the stage. The forward amplifier, A_F, is activated to amplify the forward traveling wave ($S_{21} > 1$). In this case the backward amplifier is nulled ($A_B = 0$). The backward amplifier, A_B is activated to amplify the backward traveling wave ($S_{12} > 1$) and the forward amplifier is nulled ($A_F = 0$).

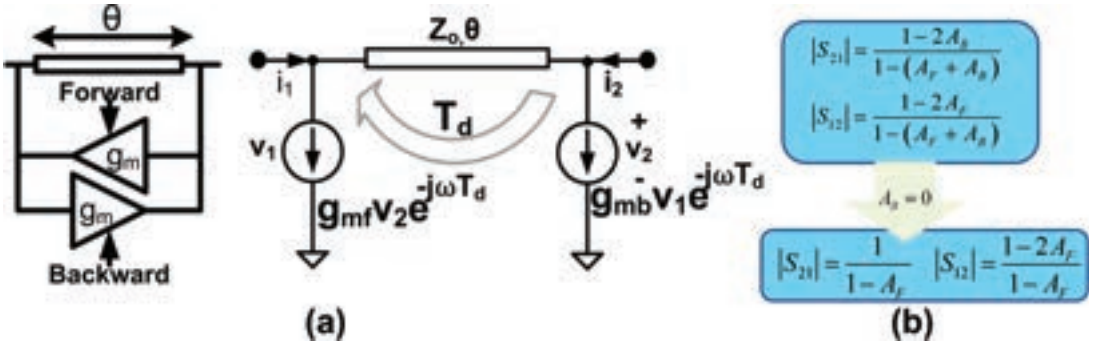

Figure 5.7: (a) Small-signal model for a single bidirectional amplifier stage and (b) the forward and backward S-parameters expressed in terms of the feedback amplifier gains.

The frequency response of this amplifier depends on the relative phase through the transmission line, θ, and the time delay through the feedback circuit, T_d. Constructive interference of the forward traveling wave and destructive interference of the

backward traveling wave occurs when $\theta + T_d = \pi$ and $\theta + T_d = 0$. This condition is satisfied at the center frequency of the amplifier defined by $f_o = 1/4T_d$. For a center frequency of 92 GHz, the feedback delay amounts to around 2.7 ps of delay. The feedback voltage gain is determined by the product of the transconductance and the transmission line impedance. The forward feedback voltage gain is defined as $A_F = 0.5 g_{mf} Z_o$ and the backward feedback gain is $A_B = 0.5 g_{mb} Z_o$, where g_{mf} and g_{mb} are shown in Fig. 5.7 (b). At f_o, the forward and backward S-parameters are expressed in terms of the feedback amplifier gains as shown in Fig. 5.7 (b).

Spectre simulations of the circuit are shown in Fig. 5.8 (a) for forward amplification. The peak gain is 22 dB at 94 GHz. The isolation is 28 dB at 94 GHz. The input return loss is better than 9 dB from 60 to 110 GHz and the output return loss is better than 13 dB over the same frequency range. Simulation of the backward amplification produces symmetric results with similar performance since the circuit is symmetrical. The circuit is stable as shown in Fig. 5.8 (b).

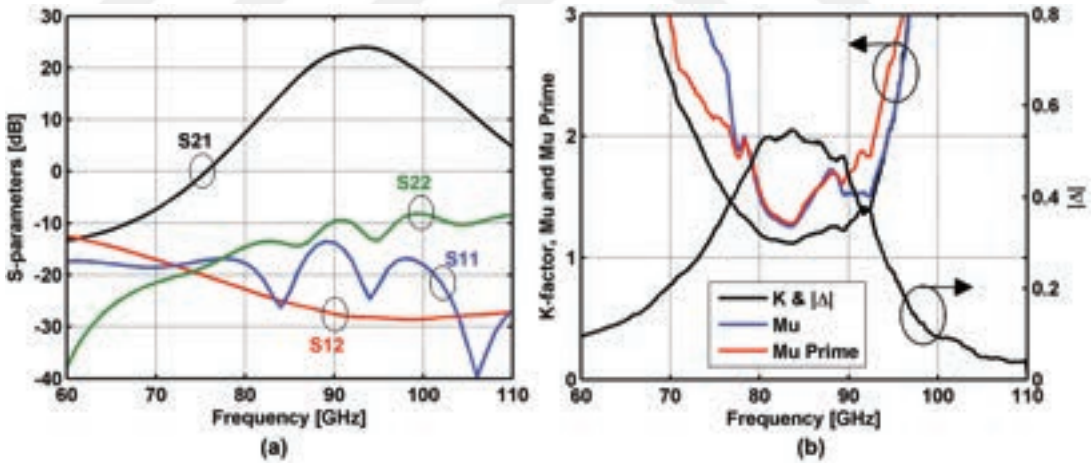

Figure 5.8: (a) Spectre simulations of the S-parameters and (b) stability in the forward and backward amplification mode.

The time settling between the LNA and PA operation limits minimum range in radar systems. The time settling of the bidirectional amplifier is dependent on the bias resistors connected to the gates of the control transistors, M_2 and M_3, which are shown in Fig. 5.5. The rise and fall times are simulated to be between 50 ps and 100 ps as shown in Fig. 5.9 (a).

An additional feature of the implemented circuit is that the passband of the frequency response is tuned with the bias voltage of the NMOS emitter degeneration. By increasing the bias current, $I_{bias,f}$, the gate-source voltage of the diode connected reference NMOS increases and reduces the channel resistance of the NMOS device. The reduced channel resistance increases the feedback voltage gain of each stage and the forward gain increases to 20 dB. However, the reduced emitter degeneration introduces more delay through the feedback path and the center frequency of the amplifier moves to a lower frequency. The tunable frequency response is plotted in Fig. 5.9 (b). The arrow indicates a linear increase in the bias current from the nominal bias, $I_{bias,f}$ = 1.68mA to $I_{bias,f}$ = 7.39mA. Increasing the bias current shifts the center frequency down to 77 GHz while the peak gain increases to 20 dB. The increasing bias current is only changing the gate source voltage of the NMOS degeneration and does not significantly change the power consumption of the stage of the circuit. The input return loss is also plotted in Fig. 5.9 (b) under the bias current variation. The input return loss is relatively insensitive to the changes in the bias current and remains better than 13 dB from 40-110 GHz regardless of the location of the peak gain.

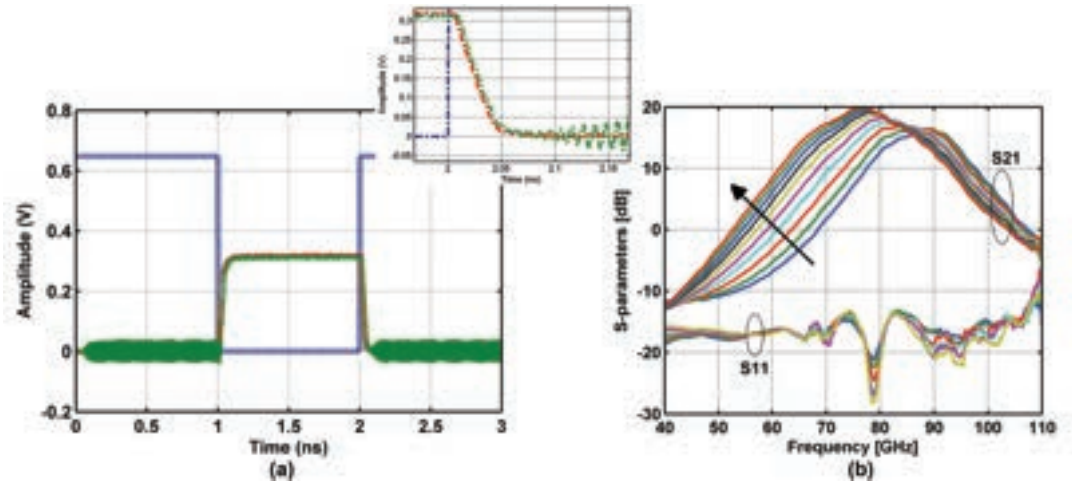

Figure 5.9: (a) Time settling between LNA and PA operation. (b) Measured gain and input return loss of the amplifier at different bias.

Fig. 5.10 shows the process variations for the bidirectional amplifier noise figure, gain and return losses. The noise figure varies by 1 dB while the gain varies by 6 dB in a 3 sigma variation.

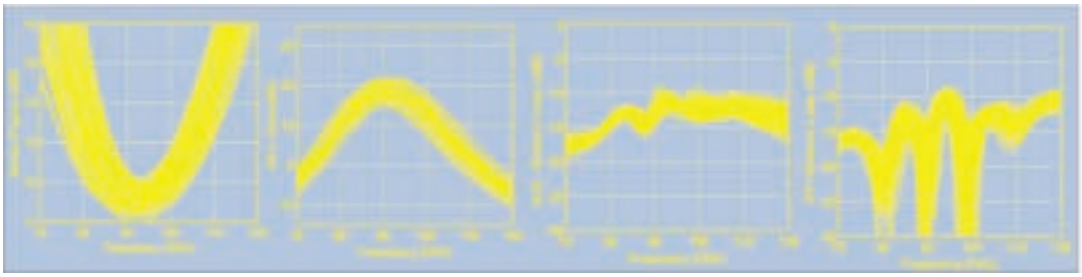

Figure 5.10: Process variations for the bidirectional amplifier noise figure, gain and return losses in a 3 sigma variation.

5.3.2 Measurements

The BCWA is fabricated in a 0.12 μm SiGe BiCMOS process (f_T = 200 GHz) and the chip microphotograph of the circuit is illustrated in Fig. 5.11. The area including the RF and DC pads is 0.52 mm x 0.9 mm (0.47 mm^2).

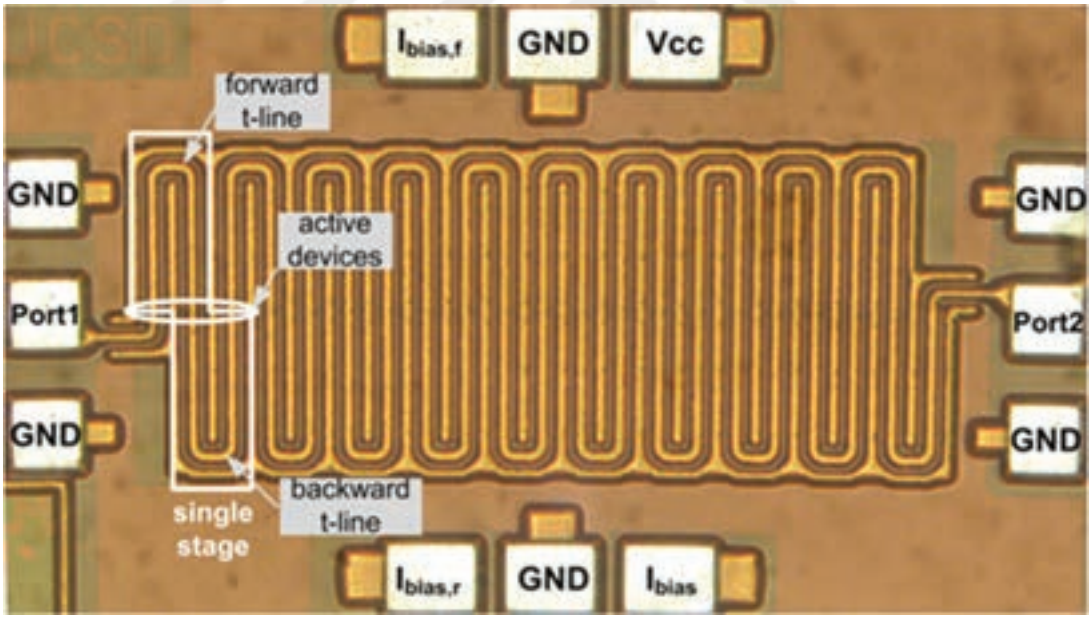

Figure 5.11: The chip microphotograph of the bidirectional amplifier in a 0.13-μm SiGe process.

The nominal bias conditions are V_{cc} = 2 V, V_{bias} =2 V, I_{bias} =2 mA, $I_{bias,f}$ =1.86 mA, and $I_{bias,r}$ = 0 mA for forward amplification. The current consumption through the ten emitter followers is 15.9 mA from the 2 V supply (approximately 1.6 mA per stage) and the current consumption for the ten common emitter stages is 17 mA from

the 2 V supply. The total power consumption under nominal conditions is 65.8 mW. Small signal characteristics are measured with the Cascade ACP110-LW GSG probes and the Agilent E8361A two-port network analyzer with N5260A mm-Wave controller. The measured S-parameters for forward and backward amplification are plotted in Fig. 5.12.

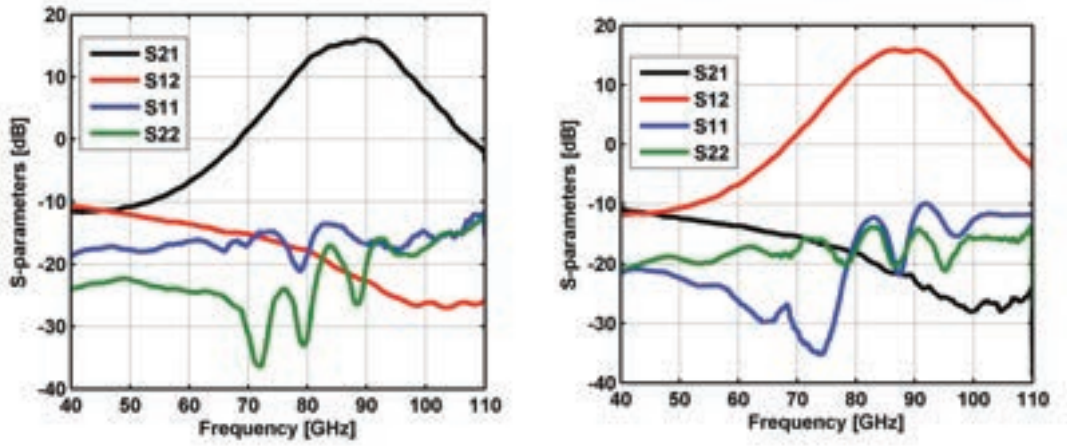

Figure 5.12: Measured forward and backward amplification.

Fig. 5.12 shows the S-parameters measurement. For forward amplification, the measured S_{21} demonstrates peak gain of 16 dB at 90 GHz and a 3 dB bandwidth of the 14.5 GHz at the nominal bias conditions. The isolation S_{12} is 23 dB at 90 GHz. The input return loss S_{11} is better than 13 dB from 40 to 110 GHz and output return loss S_{22} is better than 16 dB over the same range. For backward amplification, the bias conditions are identical except $I_{bias,r}$ = 1.86 mA and $I_{bias,f}$ = 0 mA. S_{12} demonstrates peak gain of 16dB at 90 GHz and the isolation S_{21} is 22 dB at 90 GHz. The input and output loss S_{11} and S_{22} from 40 to 110 GHz remain below 10 dB and 14 dB, respectively. It is demonstrated that the forward and backward response are symmetric. The μ-factor is greater than 2.7 from 40-110 GHz and indicates unconditional stability in either mode of operation.

Fig. 5.13 (a) shows the noise figure of the BCWA in forward amplification mode. The output noise spectrum of the BCWA is down-converted using the Pacific Millimeter Wave W-band mixer to an IF frequency between 4 and 10 GHz. A two-stage IF amplifier provides 24 dB of gain to compensate the conversion loss of the mixer. The noise figure

of the downconversion set-up is initially calibrated with an Agilent E4440 spectrum analyzer. The measured minimum noise figure is 10.9 dB at 90 GHz and 100 GHz. Fig. 5.13 (b) shows that the output-referred P1dB is 1 dBm at 90 GHz.

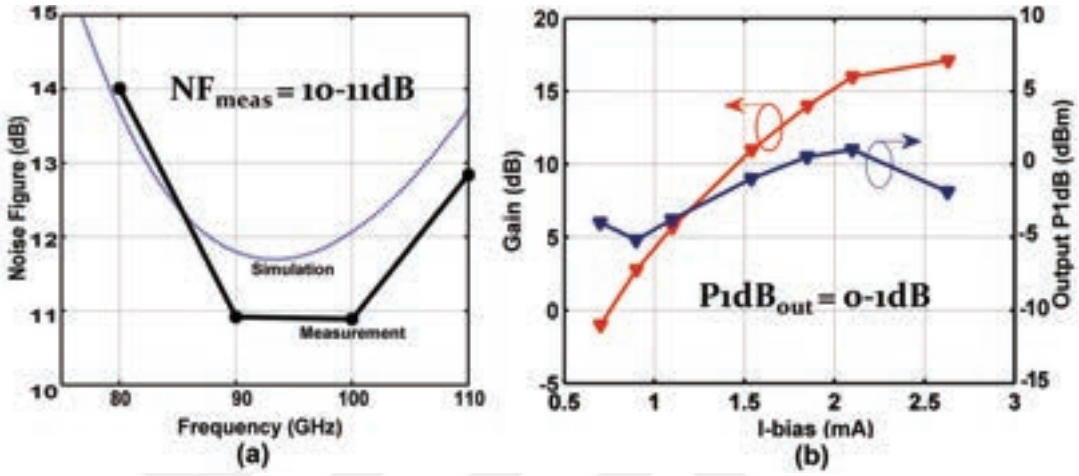

Figure 5.13: (a) Measured noise figure and (b) output-referred P1dB characteristics of the bidirectional amplifier.

5.4 W-Band Bidirectional Phase Shifter and VGA

Phased array systems require amplitude and phase control of the RF signal to control the main beam and sidelobe levels. Phase and amplitude errors between channels contribute to increased sidelobe levels, reduced directivity, pointing error, and symbol errors. Recent phased array receivers have been demonstrated with discrete phase and amplitude control schemes using active vector modulators [13, 21]. Passive phase shifters have been demonstrated at *K*-band in GaAs and offer an alternative to active modulators at *W*-band at the expense of chip area [48]. However, passive phase shifter losses are high in a silicon/silicon-germanium process and substantially increase the receiver noise figure since low receive gain increases sensitivity to the high mixer noise figure. In a transmitter, the saturated output power of the phase shifter is relevant to the power amplifier gain requirements and transmit error-vector magnitude. Previous work at lower frequencies has incorporated loss compensation in the phase shifter to compensate this loss at the expense of linearity and power dissipation [49–51].

Continuous phase and amplitude control is proposed for the calibration of the relative phase and gain errors in a phased array transceiver as shown in Fig. 5.14 (a). This section presents a continuous analog phase shifter/variable gain amplifier that incorporates a constructive wave amplifier along a varactor-loaded transmission line to compensate for the varactor quality factor without introducing a significant phase or gain imbalance. The section discusses the circuit design and measurements of the varactor-loaded constructive wave amplifier operating at *W*-band as a phase shifter or variable gain amplifier one at a time.

Continuous phase shift is possible with a varactor-loaded transmission line. Unfortunately, millimeter-wave hyperabrupt varactors in a 0.12 μm SiGe BiCMOS process and operating at *W*-band have a *Q* of less than six. To compensate for the low varactor *Q* without introducing a significant phase/gain imbalance, a *W*-band phase shifter/VGA is proposed incorporating the bidirectional amplifier in Section 5.3 with a varactor loaded transmission line as illustrated in Fig. 5.14 (b).

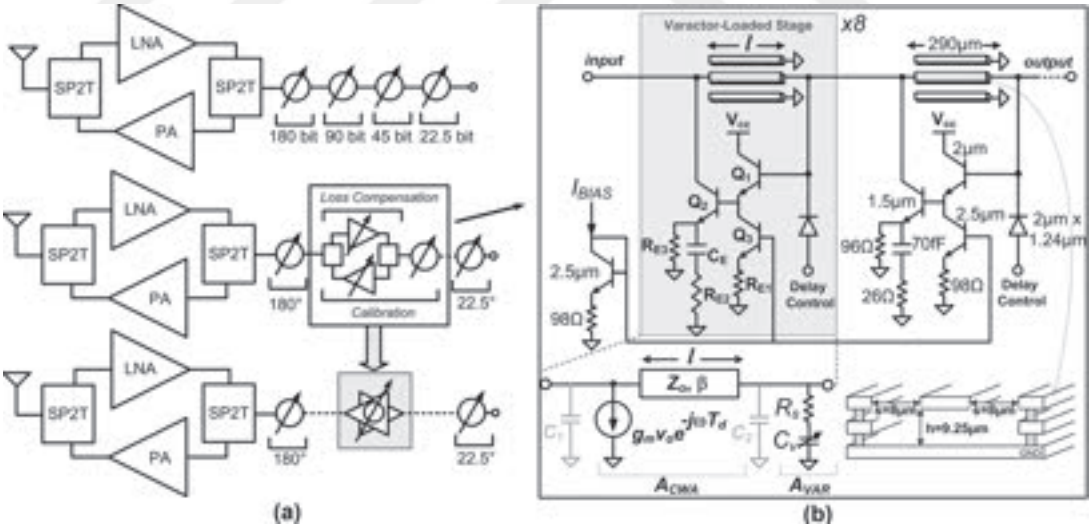

Figure 5.14: (a) Calibration of the relative phase and gain errors with continuous phase and amplitude control. (b) Phase shifter/VGA circuit schematic, small signal model and cross section geometry of the coplanar microstrip line.

5.4.1 Circuit Design

The proposed varactor-loaded constructive wave phase shifter/VGA is shown in Fig. 5.14 and consists of the constructive wave amplifier loaded with a varactor. The constructive wave amplifier uses a transmission line and an active shunt feedback circuit which feeds current back to the input of the quarter-wave transmission line to introduce positive feedback. As described in [47], the chain matrix for the amplifier is

$$[A_{CWA}] = \begin{bmatrix} \cos(\beta l) & jZ_o \sin(\beta l) \\ \frac{j}{Z_o}\sin(\beta l) + g_m e^{-j\omega T_d} & \cos(\beta l) \end{bmatrix} \tag{5.1}$$

where β and l are the phase constant and length of the transmission line, Z_o is the transmission line impedance, g_m is the feedback transconductance, and T_d is the delay through the feedback circuit. In [47], low feedback voltage gain, $A_v = \frac{g_m}{2Z_o} \approx \frac{1}{4}$, is demonstrated to result in a forward gain, $|S_{21}| \approx \frac{1}{1-A_v}$ = 2.7dB, when $\beta l = \omega T_d = \frac{\pi}{2}$. This gain is applied to compensate insertion loss of the varactor.

A hyperabrupt junction varactor provides capacitance tuning as a function of the reverse bias voltage applied to the diode. The chain matrix A_{VAR} for the shunt varactor diode is

$$[A_{VAR}] = \begin{bmatrix} 1 & 0 \\ j\omega C_v \parallel R_S^{-1} & 1 \end{bmatrix} \tag{5.2}$$

where C_v is the varactor capacitance and R_s is the series resistance that determines the quality factor, *Q*, of the varactor. Phase shift is induced by the varactor capacitance. The *C-V* characteristic simulated in Fig. 5.15 for an anode measuring 2 μm x 1.24 μm demonstrates a capacitance tuning range from 12 to 30 fF. The cathode of each varactor is biased at 2 V and the delay control voltage is connected to the anode of the varactors. While hyperabrupt diodes have high *Q* at a low frequency (*Q* > 100 @ 2 GHz), the *Q* is significantly lower at *W*-band. The *Q* is generally less than 6 at 94 GHz and the low quality factor induces high insertion loss in a varactor-loaded transmission line.

The response of the cascaded constructive wave amplifier and varactor is determined from chain matrix multiplication, $[A_{SS}] = [A_{CWA}]\,[A_{VAR}]$. Translating the chain matrix to *S*-parameters, the phase shift through a single stage is

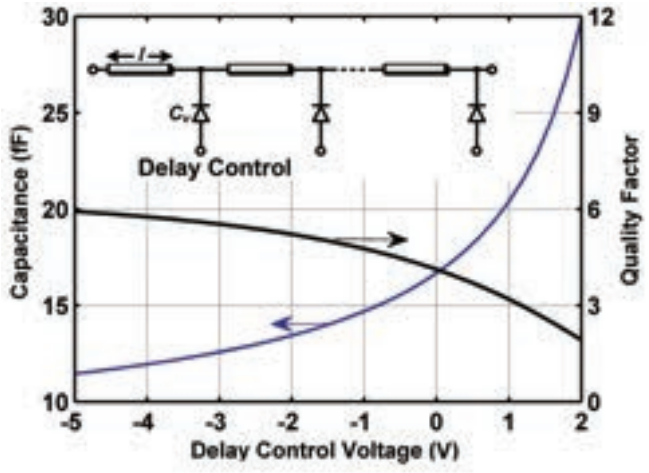

Figure 5.15: Simulation of the capacitance tuning at 94 GHz for SiGe hyperabrupt junction varactors (2 μm x 1.24 μm, Vc = 2V).

$$\tan\theta = \frac{-\sin(\beta l) - \omega\tau\cos(\beta l) + A_v \sin(\omega T_d)}{\cos(\beta l) - \omega\tau\sin(\beta l) + A_v \cos(\omega T_d)} \tag{5.3}$$

where $\tau = \frac{1}{2} Z_o C_v$. The equation (5.3) estimates the interdependence of gain and phase. The phase through the transmission line segment, l, varies with the capacitance. While the phase changes with the capacitance, the gain also influences the phase. When $\beta l = \omega T_d = \frac{\pi}{2}$, the phase shift is approximately $\theta = \arctan\left((1 - A_v) / (\omega\tau)\right)$. Larger feedback gain, A_v increases the phase shift.

The circuit is implemented in a 0.13-μm SiGe BiCMOS process (f_T / f_{max} = 200/260 GHz). Fig. 5.14 (b) illustrates the implementation of the phase shifter circuit which consists of a total of eight identical varactor-loaded, loss compensated stages. The feedback network consists of emitter follower and common emitter stages with emitter lengths of 2.0 μm and 1.5 μm, respectively, and biased at 2.5 mA per stage. A zero is introduced into the emitter degeneration network to improve the gain at high-frequency. The cross section of the shielded CPW is also illustrated in Fig. 5.14 (b). The coplanar waveguide (CPW) is implemented in a thick aluminum layer. The signal line is 8 μm thick and separated from the side shields by 8 μm. Each section has a length of 290 μm and the simulated phase velocity along the loaded transmission line is v_p = 1.2×10^8 $\frac{\text{m}}{\text{sec}}$.

5.4.2 Measurements

The chip microphotograph of the circuit is illustrated in Fig. 5.16. The area including the RF and DC pads is 0.7 mm x 0.3 mm (0.21 mm^2).

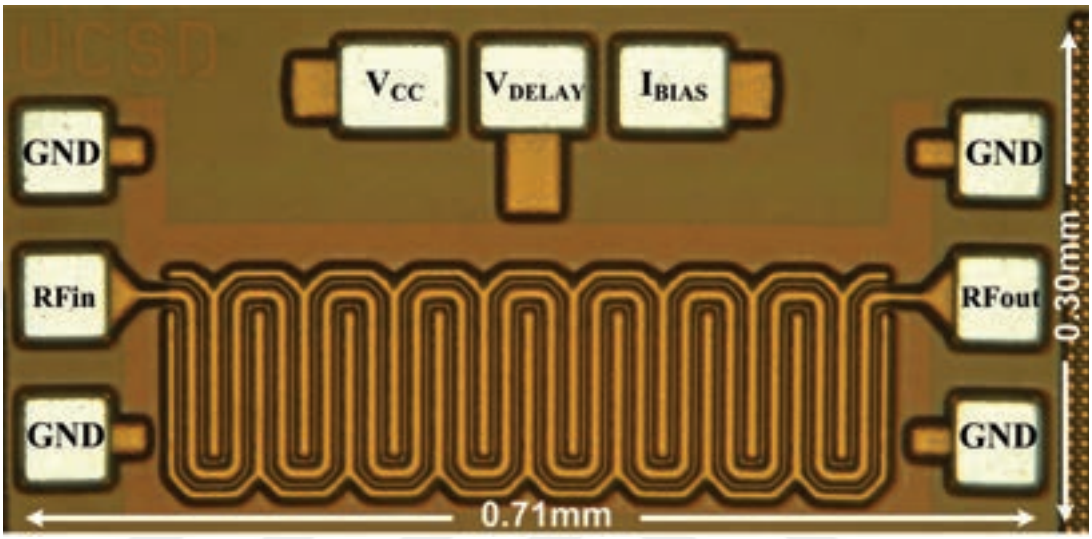

Figure 5.16: The chip microphotograph of the bidirectional phase shifter/VGA in a 0.13-μm SiGe process.

The die is tested using Cascade 110-GHz GSG probes and the Agilent E8361A 67-GHz PNA with extenders up to 110 GHz. First, the circuit is tested under passive conditions. When the bias current of the feedback amplifier is zero, the circuit behaves as a passive varactor-loaded transmission line. As the delay voltage varies from -5 V to 0 V, the phase and insertion loss are plotted in Fig. 5.17 (a) and are compared with Spectre simulations. The phase is measured as a relative value with respect to the different bias conditions. At 90 GHz, the phase tuning range is 65° and, consequently, each stage provides a maximum of 8° of the phase shift. Additionally, the phase shifter response is wideband illustrating the linear phase from 70 to 110 GHz. However, the insertion loss of the phase shifter varies by 7 dB - the minimum insertion loss is 7 dB at 90 GHz (0.9 dB per stage) and increases to more than 14 dB. The input and output return losses (not shown) are better than 13 dB for all phase states.

Next, active feedback is introduced to compensate the insertion loss. The gain is plotted in Fig. 5.17 (b) for a control voltage of -5 V and also compared with Spectre simulations. As the bias current is varied from 1.5 to 2.5 mA, the gain varies from 9 to

16 dB. The phase imbalance is minimized at 98 GHz. The input and output return losses again remain better than 12 dB.

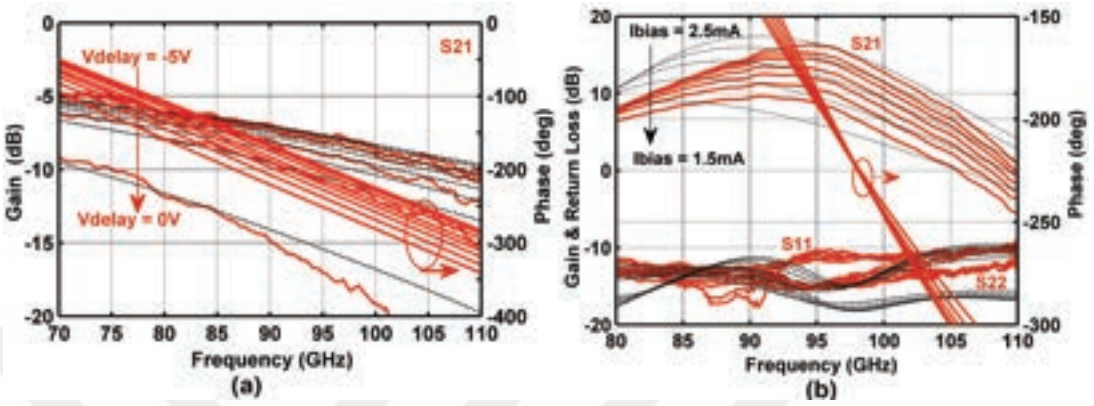

Figure 5.17: (a) Simulated (dashed) and measured (solid) gain and phase of the passive phase shifter with delay voltage ($I_{bias} = 0$ mA, $V_{cc} = 0$ V). (b) Simulated (dashed) and measured (solid) gain and phase of the VGA with bias current ($V_{delay} = -5$ V).

Since the measured gain and phase shift at 90 GHz depends on both feedback bias current and control voltage, the phase and gain contours are plotted in Fig. 5.18 (a) and Fig. 5.18 (b), respectively. Loci of constant gain of 7 dB and 45° phase shift is shown on each contour, respectively.

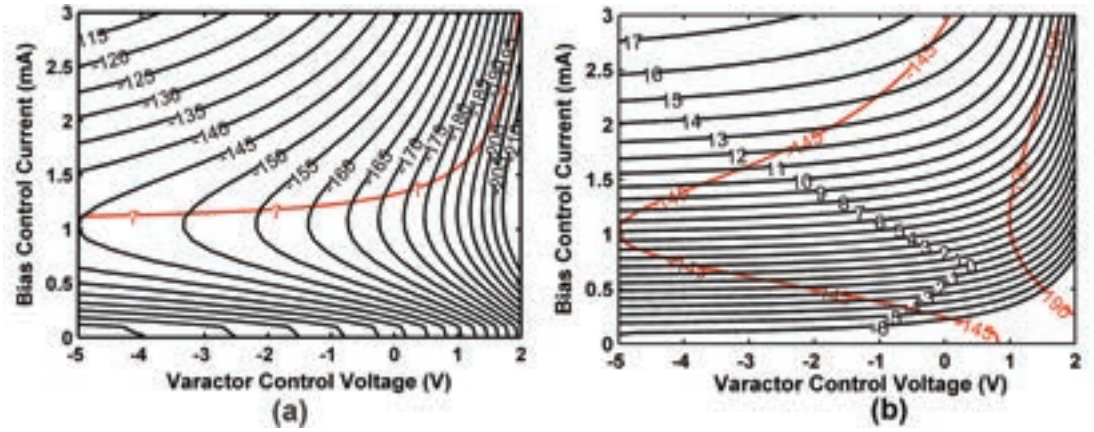

Figure 5.18: Measured (a) phase and (b) gain contours at 90 GHz.

Ideally, the gain depends only on the bias current and the phase shift depends only on the delay voltage. Measured constant gain and phase loci are plotted on each contour to illustrate the interdependence of gain and phase. The circuit provides gain

from -6.7 dB to 16.7 dB and a relative phase control of more than $45°$. At $I_{bias} = 1$ mA, the phase shift range is lower than at higher currents. When the phase shifter is operated at its maximum gain of 16.7 dB, the total power consumption is 20 mA from a 1.8 V supply - a power consumption of 4.5 mW per stage.

At a bias of 1.5-2.5 mA per stage, the measured noise figure of the VGA is 10-10.5 dB at 90 GHz for a reverse bias of -1 V. Finally, the output-referred one-dB compression point is separately plotted as a function of the delay control voltage and the feedback bias current in Fig.5.19. For a bias of 2 mA, the measured P_{1dB} is between -8 dBm and -9 dBm as the varactor control voltage is tuned between -5 V and 0 V. For control voltages higher than 1 V, the varactor linearity degrades. The simulations predict a P_{1dB} that is roughly 3 dB lower. The output-referred P_{1dB} increases with the bias current level ($V_{delay} = -1$) and indicates that the maximum P_{1dB} is -7.5 dBm.

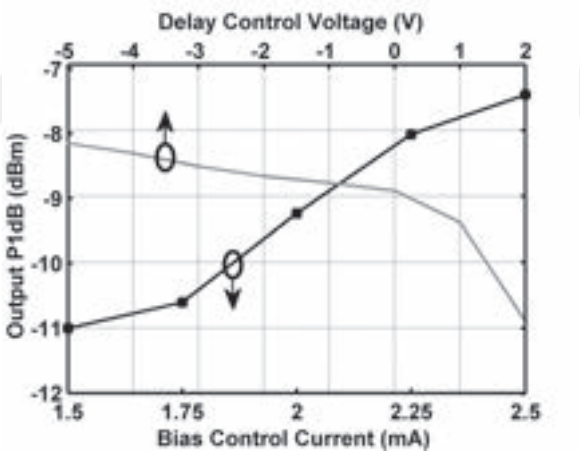

Figure 5.19: Measured output-referred P_{1dB} compression point.

5.5 Passive Switched-Beam Transceivers

A *N*x*N* Butler matrix is a switched-beam that synthesizes *N* simultaneous beams from *N* antennas using only passive components and does not consume power and offers high linearity [52]. Since the Butler matrix has *N* paths, *N* amplifiers are required at the input and output, increasing the power consumption. A 8x8 butler matrix is shown in Fig. 5.20 (a) and is composed of hybrid couplers and fixed phase shifters. Conceptual

block diagram of the Butler matrix used in a switched-beam system is illustrated in Fig. 5.20 (b). Since Butler matrix or other switched beam matrixes are composed of hybrid couplers and fixed phase shifters, they introduce loss and degrade the noise figure. Therefore, a TX/RX is introduced in the front-end and if desired in the back-end of the Butler matrix to compensate the losses.

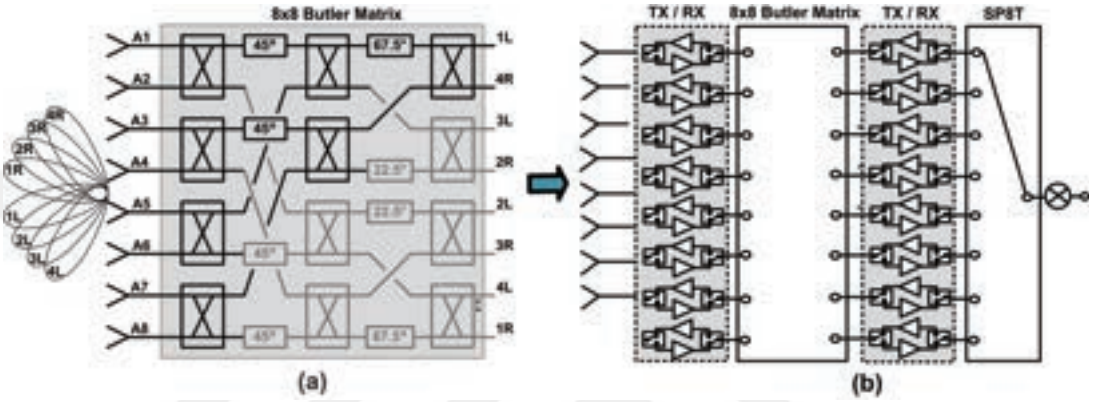

Figure 5.20: (a) Circuit diagram of an 8x8 Butler matrix and (b) the conceptual block diagram of the Butler matrix used in a switched-beam system

To compensate the losses due to the passive structures, Fig. 5.21 (a) proposes a bidirectional amplifier that can replace the switch, PA and LNA at the same time in case of a transceiver.

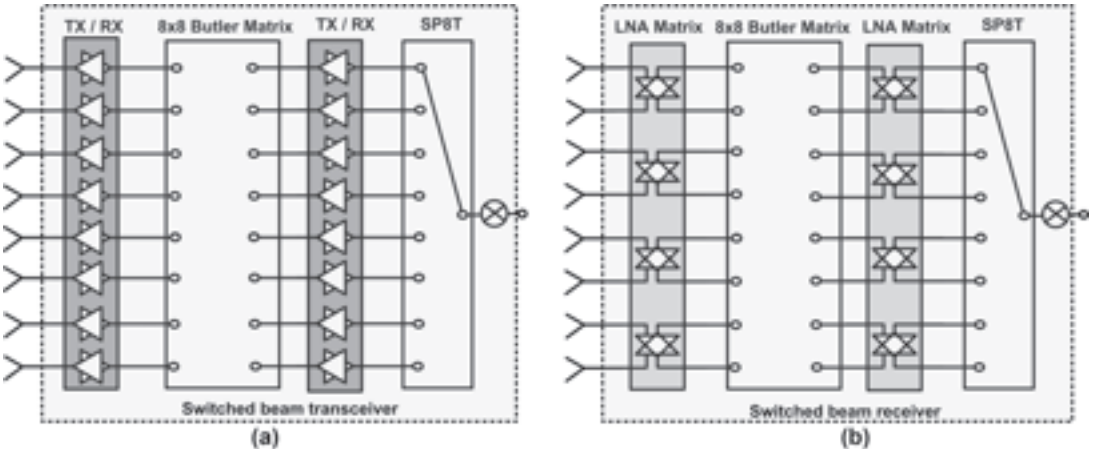

Figure 5.21: (a) Proposing a bidirectional amplifier that can replace the switch, PA and LNA at the same time in case of a transceiver. (b) Proposing a circuit structure that can replace two LNAs at the same time in case of a receiver.

Fig. 5.21 (b) proposes a circuit structure that can replace two LNAs at the same time in case of a receiver. The area, cost and power consumption of the system can be reduced significantly with increasing number of paths in switched beam structure.

5.6 Dual-Channel Distributed Amplifier

The dual-channel distributed amplifier proposed in this chapter replaces two conventional LNAs at the same time at the front and back of the switched beam system to minimize the power consumption, to minimize the noise figure and compensate the loss as shown in Fig. 5.22. Distributed amplifiers offer wideband frequency response and higher linearity than a common source amplifier in a given integrated circuit process at the expense of higher power and area requirements. However, sharing a single DA for two receive channels amortizes this penalty. K-band LNAs using 0.18-μm CMOS and 0.13-μm CMOS technologies have previously reported 5-6 dB noise figure while consuming 54 mW and 17 mW, respectively [53, 54]. More recently, a 3-stage LNA for a 24 GHz phased array consumes 19 mW power providing 13 dB gain and 6 dB noise figure [55].

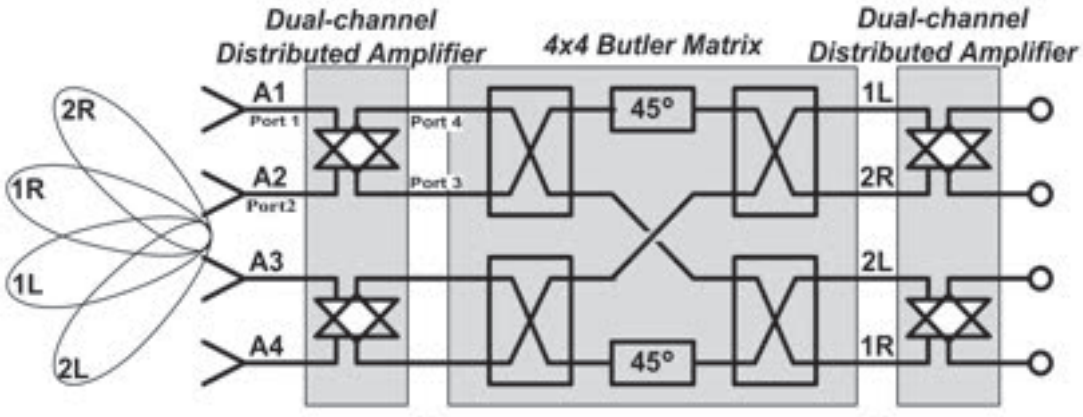

Figure 5.22: Application of a dual-channel distributed amplifier in a switched beam receiver.

Distributed amplifiers can isolate and amplify signals between respective input and output ports. Dual-channel amplifiers have been suggested for bidirectional applications [56, 57] and active circulators [58, 59]. These prior demonstrations show how

the circuit parameters relate to the response from one port to each of the distributed circuits output ports. This work presents a dual-channel distributed amplifier with low noise figure and high linearity. Proper choice for the number of stages and cutoff frequency of the distributed circuit realizes isolation between amplifier channels. Analysis of the distributed circuit describes the role of reverse gain in minimum noise figure and intermodulation distortion. The dual-channel distributed amplifier design is discussed in terms of forward and reverse gain, noise figure, and linearity in Section 5.6.1, 5.6.2, 5.6.3, 5.6.4, respectively. This discussion will show how the isolation of the dual channel response is achieved at multiple bands or over a desired bandwidth while achieving high linearity and low noise figure. Previous linearity analysis for distributed amplifiers has not considered multiple signal paths. This work provides an analysis of intermodulation distortion resulting from signals propagating in the same and opposite directions through the distributed amplifier. Section 5.6.5 discusses the circuit design for the distributed amplifier. Section 5.6.6 presents the performance of the dual-channel amplifier and compares this work against previous designs.

The schematic of an *N*-stage distributed amplifier is shown in Fig. 5.23. A gate artificial transmission line is formed with a *T*-network of interstage inductors, L_G/2, and shunt capacitance, C_G, contributed by the common source transistor, M_{ai}. The characteristic impedance of the transmission line is $Z_G = \sqrt{L_G/C_G}$.

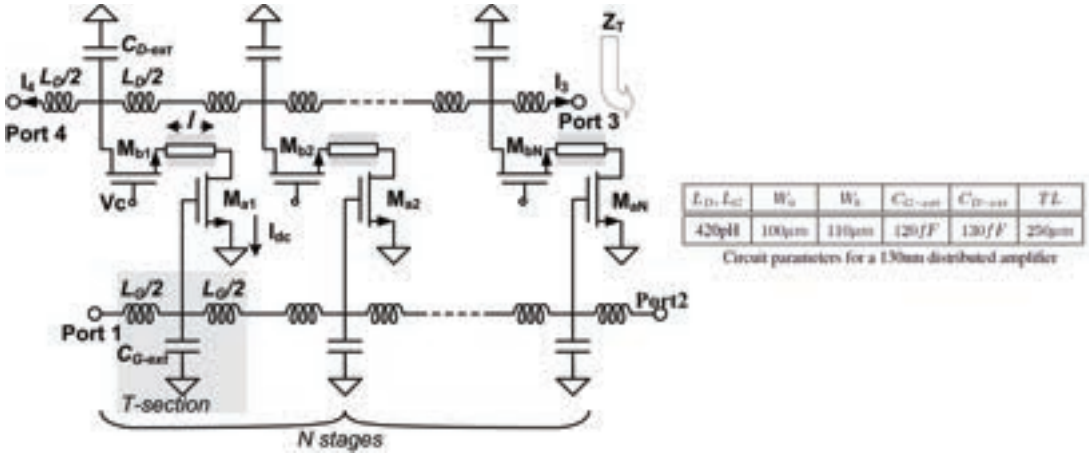

Figure 5.23: Circuit schematic of the *N*-stage distributed amplifier with cascode stages and interstage inductance.

Similarly, the gate-drain and drain-body capacitance, C_D, of the cascode tran-

sistor, M_{bi}, is absorbed into the drain artificial transmission line with impedance $Z_D = \sqrt{L_D/C_D}$. Here, both Z_G and Z_D are matched to an external impedance of $Z_T = 50$ Ω. The lumped elements of the *T*-network define a cut-off frequency, $f_c = 1/\pi\sqrt{L_G C_G}$ [60].

5.6.1 Forward Gain

Two signal paths are available in a single distributed amplifier, as shown in Fig. 5.24. Illustrated in Fig. 5.24 (a), signals incident at ports one and two are amplified as they propagate respectively towards ports two and one. The maximum forward power gain, S_{31} and S_{42}, is defined for frequencies below the cut-off frequency of the transmission line ($f \leq f_c$) and is equal to

$$G_F = \frac{N^2 g_{ma}^2 Z_D Z_G}{4} \approx \frac{(N I_d)^2 Z_T^2}{V_{ov}^2} \tag{5.4}$$

where g_{ma} is the transconductance of each transistor, M_{ai}, and N is the number of stages. The final approximation holds assuming a short-channel transistor is biased in saturation with overdrive voltage, $V_{ov} = V_{gs} - V_t$, since the transconductance is $g_{ma} \approx 2I_d/V_{ov}$ with a small overdrive voltage and drain current, I_d. For a fixed power consumption, the drain current is constrained and the gain increases with lower overdrive voltage and larger W/L. Since gate-source capacitance is related to $C_{gs} \propto WL$, the cut-off frequency can only be increased at the expense of gain.

5.6.2 Reverse Gain

Illustrated in Fig. 5.24 (b), when a DA is driven from one of the input ports (*e.g.* port one in Fig. 5.24), half of the current from M_b propagates in the forward direction (*e.g.* towards port three) and contributes to the forward power gain while the other half propagates in the reverse direction (*e.g.* towards port four) and contributes to reverse gain, S_{32} and S_{41}. Reverse gain is distinguished from reverse isolation, S_{13} and S_{24}. To implement a dual-channel DA, the reverse gain should be zero at the bands of interest to isolate the amplified signals. When a signal is incident at port one, V_1^+, the total current at port four is

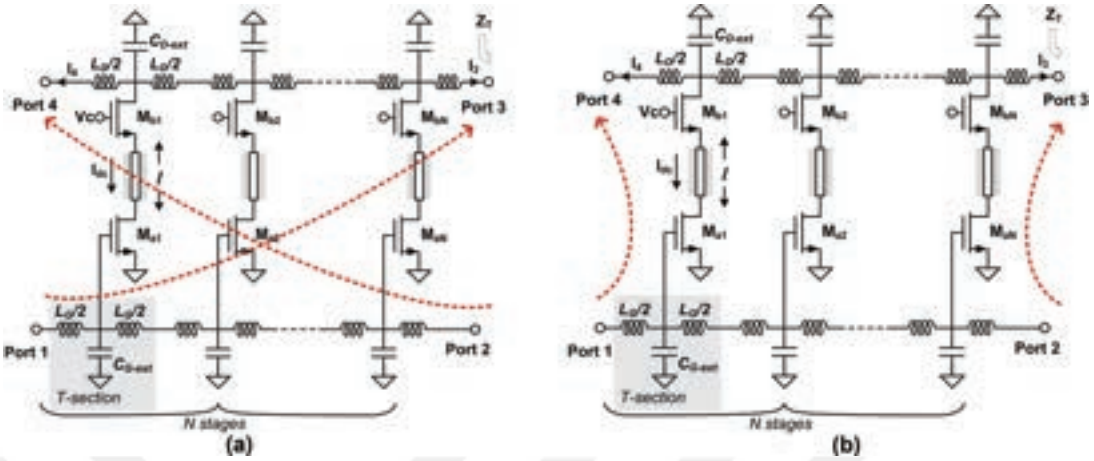

Figure 5.24: 4-Channel DA operation - (a) maximization of the forward gain and (b) minimization of the reverse gain.

$$I_4 = \frac{1}{2} V_1^+ g_{ma} \sum_{n=1}^{N} e^{-j\left(\frac{2n-1}{2}\right)(\theta_G + \theta_D)} \tag{5.5}$$

where $\theta_G = \omega\sqrt{L_G C_G}$ and $\theta_D = \omega\sqrt{L_D C_D}$ are the *T*-section phases of the gate and drain line. Currents sum in phase in the forward direction but cancel in the reverse direction at certain frequencies. If $\theta = \theta_G = \theta_D$, the reverse gain, $S_{41} = S_{32}$, for a lossless uniform DA is defined in [61] as

$$G_R = G_F \left(\frac{\sin(N\theta)}{N \sin\theta} \right)^2 . \tag{5.6}$$

Therefore, the forward and reverse gain expressions differ by a distribution factor which is equal to

$$DF = \left(\frac{\sin(N\theta)}{N \sin\theta} \right)^2 . \tag{5.7}$$

A dual-channel amplifier minimizes reverse gain at the band of interest to isolate the forward and backward propagating signals. When $N\theta = k\pi$ is satisfied, $DF = 0$ and the null index, *k,* provides isolation at $k \leq N-1$ bands. The choice of cut-off frequency places nulls of G_R at $\theta = \pi/N$ through $\pi(N-1)/N$. Therefore, the bands of interest

relate to the cut-off frequency as

$$f_{RF} = k\pi f_c/2N. \tag{5.8}$$

However, not all *k* provide forward gain since the cut-off frequency must be higher than the RF carrier frequency, $k \leq frac2N\pi$. For instance, a null at 24 GHz exists for k =3 if $N = 7$ and $f_c = 35$ GHz. Consequently, the dual-channel amplifier operation demands a higher cut-off frequency than the frequency of operation, $f_c > f_{RF}$.

Non-uniform transconductance and reverse gain

Non-uniform arrays provide additional degrees of freedom to tailor the distribution factor in a manner analogous to the array factor of an *N*-element linear antenna array. Dolph proposed a method to design arrays to a desired sidelobe level or half-power beamwidth by approximation of the array pattern with a Chebyshev polynomial [62]. By assigning Chebyshev polynomials to antenna weights, interference is rejected at sidelobe nulls. Similarly, proper polynomials are assigned to the transconductance of each stage to control the reverse gain response. From (5.5), the generalized distribution factor is

$$DF = \sum_{n=1}^{N} g_n e^{-j(2n-1)\theta} \tag{5.9}$$

where $g_n = \frac{g_{m,n}}{g_{ma}}$ is a normalized transconductance. This equation reduces to (5.7) when $g_n = 1$ for all stages. A wideband reverse gain null for S_{41} is obtained if binomial coefficients are applied to the transconductance values. A binomial weighting scheme is compared to a uniform scheme in Fig. 5.25 (a). The uniform scheme provides a relatively narrowband reverse gain response while binomial distribution produces wideband null in the reverse gain. Unfortunately, non-uniform weighting also reduces the maximum gain and increases the noise figure. As shown in the figure, the binomial coefficients result in an 8 dB gain reduction. When narrowband rejection is required, uniform weighting provides the best choice for the dual-channel amplifier.

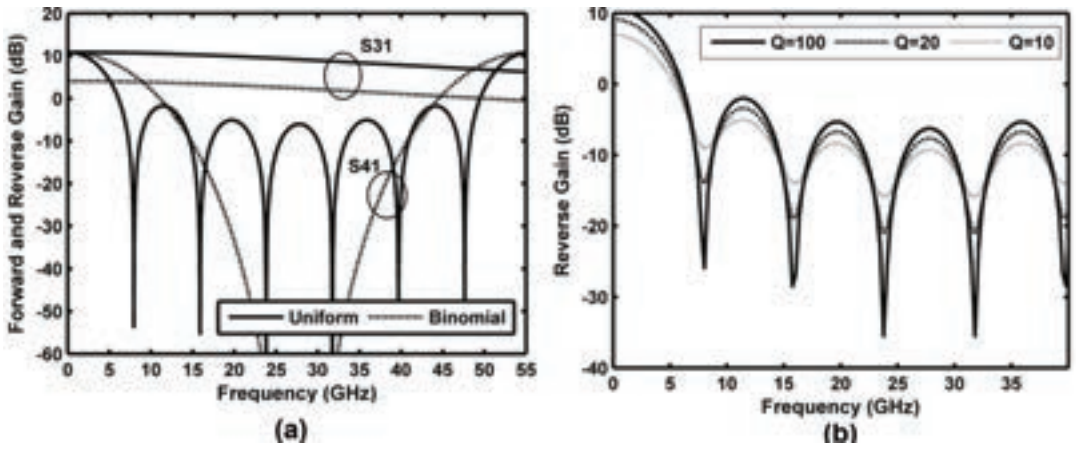

Figure 5.25: (a) Reverse gain for a uniform and non-uniform transconductance distributed amplifier. (b) The effect of inductor quality factors on the reverse gain nulls.

Effect of Quality Factor on Reverse Gain

Transmission lines losses impact the reverse gain. Considering the impact of attenuation, the distribution factor from (5.7) is modified to

$$DF = \left(\frac{\sinh\left(N\gamma l\right)}{N\sinh\left(\gamma l\right)} \right)^2 \tag{5.10}$$

where $\gamma = \alpha + j\beta$ is the complex propagation constant. If the transmission line quality factor is defined as $Q = \frac{\beta}{2\alpha}$, the degradation in the null depth is determined as a function of Q. The effect of attenuation on the depth of the nulls is shown in Fig. 5.25 (b). A Q of ten results in a maximum isolation of 15 dB. Ultimately, the Q determines whether the reverse gain is suppressed sufficiently to provide isolation between the amplifiers.

5.6.3 Noise Figure

Prior analysis of noise figure in distributed amplifier considers the noise contributions from impedance terminations and active devices [63]. The noise factor of a distributed amplifier is summarized as

$$F_{DA} = 1 + \frac{1}{4G_F} + DF + F_{mos} \tag{5.11}$$

where G_F and DF are described in (5.4) and (5.7). The first, second, and third terms represent respectively the contributions of thermal noise from the source impedance,

the drain-line termination, and the gate-line termination. The drain termination noise contribution is reduced by increasing the forward gain. The gate termination noise is shielded by the reverse gain of the DA. The distribution factor in (5.7) indicates the gate termination noise is suppressed at the same frequencies that the DA provides signal isolation. Hence, the gate-line termination is negligible when the DA is operated at $N\theta = k\pi$.

Therefore, the noise figure of the DA is reduced to $F_{DA} \approx 1 + F_{mos}$ in bands located at the reverse gain nulls. In [63], the noise figure of the MOS device incorporating the contribution associated with the common-source transistor channel noise and correlated gate-induced noise is

$$F_{mos} = \frac{\gamma}{N g_m Z_T}\left(1 + \omega\left(2N\kappa_c\tau_{gs} + \frac{\left(2N^2+1\right)}{3}\frac{|\kappa_c|^2\omega\tau_{gs}^2}{|c|^2}\right)\right) \tag{5.12}$$

where γ is the excess channel noise of the FET, τ_{gs} is the time constant associated with the gate capacitance, c is the correlation coefficient between gate and drain current noise, and κ_c is a technology dependent noise factor. Assuming the gate time constant is dominated by the impedance of the line, $\tau_{gs} = \left(\frac{Z_T}{2} + \frac{r_{gate}}{3}\right) C_{gs}$, the time constant is inversely proportional to the cut-off frequency of the line, i.e. $\tau_{gs} = \frac{1}{2\pi f_c}$.

Increasing N decreases the first term of F_{mos} but increases the second term in (5.12). Therefore, an optimum N minimizes the noise figure over a specific band due to the MOS devices and is equal to

$$N_{opt} = \frac{|c|}{2\,|\kappa_c|\,\omega_{RF}}\sqrt{\frac{3}{\tau_{gs}^2}} \approx \frac{\sqrt{3}\,|c|}{2\,|\kappa_c|}\frac{\omega_c}{\omega_{RF}}. \tag{5.13}$$

Notably, the optimum number of stages increases as the ratio of $\frac{\omega_c}{\omega_{RF}}$ increases. However, this ratio is determined from (5.8). Substituting this expression into (5.13), the optimum null index can be found as

$$k_{opt} = \frac{\sqrt{3}}{\pi}\frac{|c|}{|\kappa_c|}. \tag{5.14}$$

Since $|c| \,/\, |\kappa_c|$ is approximately 5.5 for 0.13 μm CMOS process [63], the optimum null index to use for a dual-channel distributed amplifier is $k_{opt} = 3$. From (5.13), N_{opt} is about 4.5 times of $\frac{\omega_c}{\omega_{RF}}$. If we use a seven-stage distributed amplifier, the cut-off

frequency of the transmission line must be 35 GHz for the 24 GHz ISM band. Therefore, noise figure constraints impose a similar design criterion on the cut-off frequency to the distribution factor.

5.6.4 Linearity

Wideband LNAs are prone to intermodulation distortion due to the presence of in-band interferers. Assuming distortion is introduced by the transistor, the linearity of the DA is estimated from the distortion introduced by the common-source transistor, e.g. M_a as shown in Fig. 5.26 [64]. The drain current at each stage is modeled as a weakly nonlinear transconductance and can be written as

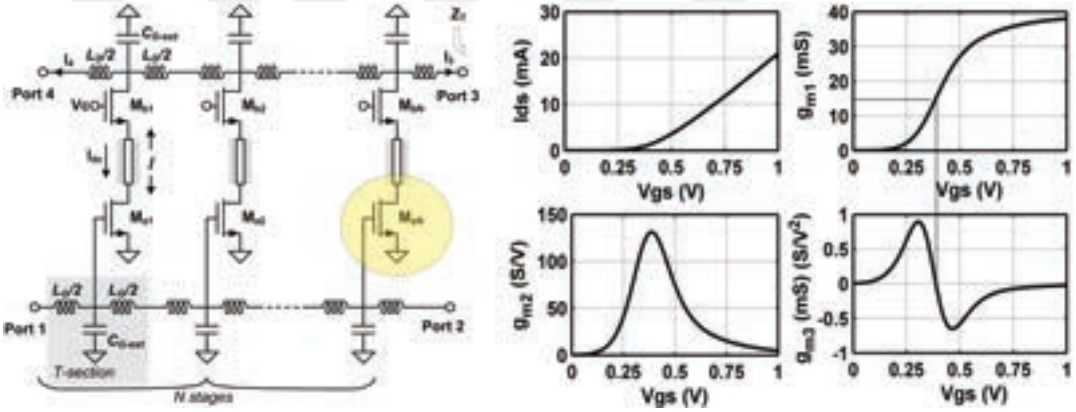

Figure 5.26: Simulated first, second and third-order transconductance versus gate voltage for a 0.13 μm CMOS process ($W = 100\mu m$).

$$I_{d,n} = g_{m,1}V_{gs,n} + \frac{1}{2}g_{m,2}V_{gs,n}^2 + \frac{1}{6}g_{m,3}V_{gs,n}^3 \tag{5.15}$$

where $g_{m,k} = \frac{\partial^k I_d}{\partial V_{gs}^k}$. Third-order intermodulation products (IM3) predominantly result from the last term, i.e. $IM_3 = \frac{3}{4}g_{m,3}V_{gs}^3$. When a FET is biased in weak or moderate inversion, the drain current closely follows square-law behavior. This provides a significant increase in device linearity without requiring high power consumption [65,66]. For a 0.13 μm CMOS process, the transconductance terms in (5.15) are plotted in Fig. 5.26 for a device width of 100 μm. IM3 is minimized when $g_{m,3}$ is zero at approximately 390 mV. This gate voltage biasing allows 14 mS of transconductance (I_d = 2 mA). The low

transconductance prevents high gain from a single stage circuit but the distributed structure realizes higher gain across multiple stages. Biasing each device in weak inversion results in the highest input-intercept point for the distributed amplifier.

The dual-channel distributed amplifier is characterized from intermodulation distortion resulting from co-propagating and cross-propagating signals. Co-propagating signals are incident at the same port while cross-propagating signals are incident at opposite input ports as shown in Fig. 5.27 (a). The following analysis indicates that co-propagating signals result in conventional intermodulation behavior, however, cross-propagating signal result in intermodulation behavior that depends on the distribution factor as shown in Fig. 5.27 (b).

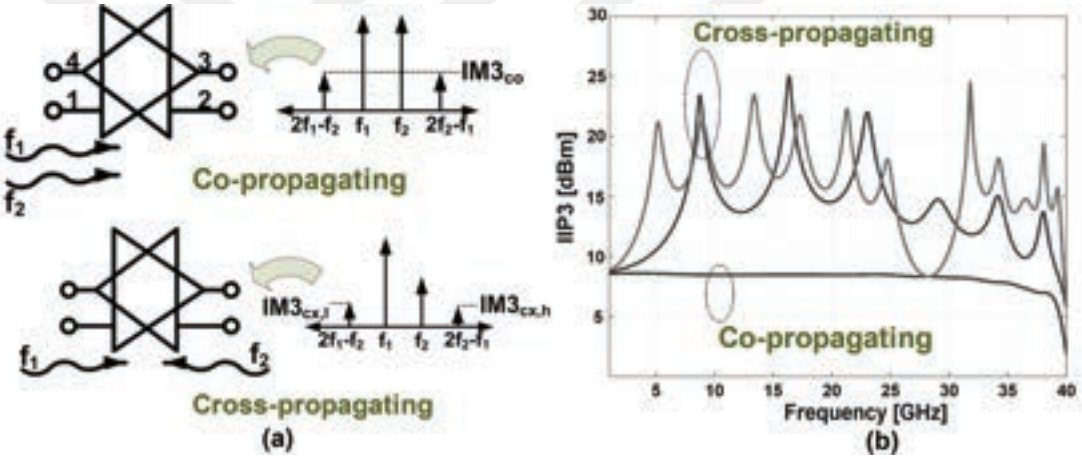

Figure 5.27: (a) Co-propagating and cross-propagating signals (b) Circuit simulation results for the IM3 of co-propagating and cross-propagating signals in a seven stage distributed amplifier (Δf = 10 MHz).

Co-propagating Intermodulation Products

Two signals at frequencies, f_1 and f_2, propagating in the *same* direction along the gate transmission line generate a voltage $V_{gs,n}$ at each transistor gate which can be written as

$$V_{gs,n} = V_o \left(\cos\left(\omega_1 t - n\theta_1\right) + \cos\left(\omega_2 t - n\theta_2\right)\right) \tag{5.16}$$

where θ_1 and θ_2 represent the phases of ω_1 and ω_2 through each distributed stage. IM3 terms are generated at $\omega_l = 2\omega_1 - \omega_2$ and $\omega_h = 2\omega_2 - \omega_1$ due to the nonlinear current in (5.15) and each product at these new frequencies has the same magnitude:

$$IM3_{co} = \frac{3}{4} g_{m,3} N V_o^3. \tag{5.17}$$

Therefore, co-propagating signals at two frequencies below the cut-off frequency result in intermodulation products that are determined by the nonlinear device transconductance and the number of stages. Since the signal power increases linearly in *N*, the overall IIP3 of the distributed circuit is independent of *N*, i.e. $IIP3 = \sqrt{\frac{4}{3}\frac{g_{m,1}}{g_{m,3}}}$.

Cross-propagating Intermodulation Products

For the same signals propagating in *opposite* directions along the gate transmission line, the gate voltage $V_{gs,n}$ at each transistor along the gate transmission line is represented as

$$V_{gs,n} = V_o \left(\cos\left(\omega_1 t - n\theta_1\right) + \cos\left(\omega_2 t - \left(N + 1 - n\right)\theta_2\right)\right) \tag{5.18}$$

where the incident signal at port one is at f_1 and the incident signal at port two is at f_2. The magnitude of the IM3 terms at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are different at the forward port (port three) and are equal to

$$\begin{aligned} &IM3_{cross,\omega_l} = \tfrac{3}{4} g_{m,3} V_o^3 \times \\ &\sum_{n=1}^{N} \cos\left(\omega_l t - 2n\theta_2 + 2\left(N+1\right)\left(\theta_2 - \theta_1,\right)\right) \end{aligned} \tag{5.19a}$$

$$\begin{aligned} &IM3_{cross,\omega_h} = \tfrac{3}{4} g_{m,3} V_o^3 \times \\ &\sum_{n=1}^{N} \cos\left(\omega_h t + 4n\theta_2 + \left(N+1\right)\left(\theta_1 - 4\theta_2.\right)\right) \end{aligned} \tag{5.19b}$$

Evaluating these sums, each of the intermodulation terms can be expressed in terms of the distribution factor:

$$\begin{aligned} &IM3_{cross,\omega_l} = \\ &\tfrac{3}{4} g_{m,3} N V_o^3 \cos\left(\omega_l t + 2\theta_2 - 2\left(N+1\right)\theta_1\right) \tfrac{\sin(N\theta_2)}{N\sin(\theta_2,)} \end{aligned} \tag{5.20a}$$

$$IM3_{cross,\omega_h} = \frac{3}{4} g_{m,3} N V_o^3 \cos\left(\omega_h t - 4\theta_2 + (N+1)\,\theta_1\right) \frac{\sin(2N\theta_2)}{N\sin(2\theta_2.)} \tag{5.20b}$$

Each of the IM3 terms vanish when $N\theta_2 = k\pi$. Under this condition, the cross-propagating signal at f_2 does not introduce intermodulation terms at port three. While f_1 and f_2 generate intermodulation products at each stage of the distributed circuit, this distortion is cancelled at the reverse port at certain frequencies. The IM3 terms are roughly independent of the frequency spacing between the tones since the distribution factors do not depend on θ_1. Similarly, the intermodulation products at port four would cancel when $N\theta_1 = k\pi$.

The IM3 products are confirmed with circuit simulations of IIP3 in Fig. 5.27 (b). The co-propagating IIP3 is constant over the bandwidth of the distributed structure as predicted from (5.17). However, the cross-propagating IIP3 is generally better than the co-propagating IIP3 because of the distribution factor in (5.20a) and (5.20b). Since (5.20b) depends on $2\theta_2$, twice as many peaks occur in the IIP3 of this term as opposed to (5.20a).

5.6.5 Circuit Design

The seven-stage distributed amplifier is designed for operation at the 24-GHz ISM band. Optimum N, f_c and V_{gs} exist to increase the forward gain and IIP3 while reducing noise figure for dual channel operation. To minimize the distribution factor in (5.7), the parameters N and f_c trading-off reverse gain null location and noise figure have been shown in Section 5.6.2 and 5.6.3.

In moderate inversion ($V_{gs} = 390$ mV), the proposed DA is simulated with respect to the number of stages in Fig. 5.28. At 24 GHz, the noise figure is found to be minimum for seven stages. The minimum noise figure occurs between 10 and 15 GHz or at roughly half the cut-off frequency of the amplifier. At 24 GHz, more than seven stages increases the noise figure.

Next, (5.8) indicates that a cut-off frequency of f_c = 35 GHz places a null of the reverse gain frequency response at 24 GHz when $N = 7$ at the third null ($k = 3$) of the reverse gain. Alternatively, the null at 24 GHz could be realized if $N = 6$ and $f_c = 30$

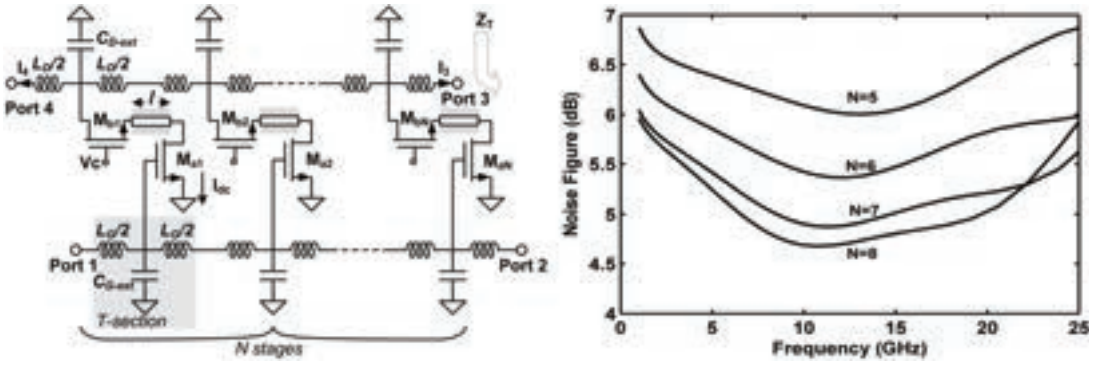

Figure 5.28: Noise figure as a function of the number of stages.

GHz.

Given f_c = 35 GHz, the seven-stage distributed amplifier is implemented as shown in Fig. 5.28 using the design parameters summarized in Fig. 5.23. The common-source device width is chosen to be 100 μm to provide a gate capacitance of 70 fF that is absorbed into the *T*-network with an inductance of 420 pH and an external capacitance is chosen to be 120 fF to provide a total gate capacitance of 190 fF. This sets the cut-off frequency and the impedance of the transmission line. DAs are limited by the attenuation of the gate and drain transmission lines in standard bulk CMOS technologies. The series resistance of the inductors impacts the quality factor of the transmission line. Square spiral inductors are fabricated on the two thick aluminum metal layers with a patterned ground shield under the inductor and the width of the inductor is increased to reduce the loss of the inductor. Electromagnetic simulations using SONNET shows that the *Q* of the inductor is improved from 13 to 15 at 24 GHz with the patterned ground shield.

The common source and cascode devices are low voltage threshold devices with V_{th} = 260 mV. Each stage in Fig. 5.28 employs a cascode to improve reverse isolation and eliminate the Miller capacitance of M_a. Additionally, the cascode output impedance is increased by approximately $1 + (g_m + g_{m,b})r_{ds}$ to reduce the conductive loading on the drain transmission line. To improve bandwidth and decrease noise, the cascode stage incorporates an inductor between the common-source drain and common-gate source to resonate the transistor capacitances [63]. In this design, the cascode transistor is isolated by a transmission line rather than an inductor. At 24 GHz, a length of 250 μm provides

an additional 1dB of gain over a design without the cascode transmission line.

5.6.6 Measurements

The circuit is implemented in a 0.13 μm CMOS process (f_T = 85GHz) with 1 μm-thick copper interconnects. The chip microphotograph is shown in Fig. 5.29. The circuit occupies an area of 0.50 mm x 1.20 mm (0.60mm^2) including the pads. Gate and drain biasing is provided through external bias-tees at each of the four ports.

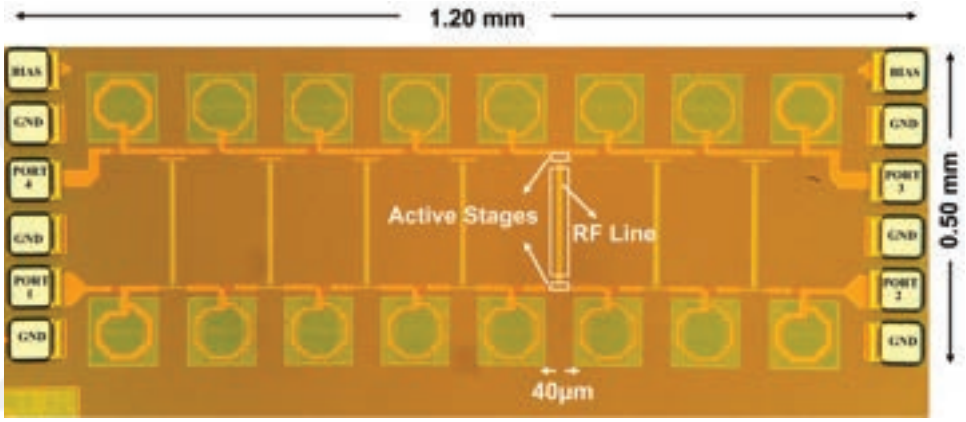

Figure 5.29: The chip microphotograph of the distributed amplifier in a 0.13μm CMOS process.

S-parameters are measured using on-chip probing with the Agilent E8361A two-port network analyzer. The measured *S*-parameters for forward gain and reverse gain are plotted in Fig. 5.30 (a). The forward gain, S_{31}, is 9.6 dB at 24 GHz with a 0.4-dB ripple over a bandwidth of 35 GHz. The reverse gain, S_{41}, is 17 dB and remains better than 10 dB over a bandwidth of 4 GHz. The measured depth of the nulls is compared to the simulation in Fig. 5.30 (a) and indicates that the *Q* of the transmission line section is around 15. The artificial transmission line loss, S_{21}, is measured and compared to simulation in Fig. 5.30 (a) and illustrates that frequency-dependent loss of the transmission line is 4 dB or roughly 0.5 dB per stage at 24 GHz.

The input and output return loss, S_{11} and S_{22}, are plotted in Fig. 5.30 (b) and remain below 10 dB over a bandwidth of 35 GHz. Low return losses at low and high frequencies are introduced by the transmission line impedance matched to the source and load impedances. The reverse isolation, S_{13}, is better than 30 dB due to cascode

gain stages. The DA is unconditionally stable over the bandwidth with a minimum μ-factor of 2.9.

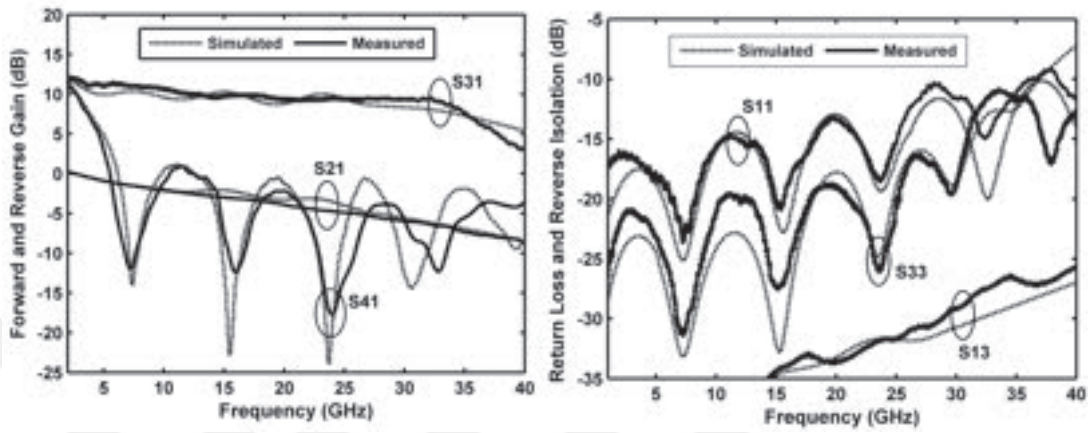

Figure 5.30: Measured S-parameters illustrating (a) forward and reverse port gain and (b) measured input and output return loss and isolation.

The noise figure is plotted in Fig. 5.31 (a) as a function of the gate voltage. The noise figure is measured using the Agilent 346CK01 noise source and the Agilent E4447A spectrum analyzer. The optimum gate voltage is 415 mV for a minimum noise figure of 5.7 dB at 24 GHz. The minimum noise figure occurs at a 400 mV bias at 8 GHz and is relatively independent of frequency.

The IIP3 is plotted in Fig. 5.31 (b) as a function of the gate voltage under the co-propagating signal conditions. The optimum gate voltage is 415 mV for a maximum IIP3 of 4.5 dBm at 24 GHz. Notably, the maximum IIP3 and minimum noise figure occurs at roughly the same gate-source bias voltage. The maximum IIP3 increases to 9.4 dBm at 8 GHz for a slightly lower bias voltage. Consequently, the circuit is biased in moderate inversion and each transistor consumes 2.1 mA of drain current from a 1.2 V supply for a total power consumption of 18 mW. The measured noise figure and output referred one-dB compression point are plotted versus frequency in Fig. 5.32. The noise figure is between 5.5 dB and 6 dB at 24 GHz. The P1dB at 8 GHz and 24 GHz is 6.2 dBm and 4.9 dBm, respectively, for $V_{gs} = 400$ mV.

The proposed DA performance is compared with other 24 GHz LNAs and DAs in similar silicon technologies in Table 5.1. The amplifier performance is optimized with respect to maximum linearity. The proposed dual-channel amplifier at 24GHz is

comparable in power consumption, gain, and noise figure and demonstrates the highest IIP3 and P1dB when compared to previous work and does not constrain noise figure.

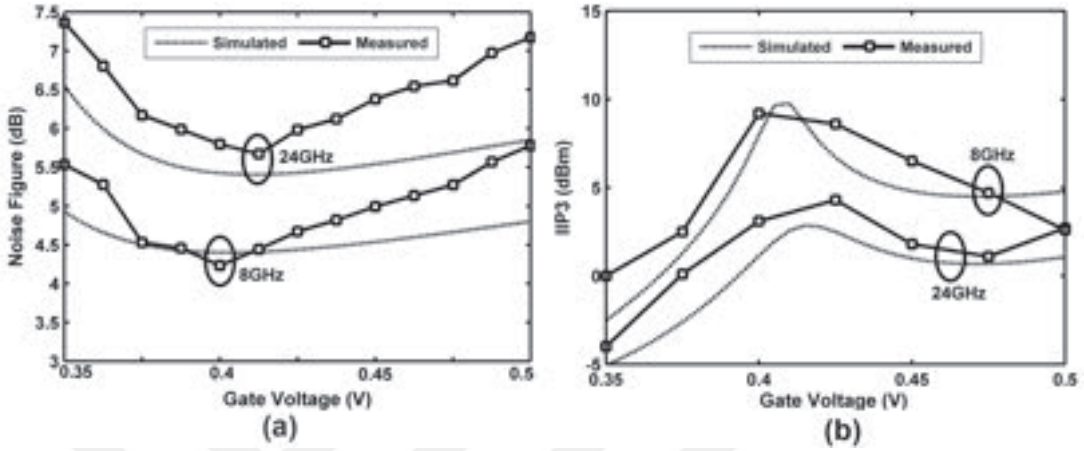

Figure 5.31: Measured and simulated (a) noise figure and (b) IIP3 variation with gate biasing.

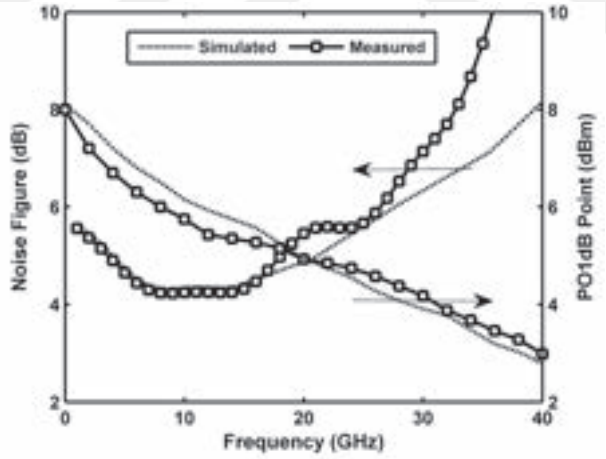

Figure 5.32: Measured and simulated noise figure variation as a function of frequency ($V_{GS} = 400$ mV)

Table 5.1: Comparison to reported tuned and wideband amplifiers

Ref.	Technology	Topology	Frequency (GHz)	Gain (dB)	NF (dB)	PO1dB (dBm)	IIP3 (dBm)	Power/Vdd (mW/V)
[53]	0.18μm CMOS	CS LNA	22-26	13	4	1	0.5	14 / 1
[55]	0.13μm CMOS	CG LNA	20-27	14	6	-9	-13	19 / 1.5
[67]	0.13μm CMOS	CS LNA	18-26	12.5	4.5	N.A.	0.5	17 / 1.2
[68]	0.18μm CMOS	CG LNA	21-27	9.3$\pm$1.3	4.9 - 6.1	-4.7	-4	27 /1.8
[69]	0.18μm CMOS	CS LNA	22-26	12.8	3.3	N.A.	N.A.	8 / 1
[70]	0.18μm SiGe	DA	0.1-23	14.5$\pm$0.9	5	-12	0.3	54 / 3.6
[71]	0.18μm CMOS	CMOS DA	2-24	5$\pm$2	6	4	N.A.	40 / 1.2
[72]	0.18μm CMOS	CMOS DA	0.1-22	7.3$\pm$0.8	4.3-6.1	5.3	N.A.	52 / 1.3
[73]	0.13μm SOI CMOS	CMOS DA	1-26	7.1$\pm$1.1	6.5-7.5	5	N.A.	57 / 1.4
This work	0.13μm CMOS	CMOS DA	23-25	9.6$\pm$0.4	5.5-6	4.9	4.8	18 / 1.2

*: $IIP3$ =input referred $P1dB + 10dB$ is an assumption made. CS: Common source, CG: Common gate

5.6.7 Multi-Band Dual Channel Circuit Design

The previous discussion has suggested the use of the dual-channel distributed amplifier for narrowband applications at the 24-GHz ISM band. The array factor analysis in (5.7) demonstrates reverse gain nulls at $\theta = k\pi/N$ and suggests that the distributed amplifier can operate at multiple bands since the reverse gain of the DA is minimized at integer intervals of *k*. For the multi-band operation as described in Fig. 5.33, high and low-pass terminations terminate each of the different bands. Each termination could be a notch filter with resonance at the input frequencies. As shown in Fig. 5.33, the low frequency band propagates along the gate line from left to right, S_{31} while the high frequency band propagates from right to left, S_{42}. The gate line demonstrates the nulls at both 8 GHz and 24 GHz.

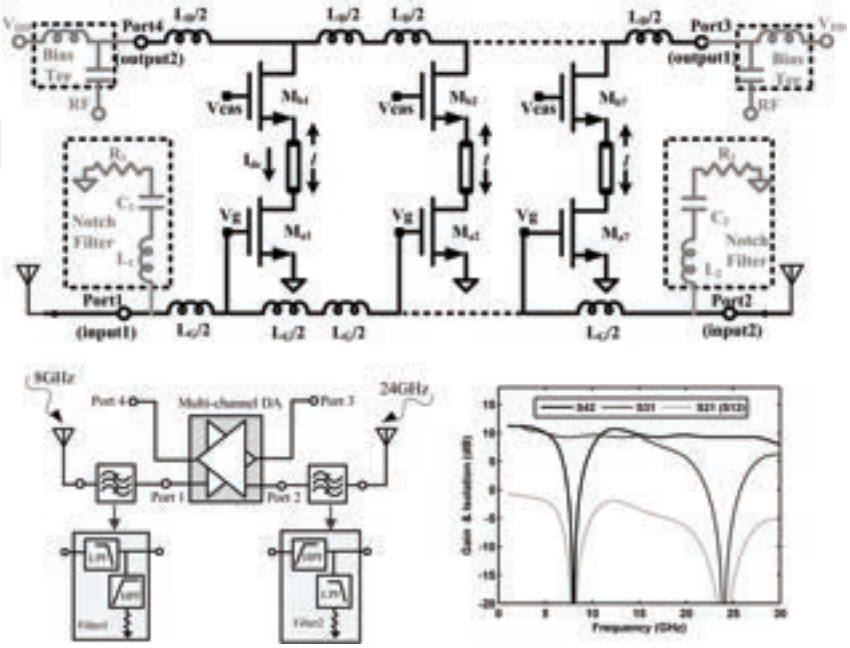

Figure 5.33: Multi-band dual channel circuit design.

5.7 Conclusion

This chapter presents the novel circuits replacing the conventional elements in an active/passive beamforming front-end transceiver. The bidirectional circuit elements are

proposed to place in a bidirectional active phased array transceiver which can be placed at the front-end of a low power and low cost pulse compression radar (PCR) system.

A *W*-band bidirectional amplifier, which operates as either an LNA or PA, is designed and fabricated in a 0.13 μm BiCMOS technology. The bidirectional amplifier that switches between low-noise amplification and power amplification is proposed to avoid the insertion losses due the SPDT switches. This design is based on the cascaded constructive wave amplifier (CCWA) which uses a transmission line and an active shunt feedback circuit which feeds current back to the input of the quarter-wave transmission line to introduce a small amount of positive feedback to generate gain. Feedback amplifiers decide the direction of amplification and only one feedback amplifier operates at a time to provide gain in either the forward and backward direction. The measured amplifier has a peak gain of 16 dB, a bandwidth of 14.5 GHz at 90 GHz, a noise figure of 11 dB and an output-referred P1dB of 1 dBm at 90 GHz.

A *W*-band, varactor-loaded, constructive wave phase shifter/VGA is designed in 0.13 μm BiCMOS technology for continuous phase and amplitude control and calibration of the relative phase and gain errors. The analog phase shifter/VGA incorporates a constructive wave amplifier along a varactor-loaded transmission line to compensate for the varactor losses without introducing a significant phase or gain imbalance. In the phase shifter mode, more than 65° of continuous phase control is demonstrated with a maximum gain of 16 dB to compensate for varactor losses with a power consumption of only 36 mW. A 7dB gain variation - from 9 dB to 16 dB - is achieved in the VGA mode while the phase imbalance is minimized at 98 GHz.

A low-power DA with isolation between amplifier channels is presented to replace two LNAs. The DA is biased in moderate inversion to simultaneously obtain low NF and high linearity while consuming low power. The dual-channel DA is fabricated in a bulk 0.13-μm CMOS process, achieves a forward gain of 9.6 dB and a NF of 4.9 dBm, and consumes 18 mW power which is equivalent to 9 mW per low noise amplifier.

5.8 Acknowledgement

I would like to acknowledge that bidirectional circuits were funded with DARPA Young Faculty Award under Dr. Michael Fritze at DARPA MTO. The TAPO office supported the fabrication of the bidirectional circuits in 0.13 μm BiCMOS technology. The support of Don Kimball at the CaliT2 mm-wave Laboratory is greatly appreciated. The authors thank Dr. Joohwa Kim for his help on the bidirectional amplifier measurements.

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1. M. Parlak, M. Matsuo and J. F. Buckwalter, "Bidirectional Circuitry for Millimeter-Wave Pulse Compression Radar", *IEEE International Radar Conference (RadarCon)*, pp. 1062-1067, May 2011.

2. M. Parlak and J. F. Buckwalter, "A Low-power, Dual-channel Distributed Amplifier for Multi-element Receivers", *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 2, pp. 435-442, Feb. 2011.

3. M. Parlak and J. F. Buckwalter, "A Low-Power, W-Band Phase Shifter in a 0.12-μm SiGe BiCMOS Process", *IEEE Microwave and Wireless Components Letters*, vol. 20, no. 11, pp. 631-633, Nov. 2010.

4. J. Kim, M. Parlak, and J. F. Buckwalter, "A 77-GHz to 90-GHz Bidirectional Amplifier for Half-duplex Front-ends" *IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2010. [Intel/CICC Student Scholarship Award]

5- M. Parlak and J. F. Buckwalter, "Bidirectional Beamforming with Analog / Baseband Pulse Compression System", SD2012-389 - *Patent submitted via Tech Transfer Office at UCSD*.

The dissertation author was the primary author of this material except the conference paper at CICC, 2010.

Chapter 6

Integrated *Q*-Band Receiver Circuits in 45-nm SOI CMOS Process

This chapter presents the design and the measurement of millimeter-wave integrated circuits implemented in a 45-nm CMOS silicon-on-insulator (SOI) process. The performance of a single-pole double-throw (SPDT) switch, a passive I/Q mixer and a low noise amplifier (LNA) at Q-band is demonstrated. Section 6.1 introduces the motivation for SOI-process and its promise for commercial applications. In Section 6.2, the 45-nm CMOS SOI process is introduced. The switch performance at millimeter-wave bands in 45-nm CMOS SOI process is compared to the performance in bulk CMOS processes. A series switch insertion loss is simulated to emphasize the benefits of 45-nm SOI technology over bulk CMOS processes for passive performance at mm-wave bands in Section 6.2.1. Circuit analysis, simulation and measurements of the broadband SPDT switch are presented in Section 6.3. Circuit analysis, simulation and measurements of the I/Q passive mixer are presented in Section 6.4. Finally, a *Q*-band LNA is presented in Section 6.5. The results indicate that 45-nm CMOS SOI demonstrates the lowest switch insertion loss, lowest ring mixer conversion loss and lowest noise figure compared to other CMOS processes [74–76].

6.1 Introduction

Highly-scaled digital CMOS SOI is an excellent candidate platform for digital, analog and RF integration in a monolithic system-on-chip (SOC) package. Monolithic integration in CMOS SOI minimizes the system and packaging complexity, reduces system variability, and supports embedded RAM and microprocessors for radiation hard applications [77]. However, the application of digital CMOS SOI technologies for RF applications requires a focus beyond the scaling and optimization of transistors. Passive devices such as inductors, baluns, transmission lines, and pads degrade as metallization dimensions are scaled down to increase the transistor speed and the integration density. Nonetheless, a variety of efforts based on scaled CMOS SOI technology have shown low-noise and high-power handling circuits, distributed wideband amplifiers, mixers, SPDT switches, and optical transceivers [73, 78–85].

In the near future, beamforming systems and phased arrays will be provided as the front-ends of indoor/outdoor surveillance, intelligent sensing and imaging sensors which require significantly low power consumption. In such case, passive circuits are critical components in virtually every wireless-transceiver building block and are preferred to take place in each channel of the array to reduce the overall power consumption. Passive circuits are usually implemented as a combination of switches such as on/off FET devices and the performance of the passive circuits are dependent on the performance of the switches.

Fig. 6.1 (a) shows the block diagram of a low power, RF phase shifting beamformer transceiver with several key front-end circuits including the SPDT switch, phase shifter and I/Q mixer implemented as passive elements.

The SPDT switch is realized by switching the port 1 between ports 2 and 3 with the help of CMOS transistors as switches as shown in Fig. 6.1 (b). The SPDT switch combine the series and parallel switches to provide isolation between the transmitter and receiver. The switch must exhibit low insertion loss to maintain high transmitter efficiency and output power and low receiver noise figure to achieve a reasonable SNR. High linearity is also important to prevent the compression and intermodulation distortion. The passive ring mixers are realized by switching FET gates of a ring topology and biasing the transistor gates at the threshold voltage as shown in Fig. 6.1 (c). The

insertion loss and linearity of the switch determines the performance of the mixer. The phase shifters are composed of cascaded switch elements and the insertion loss of the phase shifter is the sum of the losses through the switches and generally increases with phase shift range as shown in Fig. 6.1 (a). Achieving full 360° phase variation with fine resolution from a passive phase shifter is too lossy.

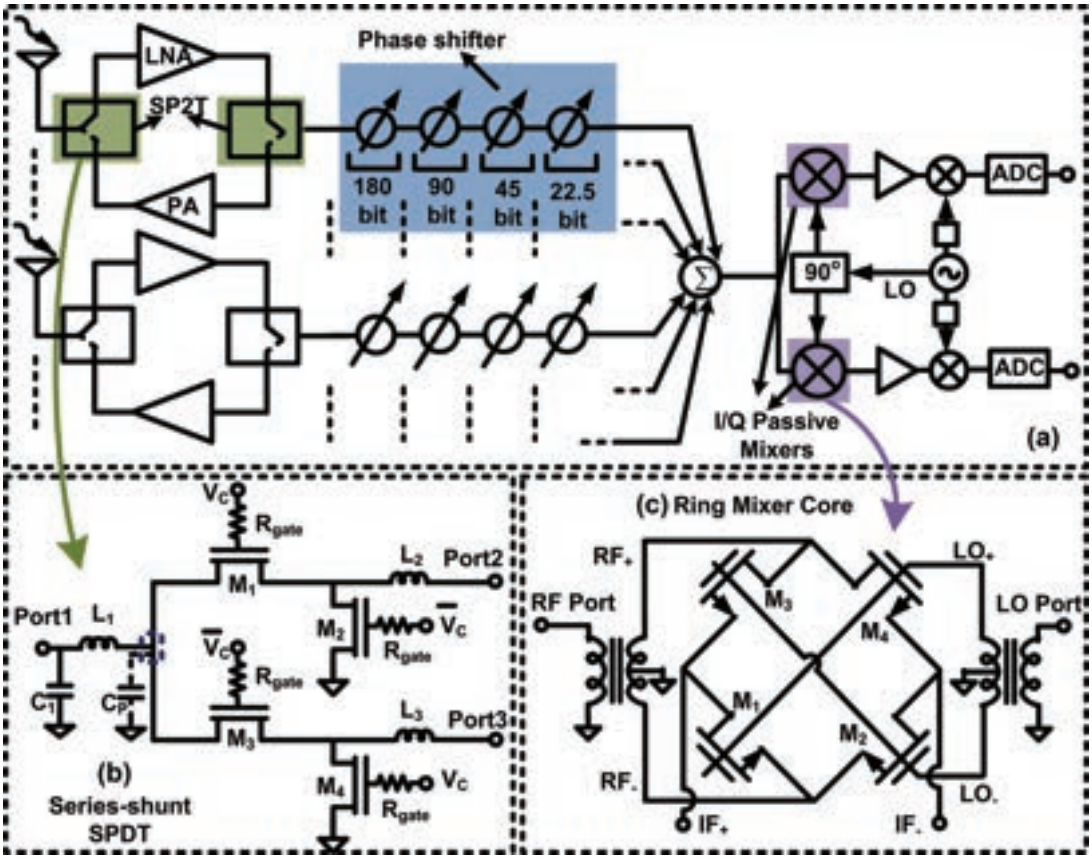

Figure 6.1: (a) Block diagram for RF phase shifting beamformer transceiver with the (b) SPDT switch and (c) I/Q mixer implemented as passive elements.

6.2 45-nm SOI CMOS Process

In Fig. 6.2, the cross-sections of the bulk triple well CMOS and detailed stack-up for the digital 45-nm SOI CMOS process are shown. In the SOI process, eleven metal layers are available with a 2.2 μm thick aluminum top metal layer (LB). The SOI substrate is a p-doped "handle" wafer with a resistivity of 13.5 Ω-cm and is isolated from

the active region with a thin buried oxide (BOX) layer, which isolates the transistor from the substrate. The BOX thickness is 145 nm in this process - roughly three times the minimum gate length. Nonetheless, the BOX mitigates many of the problems associated with bulk processes at millimeter-wave frequencies. The BOX layer provides significant isolation of the active transistor area from the substrate without degrading the voltage threshold of the NFET. The technology also utilizes shallow trench isolation (STI) to provide a denser isolation between devices. The STI extends 80 nm through the active silicon layer and increases the isolation between the diffusions of different NMOS transistors. The switch design and passive circuit design in The 45-nm SOI CMOS process helps reduce the main limitations of CMOS transistors when used as a switch. The junction diode between the source/drain node and the substrate, C_{jd} and C_{js}, is much less compared to the one in bulk processes and this enables low isolation. As shown in Fig. 6.2 (b), the substrate resistance network, R_{sub}, from the junction to the substrate ground is isolated and less critical owing to the BOX layer and C_{jSTI} in SOI CMOS process compared to the uncertain value of R_{sub} in bulk CMOS resulting in the insertion loss and isolation discrepancies. The SOI process offers body-contacted and floating-body NFET which has an f_T of 380 GHz with low drain/source coupling to the substrate and low high-frequency noise.

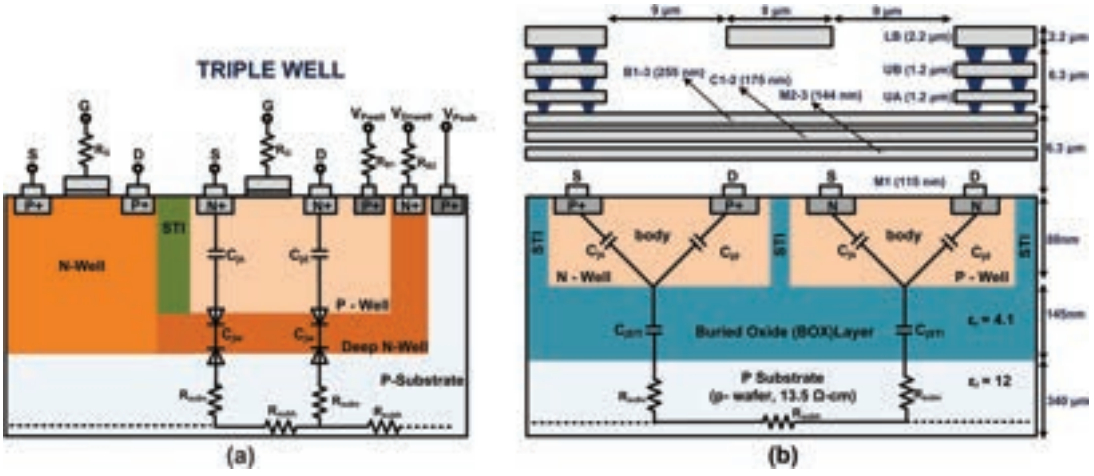

Figure 6.2: Cross section of (a) the bulk CMOS triple well and (b) 45-nm SOI CMOS process.

SONNET was used to simulate the performance of the spiral inductors, pas-

sive baluns, multiple finger fringe capacitors, conventional CPW-lines, on-chip interconnects, and pads in *Q*-band. The effect of the substrate resistivity and BOX thickness on the quality factor of the spiral inductors is investigated. In Fig. 6.3, the quality factor of a spiral inductor is investigated as a function of frequency for different combinations of substrate resistivity and BOX thickness. When the substrate resistivity is increased from 0.01 to 13.5, the quality factor of the spiral inductor increases significantly. Increasing its resistivity to > 100 Ω-cm reduces the impact of thinner BOX on parasitic capacitance and also improves the quality factor of passive components. When substrate is highly-resistive, increasing the BOX thickness has an insignificant effect on the quality factor. However the quality factor increases with the increasing BOX thickness when the substrate is rather more conductive. The increasing of the quality factor of the passive components is mainly attributed to the increasing substrate resistivity of the SOI wafer to > 10 Ω-cm, which leads to dramatically decreasing of coupling loss to the Si substrate.

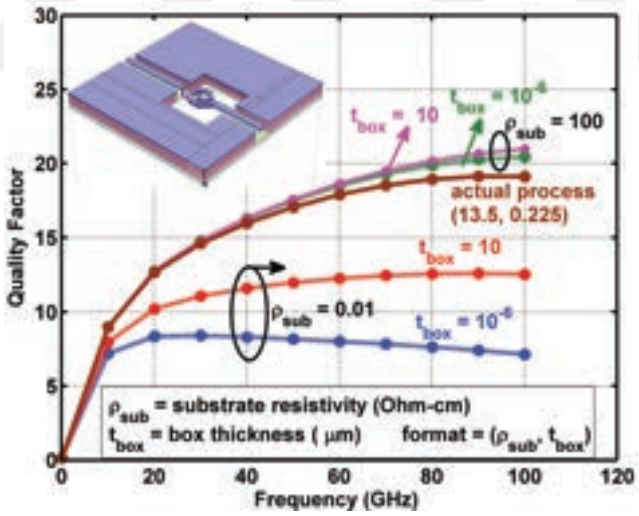

Figure 6.3: The effect of the BOX thickness and substrate resistivity on the quality factor of inductors.

A vertical natural capacitor model (VNCAP) is used for high-frequency capacitors and is formed with inter-digitated metal fingers composed of C1 to B3 metal layers. Lower metal layers are not used since they result in higher parasitic shunt capacitance per 1 fF of series capacitance, which degrades the performance at millimeter-wave frequencies. A shielded coplanar waveguide (CPW) transmission line is designed using

LB for the signal line and B3 for the ground plane, and the LB side grounds are connected to B3 using UA and UB metal layers as shown in Fig. 6.2 (b). A signal line width of 8 μm with 9 μm spacing to the side grounds results in a 50 Ω transmission line at millimeter-wave frequencies.

In summary, the reported benefits of 45-nm SOI technology relative to bulk CMOS processes include lower parasitic capacitance due to the BOX isolation from the bulk silicon as shown Fig. 6.2. The junction capacitances are limited to the BOX capacitance and are 4 to 7 times smaller than in bulk CMOS. Other benefits of the SOI process includes system on chip (SoC) full integration capabilities, negligible substrate leakage, higher isolation, increased f_t/f_{max} performance enabling efficient amplification. Therefore 45-nm technology in SOI is a good candidate to explore for improved loss, isolation and linearity characteristics. The FET channel resistance, R_{ch}, and insertion loss of the switches improves with the device scaling and, consequently, both resistive mixer conversion loss and SPDT insertion loss will improve due to the FET scaling. And the buried oxide layer between the body of the FET and substrate improves the isolation, leakage and linearity characteristics. To quantify the claims made in this section, the series NFET switch insertion loss and isolation is simulated with respect to its width, W_T, in five different processes - IBM SiGe 8HP (130nm), IBM CMOS 9RF (90nm), TSMC CMOS CRN90LP (90nm), IBM CMOS 7SOI (180nm) and IBM CMOS 12SOI (45nm) technologies. Before the comparison is illustrated, the switch principles are explained in the next section 6.2.1.

6.2.1 SOI CMOS Process versus bulk CMOS

A test-bench and the small signal models of the switch in the on and off states are illustrated in Fig. 6.4. When the FET is on and off, the equivalents impedances Z_{on} and Z_{off} are

$$Z_{on} = R_{ch} = \frac{L_g}{\mu_n C_{ox} W_t \left(V_{gs} - V_t\right)}, \tag{6.1}$$

$$Z_{off} = \frac{1}{1/j\omega_{RF}\left(C_{eqv.}\right)}, \tag{6.2}$$

$$C_{eqv.} = C_{gs} \parallel C_{gd} + C_{js} \parallel C_{jd} \tag{6.3}$$

where $C_{gs} \simeq W_t L_g C_{ox}/2$.

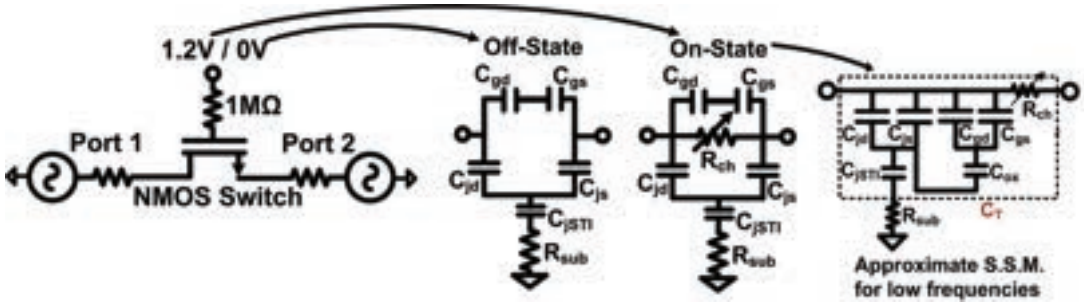

Figure 6.4: The test bench for a nMOS switch and its simplified small-signal circuit model in the ON and OFF states.

The Z_{on} impedance is dominated by the channel resistance, R_{ch}. The Z_{off} impedance is dominated by the parasitic capacitances - parallel combination of the series capacitance of the gate-drain and gate-source capacitances, (C_{gd} and C_{gs}), and series capacitance of the drain and source junction capacitances, (C_{jd} and C_{js}).

Insertion Loss and Isolation of a Series Switch

The insertion loss is determined mostly by the Z_{on} impedance. Increasing the FET width, W_T, provides lower channel resistance and lower insertion loss however also reduces the off-state impedance, Z_{off}, degrading the isolation. The choice of W_T establishes the trade-off between Z_{on} and Z_{off}, and between insertion loss, isolation and linearity. In the off-state, R_{ch} is high. Since $C_{eqv.}$ is proportional to W_T, increasing the off-impedance requires a smaller device width, W_T.

To assess the impact of the BOX layer and substrate resistance, the insertion loss from a single MOS transistor has been analyzed based on the MOS transistor shown in Fig. 6.4. Since the impedance of the junction capacitance is very low at millimeter-wave frequencies, the substrate resistance R_{sub} plays a critical role. It has been shown that insertion loss can be reduced by increasing R_{sub} to a very large value or by decreasing R_{sub} to near zero [86]. In terms of the underlying physical mechanism, when R_{sub} becomes large, signals cannot couple through R_{sub} and the power delivered to R_{sub} is small. When R_{sub} is zero, there is no loss associated with R_{sub} and the power loss is once again reduced. In this digitally-compatible SOI process, R_{sub} is smaller comparatively to the other technologies and the BOX layer provides a capacitance C_{jSTI} that is small

and isolates the body from substrate. In other words,

$$C_T = \left(\frac{(C_{gs} + C_{gd})\, C_{ox}}{C_{gs} + C_{gd} + C_{ox}} + C_{js} + C_{jd} \right) \shortparallel\, C_{jSTI} \tag{6.4}$$

is the equivalent capacitance shown in the approximate small signal model in Fig. 6.4. C_T is zero when $C_{jSTI} \sim 0$ and when $C_T = 0$, the insertion loss is defined by [86]

$$IL \sim \left(\frac{R_{ch} + 2Z_0}{2Z_0} \right)^2 \text{when } C_T = 0 \tag{6.5}$$

which is used to estimate the insertion loss at low frequencies.

The comparison of the insertion loss and isolation of a series switch in various technologies is illustrated in Fig. 6.5 and in Fig. 6.6. In bulk processes, higher insertion loss is found as a result of the high channel resistance of the ON switch and coupling loss through the substrate via parasitics. Therefore deep n-well transistors, high substrate contact resistance, and deep trench isolation are provided for bulk CMOS in the literature. As shown in Fig. 6.5, the insertion loss starts to degrade again after an optimum value of transistor width since signals start to leak to the substrate through the parasitics in bulk processes. The luxury of being able to select larger the transistor width enables less insertion loss for the switches, passive mixers and passive phase shifters in CMOS SOI process and switches can be designed with better conversion loss characteristics. Fig. 6.6 shows the isolation of the switch in various technologies. Although C_{jd} and C_{js} are much smaller compared to the ones in bulk CMOS, C_{gd} and C_{gs} are comparable sizes so CSOI7 and CMOS 12SOI don't improve the series transistor isolation.

The optimum widths corresponding to the minimum insertion losses are chosen for the five processes. Fig. 6.7 (a) shows the comparison of the insertion loss of a series switch versus frequency when the series switch is on. The 12SOI 45-nm SOI and CSOI7 process provides the best insertion loss demonstrating the superiority of SOI process over bulk processes. Fig. 6.7 (b) shows the comparison of the isolation of a series switch versus frequency when the series switch is off. The isolation of the series transistor in SOI CMOS is not better than the other technologies since C_{gd} and C_{gs} are comparable sizes.

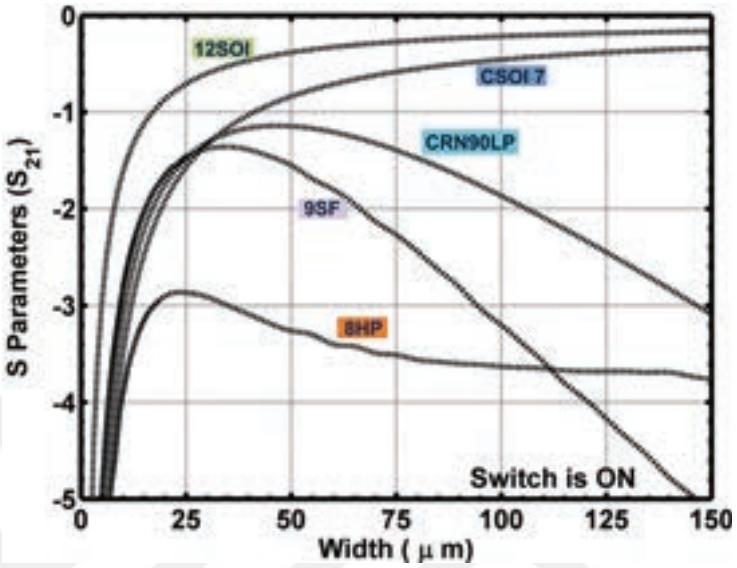

Figure 6.5: The insertion loss of a series switch in various technologies.

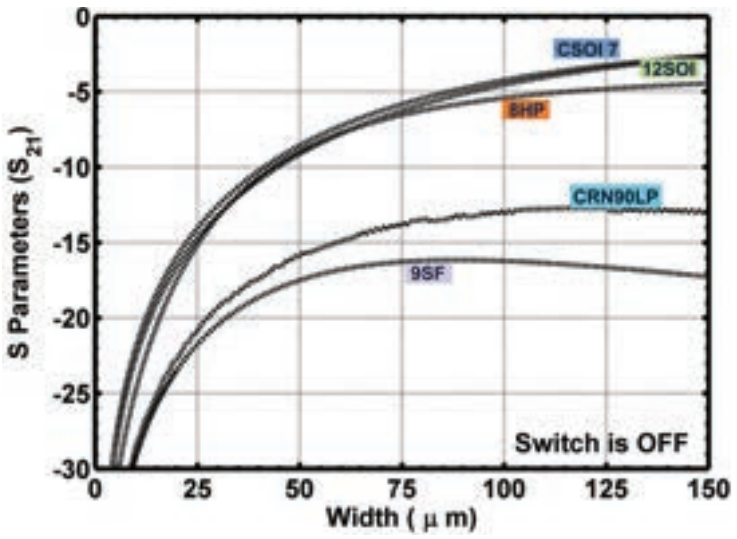

Figure 6.6: The isolation of a series switch in various technologies.

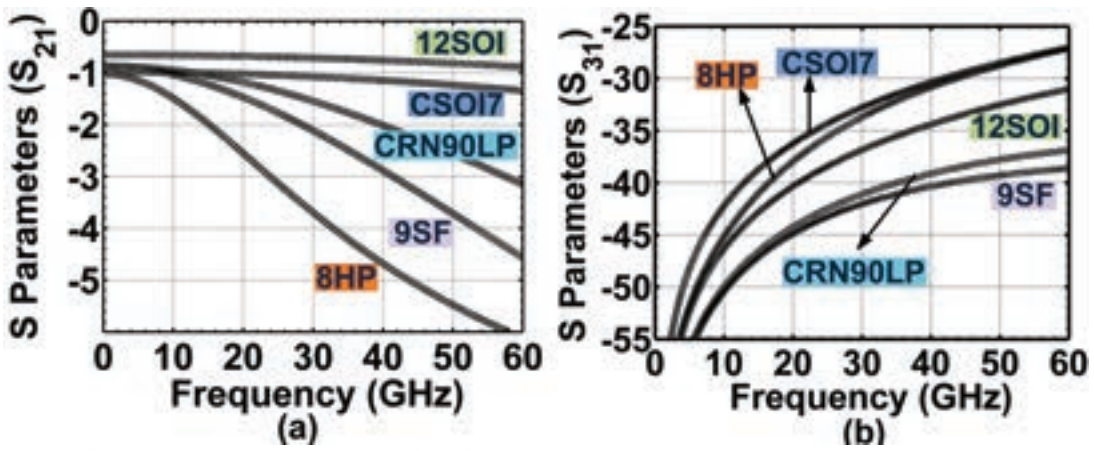

Figure 6.7: Comparison of (a) the insertion loss and (b) the isolation of a series switch in various technologies.

6.3 Single-Pole Double-Throw (SPDT) Switch

RF transceivers require a SPDT switch to provide isolation between the transmitter and receiver. The switch must exhibit low insertion loss to maintain high transmitter efficiency and output power and low receiver noise figure to achieve a reasonable SNR. High linearity is also important to prevent intermodulation distortion. Previously, SPDT switches have been demonstrated using bulk CMOS processes which tend to increase the signal coupling to the semi-conductive silicon substrate at millimeter-wave bands [87–93]. In bulk processes, higher insertion loss and lower isolation is found as a result of resistive coupling through the substrate. CMOS SOI processes improve the insertion loss and isolation of millimeter-wave SPDT switches [83].

Shown in Fig. 6.8 are four different topologies for SPDT switches, which switch between port 1 and ports 2 and 3. The switches consist of NFETs with aspect ratio of 40 μm / 45 nm. The return loss of each design is simulated to be better than 25 dB. The $\lambda/4$ transmission line in the shunt-shunt switch creates an open circuit at the common node when the shunt FET is biased at triode, which limits the bandwidth of the switch.

On the other hand, the series-shunt switch is more broadband and offers more compact layout. However, neither the series-shunt and shunt-shunt switches tend to offer as much isolation as the series-shunt cascaded switches offer (> 60dB) however the additional series FETs degrades the insertion loss. A comparison of the insertion

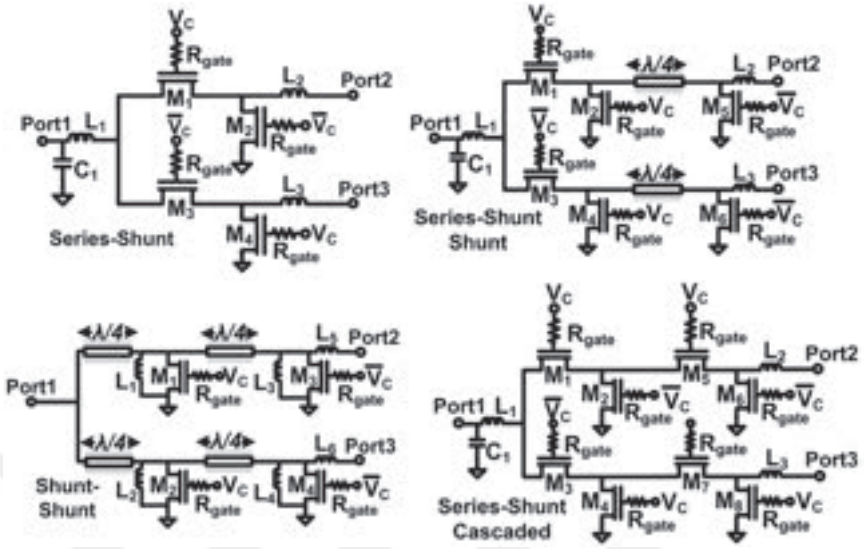

Figure 6.8: Various SPDT circuit architectures.

loss and isolation for each type of switch is shown in Fig. 6.9. The series-shunt switch offers the lowest insertion loss and highest bandwidth with acceptable isolation.

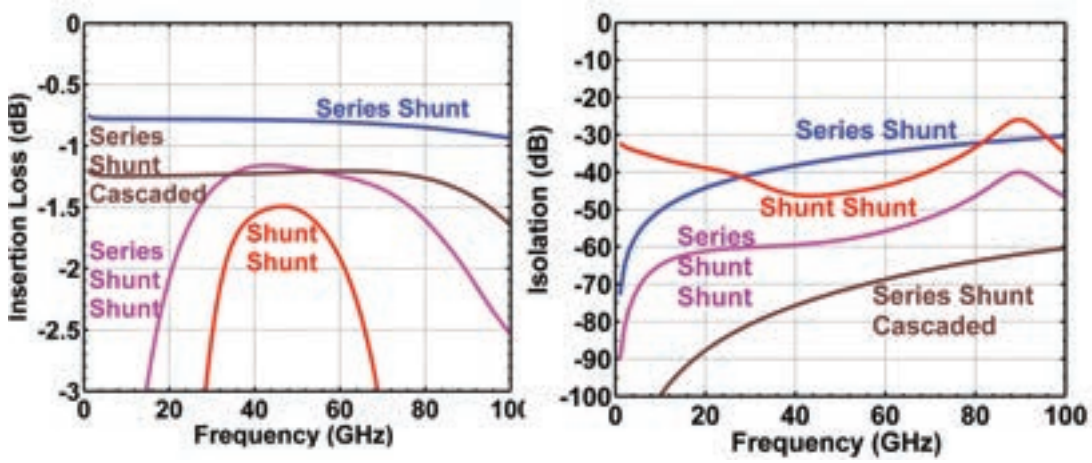

Figure 6.9: Comparison of insertion loss and isolation for various SPDT circuit architectures.

Signal paths degrading the insertion loss and isolation of the series-shunt switch are shown in Fig. 6.10. The insertion loss degrades due to the undesirable signal paths, i.e. path 1, path 2 and path 3. Path 1 occurs due the capacitance between drain and source, i.e. the series combination of the gate-source, C_{gs}, and gate-drain capacitor, C_{gd}, of the series transistor. Path 3 occurs because of series capacitance between the

source junction capacitance, C_{js}, and drain junction capacitance, C_{jd}. Path 2 is through the channel resistance and should dominate over paths 1 and 3. Similarly, the isolation degrades due to signal paths 4-6 as shown in Fig. 6.10. Path 4 is analogous to Path 1 for the series on device and path 5 is similar to path 3. However, path 6 crosses the BOX, C_{jSTI}, transits through the substrate resistance, R_{subh}, and returns through C_{jSTI}.

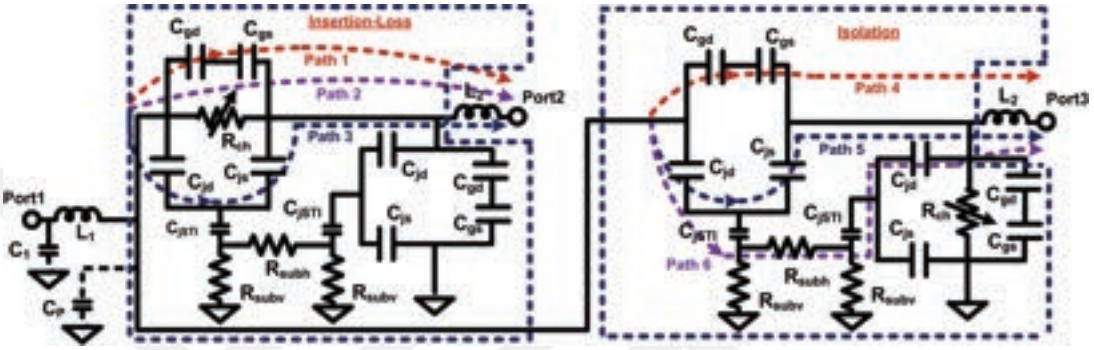

Figure 6.10: Small-signal circuit model describing the paths that degrade the insertion loss and isolation of the series-shunt switch.

6.3.1 Circuit Design

Fig. 6.11 (a) shows the implemented switch schematic based on a combination of two series-shunt SPST circuits with input and output matching networks. EM simulation models series inductors at ports 1, 2, and 3 to isolate the parasitic capacitance as shown in Fig. 6.11 (a). The capacitance at the common node is matched using a wideband CP-L_1-$C1$ circuit, where L_1 = 198 pH and $C1$ = 52 fF. The output matching circuit is implemented using a series 115 pH inductor.

The insertion loss and isolation are plotted as a function of the FET width, W_T as shown in Fig. 6.11 (b). The insertion loss is mostly dependent on the size of the series FET, M_1. As W_T increases, the parasitic capacitance also increases the capacitive coupling to the substrate and eventually results in unacceptable signal loss. $M1$ is chosen as 70 μm with 30 fingers for a minimum insertion loss of 1.7 dB at 45 GHz. Next, the shunt size is chosen based on the required isolation. The isolation improves with a wider shunt FET, however, the required shunt inductor to resonate out the equivalent capacitance of the FET in the off-state also increases at the expense of self-resonant frequency. A FET

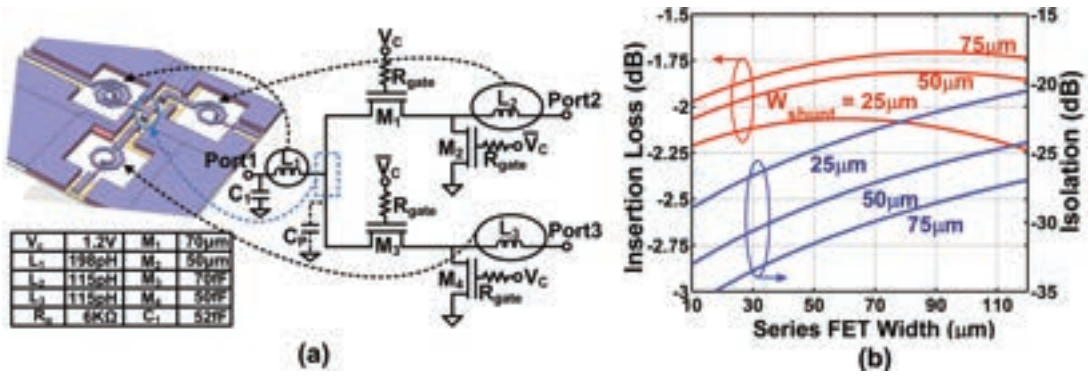

Figure 6.11: (a) The schematic of the SPDT switch with the associated spiral inductors/passives simulated with EM. (b) Optimization for series and shunt transistor width.

width of 50 μm (25 fingers) is chosen for an isolation of 25 dB as shown in Fig. 6.11 (a) and maintains more than 60 GHz of bandwidth.

The gate biasing resistor is an important parameter for determining the equivalent parasitics, switching speed, linearity, and insertion loss. The switching time is improved using a smaller value gate biasing resistor at the expense of a slight increase in loss as shown in Fig. 6.12. The switching speed of the SPDT switch is determined by the gate biasing resistor and the junction capacitance at the gate. The simulated switching time at 45 GHz is around 300 ps when R_{gate} is chosen as 6 $k\Omega$ as shown in Fig. 6.12. The power handling is also influenced by the choice of R_{gate} of the shunt FET. As is illustrated in Fig. 6.12, the one-dB compression is better than 7 dBm for R_{gate} over 1 $k\Omega$.

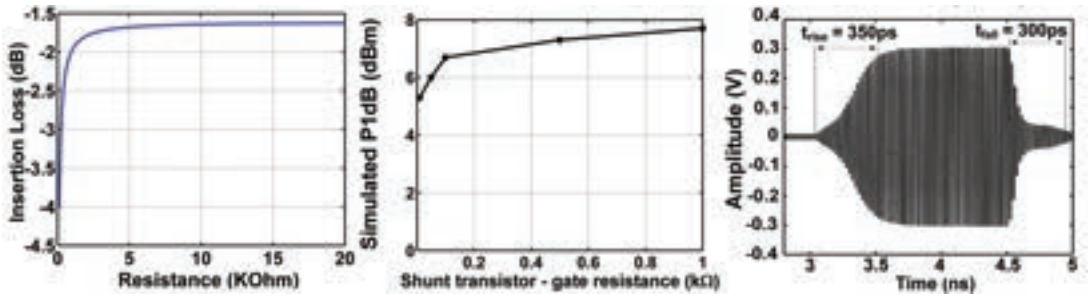

Figure 6.12: Effect of bias resistance on linearity, ins. loss and switching time.

6.3.2 Measurements

The SPDT switch is fabricated in a 45-nm SOI CMOS process and the chip microphotograph is shown in Fig. 6.13. The switch active area is 0.18 mm x 0.22 mm (0.04 mm^2), not including the pads.

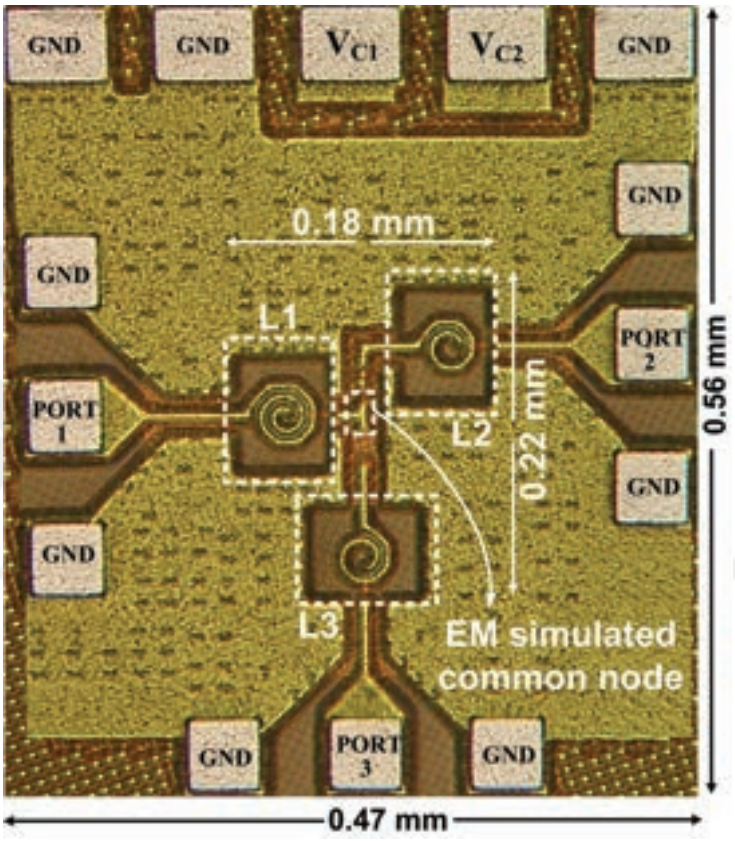

Figure 6.13: The chip microphotograph of the SPDT switch

S-parameter measurements were performed to 60 GHz using the 67 GHz Agilent E8361A PNA and 60 GHz RF probes. The SPDT results in an insertion loss of 1.7 dB at 45 GHz and less than 2.5 dB at 60 GHz with excellent input and output match as illustrated in Fig. 6.14 (a-b). The measured insertion loss and reflection coefficient are nearly identical for port 2 and port 3, showing the symmetry of the layout, and agreement with simulations. The measured isolation between the two output ports is better than 25 dB at 45 GHz as shown in Fig. 6.15 (a) and agrees with simulations. Fig. 6.15 (a) also compiles the measured insertion loss and isolation as a function of the control voltage at 45 GHz. The insertion loss and isolation changes 0.2 dB and 2 dB, respectively when

gate control voltage is varied from 0.9 V to 2.1 V.

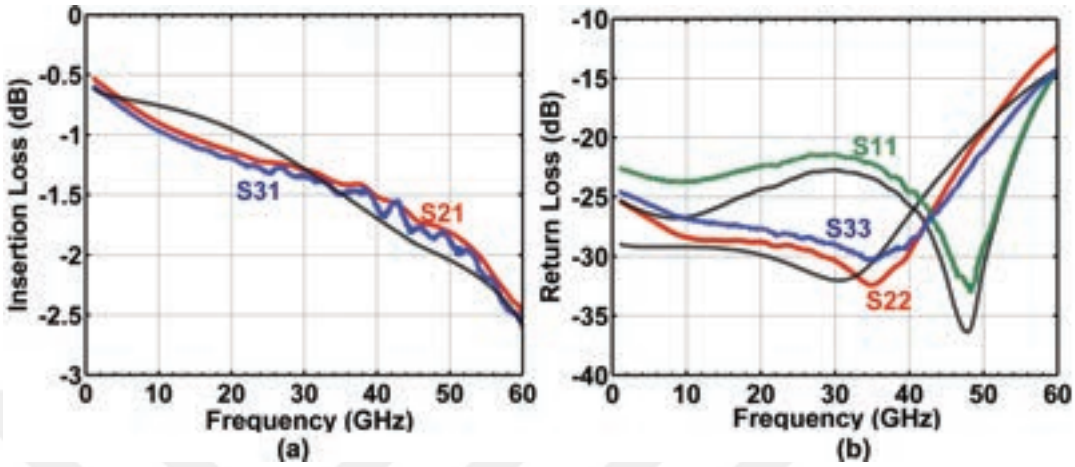

Figure 6.14: Measured (solid) and simulated (dashed) (a) insertion loss and (b) return losses.

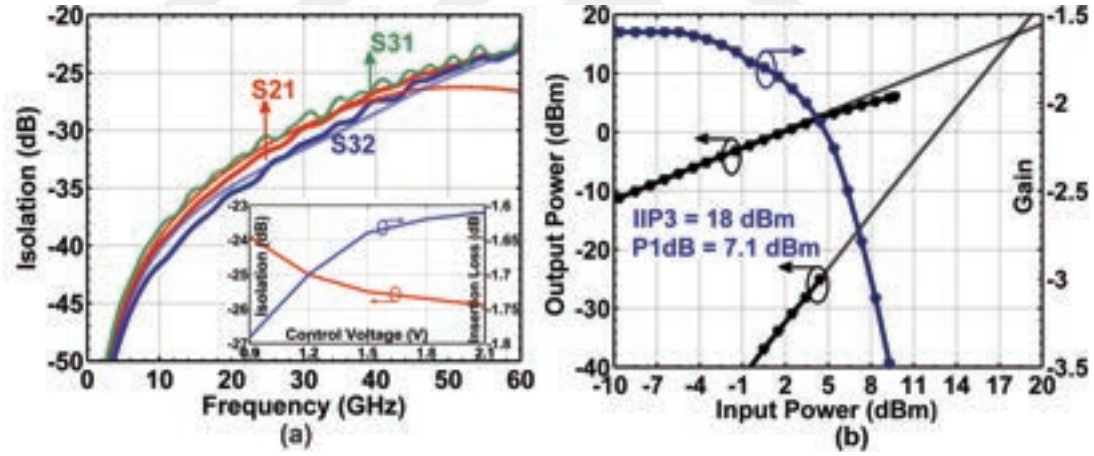

Figure 6.15: Measured (a) isolation and (b) output-input power characteristics of the SPDT switch.

The power handling capability was measured at 45 GHz using an Agilent E8257D signal source, an Agilent V8486A V-band power sensor and the results are also confirmed with the Agilent E4448A spectrum analyzer. As seen in Fig. 6.15 (b), the switch results in a P1dB of 7.1 dBm and an IIP3 of 18.2 dBm at 45 GHz. Table 6.1 presents the comparison of the 45-nm SOI SPDT switch design with other reported mm-wave SPDT switches indicating that this design offers similar bandwidth and lowest insertion loss compared to those implemented in bulk CMOS technologies.

Table 6.1: Comparison to reported switches

Ref.	Technology	Topology	Insertion Loss (dB)	Isolation (dB)	PO1dB (dBm)	BW (GHz)
[87]	130nm CMOS	series-shunt SPDT	2.4 @ 35 GHz	~31	~14	DC-35
[89]	180nm CMOS	series-shunt SPDT	2.5 @ 20 GHz	~25-32	~22	DC-20
[90]	180nm CMOS	distributed	6 @ 50 GHz	38	17.4	DC-50
[88]	130nm CMOS	series-shunt SP4T	3.1 @ 30 GHz	> 25	9	DC-30
[92]	130nm CMOS	series-shunt SP4T	3.5 @ 67 GHz	> 25	9-10	DC-70
[91]	90nm CMOS	transformer based	3.4 @ 50 GHz	13.7	14	40-55
[93]	65nm CMOS	shunt SPST	1.6 @ 94 GHz	30	> 9	DC-94
[83]	45nm SOI CMOS	distributed	5.3 @ 94 GHz	20.5	11	N/A
[94]	GaAs HJFET	series–shunt	1.64 @ 60 GHz	20.6	21	DC-60
[95]	GaAs pHEMT	shunt	1.8 @ 60GHz	40	N/A	55-65
[96]	PIN Diode	N/A	2 @ 58 GHz	> 27	25	36-84
[97]	MEMS	N/A	2.4 @ 35GHz	13	> 65 @ 1GHz *	DC-40
[98]	MEMS	series–shunt	0.34 @ 50GHz	15.5	N/A	35-60
This work [76]	45nm SOI CMOS	series-shunt	1.68 @ 45 GHz	> 25	7.1	DC- > 60

*: $IIP3$ =input referred intercept point

6.4 In-Phase/Quadrature Passive Mixer

An in-phase/quadrature (I/Q) mixer realize the highest linearity using passive (resistive) mixers as well as eliminating the 1/f noise contribution. The primary drawback of the passive mixer is high conversion loss. However, the FET channel resistance improves with device scaling and both resistive mixer conversion loss and noise figure improve due to the FET scaling, consequently.

Double-balanced mixers generally help eliminate the LO-to-RF and LO-to-IF feedthrough. Additionally, the double-balanced passive mixer is inherently bidirectional allowing the I/Q mixer to be used for both up-conversion and down-conversion. With the aim of reducing size and cost of the beamforming systems, a bidirectional amplifier and phase shifter is recently reported [35,76]. Sharing components between the transmit and receive paths greatly simplifies the implementation of phased arrays.

A simplified schematic and equivalent circuit of the balanced resistive ring mixer is presented in Fig. 6.16. When the gate voltage bias is below the threshold voltage, the switch is off and the channel resistance is high with a set of parasitic capacitances in parallel modeled as the impedance Z_{off}. When the switch is on, the impedance Z_{on} from is dominated by the channel resistance, R_{ch}, as presented in Section 6.3.

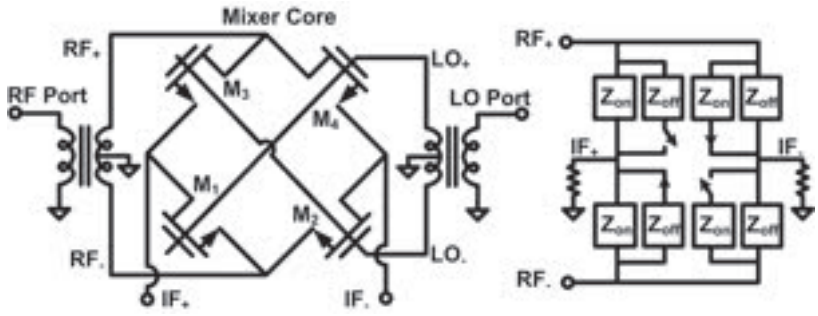

Figure 6.16: The model of the core of the double balanced mixer.

The bandwidth of the resistive mixer is basically controlled by the Z_{on} and the capacitance associated with it. Increasing the device size decreases the RF bandwidth because of the larger capacitance. On the other hand, decreasing the device size would be detrimental to the conversion loss. The ideal conversion loss of the double-balanced passive mixer is 3.9 dB neglecting many parasitic effects that affect the real transis-

tor and the interconnection networks. In the presence of finite channel resistance, the conversion gain is

$$G_c = 20\log_{10}\left(\frac{2}{\pi}\left(\frac{Z_L}{Z_L + Z_{on} \parallel Z_{off}} - \frac{Z_L}{Z_L + Z_{off}}.\right)\right) \tag{6.6}$$

A trade-off also exists between linearity, conversion loss, and matching. Wider FETs provide lower on-resistance, which improves conversion loss. However, increasing the FET width increases parasitic capacitance and contributes to worse linearity, port-to-port isolation and the requirement for higher LO power.

6.4.1 Circuit Design

The schematic of the quadrature mixer is illustrated in Fig. 6.17 along with the layout for inductors, baluns, and transmission lines.

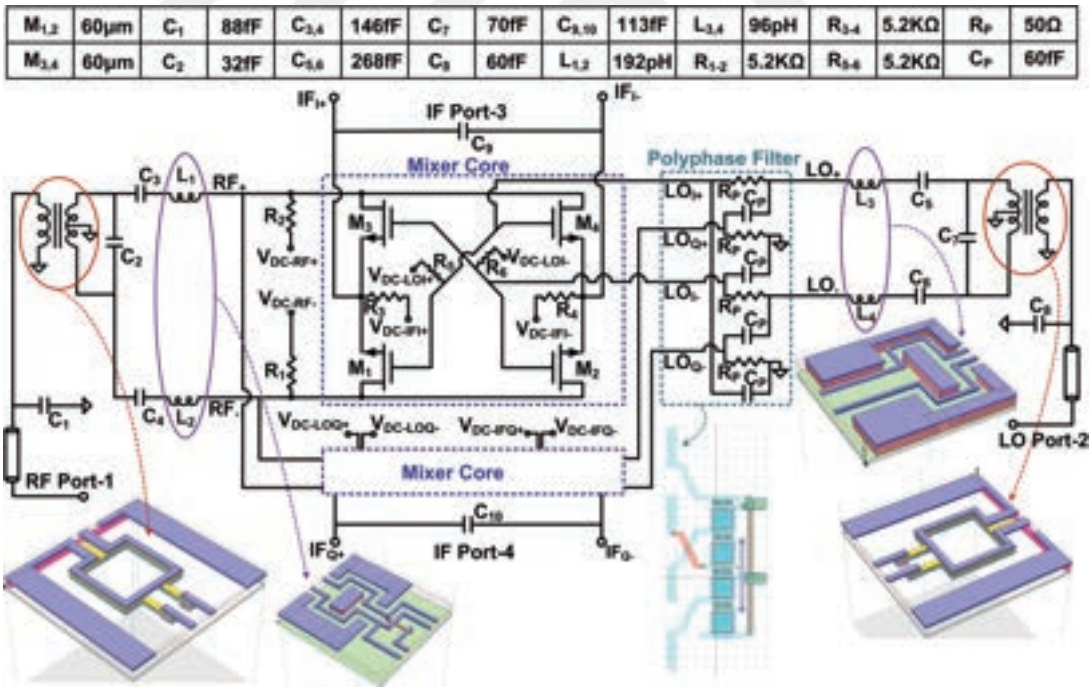

Figure 6.17: Circuit schematic of the I/Q passive resistive ring mixer and illustrating the associated passive models.

The LO signal of the mixer is used to pump the channel resistance of the FET. To reduce the conversion loss for moderate LO power, the gates of the mixing transistors,

M_1 - M_4, are biased near the threshold voltage with on-chip biasing. The transistor bias condition is crucial for mixer conversion gain and return losses of the RF and LO ports. The RF, IF and LO bias voltage should be set correctly to minimize the conversion loss. As shown in Fig. 6.17, the DC path at the drain, source and gate has been realized with resistors R_1, R_2 and R_3 of $6K\Omega$. Ten DC pads are placed in the final circuit to tune the passive mixer for minimum conversion loss, I/Q gain and phase mismatch and return losses.

The conversion loss contours is simulated with RF (IF) and LO bias voltage as shown in Fig. 6.18 (a). The minimum conversion loss occurs when difference in the DC bias across the LO and RF (IF) ports is set to 0.3 V, roughly the threshold of the floating body NFET.

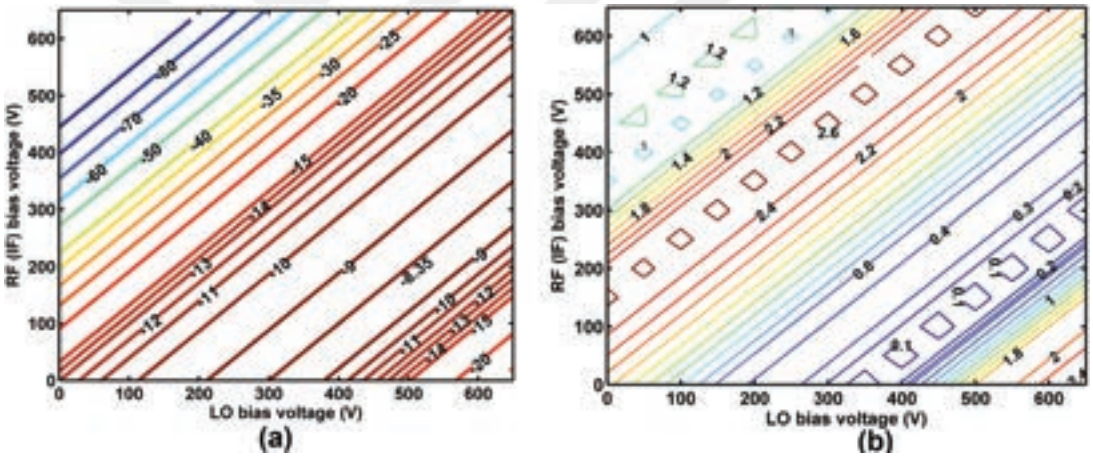

Figure 6.18: (a) Simulated conversion loss contours. (b) Simulated conversion loss I/Q mismatch contours.

Fig. 6.18 (b) shows that minimum conversion gain mismatch occurs when difference in the DC bias across the LO and RF (IF) ports is set to 0.35 V and the respective DC bias is kept same both for in-phase and quadrature mixers.

Differential Generation

Single-ended to differential conversion is provided at the RF and LO ports of the mixer with a passive balun. The IF port is differential to allow homodyne mixing. The IF signals are fed to the pads through CPW-line from the center of the chip. The passive

balun is shown in Fig. 6.19 (a). The minimum imbalance is achieved when port 1 and port 2 or 3 are oriented to the west and east, respectively. For a balun with a primary or a secondary inductor with more than one turn, a gain and phase imbalance cannot be avoided [55].

The spiral balun has a one-turn primary square inductor, built using the top metal layer LB, and the secondary coil composed of stacked UB and UA metals as shown in Fig. 6.19 (a). The grounded nodes are connected to the UB layer through vias. The magnetic coupling occurs vertically between the primary and secondary coil. The distance to the ground plane is 17 μm on each side and the trace width is 5 μm. The thickness between the metal layers LB and UB is 3.3 μm and determines the resonant frequency of the balun. The core balun has a size of 5 μm and 56 μm and has a resonant frequency of 128 GHz for 3 ports terminated into $50\ \Omega$. The frequency response of the balun for RF and LO ports including the matching capacitor is shown in Fig. 6.19 (a). The balun has a gain imbalance of 0.3 dB and a phase imbalance of 1.5° at 45 GHz.

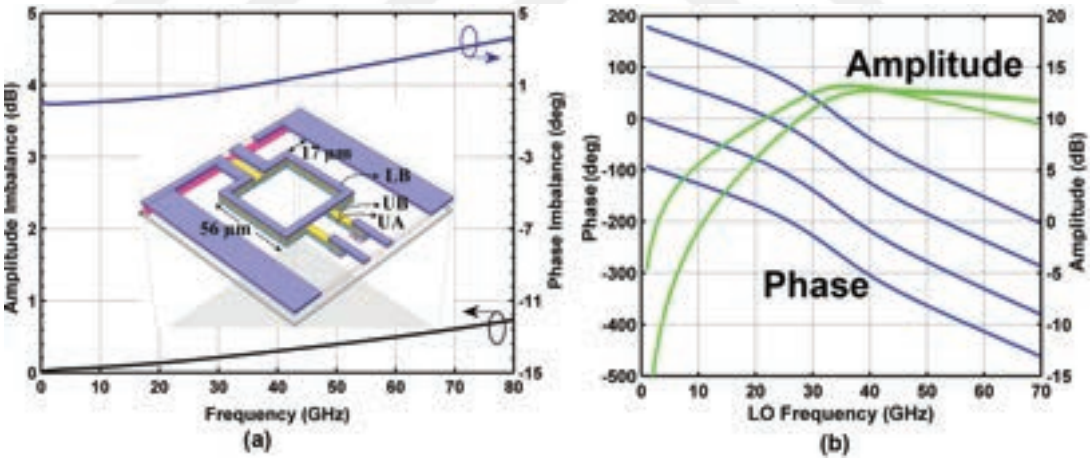

Figure 6.19: (a) Illustration of the balun amplitude/phase imbalance (b) In-phase / quadrature output signals of the polyphase filter.

Quadrature Generation

Quadrature LO generation is based on a *RC* polyphase filter, which is satisfactory for the bandwidth required in this application. There are basically two options for I/Q signal generation. The RC filter can be designed for accurate amplitude balance

over a wideband, but the correct quadrature phase relationship occurs only at the center frequency. Alternatively, the phase relationship can be wideband at the expense of amplitude balance.

Final optimization of the polyphase filter component values and physical size was based on simulations of the extracted layout as illustrated in Fig. 6.19 (b). The filter resistor values are chosen to be $R_1 = 50\,\Omega$ (two p+ doped polysilicon resistors in parallel), leading to a required capacitor of $C_1 = 70$ fF (vertical natural capacitors) at the filter resonance frequency $f_{PPF} = 1/2\pi RC$ = 45 GHz. With increasing frequency additional effects have to be considered such as parasitic capacitances of the filter resistors, the interconnect inductance and the finite Q of the filter capacitors. The simulated transfer loss due to polyphase filter is 3.3 dB at 45 GHz and the maximum absolute gain variation is 0.2 dB from 40 to 50 GHz which restricts the LO signal to be relatively narrowband. Multi-stage polyphase circuits remedy the situation at the expense of additional insertion loss.

Fig. 6.19 (b) shows the phase and amplitude at the outputs of the polyphase filter. Because of the lossy passive components, the insertion loss of the LO input network is around 7 dB and LO power delivered to the mixer is less than 14 dBm when a LO signal of 20 dB is applied at the LO port. To drive the mixer in the test setup, a *Q*-band amplifier is placed at the LO port to generate enough LO power. To maximize the LO swing at the outputs of the polyphase, using LO buffers is an option however the current consumption of the LO buffers significantly contributes to the RF front-end power budget. Therefore they are not preferred.

Matching Networks

A multistage, π network at the RF input is formed from a 88 fF shunt capacitor, C_1 at the input, the RF balun, a 32 fF differential capacitor, C_2 at the balun output and 146 f F series capacitors, C_{3-4}. Similarly the LO matching network is formed with a 60 f F shunt capacitor, C_8 , the LO balun, a 70 f F differential capacitor, C_7, and 268 f F series capacitors, C_{5-6}. Resonant elements are not included for matching at the IF output port. To attenuate the high frequency LO and RF signal, capacitors C_9 and C_{10} have been added to the IF outputs to provide a low impedance path to ground for the

input RF and LO signals at higher operation frequencies. Additionally, wideband on-chip bypass networks composed of a 5 Ω polysilicon resistor in series with 0.6–2 pF thick-oxide capacitor banks have been connected to the power supply lines to clean the DC voltages.

6.4.2 Measurements

The chip microphotograph of the passive resistive ring mixer chip is shown in Fig. 6.20. The area excluding the RF and DC pads is 0.18 mm x 0.22 mm (~0.40 mm^2).

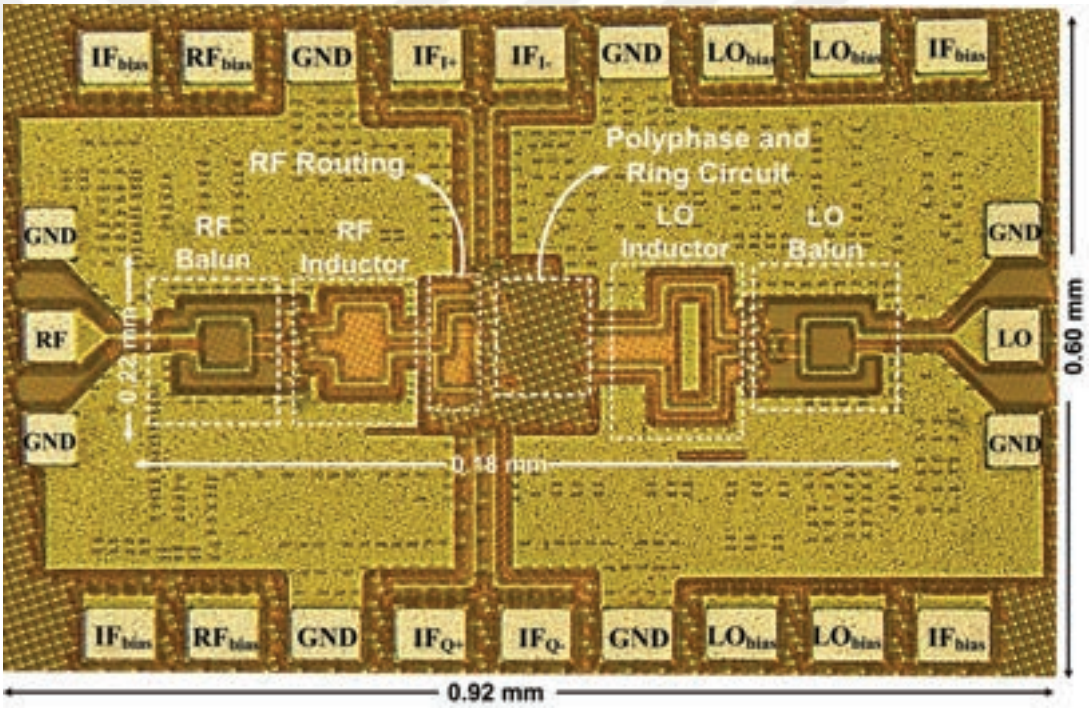

Figure 6.20: The chip microphotograph of the mixer.

S-parameters are measured on-wafer with the Agilent E8361A network analyzer. The RF and LO signals are provided via GGB Model 50A ground-signal-ground (GSG) probes. The RF and LO input signals are generated by two Agilent E8257D signal generators. The RF signal at the *Q*-band is downconverted to an I/Q IF with a maximum bandwidth of 250 MHz via the LO quadrature signals generated by the polyphase filter and the quadrature mixers. An off-chip balun is used to combine the IF differential signals.

The measured and simulated return losses of the LO and RF ports are shown in Fig. 6.21. External pads for the DC biasing of LO, RF, and IF ports are placed on chip to alter the matching of the RF and LO ports, if necessary. Fig. 6.21 shows the return losses when $V_{BIAS-LO}$ and $V_{BIAS-RF}$ ($V_{BIAS-IF}$) are 300 mV and 0 V, respectively. The bias is altered to improve the RF return loss. The RF matching gets better and LO matching remains unchanged when $V_{BIAS-LO}$ and $V_{BIAS-RF}$ ($V_{BIAS-IF}$) are altered to 650 mV and 300 mV, respectively as shown in Fig. 6.21. Fig. 6.21 also shows the sensitivity of the return losses to the LO and RF/IF bias voltages. The measured return loss of the RF and LO port is better than 14 dB and 32 dB at 45 GHz.

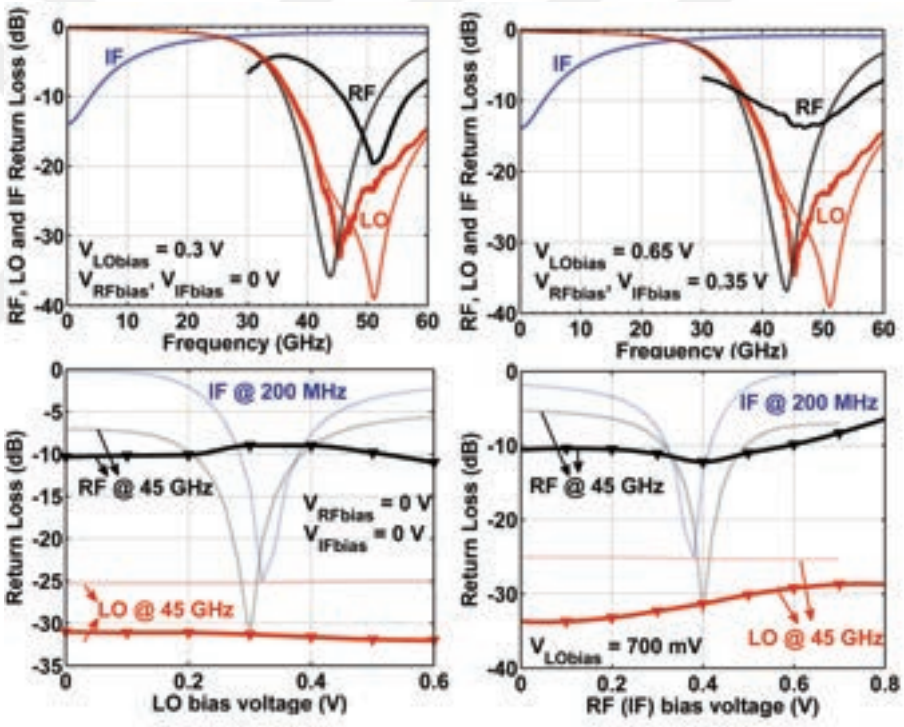

Figure 6.21: Measured (solid) and simulated (dashed) RF/LO/IF port return loss with various voltage control

The simulation and measurement of conversion gain versus LO input power is presented in Fig. 6.22. Measurement and simulations show that LO power of 10 dBm is sufficient to achieve within 1 dB of the minimum conversion loss.

As illustrated in Fig. 6.23 (a), when the LO frequency is fixed at 43.4 GHz, the conversion gain versus IF frequency is measured while the RF frequency is varied from

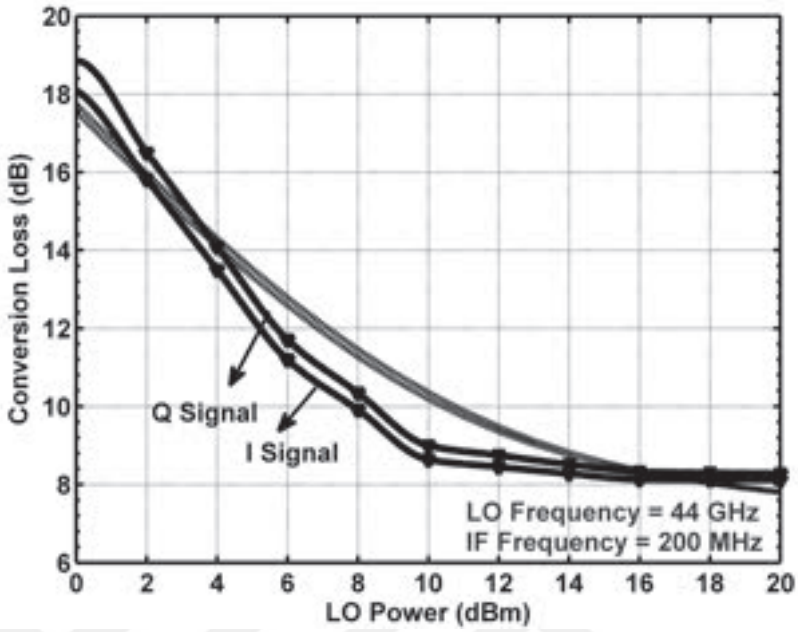

Figure 6.22: Measured (solid) and simulated (dashed) conversion loss versus LO power.

43.4 GHz to 43.65 GHz. Measurement and simulations show that the gain and phase imbalance increases, when the IF frequency is increased. To determine the gain and phase imbalance, the IF frequency is fixed at 200 MHz and the RF frequency is varied from 40 to 50 GHz and LO frequency is varied from 39.8 to 49.8 GHz as both the I and the Q signals are down-converted. The conversion gain and gain/phase mismatch of the I/Q path is shown in Fig. 6.23 (b). The I/Q balance is measured by comparing the IF using the Agilent DSO80604B oscilloscope. The peak conversion loss of one channel is 8.35 dB when the LO and RF frequency is fixed at 43.4 GHz and 43.6 GHz. The minimum gain and minimum phase imbalance of 2° occurs at 43.5 GHz and 45 GHz, respectively.

Small gain and phase imbalances are compensated by independently altering the ten DC voltage biases of the in-phase and quadrature mixers without significant impact on the conversion gain of the mixer. Fig. 6.24 (a) shows that zero loss imbalance occurs when the difference in the DC bias across the LO and RF (IF) ports of the I and Q mixers is set respectively to 0.35 V and 0.31 V. However phase imbalance degrades and further optimization provides the minimum I/Q gain and phase imbalance at the same time and is found as 0.25 dB and 1.9°, respectively.

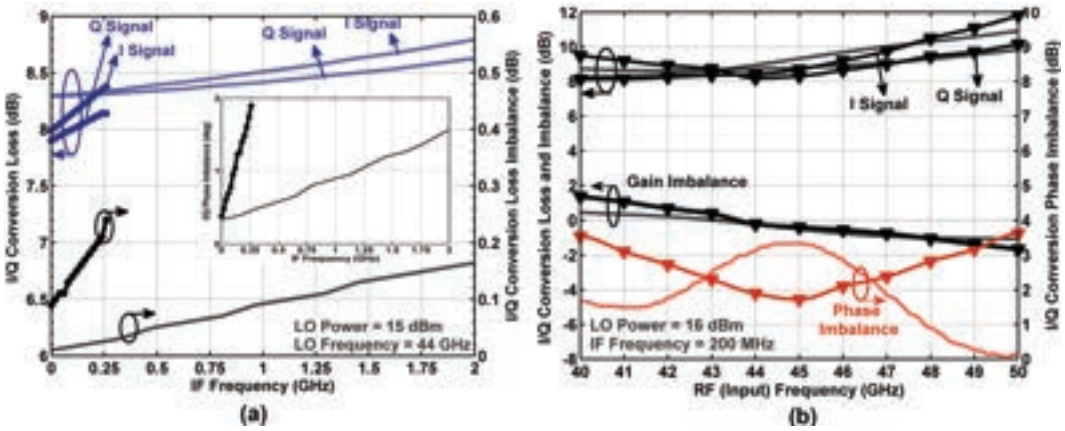

Figure 6.23: (a) Measured (solid) and simulated (dashed) conversion loss and gain and phase imbalance with fixed LO frequency. (b) Measured (solid) and simulated (dashed) conversion gain/phase imbalance of the mixer with fixed IF frequency of 200 MHz.

As shown in Fig. 6.24 (b), the power handling capability was measured using an Agilent E8257D signal source, an Agilent V8486A V-band power sensor and the results are also confirmed with the Agilent E4448A spectrum analyzer.

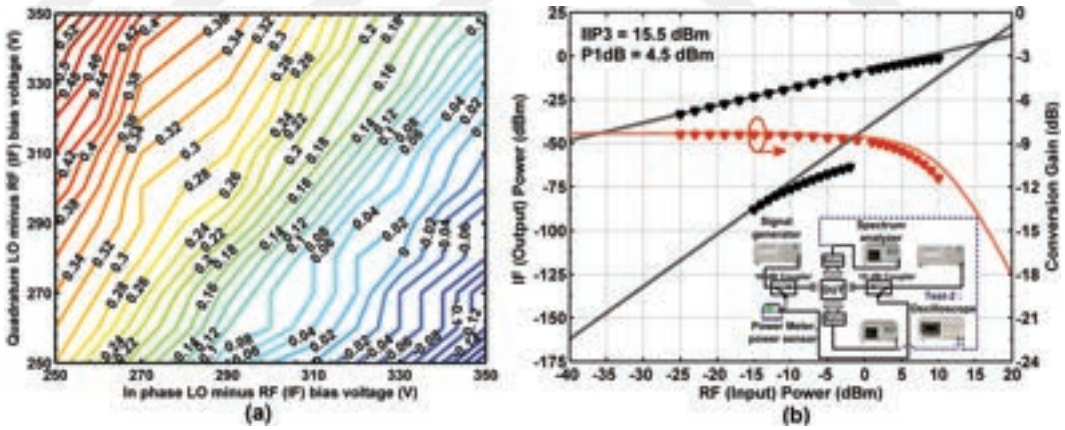

Figure 6.24: (a) Measured conversion loss I/Q mismatch contours with independent in-phase DC biases, $V_{BIAS-LO,RF,IF}$, and quadrature DC biases, $V_{BIAS-LO,RF,IF}$. (b) Measured (solid) and simulated (dashed) input-output power characteristics and associated set-up.

The RF and LO frequency are 43.3 GHz and 43.1 GHz, respectively. The mixer results in a gain compression point (P1dB) of 4.5 dBm at 43.3 GHz as shown in Fig. 6.24 (b). Finally, the third-order intermodulation products are measured at two tones at 43.20 GHz and 43.22 GHz (spaced by 20 MHz). The extrapolated intermodulation

intercept point (IIP3) is +15.5 dBm as illustrated in Fig. 6.24 (b).

The isolation between the ports LO-RF and RF-LO is simulated and measured. LO suppression at RF (LO-RF isolation) is simulated and measured as 66.5 dB and 49 dB. The measured port-to-port isolation at LO port for the RF feed through is better than 65 dB at the center frequency of 44 GHz. The LO-IF and RF-IF isolation is not measured due to the probe limitations mentioned before. The LO-IF and RF-IF isolation is simulated and found as 68 dB and 48 dB, respectively.

Table 6.2 presents a comparison of reported mm-wave mixers. Most prior work does not provide results discussing gain and phase mismatch. In this table, wideband performance mixers are presented by [99–101]. Ref. [101] provides very wide operation bandwidth and good conversion efficiency, however LO-RF isolation is poor due to the distributed structure of the mixer. Good performance passive mixers in SOI is demonstrated in [79, 81]. A compact mixer compared to the previously reported star mixers, which is due to the novel balun structures is proposed in [102–104]. This design is the first millimeter-wave I/Q passive mixer in SOI and offers very low insertion loss and high LO-RF isolation at satellite bands.

Table 6.2: Comparison to reported mixers

Ref.	Tech.	Topology	LO Power (dBm)	BW (GHz)	Conv. Loss (dB)	LO-RF Isolation (dB)	LO-IF Isolation (dB)	Input P1dB (dBm)
[79]	90nm CMOS	Drain-pumped	7.5	30-40	4.6	11	45	-6
[81]	90nm CMOS	Gate-pumped	0	26.5-30	10.3	24	22	N/A
[99]	180nm CMOS	Resistive ring	9	1-11	7.5 ± 0.5	37+1	N/A	4-6
[100]	130nm CMOS	Resistive ring	10	15-50	15.5 ± 1.5	> 35	> 40	5-10
[101]	130nm CMOS	Passive distributed drain	10	0.8-77.5	5.5 ± 1	> 10	N/A	-4 @ 20GHz
[105]	180nm SiGe	Single-balanced	3	22-39	> 10	15-40	40-60	-1.5
[102]	150nm GaAs	Resistive Star	7	25-55	11± 2	> 25	> 30	5
[102]	130nm CMOS	Resistive Star	7	25-45	12± 2	> 30	> 30	5
[103]	150nm GaAs	Diode	12.5	46-78	9 ± 1	> 20	N/A	N/A
[104]	130nm CMOS	Diode	11	16-46	13 ± 1.5	> 20	> 37	4
This work [74]	45nm SOI CMOS	I/Q Resistive ring	15	40-50	8.35	> 49	N/A	4.5

6.5 Low Noise Amplifier

At millimeter-wave bands, III-V devices tend to offer excellent low-noise behavior. However, CMOS technology scaling tends to increase NFET f_T and improve the sensitivity of CMOS LNAs. Q-band LNAs have been demonstrated using 130 nm, 90 nm, and 65 nm CMOS processes [78, 106–110]. A source resistance R_S is matched to the LNA with a combination of inductive source degeneration and gate inductance. At a center frequency f_o, the conventional common-source LNA has a noise factor defined by

$$F = 1 + \frac{2\pi f_o L_{g1}}{R_S Q_{g1}} + \frac{r_g}{R_S} + \gamma g_{do} R_S \left(\frac{f_o}{f_T}\right)^2 \tag{6.7}$$

where Q_{g1} is the quality factor of the gate inductance L_{g1}, r_g is the gate resistance, γ is the short channel excess noise factor, and g_{do} is the channel conductance. Degradation of the F arises from the lower quality factor of the gate inductor Q_{g1} and the low ratio of the center frequency f_o to f_T. The 45-nm SOI CMOS process offers a higher f_T but Q_{g1} is slightly lower relative to the transistor improvement.

The minimum noise factor and f_T for the common source and cascode devices is simulated for the 45-nm SOI CMOS process as shown in Fig. 6.25 (a). The gate resistance strongly depends on the FET layout due to the thin metallization. Additionally, metal-metal and metal-poly parasitic capacitances reduce the actual f_T and f_{max}. The f_{max} of the native model drops significantly from a predicted value of roughly 480 GHz. For example, a cascode structure reduces f_T from 200 GHz to 140 GHz once the interconnect parasitics are taken into account. Accurate modeling of r_g is critical for FET gain and stability. All of the metal and polysilicon layers at the FET gate and drain are extracted up to M2 using an RC parasitic extraction tool [111]. The source is extracted up to the surrounding M1 ground plane. Several blocks of stacked vias are used to connect the top level grounds (LB and B3 layers).

The minimum noise figure for the cascode structure is predicted to be around 0.9 dB. When the circuit model considers extraction, the optimum drain current density for minimum noise factor of the cascode stays the same and is around 0.21 mA/μm. The peak f_T for the cascode structure occurs for a device current density of 0.65 mA/μm. Notably, the f_T at the drain current density for minimum noise factor is 120 GHz - about

15% lower than the peak f_T as shown in Fig. 6.25 (a).

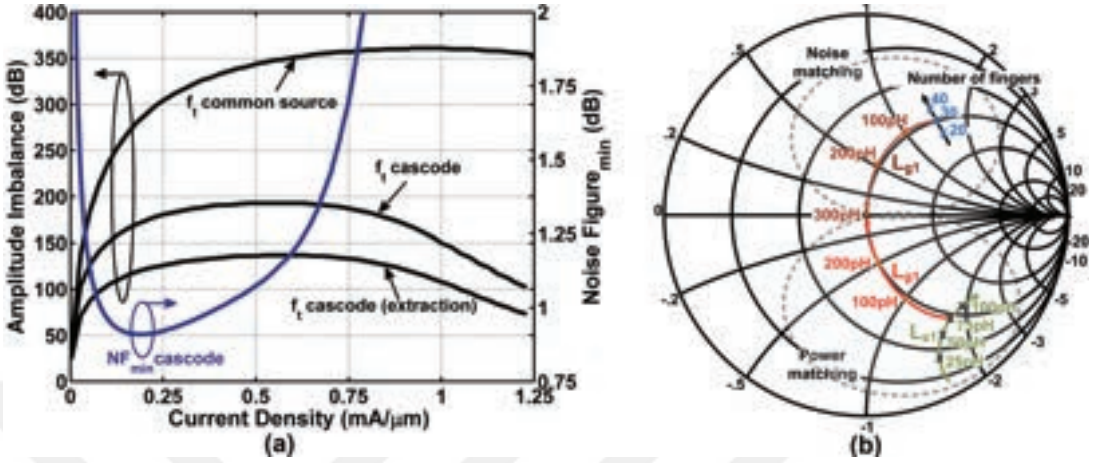

Figure 6.25: (a) The optimum drain current density for minimum noise factor and gain with f_T degradation curves. (b) Simultaneous noise and power matching illustrated on Smith chart.

6.5.1 Circuit Design

The *Q*-band LNA is a two-stage cascode design and is shown in Fig. 6.26. To improve the gain and isolation, the cascode is used for each stage and does not substantially degrade the noise figure. The geometry of the first stage common source device, M_1 , is chosen to provide simultaneous impedance and noise matching as shown in Fig. 6.25 (b).

First, a FET width of 40 μm is chosen to allow simultaneous impedance and noise matching. Next, the number of FET fingers is chosen to set the real part of the optimum noise impedance to the source impedance at 45 GHz. The drain current and gate voltage that minimizes the noise figure is 8 mA and 570 mV for a 40 μm wide device split between 32 fingers, where each finger has a current density of 0.2 mA/μm. A shorted stub is used at the source of the first-stage FET and acts as a degeneration inductor and increases the real part of the impedance seen at the gate. By adding the source inductance L_{s1} , the real part of the input impedance is transformed to $R_s = r_g + \omega_T L_{s1}$, where r_g is the gate resistance and a wideband input impedance is achieved when combined with the low-Q matching sections at the input S_{11} < -20 dB at 40–60

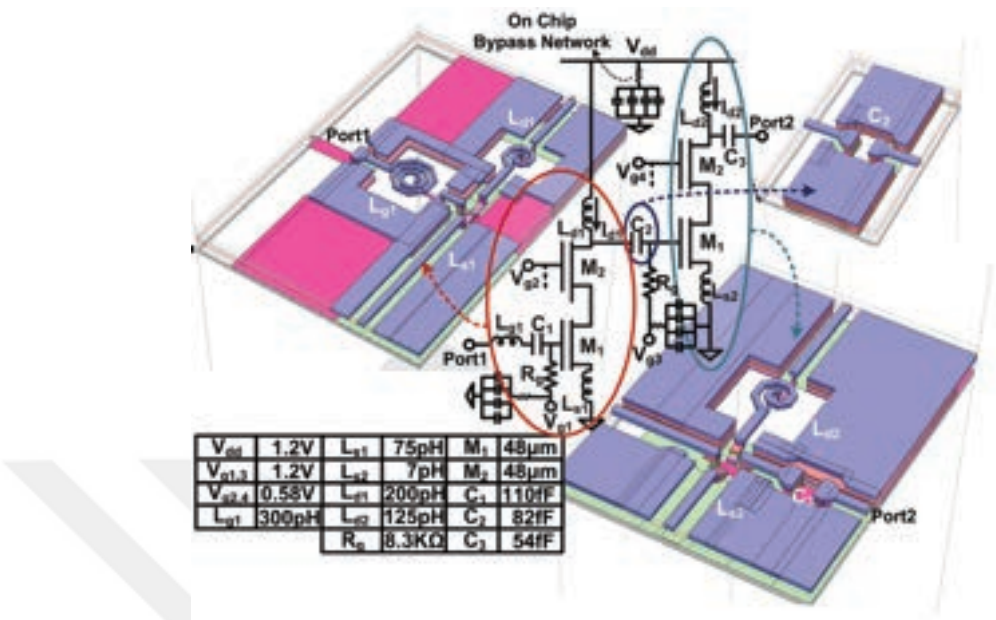

Figure 6.26: Schematic of the two-stage low noise amplifier and the associated passives.

GHz. The source degeneration increases the input resistance of the device according to $\omega_T L_{s1}$. The reactive part of the input matching is provided with the gate inductor L_{g1} according to $\omega_o\left(L_{g1}+L_{s1}\right)$=$\left(\omega_o C_{gs1}\right)^{-1}$. Γ_{opt} at the input of the first stage moves toward the 50 Ω-region on the Smith chart with the gate inductor L_{g1} and results in a simultaneous gain and noise figure match.

For the chosen width of *M1*, the gate capacitance is determined to be $C_{g,1}=34$ fF and suggests that the total inductance of L_{g1} and L_{s1} should be around 375 pH at 45 GHz. Larger source degeneration inductors also improve the amplifier linearity. To achieve high quality factor, the source degeneration inductors are implemented with grounded CPW lines that are 8 μm wide and spaced 13 μm from the side shield. The CPW line has a loss of 1.2 dB/mm and a Q of 15 at 40–50 GHz.

The second stage consumes 11 mA. The device size and current density for the second stage transistor is 40x1.25 μm and 0.25 mA/μm for high output power, respectively. The output capacitance and the output inductance is respectively $C_{d,2}=34fF$ and $L_{g1}=183pH$.

Wideband on-chip bypass networks, composed of a 5 Ω polysilicon resistor in series with 0.6–2 pF thick oxide capacitor banks, are implemented and connected to the

power supply lines to prevent any oscillations. Also, a 2 Ω resistor is placed in series with the second stage drain matching inductor to further improve the stability. The gate biasing is done by using 5 kΩ resistors.

6.5.2 Measurements

The chip microphotograph of the LNA is shown in Fig. 6.27. The area including the RF and DC pads is 0.6 mm x 0.58 mm (0.35 mm^2) and 0.14mm^2 without the pads. The two-stage LNA draws 19 mA from 1.2 V supply voltage. The power consumption including the biasing is 25 mW.

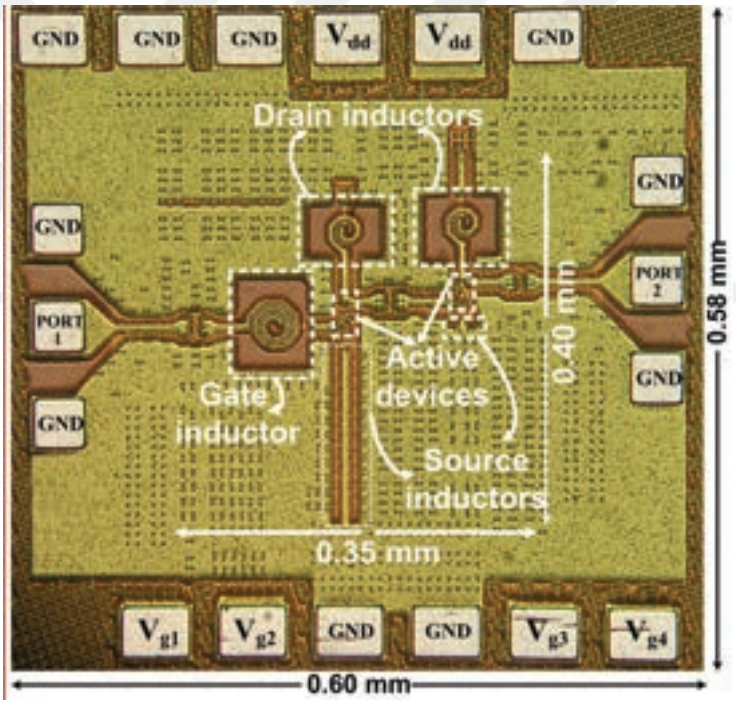

Figure 6.27: The chip microphotograph of *Q*-band LNA.

The LNA *S*-parameters are probed with the Agilent E8364B network analyzer using SOLT calibration to the probe tips and is plotted in Fig. 6.28 (a). Measurement over 2 different chips shows stable performances over process variations. The measured peak gain is 18.5 dB and the measured input and output return losses are better than 15 dB at 48 GHz. The 3-dB bandwidth is 10 GHz from 43 to 53 GHz. The measured gain is greater than 10 dB and the input return loss is greater than 6 dB between 40 and 60

GHz. When simulation and measurement results are compared, the peak gain shifts by 10% (4 GHz) presumably due to the mismodeled drain inductance of the first stage.

The noise figure of the LNA is measured using Agilent 346CK01 noise source, Agilent E4448A spectrum analyzer and a *Q*-band preamplifier. The noise figure is measured from 40 to 50 GHz since the noise source and preamplifier operates up to 50 GHz. As shown in Fig. 6.28 (b), the minimum noise figure is 2.9 dB at 47 GHz but remains under 4 dB over the 40 to 50 GHz band.

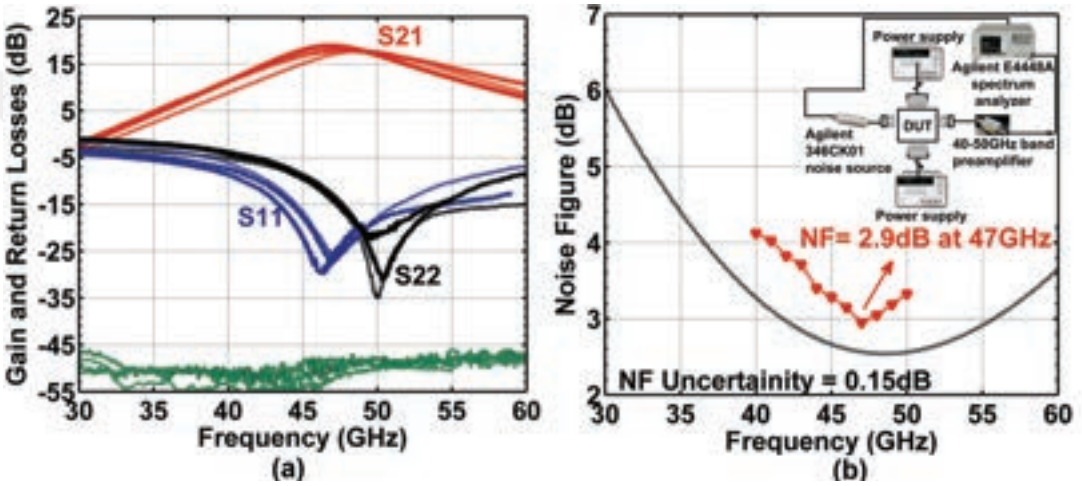

Figure 6.28: Measured (solid) and simulated (dashed) (a) gain, return loss and (b) noise figure.

The large signal measurements of the LNA are illustrated in Fig. 6.29. The mea-

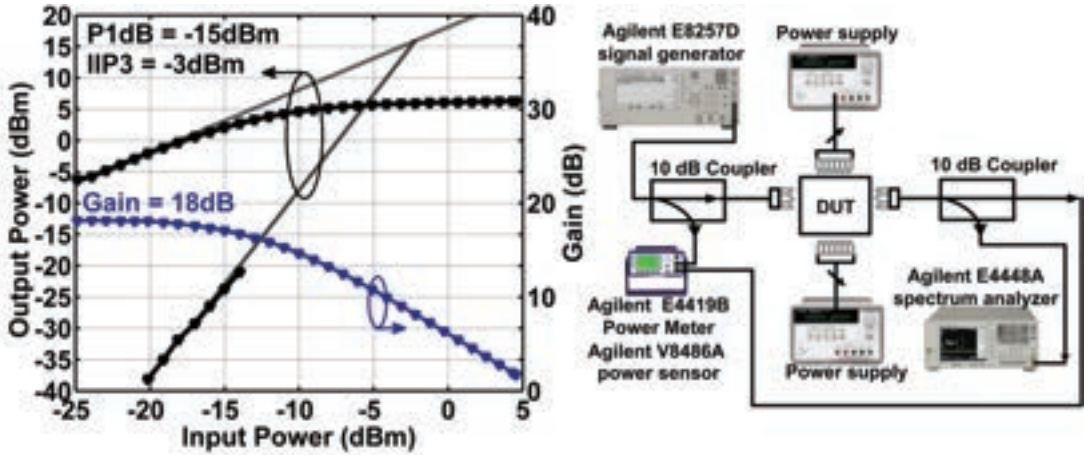

Figure 6.29: Input-output power characteristics of the LNA and associated test set-up.

sured 1 dB gain compression point (P1dB) at 48 GHz is -14.5 dBm and 3 dBm at the input and output ports, respectively. Finally, the third-order intermodulation products are measured at two tones at 48 GHz spaced by 50 MHz. The extrapolated intermodulation intercept point (IIP3) is -3 dBm and +15.5 dBm at the input and output ports. Large signal measurements verify a saturated power of 7 dBm. Fig. 6.29 also shows the test set-up for the large-signal measurements. Careful and repeatable calibration of test setup losses is necessary for accurate power measurement. The large-signal characterization is made using an Agilent E8257D spectrum analyzer and Agilent E4419B power meter with 8486A power sensor. The spectrum analyzer is used to observe potential oscillations under large-signal conditions. An Agilent 10-dB directional coupler (AG 87301) at the input is used to sense the input. To ensure the circuit is not exhibiting any oscillation, another 10-dB directional coupler is used at the output node to feed an Agilent E8257D power spectrum analyzer (PSA). Probe losses are calibrated from a CS-5 calibration substrate at 0.4 dB at 45 GHz.

Table 6.3 presents a summary of *Q*-band CMOS amplifiers. It is seen that the 45-nm SOI CMOS technology results in the lowest NF, highest FOM and high linearity, gain and saturated output power values and best figure of merit in silicon technologies. Compared to the 90 nm SOI process, the proposed LNA doubles the FOM at a similar frequency of operation and is comparable with the best SiGe results.

Table 6.3: Comparison to reported LNAs

Ref.	Technology	Topology	Peak Gain (dB)	Minimum NF (dB)	PO1dB (dBm)	OIP3 (dBm)	Power Dissipation (mW)	FOM*
[106]	130nm CMOS	** 3 stage	19 @ 40 GHz	N/A	-0.9	N/A	36	N/A
[107]	130nm CMOS	** 1 stage triple	14.3 @ 38 GHz	3.8	-6	4	28.8	0.062
[108]	120nm SOI	** 2 stage	14 @ 40 GHz	3.6	N/A	N/A	19.2	N/A
[109]	120nm SiGe	** 2 stage	23.5 @ 34 GHz	2.9	-6	4	11	0.024
[78]	90nm SOI	** 1 stage	11.9 @ 35 GHz	3.6	4	14	40	0.049
[110]	65nm CMOS	** 2 stage	14.3 @ 42 GHz	6	6	N/A	43.2	0.031
[112]	150nm GaAs	3 stage	19 @ 42 GHz	3.1	N/A	28	400	0.1514
[113]	150nm GaAs	N/A	11 @ 44 GHz	3.5	N/A	N/A	N/A	N/A
This work [75]	45nm SOI	** 2 stage	18.5 @ 48 GHz	2.9	3	15.5	22.8	0.0921

*: $FOM = [G/(F-1)]\, x\, [P_{in-1dB}/P_{dc}]$ **: $cascode$

6.6 Conclusion

This chapter presents the design and the measurement of millimeter-wave integrated circuits implemented in a 45-nm CMOS silicon-on-insulator (SOI) process. The technology provides higher f_t than other CMOS processes and allows the substrate isolation, therefore 45-nm CMOS is an excellent candidate for millimeter-wave low-noise amplifiers and passive circuits - SPDT switches and ring mixers. Electromagnetic simulations were extensively used to model the high frequency behavior of any passive components such as the conventional CPW-line, grounded stubs, inductors, and baluns. First, a single pole double throw (SPDT) switch demonstrates a measured insertion loss of less than 1.7 dB at 45 GHz and IIP3 of 18.2 dBm. Second, a double-balanced passive I/Q mixer exhibits a conversion loss of 8.35 dB at 44 GHz and IIP3 of 15.5 dBm. At a fixed IF of 200 MHz, the minimum I/Q gain and phase imbalance is 0.25 dB and 1.9°. Finally, a low noise amplifier (LNA) is designed with simultaneous noise and input power matching and shows a noise figure of 2.9 dB at 47 GHz. The output P_{1dB} compression power is 3 dBm.

6.7 Acknowledgement

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1. M. Parlak and J. F. Buckwalter,"Passive Millimeter-wave Circuits in 45-nm SOI Technology", *in preparation for publication to IEEE Transactions on Microwave Theory and Techniques*.

2. M. Parlak and J. F. Buckwalter, "A 2.5-dB Insertion Loss, DC-60 GHz CMOS SPDT Switch in 45-nm SOI" *IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Oct. 2011.

3. M. Parlak and J. F. Buckwalter, "A 2.9-dB Noise Figure, *Q*-Band Millimeter-Wave CMOS SOI LNA", *IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2011.

The dissertation author was the primary author of this material.

Chapter 7

Second Generation, Future Research and Summary

This dissertation presented several new architectures and integrated circuits in silicon processes for the realization of low cost and low power wireless beamforming transceivers for pedestrian detection imaging radar systems. The bidirectional beamforming and analog signal processing circuits and architectures presented exploit the benefits of silicon integration to ease the area and power requirements of radar systems and enhance their functionality. Multiple-antenna transceivers integrated with these subsystems and circuits will play a key role in the success of emerging commercial radar applications such as pedestrian detection, indoor/outdoor surveillance, automotive radar and millimeter-wave imaging.

This chapter concludes the dissertation by presenting the second generation PCR chip and topics for future research. Second generation baseband/analog signal processing radar-on-chip is briefly presented in Section 7.1. The topics for future research are explained in Section 7.2. The dissertation is summarized in Section 7.3. The relevant papers and patents relevant to this dissertation are summarized in Section 7.4.

7.1 Second Generation Baseband/Analog Signal Processing

As described in Chapter 6, the sweep of the template signals in time is provided via registers in the FPGA. And digitization is provided with a comparator instead of a 4-bit analog-to-digital converter (ADC) for the sake of simplicity. For the second generation prototype, the DLL and ADC is integrated into the circuit for the on-chip synchronization and digitization of baseband analog signal processing system as shown in Section 7.1 and Section 7.1, respectively. Fig. 7.1 shows the die photomicrograph of the next generation PCR with on-chip synchronization and digitization. The use of the FPGA is minimized owing to the on-chip synchronization and digitization. The system is implemented in a 90-nm CMOS process. The chip has an area of 1.8 mm x 1.8 mm ($3.24mm^2$) including the pads.

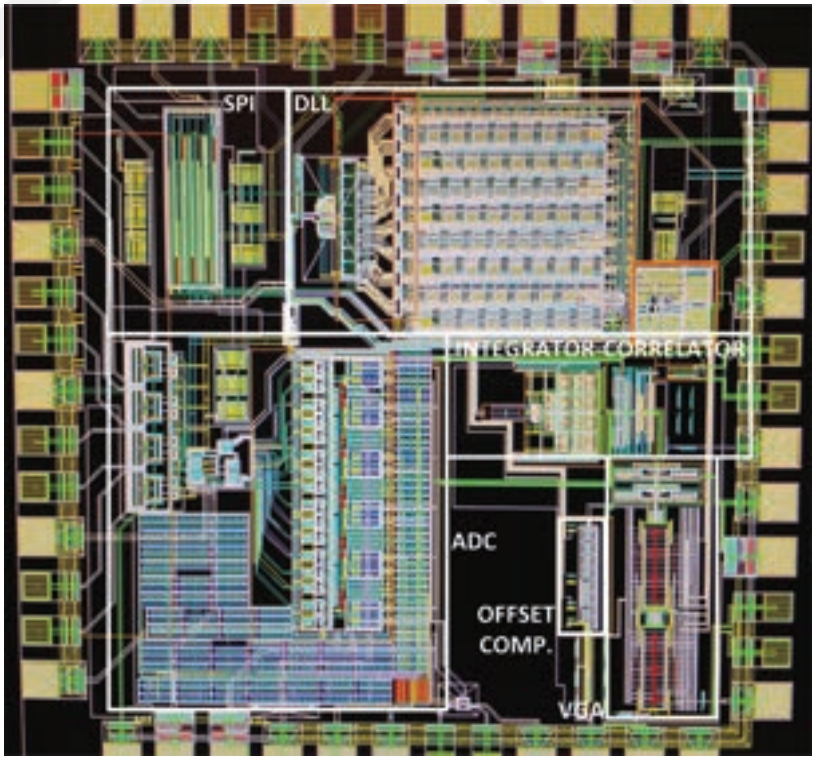

Figure 7.1: The die photomicrograph of the next generation PCR with on-chip synchronization (with DLL) and digitization (with ADC).

7.1.1 Synchronization

Instead of using a FPGA, the timing circuit is proposed to be on-chip - a 16-phase delay lock loop (DLL) integrated into the chip. The proposed architecture should be adaptive to provide a wide range of range resolution achievable. Therefore the synchronization circuit should have wide working range besides providing precise multi-phase clock. That means the DLL should have wide tuning range to provide a reconfigurable pulse width.

For low power and low complexity design, a multiplying type DLL (MDLL) is proposed here. The output clock is designed to cover from 100MHz to 2GHz. Fig. 7.2 (a) shows the schematic of MDLL. 64 phases delay line is adopted as DLL core. With the help of phase shifter, 16 groups of signal can be selected for edge combining and each group generates one specific phase with desired delay. The phase shifter is realized by 4 stages MUX21 and be configured by 4-bits control signal.

The edge combiner, shown in Fig. 7.2 (b), is also reconfigurable of X1/X2/X4 by proper setting MC <7:0>. For instance, a 500 MHz input signal can generate 2 GHz synchronized clock when edge combiner is configured in X4 mode. A <7:0> is one group output signal of phase shifter. After delay and XOR logic, the pulse would be generated. With all MC signal enabled, the output signal Y would have up to 8 pulses. A toggle latch, shown in Fig. 7.2 (c), is designed to generate final clock signal. The output of toggle pulsed latch flips whenever a pulse input triggers it. In other words, it is a divider by 2 but triggered by pulse input. Then 8 pulses would merge a clock signal with 4 times of the frequency.

Compared to PLL based clock generator, multiplying type DLL is simple and easy to be stable. It also has better performance because no jitter accumulation occurs in the loop. The disadvantage of multiplying operation is that the merging logic works in open loop which also brings the noise and decreases the performance. The more logic gates are used, the worse the performance would be. So we propose a system level configuration by not using the divider chain to generate low frequency multi-phase signal and then select the outputs with different logic path. System configuration promises the same logic path for all frequency outputs, and keep the multi-phase relation. Based on simulation, the main loop can work from 50 MHz to 550 MHz. With the help of edge

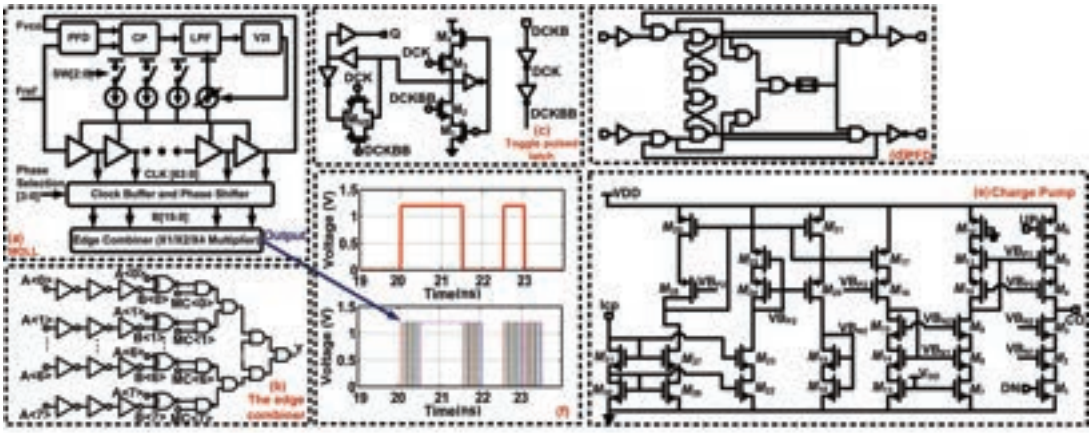

Figure 7.2: (a) Block diagram of the multiplying delay lock loop. (b) Schematics of the edge combiner and (c) toggle pulsed latch and (d) pulse frequency detector (PFD) and (e) charge pump (CP). (f) Simulation of the DLL synchronized data.

combiner, the output clock could be generated from 50 MHz to 2.2 GHz.

To avoid error locking, pulse frequency detector (PFD) is used in main loop as shown in Fig. 7.2 (a). Fig. 7.2 (d-e) shows the schematic of PFD and charge pump (CP). The PFD can work up to 600 MHz with 280 ps turn on time. Turn on time is to kill the dead zone. The charge pump is a single end cascode circuit and can work between 0.4 V and 0.9 V within 5% mismatch. Current starving delay cell is used for delay line. For better linearity, four bands are implemented by using different charge pump current. The tuning voltage is limited between 0.4 V and 0.9 V. Two comparator can be placed at the output of LPF to detect the working status and realize automatic band selection.

Fig. 7.2 (f) shows the synchronized barker codes. 16 phase data can be achieved by configuring the selection logic of phase shifter. Based on the simulation, the rms jitter is less than 1.2 ps. In the proposed architecture, 1/16 phase error in synchronization equals $0.125N$ drop in voltage, where N is the length of pulse. If ADC is working at the sub-pulse rate, 4-bits ADC would be enough to recognize the received signal and configure the VGA to achieve desired swing through the feedback loop.

7.1.2 Digitization

As described in Chapter 6, the comparison of the correlator output with a threshold reference is realized via a differential comparator - one bit ADC. For complete characterization of the analog correlator output, 4-bits up to 2 GS/s ADC is needed. For low power design, an interpolated flash ADC is proposed here. Fig. 7.3 (a) shows the schematic of the ADC. Resistor load type preamplifier is also used for averaging technique as shown in Fig. 7.3 (b).

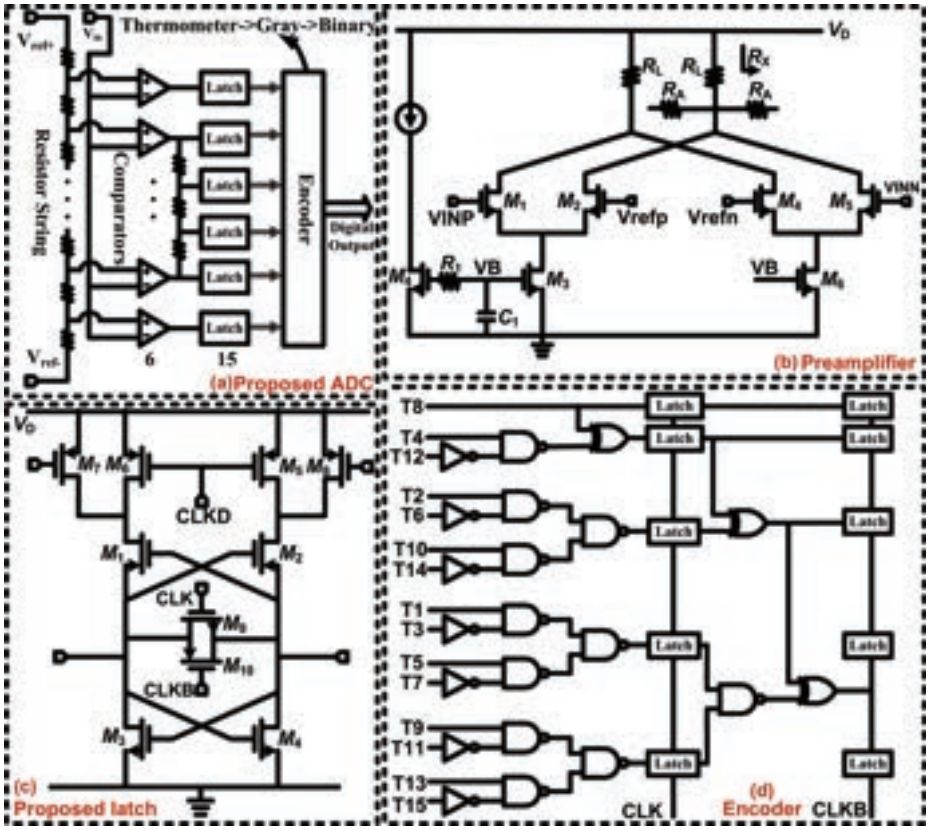

Figure 7.3: Schematic of the proposed flash ADC and (b) preamplifier and (c) latch and (d) encoder.

Then the DNL is less than 0.25 least significant bit (LSB). Fig. 7.3 (c-d) also shows the high speed latch and the encoder circuit proposed. In sampling phase, the latch is reset to half supply voltage V_D which promises high speed logic settling in comparison phase. As shown in Fig. 7.4 (a), the DNL and INL is less than 0.25 LSB based on Monte Carlo simulations. Spurious-free dynamic range (SFDR) is higher than

24 dB over the whole Nyquist band as shown in Fig. 7.4 (b). The total power of ADC is 32 mW which can work up to 2 GS/s.

For reconfigurable system, the input clock of Flash ADC can be achieved by passing the DLL output to multi-modus divider. The divider ratio is chosen based on baseband adaptive control algorithm. Then the system is flexible for different pulse configurations. However, if the pulse length is too long and saturate the ADC, the system would lose the information. That is the dynamic issue described above. Therefore, we propose the hybrid correlator which includes analog part and digital part. Analog part is a conventional mixer and digital part is a sum operator. With the help of hybrid correlator, correlation would be done in two steps. First step is doing high speed quantization in analog domain. Then system integrates the quantized signal again in digital domain. In circuit view, the second step is only a digital adder.

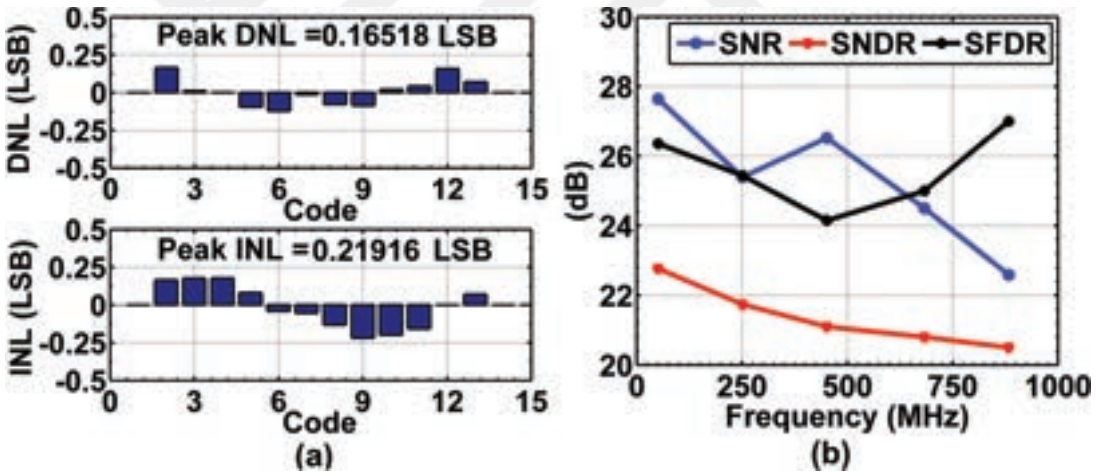

Figure 7.4: (a) Dynamic and static performance of the ADC - DNL and INL. (b) Signal-to-noise and distortion ratio and spurious-free dynamic range of the ADC.

7.2 Topics for Future Research

The investigations that have formed this dissertation have opened up several topics for future research. These topics are listed here briefly in this Section. The analysis for the analog signal processing for PCR ignored the effects of jitter noise in the template in the case of an on-chip clock generation, the quantization noise in the case of an on-

chip ADC and flicker noise at the output of the correlator which are serious challenges, especially in deep-submicron CMOS. The incorporation and analysis of the noises in the blocks into the SNR formulation must be accomplished in the future. It was determined that purely-digital signal processing is often not feasible for high-bandwidth, high-dynamic-range applications due to the high power consumption of the high-speed ADC that is required. Therefore, application-specific, power-efficient analog-/mixed-signal processing techniques should be investigated that can be performed prior to conversion to ease the ADC's performance requirements.

7.3 Conclusion

The low cost, low power, reliable pedestrian detection sensors should be embedded at several locations to sense and image the local surroundings in an intelligent environment and be benefited in the future environment which is adaptive and responsive to the objects and human beings that occupy it. The wide and low cost deployment of pedestrian detection radar sensors is a must however deployment of them around the car or local environment is very costly.

The dissertation proposes a radar transceiver compatible with a communication system and combines the proprietary design techniques - bidirectional beamforming transmission (provisional patent is being applied through UCSD) with the pulse coded signal transmission and adaptive analog signal processing (provisional patent is being applied through UCSD). The sub-systems and circuits achieving these functions are designed and implemented to achieve low noise figure, low power consumption, high linearity and high bandwidth in circuit level and provide the maximum detection distance, good range and angle resolution for the overall system level.

Range resolution of beamforming pulse-compression radar degrades with the increasing array size, therefore medium size beamforming and analog pulse compression are used together to improve the range and angle resolution, maximum detection range, SNR, detection probability and false alarm requirements. The specifications, maximum and minimum range limitation, resolution limits of the beamforming pulse-compression radar system in silicon are described. The block diagram of the proposed architecture

is depicted. The link budget with beamforming, pulse compression, and non-coherent integration in pulse compression radar are illustrated. Front-end and baseband signal processing architectures and their trade-offs are illustrated. The required time-scan and power consumption of the baseband signal processing units is illustrated.

Next, the analog signal processing system in 90nm CMOS process is demonstrated. The baseband circuitry is designed for pulse compression radar system that exhibits the autocorrelation properties of the polyphase codes, maximizes the sensitivity and resolution of a pulse radar system and alleviates speed and resolution requirements of the ADC via an analog correlator, which replaces a matched filter. The baseband circuitry includes a two-stage VGA for high dynamic range, a correlator /integrator circuit, a comparator, and offset calibration circuits. The chip is wire-bonded on the FR4 printed circuit board and tested with Stratix IV FPGA board to evaluate the system performance for different polyphase codes and their parameters. The differential, 6-bit variable gain amplifier (VGA) precedes in the system. The VGA is designed to track Friis path loss through rapid change of the VGA gain and reduces the dynamic range on the correlator and ADC. VGA has a gain variation of 52dB and a low group delay imbalance of 50 ps over 64 states. The different lengths of Barker and PRN codes are given as inputs and templates to the baseband circuitry chip to find the time of flight, monitor the correlator output and investigate the effect of various codes on the correlation. Chapter 4 presents the pulse compression radar baseband/analog signal processing blocks which are implemented and fabricated in TSMC 90-nm process. The system exhibits the autocorrelation properties of the polyphase codes and alleviates speed and resolution requirements of an ADC which is demonstrated both with simulations and measurements.

Next chapter present the novel front-end circuits for low cost, low power active and passive beamforming systems. As the first design, the first bidirectional amplifier in silicon/ silicon-germanium is reported to date - bidirectional cascaded constructive wave amplifier (BCCWA). This design is based on the cascaded constructive wave amplifier (CCWA) which uses a transmission line and an active shunt feedback circuit which feeds current back to the input of the quarter-wave transmission line to introduce a small amount of positive feedback to generate gain. For the BCCWA, two feedback amplifiers decide the direction of amplification and only one feedback amplifier operates

at a time to provide gain in either the forward and backward direction. The BCCWA is proposed to avoid the insertion losses due to the SPDT switches and decrease the area and power consumption. They are motivated by the requirements of scalable microwave and millimeter-wave phased array transceivers. The W-band BCCWA, which operates as either an LNA or PA, is designed and fabricated in a 0.13 μm SiGe BiCMOS process. The measured amplifier has a peak gain of 16 dB at 90 GHz, a bandwidth of 14.5 GHz, a noise figure of 11 dB and its output-referred P1dB is 1 dBm at 90 GHz. The circuit occupies an area of 0.47 mm^2, and consumes approximately 32 mA from a 2 V supply. Therefore, it does not impose significant circuit area or power consumption to operate as a bidirectional element and is a good candidate for the millimeter-wave (mm-wave) front-end of the PCR system.

Next, the first phase shifter/variable gain amplifier at 94 GHz in silicon/silicon-germanium is also reported to date. This design is also based on the cascaded constructive wave amplifier. The CCWA circuit architecture loaded with varactors is used to design a loss-compensated, varactor-loaded transmission line. The circuit can operate both as a continuous variable gain amplifier and phase shifter one at a time. Analog varactor control introduces a small amount of phase shift and analog feedback amplifier control in the signal path introduces a small amount of gain shift while compensating for the distributed varactor losses. Beamforming channels can be calibrated with this circuit since continuous phase and amplitude control allows phase/gain shift and calibration of the relative phase and gain errors in the channels of the beamforming systems. More than 65° of continuous phase control and 7 dB gain control (with a maximum gain of 16 dB) one at a time is demonstrated with a maximum power consumption of only 36 mW (when the feedback circuit is fully turned on).

As the third design in this chapter, although not specifically designed for the radar system front-end, a low-power dual channel distributed amplifier (DA) is implemented to reduce the number of elements in a beamforming front-end. Dual channel DA provides isolation between amplifier channels and is proposed to replace two LNAs at the same time. The DA is biased in moderate inversion to simultaneously obtain low noise figure and high linearity while consuming low power. The dual-channel DA is fabricated in a bulk 0.13μm CMOS process, achieves a forward gain of 9.6 dB and a

P_{1dB} of 4.9 dBm. The chip consumes 18 mW power.

In the next chapter, mm-wave high performance front-end circuits in 45-nm SOI CMOS process are demonstrated. The design and state-of-the-art measurement results of mm-wave (*Q*-band) balanced resistive ring mixer, SPDT switch and LNA in 45-nm SOI CMOS are presented. The technology allows the substrate isolation and provides higher f_t than other CMOS processes therefore 45-nm CMOS is an excellent candidate for mm-wave passive circuits - SPDT switches and ring mixers - and low-noise amplifiers. Electromagnetic simulations are extensively used to model the high frequency behavior of any passive components such as the conventional CPW-line, grounded stubs, inductors, and baluns. The passive resistive I/Q ring mixer demonstrates a conversion loss of 8.35 dB and input P_{1dB} of 4.5 dBm at 43.3 GHz. The gain and phase imbalance of the mixer is 0.25 dB and 2°, respectively and minimized using 10 DC pads for in-phase/quadrature paths. The record SPDT insertion loss is 1.7 dB at 45 GHz and less than 2.5 dB at 60 GHz with an isolation of greater than 25 dB at 45 GHz. The input P_{1dB} of the switch is 7.1 dBm. The LNA demonstrates a record low noise figure of 2.9 dB at 47 GHz with 18.5 dB of gain and OIP3 of 15.5dBm.

In the last chapter, the dissertation discusses the second generation baseband / analog signal processing - PCR with on-chip synchronization and digitization - and presents potential topics for future research.

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1. M. Parlak and J. F. Buckwalter, "Bidirectional Beamforming with Analog / Baseband Pulse Compression System", SD2012-389 - *Patent submitted via Tech Trans-*

fer Office at UCSD.

2. J. Li, M. Parlak, M. Matsuo and J. F. Buckwalter, "Analog Signal Processing with On Chip Timing and Digitization Circuits", *in preparation for publication to IEEE Transactions on Microwave Theory and Techniques*.

3. M. Parlak and J. F. Buckwalter,"Passive Millimeter-wave Circuits in 45-nm SOI Technology", *in preparation for publication to IEEE Transactions on Microwave Theory and Techniques*.

4. M. Parlak, M. Matsuo and J. F. Buckwalter, "Analog Signal Processing for Pulse Compression Radar System in 90nm CMOS", *accepted to IEEE Transactions on Microwave Theory and Techniques*.

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