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ANALOG IMPLEMENTATION OF FRACTIONAL-ORDER ELEMENTS AND THEIR APPLICATIONS
ANALOGOVÁ IMPLEMENTACE PRVKŮ NECELOČÍSELNÉHO ŘÁDU A JEJICH APLIKACE

DOCTORAL THESIS
DIZERTAČNÍ PRÁCE

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ABSTRACT

With advancements in the theory of fractional calculus and also with widespread engineering application of fractional-order systems, analog implementation of fractional-order integrators and differentiators have received considerable attention. This is due to the fact that this powerful mathematical tool allows us to describe and model a real-world phenomenon more accurately than via classical “integer” methods. Moreover, their additional degree of freedom allows researchers to design accurate and more robust systems that would be impractical or impossible to implement with conventional capacitors. Throughout this thesis, a wide range of problems associated with analog circuit design of fractional-order systems are covered: passive component optimization of resistive-capacitive and resistive-inductive type fractional-order elements, realization of active fractional-order capacitors (FOCs), analog implementation of fractional-order integrators, robust fractional-order proportional-integral control design, investigation of different materials for FOC fabrication having ultra-wide frequency band, low phase error, possible low- and high-frequency realization of fractional-order oscillators in analog domain, mathematical and experimental study of solid-state FOCs in series-, parallel- and interconnected circuit networks. Consequently, the proposed approaches in this thesis are important considerations in beyond the future studies of fractional dynamic systems.

KEYWORDS

Analog integrated circuit, circuit connections, fabrication, fractional calculus, fractional-order capacitor, fractional-order derivative, fractional-order device, fractional-order element, fractional-order inductor, fractional-order integrator, fractional-order system, fractional-order oscillator, solid-state fractional-order capacitor.

ABSTRAKT

S pokroky v teorii počtu neceločíselného řádu a také s rozšířením inženýrských aplikací systémů neceločíselného řádu byla značná pozornost věnována analogové implementaci integrátorů a derivátorů neceločíselného řádu. Je to dáno tím, že tento mocný matematický nástroj nám umožňuje přesněji popsat a modelovat fenomén reálného světa ve srovnání s klasickými „celočíselnými“ metodami. Navíc nám jejich dodatečný stupeň volnosti umožňuje navrhovat přesnější a robustnější systémy, které by s konvenčními kondenzátory bylo nepraktické nebo nemožné realizovat. V předložené disertační práci je věnována pozornost širokému spektru problémů spojených s návrhem analogových obvodů systémů neceločíselného řádu: optimalizace rezistivně-kapacitních a rezistivně-induktivních typů prvků neceločíselného řádu, realizace aktivních kapacitorů neceločíselného řádu, analogová implementace integrátoru neceločíselného řádů, robustní návrh proporcionálně-integračního regulátoru neceločíselného řádu, výzkum různých materiálů pro výrobu kapacitorů neceločíselného řádu s ultraširokým kmitočtovým pásmem a malou fázovou chybou, možná realizace nízkofrekvenčních a vysokofrekvenčních oscilátorů neceločíselného řádu v analogové oblasti, matematická a experimentální studie kapacitorů s pevným dielektrikem neceločíselného řádu v sériových, paralelních a složených obvodech. Navrhované přístupy v této práci jsou důležitými faktory v rámci budoucích studií dynamických systémů neceločíselného řádu.

KLÍČOVÁ SLOVA

Analogový integrovaný obvod, obvodové zapojení, výroba, počet neceločíselného řádu, kapacitor neceločíselného řádu, derivace neceločíselného řádu, zařízení neceločíselného řádu, prvek neceločíselného řádu, induktor neceločíselného řádu, integrátor neceločíselného řádu, systém neceločíselného řádu, oscilátor neceločíselného řádu, kapacitor s pevným dielektrikem neceločíselného řádu.

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DECLARATION

I declare that I have written the Doctoral Thesis titled "*Analog implementation of fractional-order elements and their applications*" independently, under the guidance of the advisor and using exclusively the technical references and other sources of information cited in the thesis and listed in the comprehensive bibliography at the end of the thesis.

As the author of the doctoral thesis I furthermore declare that, in regard to the creation of this doctoral thesis, I have not infringed any copyright. In particular, I have not unlawfully encroached on anyone's personal and/or ownership rights and I am fully aware of the consequences in the case of breaking Regulation § 11 and the following of the Copyright Act No 121/2000 Sb., and of the rights related to intellectual property right and changes in some Acts (Intellectual Property Act) and formulated in later regulations, inclusive of the possible consequences resulting from the provisions of Criminal Act No 40/2009 Sb., and of the rights related to intellectual property right and changes in some Acts (Intellectual Property Act) and formulated in later regulations, inclusive of the possible consequences resulting from the provisions of Criminal Act No 40/2009 Sb., Section 2, Head VI, Part 4.

Brno ……

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Author's signature

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To my teachers…

Eserinin Üzerinde Imzası Olmayan Yegâne Sanatkâr Öğretmendir.
Mustafa Kemal Atatürk

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Aslihan Kartci

May 22, 2019, Brno, Czech Republic

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1 INTRODUCTION

1.1 Brief History of Fractional Calculus

Fractional calculus, the branch of mathematics regarding differentiations and integrations to non-integer orders, is a field that has been introduced 300 years ago [1]. Inspiring from the fractal models in the environment, from integer to non-integer models was explored. It origins from 30th of September in 1695 between Leibniz and L'Hopital correspondance, with L'Hôpital inquiring about Leibniz's notation, $d^n y/dx^n$ where n is a positive integer. L'Hôpital addressed in this letter the question [2]: what happens if this concept is extended to a situation, when the order of differentiation is arbitrary (non-integer), for example, $n = 1/2$? Since then the concept of fractional calculus has drawn the attention of many famous mathematicians, including Euler, Laplace, Fourier, Liouville, Riemann, Abel, and Laurent.

First organized studies on fractional calculus were performed in the beginning and middle of the 19th century by Liouville and Riemann. Liouville (1832) expanded functions in series of exponentials and defined the derivative of such a series by operating term-by-term under the assumption of derivative order being a positive integer. Riemann (1847) proposed a different definition which involved a definite integral and was applicable to power series with non-integer exponents [3].

It was A. K. Grünwald and Krug who first unified the results of Liouville and Riemann. Grünwald (1867) adopted as his starting point the definition of a derivative as the limit of a difference quotient and arrived at definite integral formulas for differentiation to an arbitrary order. Sonin in 1869 where he used Cauchy‘s integral formula as a starting point to reach differentiation with arbitrary index. A. V. Letnikov wrote several papers on this topic from 1868 to 1872. A. V. Letnikov extended the Sonin's idea in 1872. Both tried to define fractional derivatives by utilizing a closed contour. Krug (1890), working through Cauchy's integral formula for ordinary derivatives, showed that Riemann's definite integral had to be interpreted as having a finite lower limit while Liouville's definition corresponded to a lower limit $-\infty$ [3], [4].

Grünwald and Letnikov provided the basis for another definition of fractional derivative which is also frequently used today. The Grünwald-Letnikov definition is mainly used for derivation of various numerical methods with finite sum to approximate fractional derivatives. Among the most significant modern contributions to fractional calculus are those made by the results of M. Caputo in 1967 [3].

In the 20th century notable contributions were made to both the theory and application of the fractional calculus. Some of the work worth mentioning was done by Weyl (1917), Hardy and Littlewood (1925, 1928, 1932), Kober (1940), and Kuttner (1953) who examined some properties of both differentiation and integration to an arbitrary order of functions belonging to Lebesgue and Lipschitz classes. Erdélyi (1939, 1940, 1954) and Osler (1970) gave definitions of differentiation and integration to an arbitrary order with respect to arbitrary functions. Post (1930) used difference quotients to define generalized differentiation for operators. Riesz (1949) developed a theory of fractional integration for functions of more than one variable. Erdelyi (1964, 1965) applied the fractional calculus to integral equations; Higgins (1967) used fractional integral operators to solve differential equations [1], [3], [4]. Later on in chronological sequence; S. C. Dutta Roy (1967), Oldham-Spanier (1974), K. Nishimoto (1987),

Mainardi (1991), L. Debnath (1992), H. M. Srivastava, Miller and Ross (1993), Kolwankar and Gangal (1994), Oustaloup (1994), Carl Lorenzo (1998) Tom Hartley (1998), R. K. Saxena (2002), Igor Podlubny (2003), R. K. Bera and S. Saha Ray (2005) [10], Khalil (2014) [5], Caputo-Fabrizio (2015) [6], Atangana-Balenau (2016) [7] contributed in many parts of fractional calculus. There exist many other definitions because fractional order calculus is still under development. Each different definition is or can be used in the function that fits different process [3].

Considering the non-integer order n, such as 1.3, $\sqrt{2}$, $3j$-4 or any other real or imaginary order, the differentiation $d^n f(t)/dt^n$ is solved by fractional calculus. Understanding the solutions of fractional-order differential equations is the key to building better models for fractional order dynamic systems. For that purpose, only the significant definitions and their useful properties will be presented here.

First one is a Riemann-Liouville definition [1] of a fractional derivative:

$$ {}_aD_t^{\alpha} f(t) = \frac{d^n}{dt^n}\left[\frac{1}{\Gamma(n-\alpha)}\int_a^t \frac{f(\tau)}{(t-\tau)^{\alpha-n+1}}d\tau\right], \tag{1.1}$$

second one is a Grünwald-Letnikov approximation and expressed as:

$$ {}_aD^{\alpha} f(t) = \lim_{h\to 0}\frac{1}{h^{\alpha}}\sum_{m=0}^{\left[\frac{x-\alpha}{h}\right]}(-1)^m \frac{\Gamma(\alpha+1)}{m!\Gamma(\alpha-m+1)} f(t-mh), \tag{1.2}$$

and third one is Caputo derivative [3] and given as:

$$ {}_aD_t^{\alpha} f(t) = \frac{1}{\Gamma(n-\alpha)}\int_a^t \frac{f^{(n)}(\tau)}{(t-\tau)^{\alpha+1-n}}d\tau, \tag{1.3}$$

where $\Gamma(\cdot)$ is the gamma function, and n-1 < α < n. Similarly to the Grünwald-Letnikov and Riemann-Liouville approaches, the Caputo also provides an interpolation between integer-order derivatives. The main advantage of Caputo's approach is that the initial conditions for fractional differential equations take on the same form as integer-order differential equations. Laplace transform of the Riemann-Liouville fractional derivative allows utilization of initial conditions which may cause problems with their interpretations. However, the Laplace transform of the Caputo derivative allows utilization of initial values of classical integer order derivatives with known physical interpretations. Mathematical expressions such as difference or differential equations may be considered as advanced mathematical or analytical models and they are preferred to the simpler models once the application becomes complicated. Mathematical models are categorized into groups such as time continuous or time discrete, lumped or distributed, deterministic or stochastic, linear or nonlinear. Each of these adjectives marks a property of the used model for the dynamic system and thus determines the type of the equation.

1.2 Fractional Calculus in Electrical Engineering

Time has proven Leibniz as the applications of fractional calculus e.g., differentiation or integration of non-integer order, has seen explosive growth in many fields of science and engineering. These mathematical phenomena allow us to better characterize many

real dynamic systems. The concept of fractional calculus has tremendous potential to model and control the nature around us.

Although the invention of fractional calculus is as old as the classical calculus going back to the late 1600s, it has not been widely used as a tool for modelling dynamic systems. One of the first applications was the tautochrone problem where the integral equation solved by Abel (1823) via an integral transforms which could be written as a semi-derivative form. A powerful boost in the use of fractional calculus to solve problems was provided by Boole. Boole (1844) developed symbolic methods for solving linear differential equations with constant coefficients. The next important step in the application of fractional order calculus was made by Heaviside developing the operational calculus to solve certain problems of electromagnetic theory [8]. In the year of 1920, he introduced a fractional-order differential equation on semi-infinite lossy transmission line [8]. Another equivalent system is the diffusion of heat into a semi-infinite solid. Here the temperature is described from the boundary that is equal to the half integral of the heat rate there. Other systems that are known to display fractional-order dynamics are electrode-electrolyte polarization [9], [10], dielectric polarization [11], electromagnetic waves, an ideal capacitor model [3], [12] etc. As many of these systems depend upon specific material and chemical properties, it is expected that a wide range realization of fractional-order behaviors are also possible using different materials.

There are two methods for realization of fractional-order integral and derivative operators. First one is digital realization based on microprocessor devices and appropriate control algorithm and the second one is analogue realization based on analog circuits. An analog circuit emulating fractional-order behavior is often modeled by fractional-order differential equations based on the current-voltage relationship of the electrical circuits. They are called as fractional-order elements (FOE), and fractional-order capacitor (FOC) or fractional-order inductors (FOI) defining the integrator and differentiator operators, respectively. These devices have characteristic of the constant phase which is independent of the frequency within a wide frequency band.

Since their mathematical representations in the frequency domain are irrational, direct analysis methods and corresponding time domain behavior seem difficult to handle. Therefore, design of FOEs is done easily using any of the rational approximations. Then, it must be transformed to the form of a continued fraction. Only in some specific approximations this step might be omitted. If all the coefficients obtained from finite continued fraction are positive then the FOE can be made of classical passive elements e.g., resistor, capacitor, inductor using circuit network theory [13]-[16] or active elements e.g., commercial amplifiers, operational transconductance amplifiers etc. using a general active filter configuration [17]-[19]. If some of the coefficients are negative, then the FOE can be made with the help of negative impedance converters [20]. Thus, in order to effectively design such systems, it is necessary to develop approximations to the fractional operators using the standard integer order operators. The most prominent and applied approximation methods are Newton's Method [13], Matsuda's Method [21], Oustaloup's Method [22], Continued Fraction Expansion (CFE) [23], Charef's Method [24], Laguerre approximation [25], El-Khazali [26]. However, no specific method for recovering a fractional process model was provided. These methods also have computational difficulties in higher orders thus their practical realization becomes more complex.

Fractional-order systems, or systems containing fractional derivatives and integrals, have been studied in many engineering areas. For instance, filters [27]–[32], oscillators [33]–[41], controllers [42]–[51], bio-impedance modeling [62], [53], transmission line design [54]–[56], reluctance inductive transducer realization [57], dc–dc boost converters [58] are among in emerging fields. Their implementation evidently requires the use of a FOE, which brings to researchers several design features such as offer additional degrees of freedom and versatility in electrical circuits [59]–[62]. These systems constructed using *n* number of FOEs are described with an *n*th-order fractional systems of fractional differential equations.

Sinusoidal oscillators, which are key electronic circuits, are classically known to be realizable using at least a second-order circuit. Most of the famous oscillators are either second-order or third-order oscillators. In the last years, the study of fractional-order oscillators started to be one of the main fundamental topics in fractional-order dynamic systems. This originated from the fact that extremely low and high frequencies of oscillation are possible through such structures [34], [63]. Particularly, the studied quadrature or multiphase oscillators are the classic ones such as the Hartley oscillator [33], and Wien-bridge oscillator [39], [64], Colpitts oscillator [40], [65]. The fundamental technique for designing fractional-order oscillators have been introduced in [33]. The study shows that the design of fractional-order oscillator is derived from classical active elements-based structures such as op-amps and with their equivalent macro models containing two or more FOEs. Considering the FOEs with an order of less than one, the total system order also decreased from two or three. However, the oscillation criterion is still sustained. It is evident that available circuit design techniques are dominantly based on the assumption of a target realizable integer-order circuit. The implementation of such oscillators brings to researchers several design features such as possibility of changing the frequency of oscillation (FO) and condition of oscillation (CO) independent then each other. Also the lack of Barkhausen criteria is shown [33].

Identification on real systems has shown that fractional-order models can be more intrinsic and adequate than integer-order models in describing the dynamics of many real systems [66], [67]. Indeed, the fractional derivatives provide an excellent tool for the description of memory and hereditary properties of various materials and processes. This is the main advantage of fractional-order models (fractional derivatives) in comparison with classical integer-order models, in which such effects are in fact neglected. Moreover, defining a system as fractional is that the fractional-order gives an extra degree of freedom (coming from its arbitrary order) in controlling the system's performance. It leads researchers to believe that the future of discrete element circuit design and fabrication of single solid-state components will undergo a paradigm shift in favor of FOEs.

1.3 Research Objectives

Based on the state of the art and relevant discussion, the following problems may be formulated and constitute the motivation for the work presented in this thesis. With advancements in theory of fractional calculus and also with widespread engineering application of fractional-order dynamics, analog implementation of fractional dynamics has received considerable attention. One of them is the modelling and fabrication of FOEs which can be separated to two categories: single and multicomponent realization of FOEs. As the basis of multicomponent implementation in analog domain, passive

synthesis of fractional immittance function is one of the most important topics to study. However, they have two design considerations: accuracy and limited operation time. For instance, response of a passive circuit of FOC is approximately proportional to the semi-integral of the input signal meaning the circuit has a degree of accuracy. Secondly this circuit can approximate the behavior of a real semi-integrator only over a limited time interval which has a finite upper limit and a non-zero lower limit. Although these two issues may be improved by selecting better components and increasing the number of components, the cost of the design will inevitably increase [63]. Thus, to find the optimal emulation of an FOE e.g., FOC and FOI, a new approach for the optimization of phase and impedance responses of fractional-order capacitive and inductive elements should be benefited from the evolutionary algorithms.

Another analog implementation for a multicomponent FOE is the active element design of fractional-order differentiators and integrators. These operators are used to compute the fractional-order time derivative and integral of the given signal. In industrial electronic, they named as proportional-integral-derivative (PID) controllers. They can be realized using commercial operational amplifiers as known from the basic electronic circuit theory. However, this realization is limited in the frequency range according to amplifier specifications and they do not offer integrated circuit design [68]. Therefore, there is need to use transistor based active building blocks. So-called bilinear transfer segment (BTS) is a two port network with a single pole and single zero. Cascade of BTSs creates a constant phase block, which generates desired magnitude and phase response by proper setting of both polynomial roots (zero and pole frequencies) of each BTS [17]. It is worth to mention that fractional-order transfer function of the controller leads to the concept of fractional poles and zeros in the complex *s*-plane. Therefore, using the electronic parameters of BTSs e.g., voltage, current, resistor, transconductance, the fractional-order systems can be designed and controlled.

Other way of implementation for single FOE is the fabrication of passive, two terminal fractional-order devices (FODs) benefiting from the lossy nature of the dielectric materials [69]. Fabrication of FOCs allows us to make direct and easy implementation of fractional-order systems since it will be just replaced with its integer-order counterpart. That will also help to increase the fractional-order application area. Recent researches presented liquid, solid, and semi-solid electrolyte type FODs. However the limitation on frequency bandwidth, order, packaging, and high fabrication cost push researchers to develop the better one. In open literature, only FOC is mentioned due to the non-existence of fabricated FOI.

Once an optimal model and design of a FOC is established, one may proceed with FOC based stable, integrated circuit design. The very first step should be the test of FOCs in circuit network configurations. This is crucial because FOC possesses both a real and imaginary impedance part while its phase is frequency independent that differs from the series connected resistor and capacitor. However, an ideal capacitor has only an imaginary part. This is particularly important, if the proposed application requires a configuration using capacitors, where errors accumulate the metrics of the individual components. For instance, the series and parallel connections of FOCs play a crucial role in investigating the dielectric properties e.g., zinc flakes/flexible polyvinylidene fluoride (ZFs/PVDF) composites [70] and in practical applications such as modelling of supercapacitors [71] or designing of supercapacitor banks [72]. Bearing these ideas in mind, to the best knowledge of the author, there are only a few studies that focus on the

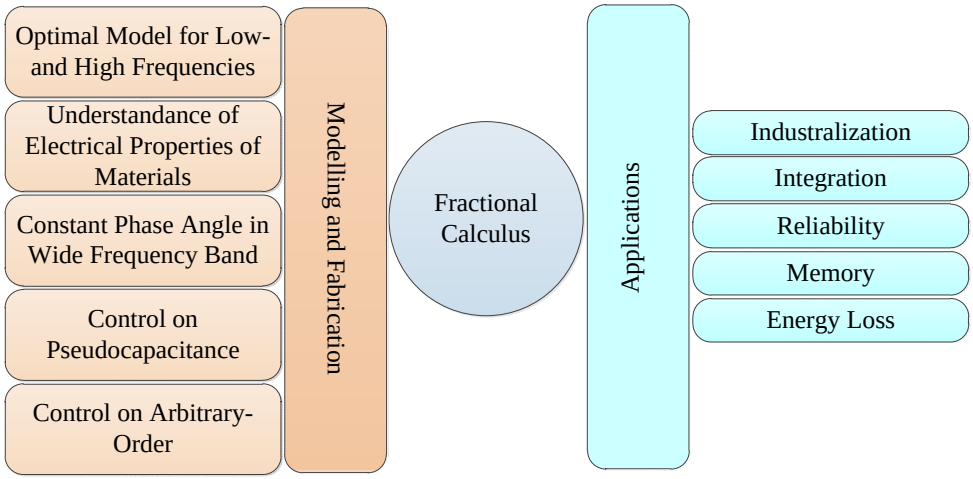


Fig. 1.1: Challenges in fractional-order dynamic systems

series and parallel connection of FOCs, mainly on the theoretical level only due to lack of real FOCs [73]−[76].

Due to the additional control parameter of FOCs, sinusoidal oscillators are capable of outperforming their integer-order counterparts, since more design specifications may be fulfilled [27]. Thus, developing a general method for sinusoidal oscillator tuning is very desirable. The import of concepts from fractional calculus allows for the creation of a more ideal design procedure, with the potential for compact MOS based oscillators to be designed to meet the exact design requirements e.g., oscillation condition, oscillation frequency, and phase or amplitude specifications. This idea of compact MOS based oscillator design is a very new field, with much work that needs to be accomplished in order to create a more general and ideal integrated circuit design for oscillators.

As stated above, of particular importance is the use of fractional-order models and their applications in analog circuit design. Studies show that a huge portion of FOEs realizations —about 90%—are of multicomponent FOEs; moreover, it was found that about 80% of these existing FOEs are realized on FOC part with poorly control of constant phase angle [77]. These facts will be further analyzed with deep literature survey in the following chapter. However some of the challenges generally in fractional-order systems are shortly described in Fig. 1.1. Since the application of FOCs in analog domain offer tunability, independent control of parameters between each other, it is expected that their integrated circuit design will result in considerable benefit. Therefore, the main contribution of the author of the thesis is the development of optimum design for passive FOEs for systems described by fractional dynamic models and increasing their availability in analog electronic circuit design. This contribution comprises three consecutive parts:

- Optimization: Instead of approximating the rational functions of irrational transfer functions using the above mentioned approximations at a certain frequency (or bandwidth), the phase and/or impedance responses of RC/RL networks in the whole desired frequency range is optimized. This is achieved with a new approach based on the mixed integer-order genetic algorithm (GA) to obtain accurate phase and magnitude response with minimal branch number and optimum passive values [78]. Standardized, IEC 60063 compliant commercially available passive component values are used; hence, no correction on passive

elements is required which leads us to a decrease of phase angle deviation and overall enhancement of the performance of the FOE. This approach is also used in modelling of filler in double layer capacitor [79] to find the best fit of fabrication of FOC with hexagonal-boron nitride (*h*BN) over a frequency range of five decades.

- Integration: The main objective of this part is to introduce a new analogue implementation of FOEs and their applications in oscillator design using compact CMOS active building blocks (ABBs) with reduced transistor count. The first implementation is the design of fractional-order integrator, which is a synonym of FOC in analog design, using cascade of first-order BTSs. The performance of this circuit is used in fractional-order proportional-integral ($FOPI^{\lambda}$) control [80] for a speed control system of an armature controlled DC motor, which is often used in mechatronic and other fields of control theory. The second implementation is the fractional-order oscillators. The increased circuit complexity, the power dissipation of the active cells becomes quite high. In order to overcome this obstacle, novel very simple voltage–mode (VM) fractional-order oscillator topologies are introduced [81]-[83].
- Experimental verification: The accuracy and stability of proposed FOEs and their primary versions are experimentally verified on real-life analog electronic circuits. The solid-state, PCB compatible polymer composite based FOCs [79], [84] are tested in circuit network connections considering the identical- and arbitrary-orders of the elements. The theory of fractional-order circuit network connections is formulated and experimentally verified [85], [86]. This study helps to show the stability of the solid-state FOCs. Moreover, the PCB-compatible FOCs fabricated using molybdenum disulfide (MoS_2)-ferroelectric polymer composites [87] are used in Wien oscillator [88].

1.4 Thesis Outline

This thesis consists of an introductory part comprising eight chapters and of eight main publications referred to as [78], [80]-[83], [85], [86], [88]. Additionally, the scope of this work is closely related to publications [19], [29], [30], [31], [41], [49], [50], [56], [89], [90] and [91], which are summarized and seamlessly integrated into the body of the manuscript. In order to make this text accessible by a more general audience, the fundamental definitions and core trade-offs related to FOEs and fractional-order applications are given. Then thesis gradually shifts toward optimization, design and fabrication of FOEs and their applications. Finally, each chapter of the thesis is concluded with a summary section containing important remarks pertaining to theoretical and practical results reported in the corresponding chapter. Facilitating the flow of thought, the material given in the initial chapters is reused by the subsequent chapters. As such, the focus of the narration tends to transfer from more general to more detailed problem formulations and related research.

In Chapter 1, a brief history of fractional calculus, its application in electrical engineering and the core motivation behind this thesis research are given. Then it is continued with the scope of this work by highlighting the key problems addressed in the thesis. The main contributions of this thesis along with the related list of publications are also summarized.

In Chapter 2, a comprehensive review of passive and active implementation of

FOEs can be found in chronologically. The RC/RL models are elaborated as distributed element realization while material based ones as fractional-order devices. Their boundaries and barriers are discussed point by point. Then many other realizations are discussed together with the chapter summary.

In Chapter 3, an optimization for the magnitude and phase response of fractional-order capacitive and inductive elements is proposed by using genetic algorithm (GA). Particular attention is given to Foster-II and Valsa networks of FOEs, since these networks are the best in total capacitance and low phase error point of view, respectively. Standardized, IEC 60063 compliant commercially available passive component values are used. To the best knowledge of the author, this particular approach has not been used in prior art. A bandwidth of four decade, and operating up to 1 GHz with low phase error of approximately ±1°, without correction on passive elements are obtained with optimum and minimal branch number. As validation, numerical simulations using MATLAB® and experimental measurement results are presented for precise and/or high-frequency applications.

In Chapter 4, an approach to design a fractional-order integral operator using an analogue technique is presented. The integrator with a constant phase angle is designed by cascade connection of first-order bilinear transfer segments and first-order low-pass filter. The performance of suggested realization is demonstrated in a fractional-order proportional-integral (FOPI$^{\lambda}$) controller where λ is an arbitrary real order of the integrator. The behavior of both proposed analogue circuits is confirmed by SPICE simulations using TSMC 0.18 μm level-7 LO EPI SCN018 CMOS process parameters.

In Chapter 5, a hexagonal boron nitride (*h*BN) -polyevinelidenefluoride-trifluoroethylene-chlorofluoroethylene (P(VDF-TrFE-CFE)) polymer composite is used to fabricate a new FOC. Different constant phase angles are measured with changing the volume ratio of two tuning knobs e.g. carbon nanotube (CNT) and *h*BN. The resulting FOC's bandwidth of operation, where the variation in the phase angle is no more than approximately ±4° is five decades between 100 Hz - 10 MHz.

In Chapter 6, general analytical formulas are introduced for the determination of equivalent impedance, magnitude, and phase, i.e. order, for *n* identical and arbitrary FOCs connected in series, parallel, and their interconnection. Three types of solid-state FOCs of different orders, using ferroelectric polymer and reduced Graphene Oxide (rGO)-percolated P(VDF-TrFE-CFE) composite structures, are characterized. Multiple numerical and experimental case studies are given, in particular for two and three connected FOCs. The fundamental issues of the measurement units of the FOCs connected in series and parallel are derived. A MATLAB open access source code is given in Appendix B for easy calculation of the equivalent FOC magnitude and phase.

In Chapter 7, four types of fractional-order sinusoidal oscillators are studied namely compact voltage-mode oscillator and Colpitts and Wien oscillators. First, their design method is described. Then, except the Wien oscillator, each of oscillators is designed using ABBs and studied numerically using MATLAB program while their performance have been evaluated by SPICE simulations. The active FOI emulation circuit is designed using RC networks for fractional-order Colpitts oscillator. The classic well-known Wien oscillator is experimentally verified using MoS_2 based solid-state FOCs. Our results confirm that proposed solutions are successful in bridging across the indicated system vulnerabilities.

Chapter 8 concludes the introductory part and outlines some interesting directions for future work.

2 A SURVEY ON FRACTIONAL-ORDER ELEMENTS AND DEVICES

The term fractance or FOC, an electrical elements having properties between resistance and capacitance, was suggested by A. Le Mehaute in 1983 [92] for denoting electrical elements with non-integer order impedance. In electrical engineering in particular, the constant-phase behavior of capacitors is explained as the frequency dispersion of the capacitance by dielectric relaxation, where the electric current density follows changes in the electric field with a delay. In 1994, to express this phenomenon of "off the shelf" real capacitors mathematically, the capacitance current in the time domain was given as [12]:

$$i(t) = C\frac{d^{\alpha}u(t)}{dt^{\alpha}}, \tag{2.1}$$

where $d^{\alpha}u(t)/dt^{\alpha}$ denotes the "fractional-order time derivative". In same way, the given relationship for FOI is expressed as:

$$i(t) = \frac{1}{L}\int_{-\infty}^{t} u(t)dt^{\alpha}, \tag{2.2}$$

where $\int_{-\infty}^{t} u(t)dt^{\alpha}$ denotes the "fractional-order time integral" with having the order $0 < \alpha < 1$. Fig. 2.1 shows these fundamental components in frequency domain and possible FOEs in four quadrants [93]. Their impedance is described as $Z(s) = Ks^{\alpha}$, where ω is the angular frequency in $s = j\omega$, and the phase is given in radians ($\varphi = -\alpha\pi/2$) or in degrees (°) ($\varphi = -90\alpha$). Obviously the impedance of the FOE has a real part dependent on the non-zero frequency and its magnitude value varies by 20α dB per decade of frequency. In particular, the impedance of Type IV FOEs, i.e. FOCs in quadrant IV, is provided with an order of $-1 < \alpha < 0$ and pseudocapacitance of $C_{\alpha} = 1/K$, whereas FOIs in quadrant I (Type I) have an order of $0 < \alpha < 1$ and pseudoinductance of $L_{\alpha} = K$. Their units are expressed in units of farad·sec$^{\alpha-1}$ (F·s$^{\alpha-1}$) and henry·sec$^{\alpha-1}$ (H·s$^{\alpha-1}$). The higher order FOCs and FOIs with the described impedances then matched in quadrant II and III (Type II and III), respectively. Their characteristics such as pseudocapacitance, pseudoinductance, constant phase zone (CPZ), constant phase angle (CPA – defined phase angle in CPZ), and phase angle deviation (PAD – maximum difference between a designed/measured phase and a target phase) profoundly impact the transfer function of the fractional systems [59], [62], [94]. Therefore, in order to practically realize fractional operators, a finite, infinite, semi-infinite dimensional integer-order system resulting from the approximation of an irrational function can be used. This equivalent integer-order transfer functions then can be used also in design of analog integrator and differentiator circuit by selecting proper time constant or correct distribution of zeros and poles of the function. Apart from circuit combinations of resistive and capacitive networks, realizations of FOEs expressing the anomalous diffusion phenomenon in chemical reaction and viscoelastic property of some polymers expressed by fractional-order differential equation are also found in literature [62] As a result, realization of FOE becomes an important and

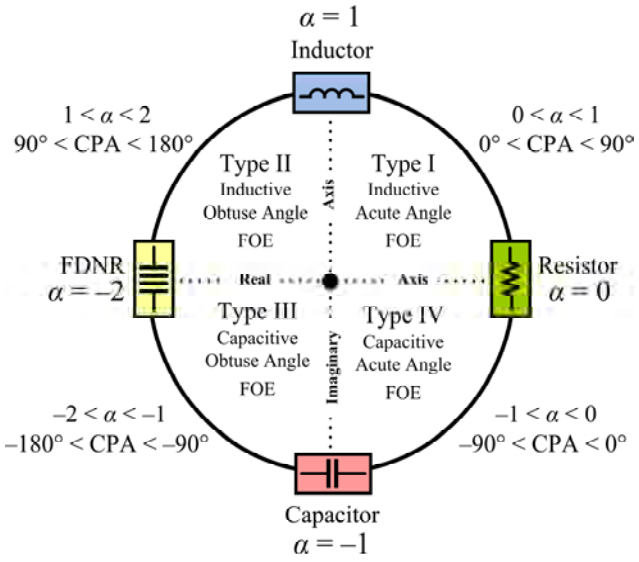


Fig. 2.1: Description of fractional-order elements in four quadrants [93]

necessary step to explain this natural phenomenon. Therefore, in this section, an overview of FOEs and FODs is provided to understand and evaluate the early studies, and move forward with the missing points. The section is separated to two parts; the first is discrete element approximations of FOEs and the second is fabricated FODs made using materials up-till now.

2.1 Discrete Element Realizations of Fractional-Order Elements

The standard definitions of the fractional differintegral do not allow direct implementation of the operator in time-domain simulations of complicated systems with FOEs. Their mathematical representations in the frequency domain are irrational. Thus, in order to effectively analyze such systems, it is necessary to develop approximations to the fractional operators using the standard integer-order operators.

This makes the task of finding integer-order approximations of fractional transfer functions a most important one. What is meant by this is that when simulations are to be performed or models are to be identified or controllers are to be implemented, fractional transfer functions are usually replaced by rational transfer functions which are easier to handle. Numerous methods for synthesis of FOEs have been proposed. They differ by the approximation of their functions. They are expanded using analytical methods to calculate the parameters of their equivalent circuits. They consist of capacitors and resistors, which are described by conventional (integer) models; however, the circuit itself may have non-integer order properties, becoming a so-called constant phase element, or fractional-order capacitor. The realization of fractional order inductors using resistive/inductive networks are limited due to their size, cost and limited operating frequency range. Therefore, the research on this area remained limited.

2.1.1 Methods and Structures

Around the year 1890 several people worked with the idea to improve the properties of

long-distance transmission lines by inserting coils at regular intervals in these lines. Among those people were Vaschy and Heaviside. The results were discouraging at that time, and no real progress was made, until M. I. Pupin investigated these cables in 1899 [95]. By his thorough mathematical and experimental research, Pupin found that the damping in cables for telegraphy and telephony can be substantially reduced by judiciously inserting these coils, which has resulted in a widespread use of these so-called “Pupin lines” throughout the world. The properties of these lines were further investigated by George A. Campbell. In 1903 he published some findings [96] namely that they have a well-defined critical frequency that marks a sudden change in the damping characteristics. While he was investigating these dumping effects, Campbell pointed out that he used this effect to eliminate harmonics in signal generators. In fact he used the cable as a low-pass filter, and he even mentioned the possibility of using the cable as a band-pass filter by replacing the coils by combinations of coils and capacitors. In 1915, Karl Willy Wagner [97] from Germany, and Campbell from America [98] independently simulated the line by a ladder construction of impedances, mostly constructed as combinations of inductances and capacitances. It was this invention that made the year 1915 to be usually regarded as the birth year of the electrical filter. The design theory of this type of filter bears the heritage from the transmission-line theory and was expressed in terms of characteristic impedances that should be matched if stages were cascaded, and wave-propagation constants that were used to describe the attenuation characteristics of the filter. Later on, in a period that roughly extends from 1930 to 1940, Wilhelm Cauer published a number of articles in which he designed passive filters with well-defined transfer functions using Chebyshev approximations with a defined attenuation behavior [99]. In 1939, Sidney Darlington followed Cauer with his “insertion-loss theory” [100]. Unfortunately, these theories, as they were formulated, had few connections with practice, which made them unpopular. Filters were realized as networks of inductors, capacitors, and resistors. Due to the large and expensive quality factor of inductors in many applications direct us to use of capacitors. Moreover, the filter transfer functions that can be realized with capacitive and resistive elements only have their poles on the negative real axis of the complex Laplace plane. Complex poles are realizable if active circuits are added. This gave rise to the use of active RC filters [101].

In 1950, Sidney Darlington proposed a more compact form of the transfer functions that is more suitable for determining the degree of approximation (n) and its analysis using pairs of capacitive-resistive phase-shifting networks [102]. Each network terminated with its separate load along with n number of all-pass sections. Each all-pass function has the property of exhibiting equal ripple while the value of frequency “ω” moves from the ω_1 to ω_2, where they denote the lower and upper ends, respectively. Therefore, CPZ is attributed to the phase shift network and dependent on the complex nature of it. The theoretical study showed that phase error is inversely and frequency range is directly proportional to the degree of the approximation. The main lack of this approximation was the use of inductors and capacitors in all-pass sections which brings to difficulties of the practical circuit realization.

Several networks with a parallel combination of a number of series infinite number RC elements to obtain a nearly constant argument (phase) over an infinite frequency range were showed in 1959 by Ralph Morrison [103]. These networks have the basic canonic forms as Foster and Cauer. The constant phase behavior and scaling factor were described mathematically and their relations were discussed over a two-decade frequency range. Moreover, their measurement results were shown. The effect of

terminating (correcting, single, parallel connected) elements were given. A feedback amplifier design using a constant argument network was explained theoretically.

Donald C. Douglas has given a design procedure to obtain a constant phase angle from –90° to +90° with predefined phase error in specified frequency bandwidth in 1961 [104]. The phase error is independent than the network complexity while the frequency range is. The theory was based on Morrison's study and explained on a periodic rippling phase function by centering an infinite number of identical characteristics at equal intervals on a logarithmic frequency scale. For a phase angle of 45°, the error was ±0.015° while the error might vary for other phase angles. Setting the CPA with the phase error and using simple schematic were the advantages of this method. However, some special tables were required to attain the specified phase angle and error. This study differs from Morrison's method by the product of infinite number of basic transfer functions (Morrison's development was based on a summation of an infinite number of basic admittance functions).

In 1963, Robert M. Lerner has proposed the finite network in which the pole and zeros of the series string of parallel RL and RC pairs were set according to the order k whether equal to be positive or negative [105]. The successive pairs of inductance or capacitance were set in the ratio of p, and the resistors were in the ratio of p^k. Even though, the similar structures as in Morrison's study were used, Lerner took resistors with the power-law instead of p as Morrison thereby reduced the repetitive errors in magnitude. In addition, the compensation impedance was specified to correct the edge ripples which could be modelled as the additional poles in the transfer function. An experimental admittance constructed with five capacitors and five resistors approximated half-order impedance within the accuracy of 1% in magnitude and ±1° in phase over the frequency range of 50 Hz - 10 kHz.

In 1964, G. E. Carlson and C. A. Halijak showed applications of a Newton process for approximating the characteristic of a balanced symmetric RC lattice (cross RC ladder) [14]. The networks were cascades of balanced symmetric lattices with unit resistors in the parallel arms and unit capacitors in the cross arms. The cascade was terminated in a unit resistor. This process for approximations used to deal with higher order of fractional capacitors whereas classical iterative methods did not even exist. The Newton process generated rational functions of the nth root of $1/s$. Thus, a fractional capacitor of nth order formally suggested and investigated first time in the literature.

Until 1967, there have been few more studies in particularly; K. Steiglitz [106] has suggested a rational function approximation while Lerner employed a passive building block, C. A. Hesselberth has investigated the lumped equivalent of Morrison's RC circuits [107] (Foster-type network). However, these networks were on the theoretical interest only, because they were very difficult to fabricate the structure with present day materials technology. In 1966, Suhash C. Dutta Roy [23] pioneered the lumped element model of RC networks whose impedance has –45° and is suitable for fabrication in micro-miniature form using thin film techniques. Later on, he detailed this work [108] on non-uniform networks based on continued fraction expansion (CFE) and compared between cascaded networks and rational function approximations. Moreover, the approximation of $(1+s^{\pm 1})^{\pm \lambda}$ at low and high frequencies with suitable networks were discussed. Elliptic functions and an equiripple approximation were used. However, this study suffered from the computational difficulties of the approximations and realization complexity.

In 1973, Keith B. Oldham proposed a circuit having two stages; resistive-capacitive

line subdivided into *n*-equal segments and each segment is replaced by a “T” element composed of two resistors and a capacitor [109]. Then, the geometric ladder was generated by a similar two stage process, only being different from the initial subdivision into unequal segments. The proposed circuits were adopted for any order. Resistances and capacitances selected according to geometric progression that makes calculations much simpler and providing uniqueness to this method.

Between 1975 and 1981, the synthesis of the transfer functions were led to eight recursive arrangements of RC or RL cells ensuring a non-integer order, no longer limited to an half, but being orders between either 0 and 1 or 0 and −1 [110]:

- a parallel arrangement of series RC cells;
- a series arrangement of parallel RC cells;
- a cascade arrangement of gamma RC cells;
- a parallel arrangement of series RL cells;
- a series arrangement of parallel RL cells;
- a cascade arrangement of gamma RL cells.

J. C. Wang, in 1987, made a study [111] based on some of the results of Schrama's thesis [112]. He proposed a systematic way to construct RC transmission lines and ladder networks that had generalized Warburg impedance. The main outcome was to show non-constant resistance and capacitance per unit length of the line, while still referring the term “Warburg impedance”. Specification of the starting points of the transmission lines in this study made it different than Schrama.

In 1992, A. Charef et al. proposed to approximate the fractional power pole [24], [113]. Using a simple graphical method, the zeros and the poles of the approximation for a specified error in dB were found to be in a geometric progression form, which is called “Charef’s method”. In same year, M. Nakagawa and K. Sorimachi proposed a circuit which has a fractal structure (tree fractance) [114] composed of resistances and capacitors. The impedance of the element described as $Z(j\omega) = (R/C)^{1/2}\,\omega^{-1/2}\exp(\pi j/4)$. Eventually, the presented structure used in a fractional integral circuit as well as a fractional differential circuit and confirmed that output wave forms agree well with those derived from a computer simulation. K. Matsuda presented an approach in 1993 for designing broadband compensator that applies the $H\infty$ control theory [115]. In 1995, A. Oustaloup developed a new system called the CRONE suspension [116], [117] from the link between recursive and non-integer derivation. The non-integer derivation, by using *n* elementary spring-damper cells whose time constants were distributed recursively, was synthesized based on a frequency interval. However, the quality of the Oustaloup’s approximation may not be satisfactory in high and low frequency bands near the fitting frequency bounds and is restricted with odd orders. In 2006, this problem was solved by D. Xue et al. [118].

In 2002, M. Sugi et al. have investigated self-similar ladder circuits with RC elements (domino-type), forming a geometric progression as simulating the fractional impedance with various orders [119]. The claimed advantage with these self-similar circuits over those corresponding optimized circuits is the characterization of one single optimum pole interval determined by the distributed-relaxation-time models. The eighteen sections or less were used to realize half-order element in five decades bandwidth. In 2005, P. Yifei et al. in their work have analyzed a tree type network of

classical half-order FOE resembling neural networks and also proposed three new configurations [120]; half-order net-grid type, half-order two-circuit series, and half-order *H*-type. In 2008, A. A. Arbuzov et al. presented the three-dimensional self-similar RC models [121] of the electric double layer and electrolytic medium that gives the fractional impedance response. The complex conductance of circuits consists of fractional-power expressions with real and complex-conjugated exponents were shown. The dependence of the order on the resistance and capacitance was reduced. Moreover, the fractional order related with the dynamic fractal dimension which gives a new geometrical meaning.

In 2011, J. Valsa et al. [122] showed a systematic way to simulate the properties of a FOE in a desired frequency range with good accuracy. The method works for arbitrary orders of the fractional order operators. The parallel connected of series *R*-*C* elements was used with parallel, single resistor and capacitor as correction elements. The presented approach was based on recursive algorithm (RA) that allowed setting initial values from standardized ones. Therefore, the remaining network values were close to standard passive elements. Again in this year, D. Sierociuk et al. introduced a new structure called the nested ladder. Together with the known domino structure, both studied types of electrical circuits provided the first known examples of circuits, which were made of passive elements only and exhibited in the time/frequency domain behavior of variable order [123], [124]. While the frequency dependent parameter was obvious from Bode plot, the variable order behavior of considered circuits in time domain was designed with help of Mittag-Leffler function as a link between data fitting and fractional-order differential equations. In 2014, R. El-Khazali proposed a biquadratic approximation to fractional order differintegral operators [26], [125]. The circuit was synthesized with series RC and RL networks. The performance of the structures showed better results than equiripple and Oustaloup's approximations. However, the obtained passive values were not so realistic.

There are available other structures that validate the passive and active analog realizations of fractional-order impedances. For instance; composed of a FOC and some RLC components [126], active cells such as operational amplifiers, operational transconductance amplifiers, current conveyors, and current feedback operational amplifiers [19], [127], [128], weighted sum of first-order high-pass filters [129] and many others [130]-[132].

2.1.2 Boundaries and Constrains

Various passive electrical networks are used to realize the fractional impedance. The irrational input impedance is represented commonly in terms of a rational transfer function [62]. Therefore, to implement these functions and obtain the passive network component values there are several conditions:

- The transfer function must be real for real Laplace operator *s*.
- The transfer function possesses distinct features in the complex plane with negative real poles located in the open left-side of *s*-plane.
- The input impedance Z(*s*) pole or the input admittance Y(*s*) zero should be the closest to the origin of the coordinates.

Validating the conditions in above, there are also several drawbacks:

- Approximated rational functions require complex mathematical analysis.

- Constrained optimization to identify the network.
- The value of the components are not well-scaled and negative values may be obtained, in which case one would need to use negative impedance converters.
- Obtained values have to be approximated to closest a standardized value which leads to overall degradation of the performance of the FOE.
- High numbers of elements are used for low phase error, in which clearly requires increased branch number thus high-order transfer functions.
- High numbers of elements also requires large circuit layout which results in extra parasitic due to the transmission line effects especially at high frequencies.

Therefore, a systematic way should be followed as:

- Use a suitable approximation technique to obtain the impedance in the form Z(*s*) and develop it into a suitable expansion, thus obtain *R* and *C* component values.
- Use an appropriate network to reduce phase ripple at low-, mid- and high-frequencies. Thus, the network should be selected according to frequency range of application.
- Use an evolutionary approximation technique to optimize the design specifications such as: phase, order, phase ripple, frequency bandwidth, and passive element values.

Additionally, fractional-order calculus operations have been simulated by digitally approximating the problems and calculating approximate solutions. Digital approximations are necessarily limited in bandwidth, highly consumptive of computer resources, and can suffer from numerical instabilities due to finite precision arithmetic. We would also be faced with the problem that the amount of memory required would be dictated by the values of the exponents and coefficients. These limitations can make digital techniques impractical or incapable of solving many problems, such as controlling fast processes, which involve strong opposing forces [126]. Thus, another study should continue on this way.

2.2 Development of Fractional-Order Devices

An ideal dielectric in a capacitor would violate causality. Thus, it is typical to look for dielectrics for instance “low-loss" dielectrics for the order “α” of *s* as close to unity as possible, as the exponent is directly related to the constant phase angle. This can be explained in electrical engineering as the frequency dispersion of capacitance by dielectric relaxation, where the electric current density follows the change of an electric field with a delay [134]. A wide range of relaxation phenomena is associated with interfacial processes in metal–insulator, semiconductor–insulator, electrode–electrolyte and similar systems. Therefore, Andrew K. Jonscher expressed the principle of “universality” of dielectric response and defined the following principal dielectric functions [69]:

- The complex permittivity $\tilde{\varepsilon}(\omega)$ and susceptibility $\tilde{X}(\omega)$,

$$\tilde{X}(\omega) \equiv \left[\tilde{\varepsilon}(\omega) - \varepsilon_{\infty}\right] / \varepsilon_0 = X'(\omega) - jX''(\omega), \tag{2.3}$$

where ε_0 is the permittivity of free space, ε_∞ is a suitable high-frequency permittivity and the physical emphasis is on the real and imaginary components of the polarization.

- The dielectric modulus, which is the reciprocal of ε_∞,

$$\tilde{M} = M'(\omega) + jM''(\omega) = \frac{1}{\tilde{\varepsilon}(\omega)}$$
$$\frac{1}{\tilde{\varepsilon}(\omega)} = \frac{\varepsilon'(\omega) + j\varepsilon''(\omega)}{\left[\varepsilon'(\omega)\right]^2 + \left[\varepsilon''(\omega)\right]^2}, \tag{2.4}$$

which emphasizes series processes that may be acting in the material.

- The complex capacitance

$$\tilde{C}(\omega) = (A/d)\,\tilde{\varepsilon}(\omega), \tag{2.5}$$

which relates to a sample of planar geometry of area *A* and thickness *d*, or some other appropriate geometrical factor for other geometries. Susceptance is the quantity corresponding to susceptibility,

$$\tilde{X}(\omega) = \tilde{C}(\omega) - C_\infty. \tag{2.6}$$

Their use is recommended wherever the geometry of the sample is not well defined. They both emphasize parallel processes acting in the sample.

- The admittance of the sample representing the equivalent parallel conductance $G(\omega)$ and capacitance $C(\omega)$,

$$\tilde{Y}(\omega) = I/V = j\omega\tilde{C}(\omega) \equiv G(\omega) + j\omega C(\omega), \tag{2.7}$$

The frequency dependence of these elements arises from the fact that they represent an equivalent circuit of a system that is not necessarily a parallel combination of frequency independent elements.

- The impedance of the sample which is the reciprocal of admittance,

$$\tilde{Z}(\omega) = V/I = 1/\tilde{Y}, \tag{2.8}$$

which emphasize series processes.

Then, the obtained data can be represented by commonly in two-ways:

1. Plots of the real and imaginary components in logarithmic scale against frequency. The log-log form is particularly useful in representing dielectric functions which are often power-law functions of frequency:

$$\tilde{X}(\omega) \propto (j\omega)^{n-1}, \text{ where } 0 < n < 1. \tag{2.9}$$

In the frequency region above any loss peaks, this referred to as the “universal” law.

2. Polar plots of the real and imaginary components in linear scale against frequency. These plots are limited mainly to rudimentary diagnostics, to

characterization by shape as Debye, Cole-Cole etc. as means of finding series combinations of elements in *Z* plots.

This statement clearly shows that an ideal capacitor cannot exist in nature. Considering also the definition of Warburg impedance, the impedance varying as the square-root of frequency, several FOCs are designed and fabricated. Many of the studies are done after 1990s since the connection between math's and physical properties of materials established after this year [12].

2.2.1 Materials and Structures

In the early 1960s, by R. Sh. Nigmatullin et al. proposed a FOE called as electrochemical converters of information (ECCI) that contains two platinum electrodes encased into a vacuum-sealed glass bulb filled with water solution of potassium ferrocyanide $K_4[Fe(CN)_6]$ and potassium ferricyanide $K_3[Fe(CN)_6]$ with same concentration [62]. Their practical use to perform fractional half-order integrator and differentiator were demonstrated. However, the presence of liquid electrolyte and the need to vacuum and seal the electrochemical diode container made it difficult to use this device as compact components produced via the integrated circuit technology. Later on, same group fabricated a temperature sensitive solid electrolyte type FOE using a rubidium silver ionide ($RbAg_4I_5$) as solid insulator [62]. The order was tunable between 0.64 and 0.82 with temperature change from –20 °C to +50 °C. Another study was the fabrication of the half-order resistive-capacitive elements with distributed parameters (RC-EDP, semi-infinite RC transmission line) by means of film and semiconductor (bi-polar transistor, MOS) structures [62], [135]. The schematic methods include variation of interlayer connections and variations of connection layout. Their size was significantly small, thermally stable and their precision of modelling the features of an ideal RC cable was higher. Furthermore, their parameters can be adjusted using physical magnetic fields on the corresponding sensitive materials of resistive and dielectric layers.

T. C. Haba et al. [136], [137] demonstrated that it is possible to create fractional order impedances in the range of 100 kHz − 10 GHz by fabrication of a fractal structure on silicon substrate. In1998, Samavati put a similar study like Haba et al. [138].

In 2002, G. Bohannan introduced the FOE design using fractal geometry properties of the electrode-electrolyte interface [139]. The device had sandwich type constituted by two parallel copper electrodes separated by one conducting plate both side with electrolyte. The conducting plate required to specify the order. Ionic gel with Lithium Nitride and Tetraethy-Ortosilicate was used as electrolyte. The phase angle varied from −30° to −60° with phase angle deviation of ±5° over five decades of frequency range. This FOE was able to operate over low- and infra-low frequency ranges (from Hz to kHz) due to the diffusion and drift of the electrolyte ions. The device was packaged and demonstrated in controller. On the other hand another study reported by G. Bohannan et al. in 2006 [133] using nanostructured materials for instance $[NH_2BU_2]_x[Pt(Ox)_2]$. The device covered wide frequency range (4 decade) but suffered from high phase ripple (approximately 5), small phase angle from −13° to −18°. In 2008, next study was reported by developing lithium ions on the rough surface of metal electrodes [140]. However, by this method, it is not easy to reproduce a FOE with desired specifications.

In 2006, K. Biswas et al. developed a liquid electrochemical FOC [141] and showed its application in fractional order differentiator circuit. The constant phase

response was taken by dipping the poly-methyl-methacrylate (PMMA) coated Cu/Pt electrode in polarizable medium (solution). The constant phase angle was observed over a frequency range of about one decade (200 kHz − 1 MHz). This device is low cost, easy to fabricate. The major advantage of the proposed device is that, varying the conductivity of the polarizable medium and depth of insertion so that constant phase angle behavior can readily be obtained in different orders (from –15° to –60°) [142] however it is not compatible for circuit applications and suffers from high phase ripples (from 6° to 15°).

In 2008, I. S. Jesus and J. A. Tenreiro Machado implemented the electrodes through one-sided cooper-based printed circuit boards with the fractal geometries cases with a dimension from 1 up to 2 for instance; the curve of Koch (FDim = 1.262), carpet of Sierpinski (FDim = 1.893), curves of Hilbert (FDim = 2.000), and Peano (FDim = 2.000) [142]. Therefore, fractal structures were adopted in an electrolyte process. They investigated the influence of several factors: FDim, different sodium chloride solution concentrations and the introduction of a fractal material in the solution. The experimental results demonstrate the possibility to get FOEs by adopting non-classical electrodes but suffered from high-dimension issue and reproducibility of specifics.

In 2011, M. S. Krishna et al. realized a FOC by dipping a capacitive type probe into the PMMA-choloroform solution for particular thickness and then used spin coating technique [143]. The electrochemical based capacitor enables only a limited phase variation of –12° to –6° by controlling the depth of the electrode immersion. Moreover, the thickness, uniformity, and stability of the porous film, on the electrode, are responsible for different orders [144]. Clearly, this method does not allow integration with current microelectronic systems or printed circuit boards and works in narrow bandwidth with low phase angles.

A realization of compact and stable electrostatic fractional capacitors is reported by Elshurafa et al. in 2013 [145]. It is fabricated by using percolated polymer composites in which the matrix is a dielectric polymer and the filler is graphene (rGO) nanosheets. Its tunability was shown with in total five fractional capacitors that were fabricated, in which the graphene weight loading tune from 2.5% up to 12%. Phase angles varied from –67° to –31°, corresponding to order of 0.73 to 0.33, respectively. The operating frequency range was 50 kHz – 2 MHz. The main advantages are its small size and PCB compatibility. However, the fabrication technique is complex and costly.

Ionic polymer metal composites (IPMCs) composed of a perfluorinated ion-exchange membrane, Nafion 117, which was surface-composited by platinum via chemical process proposed by R. Caponetto et al. in same year [146], [147]. Both sides were metallized with a noble metal to realize the electrodes. IPMC device in $1\ \text{cm} \times 1\ \text{cm}$ mechanically fixed within a Plexiglas sandwich that allows neglecting its electromechanical properties and FOC using on the electrical behavior. Two different IPMCs with different platinum absorption times (5 h and 20 h) showed the fractional-order dynamics in the frequency range of 1 Hz – 100 Hz and 1 Hz – 10 Hz with an orders of 0.05 and 0.3. This solid/semisolid FOC is useful in low frequency zone however emulates only quite small orders.

In 2015, A. Adhikary et al. developed an electrochemical type FOC [148]. A composition of 4,4’-(4,4’-isopropylidene di phenoxy) bis (phthalic anhydride) (BPADA) and m-phenylene diamine (mPD) (BPADA-mPD polymer) with carbon nanotube (CNT) in DCM solution was coated on the surface of Cu electrodes by dip

coating technique. By varying the percentage of CNT in polymer-CNT composite and the nature of polarizing solution, two different types of FOEs have been realized. Probe coated with BPADA-mPD + 1% CNT has constant phase zone of five decades (20 Hz – 2 MHz) with a ripple of –2° only. However, a proper packaging scheme needs to be developed. Its longevity and design parameters for tunability must be studied in deep.

The fabrication of a solid-sate, multi-walled carbon nanotube (CNT) -epoxy resin nanocomposite FOC which provides constant phase zones of two decades in the range of 100 Hz – 20 MHz is introduced by D. John in 2017 [149], [150]. The upper and lower plates (1.5 cm × 1.5 cm × 0.02 cm) made of copper act as the electrodes. Middle copper plate (1 cm × 1 cm × 0.02 cm) coated with the porous PMMA film was inserted to enhance the distributive nature of the electron flow from one plate to the other. It has been observed that as the percentage of CNTs loading increases, the CPA increases from –85° to –45° above the frequency range of 100 Hz. The developed device is compact and it can be easily integrated with the electronic circuits.

A systematic way to design and fabricate solid state bilayer FOCs using different polymer and composites solutions as filler has been followed by Agamyrat et al. Au-covered, 2 cm × 2 cm Si/SiO_2 wafers were used to fabricate the FOC by drop-casting the composite solution. In total, three different polymer and composite solutions labeled polyevinelidenefluoride P(VDF) –trifluoroethylene P(VDF-TrFE) -chlorofluoroethylene P(VDF-TrFE-CFE) are prepared in the study of 2017 [84]. The constant phase angle from –83° to –65° in the frequency range of 10 kHz – 10 MHz tuned by mixing the polymers. Later on, the tunability of the devices has been shown based on the thickness and ratio of the layers [79]. A FOC where the filler made of ferroelectric P(VDF-TrFE-CFE) terpolymer containing CNTs was developed [151] in 2018. Changing the weight percentage of CNTs, the constant phase angle range from –65° to –7° in the fixed constant phase zone of 150 kHz – 2 MHz. The latest study was done by the same group in same year by using the molybdenum disulfide (MoS_2)-ferroelectric composites [87]. The resulting FOC's bandwidth is in 100 Hz-10 MHz where the variation in the phase angle is no more than ±4°. The constant phase angle can be tuned from –80° to –58° by changing the type of the ferroelectric polymer in the composite and the volume ratio of MoS_2. K. Biswas et al. in 2018 has been realized a FOC based on carbon black-Sylgard nano-composites [152]. The investigated devices were characterized by the same carbon black mass concentration, while differed for the curing temperature. The accurate impedance responses were obtained at higher temperatures that showed for the production procedure to realize bulky and rigid devices. The fabricated device is also quite large, requires larger orders, mostly higher than 0.7. Average CPZ was observed over three decades of frequency ranging from 10 Hz to 100 MHz. The low pass application of the fabricated devices was studied in [153].

As summary, use of polymer-based dielectrics, simple and low-cost fabrication processes, and PCB compatibility makes FOCs attractive for circuit designers. However, fabricated FOCs have small capacitance and its tunability needs to be studied in further.

2.2.2 Boundaries and Constrains

The fabrication of FOCs based on different insulating layer and conducting electrodes have been reported. They can be categorized as liquid, solid and semi-solid fractional order capacitors based on the insulating layer. Materials as insulating or semi-insulating

layer might include liquids, inorganic glasses, electrolytes, ionic conductors, dielectrics, gate insulators of electronic devices, amorphous semiconductors, polymer melts and solutions, amorphous polymers, epoxies, ferroelectrics, biopolymers etc. The desired structure on electrodes can be provided by using the intensively developed methods of surface treatment with concentrated energy flows (laser, plasma, and electric-discharge treatment) using nanotechnology processes such as chemical assembly, sol-gel processes, vapor-phase deposition of metals, and atomic layered epitaxy. These different methods of emulating the fractional impedance provide opportunities to produce FOEs for a wide frequency range with various orders. However, to make such components as widely used as the conventional passive components, it is necessary to satisfy the design and the technology with the following requirements:

- Compatibility with manufacturing technology of semiconductors or thin-film integrated circuits.
- Constant phase response for a wide frequency spectrum.
- Fractional impedance dependence on the maximum range of allowed order "$0 < \alpha < 1$".
- Precise adjustment of the fractional impedance parameters and characters, especially the control on pseudocapacitance "C_α".
- Capability of parameter dynamical adjustment.
- Suitable packaging for circuit applications.
- Size in terms of electrodes.
- Longevity of the lifetime.

Fractional elements based on electrochemical converters with liquid electrolyte are hardly compatible with modern integrated circuit technologies however obviously advantageous from their capability of working ultra-low frequencies. On the other hand, the semiconductor based FOEs also have good potential, especially due to the small size and capability to control parameters with electric field, motion of dipoles, dielectric properties, relaxation time and its distribution etc. Nevertheless, there is no precise method to fabricate fractional impedances with a desired and accurate value of fractional order. This problem is caused by the difficulties associated with recording the surface and volume effects in the semiconductor crystal and the interaction of the integrated circuit elements.

2.3 Summary

Since appearance of works by Mandelbrot on the fractal nature of real objects and development of the fractional calculus, many physical phenomena were given a clearer and more comprehensive explanation. By assuming self-similar structure of the medium and/or processes occurring in it, it becomes possible to get insight into the phenomenon of universal dielectric response observed by A. Jonscher in many physical systems and also to explain the electric properties of the interface of a metal electrode with a solid electrolyte. A substantial stimulus to further studies is the possibility of carrying out numerous theoretical studies. Recent decades were marked by the development of passive and active FOEs and fractional dimensionality, as well as different models of fractal electrodes describing the processes in electrochemical cells. As the models in

these studies, the equivalent self-similar (fractal) circuits are considered. Note that an electric dipole can be considered as a certain elementary capacitance, while the elementary motion of charge carriers in a resistive medium can be associated with a certain value of Ohmic resistance. This can be explained in detailed with Debye model [154], [155]. The Debye response is obtained for an assembly of non-interacting ideal dipoles or identical dipoles which have the same waiting time before making a transition, or have a loss of energy proportional to frequency, respectively. The latter is the original Debye model of dipoles floating freely in a viscous medium. The Debye response is also obtained with a series combination of a frequency-independent capacitance C and resistance R which give the peak frequency $\omega_p = (R \cdot C)^{-1}$. This becomes relevant with the appearance of an interfacial capacitance in series with a bulk region, which constitute the basis of the Maxwell–Wagner model.

Various approaches to realize FOEs obey the above statements. However, there is still need the find explanation for many missing points. Therefore, the chronological literature survey has been made in this part. The growth of circuit network realizations of FOEs are almost reached the saturation line. However, with the discovery of the electrical properties of materials, fabricated liquid, solid/semi-solid FOEs have been a major field of research and application in last 20 years. As seen from the various accounts of the FOE realizations, a standard and optimized device still is far from being a reality. A standard FOE employing in various electronic circuitries would propose a new era of devices with precise and robust control than already existing integer-order ones. In addition to these, an optimal design of the FOEs might be obtained by having dynamic tunability features. The fractional-order, constant phase zone, pseudocapacitance or pseudoinducntance can be set by tuning the circuit parameters e.g., voltage, current, frequency. This can happen by using transistor base active building blocks with the conventional IC fabrication technologies. Therefore this could be another area to investigate.

3 SYNTHESIS AND OPTIMIZATION OF FRACTIONAL-ORDER ELEMENTS USING A GENETIC ALGORITHM

Up until now, evolutionary computing algorithms have been used to reduce the drawbacks in traditional optimization methods and to solve complex problems where conventional techniques fail in many areas of the fractional-order domain such as chaos [156], control [157], or extracting the design parameters of filters [158]. In this regard, flower pollination algorithm [159], particle swarm optimization [160] etc. are used.

In this chapter, a mixed integer-order GA in MATLAB® is employed [161]. Instead of approximating s^{α} using the mentioned approximations in Chapter 2 at a certain frequency (or bandwidth), we optimize the phase and/or impedance responses of RC/RL networks in the whole desired frequency range. Furthermore, the required values are obtained with GA, even if the passive component values are restricted to commercially available kit values defined by standard IEC 60063. Hence, this chapter aims to introduce an FOE optimization method that achieves a broad operating frequency range with CPA deviation of approximately ±1° using commercially available passive component values in RC and RL structures with five branches of Foster-I, Foster-II, Cauer-I, Cauer-II, and Valsa networks. Most crucially, the presented approach avoids the use of negative component values, GICs, or random passive element values. Thus, the best optimal emulation of an FOE is introduced currently available in the literature. In particular, Foster-II and Valsa networks are selected as our main objective, because the former offers a minimum total capacitance value and the latter provides a minimum CPA deviation. Here it is also worth noting that, to the best knowledge of the author, an FOI design using the listed five RL networks is studied for the first time in the open literature.

3.1 Description of the Genetic Algorithm Approach

The GA is a powerful computational technique, which mimics the process of natural selection theory. It consists of a population of representations of candidate solutions to an optimization problem, which evolve toward enhanced solutions. It is important to mention that the GA uses the objective function itself, not derivatives or other auxiliary knowledge based on probabilistic/deterministic characterization. These features make this optimization method the most suitable technique to optimize the CPA in distributed RC/RL networks.

Tab. 3.1 summarize the FOC and FOI approximation methods used in this work with their synthesized RC and RL networks and equivalent admittances or impedances. The admittances of some of the RC networks can be found in [62], [162]. The impedance and phase optimization of all structures using the GA is obtained with predefined R and C values. The desired constant phase and/or pseudocapacitance, pseudoinductance, number of branches, and frequency range (i.e. CPZ) are defined as design parameters.

To provide more detail regarding the exact steps that were performed by the GA approach, its pseudocode in Algorithm 1 based on [161] is presented. Tab. 3.2 presents the parameters employed during the training phase of the GA approach. Fitness, also

known as the cost function of the solution set, is determined using the following equation:

$$F = \left| \varphi_{\text{sim}} - \varphi_{\text{targ}} \right|, \tag{3.1}$$

where φ_{sim} and φ_{targ} express the simulated and target phase, respectively. The flow of steps can be divided into five parts:

Initialization: Once the genetic representation and the fitness function (desired phase angle value) are defined, the GA randomly proceeds to initialize a population of solutions from predefined *R* and *C* values. The random indices (gene: a single encoding of part of the solution space) from the available resistors and capacitors are assigned to create a solution (chromosome: a string of genes that represent the solution), and population (possible solution sets) is created around the assigned genes.

Evaluation: The evolution starts from a population of randomly generated individuals and continues with evaluation of the fitness. Fitness, also known as the cost function of the solution set is given in the following sections.

Selection: In each generation, not only the fitness of every individual in the population is evaluated, but also several individuals are stochastically selected from the current population and modified to form a new population. The new population is then used in the next iteration of the algorithm.

Breeding: Produce new individuals by using genetic operators on the individuals chosen in the selection step. The GA improves it through the repetitive application of mutation and crossover.

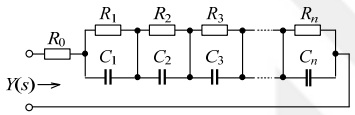
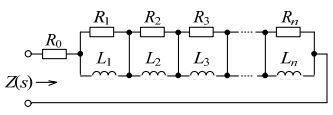
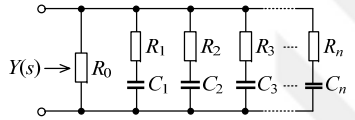
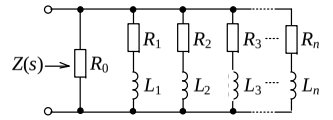
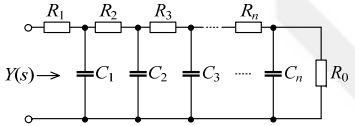
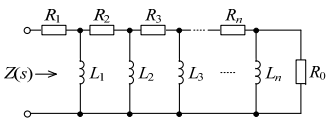
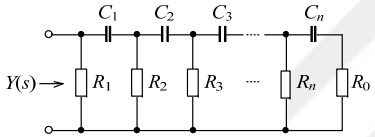
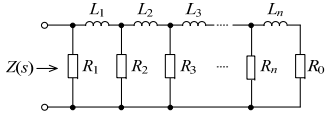
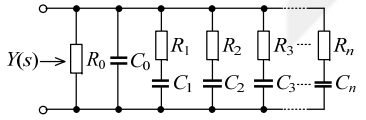
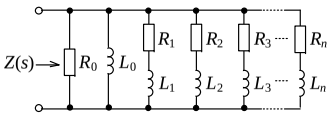
Population update: The GA terminates until:

1. The maximum number of generations is produced.
2. Satisfactory fitness level has been reached ($F = 0$).
3. No progress in fitness value of population within defined stall generation number.

Algorithm 1: Genetic algorithm pseudocode

```
for i = 1 to NumOfGenerations (or until an acceptable solution is found) do
  if first generation, then
    Generate the initial population with primitives
    (CPZ, CPA, pseudocapacitance, pseudoinductance, number of branches,
    resistor, capacitor, and inductor set)
  else
    With current population, generate a new one using crossover and mutation
  end if
  Calculate fitness of population members
    if fitness ≠ 0 then
      Return to generate new population
    else
      Break the loop
    end if
end for
Return best individual in last population
```

Tab. 3.1: FOC and FOI approximation methods used in this study (Note: All bellow networks are optimized using GA)

FOC Approximation			FOI Approximation		
Method	Admittance, $Y(s)$	RC Network	Method	Impedance, $Z(s)$	RL Network
Oustaloup	$Ck_f \prod_{i=1}^{n} \frac{1+(s/\omega_i')}{1+(s/\omega_i)}$ [22]	 Foster-I	GA	$R_0 + \sum_{i=1}^{n} \frac{sL_iR_i}{R_i + sL_i}$	 Foster-I
CFE	$\frac{1}{R_0} + \sum_{i=1}^{n} \frac{sC_i}{sR_iC_i + 1}$	 Foster-II	GA	$\frac{1}{\frac{1}{R_0} + \sum_{i=1}^{n} \frac{1}{R_i + sL_i}}$	 Foster-II
CFE	$R_1 + \frac{1}{sC_1 + R_2 + sC_2 + \cdots \frac{1}{sC_i + R_0}}$	 Cauer-I	GA	$R_1 + \frac{1}{\frac{1}{sL_1} + \frac{1}{R_2 + \frac{1}{sL_2} + \cdots \frac{1}{sL_i} + \frac{1}{R_0}}}$	 Cauer-I
CFE	$\frac{1}{\frac{1}{R_1} + \frac{1}{sC_1} + \frac{1}{R_2} + \frac{1}{sC_2} + \cdots \frac{1}{sC_i} +} R_0$	 Cauer-II	GA	$\frac{1}{\frac{1}{R_1} + sL_1 + \frac{1}{\frac{1}{R_2} + sL_2 + \cdots sL_i +} R_0}$	 Cauer-II
Recursive Algorithm (RA)	$\frac{1}{R_0} + sC_0 + \sum_{i=1}^{n} \frac{sC\varepsilon^i}{sCR + (\eta\varepsilon)^i}$ Note: η is capacitance and ε is resistance scaling factors [43], [168]	 Valsa	GA	$\frac{1}{\frac{1}{R_0} + \frac{1}{sL_0} + \sum_{i=1}^{n} \frac{1}{R_i + sL_i}}$	 Valsa

Tab. 3.2: Genetic algorithm parameters

Run parameter	Value
Population size	100
Max. stall generation	125
Max. generation	10 000
Input variables	6
Crossover probability	0.5
Commercially available resistor kits	YAGEO RC-0603-FR-07 E96 Kit [163] and Vishay 0402 [164]
Commercially available capacitor kits	muRata C0603 [165] and Kemet 0402 [166]
Commercially available inductor kit	Coilcraft 0603 ceramic inductors [167]

3.2 Optimization and Verification of FOC

As an exemplary study, primarily the Foster-II [162] and Valsa [168] networks are optimized within this section. For the reason that; Foster-II network offers a minimum total capacitance value and Valsa network provides a minimum PAD.

3.2.1 Optimization of Foster-II Structure

For a Foster-II realization, the component values are given by the partial fraction expansion and its admittance is expressed in Tab. 3.1. Here, n is the number of branches, R_0 is the initial resistor, and R_i and C_i are the resistances and capacitances of i-th branch. Firstly, the performance of the network obtained using the GA with the Oustaloup and CFE methods is compared to show the advantage of the GA. The desired bandwidth, number of branches which is equivalent of a fifth-order admittance function ($n = 5$), and CPA are respectively set as 100 Hz – 1 MHz, 5, and –45° with a pseudocapacitance of $C_\alpha = 100\ \text{nF}\cdot\text{s}^{-0.5}$. As a population, the random and commercially available passive elements defined in Tab. 3.2 are used. The central frequency in case of CFE is set to 10 kHz. It can be observed from Fig. 3.1(a) that all three approximations provide a constant phase response with target CPA near a central frequency, specifically between 1 kHz and 100 kHz. However, errors in phase for the approximation models increase significantly when the frequency is 2 decades above and below the central frequency, whereas the phase response obtained using the GA is satisfied in the whole frequency range of interest. Furthermore, Fig. 3.1(b) shows relative phase errors and corresponding normalized histograms (%) of phase angle deviation from CPA as an inset. It can be seen that the maximum deviation in the GA is limited to only ±2°, whereas in both CFE and Oustaloup, ±25° errors occur. Because no direct control exists over the R and C values obtained from the last two approximations, a correction to use the commercially available RC kit values is obligatory to build the FOCs. However, this correction is not needed for the results obtained by the GA since it directly provides the standard IEC 60063 compliant RC values as the results. Indeed, it is possible to include in the population, i.e. available R and C values to MATLAB® and the GA performs the optimization using only given values. Fig. 3.1(c) shows the simulated phase response of corrected RC network values using the Oustaloup, CFE, and optimized network using

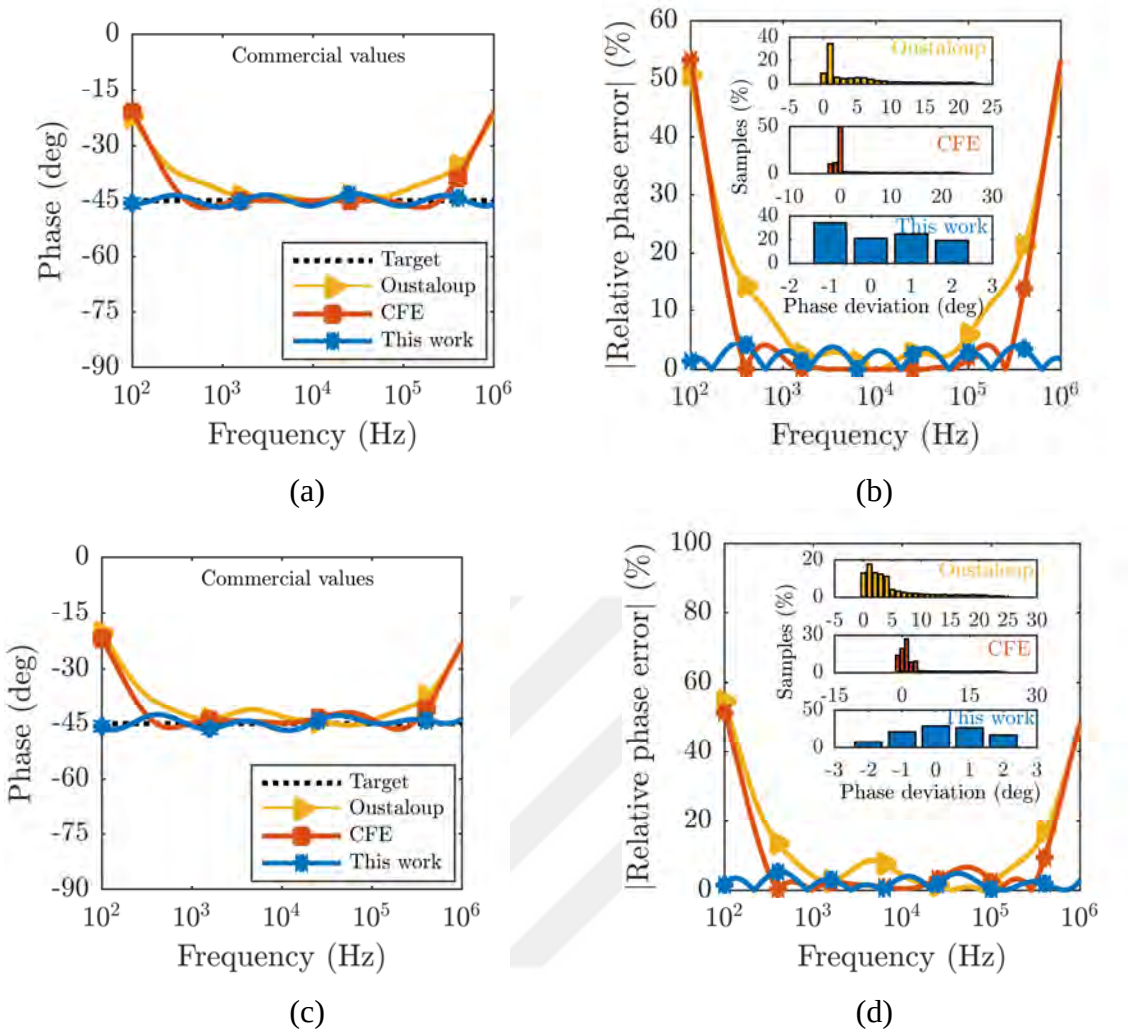


Fig. 3.1: (a) Numerical phase response plots of the Foster-II RC network using the Oustaloup, CFE, and GA methods with random values, (b) relative phase errors and corresponding normalized histograms (%) of phase angle deviation from CPA as inset, (c) phase angle response of the RC network using the Oustaloup and CFE methods after RC value correction, and the GA optimized for commercially available RC kit values, (d) relative phase errors and corresponding normalized histograms (%) of phase angle deviation from CPA as inset. Phase responses are optimized in the frequency range of 100 Hz–1 MHz

the GA, while the commercially available 0603 size R and C kit values defined in Tab. 3.2 are used. The rest of the simulation setup is identical to the simulation setup for Fig. 3.1(a). Fig. 3.1(d) plots the relative phase errors and corresponding normalized histograms (%) of phase angle deviation from CPA as an inset. As it can be observed, the maximum deviation in the GA is limited to ±2.8°, whereas ±30° error is obtained in both Oustaloup and CFE approximation results. Notably, the maximum error in the phase obtained from both approximation methods are further increased compared with the results in Fig. 3.1(b) with no RC value correction. However, no significant change is observed in the phase of the circuit obtained using the GA.

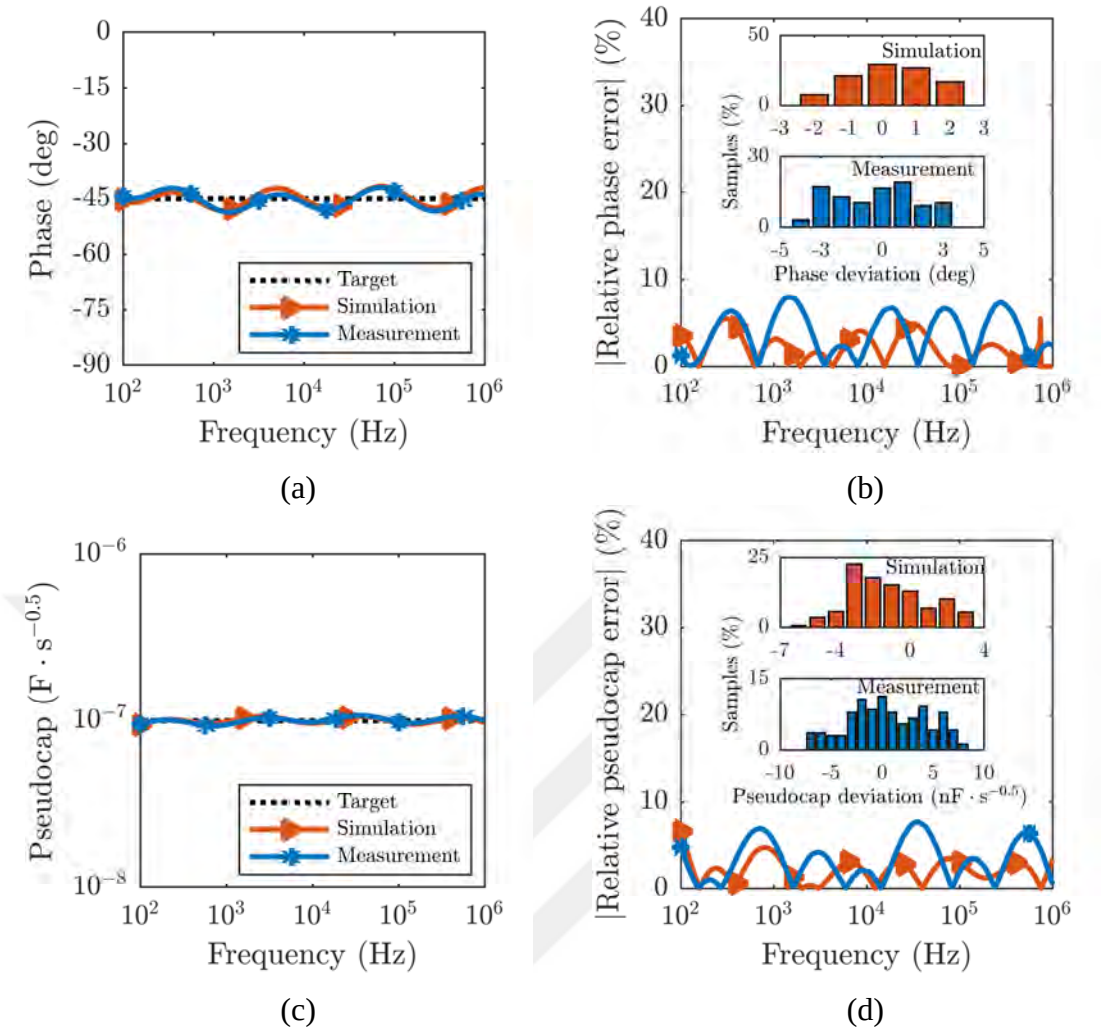


Fig. 3.2: Target (ideal), simulated, and measured (a) phase responses, (b) relative phase errors and corresponding normalized histograms (%) of phase angle deviation from CPA as an inset, (c) pseudocapacitance responses, and (d) relative pseudocapacitance errors and corresponding normalized histograms (%) of pseudocapacitance deviation from CPA as an inset, respectively, of the Foster-II network optimized using GA. Impedance and phase responses are optimized in the frequency range of 100 Hz–1 MHz

Figs. 3.2(a) and (c) show the target, simulated, and measured phase angle and pseudocapacitance responses of the RC network optimized using the GA. The same passive element values are used from the commercially available RC kits as depicted in Fig. 3.1(c) (see “This work”) with the setup listed in Appendix A. The experimental verification uses the Agilent 4294A Precision Impedance Analyzer. Standard calibration tests (open and short circuits) of the Keysight 16048G Test Leads are performed to calibrate the instrument. From the results in Figs. 3.2(b) and (d), it can be seen that the maximum CPA deviation between target (ideal) and simulated as well as measured values is only ±2.8° and ±3.2°, respectively, whereas the pseudocapacitance is ±6.6 nF·s–0.5 and ±7.3 nF·s–0.5.

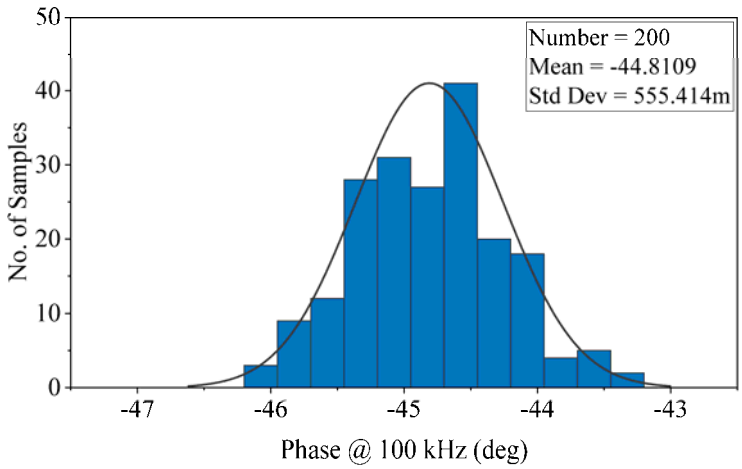
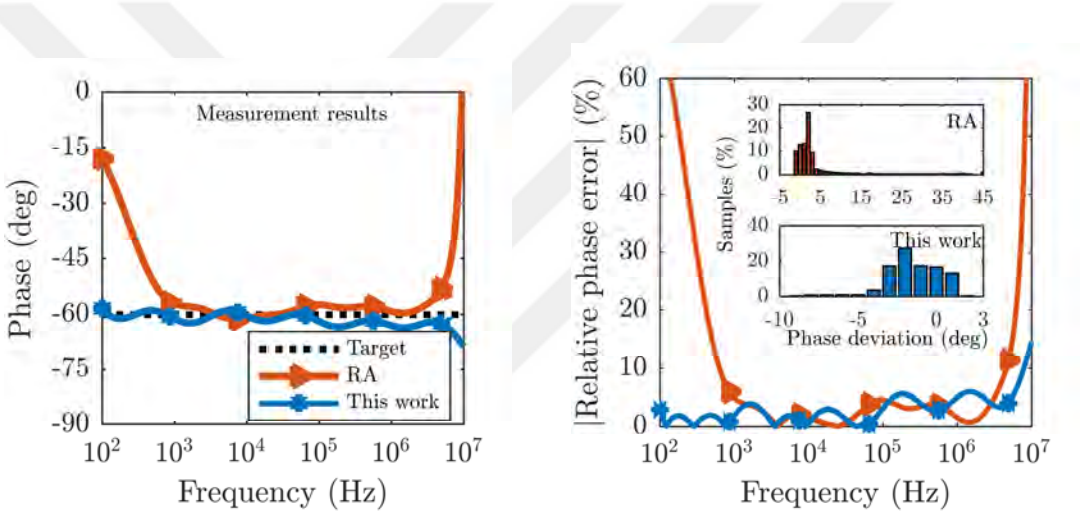


Fig. 3.3: Monte Carlo analysis: Phase variation at 100 kHz of the Foster-II network optimized using GA (values used in Fig. 3.2(a))



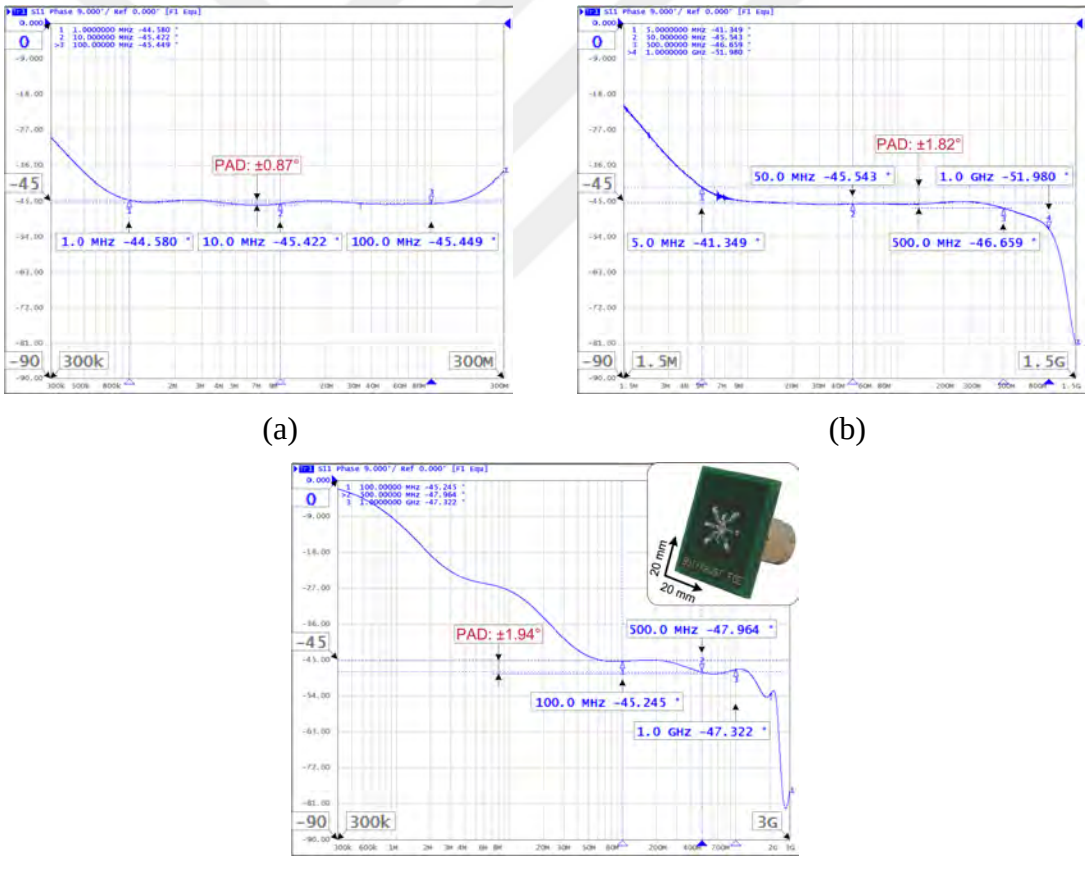
(a) (b)

Fig. 3.4: Measured phase responses of the Valsa structure using the RA and GA methods (commercially available kits are used), and (b) relative phase errors and corresponding normalized histograms (%) of phase angle deviation from CPA as an inset. Impedances are measured in the frequency range of 100 Hz – 10 MHz

Statistical analysis of Monte Carlo (MC) was performed in OrCAD PSpice® simulation software with passive element tolerances based on their datasheets [163], [165] and 200 runs to observe effects due to manufacturing processes. The histogram shown in Fig. 3.3 demonstrates the variation of the phase at 100 kHz of the Foster-II network optimized using GA. The mean value with standard deviation 0.555 is –44.8109°, which is very close to the theoretical value –45° confirming that the proposed network has low sensitivity characteristic on passive components. The analysis results of MC for all studied networks at their middle frequency are listed in Appendix A.

3.2.2 Optimization of Valsa Structure

The Valsa network in Tab. 3.1 [168] is proposed to emulate FOC behavior and realized using RA. The possibility of designing this network using commercially available *R* and *C* values was claimed by the authors [168]. However, the RA allows us to set only initial values and the remaining branch values must be adjusted according to commercially available passive element values. With this in mind, similar to with the Foster-II structure, the GA is applied to the Valsa network in this subsection. The admittance function is given in Tab. 3.1, where compared to Foster-II network the additional C_0 denotes an initial capacitor. In our study, to provide a fair comparison with [36], the phase responses of RA and the GA of an order of $\alpha = -0.67$ using commercially available 0603 size RC kit values are experimentally evaluated. The used passive element values are listed in Appendix A (see "Fig. 3.4" columns). During the experimental verification, the same instruments listed in section 3.2.1 are used. With the phase error equal to ±2.1°, the approximation with the GA experimentally reaches a wider bandwidth of 100 Hz–5 MHz, as shown in Fig. 3.4(a). Considering the full frequency band up to 10 MHz, the error is still only ±3.2° (see Fig. 3.4(b)).



(a) (b)

(c)

Fig. 3.5: Measurement results of an $\alpha = -0.5$ order FOC implemented using the Valsa network optimized using GA for two decades in different frequency ranges: (a) 1 MHz – 100 MHz, (b) 5 MHz – 500 MHz, and (c) 50 MHz – 1 GHz

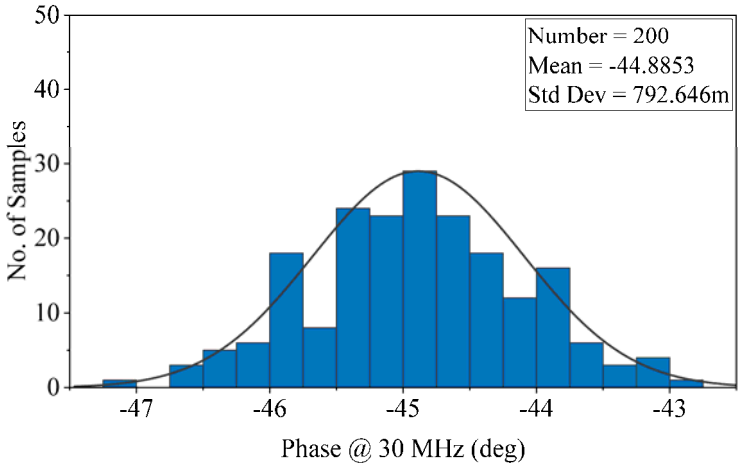


Fig. 3.6: Monte Carlo analysis: Phase variation at 30 MHz of the Valsa network optimized using GA (values used in Fig. 3.5(a))

Furthermore, the measurement results of $\alpha = -0.5$ order FOCs using an ENA Series Network Analyzer E5071C (300 kHz–20 GHz) in three different frequency ranges [case study (a) in 1 MHz–100 MHz, (b) 5 MHz–500 MHz, and (c) 50 MHz–1 GHz] are shown in Fig. 3.5. Two variants of the FOE device with dimensions of 20 mm × 20 mm were designed (for 0402 and 0603 size passive components) employing a subminiature version A (SMA) coaxial RF connector. The fabricated printed circuit board for 0402 size kit values is shown in Fig. 3.5(c) as an inset. Considering an input impedance 50 Ω of the connector, the phase is measured by defining the equation of impedance as $Z = 50 \cdot [(1 + S11)/(1 - S11)]$. As passive elements, RF-type resistors from Vishay [164] and capacitors from Kemet [166] are used. Because of the producers fabrication boundaries, used passive components having CPA in limited frequency range, operate up to a maximum of 5 GHz. In addition, this frequency range is inversely proportional to the resistance values. For instance, a 100 Ω resistor works until 8 GHz, whereas a 1 kΩ resistor has a constant zero-degree phase response up to 800 MHz and so forth. At high frequencies, the transmission line effect becomes dominant; therefore, we maintain the distance between passive elements the least. Despite the above mentioned limitations, we obtained the results until 1 GHz with low phase angle deviations as shown in Figs. 3.5(a)–(c).

MC analysis was performed in OrCAD PSpice® simulation software with 0402 kit resistors [164] and capacitors [166] with tolerance according to their datasheets, and 200 runs. The histogram shown in Fig. 3.6 demonstrates the variation of the phase at 30 MHz with values used in Fig. 3.5(a). The mean value with standard deviation 0.793 is –44.8853°, which is again very close to the theoretical value –45°.

One of the advantage of the proposed GA to design FOC is its suitability for any RC ladder topology, such as Cauer-I, Cauer-II, or Foster-I. In general, by replacing the admittance function of the desired topology, it is possible to determine the required resistance and capacitance values to build an FOC with desirable electrical properties. Notably, the list of admittances of listed networks can be found in Tab. 3.1. Fig. 3.7

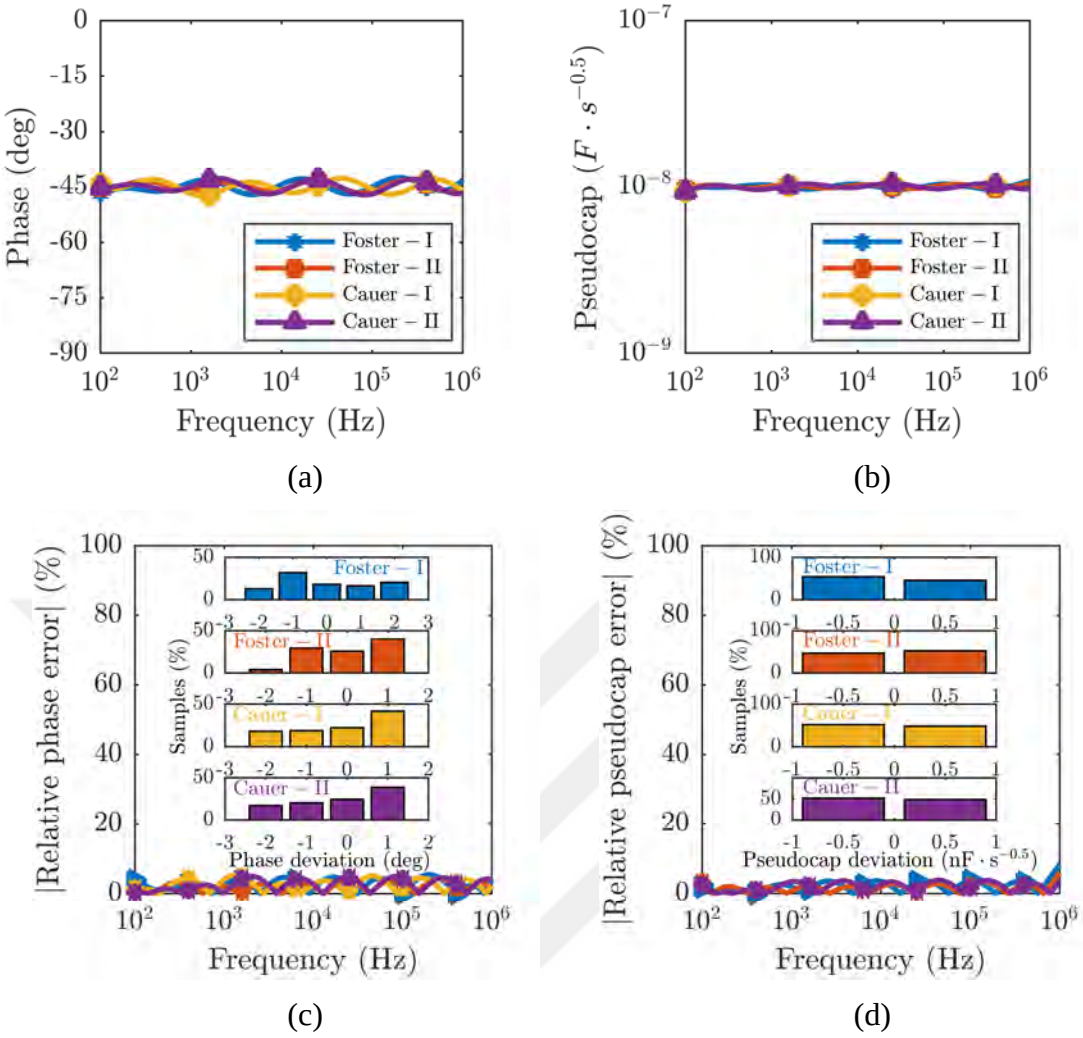
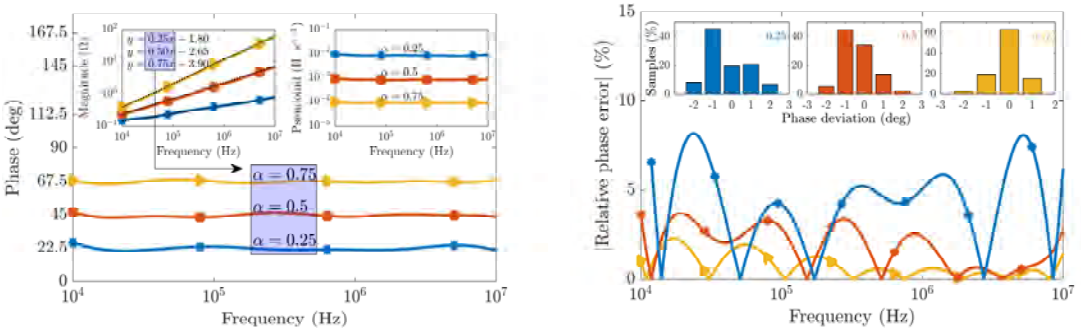


Fig. 3.7: (a) Simulated phase and (b) pseudocapacitance responses, (c) relative phase errors and corresponding normalized histograms (%) of phase angle deviation from CPA as an inset, (d) relative pseudocapacitance errors and corresponding normalized histograms (%) of pseudocapacitance deviation from CPA as an inset, respectively, of four RC networks optimized using GA. Responses are optimized in the frequency range of 100 Hz – 1 MHz

shows the phase and pseudocapacitance responses with corresponding relative errors and normalized histograms (%) of deviations of four RC topologies while the target phase, pseudocapacitance, and frequency bandwidth are set to −45°, 10 nF·$s^{-0.5}$, and 4 decades in the frequency range of 100 Hz – 1 MHz, respectively. The largest deviation between the desired and simulated phase values in all topologies is up to ±2.5° with low pseudocapacitance deviation.

3.3 Optimization and Verification of FOI

The most popular technique to mimic an inductor is using a GIC employing Op-Amps, resistors, and capacitors [19], [20], [26], [49], [57], [58], [94], [169]-[172]. However, the



(a) (b)

Fig. 3.8: Numerical simulation results of five-branches Valsa RL network using 0603 kit *R* and *L* values for FOI design: (a) phase, pseudoinductance, and magnitude responses, (b) relative phase errors and corresponding normalized histograms (%) of three different orders in the frequency range of 10 kHz – 10 MHz

performances of these GIC-based active inductance simulators often suffer from the non-idealities of Op-Amps. Therefore, this section deals with the optimal emulation of an FOI for the first time in the literature. The FOI design using the GA is studied numerically and experimentally verified.

The Valsa RC network in Tab. 3.1 is modified to an RL-type structure by replacing all capacitors with inductors as shown in corresponding figure. Its equivalent impedance function is given in Tab. 3.1, where n is the number of branches, R_0 is the initial resistor, L_0 is the initial inductor, R_i and L_i are the resistances and inductances of the i-th branch, respectively, while the fitness function is described as (3.1). The frequency response of five-branch FOIs with three different angles using 0603 kit R [163] and L [167] values is studied numerically and shown in Fig. 3.8. The pseudoinductances of orders $\alpha = \{0.25, 0.5, 0.75\}$ are 8.52 mH·s$^{-0.75}$, 834.62 µH·s$^{-0.5}$, and 89.62 µH·s$^{-0.25}$, which are constant with small deviations in the whole frequency range. Furthermore, the slope of magnitude in the inset of Fig. 3.8(a) shows that the inductive reactance (impedance) of the FOI increases as the supply frequency across it increases. To estimate the equivalent order α, the simulated magnitude responses are fitted to the function $\log_{10}|Z| = \alpha \log_{10} f + \log_{10}(2\pi)^{\alpha} L_{\alpha}$ using the linear least squares method. The equivalent equations from fitting the magnitude are provided inside Fig. 3.8(a). The maximum PAD and relative phase errors of the related orders are {±1.84°, ±1.66°, ±1.55°} and {±8.16%, ±3.68%, ±2.29%}, respectively, as depicted in Fig. 3.8(b). The operating frequency range is chosen between 10 kHz and 10 MHz because of the working frequency range of the 0603 kit ceramic chip inductors [167]. Considering that the maximum PAD is around ±2°, order of 0.25 is limited from 12 kHz. The used passive element values are listed in Appendix A.

Moreover, the behavior of an $\alpha = 0.5$ order FOI, numerically simulated in Fig. 3.8, was verified using the Agilent 4294A precision Impedance Analyzer. Standard calibration tests (open and short circuits) of the 16047E Test Fixture were performed to calibrate the instrument. During the experimental validation in the frequency range 400 kHz – 40 MHz (801 logarithmically spaced points in two decades), a sinusoidal input signal with a default AC voltage of 500 mV and a frequency of 1 MHz was applied, while one of

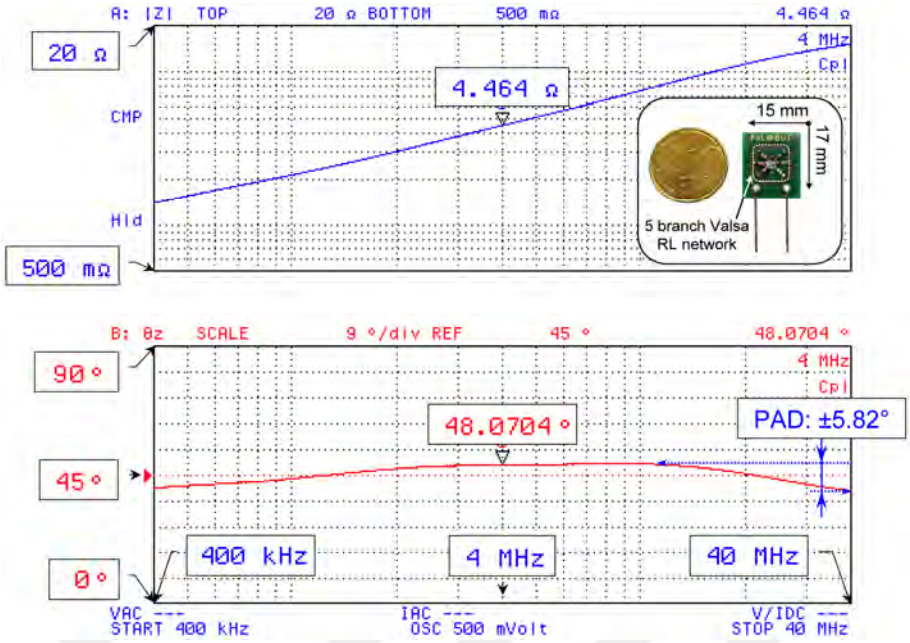


Fig. 3.9: Measurement results of an α = 0.5 order FOI from Fig. 3.8 and the fabricated device with dimensions of 15 mm × 17 mm as in inset (blue line - impedance response; red line - phase response)

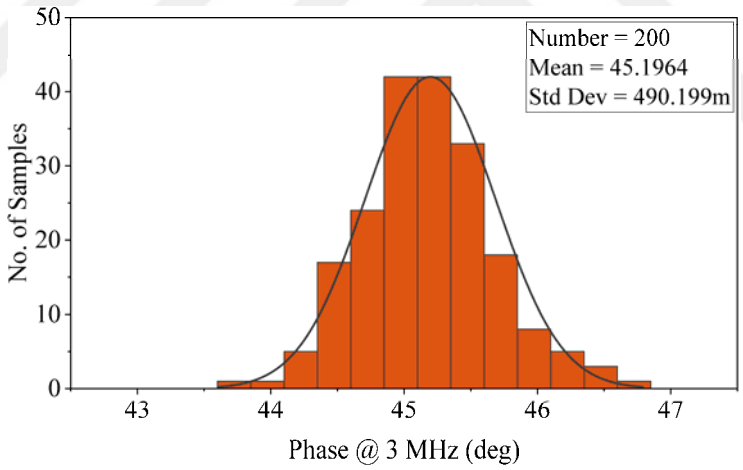


Fig. 3.10: Monte Carlo analysis: Phase variation at 3 MHz of the Valsa RL network optimized using GA (α = 0.5 order FOI with values used in Figs. 3.8 and 3.9)

terminals was grounded. The measurement results and a photograph of the fabricated device with dimensions of 15 mm × 17 mm are depicted in Fig. 3.9. The measured PAD in two decades of the frequency range of our interest is ±5.82°.

In addition to an $\alpha = 0.5$ order FOI, a MC statistical analysis was also performed in the OrCAD PSpice® simulation software. The passive element tolerances according to 0603 kit datasheets [163], [167] and 200 runs were set to observe affects due to

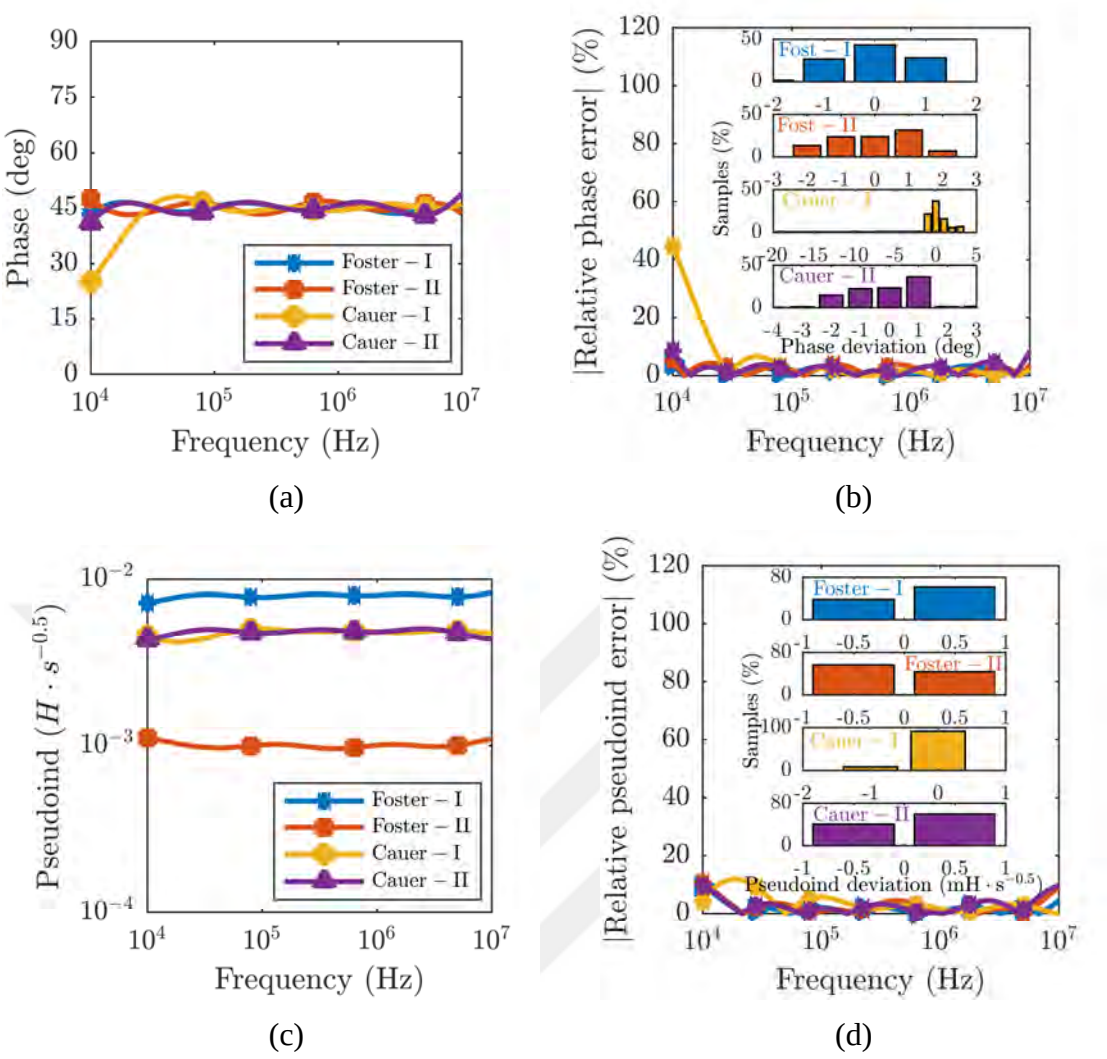


Fig. 3.11: (a) Simulated phase responses, (b) relative phase errors and corresponding normalized histograms (%) of phase angle deviation from CPA as an inset, (c) pseudoinductances responses, and (d) relative pseudoinductances errors and corresponding normalized histograms (%) of pseudoinductances deviation from CPA as an inset, respectively, of different RL networks optimized using GA for FOI design. Impedance and phase responses are optimized in the frequency range of 10 kHz–10 MHz

manufacturing processes. The histogram shown in Fig. 3.10 demonstrates the variation of the phase at 3 MHz. The mean value with standard deviation 0.49 is 45.1964°, which is very close to the theoretical value 45° confirming that the proposed network has low sensitivity characteristic on passive components.

In addition, for the first time in the literature, the Foster-I, Foster-II, Cauer-I, and Cauer-II type of RL networks are also studied. The impedance function of all networks optimized using GA are given in Tab. 3.1. Fig. 3.11 shows the phase and pseudoinductance responses with corresponding relative errors and normalized histograms (%) of deviations of four RL topologies. The target phase and frequency bandwidth are set to 45° and 3 decades in the frequency range of 10 kHz – 10 MHz, respectively, with no pseudoinductance specification to obtain the best result. In summary, the minimal error is obtained with Foster-I structure while the least spread of

passive element values are observed with the Foster-II. The detailed analysis including MC results for all studied networks is presented in Appendix A.

3.4 Discussions

Tab. 3.3 compares the performance of RC networks built using Oustaloup, CFE, RA, and the GA. For instance, for the Foster-II network composed of the same number of branches, the performance of the GA is compared with that of Oustaloup and CFE. The results obtained with the GA have the lowest PAD in a wider frequency range than Oustaloup and CFE. To provide the overall performance evaluation, a numeric Figure of Merit (FoM) value is calculated as:

$$\mathrm{FoM} = \frac{\mathrm{BW}}{\mathrm{No.\ of\ Branches} \times \mathrm{No.\ of\ Cap.} \times \mathrm{No.\ of\ Res.} \times |\mathrm{CPA\ Dev.}|}. \tag{3.2}$$

Notably, the FoM in our study for Foster-II network using the GA was 30.3×10^{-3}, which is the largest value. An improvement of approximately 396% over the Oustaloup and 354% over the CFE was achieved using the same number of elements and least CPA deviation in a wider bandwidth. In the same manner, the Valsa structure is compared between the RA and GA. Evidently, the GA provides a wider bandwidth than RA with lower CPA error. Moreover, the FoM shows significant improvements to the Valsa network with the GA (294% in case of Fig. 3.4 results). To comprehensively evaluate the performance of the Valsa structure using the RA and GA in Tab. 3.3, a radar chart is depicted in Fig. 3.12, which shows that a smaller area of pentagon provides superior

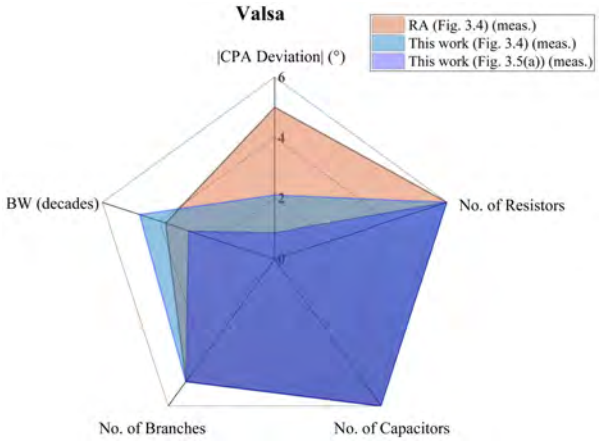


Fig. 3.12: Radar chart showing an evaluation of Valsa RC structure results from Tab. 3.3

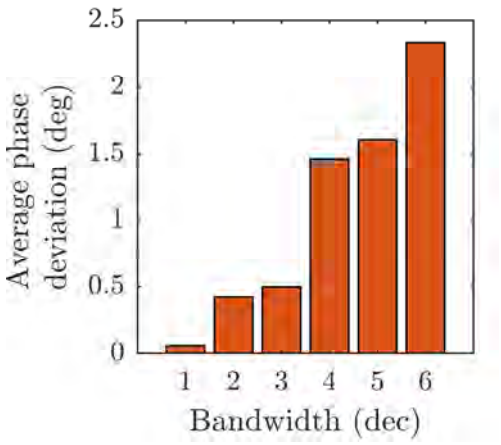
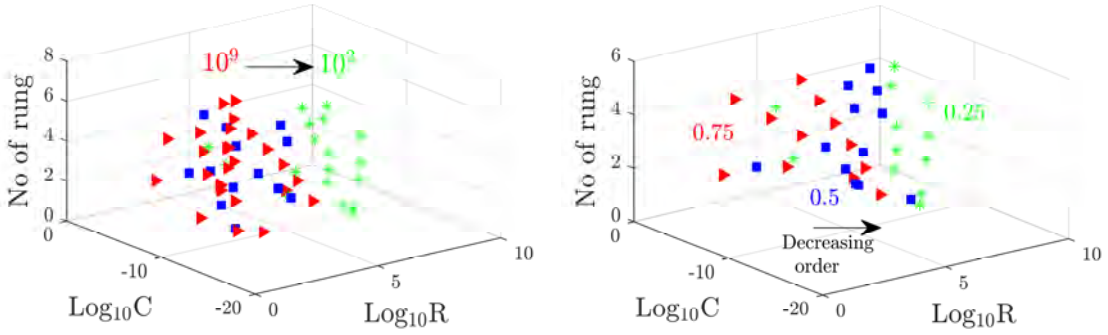


Fig. 3.13: Numerical study of five-branches RC networks using random *R* and *C* values and plot of average phase angle deviation of an order of $\alpha = -0.5$ by increasing the operation bandwidth from 100 Hz up to 100 MHz

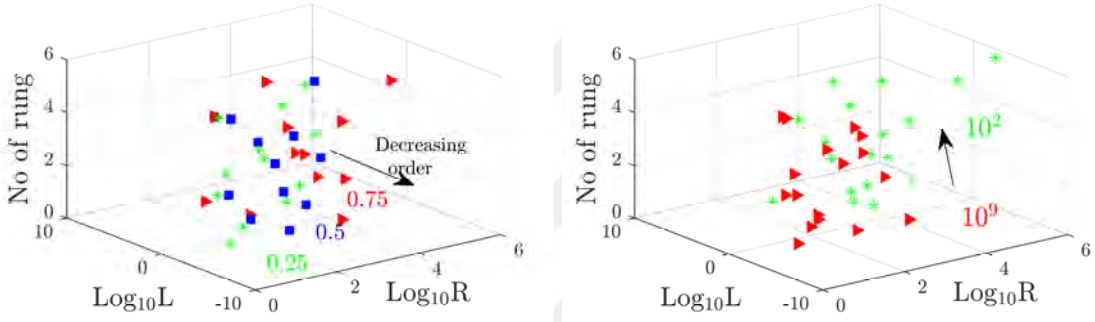
Tab. 3.3: Comparison of simulation and measurement results of used methods for FOC design

Topology	Method	No. of Branches	No. of Capacitors	No. of Resistors	|CPA Dev. (°)	BW (decades)	FoM (°)
Foster-II	Oustaloup (Fig. 3.1(c)) (simul.)	5	5	6	5	2.1	7.64×10^{-3}
	CFE (Fig. 3.1(c)) (simul.)	5	5	6	5	2.35	8.55×10^{-3}
	This work (Fig. 3.1(c)) (simul.)	5	5	6	2.4	4	30.3×10^{-3}
Valsa	RA (Fig. 3.4) (meas.)	5	6	6	5	3.8	12.67×10^{-3}
	This work (Fig. 3.4) (meas.)	5	6	6	2.1	4.7	37.3×10^{-3}
	This work (Fig. 3.5(a)) (meas.)	5	6	6	0.87	3	57.47×10^{-3}



(a) (b)

Fig. 3.14: (a) Order and (b) frequency effect on *R* and *C* values on each rung of the Foster-II and Valsa structures for FOC design



(a) (b)

Fig. 3.15: (a) Order and (b) frequency effect on *R* and *L* values on each rung of the Valsa structures for FOI design

performance (for instance, the GA in Fig. 3.5(a)). On the other hand, the error increases by increasing the bandwidth while maintaining the five branches as default (see numerical study in depicted in Fig. 3.13). It is clear that the phase angle deviation is less than ±2.3° even with 6 decades of operation (from 100 Hz up to 100 MHz).

The performance of RC network optimizations is primarily compared through the utilization of the results in Appendices A. Here, total and spread of resistances and capacitances, phase angle deviation, relative phase error, and MC analysis for all networks are given. According to these, the GA generally provides the minimum total capacitance value and can be limited in any range of the designer's choice. Furthermore, as the order increases, the total capacitance increases and the resistance decrease, as shown in Fig. 3.14(a). Maintaining the order constant and increasing the capacitance value provides the same results as in the previous case. The frequency effect on the values is shown in Fig. 3.14(b). At high frequencies, small *R* and *C* values are used (as also seen in Appendix A), whereas larger passive values are used at low frequencies. This fact can be explained by the dissipation factor (DF) expressed as DF = ESR / X_C, where ESR and X_C denote the equivalent series resistance and capacitors reactance, respectively, or as a tangent of the loss angle [173].

Fig. 3.15 shows the distribution of R and L values depending on an order and the frequency range for FOI design. Different to the FOC evaluation, resistance and inductance vary linearly with an order. It is also clear from Appendix A that an increasing FOI order has the effect of increasing passive values. This result can be explained by the quality factor (Q) definition $Q = X_L/R$, where X_L is the inductive reactance and R is the DC resistance [174]. Maintaining the Q constant, increasing an order (effecting X_L) has the effect of increasing the R. At low frequencies and within limits, both passive values become much greater than their equivalents at high frequencies.

3.5 Summary

In this chapter, a new approach for the design of an FOE, mainly from the Foster-II and Valsa structures, with desired properties was introduced. The mixed integer-order GA was used to determine the optimal phase response with minimum phase angle deviation in a defined frequency range. The values of the passive elements have been optimized in accordance with the commercially available IEC 60063 compliant kits. Therefore, the introduced approach offers enormous freedom to design RC/RL networks without making any value adjustments, which could lead to degeneration of FOE performance during measurements. Furthermore, designers can obtain the optimal phase and impedance response at low-, mid-, and high frequencies with wide bandwidths and low phase errors with minimum total passive element.

The results demonstrated excellent performance as well as adaptability for application to various types of structure, such as Cauer-I, Cauer-II, and Foster-I either for FOC or FOI design, which was carried out for the first time in the literature. All these features make this approach strong and beneficial analogue designer. It is also important to note that the proposed approach outperformed other approximations or algorithms such as the RA [175], Oustaloup's approximations [22], graphical method [58], meta-heuristic algorithms [129], and the design using bilinear sections [49]. In other words, a fifth-order approximation of FOE using GA shows better performance than for example fourteenth- [175] or ninth-order [58] approximations. In addition, during our research, we found that there is a connection between the FOE and the equivalent circuit model of the inductors and electrolytic capacitors. Thus, more accurate models of the FODs can be developed in the future.

4 ANALOG IMPLEMENTATION OF FRACTIONAL-ORDER PI$^{\lambda}$ CONTROLLERS

In general, the case of controller realization is not equivalent to the cases of simulation or numerical evaluation of the fractional-order integral and differential operators. It is also important to have discrete equivalents or approximations with poles and zeros, that is, in a rational form. Then, it brings us to the following question: how to implement proposed realizations? Basically, there are two methods for realization of the FOC. One is a digital realization based on microprocessor devices and appropriate control algorithm and the second one is an analogue realization based on analogue circuits so-called FOCs, FOIs.

In this chapter, particularly, fractional-order integral operator $s^{-\lambda}$ (integrator I$^{\lambda}$, where $0 < \lambda < 1$) is implemented employing two-stage Op-Amps. Cascade of first-order bilinear transfer segments (BTSs) is used, which is a two-port network with a single pole and a single zero. The behavior of both proposed analogue circuits employing two-stage Op-Amps is confirmed by SPICE simulations using TSMC 0.18 μm level-7 LO EPI SCN018 CMOS process parameters with ±0.9 V supply voltages. The cascade of BTSs creates so-called constant phase block, which generates desired magnitude and phase response by proper setting of both polynomial roots (zero and pole frequencies) of each BTS [17]. As Fig. 4.1 illustrates, the traditional PIDs are a particular case of fractional-order PI$^{\lambda}$D$^{\mu}$ (FOPI$^{\lambda}$D$^{\mu}$) controllers. Hence, this approach ensures direct emulation of the behavior of an I$^{\lambda}$, which is very beneficial for fractional-order PI$^{\lambda}$ (FOPI$^{\lambda}$) design. FOPI$^{\lambda}$ controller, which is used as an application of I$^{\lambda}$ in this chapter, are widely used in industrial applications because of their simplicity and applicability to wide range of industrial control problems. In recent years, the survey [176] indicates fractional-order controllers become an emerging research topic. While design, these controllers have an additional degree of freedom and thus offer potential reduction of the control effort, which also results in reduction of wasted energy. Furthermore, their analog implementation allows us to integrate full design in chip and tune the control parameters easily.

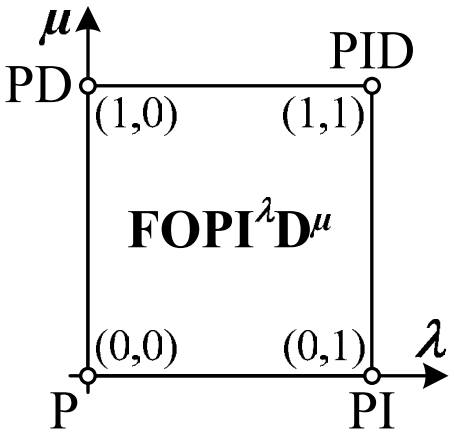


Fig. 4.1: Generalization of FOPI$^{\lambda}$D$^{\mu}$ controller from points to plane

4.1 Theory

A general block diagram of a single loop feedback control system is depicted in Fig. 4.2(a), which transfer function can be expressed as [48]:

$$\frac{Y(s)}{R(s)} = \frac{C(s)G(s)}{1+C(s)G(s)}, \tag{4.1}$$

where $G(s)$ is a plant, $C(s)$ is a controller, $R(s)$ is a reference input signal, $Y(s)$ is an output signal, $T_d(s)$ is an external disturbance, $U(s)$ is a control signal, and $E(s)$ is an error signal, which is given by $E(s) = R(s) - Y(s)$.

An implementation of a control system used to control the speed and position of an armature controlled DC motor is show in Fig. 4.2(b). The system is composed of a new analogue implementation of a fractional-order PI$^{\lambda}$ controller ($C(s)$) and $G(s)$ is the mathematical model of a DC motor - the plant [44]. In brief, assuming the external disturbance, i.e. load torque $T_d(s)$ is zero, the transfer function (TF) of the motor speed control in Laplace domain can be expressed as [51]:

$$G(s) = \frac{\omega(s)}{V_{\mathrm{PI}^{\lambda}}(s)} = \frac{K_{\mathrm{m}}}{\left(L_{\mathrm{a}}s + R_{\mathrm{a}}\right)\left(Js + b\right) + K_{\mathrm{b}}K_{\mathrm{m}}}, \tag{4.2}$$

where $V_{\mathrm{PI}}{}^{\lambda}(s)$ is the applied armature voltage, $\omega(s)$ is the angular velocity (controlled variable), L_a is an inductance of armature winding, R_a is an armature resistance, K_b is back-emf constant, K_m is a torque constant, and J is an equivalent moment of inertia and b is friction coefficient of motor and load referred to motor shaft. As the armature time constant for most of DC motors is negligible, the TF of resulted simplified model has the form $G(s) = K_{DC}/(\tau s + 1)$, where $\tau = R_aJ/(R_ab + K_bK_m)$ is the time constant and $K_{DC} = K_m/(R_ab + K_bK_m)$ is the gain with $K_b = K_m$. Similarly, the TF for armature voltage and position $\theta(s)$ (controlled variable) will be $G_\theta(s) = K_{DC}/[s(\tau s + 1)]$.

4.2 Fractional- Order PI$^{\lambda}$ Controller Design

In control theory, the gain crossover frequency (ω_{cg}) implies that the modulus of the open-loop transfer function follows $|C(j\omega_{cg})G(j\omega_{cg})| = 1$ and phase margin (Φ_m) sets a condition upon the phase of the open-loop system at the ω_{cg}, which can be expressed as $\Phi_m = \arg[C(j\omega_{cg})G(j\omega_{cg})] + \pi$. Considering the setup [51], the TF of the DC motor voltage-speed with 25% break is:

$$G(s) = \frac{\omega(s)}{V_{\mathrm{PI}^{\lambda}}(s)} = \frac{0.25}{1.45s+1}, \tag{4.3}$$

while the performance specification is $\omega_{cg} = 1.5$ rad/s and $\Phi_m = 60°$.

The speed (4.3) of a DC motor can be controlled using FOPI$^{\lambda}$, which TF in general has a form:

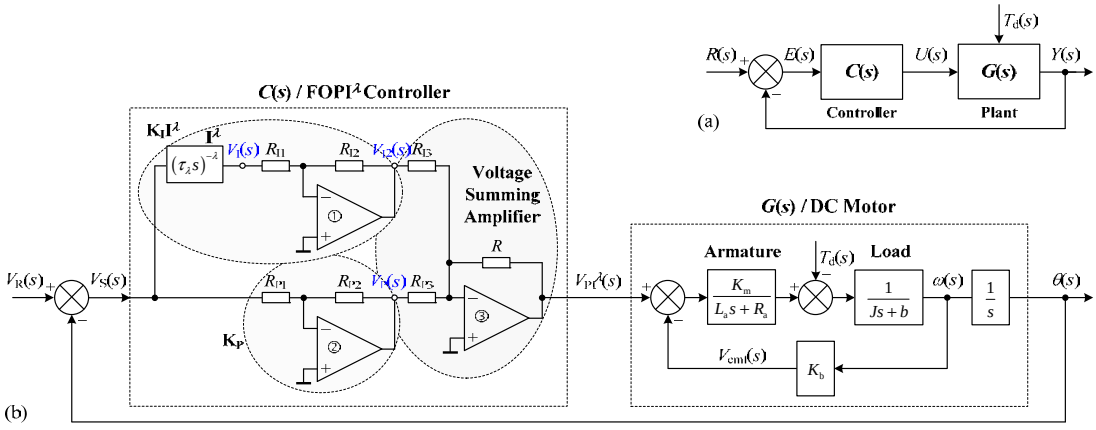


Fig. 4.2: (a) Block diagram of a control system, (b) an implementation of an analogue fractional-order PI$^{\lambda}$ controller and the mathematical model of a DC motor

$$C(s)=\frac{U(s)}{E(s)}=\frac{V_{\mathrm{PI}^{\lambda}}(s)}{V_{\mathrm{S}}(s)}=K_{\mathrm{P}}+K_{\mathrm{I}}s^{-\lambda}, \tag{4.4}$$

which corresponds in discrete domain to a TF as follows:

$$C(z^{-1})=\frac{U(z^{-1})}{E(z^{-1})}=K_{\mathrm{P}}+K_{\mathrm{I}}\left[\omega\left(z^{-1}\right)\right]^{-\lambda}. \tag{4.5}$$

Equations (4.4) and (4.5) indicate the following three parameters, which can be independently set:

(i) K_{P} is the proportional constant,

(ii) K_{I} is the integration constant,

(iii) λ $(0<\lambda<1)$ is the fractional order of an integrator in Laplace domain, while in discrete domain it is an arbitrary real number.

Following [51], the graphical method yields the solution for design parameters, which are $K_{\mathrm{P}}=1.37$, $K_{\mathrm{I}}=2.28$, and $\lambda=0.89$. Thus, the FOPI$^{\lambda}$ controller was obtained as:

$$C(s)=\frac{U(s)}{E(s)}=\frac{V_{\mathrm{PI}^{\lambda}}(s)}{V_{\mathrm{S}}(s)}=1.37+2.28s^{-0.89}. \tag{4.6}$$

The FOPI$^{\lambda}$ controller shown in Fig. 4.2(b) requires presence of a precise I$^{\lambda}$ design. Block diagram of a proposed integrator by cascade connection of first-order BTSs and first-order low-pass filter (LPF) is depicted in Fig. 4.3 and can be expressed as:

$$K_{\mathrm{I}^{\lambda}}(s)=\frac{V_{\mathrm{I}}(s)}{V_{\mathrm{S}}(s)}=\frac{\prod_{i=1}^{m}\left(s-z_i\right)}{\prod_{j=1}^{n}\left(s-p_j\right)}=\left.\frac{\sum_{i=1}^{m}a_i s^i}{\sum_{j=1}^{n}b_j s^j}\right|_{z_i,\,p_j\in\Re}, \tag{4.7}$$

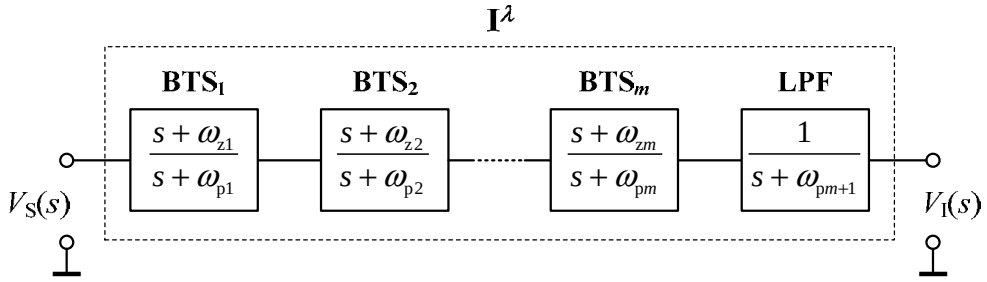


Fig. 4.3: Block diagram of a fractional-order integrator using BTSs and LPF

where m denotes total number of BTS needed for the design of constant phase block and $n = m + 1$ will be mathematical order of the final circuit due to use of an additional LPF. The usefulness of LPF is described below.

Proposed realization of BTS using two ideal Op-Amps (assuming open loop gain $A \to \infty$) and a set of passive components is shown in Fig. 4.4(a), while the non-inverting LPF is depicted in Fig. 4.4(b). Transfer function of each segments are:

$$K_{\mathrm{BTS}\_m}(s) = \frac{V_{\mathrm{BTS\_OUT}m}(s)}{V_{\mathrm{BTS\_IN}m}(s)} = \frac{s+\omega_{zm}}{s+\omega_{pm}} = \frac{2sC_m + \left(R_\mathrm{b} \parallel R_{zm}\right)}{2sC_m + \left(R_\mathrm{b} \parallel R_{pm}\right)}, \tag{4.8a}$$

$$K_{\mathrm{LPF}}(s) = \frac{V_{\mathrm{LPF\_OUT}}(s)}{V_{\mathrm{LPF\_IN}}(s)} = \frac{1}{s+\omega_{pm+1}} = \frac{1}{sC_{pm+1}R_{pm+1}+1}, \tag{4.8b}$$

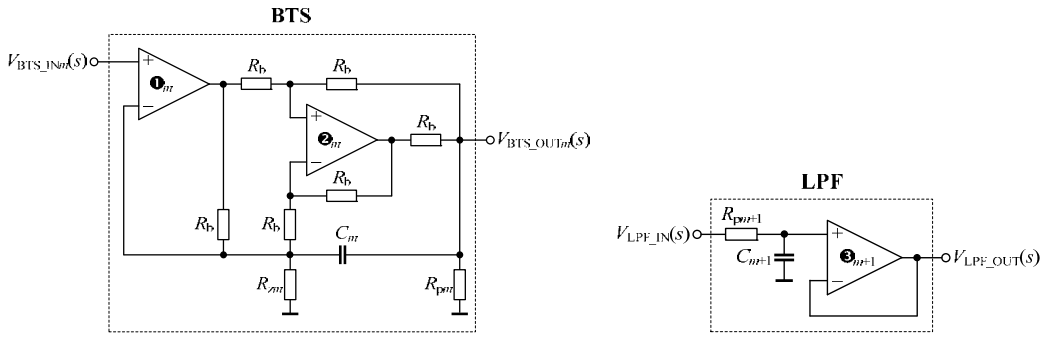
hence, pole and zero frequencies are $\omega_{pm} = (R_\mathrm{b} \parallel R_{pm})/(2C_m)$, $\omega_{zm} = (R_\mathrm{b} \parallel R_{zm})/(2C_m)$, $\omega_{pm+1} = 1/C_{pm+1}R_{pm+1}$, and transfer zero and poles are adjustable by resistors R_{zm}, R_{pm}, and R_{pm+1}.

Now, TF of cascade of m BTS and LPF in our particular case as depicted in Fig. 4.3 can be expressed as:

$$\begin{aligned} K_{\mathrm{I}^\lambda}(s) &= \frac{V_\mathrm{I}(s)}{V_\mathrm{S}(s)} = K_{\mathrm{BTS}\_1}(s)K_{\mathrm{BTS}\_2}(s)\ldots K_{\mathrm{BTS}\_m}(s)K_{\mathrm{LPF}}(s) = \\ &= \prod_{i=1}^{m}\left[\frac{2sC_m + \left(R_\mathrm{b} \parallel R_{zm}\right)}{2sC_m + \left(R_\mathrm{b} \parallel R_{pm}\right)}\right]\left(\frac{1}{sC_{pm+1}R_{pm+1}+1}\right) = (\tau_\lambda s)^{-\lambda}. \end{aligned} \tag{4.9}$$

Generalized TF (4.9) of a fractional-order I^λ has feature to set m pairs of zeros and poles independently and an additional pole as our design requires. The main advantage of this approach is an easy and low-cost realization of I^λ using discrete passive components and on the shelf available Op-Amps.

Ones the I^λ is designed, its integration constant K_I must be also realized. For this purpose the inverting Op-Amp configuration was selected, which closed loop voltage gain using an ideal Op-Amp can be calculated by ratio of two resistors in the path as $\mathrm{K_I} = -R_{I2}/R_{I1}$. The minus sign (–) comes from the inverting Op-Amp configuration and indicates a 180° phase shift. Now, the output voltage of the proposed fractional-order integrator with integration constant ($\mathrm{K_I I}^\lambda$) in time domain can be given as:



(a) (b)

Fig. 4.4: (a) Realization of a bilinear transfer segment and (b) low-pass filter using Op-Amps

$$V_{\mathrm{I2}}(t) = -\frac{R_{\mathrm{I2}}\tau_{\lambda}^{-\lambda}}{R_{\mathrm{I1}}}\int_0^t V_{\mathrm{S}}(t)dt^{\lambda}\,, \tag{4.10}$$

while in Laplace domain its TF is $-R_{\mathrm{I2}}(\tau_{\lambda}s^{-\lambda})/R_{\mathrm{I1}}$. Similarly, the inverting Op-Amp configuration was used also for proportional constant K_{P} realization and its output voltage is:

$$V_{\mathrm{P}}(t) = -\frac{R_{\mathrm{P2}}}{R_{\mathrm{P1}}}V_{\mathrm{S}}(t)\,. \tag{4.11}$$

Equations (4.4)–(4.6) indicate that a summing block is also required for FOPI$^{\lambda}$ design. In analogue electronics the Op-Amp-based summing amplifier is a suitable circuit for this purpose enabling inverting weighted sum of input signals. Hence, the minus sign in (4.10) and (4.11) will be eliminated. Moreover, assuming the input resistors R and R_{P3} in Fig. 4.2(b) are equal, a unity gain adder will be made with no disturbance of K_{P} and K_{I} constants. Finally, summing (4.10) and (4.11) as indicated in Fig. 4.2(b), the output voltage of the proposed FOPI$^{\lambda}$ in time domain will be:

$$\begin{aligned} V_{\mathrm{PI}^{\lambda}}(t) &= -R\left[\frac{V_{\mathrm{P}}(t)}{R_{\mathrm{P3}}} + \frac{V_{\mathrm{I2}}(t)}{R_{\mathrm{I3}}}\right] = \\ &= R\left[\frac{R_{\mathrm{P2}}}{R_{\mathrm{P1}}R_{\mathrm{P3}}}V_{\mathrm{S}}(t) + \frac{R_{\mathrm{I2}}\tau_{\lambda}^{-\lambda}}{R_{\mathrm{I1}}R_{\mathrm{I3}}}\int_0^t V_{\mathrm{S}}(t)dt^{\lambda}\right], \end{aligned} \tag{4.12}$$

and its equivalent transfer function in Laplace domain can be given as:

$$\begin{aligned} C(s) &= \frac{U(s)}{E(s)} = \frac{V_{\mathrm{PI}^{\lambda}}(s)}{V_{\mathrm{S}}(s)} = \\ &= K_{\mathrm{P}} + K_{\mathrm{I}}K_{\mathrm{I}^{\lambda}}(s) = R\left[\frac{R_{\mathrm{P2}}}{R_{\mathrm{P1}}R_{\mathrm{P3}}} + \frac{R_{\mathrm{I2}}(\tau_{\lambda}s)^{-\lambda}}{R_{\mathrm{I1}}R_{\mathrm{I3}}}\right]. \end{aligned} \tag{4.13}$$

Comparing (4.4) and (4.13), the following design equations are derived:

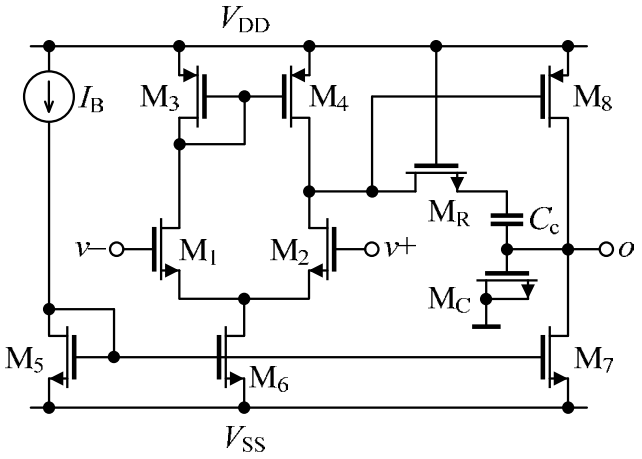
$$K_P = \frac{RR_{P2}}{R_{P1}R_{P3}}, \quad K_I = \frac{R_{I2}(\tau_\lambda)^{-\lambda}}{R_{I1}R_{I3}}, \tag{14a,b}$$

which will be useful in next section for FOPI$^\lambda$ design according to parameters as defined by (4.6).

4.3 Simulation Results

To verify the theoretical analysis, the behavior of the proposed I$^\lambda$ and FOPI$^\lambda$ controller employing Op-Amps have been simulated using SPICE program. DC power supply voltages of designed CMOS implementation of two-stage Miller compensated Op-Amp shown in Fig. 4.5(a) were set $+V_{DD} = -V_{SS} = 0.9$ V. In [177], discrete components are assumed for both Miller resistor and load capacitor. The Op-Amp structure shown in Fig. 4.5 is more favorable for full CMOS integration, because both components are realized via MOS-only technique, while the Miller capacitor can be realized as double poly (poly1-poly2) or metal-insulator-metal (MIM) capacitor. In the design, transistors were modeled by the TSMC 0.18 μm level-7 LO EPI SCN018 CMOS process parameters ($V_{THN} = 0.3725$ V, $\mu_N = 259.5304$ cm^2/(V·s), $V_{THP} = -0.3948$ V, $\mu_P = 109.9762$ cm^2/(V·s), $T_{OX} = 4.1$ nm). Following the design procedure described in [177], the computed aspect ratios of CMOS transistors and Op-Amp main parameters obtained with DC, AC, and transient analyses are listed in Fig. 4.5(b) and Tab 4.1, respectively. During all simulations the bias current in the structure was set as $I_B = 130$ μA.

Firstly, the I$^\lambda$ of order 0.89 (i.e. the time constant $\tau_\lambda^{-\lambda}$) was designed. The five-branch Valsa structure [122] was used, which provides a minimum PAD. Required R and C values were calculated via approach [122] implemented in Matlab with the following inputs: pseudo-capacitance $C_\lambda = 20$ μF·sec$^{-0.11}$, bandwidth (CPZ) from 30 mHz up to 100 Hz (> 3 decades), CPA –80.1° (i.e. $\lambda = 0.89$), and PAD = ±1°. Preliminary calculations showed that five BTSs ($m = 5$) and a LPF are required in the constant phase block shown in Fig. 4.3 in order to achieve the design specification. Note that the LPF is used for correction purposes of additional pole in Valsa structure. As the



(a)

Transistors	W/L (μm)
M_1, M_2	25.8 / 0.3
M_3, M_4	10.6 / 0.3
M_5	15.4 / 0.3
M_6	16.4 / 0.3
M_7	58 / 0.3
M_8	95.9 / 0.3
M_R	4 / 0.3
M_C	288 / 3.6

(b)

Fig. 4.5: (a) CMOS structure, (b) transistor dimensions of two-stage Op-Amp

Tab. 4.1: Behavior of CMOS Two-Stage Op-Amp in Fig. 4.5(a)

Parameter	Value	Unit
Power supply	±0.9	(V)
Unity gain bandwidth	230.2	(MHz)
DC gain	60	(dB)
Phase margin	60	(degree)
Slew rate +/–	163 / 121	(V/μs)
PSRR +/–	72.4 / 68.5	(dB)
CMRR	62.4	(dB)
Compensation resistor (NMOS M_R)	≅ 615	(Ω)
Compensation capacitor C_c	0.8	(pF)
Load capacitor (NMOS M_C)	≅ 3	(pF)
Power dissipation	1.39	(mW)
Total area	1 115.6	$(\mu m^2)^{\#}$

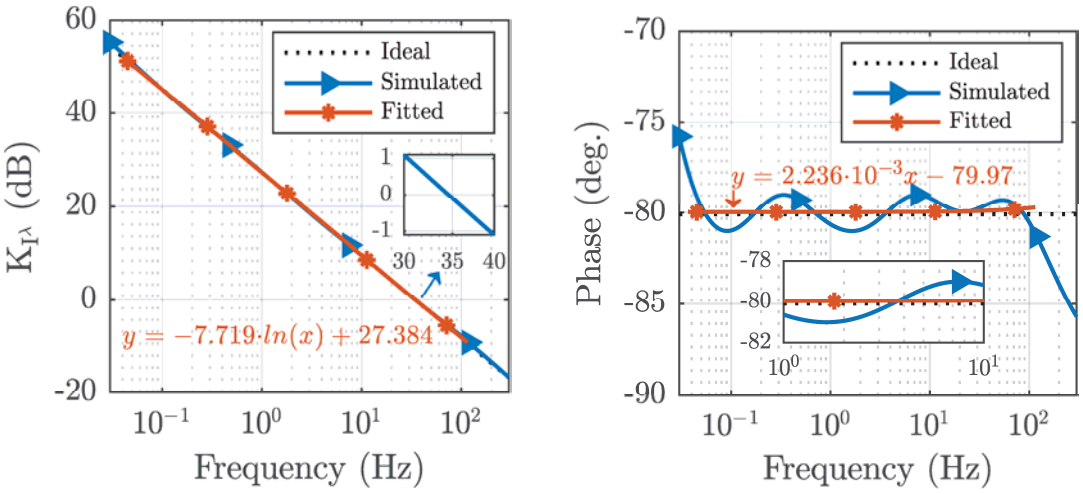
$^{\#}$Sum of products of widths and lengths of each transistors in the CMOS implementation

Tab. 4.2: Computed component values used in BTSs and LPF for fractional-order I^{λ} design

Capacitors (F)					
C_1	C_2	C_3	C_4	C_5	C_6
27 μ	10 μ	12 m	68 μ	1.8 m	150 n
Resistors (Ω)					
R_b	R_{z1}	R_{z2}	R_{z3}	R_{z4}	R_{z5}
24 k	49	1.37 k	50.5 k	1.01 k	156
R_{p1}	R_{p2}	R_{p3}	R_{p4}	R_{p5}	R_{p6}
14 k	1 k	1.8 k	942	50.5 k	13 k

next step, zero and pole frequencies were recalculated and corresponding passive component values of R_{zm}, R_{pm}, R_{pm+1}, C_m, and C_{pm+1} obtained via Matlab algorithm and optimized using modified least squares quadratic method. Component values used in BTSs and LPF for I^{λ} design are listed in Tab 4.2.

Ideal and simulated gain and phase responses in frequency domain are given in Fig. 4.6. Selected zooms and equivalent equations for fitting the gain and phase in CPZ 45 mHz – 115 Hz via natural logarithm and linear regressions, respectively, are provided inside Figures. Simulated value of the unity-gain frequency of the I^{λ} was 34.6 Hz. As it can be seen in Fig. 4.7, in CPZ the maximum relative phase error is 1.38% and corresponding absolute PAD about 1°. Monte Carlo (statistical) analysis was performed with capacitors 5% tolerance, resistors 1% tolerance, and 200 runs to observe affects due to manufacturing processes. The histogram shown in Fig. 4.8 demonstrates the variation of the phase of I^{λ} at 3 Hz. The mean value is –80.2389°, which is very close to theoretical value –80.1° confirming that the proposed I^{λ} has low sensitivity characteristic on passive components. Equation (4.6) indicates the following design parameters of the FOPI$^{\lambda}$ controller depicted in Fig. 4.2(b): $K_P = 1.37$, $K_I = 2.28$, and



(a) (b)

Fig. 4.6: Ideal, simulated, and fitted (a) gain and (b) phase responses of 0.89-order integrator

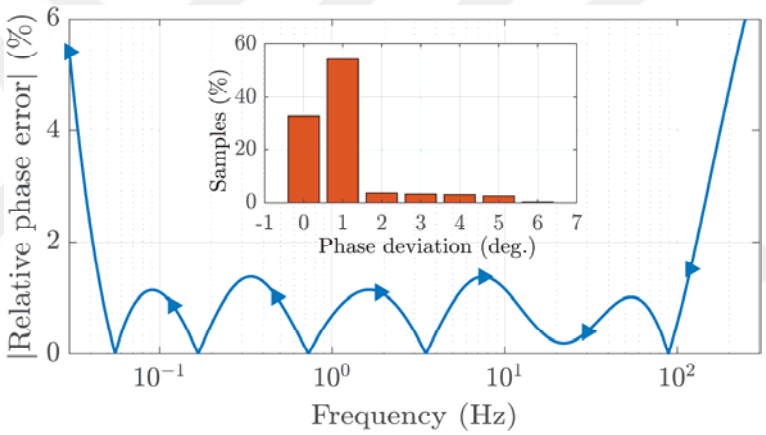


Fig. 4.7: Relative phase error and the corresponding normalized histogram for phase angle deviation evaluated in full frequency range

$\lambda = 0.89$. As the I^λ is designed, the remaining design parameters can be recalculated using (4.14), which are the following: $R = R_{P1} = R_{P3} = 10$ kΩ, $R_{P2} = 13.7$ kΩ, $R_{PI1} = 27.4$ kΩ, $R_{PI2} = 1.3$ kΩ, and $R_{PI3} = 24.9$ kΩ. An ideal and simulated gain and phase responses of the $FOPI^\lambda$ are given in Fig. 4.9 confirming the accurate operation of the controller.

Moreover, in order to illustrate the time-domain performance of I^λ and $FOPI^\lambda$ controller, transient analyses were performed and results are depicted in Fig. 4.10. A square wave input signal with amplitude 150 mV and frequency 100 mHz ($T_D = 0$, $T_R = 1$ ms, $T_F = 1$ ms, $T_{PW} = 10$ s, $T_{PER} = 20$ s, i.e. $12\,\tau_\lambda^{-\lambda}$) was applied to both circuits. Hence, following the theory, in Fig. 10(a) the simulated output signal of the I^λ has triangular waveform, while Fig. 10(b) indicates increasing gain in the proposed $FOPI^\lambda$ controller as the effect of the K_P.

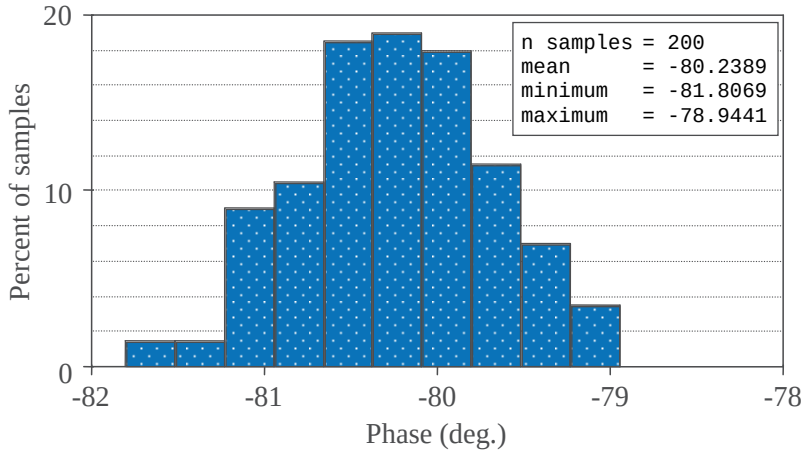


Fig. 4.8: Monte Carlo analysis: Variation of the phase of I^{λ} at 3 Hz

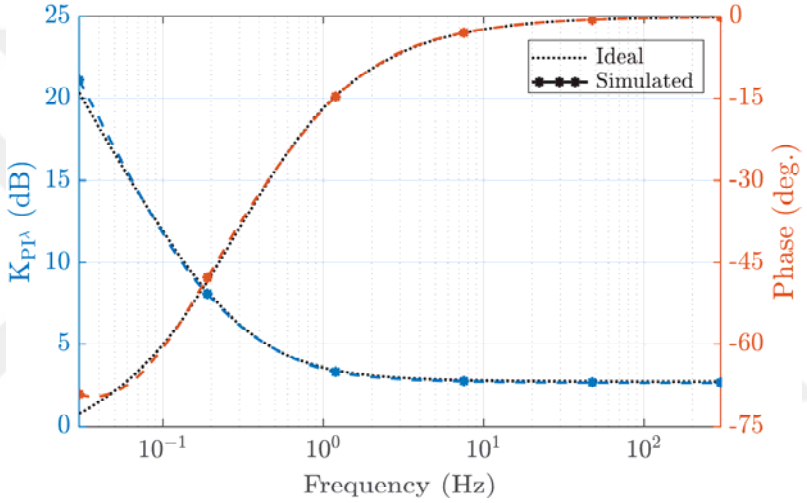
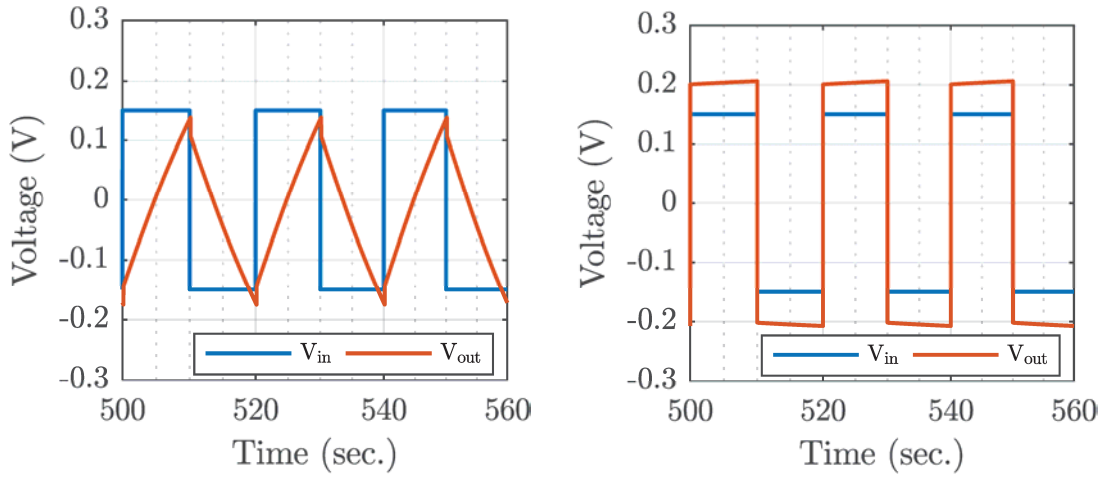


Fig. 4.9: Ideal and simulated gain and phase responses for the proposed $FOPI^{\lambda}$ controller



(a) (b)

Fig. 4.10: Time-domain responses of proposed (a) I^{λ} and (b) $FOPI^{\lambda}$ controller with applied square wave input voltage signal with frequency 100 mHz

4.4 Summary

In this chapter, an analogue realization of a fractional-order I^{λ} and $FOPI^{\lambda}$ controller is proposed based on design specification corresponding to a speed control system of an armature controlled DC motor. The integrator with a constant phase angle −80.1° (i.e. order $\lambda = -0.89$), bandwidth greater than 3 decades, and maximum relative phase error 1.38% is designed by cascade connection of first-order bilinear transfer segments and first-order low-pass filter. The performance of suggested realization is demonstrated in a fractional-order proportional-integral ($FOPI^{\lambda}$) controller described with proportional constant 1.37 and integration constant 2.28. The design specification corresponds to a speed control system of an armature controlled DC motor, which is often used in mechatronic and other fields of control theory. The behavior of both proposed analogue circuits employing two-stage Op-Amps is confirmed by SPICE simulations using TSMC 0.18 μm level-7 LO EPI SCN018 CMOS process parameters with ±0.9 V supply voltages.

The main advantage of this approach is an easy and low-cost realization using discrete components. For the I^{λ}, SPICE simulations using two-stage CMOS Op-Amps showed an absolute PDA about 1° in CPZ from 45 mHz to 115 Hz. Statistical analysis proved its low sensitivity characteristic on passive components. Simulated gain and phase responses of the $FOPI^{\lambda}$ confirmed accurate operation of the controller.

5 FABRICATION OF A FRACTIONAL-ORDER CAPACITOR

In Chapter 2, the literature survey on the development of FOEs was presented and summarized with giving the limitations and boundaries. As a device, only FOCs have been fabricated so far. This is due to modelling difficulties and understanding the material characteristics of FOIs. As per discussion on development of FOCs, the working principle behind the FOCs can be explained with the following scenario: Electrical conduction through the fractional-order material (semi-conductive filler instead of dielectric) causes electrical current to flow down various paths. For example, conduction can be along polymer composite and across gaps between it. Each path through fractional-order material may be considered to have individual impedance that is favorable to conducting electrical signals of various frequencies. Also, polymer composites may have a distribution of sizes and spacing, and the paths may have a distribution of electrical characteristics, with an associated distribution of favored signal frequencies. Furthermore, the impedance of each path is also changed by electrical coupling to other paths. Therefore, the combination of various electrical paths through fractional-order material may cause its impedance to have a magnitude that is substantially linear and a phase that is substantially constant over a bandwidth of input signal frequencies. Related formulas with their explanations were given in section 2.2 and 2.3. This approach opens up a new avenue in fabricating FOCs involving a variety of heterostructures combining the different fillers and different matrixes.

Thus, in this chapter, fabrication of a FOC using the hexagonal boron nitride (*h*BN) -ferroelectric polymer blends is investigated. The tunability of the constant phase is obtained using only two tuning knobs e.g., different volume ratio of *h*BN and multi-walled carbon nanotube (CNT). This fabrication process is therefore quite simple rather than previously fabricated ones [87], [151]. Fig. 5.1 schematically shows an exemplary FOC that has fractional order impedance. The proposed FOC integrates layers of two conductive films, and between them polymer composite with significantly improved CPA, CPZ, and phase angle variation performance. The device is mounted PCB with having one common and nine pins while each showing a FOC characteristic.

It can be categorized between solid-state and passive FOCs. The presented FOCs show better performance in terms of fabrication cost and dynamic range of constant phase angle compared to FOCs from already existing devices. It is important make clear

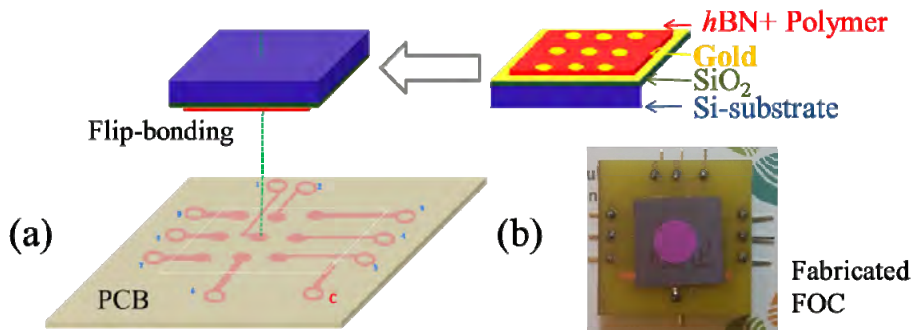


Fig. 5.1: Illustration showing FOC fabrication from bilayer polymer. Photograph showing the final device [84]

here that this schematic is previously proposed by our collaborators [79], [84] however the study based on *h*BN-ferroelectric polymer was not investigated.

5.1 Method

An FOC requires an insulator with high dielectric constant, dissipation factor, and dielectric loss. One potential candidate with such electrical properties is P(VDF-TrFE-CFE) terpolymer. Thus, it is a good reason to explore the possibility of using terpolymer in FOC fabrication. They are easily available in the market and good candidates after a closer look at the behavior of the phase angle. This behavior can be tracked by studying the relaxation phenomenon due to polarization, e.g. dipolar (orientation), ionic and interfacial polarization, in polymer dielectrics. For instance, when a time-dependent electrical field is applied, the permanent (or induced) dipoles tend to align along the direction of the applied electric field. The frequency of the applied field determines how the dipoles behave: if the frequency is small, the dipoles are easily polarized, and the material behaves as close to the ideal capacitor ($\varphi = -90°$). However, at higher frequencies, the dipoles do not have enough time to respond therefore remain the electrical field and therefore remain relaxed ($\varphi = -90°$). At intermediate frequencies, friction accompanies the polarization, resulting in a conductive electrical current and a complex permittivity (with an imaginary part). Consequently, the phase angle satisfies $-90° < \varphi < 0°$, which allows us to design FOC. This phenomenon is called dipolar (or orientation) relaxation [69], [134].

Thus, using the phenomenon above and using the formulas from section 2.2, the *h*BN is selected as a good candidate to fabricate *h*BN-ferroelectric polymer based FOC. The fabrication procedure is given as the following:

- 200 mg P(VDF-TrFE-CFE) is dissolved in a 2 ml solvent, N, N-Dimethylformamide (DMF), under constant stirring at room temperature for two days to obtain 0.1 g/ml polymer solution.
- The *h*BN powders are dispersed in DMF at a concentration of {50, 100, 150, 200, 250} mg/ml and stirred one hour using ultrasonication.
- {5, 10, 15} mg of CNTs are suspended in 1 ml DMF, and dispersed via ultrasonication for 1 hour.
- The dispersed CNT solutions are poured onto the dissolved *h*BN:P(VDF-TrFE-CFE) polymer solution and mixed under continuous stirring for another 24 hours. This step is valid only for *h*BN:P(VDF-TrFE-CFE):CNT composites.
- 10 nm Ti followed by 190 nm Au is deposited on Si/SiO_2 wafers via DC sputter to define the bottoms of the electrodes.
- Then, the composite solutions are drop-casted onto the Au-deposited 2 cm x 2 cm wafers and dried for 12 hours 90°C under a vacuum.
- The circular Au electrode with 3 mm diameter and 200 nm thickness is deposited by similar method using a shadow mask to permit the fabrication of nine individual FOCs on a 2 cm x 2 cm sample area. The FOC fabrication process is depicted in Fig. 5.1.

Two types of FOCs are fabricated using two different knobs. First is the *h*BN:P(VDF-TrFE-CFE) polymer blend while second is its composition with CNT.

Their material and electrical characterization with different volume ratios of *h*BN and CNT are given in following chapters.

5.2 Characterization of the Device

The transmission electron microscopy (TEM) image in Fig. 5.2 shows an exfoliated *h*BN nanosheet with a 0.5 µm and 200 nm lateral size. Furthermore, the TEM image of the P(VDF-TrFE-CFE) composite with fillers of *h*BN and CNT is shown in Fig. 5.3. The CNTs are clearly distinguished from the polymer in the TEM image of the composite provided in Fig. 5.3.

The change in CPA and impedance with composition might imply that the electrical properties of the devices e.g., P(VDF-TrFE-CFE), *h*BN:P(VDF-TrFE-CFE) and *h*BN:P(VDF-TrFE-CFE) containing CNTs are modified in the blend. To further investigate this, the five different blends using X-ray powder diffraction (XRD) techniques are studied. Results are shown in Fig. 5.4 in full spectrum. Note that the XRD spectra are normalized with respect to the gold peak at 38°.

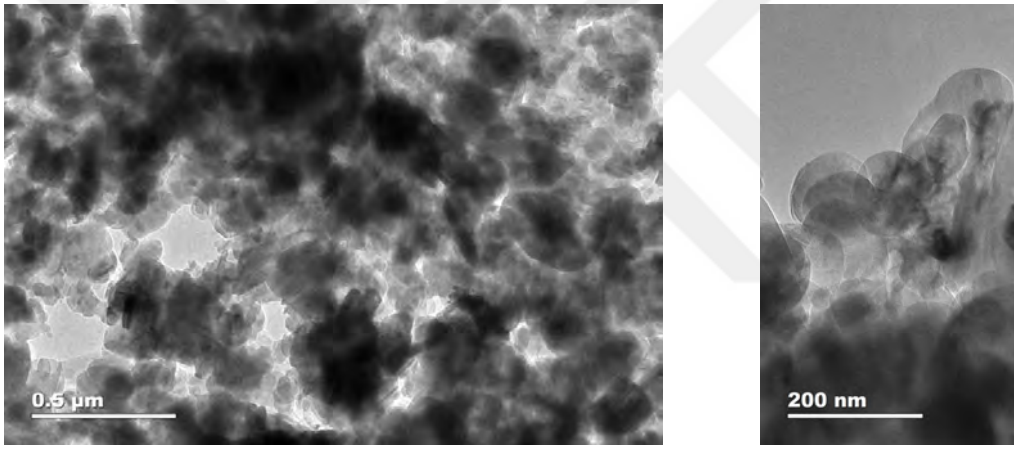


Fig. 5.2: Material characterization of the developed *h*BN:P(VDF-TrFE-CFE) based FOC. TEM image of the stacked BN particle, defoliated layers

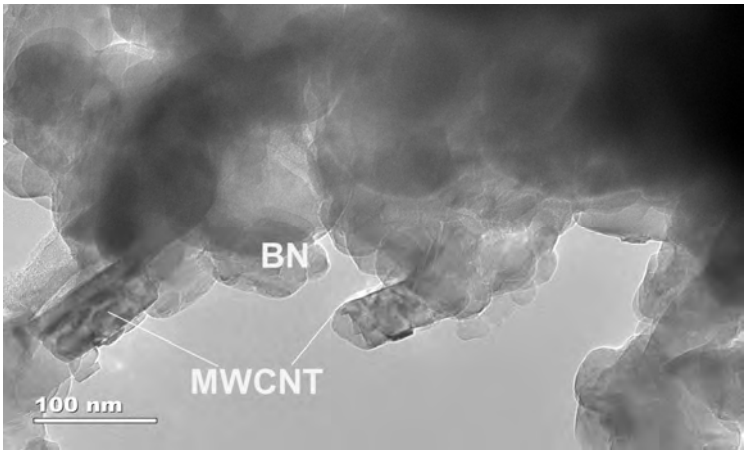


Fig. 5.3: TEM image of the *h*BN polymer composites with CNT

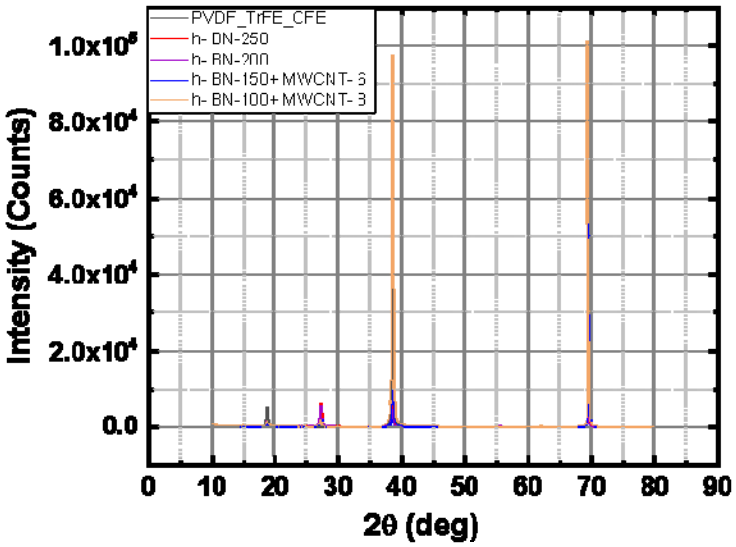


Fig. 5.4: XRD spectra for P(VDF-TrFE-CFE), *h*BN:P(VDF-TrFE-CFE) with two different concentration and *h*BN:P(VDF-TrFE-CFE) containing CNT in full spectrum

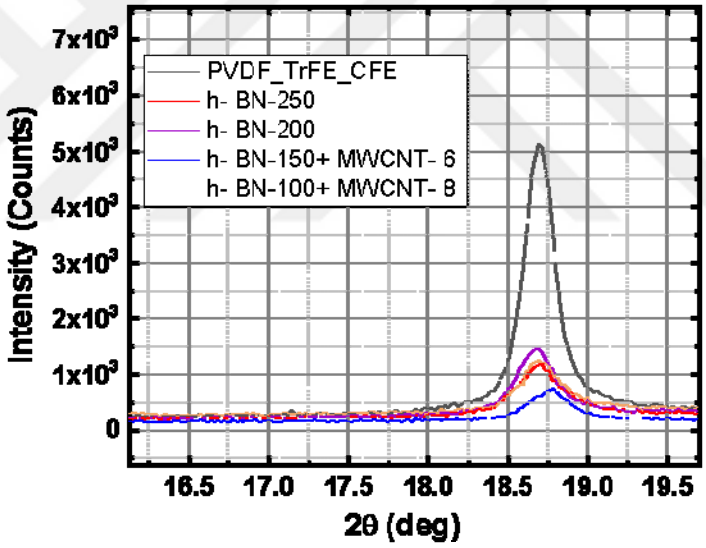


Fig. 5.5: XRD spectra for P(VDF-TrFE-CFE), *h*BN:P(VDF-TrFE-CFE) with two different concentration and *h*BN:P(VDF-TrFE-CFE) containing CNT in narrow spectrum. Note that there is an intense peak at 18.6° which belongs to P(VDF-TrFE-CFE) signature

In Fig. 5.5, the XRD spectrum of the P(VDF-TrFE-CFE) film shows an intense peak at 18.6°, which is close to the theory at 18.2° corresponding to a (111) plane. The higher d-spacing in P(VDF-TrFE-CFE) is due to the TrFE-CFE molecules merging into the PVDF chains. An additional peak is observed around 27.3° in the spectrum of the composite due to interlayered spacing between adjacent *h*BN layers of CNTs as shown in Fig. 5.6. This is consistent with the results that have been reported in the literature. The XRD spectrum of the composite also confirms that no additional complex molecular structures are formed at the interface.

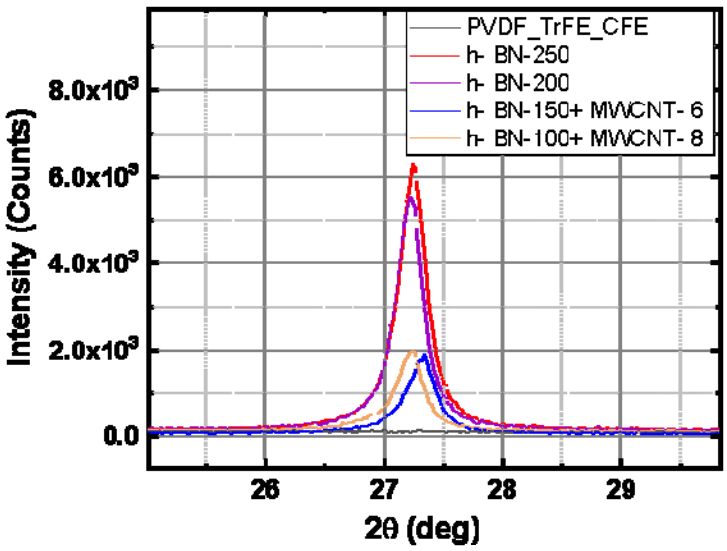


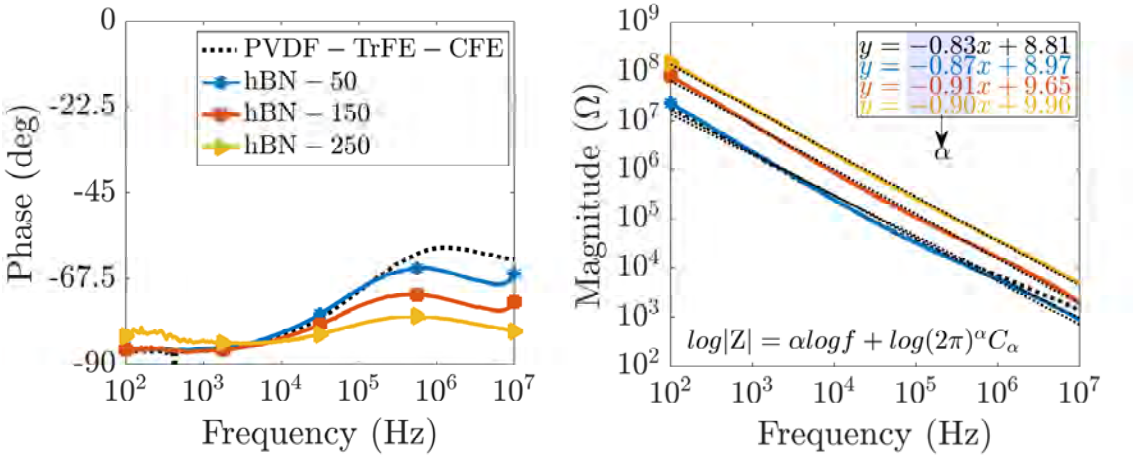
Fig. 5.6: XRD spectra for P(VDF-TrFE-CFE), *h*BN:P(VDF-TrFE-CFE) with two different concentration and *h*BN:P(VDF-TrFE-CFE) containing CNT in narrow spectrum. Note that there is an intense peak around 27.3° which shows the *h*BN signature

5.3 Results and Discussions

An Agilent 4294A Precision Impedance Analyzer was used for the electrical measurements. Individual FOCs were characterized for the impedance, and phase angle in the frequency range of 100 Hz - 10 MHz (logarithmically spaced 200 points) at 0.5 V. Standard calibration tests (short, and open circuits) as provided in the manual were performed to calibrate the instrument.

First, the best phase response of *h*BN:P(VDF-TrFE-CFE) composite is investigated. Fig. 5.7(a) plots the phase versus frequency for different volume ratio of the *h*BN and only P(VDF-TrFE-CFE). Figure clearly shows that the most stable phase response is obtained from the 250 mg *h*BN-polymer blend. This is because the constant phase zone overlaps with the frequency range where dipolar relaxation occurs in the ferroelectric polymer. Additionally, the magnitude responses of FOCs are shown in Fig. 5.7(b). Their magnitude of the impedance decrease by increasing the frequency as proved the impedance formula. The fractional order can be calculated either from the phase angle or the fitting equation given in Fig. 5.7(b) (left-bottom).

Using linear least square algorithm, the fitted equations for magnitudes of FOCs are given inside the same figure and shows the estimated orders fit from the measured phase responses. The best CPA is observed with 250 mg *h*BN composite. The average CPA and PAD are evaluated in Tab. 5.1 in the frequency range of each decade. The minimum PAD is ±0.1° between 1 kHz - 10 kHz while in full range only ±2.2°. Secondly, the tuning of FOCs is obtained by using CNT in different ratios. The phase response of the four FOCs based on *h*BN:CNT polymer composite (100 mg *h*BN and {5, 8, 9, 11} mg CNTs), and one FOC based on *h*BN:P(VDF-TrFE-CFE) composite and one FOC based on P(VDF-TrFE-CFE) composites are shown in Fig. 5.8. Figures 5.7(a)



(a) (b)

Fig. 5.7: (a) Phase and (b) magnitude response of various *h*BN+P(VDF-TrFE-CFE) composite

Tab. 5.1: Evaluation of 250 mg *h*BN-polymer composite in each decade

Frequency range	Average CPA	PAD
10^2 - 10^3	–82.5°	±1.0°
10^3 - 10^4	–84.2°	±0.1°
10^4 - 10^5	–81.8°	±1.2°
10^5 - 10^6	–77.8°	±0.2°
10^6 - 10^7	–79.4°	±0.9°
10^2 - 10^7	–81.2°	±2.2°

and 5.8 clearly show that the phase angle level in the 100 Hz - 10 MHz range is increased by introducing the conductive fillers CNT into the P(VDF-TrFE-CFE) films. This could be explained with the overlap of two phenomena [87]: 1) Maxwell-Wagner-Sillars relaxation that occurs at the interface of the filler and polymer matrix. 2) Dipolar relaxation that takes place at intermediate frequencies. Adding more filler results in shifting of Maxwell-Wagner-Sillars relaxation towards higher frequencies. Therefore, the overlap between the two phenomena increases the phase angle level of the composite at the frequency zone where the dipolar relaxation occurs. The electrical properties of the materials help us to select the best material to reach in desired frequency range and order. However, the design limitations and some additional effects during fabrication processes push us to use trial method. Therefore, the several experiments have been done to find the best FOC. Finally, the obtained CPAs from the fabricated best FOCs are evaluated in Fig. 5.9 and Tab 5.2. The {200, 250 mg *h*BN-polymer composites and 100 mg *h*BN with {6, 8} mg CNT polymer composites are among them. The minimum CPA is obtained from 250 mg *h*BN polymer composite with ±2.2° phase ripple while the maximum is from 8 mg CNT filler in 100 mg *h*BN-polymer composite with ±4° phase ripple. The detailed analysis is given in Tab. 5.2.

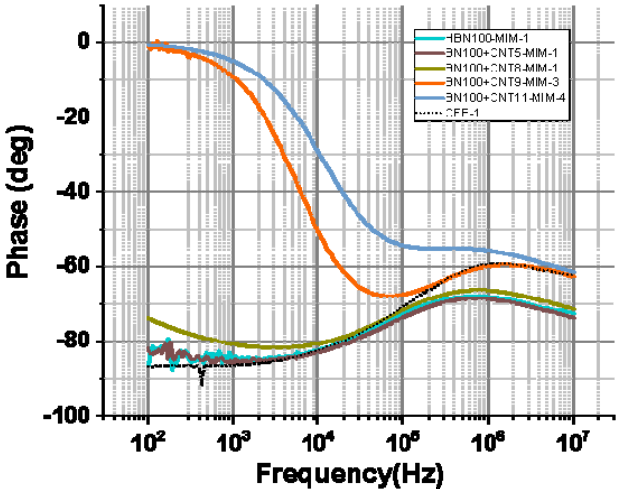


Fig. 5.8: Constant phase angle with tuning CNT in *h*BN polymer composite

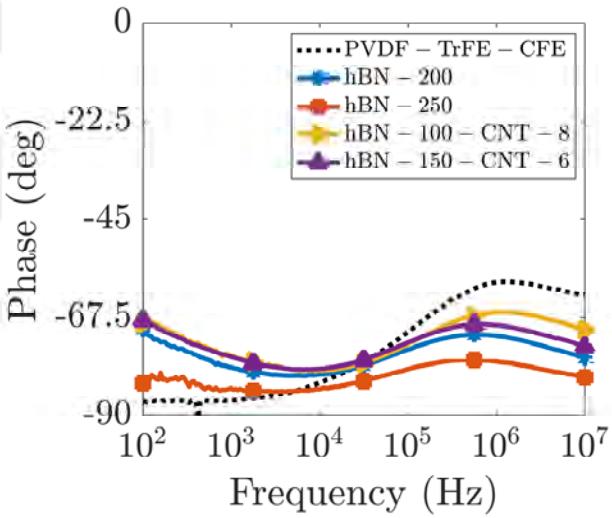


Fig. 5.9: Constant phase angle responses of best *h*BN polymer composite

Tab. 5.2: CPA comparison of the *h*BN and *h*BN:CNT polymer composite based FOCs

Frequency range (Hz)	*h*BN-100 + CNT-8		*h*BN-150 + CNT-6		*h*BN-200		*h*BN-250	
	Average (°)	Variation in (°)	Average (°)	Variation in (°)	Average (°)	Variation in (°)	Average (°)	Variation in (°)
$10^2 – 10^3$	–70.2	±2.7	–72.8	±2.2	–75.3	±2.1	–82.5	±1
$10^3 – 10^4$	–77.2	±1	–78.7	±0.7	–80.4	±0.4	–84.2	±0.1
$10^4 – 10^5$	–76.6	±1.4	–76.8	±1.6	–78.2	±1.5	–81.8	±1.2
$10^5 – 10^6$	–68.8	±0.9	–70.2	±0.5	–72.4	±0.4	–77.8	±0.2
$10^6 – 10^7$	–67.8	±1.1	–71.4	±1.3	–74.1	±1.3	–79.4	±0.9
$10^2 – 10^7$	–72.1	±4	–74	±3.2	–76.1	±2.9	–81.2	±2.2

5.4 Summary

A solid-state FOC design based on *h*BN: P(VDF-TrFE-CFE) polymer composite is presented. Results are optimized within a frequency range of 100 Hz – 10 MHz. The best, optimum devices are found using {200, 250} mg *h*BN, 100 mg hBN mix with 8 mg CNT, and 150 mg hBN mix with 6 mg CNT –polymer composites with ±2.9°, ±2.2°, ±4°, ±3.2° phase error, respectively. To the best of the author' knowledge, these are best results in given bandwidth until now in open literature. Moreover, the advantages of this new method can be summarized as:

- Fabrication cost of this new FOC is expected to be lower than that of the previously developed FOCs [145]
- Fabrication process employs simple solution-mixing and drop-casting approach
- Relatively small error in larger dynamic range
- Variability of the phase reached with controlling two tuning parameter: concentration of *h*BN or CNT

This work demonstrates that FOCs fabricated using CNT-ferroelectric polymers composites have the potential to become essential components for reliable/robust electrical and electronic systems.

6 ANALYSIS AND VERIFICATION OF IDENTICAL- AND ARBITRARY-ORDER SOLID-STATE FRACTIONAL-ORDER CAPACITOR NETWORKS

6.1 Mathematical Description of *n* FOCs Connection

The lossy nature of the dielectric material in capacitors and their electrical conductivity does not allow us to treat them as ideal capacitors since their impedances show a complex frequency-dependent behavior. Due to this fact a FOC, also called as constant phase element, possess both a real and imaginary impedance part $Z(j\omega) = 1\Big/\left(\omega^{\alpha} C_{\alpha}\left[\cos\left(\frac{\alpha\pi}{2}\right) + j\sin\left(\frac{\alpha\pi}{2}\right)\right]\right)$ while its phase is frequency independent. However, an ideal capacitor has only an imaginary part [12]. This is particularly important, if the proposed application requires a configuration using capacitors, where errors accumulate the metrics of the individual components. Therefore, the main contributions of the study in this chapter are:

- The general formulas for impedance, magnitude, and phase response of the series and parallel arbitrary-order *n* FOCs according to the main definition of the FOC are given as a complete study. Furthermore, the units of these physical dimensions are discussed.
- Three types of solid-state ferroelectric polymer or reduced Graphene Oxide (rGO)-percolated P(VDF-TrFE-CFE) composite structure-based FOC devices of three different orders are described, together with their precise characterization including their pseudo-capacitances and bandwidth of operation. Note that this is the first experimental verification of series- and parallel-connected FOCs by fabricated solid-state passive FOCs, in contrast to using RC ladder structures [73] or active IC emulators [74].
- Theoretical assumptions calculated via a newly developed MATLAB open access source code given in Appendix B are proved by experimental verification using fabricated passive FOCs. Here it is important to underline that although the integer-order case (identical orders $\alpha = 1$) is well-known as the core of the physical calculation, the fractional-order (arbitrary-orders) as a novel case also matches well with the assumptions and proves our novel core idea.

The rest of the chapter is organized as follows: First, the general formulas for impedance, magnitude, and phase responses of series- and parallel-connected *n* FOCs are derived. Secondly, fabrication process and experimental characterization of three types (orders 0.69 (TP2), 0.92 (P2), 0.62 (G2)) of solid-state compact and stable-in-phase (in the measured frequency range 0.2 MHz − 20 MHz) electric passive FOCs are explained. The experimental results for two and three series-, parallel-, and inter-connected FOCs are presented in following sub-section. Lastly, a brief discussion of obtained results and final conclusions are given, respectively.

6.1.1 Series Connection

In particular, having multiple FOCs in a circuit, the main aim is to replace them with a single equivalent capacitor and/or reach a desired phase angle with a combination of arbitrary-order capacitors. Therefore, considering the connection of n FOCs in series as shown in Fig. 6.1, the impedance of each FOC can be described as: $Z_{\alpha_1}(s) = \frac{1}{s^{\alpha_1} C_{\alpha_1}}$, $Z_{\alpha_2}(s) = \frac{1}{s^{\alpha_2} C_{\alpha_2}}$, $Z_{\alpha_3}(s) = \frac{1}{s^{\alpha_3} C_{\alpha_3}}$, …, $Z_{\alpha_n}(s) = \frac{1}{s^{\alpha_n} C_{\alpha_n}}$. Assuming the voltage across it is $v_{\alpha 1} + v_{\alpha 2} + v_{\alpha 3} + \ldots + v_{\alpha n} = v_{\text{eq,s}}$ and the current flowing through is $i_{\alpha 1} = i_{\alpha 2} = i_{\alpha 3} = \ldots = i_{\alpha n} = i_{\text{eq,s}}$, the equivalent total impedance $Z_{\text{eq,s}}$, and its unit is derived as:

$$Z_{\text{eq,s}}(s) = Z_{\alpha_1} + Z_{\alpha_2} + Z_{\alpha_3} + \ldots + Z_{\alpha_n} = \sum_{i=1}^{n} \frac{1}{s^{\alpha_i} C_{\alpha_i}}. \ (\Omega) \tag{6.1}$$

By using Euler's identity $s = j\omega$, while $j = e^{j\pi/2}$, and substituting in (6.1), the general formulas for equivalent magnitude and phase responses of n FOCs connected in series are expressed as (6.2) and (6.3), respectively, where the indexes from i to k are the numbers of FOCs, each counted from 1 to n. The function of the sum is valid under the condition that $i < j < \ldots < l$ and $k \neq i, j, \ldots, l$. Note that the derived orders of FOCs affect the power of angular frequency and also the degree of the cosine in magnitude function (6.2). Furthermore, the phase of the equivalent FOC is dependent on the angular frequency ω. From (6.3) it is evident that the angle with the positive x-axis is decreasing while the sum of orders is increasing. The phase of FOC must be between $0 < \text{Arg}[Z_{\text{eq,s}}(s)] < -\pi/2$.

Now, let us consider Case I, when FOCs have different pseudo-capacitances, i.e. $C_{\alpha 1} \neq C_{\alpha 2} \neq C_{\alpha 3} \neq \ldots \neq C_{\alpha n}$, while assuming their orders are identical $\alpha_1 = \alpha_2 = \alpha_3 = \ldots = \alpha_n = \alpha$ ($\alpha \in (0,1]$). Then the impedance, magnitude, and phase formulas in (6.1)−(6.3) turn out to be as given in Tab. 6.1, where in (6.4) and (6.5) $\sum_{i=1}^{n} \frac{1}{C_{\alpha_i}} = \frac{1}{C_{\text{eq,s}}}$. The given case study is straightforward since each capacitor will be experiencing the same current and the voltage across each FOC will increase with respect to this current. Thus, the total voltage across all capacitors will increase at a greater rate than the voltage across individual capacitors.

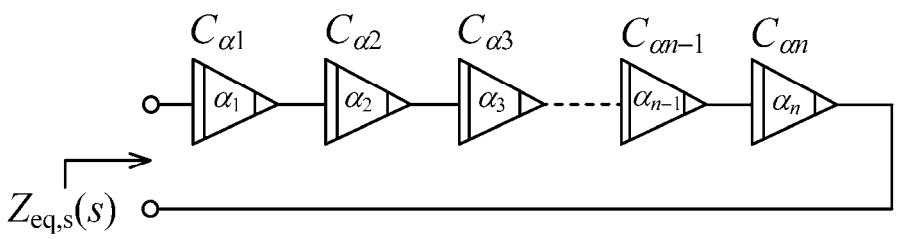


Fig. 6.1: Series-connection of n FOCs

$$\left|Z_{\text{eq,s}}(s)\right| = \frac{\sqrt{\sum_{\substack{i,j,\ldots,l,k=1 \\ i<j<\ldots<l \\ k\neq i,j,\ldots,l}}^{n} \omega^{2(\alpha_i+\alpha_j+\ldots+\alpha_l)} \frac{1}{C_{\alpha_k}^2} + 2\left\{\sum_{\substack{i,j,\ldots,l,k=1 \\ i<j<\ldots<l \\ k\neq i,j,\ldots,l}}^{n} \omega^{\alpha_i+\alpha_j+\ldots+\alpha_l+2\alpha_k} \cos\left[\left(\alpha_i-\alpha_j\right)\frac{\pi}{2}\right]\right\}}}{\prod_{i=1}^{n}\omega^{\alpha_i}}, \quad (\Omega) \qquad (6.2)$$

$$\text{Arg}\left[Z_{\text{eq,s}}(s)\right] = \tan^{-1}\left\{\frac{\sum_{\substack{i,j,\ldots,l,k=1 \\ i<j<\ldots<l \\ k\neq i,j,\ldots,l}}^{n} \omega^{\alpha_i+\alpha_j+\ldots+\alpha_l} \frac{1}{C_{\alpha_k}} \sin\left[\left(\alpha_i+\alpha_j+\ldots+\alpha_l\right)\frac{\pi}{2}\right]}{\sum_{\substack{i,j,\ldots,l,k=1 \\ i<j<\ldots<l \\ k\neq i,j,\ldots,l}}^{n} \omega^{\alpha_i+\alpha_j+\ldots+\alpha_l} \frac{1}{C_{\alpha_k}} \cos\left[\left(\alpha_i+\alpha_j+\ldots+\alpha_l\right)\frac{\pi}{2}\right]}\right\} - \sum_{i=1}^{n}(\alpha_i)\frac{\pi}{2}, \quad \text{(Degree)} \qquad (6.3)$$

Tab. 6.1: Case studies of series-connected FOCs in (6.1)−(6.3)

$Z_{\text{eq,s}}(s)$ (Ω)	$\left\|Z_{\text{eq,s}}(s)\right\|$ (Ω)	$\text{Arg}\left[Z_{\text{eq,s}}(s)\right]$ (Degree)
Case I: $C_{\alpha 1} \neq C_{\alpha 2} \neq C_{\alpha 3} \neq \ldots \neq C_{\alpha n}$ with identical order α		
$\frac{1}{s^{\alpha}}\left(\sum_{i=1}^{n}\frac{1}{C_{\alpha_i}}\right)$ (6.4)	$\frac{1}{\omega^{\alpha}}\left(\sum_{i=1}^{n}\frac{1}{C_{\alpha_i}}\right)$ (6.5)	$-\alpha\frac{\pi}{2}$ (6.6)
Case II: $C_{\alpha 1} = C_{\alpha 2} = C_{\alpha 3} = \ldots = C_{\alpha n} = C_{\alpha}$ with identical order α		
$\frac{n}{s^{\alpha}C_{\alpha}}$ (6.7)	$\frac{n}{\omega^{\alpha}C_{\alpha}}$ (6.8)	$-\alpha\frac{\pi}{2}$ (6.9)

On the other hand, in Case II, when considering the same pseudo-capacitances of FOCs, i.e. assuming $C_{\alpha 1} = C_{\alpha 2} = C_{\alpha 3} = \ldots = C_{\alpha n} = C_{\alpha}$ with identical orders, the impedance, magnitude, and phase in (6.1)−(6.3) respectively become (6.7)−(6.9) of Tab. 6.1. From (6.9) it is clear that the phase is independent of angular frequency and number of capacitances, while the magnitude is dependent on both these values. However, the order of capacitors affects all responses. In other words, FOCs follow the same rule as integer-order capacitors when combined in series only if they have both identical pseudo-capacitances and equal orders. From (6.6) and (6.9), the order of an equivalent FOC can be easily calculated from $\alpha = -2\text{Arg}\left[Z_{\text{eq,s}}(s)\right]/\pi$.

6.1.2 Parallel Connection

When n FOCs with arbitrary order are connected in parallel as shown in Fig. 6.2, the goal is again to replace them with a single equivalent FOC.

According to Kirchhoff's Voltage Law, the voltage across each capacitor must be the same and let us label it as $v_{\mathrm{eq,p}}$. In addition, applying Kirchhoff's Current Law, the sum of currents in nodes will be $i_{\alpha 1} + i_{\alpha 2} + i_{\alpha 3} + \ldots + i_{\alpha n} = i_{\mathrm{eq,p}}$. Hence, by substituting the current flowing through each capacitor in the time-domain and transforming it to the Laplace domain, the equivalent total impedance $Z_{\mathrm{eq,p}}$ of n arbitrary-order FOCs connected in parallel can be expressed as:

$$\frac{1}{Z_{\mathrm{eq,p}}(s)} = \frac{1}{Z_{\alpha_1}} + \frac{1}{Z_{\alpha_2}} + \frac{1}{Z_{\alpha_3}} + \ldots + \frac{1}{Z_{\alpha_n}}, \tag{6.10}$$

$$Z_{\mathrm{eq,p}}(s) = \frac{1}{s^{\alpha_1}C_{\alpha_1} + s^{\alpha_2}C_{\alpha_2} + s^{\alpha_3}C_{\alpha_3} + \ldots + s^{\alpha_n}C_{\alpha_n}} = \frac{1}{\sum_{i=1}^{n} s^{\alpha_i}C_{\alpha_i}}. \quad (\Omega) \tag{6.11}$$

Thus, by substituting in (6.11) $s = j\omega$, while $j = e^{j\pi/2}$, the expressions for magnitude and phase are as follows:

$$\left|Z_{\mathrm{eq,p}}(s)\right| = \frac{1}{\sqrt{\sum_{i=1}^{n}\omega^{2\alpha_i}C_{\alpha_i}^2 + 2\left[\sum_{\substack{i,j=1 \\ i<j}}^{n}\omega^{\alpha_i+\alpha_j}C_{\alpha_i}C_{\alpha_j}\cos\left(\alpha_i-\alpha_j\right)\frac{\pi}{2}\right]}}, \quad (\Omega) \tag{6.12}$$

$$\mathrm{Arg}\left[Z_{\mathrm{eq,p}}(s)\right] = -\tan^{-1}\left[\frac{\sum_{i=1}^{n}\omega^{\alpha_i}C_{\alpha_i}\sin\left(\alpha_i\frac{\pi}{2}\right)}{\sum_{i=1}^{n}\omega^{\alpha_i}C_{\alpha_i}\cos\left(\alpha_i\frac{\pi}{2}\right)}\right]. \quad \text{(Degree)} \tag{6.13}$$

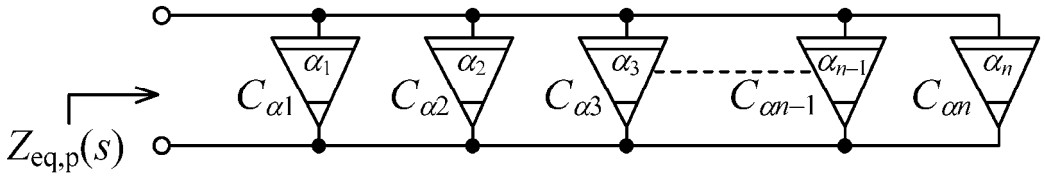


Fig. 6.2: Parallel-connection of n FOCs

Tab. 6.2: Case studies of parallel-connected FOCs in (6.11)−(6.13)

$Z_{\text{eq,p}}(s)$ (Ω)	$\lvert Z_{\text{eq, p}}(s)\rvert$ (Ω)	$\text{Arg}\left[Z_{\text{eq, p}}(s)\right]$ (Degree)
Case III: $C_{\alpha 1} \neq C_{\alpha 2} \neq C_{\alpha 3} \neq \ldots \neq C_{\alpha n}$ with identical order α		
$\dfrac{1}{s^{\alpha}\left(\sum_{i=1}^{n} C_{\alpha_i}\right)}$ (6.14)	$\dfrac{1}{\omega^{\alpha}\left(\sum_{i=1}^{n} C_{\alpha_i}\right)}$ (6.15)	$-\alpha\dfrac{\pi}{2}$ (6.16)
Case IV: $C_{\alpha 1} = C_{\alpha 2} = C_{\alpha 3} = \ldots = C_{\alpha n} = C_{\alpha}$ with identical order α		
$\dfrac{1}{s^{\alpha}\left(nC_{\alpha}\right)}$ (6.17)	$\dfrac{1}{\omega^{\alpha}\left(nC_{\alpha}\right)}$ (6.18)	$-\alpha\dfrac{\pi}{2}$ (6.19)

Again, when considering Case III, where FOCs have identical orders $\alpha_1 = \alpha_2 = \alpha_3 = \ldots = \alpha_n = \alpha$ $(\alpha \in (0, 1])$ but different pseudo-capacitances, i.e. $C_{\alpha 1} \neq C_{\alpha 2} \neq C_{\alpha 3} \neq \ldots \neq C_{\alpha n}$, then the impedance, magnitude, and phase responses are derived as (6.14)−(6.16) of Tab. 6.2, where in (6.14) and (6.15) $\sum_{i=1}^{n} C_{\alpha_i} = C_{\text{eq,p}}$. On the other hand (Case IV), if $\alpha_1 = \alpha_2 = \alpha_3 = \ldots = \alpha_n = \alpha$ $(\alpha \in (0,1])$ and $C_{\alpha 1} = C_{\alpha 2} = C_{\alpha 3} = \ldots = C_{\alpha n} = C_{\alpha}$, then (6.14)−(6.16) turn out to be (6.17)−(6.19).

Similar to Cases I and II of the arbitrary FOCs connected in series, the equivalent order of the resulting network is frequency-dependent and given by (6.13), but if the orders are identical, then it is frequency-independent as shown in (6.16) and (6.19) of Tab. 6.2. However, when *n* identical-order FOCs are connected in parallel, the total equivalent impedance, magnitude, and phase responses are as simple as (6.17)−(6.19). It is worth noting that these relations are similar to integer-order capacitors connected in parallel. Hence, by increasing the number of capacitors, the equivalent magnitude may decrease and equivalent pseudo-capacitance may increase. In addition, the frequency and number of capacitors influence only the magnitude, while the order affects both the magnitude and phase responses. Units of impedance, magnitude, and phase responses of FOCs remain in both the series and parallel cases the same as in the integer-order case, i.e. the impedance and magnitude are in units of ohms and the phase in units of degrees, respectively.

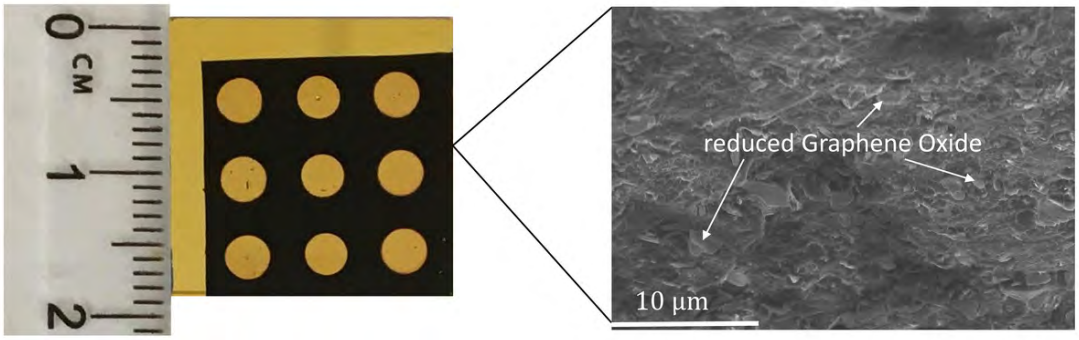
6.2 Experimental Verification

In this section, three types of FOCs of different phase angles are used for experimental verification. In summary, their fabrication procedure is as follows. First, the PVDF and P(VDF-TrFE-CFE) powders are dissolved in a solvent, N, N-Dimethylformamide (DMF) separately in different vials (one vial for PVDF and three vials for P(VDF-TrFE-CFE)), under constant stirring at room temperature for two days to obtain 0.1 mg/ml polymer solutions. An rGO is weighed with the desired weight percentage, suspended in 1 ml DMF, and dispersed via ultrasonication for 1 hour. Later, dispersed rGO solutions are poured onto the dissolved P(VDF-TrFE-CFE) (two vials) polymer solution and mixed under continuous stirring for another 24 hours. In total, three different polymer and composite solutions labeled TP2, P2, and G2 are prepared. Au-covered, $2\text{ cm} \times 2\text{ cm}$ Si/SiO_2 wafers are used to fabricate the FOC by drop-casting the

composite solution. A 10 nm Ti layer followed by 190 nm Au layer is deposited on Si/SiO_2 wafers via DC sputter to define the bottom electrode. The composite solutions are drop-cast and dried for 12 hours at 85 ºC under a vacuum. The other Au circular form electrodes of 3 mm diameter and 200 nm thickness are deposited in a similar way, using a shadow mask. Finally, nine samples of FOCs of the same order are flip-bonded on a printed circuit board and each capacitor gives a separate connection for the electrical measurements [79], [84]. The photo of an example of the fabricated G2 device, including a cross-sectional SEM image of rGO nanosheets/P(VDF-TrFE-CFE) nanocomposite, is shown in Fig. 6.3.

The behavior of three types (TP2, P2, G2) of fabricated FOCs of different orders (respectively $\alpha = \{0.69, 0.92, 0.62\}$) was verified using the Agilent 4294A precision Impedance Analyzer. A photograph of the experimental workstation with fabricated solid-state G2 device is given in Fig. 6.4. During the experimental validation in the frequency range of our interest, 0.2 MHz – 20 MHz (801 logarithmically spaced points), a sinusoidal input signal with a default AC voltage of 500 mV and a frequency of 1 MHz was applied, while the common node was grounded ($V_g = 0$ V). Standard calibration tests (open and short circuits) of the 16047E Test Fixture were performed to calibrate the instrument. The measurement results are summarized in Tab. 6.3. Here, the magnitude, phase angle, i.e. FOC order, pseudo-capacitance, and equivalent integer-order capacitance at center frequency $f_c = 2$ MHz of the corresponding pins of all the devices are provided. From the results, a slight difference in the pseudo-capacitance values within the same device can be observed, which, however, gives us the flexibility to use different values within the same chip. On the other hand, the relative phase error at f_c is significantly low. In addition, the measured phase angle deviation in two decades of the frequency range of our interest is only ±4 degrees ([max – min]/2).

To validate the introduced theory, the series- and parallel-connected identical- and arbitrary-order FOC structures depicted in Figs. 6.1 and 6.2 and their selected interconnections were verified via experimental measurements using fabricated solid-state passive FOCs introduced above. The experimental setup described in this section



(a) (b)

Fig. 6.3: (a) 2 cm × 2 cm fabricated G2 device area with nine FOCs, (b) cross-sectional SEM image of rGO nanosheets/P(VDF-TrFE-CFE) nanocomposite, when the rGO nanosheets are distributed uniformly inside the polymer

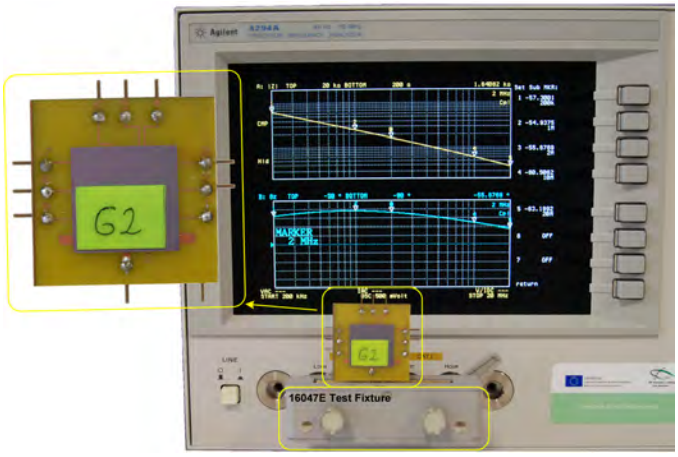


Fig. 6.4: Experimental workstation and the fabricated solid-state G2 device (yellow line - impedance response; cyan-blue line - phase response)

was used. The magnitude and phase responses of equivalent FOCs obtained using the Agilent 4294A precision Impedance Analyzer were proved by theoretical calculations (values given in parentheses in Tabs. 6.4 – 6.7) via the MATLAB open access source code given in Appendix B. In order to compare the FOCs, the fundamental orders (the Warburg pseudo- and integer-order ideal capacitance are set as 790 $nF{\cdot}s^{-0.5}$ and 158 pF, respectively) are plotted in all Figures by means of magnitude and phase.

6.2.1 Identical-Order FOC Connections

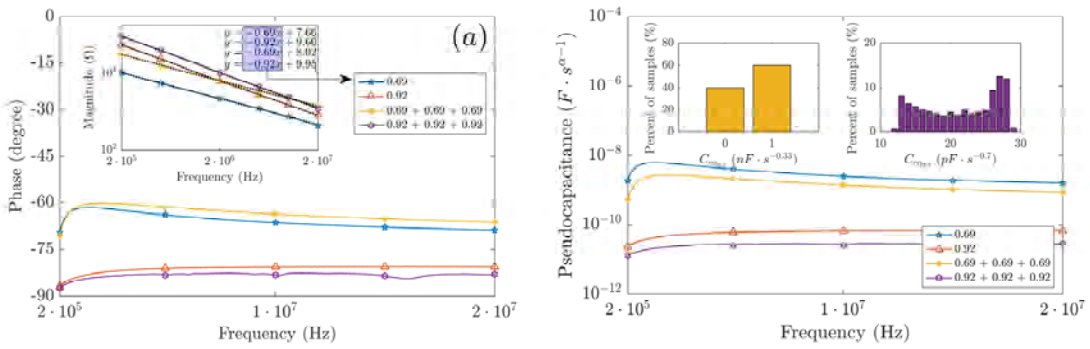
6.2.1.1 Series Connection of Identical-Order FOCs

Considering three series-connected FOCs ($C_{\alpha 2}$, $C_{\alpha 4}$), and assuming each with identical orders, the equivalent impedance, magnitude, and phase responses can be calculated from the equations in Tab. 6.1. The phase, magnitude, and pseudo-capacitance responses of the equivalent impedances $Z_{Ceq,s}(s)$ are shown in Fig. 6.5. For reference, both pseudo-capacitance and phase for an individual FOC have been plotted inside same figures. Compared to a single device, we note that the phase response of three identical order FOCs connected in series remains same. However, its magnitude of the equivalent impedance is tripled while pseudo-capacitance is one-third as shown in the inset of Fig. 6.5(a), and Fig. 6.5(b).

The comparison of measured values @ f_c = 2 MHz and expected results, i.e, calculated via MATLAB are evaluated in Tab. 6.4. For cases #1 → #2 given in Tab. 6.4, equivalent magnitudes vary in ranges $(31.79 \rightarrow 1.36)\,k\Omega$ and $(95.20 \rightarrow 1.19)\,k\Omega$, respectively. The table also includes calculated relative phase error and corresponding pseudo-capacitance of each connection. The magnitude and pseudo-capacitance responses are plotted in the logarithmic scale meanwhile the phase is in linear scale

Tab. 6.3: Measurement results of fabricated fractional-order capacitors (Note: * at f_c = 2 MHz)

Capacitor No.	Device Type	Device Pin No.	$\lvert Z\rvert^*$ (kΩ)	φ^* (Degree)	Order α^* (–)	Pseudo-Capacitance* ($F \cdot s^{\alpha-1}$)	Equivalent C_{int}^* (F)	Phase Angle Deviation in Range (0.2 – 20) MHz (Degree)	Fabrication Technology
$C_{\alpha 1}$	TP2	1	2.37	–61.91	0.69	5.52 n	33.6 p	±4.01	Polymer dielectric
$C_{\alpha 2}$	TP2	4	2.24	–61.86	0.69	5.89 n	35.54 p	±3.84	Polymer dielectric
$C_{\alpha 3}$	P2	9	6.09	–82.63	0.92	49.90 p	13.07 p	±3.18	Polymer dielectric
$C_{\alpha 4}$	P2	8	6.43	–82.59	0.92	47.52 p	12.37 p	±3.12	Polymer dielectric
$C_{\alpha 5}$	G2	1	1.64	–55.68	0.62	24.74 n	48.50 p	±3.15	rGO-Polymer Composite



(a) (b)

Fig. 6.5: Experimental verification of three identical-order FOCs connected in series: (a) phase, magnitude, (b) pseudo-capacitance responses

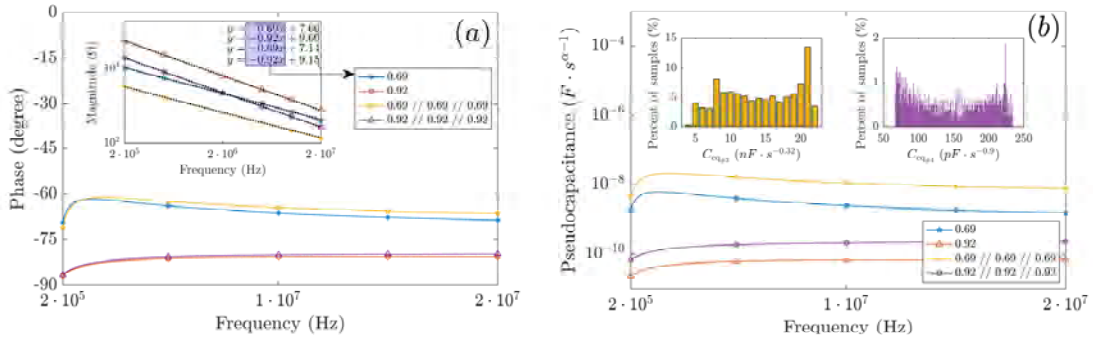
Tab.6.4: Comparison of identical-order series-connected FOCs: Measured and calculated results

No.	#1	#2
Connection of Orders	0.69 + 0.69 + 0.69	0.92 + 0.92 + 0.92
Equivalent Impedance @ f_c (kΩ)	6.58 (6.65)	10.54 (22.09)
Phase (°)	−60.26 (−62.13)	−83.99 (−81.64)
Relative Phase Error (%)	−3.00	2.88
Equivalent Order α (−)	0.67 (0.69)	0.93 (0.91)
Pseudo-Capacitance ($F \cdot s^{\alpha-1}$)	2.68 (1.89) n	22.48 (16.46) p

Moreover, to estimate the equivalent order α (or phase), the measured magnitude data are fitted to the function $\log|Z| = \alpha \log f + \log (2\pi)^{\alpha} C_{\alpha}$ using the linear least squares (LLS) method. The obtained equivalent equations from fitting the magnitude is equal to measurement samples that are provided inside Fig. 6.5(a). As a result, the orders of single devices TP, P2, i.e. 0.69, 0.92 with corresponding phases −61.86°, −82.59° are evidently respond to their equivalent orders from series connections that are found to be 0.67, 0.93 (corresponding to Tab. 6.4 cases #11 → #2 with phases −60.26, −83.99).

6.2.1.2 Parallel Connection of Identical-Order FOCs

In case of parallel connection of three identical-order FOCs as in Fig. 6.2, the equivalent impedance, magnitude and phase responses can be expressed as in Tab. 6.2. In order to demonstrate the behavior of an equivalent FOC with impedance $Z_{Ceq,p}$, the phase, magnitude and pseud-capacitance responses was experimentally verified. The obtained measurement results are shown in Fig. 6.6 while the comparison of measured values @ f_c = 2 MHz and calculated results via MATLAB are listed in Tab. 6.5, respectively. Inspecting the obtained results, it is evident that the phase remains identical to initial single FOCs phase and the only change is in the magnitude response, which reflects the pseudo-capacitance C_{α}. Obviously, the magnitude is the one-third of individual FOC.



(a) (b)

Fig. 6.6: Experimental verification of three identical-order FOCs connected in parallel: (a) phase, magnitude, (b) pseudo-capacitance responses

Tab. 6.5: Comparison of identical-order parallel connected FOCs: Measured and calculated results

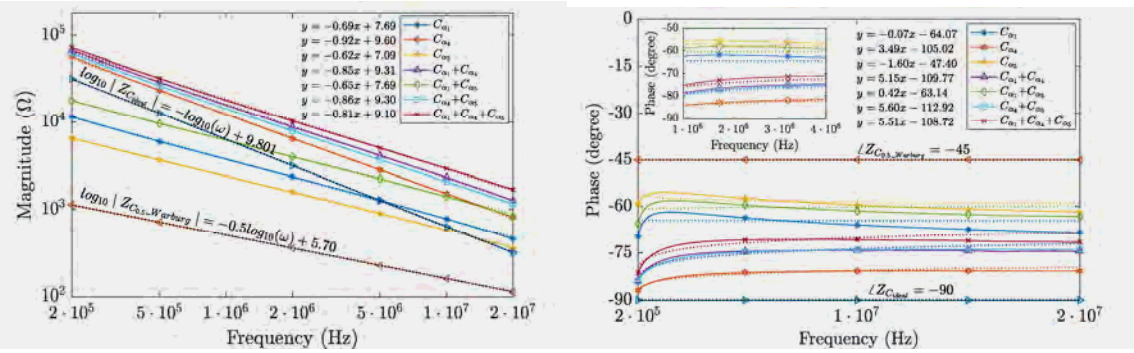
No.	#3	#4
Connection of Orders	0.69 || 0.69 || 0.69	0.92 || 0.92 || 0.92
Equivalent Impedance @ f_c (kΩ)	0.700 (0.737)	2.30 (2.34)
Phase (°)	−61.12 (−62.13)	−82.14 (−82.20)
Relative Phase Error (%)	−1.63	−0.08
Equivalent Order α (−)	0.68 (0.69)	0.91 (0.91)
Pseudo-Capacitance (F·s$^{\alpha-1}$)	21.55 (17.04) n	144.45 (140.23) p

The equivalent orders, which are obtained using the LLS fitting and given in Fig. 6.6(a) as an inset, are found to be 0.69 and 0.92 as equal to related FOC order. The calculated relative phase errors for these cases are –1.63% and –0.08%. It is worth to note that the accuracy of above theoretical analyzes are verified and showed a flexibility and degree of freedom to work with any order of FOCs with a random connection.

6.2.2 Arbitrary-Order FOC Connections

6.2.2.1 Series Connection of Arbitrary-Order FOCs

Firstly, the magnitude and phase responses of two and three arbitrary-order series-connected FOCs are studied. The results obtained, including each individual FOC, are shown in Figs. 6.7(a) (magnitude) and (b) (phase), while the comparison of measured values at f_c = 2 MHz and calculated results is evaluated in Tab. 6.6. To estimate the equivalent order α (or phase), the magnitude data measured are fitted to the function $\log|Z| = \alpha \log f + \log(2\pi)^{\alpha} C_{\alpha}$ using the LLS method. Note that the magnitude responses are given in the logarithmic scale, while the phase responses in linear scale. The equivalent equations from fitting the magnitude or phase as obtained from measurement



(a) (b)

Fig. 6.7: Two and three arbitrary-order FOCs connected in series: (a) magnitude, (b) phase responses

samples are provided inside Fig. 6.7. From the results the orders are evident of FOCs as single devices TP2, P2, G2, i.e. 0.69, 0.92, and 0.62, with corresponding phases −61.91°, −82.59°, and −55.68°, while their equivalent orders from series connections are found to be 0.85, 0.65, 0.85, 0.81 (corresponding to Tab. 6.6 cases #1 → #4 with phases −76.11, −58.19, −76.81, −72.49).

The equivalent magnitudes vary in ranges of (67.2 → 1.26, 17.87 → 0.829, 61.69 → 1.16, and 72.38 → 1.69) kΩ for cases #1 → #4, respectively. Via experiments we also demonstrated that the phase can be tuned by connecting different orders as depicted in Fig. 6.7(b). Furthermore, Tab. 6.6 gives the corresponding pseudo-capacitances and relative phase errors of measured phases relative to the calculated values, which are at f_c in the range of –2.58% to –0.98%.

6.2.2.2 Parallel Connection of Arbitrary-Order FOCs

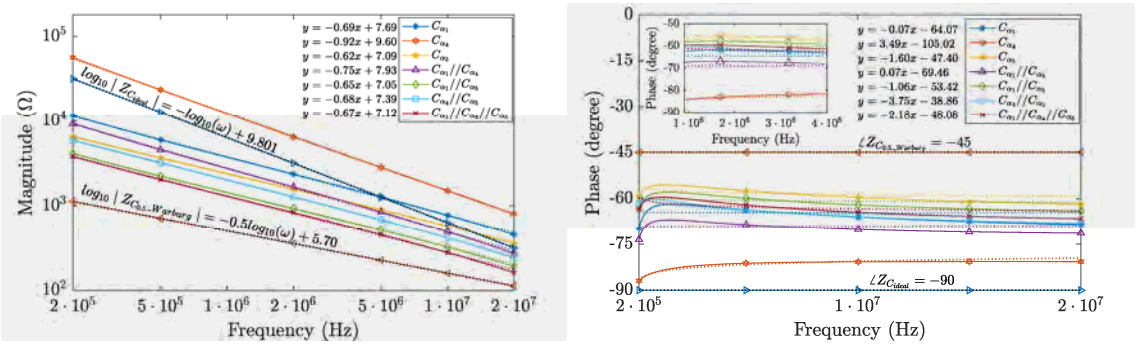
Secondly, the behavior of two and three arbitrary-order FOCs connected in parallel was experimentally verified. The magnitude and phase responses of the equivalent impedances are shown in Figs. 6.8(a) and (b), respectively, while a comparison of the values measured at f_c and the results calculated via the MATLAB open access source code are listed in Tab. 6.7. The equivalent new orders, which are achieved using the LLS fitting and given in Fig. 6.8(a) next to the legend, are found to be 0.74, 0.64, 0.68, and 0.66. As can be observed, the orders match well to those obtained from the measured phase responses, which are depicted in Fig. 6.8(b). Overall, the equivalent impedances have capacitive behavior and vary in ranges of (9.24 → 0.27) kΩ, (4.11 → 0.19) kΩ, (5.84 → 0.24) kΩ, and (3.78 → 0.16) kΩ for cases #5 → #8, respectively. It is also worth noting that the relative phase errors at f_c are again small and vary in the range of –2.65% to 0.10%.

Tab. 6.6: Results of arbitrary-order series-connected two and three FOCs: Measurement (calculated via MATLAB code)

No.	#1	#2	#3	#4
Connection of FOCs	$C_{\alpha 1} + C_{\alpha 4}$	$C_{\alpha 1} + C_{\alpha 5}$	$C_{\alpha 4} + C_{\alpha 5}$	$C_{\alpha 1} + C_{\alpha 4} + C_{\alpha 5}$
Connection of Orders	0.69 + 0.92	0.69 + 0.62	0.92 + 0.62	0.69 + 0.92 + 0.62
Equivalent Impedance @ f_c (kΩ)	8.72 (8.51)	4.00 (3.82)	7.84 (7.73)	10.22 (9.83)
Phase (°)	−76.11 (−77.31)	−58.19 (−59.73)	−76.81 (−77.57)	−72.49 (−74.03)
Relative Phase Error (%)	−1.55	−2.58	−0.98	−2.08
Equivalent Order α (−)	0.85 (0.86)	0.65 (0.66)	0.85 (0.86)	0.81 (0.82)
Pseudo-Capacitance (F·s$^{\alpha-1}$)	113.78 (93.72) p	6.42 (5.14) n	111.33 (98.47) p	187.33 (148.03) p

Tab. 6.7: Results of arbitrary-order parallel-connected two and three FOCs: Measurement (Calculated via MATLAB code)

No.	#5	#6	#7	#8
Connection of FOCs	$C_{\alpha 1} \parallel C_{\alpha 4}$	$C_{\alpha 1} \parallel C_{\alpha 5}$	$C_{\alpha 4} \parallel C_{\alpha 5}$	$C_{\alpha 1} \parallel C_{\alpha 4} \parallel C_{\alpha 5}$
Connection of Orders	0.69 ‖ 0.92	0.69 ‖ 0.62	0.92 ‖ 0.62	0.69 ‖ 0.92 ‖ 0.62
Equivalent Impedance @ f_c (kΩ)	1.67 (1.72)	0.934 (0.934)	1.28 (1.27)	0.835 (0.812)
Phase (°)	−67.03 (−67.66)	−58.03 (−58.36)	−61.16 (−61.10)	−59.83 (−61.46)
Relative Phase Error (%)	−0.93	−0.57	0.10	−2.65
Equivalent Order α (−)	0.74 (0.75)	0.64 (0.65)	0.68 (0.68)	0.66 (0.68)
Pseudo-Capacitance (F·s$^{\alpha-1}$)	3.10 (2.68) n	28.34 (26.67) n	11.66 (11.89) n	22.84 (17.42) n



(a) (b)

Fig. 6.8: Two and three arbitrary-order FOCs connected in parallel: (a) magnitude, (b) phase responses

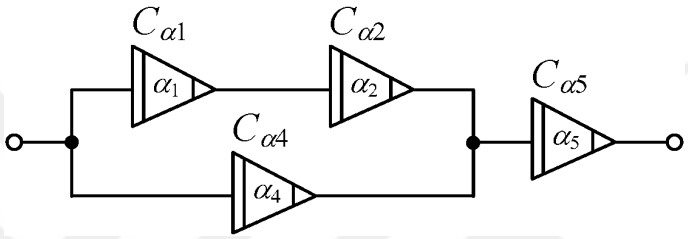


Fig. 6.9: First series-parallel interconnection of arbitrary-order FOCs (#9)

6.2.2.3 Series-Parallel Interconnection of Arbitrary-Order FOCs

Finally, two selected series-parallel interconnections of FOCs were evaluated. The equivalent impedance of the first topology from Fig. 6.9 can be expressed as:

$$Z_{\text{eq,\#9}}(s) = \frac{3s^{\alpha_1}C_{\alpha_1} + 2s^{\alpha_4}C_{\alpha_4}}{s^{\alpha_1+\alpha_5}C_{\alpha_1}C_{\alpha_5} + 2s^{\alpha_4+\alpha_5}C_{\alpha_4}C_{\alpha_5}}, \quad (\Omega) \tag{6.20}$$

where $\alpha_1 \cong \alpha_2 \neq \alpha_4 \neq \alpha_5$ and $C_{\alpha 1} \cong C_{\alpha 2} \neq C_{\alpha 4} \neq C_{\alpha 5}$.

Similarly, the equivalent impedance of the structure given in Fig. 6.10 can be found as:

$$Z_{\text{eq,\#10}}(s) = \frac{2}{2s^{\alpha_1}C_{\alpha_1} + 3s^{\alpha_3}C_{\alpha_3}}, \quad (\Omega) \tag{6.21}$$

while $\alpha_1 \cong \alpha_2 \neq \alpha_3 \cong \alpha_4$ and $C_{\alpha 1} \cong C_{\alpha 2} \neq C_{\alpha 3} \cong C_{\alpha 4}$.

Here it is important to note that this is the very first attempt in the literature to calculate and measure the equivalent magnitude and phase of the arbitrary-order interconnected FOCs. A detailed comparison of the results at f_c is given in Tab. 6.8 and depicted in Fig. 6.11. The equivalent orders of interconnections #9 and #10 obtained

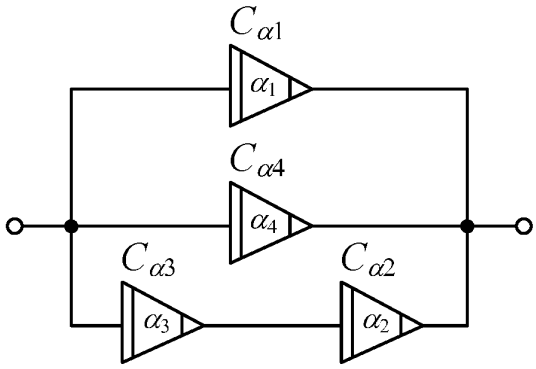
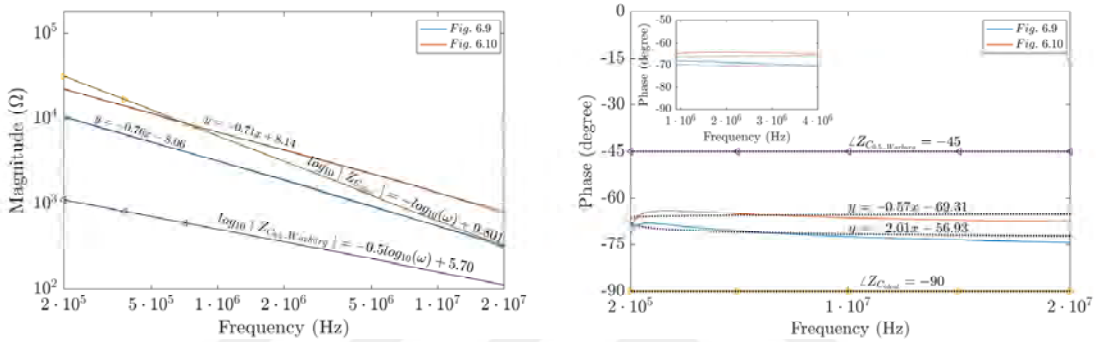


Fig. 6.10: Second series-parallel interconnection of arbitrary-order FOCs (#10)



(a) (b)

Fig. 6.11: Interconnected FOCs given in Figs. 6.9 and 6.10, (a) magnitude, (b) phase responses

Tab. 6.8: Results of interconnected (series-parallel) arbitrary-order FOCs: Measurement (Calculated via MATLAB code)

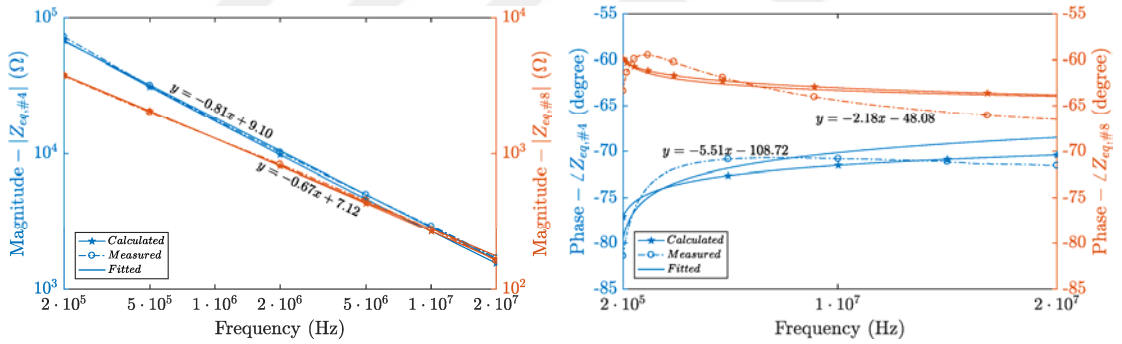
No.	#9	#10
Connection of FOCs	$[(C_{\alpha 1} + C_{\alpha 2}) \parallel C_{\alpha 4}] + C_{\alpha 5}$	$C_{\alpha 1} \parallel C_{\alpha 4} \parallel (C_{\alpha 2} + C_{\alpha 3})$
Connection of Orders	[(0.69 + 0.69) || 0.92] + 0.6	0.69 || 0.92 || (0.69 + 0.92)
Equivalent Impedance @ f_c (kΩ)	4.33 (4.26)	1.91 (1.39)
Phase (°)	−64.09 (−65.58)	−68.68 (−69.27)
Relative Phase Error (%)	−2.27	−0.85
Equivalent Order α (−)	0.71 (0.73)	0.76 (0.77)
Pseudo-Capacitance (F·s$^{\alpha-1}$)	2.04 (1.58) n	2.01 (2.47) n

using the LLS fitting are 0.71 and 0.76, which correspond to the phases −64.09° and −68.68°, respectively. The calculated relative phase errors are respectively −2.27% and −0.85% for the first and second topology, which are very favorable results. Overall, from the results obtained it is clear that the measurement results are in very good agreement with theoretically predicted ones.

6.3 Brief Discussion of Results

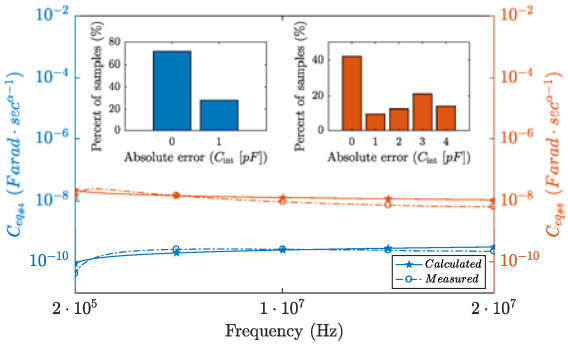
Figures 6.12(a) and (b) give a comparison of the calculated, measured, and fitted line values of the magnitude and phase responses of three arbitrary-order series- and parallel-connected FOCs (cases #4 and #8 of Tabs. 6.6 and 6.7, respectively). It is evident that the results calculated using the MATLAB open access source code match well with the fitted values and the measured values. Furthermore, the equivalent pseudo-capacitance versus frequency is plotted for both circuits in Fig. 6.12(c). As can be observed, the pseudo-capacitance of both FOCs is constant in the same region as the phase is. The normalized histograms show low absolute error between the measured and the calculated equivalent integer-order capacitance values, which is less than 1 pF and 4 pF, respectively, for the series- and parallel-connected FOCs.

Evaluating in brief the obtained results it can be concluded that the equivalent impedances of fabricated arbitrary-order FOCs connected in series and parallel exhibit the same capacitive behavior as integer-order capacitors. Despite the claim in [74], here it is important to underline that the phase responses of series- and parallel-connected FOCs of arbitrary orders are constant. The experimental results are in good agreement with theory and calculated results. Note that the accuracy of the above theoretical analyses is proved and the proposed approach offers flexibility and a degree of freedom to work with any order of FOCs with random connection.



(a)

(b)



(c)

Fig. 6.12: Comparison of (a) magnitude, (b) phase, and (c) pseudo-capacitance versus frequency of three arbitrary-order FOCs connected in series (#4 - blue color) and parallel (#8 - orange color)

6.4 Summary

In this chapter, a novel analytical approach of series- and parallel-connected *n* arbitrary-order FOCs is presented. Particularly, as practical case studies, two and three arbitrary-order FOCs were used in series- and parallel-connected circuits and the magnitude and phase responses, i.e. the order, of the equivalent impedances were evaluated in detail. In addition, the units of these physical dimensions were discussed. Moreover, the very first effort in the literature to derive and validate the equivalent magnitude and phase of arbitrary-order connected FOCs was successfully accomplished.

The behavior of the equivalent FOCs was evaluated experimentally. During the measurements, three fabricated ferroelectric polymer and rGO-percolated P(VDF-TrFE-CFE) composite structure-based FOCs were used. In this regard, FOCs were found to be in orders of 0.69 for the first (TP2), 0.92 for the second (P2), and 0.62 for the third device (G2) over two decades, i.e. in the frequency range $0.2\ \text{MHz} - 20\ \text{MHz}$. The obtained phase angle deviation of single devices at 2 MHz is ± 4 degrees, while the calculated relative phase errors of all studied FOC connections at this frequency varied in a range of –2.65% to 0.10%. Furthermore, the enclosed MATLAB open access source code can be used as a powerful tool for precise calculation of any kind of series or parallel FOC connections based on their order and pseudo-capacitances.

7 DESIGN AND IMPLEMENTATION OF FRACTIONAL-ORDER OSCILLATORS

In the last years, the study of fractional-order oscillators started to be one of the main fundamental topics in fractional-order dynamic systems. This originated from the fact that extremely low and high frequencies of oscillation are possible through such structures [34], [63].

In this chapter, design of voltage-mode fractional-order oscillators, fractional-order Colpitts and Wien oscillators are studied. Main focus of this chapter is to study the effect of FOEs in system equations which results in several design features such as possibility of changing the frequency of oscillation (FO) and condition of oscillation (CO), amplitude and phase etc. Their design in integrated circuit design is another study point. Many classical fractional-order oscillators were presented using conventional op-amps or its equivalent macromodels. Although the aforementioned solutions could be implemented using commercially available discrete-component ICs, from the integration point of view they suffer from the increased transistor count that they are required for implementing the active cells as will be shown in section 7.2. Moreover, part of attention will be on validity check of Barkhausen conditions. Because, an accurate oscillator models are designed with differential equations to be certainly nonlinear due to the lack of unstable periodic oscillations in the pure integer-order or fractional-order linear systems, and also insufficient oscillation condition according to the Barkhausen criteria. Therefore, general fractional-order Barkhausen conditions of oscillation using stability analysis of fractional-order systems are studied in section 7.1.

In addition, to overcome the increased circuit complexity, the power dissipation of the oscillators, novel very simple voltage–mode (VM) fractional-order oscillator topologies are introduced in section 7.2. As for demonstration of the solid-state devices [87], the classic Wien oscillator is experimentally verified.

7.1 Theory

The theory was first presented in [33] and states that a linear fractional-order system with two FOEs can be modelled as follows:

$$\begin{bmatrix} D^{\alpha}V_{o1}(t) \\ D^{\beta}V_{o2}(t) \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} V_{o1}(t) \\ V_{o2}(t) \end{bmatrix} = AV(t). \tag{7.1}$$

Transforming (7.1) into the *s*-domain, the characteristic equation (CE) of the system is obtained as:

$$\mathrm{CE}: \quad s^{\alpha+\beta} - a_{11}s^{\beta} - a_{22}s^{\alpha} + |\mathrm{A}| = 0, \tag{7.2}$$

where $|A| = (a_{11}a_{22} - a_{12}a_{21})$ is the determinant of the system coefficient matrix. Using Euler's expansion $s^{\alpha} = \omega^{(\alpha j\pi/2)}, s^{\beta} = \omega^{(\beta j\pi/2)}$, and writing separately the real and imaginary part:

$$\omega^{\alpha+\beta}\cos(0.5(\alpha+\beta)\pi) - a_{11}\omega^{\beta}\cos(0.5\beta\pi) - a_{22}\omega^{\alpha}\cos(0.5\alpha\pi) + |A| = 0, \tag{7.3a}$$

$$\omega^{\alpha+\beta}\sin(0.5(\alpha+\beta)\pi)-a_{11}\omega^{\beta}\sin(0.5\beta\pi)-a_{22}\omega^{\alpha}\sin(0.5\alpha\pi)=0\,. \tag{7.3b}$$

This system can admit sinusoidal oscillations if and only if a value of ω exists there which satisfies simultaneously the two equations.

Phase difference φ between two outputs $V_{o1}(t)$ and $V_{o2}(t)$ can be calculated as:

$$\varphi=\varphi_{\alpha}-\frac{\pi(1-\mathrm{sgn}(a_{12}))}{2}=\frac{\pi(1-\mathrm{sgn}(a_{21}))}{2}-\varphi_{\beta}\,, \tag{7.4}$$

while $\varphi_{\alpha}=\tan^{-1}\dfrac{\omega^{\alpha}\sin(0.5\alpha\pi)}{\omega^{\alpha}\cos(0.5\alpha\pi)-a_{11}}$, $\varphi_{\beta}=\tan^{-1}\dfrac{\omega^{\beta}\sin(0.5\beta\pi)}{\omega^{\beta}\cos(0.5\beta\pi)-a_{22}}$ and sgn(·) = ±1.

7.2 Compact MOS-RC Voltage-Mode Oscillators

The proposed topologies are demonstrated in Figs. 7.1 and 7.2. Replacing the ideal capacitors C_i for $i = \{1, 2\}$ with a FOC ($C_1 \Rightarrow C_\alpha$, $C_2 \Rightarrow C_\beta$) with impedance of $Z_\alpha(s) = 1/(s^\alpha C_\alpha)$, $Z_\beta(s) = 1/(s^\beta C_\beta)$, the linear fractional-order system can be described as:

$$\begin{pmatrix}\dfrac{d^{\alpha}V_{C_\alpha}}{dt^{\alpha}}\\[2ex]\dfrac{d^{\beta}V_{C_\beta}}{dt^{\beta}}\end{pmatrix}=\begin{pmatrix}\dfrac{g_{m1}}{C_\alpha} & -\left(\dfrac{g_{m1}}{C_\alpha}+\dfrac{1}{RC_\alpha}\right)\\[2ex]\dfrac{g_{m2}}{C_\beta} & -\dfrac{g_{m2}}{C_\beta}\end{pmatrix}\begin{pmatrix}V_{C_\alpha}\\V_{C_\beta}\end{pmatrix}, \tag{7.5}$$

and,

$$\begin{pmatrix}\dfrac{d^{\alpha}V_{o1}}{dt^{\alpha}}\\[2ex]\dfrac{d^{\beta}V_{o2}}{dt^{\beta}}\end{pmatrix}=\begin{pmatrix}-\dfrac{1}{RC_\alpha} & \left(\dfrac{g_{m1}}{C_\alpha}+\dfrac{1}{RC_\alpha}\right)\\[2ex]-\dfrac{1}{RC_\alpha} & \left(\dfrac{g_{m1}}{C_\alpha}+\dfrac{1}{RC_\alpha}\right)-\dfrac{g_{m2}}{C_\beta}\end{pmatrix}\begin{pmatrix}V_{o1}\\V_{o2}\end{pmatrix} \tag{7.6}$$

for Figs. 7.1 and 7.2, respectively. Hence, the CE from (7.2) becomes in general form as:

$$\mathrm{CE}:\quad s^{\alpha+\beta}-s^{\beta}\frac{g_{m1}}{C_\alpha}+s^{\alpha}\frac{g_{m2}}{C_\beta}+\frac{g_{m2}}{C_\alpha C_\beta R}=0\,. \tag{7.7}$$

By solving (7.7) the CO and FO of fractional-order oscillator can be obtained as:

$$\begin{aligned}&\mathrm{CO}:\quad \omega^{\alpha+\beta}\cos\frac{(\alpha+\beta)\pi}{2}-\frac{g_{m1}}{C_\alpha}\omega^{\beta}\cos\frac{\beta\pi}{2}+\frac{g_{m2}}{C_\beta}\omega^{\alpha}\cos\frac{\alpha\pi}{2}+\frac{g_{m2}}{RC_\alpha C_\beta}=0,\\&\mathrm{FO}:\quad \omega^{\alpha+\beta}\sin\frac{(\alpha+\beta)\pi}{2}-\frac{g_{m1}}{C_\alpha}\omega^{\beta}\sin\frac{\beta\pi}{2}+\frac{g_{m2}}{C_\beta}\omega^{\alpha}\sin\frac{\alpha\pi}{2}=0.\end{aligned} \tag{7.8}$$

Then, depending on the selection which capacitor is fractional-order, three possible

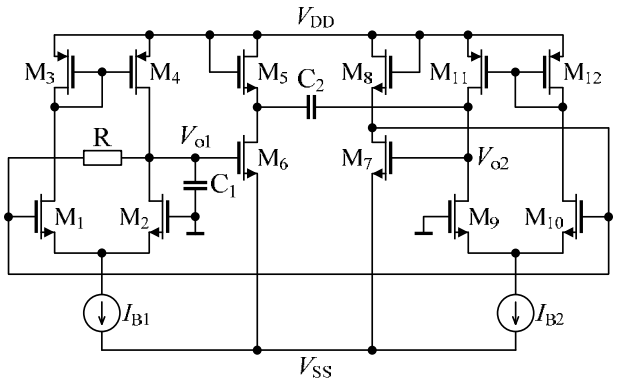


Fig. 7.1: The proposed compact voltage-mode oscillator using OTAs and IVBs

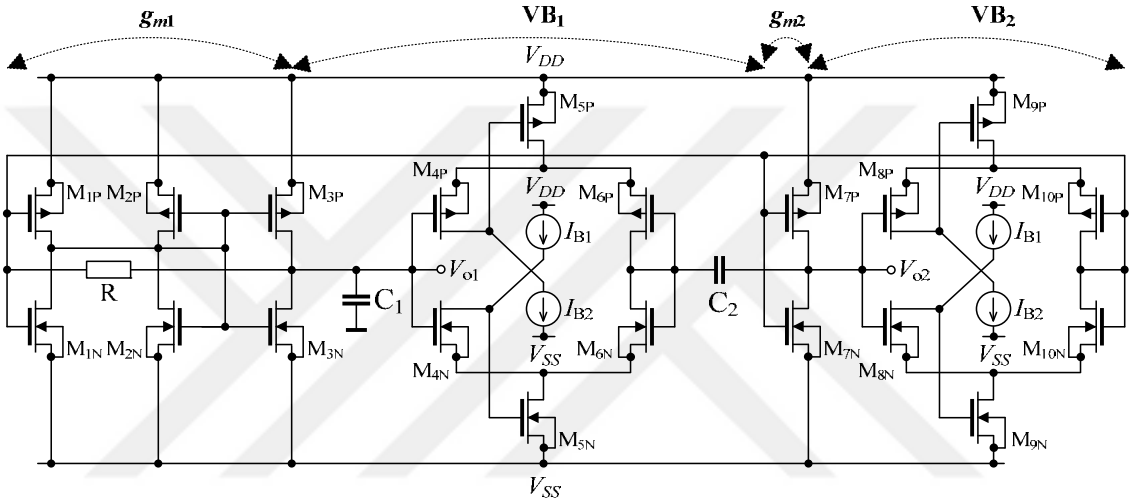


Fig. 7.2: Proposed voltage-mode oscillator using unity-gain voltage buffers and OTAs

cases can be considered:

Case 1: Firstly, the capacitor C_1 is considered to be fractional-order with impedance $Z_{C_1} = 1/\left(s^{\alpha} C_{1\alpha}\right)$, while the other capacitor C_2 remains an integer-order capacitor with impedance $Z_{C_2} = 1/\left(sC_2\right)$.

Case 2: Secondly, the capacitor C_2 is considered as fractional-order capacitor with an impedance $Z_{C_2} = 1/\left(s^{\beta} C_{2\beta}\right)$, while $Z_{C_1} = 1/\left(sC_1\right)$.

Case 3: Lastly, both capacitors are considered as fractional-order capacitors with impedances $Z_{C_1} = 1/\left(s^{\alpha} C_{1\alpha}\right)$, and $Z_{C_2} = 1/\left(s^{\beta} C_{2\beta}\right)$, respectively.

The characteristic equations in all discussed cases can be written as follows:

$$\mathrm{CE}_1: \quad s^{1+\alpha} + s^{\alpha}\frac{g_{\mathrm{m2}}}{C_2} - s\frac{g_{\mathrm{m1}}}{C_{1\alpha}} + \frac{g_{\mathrm{m2}}}{RC_{1\alpha}C_2} = 0\,. \tag{7.9}$$

$$\mathrm{CE}_2: \quad s^{1+\beta} + s\frac{g_{m2}}{C_{2\beta}} - s^{\beta}\frac{g_{m1}}{C_1} + \frac{g_{m2}}{RC_1C_{2\beta}} = 0\,. \tag{7.10}$$

$$\mathrm{CE}_3: \quad s^{\alpha+\beta} + s^{\alpha}\frac{g_{m2}}{C_{2\beta}} - s^{\beta}\frac{g_{m1}}{C_{1\alpha}} + \frac{g_{m2}}{RC_{1\alpha}C_{2\beta}} = 0\,. \tag{7.11}$$

Setting $s = j\omega$ in (7.9) – (7.11), the derived FOs and COs that correspond to the aforementioned cases are summarized in Tab. 7.1.

In fractional-order case the relation between the outputs of the oscillator is:

$$\frac{V_{o1}}{V_{o2}} = -\frac{g_{m1}R+1}{s^{\alpha}RC_{1\alpha}+1}, \tag{7.12}$$

while the phase difference "φ" between two outputs V_{o1} and V_{o2} can be calculated as:

$$\varphi = \tan^{-1}\frac{\omega^{\alpha}\sin(0.5\alpha\pi)}{\omega^{\alpha}\cos(0.5\alpha\pi) - \dfrac{g_{m1}}{C_{1\alpha}}} - \pi = -\tan^{-1}\frac{\omega^{\beta}\sin(0.5\beta\pi)}{\omega^{\beta}\cos(0.5\beta\pi) + \dfrac{g_{m2}}{C_{2\beta}}}. \tag{7.13}$$

Note that setting $\alpha = \beta = 1$ in the expressions in Tab. 7.1 as well as in (7.12) – (7.13), then expressions $\frac{g_{m1}}{C_1} = \frac{g_{m2}}{C_2}$, $\omega_0 = \sqrt{\frac{g_{m2}}{RC_1C_2}}$, $\frac{V_{o1}}{V_{o2}} = -\frac{g_{m1}R+1}{sRC_1+1}$, $\varphi = \tan^{-1}\left(\frac{\omega C_1}{g_{m1}}\right) - \pi = -\tan^{-1}\left(\frac{\omega C_2}{g_{m2}}\right)$, are derived for CO, FO, amplitude, and phase, respectively.

7.2.1 Numerical Analysis

One of the advantages of fractional-order oscillators is to generate higher FOs than their integer-order counterparts. Considering the fractional-order oscillator of Case 3 and assuming typical active parameters of OTA and passive component values as follows: $g_{m1} = g_{m2} = 100$ µA/V, $R = 10$ kΩ, $C_{1\alpha} = 10$ µFs$^{(\alpha-1)}$, then from Tab. 7.1 the following frequency of oscillation and oscillation start-up condition values $f_0 = \{1.18;\ 4.26;\ 1.25\ \mathrm{k}\}$Hz and $C_{2\beta} = \{63.8\ \mu;\ 37.3\ \mu;\ 155\ \mathrm{n}\}Fs^{(\beta-1)}$ for $\alpha = \{0.65;\ 0.5;\ 0.25\}$ and $\beta = \{0.4;\ 0.5;\ 0.9\}$, are derived. Figure 7.3 shows MATLAB plots of frequency of oscillation versus fractional-orders α and β (see in Tab. 7.1 FO of Case 3). As it can be observed the FO increases while the order of α decreases and β increases. In other words, FO decreases while the order of α increases and β decreases. Note that, the CO in integer-order case requires equality of both capacitances and transconductances. Therefore, considering an integer-order capacitor ($\alpha = 1$) with the same ideal capacitance $C_1 = 10$ µF, the FO and oscillation start-up condition are respectively 1.5915 Hz and 10 µF, as shown in Figures 7.3 and 7.4. Furthermore, it can be observed that the start-up condition $C_{2\beta}$ decreases while the frequency of oscillation increases with increasing the order β or decreasing α. Fig. 7.5 shows the phase difference between

Tab. 7.1: Main design parameters of fractional-order oscillator

No.	Case	Condition of oscillation, frequency of oscillation
1)	$0<\alpha\le 1$ $\beta=1$	CO: $C_2=\dfrac{\omega^{\alpha-1}g_{m2}C_{1\alpha}\sin(0.5\alpha\pi)}{g_{m1}-\omega^{\alpha}C_{1\alpha}\cos(0.5\alpha\pi)}=\dfrac{g_{m2}\left[\omega^{\alpha}\cos(0.5\alpha\pi)+\dfrac{1}{RC_{1\alpha}}\right]}{\omega^{1+\alpha}\sin(0.5\alpha\pi)}$ FO: $\omega^{2\alpha}g_{m2}C_{1\alpha}+\omega^{\alpha}g_{m2}\cos(0.5\alpha\pi)\left(\dfrac{1}{R}-g_{m1}\right)-\dfrac{g_{m1}g_{m2}}{RC_{1\alpha}}=0$
2)	$\alpha=1$ $0<\beta\le 1$	CO: $C_{2\beta}=-\dfrac{g_{m2}}{\omega^{\beta}\cos(0.5\beta\pi)-\omega^{\beta-1}\dfrac{g_{m1}}{C_1}\sin(0.5\beta\pi)}=\dfrac{g_{m2}}{\omega^{1+\beta}RC_1\sin(0.5\beta\pi)+\omega^{\beta}g_{m1}R\cos(0.5\beta\pi)}$ FO: $\omega^2+\dfrac{\omega\cot(0.5\beta\pi)}{RC_1}(g_{m1}R+1)-\dfrac{g_{m1}}{RC_1^{\,2}}=0$
3)	$0<\alpha\le 1$ $0<\beta\le 1$	CO: $C_{2\beta}=\dfrac{\omega^{\alpha}g_{m2}C_{1\alpha}\sin(0.5\alpha\pi)}{-\omega^{\alpha+\beta}C_{1\alpha}\sin(0.5(\alpha+\beta)\pi)+\omega^{\beta}g_{m1}\sin(0.5\beta\pi)}=\dfrac{g_{m2}\left[\omega^{\alpha}RC_{1\alpha}\cos(0.5\alpha\pi)+1\right]}{-\omega^{\alpha+\beta}RC_{1\alpha}\cos(0.5(\alpha+\beta)\pi)+\omega^{\beta}g_{m1}R\cos(0.5\beta\pi)}$ FO: $\omega^{2\alpha}RC_{1\alpha}^{\,2}\sin(0.5\beta\pi)-\omega^{\alpha}g_{m1}RC_{1\alpha}C_{2\beta}\left[\sin(0.5(\alpha-\beta)\pi)+\dfrac{1}{g_{m1}R}\sin(0.5(\alpha+\beta)\pi)\right]+g_{m1}\sin(0.5\beta\pi)=0$

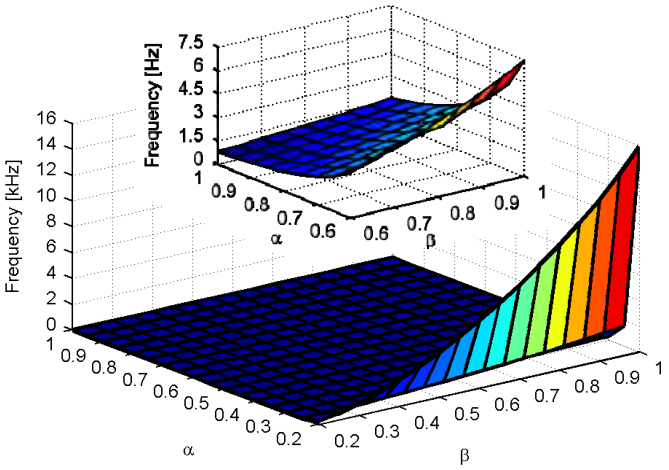


Fig. 7.3: Frequency of oscillation versus alpha (α) and beta (β)

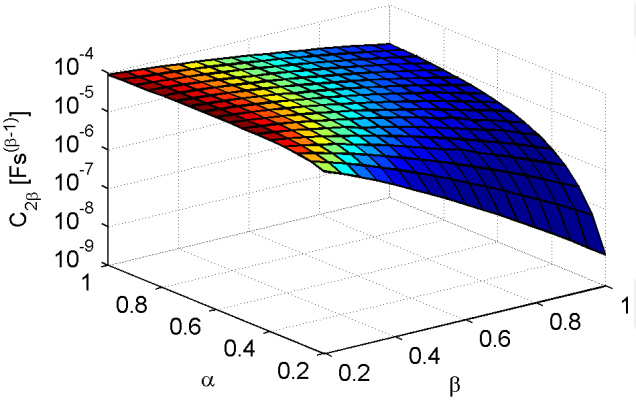


Fig. 7.4: Condition of oscillation versus alpha (α) and beta (β)

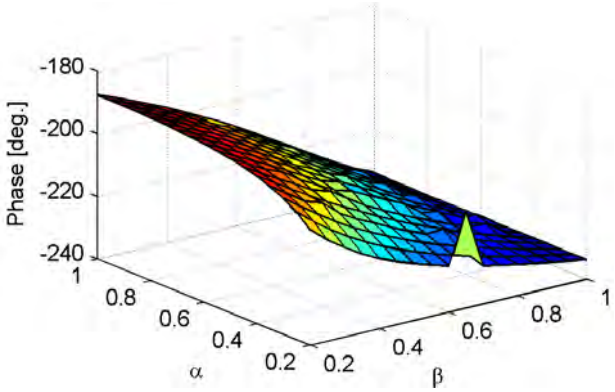


Fig. 7.5: Phase difference between the outputs versus alpha (α) and beta (β)

with increasing the order β or decreasing α. Fig. 7.5 shows the phase difference between two outputs based on (7.13). Considering again the orders $\alpha = \{0.65; 0.5; 0.25\}$ and $\beta = \{0.4; 0.5; 0.9\}$, the phase differences were calculated as $\phi = \{-199.4°; -208.7°; -231.6°\}$, respectively. Hence, by increasing the order α or decreasing β the phase difference is increasing.

7.2.2 Simulation Results

7.2.2.1 Fractional–Order Oscillator Employing OTAs and IVBs

The proposed topology is demonstrated in Fig. 7.1. It is constructed from two CMOS OTAs ($M_1 - M_4$ and $M_9 - M_{12}$), two NMOS based IVBs ($M_5 - M_8$), one resistor, and two capacitors.

In order to validate the numerical results of the proposed oscillator, the simulation results were performed using SPICE program. In the design, transistors were modeled by the TSMC 0.18 µm Level-7 CMOS process parameters (V_{th_N} = 0.35 V, μ_N = 327 cm^2/(V·s), V_{th_P} = –0.41 V, μ_P = 129 cm^2/(V·s), T_{OX} = 4.1 nm). The DC power supply voltages were set equal to $+V_{DD} = -V_{SS}$ = 1 V. Aspect ratios of CMOS transistors are W/L = 40 µm/1.2 µm for all PMOS and W/L = 0.8 µm/1.2 µm for NMOS in OTAs. In inverting voltage buffers both NMOS were set W/L = 60 µm/1 µm. The bias currents in OTAs were set $I_{B1} = I_{B2}$ = 100 µA, which results in transconductance equal to 100 µA/V.

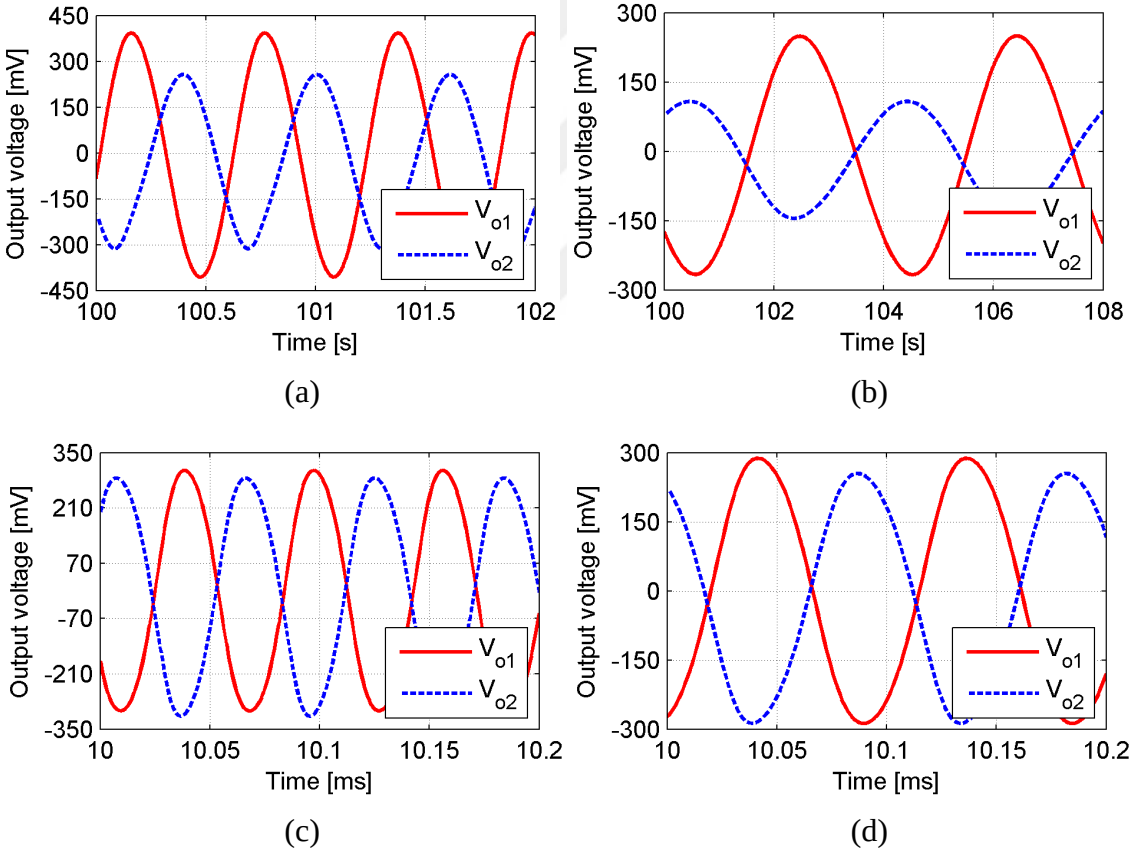


Fig. 7.6: Transient responses of the output voltages: (a) $\alpha = 1$ and $\beta = 1$, (b) $\alpha = 1$ and $\beta = 0.2$, (c) $\alpha = 0.2$ and $\beta = 1$, (d) $\alpha = 0.2$ and $\beta = 0.8$

Tab. 7.2 Component values used in Fig. 7.1 for simulation of fractional-order oscillator

Components	Component Values			
	Case 1	Case 2	Case 3	
	$\alpha = 0.2$ $C_\alpha = 10\ \mu Fs^{-0.8}$ @15.9 kHz	$\beta = 0.2$ $C_\beta = 91.21\ \mu Fs^{-0.8}$ @0.25 Hz	$\alpha = 0.2$ $C_\alpha = 10\ \mu Fs^{-0.8}$ @9.64 kHz	$\beta = 0.8$ $C_\beta = 89.9\ nFs^{-0.2}$ @9.64 kHz
R_a (Ω)	5.45 k	5.45 k	6.03 k	79.1
R_b (Ω)	4.3 k	4.26 k	4.7 k	659.6
C_b (F)	836 p	52.8 µ	1.25 n	19.3 n
R_c (Ω)	8.6 k	8.61 k	9.52 k	34.1 k
C_c (F)	5.97 n	376.9 µ	8.91 n	376.9 µ

First of all, the integer-order case ($\alpha = \beta = 1$) with passive component values $C_1 = 10$ µF and $R = 10$ kΩ was studied. By solving the system of (7.7) and (7.8), the oscillation start-up condition and frequency of oscillation are found as $C_2 = 10$ µF and $f_{0\_theor\_int} = 1.59$ Hz, which is close to simulated value $f_{0\_sim\_int} = 1.5$ Hz. The simulated phase difference between the outputs was −203.7°, close to −233.7°, which is theoretically predicted by (7.13). The transient responses of the outputs are shown in Fig. 7.6(a) and simulated peak-to-peak values of oscillation amplitudes are $V_{o1\_PP} = 798.4$ mV; $V_{o2\_PP} = 570.1$ mV. The theoretical ratio of amplitudes according to (7.12) is 1, however, by simulations reached one is 1.4.

Secondly, the fractional-order cases are studied for selected orders $\alpha = \{1; 0.2; 0.2\}$ and $\beta = \{0.2; 1; 0.8\}$, respectively. The fractional-order capacitors were realized using the Foster I network depicted in Fig. 7.7. The values of passive elements have been calculated by employing the second-order CFE method, and they are given in Tab. 7.2. The calculated oscillation start-up conditions are $C_{2\beta} = \{91.21\ \mu; 6.31\ n; 89.9\ n\}Fs^{(\beta-1)}$ and the FOs are $f_{0_theor_fract} = \{0.25; 15.9\ k; 9.64\ k\}$Hz, while the simulated FOs are 0.25 Hz, 15 kHz, and 10 kHz, respectively. Transient responses of the outputs for fractional-order cases are shown in Figs. 7.6(b)–(d). The following peak-to-peak values of oscillation amplitudes were simulated for outputs $\{V_{o1}; V_{o2}\}$: Case 1 {516.6; 253.1}mV, Case 2 {608.9; 602.8}mV, and Case 3 {575.1; 542.1}mV, respectively. Here the theoretical ratios of amplitudes according to (7.12) are 1.72; 1; 1.05.

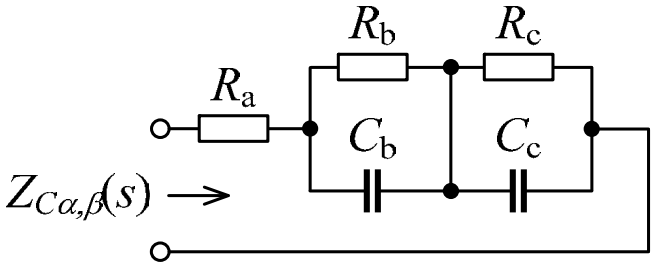


Fig. 7.7: RC tree realization of FOC

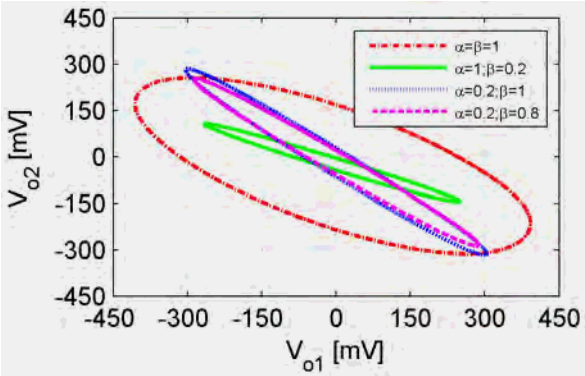


Fig. 7.8: Lissajous patterns of all discussed cases showing phase shifts of V_{o2} against V_{o1}

On the other hand, the simulated ratios are 2.04; 1.01; 1.06. The simulated phase shifts were {−190.05°; −180.03°; −180.1°}, while the calculated values were {−233.7°; −187.5°; −187.9°} while. Lissajous patterns of all discussed cases showing phase shifts between outputs are depicted in Fig. 7.8.

7.2.2.2 Fractional–Order Oscillator Employing Class-AB Flipped Voltage Followers and OTAs.

The CMOS implementation of unity-gain voltage buffer (VB) based on class-AB flipped voltage follower, i.e. $V_{out} = V_{in}$, is shown in Fig. 7.2 [178]. As it is evident, it uses two complementary differential flipped voltage followers (DFVFs) $M_{4P} - M_{6P}$ ($M_{8P} - M_{10P}$) and $M_{4N} - M_{6N}$ ($M_{8N} - M_{10N}$) with quiescent currents I_{B1} and I_{B2}, respectively. When the input voltage signal V_{in} (e.g. from the node between $M_{4P} - M_{4N}$) increases with respect to the output voltage V_{out} (e.g. from the node between $M_{6P} - M_{6N}$), then $V_{SG(M6P)}$ increases while $V_{GS(M6N)}$ decreases. Similarly, current through M_{6P} increases and M_{6N} decreases. This generates a positive output current that charges the load capacitance and increases the output voltage V_{out} until it reaches a value V_{in}. This buffer operates in class AB, resulting in transient currents of the output transistors much larger than their corresponding quiescent currents I_{B1} and I_{B2}. Theoretically, the input and output impedance of this buffer are infinite and zero, respectively.

The CMOS implementation of single-input differential-output transconductor is also shown in Fig. 7.2. Assuming square-law behavior for the current–voltage relationship of the MOS transistors M_{1P} and M_{1N} and ignoring channel-length modulation effect, their drain currents will be given as in [179], [180], and, thus, the current–voltage relationship of the transconductor can be approximated by the linear expression: $I_{out-} = -g_m V_{in}$, where $g_m = k_N V_{DD}$. This linear behavior is achieved under the assumptions: $k_P \cong k_N$ and $V_{SS} \cong V_{DD} + V_{th\_N} - |V_{th\_P}|$, where V_{th_N} and V_{th_P} are the threshold voltages of the NMOS and PMOS transistors. In order to keep the transistors in saturation region, the constraints $V_{D1} + V_{th\_N} \geq V_{in} \geq V_{D1} - |V_{th\_P}|$ should be satisfied, where V_{D1} is the (common) drain voltage of transistors M_{1P} and M_{1N}, respectively. Interconnecting the transconductor with unity-gain current follower (see $M_{2P} - M_{3P}$, M_{7P} and $M_{2N} - M_{3N}$, M_{7N} in Fig. 7.2 [181]) the current–voltage relationship of the transconductor can be characterized with the equation $I_{out+} = g_m V_{in}$.

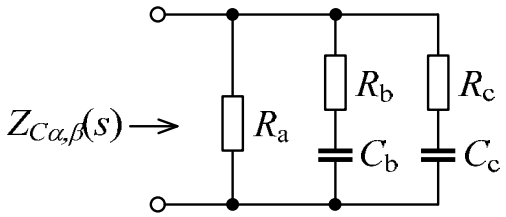


Fig. 7.9: RC tree realization of FOC

Tab. 7.3: Component values used in SPICE simulations for $C_\alpha = 55\ \text{nF}\cdot s^{\alpha-1}$, $C_\beta = 100\ \text{nF}\cdot s^{\beta-1}$

Variables / Orders	$\alpha = 0.5$	$\beta = 0.5$	$\alpha = 0.9$	$\beta = 0.6$
R_a (kΩ)	10.6	5.9	98.6	8.04
R_b (Ω)	508	279.4	39.5	161.3
C_b (nF)	24.3	44.2	48	54.1
R_c (kΩ)	3.5	1.9	85.6	1.9
C_c (nF)	6.4	115.8	14.4	97.3

The behavior of voltage buffer, transconductor, and proposed voltage-mode integer- and fractional-order oscillators have been verified by SPICE simulations. In the design, transistors are modeled by the TSMC 0.35 μm level-3 CMOS process parameters ($V_{th\_N} = 0.545$ V, $V_{th\_P} = -0.714$ V, $\mu_N = 436.26\ \text{cm}^2/(\text{V}\cdot\text{s})$, $\mu_P = 212.23\ \text{cm}^2/(\text{V}\cdot\text{s})$, $t_{OX} = 7.9$ nm). In simulations, the DC power supply voltages of given structures were set equal to $+V_{DD} = -V_{SS} = 1.65$ V and the aspect ratios of MOS transistors were 15 μm/0.5 μm and 5 μm/0.5 μm for all PMOS and NMOS, respectively. The bias currents in voltage buffers were set $I_{B1} = I_{B2} = 250$ μA, which results in DC voltage gain 0.957 with f_{-3dB} frequency of 1.644 GHz. Similarly, the transconductance gains g_{m1} (I_{out+}/V_{in}) and g_{m2} (I_{out-}/V_{in}) are computed as 1.639 mA/V and 1.778 mA/V, respectively, and their f_{-3dB} frequency is found to be 3.83 GHz and 47.63 GHz. Hence, the maximum operating frequency of transconductors are $f_{max} = \min\{f_{gm1}, f_{gm2}\} \approx 3.83$ GHz.

As a first step, the performance of the proposed integer-order oscillator ($\alpha = \beta = 1$) was evaluated. In this case, both capacitances have been chosen as: $C_1 = 55$ nF, $C_2 = 100$ nF, while the resistor was: $R = 1$ kΩ; according to (7.8), the theoretical value of the oscillation frequency was $f_0 = 2.86$ kHz. Figure 7.10(a) shows the simulated output waveforms with frequency of oscillation 1.63 kHz.

As a second step, the fractional-order oscillator with an order of $s^{1.5}$ has been implemented. For this purpose, the capacitors of the integer-order oscillator in Fig. 7.2 were replaced with their fractional-order equivalents which were realized using the second-order RC tree shown in Fig. 7.9. Note that the values of $g_{m1,2}$ have been kept the same with the previous case. Considering that $\alpha = 0.9$ and $\beta = 0.6$, their equivalent

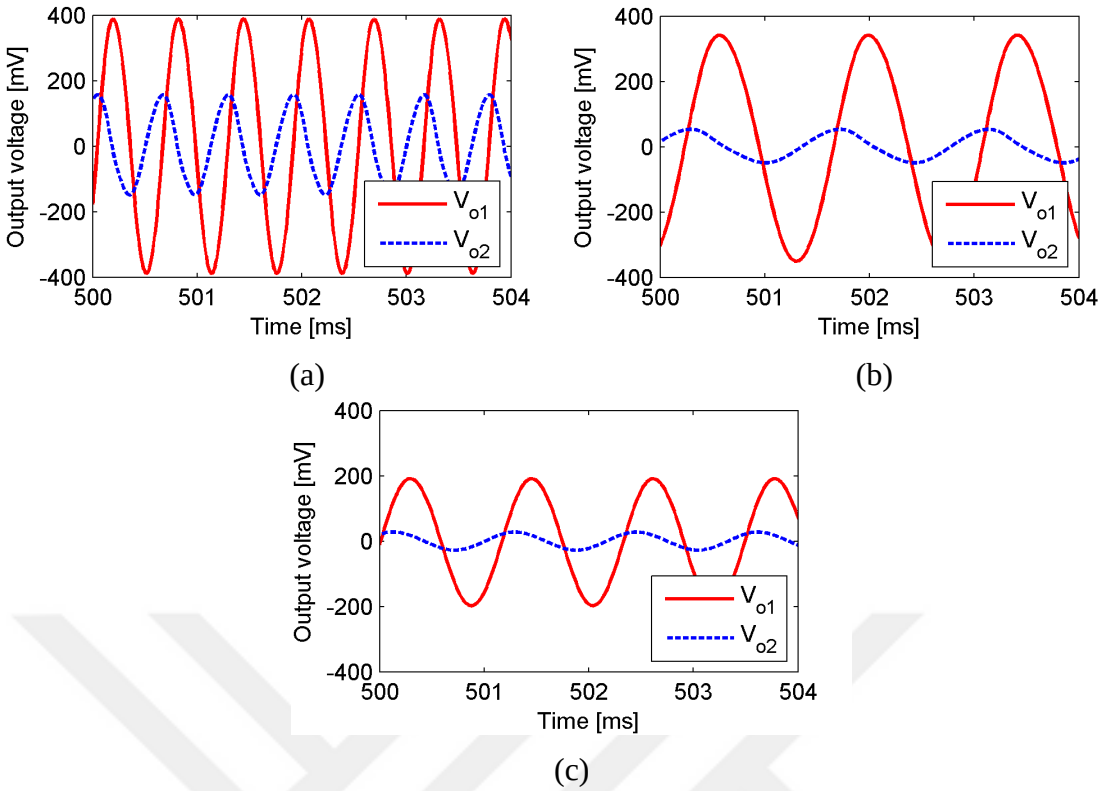


Fig. 7.10: Simulated output waveforms of the proposed voltage-mode oscillator: (a) $\alpha = \beta = 1$, (b) $\alpha = 0.9$, $\beta = 0.6$, (c) $\alpha = \beta = 0.5$

pseudo-capacitance values will be as follows: $C_\alpha \approx 136.3\ \text{nF}\cdot\text{s}^{-0.1}$ ($C_1 = 55$ nF @ f_o) and $C_\beta \approx 3.78\ \mu\text{F}\cdot\text{s}^{-0.4}$ ($C_2 = 100$ nF @ f_o). Also, the resistor R will equal to 1.64 kΩ. Computed component values are given in Tab. 7.3. During simulations, in order to start up the oscillations, the resistor was set 3.4 kΩ and the obtained FO was $f_0 = 0.741$ kHz. The simulated output waveforms are shown in Fig. 7.10(b).

As a last step, a fractional-order oscillator with $\alpha + \beta = 1$ has been investigated. Here, considering again the same values of $g_{m1,2}$, the computed pseudo-capacitances for $\alpha = \beta = 0.5$ were $C_\alpha \approx 5.1\ \mu\text{F}\cdot\text{s}^{-0.5}$ ($C_1 = 55$ nF @ f_o) and $C_\beta \approx 9.2\ \mu\text{F}\cdot\text{s}^{-0.5}$ ($C_2 = 100$ nF @ f_o), which after substituting in (6a) the resulting condition of oscillation was $R = 4.48$ kΩ. Computed component values used in SPICE simulations are also given in Tab 7.3. Fig. 10(c) shows the output responses and simulated FO is equal to $f_0 = 0.861$ kHz. In addition, the simulated frequency spectrum of outputs for each case is given in Fig. 7.11. The total power dissipation of the oscillator in all three cases is found to be 11.5 mW.

As it is evident from the obtained SPICE simulation results, there is a slight deviation in simulated FOs compared to theory. For an instance, considering a non-zero parasitic resistance R_β at output terminal of the first voltage buffer, which appears in series with capacitor C_2 (integer-order case), i.e. $Z_2(s) = R_\beta + 1/sC_2$, the non-ideal FO in in integer-order case becomes $\omega_0 = \left[g_{m2} \Big/ \left\{ C_1 C_2 R \left(g_{m2} R_\beta + 1 \right) \right\} \right]^{0.5}$. Similarly, FOs of both fractional-order cases are also affected by R_β, which is shown in Fig. 7.12.

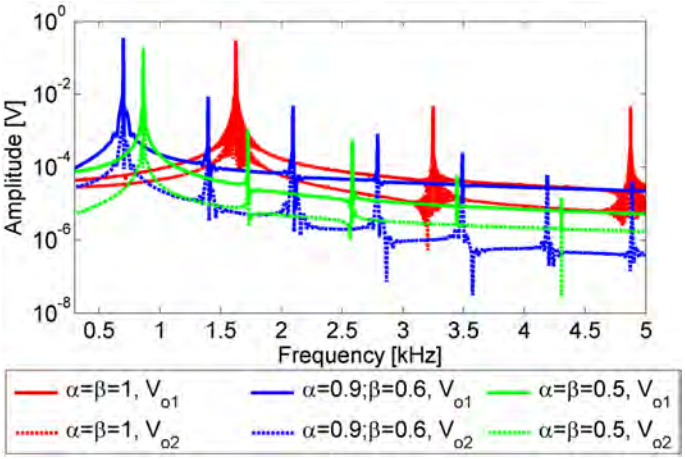


Fig. 7.11: Simulated frequency spectrum of outputs

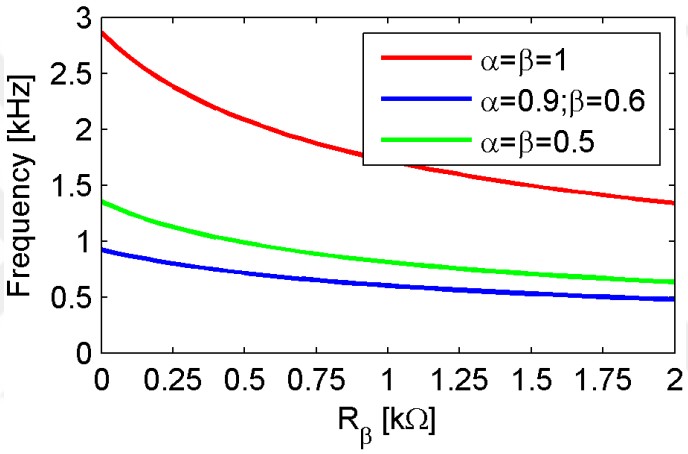


Fig. 7.12: Effect of parasitic resistance R_β on frequency of oscillation

7.3 CMOS-RC Colpitts Oscillator Design Using Floating Fractional-Order Inductance Simulator

The Colpitts oscillator is an LC oscillator, which contains a tuned tank circuit consisting of one inductor and two capacitors; the two capacitors therein are making a capacitive voltage divider.

Here, Colpitts oscillator implemented using two CMOS-based transconductors is shown in Fig. 7.13, wherein the three terminal LC networks are connected in such a manner that between two nodes of the three terminal LC circuits, a transconductor of gain $-g_m$ is connected, whereas the common node of the two capacitors is connected to ground [182]. Replacing the ideal capacitors C_i for $i = \{\alpha, \beta\}$ with FOCs (i.e. C_α and C_β) having impedance $Z_\alpha(s) = 1/(s^\alpha C_\alpha), Z_\beta(s) = 1/(s^\beta C_\beta)$, and FOI ($L_\gamma$) with impedance of $Z_\gamma(s) = 1/(s^\gamma C_\gamma)$, routine circuit analysis provides the following description of this fractional-order system [33]:

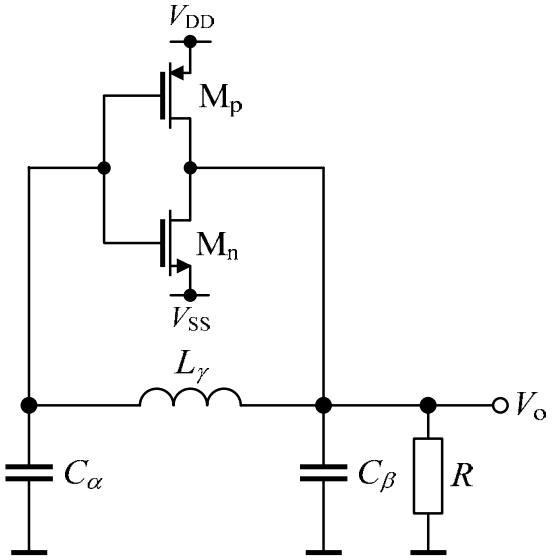


Fig. 7.13: Voltage-mode Colpitts oscillator

$$\begin{pmatrix} d^{\alpha}V_{C_\alpha}/dt^{\alpha} \\ d^{\beta}V_{C_\beta}/dt^{\beta} \\ d^{\gamma}I_{L_\gamma}/dt^{\gamma} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 1/C_\alpha \\ -g_{\mathrm{m}}/C_\beta & -1/RC_\beta & -1/C_\beta \\ -1/L_\gamma & 1/L_\gamma & 0 \end{pmatrix} \begin{pmatrix} V_{C_\alpha} \\ V_{C_\beta} \\ I_{L_\gamma} \end{pmatrix}. \tag{7.14}$$

Hence, the CE from (7.14) has the following general form:

$$\mathrm{CE}: s^{\alpha+\beta+\gamma}RC_\alpha C_\beta L_\gamma + s^{\alpha+\gamma}C_\alpha L_\gamma + s^{\alpha}RC_\alpha + s^{\beta}RC_\beta + Rg_{\mathrm{m}} + 1 = 0. \tag{7.15}$$

An ideal third-order Colpitts oscillator corresponds to setting $\alpha = \beta = \gamma = 1$, which results in the well-known CO: $g_{\mathrm{m}}R = C_1/C_2$ and FO: $\omega = \sqrt{1/(LC_{eff})}$, where $C_{\mathrm{eff}} = C_1C_2/(C_1+C_2)$ and it can be proved from (7.14) and (7.15).

Considering C_1 and C_2 as integer-order capacitors (i.e. $C_\alpha \Rightarrow C_1$ and $C_\beta \Rightarrow C_2$) and inductor L_γ remains as a fractional-order inductor, the general CE in (7.15) turns to:

$$\mathrm{CE}_\gamma: s^{2+\gamma}RC_1C_2L_\gamma + s^{1+\gamma}C_1L_\gamma + sR(C_1+C_2) + Rg_{\mathrm{m}} + 1 = 0, \tag{7.16}$$

and substituting $s = j\omega$ therein, the derived CO_γ and FO_γ are respectively given by:

$$\begin{aligned} \mathrm{CO}_\gamma: R &= -\frac{1+\omega^{1+\gamma}C_1L_\gamma\cos\left[0.5\pi(1+\gamma)\right]}{\omega^{2+\gamma}C_1C_2L_\gamma\cos\left[0.5\pi(2+\gamma)\right]+g_{\mathrm{m}}} = \\ &= -\frac{\omega^{1+\gamma}C_1L_\gamma\sin\left[0.5\pi(1+\gamma)\right]}{\omega^{2+\gamma}C_1C_2L_\gamma\sin\left[0.5\pi(2+\gamma)\right]+\omega(C_1+C_2)}, \end{aligned} \tag{7.17}$$

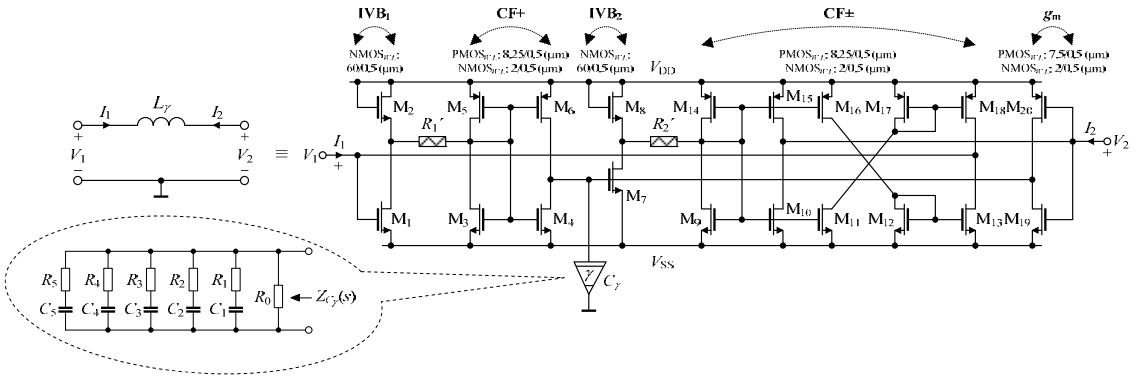


Fig. 7.14: Proposed CMOS fractional-order inductance simulator including RC network emulating fractional-order capacitor

$$\begin{aligned} \mathrm{FO}_\gamma : & \omega^{2+\gamma} C_1^2 C_2 L_\gamma^2 - \omega C_1 C_2 L_\gamma \sin\left(0.5\pi\gamma\right) - \\ & - \omega C_1 L_\gamma \left(C_1 + C_2\right) \cos\left(0.5\pi\gamma\right) + \\ & + \omega^{-1} C_1 L_\gamma g_\mathrm{m} \sin\left(0.5\pi\gamma\right) - \omega^{-\gamma} \left(C_1 + C_2\right) = 0. \end{aligned} \tag{7.18}$$

As it is evident, the proposed oscillator offers independent tuning of the frequency and condition of oscillation.

7.3.1 Proposed CMOS Fractional-Order Inductance Simulator Design

In analog electronics, due to the large silicon area, cost, and lack of electronically tunability, CMOS-based inductance simulators are used [183]. The CMOS implementation of the proposed FOI simulator is shown in Fig. 7.14. It consists from two inverting voltage buffers (IVBs), two unity-gain current followers (CFs), and one simple transconductor. In brief, for example IVB$_1$ assuming that both NMOS work in saturation region, $V_{\mathrm{THN1}} = V_{\mathrm{THN2}}$, $+V_{\mathrm{DD}} = -V_{\mathrm{SS}}$, and process transconductance parameters $k_{\mathrm{N1}} = k_{\mathrm{N2}}$, voltage transfer can be described simply as $V_{\mathrm{out}} = -V_{\mathrm{in}}$. Thus, it behaves as a linear IVB without DC offset. In order to keep the M$_1$ in saturation region the condition $V_{\mathrm{in}} < V_{\mathrm{out}} + V_{\mathrm{THN1}}$ should be satisfied. Note that the M$_2$ always operates in saturation region since its drain and gate terminals are connected. Considering CF± structures used in Fig. 7.14, it can be observed that both were designed by superposition of top PMOS sourcing mirrors and bottom NMOS sinking mirrors. However, from another viewpoint this configuration may be seen as a cascade of two CMOS inverters with the first one having shorted input and output. In general, CF± can be described as $V_{\mathrm{in}} = R_{\mathrm{CF\_in}k} I_{\mathrm{in}}$ and $I_{\mathrm{out}\pm} = \pm I_{\mathrm{in}}$ for $k = \{1, 2\}$. Here, $R_{\mathrm{CF\_in}k}$ denotes intrinsic input resistance, which can be set via supply voltages. Finally, the current-voltage relationship of used transconductor is $I_{\mathrm{out}} = -g_{\mathrm{m}} V_{\mathrm{in}}$. Detailed description of used active building blocks (ABBs) can be find in [180], while transistors main parameters obtained after re-design are listed in Tab. 7.4.

Considering described ABBs, one capacitor, and assuming matching condition $g_{\mathrm{m}} = 1/R_{\mathrm{CF\_in1}}$, while $R_{\mathrm{CF\_in}k} \approx R_k'$, routine circuit analysis yields the following short

Tab. 7.4: Behavior of CMOS Transconductor, IVB, and CF±

Transconductor (g_m)	
Parameter	*Value*
Transconductance gain g_m I_{out}/V_{in} (μA/V)	835
Tracking error ε_{gm} @ g_o = 833 μA/V (–)	–0.002
$f_{-3\,dB}$ @ g_m (GHz)	7.195
DC linearity for V_{in} (V)	±0.535
R_{gm_in} (Ω)	≅ ∞
R_{gm_out} (kΩ) || C_{gm_out} (fF)	64.44 || 6.42
Inverting Voltage Buffer (IVB)	
Parameter	*Value*
Voltage gain V_{out}/V_{in} gain (β_o)	0.972
Tracking error $\varepsilon_{\beta o}$ (–)	0.028
$f_{-3\,dB}$ @ V_{out}/V_{in} (GHz)	17.152
DC linearity V_{out}/V_{in} (V)	$-1 \rightarrow +0.445$
R_{IVB_in} (Ω)	≅ ∞
R_{IVB_out} (Ω)	80.6
Current Follower (CF±)	
Parameter	*Value*
Current gains I_{out+}/I_{in}; I_{out-}/I_{in} (α_{oj})	0.982; 0.947
Tracking errors $\varepsilon_{\alpha oj}$ (–)	0.018; 0.053
$f_{-3\,dB}$ @ I_{out+}/I_{in}; I_{out-}/I_{in} (GHz)	1.138; 0.871
DC linearity I_{out+}/I_{in}; I_{out-}/I_{in} (μA)	±944; ±333
R_{CF_in} (R_k') (kΩ)	1.122
R_{CF_out+} (kΩ) || C_{CF_out+} (fF)	61.71 || 14.75
R_{CF_out-} (kΩ) || C_{CF_out-} (fF)	61.71 || 20.94

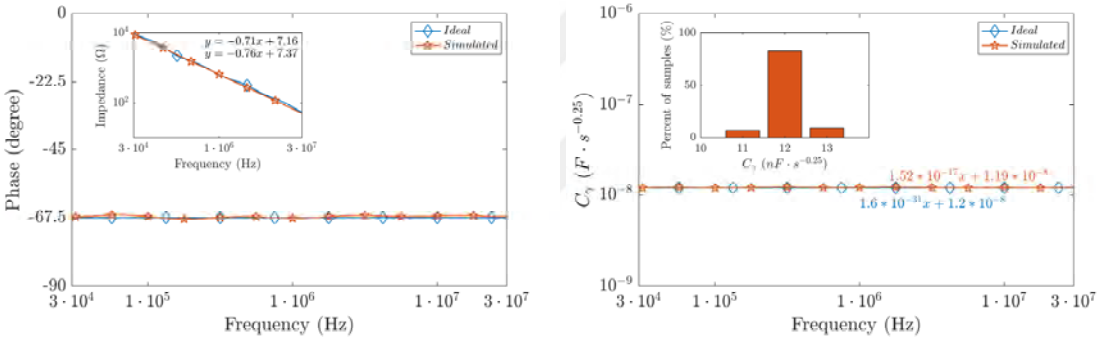
circuit admittance matrix $[Y_{L_\gamma}] = \frac{1}{s^\gamma L_\gamma}\begin{bmatrix} +1 & -1 \\ -1 & +1 \end{bmatrix}$, from which $L_\gamma = R_1'R_2'C_\gamma$. As it can be seen the equivalent inductance value is adjustable by order of the FOC (or phase). The Foster II structure has been used to realize the FOC with a fractional-order of $\gamma = 0.75$. Component values obtained via modified least squares quadratic (MLSQ) method. Parameters of both $C_{0.75}$ and subsequently $L_{0.75}$ emulators are summarized in Tab. 7.5.

7.3.2 Simulation Results

The behavior of the ABBs used in CMOS implementation of the FOI simulator and subsequently in Colpitts oscillator in Figs. 7.13 and 7.14 have been verified by SPICE simulations with DC power supply voltages $+V_{DD} = -V_{SS} = 1$ V. In the design, transistors are modeled by the TSMC 0.18 μm level-7 LO EPI SCN018 CMOS process parameters (V_{THN} = 0.3725 V, μ_N = 259.5304 cm^2/(V·s), V_{THP} = –0.3948 V, μ_P = 109.9762 cm^2/(V·s), T_{OX} = 4.1 nm) [184]. The aspect ratios of transistors in structures and their main parameters obtained with AC and DC analyses are listed in

Tab. 7.5: Parameters of $C_{0.75}$ and $L_{0.75}$ emulators in Fig. 7.14. (Note: # in 30 kHz - 30 MHz; ‡ in 130 kHz - 2.5 MHz ranges)

Component values (kΩ) / (pF)										
R_0	R_1	R_2	R_3	R_4	R_5	C_1	C_2	C_3	C_4	C_5
51.1	3.48	0.261	0.909	13.3	0.01	130	51	82	240	91
Total resistance (kΩ) / capacitance (pF)										
69.06							594			
Spread of resistance / capacitance										
5 110							4.71			
C_γ: Order (–) / phase (degree) / pseudo-capacitance (nF·sec$^{\gamma-1}$)										
0.75 / –67.5 / 12										
C_γ: Phase angle deviation# (degree) / relative error# (%)										
±0.9 / –1.35 → 0.6										
L_γ: Order (–) / phase (degree) / pseudo-inductance (mH·sec$^{\gamma-1}$)										
0.75 / 67.5 / 17.3										
L_γ: Phase angle deviation‡ (degree) / relative error‡ (%)										
±5 / 3.7 → 8.7										



(a) (b)

Fig. 7.15: Ideal and simulated (a) phase and (b) pseudo-capacitance responses of 0.75-order fractional-order capacitor

Tab. 7.4. The equivalent intrinsic input resistance and the transconductance gain value are set $g_m \cong (1/R_k' + 1/R_{IVB\_out}) \cong 835$ µA/V in order to fulfill the required parameter matching.

In order to verify the workability of the proposed Colpitts oscillator employing FOI simulator shown in Fig. 7.14, first of all the phase and pseudo-capacitance response of the FOC with an order $\gamma = 0.75$ and value $C_\gamma = 12$ nF·s$^{-0.25}$ (300 pF @ 407.5 kHz), emulated via 5th-order Foster II *RC* network, which has an admittance in following form: $Y_{C_\gamma} = 1/Z_{C_\gamma} = 1/R_0 + \sum_{k=1}^{5} sC_k/[sR_kC_k + 1]$ and values optimized using MLSQ method, has to be evaluated. Figure 7.15(a) shows that the constant phase zone of the FOC is from 30 kHz to 30 MHz with –67.5°, which is proven by the fitting equations as

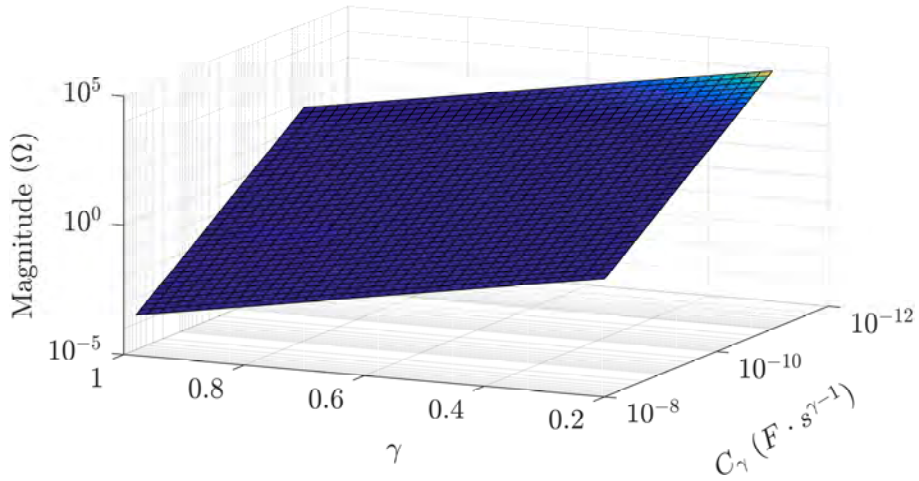


Fig. 7.16: Effect of C_γ vs. γ on FOI magnitude

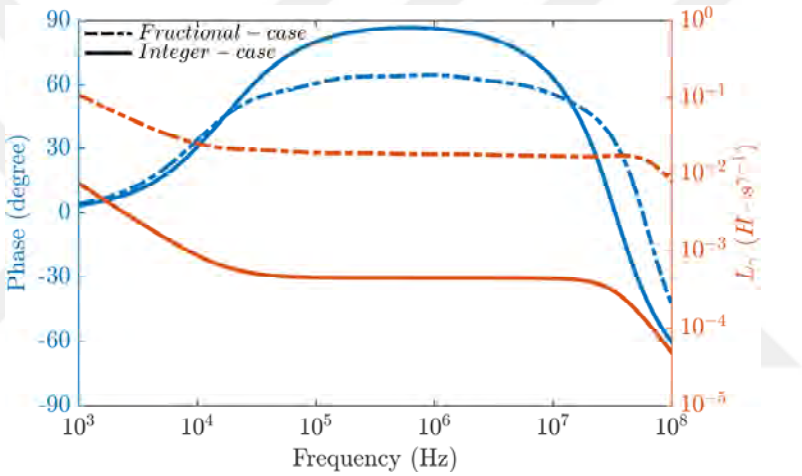


Fig. 7.17: Phase (left) and (pseudo)-inductance (right) responses of proposed 0.75 and integer-order CMOS inductance simulator

an inset of the figure. To estimate the equivalent order γ (or phase), the magnitude data simulated are fitted to the function $\log Z = \gamma \log f + \log(2\pi j)^\gamma C_\gamma$. Similarly, the pseudo-capacitance with stable C_γ is shown in Fig. 7.15(b). Note that the phase angle deviation in given range is only ±0.9 degree, while the corresponding relative pseudo-capacitance error in same range varies from –1.35% to +0.6%. The performance of the proposed FOI simulator shown in Fig. 7.14 was also evaluated. Fig. 7.16 shows the effect of C_γ vs. γ on FOI magnitude. The simulated phase (pseudo)-inductance responses of 0.75 and integer-order inductance simulator are shown in Fig. 7.17. In this case the circuit was simulated with C and C_γ given above, which in fractional-order case theoretically resulted in $L_{\gamma\_theor} = 17.3\ \text{mH}\cdot\text{s}^{-0.25}$ and the simulated one has a value $L_{\gamma\_sim} = 18.4\ \text{mH}\cdot\text{s}^{-0.25}$. Considering ±5 degree deviation in phase, the useful frequency range for $L_{0.75}$ is about 138 kHz up to 2.45 MHz.

Both 2.75^{th} and 3^{rd} order Colpitts oscillator were designed with CMOS transconductance given in Tab. 7.4 and capacitor values were selected as

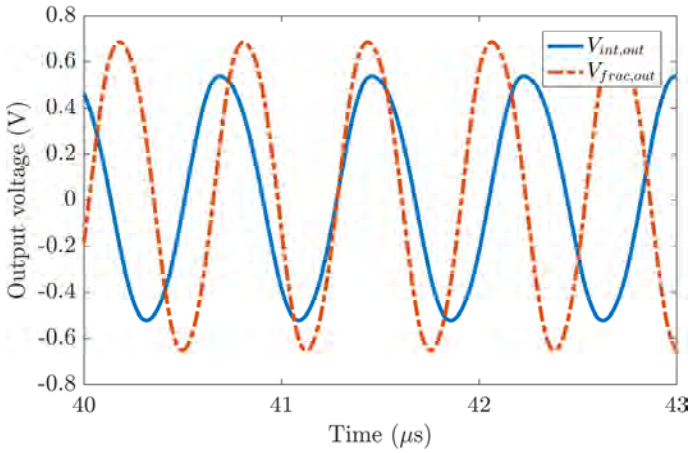
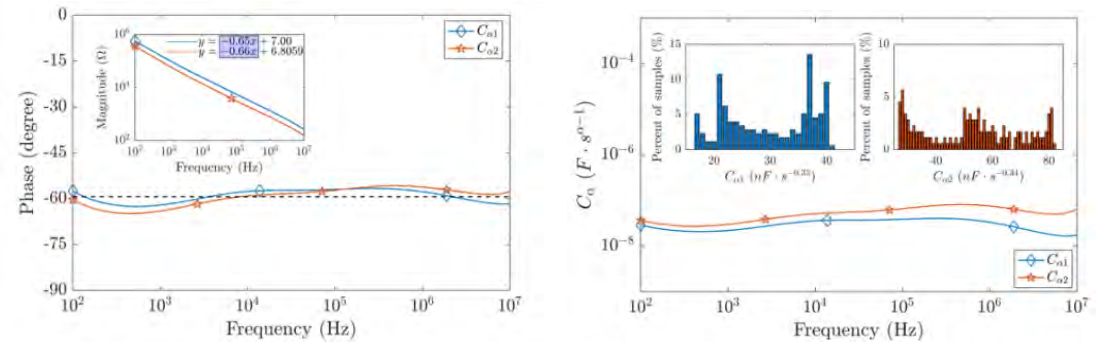


Fig. 7.18: Simulated output voltage waveforms of the proposed 2.75th and 3rd-order Colpitts oscillator

$C_1 = C_2 = 61$ pF. The calculated oscillation start-up condition is $R = 28.13$ kΩ and the FO is $f_{0\_theor\_fract} = 1.3$ MHz, while the simulated CO is $R = 30$ kΩ and FO is 1.58 MHz. On the other hand, the CO is 1.8 kΩ and FO is 1.26 MHz in integer-order case. The steady-state output voltage waveforms of both cases are depicted in Fig. 7.18. For the output the generated peak-to-peak value is 1.34 V and 1.06 V for 2.75th and 3rd-order, respectively, while the total harmonic distortion (THD) at the outputs are about 4.1% and 5.3% for the fractional and integer cases, respectively.

7.4 Fractional- Order Wien Oscillator

A PCB-compatible FOCs using molybdenum disulfide (MoS_2)-ferroelectric polymer composites are first presented in [87]. In this chapter, their application in fractional-order Wien oscillator is shown. The impedance of two fabricated FOCs is analyzed using the Agilent 4994A Precision Impedance Analyzer with the 16048G model test fixture. Figure 7.19(a) plots the phase of the impedance versus frequency and shows that it remains constant at -58.5° and -59.4° with only ±4° phase deviation between 100 Hz and 10 MHz (five decades) for both of the FOCs. The pseudocapacitances of these FOCs, which are extracted from impedance magnitude measurements, are shown in Fig. 7.19(b). Their values at 25 kHz are $C_{\alpha 1} = 37.2$ nF·s$^{-0.35}$ and $C_{\alpha 2} = 55.2$ nF·s$^{-0.34}$.



(a) (b)

Fig. 7.19: (a) Phase and magnitude of the impedance and (b) pseudo-capacitance of the fabricated FOCs

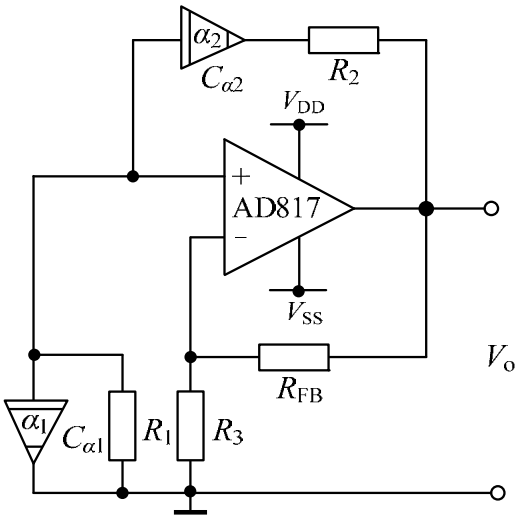
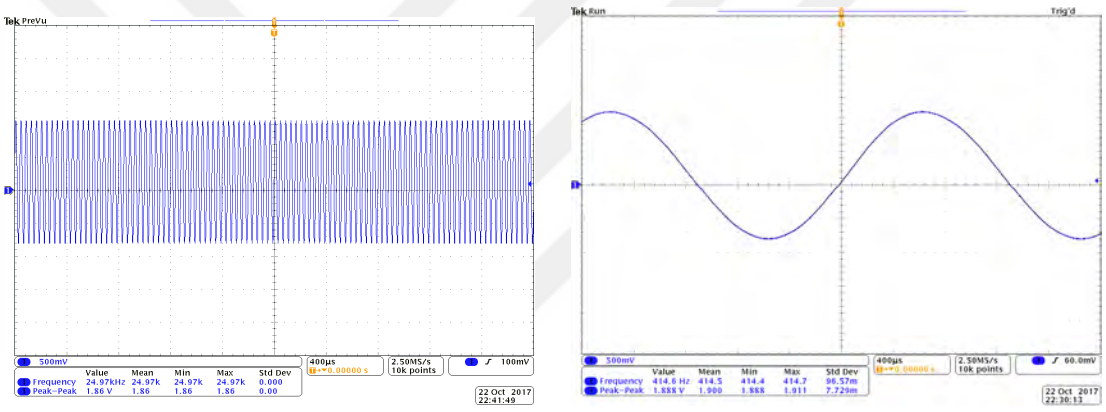


Fig. 7.20: Schematic of fractional-order Wien oscillator



(a) (b)

Fig. 7.21: Measured steady-state output voltage waveform of (a) the fractional-order Wien oscillator and (b) the conventional one as an inset

It should be noted here the constant phase angle can be tuned by using different types of polymers in the composite.

The performance of the fabricated FOCs is demonstrated in a fractional-order Wien oscillator (Fig. 7.20). In the circuit of Fig. 7.20, the passive element values are $R_1 = R_2 = 10\ \text{k}\Omega$, $R_2 = 47\ \text{k}\Omega$, $C_{\alpha 1} = 37.2\ \text{nF}\cdot\text{s}^{-0.35}$, and $C_{\alpha 2} = 55.2\ \text{nF}\cdot\text{s}^{-0.34}$. The measured frequency of oscillation (FO) is 24.87 kHz as seen in Fig. 7.21(a) while the one calculated using the above values is 23.52 kHz [33]. The measurement is repeated after the FOCs are replaced with two conventional capacitors with a capacitance value of 30 nF and 50 nF. For this case the FO is measured to be 0.414 kHz as seen in Fig. 7.21(b). This demonstrates that the fractional-order Wien oscillator has a significantly higher FO that its conventional counterpart. It should also be noted here that the peak-to-peak amplitudes of the output voltage of both oscillators are same and equal to 1.88 V.

7.5 Summary

The integrated analog design of fractional-order oscillator design and experimental verification of FOCs in well-known Wien oscillator are studied in this chapter. Moreover, active FOI emulator using ABBs was proposed. The proposed compact CMOS fractional-order oscillators and active FOI emulator behavior and performance was verified using SPICE simulations. Some numerical studies were done using MATLAB environment. The main motivation of this study by designing fractional-order oscillator was to prove that these types of oscillators offer:

(i) Independent tuning of the frequency and condition of oscillation,

(ii) Higher frequency of oscillation than its integer-order counterpart,

(iii) Requirement for capacitances with reasonable values,

(iv) Possibility for achieving different frequency of oscillation/start-up condition by only changing the order/capacitance values.

The novelties of this chapter are the analog integrated circuit design of compact voltage-mode fractional-order oscillator and real-time application of the solid-state FOC in Wien oscillator. Moreover, compared with the corresponding already introduced fractional-order oscillators, the proposed structures offer the benefit of low transistor count and, therefore, simplicity of its structure. To the best knowledge of the author, the proposed fractional-order Colpitts oscillator is studied for the first time in open literature.

8 CONCLUSIONS

In this chapter the conclusions of the work presented in this thesis are addressed. The main contributions and future work are emphasized. The conclusions are drawn from two perspectives: analog realization of FOEs and their application in analog integrated circuits.

8.1 Thesis Summary

Throughout this thesis, a wide range of problems associated with analog circuit design of fractional-order dynamic systems are covered: passive component optimization of resistive-capacitive and resistive-inductive type FOEs, active realization of FOCs, analog integrated circuit design of fractional-order integrator, robust fractional-order proportional-integral control design, investigation of different materials for ultra-wide band, low phase error FOC, possible low- and high-frequency realization of fractional-order oscillators in analog circuit design, stability study of solid-state FOCs in series-, parallel- and interconnected networks. The major target of this thesis is to develop novel stable and accurate solutions in the form of FOE realization, analog circuit design of fractional-order dynamic systems and their performance evaluation frameworks to significantly improve requirements of analog circuit designs.

When discussing distributed element realization of FOEs and fabrication of FODs in Chapter 2, the need for joint study of precise modelling and characterizing electrical properties of dielectric materials is realized. Several structures have been proposed for FOEs design and studied within fractional-order systems. Highlighting important practical trade-off in Chapter 2, the results from Chapter 3, 4 and 5 indicated significant promise for future research in the area of analog circuit design of fractional-order systems. In particular, in Chapter 2, an optimization of passive component values in RC/RL networks improves the constant phase angle and makes them easily use in experimental verification of fractional-order systems. Extending this idea on precise modelling and then the fabrication of FODs, a new solid-state FOC based on *h*BN-P(VDF-TrFE-CFE) polymer composites is presented in Chapter 5 and analyzed within a frequency range of 100 Hz - 10 MHz and minimum ±2.2°, maximum ±4° phase error.

Whereas there is a natural connection between Chapters 3 and 5, the fractional-order integral design using cascade of BTSs is presented in Chapter 4. The structure benefits from the rational approximation of irrational impedance functions and their zero-pole distributions. An example for the analog integrated circuit design using ABBs of BTSs is shown and studied FOPI$^{\lambda}$ controller. There is still need to investigate proper approximation and structure to build a low cost hardware for industrialization. However, the preliminary results prove the possibility of the idea and are currently sufficient to move on this direction.

While improving the performance and increasing the variability of FOEs and FODs, their stability and accuracy becomes important. This can be simply tested in circuit network connections. Therefore, the series-, parallel- and interconnected identical- and arbitrary-order FOCs are studied mathematically in Chapter 6.

Derived formulas are experimentally verified. I believe that this study might be one of the fundamental topics of electronic circuit lectures in fractional domain in the future.

In Chapter 7, the effect of FOEs on system design equations of fractional-order oscillators is investigated. For that, new design structures for compact voltage-mode fractional-order oscillators are presented. Beside it, the classic oscillators e.g. Colpitts and Wien are studied. Some of early fabricated FOCs are used in application of Wien oscillator. Our analysis confirms that it is possible to reach extremely low- and high-frequency FO by only changing the order without necessity to use high value capacitors or inductors.

The complex research summarized in this thesis results in both theoretical innovations and practical applications. It is expected that the proposed solutions and their future extensions will become of significant importance toward further development of analog implementation of fractional-order systems. Author's previously published papers [185]-[209] will significantly help on this direction. These solutions are primarily intended for, but not limited to, fractional-order integrators, fractional-order differentiators, analog integrated circuit design, nanofabrication, and electronic component producers.

8.2 Future Work

Even though optimum FOE design and accurate solid-state FOC with their applications presented in this thesis constitute an integrated research, there exist many opportunities to extend and every particular component. For instance, optimization of FOEs designed with optimum branch number, minimal passive component do not take into account the order with complex number e.g. "a+*j*b". As such, they may be extended to a complex-order FOE realization.

Due to the increasing progress in modelling and fabrication of FOEs, the direct implementation of fractional-order dynamics has become a noteworthy research topic. However, the investigations are more on about phase ripple minimization and bandwidth extension. Yet, there is no study on controlling pseudocapacitance. This is particularly important in energy storage elements e.g. memory cells, batteries etc.

With the fractional-order integrator design in Chapter 4, we barely show their applications in fractional-order control. This study may continue on realization of the plant and FOPI$^{\lambda}$D$^{\mu}$ controller design.

As the effect of FOEs on system equations of fractional-order oscillators is studied, the further research might be their full integration and implementation together with their experimental verification. Consequently, the proposed approaches in this thesis are important considerations in beyond the future studies of fractional dynamic systems.

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List of Abbreviations

ABB	Analog Building Block
BPADA	Bis (Phthalic Anhydride)
BTS	Bilinear Transfer Segment
CE	Characteristic Equation
CF	Current Followers
CFE	Continued Fraction Expansion
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nanotube
CO	Condition of Oscillation
CPA	Constant Phase Angle
CPZ	Constant Phase Zone
DF	Dissipation Factor
DMF	Dimethylformamide
DFVF	Differential Flipped Voltage Followers
ESR	Equivalent Series Resistance
FDNR	Frequency Dependent Negative Resistors
FO	Frequency of Oscillation
FOC	Fractional-Order Capacitor
FOD	Fractional-Order Device
FOE	Fractional-Order Elements
FOI	Fractional-Order Inductors
FoM	Figure of Merit
$FOPI^{\lambda}$	Fractional-Order Proportional-Integral
$FOPI^{\lambda}D^{\mu}$	Fractional-Order Proportional-Integral-Derivative
GA	Genetic Algorithm
*h*BN	hexagonal-Boron Nitride
IVB	Inverting Voltage Buffer
IPMC	Ionic Polymer Metal Composites
$K_3[Fe(CN)_6]$	Potassium Ferricyanide
$K_4[Fe(CN)_6]$	Potassium Ferrocyanide
LLS	Linear Least Squares
LPF	Low-Pass Filter
MC	Monte Carlo
MIM	Metal-Insulator-Metal
MLSQ	Modified Least Squares Quadratic
MoS_2	Molybdenum diSulfide
MOS	Metal Oxide Semiconductor
mPD	m-Phenylene Diamine
OTA	Operational Transconductance Amplifier

PAD	Phase Angle Deviation
PCB	Printed Circuit Board
PID	Proportional-Integral-Derivative
PMMA	poly-methyl-methacrylate
P(VDF)	Polyevinelidenefluoride
P(VDF-TrFE)	Polyevinelidenefluoride–Trifluoroethylene
P(VDF-TrFE-CFE)	Polyevinelidenefluoride–Trifluoroethylene-Chlorofluoroethylene
$RbAg_4I_5$	Rubidium Silver Ionide
RC-EDP	Resistive-Capacitive Elements with Distributed Parameters
rGO	reduced Graphene Oxide
SMA	Subminiature Version A
TEM	Transmission Electron Microscopy
TF	Transfer Function
THD	Total Harmonic Distortion
XRD	X-Ray Powder Diffraction
VM	Voltage–Mode
ZFs/PVDF	Zinc Flakes/Flexible Polyvinylidene Fluoride

List of Symbols

α	order
A	planar geometry of area, open loop gain
b	friction coefficient of motor
C_α	pseudocapacitance
$C(s)$	controller
d	thickness
$E(s)$	Error signal
ε_0	permittivity of free space
ε_∞	high-frequency permittivity
$\tilde{\varepsilon}(\omega)$	complex permittivity
F	Fitness function
g_m	transconductor
G	conductance
$G(s)$	plant
I^λ	fractional-order integrator
j	complex number
J	an equivalent moment of inertia
K_I	the integration constant
K_P	the proportional constant
K_b	back-emf constant
K_m	a torque constant
L_α	pseudoinductance
$\tilde{M}$	dielectric modulus
n	system order
Q	quality factor
R_a	an armature resistance
$R(s)$	a reference input signal
s	Laplacian operator
$T_\mathrm{d}(s)$	an external disturbance
$U(s)$	control signal
$\tilde{X}(\omega)$	susceptibility
X_C	equivalent series capacitors
X_L	inductive reactance
ω	angular frequency
ω_cg	the gain crossover frequency
$\mathrm{Y}(s)$	admittance

$Z(s)$	impedance
°	degree
%	percent
φ	phase angle
Φ_m	phase margin
$\Gamma(\cdot)$	Gamma function

List of Appendices

A Passive Element Values of FOEs and Their Performance Characteristics [78]

The Optimized Foster-II Network (RC-Type) with GA for FOC Design

Element	Fig. 3.1(a)			Fig. 3.1(c)		
	$\alpha = -0.5$; $C_\alpha = 100\ \text{nF}\cdot\text{s}^{-0.5}$					
	This work	CFE	Oustaloup	This work	CFE	Oustaloup
R_0 (Ω)	979.5 k	438.84 k	3.99 k	910 k	430 k	3.9 k
R_1 (Ω)	42.1 k	4.44 k	4.12 k	36 k	4.3 k	4.3 k
R_2 (Ω)	13.6 k	37.87 k	11.52 k	15 k	39 k	12 k
R_3 (Ω)	2.1 k	94.10 k	28.58 k	330 k	91 k	30 k
R_4 (Ω)	409.8 k	155.28 k	77.49 k	120 k	150 k	75 k
R_5 (Ω)	132.5 k	202 k	272.24 k	2.4 k	200 k	270 k
C_1 (F)	229.3 p	74.04 p	153.90 p	120 p	68 p	150 p
C_2 (F)	70.8 p	87.66 p	346.88 p	390 p	100 p	330 p
C_3 (F)	33.5 p	127 p	852.84 p	10 p	120 p	680 p
C_4 (F)	2.3 n	248.16 p	2.05n	0.47 p	270 p	2.2 n
C_5 (F)	722.5 p	913.85 p	3.69 n	120 p	1 n	3.3 n
Operating frequency range						
100 Hz – 1 MHz						
Total resistance (Ω) / Total capacitance (F)						
	467.7 k / 3.17 n	932.53 k / 1.45 n	397.94 k / 7.09 n	1.41 M / 3.05 n	914.3 k / 1.56 n	395.2 k / 6.66 n
Spread of resistance / capacitance						
	198.75 / 69.79	98.84 / 12.34	68.23 / 23.98	379.17 / 66.67	100 / 14.71	69.23 / 22
Max. phase angle deviation (°) / relative phase error (%)						
	±1.8 / ±4.09	±25 / ±53.23	±25 / ±50.61	±2.4 / ±5.43	±40 / ±79.44	±30 / ±54.5
Monte Carlo analysis: Variation of phase @ 10 kHz (mean / min / max (°))						
	–46.35 / –48 / –44.83	–45.06 / –46.45 / –43.68	–45 / –46.25 / –43.51	–46.74 / –47.7 / –45.61	–44.77 / –46.1 / –43.33	–43.02 / –44.41 / –41.41

Element	Fig. 3.4 (α = –0.67)		Fig. 3.5 (α = –0.5)		
	This work	RA	This work (a)	This work (b)	This work (c)
R_0 (Ω)	10 M	24 k	1 k	330	250
R_1 (Ω)	24 k	10 k	1 k	250	10
R_2 (Ω)	4.7 k	3 k	221	330	100
R_3 (Ω)	110 k	820	221	50	25
R_4 (Ω)	2.4 M	270	250	500	200
R_5 (Ω)	470 k	75	20	221	221
R_6 (Ω)	–	–	1 k	20	330
C_0 (F)	7 p	1 n	0.1 p	4.7 p	1.5 p
C_1 (F)	18 p	10 n	100 p	68 p	2.7 p
C_2 (F)	10 p	4.7 n	68 p	8 p	8 p
C_3 (F)	39 p	3.3 n	12 p	15 p	6 p
C_4 (F)	200 p	1.5 n	12 p	12 p	12 p
C_5 (F)	91 p	0.82 n	22 p	15 p	6.8 p
C_6 (F)	–	–	100 p	7 p	100 p
Operating frequency range					
	100 Hz – 10 MHz		1 MHz – 100 MHz	5 MHz – 500 MHz	50 MHz – 1 GHz
Total resistance (Ω) / Total capacitance (F)					
	13.01 M / 365 p	38.17 k / 21.32 n	3.71 k / 314.1 p	1.7 k / 129.7 p	1.14 k / 137 p
Spread of resistance / capacitance					
	416.67 / 28.57	320 / 12.2	50 / 1000	25 / 14.47	33 / 66.67
Max. phase angle deviation (°) / relative phase error (%) Note: *100 Hz – 5 MHz					
	±2.1* / ±4.04*	±74.7 / ±124.51	±0.87 / ±1.94	±1.82 / ±4.63	±1.94 / ±4.58
Monte Carlo analysis: Variation of phase (mean / min / max (°))					
	–60.08 / –62.93 / –57.39 @30 kHz	–60.29 / –62.13 / –57.78 @30 kHz	–44.98 / –46.67 / –46.23 @30 MHz	–45.54 / –46.84 / –43.89 @60 MHz	–45.24 / –46.88 / –43.88 @400 MHz

The Optimized RL Networks with GA for FOL Design

Element	Fig. 3.8 (This work – Valsa network)			Fig. 3.11 (α = 0.5)			
	α = 0.25 L_α = 8.52 mH·s$^{-0.75}$	α = 0.5 L_α = 834.62 µH·s$^{-0.5}$	α = 0.75 L_α = 896.23 µH·s$^{-0.25}$	Foster-I L_α = 8 mH·s$^{-0.5}$	Foster-II L_α = 1 mH·s$^{-0.5}$	Cauer-I L_α = 4.78 mH·s$^{-0.5}$	Cauer-II L_α = 4.84 mH·s$^{-0.5}$
R_0 (Ω)	1	15	6.80 k	1	16	1	1 k
R_1 (Ω)	1	1	1	18	2.2	5.6	24
R_2 (Ω)	1	10	30 k	6.8	1	13	8.2
R_3 (Ω)	1	1	7.5	120	6.8	33	3
R_4 (Ω)	1	1.2	36	1.8	1	120	470 k
R_5 (Ω)	1	3.9	110	1	1	180 k	1
L_0 (H)	6.80 µ	6.80 µ	7.80 µ	–	–	–	–
L_1 (H)	270 n	6.80 µ	7.80 µ	1.5 µ	820 n	7.8 µ	360 n
L_2 (H)	3.30 µ	220 n	27 n	3.9 µ	3.3 µ	2.7 µ	1.8 µ
L_3 (H)	36 n	6.8 µ	5.60 µ	820 n	270 n	1.2 µ	4.7 µ
L_4 (H)	1.50 µ	1.2 µ	3.90 µ	7.8 µ	7.8 µ	470 n	6.8 µ
L_5 (H)	3.90 µ	470 n	1.50 µ	7.8 µ	7.8 µ	33 n	7.8 µ
	Operating frequency range						
	10 kHz – 10 MHz						
	Total resistance (Ω) / Total inductance (H)						
	6 / 15.81 µ	32.1 / 22.29 µ	36.96 k / 26.63 µ	149 / 21.82 µ	27 / 20 µ	180.17 k / 12.2 µ	471.04 k / 21.46 µ
	Spread of resistance / inductance						
	1 / 188.9	15 / 30.91	30 k / 288.89	120 / 9.51	16 / 2.89	180 k / 236	470 k / 21.67
	Max. phase angle deviation (degree) / relative phase error (%) Note: *12 kHz – 10 MHz						
	±1.84* / ±8.16*	±1.66 / ±3.68	±1.55 / ±2.29	±1.9 / ±4.22	±2.44 / ±4.26	±20.04 / ±44.54	±3.91 / ±8.69
	Monte Carlo analysis: Variation of phase (mean / min / max (°))						
	21.45 / 20.58 / 22.37 @300 kHz	45.2 / 43.79 / 46.71 @3 MHz	67.26 / 64.55 / 69.4 @300 kHz	45.16 / 43.99 / 46.42 @100 kHz	45.7 / 44.78 / 46.92 @100 kHz	44.81 / 42.47 / 46.97 @300 kHz	45.53 / 42.97 / 47.73 @300 kHz

B Matlab Code for Calculation of *n* FOCs Connections [85]

%%%

% MATLAB code for calculating the equivalent impedance of *n* FoCs and plotting the magnitude and phase responses
% Copyright (c) 2018, A. Kartci, A. Agambayev, N. Herencsar, and K. N. Salama
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% All rights reserved.
% Feel free to use/modify these codes as you see fit. Any publications codes, papers, technical reports, etc.) in which our codes (in their original or a modified format) have been used should cite the original paper.
% Related Publications:
% [1] A. Kartci, A. Agambayev, N. Herencsar, and K. N. Salama, "Series-, Parallel-, and Inter-Connection of Solid-State Arbitrary Fractional-Order Capacitors: Theoretical Study and Experimental Verification," IEEE Access, vol. 6, pp. 10933-10943, 2018.
% [2] A. Kartci, A. Agambayev, N. Herencsar, and K. N. Salama, "Analysis and Verification of Identical-Order Mixed-Matrix Fractional-Order Capacitor Networks," In Proc. of the 2018 14th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), Prague, Czech Republic, 2018, pp. 277-280

%%%.

```
syms s f z z1

% Set the order and fractional-order capacitance value
order = [0.69 0.92 0.62];
FOC = [5.52e-9 47.52e-12 24.74e-9];

% Calculating the equivalent impedance
for n=1:length(order)
 Z(n) = 1/((s^order(n))*FOC(n));
 pretty(Z(n));

% Equivalent impedance of series-connection
 Zstot = sum(Z(1:n));
 Y(n) = ((s^order(n))*FOC(n));
 pretty(Y(n));

% Equivalent impedance of parallel-connection
 Zptot = sum(Y(1:n))
 Zptot = 1/Zptot;
end

% Plotting the results for series-connected FOCs
NUM=eval(Zstot);
z=[z; (solve(NUM))];
```

```
zz = z/(2*pi);
f =logspace(log10(1e5),log10(1e8),100);
l = size(f);
for n=1:1:l(2)
module(n)=(abs(subs(NUM,s,j*2*pi*f(n))));
end
for n=1:1:l(2)
phase(n)=(angle(subs(NUM,s,j*2*pi*f(n))))*180/pi;
end
figure (1);
subplot(2,1,1)
loglog(f,module,'-b','LineWidth',2)
hold on;
xlabel('f (Hz)','FontSize',10)
ylabel('Zc (ohm)','FontSize',10)
subplot(2,1,2)
semilogx(f,phase,'-b','LineWidth',2)
hold on;
xlabel('f (Hz)','FontSize',10)
ylabel('arg (deg)','FontSize',10)

% Plotting the results for parallel-connected FOCs
NUM1=eval(Zptot);
z1=[z1; (solve(NUM1))];
zz1 = z1/(2*pi);
f =logspace(log10(1e5),log10(1e8),100);
l = size(f);
for n=1:1:l(2)
module1(n)=(abs(subs(NUM1,s,j*2*pi*f(n))));
end
for n=1:1:l(2)
phase1(n)=(angle(subs(NUM1,s,j*2*pi*f(n))))*180/pi;
end
figure (1);
subplot(2,1,1)
loglog(f,module1,'-.r','LineWidth',2)
hold on;
xlabel('f (Hz)','FontSize',10)
ylabel('Zc (ohm)','FontSize',10)
subplot(2,1,2)
semilogx(f,phase1, '-.r','LineWidth',2)
hold off;
xlabel('f (Hz)','FontSize',10)
ylabel('arg (deg)','FontSize',10)
```

Aslihan Kartci

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PROFILE

- Researcher on analog integrated circuit design of fractional-order circuits
- Experienced in modelling and fabrication of fractional-order elements
- Author and co-author of 13 journal, 32 conference papers
- Multidisciplinary international experience as R&D engineer, lecturer, and researcher

QUALIFICATION

Position

2016 – present:	*Research Assistant* – Dept. of Telecommunications, Brno University of Technology
2017 – 2018:	*Teaching Assistant* – Dept. of Radio Electronics, Brno University of Technology

Education

2016 – till now	*Ph.D.* – Brno University of Technology (specialization: Electronics and Communication)
2013 – 2015	*M.Sc.* – Yildiz Technical University, Turkey (specialization: Electronics and Communication)

PROFESSIONAL ACTIVITIES

Research Topics of Interest	Fractional-order components & systems; analog integrated circuits with modern active elements, and their applications as filters and oscillators, general element simulator, numerical methods for analysis of electronic networks, computer-aided methods for simulation of electronic circuits.

Selected Internships & Trainings

16/01/ – 18/05/2018:	Freemover Internship at the Sensors Laboratory, King Abdullah University of Science and Technology (KAUST), Thuwal, Saudi Arabia - Supervisor: Prof. Khaled Nabil Salama
24/02/ – 03/03/2018:	COST Action CA15225 "Short Term Scientific Missions (STSM)", University of Sharjah, Emirates - Visited Professor: Prof. Ahmed Elwakil
05 – 08/09/2017:	COST Action CA15225 "Training School on Fractional Order Controllers: From Theory to Application", University of Catania, Italy
05 – 17/03/2017:	COST Action CA15225 "Short Term Scientific Missions (STSM)", University of Patras, Greece - Visited Professor: Prof. Costas Psychalinos
24 – 26/11/2016:	COST Action CA15225 "COST/IEEE-CASS Seasonal Training School in Fractional-Order Systems", Brno, Czech Republic
10/01/ – 10/06/2015:	ERASMUS Exchange Student, Brno University of Technology, Czech Republic
27/06/ – 30/09/2011:	ERASMUS Training, Brno University of Technology, Czech Republic
09/2010 – 02/2011:	ERASMUS Exchange Student, Brno University of Technology, Czech Republic

Memberships / Volunteering

Since 2019	IEEE Czechoslovakia Section Student Activities Chair
Since 2017:	IEEE Czechoslovakia Section SP/CAS/COM Joint Chapter Student Chair
2016 – 2018:	IEEE Czechoslovakia Section Brno University of Technology Student Branch Vice-President
Since 2015:	IEEE Circuits and Systems Society (CASS) Member
Since 2015:	Student Member of Institute of Electrical and Electronic Engineers (IEEE)

Selected Editorships / Technical Program Committee (TPC) Memberships

2017:	*Technical Program Committee Member* of 2017 24th IEEE Int. Conference on Electronics, Circuits and Systems (ICECS), Batumi, Georgia, Organized by IEEE CASS - http://icecs2017.org/
2016:	*Organizer* of COST/IEEE-CASS Seasonal Training School in Fractional-Order Systems, Brno, Czech Republic, Organized by IEEE CASS, COST Association, and IEEE Czechoslovakia Section - http://fractal.utko.feec.vutbr.cz/
Since 2016:	*Congress Publicity Chair* of Int. Congress on Ultra-Modern Telecommunications and Control Systems (ICUMT) - https://www.icumt.info
Since 2016:	*Publicity and Social Media Chair* of Int. Conference on Telecommunications and Signal Processing (TSP), Technically co-sponsored by IEEE R8 & IEEE Czechoslovakia Section - http://tsp.vutbr.cz/
Since 2015:	Number of *Peer-Reviewed SCI-E Journal & Conference Proceedings Paper Reviews*: 50

SELECTED RESEARCH RESULTS AND GRANT PROJECTS

Developed Integrated Circuit

2018:	N. Herencsar, R. Sotner, V. Kledrowetz, A. Kartci, J. Jerabek, and J. Koton, *UDE - Universal Differencing Element* (in EUROPRACTICE IC Service).

Participation In Grant Projects

Projects supported by the MŠMT INTER-EXCELLENCE - INTER-COST:

2018 – 2020:	LTC18022: Analogue Fractional Systems, Their Synthesis and Analysis. Holder: doc. Ing. Jan Jeřábek, Ph.D.

Projects supported by the Czech Science Foundation (GA CR):

2019 – 2021:	GA1924585S: Synthesis of Reliable Electrical Phantoms Describing Fractional Impedance Behavior of Real-World Systems. Holder: doc. Ing. Jaroslav Koton, Ph.D.
2016 – 2018:	GJ16-11460Y: Active Devices with Differencing Terminals for Novel Single-Ended and Pseudo-Differential Function Block Design. Holder: doc. Ing. Norbert Herencsár, Ph.D.
2015 – 2017:	GA15-18288S: Research of Signal Integrity at High-Speed Interconnects. Holder: prof. Ing. Lubomír Brančík, CSc.

FIVE SELECTED SIGNIFICANT PUBLICATIONS (Last 3 years)

[1] A. Kartci, A. Agambayev, M. Farhat, N. Herencsar, L. Brančík, H. Bagci, and K. N. Salama, "Synthesis and Optimization of Fractional-Order Elements Using a Genetic Algorithm," *IEEE Access*, 2019, accepted. (IF = 3.557)

[2] R. Sotner, J. Jerabek, A. Kartci, O. Domansky, N. Herencsar, V. Kledrowetz, B. B. Alagoz, and C. Yeroglu, "Electronically Reconfigurable Two-Path Fractional-Order PI/D Controller Employing Constant Phase Blocks Based on Bilinear Segments Using CMOS Modified Current Differencing Unit," *Microelectronics Journal*, vol. 86, pp. 114–129, 2019. (IF = 1.322)

[3] A. Kartci, A. Agambayev, N. Herencsar, and K. N. Salama, "Series-, Parallel-, and Inter-Connection of Solid-State Arbitrary Fractional-Order Capacitors: Theoretical Study and Experimental Verification," *IEEE Access*, vol. 6, pp. 10933–10943, 2018. (IF = 3.244)

[4] N. Al-Zubaidi R-Smith, A. Kartci, and L. Brančík, "Application of Numerical Inverse Laplace Transform Methods for Simulation of Distributed Systems with Fractional-Order Elements," *Journal of Circuits Systems and Computers*, vol. 27, no. 11, pp. 1–25, 2018. (IF = 0.481)

[5] A. Kartci, R. Sotner, J. Jerabek, N. Herencsar, and J. Petržela, "Phase Shift Keying Modulator Design Employing Electronically Controllable All-Pass Sections," *Analog Integrated Circuits and Signal Processing*, vol. 89, no. 3, pp. 781–800, 2016. (IF = 0.623)

OVERALL RESEARCH RESULTS (According to Web of Science)

h-index:	8
No. of papers published in SCI-E journals / conferences:	10 / 28
Sum of times cited / without self-citations:	211 / 167
Average citations per item:	5.55
Citing articles / without self-citations:	133 / 102

List of Publications

Publications in journals

Related to the research presented in this thesis

1. A. Kartci, et al. “Solid-State Fractional-Order Capacitor Design using *h*BN-Polymer Composites”, under preparation.
2. A. Kartci, A. Agambayev, M. Farhat, N. Herencsar, L. Brančík, H. Bagci, and K. N. Salama, “Synthesis and Optimization of Fractional-Order Elements Using a Genetic Algorithm,” *IEEE Access*, 2019, accepted..
3. J. Dvorak, D. Kubanek, H. Herencsar, A. Kartci, P. Bertsias, “Electronically Adjustable Emulator of the Fractional-Order Capacitor,” *Elektronika Ir Elektrotechnika*, 2019, accepted.
4. R. Sotner, J. Jerabek, A. Kartci, O. Domansky, N. Herencsar, V. Kledrowetz, B. B. Alagoz, and C. Yeroglu, “Electronically Reconfigurable Two-Path Fractional-Order PI/D Controller Employing Constant Phase Blocks Based on Bilinear Segments Using CMOS Modified Current Differencing Unit,” *Microelectronics Journal*, 2019.
5. G. Tsirimokou, A. Kartci, J. Koton, N. Herencsar, and C. Psychalinos, “Comparative Study of Discrete Component Realizations of Fractional-Order Capacitor and Inductor Active Emulators,” *Journal of Circuits Systems and Computers*, vol. 27, no. 11, pp. 1850170-1–1850170-26, 2018.
6. N. Al-Zubaidi R-Smith, A. Kartci, and L. Brančík, “Application of Numerical Inverse Laplace Transform Methods for Simulation of Distributed Systems with Fractional-Order Elements,” *Journal of Circuits Systems and Computers*, vol. 27, no. 11, pp. 1–25, 2018.
7. A. Kartci, A. Agambayev, N. Herencsar, and K. N. Salama, “Series-, Parallel-, and Inter-Connection of Solid-State Arbitrary Fractional-Order Capacitors: Theoretical Study and experimental Verification,” *IEEE Access*, vol. 6, pp. 10933–10943, 2018.

Additional others

8. R. Sotner, N. Herencsar, J. Jerabek, A. Kartci, J. Koton, and T. Dostal, “Pseudo-Differential Filter Design Using Novel Adjustable Floating Inductance Simulator with Electronically Controllable Current Conveyors,” *Elektronika Ir Elektrotechnika*, vol. 23, no. 2, pp. 31–35, 2017.
9. A. Kartci, R. Sotner, J. Jerabek, N. Herencsar, and J. Petrzela, “Phase Shift Keying Modulator Design Employing Electronically Controllable All-Pass Sections,” *Analog Integrated Circuits and Signal Processing*, vol. 89, no. 3, pp. 781–800, 2016.
10. R. Sotner, N. Herencsar, J. Jerabek, R. Prokop, A. Kartci, T. Dostal, and K. Vrba, “Z-Copy Controlled-Gain Voltage Differencing Current Conveyor: Advanced Possibilities in Direct Electronic Control of First- Order Filter,” *Elektronika Ir Elektrotechnika*, vol. 20, no. 6, pp. 77–83, 2014.

11. R. Sotner, N. Herencsar, J. Jerabek, R. Dvorak, A. Kartci, T. Dostál, and K. Vrba, "New Double Current Controlled CFA (DCC−CFA) Based Voltage–Mode Oscillator with Independent Electronic Control of Oscillation Condition and Frequency," *Journal of Electrical Engineering*, vol. 64, no. 2, pp. 65–75, 2013.
12. R. Sotner, A. Lahiri, A. Kartci, N. Herencsar, J. Jerabek, and K. Vrba, "Design of Novel Precise Quadrature Oscillators Employing ECCIIs with Electronic Control," *Advances in Electrical and Computer Engineering*, vol. 13, no. 2, pp. 65–72, 2013.
13. R. Sotner, A. Kartci, J. Jerabek, N. Herencsar, T. Dostal, and K. Vrba, "An Additional Approach to Model Current Followers and Amplifiers with Electronically Controllable Parameters from Commercially Available ICs," *Measurement Science Review*, vol. 12, no. 6, pp. 255–265, 2012.

Publications in conference proceedings

Related to the research presented in this thesis

1. A. Kartci, N. Herencsar, O. Cicekoglu, and B. Metin, "Synthesis and Design of Floating Inductance Simulators at VHF-Band Using MOS-Only Approach," *In Proceedings of the 62nd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Dallas, Texas, 2019, accepted.
2. N. Herencsar, A. Kartci, R. Sotner, J. Koton, B. B. Alagoz, and C. Yeroglu, "Analogue Implementation of a Fractional-Order PI^{λ} Controller for DC Motor Speed Control," *In Proceedings of the 28th International Symposium on Industrial Electronics (ISIE)*, Vancouver, Canada, 2019, accepted.
3. N. Herencsar, A. Kartci, H. A. Yildiz, R. Sotner, J. Dvorak, D. Kubanek, J. Jerabek, and J. Koton, "Comparative Study of Op-Amp-based Integrators Suitable for Fractional-Order Controller Design," *In Proceedings of the 42nd International Conference on Telecommunications and Signal Processing (TSP)*, Budapest, Hungary, 2019, accepted.
4. R. Sotner, J. Jerabek, O. Domansky, N. Herencsar, A. Kartci, and J. Dvořák, "Practical Design of Fractional-Order Oscillator Employing Simple Resonator and Negative Resistor," *In Proceedings of the 10th International Congress on Ultra Modern Telecommunications and Control Systems and Workshops (ICUMT)*, Moscow, Russia, pp. 1–4, 2018.
5. N. Herencsar, A. Kartci, E. Tlelo-Cuautle, B. Metin, and O. Cicekoglu, "All-Pass Time Delay Circuit Magnitude Response Optimization Using Fractional-Order Capacitor," *In Proceedings of the 61st IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Windsor, Canada, pp. 129–132, 2018.
6. A. Kartci, N. Herencsar, L. Brančík, and K. N. Salama, "CMOS-RC Colpitts Oscillator Design Using Floating Fractional-Order Inductance Simulator," *In Proceedings of the 61st IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Windsor, Canada, pp. 905–908, 2018.
7. A. Kartci, A. Agambayev, A. H. Hassan, H. Bagci, and K. N. Salama, "Experimental Verification of a Fractional-Order Wien Oscillator Built Using Solid-State Capacitors," *In Proceedings of the 61st IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Windsor, Canada, pp. 544–545,

2018.

8. A. Kartci, A. Agambayev, N. Herencsar, and K. N. Salama, “Analysis and Verification of Identical-Order Mixed-Matrix Fractional-Order Capacitor Networks,” *In Proceedings of the 14th Conference on PhD Research in Microelectronics and Electronics (PRIME)*, Prague, Czech Republic, pp. 277–280, 2018.
9. A. Agambayev, A. Kartci, A. H. Hassan, N. Herencsar, H. Bagci, and K. N. Salama, “Fractional-Order Hartley Oscillator,” *In Proceedings of the 14th Conference on PhD Research in Microelectronics and Electronics (PRIME)*, Prague, Czech Republic, pp. 45–48, 2018.
10. N. Herencsar, R. Sotner, A. Kartci, and K. Vrba, “A Novel Pseudo-Differential Integer/Fractional-Order Voltage-Mode All-Pass Filter,” *In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, pp. 1–5, 2018.
11. J. Dvorak, Z. Polesakova, J. Jerabek, L. Langhammer, A. Kartci, and J. Koton, “Non-Integer-Order Low-Pass Filter with Electronically Controllable Parameters,” *In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, pp. 1–5, 2018.
12. A. Kartci, N. Herencsar, J. Koton, and C. Psychalinos, “Compact MOS-RC Voltage-Mode Fractional-Order Oscillator Design,” *In Proceedings of the 2017 23 European Conference on Circuit Theory and Design (ECCTD)*, Catania, Italy, pp. 1–4, 2017.
13. N. Herencsar, A. Kartci, J. Koton, G. Tsirimokou, and C. Psychalinos, “Voltage Gain-Controlled Third-Generation Current Conveyor and its All-Pass Filter Verification,” *In Proceedings of the 23 European Conference on Circuit Theory and Design (ECCTD)*, Catania, Italy, pp. 1–4, 2017.
14. A. Kartci, N. Herencsar, J. Koton, L. Brančík, and K. Vrba, G. Tsirimokou, and C. Psychalinos, “Fractional-Order Oscillator Design Using Unity-Gain Voltage Buffers and OTAs,” *In Proceedings of the IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Boston, USA, pp. 555–558, 2017.
15. N. Al-Zubaidi R-Smith, A. Kartci, and L. Brančík, “Fractional-Order Lossy Transmission Line with Skin Effect Using NILT Method,” *In Proceedings of the 40th International Conference on Telecommunications and Signal Processing (TSP)*, Barcelona, Spain, pp. 730–734, 2017.
16. G. Tsirimokou, A. Kartci, J. Koton, N. Herencsar, and C. Psychalinos, “Comparative Study of Fractional- Order Differentiators and Integrators,” *In Proceedings of the 40th International Conference on Telecommunications and Signal Processing (TSP)*, Barcelona, Spain, pp. 714–717, 2017.
17. A. Kartci and L. Brančík, “CFOA-Based Fractional-Order Oscillator Design and Analysis with NILT Method,” *In Proceedings of the 27th International Conference Radioelektronika*, Brno, Czech Republic, pp. 1–4, 2017.

Additional others

18. R. Sotner, N. Herencsar, V. Kledrowetz, A. Kartci, and J. Jerabek, “New Low-Voltage CMOS Differential Difference Amplifier (DDA) and an Application Example,” *In Proceedings of the 61st IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Windsor, Canada, pp. 133–136., 2018.
19. L. Brančík, N. Al-Zubaidi R-Smith, and A. Kartci, “Numerical Simulation of Nonuniform Multiconductor Transmission Lines with HF Losses in Matlab,” *In Proceedings of the 28th International Conference Radioelektronika*, Prague, Czech Republic, pp. 1–5, 2018.
20. H. A. Yildiz, N. Herencsar, and A. Kartci, “A New Low Voltage Operational Transresistance Amplifier and Its Applications in Analog Circuit Design,” In *Proceedings of the 10th International Conference on Electrical and Electronics Engineering (ELECO)*, Bursa, Turkey, pp. 1238–1241, 2017.
21. N. Herencsar, and A. Kartci, “Resistorless Electronically Tunable Grounded Inductance Simulator Design,” *In Proceedings of the 40th International Conference on Telecommunications and Signal Processing (TSP)*, Barcelona, Spain, pp. 279–282, 2017.
22. L. Brančík, A. Kartci, and N. Al-Zubaidi R-Smith, “Matlab simulation of transmission lines with skin effect via fractional telegraph equations and NILT,” *In Proceedings of the 27th EAEEIE Annual Conference*, Grenoble, France, pp. 1-5, 2017.
23. R. Sotner, J. Jerabek, N. Herencsar, J. Petrzela, A. Kartci, and T. Dostal, “Discussion on Two Solutions of Inductance Simulators Using Single Controlled Gain Voltage, Differencing Current Conveyor and the most Important Parasitic Effects,” *In Proceedings of the 26th International Conference Radioelektronika*, Košice, Slovakia, pp. 162–167, 2016.
24. J. Jerabek, R. Sotner, R. Prokop, V. Kledrowetz, A. Kartci, and U. E. Ayten, “Inductance Simulator Based on Dual Controlled CMOS Voltage Differencing Current Conveyor,” *In Proceedings of the IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Abu Dhabi, United Arab Emirates, pp. 593–596, 2016.
25. A. Kartci, N. Herencsar, K. Vrba, and S. Minaei, “Novel Grounded Capacitor-Based Resistorless Tunable Floating/Grounded Inductance Simulator,” *In Proceedings of the IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Abu Dhabi, United Arab Emirates, pp. 747–750, 2016.
26. J. Jerabek, R. Sotner, N. Herencsar, and A. Kartci, “Importance of Amplitude Stability and Spectral Purity of Produced Signals in a Quadrature Oscillator,” *In Proceedings of the IEEE 16th International Conference on Computer as a Tool (EUROCON)*. Salamanca, Spain, pp. 1–5, 2015.
27. A. Kartci, U. E. Ayten, N. Herencsar, R. Sotner, and K. Vrba, “Floating Capacitance Multiplier Simulator For Grounded RC Colpitts Oscillator Design,” *In Proceedings of the 20th International Conference on Applied Electronics (AE)*, Pilsen, Czech Republic, pp. 93–96, 2015.
28. A. Kartci, U. E. Ayten, N. Herencsar, R. Sotner, J. Jerabek, and K. Vrba, “Application Possibilities of VDCC In General Floating Element Simulator

Circuit," *In Proceedings of the 22nd European Conference on Circuit Theory and Design (ECCTD)*, Trondheim, Norway, pp. 1–4, 2015.

29. R. Sotner, J. Jerabek, A. Kartci, N. Herencsar, R. Prokop, J. Petrzela, and K. Vrba, "Behavioral Models of Current Conveyor of Second Generation with Advanced Controllable Inter-Terminal Relations," *In Proceedings of the 38th International Conference on Telecommunications and Signal Processing (TSP)*, Prague, Czech Republic, pp. 360–365, 2015.
30. J. Jerabek, R. Sotner, A. Kartci, N. Herencsar, T. Dostal, and K. Vrba, "Two Behavioral Models of the Electronically Controlled Generalized Current Conveyor of the Second Generation," *In Proceedings of the 38th International Conference on Telecommunications and Signal Processing (TSP)*, Prague, Czech Republic, pp. 349–353, 2015.
31. R. Sotner, J. Jerabek, J. Petrzela, R. Prokop, K. Vrba, A. Kartci, and T. Dostal, "Quadrature Oscillator Solution Suitable with Arbitrary and Electronically Adjustable Phase Shift," *In Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, Portugal, pp. 3056–3059, 2015.
32. A. Kartci, U. E. Ayten, R. Sotner, and R. Arslanalp, "Elektronik Olarak Ayarlanabilen VDCC Tabanli Yüzen Kapasite Carpma Devresi," *In Proceedings of the IEEE 23. Sinyal İşleme ve İletişim Uygulamaları Kurultayı (SIU)*, Malatya, Turkiye, pp. 2369–2372, 2015.
33. Z. G. Çam, A. Kartci, and T. Yildirim, "Çok Katmanlı Algılayıcı Ağının Eğitim Parametrelerinin Yapay Arı Kolonisi ve Genetik Algoritma ile Optimizasyonu," *In Proceedings of Akıllı Sistemlerde Yenilikler ve Uygulamaları (ASYU) Sempozyumu*, Izmir, Turkey, pp. 1–4, 2014.