A BIAS CONFIGURABLE, SWITCHABLE NOVEL LNA DESIGN in 0.15um GaAs pHEMT TECHNOLOGY ESPECIALLY FOR WI-FI 6 APPLICATIONS

by

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ABSTRACT

A BIAS CONFIGURABLE, SWITCHABLE NOVEL LNA DESIGN in 0.15um GaAs pHEMT TECHNOLOGY ESPECIALLY FOR WI-FI 6 APPLICATIONS

This master thesis study introduces the design and fabrication of a 0.15 um GaAs pHEMT technology based bias configurable switchable low noise amplifier design for Wi-Fi 6 applications. The proposed design has three frequency cases which are single 2.4 GHz, single 5.8 GHz and concurrent dual band applications. Switching is provided by two switch transistors on the feedback paths. The switching voltage is bias configurable which means there is no need for additional voltage supply for controlling the state of the switching transistors. The designed low noise amplifier chip is fully integrated, no external components are required for the matching. The EM simulation results for the proposed design give the gain of 17.33 dB, noise figure of 2.23 dB and P1dB of 8.32 dBm for 2.4 GHz frequency band. Similarly, the EM simulation results for the 5.8 GHz frequency band, the gain is 18.44 dB, the noise figure is 1.5 dB and P1dB is equal to 3.25 dBm. Lastly, the concurrent dual band operation which contains the 2.4 GHz and 5.8 GHz frequency operation simultaneously, the gain is 17.34 dB and 15.79 dB, the noise figure is 2.23 dB and 1.62 dB, P1dB is 7.77 dBm and 5.34 dBm for 2.4 GHz and 5.8 GHz, respectively. The power consumption of the designed low noise amplifier chip is 216 mW with 3.3 V single voltage supply. The design also involves the techniques of current reuse, self-biasing, inductive degeneration to optimize the power consumption, area saving and performance enhancements. The dimensions of the designed chip are 3.4x1.5 mm^2 including all input and output pads. All simulations and circuit analyses are performed at the AWR design environment by WIN-PL1512 process design kit. To the best of the author's knowledge, there is no other low noise amplifier topology found in literature which combines two different single frequency applications with concurrent dual band condition.

ÖZET

WI-FI 6 UYGULAMALARI İÇİN, 0.15um GaAs pHEMT TEKNOLOJİSİ KULLANILARAK ÖN GERİLİM İLE AYARLANABİLEN, ANAHTARLAMALI, ÖZGÜN DÜŞÜK GÜRÜLTÜLÜ YÜKSELTİCİ TASARIMI

Bu yüksek lisans tez çalışmasında, Wi-Fi 6 uygulamaları için 0.15um GaAs pHEMT teknolojisi kullanılarak, ön gerilim ile ayarlanabilen düşük gürültülü yükseltici tasarımı ve üretimi konusu sunulmuştur. Sunulan çalışma üç farklı frekans durumunda, yalnızca 2.4 GHz ve yalnızca 5.8 GHz frekanslarında, ayrıca 2.4-5.8 GHz ikili bandı için eşzamanlı olarak çalışmaktadır. Frekans ayarlaması geri besleme yollarındaki iki adet anahtarlama transistörü sayesinde yapılmaktadır. Tasarımda kullanılan ön gerilim kaynağı haricinde ek bir gerilim kaynağına ihtiyaç olmadan frekans ayarlaması anahtarlama transistörlerine uygulanan ön gerilim ile yapılabilmektedir. Tasarlanan düşük gürültülü yükseltici tam entegredir, empedans uyumlaması için dışarıdan herhangi bir devre elemanı kullanılması gerekmemektedir. Sunulan tasarımın elektromanyetik (EM) simülasyonu sonuçları 2.4 GHz frekans durumu için kazancı 17.33 dB, gürültü faktörü değeri 2.23 dB ve P1dB değeri 8.32 dBm olarak analiz edilmiştir. Benzer olarak, 5.8 GHz frekans durumu için kazanç değeri 18.44 dB, gürültü faktörü 1.5 dB ve P1dB 3.25 dBm sonuçları EM simülasyonu sonucunda elde edilmiştir. Son olarak, 2.4-5.8 GHz ikili bandı için eşzamanlı durumunda EM simülasyonu sonuçlarında sırasıyla 2.4 GHz ve 5.8 GHz için kazanç 17.34 dB ve 15.79 dB, gürültü faktörü 2.23 dB ve 1.62 dB, P1dB parametresi 7.77 dBm ve 5.34 dBm değerleri alınmıştır. 3.3 V tek gerilim kaynağı kullanılarak tasarlanan düşük gürültülü yükseltici kıymığının güç tüketimi 216 mW'dır. Tasarımda güç tüketimi, kıymık alanının azaltılması ve performans iyileştirmeleri için akımın tekrar kullanım tekniği, otomatik öngerilim ve endüktans dejenerasyonu metotları kullanılmıştır. Tasarlanan kıymık, tüm giriş ve çıkış padleri dahil olmak üzere 3.4x1.5 mm^2 boyutlarına sahiptir. Bütün tasarım, simülasyon ve devre analizleri AWR simülasyon ortamında WIN-PL1512 tasarım kütüphanesi kullanılarak yapılmıştır. Yazarın bildiği kadarı ile literatürde düşük gürültülü yükseltici çalışmalarında iki farklı tek frekans uygulamasını, eşzamanlı ikili band uygulaması ile birleştiren bir tasarım çalışmasına rastlanmamıştır.

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LIST OF SYMBOLS/ABBREVIATIONS

AWR	Advancing the Wireless Revolution Simulation
BJT	Bipolar junction transistor
BSS	Broadcast satellite service
CD	Common drain
CG	Common gate
CS	Common source
dB	Decibel
dBm	Decibel milliwatt
DBS	Direct broadcast satellite
DSB	Double sideband
DVi	Digital visual interface
FCC	Federal communications commission
FET	Field effect transistor
FSS	Fixed satellite service
GaAs	Gallium arsenide
GaN	Gallium nitride
gm	Transconductance
GNSS	Global navigation satellite systems
GPS	Global positioning system
GSE	Ground support equipment
HBT	Heterojunction bipolar transistor
HEMT	High electron mobility transistor
IEEE	Institute of Electrical and Electronics Engineers
IIP3	Input third order intercept point
IM	Intermodulation distortion
InP	Indium phosphide
IP1dB	Input one dB compression point
IP3	Third order intercept point
LNA	Low noise amplifier
LO	Local oscillator

MESFET	Metal semiconductor field effect transistor
mHEMT	Metamorphic high electron mobility transistor
MMIC	Monolithic microwave integrated circuit
NF	Noise figure
ns	nanosecond
OIP3	Output third order intercept point
P1dB	One dB compression point
PA	Power amplifier
PAE	Power added efficiency
PDK	Process design kit
pHEMT	Pseudomorphic high electron mobility transistor
RF	Radio frequency
Si	Silicon
SiGe	Silicon germanium
SNR	Signal to noise ratio
SSB	Single sideband
UWB	Ultra-wide bandwidth
VGA	Video graphics array
VSAT	Very small aperture terminal
WiGig	Wireless gigabit

1. INTRODUCTION

One of the most important characteristics of humankind is its capability and need to communicate with each other. The reasons for the need in communication over the centuries were stating the emotions, transmitting information or just for ensuring entertainment. It is an impressive fact that it takes a few seconds to communicate with the language for people, in contrast, it took thousands of years for people to perfect their language as we know and develop the communication methods [1].

The immediate communication way was limited as the range of a man could shout around 200 years ago. However, rapid development of the industrial sector caused the necessity for faster communication techniques. In the beginning of the 1800s, optical and semaphore signaling were established in Roman Empire and minutely networks were starting to be used in the continent of Europe [2]. As a resulting impact of this, in the beginning of 1830's, Samuel F.B. Morse developed the American system for telegraph and this method has conquered over its familiars because of its simplicity. Thanks to his genius, he designed an electric circuit which has both transmitting and receiving sides which are connected via wire and the current is flowing through the wire when the key is pressed and he included a battery and a key at the transmitting side and an electromagnet at the receiving side [3]. The information carrying text message could be successfully transmitted almost simultaneously with using formerly advanced transformation of the English language into a code consisting of dot, dash and space [4].

In Boston, Alexander Graham Bell was expanding his experiments about telegraphy. He invented the idea of a harmonic multiple telegraph system which was promising for delivering a couple of information over the same line at different frequencies [5]. Harmonic telegraph conceived Bell's very first idea for the telephone. During his experimental process about harmonic telegraph, he realized that he could hear the transmitted pitches through the reed at different frequencies when he pressed his ear to the receiver reed [6]. In March 1876, he succeeded in the invention of the telephone which was life changing and a huge step for human communication history and patented it [7].

Over the years, scientists and engineers studied the methods of communication in order to get rid of the bulkiness of the cables and wires used in the communication system. The term wireless originally comes from without use of wires. The magnetic induction, electrostatic coupling, electromagnetic radiation and waves used as footsteps for the wireless communication concept [8]. However, electrostatic coupling, conduction and magnetic induction mechanisms were suffering from losses at distances which they were capable of covering. The milestone for wireless communication was the successful usage of electromagnetic radiation [9]. The short term for electromagnetic radiation took place in literature and daily lives as radio back in 1895, after the contributions of wireless communication which was the very first invention came from Guglielmo Marconi. He managed to transmit and receive coded messages at a distance of 1.75 miles near his home in Italy [10].

Marconi has continued his works about wireless communication via antennas and his studies in antenna design made him won the Nobel Prize [11]. Thanks to all inventors and scientists mentioned before, their contributions in communication technologies have affected human's lives tremendously. Due to the limited length in antenna sizes and relatively high costs according to increments in size, scientists and engineers have started to study high frequency systems because the antenna's length is inversely proportional to the transmitted signal's frequency. In addition to that, the rising demand for high data rates and ultra-wideband applications lead the studies related to high frequency [12].

In wireless electronics, radio waves which are a type of electromagnetic radiation, does not require a medium such as air in order to travel and radio frequency propagation occurs at the speed of light.

The International Telecommunication Union (ITU) has designated radio frequencies at a range between 3-30 GHz as Super High Frequency (SHF). The radio frequencies at this range are also named as microwave because these frequencies intercept with the microwave band. Furthermore, the Institute of Electrical and Electronics Engineers (IEEE) has designated the several frequency bands distinctions, named them as a letter and distinguished their operational range in 1976. In Figure 1.1, distinguished frequency ranges and their letter names are shown.

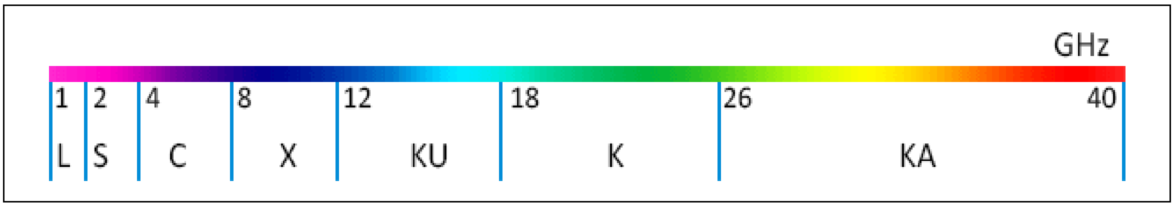


Figure 1.1. IEEE frequency band spectrum for SHF [13]

According to the SHF band spectrum distinction which is given in Figure 1.1, it should be mentioned that some frequency bands have more advantages or disadvantages than others. The frequency band letters and their corresponding application areas are demonstrated in Table 1.1 below.

Table 1.1. General applications of the frequency bands [14]

Band	**Frequency Range (GHz)**	**General Applications**
L	1-2	Satellite, Navigation (GPS etc.), Cellular Phones
S	2-4	Satellite, WiMAX, Wi-Fi, Bluetooth, Cordless Phones, GPS
C	4-8	Satellite, Wi-Fi, Cordless Phones, Surveillance, Weather Radar
X	8-12	Radar, Meteorological Aids, Radiolocation
KU	12-18	Satellite TV, Police Radar
K	18-26	Fixed Satellite, Space Research, Earth Exploration Satellite
KA	26-40	Inter-Satellite, Mobile Satellite

1.1. FREQUENCY SELECTION

In comparison to the other frequency bands, S-band and C-band contain a series of important applications that have impacts on the daily used technological devices. For instance, integrated S-band transceiver designs at 2.4 GHz are being broadly used for wireless local area network, Bluetooth and ZigBee applications [15]. In addition, WLAN and Worldwide Interoperability for Microwave Access (WiMAX) have been involved in handheld computers and smartphones because of these two techniques' viability, cost-effectiveness and availability for the user's mobility. Moreover, 2.4 GHz, 5.2 GHz and 5.8 GHz frequency bands have been covered as standards for WLAN in IEEE 802.11. Frequency bands of 3.5 GHz and 5.5 GHz comprised by WiMAX applications in practice [16].

The ISM band, which is an abbreviated form of Industrial, Scientific and Medical, is commonly used as a result of its unlicensed nature. Moreover, perhaps the 2.4 GHz band is the most popular frequency band due to its availability for Wi-Fi (802.11), Bluetooth (IEEE 802.15.1) and ZigBee (IEEE 802.15.4) applications. Short distance (around 30-feet) wireless connections between modems, computers, smart phones, headsets, personal digital assistants (PDAs), projectors, printers can be realized via Bluetooth applications at 2.4 GHz thanks to the Bluetooth technology [17]. In portable devices, small sized, low manufacturing cost, low powered radios can be embedded with the help of this technology's worldwide compatibility.

The C band covers the 5.8 GHz ISM band which is generally used for medical and industrial heating appliances and several unlicensed short distance microwave communication appliances namely keyless entry systems for cars, baby monitors, and cordless phones. The C band also includes Wi-Fi applications for wireless computer networks at 5.8 GHz announced at IEEE 802.11a standard [18].

1.2. RECEIVER SYSTEM ARCHITECTURES

The demands for wireless communication systems are increasing fast day by day. The receiver systems have to meet the requests about low power consumptions, low supply voltages, low price, high integration and high frequency. The continuing part aims to examine the fronted structures' working principles and discuss their advantages and disadvantages.

1.2.1. Heterodyne Receiver Architecture

This type of receiver has a mature theory foundation with practical background. It is a traditional receiver type, so that most RF communication transceivers still utilizes the heterodyne approach in the manufactured designs. It can perform quadrature down conversion to baseband at the last stage [19]. The signals coming from two branches are combined together and transferred to another stage after the down conversion. This structure has advantages over image reject suppression and relaxing the design of filters [20]. For example, as a result of the first intermediate frequency (IF) being higher than the radio frequency (RF), a single low pass filter can be used instead of a band pass filter. This effect eases the receiver design. In contrast, at high frequency, a super heterodyne receiver acquires discrete filters to reject image signals. In Figure 1.2, receiver architecture for a heterodyne system is given.

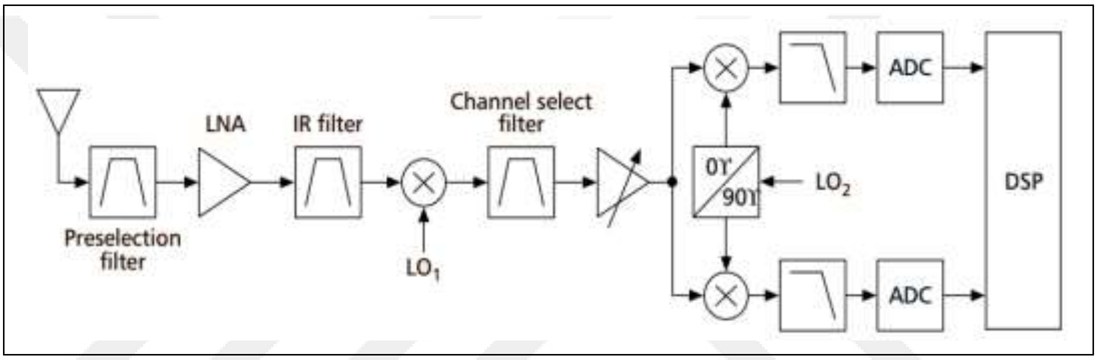


Figure 1.2. The heterodyne receiver block diagram [21]

In order to remove the out of band signal energy with the part of image band signals, RF front end preselection filter is used. As can be seen in Figure 1.2, after the RF pre-filtering, a low noise amplifier (LNA) is added to amplify the received signal. At the image band frequencies, IR filter further attenuates the unwanted signals. The output of the IR filter which has the desired signal applied to down conversion from the carrier frequency to a fixed IF combined with the output of the local oscillator (LO). For reducing the distortions and requirements for the dynamic range at the subsequent receiver blocks, IF filter is used with the combination of variable gain amplifiers [22]. The varactor diodes and high-Q inductors are added to the voltage controlled oscillators (VCO) for the sake of low phase noise and high performance. As an integrated solution, this is the reason why heterodyne receivers are impractical to realize at high frequencies.

The addition of the high-Q discrete component filters such as surface acoustic wave (SAW) or ceramic filters make advantages on selectivity and sensitivity.

1.2.2. Direct Conversion Receiver Architecture

This type of receiver architecture is also known as homodyne or zero-IF conversion since its method for down converting RF signal to directly baseband without any IF stages. Since the key for improving receiver's integration, discrete components should be eliminated [23]. Therefore, one advantage of the homodyne architecture is the wanted signal channel is down converted to zero intermediate frequency. In Figure 1.3, generic structure for the homodyne receiver is demonstrated.

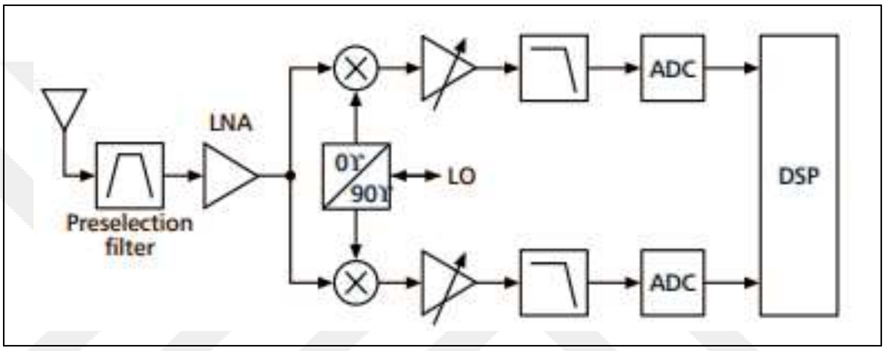


Figure 1.3. The homodyne receiver architecture diagram [24]

Due to the two sidebands of the RF spectrum being usually different, the quadrature down conversion which contains I and Q channels is a necessity for modulation. The requirement for IR filter is circumvented since the intermediary IF stages are absent. The second advantage of the homodyne architecture over heterodyne is that the LNA does not need to drive 50-Ω load since there is no requirement for the bulky off-chip image reject filter [25].

The homodyne receiver architecture is severe from the unwanted DC off-sets that can be eliminated via AC coupling at the down converted signal path or minimizing the baseband signal energy near dc by selecting dc free modulation scheme [26]. Furthermore, the flicker noise of the devices has a major effect on SNR because of the down converted signal fitted around zero frequency [27].

1.3. RESEARCH GOAL AND MOTIVATION

The demand for wireless communication system technologies are growing rapidly over the years. In order to meet these demands, higher spectrum efficiency, higher communication speed and better performances in high network densities are needed. According to that, the Wi-Fi Alliance started to certify the appliances and networks as Wi-Fi 6 which satisfies the specifications of the IEEE 802.11ax standards [28]. These standards can be applied to house appliances, smart phones, routers as well as the networks themselves.

Wi-Fi 6 follows the naming conventions after Wi-Fi 5 and Wi-Fi 4. Additionally, it covers the frequency range to 1 to 6 GHz which was specified by IEEE 802.11ax standard. IEEE 802.11ax standard was first studied in 2014 by IEEE High Efficiency WLAN Study Group (HEW SG). The Wi-Fi Alliance started to approve certifications in late 2019. The purpose for development of this technology is not unpredictable, the main goal is supporting the high speed communication for high demand devices at the same time.

While 2.4 GHz Wi-Fi provides greater range and good penetration of walls and ceilings due to smaller operating frequency, as a trade-off 5.8 GHz Wi-Fi supplies great data rate [29]. Increasing the number of access points in order to keep the signal at strong levels for connected devices can be a solution for industrial and commercial installations.

Moreover, frequency range adaptability is an important requirement for multi usage of a design. For example, dual band modem routers have been always appealing for customers because of their offerings in frequency operation. In higher data rate requirements such as watching a high quality video or playing a video game, customers can select high speed mode which means higher frequency operation mode from their routers. For other daily applications, customers may choose moderate speed mode and they do not cause any traffic in the wireless internet system in their home. Thanks to this modem router which gives the author a curiosity in working principles of multiband operating appliances.

To the author's best knowledge, there is no study reported related to a switchable low noise amplifier which operates in single 2.4 GHz, single 5.8 GHz and concurrent dual 2.4-5.8 GHz frequency bands. There are many works published based on single band switchable or concurrent dual band low noise amplifiers, however there is not any low noise amplifier design which covers the four cases for application including bypass condition. On a single chip, there is one low noise amplifier operating in three different frequency conditions by only changing the gate voltages of controlling transistors. After completing the literature review, this was the strongest motive behind the master thesis design.

In the analysis of the commercial products, the proposed low noise amplifier design would be used in Bluetooth, Wi-Fi 6, point to point communication, GPS navigation systems, satellite, pagers and IoT appliances in a household.

1.4. THESIS ORGANIZATION

In chapter 1,brief information about frequency selection and types of receiver architectures are stated. The research goal and main motivation behind the master thesis study is explained.

In chapter 2, technology selection subject is examined with respect to operating frequency, noise performance, power consumption, linearity concerns and fabrication cost consideration.

In chapter 3, general information about the fundamentals of the radio frequency circuit design is studied. The radio frequency performance metrics such as noise types, stability, sensitivity, linearity, scattering parameters and impedance matching are mentioned. Design difficulties of radio frequency integrated circuits are explained.

In chapter 4, various feedback topologies used in low noise amplifier circuit designs are investigated and their comparison between each other is stated based on performance.

In chapter 5, different design techniques which are commonly used in low noise amplifier design are mentioned. A general idea about the inductive degeneration, inductive peaking, diode connected load, self-biasing and the current reuse methods are given.

In chapter 6, the design concept of the low noise amplifier circuits is stated. The subjects of frequency applications and commonly used topologies are mentioned in this section of the thesis.

In chapter 7, brief information about the master thesis design and its simulation results which includes both schematic and EM simulations are shown. The comparison between schematic and EM simulation is stated. In addition, temperature analysis and power consumption of the chip is given.

In chapter 8, summary of the thesis is given with the future work ideas related to the design. Moreover, comparison tables that are constructed during the literature review phase are shared in order to analyze the results obtained by the master thesis design with other academic papers.

2. TECHNOLOGY SELECTION

This chapter of the thesis aims to clarify the reasons behind the study in manners of frequency of function, noise performance, power consideration, linearity performance and comparison with other technologies.

2.1. FREQUENCY OF OPERATION

Radio frequency spectrum takes place between 3 kHz to 300 GHz and it is a finite natural source of electromagnetic radiation [30]. The radio frequency spectrum is divided into several frequency bands which allocate the applications for specific radio transmission technologies. Even though the radio frequency spectrum is extensive, the restraints of technology limits the usable spectrum. In terms of cellular communication, three categories split under the radio frequency spectrum which is low-band, mid-band and high-band. The low-band covers the range for under 1 GHz while mid-band is from 1 GHz to 6 GHz and high-band is in the range of 24 GHz to 100 GHz [31]. The mobile wireless networks for 4G applications use radio frequency in low and mid band which is 600 MHz to 3.5 GHz while 5G expands to higher frequencies. The commercial services for instance mobile voice and data or television broadcasting, as well as government functions such as aviation communication, weather services, homeland security and national defense make spectrum division essential. The spectrum managers are studying the techniques for the usage of spectrum smarter while the rapid growth in technologies which requires the radio frequency spectrum do not limit the availability of broadband and maintain crucial services. Figure 2.1 demonstrates the radio frequency spectrum applications for specific frequency ranges. The extremely high throughput is abbreviated as EHT on the following figure.

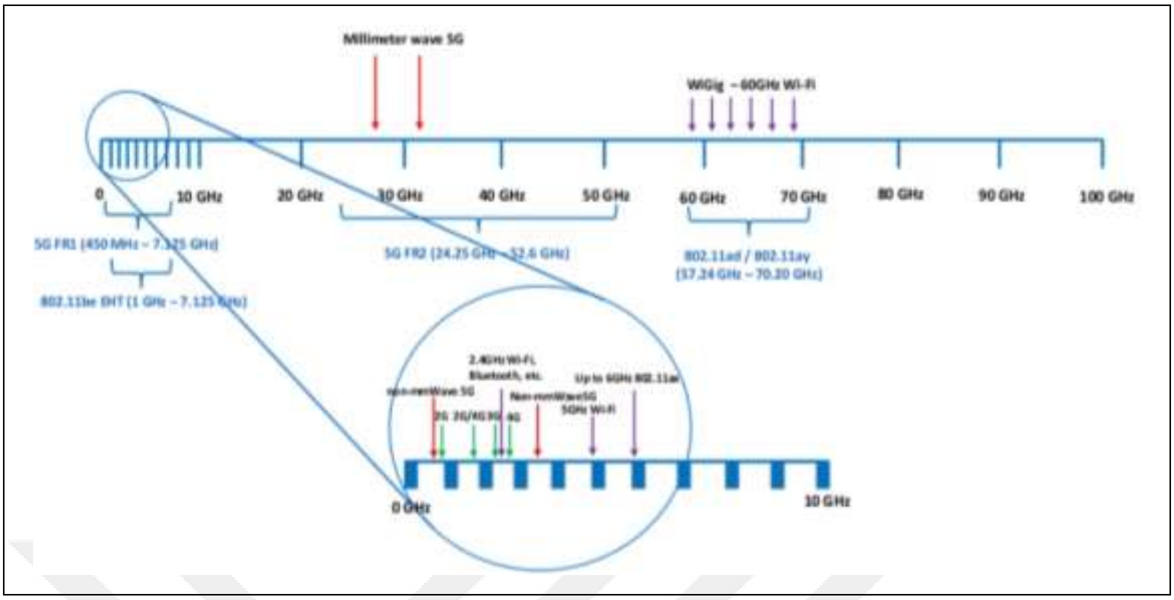


Figure 2.1. Spectrum investigation for 5G and various Wi-Fi protocols [32]

The sixth generation of wireless protocol IEEE 802.11ax is a standard for wireless local area networks (WLAN) and it is marketed as Wi-Fi 6 or Wi-Fi 6E. Moreover, it is the successor of IEEE 802.11.ac which was the fifth generation of wireless protocol and labeled as Wi-Fi 5 by Wi-Fi Alliance. The Wi-Fi 6 applications cover the frequencies of 2.4 GHz and 5 GHz while the Wi-Fi 6E mainly focuses on 6 GHz. Additionally, the main goal of this protocol is improvement in throughput per area in high density local areas such as shopping malls, offices or residential apartments. During comparison studies with IEEE 802.11.ac, reports stated the nominal data rate has improved by 37 percent and overall throughput improved by 400 percent while 75 percent of lower translation latency [33].

Meanwhile at the IEEE 802.1 committee, the standard setters in the working group have been studying on finalizing the specifications for the next stage wireless local area networks. The committee released the detailed technical criteria information about the new technology which is referred to as 802.11.be and expected to be named as Wi-Fi 7 in the late 2024 [34]. The development for the 802.11.be is still ongoing, however its studies are installed upon 802.11.ax (Wi-Fi 6) and it offers high speed in the 2.4 GHz, 5 GHz and 6 GHz frequency bands [35]. Figure 2.2 states the different marks between three generation wireless fidelities.

Figure 2.2. Three generations of Wi-Fi comparisons [36]

In order to compile all the information about wireless local area network technologies according to IEEE standards and Wi-Fi Alliance's industrial designations, Figure 2.3 is attached.

Figure 2.3. IEEE standards and Wi-Fi Alliance statements [37]

On Table 2.1, detailed comparisons between five different wireless fidelity technologies are shown. As mentioned before, studies related to the seventh generation of wireless fidelity are still ongoing.

Table 2.1. Wireless network technology performance comparisons [38]

Protocol	Wi-Fi		Wi-Fi 4	Wi-Fi 5	Wi-Fi 6/6E	Wi-Fi 7 (ongoing)
Release Year	1999	2007	2009	2013	2020	2023
Frequency Band	2.4 GHz	2.4 GHz	2.4 and 5 GHz	5 GHz	2.4, 5 and 6 GHz (6E)	2.4, 5 and 6 GHz
Bandwidth	20 MHz	20 MHz	40 MHZ	80 MHz, 160 MHz	80 MHz, 160 MHz	240 MHz, 320 MHz

Briefly, the main reason for this study to design on 2.4 GHz and 5.8 GHz frequency bands is its adaptability for Wi-Fi 6 and Wi-Fi 6E applications with being appropriate for the usage in the areas specified in range of ISM band.

2.2. NOISE PERFORMANCE

Increasing demand and growth in technology made margins in designs squeezed, adjunct concurrency was added for the purpose of the circuits being able to run at higher frequencies than in the past. According to Moore's Law, which is the statement that for every three years, the density of the digital integrated circuits would double at half the cost, it is starting to slow down. That might cause the technology to go through saturation in some manners, designs should do more with less capability. Because of that, noise is one of the most potentially outcome metrics that would cause concerns in a chip’s performance [39]. For a three-terminal device, the noise performance can be separated into three parts as demonstrated in Figure 2.4.

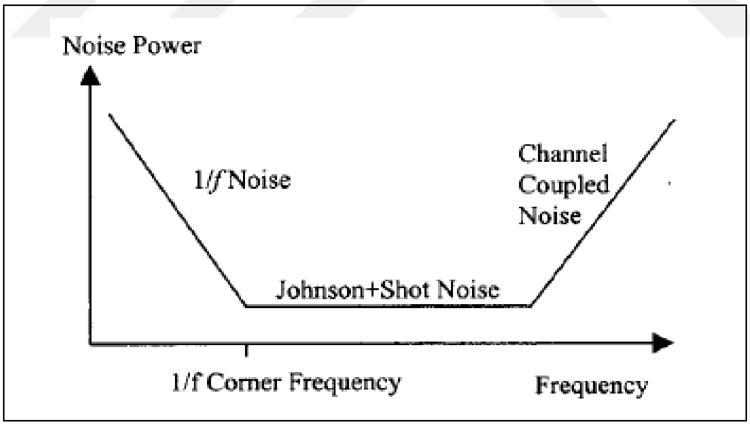


Figure 2.4. The noise power density spectrum relation with frequency of a three terminal device [40]

In the junction interfaces or in the surface of substrate, trapping effects in the bulk material makes a greater contribution to the noise performance at lower frequencies. 1/f relation is combined by these effects to give noise power spectral density. As can be seen in Figure 2.4, above the 1/f corner frequency, the Johnson noise resulted from the resistances in current path with the addition of the current shot noise. The Johnson noise arises when access resistance in the collector and emitter regions, the dynamic resistance of the collector-emitter and base-emitter junctions and the base's intrinsic resistance in bipolar technologies. Moreover, the channel resistance and the drain and source resistances cause the Johnson noise in HEMTs and MESFETs [41].

As the frequency increases, the noise increases while the parasitic coupling becomes efficient. As can be predicted, in order to minimize the Johnson noise which might be coupled to the input and output, a low noise device ought to have small input resistance, low internal resistance and low capacitance [42]. Additionally, from the shot noise contribution aspect, the noise will be current dependent.

After silicon, gallium arsenide (GaAs) is the most commonly chosen material in semiconductor devices. It is a member of the III-V compound semiconductor family. Generally gallium, aluminum and indium from column III of periodic table alloys with arsenic, phosphorus from column V [43]. Higher electron mobility and direct band gap properties are its main advantages over silicon. Thus, in wireless data transmission applications and mobile phones, integrated circuit technologies structured on GaAs are now firmly established. On Table 2.2, comparisons of field effect and bipolar technologies in terms of the noise performance is listed.

Table 2.2. The noise performance analysis comparison for different technologies [44]

Technology	**1/f corner frequency**	**Minimum Noise Figure**	**Associated Gain**
Si bipolar	< 1 kHz	1.5 dB @ 2 GHz	21 dB @ 2 GHz
SiGe HBT	< 1 kHz	0.65 dB @ 2 GHz 3 dB @ 2 GHz	21 dB @ 2 GHz 5 dB @ 12 GHz
GaAs HBT	< 1 kHz	0.4 dB @ 2 GHz	25 dB @ 2 GHz
GaAs MESFET	> 10 MHz	0.8 dB @ 12 GHz	12 dB @ 12 GHz
GaAs pHEMT	> 10 MHz	0.25 dB @ 2 GHz 1 dB @ 18 GHz	16 dB @ 4 GHz 10 dB @ 18 GHz
InP HEMT	> 10 MHz	0.3 dB @ 18 GHz	17 dB @ 18 GHz

Due to its high integrity for gain versus noise figure performance, GaAs pHEMTs are one of the most suitable technologies for low noise amplifier design. By being the first amplifying stage in the receiving architecture, low noise amplifiers are designed to amplify weak signals coming from the antenna with considerably low noise so that not to disturb the original signal. Therefore, this master thesis project has been done under the beneficial substrate of gallium arsenide pseudomorphic high electron mobility transistor (pHEMT).

2.3. POWER CONSUMPTION AND LINEARITY BEHAVIOUR

The growth in cellular infrastructure business, base-station and obtaining new standards which require excellent linearity and high efficiency from a power amplifier together with cost effectiveness are the major drivers that lead gallium arsenide radio frequency semiconductor business to rapidly progress. This reason caused increased demand in GaAs power products. Furthermore, the unprecedented requisitions in the handset market was another major driver in this technology.

The minimum and maximum current and voltage levels that can be supported by a transistor define the power handling capability of a device. Therefore, it is essential to maximize the breakdown voltage of the device simultaneously with maximizing the drive current capability for a selected device geometry whilst minimizing device access resistance [45]. Thanks to its tolerance to high breakdown voltages, GaAs becomes superior amongst other semiconductor technologies.

In Figure 2.5, the technology roadmap for different materials used in radio frequency designs is demonstrated.

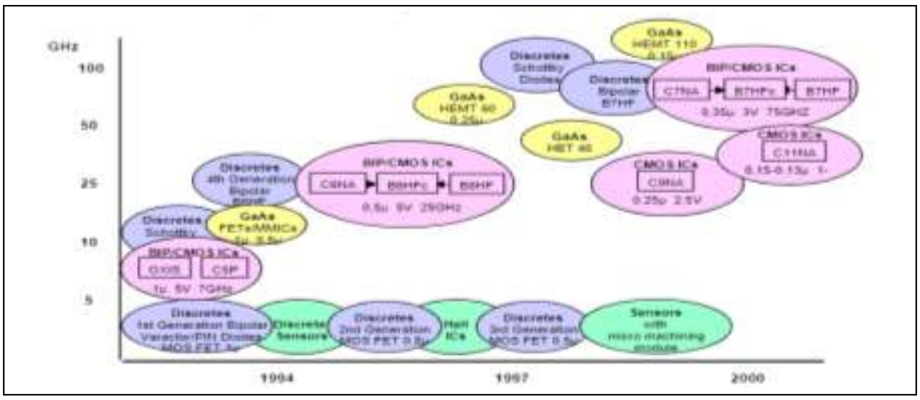


Figure 2.5. Siemens radio frequency technology roadmap [46]

The documentation from Siemens semiconductor group stated that, great deal of low noise applications in receiver systems are going to be covered by Si technologies. The low noise application conditions can be satisfied by both GaAs and Si. However, for special applications like super linear mixers with high input IP3 is still going to be in domain for gallium arsenide technologies [47]. In addition to that, due to its high performance at high frequencies, many power amplifier designs have been published under the roof of GaAs [48]. On Table 2.3, comparisons for semiconductor technologies are given in terms of power, gain and efficiency.

Table 2.3. Performance comparisons according to weakness and strength of different technologies [49]

	GaAs based Technology			**Si based Technology**	
Parameter	MESFET	HEMT	HBT	Si BJT	SiGe HBT
LF < 100 MHz	moderate	moderate	good	best	best
RF ~ 2 GHz	best	best	best	good	good
RF ~ 10 GHz	good	best	good		moderate
Gain	good	best	best	best	best
Power < 0.5 W	best	best	best	good	good
Power > 2W	best	best	best		
Efficiency	good	best	good	moderate	moderate

The efficiency of a system diminishes as a result of the presence of nonlinearities in the design. Nonlinearity causes distortion and it hampers the overall system performance. Thus, nonlinearity in a design is highly undesirable and should be taken into account so that it will not affect the working efficiency of the system [50]. GaAs FET device technologies suffer from their ability to ensure ultra-low noise as well as low intermodulation distortion with low dc power consumption. However, GaAs HEMT and MESFET devices are adjustable for low noise applications, they are outperformed by HBT devices in terms of linearity [51]. For the same output third order intercept point (IP3), narrow band tuned HBT technology consumes fourth or sixth times less dc power in comparison with HEMT and MESFET devices. On Table 2.4, overviews for different radio frequency solid state technologies are stated.

Table 2.4. Comparison for linearity and PAE for solid-state RF power transistor technologies [52]

Technology	Power Density	Linearity	Frequency	PAE
Si BJT	Medium	Poor	< 2 GHz	Low
SiGe BJT	Medium	Good	> 2 GHz	High
Si LDMOS	Low	Very Good	< 3 GHz	Medium
SiC MESFET	Very High	Good	> 4 GHz	Medium
GaAs MESFET	Medium	Good	> 2GHz	Medium
GaAs pHEMT	Medium	Very Good	> 2 GHz	High
GaAs HBT	High	Good	> 4 GHz	Medium
GaN HEMT	Very High	Promising	> 12 GHz	High

2.4. FABRICATION COST ANALYSIS

High level of utilization of the available means in order to assure the maximum productivity makes semiconductor wafer processing one of the most advanced and challenging fabrication types. Keeping the operation as lean as possible is key to cost effectiveness. In addition to semiconductor tools being expensive, there would also be a need for extra spending for infrastructure. The creativity and innovations are generated by fab engineers as a result of this escalating ratio of fabrication. In Figure 2.6, the factory establishment cost (fab cost) changes over the years is demonstrated.

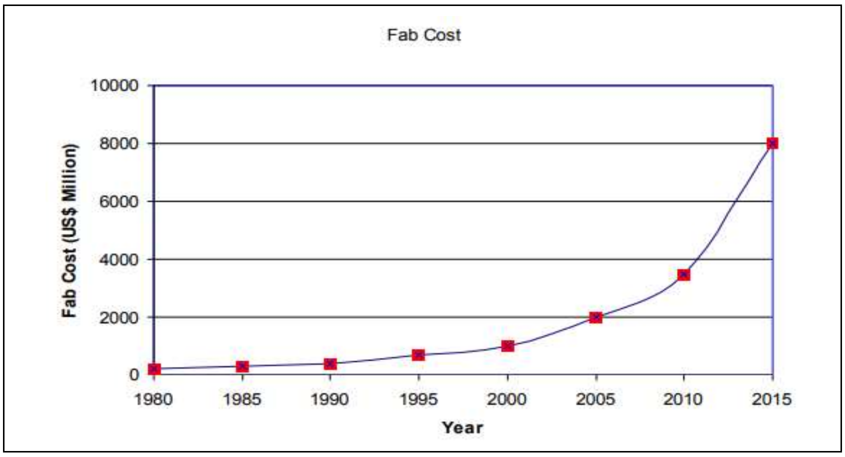


Figure 2.6. Factory cost increment between 1980 and 2015 [53]

Most of the new semiconductor technology factories are planned to be built under construction in East and Southeast Asia regions of the world [54]. With the global-wise perspective, countries with high populations are not only beneficial for human resources and capitals for technological resources but also provide huge markets for industrial products. Huge population causes relatively cheap and high-quality labor, in addition to that, considerably stable economical political issues makes Far East and some Southeast Asia countries one of the most suitable investments for semiconductor manufacturing. For example, Figure 2.7 states the global distribution of 300 mm factories in the world. It is expected that the increased number of factories in the East and Southeast Asia region will eventually dominate the world semiconductor manufacturing.

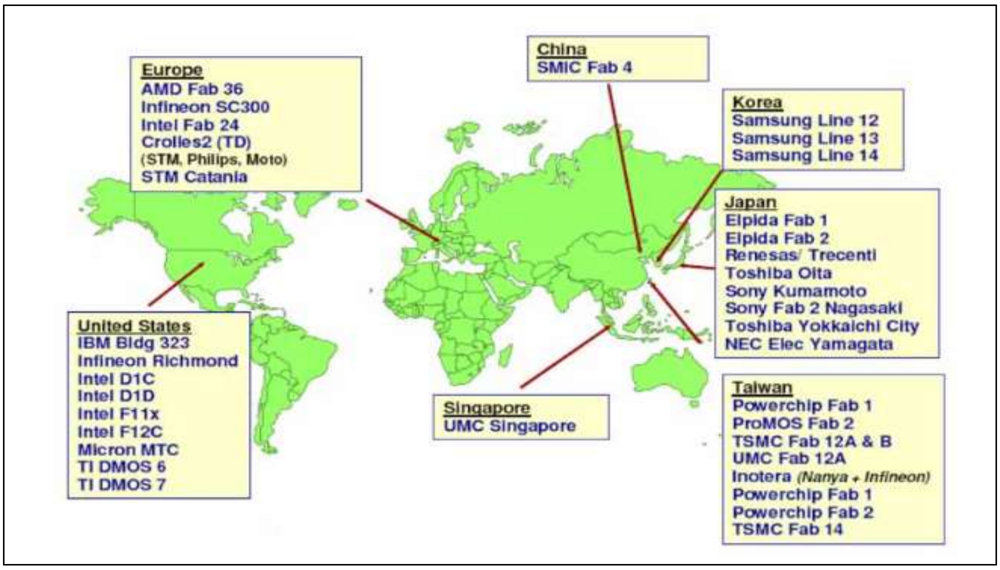


Figure 2.7. Global distribution of the 300mm wafer diameter factories [55]

The continuous paragraphs of this subsection explains different semiconductor material technologies from the RFIC point of view. For being the most cost effective, large wafer size and offering high yields in many factories with years of experience, complementary metal-oxide semiconductor (CMOS) provides billions of computer memory chips to analog or digital building block devices. Motivated by the computing industry and Moore’s Law, operation for higher frequencies allowed by the CMOS technology just by reduction in physical size. So that CMOS is a promising application for cost versus performance effective future for RFIC technology.

The appropriate process and design simulating tools and development of consistent doping profiles were the initial difficulties in SiGe and BiCMOS processes. This reason kept the cost of the SiGe process high for a long time [56].

For GaAs and other III-V semiconductors, the early drawback was in modeling of the distributed elements and passive components in the time domain. This was a distinct modeling path from silicon processes, therefore companies came to a crossroad; whether they have the budget for GaAs specialized tools which had no use in silicon realm or not. However, costs have been reduced thanks to recent increase in the use of pHEMT technology which provides high frequency advantages with the performance enhancements [57]. The International Technology Roadmap for Semiconductor (ITRS) made a report for related cost in power amplifier fabrications in 2006, Table 2.5 shows the reported analysis.

Table 2.5. Power amplifier die costs in 2006 projected by ITRS [58]

Technology	SiGe HBT	GaAs FET	GaAs HBT
Cost / mm^2 ($)	0.12	0.25	0.35
Product Cost ($)	0.30	1.00	0.875

On the other hand, Table 2.6 demonstrates power amplifier fabrication costs together with the wafer and process costs of different semiconductor technologies. The reference literature was published in 2003.

Table 2.6. Power amplifier chip cost comparison with wafer sizes [59]

Technology	Wafer Diameter Size (mm)	Wafer Cost ($)	Process Cost ($)
GaAs MESFET	100	150	3000
GaAs PHEMT	100	500	5000
GaN HEMT	75	3000	5000
Si LDMOS	125	100	1000
SiC MESFET	75	3000	4000

3. FUNDAMENTALS OF THE RF CIRCUIT DESIGN

This section of the thesis contains information about the factors that have a direct impact on the radio frequency equipment such as noise, stability, sensitivity, linearity, scattering parameters, impedance matching and design difficulties that are generally experienced in RFIC designs.

3.1. CONSIDERATIONS IN RADIO FREQUENCY TECHNOLOGY

The background information is strongly needed about the basic concepts of considerations in RF electronics. The goal of this part is to declare and explain the fundamentals about given concepts.

3.1.1. Noise Types

In electronics, noise is a random, undesired disturbance in an electrical signal. The noise which coincides with the transmitted message can be generated in a communication system as a result of communicating medium or can be produced at the receiver side. In a circuit block, any random disturbance in current or voltage can result in noise. Therefore, it is analyzed that there are many sorts of noise sources namely, thermal noise, shot noise, flicker noise, avalanche noise and burst noise [60].

3.1.1.1. Thermal Noise (Johnson Noise)

It is also known as Johnson-Nyquist noise. The random process of the fluctuation of resistance causes thermal noise. The resistance in a device is directly related to collision between electrons or other charge carriers.

Thermal noise which is generated by the arbitrary thermal motion or collision of the electrons or charge carriers still present at the absence of current [61]. Additionally, thermal noise is usually considered as white noise meaning that it has nearly equal power spectral density throughout the frequency spectrum.

3.1.1.2. Shot Noise

In the process of a charge carrier such as electrons traversing a gap, unavoidable random fluctuations in electric current causes shot noise in the electronic devices [62]. The discrete arrival times of the electrons reaching across a barrier generate shot noise. These current elements differ from each other because they have different velocities. The arbitrary movement of the holes and electrons across the PN junction creates shot noise. At the junction of a semiconductor, the summation of all current elements results in a huge number of current pulses. The fluctuations around the average value of the current pulses are called shot noise [63].

3.1.1.3. Flicker Noise

Like the shot noise, occurrence of the flicker noise is always related to direct current. Thus, a resistor without a direct current flowing through does not produce flicker noise. The crystal defects and contaminations cause the flicker noise [64]. This type is also known as 1/f noise. Especially when designing RF oscillators, the effect of the flicker noise can be minimized by selecting proper devices. Flicker noise precedence at low frequencies or low frequency offsets from the oscillators [65].

3.1.1.4. Avalanche Noise

The avalanche noise occurs only in PN junctions biased with a voltage value that is near the breakdown voltage. In addition, it is related to the reverse biased junctions [66]. The leakage current is multiplied by the avalanche phenomenon, for high reverse junction voltages. In the existence of the large electric field, the charge carriers at the junction gain energy during their collision with the crystal lattice. Another pair of charge carriers can be produced whether the energy gained during the collision is large enough [67]. As a result, the reverse biased current might be multiplied. It has been noted that the effect of the avalanche noise is generally larger than the other noise components.

3.1.1.5. Burst Noise

This type of noise is also known as popcorn noise or radio telegraph signal (RTS) noise which happens when random fluctuations occur in voltage or current with the equally high random discrete impulses [68]. At unexpected times, the level of burst noise might be as high as a hundred microvolts. RTS or burst noise was a serious issue back when first operational amplifiers were designed. It has the name of popcorn noise because it affects the loudspeakers to generate the sound like cooking popcorn. The burst noise is not very common since semiconductor manufacturing has high standards in these days [69].

3.1.2. Stability

The potential of the instability is an important property for a non-unilateral transistor. The transistor might be caused to oscillate according to certain combinations of the input and output terminal impedances. Although the very first contribution to stability analysis belongs to Rollet's paper [70], Kurokawa's point of view about stability based on scattering parameters has provided an alternative method for the stability analysis. The unconditional stability condition is obtained for a transistor if the following inequalities related to scattering parameters are satisfied [71];

$$K = \frac{1 - |S_{11}| - |S_{22}| + |\Delta^2|}{2|S_{12}S_{21}|} > 1 \tag{3.1}$$

$$|\Delta| < 1 \tag{3.2}$$

Equations 3.1 and 3.2 are known as Kurokawa's stability criterion. Delta (Δ) is the determinant of the transistor scattering matrix. It can be stated as the Equation 3.3 [72].

$$\Delta = S_{11}S_{22} - S_{21}S_{12} \tag{3.3}$$

Additionally, there are many microwave circuit design tools that capable of simulating K and Δ factors. The transistor is said to be stable whether inequalities given in Equation 3.1 or Equation 3.2 are satisfied.

The amplifier should be stable not only in its operating frequency but also it should perform a stable behaviour up to the transistor's transition frequency. Any instabilities out of the working band may result in oscillations which cause saturation of the amplifier and total degradation of the gain or intermodulation with the desired signal and generating spurs [73]. Moreover, out of operation frequency terminating impedances usually have more impact on stability than operation frequency ones and this situation increases out of the band stability requirement.

3.1.3. Sensitivity

The weakest signal that can be successfully received at the receiver side is the criterion for a radio receiver's sensitivity. Sensitivity is a key property for a radio receiver so that a number of figures of merits or methods have been used depending on the applications [74].

3.1.3.1. Signal to Noise Ratio (SNR)

Generally, SNR is a reasonable comparison for sensitivity in radio communication equipment at high frequency and a straightforward method for computing the ratio of a desired signal to noise within the receiver system. By definition, the lower the noise presenting in the system, the better the signal to noise ratio. The signal to noise ratio can be represented as S/N in some literatures and the formula for this parameter is given in Equation 3.4 as follows [75]. Power of the signal and power of the noise signal are stated as P_{signal} and P_{noise}, respectively.

$$\mathrm{SNR} = \frac{P_{signal}}{P_{noise}} \tag{3.4}$$

The formula given in Equation 3.4 can be modified as Equation 3.5 if all power parameters are expressed in decibels.

$$\mathrm{SNR(dB)} = P_{signal}(\mathrm{dB}) - P_{noise}(\mathrm{dB}) \tag{3.5}$$

Being the most basic and easy to comprehend way to analyze the sensitivity of a receiver, SNR is widely used while ranging from broadcast reception to mobile or fixed radio communications.

3.1.3.2. Signal to Noise Distortion (SINAD)

The signal to noise distortion is a commonly used parameter for computing the sensitivity of a system at the base of FM and VHF/UHF. Additionally, it is being used in other radio communication systems as well.

The formulation for the SINAD in decibels is quite straightforward which is stated in Equation 3.6 [76].

$$\mathrm{SINAD(dB)} = 10\log_{10}\left[\frac{P_{Signal} + P_{Noise} + P_{Distortion}}{P_{Noise} + P_{Distortion}}\right] \tag{3.6}$$

It is worth mentioning that the SINAD formulation given in Equation 3.6 is in power ratio levels, not in voltage ratio.

The special measurement instruments for testing SINAD are available. These devices are commonly used in design stages of the RF circuits. Therefore, SINAD is a commonly used figure of merit for radio sensitivity [77].

3.1.3.3. Noise Factor and Noise Figure

The degradation of the signal and noise ratio at the input port versus output port can also be expressed by the noise factor. Inasmuch as the signal to noise ratio at the output will always be less than signal to noise ratio at the input, noise factor is expected to be greater than 1 in a receiver system. The sensitivity of a system is better when noise factor is lower [78]. The formulation of the noise factor is shown in Equation 3.7. The S and N abbreviations express the signal and noise occurring in the system.

$$\text{Noise Factor} = \frac{\frac{S_{IN}}{N_{IN}}}{\frac{S_{OUT}}{N_{OUT}}} \tag{3.7}$$

It should be mentioned that parameters given in Equation 3.7 are in signal levels. Thus, the more convenient and practical way of describing the noise factor is called the noise figure which is in decibels. The noise figure can be found as Equation 3.8 [79].

$$\text{Noise Figure (dB)} = 10 \text{ x} \log(\text{Noise Factor}) \tag{3.8}$$

Essentially, noise figure is a metric that shows the amount of noise which an element adds to the system. These elements might be a complete receiver, preamplifier or mixer.

3.1.4. Linearity

The linearity of a microwave system or a component is the ability of the output signal being proportional to the input signal. However, it is not quite easy to achieve good linearity in communication systems. Many obstacles to linearity should be overcome in order to achieve good linearity at the sacrifices in other parameters such as gain, noise figure etc. whether the components are amplifiers, mixers or a complete system [80].

Ideally for an amplifier, the plot of the output power versus the input power is expected to be a straight line which has a slope equal to the gain of the amplifier. The line would be straight whether the gain vs frequency response is quite coequal. However, in RF or microwave amplifiers the line tends to decline in gain at higher frequencies [81].

In a wireless communication system, linearity becomes a crucial metric for its receivers, transmitters as well as its components. Furthermore, good linearity is strongly needed in devices like power amplifiers, switches and mixers since poor linearity is the most conspicuous in them. Generally, a RF power amplifier consists of several semiconductors which have nonlinearity in its nature. Moreover, the unwanted levels of intermodulation distortion mixing and signal generation may have occurred as a result of nonlinear behavior [82].

For analyzing the potential nonlinearity of an amplifier, several parameters have been commonly used. These parameters are named as; 1-dB compression point (P1dB), third order intercept point (IP3 or TOI) or second order intercept point (IP2) [83].

If a device such as a power amplifier, mixer etc. is operating in its linear region, gain through that device is expected to be constant. When the input power is increasing, the device reaches a point where the output power can not be increased by the same amount as the input signal power. That means that there is a compression of power at the output. That point is named as 1-dB compression point. A general representation for P1dB and IP3 is shown in Figure 3.1.

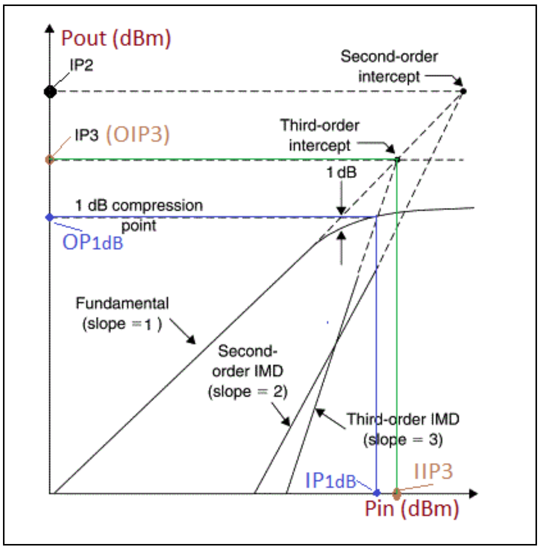


Figure 3.1. Input power versus output power graph [84]

The relation between input and output P1dB is expressed in Equation 3.9. In this equation, the unit for input and output P1dB values is dBm.

$$\text{Output P1dB} = \text{Input P1dB} + \text{Gain} \tag{3.9}$$

Third order intermodulation products result in IIP3 and OIP3. At the IIP3 input level, RF circuits can not properly amplify the input signal nor function correctly. The third order intercept point measurement is another way to observe the linearity performance of the system. The unwanted signals such as intermodulation signal and harmonics of the input signal severely affect the linearity. The graphical representation for this parameter is demonstrated in Figure 3.1. The equation for IP3 is stated in Equation 3.10 [85]. In that equation, IP3 and P1dB are in dBm levels.

$$\text{IP3} = \text{P1dB} + 10\text{ dB (roughly)} \tag{3.10}$$

3.1.5. Scattering Parameters

Formerly back in the 1950s, the primary method for analyzing a circuit performance at high frequencies were Y and Z-parameters which are network parameters that were commonly used [86]. However, relationships of current and voltage with circuit performance were not convenient circuits with using transmission lines as waveguides at higher frequencies. The s-parameters are related with the power waves and express the scattering matrix of a microwave circuit which quantifies the act of RF signal energy in a multiport network [87]. During the 1960s, the progress in the s-parameter concept helped Hewlett-Packard to develop very first microwave network analyzers.

In order to understand the concepts of s-parameters, Figure 3.2 shows a transistor whose input incident and reflected waves are illustrated with a_1 and b_1 and output incident and reflected waves stated as a_2 and b_2, respectively. For an RF signal applied to the input port of a transistor, some fraction of that signal is reflected back through or into the incident port.

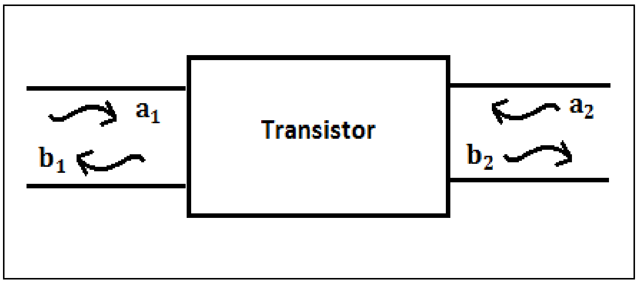


Figure 3.2. Incident and reflected wave propagations of a transistor

There are four sets of s-parameters, which help to analyze important metrics of the RF design separately. One of them is S_{11} which is the input reflection coefficient with output properly terminated. The Equation 3.11 gives the formulation and its condition for the calculation. Additionally, S_{11} is also known as input matching in short terms.

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \tag{3.11}$$

To continue, S_{12} is another parameter that defines the reverse transmission coefficient with input properly terminated which means a_1 equals to zero. The formulation is in Equation 3.12 as follows.

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \tag{3.12}$$

The gain is the one of the most important metrics in an amplifier design. Thus, S_{21} is the forward transmission coefficient with output properly terminated. It is a key parameter for the gain in RF circuit designs. The Equation 3.13 demonstrates the gain calculation for situations when a_2 equals zero.

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \tag{3.13}$$

The output isolation is another issue to consider in RF circuit design. The output reflection coefficient with input properly terminated is said to be S_{22}. The formulation for the S_{22} when a_1 equals to zero is given in Equation 3.14.

$$S_{22} = \frac{b_2}{a_2}\bigg|_{a_1=0} \tag{3.14}$$

3.1.6. Impedance Matching

Between source and load, in order to achieve maximum possible power transfer, impedance matching becomes a vital issue in RF circuit design. Especially in an amplifier design, the impedance matching analysis of a two port network in terms of S-parameters have importance [88].

Designers have two options to choose if they have any RF circuit components with un-matched impedances; one of them is modifying the component and the other one is correcting the mismatch by adding a circuit. Generally, the second method is chosen for its convenience and practicableness. There are several conventional methods studied about impedance matching such as lumped element matching or distributed matching networks which separated into different types subsequently [89].

3.2. DIFFICULTIES IN RFIC DESIGNS

There are several difficulties reported in the RFIC design such as unavailability to obtain high quality inductors, the need for zero capacitors and potential problems caused by the bond wires [90]. During the RFIC design process, inductors are built on the IC substrate. The spiral configuration must be used because it is built on a two dimensional plane. There are three problems raised according to the spiral inductor, such as; extremely low quality value, occupying large area, easiness on interfering with other interference sources because of the created magnetic flux.

The quality factor of a spiral inductor is around 10 in the radio frequency range in most libraries supplied for IC designs [91]. In contrast, in the RF circuit design with discrete parts, the quality factor of a spiral inductor is over 100. Therefore, the low quality factor of the spiral inductors is the biggest bottleneck in the RFIC design. Furthermore, the spiral inductor occupies a larger area on the chip which affects the cost of the die tremendously [92].

The zero capacitance which is a professional jargon is the second drawback of the RFIC designs. The term zero capacitor indicates that at the specified frequency range, the capacitance of the capacitor approaches zero [93]. The zero capacitors can function in circuitry as DC block capacitors or AC bypass capacitors. The development of the zero capacitors directly on the IC chip is difficult since its large size.

4. FEEDBACK IN ELECTRONICS

There are various ways that feedback is used in electronic circuit designs. Feedback is a technique which can be defined as a fraction of the output signal, which can be either voltage or current, applied to input for the further process. Its type can be either negative or positive, which depends on whether the fraction of the applied signal through the feedback path to input is opposite or same in value or phase. If it has a degenerative effect on the input signal to be processed, it is called negative feedback. Generally in amplifier designs, positive feedback is not recommended because continuous summation of the signal would cause uncontrollable instability in the electronic circuits. Because of this reason, in oscillator designs, it is preferred to apply positive feedback as an instability tool for circuitry while keeping it under control. However, in most amplifier topologies, negative feedback is applied for controlling the gain or output voltage, reducing distortion, improving stability and most significantly, expanding the bandwidth of the designs [94].

In high power audio amplifiers, the earliest use of negative feedback was to reduce distortions. Other common applications were in the modulator of amplitude modulated (AM) broadcast transmitters and audio amplifiers of the telephone system [95]. Today, radio frequency amplifiers adjust one or more techniques to achieve desired linearity through negative feedback. Block diagram of a simple negative feedback amplifier is shown in Figure 4.1.

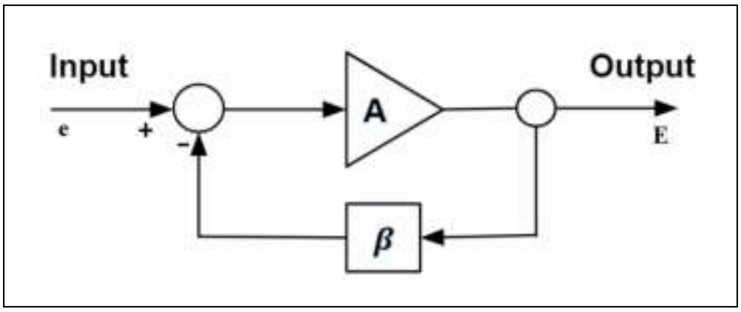


Figure 4.1. Block diagram of an amplifier with a negative feedback

As can be seen in Figure 4.1, a fraction of the output signal is sampled and reintroduced at the input. The term “negative” comes from the concept of the feedback signal being inverted in phase which is almost automatically achieved as a result of most single stage amplifiers inverting the phase of the signal. Moreover, it is required to have a voltage divider in order to control the amount of feedback desired [96].

In the absence of the feedback path, the output equation can be simply written as Equation 4.1.

$$E = eA \tag{4.1}$$

After the feedback path is designed, the amount of feedback which equals "βE" is applied to the input. The equation for the input signal turns into Equation 4.2. This applied input generates the output as Equation 4.3.

$$Input\ with\ feedback\ = e + \beta E \tag{4.2}$$

$$Output\ with\ feedback = (e + \beta E)A \tag{4.3}$$

The amplifiers' gain is defined as the ratio of output signal to its input signal. Therefore, one can simply write the gain formula as the Equation 4.4 [97].

$$Gain\ = \frac{Output\ signal\ (voltage\ or\ current)}{Input\ signal\ (voltage\ or\ current)} = \frac{A}{1 - \beta A} \tag{4.4}$$

The distortion at the output is reduced via feedback path since it is fed back to the input stage and re-amplified again and it cancels out a greater part of the distortion. The amount of distortion reduction is the same with the reduction in gain. Therefore, designers should be careful during deciding the amount of the feedback signal in the circuit since it is inversely proportional with the gain.

In the radio frequency point of view, physical dimensions tend to introduce greater phase shift at the feedback path as the frequency increases. It will lead the amplifier to be unstable if it becomes too large. Additionally, undesired feedback paths may also be present in the circuits, thus designers should take these in consideration [98]. Furthermore, the device gain has tendency to reduce in high frequencies which might cause insufficient and limited amount of feedback.

Noise is another significant factor for the amplifiers using feedback topologies as well. Each resistive feedback path acts like a noise source in the circuit which is added to the input noise. As a result, feedback can increase the noise occurring in the system. In order to compensate for this effect, there are numerous topologies which change the resistive coupling with transformer coupling although it often reduces output to input port isolation with increased risk of instability [99]. These techniques are named as “noiseless” and they have less bandwidth than resistive feedback designs. As much as transformer coupling becomes difficult during frequency increases, there might not be a problem for circuits which do not require broadband applications and are designed to operate in moderate bandwidth [100].

The following subsections of this part focuses on the various feedback topologies in electronics fundamentals and their advantages over radio frequency circuit design applications.

4.1. FEEDBACK TOPOLOGIES

This section of the thesis gives information about different feedback topologies especially used in low noise amplifier design such as resistive feedback, impedance feedback, transformer feedback and active feedback. The circuit schematics are obtained from literature reviews, there might be different design techniques based on feedback however these techniques are investigated as this thesis’s concern.

4.1.1. Resistive Feedback

In order to obtain constant input matching over a wide frequency range of operation, resistive feedback topology can be applied to design. Shunt resistive feedback is commonly used in low noise amplifier circuits. It has benefits in terms of stability performance. The resistor can be combined with a capacitance, which can be named as a RC shunt feedback in literatures. The feedback is in shunt configuration since it is parallel with the input voltage. An example for the shunt resistive feedback topology is shown in Figure 4.2.

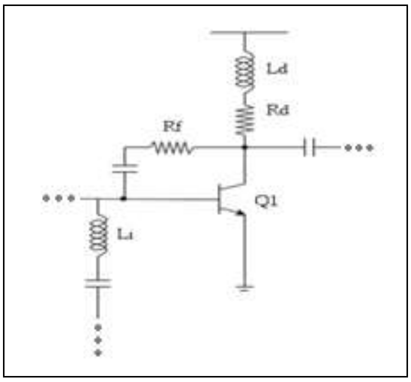


Figure 4.2. Part of a LNA design with R_f resistive feedback obtained from literature review [101]

There are several topologies that offer flat gain over a wide frequency range, however shunt resistive feedback is one step ahead by its good linearity and wideband input matching. However, feedback negatively affects the noise figure performance and degrades the maximum available power gain for an active device [102]. The feedback resistor which is in shunt configuration ensures negative feedback for the amplifier and broadband matching in the input with improved performance of stability factor.

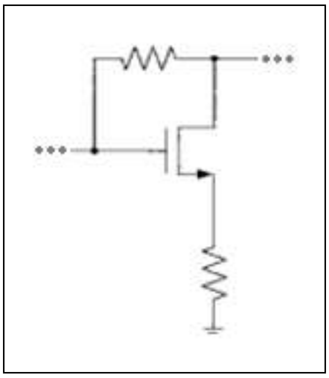


Figure 4.3. Shunt series feedback architecture

In Figure 4.3, another approach called shunt series or dual negative feedback is demonstrated for resistive feedback type. It is evident that extremely high power dissipation occurs in shunt series feedback topology compared with others yet having similar noise performance [103]. Moreover, on-chip resistors with reasonable quality are required in shunt series feedback topology which generally is not available in most CMOS technologies [104].

A parallel resistance-capacitance shunt feedback is another feedback topology option. It offers broadband input matching and reduced level of noise figure if it is combined with inductive source degeneration. An example circuitry found via literature review is shown in Figure 4.4 [105]. The literature reported that the local noise is inversely proportional with the value of R_F so that larger values of resistance would be selected in behalf of suppressing the noise.

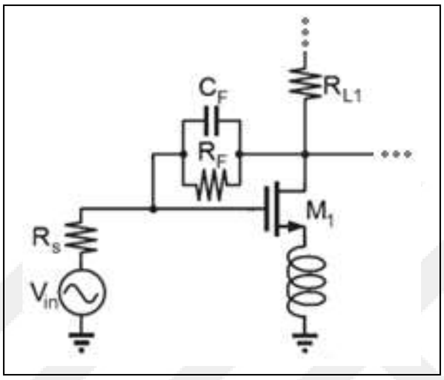


Figure 4.4. Part of a LNA design with parallel resistance-capacitance shunt feedback obtained from literature review

4.1.2. Impedance Feedback

The impedance feedback would be found as RLC feedback in the literature. It is a combined version of a resistor, a capacitor and an inductor in the series manner. Usually, it is generally introduced between gate and drain terminals of the active device. The frequency dependence in the loop is provided by the inductance [106]. The gain flatness and impedance matching can be achieved by this feedback topology. At low frequencies, resistance in the feedback loop minimizes the gain peaking and it mitigates the risk of oscillation. The exemplary schematic of a common RLC feedback topology is shown in Figure 4.5.

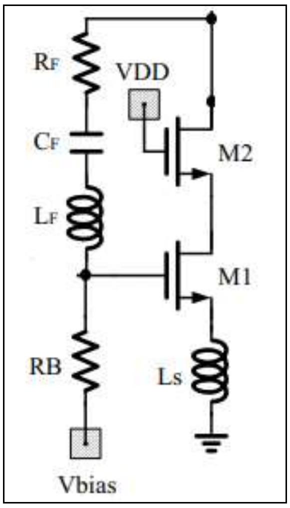


Figure 4.5. Part of a LNA design with impedance feedback technique applied [107]

4.1.3. Inductive Feedback

The passive losses and device parasitics becomes significant due to increasing in frequency and it directly degrades the gain of the cascode amplifier topologies. In order to overcome this design problem, inductive feedback technique is applied in common gate amplifiers. The literature has been reported on inductive feedback stating that common gate inductive feedback indeed increases gate to source voltage of the active device which results in better gain performance. Additionally, the extension in bandwidth, improvement in noise performance and convenience in impedance matching have been stated [108]. Figure 4.6 demonstrates an exemplary schematic of the related feedback technique.

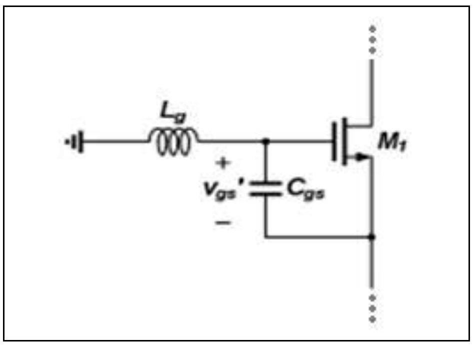


Figure 4.6. Part of a LNA design with inductive feedback technique applied [109]

In addition to the above configuration, an inductor can be placed between drain and gate terminals of the active device. This condition is named as inductive drain feedback in literature [110]. Besides overcoming limitations in bandwidth and stability, inductive feedback helps effectively reduce the noise figure in high frequencies [111].

4.1.4. Capacitive Feedback

It has been reported that resistive shunt-shunt feedback is a conventional topology for enhancing the bandwidth of an amplifier. Although, for ultra-wide band applications, its corresponding gain performance is not satisfactory. The tradeoff between bandwidth and gain performance is considerable. For this reason, capacitive feedback technique is reported as a suitable method. Moreover, capacitive feedback technique is also appropriate for multiband applications [112]. The capacitive feedback method utilizing Miller effect is supplied with ultra-wide frequency band input impedance matching. A schematic of this feedback topology is shared in Figure 4.7 from literature review.

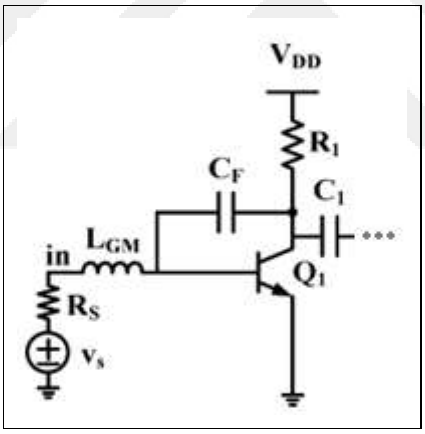


Figure 4.7. Part of a LNA design with capacitive feedback technique applied [113]

This type of feedback can be found as Miller capacitance feedback in the literature because it enlarges the capacitive effect at the input capacitance. This type of feedback also introduces less noise figure compared to others. Intentional feedback MIM capacitors can be added to designs in order to make the circuit less prone with the process variations [114]. In addition, capacitive feedback technique can be used as a tool for simultaneous noise and power match in the circuits with inductively source degenerated besides improvement in stability [115].

4.1.5. Transformer Feedback

On the block diagram given below, feedback circuit β is a transformer. The output current of A_{OL} is sampled by the secondary windings of the transformer. Then, current is induced at the first winding and introduced back at the input. From the radio frequency point of view, this technique has difficulties over stability and noise performance [116]. A block diagram example of a transformer feedback is demonstrated in Figure 4.8.

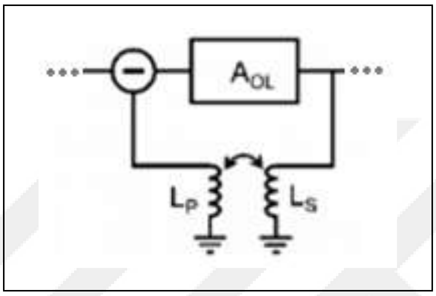


Figure 4.8. Feedback circuit based on transformers

A conventional method for shunt-series transformer feedback for amplifiers is shown in Figure 4.9. The gate of the input transistor M_1 is having a parallel connected inductor L_1 while the second coil L_2 is placed series at the source terminal. The negative feedback is assured since the coil's polarities are opposite to each other. The literature stated that the transformer feedback technique introduces less noise compared with the resistive and active feedback. In contrast, it costs more chip area [117].

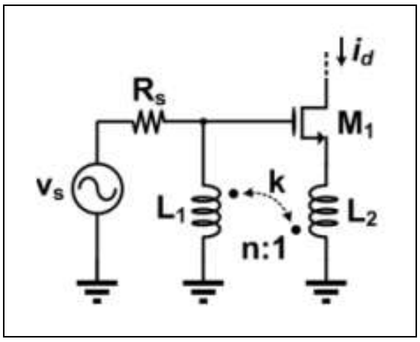


Figure 4.9. Shunt-series transformer feedback topology [118]

In circuit design, the transistor M_1 is desired to have a large gm_1 in order to minimize the noise figure. However, increase in the turn ratio of the transformer required with the increase in gm_1 transconductance in order to achieve good input matching performance. Due to having physical limitations, the turn ratio of the coil might not be too large [119].

4.1.6. Active Feedback

For ultra-low power low noise amplifier designs, input matching network is one of the main difficulties with the available power budget. Low noise amplifier topologies are divided into two categories based on the input stage, such as common gate and common source. For common source architecture, the most common matching technique is inductive degeneration and a LC network is required at the input. This might lead to a high number of bulky inductors on chips in some low noise amplifier designs [120]. The input matching constraints determine the g_m of the topology so that it might not be reduced for lower power consumption. The tradeoffs between noise and gain with the input matching generally exhibits high power consumption in traditional resistive feedback technique [121]. However, using active feedback supplies good performance in common source low noise amplifiers but it also causes high power consumption.

Another approach for low noise amplifier design is using common gate topology which exhibits a good input matching performance over a wide frequency range. Moreover, reverse isolation and stability performance is better compared with the common source transistors due to absence of the Miller effect with the cost of higher noise figure [122]. The consumed power in the feedback stage should be considered in ultra-low power applications. The example of this common source active feedback topology is shown in Figure 4.10.

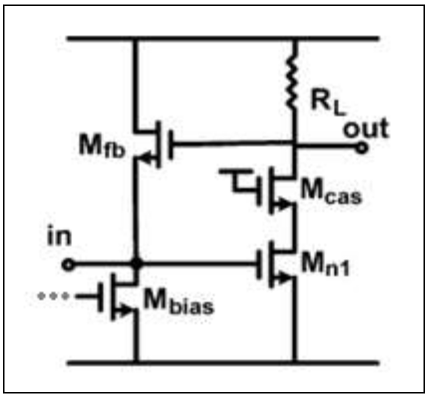


Figure 4.10. Part of a CS LNA design with active feedback technique applied [123]

The gain roll-off at high frequencies degrades the input matching performance since the feedback signal is taken from the output node that has relatively narrow bandwidth and high gain. The large signal swings are driven at the output and for this reason nonlinear feedback transistor M_{fb} can severely degrade the linearity of the low noise amplifier [124].

There are countless ways that feedback techniques are applied in the low noise amplifier designs. Not only mentioned topologies have been used in the designs, there are a variety of different applications that take place in literature. However, these topologies are basilar in circuit design level.

4.2. COMPARISON BETWEEN DIFFERENT FEEDBACK TYPES USED IN LOW NOISE AMPLIFIER DESIGNS

Feedback is one superior tool in electronics. It is an obligatory process to select appropriate feedback topology and investigate advantages or disadvantages of each feedback technique separately. In electronics, feedback provides advantages over bandwidth, stability and linearity with the risks of degraded noise figure performance, higher power consumption or high chip area. It is also worth mentioning that there are many other feedback techniques that are covered in the literature such as noiseless feedback, frequency dependent feedback loop (FDFL) technique [125]. However, they have the similar design methodology fundamentals and combinations or improvements of the existing feedback types.

Table 4.1 aims to give a general perspective over the different feedback techniques studying low noise amplifiers with the same process, which is GaAs 0.15-µm pHEMT. Only references for the first inductive and capacitive feedback topologies belong to GaAs 0.25-µm pHEMT process.

Table 4.1. Comparison table for different feedback topologies

References	**Feedback Type**	**Stage**	**Frequency (GHz)**	**Gain (dB)**	**NF (dB)**	**S_{11} (dB)**
[126]	Resistive feedback	3	1.5 – 8	21	1.5	-15
[127]	Resistive feedback	2	3.1 – 10.6	13	3.4	-12
[128]	Inductive feedback	2	5.5 – 8	16	0.88	<-10
[129]	Inductive feedback	3	3.2 – 14.7	34	1.3	<-5
[130]	Capacitive feedback	2	2 - 4	32.1	0.8 – 2	< 0
[131]	Impedance feedback	4	2.5 - 31	33.5	1.6	< -10
[132]	Transformer feedback	2	2 – 39.5	19.2	2.3 - 4	< -5

In addition, to the author's best knowledge, there is not any literature reported for active feedback topology in GaAs pHEMT processes. For this type of feedback, the most common process selected by the designers is CMOS technology [133]. In this thesis work, switching transistors are placed at the feedback paths in order to combine active feedback topology with impedance feedback characteristics. The aim of this selection is to increase stability while controlling the operating frequency band.

5. DESIGN TECHNIQUES COMMONLY USED IN LOW NOISE AMPLIFIERS

In this section of the thesis, some useful methodologies named as the inductive degeneration, the inductive peaking, diode connected load, self-biasing and current reuse which are generally adapted in low noise amplifier designs are briefly mentioned. The tradeoffs between whether selecting to adapt these techniques in design is also explained.

5.1. THE INDUCTIVE DEGENERATION METHOD

The inductive degeneration or inductive source degeneration is a widely used design methodology in amplifier designs because of its superior benefits over impedance matching besides with gain and optimum noise performance. In literature, the inductive degeneration method is reported as a good input impedance matching tool for low noise amplifier architectures [134]. In addition, it allows maximum gain under minimum noise contribution with reasonably low power. In Figure 5.1, a simple schematic diagram for inductive source degeneration is represented.

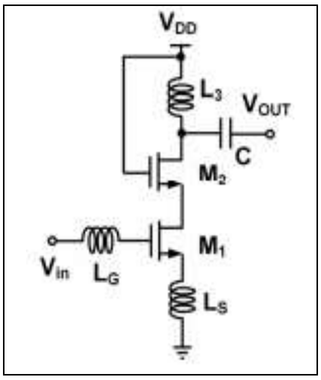


Figure 5.1. Cascode LNA configuration with inductive degeneration [135]

In cascode topologies, the literature states that transistors with inductive degeneration have the best isolation with benefits of low noise and convenience in matching [136]. Therefore especially in cascode low noise amplifier designs, inductive source degeneration is one of the most widespread methods for its advantages over high reverse isolation, low noise figure and good input-output impedance matching convenience with contributions on circuit stability [137].

5.2. THE INDUCTIVE PEAKING TECHNIQUE

In order to achieve broadband matching and high gain performance with operating bandwidth extension, inductive peaking is another practical tool for low noise amplifier designs. If inductive peaking is applied to the gate of the transistor, it is called gate inductive peaking technique in the literature. An exemplary circuit schematic for gate inductive peaking is shown in Figure 5.2.

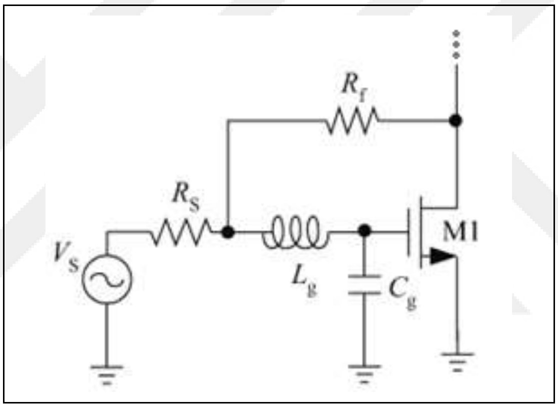


Figure 5.2. Cascode amplifier with the gate inductive peaking technique [138]

For enhancing the 3-dB bandwidth of an amplifier, a commonly used method is the inductor shunt peaking which adds an inductor in series with the load resistor. This method uses an inductor placed at the drain of the transistor, which results in a great deal of area. However in gate inductive peaking technique, an inductor is placed at the gate of the input transistor. In literature, it is stated that gate inductive peaking technique uses a much smaller inductor with the same bandwidth enhancement compared to the inductor shunt peaking [139].

Experimental studies for a low noise amplifier having common source configuration with a variety of inductive peaking techniques stated that, series peaking and shunt-series peaking methods are more efficient in bandwidth enhancement for an amplifier compared with the inductive shunt peaking technique [140]. Another advantage of the using gate inductive peaking is its superior performance for enhancing high frequency gain with the flatness. The inductive peaking technique is also applied for canceling the parasitic capacitances.

5.3. THE DIODE CONNECTED LOAD TECHNIQUE

Another studied method for low noise amplifiers is diode connected load applications. In literature review, it is learned that a common source amplifier with a diode connected load has a high input-referred third order intercept point (IIP3) since the nonlinearity of the common source input transistor is corrected by the diode connected load [141]. This technique has another advantage, which is that the overall noise of the circuit is reduced. In order to maximize input-referred third order intercept point by the post linearization, the optimum sizes of transistors for the diode connected loads should be selected. While partially compensating the gain reduction, diode connected transistors with a resistor or capacitor increase the linearity performance significantly [142].

Another reason for selecting diode connected load technique in most designs is the difficulty in fabricating resistors with high values or a reasonable physical size in many CMOS technologies [143]. Therefore, it is desirable to exchange a resistor with a MOS transistor. In Figure 5.3, a schematic representation for the diode connected load for NMOS and PMOS devices is demonstrated.

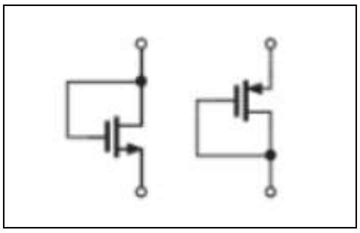


Figure 5.3. Diode connected NMOS and PMOS transistor representation

5.4. THE SELF BIASING METHOD

In the perspective of area and power saving, self-biasing technique is a key feature for designers. The tradeoff of bias circuitry is commonly reported as noise contribution in the literature [144]. The need for a bias network for each stage of the amplifiers would be totally removed if self-biasing networks are managed to design properly while meeting other specification requirements in the circuit. In literature review, it is observed that self-biasing networks may not be only used as a tool of power and area saving, they can also be adapted for input and output matching networks for convenience in matching [145].

For the cascode amplifier topologies, the self-biasing networks are able to be designed simply by a feedback resistor through a transistor [146]. In contrast, self-biasing network designs are a great deal for considering tradeoffs between power consumption, area requirements, and noise contributions. It is also reported that, since the need for multiple biasing networks does not exist, the noise performance can be improved by using less biasing networks combined with the self-biasing networks thanks to this technique. There are more complicated ways for constructing self-biasing networks, for example inserting a series inductor, continued with a parallel RC to ground. The drain current flows through the resistors and these resistors are selected properly to provide positive DC voltages at source terminals [147]. In Figure 5.4, an example for a self-biasing network is demonstrated for a pHEMT transistor.

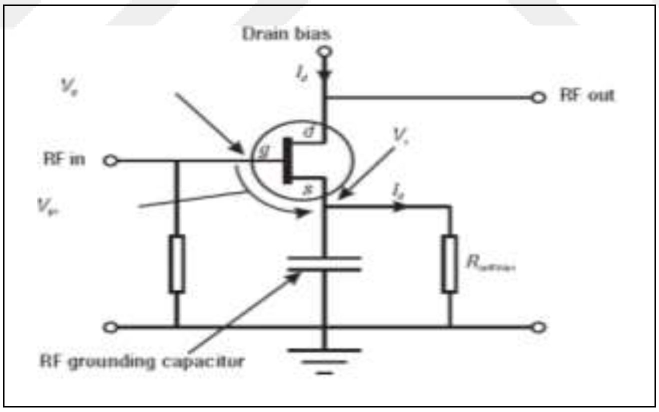


Figure 5.4. Self-biasing of a pHEMT transistor [148]

In the figure above, at the gate of the transistor, self-biasing networks remove the need for negative bias voltage supply and it allows the transistor to be biased by using a single bias supply on the drain. The placement of a resistor in the DC path from source to ground results in DC coupling the gate ground. If the drain-source current flowing through the resistor starts to increase, it raises the voltage at the source terminal to a positive voltage which makes V_{gs} more negative valued voltage.

In literature, generally two drawbacks of self-biasing technique are stated, firstly since the bias current is fixed to a value and it cannot be changed externally without affecting the drain voltage. Secondly, careful control must be done about the self-bias resistor value since the bias point is a function of it.

In conclusion, structures may differ from each other based on the selected technologies for self-biasing circuit designs. Not only the mentioned structures, but also there are a variety of options reported for self-biasing networks in the literature. However, the main idea behind this technique is reducing the power consumption while minimizing the chip area while obtaining the reasonable noise performance behavior in the low noise amplifier design.

5.5. THE CURRENT REUSE TECHNIQUE

Since DC power consumption is a big concern for designers, the current reuse method has been introduced to meet the requirements. The current reuse technique supplies multistage radio frequency performance with a single stage DC power consumption [149]. As a result of DC bias current being cycled through multi stages of the design under a single supply voltage, this method provides a higher gain-bandwidth product with lower current and power consumption.

The inductively source degeneration with current reuse technique are successfully combined together in low noise amplifier designs, however it might have a narrowband input matching capability to 50Ω if not be carefully designed. Additionally, the distributed amplifiers have wideband characteristics but they tend to dissipate large DC current and have poor noise performance. As a result, for solving the problem of power consumption and reducing the number of external bias voltages, the current reuse technique has been introduced in literature [150].

Another advantage of the current reuse configuration is in linearity performance. Besides having low noise figure and good gain properties, the current reuse method can be applied for high linearity purposes [151]. One option of having a current reused amplifier shown in Figure 5.5.

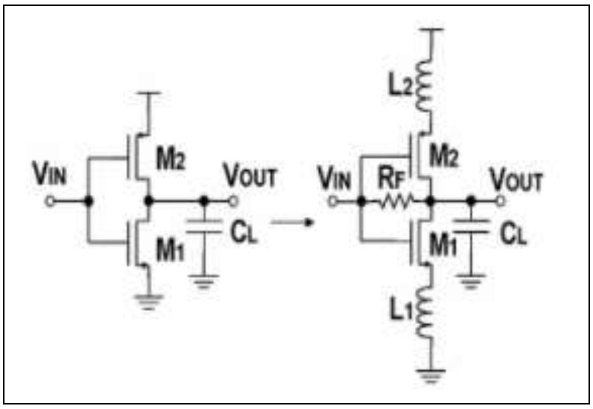


Figure 5.5. An example of current reuse configuration applied amplifier [152]

In the figure above, this amplifier topology has been disregarded for having high input impedance. Therefore, contributions have been made by the designers so that the addition of resistive feedback and inductive source degeneration to this topology provides very wideband matching [153].

In conclusion, there is not one specific configuration type for current reuse topology in literature which means that there are countless ways of adapting this technique to low noise amplifier designs. It can be said that the limit is set by the designer’s flexibility in chip area or other considerations. However, this technique offers indeed low power consumption with low noise contribution while supplying good linearity performance.

6. LOW NOISE AMPLIFIER CONCEPT

In a typical microwave receiver system, a low noise amplifier is the first active stage. Amplifiers are the very first stage in the receiving chain and get a weak electric signal from the antenna. In addition to the weak signal, strong interfering signals might also be present in the system. Therefore, care should be given while designing a low noise amplifier since its noise and gain performance affect the overall receiver's noise figure [154]. In general, main considerations for designing a low noise amplifier are minimizing the noise figure of the system while providing desired gain with sufficient linearity, input impedance to be ensured at stable 50Ω with low power dissipation at the same time.

6.1. FREQUENCY APPLICATIONS

The very first low noise amplifiers were designed to operate in a single frequency. However, due to the increased demand in more flexible electronic appliances made the requirement for several different frequency bands of operations.

There has been a great deal of evolution in the software and hardware areas in the wired or wireless telecommunication systems sector in the past two decades. In order to keep up with the advancements in wireless standards and accelerated developments in cellular phone technologies, there occurred a place which continuously developed in the wireless market. Generally, wideband or multi band low noise amplifiers are designed for common receiver architectures [155]. For a solution of the requirement for more than one operating frequency band, designers worked on combining multiple single band low noise amplifiers in the receiver architectures. However, an architecture which has multiple single band low noise amplifiers increases the packaging cost significantly and it requires a larger silicon footprint which also results in higher cost. Therefore, design of a dual band or multiband low noise amplifier is an interesting context because they can support multi standard operations. The noise figure and chip area optimization with respect to matching network design is a challenging task for these studies.

For example, it was reported in literature that, in order to reduce the silicon cost in 5G front-ends broadband or multiband operations are quite important because depending on the actual region of operation, different bands should be covered. It was stated that single band 5G front-ends are only able to work on a subset of the possible regions [156].

There are countless ways of design techniques reported for increasing the flexibility in the low noise amplifier concept. In recent years, quad-band or even more multiband of low noise amplifier articles reported in the literature [157]. Based on the limitations or required specifications, low noise amplifiers can be designed to operate on multi frequency bands either simultaneously or separately. For example, if a dual band low noise amplifier is able to operate at its two different frequencies at the same time, this type of frequency operation is called concurrent dual band. The concurrent dual band low noise amplifiers have the advantage of no requirement for the separate mode control switch for channel selection [158].

As previously mentioned, for extending the communication system functionalities multi band or dual band transceivers have emerged. Wireless local area networks (WLANs) are used widely in houses and offices for providing high data rate and multi standard receivers. Therefore, it is a necessity for a RF front-end receiver to support multi standard, multi band applications. For being the first active stage of the receiver chain, low noise amplifiers determine the overall dual band receiver performance [159].

In conclusion, the idea of concurrent dual band operation combined with the two different single band frequencies is an inspiring motive for this thesis work. To the author's best knowledge, there are no other low noise amplifier designs reported which combine both concurrent dual band and separate single band frequency applications.

6.2. LOW NOISE AMPLIFIER TOPOLOGIES

The first stage in the receiver chain of a communication system is the low noise amplifier. The low noise amplifier is directly connected to the antenna, therefore it plays a crucial role for determining overall noise figure performance of the system. The low noise amplifiers are designed to amplify the very weak signal which comes from the antenna while minimizing the possible noise addition. Since noise figure is an important design parameter with tradeoffs between other design parameters namely third order input intercept point (IIP3), power consumption and gain.

There exists a variety of low noise amplifier topologies for different applications. The selected topologies and added elements may vary based on specified usage area such as military applications, wireless communication system applications etc. This chapter of the thesis aims to examine fundamental structures combined with different methods in usage.

6.2.1. Cascode Amplifier Topology

During the literature review phase, it was observed that one of the most commonly used low noise amplifier topologies is cascode amplifier with inductive source degeneration [160]. Because the cascode transistor is in the same type as the input transistor, this kind of cascode amplifier is also named as a telescopic cascode amplifier in literature. In contrast, for the folded cascode amplifier topology, the cascode transistor is in the different type with the input transistor [161]. In the folded cascode topology, the NMOS and PMOS transistors are placed parallel between the supply and ground rail and they are able to operate at lower supply voltages compared with the telescopic cascode amplifiers.

It is known that cascode topology has higher gain due to increased value of the output impedance. This topology ensures better isolation between input and output ports. In addition, cascode topology may effectively reduce the Miller effect. The good reverse isolation also provides better stability performance [162].

The noise source of the cascode transistor is degenerated by the lower transistor’s output impedance in lower bands of microwave frequencies [163]. Consequently, the superior noise performance is obtained by the cascode stage. However, noise and gain performance degrades in high frequencies because the substrate parasitic admittance at the drain-source nodes increases as the frequency increases [164].

The cascode stage is also proper for narrowband applications like the common source stage. Although, using proper feedback techniques make cascode amplifier topology proper for the multi band or wide band applications. Another way of using cascode amplifier topology for wide band application is designing complicated LC matching networks in the input [165].

To conclude, cascode amplifiers provide high gain, good isolation between the ports and reduction of the Miller capacitance on lower transistors. When cascode topology is applied as a common source configuration, it provides high gain, wideband matching and low noise figure performance.

6.2.2. Cascade Amplifier Topology

A commonly used low noise amplifier circuit topology for achieving high input impedance, higher gain and low noise figure is the cascade structure. For cascaded radio frequency components, the noise figure of the system can be calculated thanks to the Friss equation if the noise figure and gain of each stage is known. The Friss equation is given by Equation 6.1 [166].

$$NF_{Total} = NF_1 + \frac{(NF_2 - 1)}{G_1} + \frac{(NF_3 - 1)}{G_1 G_2} + \cdots \tag{6.1}$$

In the above equation, NF_{Total} is the equivalent noise figure of the amplifiers cascaded together, NF_i is the noise figure of the i^{th} stage, and G_i is the gain of the i^{th} stage. This equation implies that the noise figure of the very first stage of a cascaded amplifier directly affects the overall system's noise figure performance. It can be stated that the later block contributes less to the noise figure if they preceded with the gain performance. Therefore, it is crucial for the first stage of the amplification to have low noise figure performance.

In terms of gain and noise performance, common source or cascade is a widely used technology. In literature review, it is learned that cascade amplifier topology has drawbacks of low linearity however this topology can be combined with linearity boosting techniques to overcome this situation. The cascade low noise amplifiers have difficulties with the impedance match between two same modules and stability after the cascade stage [167].

Moreover, combining the cascode topology with cascaded techniques ensures higher gain since the increase in the output impedance together with wider bandwidth and better isolation between input and output ports of the designs [168]. In Figure 6.1, a schematically represented version of the cascode and cascade topologies for the DC and signal path is shown.

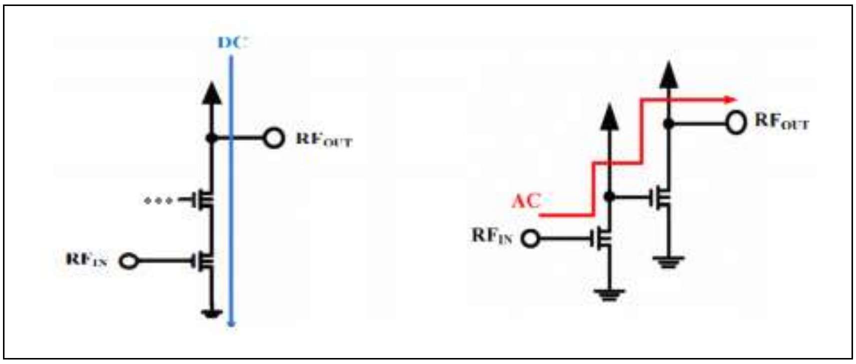


Figure 6.1 Schematic representations for the cascode and cascade amplifier topologies [169]

6.2.3. Common Gate versus Common Source Topology Comparison

There are several design considerations that make one topology superior on another based on the applications. In particular, common gate and common source amplifier topologies are usually compared with each other for radio frequency applications. The benefits or disadvantages over each other are studied in the literature. The transistors having common emitter or common source configuration have high input and output impedance whereas common base or common gate features have the lowest input impedance and highest output impedance [170].

The low noise amplifiers with common source configuration are known to have good noise performance and high gain. The common gate configuration provides robustness against parasitics and ensures a more stable circuit with low power consumption. It stated in the literature that a g_m boosted common gate low noise amplifier draws less current than common source counterpart but common gate supplies a moderate gain around 10 dB which is not suitable or sufficient for applications which require high gain, around more than 15 dB [171]. However, common gate structure can easily achieve the input impedance matching but it degrades by weak noise performance [172]. Therefore, wideband input matching is more convenient for common gate configuration therefore this topology is generally used for broadband low noise amplifier designs. In addition, the common source configuration can also be used for broadband designs with special matching and feedback techniques [173].

6.2.4. Single Stage versus Multistage Amplification Comparison

The low noise amplifier designs with single stage amplifications offer less gain compared with the multi stage amplification. However in the literature, it is reported that the noise performance of the multi stage low noise amplifier is not degraded since the noise is mainly determined by the first stage, as mentioned in the Friis equation [174].

Based on the Friis equation, high gain for the low noise amplifier is crucial for reducing the noise contribution to the mixer or following blocks in the receiver front end. Consequently, high performance receivers can be designed with the multi stage low noise amplifier methodology [175]. As an outcome disadvantage, two or more staged low noise amplifiers require high consumption of the DC power, therefore there may be a need for power reduction techniques for these designs in order to be suitable for low power applications.

7. DESIGN AND SIMULATION RESULTS OF THE LOW NOISE AMPLIFIER

In this section, the proposed low noise amplifier design is explained with circuit design techniques used in detail. The low noise amplifier topology and acquired schematic and EM simulation results are stated. For clarifying the modes of operation, signal path analysis for the RF signal is also demonstrated.

7.1. PROPOSED LOW NOISE AMPLIFIER CIRCUIT

As in the first step of the low noise amplifier circuit design, the circuit topologies and various design techniques were studied in order to meet the required specifications. After the literature review, it was decided that cascade topology could provide high gain, narrow bandwidth and low noise requirements of the proposed design.

In Figure 7.1, the schematic view of a simplified version of the constructed low noise amplifier circuit in AWR design environment is shown. As can be seen in that figure, transistors of Q1, Q2 and Q3 are connected as cascade topology.

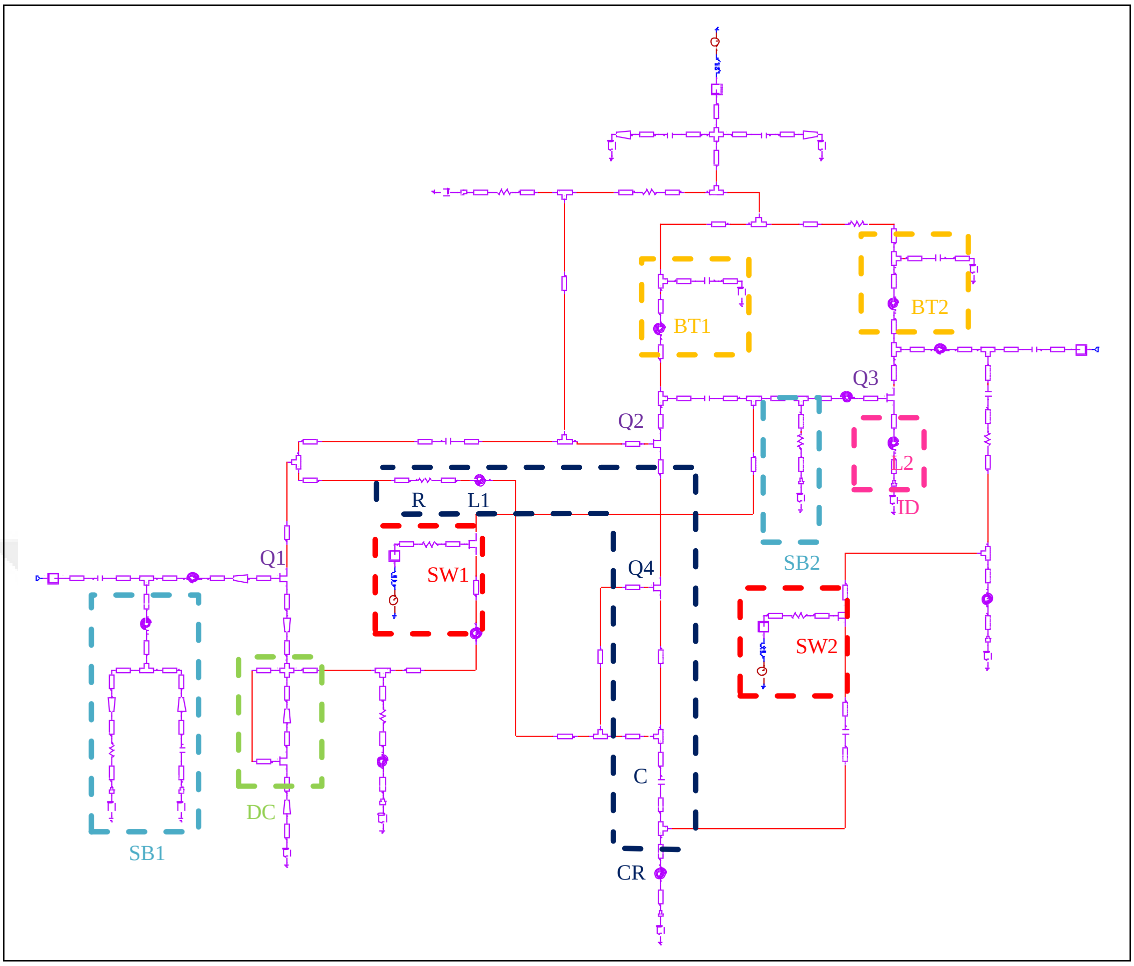


Figure 7.1. Schematic view of the low noise amplifier design

As mentioned earlier, generally the low noise amplifier designs with multiple bands of operation suffer from relatively high power consumption and noise figure performance degradation. To overcome these issues, the current reuse and self-biasing techniques were applied to the design.

In Figure 7.1, the dark blue path which is abbreviated as “CR” stands for the current reuse part of the circuit. The direct current enters the drain of the transistor Q2 and continues from this transistor’s source to ground. However, the coupling capacitor (C) below blocks the current from reaching the ground. Therefore, the direct current must flow through the drain of the transistor Q1. In addition, there are resistor (R) and inductor (L1) used in this current reuse path to ensure the minimum possibility of RF leakage by their impedance value. The optimum values for R and L1 were selected by considering the amount of direct current not degraded by the value of the resistance and the inductance of the inductor is limited by the size consideration. In the current reuse path, the gate-source shorted transistor (Q4) is also used. The gate-source shorted transistor operates above the threshold voltage since all transistors were selected in depletion mode type. Since the v_{gs} becomes constantly zero, the RF signal cannot flow through that transistor. All in all, there is no need for additional DC supply for transistor Q1 with the help of this current reuse method and this results in the reduced amount of power consumption for this design.

Another technique for reducing power consumption is the self-biasing method. In Figure 7.1, the self-biasing sections of the design are highlighted in light blue color, abbreviated as “SB1” and “SB2”. By this technique, it is aimed to keep the value of the transistor’s gate voltages in zero level since this value is still above the threshold voltage of the transistors and it is close to the maximum value for the g_m parameter.

The SB1 path involves an inductance and parallel resistor and capacitor instead of SB2 path. The reason is that, SB1 path not only provides self-biasing conditions but also helps the input matching of the design for 2.4 GHz and 5.8 GHz frequency cases. Both resistors used in the SB1 and SB2 paths are selected to have high impedance to prevent the RF signal flowing to the ground.

For noise figure performance enhancement, the diode connected configuration is used and it is remarked in green color in Figure 7.1, abbreviated as “DC” on the figure. This technique also provides superior performance in linearity perspective and improvement on the input 1 dB compression point (P1dB) value.

The inductively source degeneration method is highlighted in pink color in Figure 7.1, it is abbreviated as “ID” on the figure. The inductor in this path helps output matching with advantages in degraded noise figure and improved gain and stability performance.

The bias tee paths are emphasized in orange color in Figure 7.1 and abbreviated as “BT1” and “BT2” on the figure. These paths contain inductor and capacitor, the main objective of these paths is to separate the DC source and RF signal.

The last but not the least, the switching parts are remarked in red color in Figure 7.1, they are abbreviated as “SW1” and “SW2” on the figure. The switches control the mode of frequency operation, which will be discussed in detail in the following subsection of the thesis. The final layout view of the proposed low noise amplifier design is demonstrated in Figure 7.2.

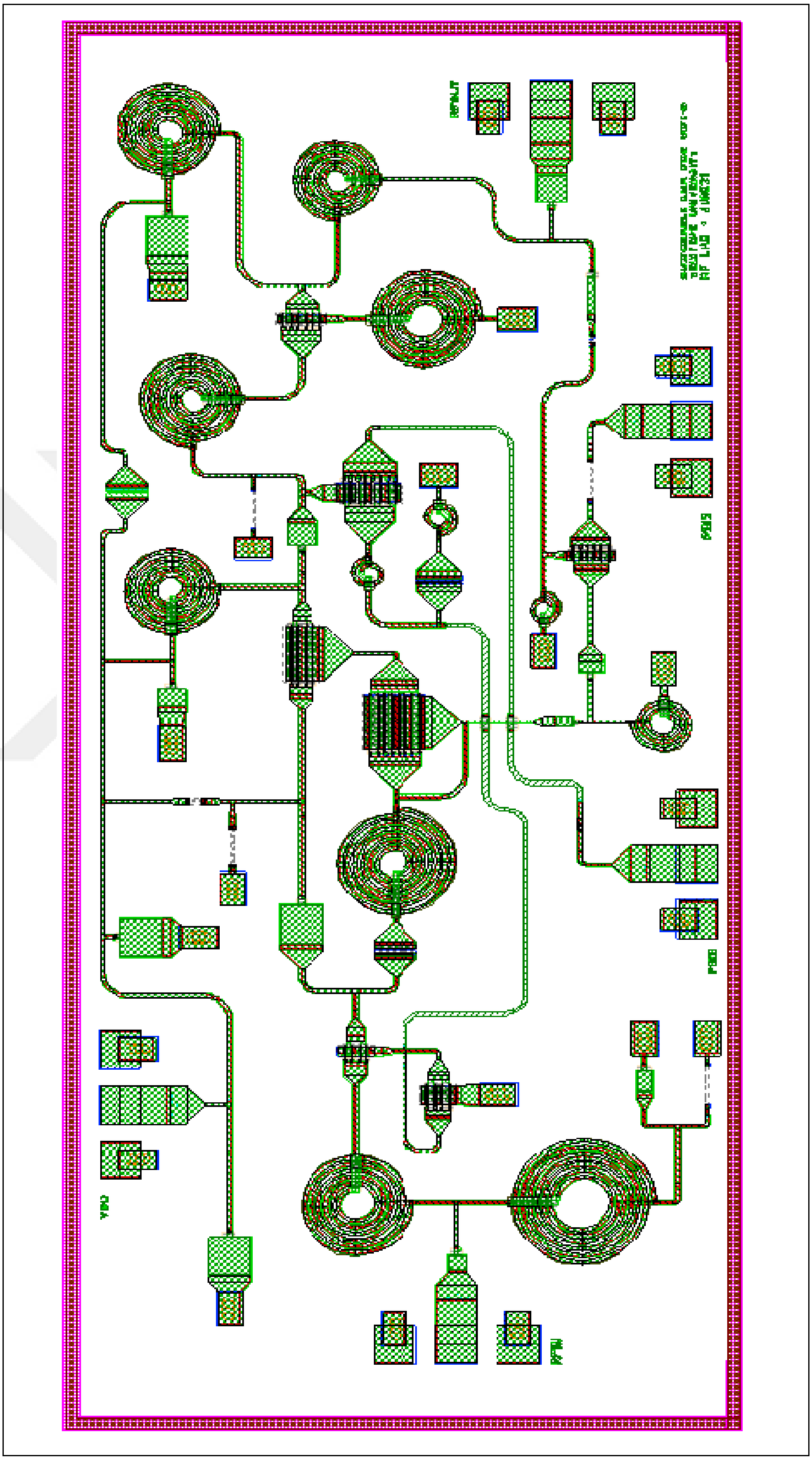


Figure 7.2. The final layout view of the designed chip (3.4x1.5 mm^2)

7.2. SIMPLIFIED SIGNAL PATH VIEW

The proposed low noise amplifier has three modes for frequency operation which are single 2.4 GHz, single 5.8 GHz and concurrent dual band that operates at 2.4 GHz and 5.8 GHz simultaneously, where they are named as Case 1, Case 2 and Case 3, respectively. These modes can be selected via two switch transistors whose DC supplies are controlled with remarked pins as “PIN1” and “PIN2” voltages in Figure 7.3. The differences in PIN1 and PIN2 voltages determine the modes of frequency operation for the low noise amplifier. These three different frequency cases denoted in Table 7.1.

Table 7.1. Controlling voltages for the different frequency cases

	Case 1 (2.4 GHz)	**Case 2 (5.8 GHz)**	**Case 3 (Dual Band)**
PIN1	-3.3V	0 V	-3.3V
PIN2	0 V	-3.3V	-3.3V

There are two different voltage values that can be applied to the pins, which are 0 V and -3.3 V. The situation when both controlling pins are applied to 0 V is considered as switch off mode, this means that the switch transistor is able to flow RF signal on it. On the other hand, if -3.3 V is applied to both controlling pins, this mode is considered as switch on mode, meaning that the switch transistors have high r_{ds} impedance so that they block flowing RF signal on it.

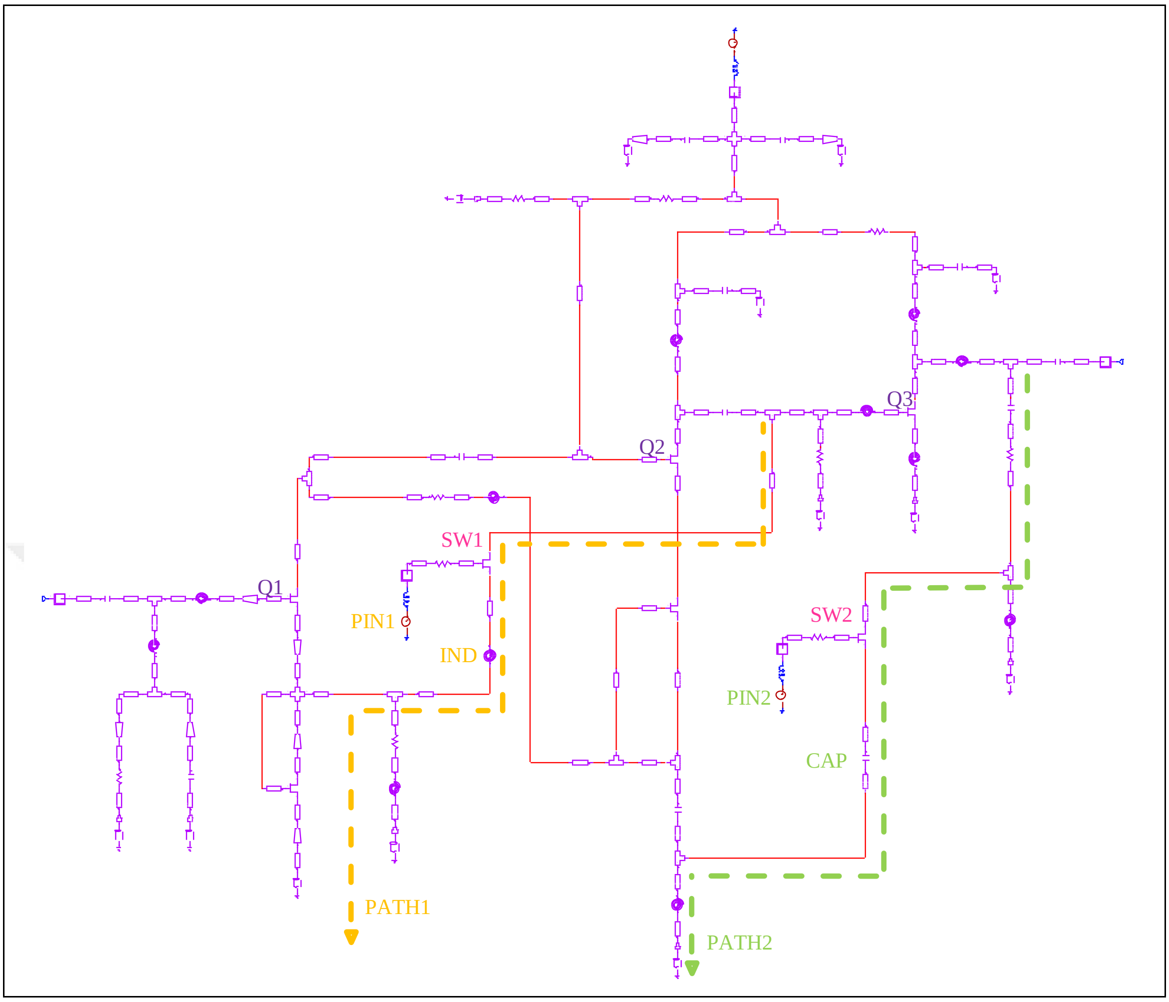


Figure 7.3. Signal path view of the low noise amplifier design

In Figure 7.3, the RF switching paths are demonstrated in orange and green colors. For the first case which is single 2.4 GHz frequency operation, PIN1 is supplied with -3.3 V and PIN2 is supplied with 0 V. Therefore as previously mentioned, SW1 is in switch on state and SW2 is in switch off state for single 2.4 GHz application. The applied RF signal from the input port is amplified via transistors Q1, Q2 and Q3. Since the controlling switch transistor in the orange signal path is in switch on state, the amplified RF signal cannot flow through it. In contrast, the controlling switch transistor in the green signal path is in the switch off state, which causes a ground path for the RF signal. However, the capacitor used in the green signal path (CAP) is selected as a high impedance value for 2.4 GHz RF signal instead of 5.8 GHz RF signal. Thus, the 5.8 GHz RF signal can be separated from 2.4 GHz and flow through the ground. In the end, the amplified single 2.4 GHz RF signal is obtained at the output port.

For the second case which is single 5.8 GHz frequency operation, PIN1 is supplied with 0 V and PIN2 is supplied with -3.3 V. In this case, SW1 is in switch off state and SW2 is in switch on state for single 5.8 GHz application. With the same logic, the applied RF signal from the input port is amplified via transistors Q1 and Q2. Because the controlling switch transistor in the orange signal path is in switch off state, this causes a ground path for RF signal. Nevertheless, the inductor in the orange path has a high impedance value for the 5.8 GHz RF signal instead of 2.4 GHz RF signal. Therefore, the 2.4 GHz RF signal can be distinguished from 5.8 GHz and flow through the ground. In contrast, the controlling switch transistor in the green path is in switch on state for this condition. Finally, the amplified single 5.8 GHz RF signal is obtained at the output port after the amplification at transistor Q3.

The last case which is concurrent dual band applications for both 2.4 GHz and 5.8 GHz simultaneously, both PIN1 and PIN2 are supplied with -3.3 V. For this case, both SW1 and SW2 are in switch on state. Due to this reason, two feedback paths containing switch transistors are unable to flow RF signal towards ground. Hereby, both 2.4 GHz and 5.8 GHz RF signals cannot be extinguished on these paths. At the output port, both 2.4 GHz and 5.8 GHz RF signals amplified via transistors Q1, Q2 and Q3 can be acquired.

Since this thesis work contains two controlling switches, there are actually four different cases for each control voltages. The unnamed condition, which was not involved for the specifications of the thesis, can be called bypass mode. This time, both control pins are supplied with 0 V. Therefore, both signal paths are in switch off state which causes attenuation of the 2.4 GHz and 5.8 GHz RF signal simultaneously. This condition for the frequency operation is also considered as a future work for this thesis.

7.3. SIMULATION RESULTS

The following subsections of this part of the thesis give information about the simulation results for both schematic and EM with the differences between them. The proposed low noise amplifier results were tested in the AWR design environment.

7.3.1. Schematic Simulation Results

Firstly, schematic simulation results for the proposed low noise amplifier are analyzed in the thesis studies. Schematic simulation results with respect to scattering parameters, noise figure, 1 dB compression point and stability are stated. The simulation results for 2.4 GHz, 5.8 GHz and concurrent dual band are given separately. After achieving the desired specifications for the proposed low noise amplifier design, an EM simulation tool for the AWR design environment was used for testing the reliability of the obtained results.

7.3.1.1. Scattering Parameters

As mentioned in section 3.1.5 of the thesis, scattering parameters are one of the most deterministic specifications for the low noise amplifier performance. It demonstrates the gain, input and output matching and finally the isolation between the ports. In Figure 7.4, schematic s-parameter results for the single 2.4 GHz case are shared.

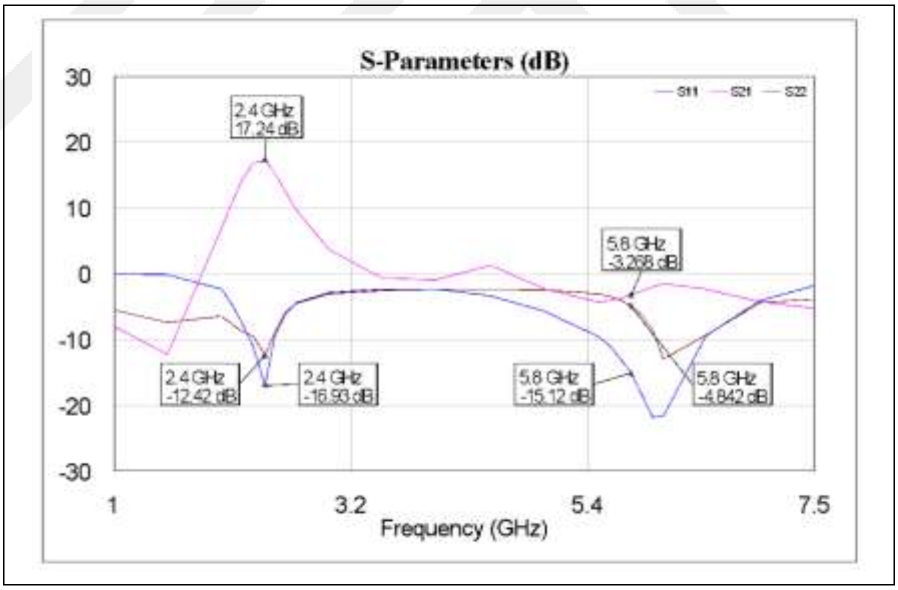


Figure 7.4. Scattering parameter results for the single 2.4 GHz case

For the single 2.4 GHz case, the proposed low noise amplifier has a gain of 17.24 dB while input and output matching results are -16.93 dB and -12.42 dB respectively. For this case, the low noise amplifier is designed to operate specifically at 2.4 GHz, therefore the gain and matching results are degraded for 5.8 GHz. In Figure 7.5, schematic s-parameter results of the single 5.8 GHz case is demonstrated.

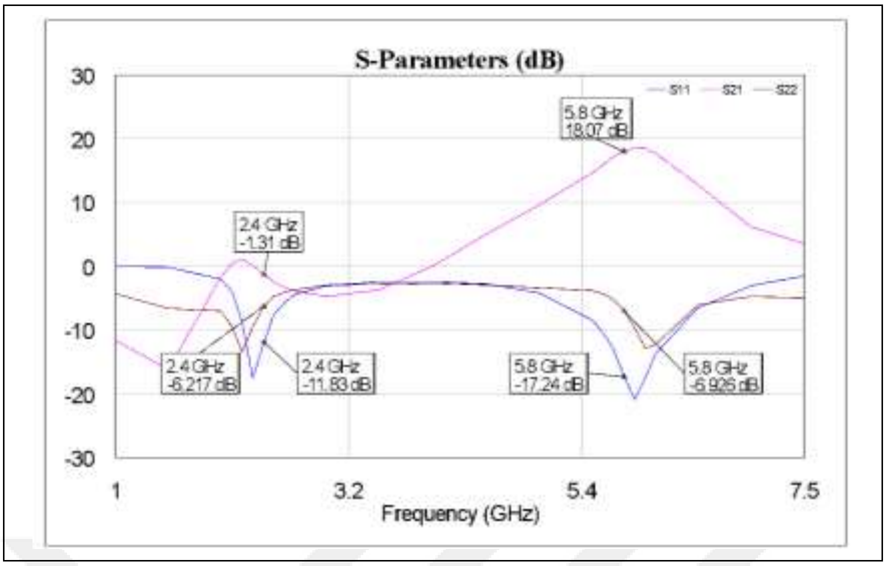


Figure 7.5. Scattering parameter results for the single 5.8 GHz case

For the single 5.8 GHz case, the proposed low noise amplifier has 18.07 dB gain and input and output matchings are -17.24 dB and -6.92 dB respectively. In contrast with the previously mentioned condition, for the single 5.8 GHz case, the low noise amplifier is designed to operate only at 5.8 GHz frequency band hence the gain and matching results are suppressed in order not to the low noise amplifier works on 2.4 GHz frequency band.

The last case which is a concurrent dual band application covers the frequency bands of 2.4 GHz and 5.8 GHz simultaneously. The scattering parameter results for the concurrent dual band case is given in Figure 7.6.

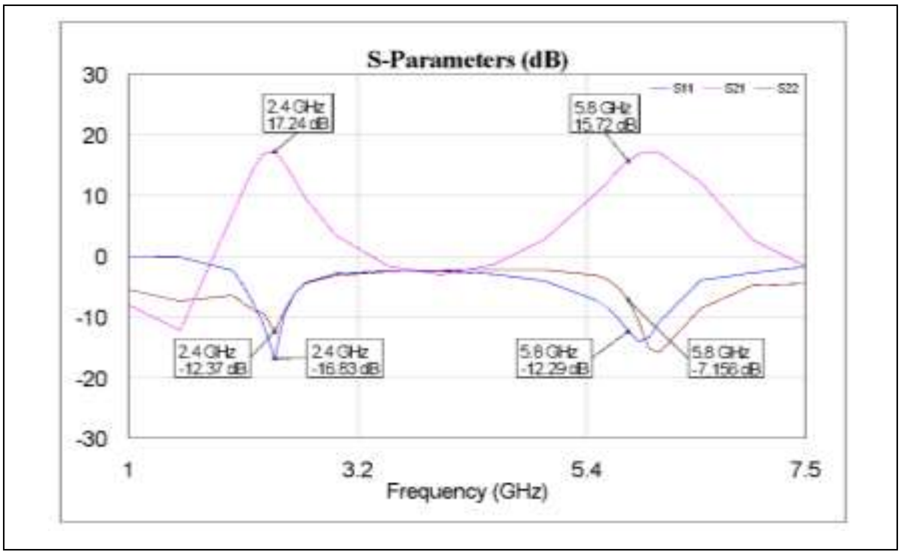


Figure 7.6. Scattering parameter results of the concurrent dual band case

The concurrent dual band low noise amplifiers operate on both frequency bands at the same time. For this case, the proposed low noise amplifier achieves the gain of 17.24 dB at 2.4 GHz and 15.72 dB at 5.8 GHz. Input and output matching results are -16.83 dB and -12.37 dB at 2.4 GHz and -12.29 dB and -7.15 dB at 5.8 GHz respectively.

7.3.1.2. Noise Figure

Together with the scattering parameter performance, noise figure analysis is yet another crucial criterion for the low noise amplifier performance. During the literature review phase, it is learned that the dual band low noise amplifiers generally tend to have slightly greater noise figure value than other single band designs as a tradeoff. Therefore, the main efforts and concentration are used up to overcome this noise figure tradeoff, the objective was keeping the noise figure as minimum as possible with combining various design techniques. In Figure 7.7, noise figure performance result for the single 2.4 GHz case is given.

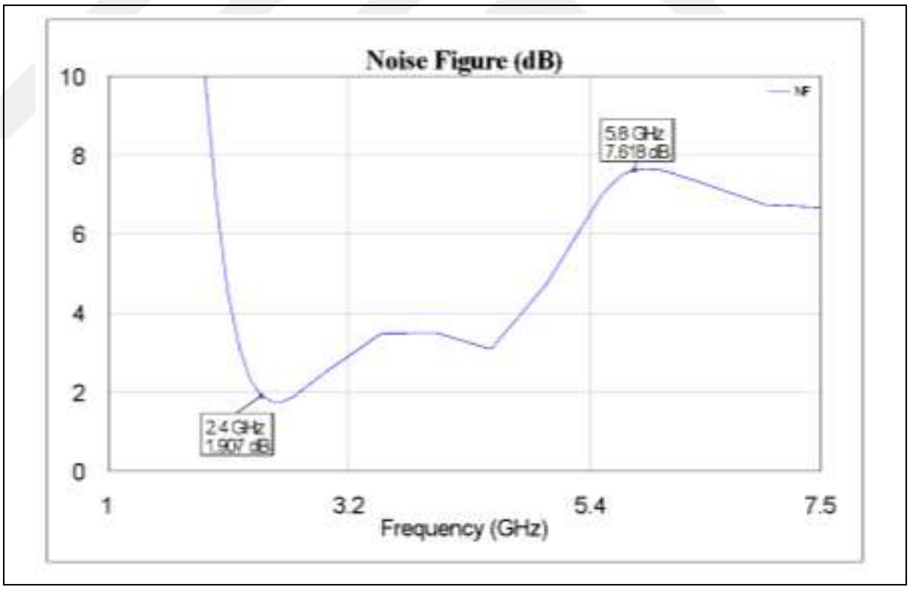


Figure 7.7. Noise figure result for the single 2.4 GHz case

For the single 2.4 GHz operation case, the proposed low noise amplifier exhibits 1.9 dB noise figure performance at 2.4 GHz. In contrast, the noise figure performance for the single 5.8 GHz case is shown in Figure 7.8.

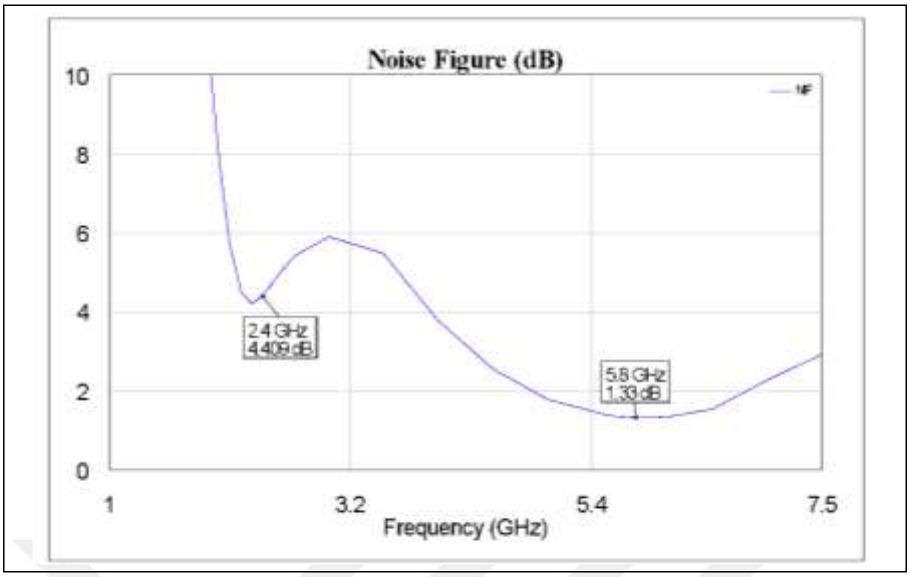


Figure 7.8. Noise figure results for the single 5.8 GHz case

For the single 5.8 GHz operation case, 1.33 dB of noise figure performance is obtained at 5.8 GHz. The last case, which is concurrent dual band for both 2.4 GHz and 5.8 GHz frequency band operation simultaneously, the schematic result for noise figure performance is shared in Figure 7.9.

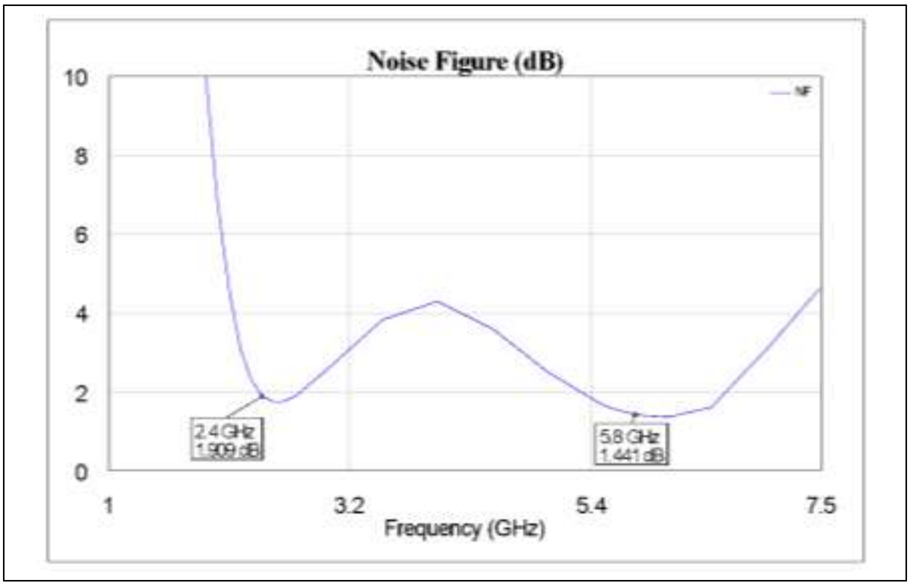


Figure 7.9. Noise figure results for concurrent dual band case

For the concurrent dual band case, the low noise amplifier has the noise figures of 1.9 dB and 1.4 dB at 2.4 GHz and 5.8 GHz respectively. The schematic results for noise figure analysis show that the objective of having the noise figure performance below 2 dB is achieved for all three cases.

7.3.1.3. 1 dB Compression Point (P1dB)

From a linearity point of view, P1dB is an essential parameter that should be analyzed carefully. It stands for the output power level at which from its constant level, the gain decreases 1 dB. Generating harmonics, distortions and intermodulation products occur when an amplifier reaches its 1dB compression point and this causes nonlinearities in the designs. Therefore, amplifiers should operate below the compression point. The P1dB results for the single 2.4 GHz case is demonstrated in Figure 7.10.

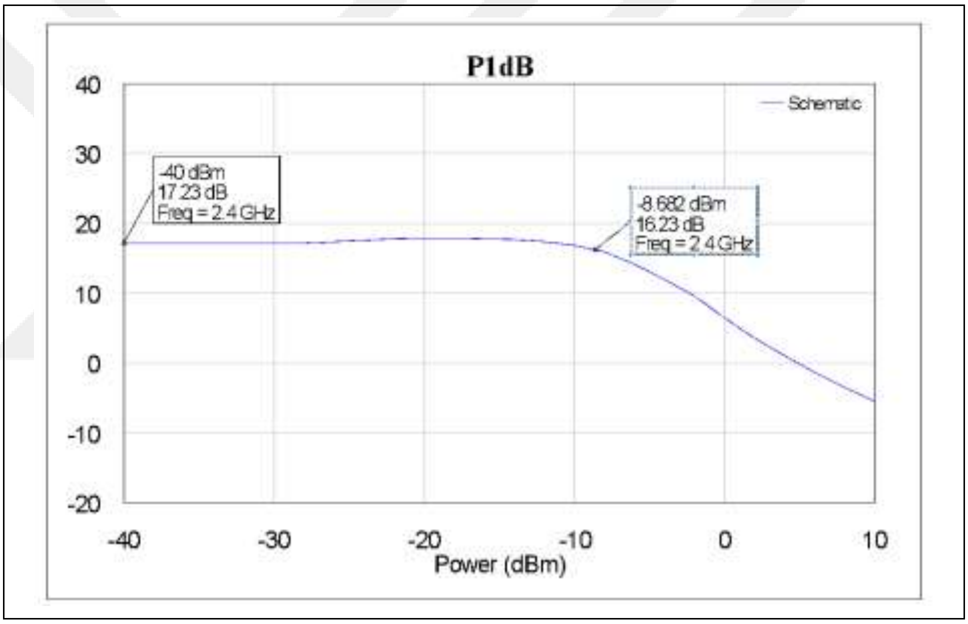


Figure 7.10. P1dB results for the single 2.4 GHz case

The graph given above states that the low noise amplifier has -8.68 dBm input P1dB value at 2.4 GHz. Since the gain equals to 16.23 dB at 2.4 GHz, output P1dB value becomes 7.55 dBm. Meanwhile, the schematic result for P1dB at the single 5.8 GHz operating case is shared in Figure 7.11.

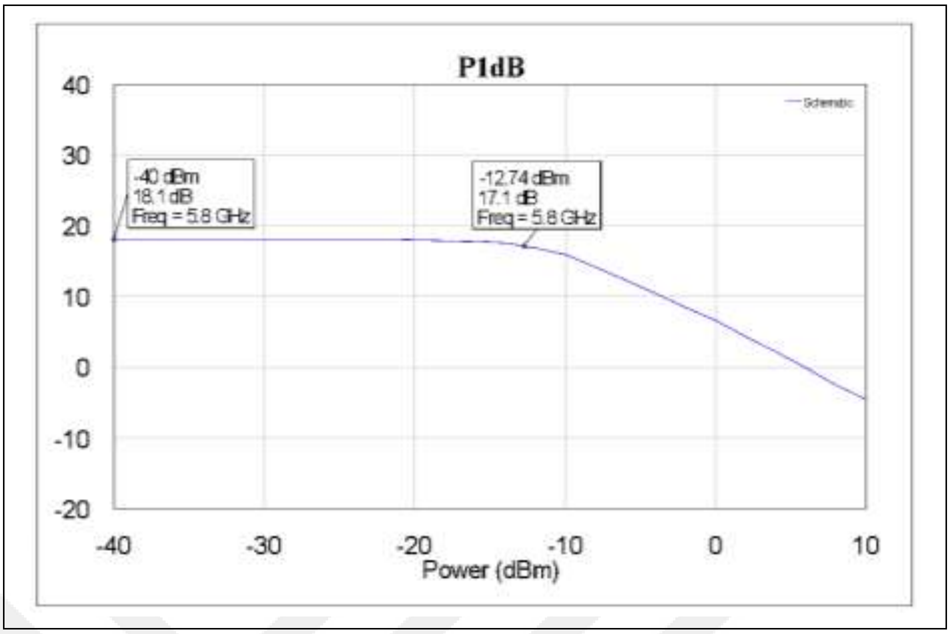


Figure 7.11. P1dB results for the single 5.8 GHz case

For the single 5.8 GHz case, the low noise amplifier has the value of -12.74 dBm input P1dB performance. In addition to that, output P1dB parameter is 4.36 dBm at 5.8 GHz. The 1 dB compression point schematic result for the concurrent dual band case is given in Figure 7.12.

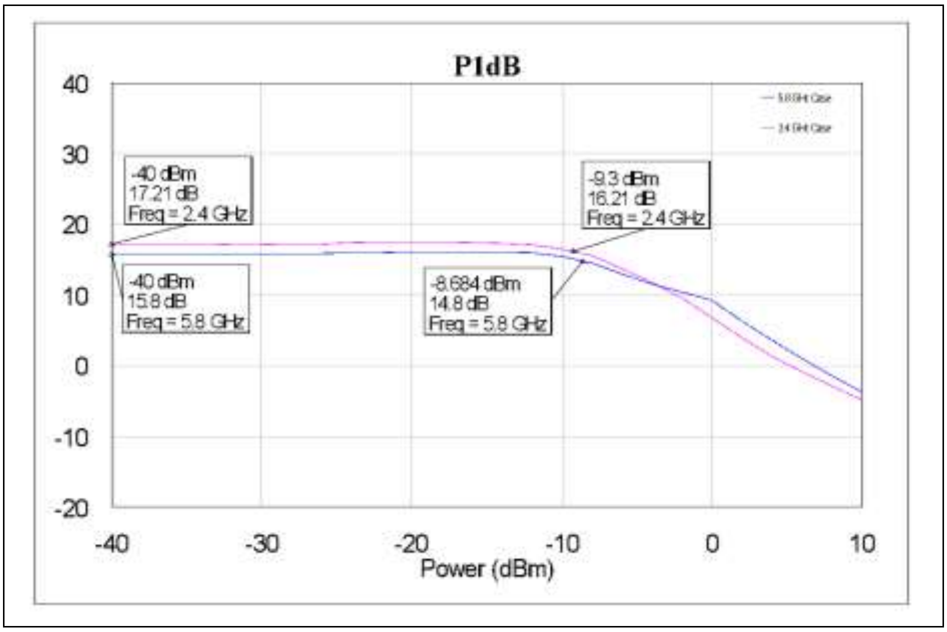


Figure 7.12. P1dB result for concurrent dual band case

For the concurrent dual band case, the proposed low noise amplifier has input P1dB values of -9.3 dBm and -8.68 dBm at 2.4 GHz and 5.8 GHz respectively. Which means that output P1dB values are equal to 6.91 dBm and 6.12 dBm respectively for concurrent dual band application.

7.3.1.4. Stability

Not only for the designed operation frequencies but also for the wide range of frequency bands, the low noise amplifiers are expected to have a stabilized performance. The stability analysis for the proposed low noise amplifier is done between 0 – 100 GHz (which is up to transition frequency (f_T) of the transistors) and the schematic results for all three cases stated there is no instability risk for a wide range of frequency bands. For stabile designs, the stability factor K should be greater than 1 for all frequencies. The AWR design tool takes the logarithm of this value in its K factor simulation, therefore it should be greater than 0 dB for all cases. The schematic results for the stability analysis at single 2.4 GHz case is given in Figure 7.13.

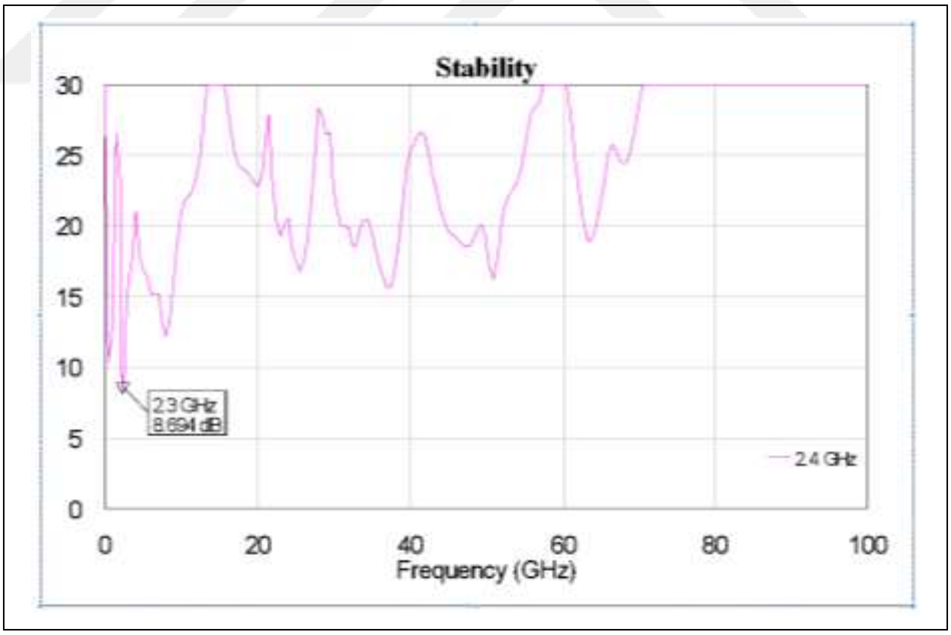


Figure 7.13. Stability analysis for the single 2.4 GHz case

The graph above, cursor states the lowest value of the stability factor K. As mentioned earlier, the proposed low noise amplifier tested for stability up to 100 GHz and it shows a stable performance for the single 2.4 GHz operating case. In addition to that, the stability analysis for the single 5.8 GHz case is demonstrated in Figure 7.14.

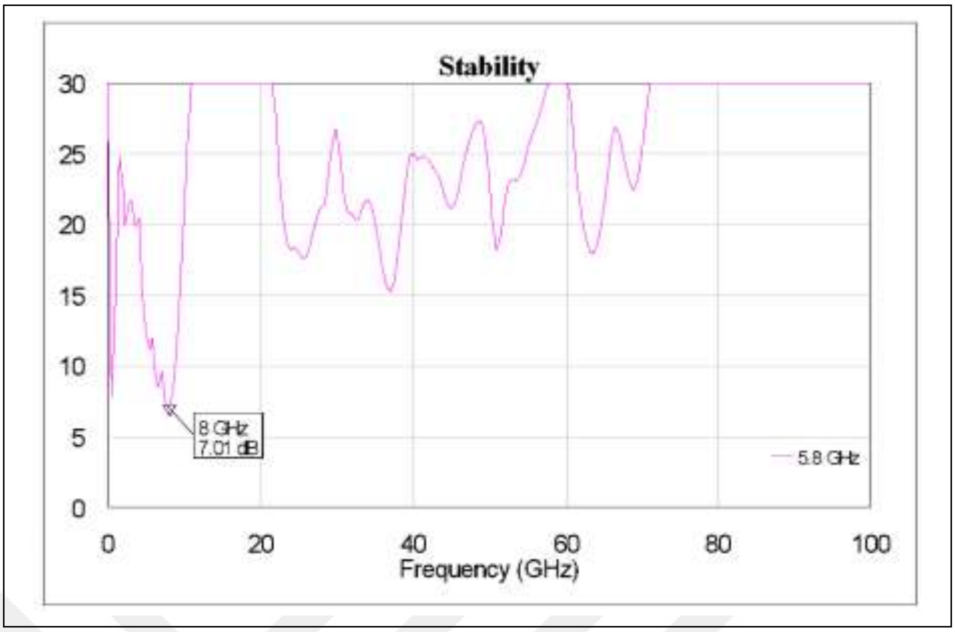


Figure 7.14. Stability analysis for the single 5.8 GHz case

The same as the previous graph, the cursor remarks the lowest value of the stability factor K up to 100 GHz. The stability results for the concurrent dual band application is shared in Figure 7.15.

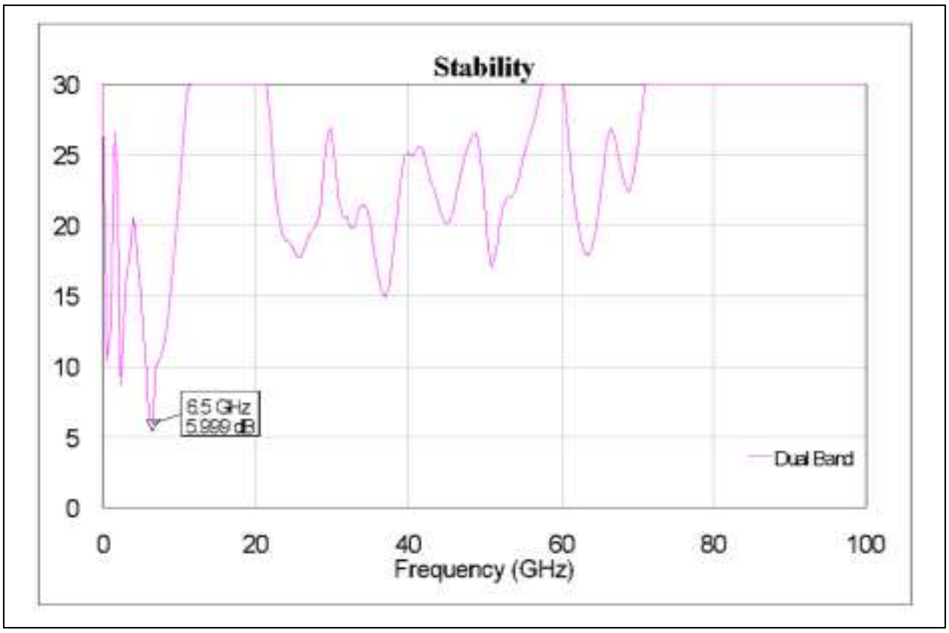


Figure 7.15. Stability analysis for concurrent dual band case

The minimum value of the stability factor is 5.99 dB achieved for concurrent dual band case. The schematic simulation results stated the stability factor K is greater than zero for all cases between DC to 100 GHz.

7.3.2. EM Simulation Results

For the radio frequency integrated circuit designs, it is generally expected to obtain differences in gathered results after running EM simulations. Moreover, EM simulation is a must-do process if the design will be taped out. The following subsections of this part states the results for the EM simulation tool for AWR design environment.

7.3.2.1. Scattering Parameters

After observing the schematic simulation results, the layout of the circuit is constructed. The component by component careful design for the layout should be done in order to have reasonable EM simulation results. The s-parameters EM simulation results for the single 2.4 GHz case is shown in Figure 7.16.

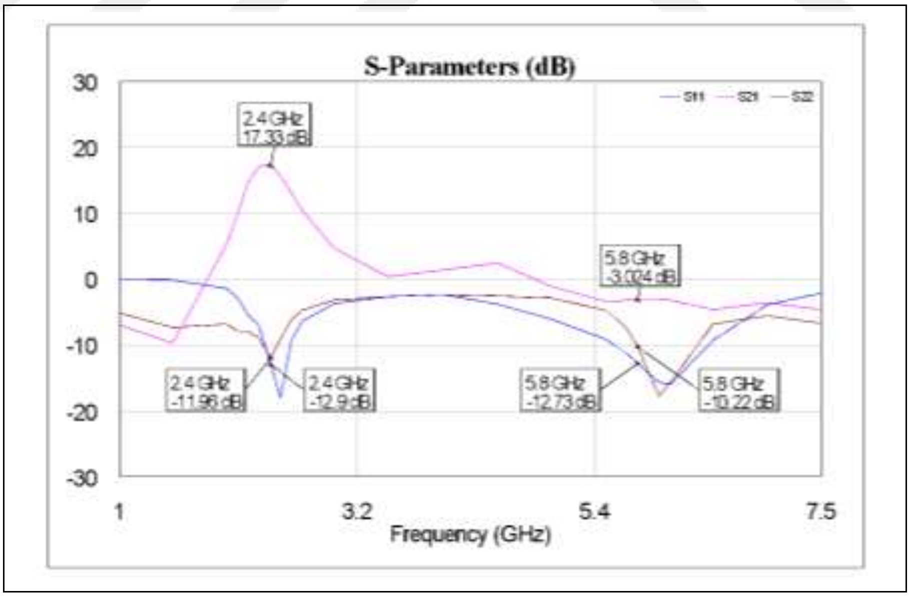


Figure 7.16. The scattering parameter results for EM simulation at single 2.4 GHz case

The scattering parameter results for the single 2.4 GHz state that the proposed low noise amplifier has the gain of 17.33 dB, input matching of -12.9 dB and output matching of -

11.96 dB for EM simulation at 2.4 GHz. In addition to that, the s-parameters EM simulation results for the single 5.8 GHz case are shared in Figure 7.17.

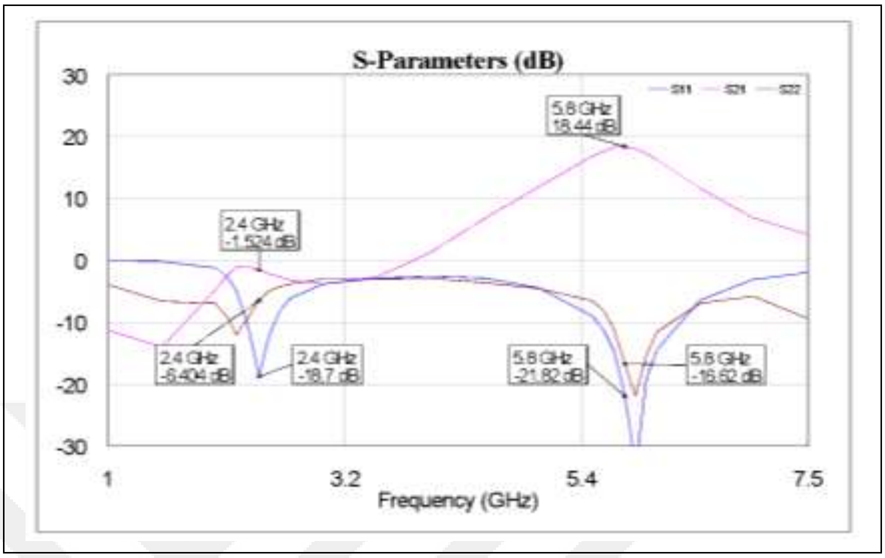


Figure 7.17. The scattering parameter results for EM simulation at single 5.8 GHz case

The EM simulation for s-parameter analysis shows that the gain of 18.44 dB, input matching of -21.82 dB and output matching of -16.62 dB is achieved for the 5.8 GHz frequency case. With the same logic, the EM simulation approves that the proposed low noise amplifier can operate two different single frequency bands which are 2.4 GHz and 5.8 GHz separately. The EM simulation results for the concurrent dual band case is given in Figure 7.18.

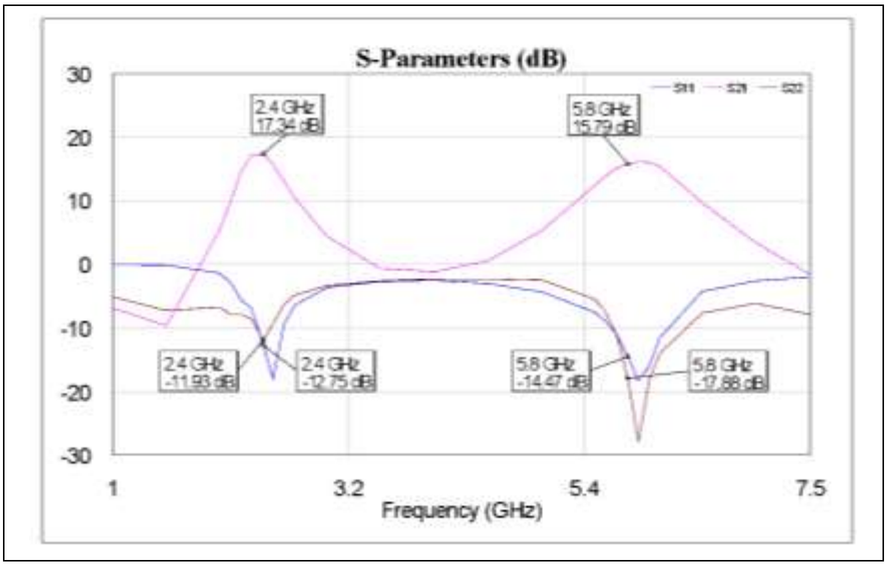


Figure 7.18. The scattering parameter results for EM simulation for concurrent dual band

As can be seen in the graph above, the designed low noise amplifier has the gain of 17.34 dB and 15.79 dB for 2.4 GHz and 5.8 GHz respectively. Input matchings are -12.75 dB for 2.4 GHz and -14.47 dB for 5.8 GHz. Meanwhile output matching values are -11.93 dB and -17.88 dB for 2.4 GHz and 5.8 GHz respectively.

7.3.2.2. Noise Figure

The EM simulation results for the noise figure analysis for three different frequency cases are studied. The noise figure result at the single 2.4 GHz case is given in Figure 7.19.

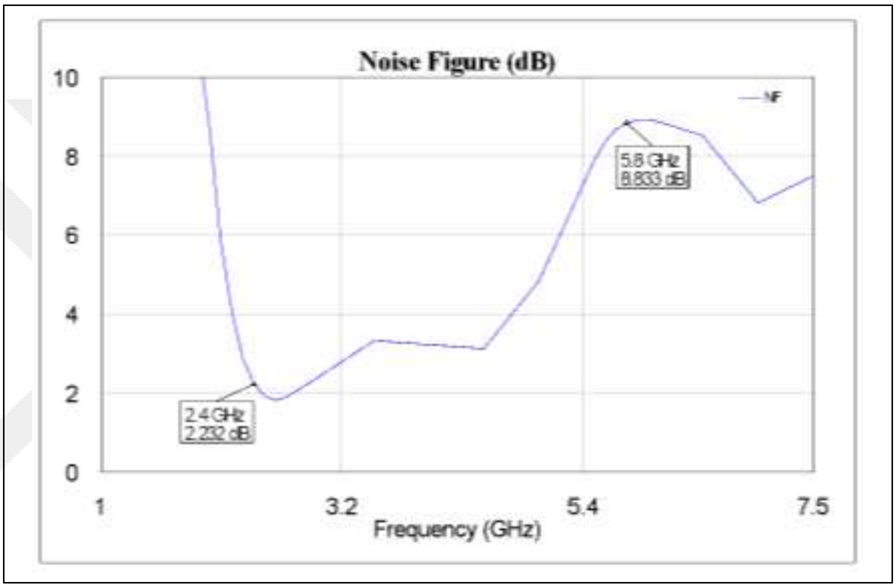


Figure 7.19. The noise figure performance for EM simulation at single 2.4 GHz case

In this case, the EM simulation indicates 2.23 dB of noise figure at 2.4 GHz. Similarly the same analysis is done for the 5.8 GHz frequency case. The EM simulation result is given in Figure 7.20.

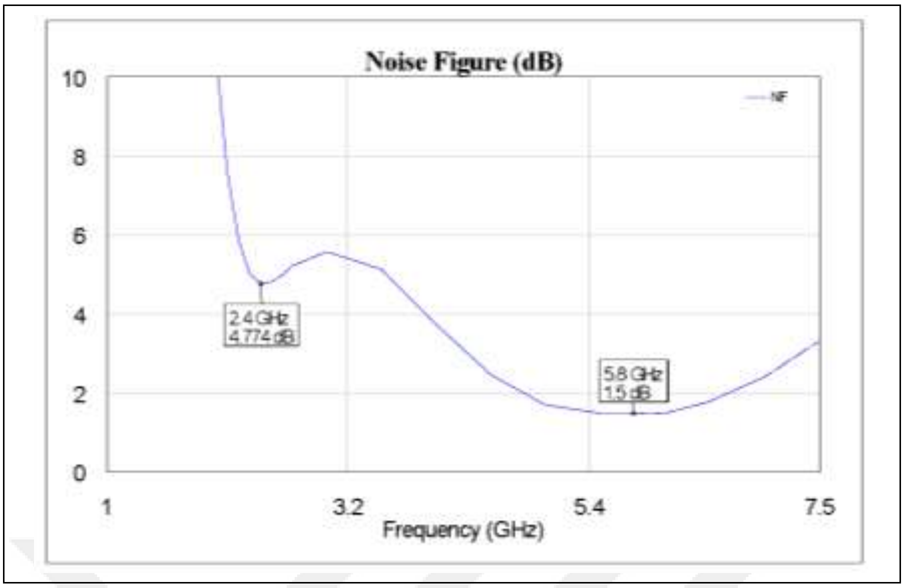


Figure 7.20. The noise figure performance for EM simulation at single 5.8 GHz case

For the single 5.8 GHz condition, the EM simulation result states 1.5 dB of noise figure performance at that specific frequency. The EM simulation for the noise figure analysis about concurrent dual band situation is illustrated in Figure 7.21.

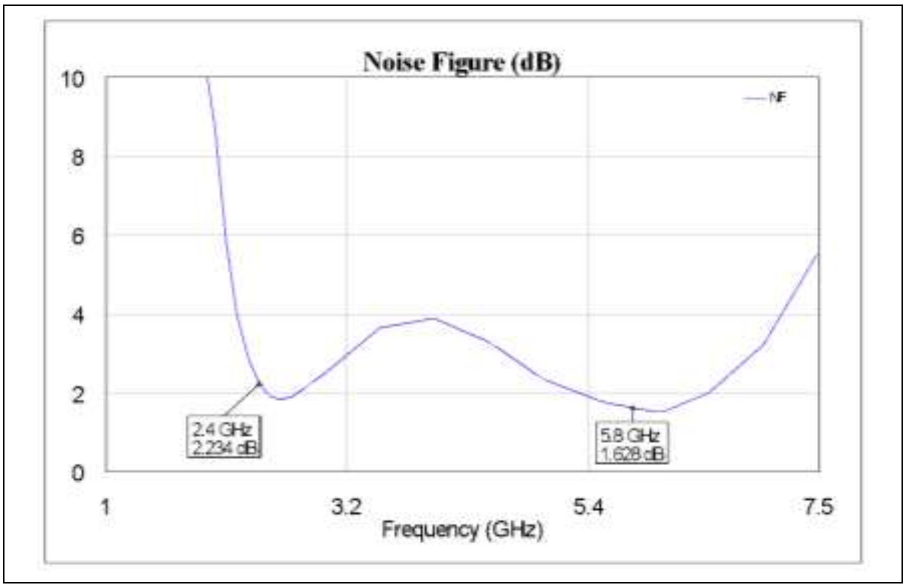


Figure 7.21. The noise figure performance for EM simulation for concurrent dual band case

The EM simulation analysis for concurrent dual band case states the noise figure of 2.23 dB and 1.62 dB at 2.4 GHz and 5.8 GHz respectively.

7.3.2.3. 1 dB Compression Point (P1dB)

To find the P1dB value for the low noise amplifier, the RF signal power has been raised from -40 dBm to 10 dBm for each frequency case. The EM simulation analysis for 1 dB compression point at single 2.4 GHz case is demonstrated in Figure 7.22.

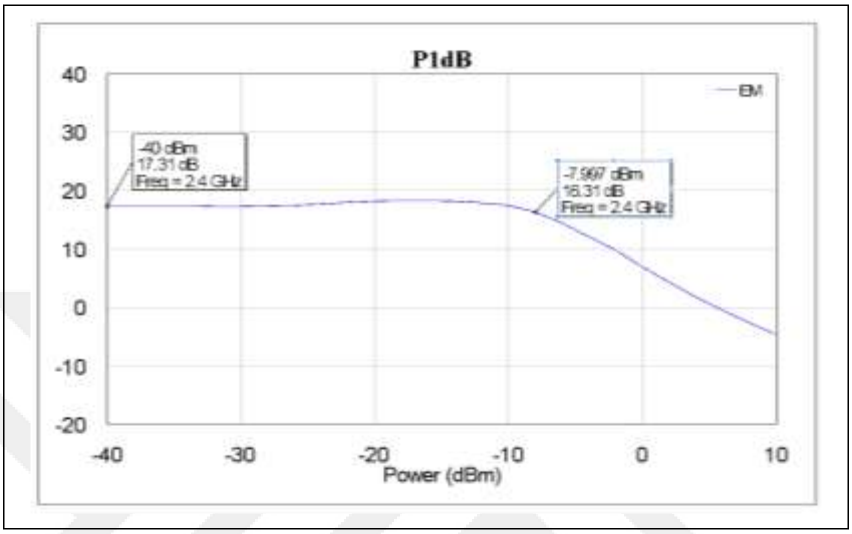


Figure 7.22. The EM simulation result for the P1dB analysis at single 2.4 GHz case

The EM simulation analysis states that the proposed low noise amplifier design has input P1dB of -7.99 dBm at 2.4 GHz. Therefore, the summation with the related gain which is 16.31 dB makes the output P1dB of 8.32 dBm. The EM simulation result for the P1dB analysis at the single 5.8 GHz case is given in Figure 7.23.

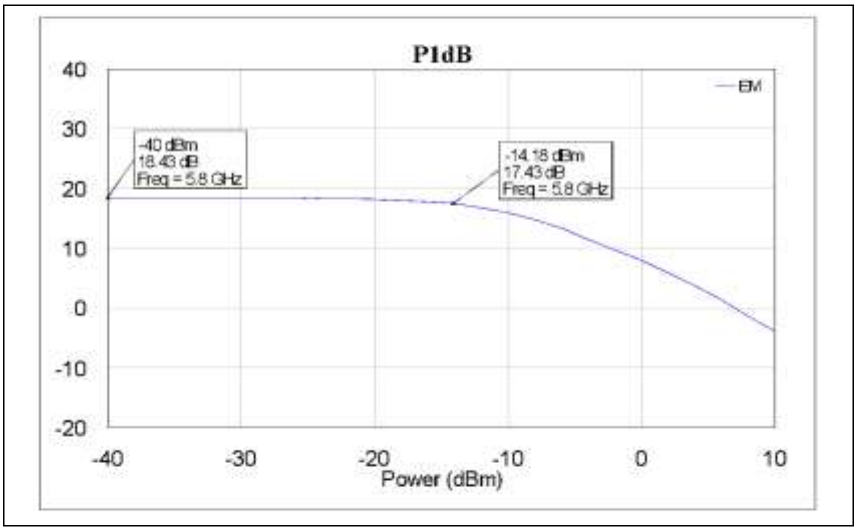


Figure 7.23. The EM simulation result for the P1dB analysis at single 5.8 GHz case

As can be seen in the graph above, the EM simulation indicates that the proposed low noise amplifier design has the input P1dB performance of -14.18 dBm at 5.8 GHz. Consequently, the output 1 dB compression point result for the EM simulation equals to 3.25 dBm. Moreover for the concurrent dual band case, the same EM simulation study has been done. The P1dB results for the concurrent dual band situation are shared in Figure 7.24.

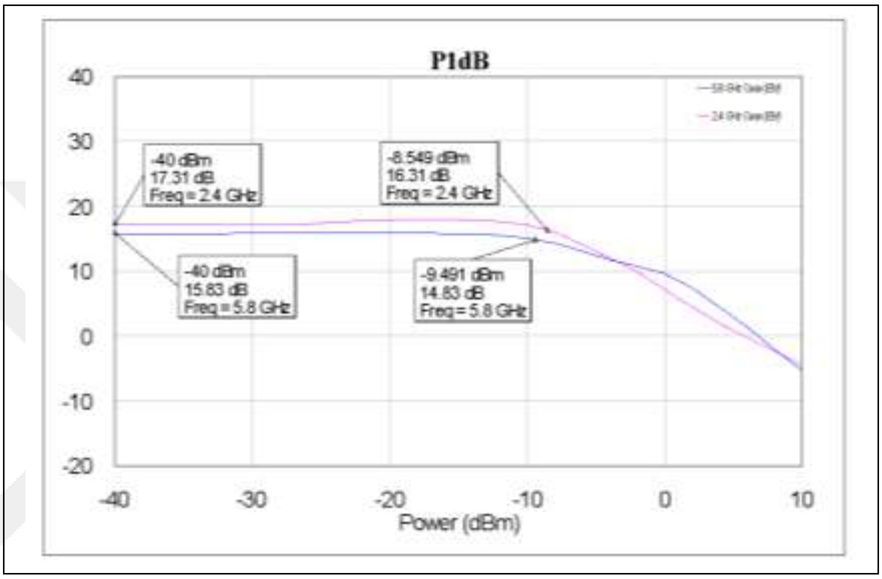


Figure 7.24. The EM simulation results for the P1dB analysis about concurrent dual band

It is observed that input P1dB values are -8.54 dBm and -9.49 dBm at 2.4 GHz and 5.8 GHz respectively. Therefore, output 1 dB compression point results for the EM simulation are 7.77 dBm and 5.34 dBm at 2.4 GHz and 5.8 GHz respectively.

7.3.2.4. Stability

The EM simulation is done for stability for all frequency cases. As mentioned at the schematic results for stability analysis, the frequency range is selected up to 100 GHz to ensure the proposed low noise amplifier has stable performance not only for the specific operation frequency but also up to transition frequency (f_T) of the transistors. The EM simulation result for the stability analysis at single 2.4 GHz frequency case is given in Figure 7.25.

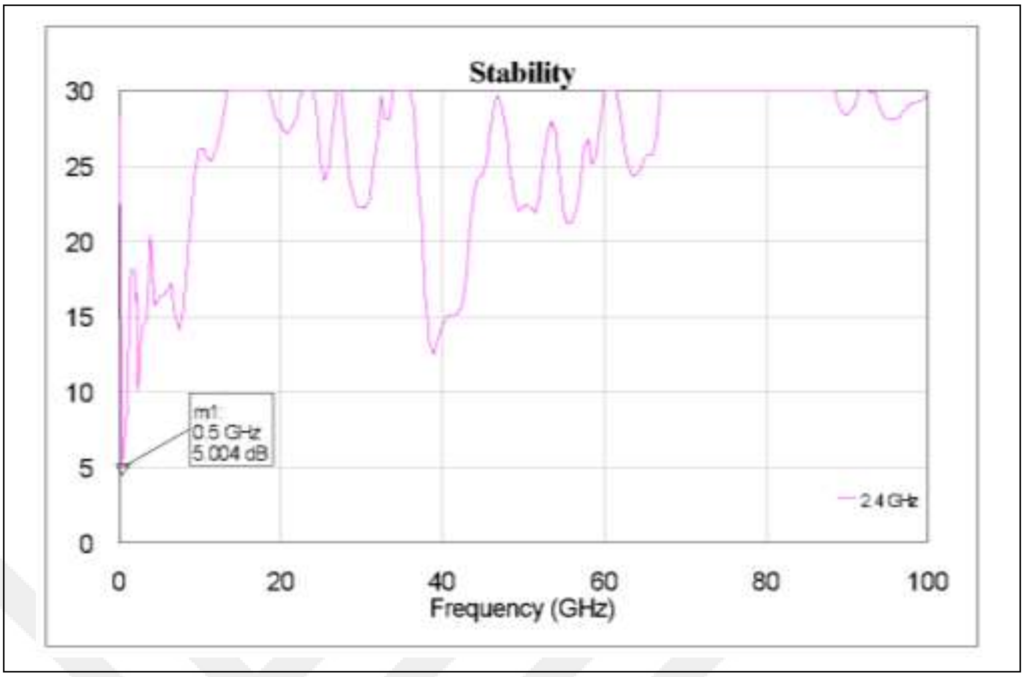


Figure 7.25. The EM simulation result for stability analysis at single 2.4 GHz case

The marker on the above graph emphasizes the minimum stability factor value between 0-100 GHz frequency range for the single 2.4 GHz frequency case. Similarly, the same EM stability analysis done for the single 5.8 GHz frequency case and result is shared in Figure 7.26.

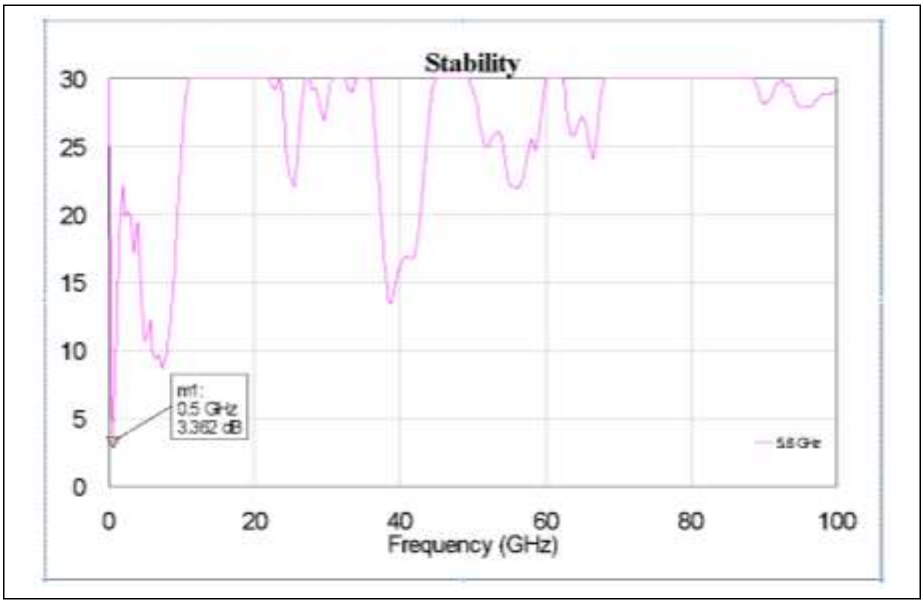


Figure 7.26. The EM simulation result for stability analysis at single 5.8 GHz case

The previous graph indicates that the lowest stability factor (K value) for the single 5.8 GHz frequency case is more than 0 dB up to 100 GHz to prevent any possibility for the instability. The EM simulation result for the stability analysis about concurrent dual band frequency case is shown in Figure 7.27.

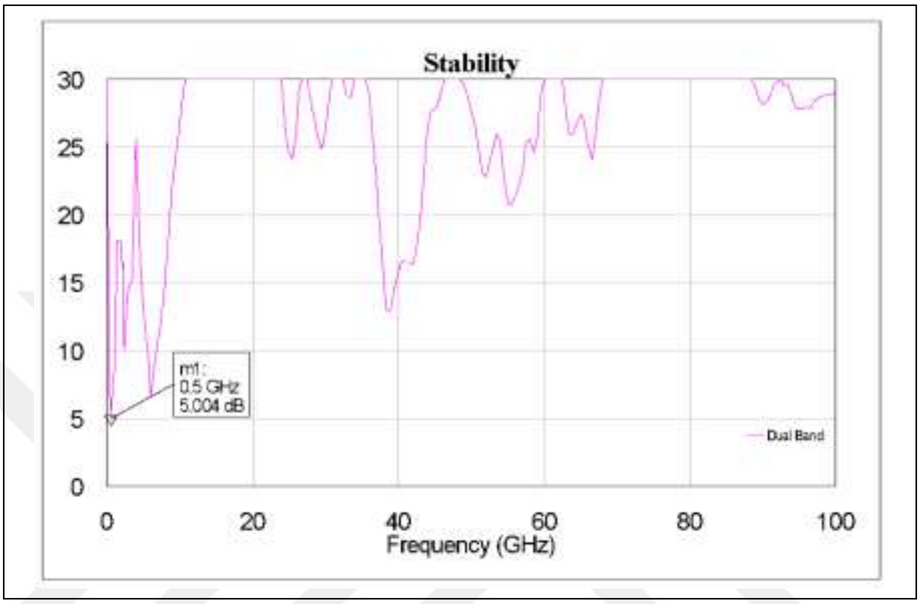


Figure 7.27. The EM simulation result for stability analysis about concurrent dual band

All in all, as can be seen in previously given three EM simulation graphs, the proposed low noise amplifier design ensures stability for each case up to 100 GHz.

7.3.3. Comparison of Schematic versus EM Simulation Results

This subsection of the thesis aims to clarify the differences between schematic and EM simulation results. Both simulations are done in the AWR design environment as mentioned before. Comparison results are based on s-parameters, noise figure performance and P1dB analysis for the proposed low noise amplifier design.

7.3.3.1. Scattering Parameter Results Comparison between Schematic and EM Simulations

In the radio frequency integrated circuit design point of view, it is generally expected to have slight differences between schematic and EM results. The first comparison is done for s-parameter perspective in order to analyze whether schematic simulation results follow the EM simulation results. In Figure 7.28, s-parameter results difference between schematic and EM simulations at the single 2.4 GHz case is shared.

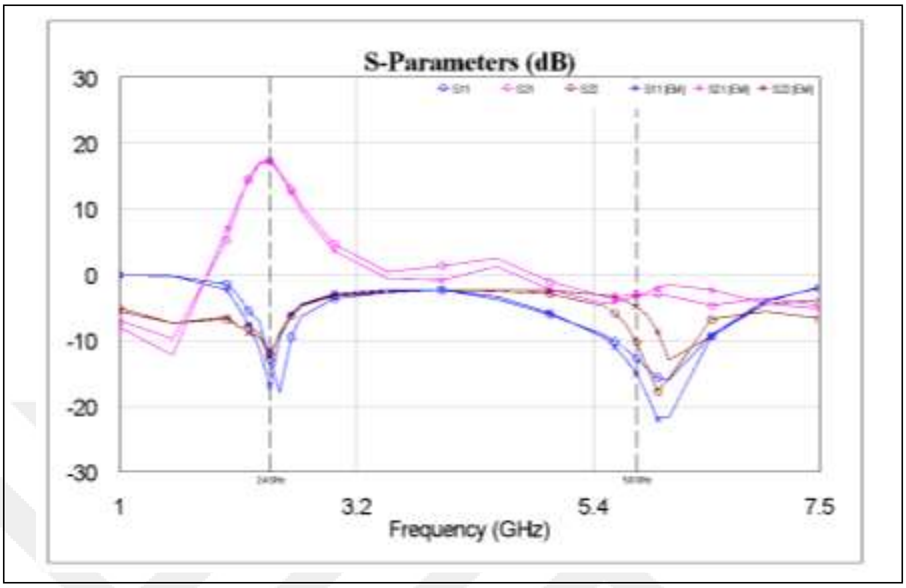


Figure 7.28. Scattering parameter comparison for the single 2.4 GHz case

It is observed that behavior of the gain, input and output matching lines overlap for both schematic and EM simulation at 2.4 GHz. The same analysis is done for the single 5.8 GHz frequency case and results of it demonstrated in Figure 7.29.

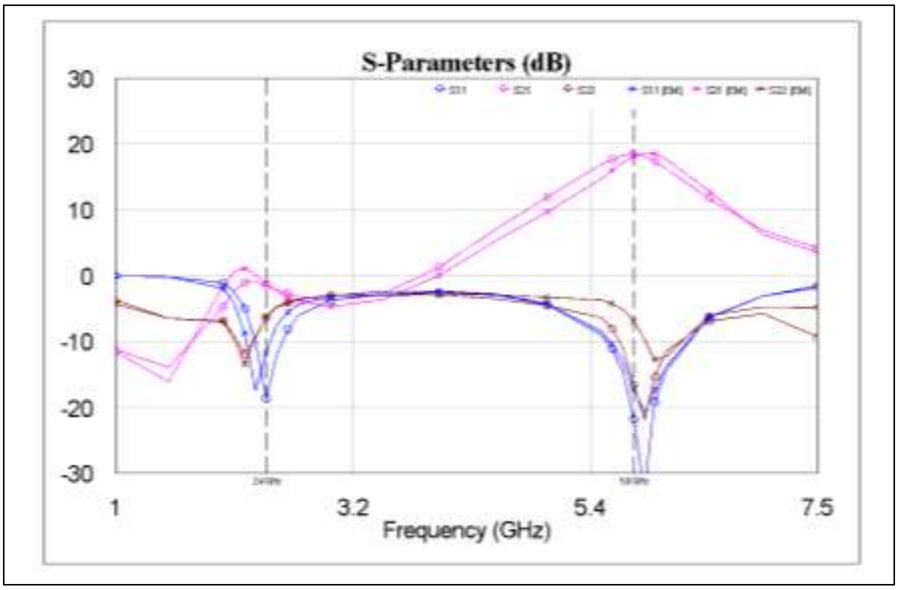


Figure 7.29. Scattering parameter comparison for the single 5.8 GHz case

The same as the previous case, it is analyzed that schematic and EM simulations for the scattering parameters at 5.8 GHz have similar behavior. The differences between schematic and EM simulation results for the concurrent dual band case is shown in Figure 7.30.

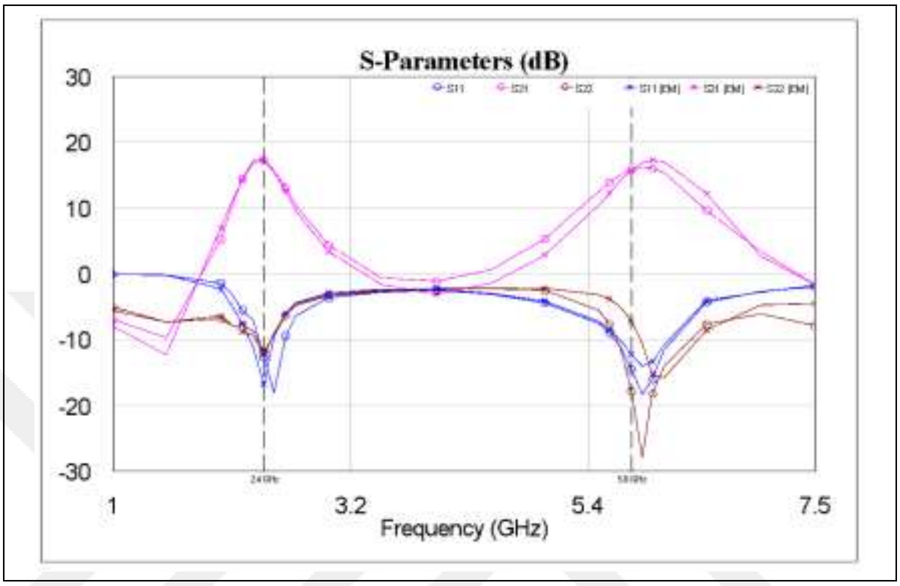


Figure 7.30. Scattering parameter comparison for concurrent dual band case

In conclusion, during the design analysis phase of the thesis, it was a reliance to have schematic and EM simulation results corresponding and not causing much differences with each other.

7.3.3.2. Noise Figure Performance Comparison between Schematic and EM Simulations

Another significant parameter for determining the performance of a low noise amplifier is known as noise figure parameter. Therefore, consistent behavior between schematic and EM simulation results is anticipated for all cases. The noise figure performance comparison between the schematic and EM simulation at single 2.4 GHz case is shared in Figure 7.31.

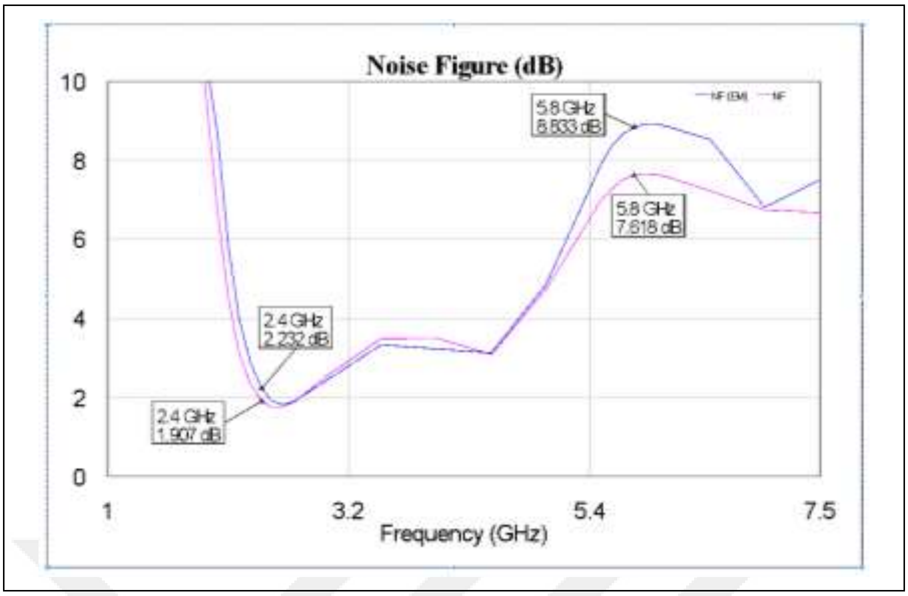


Figure 7.31. Noise figure performance comparison for the single 2.4 GHz case

The comparison graph given above states that, schematic and EM simulation results have similar tendency at 2.4 GHz. Additionally, noise figure performance comparison is also done for the single 5.8 GHz case, the graph is given in Figure 7.32.

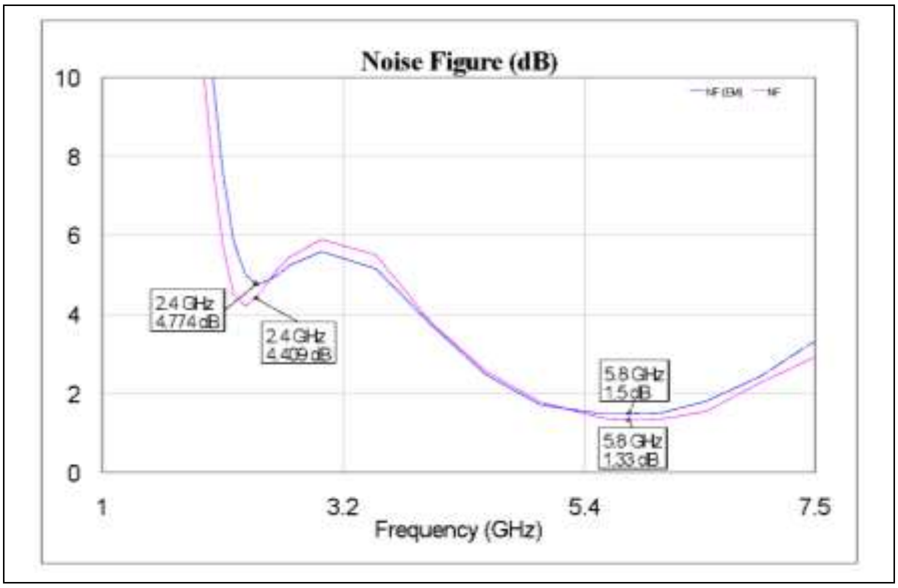


Figure 7.32. Noise figure performance comparison for the single 5.8 GHz case

The last but not the least, the same comparison procedure for concurrent dual band case is shown in the graph below, in Figure 7.33.

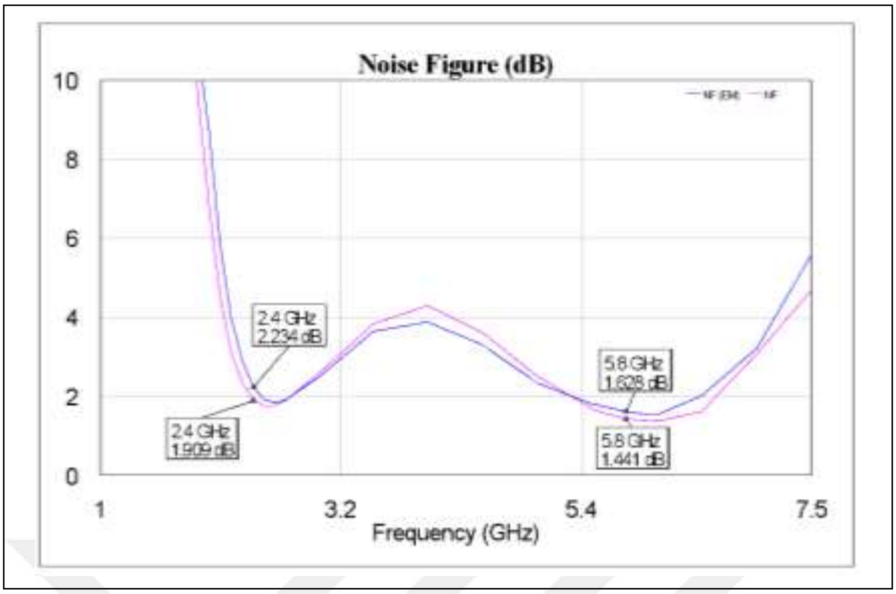


Figure 7.33. Noise figure performance comparison for concurrent dual band case

In conclusion, similar behaviors in all three cases are obtained while comparing schematic and EM simulation based on noise figure performance.

7.3.3.3. 1 dB Compression Point Comparison between Schematic and EM Simulations

The last comparison between schematic and EM simulation results is made for 1 dB compression point analysis. The first case, which is single 2.4 GHz, schematic and EM simulation results for P1dB analysis gathered in the same graph is given in Figure 7.34.

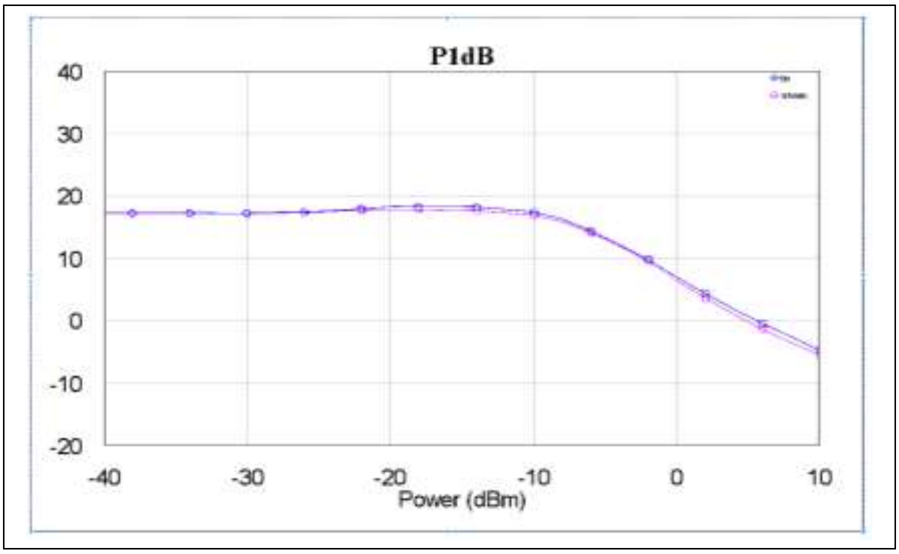


Figure 7.34. P1dB performance comparison for the single 2.4 GHz case

In a similar way, it is observed that schematic and EM simulation lines follow each other at 2.4 GHz. The same analysis is performed for the single 5.8 GHz frequency case and the resulting graph is shown in Figure 7.35.

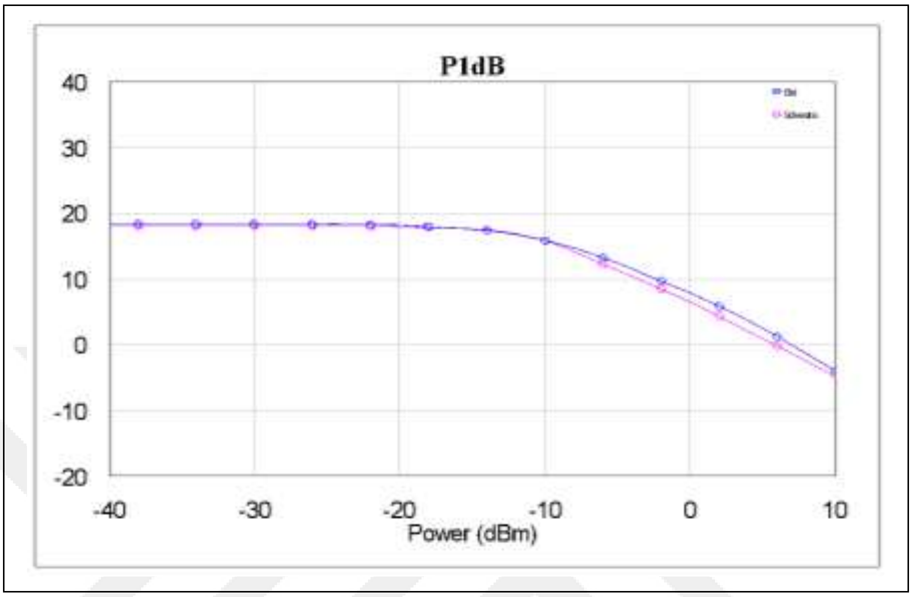


Figure 7.35. P1dB performance comparison for the single 5.8 GHz case

Once again, the similar procedure is executed for the concurrent dual band case to observe whether the schematic and EM simulation results match with each other for the P1dB parameter. The outcome comparison is demonstrated in Figure 7.36.

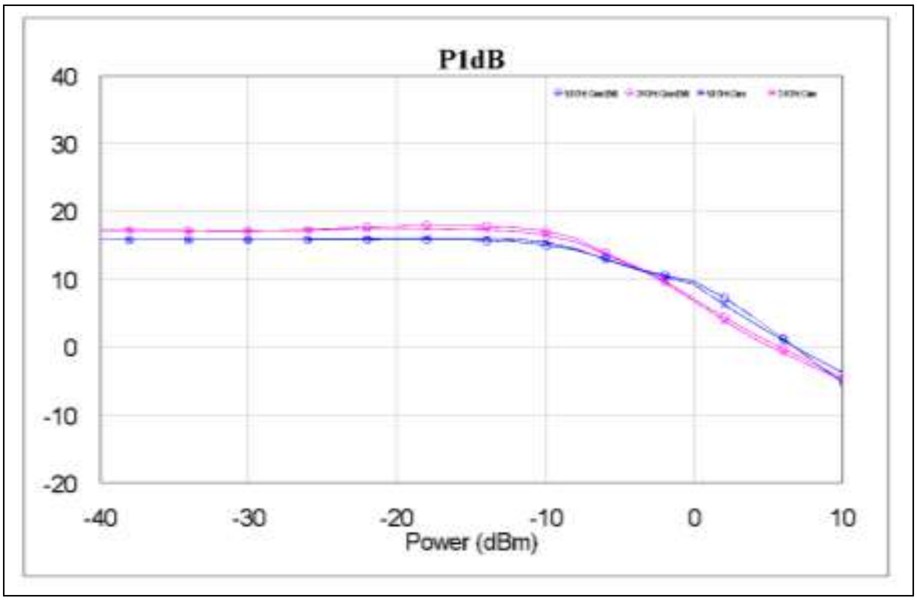


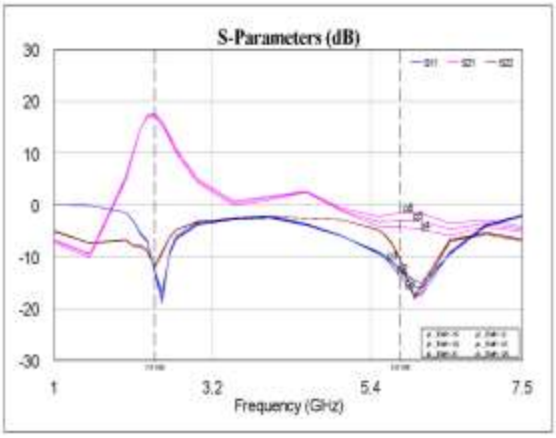
Figure 7.36. P1dB performance comparison for concurrent dual band case

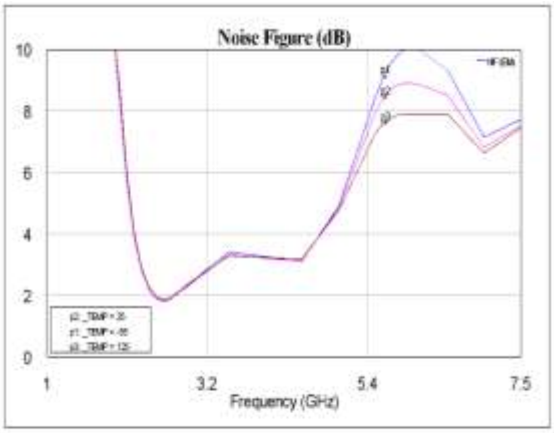
To conclude, P1dB parameter results which are procured from both schematic and EM simulation tools have similar behavior in all frequency cases.

7.3.4. Temperature Analysis of the Design

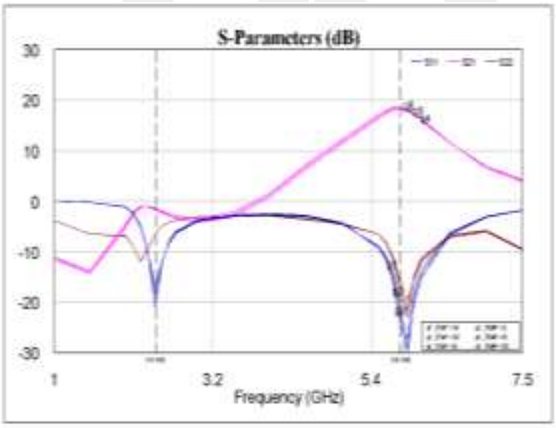
The proposed low noise amplifier design is tested and simulated under different temperature conditions in AWR design environment. For military standards, designed chips should operate at temperatures between -55ºC and 125ºC without causing any problem [176]. Furthermore, the temperature range for industrial standards is between -40ºC and 85ºC. Therefore, an inclusive method is chosen for analyzing the temperature dependence of the proposed low noise amplifier, the AWR temperature analysis is done for temperatures of -55ºC, 25ºC and 125ºC. The obtained s-parameter and noise figure performance for all three cases is shared in Figure 7.37. The results showed that there are no unsettling differences for extreme differences in temperature alteration. In other words, the design is operating properly for different temperatures of operation.

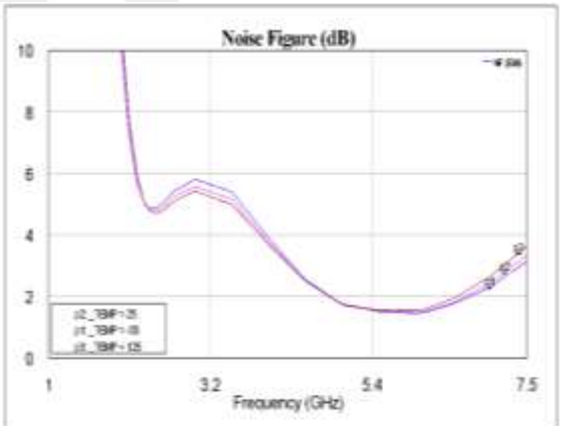
Single 2.4 GHz Case



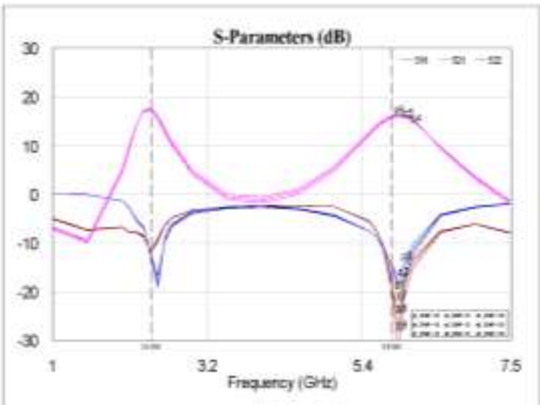


Single 5.8 GHz Case





Concurrent Dual Band Case



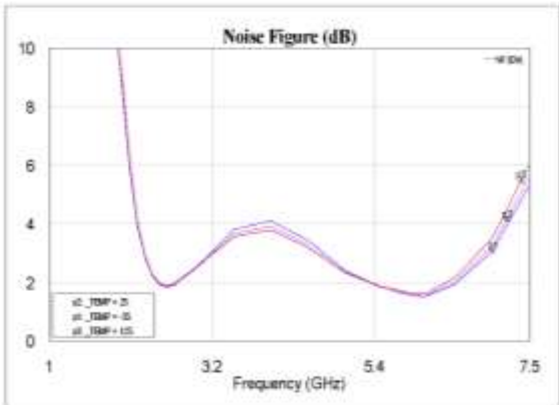


Figure 7.37. The temperature analysis results for the proposed design

7.3.5. Power Consumption of the Chip

At the literature review phase, it is observed that single band low noise amplifier designs tend to have lower power consumption than dual frequency band applications. Therefore, the power consumption is a crucial parameter especially for the multi frequency band low noise amplifier designs. The drawn DC current is 65.5mA and voltage is 3.3V which results in 216mW of power consumption for the designed chip.

All in all, the proposed low noise amplifier design meets all the performance requirements about gain, return losses, noise figure, P1dB, stability, power consumption, size and temperature dependence for both in schematic and EM simulation results for all frequency cases.

8. CONCLUSION

This chapter of the thesis aims to compile the whole thesis work study at summary subsection. After that, future work ideas to improve the design is given in the future work subsection. Finally, the comparison between other works examined during literature review is shared.

8.1. SUMMARY OF THE THESIS

This thesis study presents the design and simulation analysis for a low noise amplifier which can operate at single 2.4 GHz, single 5.8 GHz and concurrent dual band application for 2.4 GHz and 5.8 GHz simultaneously in 0.15um GaAs pHEMT technology. The design is fully integrated onto a single die and it does not require any external component for matching.

The proposed low noise amplifier design works for the S and C band of the IEEE frequency spectrum. Therefore it is suitable for the applications mentioned in the Chapter 1.1 of the thesis. The main motivation for selecting the operation frequency is designing the low noise amplifier which is suitable for Bluetooth and Wi-Fi 6 applications. During the literature review phase, the low noise amplifiers having similar operation frequencies were studied. However, to the best of the author’s knowledge, there is no low noise amplifier design that combines two single frequency band applications with the concurrent dual band operation. This fact improves the frequency flexibility of the proposed low noise amplifier design and contributes a novel idea for the master thesis study.

The operation frequency is controlled by the two switching transistors presented in the feedback paths. The control voltage for the switches is bias configurable, which means there is no need for extra DC supply voltage to control the frequency of operation. The single DC bias voltage has the value of 3.3 V.

In the design, the advantages of the feedback is used in depth. Since the switching transistors are on the feedback paths, their state for whether being on or off directly affects the signal’s frequency and gain which can be obtained at the output port. Moreover, the usage of the feedback in this manner affected stability of the design in a positive way.

The low noise amplifier design involves three stages of cascade amplification provided by pHEMT depletion mode transistors having common source configuration. Moreover, a variety of design methods are beneficially used for the thesis. Since the proposed low noise amplifier design has multiple bands of frequency operations, it was assumed that power consumption of the chip might be the first concern of the design. To overcome this issue, the current reuse technique is used which eliminates the need for the increased number of voltage supplies for biasing the transistor. In addition to that, the current reuse technique helps to reduce the total chip area, since the need for additional bias tee does not exist. Secondly, the self-biasing method is studied and applied to the proposed design. In the same manner with the power and area saving of the design, self-biasing technique is used. It is used not only for eliminating the requirement for the complex bias network for each stage of the amplification but also as a tool for input matching of the first stage of the amplification. Thirdly, a commonly used technique which is inductive degeneration is adapted to the design to improve the matching and gain performance of the design with minimum possible noise addition. Lastly, a diode connected transistor is used instead of a resistor to reduce the noise contribution.

All in all, the achieved EM simulation results for gain, noise figure and output P1dB performance of the proposed low noise amplifier design for the single 2.4 GHz case are; 17.33 dB, 2.23 dB and 8.32 dBm respectively. Similarly for the single 5.8 GHz case, the gain is 18.44 dB, the noise figure is 1.5 dB and output P1dB is 3.25 dBm obtained from the EM simulation. Finally, the last case which contains the concurrent dual band operation at 2.4 GHz and 5.8 GHz simultaneously has the gain performance of 17.34 dB and 15.79 dB, noise figure of 2.23 dB and 1.62 dB, output P1dB of 7.77 dBm and 5.34 dBm for 2.4 GHz and 5.8 GHz frequencies respectively. The power consumption of the designed chip is calculated as 216 mW with 3.3 V single voltage supply. The dimensions of the designed low noise amplifier chip are 3.4x1.5 mm^2, all input and output pads included.

All simulations were performed thanks to the AWR design environment and done tape-out by WIN Foundry.

8.2. COMPARISON BETWEEN VARIOUS WORKS IN LITERATURE

In tables numbered between 8.1 and 8.5, different studies published in the literature compared with respect to frequency of operation, concurrent or dual band application and technology selection.

Table 8.1. Comparison between LNAs based on single 2.4 GHz operating frequency

	[177]*	[178]*	[179]*	[180]*	[181]*	[182]*	[183]*	This Work*			
										C. Dual	
Frequency (GHz)	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	5.8	2.4	5.8
S_{21} (dB)	24	15.9	20.6	18.24	18.5	20	20	17.33	18.44	17.34	15.79
S_{11} (dB)	-15.5	-12.7	-32	-15.95	27.6	-19	-12.3	-12.90	-21.82	-12.75	-14.47
S_{22} (dB)	-21.8	-16	-14	-13.89	34.3	-21	-40	-11.96	-16.62	-11.93	-17.88
Noise Figure (dB)	2.98	2.86	3.7	2.62	1.85	2.4	0.93	2.23	1.5	2.23	1.62
Output P1dB (dBm)	-	3.7	0	-	0.8	-2	10	8.32	3.25	7.77	5.34
Power (mW)	16.2	-	33	48	9.1	7.2	140	216			
Size (mm x mm)	-	1.1x1.0	0.72x0.82	-	0.99x1.37	1.62x1.28	0.77x0.78	3.4mm x 1.5mm			
Frequency Cases	1	1	1	1	1	1	1	3			
Technology	SiGe BiCMOS	SiGe BiCMOS	0.35-um CMOS	0.18-um CMOS	0.13-um CMOS	0.25-um CMOS	0.15-um pHEMT	0.15-um GaAs pHEMT			

* Simulation Results ** Measurement Results

Table 8.2. Comparison between LNAs based on single 5.8 GHz operating frequency

	[184]	[185]	[186]	[187]	[188]**	[189]**	[190]**	This Work*			
										C. Dual	
Frequency (GHz)	5.8	5.8	5.8	5.8	5.8	5.7	5.2	2.4	5.8	2.4	5.8
S_{21} (dB)	11.5	16	18.8	16	7.2	16.2	15	17.33	18.44	17.34	15.79
S_{11} (dB)	-9	-15	<-10	-18.1	-11	-7	-	-12.90	-21.82	-12.75	-14.47
S_{22} (dB)	-13.7	-13	<-10	-15.2	-17	-12	-	-11.96	-16.62	-11.93	-17.88
Noise Figure (dB)	4	4.1	2	3.07	3.2	2.4	3.5	2.23	1.5	2.23	1.62
Output P1dB (dBm)	-7.5	1	4.3	-6.5	2.5	9.5	-7	8.32	3.25	7.77	5.34
Power (mW)	6.6	100	32.4	1.5	20	72	10	216			
Size (mm x mm)	1.2x0.9	0.55x0.55	1.0x0.72	-	0.88x0.74	1.59x0.83	0.4x1.1	3.4mm x 1.5mm			
Frequency Cases	1	1	1	1	1	1	1	3			
Technology	Si BJT	Si BJT	SiGe BiCMOS	SiGe BiCMOS	0.35-um CMOS	GaAs HBT	0.7-um MESFET	0.15-um GaAs pHEMT			

* Simulation Results ** Measurement Results

Table 8.3. Comparison between LNAs based on dual band

	[191]		[192]		[193]		[194]		[195]**		This Work*			
													C. Dual	
Frequency (GHz)	2.4	5.5	1.8	2.14	2.4	5.2	3.5	5.8	2.4	5.8	2.4	5.8	2.4	5.8
S_{21} (dB)	13.5	20	14.54	16.6	10.1	10.9	12.9	18.6	11.1	5.1	17.33	18.44	17.34	15.79
S_{11} (dB)	-10	-8	-11.5	-15.1	-10.1	-11	-10.3	-20.4	-14.2	-18.8	-12.90	-21.82	-12.75	-14.47
S_{22} (dB)	-12	-12	-8.4	-10.9	-10.5	-17	-	-	-9.4	-8.4	-11.96	-16.62	-11.93	-17.88
Noise Figure (dB)	0.9	1.45	1.75	1.97	2.9	3.7	3	3.29	4.3	5.4	2.23	1.5	2.23	1.62
Output P1dB (dBm)	6.5	11	-1.46	1.8	3.1	-5.1	1.65	3.57	0.5	-2.4	8.32	3.25	7.77	5.34
Power (mW)	35.2	54.4	7.5		11.7	5.7	9.12		8.4		216			
Size (mm x mm)	-		0.8x0.68		-		-		0.86x0.58		3.4mm x 1.5mm			
Frequency Cases	2		2		2		2		2		3			
Technology	SiGe:C Bipolar		0.13-um CMOS		0.18-um CMOS		0.18-um CMOS		SiGe HBT		0.15um GaAs pHEMT			

* Simulation Results ** Measurement Results

Table 8.4. Comparison between LNAs based on concurrent dual band

	[196]			[197]**		[198]**		[199]**		This Work*			
Frequency (GHz)	3.5	C. Dual		2.4	5.25	2.44	5.25	2.45	5.25	2.4	5.8	C. Dual	
		2.4	5.2									2.4	5.8
S_{21} (dB)	20.3	19.1	17.3	20	8	19.7	14.4	13.9	8.7	17.33	18.44	17.34	15.79
S_{11} (dB)	<-10	<-10	<-10	-7	-12	-9.1	-9.4	-14.4	-12.4	-12.90	-21.82	-12.75	-14.47
S_{22} (dB)	<-10	<-10	<-10	-11	-5	-		-		-11.96	-16.62	-11.93	-17.88
Noise Figure (dB)	2.37	2.9	2.35	6.6		3	3.75	4.98	6.58	2.23	1.5	2.23	1.62
Output P1dB (dBm)	-	-	-	1	3	-4.7	-3.6	5.97	5.44	8.32	3.25	7.77	5.34
Power (mW)	6.97			15		9		2.5		216			
Size (mm x mm)	0.87x0.82			0.43x0.915		1.09x1.0		-		3.4mm x 1.5mm			
Frequency Cases	2			1		1		1		3			
Technology	0.18-um CMOS			0.18-um CMOS		SiGe HBT		SiGe BiCMOS		0.15-um GaAs pHEMT			

* Simulation Results ** Measurement Results

Table 8.5. Comparison between LNAs based on GaAs pHEMT

	[200]*		[201]*		[202]*		[203]**		[204]**		This Work*			
													Dual	
Frequency (GHz)	2.4	5.8	2.4	5	2.4	5.2	2.4	5-6	2.4	5	2.4	5.8	2.4	5.8
S_{21} (dB)	12.2	15.3	18	12	26.2	21.8	14	14.6	17	23	17.33	18.44	17.34	15.79
S_{11} (dB)	-8.5	-21.6	<-10	<-10	-23.6	-26.3	-11	-8	-8	-10	-12.90	-21.82	-12.75	-14.47
S_{22} (dB)	-10.1	.11.8	<-10	<-10	-23.8	-30.4	-		-7.3	-15.4	-11.96	-16.62	-11.93	-17.88
Noise Figure (dB)	0.53	1.43	3	3	2.07	1.84	2.2	2.8	0.9	1.5	2.23	1.5	2.23	1.62
Output P1dB (dBm)	-	-	-6	-4	1.2	1.8	-		11.5	7	8.32	3.25	7.77	5.34
Power (mW)	40		37.8		-		33		-		216			
Size (mm x mm)	2.0x2.9		1.0x1.0		1.4x1.0		1.5x2.5		1.2x0.7		3.4mm x 1.5mm			
Frequency Cases	1		2		2		2		2		3			
Technology	0.15-um GaAs pHEMT		0.15-um GaAs pHEMT		0.2-um GaAs pHEMT		0.25-um GaAs HEMT		GaAs pHEMT		0.15-um GaAs pHEMT			

* Simulation Results   ** Measurement Results

8.3. FUTURE WORK

As mentioned in the earlier sections, there are actually four cases of operation since there are two control pins in the design. Main focus was the low noise amplifier to operate at two different single frequencies and concurrent dual band mode since all the desired specifications of the low noise amplifier can be satisfied by three modes. However there can be a fourth case, which can also be named as bypass mode. By this way, the input RF signal can pass through the designed low noise amplifier without any amplification in the bypass mode. This mode could prevent any mistakes at giving the voltage supply to the control pins, so that there is no amplification for the signal therefore the mistake can be eliminated during the measurement state. That misapply in supply voltage would not cause any harm which might be the saturation or overload for the low noise amplifier and following circuit stages like mixer, filter etc.

The EM simulation results for s-parameter performance of this bypass mode is shown in Figure 8.1. As can be seen in the graph below, the gain is more than 0 dB for some frequency range. If the suppression for the gain would be succeeded, bypass mode can be operated with no amplification. In addition to that, it is aimed to enhance the output matching results for the both 2.4 GHz and 5.8 GHz frequencies.

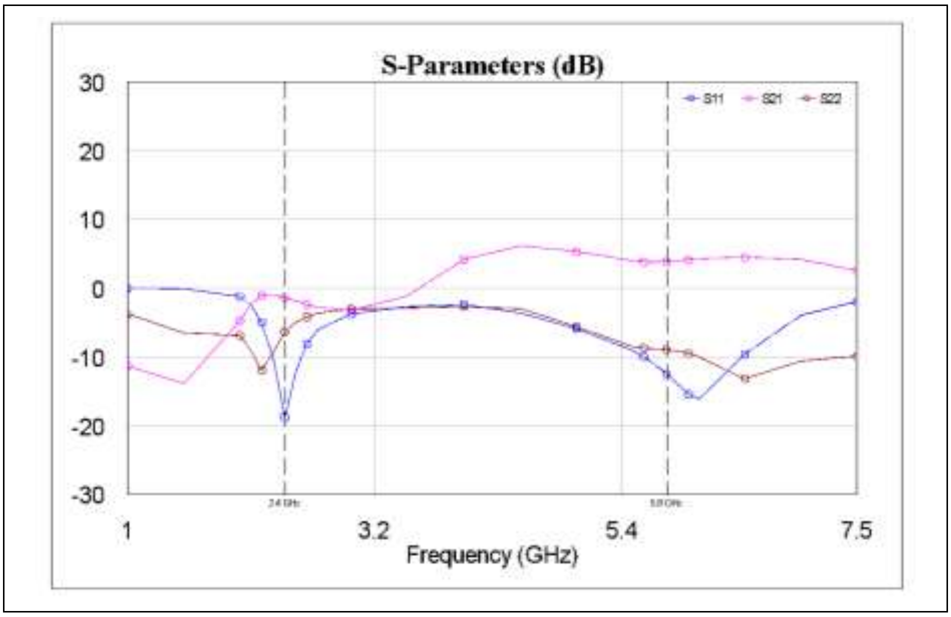


Figure 8.1. The scattering parameter EM simulation results for the bypass mode

The EM simulation analysis for the noise figure performance of the bypass mode is given in Figure 8.2. On the graph below, it is observed that the noise figure is slightly greater than it is expected. For both 2.4 GHz and 5.8 GHz frequencies, the noise figure is targeted to be below 2 dB.

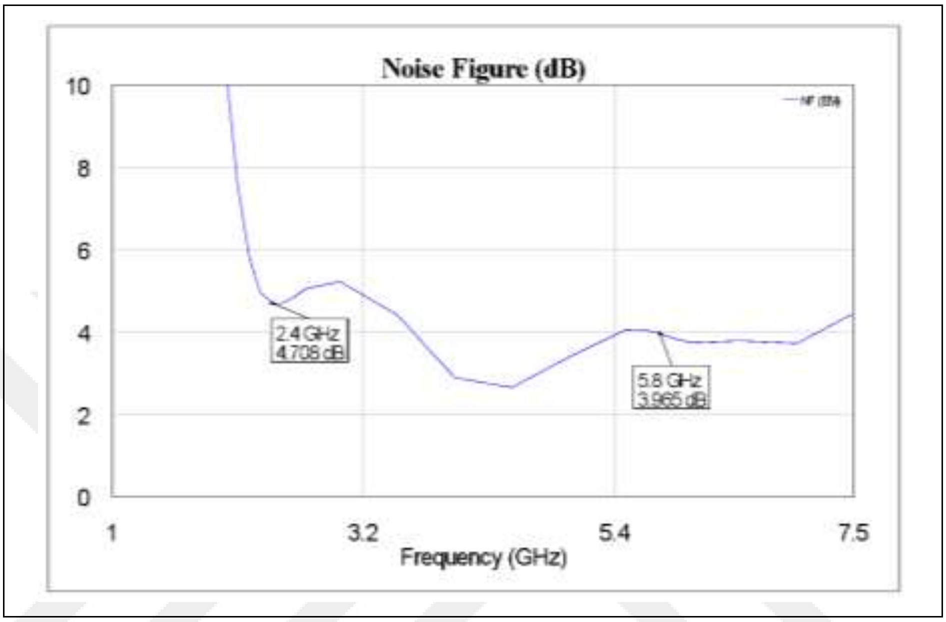


Figure 8.2. The noise figure EM simulation results for the bypass mode

The obtained results given above for s-parameter and noise figure performance for the bypass mode can be improved as a future study of this master thesis.

Last but not the least, the die whose tape-out was completed by WIN Foundry is going to be measured on the wafer under the RF probe station in the RFIC laboratory of Yeditepe University. The obtained real life measurements will be compared with the simulation results.

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