T.C.
ISTANBUL OKAN UNIVERSITY
INSTITUTE OF GRADUATE SCIENCES

THESIS

FOR THE DEGREE OF

MASTER OF SCIENCE

IN POWER ELECTRONICS AND CLEAN ENERGY SYSTEMS

NOOR ALRADHAWI

DESIGN AND ANALYSIS OF COUPLED INDUCTOR-BASED MULTILEVEL INVERTERS

THESIS ADVISOR

Asst. Prof. Dr. Sirin KOC

ISTANBUL, November 2024

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ABSTRACT

DESIGN AND ANALYSIS OF COUPLED INDUCTOR-BASED MULTILEVEL INVERTERS

Multilevel inverters have become essential in power electronics, particularly for medium and high voltage applications. This thesis introduces innovative single-phase seventeen-level and five-level inverter designs, each employing coupled inductors and optimized configurations with a smaller number of components to achieve compact and cost-effective solutions. The use of coupled inductors enables these topologies to deliver high-quality output voltages, minimizing current stress on power devices and enhancing overall performance. A level-shifted pulse width modulation (LS-PWM) technique tailored to seventeen-level topology is presented and thoroughly analyzed. Both designs were simulated, and a hardware prototype of the seventeen-level inverter was constructed to validate its performance. Results demonstrate that the proposed topologies achieve the intended performance with high efficiency and quality output. A comparative analysis with alternative multilevel inverter topologies, including cascaded H-bridge designs, further confirms the superior efficiency and cost-effectiveness of the proposed inverters, establishing them as advanced solutions in multilevel inverter technology.

Keywords: Coupled Inductor, Multilevel Inverter (MLI), Switch count.

KISA ÖZET

AKUPLE ENDÜKTANS TABANLI ÇOK SEVİYELİ EVİRİCİ TASARIMI VE ANALİZİ

Çok seviyeli eviriciler, özellikle orta ve yüksek voltaj uygulamaları için güç elektroniğinde vazgeçilmez hale gelmiştir. Bu tez, daha az bileşen sayısı ile kompakt ve maliyet etkin çözümler sunmak amacıyla bağlı indüktörler ve optimize edilmiş konfigürasyonlar kullanan yenilikçi tek fazlı on yedi seviyeli ve beş seviyeli evirici tasarımlarını tanıtmaktadır. Bağlı indüktörlerin kullanımı, bu topolojilerin yüksek kaliteli çıkış voltajları sağlamasına, güç cihazları üzerindeki akım stresini en aza indirmesine ve genel performansı artırmasına olanak tanır. On yedi seviyeli topolojiye özel olarak uyarlanmış bir seviye kaydırmalı darbe genişlik modülasyonu (LS-PWM) tekniği sunulmuş ve kapsamlı bir şekilde analiz edilmiştir. Her iki tasarım simüle edilmiş olup, on yedi seviyeli eviricinin bir donanım prototipi performansını doğrulamak için yapılmıştır. Sonuçlar, önerilen topolojilerin yüksek verimlilik ve kaliteli çıkış ile amaçlanan performansa ulaştığını göstermektedir. Kademeli H-köprüsü tasarımları da dahil olmak üzere alternatif çok seviyeli evirici topolojileriyle yapılan karşılaştırmalı analiz, önerilen eviricilerin üstün verimliliğini ve maliyet etkinliğini doğrulayarak onları çok seviyeli evirici teknolojisinde gelişmiş çözümler olarak konumlandırmaktadır.

Anahtar Kelimeler: Bağlı İndüktör, Çok Seviyeli Evirici (MLI), Anahtar Sayısı.

To the one who spent his life with a smile on his face—your soul, **my father**.

To my dear departed flower, **my mother**.

To the one who lives on in my heart, **my big brother**.

To those whose strength and support continue to uplift me, **my younger brothers**.

To the butterfly that flutters among the spring flowers, filling my life with vibrant colors of joy **Fatema.**

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All my love and appreciation go to those who celebrate our successes and those bound by loyalty and love. I extend my deepest gratitude to the relatives who stood by my side—**Karawan**, **Rajwan**, and **my aunt Ahlam**. Your kind wishes, support, and constant encouragement have helped me navigate this stage of my life. I sincerely thank you, with the utmost respect, for being an essential part of this journey.

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ABBREVIATIONS

NPC	Neutral point clamped
FC	Flying capacitor
CHB	Cascaded h-bridge
MLIs	Multilevel inverters
THD	Total harmonic distortion
EVs	Electric vehicles
RESs	Renewable energy systems
HVDC	High-voltage direct current
FACTS	Flexible ac transmission systems
N_{Level}	Number of voltage levels
C_{switch}	Cost of the switch
C_{total}	Total cost
C_L	Cost of the coupled inductor
Ap	The area product
Pc	Power for the coupled inductor
f_{sw}	Switching frequency
J	Current density
B_m	Flux density
K_u	Window utilisation
K_f	Waveform coefficient
N_{Cell}	The number of individual inverters
CII	Coupled inductor inverter
L	Self-inductance
Lσ	League inductance
M	Mutual inductance
KCL	Kirchhoff's current law
k	Coupling coefficient
TSV	Total standing voltage
PWM	Pulse width modulation
Vref	Reference signal
$\mathbf{I_{strss}}$	Current stress
$\mathbf{N_{DC}}$	Number of DC voltage sources
$\mathbf{N_S}$	The number of IGBTs/MOSFETs
$\mathbf{N_{GD}}$	Number of gate driver circuits
$\mathbf{N_L}$	Number of coupled inductors
$\mathbf{N_C}$	Number of capacitors

1. INTRODUCTION

1.1. Overview

In recent times, the use of multilevel inverters has attracted considerable interest because of their capability to generate high-quality output voltages while minimizing harmonic distortion and enhancing power conversion efficiency [1]. These inverters employ multiple voltage levels to create the desired waveform, making them well-suited for diverse applications such as renewable energy systems, electric vehicles, and high-power motor drives [2].

Typically, there exist three commonly recognized and traditional configurations for multilevel inverters Diode clamped, also known as neutral point clamped (NPC), Capacitor clamped, also known as flying capacitor (FC), Cascaded H-bridge (CHB) [3] [4]. Researchers aim to develop novel inverter topologies that can achieve higher voltage levels while minimizing the component count. This approach aims to reduce the cost while ensuring improved power quality [5].

1.2. Literature Analysis

Beside the three well-known multilevel inverter categories, various topologies of multilevel inverters have been presented in the literature which mainly focus on reducing the number of power electronic devices [7-15]. A different category of multilevel inverters is based on the addition of some passive elements such as coupled inductors to enhance their performance. Coupled windings is a passive circuit component with multiple windings that are magnetically coupled together. When it is integrated into a multilevel inverter, causes boosting output voltage or current [6], the

11-level inverter with one DC source presented in [7] owns the ability to increase the output voltage while reducing the switches' current due to using two different coupled windings, The proposed topology in [8] introduced a new five-level inverter by using less number of switches, smaller filter size, and the reduction of the current flowing by the switches that are connected directly to the windings of coupled inductors. A nine-level inverter with three coupled inductors and one DC source is proposed in [9]. In [10] a single-phase 5 Level-active-neutral-point-clamped with coupled-inductor (5L-ANPC-CI) is presented by using one DC-source and two capacitors. In [11] four distinct topologies are presented, each featuring the integration of a coupled inductor. These configurations collectively produce a nine-level output, employing two DC sources. The number of power switches across these topologies varies, ranging from eight to ten. Seventeen-level cascaded H-Bridge multilevel inverter topology based on a nine-level MLI circuit is proposed in [12] with four DC sources, four capacitors, twelve switches, and additional two bidirectional switches. While [13] proposed a seventeen-level inverter composed of essential components, including a double-mode switched-capacitor (SC) unit, a T-type unit supplied by flying capacitors (FC), a half-bridge, and a set of complementary operation switches, and one bidirectional switch. In [14] a seventeen-level MLI for high-power applications are produced by using four DC sources and two bidirectional switches in addition to ten unidirectional switches. Another seventeen-level was presented in [15] using two coupled inductors with two DC sources and twelve switches.

In response to the limitations observed in the previously mentioned configurations, this research produces two topologies based on coupled inductor with less number of components

1.3. Thesis objective

This thesis aims to introduce a novel topology for a multilevel inverter, leveraging coupled inductors to generate more levels by using less number of components. The incorporation of coupled inductors in the topology serves to mitigate total stand voltage and current stresses on the switches while concurrently reducing the overall number of semiconductors utilized in the circuit, in contrast to analogous topologies. Through comprehensive simulation studies and experimental validation, this research substantiates the efficacy of the proposed approach.

1.4. Thesis outline

in this chapter an introduction to multilevel inverter with literature review of other topologies.

chapter two introduces the topologies of the multilevel inverter and focuses on coupled inductor inverter, additionally the PWM modulation techniques.

chapter three is dedicated to presenting the proposed seventeen-level and five-level inverter based on coupled inductors. Describe the topologies in detail, including the configuration of coupled inductors and the selection of suitable PWM modulation techniques. Provide cost and power loss of the proposed inverters. Include a comparative study with existing topologies to demonstrate the advantages of the proposed approach. Finally, outline the design process for coupled inductors tailored to the proposed inverter.

Chapter Four presents the simulation studies for both seventeen-level and five-level topology and experimental results on the seventeen-level inverter.

chapter five shows the conclusion of the thesis

2. INTRODUCTION TO MULTILEVEL INVERTER

In this section, the features of multilevel power inverters are outlined. Different multilevel topologies are evaluated, considering their advantages and disadvantages. the operation principle of the coupled inductor with its equations is investigated. Additionally, the advantages of using coupled inductor in multilevel inverters have been discussed. various PWM modulation techniques designed for these inverters are summarized. Finally, several applications of multilevel inverters are elucidated.

2.1. Multilevel inverter

Multilevel inverters have become indispensable components in various power electronic applications, particularly in medium and high-voltage scenarios [16] [17].

In the design of Multilevel Inverters (MLIs), a principal consideration revolves around the total count of components, encompassing power switches, driver circuits, and DC sources within the fundamental structure. This emphasis stems from the direct correlation between the overall system cost and the aggregate number of components utilized [7].

Conventional two-level power inverters necessitate additional components like transformers or passive filters to achieve sinusoidal waveforms. Multilevel inverters (MLIs) were developed to generate staircase output voltages, thereby reducing stress on power semiconductors [18].

the origin of the term "multilevel" can be traced back to the introduction of the three-level converter [19]. Subsequently, a plethora of multilevel converter topologies have been devised. Multilevel inverters generate a stepped voltage waveform that

closely approximates a pure sinusoidal signal. This waveform typically exhibits lower total harmonic distortion (THD) compared to a two-level voltage waveform [20].

In recent times, multilevel inverters have emerged as cost-effective power electronic topologies with a wide array of applications. They find utility in various systems, including, electric vehicles (EVs), renewable energy systems (RESs), high-voltage direct current (HVDC) transmission, motor drives, marine propulsion systems, and flexible AC transmission systems (FACTS) [21].

2.2. Multilevel inverter structures

Typically, there exist three commonly recognized and traditional configurations for multilevel inverters Diode clamped, also known as neutral point clamped (NPC), Capacitor clamped, also known as flying capacitor (FC), Cascaded H-bridge (CHB) [3] [4]. Each of these configurations caters to specific needs and applications, contributing to the versatility and adaptability of multilevel inverter technology [22].

2.2.1. Cascade H-bridge

The idea of multilevel inverters was first introduced in 1975 [19] by Baker and Bannister, This topology is commonly referred to as the cascaded H-bridge (CHB) multilevel inverter, which employs several DC sources.

Fig. 2-1 shows A full H-bridge topology comprising two legs, with each branch accommodating two power semiconductor switches (MOSFET or IGBT). The midpoint of these legs is connected across the load, Every H-bridge inverter level can generate three distinct voltage outputs: +Vdc, 0, and -Vdc [23].

The cascaded H-bridge (CHB) inverter comprises two or more series-connected H-bridge cells each fed by independent voltage sources, as shown in Fig. 2-2. The total output voltage is obtained by the sum of each individual output voltage. Each inverter is able to produce three output voltage levels. The maximum number of voltage levels of the phase voltage (N_{level})is given by [21] [24] [25]:

$$N_{level} = 2N_{cell} + 1$$

where N_{cell} is the number of individual inverters.

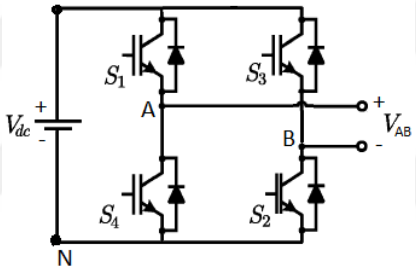


Fig. 2-1 Full H-bridge inverter

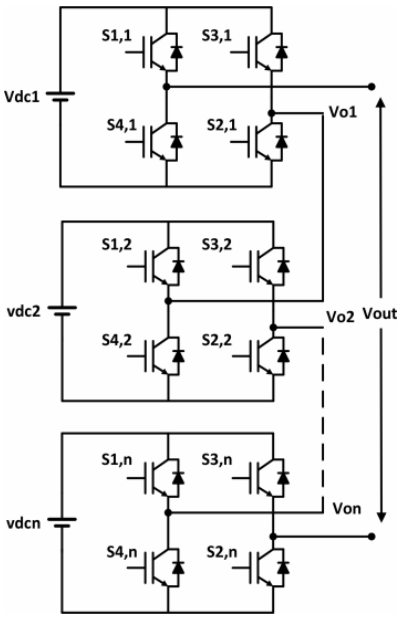


Fig. 2-2 Cascade H-bridge multilevel inverter

Among various other topologies, the cascaded H-bridge exhibits the potential to be highly reliable and possess superior fault tolerance. This is attributed to its modularity, which allows the inverter to sustain operation at reduced power levels even in the event of cell failure. Additionally, modularity facilitates straightforward stacking of cascaded multilevel inverters, making them well-suited for high-power and high-voltage applications. Nonetheless, the key distinction between this type of inverter and other multilevel inverter topologies lies in the achieved modularity through the cascading connection of H-Bridge cells [26].

2.2.2. neutral point clamped (NPC)

also known as diode clamped, was initially introduced in 1981 by Nabae, Takahashi, and Akagi [27] Fig. 2-3 shows the three-level neutral point clamp multilevel inverter. In this particular topology, the diode serves as the clamping device to regulate the DC bus voltage, thereby facilitating the generation of stepped output voltages [28] [29].

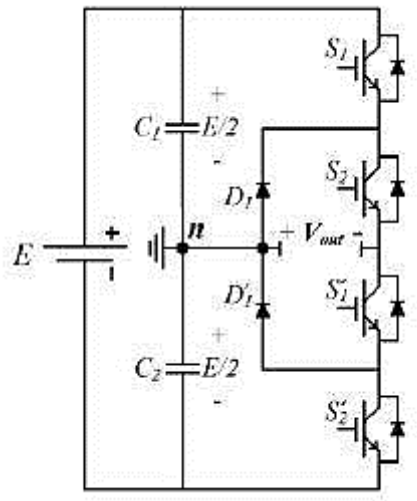


Fig. 2-3 Three-level neutral point clamp multilevel inverter

The attainment of multilevel output voltage is facilitated by employing clamping diodes and cascaded DC capacitors as depicted in Fig. 2-4. In this type of multilevel converter, A DC (Vdc) link consists of four capacitors connected to switches via clamping diodes. Consequently, each switch receives a voltage of (Vdc/4) across it. Assuming each clamping diode has the same voltage rating as the active device, this configuration necessitates ($N_{level}-1$)($N_{level}-2$) diodes per phase, where n denotes the number of levels in the output voltage of the inverter. As the number of levels (N_{level}) increases, the quantity of clamping diodes escalates, rendering the architecture cumbersome and impractical. For an n-level inverter, 2($N_{level}-1$) switching devices and ($N_{level}-1$) voltage sources are required. The shared DC bus among phases decreases capacitor requirements, and the capacitors can be pre-charged together in groups, which represents an advantage of this design [30] [31].

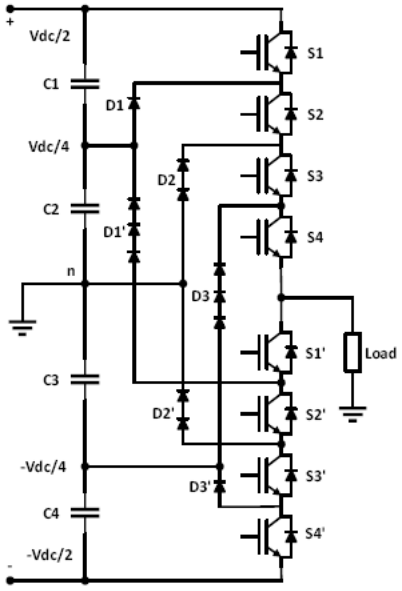


Fig. 2-4 five-level Neutral Point Clamped (NPC) multilevel inverter

Neutral Point Clamped inverters are highly efficient within the fundamental frequency switching range, making them particularly suitable for high-power medium voltage grid-connected converters [3]. The NPC topology offers an advantage by reducing the voltage stresses across the switching devices [32].

The primary disadvantage lies in the unequal voltage distribution among series-connected capacitors. Furthermore, a considerable number of diodes are necessitated for achieving higher-level outputs [33].

2.2.3. Flying Capacitor (FC)

Flying capacitor or capacitor clamped multilevel inverter, first introduced in 1992 by Meynard and Foch [34], The flying capacitor multilevel inverter bears resemblance to the diode-clamped MLI, albeit with a significant distinction lying in the utilization of capacitors for clamping instead of diodes, which constitutes a notable feature. In this topology, the DC side capacitors form a tree structure, wherein the voltage of each capacitor differs from that of the subsequent one. Another notable feature of the flying capacitor MLI is its capacity to provide switching redundancy within the phase, thereby facilitating the balancing of flying capacitors and requiring only one DC source [35] [36] [37].

The three-level flying capacitor inverter will indeed generate three distinct voltage levels, Fig. 2-5 shows the three-level flying capacitor multilevel inverter

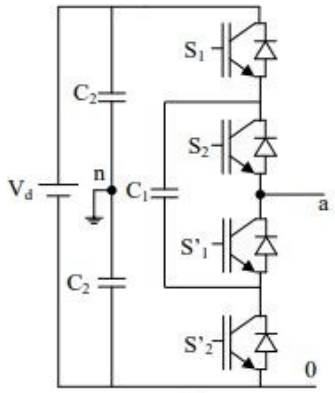


Fig. 2-5 three-level flying capacitor (FC) multilevel inverter

In a flying capacitor inverter with N_{Level} levels, the voltage across each capacitor and switch is Vdc. This configuration requires $(2N_{level}-2)$ switches and $(N_{level}-1)$ number of capacitors. Fig. 2-6 illustrate the five-level flying capacitor (FC) multilevel inverter

A drawback of this topology is the rating requirement for the capacitors, as they are subjected to large fractions of the DC bus voltage across them.

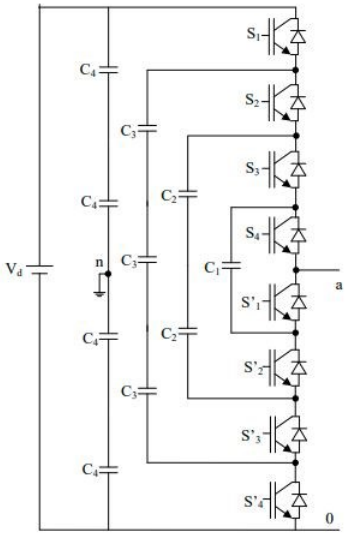


Fig. 2-6 five-level flying capacitor (FC) multilevel inverter

2.2.4. Coupled inductor inverter

In recent years, the literature has witnessed the introduction of alternative approaches to conventional topologies that can achieve higher voltage levels while minimizing the component count. This approach aims to reduce costs while ensuring the maintenance of power quality [38] [5]. To achieve this goal, the researchers focused on incorporating additional components into the circuit to enhance voltage levels, A coupled inductor is a type of inductor with multiple windings that are magnetically coupled together. When integrated into a multilevel inverter, the coupled inductor helps to boost voltage, increase the effective switching frequency, and the augmentation of the number of output voltage levels [38] [6].

The coupled inductor inverters are well-suited for diverse applications such as renewable energy systems, electric vehicles, and high-power motor drives [2].

2.2.4.1. Coupled Inductor Operation Principle

To uncover the underlying principle of the suggested multilevel inverter, the initial phase involves analyzing the function of the coupled inductors. Fig. 2-7 shows a pair of coupled inductors. [38]

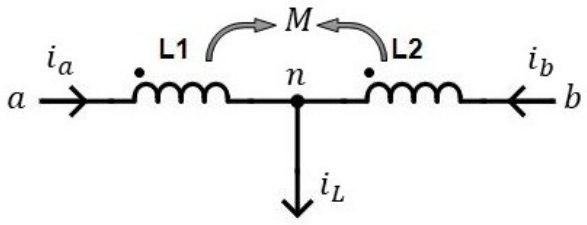


Fig. 2-7 pair of coupled inductors

when two nearby coils are magnetically linked together by a common magnetic flux they have the property of Mutual Inductance this Mutual inductance is represented by the symbol (M). while the pair of coupled inductors with the same number of turns, for that reason the self-inductance (L) and the league inductance ($L\sigma$) for the two winding are equal [39].

$$L_1 = L_2 = L \tag{II.1}$$

$$L\sigma_1 = L\sigma_2 = L\sigma \tag{II.2}$$

the voltage equations of coupled inductors are as follows: [38]

$$v_{an} = v_a - v_n \tag{II.3}$$

$$v_{an} = L\frac{di_a}{dt} - M\frac{di_b}{dt} \tag{II.4}$$

$$v_{an} = (L\sigma + M)\frac{di_a}{dt} - M\frac{di_b}{dt} \tag{II.5}$$

$$v_{bn} = v_b - v_n \tag{II.6}$$

$$v_{bn} = L\frac{di_b}{dt} - M\frac{di_a}{dt} \tag{II.7}$$

$$v_{bn} = (L\sigma + M)\frac{di_b}{dt} - M\frac{di_a}{dt} \tag{II.8}$$

By applying (KCL) Kirchhoff's current law to the node n, the following result is obtained:

$$i_a + i_b = i_L \tag{II.9}$$

From equations (2-3),(2-5),(2-8) and(2-9)), the following equation can be derived:

$$v_{an} + v_{bn} = v_a + v_b - 2v_n = L\sigma\frac{di_L}{dt} \tag{II.10}$$

To obtain the v_n voltage from equation (2-10):

$$v_n = \frac{v_a + v_b - L\sigma \frac{di_L}{dt}}{2} \tag{II.11}$$

The impact of leakage inductance is minimal and can neglected, load voltage can be written:

$$v_n = \frac{v_a + v_b}{2} \tag{II.12}$$

Where v_a and v_b are the voltages across the first winding (L_1) and the second winding (L_2) of the coupled inductor.

When two inductors are connected, the coupling coefficient (k) is commonly employed to gauge the degree of coupling intensity. The coupling coefficient is defined as follows: [40]

$$k = \frac{M}{\sqrt{L_1 L_2}} \tag{II.13}$$

as mention in equation (2-1) the self-inductance for the two windings are equal.

then (2-13) can be written:

$$k = \frac{M}{L} \tag{II.14}$$

If the inductors are not interconnected, the mutual inductance becomes null, resulting in (k) being equal to zero. Conversely, when the inductors are closely connected and there is no flux leakage, all the flux from one winding passes through the other one resulting in (k) equals one.

2.2.4.2. Coupled inductor advantages

Conventional multi-level converters encounter challenges such as circulating currents and intricate control circuitry. Undoubtedly, the escalation of the output voltage levels in the inverter inevitably entails an increase in the number of components within the circuit. Coupled inductor inverters (CII) offer a potential solution to these issues and have been extensively investigated for applications involving low and medium voltage [41].

This section delves into the advantages of the coupled inductor inverter across several dimensions. Firstly, the coupled inductor helps in reducing the current stress on the switches while maintaining high output current levels. the coupled inductor inverter appears as a useful solution to increase the output current, while the switched current through the high-frequency power devices is reduced. The coupled inductor is employed to halve the current flowing through the switches directly connected to its windings, thereby reducing it to half of the load current [7] [39].

Additionally, the coupled inductor assists in minimizing the voltage stress or the total standing voltage (TSV) on switches, thereby enhancing the overall reliability of the inverter. The concept of Total Standing Voltage (TSV) holds great importance in the decision-making process when choosing semiconductor switches. TSV reflects the sum of the highest blocking voltage experienced by individual semiconductor devices [42].

Moreover, the utilization of coupled inductors allows for a reduction in the number of inverter components while simultaneously increasing the number of output voltage levels. Another significant benefit outlined is that most inverters featuring coupled

inductors do not require additional filtering, simplifying the overall design and implementation process [8] [11].

2.3. Pulse width modulation (PWM) strategies

There are different classifications of pulse width modulation (PWM) techniques it can be organized into three types, the first one is carrier-based (CB-PWM) and The second one is Space Vector Pulse Width Modulation (SVPWM) and the third one is programmed PWM techniques [43]. Typically, PWM techniques require two signals: a reference signal and a carrier signal [44].

For carrier-based (CB-PWM) technique there is two type Level Shift PWM (LS-PWM) and Phase Shift PWM (PS-PWM), LS-PWM is a straightforward technique to implement. Three alternative LS-PWM strategies with varying phase relationships are available, for the three types, all carriers are in the same frequency and have equal magnitude [45] [46]:

- Alternate Phase Opposition Disposition (APOD): Each carrier waveform is out of phase with its adjacent carrier by 180 degrees.
- Phase Opposition Disposition (POD): All carrier waveforms above the zero reference point are in phase and for those bellow the zero are mirrored & flipped 180° from top (opposite peaks).
- Phase Disposition (PD): All carrier waveforms are in phase, the most widely used method as it provides load voltage and current with lower harmonic distortion.

SVPWM (Space Vector Pulse Width Modulation) is a unique fusion of the switch trigger sequence and pulse width control applied to the three-phase voltage source

inverter power device. Simultaneously, various research papers suggest that SVPWM is applicable and well-suited for conventional single-phase systems [47] [48].

The programmed PWM technique, rooted in selective harmonic elimination (SHE-PWM) criteria, is well-suited for high-power applications. However, a significant challenge in employing this approach lies in determining suitable switching angles, primarily due to the method's complexity in solving nonlinear equations. Nonetheless, its limitations in dynamic response and challenges in online implementation render it more appropriate for steady-state systems operating at high power [49] [50].

Among the three types of modulation techniques, carrier-based pulse width modulation (CB-PWM) methods are widely embraced [51].

2.4. Multilevel inverter applications

Based on the progress of multilevel inverters and advanced circuit topologies, the applications of multilevel inverters can be observed in the following areas:

Electric vehicles (EVs) leverage multilevel inverters to transform DC power sourced from batteries into AC power, driving the electric motor. This conversion process optimizes power utilization and control, thereby enhancing the vehicle's overall performance [52] [53].

In industrial motor drives, multilevel inverters regulate the speed and torque of AC motors utilized in diverse sectors such as pumps, compressors, and conveyor systems. They offer precise control, minimal harmonic distortion, and superior efficiency [54].

Multilevel inverters serve a pivotal role in renewable energy systems, particularly in solar and wind power generation. They facilitate the conversion of DC power

generated by solar panels or wind turbines into AC power, enabling grid connection or local consumption [55].

Furthermore, multilevel inverters are integrated into backup power systems to ensure uninterrupted operation of critical loads during mains supply failures. Their function is to deliver clean and stable AC power with minimal harmonic distortion [56].

In high-voltage direct current (HVDC) transmission systems, multilevel inverters are instrumental in converting DC power to AC power for long-distance transmission with minimal losses and voltage drops. They facilitate efficient power transfer between asynchronous AC grids or the integration of renewable energy sources into the grid [57].

2.5. Chapter Conclusions

This chapter provides a comprehensive overview of multilevel inverters, with a particular focus on their topologies and pulse width modulation techniques. The discussion encompasses various multilevel inverter configurations, including the coupled inductor inverter. Through an examination of these aspects, the chapter aims to elucidate the fundamental principles and operational strategies integral to multilevel inverter systems. Additionally, the chapter delineates several applications of multilevel inverters.

3. PROPOSED TOPOLOGIES WITH COUPLED INDUCTOR

This chapter presents the proposed topologies for both a seventeen-level and a five-level inverter, each utilizing coupled inductors. It provides a detailed analysis of the switching states and current flow characteristics within these circuits. The chapter also covers the pulse width modulation (PWM) techniques specifically developed for each inverter topology. Furthermore, it explores cost and power loss calculations, along with a comparative analysis against other multilevel inverter topologies. Lastly, the chapter discusses the design process of the coupled inductor, optimized for integration into both inverter systems.

3.1. Proposed seventeen-level inverter topology

Fig. 3-1 shows the proposed seventeen-level coupled inductor-based inverter, the circuit consist of eight unidirectional switches (S1, S2, S3, S4, S5, S6, S7, S8), one bidirectional switch (S9), three DC sources (Vdc, Vdc, and 2Vdc) and one coupled inductor.

along the switch pairs (S1, S2), (S3, S4) and (S5, S6), only one switch from each pair is required to be ON. In simpler terms, these switch pairs operate in complementary mode. The switch S3 is turned on during the positive half cycle and S4 operates complementary to the switch S3. Among the other three switches, i.e., S7, S8, and S9, only one switch is turned on at the same time depending on the desired output voltage level.

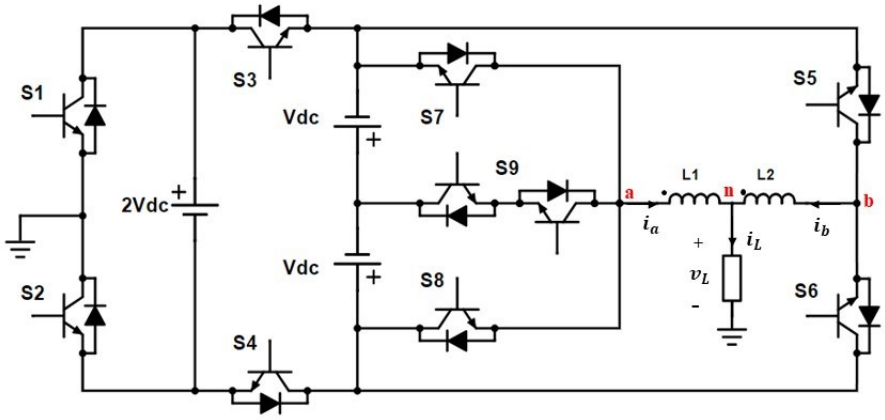


Fig. 3-1 The proposed seventeen-level inverter with coupled inductor

There are 24 switching states (SSs) to generate seventeen levels at the output as shown in TABLE 3-I. The number (1) represents the ON state of one switch and (0) represents the OFF state. The positive and the negative half cycle are symmetrical with respect to the output voltage. the switching states (SS_1-SS_8) are generating the positive half-cycle voltage across the load. the switching states (SS_{10}-SS_{17}) are generating the negative half-cycle voltage across the load. As shown in the table, the switching state (SS_9) is related to zero voltage level.

TABLE 3-I PROPOSED SEVENTEEN-LEVEL INVERTER SWITCHING STATES

Switching state	Output voltage	VL1	VL2	Switch condition								
				s1	*s2*	*s3*	*s4*	*s5*	*s6*	*s7*	*s8*	*s9*
1	4 vdc	4	4	0	1	1	0	0	1	0	1	0
2	7/2 vdc	3	4	0	1	1	0	0	1	0	0	1
3	3 vdc	4	2	0	1	1	0	1	0	0	1	0
		2	4	0	1	1	0	0	1	1	0	0
4	5/2 vdc	3	2	0	1	1	0	1	0	0	0	1
5	2 vdc	2	2	0	1	1	0	1	0	1	0	0
		2	2	1	0	1	0	0	1	0	1	0
6	3/2 vdc	1	2	1	0	1	0	0	1	0	0	1
7	1 vdc	0	2	1	0	1	0	0	1	1	0	0
		2	0	1	0	1	0	1	0	0	1	0
8	1/2 vdc	0	1	1	0	1	0	1	0	0	0	1
9	0	0	0	1	0	1	0	1	0	1	0	0
		0	0	0	1	0	1	0	1	0	1	0
10	-4 vdc	-4	-4	1	0	0	1	1	0	1	0	0
11	-7/2	-3	-4	1	0	0	1	1	0	0	0	1
12	-3 vdc	-2	-4	1	0	0	1	1	0	0	1	0
		-4	-2	1	0	0	1	0	1	1	0	0
13	-5/2 vdc	-3	-2	1	0	0	1	0	1	0	0	1
14	-2 vdc	-2	-2	0	1	0	1	1	0	1	0	0
		-2	-2	1	0	0	1	0	1	0	1	0
15	-3/2 vdc	-1	-2	0	1	0	1	1	0	0	0	1
16	-1 vdc	-2	0	0	1	0	1	0	1	1	0	0
		0	-2	0	1	0	1	1	0	0	1	0
17	-1/2 vdc	-1	0	0	1	0	1	0	1	0	0	1

Fig. 3-2 shows the switching states (SSs) current direction for the positive half cycle of the proposed seventeen-level inverter, in Fig. 3-2 (a) the SS_1 is presented. The depicted current flow shows the ON switches (S2, S3, S6, S8) for generating 4Vdc in which the voltage across each of the windings of the coupled inductor is 4Vdc.

Fig. 3-2. (b) shows the SS2 operation mode to generate 7/2Vdc where voltage equal to 3Vdc across the first winding L1 and 4Vdc is across the second winding L2.

Fig. 3-2. (c) shows the SS_3 operation mode to generate output voltage of 3 Vdc, with 4Vdc and 2Vdc across the first and the second winding (L1, L2) respectively.

Fig. 3-2. (d) shows the SS_4 operation mode to generate 5/2Vdc, where the voltage across the first and second windings of the coupled inductor is 3Vdc and 2Vdc, respectively.

In Fig. 3-2(e) the SS_5 current direction to generate the output voltage of 2Vdc, with 2Vdc across each of the windings of the coupled inductors.

Fig. 3-2. (f) shows the SS_6 operation mode to generate the output voltage of 3/2 Vdc, with 1Vdc and 2Vdc across the first and the second winding (L1, L2) respectively.

In Fig. 3-2(g) the SS_7 current direction generates zero Vdc on the first winding L1, and 2 Vdc on the second winding L2 gives the output voltage of Vdc across the load.

To generate half of Vdc (1/2 Vdc) the SS_8 in Fig. 3-2. (h) corresponds to the output voltage of 1/2Vdc in which the voltage on the windings of the coupled inducor is zero and Vdc.

In order to generate the zero output voltage, the switching combination is presented in Fig. 3-2. (i).

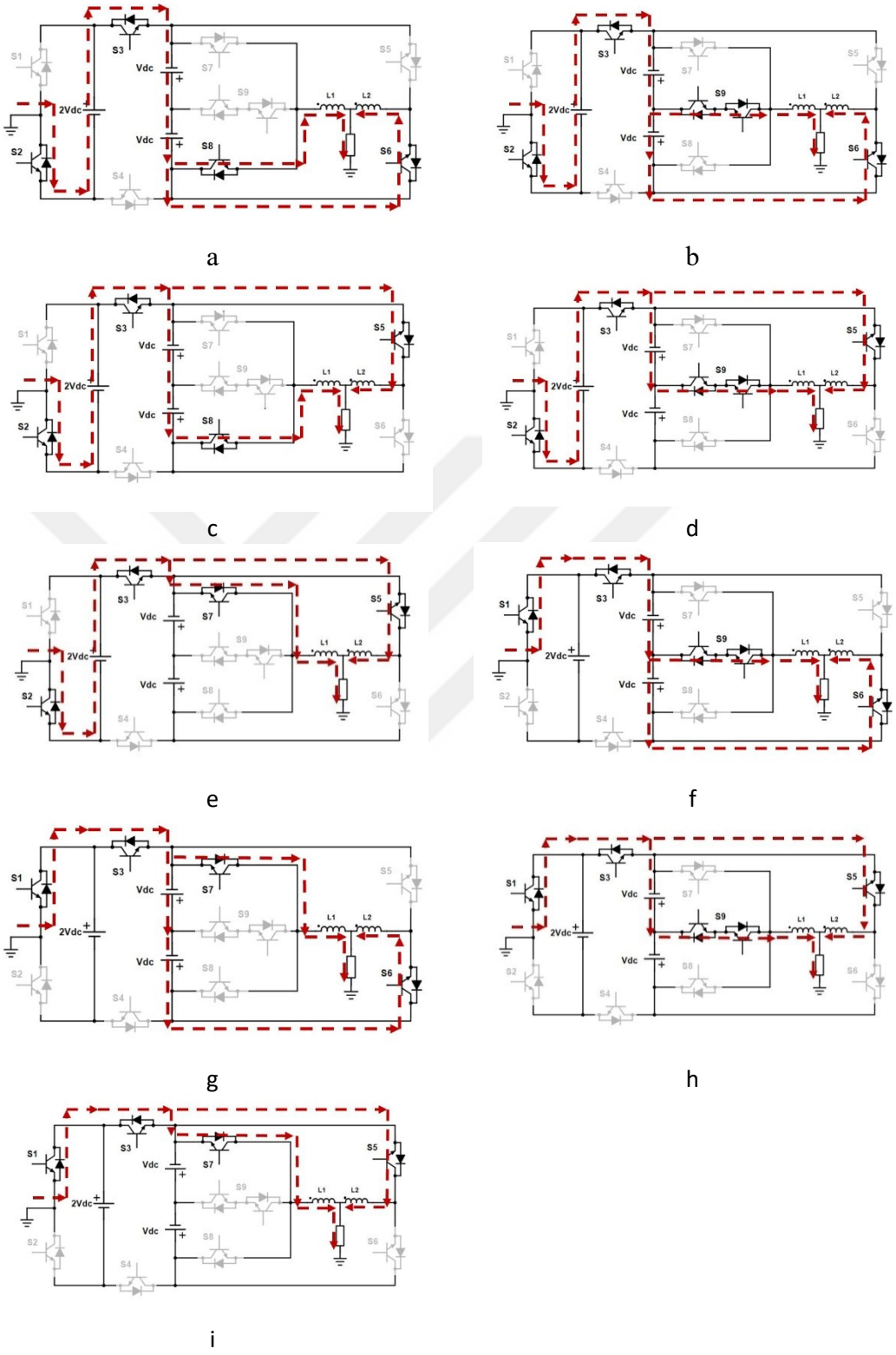


Fig. 3-2 The switching state (SS) current direction for the positive half cycle (a)SS1, (b) SS2, (c)SS3, (d) SS4, (e) SS5, (f)SS6, (g)SS7, (h)SS8, (i)SS9

Fig. 3-3 shows the switching states (SS_s) current direction for the negative half cycle of the proposed seventeen-level inverter, in Fig. 3-3 (a) the SS_{10} current direction to generate output voltage of -4Vdc, with -4Vdc across each winding of the coupled inductor.

Fig. 3-3. (b) the SS_{11} operation mode to generate output voltage of -7/2Vdc where voltage equal to -3Vdc is across the first winding L1 and -4Vdc is across the second winding L2.

Fig. 3-3. (c) shows the SS_{12} operation mode to generate output voltage of -3Vdc, with voltage equal to -2Vdc and -4Vdc across the first and the second winding (L1, L2) respectively.

Fig. 3-3. (d) shows the SS_{13} operation mode to generate output voltage of -5/2Vdc, where -3Vdc across the first winding L1 and -2Vdc across the second winding L2.

In Fig. 3-3(e) the SS_{14} current direction to generate output voltage of -2Vdc, In this switching state, the voltage across each of the windings of the coupled inductors is -2Vdc.

Fig. 3-3. (f) shows the SS_{15} operation to generate -3/2 Vdc, with -1Vdc and -2Vdc across the first and the second winding (L1, L2) respectively.

In Fig. 3-3(g) the SS_{16} current direction to generates zero Vdc on the first winding L1, and -2 Vdc on the second winding L2 gives the output voltage of Vdc across the load.

To generate half of Vdc (1/2 Vdc) the SS_{17} in Fig. 3-3. (h) shows the operation where the voltage equal to -Vdc is across the first winding and Zero Vdc is accross the second winding of the coupled inductor.

The second switching state of the Zero level is presented in Fig. 3-3. (i).

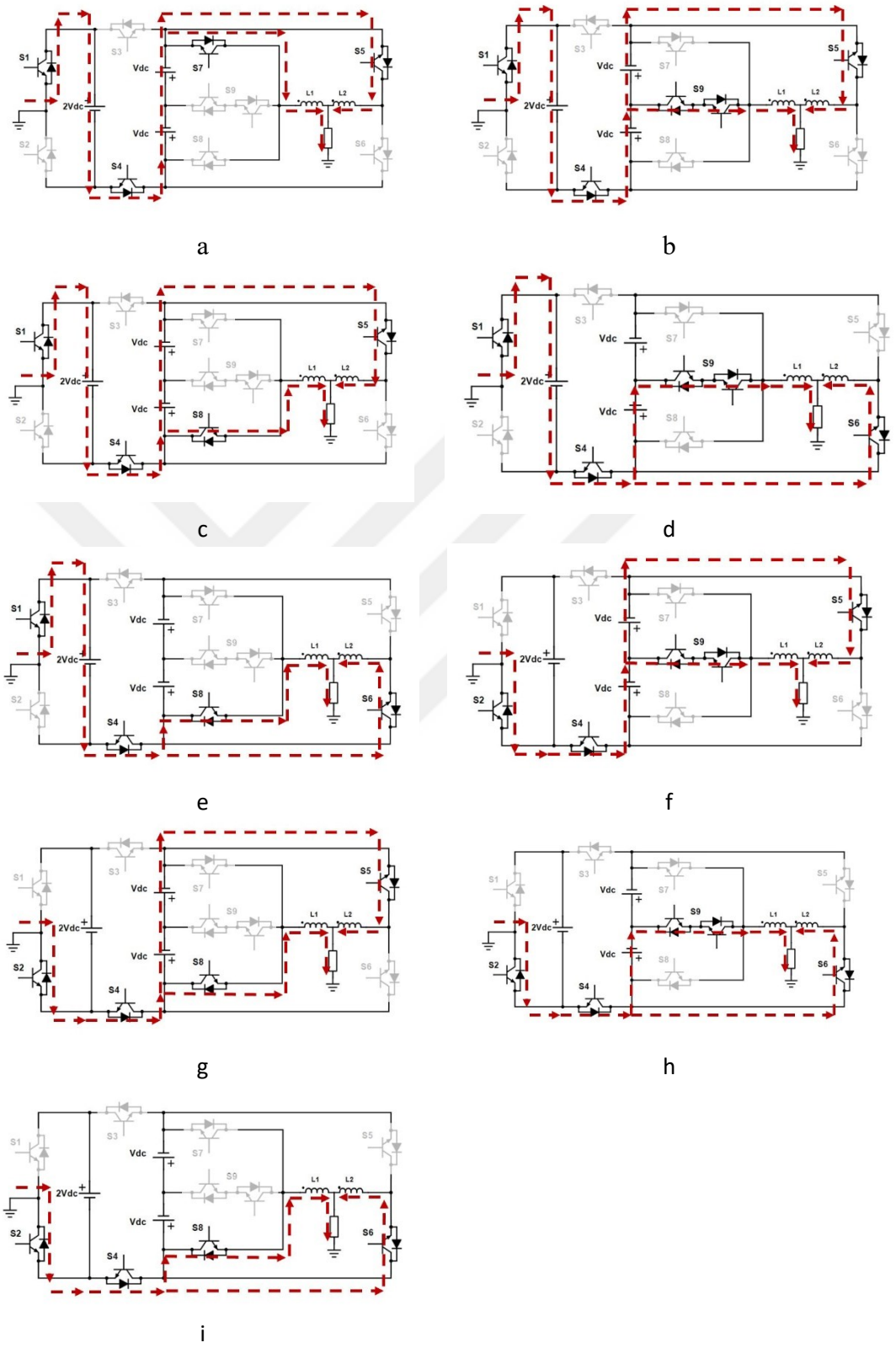


Fig. 3-3 The switching state (SS) current direction for the negative half cycle (a)SS10, (b) SS11, (c)SS12, (d) SS13, (e) SS14, (f)SS15, (g)SS16, (h)SS17, (i)SS9

3.1.1. The modulation strategy of the proposed seventeen-level inverter

The level-shifted pulse width modulation LS-PWM strategy is used to produce the seventeen level of the proposed inverter. Fig. 3-4 shows the modulation technique schematic of the proposed seventeen-level inverter.

Each modulation strategy required a reference signal and a carrier signal, A multilevel inverter with N-level requires 'N-1' triangular carriers to compare it with the reference signal. For a seventeen-level inverter, it required (16) carrier signal.

In this PWM strategy, only eight carriers are required, Which obviates the necessity for 16 carrier signals, this can be done by comparing the reference signal (Vref) with zero, to determine the positive part and the negative half cycle of the reference signal. The negative half-cycle of the reference waveform is represented as N, while the positive half-cycle is denoted by P.

The P signal is sent to the gates that operate for activating the switch during the positive half cycle, whereas the N signal is directed to the gates that operate during the negative half cycle.

as Fig. 3-4 shows the eight carriers (C1-C8) that are required to compare with the positive half of the reference signal (Vref), all carriers have the same peak-to-peak value, and the same frequency, all triangular carrier signals are located between (zero and 1) each carrier has 0.125 magnitudes, these triangular carriers are vertically disposed of such that the bands they occupy are contiguous. In other words, the triangular carrier signal (C1) has a minimum output level of zero and a maximum output level of 0.125, while the second triangular carrier signal has a minimum output level of 0.125 and a maximum output level of 0.25, At this rate, it proceeds following the remainder of triangular carrier signals.

The comparators' result along with the identified ranges of the reference signal (M1-M8), undergo processing through logic gates to generate the switching pulses for the switches.

(M1) is the region of the reference signal (Vref) that is located between zero and 0.125, while (M2) is located between 0.125 and 0.25, (M3) is located between 0.25 and 0.375, and so forth for the remaining region detection up to (M8).

The simulation results of the modulation technique for the proposed 17-level inverter are shown in Fig. 3-5 at the top of the figure shows all triangular carrier signals with the positive side of the reference sine wave, the frequency set to 10000Hz the rest of the Fig. 3-5 provide the output signal of logic gates (P1, P3, P5, P7, P9, P11, P13, P15).

Ensuring the deployment of the correct switching combinations is crucial to maintaining a balance between the currents flowing through the two branches of the coupled inductor and preventing the emergence of direct current (DC) components. For instance, the third switching state (SS3) in TABLE 3-I have two switching combinations to generate 3Vdc at the load, in the first combination, The voltage on one side of the coupled inductor will be 4Vdc, while the voltage on the other side is 2Vdc. Consequently, the average current on one side of the coupled inductor will increase and the average current on the other side will decrease. In the subsequent switching combination, the result will be reversed, thereby achieving a balance in current between the two branches of the coupled inductor.

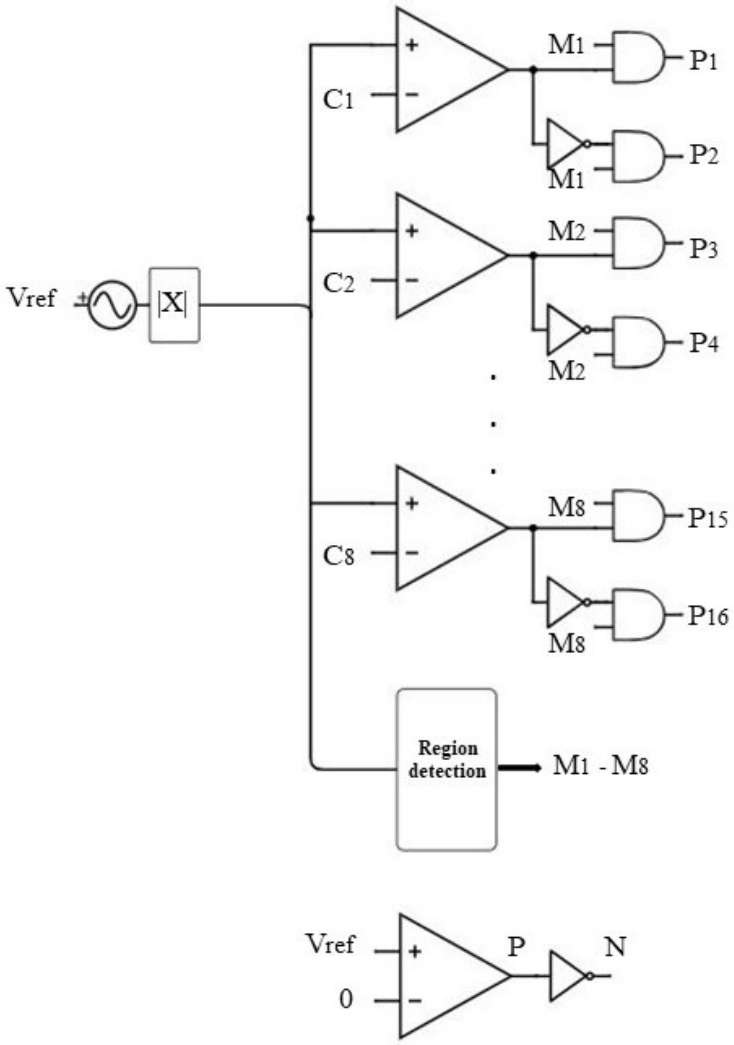


Fig. 3-4 Level-shifted pulse width modulation (LS-PWM) schematic for the proposed 17-level inverter.

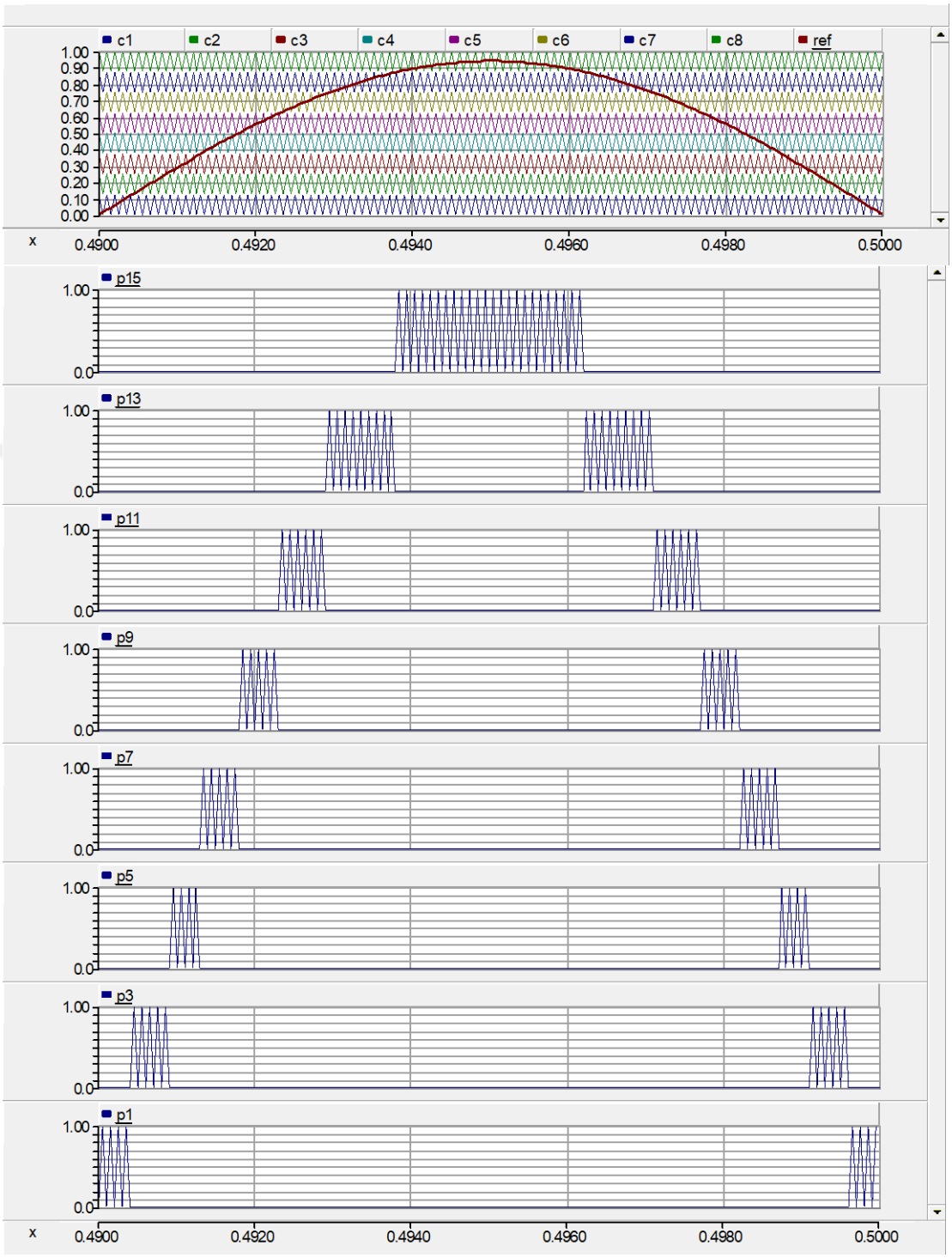


Fig. 3-5 Simulation result of the Level-shifted pulse width modulation (LS-PWM) for the proposed 17-level inverter

3.1.2. power loss calculations and efficiency analysis

Coupled inductor and power switch losses are the main losses in the circuit of the proposed inverter which are considered in this section. Power switch losses are commonly classified into conduction losses and switching losses. In an IGBT with an anti-parallel diode, both the transistor and the diode exhibit on-state resistance and on-state reverse voltage, leading to conduction losses. The conduction loss of an IGBT ($P_{C,IGBT}(t)$) and a diode ($P_{C,D}(t)$) is determined in accordance with the following calculations [58] [59]:

$$P_{C,IGBT}(t) = \left[V_{ICBT} + R_{IGBT} i^{\beta}(t)\right] i(t) \tag{3-1}$$

$$P_{C,D}(t) = \left[V_D + R_D i(t)\right] i(t) \tag{3-2}$$

In the preceding equations, V_{IGBT} and V_D represent the forward voltage drop of the IGBT and diode, respectively. Likewise, R_{IGBT} and R_D denote the equivalent resistance of the IGBT and diode, respectively, $i(t)$ the current that passes through the IGBTs and diodes at any time. while β is a constant associated with the specification of the IGBT. These parameters can be found in the device's datasheet since the selected power switches are IGBT (STGW30NC60VD) according to the assumed design values. The average conduction loss (P_C) of the switches is determined based on the number of switches (N_{sw}) that are in current path at any instant of time:

$$P_C = \frac{1}{2\pi}\int_0^{2\pi}\left[\sum_{j=1}^{N_{sw}=10}\left(P_{C,IGBT}(t) + P_{C,D}(t)\right)\right]dt = 35W \tag{3-3}$$

the conduction losses vary according to the current stress on each switch, the conduction losses for switches (S1, S2, S3, S4) are estimated to be 5 W each, as these

switches experience current stress equivalent to the output current. In contrast, switches (S5,S6,S7,S8, and S9) exhibit conduction losses of 2.5 W each, as the current stress on these switches is equal to half of the output current. Fig. 3-6.a illustrates the conduction losses of each switch expressed as a percentage of the total conduction losses. The calculation of switching losses hinges on evaluating the energy losses occurring during both turn-off and turn-on periods. To simplify the analysis, the linear variations of voltage and current for the switches during the switching period are taken into account. Based on this assumption, the following relationships can be formulated [58] [59]:

$$E_{off} = \int_0^{t_{off}} v(t) i(t) dt \tag{3-4}$$

$$E_{on} = \int_0^{t_{on}} v(t) i(t) dt \tag{3-5}$$

In the given equations, E_{off} and E_{on} represents the turn-off and turn-on losses of a switch, respectively. $v(t)$ and $i(t)$ are the voltage and current during switching transition, respectively. t_{off} and t_{on} denote the turn-off and turn-on time of the switch, respectively.

The total switching losses P_{sw} is determined by considering the energy losses incurred during the turn-on and turn-off states of all switches. Hence, we have [58] [59]:

$$P_{sw} = f_{sw} \sum_{j=1}^{N_{sw=8}} \left(E_{on} + E_{off} \right) = 1.06W \tag{3-6}$$

In the equation provided, f_{sw} denotes the switching frequency.

The switching losses for each switch vary depending on the voltage and current stresses experienced by each component. Switches S1 and S2 exhibit switching losses

of 0.25 W each. Switches S3 and S4, operating at the fundamental frequency, have identical switching losses of 0.0025 W each. The switching losses for switches S5, S6, S7, and S8 are 0.125 W each. Finally, switch S9 incurs a switching loss of 0.0675 W. Fig. 3-6.b presents the switching losses for each switch as a percentage of the total switching losses.

Additionally, since switches S3 and S4 operate at the fundamental frequency (50 Hz), their switching losses are disregarded.

Coupled inductor losses encompass both core losses (P_{core}) and copper losses (P_{cu}).

to find the core losses, the watts per kilogram, W/K should be calculated first as follows: [60].

$$W/K = k(f)^{\omega}(B)^{n} \tag{3-7}$$

Where f is the fundamental frequency, B is the operating flux density. according to the selected core EE-60, the core loss equation factors are:

$k = 7.69\times10^{-2}, \omega = 1.06, n = 2.85$

Then the coupled inductor core losses are obtained as

$$P_{core} = (W/K)(W_{core})(10^{-3}) = 5.5W \tag{3-8}$$

To evaluate the copper losses, the wire resistance for both the first and second windings of the coupled inductor must be calculated. Based on the design specifications, the appropriate wire size for the coupled inductor is determined to be AWG#15. Consequently, the equivalent resistance, measured in micro-ohms per centimeter, is as follows:

$$\left(\frac{\mu\Omega}{cm}\right) = 104.3 \tag{3-9}$$

Then the wire resistance for the first winding (R_{L1}) and second windings (R_{L2}) of the coupled inductor can be calculated as follow:

$$R_{L1}, R_{L2} = MLT\left(\frac{N}{2}\right)\left(\frac{\mu\Omega}{cm}\right)\left(10^{-6}\right) = 0.039\Omega \tag{3-10}$$

Since the number of turns for one winding is half of the total number of turns N .

next, the copper losses can be expressed as

$$P_{cu} = R_{L1} i_{rms,L1}^2 + R_{L2} i_{rms,L2}^2 = 0.78W \tag{3-11}$$

where $i_{rms,L1}$ and $i_{rms,L2}$ are the RMS current values of the first and second windings of the coupled inductor, respectively.

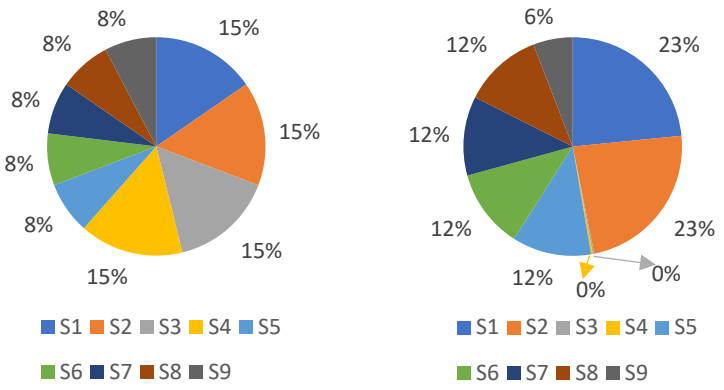
The total loss P_{loss} of the multilevel inverter is the sum of conduction losses, switching losses and coupled inductor losses, expressed as follows:

$$P_{loss} = P_c + P_{sw} + P_{core} + P_{cu} = 42.33W \tag{3-12}$$

Finally, the efficiency (η) of the multilevel inverter is compute based on the output and input power of the multilevel inverter P_{out} and P_{in} , respectively as follow:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \approx 97\% \tag{3-13}$$

The power loss values obtained from the simulation closely correspond with those derived from the theoretical analysis. Given an output power of 1800 W, this results in an efficiency of 97%.



(a) (b)

Fig. 3-6 power switch losses (a)conduction losses, (b)switching losses.

3.1.3. Comparison Study

In this section, the comparison study of the proposed seventeen-level inverter topology against the conventional inverter topologies, with the same number of output voltage levels, is presented. The aim of this study is to present the distinctive features and also the advantages of the proposed design.

TABLE 3-II provides and summarizes the results of the comparative analysis between the proposed seventeen-level inverter (P) with cascade H-Bridge multilevel inverter (CHB) and relevant inverters topologies, This table is distinguishing the key components count, including the number of DC voltage sources (N_{DC}), the number of IGBTs/MOSFETs (N_S), number of the necessary gate driver circuits (N_{GD}), coupled inductors (N_L), capacitors (N_C), and also the total current stress (I_{stress}) and total standing voltage (TSV) of the switches per-unit taking the voltage of each step (Vdc) as the base value.

As depicted in TABLE 3-II the proposed topology requires fewer DC sources (N_{DC}) than the cascaded H-bridge and other listed topologies in the table.

Additionally, it requires considerably less number of power switches (N_S) to generate a seventeen-level output than other configurations, which reduces the number of required gate driver circuits (N_{GD}) and the overall complexity and volume of the inverter. Regarding the number of capacitors (N_C), in the structure of the proposed topology, the capacitor is not used, resulting in simple control strategy in comparison with the ones using capacitors presented in [12] and [61], which uses four capacitors that require the complicated control strategy for capacitor balance. The proposed topological configuration employs a singular coupled inductor, setting it apart from the remaining structural designs which notably lack the presence of coupled inductors. This characteristic elucidates the notable disparity in the quantity of Direct Current (DC) sources utilized in the other topologies, as discerned within the provided table. As evident from the tabular data, it is noteworthy that the TSV of the proposed inverter is markedly lower in comparison with all other topologies presented in the table. The other significant advantage of the proposed topology is related to the total current stress. As depicted in the table, the total current stress of the proposed topology is impressively less than that of all presented in the table. This exclusive feature not only affects the cost of the switches to be lower, but also it cause to decrease the switch conduction losses and so increase the efficiency of the proposed inverter. these features are consequence of using the coupled inductor in the proposed design. Employing the coupled inductor in the proposed MLI elucidates the notable disparity in the count of components and DC voltage sources with respect to utilized ones in the other topologies presented in the table. The coupled inductor facilitates an increase in the number of voltage levels, thereby mitigating the current and voltage stress experienced by most of the switches.

The cost of Multilevel Inverters (MLIs) constitutes a crucial parameter necessitating comparison. Therefore, the cost assessment for each circuit element within the Multilevel Inverter (MLI), encompassing power electronic switches (IGBTs or MOSFETs) and coupled inductors, is meticulously conducted as follows [7]:

$$C_{total} = (VA)_{switch} C_{switch} + (VA)_L C_L \tag{3-14}$$

In above equation, C_{total} is the total cost of the components, C_{switch} is the cost of the switch/ (VA) and C_L is the cost of the coupled inductor/ (VA)

The total Volt-Amperes (VA) of the switches is denoted as $(VA)_{switch}$. Simultaneously, $(VA)_L$ represents the total Volt-Amperes of the coupled inductors. In the context of the proposed seventeen-level inverter, the total VA_{switch} is 4.25 times the output maximum VA. Given that the magnitude of the rated output current and voltage are $I_{o,m}$ and $V_{o,m}$ respectively, Equation (3-14) can be expressed as follows:

$$C_{total} = 4.25 V_{o,m}\ I_{o,m} C_{switch} + V_{o,m} I_{o,m} C_L \tag{3-15}$$

By defining the maximum output Volt-Ampere of the inverter as VA_{max}, the ensuing equation can be derived as follows:

$$C_{total,proposed} = \left[4.25 C_{switch} + C_L\right] VA_{\max} \tag{3-16}$$

The cost of the proposed inverter is compared with a pertinent topology presented in [62], As the presented topology features a nine-level output, to ensure a fair comparison, parameters are normalized by the output rated VA.

TABLE 3-III illustrates the comparison results. From which it is evident that the proposed structure exhibits a lower ratio of coupled inductor and count of power switches concerning the number of levels, as compared to the topology presented in [62]. Additionally, the presented structure employs eight diodes, whereas the proposed

structure does not require any diode. it is discernible that, from an economic standpoint, the proposed structure is more cost-effective compared to the referenced topology.

TABLE 3-II COMPARATIVE ANALYSIS OF THE PROPOSED INVERTER WITH RELEVANT SEVENTEEN-LEVEL INVERTERS

Topology	N_{DC}	N_S	N_{GD}	N_L	N_C	**TSV**	I_{strss}
[42]	8	20	14	-	-	42	20
[63]	8	20	20	-	-	40	20
[64]	5	15	15	-	-	56	15
[12]	4	16	14	-	4	36	16
[61]	2	14	14	-	4	40	14
CHB	8	32	32	-	-	32	32
proposed (P)	3	10	6	1	-	21	7

TABLE 3-III COST COMPARISON OF THE PROPOSED TOPOLOGY WITH RELEVANT INVERTER

Topology	N_{LEVEL}	N_S	N_S/N_{LEVEL}	N_L	N_{diode}	**Total Cost**
[62]	9	8	0.89	3	8	$C_{total.[60]} = \left[4C_{switch} + 4C_{diode} + 3C_L\right]VA_{\max}$
proposed (P)	17	10	0.59	1	-	$C_{total,proposed} = \left[4.25C_{switch} + C_L\right]VA_{\max}$

3.1.4. Coupled Inductor Design

Based on the coupled inductor design calculation in [7] certain assumptions have been made to develop the coupled inductor design for the proposed inverter, as detailed in TABLE 3-IV The value of the apparent power for the coupled inductor is as follows:

$$Pc = Vab, rms \times Iab, rms = 1800W \tag{3-17}$$

Next, the calculation of the area product (Ap), which serves as the core characteristic for selecting an appropriate core, proceeds as follows:

$$Ap = \frac{Pc \times 10^4}{K_f K_u B_m f_{sw} J} = 43.1 cm^4 \tag{3-18}$$

Based on the area product (Ap) value, the closest ferrite core to that, is EE-60, Ac according to the datasheet EE-60 is equal to 7.35 cm^2. Subsequently, the calculation of the number of turns for the coupled inductor in the proposed inverter is performed as follows:

$$N = \frac{Vab, rms \times 10^4}{K_f B_m f_{sw} A_c} = 53.45\, turns \tag{3-19}$$

the number of turns for one winding of the coupled inductor is half of N. The equivalent inductance for the coupled inductor is computed using the following method:

$$L_{CI,eq} = A_L N^2 = 19.4mH \tag{3-20}$$

where A_L is core permanence and is available by given data of EE-60.

So, by ignoring the leakage inductance of the windings of coupled inductor, the self and mutual inductances of the windings (L_1, L_2 and M) would be the same and then, the inductance values of coupled inductor are equal [65]:

$$L_1 = L_2 = M = \frac{L_{CI,eq}}{4} = 4.85mH \tag{3-21}$$

To evaluate the ripple current of the coupled inductor, we utilize the following equation:

$$i_{ripple,\max} = \frac{Vdc\, T_S}{4M} \tag{3-22}$$

Whereof the maximum voltage value across the coupled inductor windings is Vdc, so the inductance M should have the following condition:

$$M \geq \frac{Vdc\, T_S}{i_{ripple,\max}} \tag{3-23}$$

By assuming that the current ripple is 8% of the maximum current in the windings of the coupled inductor, the computed inductance as given in equation (3-21)remains applicable for equation (3-23).

Additionally, the windings bare wire area ($A_{w(B)}$) calculated by equation:

$$A_{W(B)} = \frac{Ia, rms}{J} = 0.016\,cm^2 \tag{3-24}$$

And the wire diameter (D_{AWG}) is obtained by:

$$D_{AWG} = \sqrt{\frac{4A_{W(B)}}{\pi}} = 1.4\,mm \tag{3-25}$$

Then, considering the data table of wire given in [65] the wire size that closely aligns with the calculated value corresponds to AWG #15.

TABLE 3-IV DESIGN SPECIFICATION FOR THE COUPLED INDUCTOR

The maximum voltage of the coupled inductor (Vab max)	200 V
The maximum current of the coupled inductor (Io)	9 A
operating frequency (f_{sw})	10 KHz
current density (J)	400 A/cm^2
flux density (B_m)	0.09 T
window utilisation (K_u)	0.29
waveform coefficient (K_f)	4

3.2. Proposed five-level inverter topology

Fig. 3-7 shows the proposed five-level coupled-inductor inverter. As the figure shows, the inverter consists of one dc voltage source, 4 power switches (S1, S2, S3, and S4), two diodes (D1 and D2), and one coupled inductor. S1 and S2 function at the fundamental frequency and operate complementary. To elaborate, one is activated during the positive half cycle of the output voltage, while the other is engaged during the negative half cycle. These two switches have been incorporated into the topology to ensure the availability of both negative and positive output voltage, a requisite for an

inverter's functionality. S1 is activated during the negative half cycle of the output voltage, while S2 is activated during the positive half cycle.

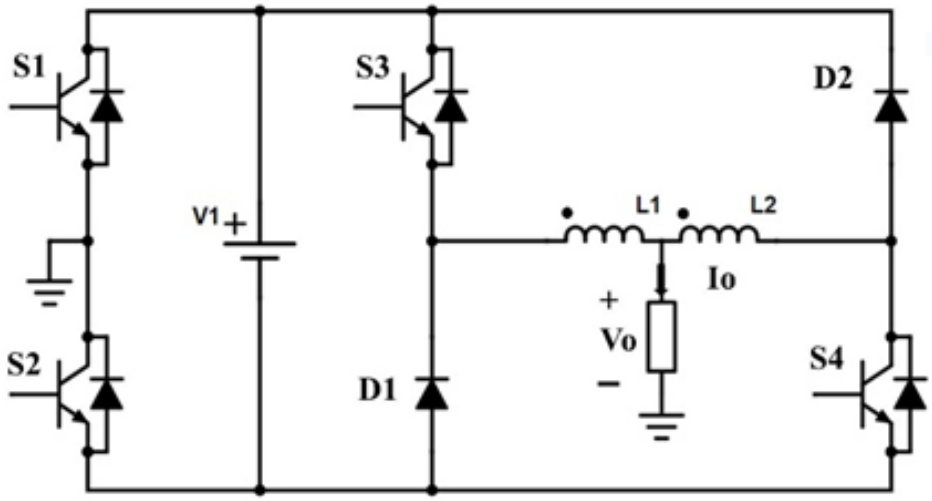


Fig. 3-7. Proposed five-level inverter with coupled inductor

there are 5 switching states (SSs) to generate five levels at the output (+V, +1/2V, 0, -1/2V, and -V) as shown in TABLE 3-V. Fig. 3-8 shows the five possible switching states (SSs):

- SS1: during this state, S2 and S3 are ON, the voltage across the first winding is Vdc while there is no voltage across the second winding of the couple inductor, therefor the voltage across the load will be Vdc, Fig.3-7. (a). shows the SS1 current direction to generate Vdc
- SS2: in this state, S2, S3, and S4 are ON, the voltage across the first winding of the coupled inductor is Vdc while the voltage across the second winding is Zero, according to (8) the voltage across the load terminal is Vdc/2, Fig.3-7. (b). displays the SS2 current direction to generate Vdc/2.
- SS3: the switches S2 and S4 are ON, diode D1 is conducting, according to that the voltage across the first and the second winding is zero, the inverter generates an

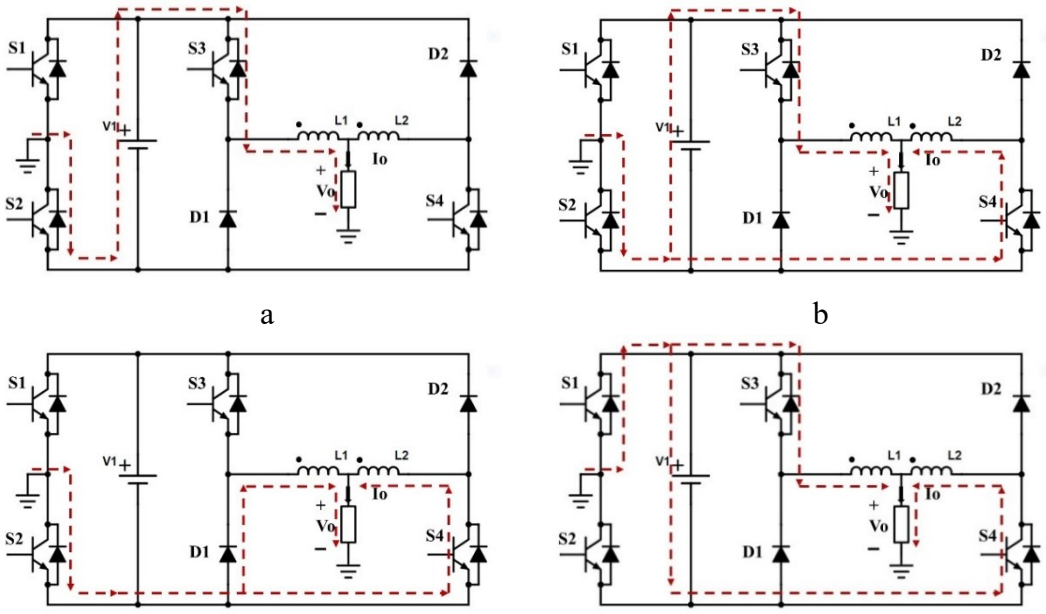
output voltage equal to zero, Fig. 3-7. (c). shows the SS3 current direction to generate the zero level.

• SS4: during this state, S1, S3, and S4 are ON, the voltage across the first winding is zero while the second winding of the coupled inductor is -Vdc, according to (8) the output voltage is -Vdc/2, Fig.3-7. (d). shows the SS4 current direction to generate -Vdc/2.

• SS5: in this state, S1 and S4 are ON, that implies -Vdc will pass through the second winding, with no voltage across the first winding according to that the voltage across the load is -Vdc, Fig.3-7. (e). shows the SS5 current direction to generate -Vdc.

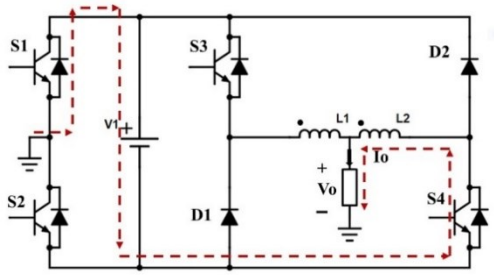
TABLE 3-V PROPOSED FIVE-LEVEL INVERTER SWITCHING STATES

Switching State SSs	**Switch condition**				**Output voltage**
	S1	*S2*	*S3*	*S4*	
1	0	1	1	0	+V
2	0	1	1	1	+1/2V
3	0	1	0	1	0
4	1	0	1	1	-1/2V
5	1	0	0	1	-V



a b

c d



e

Fig. 3-8 The switching state (SS) current direction for the proposed five-level inverter topology.

3.2.1. The modulation strategy of the proposed five-level inverter

In this section, the modulation Technique due to the structure of the proposed five-level inverter in Fig. 3-7. is provided. The switch pair (S1 & S2) are complementary, one switch is required to be ON in each state, S1 operates on the negative half levels and S2 operates on the positive half levels. The control of S1 and S2 is obtained by using a signal generator with fundamental frequency, and a duty cycle of %50, Indeed, its value is 1 during one switching cycle and returns to zero in the subsequent consecutive switching cycle. both signal generators have the same amplitude as (0 to 1) for each switch but there is a phase shift of 180 degrees for the signal generator of switch S1 to operate on the negative half-cycle. The control of the switches S3 and S4 is based on the phase shift pulse width modulation technique, two carriers with the same frequency and amplitude are placed. But there is a phase shift of 180 between the two carriers.

The first carrier has a 180-phase shift as indicated in TABLE 3-V, S3 is "ON" at the positive half levels by comparing it with the absolute value of the reference waveform (V_{ref}), the comparator's output is processed through logic gates to implement

the specified criteria and generating the switching pulses required for the switch S3. The second carrier has a zero phase to ensure the "ON" state of S4 during the negative half levels. Additionally, the carrier signal is compared with the absolute reference waveform (V_{ref}), and the resultant output is directed to the logic gates for generating the switching pulses for S4. Fig. 3-9. illustrates the block diagram of the modulation logic of the proposed inverter. The reference waveform's positive half-cycle is denoted as P, while its negative half-cycle is represented by N.

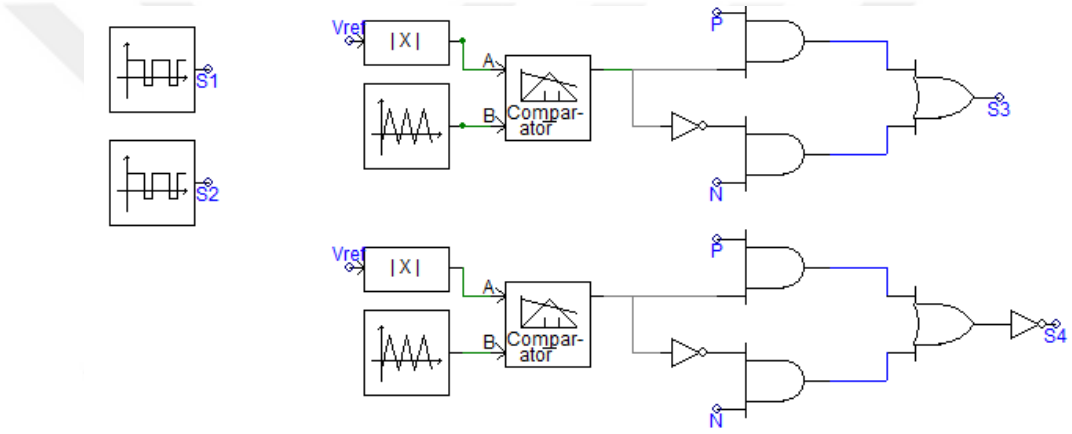


Fig. 3-9 The modulation technique of the proposed five-level inverter

3.2.2. Comparison Study

This section compares the suggested topology with a relevant five-level inverter that utilizes a single DC voltage source and incorporates coupled inductors. Subsequently, the proposed inverter is compared with the conventional cascaded H-bridge inverter in the following stage.

The comparisons have been established concerning the component count and overall voltage stress (V_{stress}) and current stress (I_{stress}) on the switches and diodes. The main reason for cumulative stress across all switches and diodes is to approximate the overall cost and losses of switches and diodes.

A. comparison with the relevant five-level inverter

In this segment, a contrast is drawn between the suggested topology and coupled inductor-based five-level inverters that rely on a single DC source. TABLE 3-VI shows the result of comparing the proposed inverter (P) with relevant inverters highlighting the numbers of IGBTs or MOSFETs and antiparallel diodes (N_S), numbers of coupled inductors (N_L), the count of diodes and capacitors (N_D) and (N_C) respectively.

TABLE 3-VI COMPARATIVE ANALYSIS OF THE PROPOSED INVERTER WITH RELEVANT FIVE-LEVEL INVERTERS

	N_{DC}	N_S	N_L	N_C	N_D	V_{stress}	I_{stress}
presented in [8]	1	4	1	2	2	6	5
presented in [66]	1	8	1	1	-	8	5
presented in [10]	1	8	1	2	-	8	8
Proposed (P)	1	4	1	-	2	6	6

As shown in TABLE 3-VI all present topologies use one coupled inductor, According to the number of switches, the proposed topology has less number of switches compared with the ones in [66] [10] a half amount of total switches. and it's clear that the proposed topology doesn’t need a capacitor.

Moreover, the total voltage stress in the proposed topology is less than the one presented in [66] and [10], it becomes evident that it outperforms them both from a technical perspective and in terms of cost-effectiveness upon a quick look, while the present structure has the same voltage stress comparing with the presented in [8] By comparison the proposed topology with the present one in [8] all the results are the same except for the capacitor the proposed topology has no capacitor while the present use two capacitors that are mean the proposed topology cheap than the present one, In addition to There is an absence of capacitors voltage balancing. As is apparent from

Table 2, the total current stress of the proposed inverter is better than the present in [10] but for the other, it's not because the current stress in most switches in the topologies present in [8] and [66] is half of the output current because of the coupled inductor and the capacitors that use in these structures.

B. comparison with the relevant nine-level inverter

Four novel Voltage Source Inverters (VSIs) are introduced in [6] for single-phase applications. These VSIs utilize a pair of balanced coupled inductors to generate a nine-level output voltage using two distinct DC sources. TABLE 3-VII. provides a concise summary of the comparison results between the proposed topology and the strictures presented in [67], [62] and [11], the latter presented four topologies. These topologies are:

- Active series voltage sources with coupled inductors (AS-CI)
- Cascaded with coupled inductors (C-CIs)
- Active neutral point clamped with coupled inductors (ANPC-CI)
- Extended ANPC-CIs (EANPC-CIs)

TABLE 3-VII COMPARATIVE ANALYSIS OF THE PROPOSED INVERTER WITH RELEVANT NINE-LEVEL INVERTERS

		N_{DC}	N_S	N_L	N_D	V_{stress}	I_{stress}
[11]	*AS-CI*	2	8	1	-	10	6
	C-CI	2	10	1	-	10	8
	ANPC-CI	2	10	1	-	12	8
	EANPC-CI	2	10	1	-	14	6
[67]		1	8	1[a]	-	8	16
[62]		2	8	3	8	16	16
Proposed (P)		1	4	1	2	6	6

a: transformer

Since the presented topologies have nine-level output to ensure a fair comparison, all the parameters under consideration are normalized. This normalization process

involves dividing these parameters by the number of output voltage levels. Fig. 3-10. Shows the comparison result. As shown in Fig. 3-10 a, the proposed structure has a less number of DC sources compared with the four topologies in [11] and the structure presented in [62] but it's not with the one in [67]. The total number of switches in a multilevel inverter circuit stands as a critical parameter. It not only influences the cost but also impacts the size of the inverter. Fig. 3-10 b demonstrates that the proposed inverter needs less number of switches compared with the other structures, Even though it incorporates two diodes, this does not hinder it from having the fewest gate drivers to control the four switches.

According to Fig. 3-10 c the structure presented in [67] has minimum voltage stress while the voltage stress of the proposed structure is better than (ANPC-CI, EANPC-CI, and [62]) and almost equal to (AS-CI and C-CI). It is clear from Fig. 3-10. d that the total current stress of the proposed topology is higher than the four topologies presented in [11] This is because all switches in the proposed structure have rated currents equal to the rated load current. While the rated current of some switches in the presented one is equal to half of the load current, it is also clear that the current stress in the proposed topology is better than the one presented in [67] and [62]. Fig. 3-10 e illustrates the coupled inductor ratio all topologies use one coupled inductor, except for [62] uses three coupled inductor to produce 9 levels, while the one present in [67] uses a transformer instead of a coupled inductor. Fig. 3-10 f shows the diode ratio, according to the figure, the proposed structure uses the minimum number of diodes compared with [62] while the other topologies don’t use diodes in their structure.

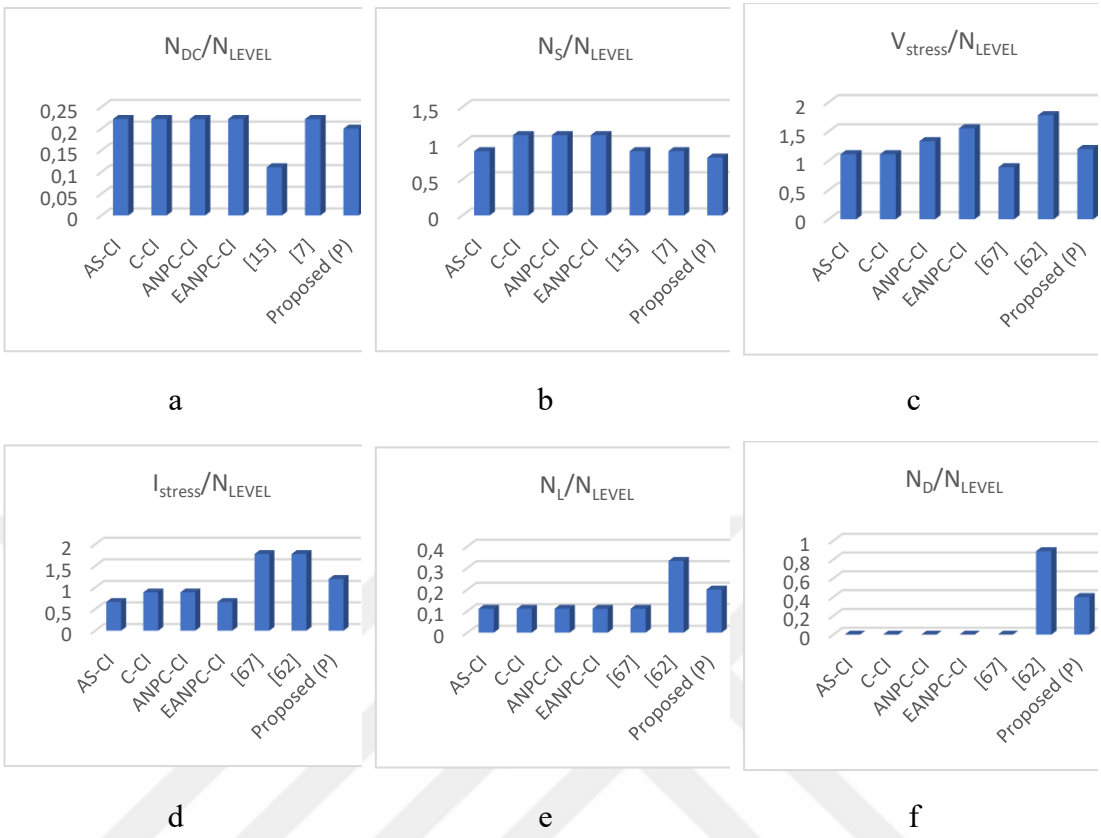


Fig. 3-10 Comparison result: (a), Number of DC ratio (b) Number of switches ratio, (c)voltage stress ratio, (d)current stress ratio, (e)number of coupled inductor ratio,(f)number of diodes ratio

3.2.3. Coupled Inductor Design

In order to formulate the coupled inductor design for the suggested inverter, certain assumptions have been made, as outlined in TABLE 3-VIII. The voltage and current parameters of the coupled inductor are substantiated based on the predefined design data of the inverter. Following the information provided in TABLE 3-VIII, the apparent power of the coupled inductor is determined as follows:

$$Pc = Vab, rms \times Iab, rms = 2000W \tag{3-26}$$

Over the years, manufacturers have utilized numerical codes to represent the power-handling capacity of their cores. This approach involves assigning an area

product (Ap) value to each core, which is calculated by multiplying the window area (Wa) with the core's cross-section (Ac). Core suppliers rely on these values to encapsulate dimensional and electrical characteristics in their catalogs.

$$Ap = \frac{Pc \times 10^4}{K_f K_u B_m f_{sw} J} = 59.87\, cm^4 \tag{3-27}$$

Based on the area product (Ap) value, the closest ferrite core of 59.87 is EE-60, It has an area product of 80 cm^4, which is close to the calculated value. From the datasheet of EE-60, we can calculate the number of the windings turns of the coupled inductor by using the equation:

$$N = \frac{Vab, rms \times 10^4}{K_f B_m f_{sw} A_c} = 66.8\, turns \tag{3-28}$$

The number of turns of one winding of coupled inductor is half of N.

The equal inductance for the coupled inductor is computed using the following method:

$$L_{CI,eq} = A_L N^2 = 30.3 mH \tag{3-29}$$

A_L is core permanence from datasheet it is equal to (6800 nH)

When neglecting leakage inductance and considering only the self-inductance (L1 and L2) and mutual inductance (M) of a coupled inductor, the inductance values of coupled inductor are equal :

$$L_1 = L_2 = M = \frac{L_{CI,eq}}{4} = 7.575 mH \tag{3-30}$$

To evaluate the ripple current of the coupled inductor we have the following equation:

$$i_{ripple,\max} = \frac{Vdc\, T_S}{4M} \tag{3-31}$$

Then the satisfy inductance M must be:

$$M \geq \frac{Vin\, T_S}{i_{ripple,max}} \tag{3-32}$$

By assuming that the current ripple is 8% of the maximum current in the windings of the coupled inductor, the computed inductance as given in equation (3-30(3-30)remains applicable for equation (3-32).

Additionally, the windings bare wire area ($A_{w(B)}$) calculated by equation:

$$A_{W(B)} = \frac{Ia, rms}{J} = 0.0177\, cm^2 \tag{3-33}$$

And the wire diameter (D_{AWG}) is obtained by:

$$D_{AWG} = \sqrt{\frac{4A_{W(B)}}{\pi}} = 1.5\, mm \tag{3-34}$$

From wire table in [65] the wire size that closely aligns with the calculated area corresponds to AWG #15.

TABLE 3-VIII DESIGN SPECIFICATION FOR THE COUPLED INDUCTOR

The maximum voltage of the coupled inductor (Vab max)	200 V
The maximum current of the coupled inductor (Io)	10 A
operating frequency (f_{sw})	8 KHz
current density (J)	400 A/cm^2
flux density (B_m)	0.09 T
window utilisation (K_u)	0.29
waveform coefficient (K_f)	4

3.2.4. Cost calculation for the proposed five-level inverter

In this section, we expound upon the cost analysis of the proposed structural configuration. To assess the cost of the suggested topology, a systematic methodology is implemented. Within this approach, due consideration is meticulously given to the

cost of all components, and these costs are systematically aggregated to derive an estimated overall cost for the proposed topology. This facilitates its comparative evaluation against other existing topologies. Operating under the assumption of a consistent input voltage, the cost assessment for each circuit element within the Multilevel Inverter (MLI), encompassing power electronic switches (IGBTs or MOSFETs) and coupled inductors, is meticulously conducted as follows [7]:

C_{switch} is the cost of the switch/ (VA)

C_{ind} is the cost of inductor/ (VA)

The comprehensive cost evaluation of the multilevel inverter is computed as follows:

$$C_{total} = (VA)_{switch} C_{switch} + (VA)_{ind} C_{ind} \tag{3-35}$$

The total Volt-Amperes (VA) of the switches is denoted as $(VA)_{switch}$, encapsulating the cumulative (VA) rating of the switches. Simultaneously, $(VA)_{ind}$ represents the total Volt-Amperes of the coupled inductors.

In the context of the proposed five-level inverter, it is pertinent to observe that four switches and the two diodes share both an identical voltage rating and an equivalent current rating. Given that the magnitude of the rated output current is *Io*,*m* and considering $V_{o,m} = V_{in}$, Equation (3-35) can be expressed as follows:

$$C_{total} = 6V_{o,m}\ I_{o,m} C_{switch} + V_{o,m} I_{o,m} C_{ind} \tag{3-36}$$

By defining the maximum output Volt-Ampere of the inverter as VA_{max}, the ensuing equation can be derived as follows:

$$C_{total,proposed} = \left[6\,C_{switch} + C_{ind}\right] VA_{\max} \tag{3-37}$$

The cost of the necessary components for both the proposed five-level inverter considering the specified rated values, is detailed in TABLE 3-IX.

TABLE 3-IX THE COSTS ASSOCIATED WITH IGBTS AND COUPLED WINDINGS OF VARIOUS RATINGS

Part	**Rated**	**Cost (USD)**	**Cost/VA**
IRFP250PBF	250V, 23A	3.35	3.35/5750
STF40250T	250V, 40A	1.26	1.26/10000
coupled inductor			
Wire:AWG #15		0.6	26.02/40000
ferrite core:EE-60		25.42	

3.3. Chapter Conclusions

This chapter has provided a comprehensive overview of the proposed seventeen-level and five-level inverter topologies, focusing on the circuit configurations, switching states, and operational principles that enable multi-level output generation. The pulse width modulation (PWM) techniques tailored for each topology were thoroughly examined to highlight their effectiveness in achieving desired output levels. Additionally, a detailed power loss analysis and a comparative evaluation with alternative multilevel topologies, such as the cascaded H-bridge inverter, underscored the efficiency of the proposed designs. The cost assessment further reinforced the feasibility of the inverters when coupled inductors are integrated, comparing them with other emerging topologies. Finally, the design process of the coupled inductor was explored to emphasize its critical role in the performance and integration of both the seventeen- and five-level inverter systems.

4. SIMULATION AND EXPERIMENTAL RESULTS

This chapter delves into the simulation studies for both a seventeen-level and a five-level inverter, and experimental results derived from the application of the seventeen-level inverter. The outcomes of both simulation endeavors and real-world experiments are meticulously analyzed and discussed. Through a comprehensive examination of simulation data and empirical evidence, this chapter sheds light on the viability of the seventeen-level inverter in real-world applications.

4.1. Simulation Studies for The Proposed Seventeen- level Inverter

The inverter, designed based on the proposed topology, was subjected to simulation using PSCAD/ EMTC software. The ensuing outcomes are presented and subsequently analyzed for discussion. The PSCAD model for the proposed seventeen-level coupled inductor inverter is presented in Fig. 4-1.

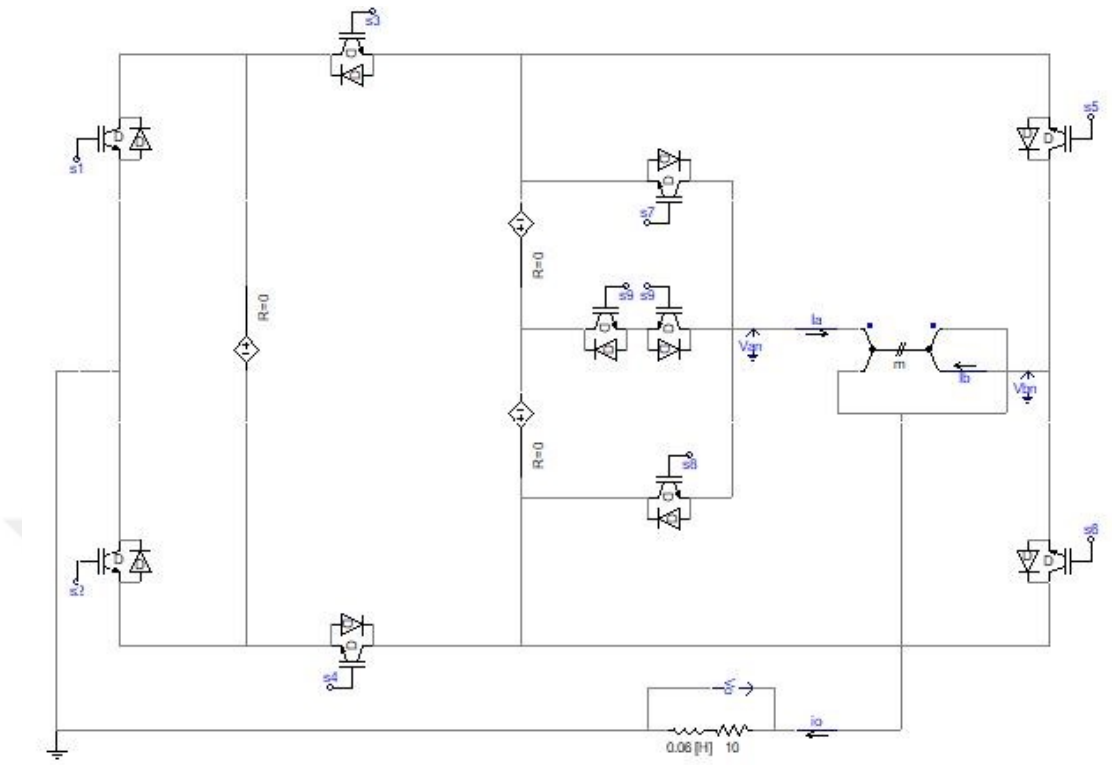


Fig. 4-1 The PSCAD model for the proposed 17-level coupled inductor inverter

The ensuing outcomes are presented and subsequently analyzed for discussion. Input voltage is considered as 50V(V_{dc}=50V) and 100V($2V_{dc}$=100V) , and the maximum magnitude of output voltage is 200V. the fundamental frequency of the load voltage and the switching frequency are 50 Hz and 10KHz respectively,

In accordance with the design objectives, the values of mutual inductance M =4.85 mH, and 0.95 coefficient of coupling is used. The inverter is responsible for supplying power to an inductive load characterized by a resistance of 10 Ω and an inductance of (60 mH).

Fig. 4-2 indicates the output voltage and current of the proposed 17-level inverter. The output voltage which is denoted by Vo is a 17-level voltage with the equal voltage steps with high quality. The output current which is denoted by Io is a near sinusoidal

waveform with total harmonic distortion of 0.4%. This is on one hand because of the low harmonic contents of the output voltage and on the other hand, it is because of the inductive nature of the load which suppresses high-frequency harmonics of the output current. Moreover, the output current lags the output voltage as the load is an inductive load.

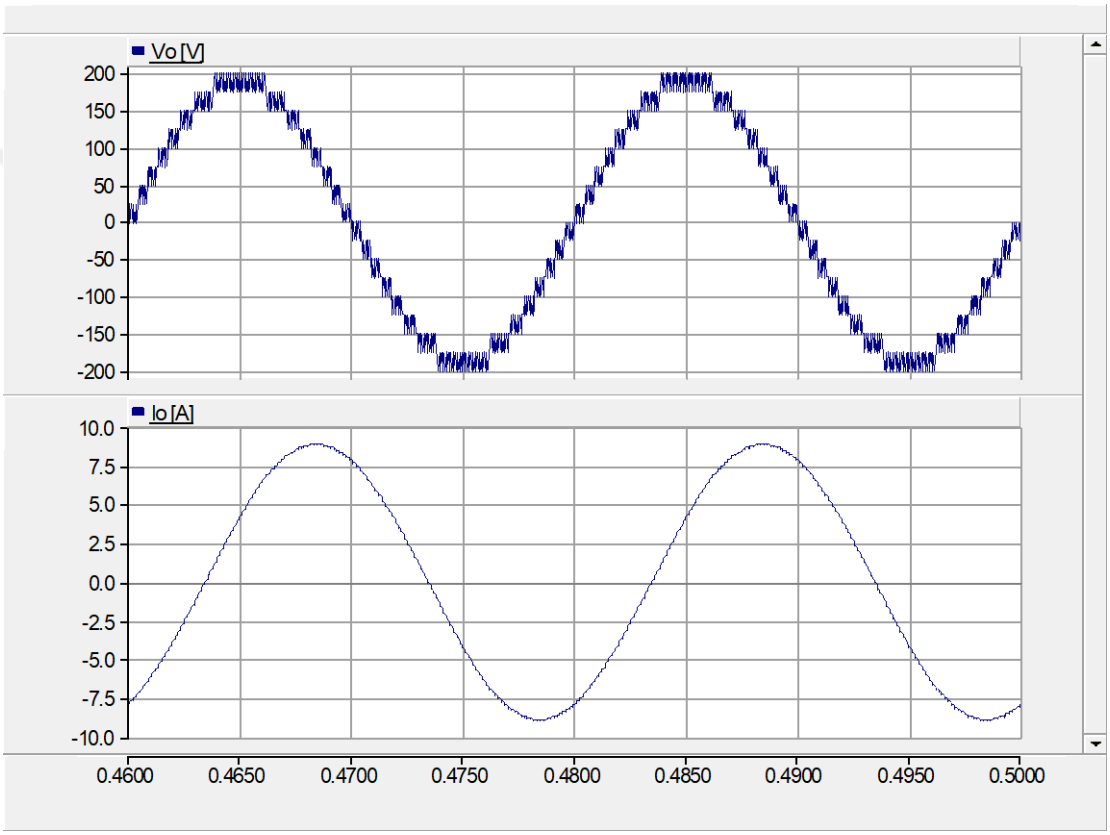


Fig. 4-2 Simulation results for the proposed 17-level inverter from top to bottom: output voltage, output current.

In Fig. 4-3 demonstrates the voltage on the both sides of the coupled inductor which are denoted by V_{L1} and V_{L2}. As seen from this figure, the maximum value of the voltage on both sides of the coupled inductors are the same as 200 V. However, the number of voltage levels of the two voltage waveform are different so that they form a 17-level output voltage together.

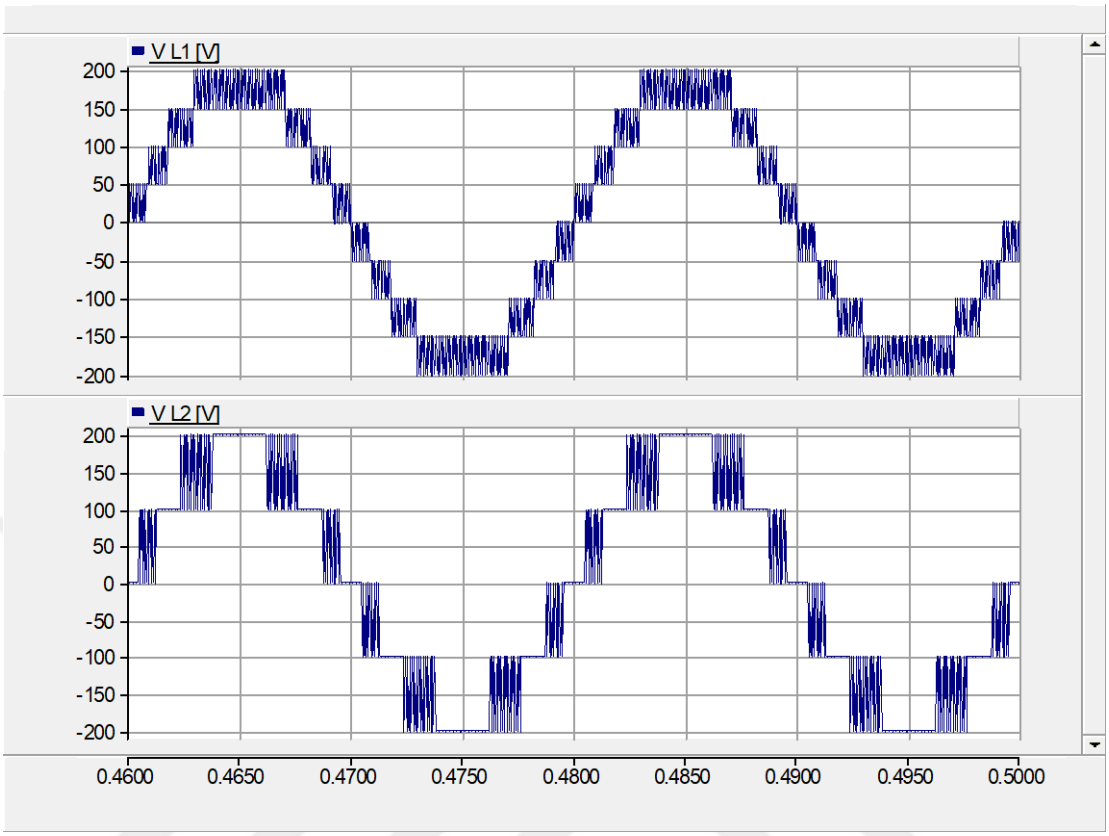


Fig. 4-3 The simulation result for the voltage across the two winding of the coupled inductor:(VL1), (VL2)

Fig. 4-4 indicates the current of the coupled inductors as well as the total output current which is the sum of the coupled inductors' current. According to the figure, the current of the coupled inductors complements each other to form a sinusoidal output current.

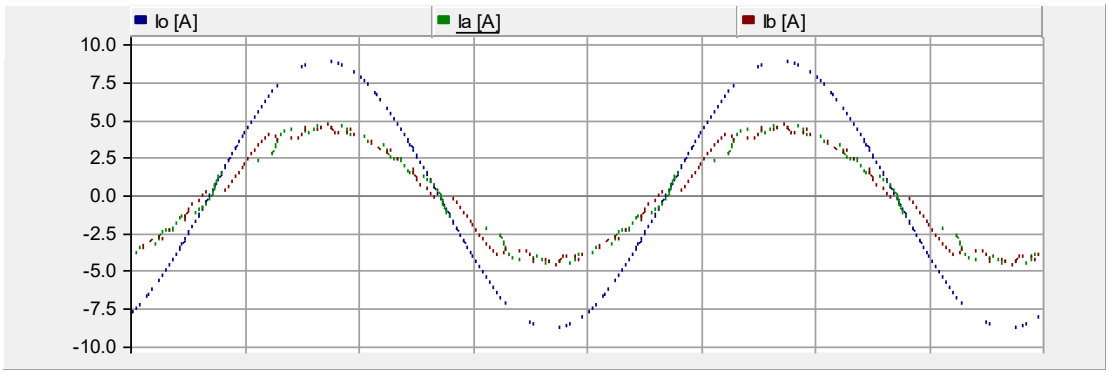


Fig. 4-4 The simulation result for the current of the two winding and output current

Fig. 4-5 to Fig. 4-8 shows the simulation result for the voltage on each switch to illustrate the voltage stress on switches.

Fig. 4-9 to Fig. 4-12 depict the simulation results detailing the current distribution across each switch, aiming to elucidate the current stress exerted on the switches. Notably, the switches directly connected to each side of the coupled inductor endure a current stress equivalent to half of the output current. This observation is discernible from Fig. 4-11 and Fig. 4-12, particularly concerning switches S5, S6, S7, S8, and S9. Conversely, the current flowing through the other switches is equivalent to the output current, this observation is clearly illustrated in Fig. 4-9 and Fig. 4-10.

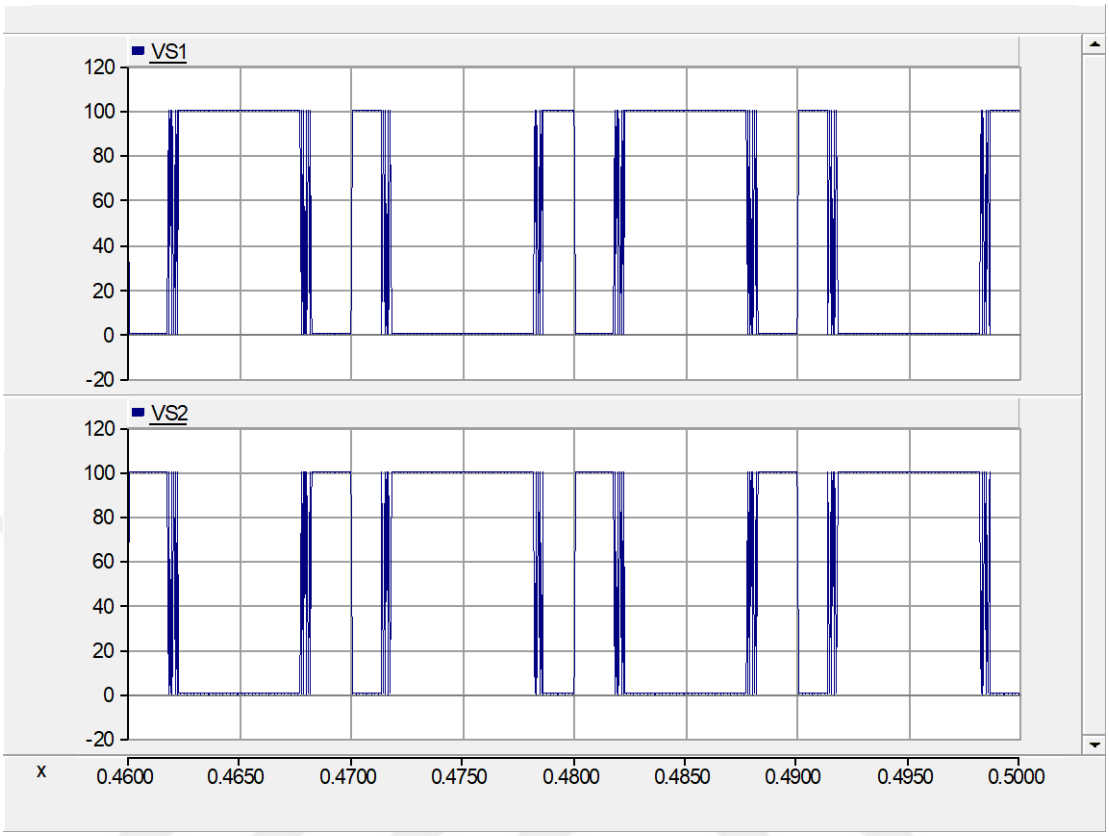


Fig. 4-5 The voltage on the switches S1 and S2

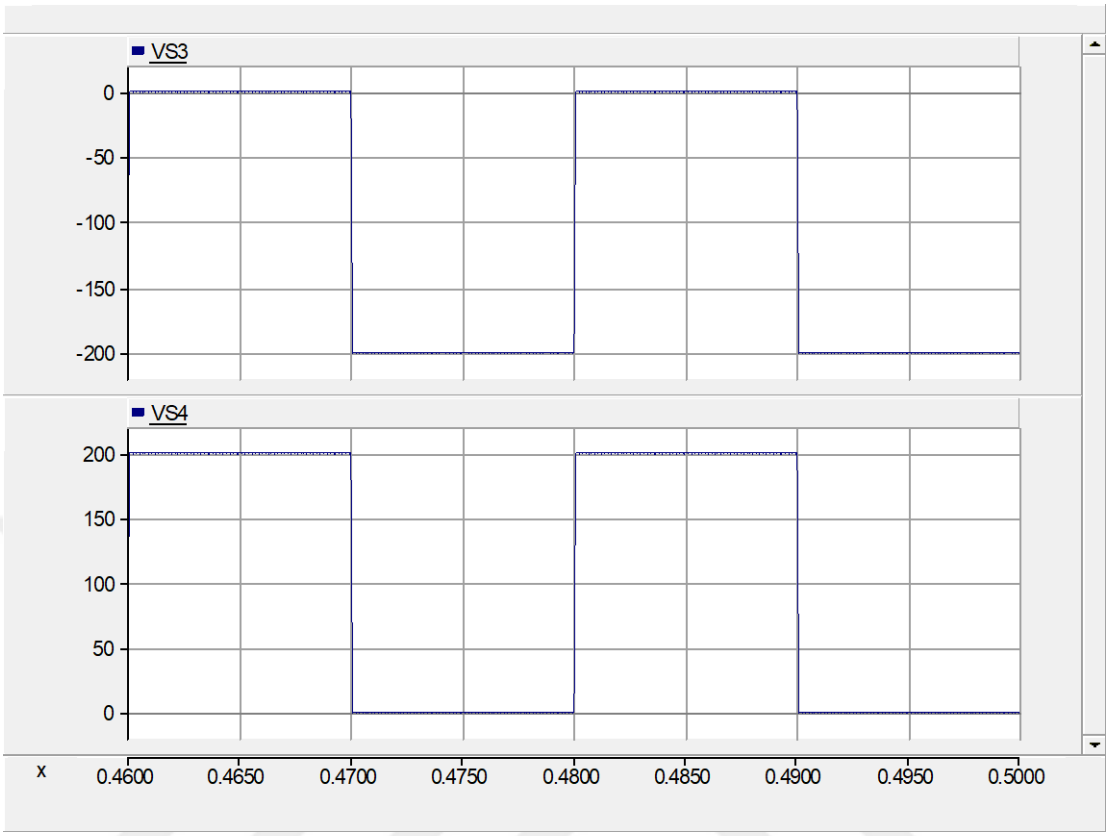


Fig. 4-6 The voltage on the switches S3 and S4

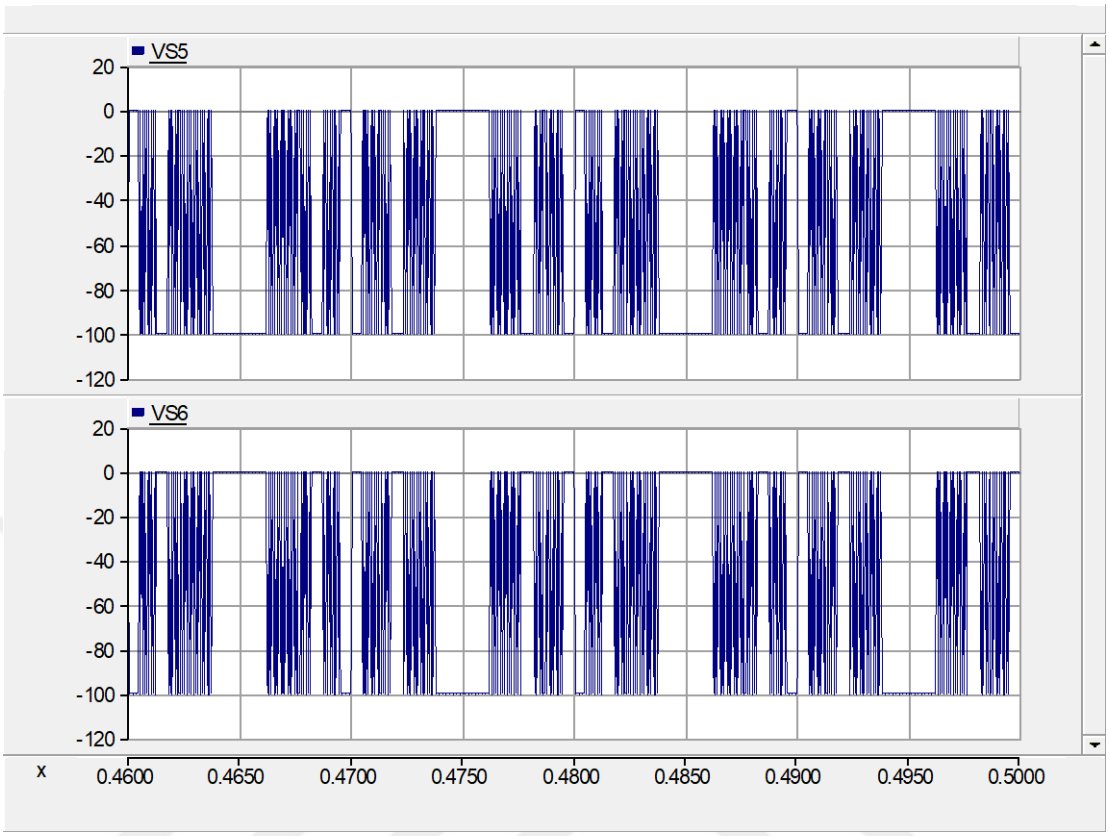


Fig. 4-7 The voltage on S5 and S6

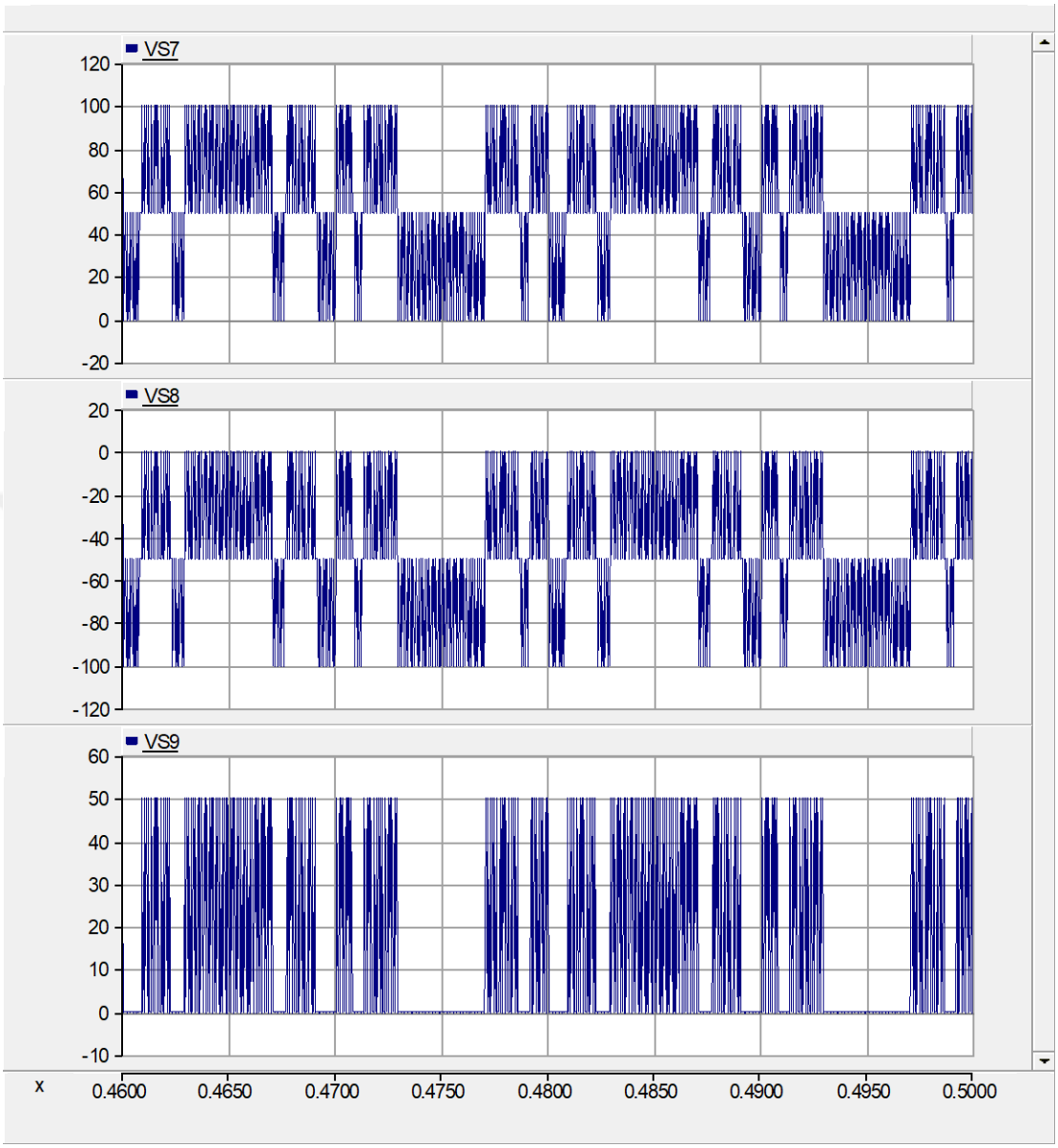


Fig. 4-8 The voltage on S7, S8 and S9

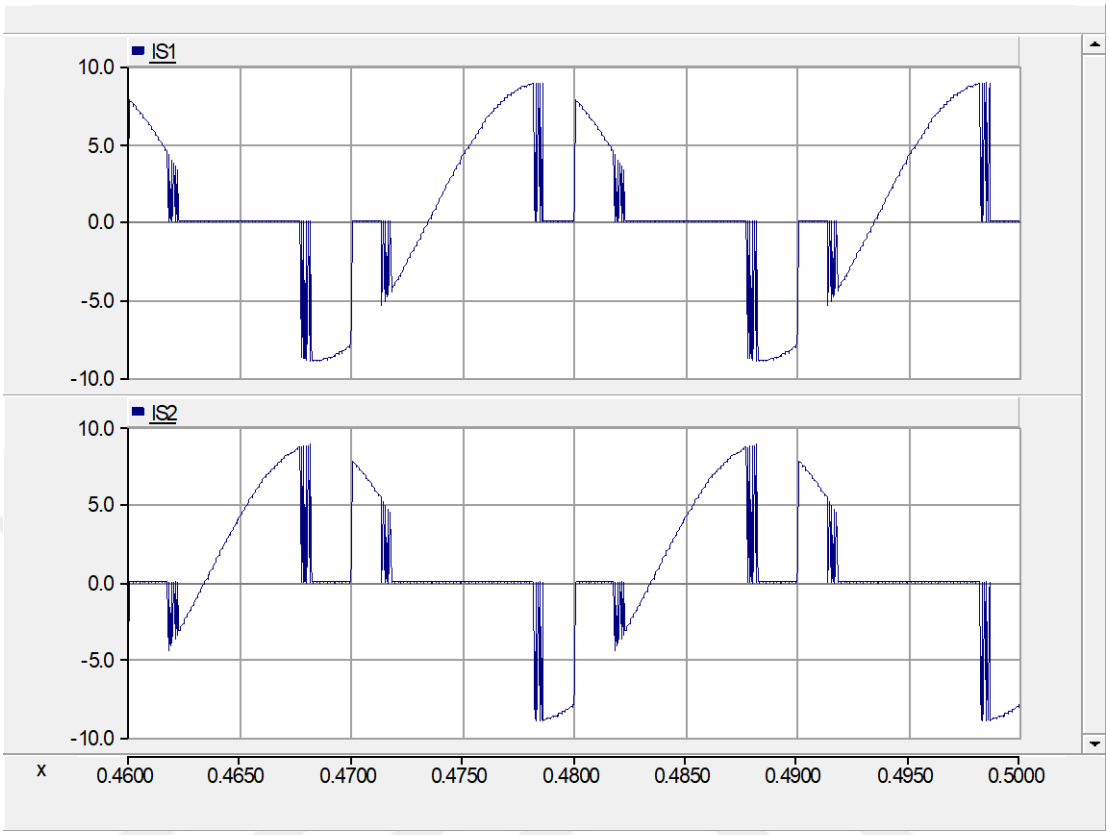


Fig. 4-9 current of the switches S1 and S2

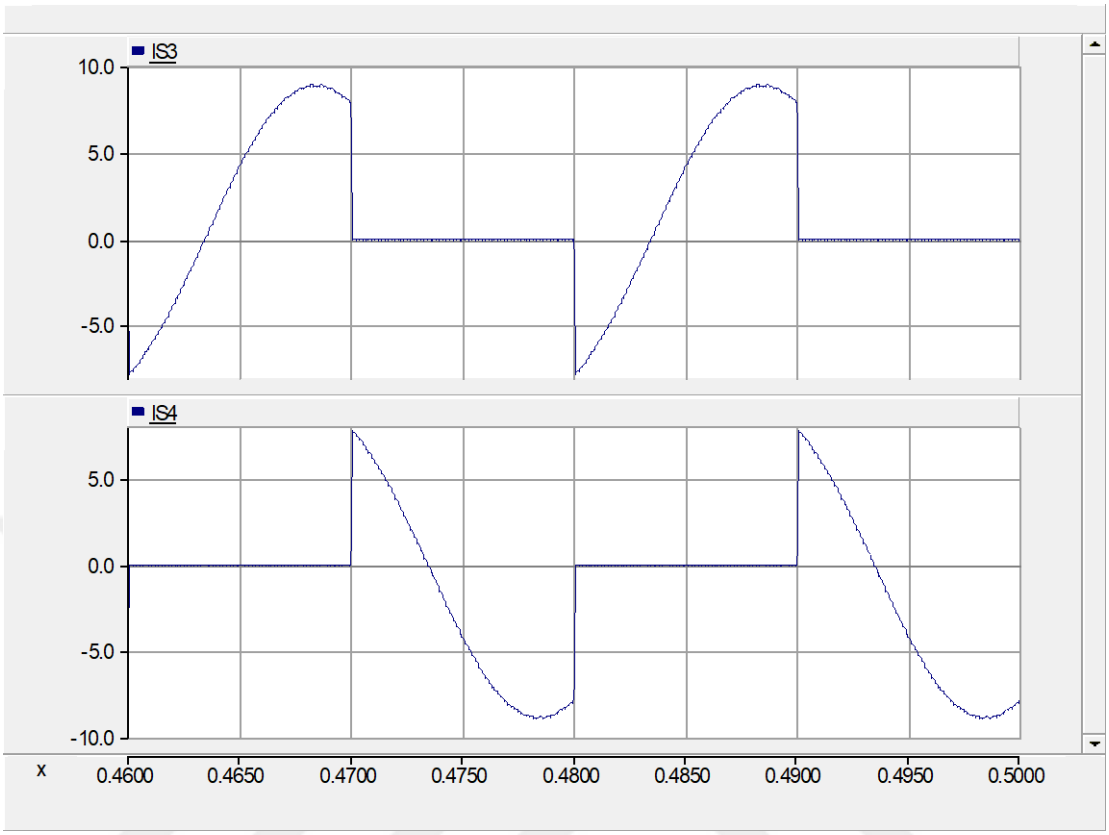


Fig. 4-10 current of the switches S3 and S4

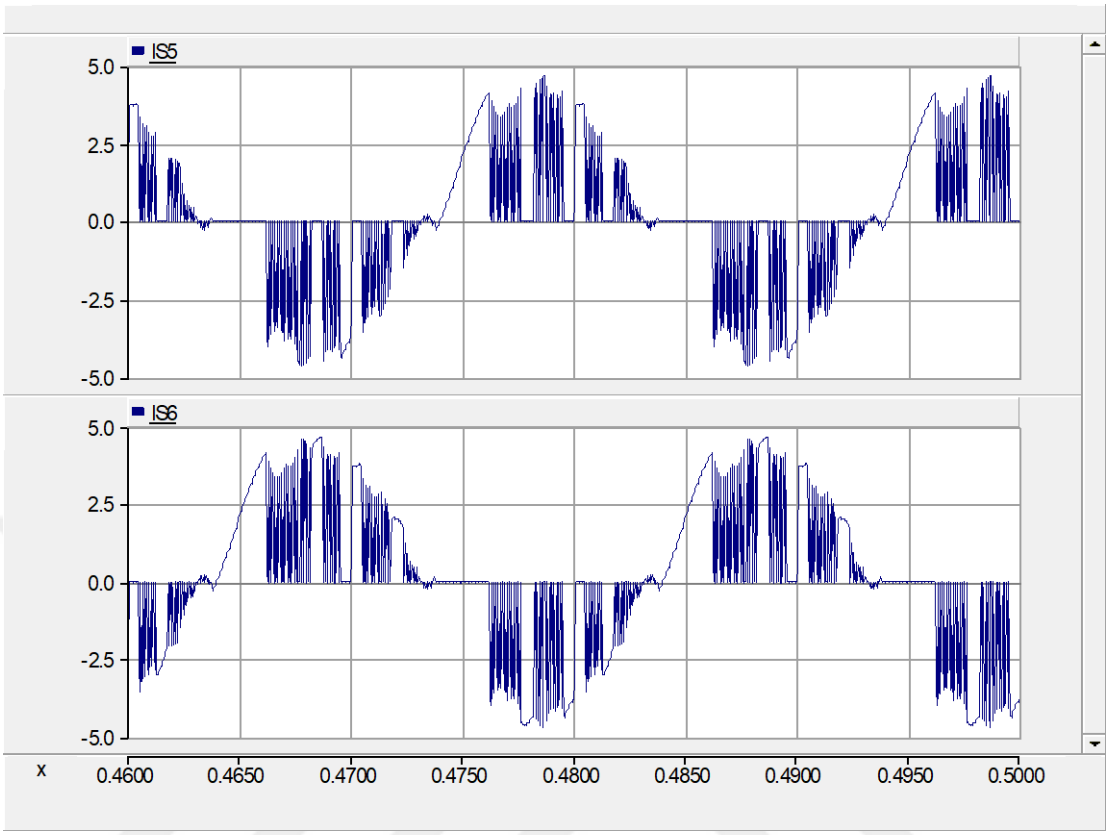


Fig. 4-11 current of the switches S5 and S6

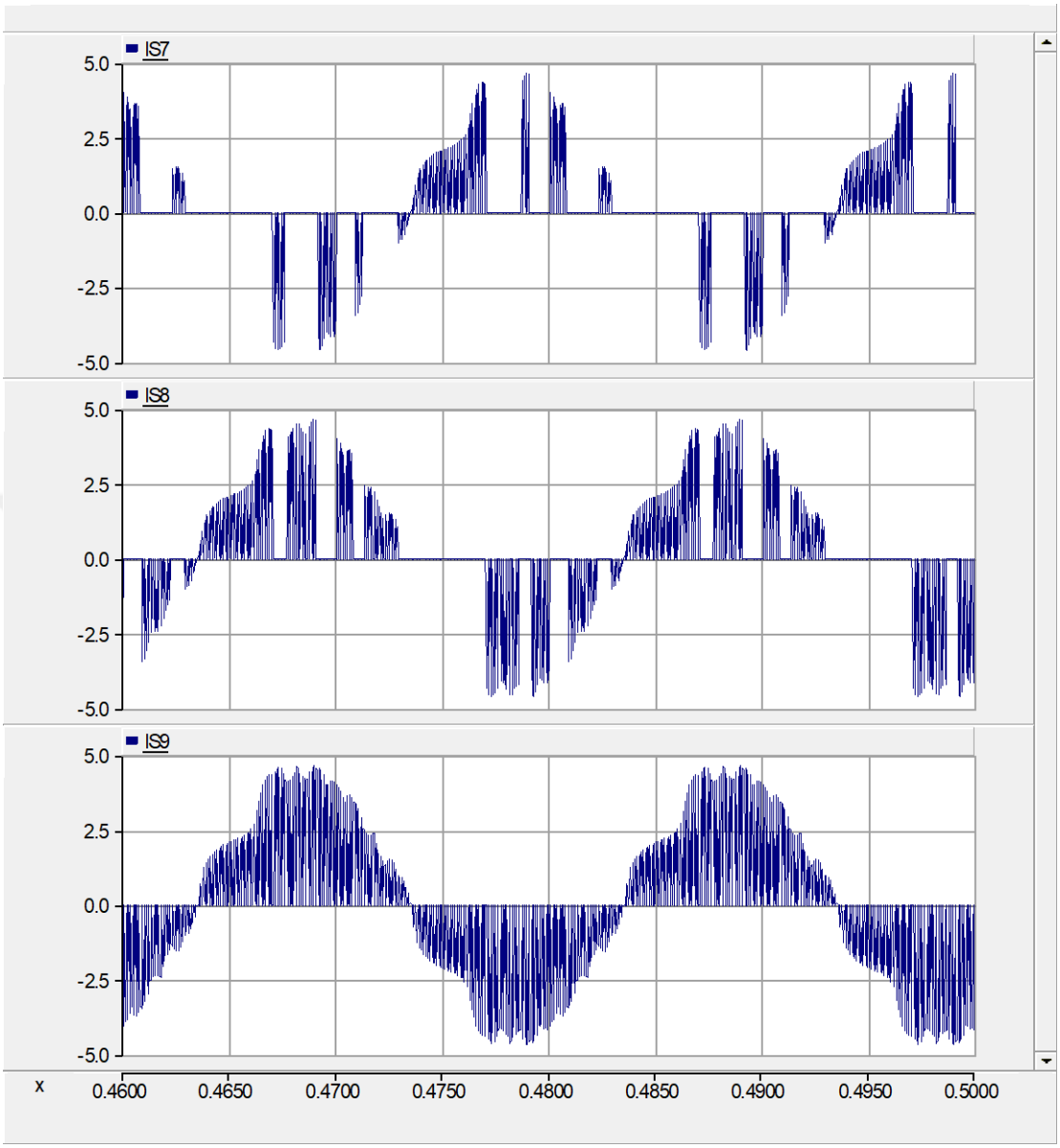


Fig. 4-12 current of the switches S7, S8 and S9

4.2. Simulation studies for the proposed five- level inverter

This section showcases the simulation outcomes of the suggested 5-level inverter. The 5-level inverter designed according to the proposed topology has been simulated using PSCAD/EMTDC software, and the results are provided and discussed. The DC voltage is set at 200 V. The inverter serves an inductive load with a resistance of 10 ohms and an inductance of 1 mH. The self-inductance of the coupled inductor windings is identical at 1 mH, and the mutual inductance is 0.9 mH. The fundamental frequency is 50 Hz, and the switching frequency is 8 kHz. The simulation outcomes of the suggested single-phase five-level inverter are displayed in Figures 6 to 10.

Fig. 4-13 shows from top to bottom, the output voltage of the two windings of the coupled inductor (V1n, V2n) and the output voltage of the proposed inverter (Vo). The traces from top to bottom in Fig. 4-14 represent the current flowing through the two branches of the coupled inductor, and the lowermost trace represents the total output current. As depicted in the figure, the current through the branches of the coupled inductor is uniform and half of the output current. Furthermore, it's worth noting that the ripples on the output current are lower than those observed in the coupled-inductor currents.

Fig. 4-15 shows the current through the semiconductors of the proposed inverter to illustrate the current stress on each one of them, As is evident the current stress on the semiconductors of the proposed structure is equal to the output current. As is clear in figure, S1 and S2 are only switching for half of the modulating signal's duration. The voltage on each switch and diode is shown in Fig. 4-16 which represents the standing voltage of each semiconductor in the structure, As is clearly apparent the standing voltage of each semiconductor is equal to the value of the DC voltage source.

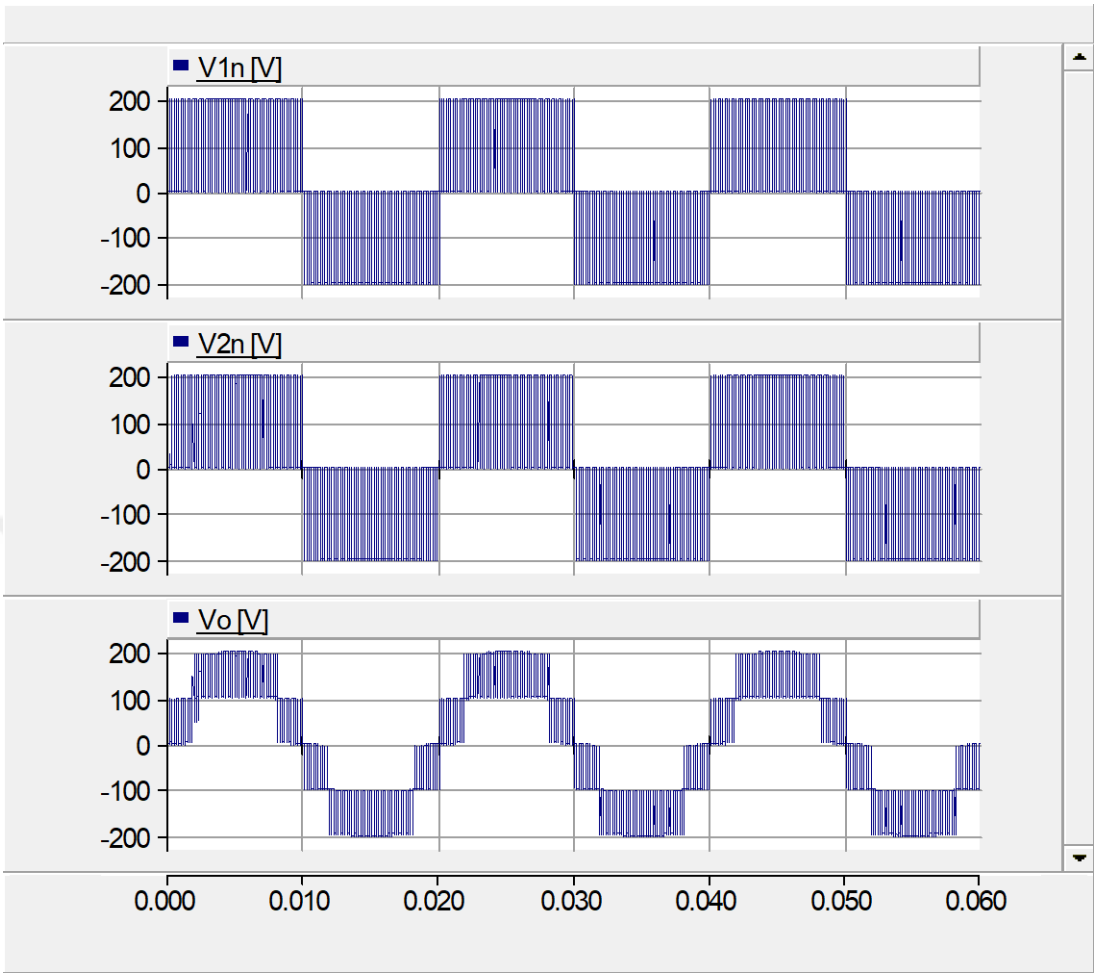


Fig. 4-13 the output voltage of the two windings of the coupled inductor and the output voltage of the proposed inverter respectively.

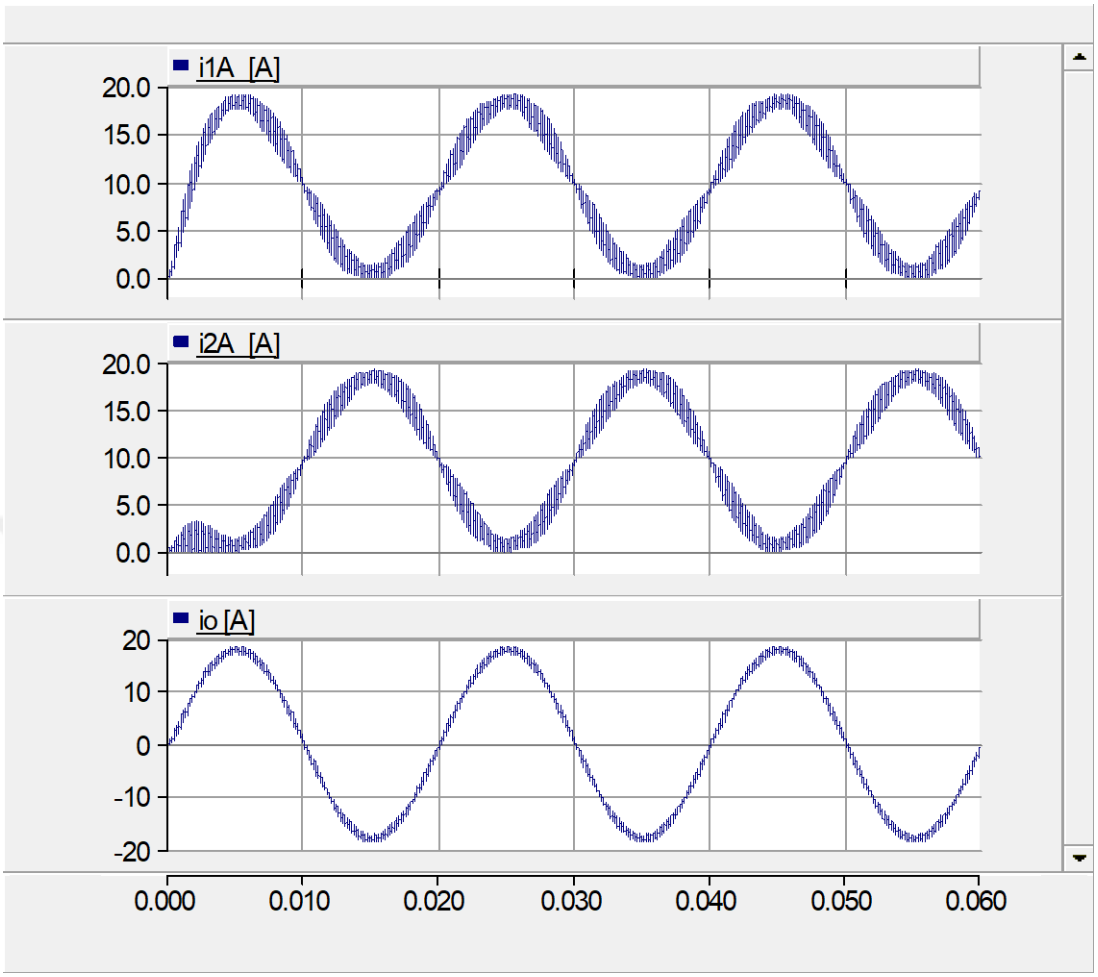


Fig. 4-14 The current through the two branches of the coupled inductor, and the output current of the proposed inverter respectively.

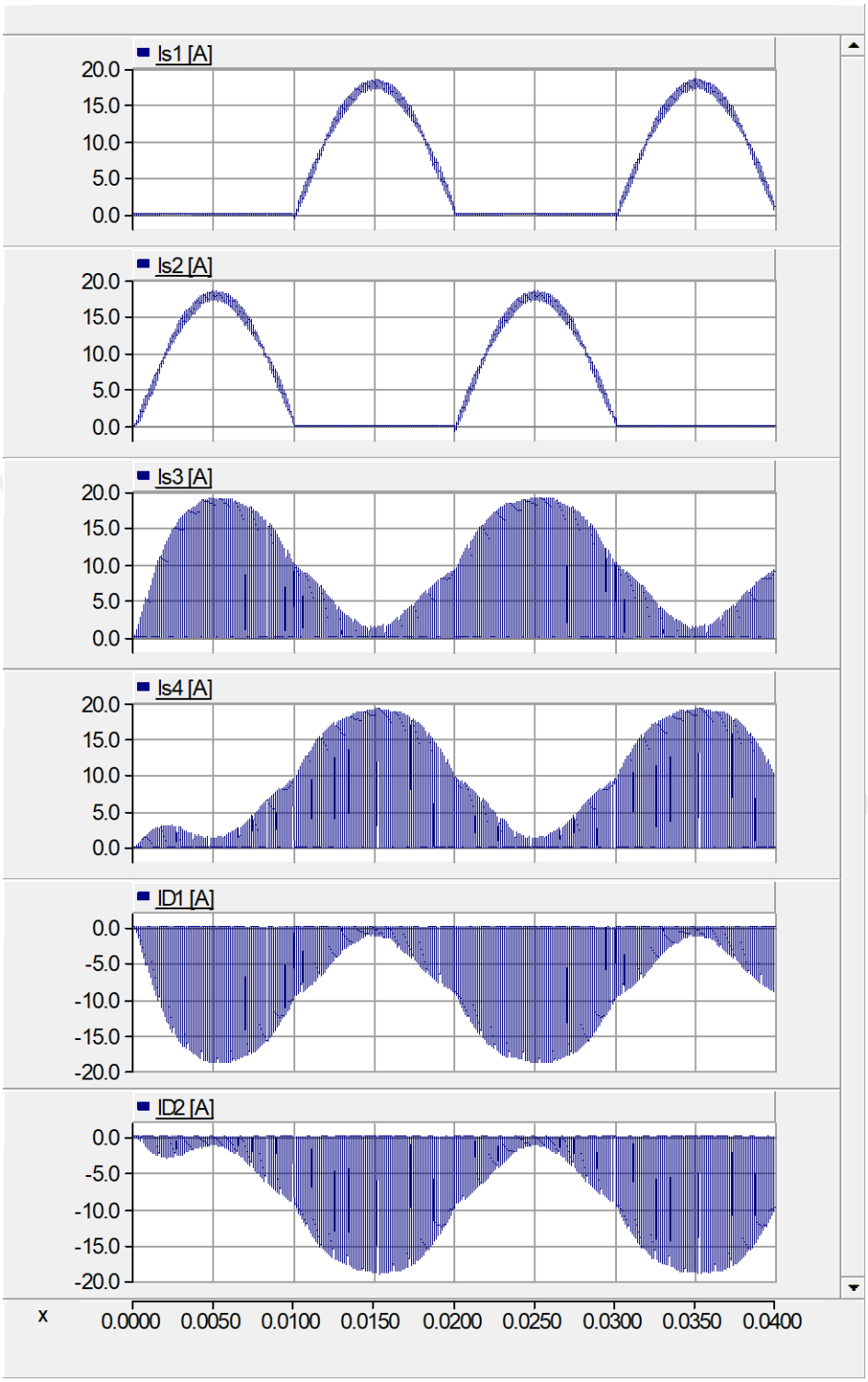


Fig. 4-15 from top to bottom, the current of the switches (S1, S2, S3, S4) and the current of the two diodes (D1 and D2)

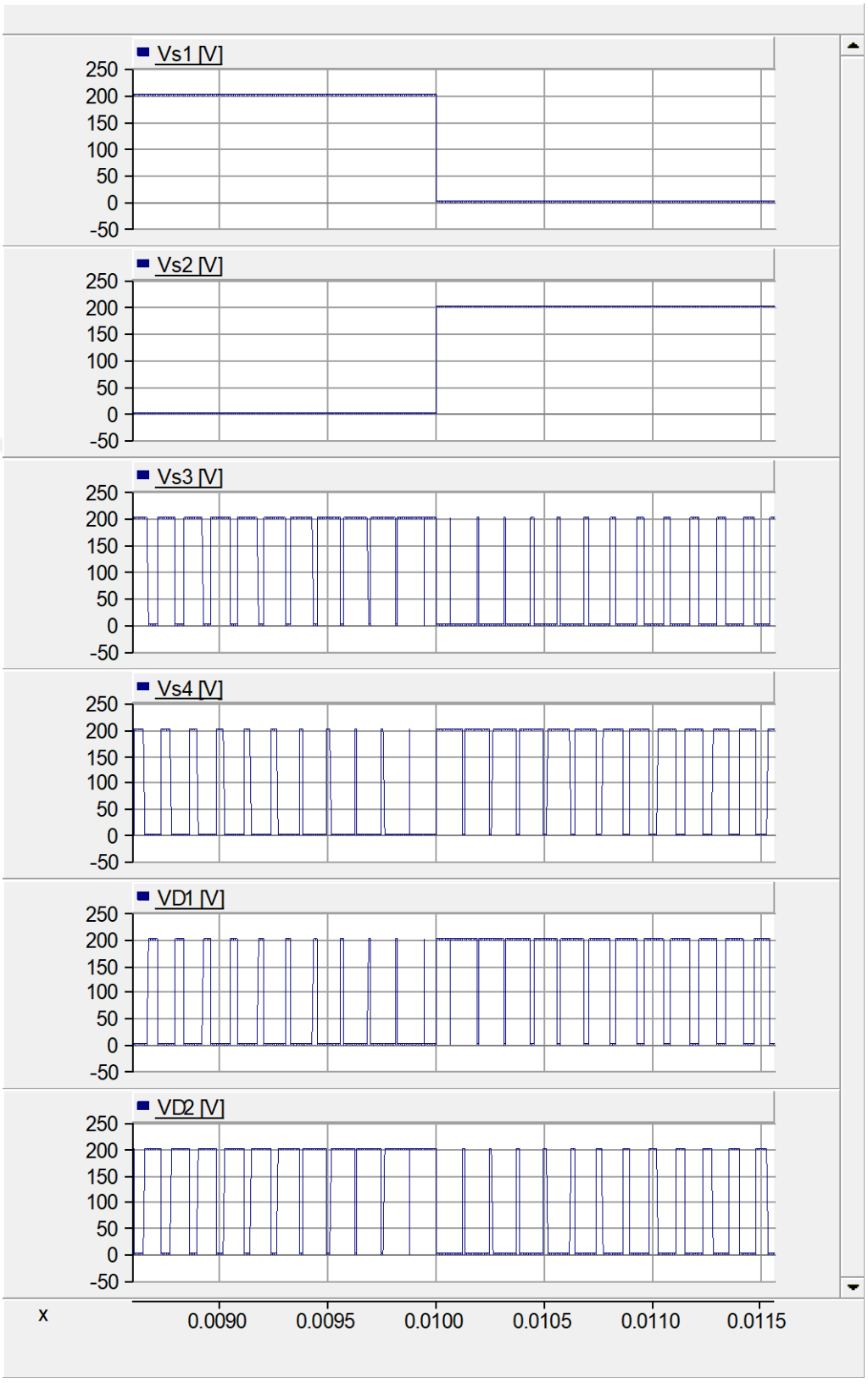


Fig. 4-16 from top to bottom, the voltage of the switches (S1, S2, S3, S4) and the diodes (D1 and D2).

4.3. Experimental Results for The Proposed Seventeen-Level Inverter

A laboratory prototype for the suggested seventeen-level inverter has been successfully developed and tested the magnitude of the DC voltage sources has been chosen as 50V and 100V. The resulting peak output voltage is 200V, featuring a voltage step of 25V and an output frequency of 50Hz. The operational performance of the proposed basic unit is assessed by connecting a series of resistive-inductive loads with 10Ω and 60mH respectively.

Fig. 4-17 depicts the experimental waveforms of the output voltage "Vo". which is a seventeen-level voltage similar to the simulation results which confirms the operation of the proposed inverter in practice

the voltage across the two windings of the coupled inductor "V_{L1}" and "V_{L2}" are shown in Fig. 4-18. These voltage waveforms are also very similar to the simulation results as expected.

The output current "Io" as well as the current flowing through the two windings of the coupled inductor "IL1" and "IL2"inductor are illustrated in Fig. 4-19.According to this figure, the current of the two windings is almost half of the output current. Also, they complete each other so that the output current is almost sinusoidal

The experimental results closely paralleled the outcomes derived from simulation studies. showcasing a strong alignment between theoretical predictions and real-world performance. This consistency serves to affirm the reliability and accuracy of the simulation model in effectively forecasting the behavior of the seventeen-level inverter across different operational scenarios.

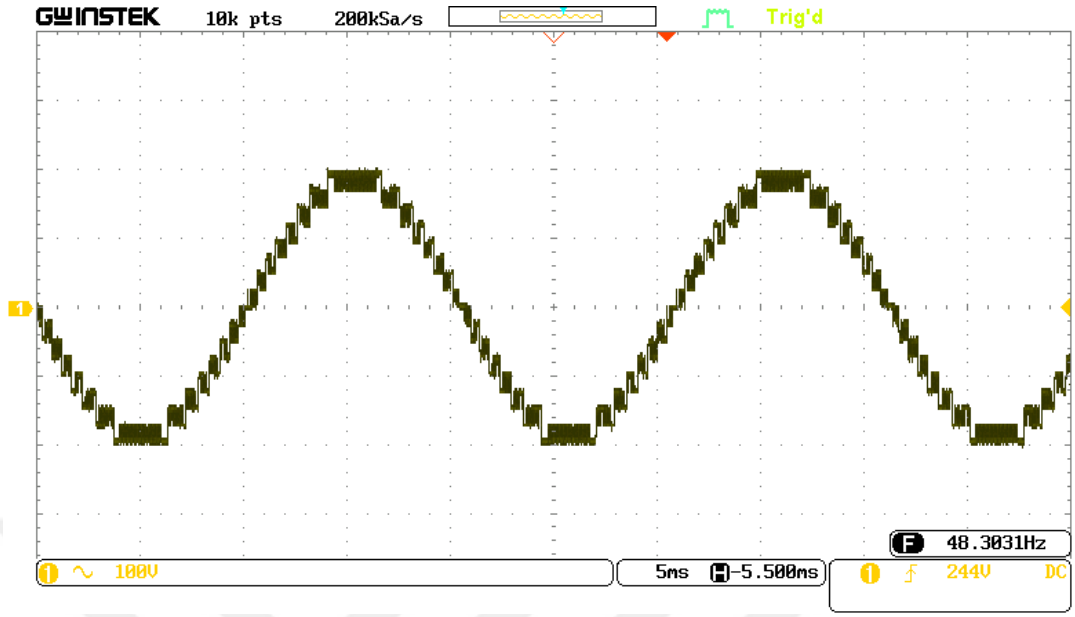


Fig. 4-17 Experimental waveforms for the proposed 17-level inverter (Vo).

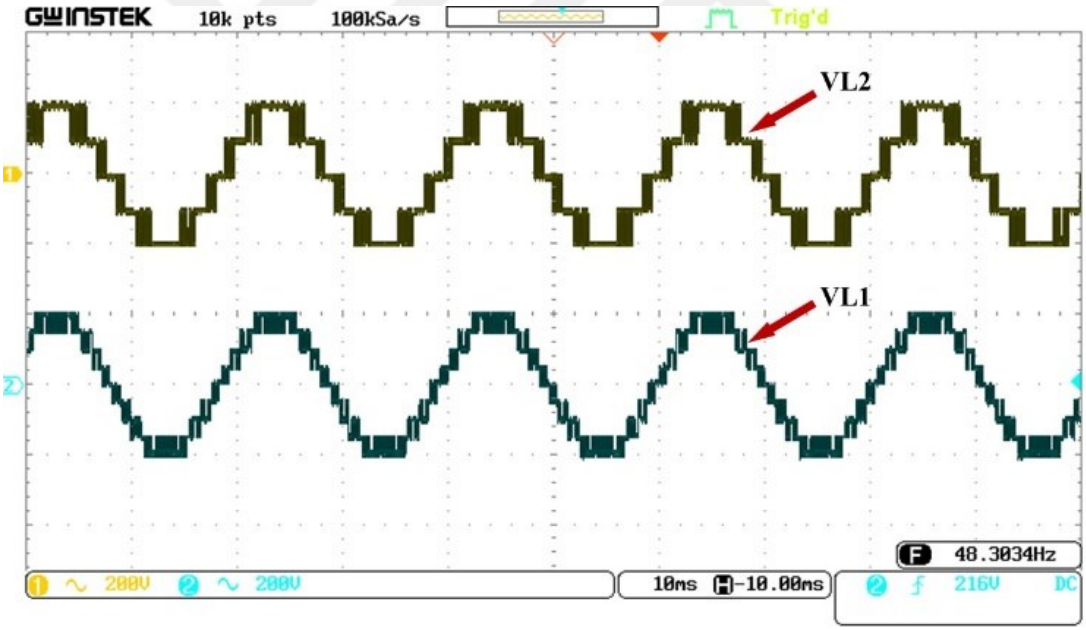


Fig. 4-18 Experimental waveforms for (V_{L1}), (V_{L2}).

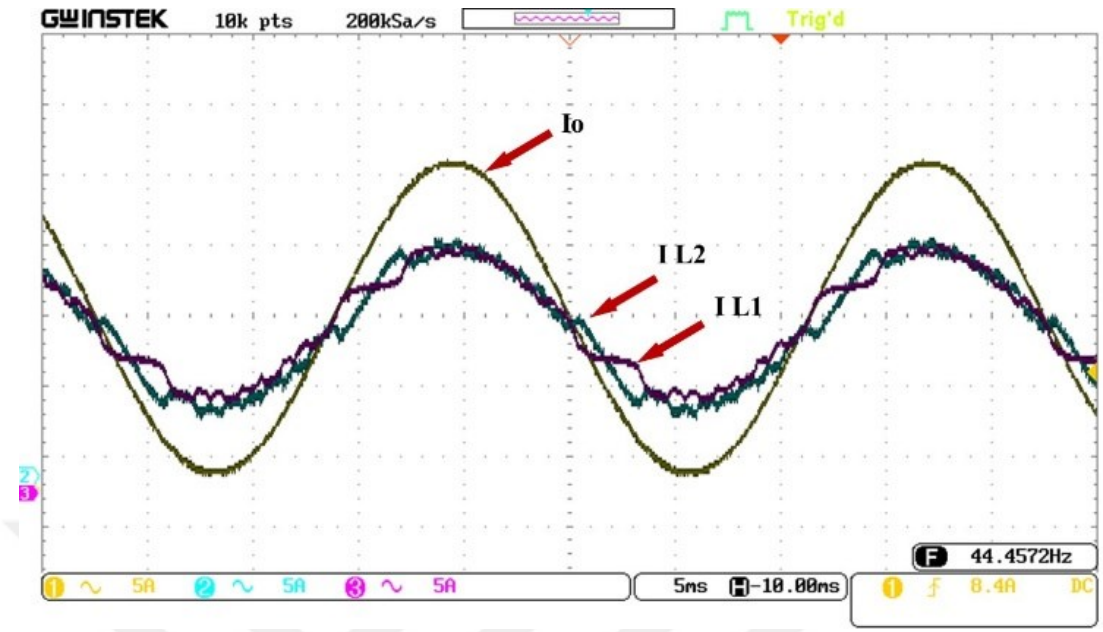


Fig. 4-19 Experimental waveforms for the proposed 17-level inverter (Io), (IL1), (IL2).

4.4. Chapter Conclusions

This chapter has provided a thorough analysis of the simulation studies performed on the proposed seventeen-level and five-level inverter designs using PSCAD/EMTDC software. The simulations offered valuable insights into the output voltage and current characteristics, as well as the voltage and current stresses experienced by each switching component in both topologies. Additionally, the behavior of currents and voltages across the two windings of the coupled inductor was closely examined, highlighting the performance and efficiency of the inductor design within each inverter. Experimental validation of the simulation results was also conducted, confirming the accuracy and reliability of the proposed designs. The findings underscore the robustness of the inverter models, establishing a solid foundation for their application in practical scenarios requiring efficient and reliable multilevel power conversion..

5. CONCLUSION

The thesis developed two topologies, the first design was a new single-phase Seventeen-Level Inverter topology, achieved through the incorporation of a coupled inductor, a bidirectional switch, and eight unidirectional switches. It also introduced a level-shifted Pulse Width Modulation (LS-PWM) technique for control and evaluation. Simulation and experimental results have been obtained for both resistive and inductive loads.

The second design was introduced as a novel single-phase five-level coupled inductor-based inverter. The proposed inverter offers several advantages, including a reduced number of switches, DC voltage sources, and the components required for switch control.

Based on the conducted comparative study of the two proposed inverters with other conventional topologies and considering the conducted loss calculations, the proposed multilevel inverters has significant advantages such as low components count, reduced voltage stress, remarkably reduced current stress on switches and so high efficiency. In addition, a cost comparison, based on cost calculations has been performed with a relevant inverter (using coupled inductor). The results verify that the proposed inverters are more economical and cost-effective. By evaluating all these factors, the proposed topologies demonstrate high performance and offer a competitive solution within the context of inverter technologies.

Moreover, the coupled inductor design, adjusted with the rated power of the proposed topologies, has been done so that the design results are used for both simulation and experimental. According to the performance validation through the

simulation and experimental results, the proposed MLIs successfully generate the expected voltage levels with equal voltage steps resulting in a high-quality output voltage and current with very low harmonic distortion. For instance, the output current THD was recorded as low as 0.4%.

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