ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE
ENGINEERING AND TECHNOLOGY

LOW POWER RF TRANSMITTERS FOR BIOIMPLANTS

M.Sc. THESIS

Kaan KULA

Department of Electronics and Communications Engineering

Electronics Engineering Programme

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

BİOIMPLANTLAR İÇİN DÜŞÜK GÜÇLÜ RF VERİCİ

YÜKSEK LİSANS TEZİ

Kaan KULA
(504151210)

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Tez Danışmanı: Asst. Prof. Tufan Coşkun KARALAR

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Kaan KULA, a M.Sc. student of ITU Graduate School of Science Engineering and Technology 504151210 successfully defended the thesis entitled "LOW POWER RF TRANSMITTERS FOR BIOIMPLANTS", which he/she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

Thesis Advisor :	**Asst. Prof. Tufan Coşkun KARALAR** Istanbul Technical University	....
Jury Members :	**Asst. Prof. Mustafa Berke YELTEN** Istanbul Technical University	....
	Assoc. Prof. Hakan DOĞAN Istanbul Medipol University	....
		....

Date of Submission : **03 May 2019**
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To my spouse,

FOREWORD

I would like to thank my advisor, Tufan Coşkun KARALAR, for his excellent help, support and academic guidance. I would like to express my gratitude to Hasan Bülent YAĞCI for his support in every sphere of my life. I thank all members of the BioPMIC project and VLSI Lab, for their help and suggestions. I would like to thank the committee members, Mustafa Berke YELTEN and Hakan DOĞAN for their attention of my project and valuable advices. I thank all family members for their encouragement. Finally, I would like to thank my spouse, Müge. Words will never express how much I love her. I am grateful to TUBITAK, The Scientific & Technological Research Council of Turkey. This work is supported by TUBITAK 215E082 project.

June 2019

Kaan KULA
(Electronics Engineer)

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ABBREVIATIONS

AIN : Aluminium Nitride
ASK : Amplitude Shift Keying
BAW : Bulk Acoustic Wave
CMOS : Complementary Metal Oxide Semiconductor
DC : Direct Current
ESD : ElectroStatic Discharge
FBAR : Thin-Film Bulk Acoustic Resonator
GHz : Gigahertz
ISM : Industrial, Scientific and Medical
LDO : Low-Dropout Regulator
LPA : Low Power Amplifier
mBVD : Modified Butterworth Van Dyke
NMOS : N-Channel Metal Oxide Semiconductor
NS : Negative-to-V_{SS}
OOK : On-Off Keying
PD : Positive-to-V_{DD}
PMOS : P-Channel Metal Oxide Semiconductor
RF : Radio Frequency
RFIC : Radio Frequency Integrated Circuit
SAW : Surface Acoustic Wave
WBAN : Wireless Body Area Network

SYMBOLS

C	**:** Capacitance
C_{ox}	**:** Oxide capacitance
g_m	**:** Transconductance
I	**:** Current
L	**:** Inductance
P	**:** Power
Q	**:** Quality factor
R	**:** Resistance
t	**:** Time
μ_n	**:** Electron mobility
V	**:** Voltage
ω_0	**:** Angular frequency

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LOW POWER RF TRANSMITTERS FOR BIOIMPLANTS

SUMMARY

Today's semiconductor technology enables the design and manufacture of the implantable RF circuits. The power sources are limited in implantable circuits. Low power wireless transmitters can transmit the information obtained from the human body to the external environment. The changes in the body can be continuously monitored without surgical intervention for every information.

In this project, FBAR-based low power 2.5 GHz RF transmitter is designed. Transmitter designed for 40nm CMOS technology includes digital logic gates, RF oscillator and low power amplifier circuits.

Digital data is transmitted by the switching of the carrier RF signal. On-off keying modulation does not require complex and power hungry circuits. Amplitude shift keying can be used as an alternative by using the ASK enable bit. If the corresponding bit is in OOK mode, the amplifiers of the oscillators are switched depending on the incoming data. When the oscillator amplifiers are closed, the transmitter almost does not consume energy . In the ASK mode, the oscillator amplifiers that are open remain in the open position regardless of the data. In this case, the data only adjust the gain setting of the low-power amplifier.

Oscillators used for RF signal synthesizing, are one of the most power hungry circuits in the RF chain. The losses of the resonators require high gain stages to ensure the oscillation. High gain leads to high power consumption which can cause the data losses. FBAR resonators are used in implantable RF transmitter circuits thanks to their small size and high quality factors. The RF oscillator consists of a 3-stage amplifier structure. The ability to adjust the gain and load capacities gives the transmitter flexibility in terms of use.

As a result, the aim of the project is to design a low-power RF transmitter suitable for biomedical applications. According to computer simulations, electrical characteristics of the circuit is suitable for biomedical application as well as the circuit size.

BİOIMPLANTLAR İÇİN DÜŞÜK GÜÇLÜ RF VERİCİ

ÖZET

Günümüz yarıiletken teknolojisi, vücut içerisine ve dokulara yerleştirilebilecek boyuttaki verici devrelerin tasarımına ve üretimine olanak tanımaktadır. Boyut sınırına ek olarak, İmplant edilebilir devrelerin güç kaynakları da oldukça sınırlıdır. Düşük güçlü RF vericiler, sınırlı enerji kaynaklarına rağmen, düşük güçte çalışabilecek şekilde tasarlanmaları sayesinde insan vücudundan elde edilen bilgileri dış ortama kablosuz olarak aktarabilmektedir. Veri aktarımının cerrahi müdahaleye gerek kalmadan tekrarlanabilir olması sayesinde vücutta meydana gelen değişiklikler sürekli olarak takip edilebilecektir.

Projede, 2.5 GHz frekansında çalışan FBAR rezonatörlü düşük güçlü RF verici tasarlanmıştr. 40nm CMOS teknolojisinde tasarlanan entegre devre içerisinde sayısal mantık kapıları, RF osilatör ve düşük güçlü kuvvetlendirici devreleri bulunmaktadır. Sayısal mantık kapılarından oluşan radyo kontrol devresi, giriş bitlerine göre, osilatörü ve düşük güçlü kuvvetlendiricinin çalışma koşullarını değiştirebilmektedir. Farklı uygulamalar ve amaçlar için, farklı çalışma modları desteklenmektedir.

Projede tasarlanan vericide sayısal veri, taşıyıcı işaretin veriye göre anahtarlanmasıyla iletilmektedir. Aç-kapa anahtarlamalı modülasyon ile verinin iletimi, güç tüketimi yüksek ve karmaşık devrelere ihtiyaç duyulmadan gerçekleştirilebilmektedir. Genlik kaydırmalı anahtarlama seçeneği, modülasyon seçim biti ile kullanılabilmektedir. İlgili bit aç-kapa anahtarlamalı modunda ise, osilatörlerin kuvvetlendiricileri gelen veriye bağlı olarak açılıp kapatılmaktadır. Mesaj işareti ile birlikte osilatörün de kapatıldığı durumda verici neredeyse hiç enerji harcamamaktadır. Genlik kaydırmalı anahtarlama modunda ise, açık olan osilatör kuvvetlendiricleri gelen veriden bağımsız olarak açık konumda kalmaktadır. Bu durumda gelen veri, sadece çıkış katı olarak kullanılan düşük güçlü kuvvetlendiricinin kazanç ayarını değiştirmektedir.

RF işaret üretimi için kullanılan osilatörler, verici devrelerde en fazla güç tüketimine neden olan RF bloklarından birisidir. Rezonatör devrelerindeki kayıplar, yüksek kazançlı kuvvetlendirici katlarına duyulan gereksinimi arttırmaktadır. Yüksek kazanç yüksek güç tüketimine neden olmakta, bu durum istenilen verinin aktarılamadan devrenin kapanmasına sonuçlanmaktadır. Bu nedenle düşük kayıplı, yüksek kalite faktörüne sahip rezonatör yapılarına ihtiyaç duyulmaktadır. FBAR rezonatörler, küçük boyutları ve yüksek kalite faktörleri sayesinde implant edilebilir RF verici devrelerinde kullanılmaktadır. FBAR rezonatörler, iki elektrot metali arasına yerleştirilen piezoelektrik malzeme ile üretilmektedir. Kalite faktörünü arttırmak için, bu yapı ile taban arasında hava boşluğu bırakılmaktadır. Bu hava boşluğu yapı ile tabanı birbirinden ayırarak elektromekanik kuplajın azaltımasını sağlamaktadır. RF osilatör 3 katmanlı paralel kuvvetlendirici yapısından oluşmaktadır. Her bir kuvvetlendiricinin geçiş iletkenliği 5mS olmak üzere, toplam geçiş iletkendiği 5mS aralıklarla 15mS

değerine kadar arttırılabilmektedir. Kazancın ve yük kapasitelerinin ayarlanabilir olması, vericiye kullanım alanı açısından esneklik sağlamaktadır. Osilatör devresinin faz gürültüsü, yapılan benzetimler neticesinde 100 kHz ötede -130 dBc/Hz olarak ölçülmüştür. Bu değer, literatürdeki diğer FBAR rezonatörlü osilatör devreleri ile karşılaştırılmış ve harcadığı güce karşılık elde edilen faz gürültüsü açısından diğer çalışmalara göre avantaj sağladığı gözlenmiştir. FBAR rezonatörlerin devreye bağlantı telleri ile bağlanması neticesinde, rezonatörün karakteristiğinde önemli değişiklikler meydana gelmektedir. Bağlantı tellerinden gelen endüktif etki, yeni yapının empedans karakteristiğinde ek bir endüktif bölge oluşturmaktadır. Yeni oluşan bölgenin endüktif olması nedeniyle, osilatörün bu bölgedeki bir frekansta parazitik osilasyona girme ihtimali bulunmaktadır. Osilatörün bu bölgedeki kazanç durumu da kontrol edilmiş ve ek bir önlem olarak, osilatörün giriş ve çıkışna ayarlanabilir kapasite eklenmiştir.

Düşük güçlü kuvvetlendirici, osilatör çıkışındaki işareti yük direncine en verimli şekilde aktarmak için tasarlanmıştır. Kuvvetlendiricinin yüksek giriş direnci sayesinde, osilatör çıkışına, arada başka bir devre olmadan bağlanabilmektedir. Ek bir tampon devresine ihtiyaç duyulmaması, devrenin toplam güç tüketimini azaltmaktadır. Düşük güçlü kuvvetlendiricinin azaltılmış iletim açısı, savak akımını yarım sinüs işareti şekline getirmekte ve harmonik bileşenler oluşturmaktadır. Çıkışta kullanılan empedans uyumlama devresi, tranzistörün savağında oluşan harmonik bileşenleri süzgeçleyerek, yüke temiz bir sinüzoidal işaret aktarımına olanak tanımaktadır. Empedans uyumlama devresinde kullanılan endüktansın kalite faktörü ile kuvvetlendiricinin verimi arasında doğrudan bir ilişki vardır. Ayrık devrelerde kullanılan endüktanslar yüksek kalite faktörlerine sahipken, entegre devrelerde kullanılan endüktansların kalite faktörler oldukça sınırlıdır. Projede empedans uyumlama devresinde kullanılan endüktansın kalite faktörü yaklaşık 10 olarak hesaplanmıştır. Devrenin implant edilebilir sensörlerde kullanılacak olması nedeniyle, tümleşik bir yapıda olması önemlidir. Bu nedenle devrede yüksek kalite faktörlerine ayrık endüktans kullanılmamıştır..

FBAR bağlantıları ve RF çıkış için, projeye özel pad tasarımı gerçekleştirilmiştir. RF Padler, düşük kapasite değerine sahip olacak şekilde tasarlanmıştır. Devrenin herhangi bir ESD olayından etkilenmemesi için, hem RF bağlantılarına, hem de sayısal girişlere ESD koruma devreleri tasarlanmıştır. Sayısal girişlerin ESD koruma devreleri, seri direnç ve iki adet eviriciden oluşmaktadır. RF bağlantıların ESD koruması ise, RF hat üzerinden besleme ve toprağa yapılan diyot bağlantıları ile sağlanmıştır.

Devrenin RF kısmının besleme gerilimi 0.8V, sayısal kısmının besleme gerilimi 1.1V olarak belirlenmiştir. Kontrol girişleri 1.1V sayısal girişleri desteklemektedir. RF çıkış gücü, uygulamaya uygun olarak, alıcı ve verici arasındaki link bütçesine uygun olarak tasarlanmıştır. Kısa mesafe haberleşmesinde kullanılacak olan bu devrenin çıkış gücü -20 dBm olarak belirlenmiştir. Yapılan literatür araştırmasına göre, implant edilebilir radyoların çalışma mesafeleri 2 metreden az olmaktadır. Yapılan benzetimlere göre, devrenin harcadığı güç yaklaşık 450 μW olarak tespit edilmiştir. Devrenin toplam alanı $0.16mm^2$ olarak hesaplanmış ve bu değerin, literatürde karşılaştırılan diğer düşük güçlü verici boyutlarına göre oldukça düşük olduğu görülmüştür. Devrenin RF çıkışının, 50Ω yük direncine uyumluluğu da test edilmiştir. Yapılan test neticesinde geri dönüş kaybının 10 dB değerinden daha düşük olduğu görülmüştür. Devrenin çalışması için çip dışı devre elemanı olarak sadece FBAR rezonatörünün bağlanması yeterlidir. Empedans uyumlama devreleri ve diğer pasif elemanlar entegre devre içerisinde gerçeklenmiştir.

Sonuç olarak, projede biyomedikal uygulamalarda kullanılmaya uygun, düşük güçlü RF verici tasarımı hedeflenmiştir. Tasarlanan devrelerin bilgisayar benzetimleri gerçekleştirilmiş, boyutunun ve elektriksel özelliklerinin de bu uygulamalar için uygun olduğu görülmüştür.

1. INTRODUCTION

1.1 Purpose of Thesis

Wireless Body Area Networks (WBANs) are the short range wireless networks that provide continuous health monitoring. The network consist of different sensors which are located to different parts of the human body. These sensors can be wearable or implantable and each of them can be used for different purposes [3] [4]. The sensors which are implanted in the body can be placed underneath the skin or in the blood stream [5]. In this thesis, RF transmitter section of the implantable sensors will be discussed and designed.

Low power RF transmitters are highly demanded for biomedical implants because of the lack of energy sources. In addition to power consumption, circuit size is another uncompromisable parameter for these applications. The proposed transmitter is suitable for implantable biomedical applications in terms of circuit size and power consumption. Such applications generally do not require high data rate and bandwidth. Therefore, single carrier and OOK modulation are used to achieve reliable and efficient communication.

The purpose of the thesis is to design an implantable low power RF transmitter and clarify the design steps and parameters of the RF blocks in the transmitter chain.

1.2 Literature Review

Low power RF transmitters have been studied in different works. In [6], FBAR oscillator based RF transmitter has been designed. The transmitter have three different FBAR oscillator that oscillates in different frequencies in the 2.4 GHz frequency band. Each FBAR oscillator and transmitter consumes 150μW and 440pJ/bit at -12.5 dBm, respectively. In [7] and [8], the oscilation frequency of the FBAR oscillators is 1.9

GHz. The power consumption and output power of the transmitters are 1.1mW, -3 dBm and 3mW, 0 dBm, respectively.

1.3 Design Summary

The proposed transmitter consists of three main blocks: digital controller, oscillator and low power amplifier as shown in Figure 1.1. Desired parameters are listed in Table 1.1.

Table 1.1 : Desired parameters for the implantable RF transmitter.

Parameter	Value
RF Supply	0.8V
Digital Input Voltage	1.1V
Carrier Frequency	2.5 GHz
RF Output Power	-20 dBm
Startup Time	4 μs
Power Consumption	< 1mW (Max)
Power Consumption	< 500 μW (Typical)
Off-Chip Components	Only FBAR
Supported Modulations	OOK, ASK
Circuit Size	0.16mm^2
Output Return Loss	< -10 dB

The supply voltage of the transmitter is 0.8V and digital inputs are 1.1 V. The transmitter should be compatible with the voltage level of the digital inputs. Level shifters are used in Digital Controller subcircuit.

Carrier frequency is determined by the resonance frequency of the FBAR resonator. In this transmitter, carrier frequency is 2.5 GHz which is one of the ISM frequencies.

RF output power is determined with the link budget between TX and RX devices [9]. Operating range of the implantable radios are generally less than 2 meters [10]. According to various scenarios, Smartphones can serve as a receiver and control point for transmitted medical data [11] [12] [13].

Startup time of the oscillator settles the data rate of the transmitter. Therefore, there is a trade-off between data rate and power consumption.

The power consumption of the transmitter is different for its on and off states. When the transmitter is on, the power consumption should be less than 1 mW. If the probability of the transmitting '1' and '0' is assumed equal to each other and there is no power consumption in off state, typical power consumption becomes the half of the maximum consumption.

Output of the transmitter should be matched to 50 Ω. Poor impedance matching may degrade the antenna characteristic and radiated power.

External interfaces of the transmitter are defined in Figure 1.1 and explained in Table 1.2.

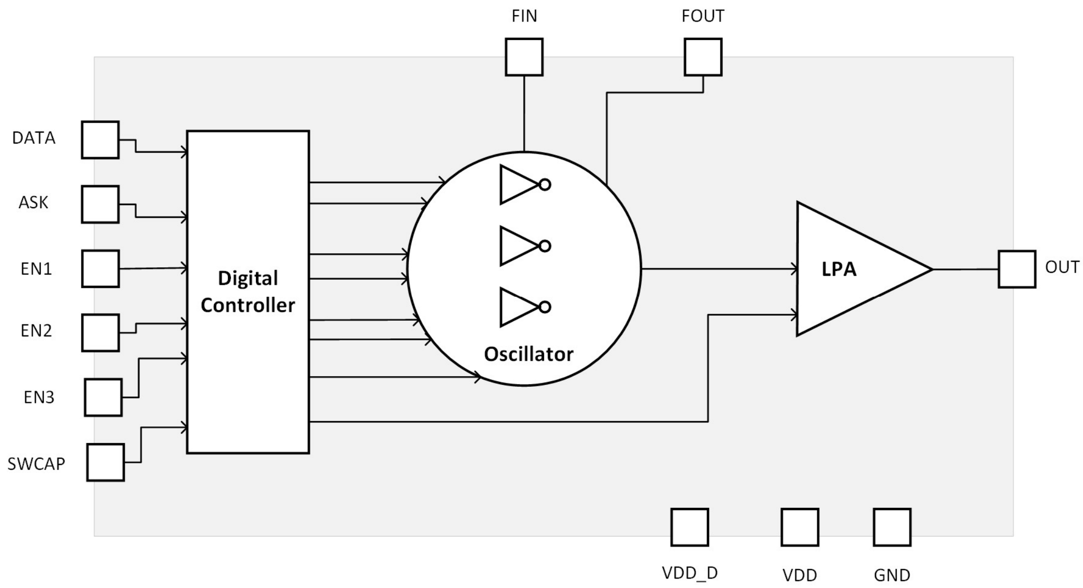

Figure 1.1 : External interfaces of the RF transmitter

Table 1.2 : External interfaces of the RF transmitter.

Interface Name	Description
VDD	0.8 VDC
VDD_D	1.1 VDC
GND	0 V
DATA	Message Signal (Serial, 1.1 V)
ASK	'1' : ASK, '0' : OOK
EN1	'1' : Enable, '0' : Disable (1^{st} Inverter)
EN2	'1' : Enable, '0' : Disable (2^{nd} Inverter)
EN3	'1' : Enable, '0' : Disable (3^{rd} Inverter)
SWCAP	+200fF load capacitance to FIN and FOUT
FIN	FBAR Connection
FOUT	FBAR Connection
RFOUT	RF Output, 50Ω

1.4 Thesis Organization

This thesis is divided into five chapters. The first chapter introduces the project overview and design parameters. Chapter 2 presents the theoretical background and calculations of the RF transmitter subcircuits. Chapter 3 describes the design principles and practical concerns of the low power RF circuit design. Simulation results of each subcircuit will be given in this chapter. Final circuit layouts and simulation result after integration is given in Chapter 4. Final chapter summarizes the project results and points out the critical steps of the whole project.

2. LOW POWER RFIC TRANSMITTER

In this chapter, the general structure and circuit blocks of the low power RF integrated transmitters will be defined.

2.1 Transmitter Structure

The basic function of the low power transmitter is to synthesize and amplify the signal to send the data over the air. These transmitters are called as direct modulation transmitters [14]. Figure 2.1 shows the general structure of the designed direct modulation transmitter. There is no frequency conversion on the RF chain. Mixers increase the current demand of the transmitter. Modulation of the message is applied to the signal by switching the oscillator in OOK modulation.

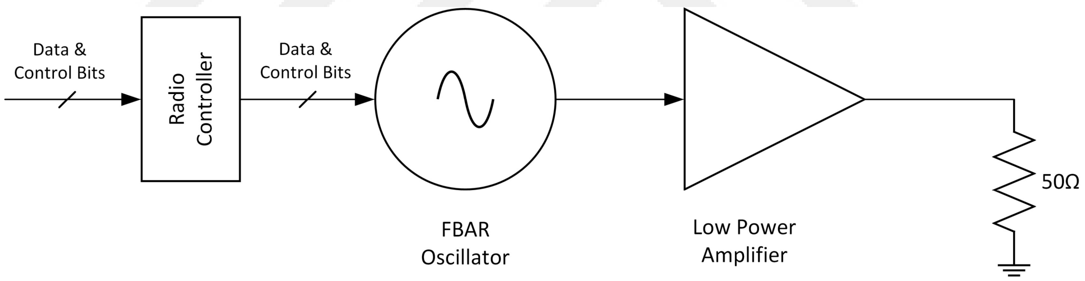

Figure 2.1 : General representation of the low power direct modulation transmitter.

Radio controller consists of the logic gates which reorganize to data and configuration bits.

An FBAR oscillator is used to synthesize the RF signals. Because of the power concerns of the transmitter, using FBAR resonator decreases the current demand to start and sustain the oscillation.

2.1.1 Modulation

The transmitter supports ASK ve OOK modulations. These modulations do not require complex circuits which consume much power. In amplitude modulation, only amplitude of the signal is changed, leaving phase and frequency of the signal is constant. According to Equation 2.1, $A(t)$ is the digital baseband signal and the frequency and phase is constant.

$$s(t) = A(t)cos(w_c t + \phi_0) \tag{2.1}$$

The modulation index of ASK modulation is calculated from the Equation 2.2. As shown in Figure 2.2, A_{max} and A_{min} are the maximum and minimum signal magnitudes, respectively. When the digital baseband input is logic high, the amplitude of the output signal is A_{max}. In the same way, when the digital baseband input is logic low, the amplitude of the output signal is A_{min}

$$m_{ASK} = \frac{A_{max} - A_{min}}{A_{max} + A_{min}} \tag{2.2}$$

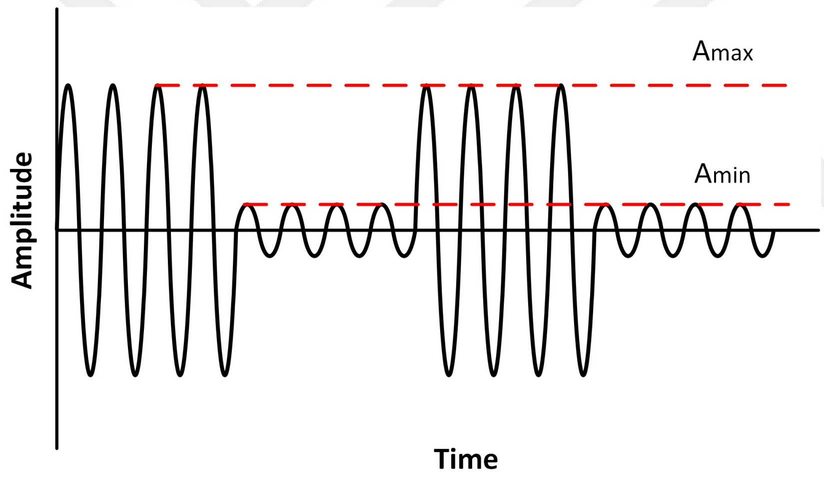

Figure 2.2 : RF waveform of the ASK modulation.

OOK modulation is the special case of ASK modulation. If the A_{min} of ASK modulation is 0, this type of modulation is called as OOK modulation. Therefore, the modulation index of OOK is 1.

ASK and OOK modulations are phase independent and can be demodulated by non-coherent receivers.

2.2 FBAR Oscillator

FBAR based Pierce oscillator is designed to synthesize 2.5 GHz RF signal. FBAR resonators are useful to design low power oscillator because of their high quality factor in small areas [15]. Pierce oscillators are generally used for integrated oscillators because of their basic structures and grounded load capacitors.

2.2.1 FBAR Resonator

Different types of resonators have been used in RF oscillator design. LC and Crystal resonators are widely used in discrete oscillator design. LC type resonators have lower quality factor and temperature tolerance compared to crystal resonators. Both of them are inappropriate for integrated designs. Acoustic resonators exhibit higher performance in terms of quality factor, temperature tolerance and size. SAW and BAW resonators convert the electrical signal to the acoustic wave**??**. BAW resonators have higher quality factor and lower insertion loss at higher frequency range. Therefore, FBAR resonator, a type of BAW resonator, is used to 2.5 GHz integrated oscillator.

FBAR resonators have one piezoelectric layer which is surrounded by two metal electrodes which are Aurum (Au) or Chromium (Cr). The piezoelectric layer is generally made from Aluminum nitride (AIN), zinc oxide (ZnO) or cadmium sulfide (CdS). The air gap can be used to improve the quality factor. An air gap decreases the electromechanical coupling to the substrate [16]. The crosssection of the FBAR resonator is shown in Figure 2.3.

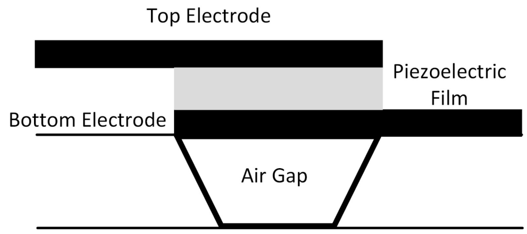

Figure 2.3 : The crosssection of the FBAR resonator. [1]

FBAR resonators can be accuretely modeled using the Modified Butterworth Van Dyke model as shown in Figure 2.4. The motional branch consists of L_m, C_m and R_m. Series resonance frequency is a function of L_m and C_m. C_0 resonates with the motional branch at the parallel resonance frequency. The mBVD model accounts for dielectric and ohmic losses using R_0 and R_S resistances.

Series and parallel resonance frequencies are calculated using Equation 2.3 and Equation 2.4. The resonance and antiresonance frequencies, at which reactance is zero, are equal to series and parallel resonance frequencies respectively if the material

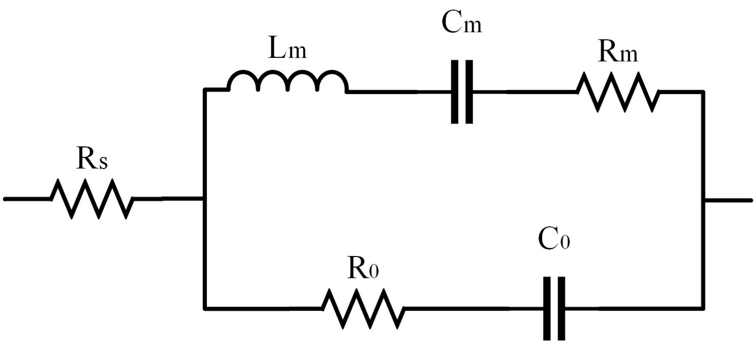

Figure 2.4 : The mBVD model of the FBAR resonator.

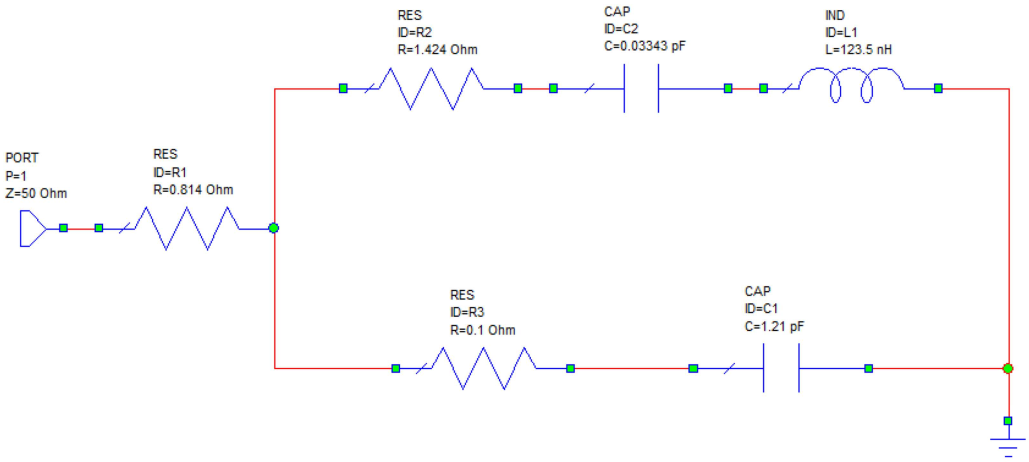

Figure 2.5 : Simulation setup to measure the impedance of the FBAR resonator.

losses are ignored [17].

$$f_s = \frac{1}{2\pi\sqrt{L_m C_m}} \tag{2.3}$$

$$f_p = f_s\left(1 + \frac{C_m}{2C_0}\right) \tag{2.4}$$

To obtain the impedance of the FBAR resonator, simulation setup shown in Figure 2.5 is used. Figure 2.6 shows the impedance of the FBAR resonator. For the frequencies which are lower than series resonance and higher than parallel resonance , FBAR resonator behaves like a capacitor. However, for the frequencies which are lower than paralel resonance and higher than series resonance frequency , FBAR resonator behaves like an inductor. In this frequency region, the impedance of the resonator increases with the frequency. Phase condition of the Barkhausen criteria is satisfied in the inductive region. According to Equation 2.5, the oscillation frequency is higher than the series resonance frequency [1].

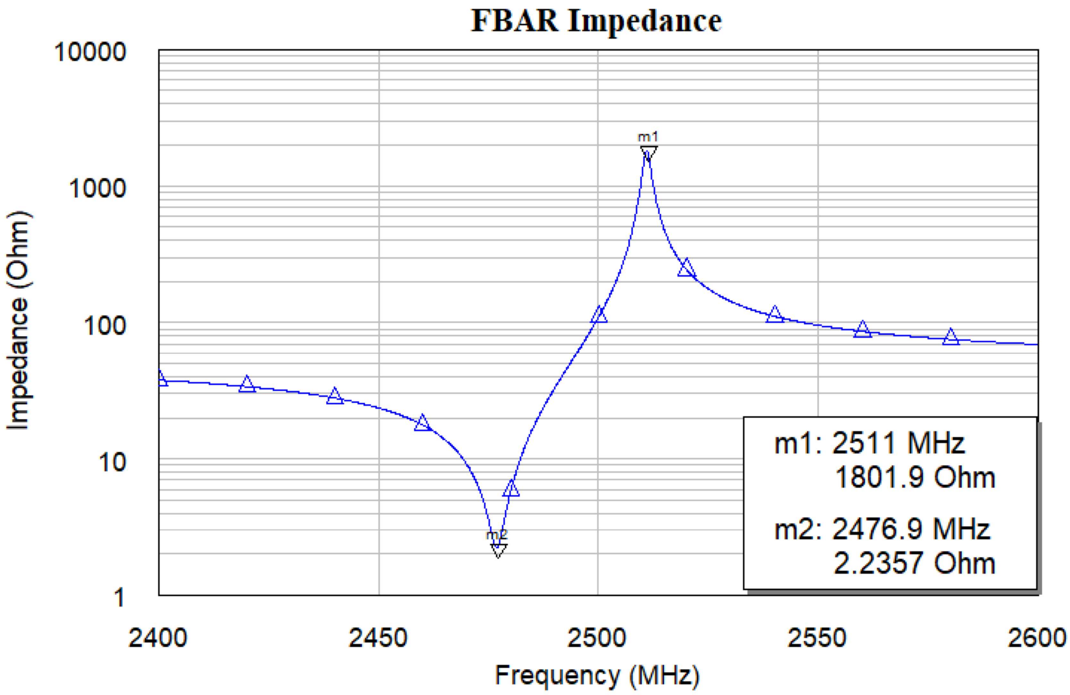

Figure 2.6 : The impedance of the FBAR resonator ($f_s \approx 2476.9$ MHz, $f_p \approx 2511$ MHz).

$$f_{osc} = f_s \sqrt{1 + \frac{C_m}{C_T}} \tag{2.5}$$

In the equation, C_m is the modeled capacitance in the motional branch and C_T is the total capacitance including C_0 and other circuit and loading capacitors.

Coupling coefficient quantifies the difference between series and resonance frequency as shown in Equation 2.6. For the AIN FBAR resonators, the typical value of the coupling coefficient is %3 - %7. Large K_t^2 is more desirable for the oscillators which have a wide tuning range [18].

$$K_t^2 = \frac{\pi^2 (f_p - f_s)}{4 f_s} \tag{2.6}$$

2.2.2 Pierce Oscillator

An oscillator circuit should satisfy the gain and phase requirements to sustain the oscillation in steady-state condition. These requirements are called as Barkhausen Criteria.

An oscillator circuit can be modelled as a linear feedback system as shown in Figure 2.7. In steady-state condition, the closed loop gain should be unity and total phase shift should be an integer multiple of the 360° as stated in Equation 2.7 and 2.8.

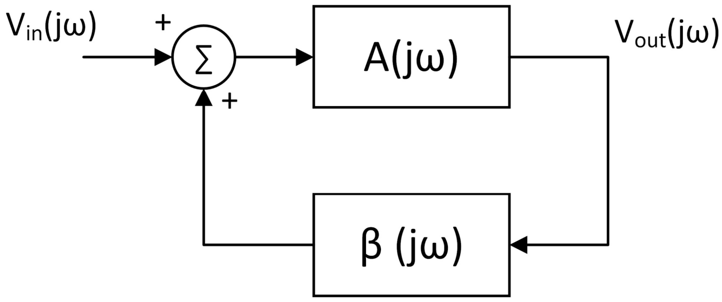

Figure 2.7 : Block diagram of a linear feedback circuit.

$$|A(j\omega)\beta(j\omega)| = 1 \tag{2.7}$$

$$\angle A(j\omega)\beta(j\omega) = n \cdot 360^\circ \tag{2.8}$$

There are different types of the crystal oscillator circuit in the literature. Pierce, Colpitts, Butler and Clapp are the mostly used ones. Pierce oscillator is a derivative of the Colpitts oscillator. The difference between the two structure is the choice of the signal ground [19]. As shown in 2.8, feedback resistor, Rb, is used to bias CMOS inverter to equalize the gate and drain voltages to VDD/2. Half supply voltage allows to maximum swing at the output of the oscillator.

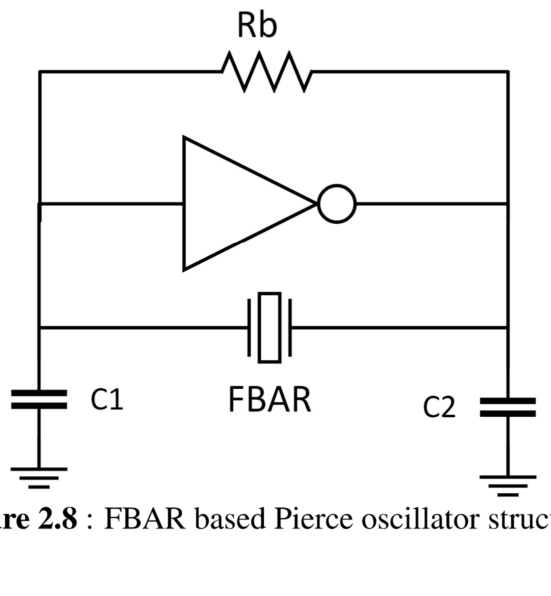

Figure 2.8 : FBAR based Pierce oscillator structure.

Three-point oscillator analysis is useful to calculate the negative impedance. As shown in 2.9, the circuit is divided into two groups: passive RLC resonant circuit and active circuit whose Z_C is the input impedance of the active part . To satisfy the start-up condition of the oscillator, the real part of the Z_C should be 2 or 3 times lower than -R_m. When the circuit reaches the steady-state, the real part of the Z_C should be equal to -R_m.

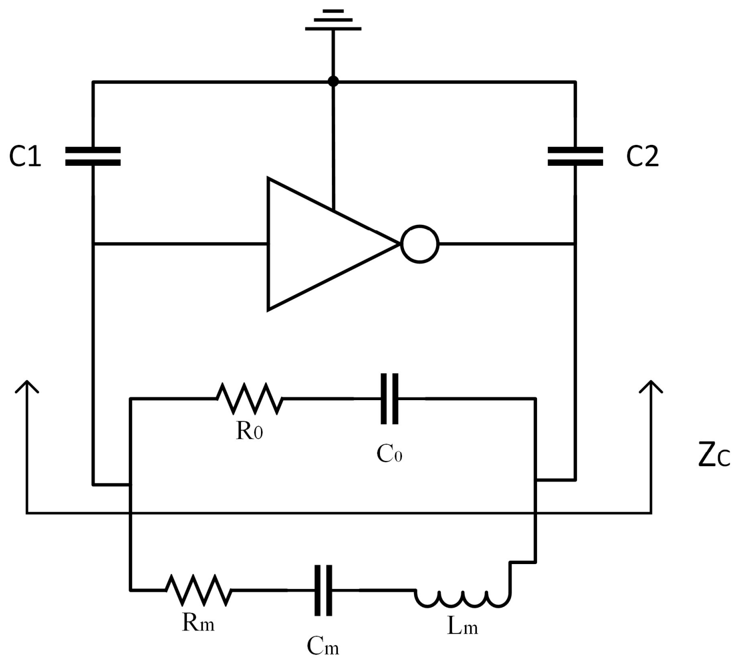

Figure 2.9 : General form of the three-point oscillator circuit.

Equation 2.12 is used to calculate the input impedance of the active part of the oscillator circuit [20]. Z_1, Z_2 and Z_3 are the impedance of the C_1, C_2 and series combination of the R_0 and C_0, respectively. To minimize the real part of the Z_C, C_1 and C_2 should be equal. As shown in Figure 2.10, if g_m, C_0 and R_0 are 10ms, 1.21pF and 0.1Ω, respectively, to obtain the minimum impedance C_1 and C_2 should be equal to 600fF. It should be noted that calculations of the capacitors are performed with 100f steps as shown in Appendix A.1. C1 and C2 are loading capacitances which are summation of fixed capacitors, tuning capacitors, CMOS and pad capacitances.

$$Z_C = \frac{Z_1Z_3 + Z_2Z_3 + g_mZ_1Z_2Z_3}{Z_1 + Z_2 + Z_3 + g_mZ_1Z_2} \tag{2.9}$$

$$Z_1 = \frac{1}{j\omega C_1} \tag{2.10}$$

$$Z_2 = \frac{1}{j\omega C_2} \tag{2.11}$$

$$Z_3 = R_0 + \frac{1}{j\omega C_0} \tag{2.12}$$

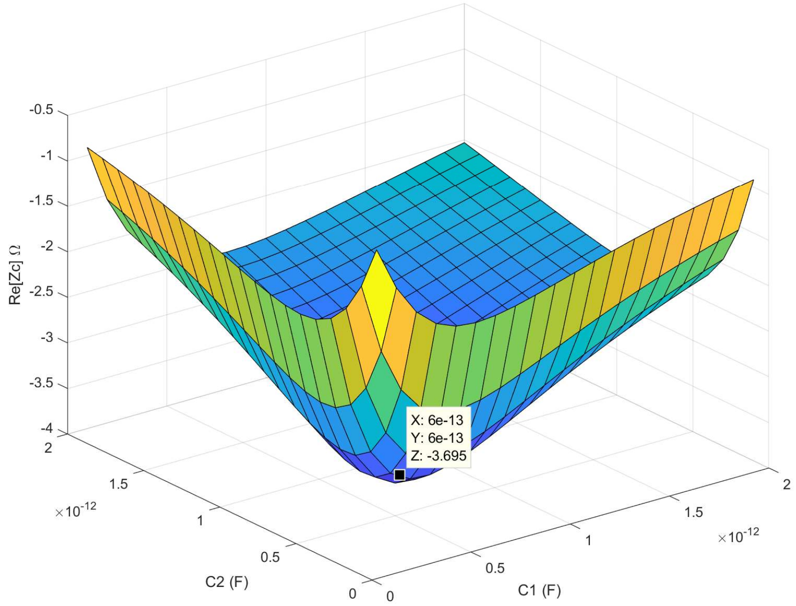

Figure 2.10 : Negative resistance of the oscillator circuit impedance,Z_C ($g_m = 10$ms, $C_0 = 1.21$pF, $R_0 = 0.1\Omega$).

In the oscillator circuits, increasing of the transconductance does not guarantee the improved real negative impedance. As shown in Figure 2.11, there is an optimum transconductance for the lowest real negative impedance.

Load capacitors are 600fF in Figure 2.11. However, optimum load capacitors may exist for each transconductance. Therefore, min[Z_C] - transconductance graph is more useful to reach the optimum power consumption.

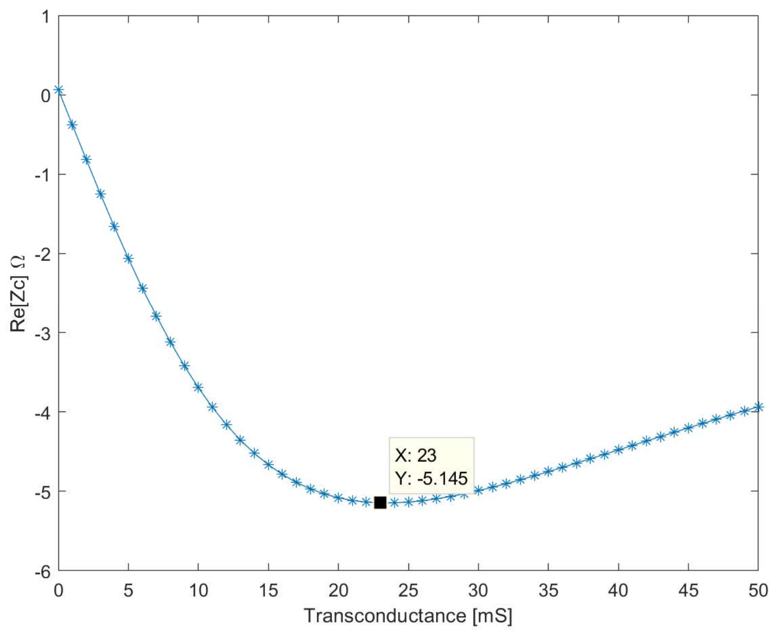

Figure 2.11 : Real part of the negative impedance is decreasing until the optimum transconductance.

2.3 Low Power Amplifier

Cascode amplifier structure is used as a low power amplifier for the transmitter. M0, called as input device, produces the current proportional to the input voltage [21]. Because of the reduced conduction angle, there are current peaks in the drain current. Matching network filter outs the harmonics and pure sinusoidal signal flow to the load as shown in Figure 2.12.

In 40nm design, voltage difference between transistor terminals should be lower than 1V [21]. Cascode structure protects the transistors from voltage stress. In this project, VDD remains below 1V, however; cascode structure is used to prevent the circuit from unexpected conditions.

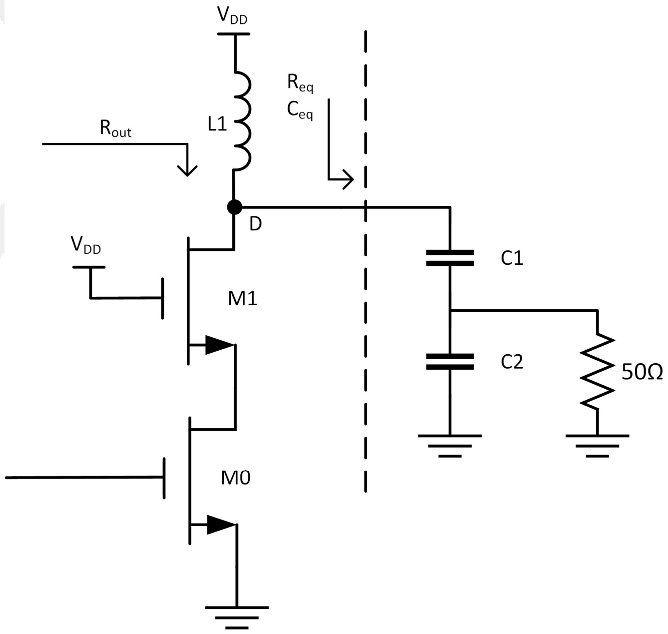

Figure 2.12 : The cascode structure and tapped-capacitor matching network of the low power amplifier [2].

The fundamental frequency component of the drain current, DC current, output power and drain efficiency are calculated from Equation 2.13, 2.14, 2.16 and 2.18, respectively [22].

$$I_{DC} = \frac{I_{dd}}{\pi}(siny - ycosy) \tag{2.13}$$

$$I_1 = \frac{I_{dd}}{2\pi}(2y - sin2y) \tag{2.14}$$

The fundamental drain current calculated from Equation 2.14 flow through the resistances seen at the node D. The fundamental current flows through the R_{eq} is calculated using Equation 2.15.

$$I_{Req} = I_1 \left(\frac{R_{ind} \parallel R_{out}}{R_{ind} \parallel R_{out} + R_{eq}} \right) \tag{2.15}$$

$$P_{out} = \frac{1}{2} I_1^2 \left(\frac{R_{ind} \parallel R_{out}}{R_{ind} \parallel R_{out} + R_{eq}} \right)^2 R_{eq} \tag{2.16}$$

$$\eta = \frac{P_{out}}{P_{dc}} = \frac{1}{2} \left(\frac{I_1}{I_{DC}} \right) \left(\frac{V_D}{V_{DD}} \right) \left(\frac{R_{ind} \parallel R_{out}}{R_{ind} \parallel R_{out} + R_{eq}} \right)^2 \cdot \left(\frac{R_{eq}}{R_{ind} \parallel R_{out} \parallel R_{eq}} \right) \tag{2.17}$$

$$\eta = \frac{1}{2} \left(\frac{I_1}{I_{DC}} \right) \left(\frac{V_D}{V_{DD}} \right) \left(\frac{R_{ind} \parallel R_{out}}{R_{ind} \parallel R_{out} + R_{eq}} \right) \tag{2.18}$$

R_{out} is the output resistance of the cascode, R_{ind} is the resistance of the inductor, V_d is the RF voltage at node D and I_{dd} is peak drain current when conduction angle is π. 2y is the conduction angle.

The input voltage of the low power amplifier is large and switching the input device continuously. Therefore, the low power amplifier can be considered as DC-RF converter [23] [24]. Looking at the circuit from the energy flow point of view, the input power is supplied from the DC voltage source.

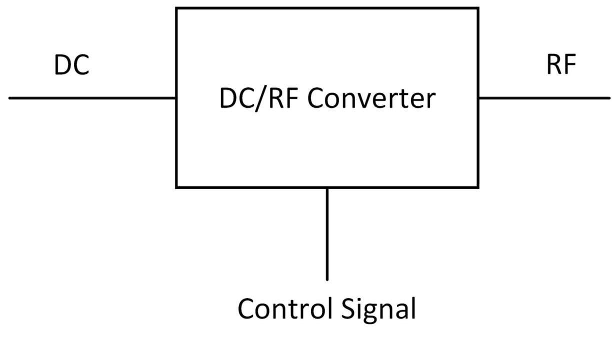

Figure 2.13 : Input signal of the amplifier can be considered as control signal of the DC/RF converter.

The tapped-capacitor impedance matching network design equations are given below [25]. Tapped-capacitor structure and component names are shown in Figure 2.14.

$$L = \frac{R_{in}}{\omega_0 Q} \tag{2.19}$$

$$C_2 = \frac{Q_2}{\omega_0 R_2} = \frac{\sqrt{\frac{R_L}{R_{in}}\left(Q^2+1\right)-1}}{\omega_0 R_L} \tag{2.20}$$

$$C_1 = \frac{C_2\left(Q_2^2+1\right)}{QQ_2 - Q_2^2} \tag{2.21}$$

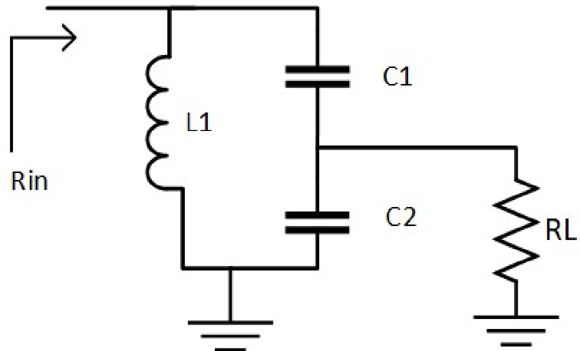

Figure 2.14 : Tapped-capacitor resonator circuit as an impedance transformer.

FBAR oscillator is directly connected to the input port of the low power amplifier. This connection increases the FBAR oscillator power consumption. However, eliminating the buffer or driver stage leads to power consumption reduction.

2.4 Digital Radio Controller

Digital radio controller makes the oscillator more flexible and suitable for different applications. Transconductance, load capacitance and modulation type are adjustable parameters. Digital circuit should meet the truth table requirements shown in Table 2.1.

The control bit of the load capacitors is directly connected to switched capacitors. Therefore, SWCAP (1.1V) is not included to Table 2.1

Table 2.1 : Truth table of the digital radio controller

DATA (1.1V)	ASK(1.1V)	EN(1.1V)	EN(0.8V)	$\overline{EN}$(0.8V)
0	0	0	0	1
1	0	0	0	1
0	1	0	0	1
1	1	0	0	1
0	1	1	1	0
1	1	1	1	0
0	0	1	0	1
1	0	1	1	0

3. CMOS TRANSMITTER CIRCUIT DESIGN

The theoretical background of the transmitter has been given in Chapter 2. Design steps of these stages using active and passive electronic components will be discussed in this chapter.

3.1 Passive Components

Resistors are realized with P+ poly resistor without salicide which offers highest sheet resistance in the process. The resistors with salicide have less sheet resistance than that of the resistors without salicide. These resistors are used to apply the gate voltage to the transistors.

MOM capacitors are used in the circuit for DC blocking and impedance matching. MOM capacitor are implemented in standard CMOS process, does not need an additional mask layer [26]. The parasitic capacitances between metal layers constitude the total capacitance of the MOM capacitor. With the advances in CMOS technology, the distance between metal layers are decreases, thus resulting in higher capacitance density [27].

Integrated spiral inductors have low quality factor of approximately 10. The quality factor is limited by the substrate losses and metal resistance. To reduce the metal resistances, upper thick metal layers can be used [28].

The interconnects can be modelled by low-pass RC circuits. Equivalent resistance is dependent on dimensions and material of the interconnect. Resistance of the interconnect is calculated from Equation 3.1, using sheet resistance, R_S. Sheet resistance is a function of bulk resistivity and thickness of the material as shown in Equation 3.2. The bulk resistivity of the metals commonly used in electronics is listed in Table 3.1.

$$R = R_s(\frac{L}{W}) \tag{3.1}$$

$$R_s = \frac{\rho}{t} \tag{3.2}$$

Table 3.1 : Bulk resistivity of the metals.

Metal	Bulk Resistivity ($\mu\Omega * cm$)
Silver (Ag)	1.6
Copper (Cu)	1.7
Gold (Au)	2.2
Aluminum (Al)	2.8

The capacitance of the interconnect is related with its dimensions and interval to the substrate. Accoring to Equation 3.3, large connections and bottom layers have higher parasitic capacitances.

$$C = \varepsilon \frac{A}{d} \tag{3.3}$$

3.2 FBAR Oscillator

According to the negative resistance approach, to satisfy the gain requirement of the oscillator, absolute negative resistance of the active circuit should be higher than the resistance of the resonator. The required transconductance will be supplied from self-biased CMOS inverter as shown in Figure 3.1. The total transconductance is the sum of the transconductance of the PMOS and NMOS transistors which are using the same current. By the help of this property of the CMOS inverter, supplied current is used efficiently.

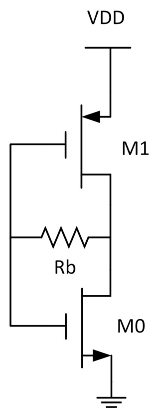

Figure 3.1 : Self-Biased CMOS Inverter.

To test the inverter, the simulation setup in Figure 3.2 is used. RF voltage signal is applied to the input and output current is measured to find the transconductance of the self-biased inverter.

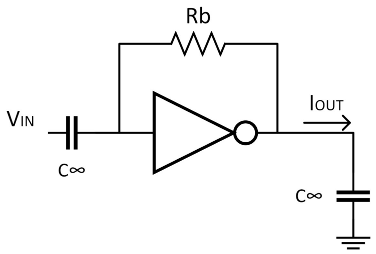

Figure 3.2 : The simulation setup of the self-biased inverter.

The three inverters will be used to adjust the total transconductance of the oscillator. The transconductance of the one inverter is determined according to the losses of the FBAR resonator. As simulated in the previous chapter, negative resistance is dependent to load capacitors. Designed inverters have 5mS transconductance as shown in Figure 3.3. Therefore, each transistor has 2.5 mS transconductance.

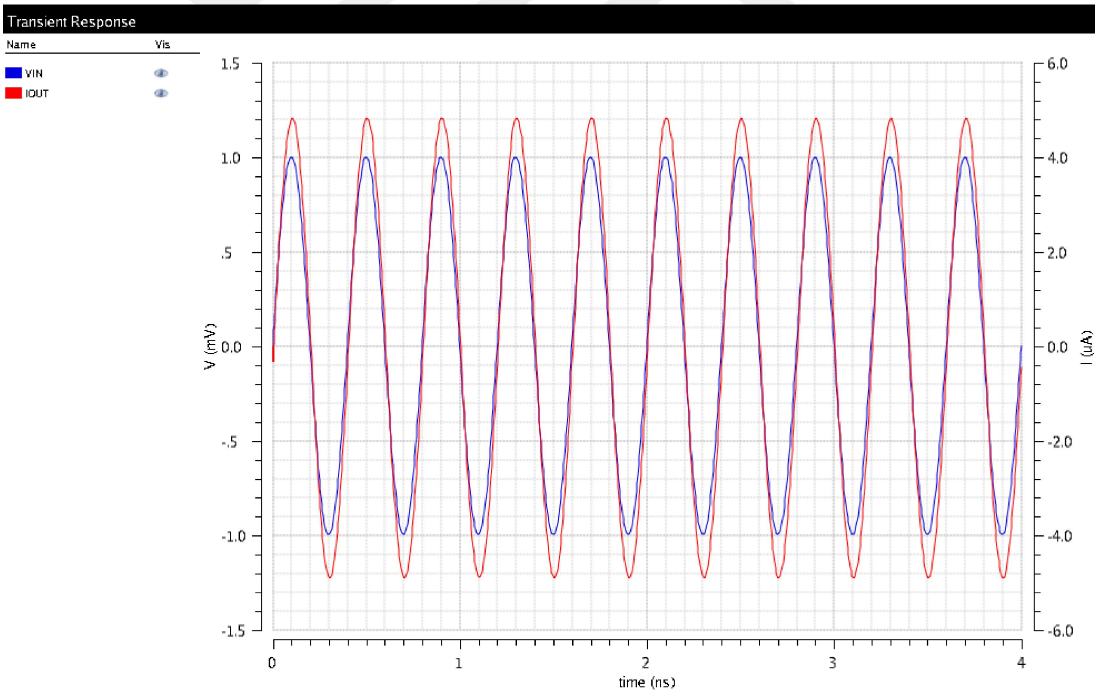

Figure 3.3 : Input voltage and output current waveform of the self-biased inverter.

According to Equation 3.4, the transconductance of the transistor is proportional to its square root of drain current. However, transconductance efficiency is not equal for all values of the I_D. In low power applications, transistors should supply the transconductance as efficiently as possible.

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \tag{3.4}$$

To simulate the transconductance efficiency of the transistor, the setup shown in Figure 3.4 is used.

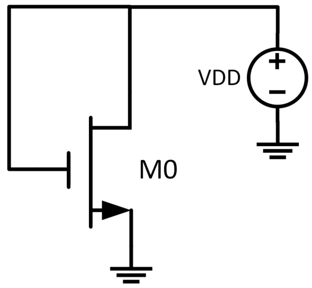

Figure 3.4 : Simulation setup to obtain the transconductance efficiency of the MOSFET.

As shown in Figure 3.5, transconductance efficiency is higher in low voltages. However, transconductance is much smaller in this operation region. To obtain higher transconductance at the same voltage, the width of the transistor can be increased. To equalize the transconductance of the NMOS and PMOS, the width of the PMOS transistor should be high than that of NMOS transistor.

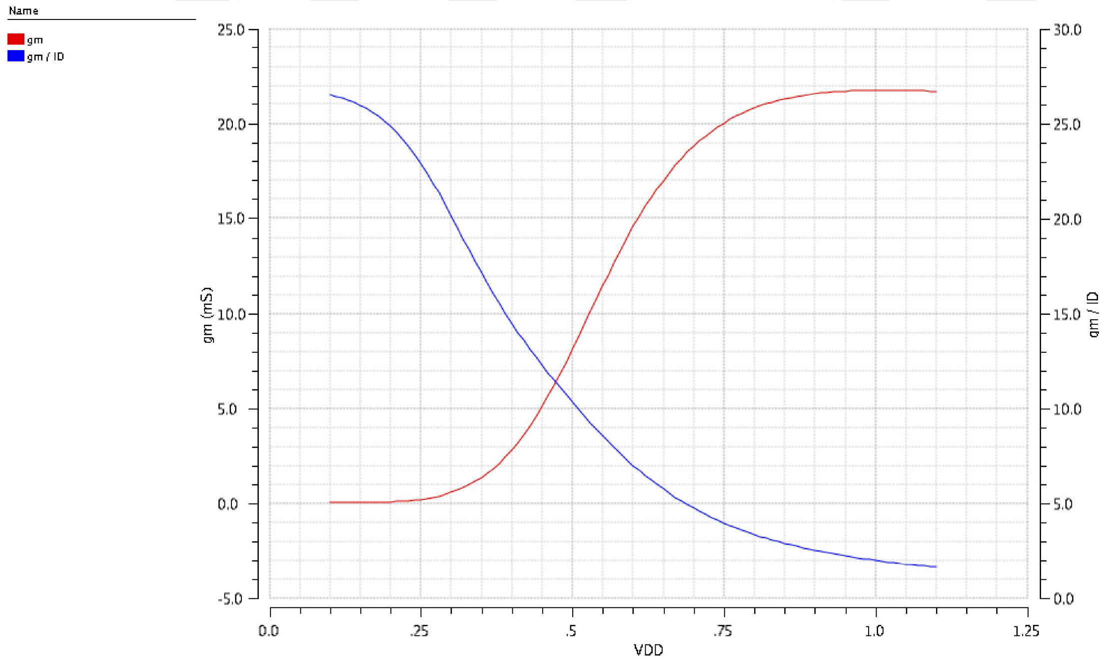

Figure 3.5 : gm and gm/ID curves of the NMOS transistor used for oscillator inverter.

After the transistor dimensions are determined, FBAR resonator and load capacitors have been calculated from the previous section are connected to the active circuit. Simulation is performed under different transconductance values with 5mS steps.

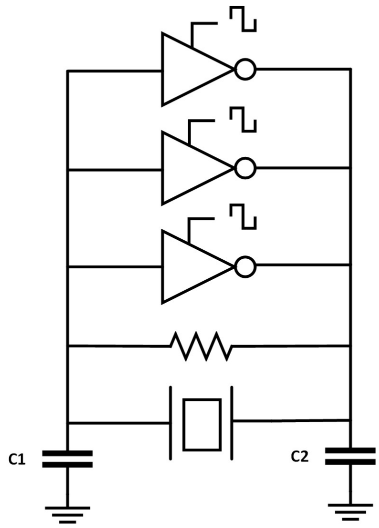

Figure 3.6 : Three parallel inverter used to adjust the transconductance of the oscillator.

As shown in Table 3.2, there are two different capacitor values for each tranconductance value. The smaller capacitor refers to minimum power dissipation for acceptable settling time.

Table 3.2 : Dissipated power and settling time according to load capacitance.

Transconductance	$C_1 = C_2 = C_L$	P_{DC}	Settling Time
15 mS	300 fF	483.8 μW	2.2 μs
15 mS	800 fF	632.1 μW	1 μs
10 mS	300 fF	418.6 μW	2.3 μs
10 mS	600 fF	506.5 μW	1.6 μs
5 mS	300 fF	290.4 μW	16 μs
5 mS	400 fF	320.1 μW	18.5 μs

Figure 3.7 and 3.8 shows the transient characteristic of the oscillation signal. Supply voltage applied at 100ns and oscillation starts to grow until the saturation of the transistors. The more negative resistance, the less settling time.

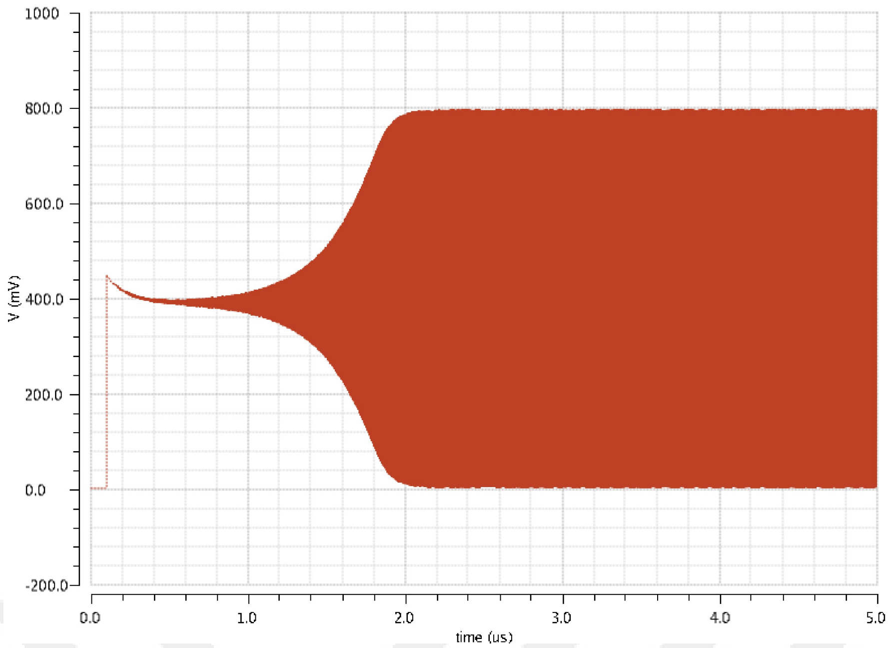

Figure 3.7 : The settling time is approximately 2.2 μs (g_m = 15mS, C_1=C_2=300fF)

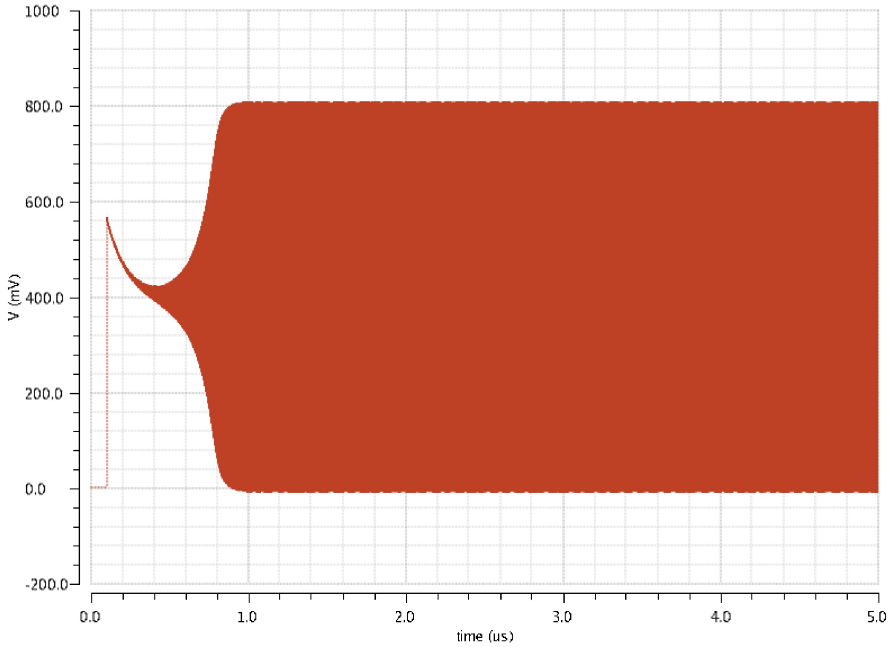

Figure 3.8 : The settling time is approximately 1 μs (g_m = 15mS, C_1=C_2=800fF)

According to the time constant, Equation 3.5, the setting time of the oscillation can be improved by increasing the negative resistance of the circuit. The drawback of the improved setting time is increased power consumption.

$$\tau_{exp} = -\frac{L_m}{Re[Z_C] + R_m} \tag{3.5}$$

The setting time of the oscillator can be calculated from the time constant using Equation 3.6. For L_m=123.5 nH, $R_m = 1.424\Omega$ and $Re[Z_C] = -3.695\Omega$ from Figure 2.11, τ_{exp} is calculated as 54.38 ns. If it is assumed that $V_{initial}$ is 1μ V, the settling time is calculated as $12.9 \cdot \tau_{exp} = 0.7\mu$s.

$$V_{final} = V_{initial} \cdot e^{t/\tau} \tag{3.6}$$

Simulated phase noise performance of the oscillator is shown in Figure 3.9. The noise of the oscillator circuit changes the amplitude and phase of the output signal. However, phase noise dominates the oscillator performance instead of the amplitude fluctuations [29].

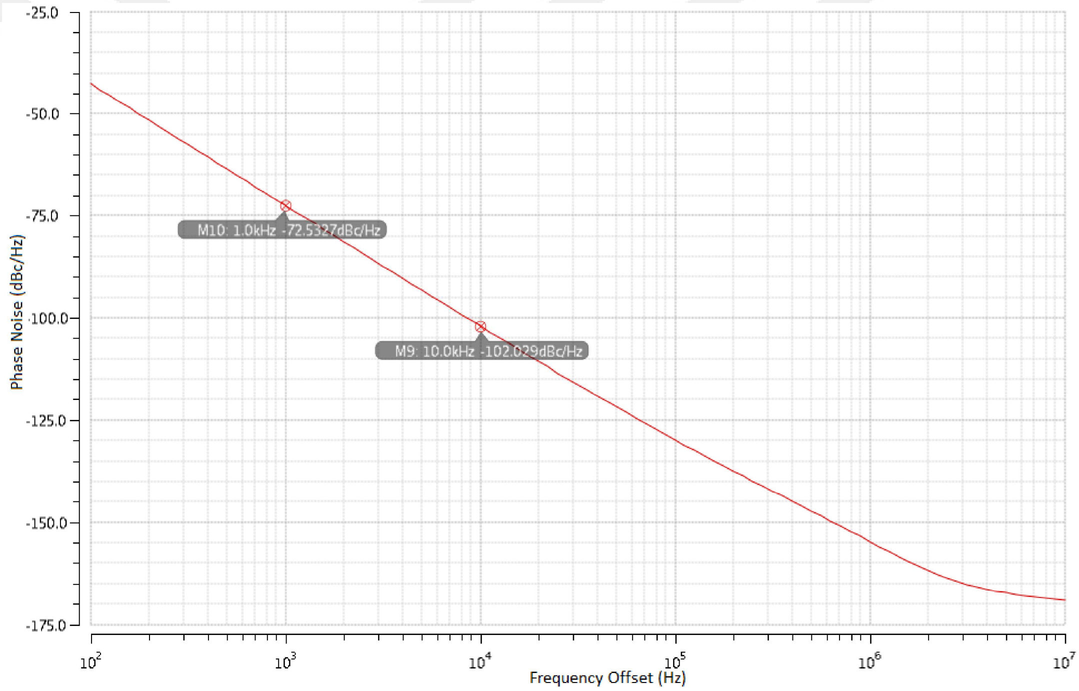

Figure 3.9 : Simulated phase noise of the oscillator.

The phase noise performance of the oscillator is compared with other FBAR oscillators published in literature in Table 3.3.

FBAR resonators are off-chip components and should be connected to the circuit using bondwires. Bondwires are modelled by series inductor and resistor which models the finite quality factor of the inductor. In Figure 3.10, the model of the bondwires is included in the FBAR resonator model. These bondwires add additional series resonance and inductive region. The inductive region comes from the bondwires can cause the parasitic oscillation. The shorter bondwires are more desireable.

Table 3.3 : Phase noise comparison of the FBAR oscillator to previously published work.

Ref.	f_{OSC} (GHz)	Power (μW)	Phase Noise @ 100 kHz Offset
This Work	2.5	506.5	-130 dBc/Hz
[1]	1.5	1020	-133 dBc/Hz
[30]	2.0	25	-121 dBc/Hz
[31]	1.9	300	-120 dBc/Hz
[32]	1.9	89	-120 dBc/Hz

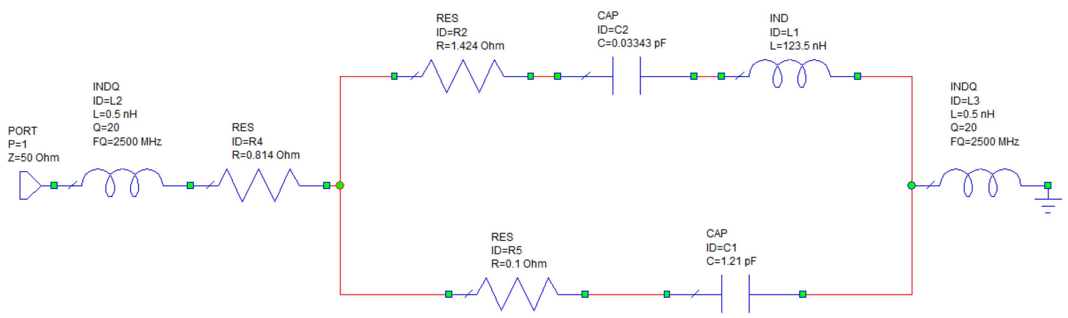

Figure 3.10 : Simulation setup to measure the effect of the bondwires.

Figure 3.11 shows the effects of the bondwires and three different situations ,which are no inductance, 0.5 nH and 1 nH for each bondwire, is performed. It is obvious from the results that bondwires shifts the series resonance frequency to the lower frequencies.

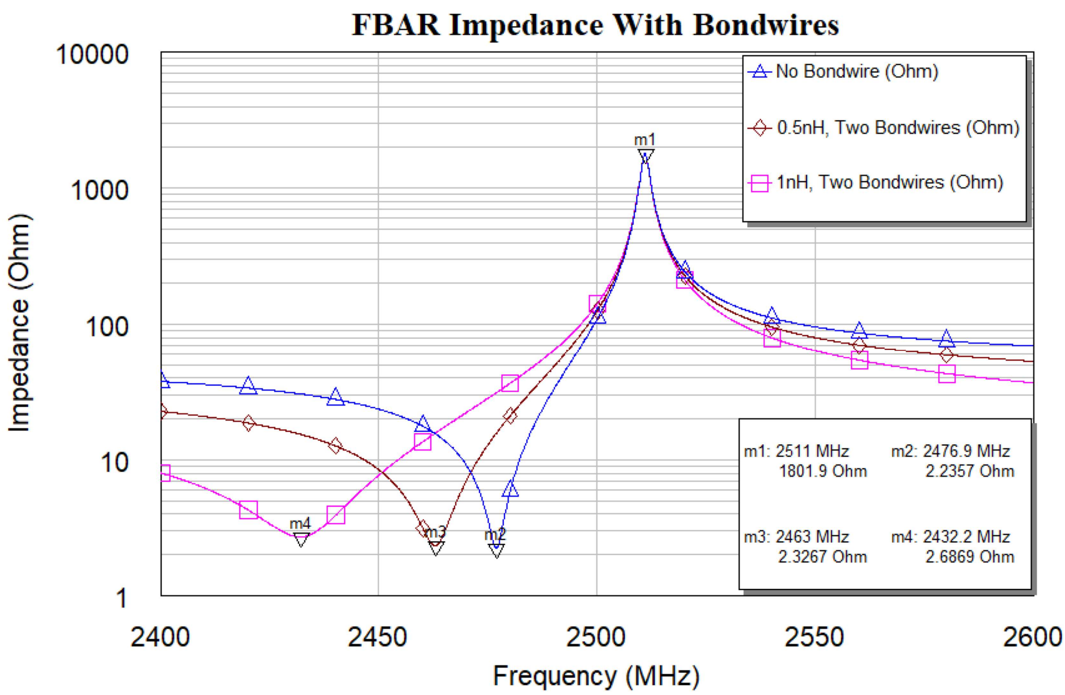

Figure 3.11 : The impedance characteristic of the FBAR resonator.

The most critical effect of the bondwires is the additional inductive region which is shown in Figure 3.12. The oscillator might start the oscillate in this higher frequency region. If the parasitic oscillation exists, load capacitors should be increased to overcome this problem.In this design, switched capacitors are added to input and output of the oscillator. In addition, bond wires should be as small as possible.

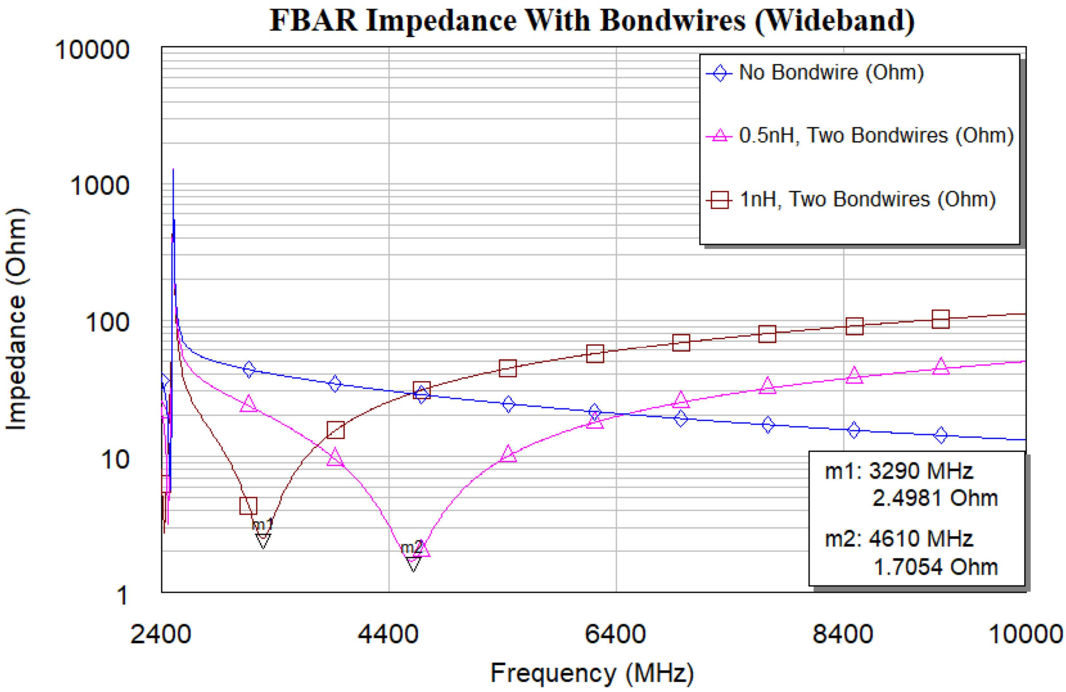

Figure 3.12 : The Wideband impedance characteristic of the FBAR resonator.

3.3 Low Power Amplifier

A Low power amplifier is designed as shown in Figure 3.13. The impedance seen by the transistor through the load is directly affecting the efficiency of the amplifier. However, due to the low quality factors of the on-chip inductors, maximum achievable impedance is limited.

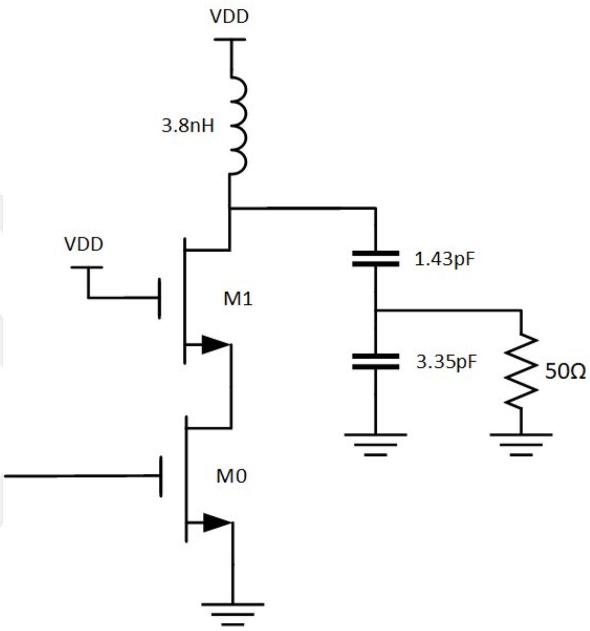

Figure 3.13 : Cascode low power amplifier.

Figure 3.14 shows the input impedance of the designed tapped-capacitor circuit. The matching network is resonating at 2.5 GHz to filter out the harmonics and to get higher impedance at the operating frequency.

To bias the transistor, voltage is applied to the gate terminal via a resistor as shown in Figure 3.15. However, because of the time constant of the gate terminal, the gate voltage cannot follow the bias voltage.

The transient response of the gate voltage is simulated for two different resistor values which are $10k\Omega$ and $100k\Omega$. According to Figure 3.16, the setting of the gate voltage takes more time for higher resistor values.

The gate of the transistor biased at 300mV when input data is logic high. Under this condition, the output power is 30 μW and DC power consumption is 430 μW.

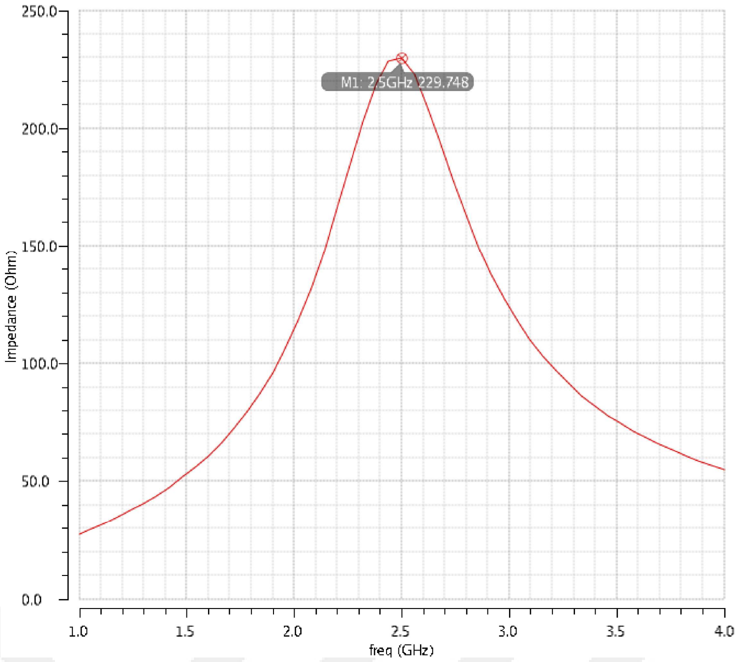

Figure 3.14 : Input impedance of the tapped-capacitor matching network.

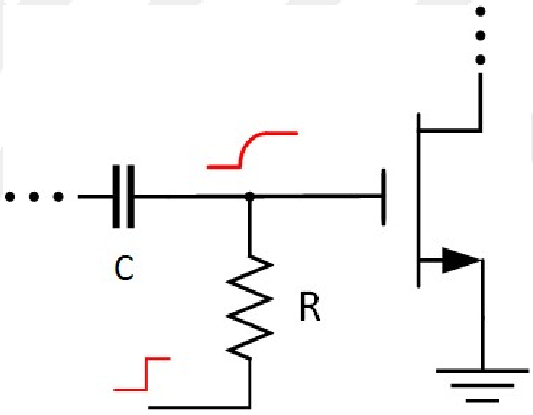

Figure 3.15 : Non-ideal characteristic of the gate biasing due to the time constant.

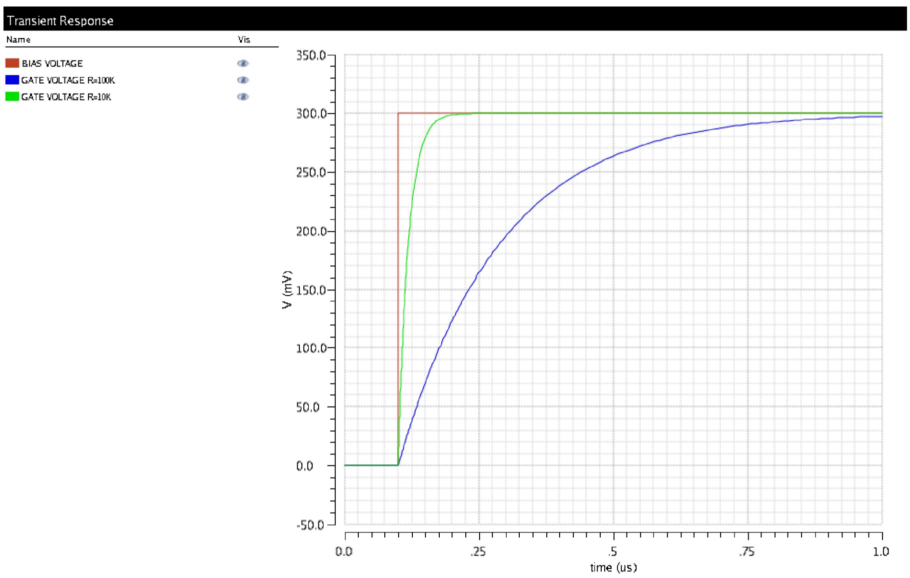

Figure 3.16 : The simulation of the gate voltage for two different resistor values.

Output impedance of the amplifier should be matched to 50 Ω to minimize the output return loss. According to Figure 3.17, the output return loss, S_{22}, is approximately -14 dB.

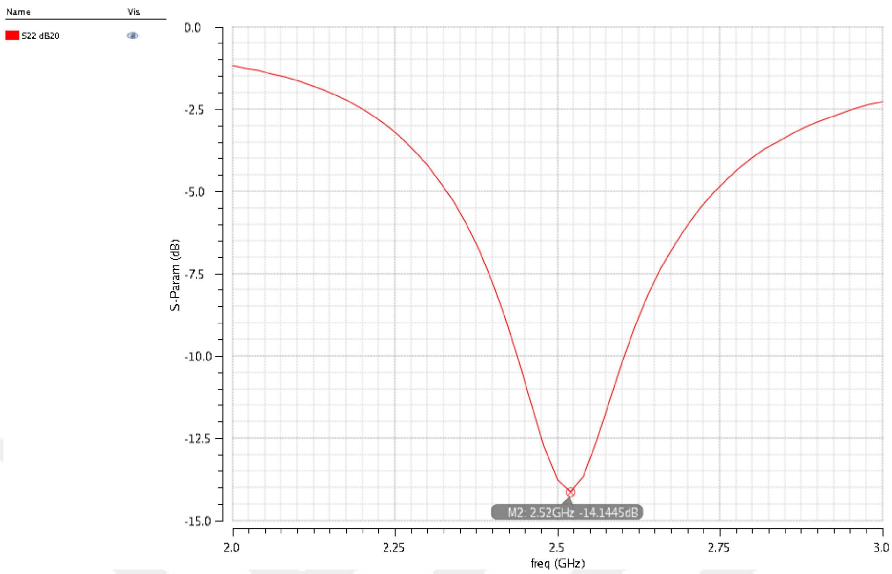

Figure 3.17 : Output return loss of the low power amplifier.

The oscillator is directly connected to the amplifier without any buffer or pre-driver circuit. Therefore, input impedance of the amplifier loads the previous stage. As shown in Figure 3.18, input impedance is high, consequently the oscillator can sustain the oscillation.

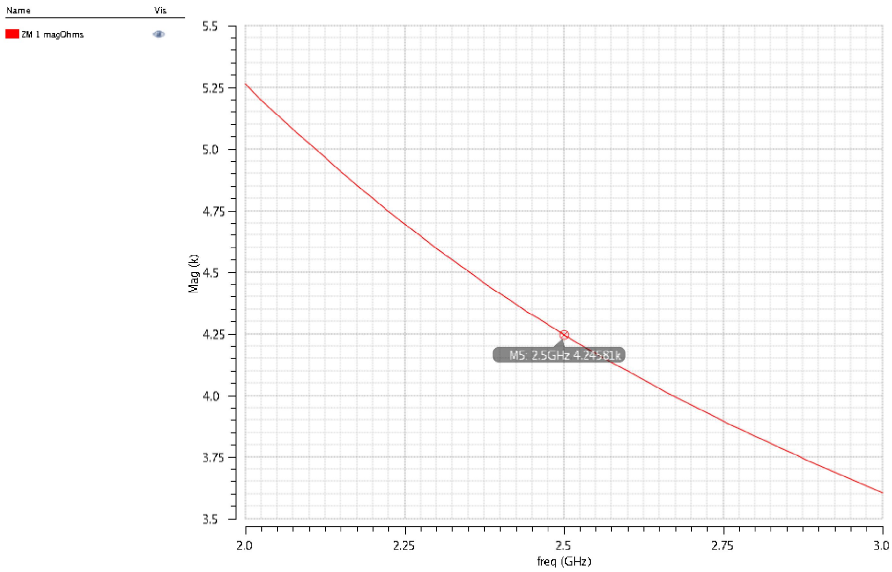

Figure 3.18 : Input impedance of the low power amplifier.

3.4 Digital Radio Controller

The characteristic and purpose of the digital radio controller have been defined in the previous section. The designed circuit according to requirements is shown in Figure 3.19. It should be noted that the voltage of the logic inputs is higher than the output voltage requirement. In addition to bit operations, the digital circuit is used as a level shifter. The supply voltage of the logic gates is 0.8V.

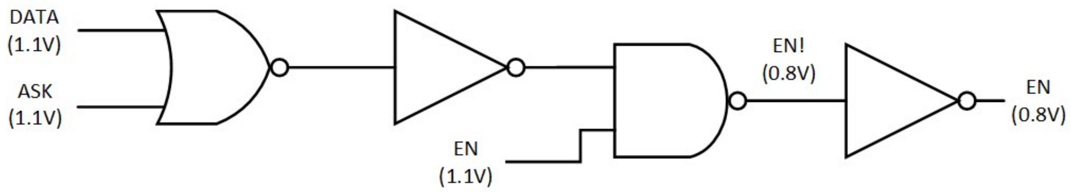

Figure 3.19 : The logic circuit of the digital radio controller.

When the inverter is enabled, either enable bit follows the data signal or fixed to logic high voltage. This behaviour of the circuit is controlled by the ASK input bit. If the OOK modulation is selected (ASK = ’0’), message signal, or oscillator inverters, is enabled or disabled according to the value of the data signal. It is clearly shown that in Figure 3.20, ENABLE signal follows the data signal and the logic level shifted to 0.8V from 1.1V.

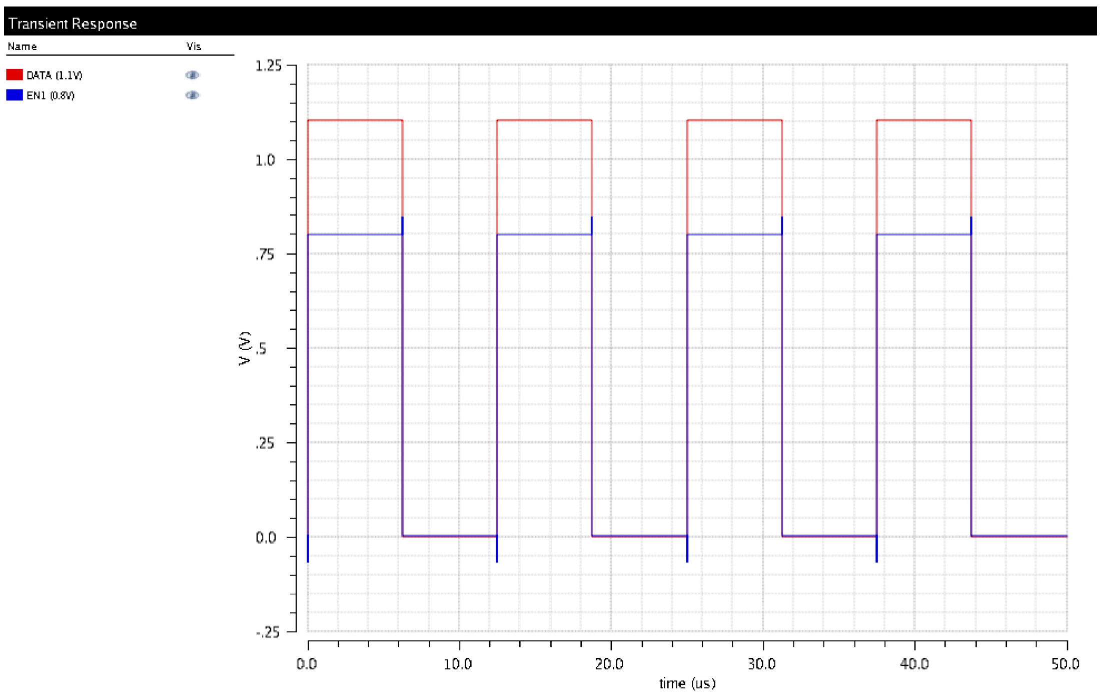

Figure 3.20 : EN1 output of the digital radio controller when ASK is ’0’.

If the ASK modulation is selected (ASK = '1'), the output of the enabled oscillators is constantly logic high. As shown in Figure 3.21, ENABLE signal does not follow the data signal and output is constantly logic high.

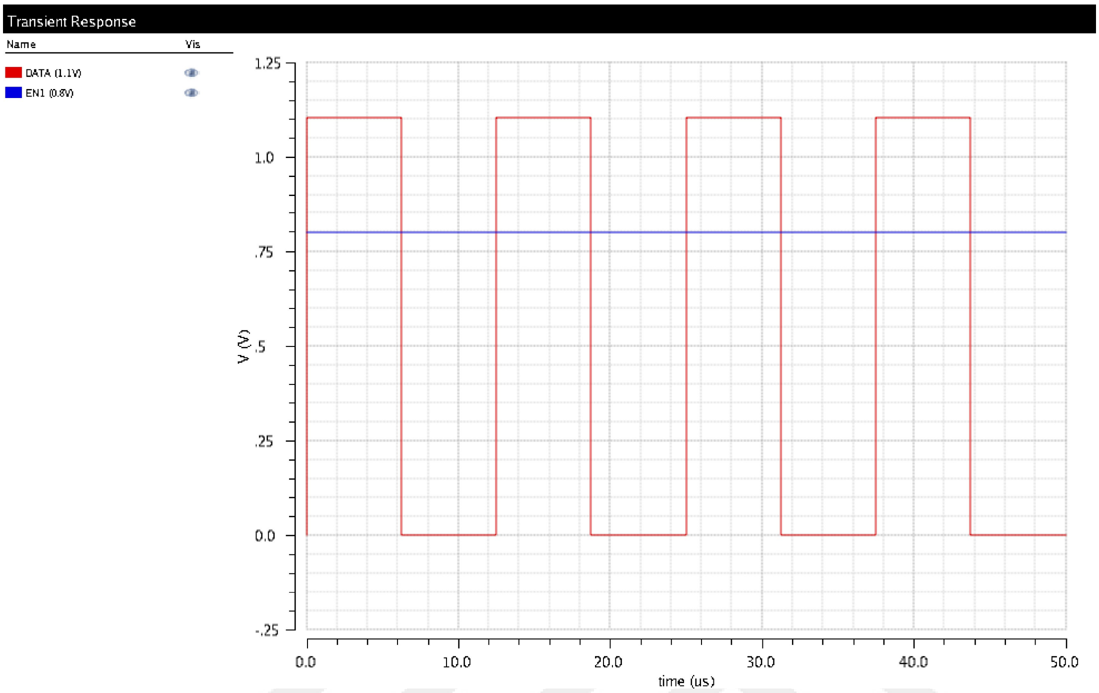

Figure 3.21 : EN1 output of the digital radio controller when ASK is '1'.

3.5 ESD Protection

Electrostatic discharge causes harmful events for the integreted ciruits if ESD protection circuit is not available inside the chip. To overcome this problem, ESD protection circuits should be used. The external interfaces of the circuits are connected to chip pads. The capacitances of the analog pads is so high to RF signals. Therefore, RF pins are connected to pads via designed ESD protection circuit shown in Figure 3.22.

If there is a voltage spike in RF pin with NS mode, NDIO diode operates under forward-biased condition. However, with PD mode, PDIO diode operates under forward-biased condition [33].

Digital pads in the process connected to digital input ports of the circuit. To improve the ESD immunity, an additional circuit is designed. The ESD protection circuit for the digital inputs is shown in Figure 3.23.

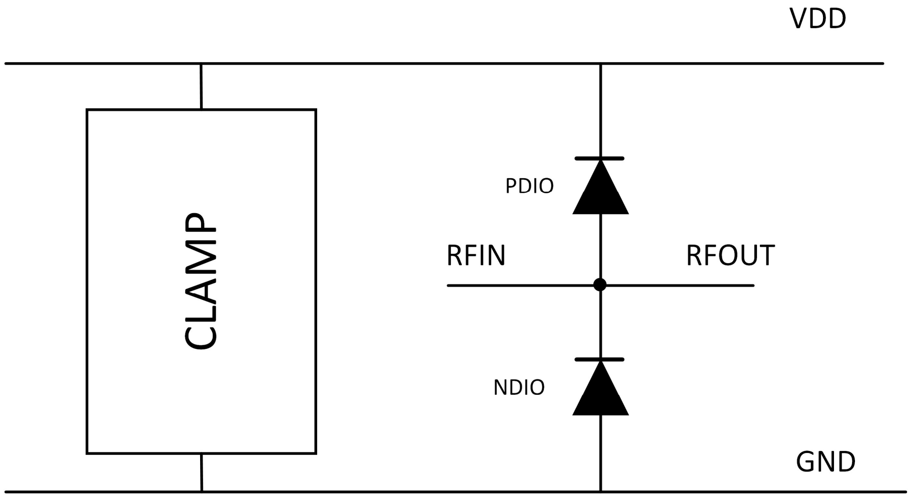

Figure 3.22 : ESD protection circuit for RF inputs and outputs.

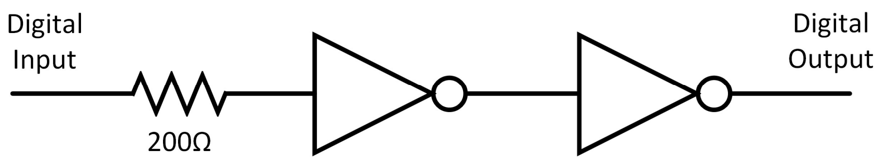

Figure 3.23 : ESD protection circuit for the digital inputs.

4. INTEGRATION OF SUBCIRCUITS

4.1 Transmitter Layouts

Schematic based simulations do not exactly shows the final performance of the circuit even if all electronic components are modeled devices. The main reason for the differences between layout and schematic simulation is the interconnects. The interconnects can be modeled with a series resistor and shunt capacitor. Therefore, the frequency response of the interconnects is similar to the low-pass filters.

Figure 4.1 shows the oscillator layout without load capacitances. Load capacitances are added to the circuit at the last step of the design. Each inverter has two digital input (EN and $\overline{EN}$) connected with metal interconnects colored as yellow and located at the bottom of Figure 4.1.

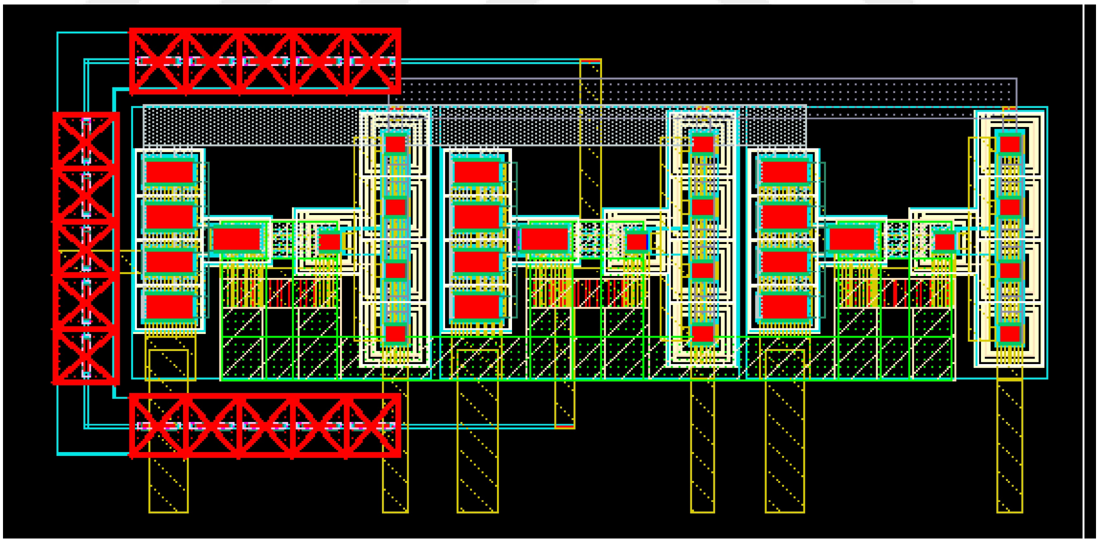

Figure 4.1 : 2.5 GHz Pierce oscillator layout without load capacitances.

As shown in Figure 4.2, the layout of the low power amplifier,the inductor is the most area consuming component.

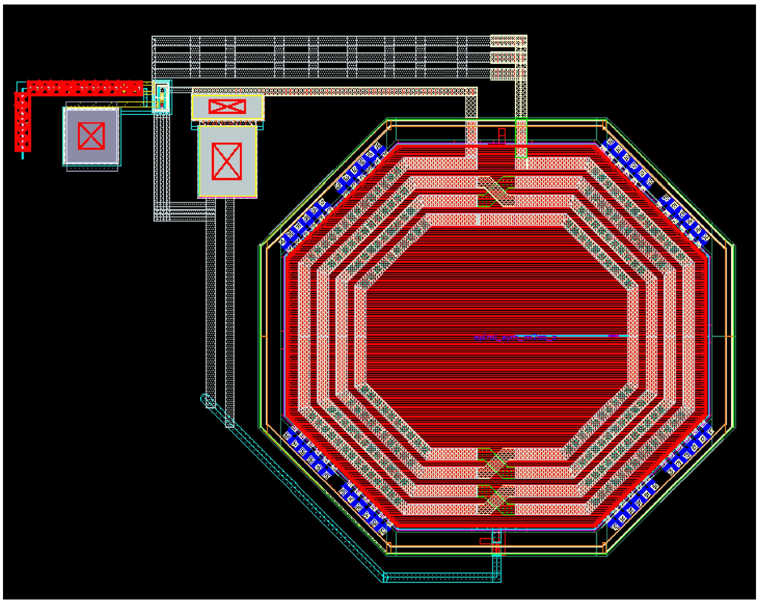

Figure 4.2 : Low power amplifier layout.

The gate terminals of the transistors used at the input logic gates are directly connected to pads. To protect the circuit from ESD events, resistor and buffer circuit is added to the inputs of the logic gates as shown in the right side of Figure 4.3.

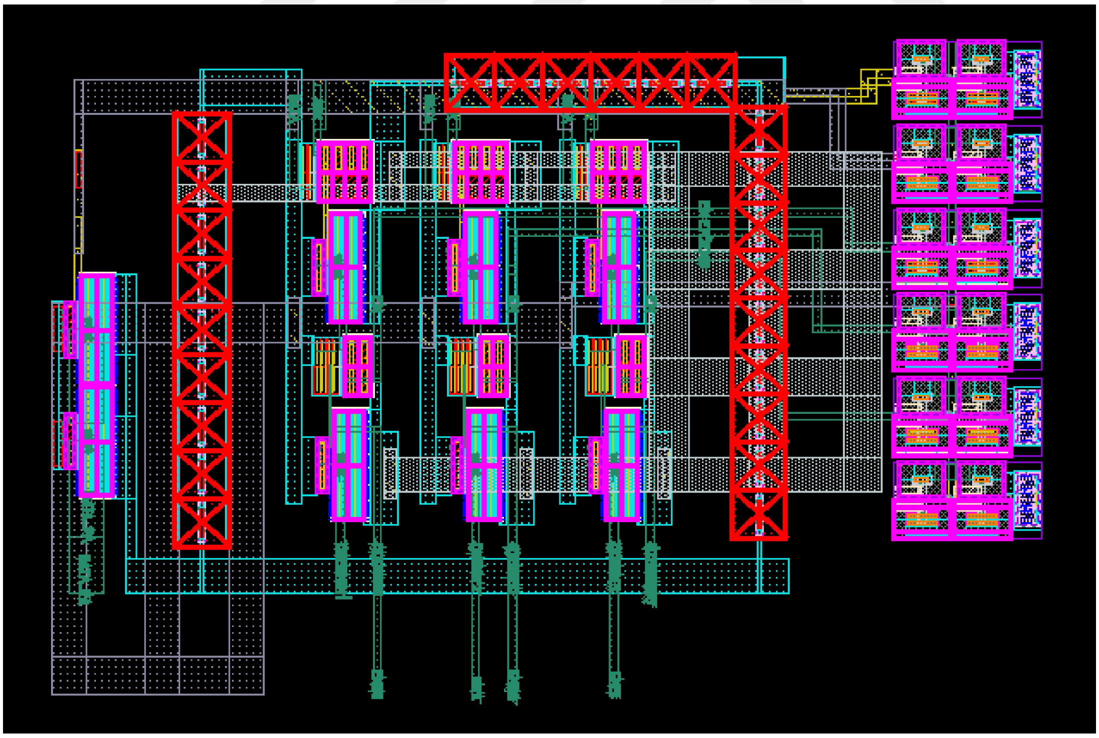

Figure 4.3 : Digital radio controller layout.

In Figure 4.4, all subcircuits and loading capacitors are connected to each other.

The transmitter is located inside the chip and pad connections are performed as shown in Figure 4.5

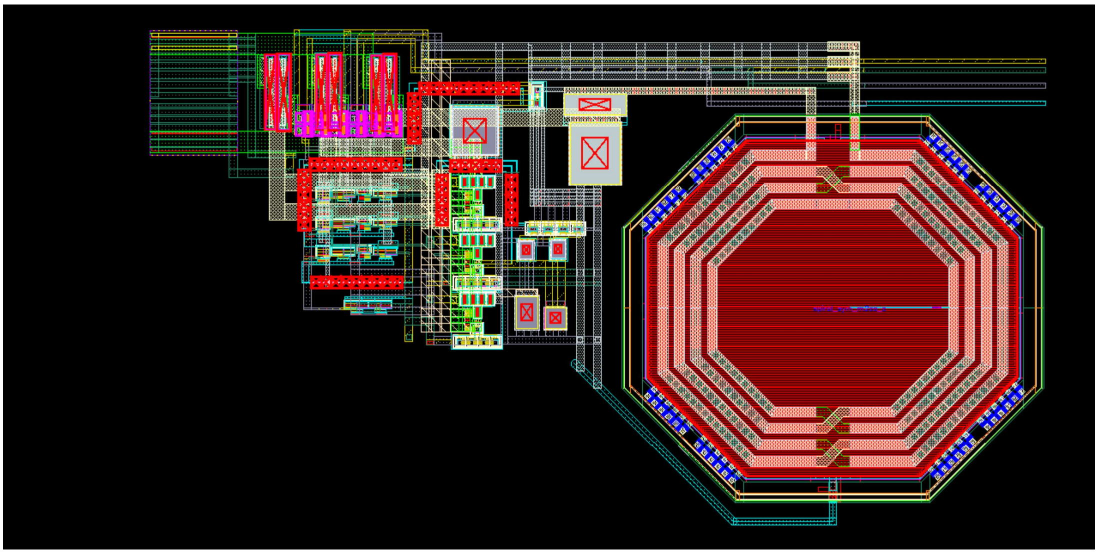

Figure 4.4 : Implantable low power RF transmitter layout.

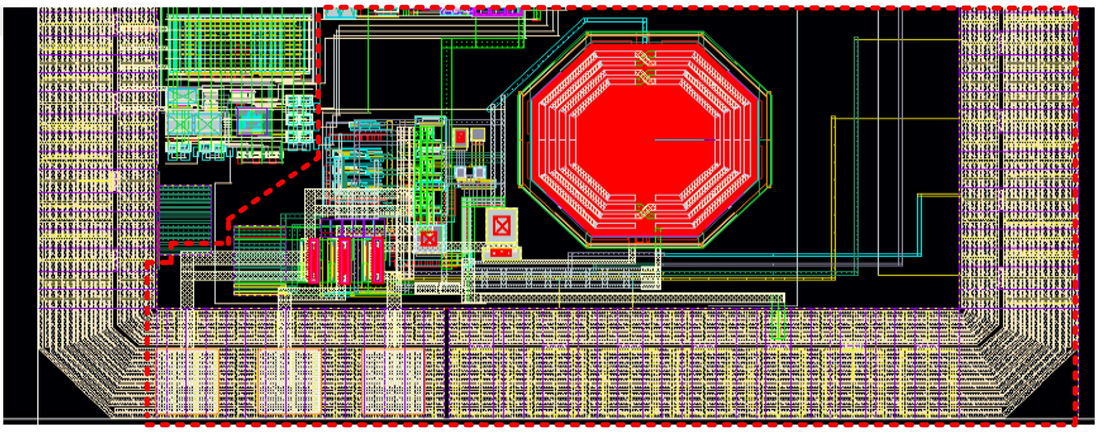

Figure 4.5 : Pad connections of the RF transmitter.

4.2 Transmitter Simulation

The low power RF transmitter is simulated after the integration of all subcircuits. During the final simulations, the transmitter is supplied from an LDO regulator. As shown in Figure 4.6, Supply voltage, VDD, of the circuit is changing with the supply current.

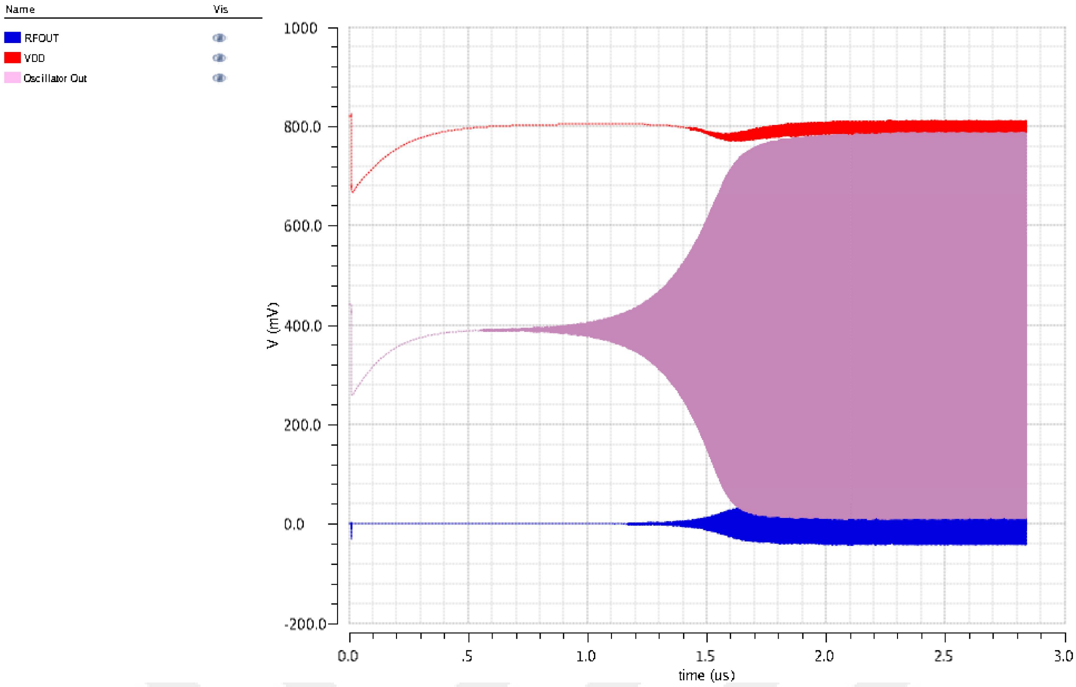

Figure 4.6 : Simulation result of the final transmitter layout (Voltage supplied from the LDO regulator).

Desired values and simulation result are listed in Table 4.1.

Table 4.1 : Desired parameters and simulated results for the implantable RF transmitter.

Parameter	Desired Value	Simulated Value
RF Supply	0.8V	0.8V
Digital Input Voltage	1.1V	1.1V
Carrier Frequency	2.5 GHz	2.5 GHz
RF Output Power	-20 dBm	-18 dBm
Startup Time	4 μs	2 μs
Power Consumption (Max)	< 1mW	900 μW
Power Consumption (Typical)	< 500 μW	450 μW
Off-Chip Components	Only FBAR	Only FBAR
Supported Modulations	OOK, ASK	OOK, ASK
Circuit Size	$0.16 mm^2$	$0.16 mm^2$
Output Return Loss	< -10 dB	-14 dB

The simulated values of the transmitter is compared with the other FBAR based transmitters in Table 4.2.

Table 4.2 : Comparison of the transmitter with other FBAR based transmitters in literature.

Parameter	This Work	[6]	[7]	[8]
CMOS Tech.	40nm	65nm	0.13μm	0.13μm
Carrier Frequency	2.5 GHz	2.4 GHz	1.9 GHz	1.9 GHz
RF Output Power	-18 dBm	-12.5 dBm	-3 dBm	0 dBm
Data Rate	500 kbps	1 Mbps	83 kbps	50 kbps
DC Power (Max.)	900 μW	468 μW	2.2 mW	6mW
DC Power (Typ.)	450 μW	N/A	1.1 mW	3mW
Circuit Size	0.16mm^2	0.324mm^2	0.4mm^2	0.3mm^2

5. CONCLUSIONS

In this thesis, low power RF tranmitter for bioimplants is desinged and simulated. Design steps have been clearly indicated in previous Chapter 2 and Chapter 3. Final simulation results after the integration of all subcircuits are obtained and compared with desired results in Chapter 4. It is clearly seen that designed transmitter is suitable to use for bioimplants. In addition, this work has been compared with other low power transmitters proposed in the literature in Table 4.2. DC power consumption of the simulated transmitter is lower than that of [7] and [8]. From this point of view, limited energy sources of the transmitter is efficiently used to transmit the health data. Circuit size of the transmitter is much lower than that of the other works.

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APPENDICES

APPENDIX A.1 : Negative Resistance vs Load Capacitances
APPENDIX A.2 : Negative Resistance vs Transconductance
APPENDIX A.3 : RF section of the implantable RF transmitter.

APPENDIX A.1

```
clc;clear;

C1=(0:0.1:2)*1e-12;
C2=(0:0.1:2)*1e-12;

[C11,C22] = meshgrid(C1,C2);
R0 = 0.1;
C0 = 1.21e-12;
gm = 10e-3;
fo = 2.5e9;
wo = fo*2*pi

Z1 = 1./(j*wo*C11);
Z2 = 1./(j*wo*C22);
Z3 = R0 + 1./(j*wo*C0);

ZC = (Z1.*Z3 + Z2.*Z3+gm.*Z1.*Z2.*Z3)./(Z1+Z2+Z3+gm.*Z1.*Z2);
figure
surf(C11,C22,real(ZC))
```

APPENDIX A.2

```
clc;clear;

C1=0.5*1e-12;
C2=0.5*1e-12;
gm=(0:1:50)*1e-3;

R0 = 0.1;
C0 = 1.21e-12;

fo = 2.5e9;
wo = fo*2*pi;

Z1 = 1/(j*wo*C1);
Z2 = 1/(j*wo*C2);
Z3 = R0 + 1./(j*wo*C0);

ZC = (Z1*Z3 + Z2*Z3+gm.*Z1*Z2*Z3)./(Z1+Z2+Z3+gm.*Z1*Z2);

figure plot(gm,real(ZC),'-*')
```

APPENDIX A.3

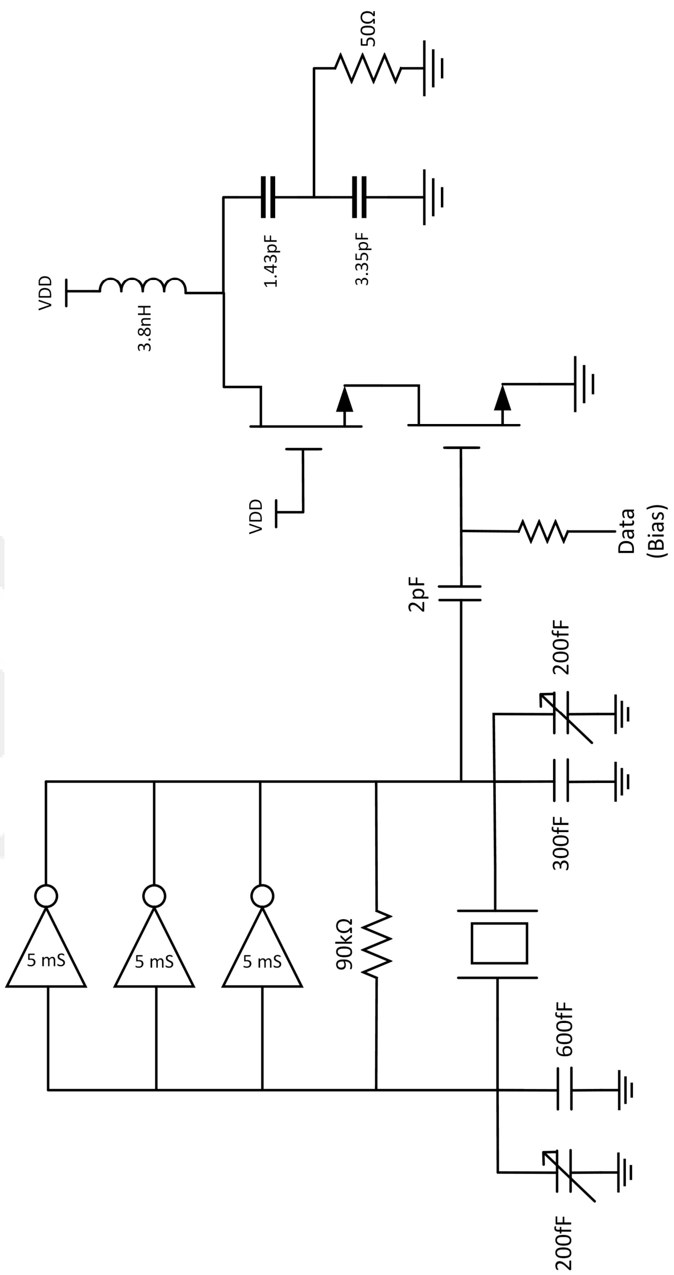

Figure A.1 : RF section of the implantable RF transmitter.

CURRICULUM VITAE

Name Surname: **Kaan KULA**

Place and Date of Birth: **Mustafakemalpaşa/BURSA, 12.03.1993**

E-Mail: **kulakaa@itu.edu.tr**

EDUCATION:

- **B.Sc.:** 2015, Istanbul Technical University, Faculty of Electrical and Electronics Engineering, Electronics and Communication Engineering Department
- **M.Sc.:** 2019, Istanbul Technical University, Department of Electronics and Communications Engineering, Electronics Engineering Programme

PROFESSIONAL EXPERIENCE AND REWARDS:

- 2013 2nd Place, Software Defined Radio Competition, International Microwave Symposium, Seattle – USA
- 2015 1st Place, Software Defined Radio Competition, International Microwave Symposium, Arizona – USA
- 2015 - 2017 ABE Technology, RF Design Engineer, Team Leader
- 2017 - Present Istanbul Technical University, Research Assistant

PUBLICATIONS, PRESENTATIONS AND PATENTS ON THE THESIS:

OTHER PUBLICATIONS, PRESENTATIONS AND PATENTS:

- Ceylan O., Caglar A.,Tugrel, H. B., Cakar, H. O., Kislal, A. O., Kula K., Yagci, H. B., 2016. Small Satellites Rock: A Software-Defined Radio Modem and Ground Station Design for Cube Satellite Communication. *IEEE Microwave Magazine*, 17(3), 26-33.

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