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OUTPHASING CLASS-E POWER AMPLIFIER FOR 5G APPLICATIONS AT SUB- 6 GHz

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ABSTRACT

OUTPHASING CLASS-E POWER AMPLIFIER FOR 5G APPLICATIONS AT SUB 6 GHz

Wireless communication systems, along with semiconductor technologies and signal processing methods, have become increasingly important in our daily and work lives. Especially, 5G applications are leading in this area, as they are on the verge of being globally accepted for their low latency, high capacity, and enhanced data speed. With 5G, faster and larger data transmission is targeted. To achieve these goals, some requirements have emerged.

One of these needs is regarding the performance of power amplifiers, which are one of the units that consume the most current in systems like base stations. The increasing number of base stations targeted with 5G increases the importance of power amplifiers.

In communication systems like 5G, where the bandwidth is higher, power amplifiers with single-stage transistor structures do not perform very well. This is because power amplifiers with single-stage transistor structures have low efficiency when its input power level is decreasing. Amplifiers with complex structures suitable for load modulation can cope with this issue. The outphasing structure provides a good solution to this problem with its ease of implementation. Outphasing power amplifiers are engineered to achieve high efficiency by dividing input signals into multiple phases and processing them separately. By utilizing fast-switching elements, these amplifiers significantly reduce energy losses and deliver high-quality signals with minimal distortion. Commonly employed in contemporary communication and audio systems, outphasing technology focuses on optimizing performance while improving energy efficiency.

In this thesis, firstly, a Class-E type power amplifier that is suitable for load modulations is analyzed and designed. QLI Class-E topology is used for these analyses. Then, outphasing analyses are conducted for 3.5 GHz. As a result of these analyses, the impedance value seen by the amplifiers is calculated to align with the real axis. Based on this calculated impedance, a combiner circuit is designed, along with a matching circuit to optimize the performance of the combiner. Following this design, an appropriate phase difference point is determined for

the output power and efficiency. Once the designed circuit is implemented, it is prepared for measurement and tested in a manner similar to the simulations conducted earlier. This ensures that the performance aligns with the expected results, validating the design's effectiveness in practical applications.

The simulation results indicate that the designed circuit achieves an output power exceeding 43 dBm with 50% efficiency. Furthermore, the simulation reveals that the circuit maintains a 40% efficiency at a 6 dB back-off. These efficiency and output power values are also confirmed with the implemented circuit, demonstrating a strong correlation between the simulation results and the actual performance. Thus, an outphasing amplifier for 3.5 GHz with a discrete transistor is designed and implemented using the QLI Class E structure and analysis.

ÖZET

6 GHz ALTI 5G UYGULAMALARI İÇİN OUTPHASING E SINIFI KUVVETLENDİRİCİSİ

Kablosuz haberleşme sistemleri, yarı iletken teknolojilerinin ve sinyal işleme yöntemleriyle birlikte gelişerek günlük ve iş hayatlarımızda daha da önemli hale geldi. Özellikle 5G uygulamaları bu konuda öncü olup, düşük gecikme süresi, yüksek kapasite ve artırılmış veri hızı sağlaması nedeniyle 5G standartları yakın zamanda dünya çapında kabul edilmek üzeredir. 5G ile birlikte, daha hızlı ve daha fazla miktarda veri iletimi hedeflenmektedir. Bu hedeflere ulaşmak için bazı gereksinimler ortaya çıkmıştır.

Bu ihtiyaçlardan biri kablosuz haberleşme sistemlerinin alt bloklarından güç yükselteçlerinin performansı hakkındadır. Güç yükselteçleri, baz istasyonu gibi sistemlerde bulunan ve sistemlerde en fazla akım tüketen birimlerinden biridir. 5G ile baz istasyonlarının sayısının artmasının hedeflenmesi güç yükselteçlerinin önemini arttırmaktadır.

5G gibi bant genişliğinin daha yüksek olduğu haberleşme sistemlerinde, tek aşamalı transistor yapısına sahip güç yükselteçleri pek başarılı bir performans sergileyememektedir. Bu durumun sebebi, tek aşamalı transistor yapısına sahip kuvvetlendiriciler geri çekilme güç seviyelerinde düşük verimliliğe sahiptir. Yük modülasyonuna uygun olan karmaşık yapılara sahip kuvvetlendiriciler bu sorunla baş edebilmektedir. Outphasing yapısı kolay uygulanabilirliği ile bu soruna iyi bir çözüm sunmaktadır. Outphasing güç yükselteçleri, giriş sinyallerini birden fazla faza ayırarak ve ayrı ayrı işleyerek yüksek verimlilik elde etmek amacıyla tasarlanmıştır. Hızlı anahtarlama elemanları kullanarak, bu amplifikatörler enerji kayıplarını önemli ölçüde azaltır ve minimum distorsiyon ile yüksek kaliteli sinyaller sunar. Modern iletişim ve ses sistemlerinde yaygın olarak kullanılan outphasing teknolojisi, performansı optimize etmeye ve enerji verimliliğini artırmaya odaklanır.

Bu tezde öncelikle yük modülasyonlarına uygun olacak yükten neredeyse bağımsız Sınıf-E tipi kuvvetlendirici analiz edilecek ve tasarlanır. Bu analizlerde QLI Sınıf E topolojisi kullanılır. Daha sonra 3,5 GHz için outphasing analizleri yapılır. Bu analizler sonucunda kuvvetlendiciler tarafından görülen empedans değeri reel eksene hizalanacak şekilde hesaplanır. Hesaplanan bu empedans değerine göre birleştirici devresi tasarlanır ve

birleştirici devresinin performansı optimize etmek için uyumlama devresi tasarlanır. Tasarlanan devre uygulandıktan sonra, ölçüm için hazırlanır ve daha önce yapılan simülasyonlara benzer şekilde test edilir. Bu, performansın beklenen sonuçlarla uyumlu olmasını sağlayarak tasarımın pratik uygulamalardaki etkinliğini doğrular.

Simülasyon sonuçları, tasarlanan devrenin %50 verimlilikle 43 dBm'yi aşan bir çıkış gücüne ulaştığını göstermektedir. Ayrıca, simülasyon devrenin 6 dB geri çekilmede %40 verimlilik sağladığını ortaya koymaktadır. Bu verimlilik ve çıkış gücü değerleri, uygulanan devre ile de doğrulanmakta olup, simülasyon sonuçları ile gerçek performans arasında güçlü bir korelasyon olduğunu göstermektedir. Böylece QLI Sınıf E yapısı ve analizleri kullanılarak ayrık bir transistor ile 3.5 GHz için outphasing kuvvetlendiricisi tasarlanmış ve gerçeklinmiş olur.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

C	Capacitor
CAD	Computer aided design
dB	decibel
dBm	decibel to miliwatt
DUT	Device under test
DVB-T	Digital video broadcasting- terrestrial
EM	Electromagnetic
GaN	Gallium Nitride
GHz	Giga Hertz
GPS	Global positioning system
GSM	Global system for mobile communications
IEEE	Institute of Electric and Electronics Engineers
IC	Integrated circuit
InP	Indium Phosphide
IMN	Input matching network
L	Inductor
LNA	Low noise amplifier
LDMOS	Laterally diffused metal Oxide semiconductor
LTE	Long term evolution
MHz	Mega Hertz
mm	milimeter
nH	nano Henry
OFDM	Orthogonal frequency division multiplexing
OMN	Output matching network
QLI	Quasi load insensitive
PA	Power amplifier
PAPR	Peak to average power ratio
PCB	Printed circuit board
pF	pico Farad
PAE	Power added efficiency
RADAR	Radio detecting and ranging

RF	Radio frequency
S-Parameters	Scattering parameters
ZVDS	Zero voltage derivative switching
ZVS	Zero voltage switching
5G	5th Generation
°	degree
Ω	Ohm
Θ	Theta
Φ	Phi
Ƞ	Efficiency
q	Resonance factor

1. INTRODUCTION

Wireless communication systems and subsystems have played a vital role in people's lives for an extended period. With the advancements that have occurred since the early 20th century, they have become a significant part of the communication networks, and this evolution continues. These systems have a considerable impact on people's daily and business activities, offering numerous benefits. There is a growing need and desire among many individuals to utilize these systems [1]. The increasing usage necessitates technological advancements to provide a faster and more reliable communication infrastructure for users. 5G applications are at the forefront of this progress, striving to offer low latency, high capacity, and increased data rates [2] [3] and their standards are accepted worldwide. Various telecommunication companies are actively engaged in research and development in this field [4].

Wireless communication enables the transfer of information between two independent points that do not have a physical connection. The information transfer between two points can be carried out with radio frequency (RF) energy [5]. This method is used in many military and commercial applications [6]. Cellular telephones, Radar applications, and GPS are some of them. A receiver and a transmitter are required to implement such applications. Figure 1.1 represents the basic block diagram of the two circuits.

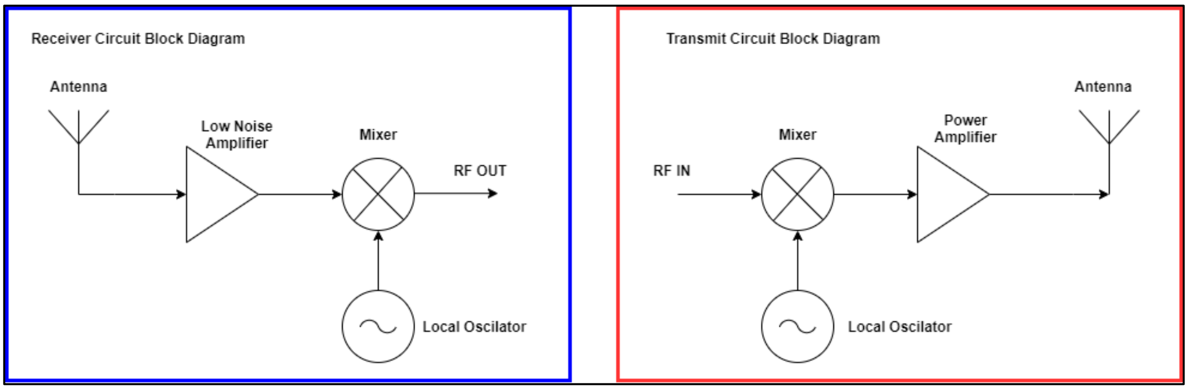

Figure 1.1 Transmit & receiver circuits basic block diagram

The blue box in Figure 1.1 represents a receiver. The low-power RF signal received from the antenna is amplified by the LNA, and then the signal is transmitted adjusted using it to the required frequency with the mixer. The red box reprensts a transmitter. The low frequency (such as kHz) of the low-power RF signal is first adjusted with the mixer. Then it is amplified by the PA. In this way, the power of the signal is increased to a high level and allowing for the transmission of the signal via the antenna. These circuits can be located in the same block and can be used in conjunction with each other. One common points of these two circuits is the amplification of the signal. The signal power that is received or intended to be transmitted is low. Both the physical resistance of the circuit and the air resistance cause attenuation in the signal [6]. The signal power must be above a certain threshold for the information to be received or transmitted correctly [7]. This highlights the importance of signal amplification.

PAs are circuits for amplifying using DC power to provide maximum power for output signal power [8] [9] [10]. The output power level is one of the important parameters of RF systems. This has made PAs a critical subsystem of RF systems and has given importance to research. Especially between the years 2000-2010, the number of PA research studies increased, and an average of 1,400 studies have been published each year in the last 10 years in IEEE Xplore digital library [10]. It is seen in Figure 1.2.

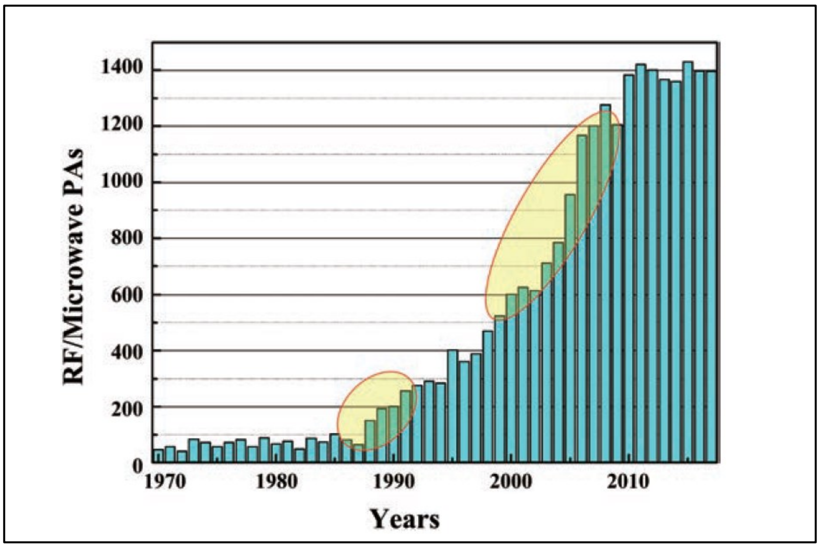

Figure 1.2 The statistics of the number of papers on RF/microwave PA published in the IEEE Xplore Digital Library [10]

Market research indicates this situation. Figure 1.3 is one of the studies about the PA market.

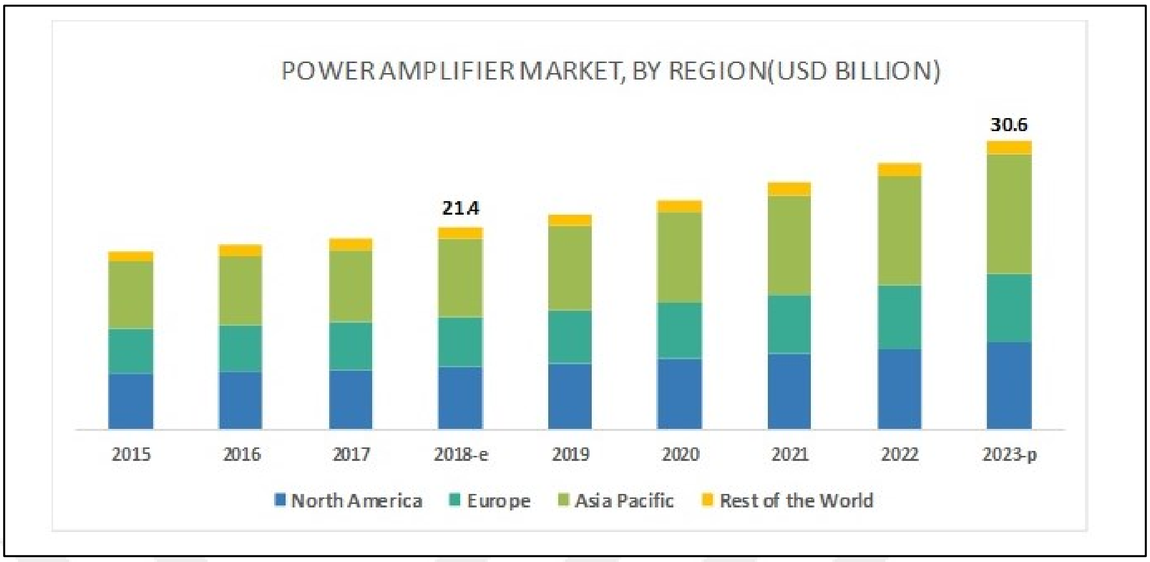

Figure 1.3 Power amplifier market resarch [11]

Early studies often focused on transistor performance [12]. PA classes emerged in the mid-1970s and research on these subjects has continued to the present day [13]. However, signal characteristics have become important with the development of analog and digital wireless communication systems. Increasing signal bandwidth and advancements in modulation techniques, basic PA circuits have struggled to keep pace with these advancements [8]. This is why more complex topologies have become popular. Doherty [14] and Outphasing [15] PA structures are some of them. With these topologies, efforts are made to compensate for the weaknesses that the bandwidth brings in the PA parameters.

Single-stage PAs are suitable for amplifying for a signal at a fixed power level [16] [17]. This limitation arises because the power level reduction of the input signal greatly reduces the efficiency of single stage PAs. Signals used in communication systems such as 5G and LTE have a high peak-to-average power ratio (PAPR) which is defined as the ratio of peak power to the average power of a signal. Figure 1.4 is an example of the modulated signal for a GSM application. As observed in the figure, the power level of the modulated signal varies depending on the frequency. The decrease in efficiency can be solved with an outphasing structure [18]. Consequently, studies on outphasing structures continue.

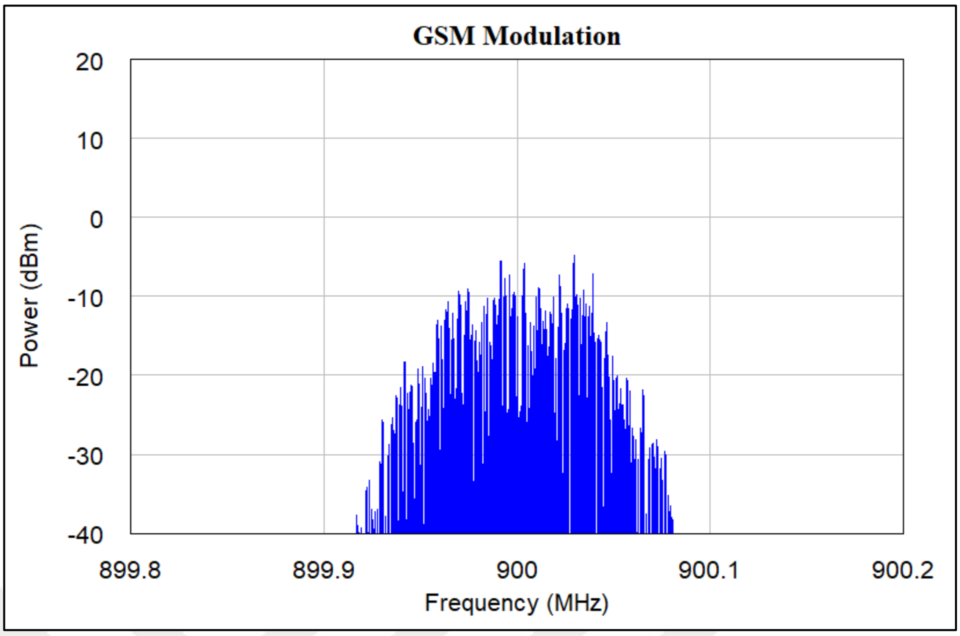

Figure 1.4 Modulated signal for GSM application

There are both analyses [19] [20] and implementation studies on outphasing. [19] presents streamlined approach for analyzing and designing outphasing transmitters that utilize Class-E power amplifiers to enhance efficiency and performance and an overview of load modulation as a technique to enhance the efficiency of RF power amplifiers is explained in [20]. There are implementations with IC [21] [22] [23] and discrete transistors [24] [25] [26] [27] in various frequency bands and various output powers.

In [24], a 43 dBm output power amplifier circuit operating between 1.7-2.2 GHz is mentioned. In this study, transistors are biased as Class-E and the back-off value of the circuit is 6 dB. In [25], an outphasing amplifier implementation for particle accelerators is shown. The class of transistors of this study is Class-F.

The factors limiting the bandwidth of an outphasing amplifier structure which provides 38 dBm output between 3.1-3.7 GHz is examined and analyzed in [26]. At [27], the behavior of the outphasing structure, which gives 44.6 dBm output power at 900 MHz is examined in different classes and the effects of harmonic termination are examined by extracting load pull curves.

In [28], the classical outphasing approach is applied between 2.4-2.8 GHz. The varactors are used in the combiner network for adjustment of the phase. The dual band outphasing amplifier is implemented in [29]. The circuit has a 6 dB back-off and 44 dBm output power at 2.6 and 3.5 GHz. Another dual-band amplifier circuit is mentioned at [30]. The implemented amplifier circuit has 43 dBm output at 1.6 and 2.2 GHz. In [31], analysis and studies about increasing the back-off value are explained. Unlike traditional transistor classes, the QLI Class-E is used in [32]. This structure is applied to the Doherty structure and a 3.8 GHz amplifier is designed.

Different classes of transistor are used in these studies. A summary of these studies is shown as Table 1. As seen in the table there are many studies different classes and different frequency bands. If the output power column of the table is examined, it can be observed that the output power is between 43-45 dBm and most of studies have 6 and 7 dB back-off value.

Table 1.1 Summary of reference studies

Reference No	**Frequency Range [GHz]**	**Output Power [dBm]**	**Class of Transistor**	**Back-off (dB)**
24	1.7-2.2	43	Class E	6
25	0.65	53	Class F	-
26	3.1-3.7	43	-	7
27	0.9	44.6	Class J	7
28	2.4-2.8	44	Class AB	6
29	2.6 and 3.5 GHz	44.3	Class B	6
30	1.6 and 2.2 GHz	43.2	-	6
31	2.6 GHz	45.2	Class B	12

Apart from the development of topologies, the development of transistor technology also affected the development of the PA. The first studies were done with a vacuum tube [10]. After the transistor was developed by Bell Laboratories in 1947, PAs began to be realized using transistors [16]. This has affected the technology of the transistor material. Many types of materials have been developed, and transistors have been produced using these materials. LDMOS, GaN, and InP are some of them. These materials have different characteristics from each other. These characteristics determine the maximum operating frequency and output power at which they can be used [33]. Figure 1.5 shows which material can used up to how many GHz and how many watts of output power it can give. It is seen that GaN HEMT material belongs to a very wide spectrum in terms of frequency and power.

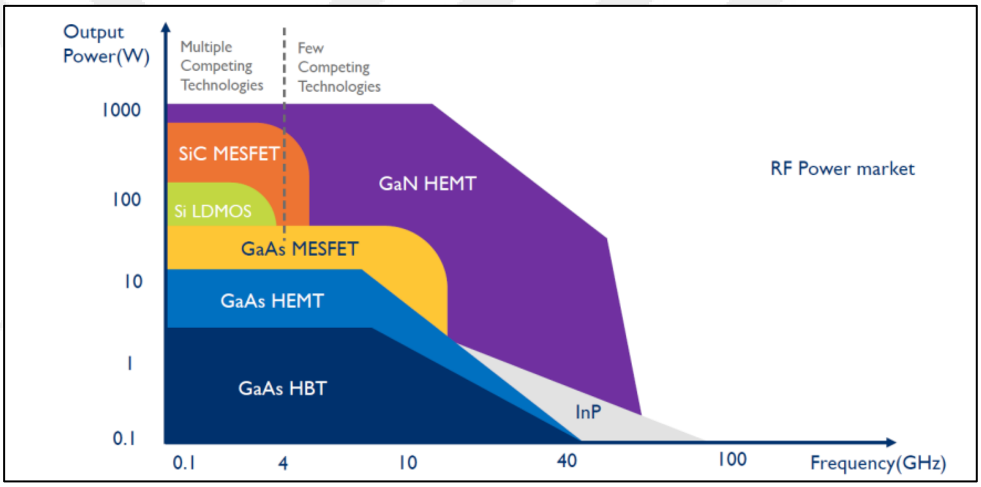

Figure 1.5 Output power and frequency regions for different semiconductor technologies demonstrating [34]

1.1. MOTIVATION

The development of wireless communication day by day and increasing in signal bandwidth affect PA performance. Complex modulated signals are desired to be transmitted both efficiently and linearly. However, these objectives are challenging for high-power active devices because these devices operate in the nonlinear region [35]. Single-stage PAs cannot be used with modulated signals because of the low efficiency at back-off power levels. Therefore, more complex structures are used. With a literature review, an outphasing power amplifier can handle linearity and efficiency at the same time. High bandwidth signals are amplified to the desired power with an outphasing structure. An outphasing power amplifier can handle linearity and efficiency at the same time. By driving two identical amplifier circuits with phase differences, the appropriate load is brought to the modulation point. Output power and efficiency can be controlled with phase. These studies are carried out using conventional different classes of transistors. Apart from traditional methods, the QLI Class-E structure has proven to be suitable for load modulated amplifiers and has become an alternative. However, the studies about this structure are with IC level transistor. It has been observed that there are no studies with using discrete transistor. It is aimed to design a discrete transistor amplifier circuit with QLI Class E structure, combine the amplifier circuit as plural and control the output power of this combined circuit with phase.

1.2. RESEARCH GOALS

This thesis is dedicated to the design and analysis of an outphasing power amplifier utilizing the QLI Class-E topology, which is intended to meet the critical demands for high efficiency and linearity in power amplifiers. The amplifier is designed to operate within the 3.3-3.8 GHz frequency band, which aligns with the sub-6 GHz range required for modern 5G communication systems. This frequency range is vital for 5G networks as it balances both coverage and capacity, ensuring robust communication links.

The study primarily focuses on implementing the QLI Class-E topology in outphasing amplifier analysis to enhance efficiency while maintaining linearity, two essential parameters for effective power amplification in wireless communications. Through this research, an outphasing amplifier circuit is designed, and its performance is meticulously controlled by adjusting phase differences between branches, allowing fine-tuning of output characteristics. Additionally, the study progresses beyond theoretical analysis to the practical production of the designed amplifier, followed by comprehensive measurements to validate its performance.

By exploring this topology and employing it in an outphasing configuration, this research contributes to the ongoing development of advanced amplifiers that meet the stringent demands of emerging wireless technologies.

1.3. THESIS ORGANIZATION

In this thesis, PAs are explained first. After explaining the effects of transistor technology on PA performances, a comparison is made between LDMOS and GaN transistors. PAs classes are described basically. The advantages and disadvantages of the different classes are explained. The Class-E structure is examined in detail and information are given about a quasi-load insensitive (QSI) Class-E.

PAs performance parameters in microwave applications are discussed. After these definitions have been expressed, the PA topologies are shown as single-ended and outphasing. The advantages and disadvantages of these structures are discussed. PAs performance parameters in microwave applications are discussed.

Design work with the selected transistor CG2H40010F is explained. Firstly, analyses are performed with the transistor for QLI Class-E structure. With these analyses, the appropriate impedance for output power and efficiency is determined and the amplifier design is made. The target value is achieved by optimizing the designed circuit. Then the combiner circuit analysis which is a part of the outphasing amplifiers is performed. With the analysis performed, a combiner circuit is designed with the appropriate impedance value. A matching circuit is designed from the impedance of the combiner circuit to 50 ohms.

With the designed combiner circuit, amplifier designs with identical structure Q Class-E structure are combined. Outphasing analyses are performed and the effect of the phase differences change are observed. Outphing simulations are repeated by performing EM analysis of the combiner and matching circuits on the output side. PCB design of the simulated design is performed. The PCB designed circuit is implemented in a lab environment and measurements are taken with the appropriate test setup. In the conclusion section, the studies conducted are summarized, the results are shown, and future studies are mentioned.

2. POWER AMPLIFIER

Amplifiers are one of the circuits of electronic devices. There are many types of amplifiers. LNA, operational amplifier and PA are some of them. PAs are usually the final stage of transmitter structures. With these circuits, the power of the signal to be transmitted is determined. In early 1900's, spark and arc techniques were used to generate RF power [16]. Between 1920 and 1970, vacuum tube technology was used [10] After the discovery of the discrete transistor, RF power was generated by transistor amplifiers [16] and is still used today. Transistor is shown left in Figure 2.1 and vacuum tube is located on the right side.

PAs also determine the linearity of these structures. Determining these parameters shows the importance of the PAs in the transmitter and it also affects the structures thermally, because PAs are the blocks that consume the most power of transmitter structures.

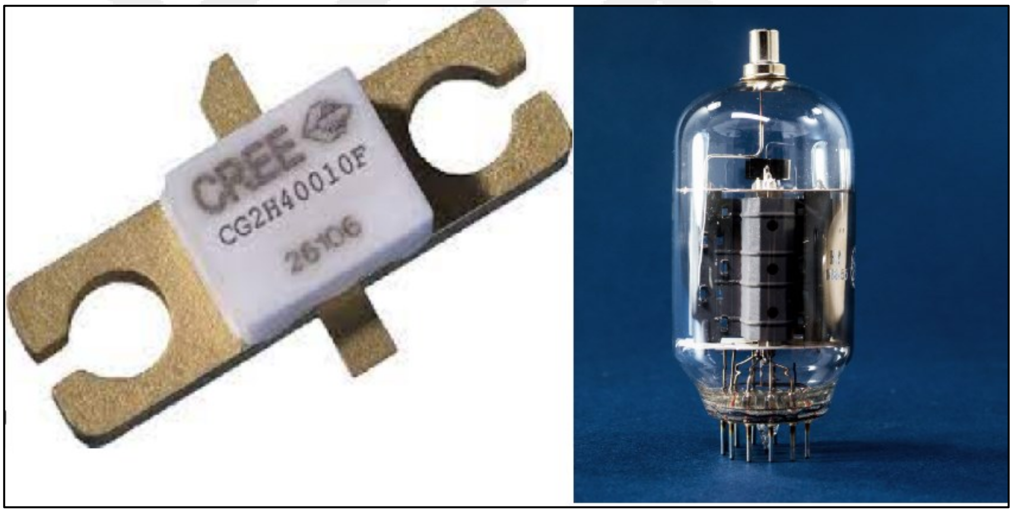

Figure 2.1 Transitor and vacuum tube

Also, the applications like RADAR or base station that they are used increase the importance of PAs. These applications continue to be updated and are developing day by day and have different requirements. RADAR systems operate with narrow band signals, systems such as base station operate with wideband signals. The output power, efficiency and linearity requirements of these systems are also different. The material of the transistor to be used, the working principle of the transistor or the bandwidth of the signal to be transmitted determine the performance parameters of a power amplifier. Due to these factors, the designing of PA consists of many stages. The first of these stages is to select the appropriate transistor according to the output power and frequency. The working principle effects the efficiency and linearity. The bandwidth of the amplified signal is effective in the topology of the amplifier circuit.

2.1. METARIALS OF TRANSISTORS

A power amplifier is an active electronic circuit. The fundamental component of the solid-state power amplifier is the transistor. Material technology of transistors is also spread over a very wide area. This technology whose infrastructure is based on semiconductors is developing day by day.

The characteristic features of the transistor determine many parameters of the power amplifier. Frequency range, outpower, and efficiency are some of them. Therefore, transistor material is selected according to the application to be used. LDMOS, GaN HEMT, GaAs HEMT, and InP are a few examples. With the frequency band they cover and the output power they can provide, GaN and LDMOS technologies are quite suitable for microwaves [36]. However, GaN transistor has preceded LDMOS in recent years. One of the main reasons for this is that GaN-based transistors are suitable for more efficient applications [37]. According to Table 2, GaN is superior to LDMOS and preferred, although more expensive.

Table 2.1 LDMOS and GaN comparison

	LDMOS	GaN
Maximum Frequency	About 20 GHz	About 30 GHz
Power Density	2 W/mm	10 W/mm
Efficiency at P1dB	60%	70%
Breakdown Voltage	Lower	Higher
Maximum RF Power	1.5 kW	1 kW
Price	Lower	Higher

2.2. CLASSES OF POWER AMPLIFIERS

One of the factors affecting the parameters of power amplifiers is the working principle of the transistor. They are generally classified to it as linear and switched mode [38]. Also, they separated into classes. Table 3 shows the linear and switch mode headings that indicate the classes below.

Table 3.1 Classes of PA

Linear Mode	Switched Mode
Class A	Class D
Class AB	Class E
Class B	Class F
Class C	

Linearity and efficiency are goals that separate these classes from each other. Linearity can be defined as the function between the input signal and the output signal being a constant number. As the name suggests, linear PAs are more linear than switched PAs. Linearity is necessary and important in modulated signal amplification. However, switched PAs are more efficient than linear mode PAs. Efficiency can be shown as 2.1. P_L presents the power which is consumed by load and the power consumed is represented by P_{DC} These situations reveal the classification according to need. The classes of PA are determined by the bias point of the transistor and load impedance [35].

$$\eta = \frac{P_L}{P_{DC}} \tag{2.1}$$

2.2.1. Linear Mode Power Amplifiers

Relation between input and output signal waveform is a linear or almost linear in linear mode PAs. The classification of these amplifiers among themselves is shown in Table 3. They have different linearity and efficiency. The difference of these values is revealed by the transistor bias point. If the transistor biased at middle of load-line, this is a Class-A PA. In this way, amplifier behaves quite linear. However, this leads to inefficiency. In Class-B, transistor bias point is set to threshold voltage of transistor. In this case, efficiency increases but only half cycle of input signal can be amplified. This shows that linearity is decreasing. The transistor in Class-AB PAs is biased in the middle with respect to Class-A and Class-B so, it exhibits a middle behaviour relative to them. Class C PAs are biased behind the threshold voltage and operate very efficiently but the linearity of signal is so low. Figure 2.2 shows the bias point of linear mode PAs.

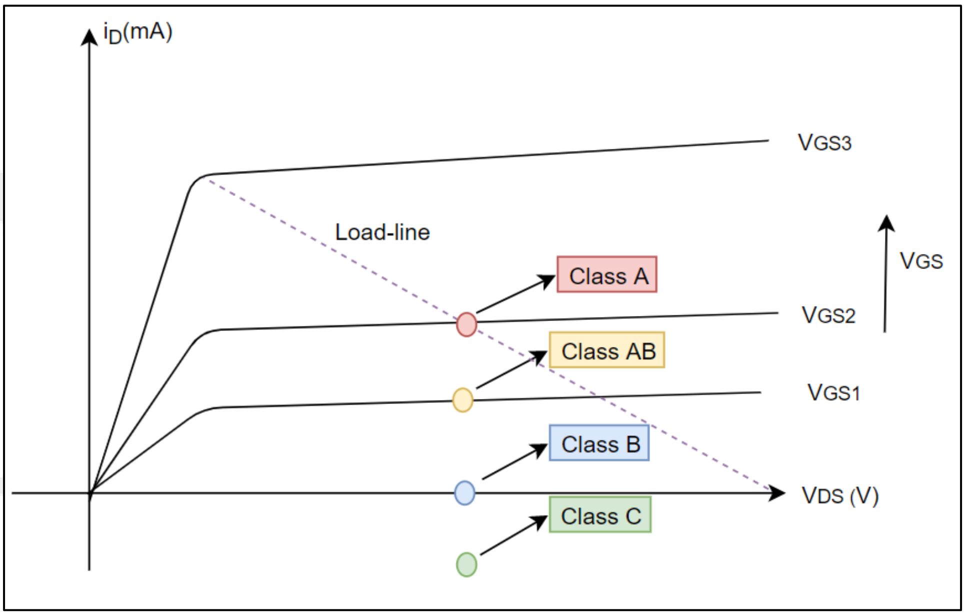

Figure 2.2 Bias points of linear mode PAs

If the transistors are biased according to Figure 2.2 the transistor current waveforms will be as in Figure 2.3. As long as the transistor is not flowing current, the signal will not be amplified, and this will break the linearity.

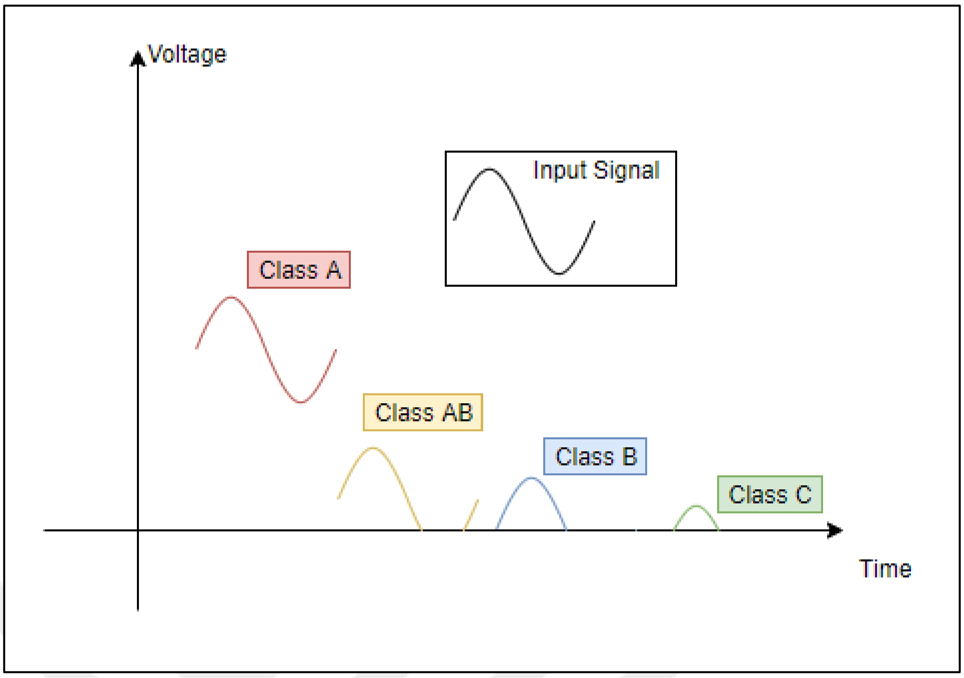

Figure 2.3 Voltage waveform of linear mode PAs

2.2.2. Switched Mode Power Amplifier

As mentioned in the previous section, efficiency is an important requirement of PAs. The main reason for this requirement is the PAs are the block that consumes the most current in transmit blocks [39]. There are many different studies on this topic [9]. Studies at the transistor level have created a high-efficiency class. These classes of PAs are called switching mode PAs. The main purpose of these PAs is to reduce power consumption [38]. In an ideal switch, current flows, and the switch is short-circuited when the switch is 'ON' state. When the switch is 'OFF' state, the current does not flow, and the switch is open-circuited. Figure 2.4 represents the voltage and current waveform for ideal switched mode PAs.

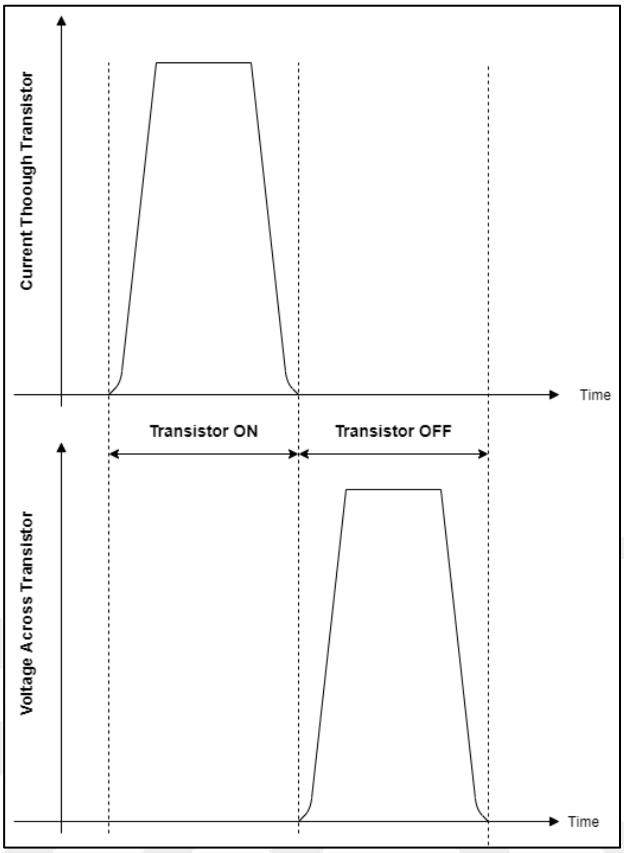

Figure 2.4 Ideal switching mode PAs voltage and current waveform

By not intersecting current and voltage in time, power consumption is reduced to zero and 100% efficiency is produced but this value cannot be reached due to parasitic effects and transistors not being ideal [38]

Class D and Class F are some of the switched-mode PAs. Class D PAs consist of two or more transistors. The square signal formed at the drain is transmitted to the load by filtering at the fundamental frequency [40]. In Class F PAs, the output signal waveform is shaped by harmonic filters, the current waveform approximates the half sine, and the voltage waveform approximates the square signal [38].

Class -E mode amplification is suitable for RF application [38]. Studies about that started in 1975 [41]. In this structure, the transistor is modeled as a switch and the load circuit includes a parallel capacitance and a series inductor. Figure 2.5 represents the basic circuit diagram of Class E.

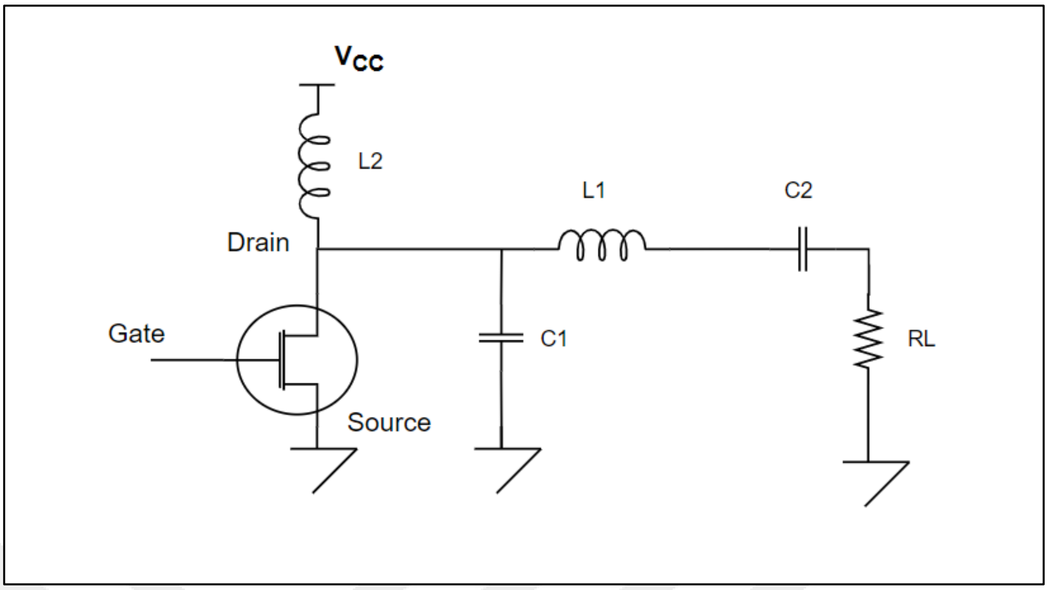

Figure 2.5 Class E power amplifier circuit diagram

When the transistor is ‘OFF’ state, there is a voltage at the drain of the transistor. The current flows the C1. There is no current on the transistor. Therefore, there is no power consumption. When it is ‘ON’ state, the current flows through the transistor and there is no voltage at the drain it because the transistor is working as an ideal switch. Again, no power consumption due to no voltage. These assumptions are valid transistor is an ideal switch, also zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) conditions. ZVS is the situation where there is no voltage on the switch at the moment it is ‘ON’ and also slope of the transistor voltage is zero is called ZVDS [42]. To obtain maximum output power at the fundamental frequency in Class-E, the transistor is operated as a 50% duty cycle [36] and provides these conditions.

Quasi-load insensitive Class-E type amplifier a variant of Class-E amplifiers. It provides high efficiency at a wide load range [43]. Being suitable for load modulation shows that it can be used in communication systems like 5G or LTE. Figure 2.6 shows the schematic of QLI Class-E. The value of the q variable affects the load modulation of the structure, and it has been proven that the q is 1.3 is the most optimal point [23].

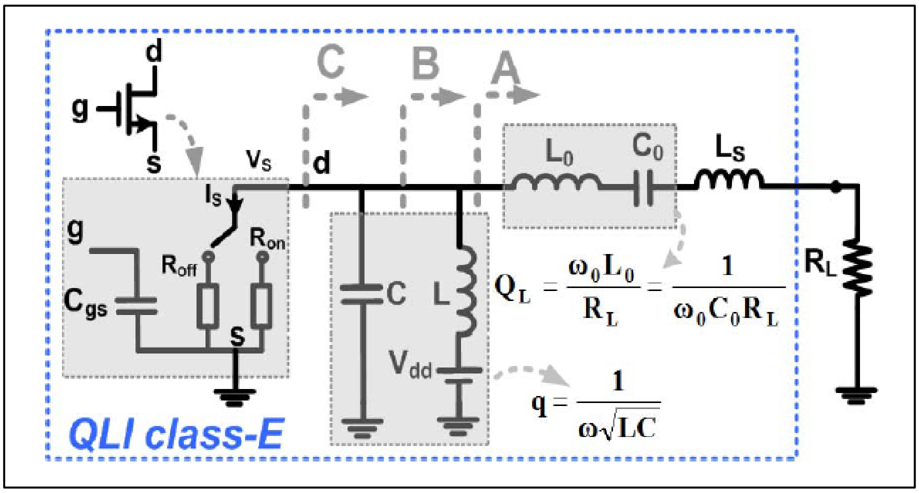

Figure 2.6 Principle schematic of the finite DC feeds inductor [23]

Figure 2.7 shows the waveform at the drain of the transistor when q is equal the 1.3 and the termination with the different loads. These loads are multiples of the optimum load. As seen figure: even if the load is up to four times, the waveforms are unaffected by this situation.

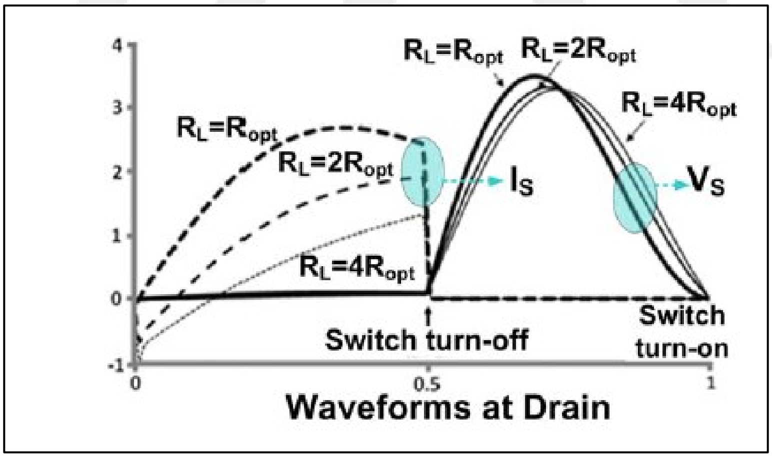

Figure 2.7 The waveforms of voltage and current in QLI Class-E [23]

3. POWER AMPLIFIER RF PERFORMANCE METRICS

The radio spectrum is one of the parts of the electromagnetic spectrum which is the representation consisting of frequency bands [44]. The general name of applications between 30 MHz and 300 GHz is radio frequency [5]. The wavelengths of the signal in this frequency band are quite small. Kirchhoff equations cannot solve RF network problems [46]. The reason for this the microwave components acts as distributed elements [5]. Therefore, the transmission line should be modeled with many components rather than a single component. Figure 3.1 is the transmission line model. Coaxial cable, microstrip line, or waveguide transmission lines used in microwave applications can be modeled in this way [17].

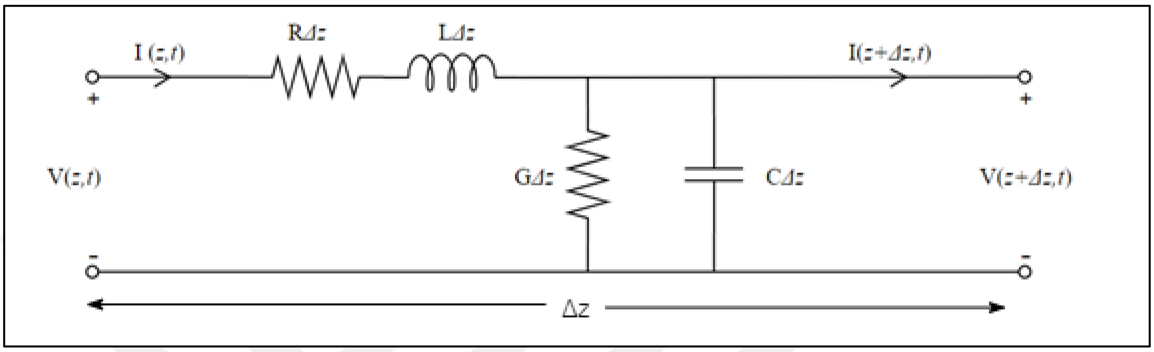

Figure 3.1 Transmission line model with distrubed elements

This model shows the voltage and current relationships between two points at Δz distance on the transmission line. R is the loss, L is the ability to store magnetic energy, G is the loss in the dielectric and C is the ability to store electrical energy. As the frequency increases, these effects are more effective at short distances.

At low frequencies, voltage and current can be measured easily and Z, Y, or ABCD parameters can be expressed easily too. However, with increasing frequency, voltage, and current measurements getting harder they cannot be measured directly. Therefore, Scattering Parameters (S-Parameters) are used at higher frequencies. These are based on the power measurement. In this way, the electrical behaviour of the RF applications can be expressed.

S-parameters derived from the scattering matrix are used in the analysis of high-frequency circuits [5]. These parameters show the relationship of the applied signal with these circuits. The states of the applied signal for two-port devices are shown in Figure 3.2.

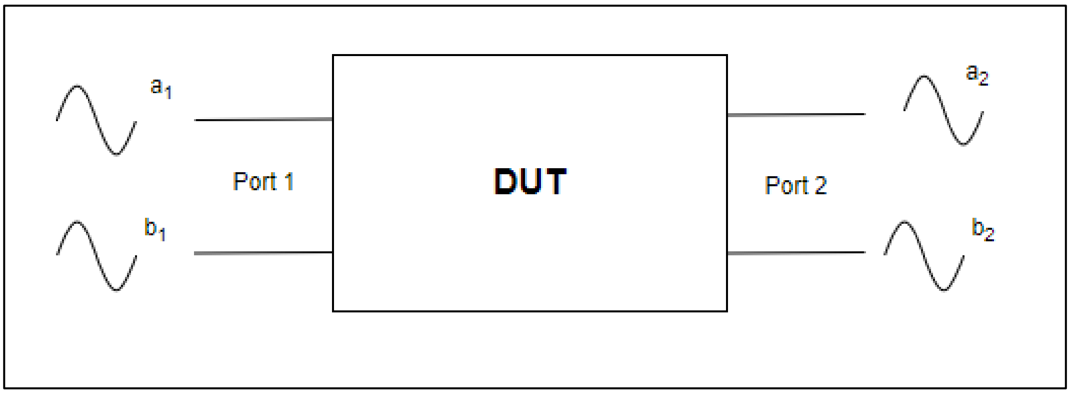

Figure 3.2 Power wave voltage for a two-port network

The lowercase a_n and b_n represent the applied signal and the wave interacting with the DUT (Device Under Test). Therefore, S-parameters can be simply defined as 3.1.

$$S_{ij} = \frac{b_i}{a_j} \tag{3.1}$$

This equation shows the S-parameters represent the ratio. There are four S-parameters for two-port devices. With these ratios, the interactions of the signal to be applied are expressed.

$$S_{11} = \frac{b_1}{a_1} | a_{2=0} \tag{3.1}$$

$$S_{12} = \frac{b_2}{a_1} | a_{1=0} \tag{3.2}$$

$$S_{21} = \frac{b_1}{a_2} | a_{2=0} \tag{3.4}$$

$$S_{22} = \frac{b_2}{a_2} | a_{1=0} \tag{3.5}$$

S_{11} represents the ratio between the reflected and applied signal when Port 2 terminated by 50 Ω. It can be named the forward reflection coefficient. S_{12} shows the reverse transmission coefficient. It is the ratio of the measured signal from Port 1 and the applied signal to Port 2. S_{21} is the opposite of the S_{12}. The signal is measured from Port 2, and it is applied to Port 1. It is the forward transmission coefficient. S_{22} shows the reverse reflection coefficient. In this case, the signal is applied to Port 2 and measured from Port 2 when Port 1 is terminated by

50 Ω. If the DUT is assumed to be an amplifier, S_{11} and S_{22} show the impedance mismatch of the amplifier with the port to which the sign is applied. S_{21} represents the gain of the amplifier and S_{12} is the isolation of amplifier. Figure 3.3 shows the S parameters for the amplifier circuit.

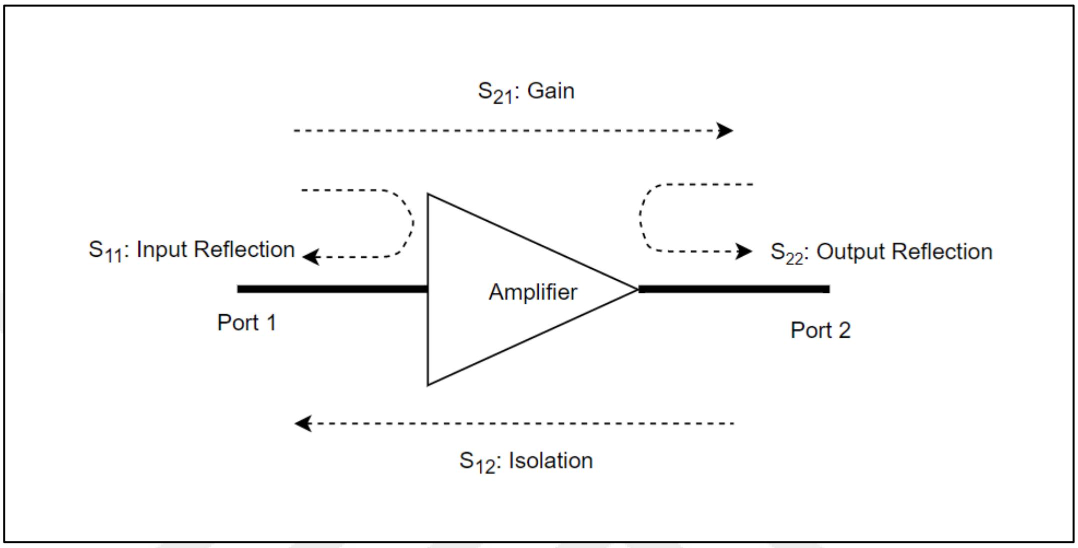

Figure 3.3 S-parameters for amplifier circuits

4. RF POWER AMPLIFIER TOPOLOGIES

Power amplifiers are frequently used in various applications. These have different requirements for each other [35]. In [35], linearity and efficiency are the most important of them. Many topologies will satisfy linearity or efficiency. These topologies can consist of a single or more transistor. Single-ended amplifiers are available. The studies about it continue from the past to the present. Generally, efficiency or linearity is achieved with these types of amplifiers. With the development of digital communication and low power consumption, it reveals the need for the simultaneous realization of two goals. Single-ended power amplifiers cannot solve these needs, these problems are overcome with complex structures.

Doherty and Outphasing power amplifiers are some of the structures for using amplified modulated signals [14] [15]. With these researches in the 1930s, AM-modulated signals were amplified efficiently. The single-stage amplifier is inefficient for modulated signals. It is seen in Figure 4.1. In this figure, the vertical axis shows the efficiency according to 100% and horizontal axis shows the ratio of the highest power level in signal to the other signal power levels. It is obviously observed if the signal power level drops in Class A and B, the efficiency will be affected which means wasting power.

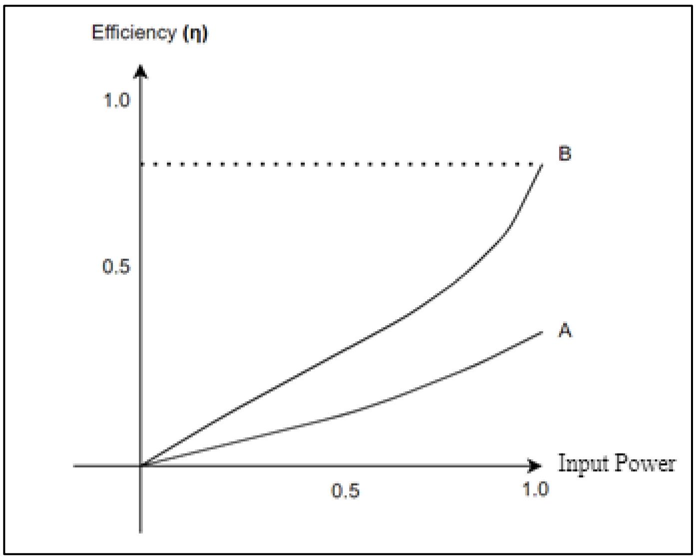

Figure 4.1 Amplitude effect of efficieny at Class A and B power amplifiers

Outphasing and Doherty power amplifier topologies solve this problem [47] [48]. The power level of the signal affects the efficiency less [16] [49]. Doherty PA consists of two transistors. One of the transistors is called the main amplifier which is biased Class AB, and the other transistor is called the auxiliary, which is biased Class C. The auxiliary amplifier is combined with the λ/4 transmission line to the main amplifier. With this structure, efficiency is maintained in input signal power level reduction [47] [50] [51].

4.1. OUTPHASING POWER AMPLIFIERS

The continuous growth of the communications industry has turned wireless communications and modulation techniques into a major field of industrial development [38]. Like DVB-T and LTE, OFDM exists at instantaneous peak power levels that are several times their average power in the time domain [27]. Amplification of these signals occurs the distortion on themself. Outphasing has been developed for obtaining energy-efficient, high-accuracy amplitude-modulated transmitters from vacuum tubes and it is still used nowadays to amplify modulated signals [15] [47] [49]. The outphasing offers to control outpower power by outphasing angle or phase shift (ϕ, θ) applied to the input signals fed into each PA branch [49].

The classical outphasing approach uses two constant-envelope phase modulated signals to produce a complex modulated output, and the PAs are expected to function as voltage generators [52]. This means that the PAs are in saturation mode. The efficiency can be preserved by amplifying signals with consistent amplitude at the optimal efficiency level for specific PAs in a classical outphasing approach. Figure 4.2 shows the vector representation of the signal in the outphasing approach [53]. $S_1(t)$ and $S_2(t)$ are the input signals of PAs. The original modulated signal (S_{in} (t)) is decomposed into two signals [53] and these signals have constant amplitude.

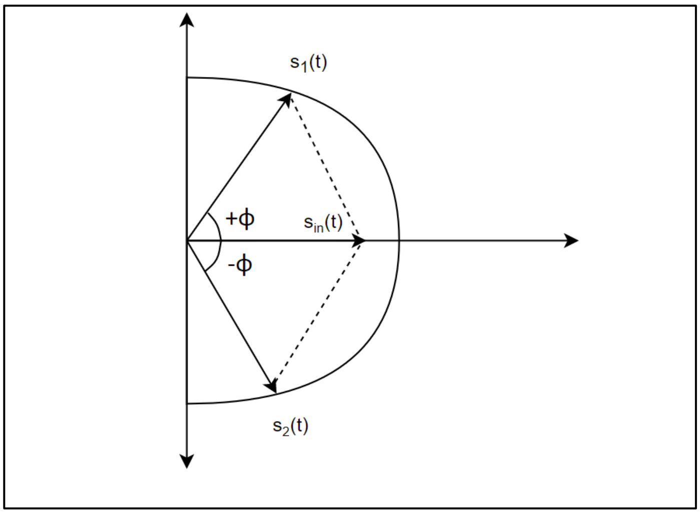

Figure 4.2 Vector representation in the clascical outphasing approach

As seen in Figure 4.3, the modulated signal is separated into two signals with signal component separator. The separated signals have a constant amplitude but they have a phase difference. These signals are amplified with switching classes PA and these signals are summed with a combiner. Thus, the input signal is amplified while preserving its form.

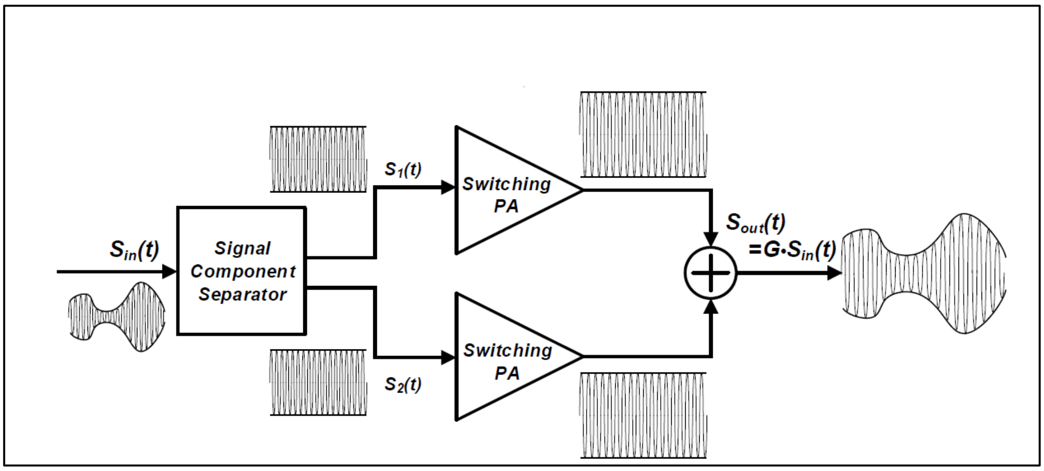

Figure 4.3 Outphasing architecture [49]

As can be seen, there are three important parts of outphasing amplify. These are input signal separation, amplifying signals, and combining signals. This thesis focuses on the last two parts.

Figure 4.4 represents the outphasing power amplifier structure basically. There are two signal sources and PAs. The outputs of PA are combined, and the combined signal is transmitted to the load. The PAs are identical to each other [54]. The differences between the two PA are they fed with two signals that have a phase difference with respect to each other and the electrical length (phase shift) of combiner circuits are also different [55]. The phase difference between two amplifiers is represented with ϕ_1 and ϕ_2. The $\theta_{1,2}$ presents the length of the combiner circuit in terms of degree.

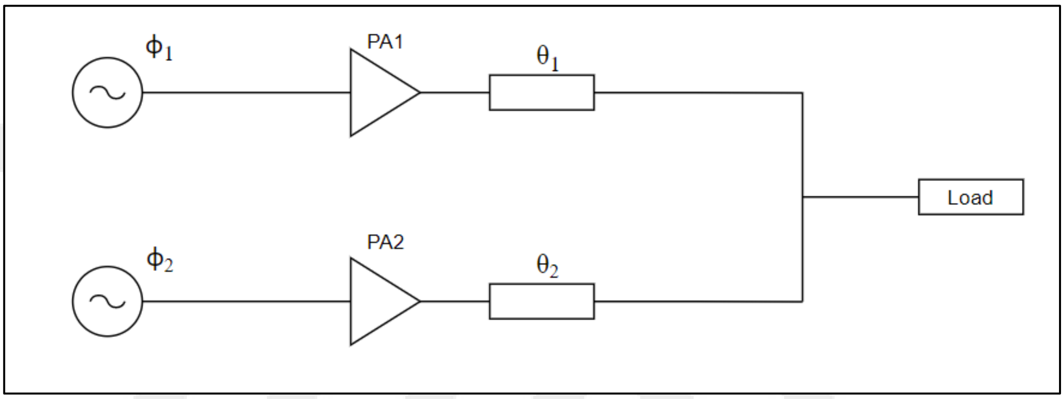

Figure 4.4 Block diagram of outphasing power amplifier

In this way, high efficiency is achieved at the back-off power level [56]. This shows that outphasing power amplifier structure is suitable for 5G communication systems. The PA maintains its efficiency up to a certain level in complex modulated signals and thus it keeps the power consumption constant to other structures. The fact that it consists of two identical PAs and a simple combiner circuit makes the structure even more attractive. Figure 4.5 shows the theoretical efficiency of outphasing PA. According to this, when the outpower is decreasing, the efficiency is constant. Compared to Figure 4.1 its advantages are clearly seen. Also, the back-off value is shown in Figure 4.5 as the point where the efficiency starts to decrease. With this value, it is expressed that the efficiency of the amplifier remains constant even if the output power drops how many dB.

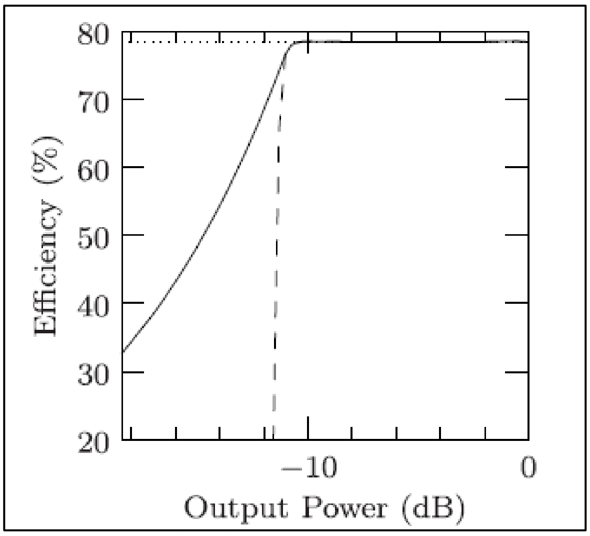

Figure 4.5 Theoretical efficiency graph of outphasing [50]

The efficiency shown in the graph can be obtained with the Doherty structure [16] but the outphasing structure has a simple design. As shown in Figure 4.4, PA1 and PA2 circuits and their input circuits are the same. They are the same class amplifiers. As mentioned, there are two different class amplifiers in Doherty.

4.2. QLI CLASS-E AMPLIFIER DESING

As mentioned in 2.2.2, studies on QLI Class-E, amplifiers can be made suitable for load modulation. This means that the impact of load modulation on amplifier performance is reduced, especially in efficiency. The resonance factor (q) has a high impact on the switching operation of Class-E [57]. In the conventional Class-E, there are capacitive power losses when RL is increased [43] which is shown in Figure 2.5 and q is also related to L1 and C1 in the same figure.

$$q = \frac{1}{\omega\sqrt{L_1 C_1}} \tag{4.1}$$

According to the [23] [58]; when the q value is 1.3, it provides an operation suitable for load modulation. Taking these studies as a reference, calculations are made so that the q value is 1.3. The work done in the references is at the IC circuit level. The discrete transistor is used in this study. The transistor used is CG2H40010F. The capacitance shown in Figure 2.5 is used as the parasitic capacitance formed in the transistor. The capacity marked with a red box in Figure 4.6 represents the parasitic capacity formed by the transistor drain source.

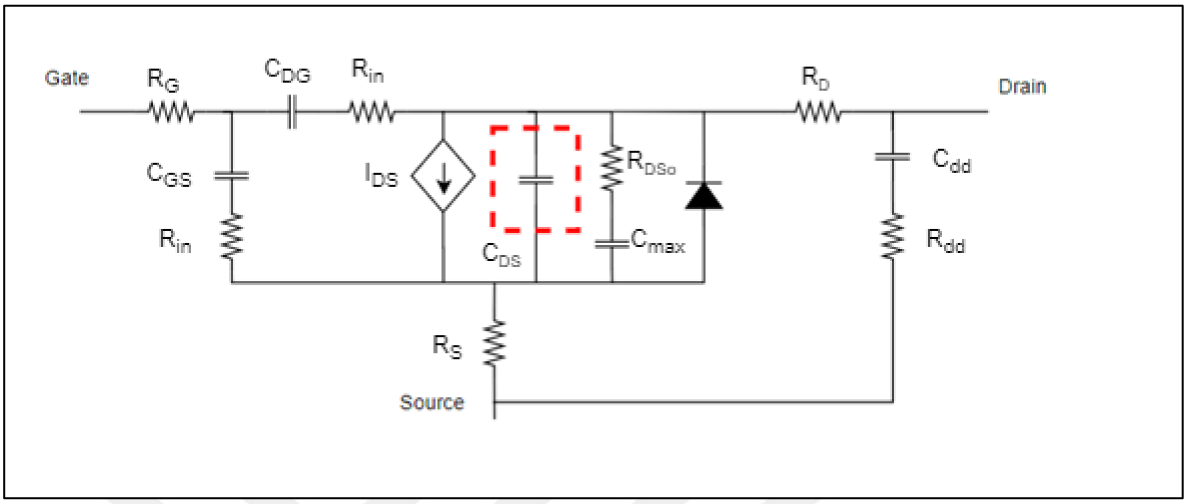

Figure 4.6 Parasitic model of transistor

This capacitance value is observed with AWR Microwave Office. For this, it uses the model file of the transistor used which was created by the transistor manufacturer. This simulation is done by connecting a port to the transistor drain node and the impedance value in the target frequency is observed. In this simulation, the transistor is biased with the ideal bias-tee circuited in this way transistor is prevented from these circuits. The circuit schematic of this simulation and the result of the simulation are shown in Figure 4.7 and Figure 4.8 respectively.

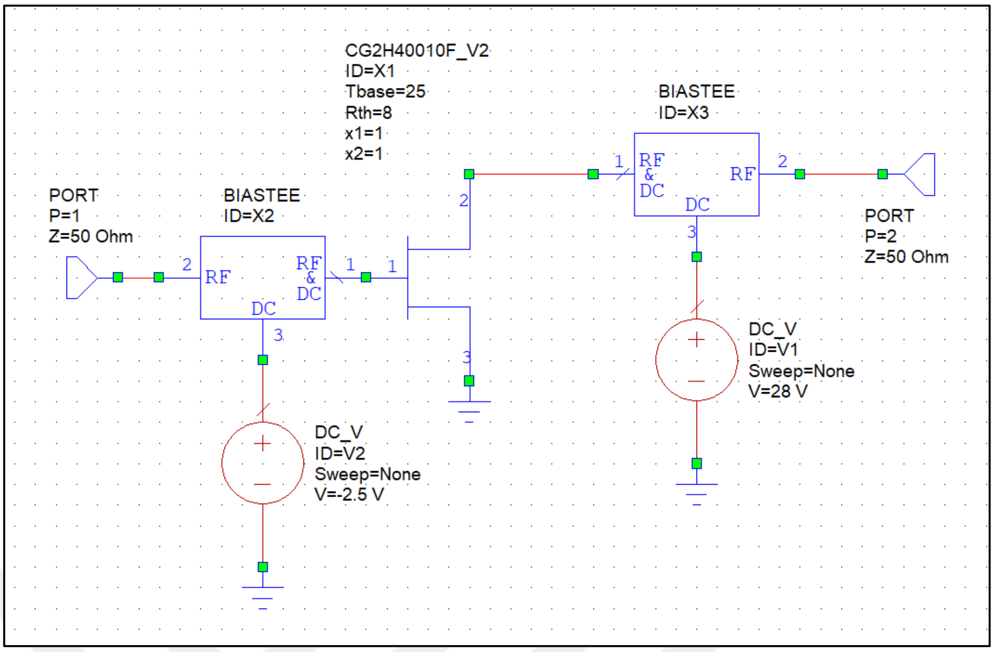

Figure 4.7 Parasitic capacitance simulation circuit

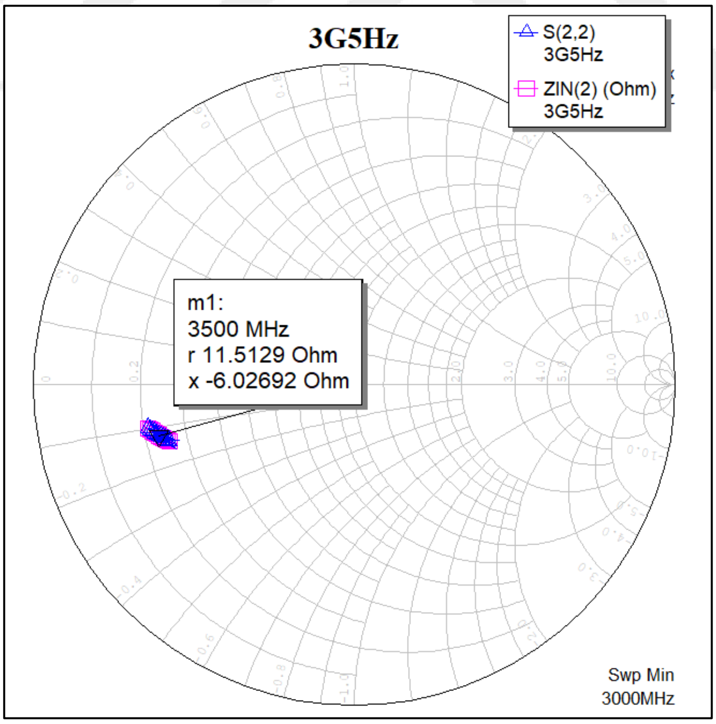

Figure 4.8 Parasitic capacitance simulation result

As a result of the simulation, the output impedance of the transistor is shown as S_{22} and the impedance on the Smit chart with a complex expression. These two results are the same. In this way, it can be said that the output impedance of the transistor is the same as the S_{22} for the Smith chart. As seen in the marker in the figure, impedance has two components. These are real and imaginary parts. It is assumed that the imaginary part formed at the output occurs due to capacitive load. This capacitive load is the parasitic effect. The imaginary part shown in Figure 5.3 is -6 Ω. The value of capacitance is calculated using 4.2.

$$Z_C = j\omega C \tag{4.2}$$

With the equation, the value of the parasitic capacitance is calculated as 7.5 pF. Using this value, it is calculated that the L value should be 0.16 nH in order for the q value in the 4.1 to be 1.3. The inductor of this value is added to the circuit. This circuit schematic is shown in Figure 4.9. The inductor added to the circuit is marked with a red box.

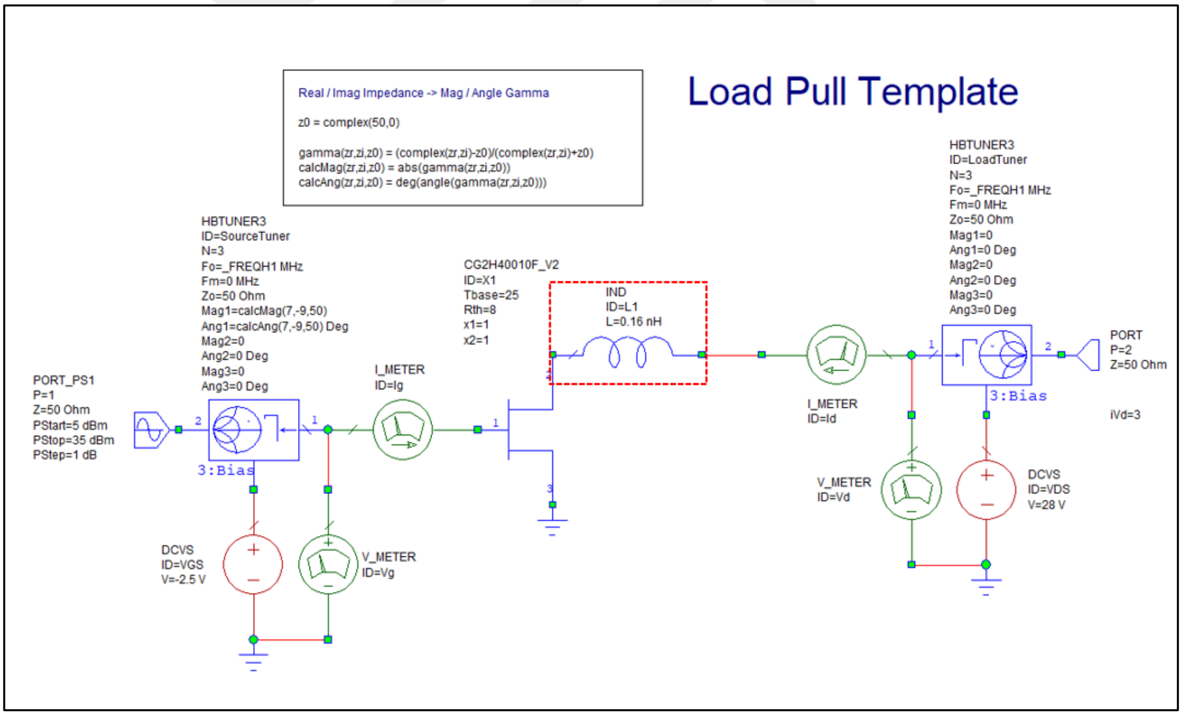

Figure 4.9. Schematic of the circuit with inductor

The circuit shown in the figure is analysed with and without an inductor. Output power and PAE values are observed by performing load-pull simulations.

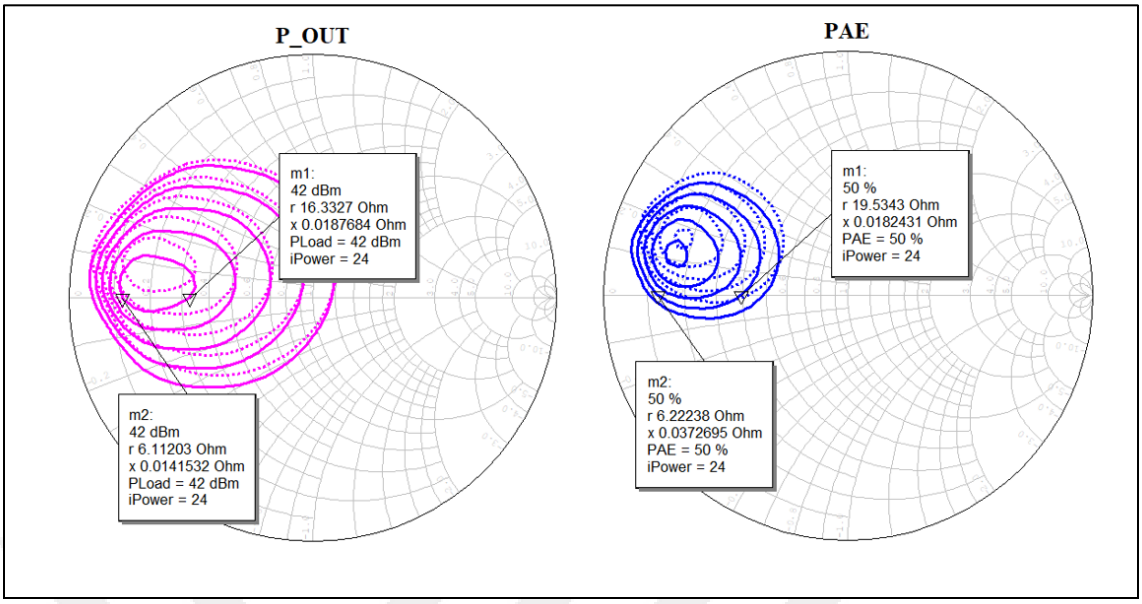

Figure 4.10 Outpower and PAE load-pull simulation results

Figure 4.10 shows the results of outpower and PAE of a schematic of Figure 4.9. Output power and PAE are shown left and right sides of this figure respectively. The dashed lines show the results without the inductor and the solid lines show the results with the inductor. As can be seen, circles get closer to the real axis with the inductor. Even if the load changes between 6 Ω and 16 Ω, there is no change in the output power value. In efficiency values, this range becomes even wider. According to these results, if the output of PAs is 10 Ω, maximum output power and high efficiency can be provided. The QLI Class-E is designed with ideal components. Figure 4.11 is the designed PA and Figure 4.12 shows the simulation result.

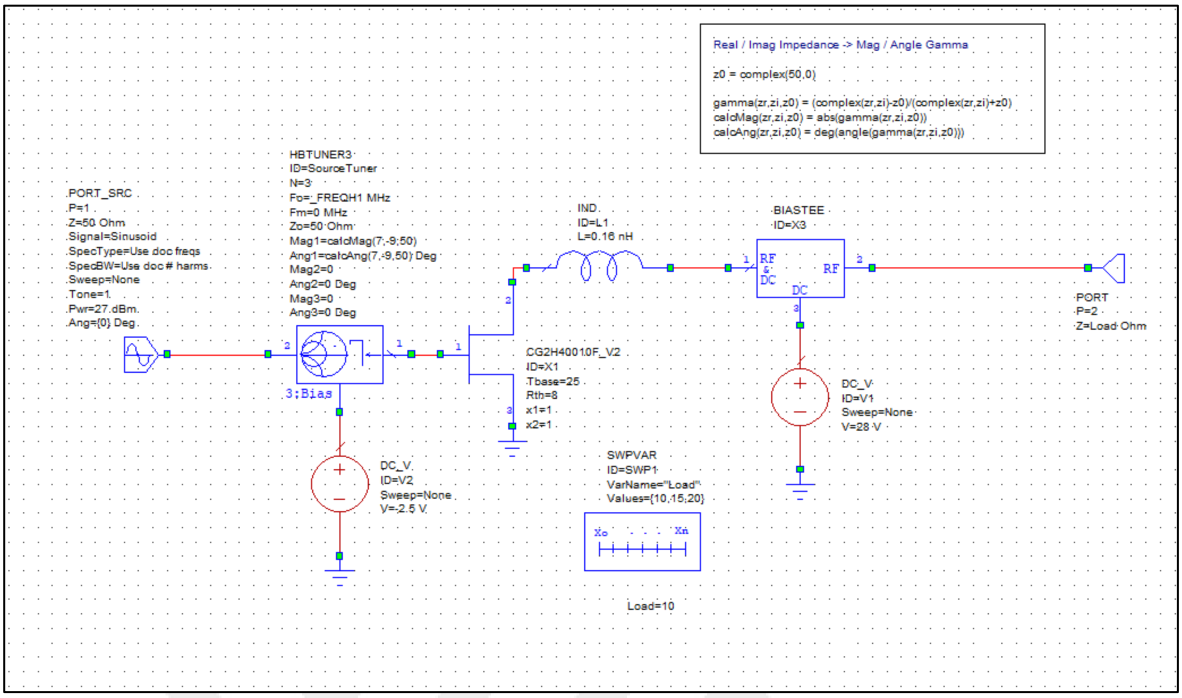

Figure 4.11 QLI Class-E PA ideal design

In Figure 4.12, outpower and drain efficiency can be observed between 3.1- 3.7 GHz. The blue and pink graphs show outpower and drain efficiency respectively. As seen in the figure, the amplifier circuit has an output power of over 42 dBm almost across the band and efficiency value is higher than 50%.

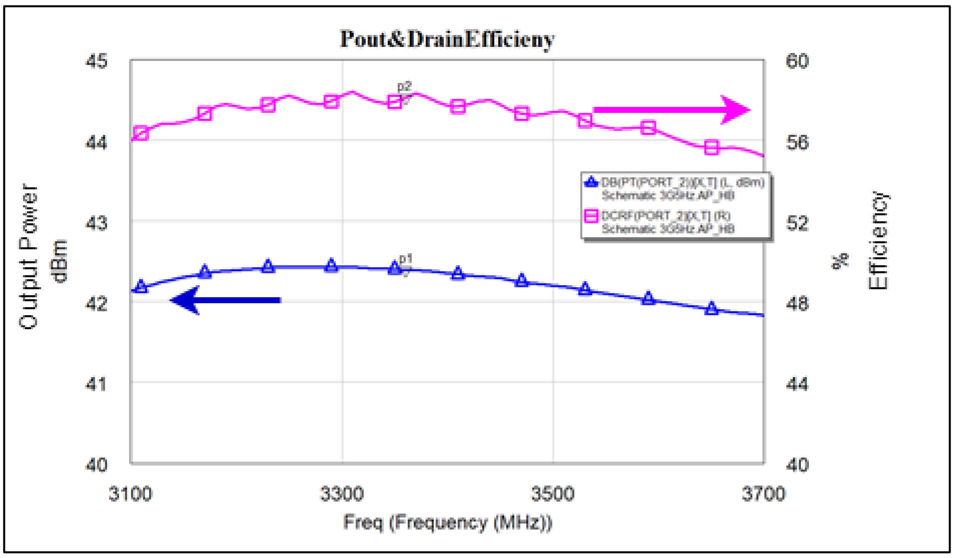

Figure 4.12 Ideal QLI Class-E PA simulation result

The input matching network (IMN) is designed instead of the tuner in Figure 4.11. IMN is compatible with the circuit found in the transistor's datasheet. Figure 4.13 is the amplifier with IMN. Figure 4.14 shows the outpower and S-parameters of this.

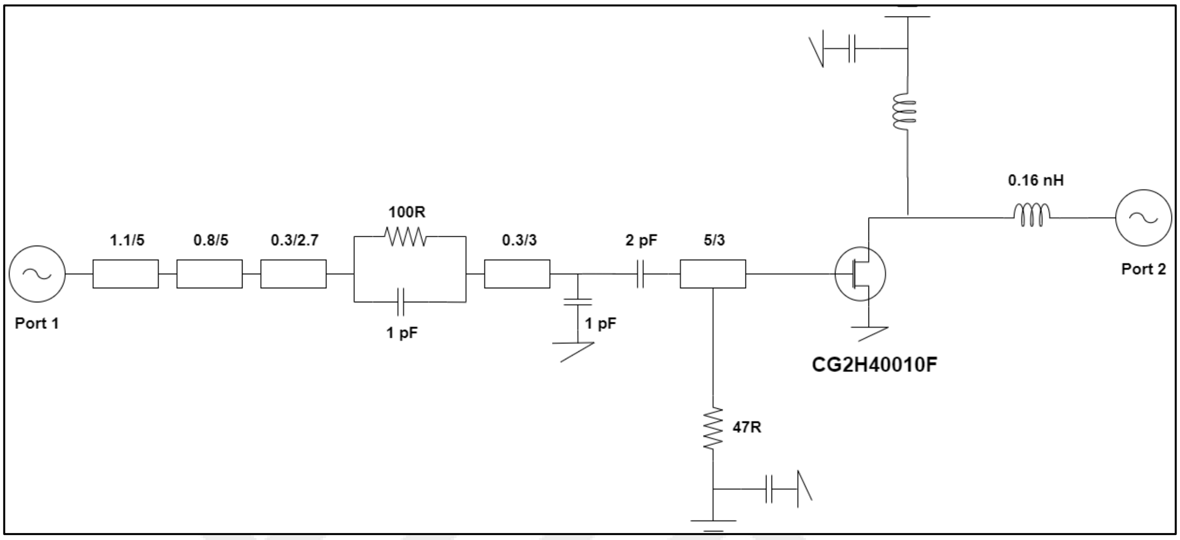

Figure 4.13 Amplifier with IMN

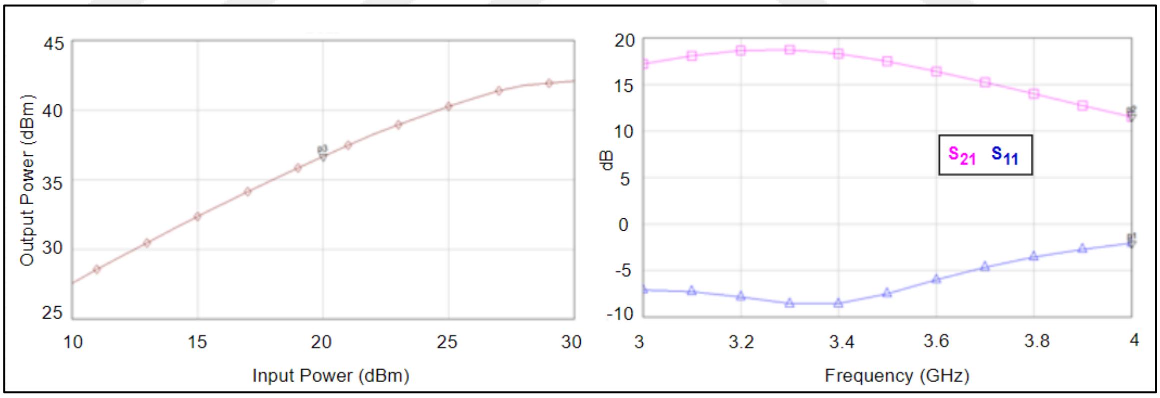

Figure 4.14 Output power and S-parameters of amplifier with IMN

In the left side of the figure, the output power is seen according to the input power. Gain and input return loss can be observed on the right side. The pink graph is the gain of the amplifier, and the blue graph is the input return loss. According to these graphs, this amplifier has 42 dBm outpower at the saturation region. It has a 17 dB gain and 7 dB input return loss at 3.5 GHz.

4.3. COMBINER DESINGING

As discussed in the previous sections, the phase difference of input signals and combiner between of two amplifier stages determines the outphasing operation. Henry Chireix's original creation featured a shunt reactance combiner that effectively minimized the reactive loading experienced by the branch amplifiers across a variety of outphasing angles [49]. Subsequent studies about combiners prove that reactive loading can be compensated through series or shunt reactance XC in the combiner to maximize the power factor [20]. Outphasing combiners can be divided into two main types isolated and non-isolated combiners [18]. Isolated combiners provide linearity, but they have a loss, non-isolated combiners are lossless [18]. With this circuit, the impedance value seen by the transistors is controlled by phase difference [53]. The observed in Figure 4.15 sources represent the amplifier circuits. As seen in the figure they connect the common load.

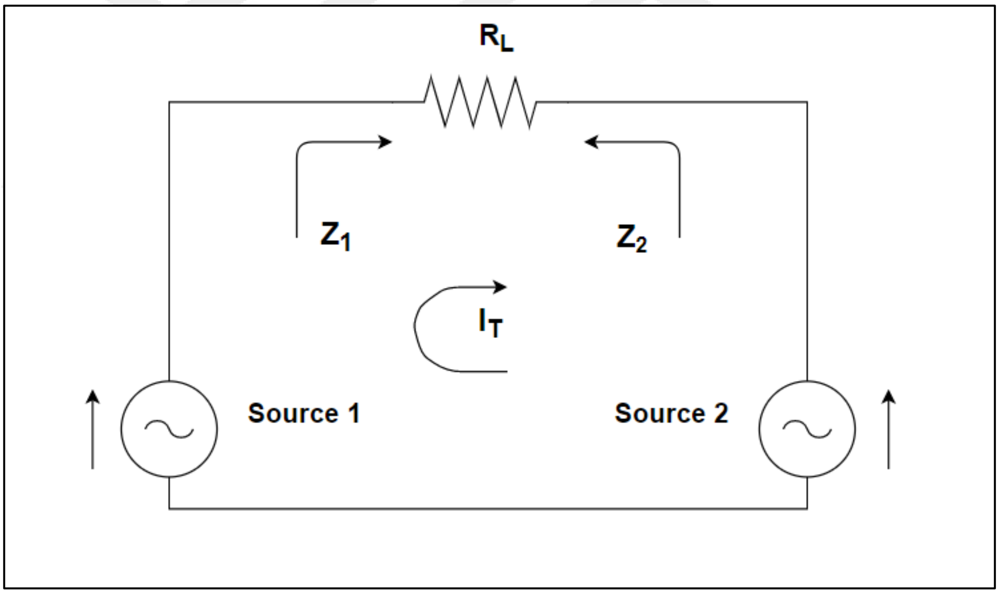

Figure 4.15 Equivalent circuits of outphansing amplifier combiner

These voltage sources have equal magnitude A and phase offset θ;

$$V_{1,2} = A \, . \, e^{\pm i\theta} \tag{4.1}$$

The total current in this equivalent circuit is given by

$$I_T = \frac{V_1 - V_2}{R} = \frac{V}{R} 2j \sin\theta \tag{4.4}$$

Z_1 and Z_2, which express the impedance value seen by the transistors, can be given as

$$Z_{1,2} = \frac{V_{1,2}}{I_T} = \frac{R}{2}(1 \pm j\ \cot\theta) \tag{4.5}$$

These analyses can be done with simulation programs. The circuit in Figure 4.15 is simulated in the Advanced Design System (ADS). In addition to this circuit, transmission lines are added after the sources to from the combiner circuit. Figure 4.16 shows the combiner analysis circuit. Impedance values can be observed with 4.5. Therefore, the probes are added to the circuit. In the figure, the transmission lines are calculated according to the electrical length. 3.5 GHz is selected as the base frequency. The characteristic impedances of these are selected according to the simulation result of QLI Class-E. This value is 10Ω. The length of these transmission lines is swept.

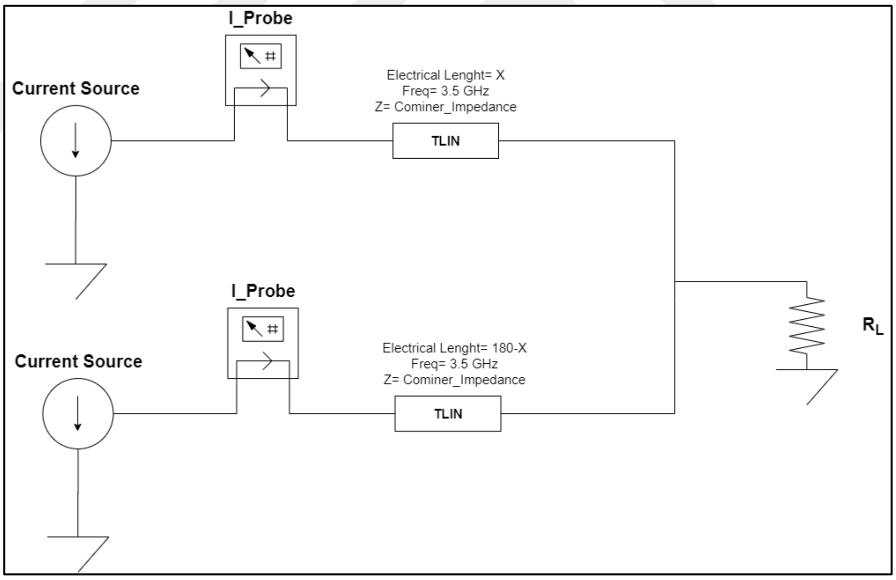

Figure 4.16 Combiner analysis circuit

A variable is assigned to the length of the transmission line of the source which phase is variable. The length of the other transmission line to be occurred by the combiner is assigned a variable value of 180 minus and half of the characteristic impedance is assigned to the load value. The result of this circuit is shown in Figure 4.17.

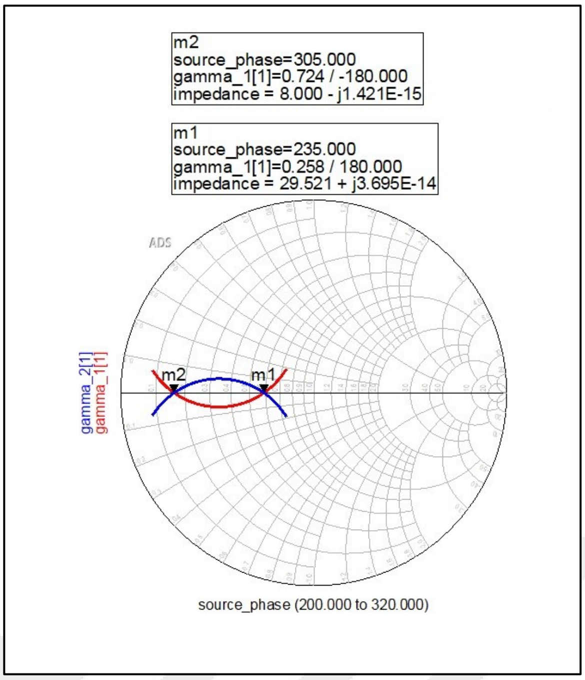

Figure 4.17 Simulation result of combiner analysis circuit

The blue and red lines represent the impedances seen by the transistors. According to the result, when the phase difference of the two sources is 235° or 305°, the impedance seen by transistors is on the real axis. These values are observed when the characteristic impedance is 10Ω and the X variable is 62.5°. An appropriate combiner circuit is designed with these values. The designed circuit is shown in Figure 4.18. In this circuit, the inductor of the end of the transistor is taken into simulation and the combiner circuit is expressed in terms of electrical length.

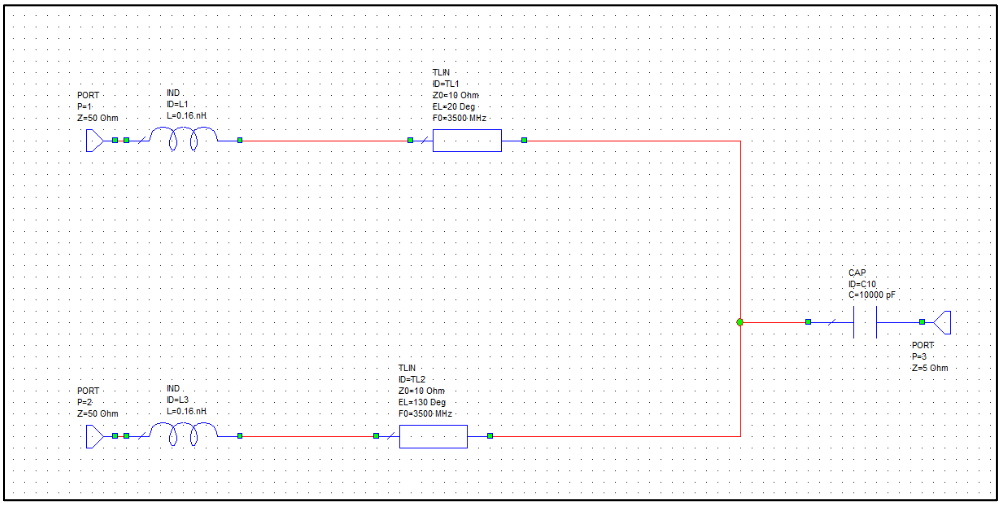

Figure 4.18 Combiner circuit with inductor and expressed with electrical length

The same circuit is also designed with transmission lines. The characteristic impedance and length degree conversion can be calculated with AWR tools. The TXLINE tool can be used. Figure 4.19 is the interface of that tool. By entering the substrate properties to be used in this interface, the thickness of the microstrip line is calculated for the desired characteristic impedance value. In this design, 0.508 mm Rogers 4003 substrate is used. Additionally, by entering the frequency and degree value, the length of the transmission line can also be calculated with this tool.

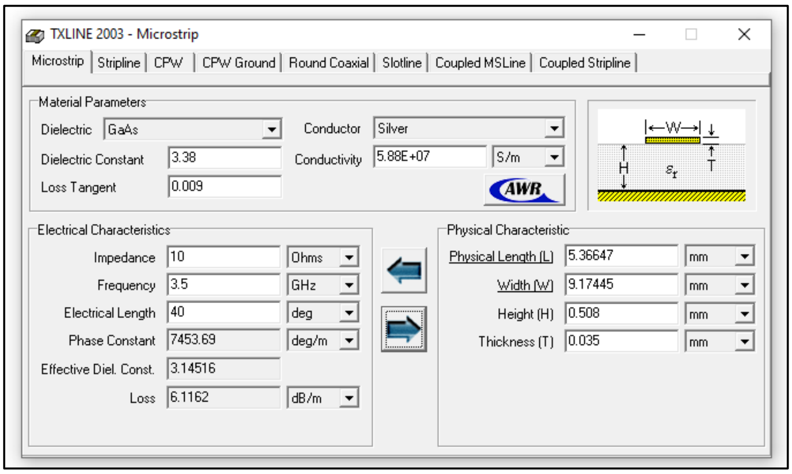

Figure 4.19 The interface of TXLINE tool

Figure 4.20 shows the combiner circuits expressed with length. In this circuit, the inductor is involved in the transmission line. The simulation results of circuits shown in Figure 4.18 and Figure 4.20 are shown in Figure 4.21.

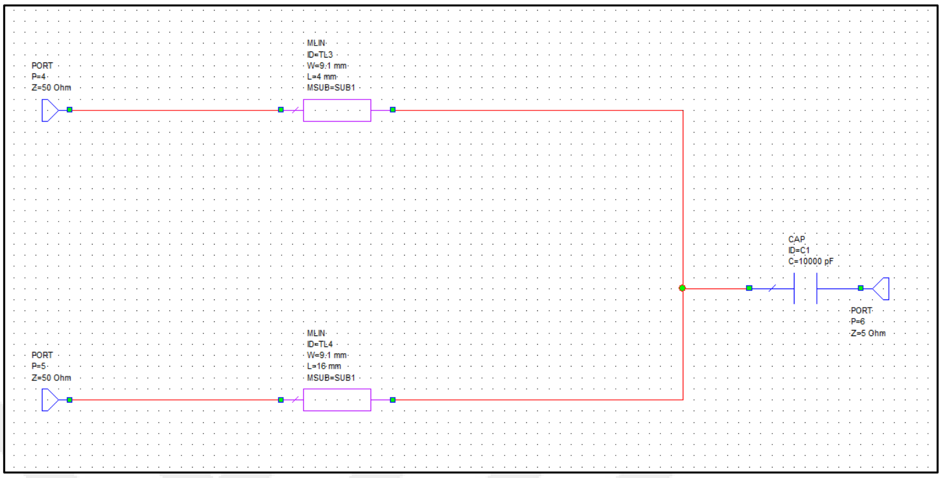

Figure 4.20 Combiner circuit as expressed with length

The reflection results of the two circuits are shown in the Figure 4.21. The combiner circuit has 3 ports. The blue and red lines show the simulation results of the circuits shown in Figure 4.18 and Figure 4.20 respectively. As seen in Figure 4.21, simulation results of two circuits are almost same.

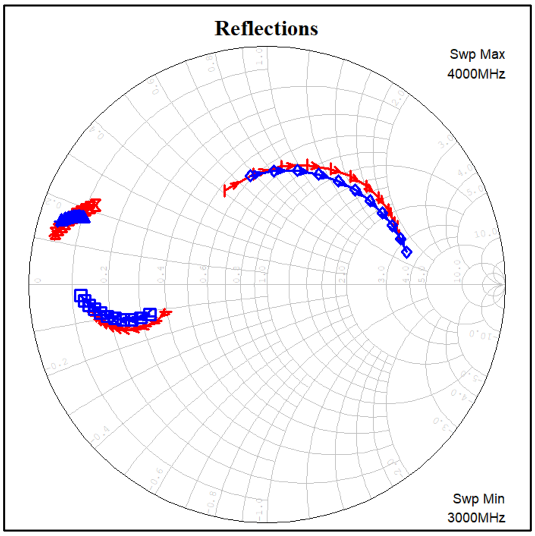

Figure 4.21 Reflection simulation results of combiner circuits

Figure 4.22 and Figure 4.23 show comparisons of the transmissions of the two circuits. The solid lines represent the circuit which expressed with electrical length and dashed lines represent the circuit which expressed with length. In Figure 4.22 shows the phase change of the transmission.

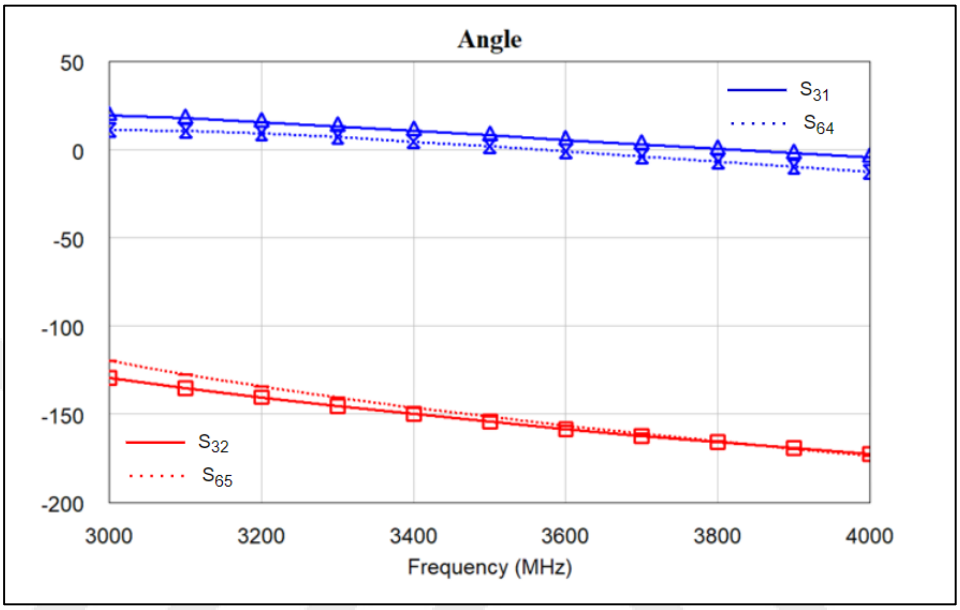

Figure 4.22 Compression of angle of two combiner circuits

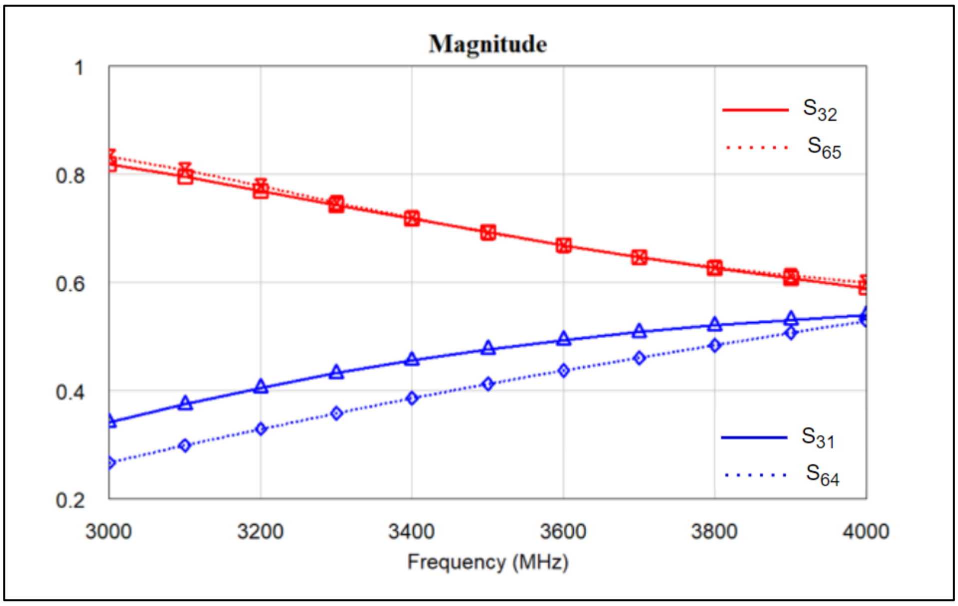

Figure 4.23 Compression of magnitude of two combiner circuits

Since the impedance of the common node of the designed combiner circuit is 5 Ω, an impedance matching circuit is designed. The output matching network (OMN) provides compatibility from 5 Ω to 50 Ω. Figure 4.24 shows the OMN.

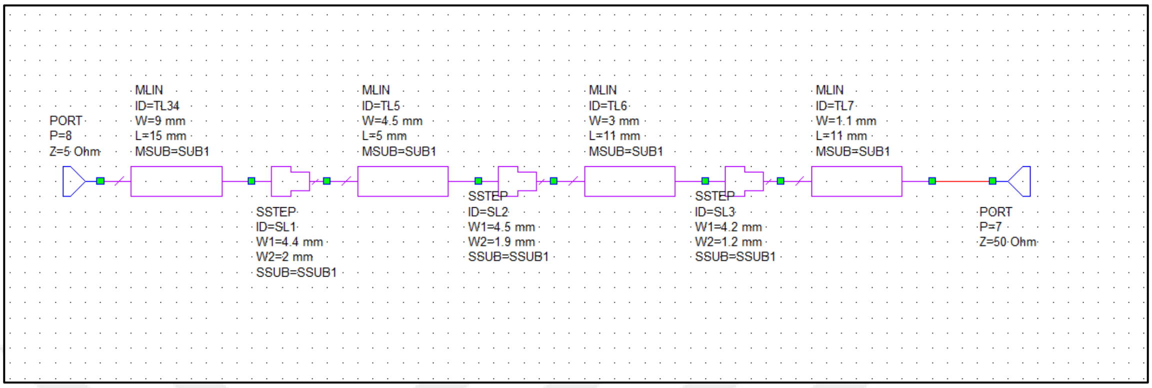

Figure 4.24 Output matching network

The S-parameters simulation results of OMN are shown in Figure 4.25. The blue and pink lines in Figure 4.25 represent S_{21} and S_{11} (insertion loss and input reflection coefficient) of OMN respectively. The insertion loss of designed OMN is almost 0.5 dB across the frequency band and the reflection coefficient is better than -10 dB.

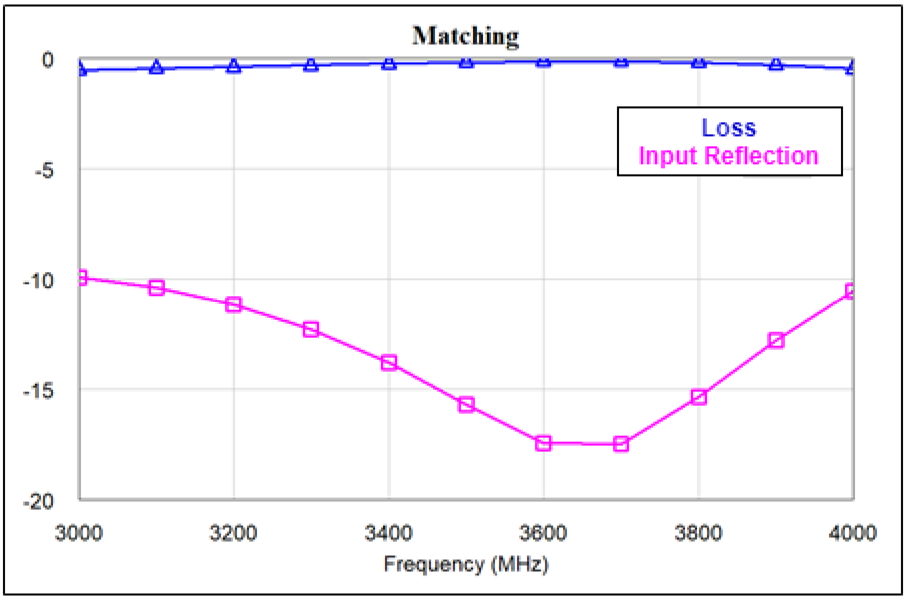

Figure 4.25 S-Parameters of OMN

4.4. OUTPHASING POWER AMPLIFIER DESINGING AND SIMULATION RESULTS

The circuit in the Figure 4.13 is multiplexed and combined with the combiner circuit in the Figure 4.20 and the impedance transformation of this structure is done with OMN in the Figure 4.24. All the circuits form the outphasing amplifier circuit with the QLI Class-E topology. The schematic of designed power amplifier circuit is shown in the Figure 4.26. With this circuit, the amplifiers are fed to different phases and the effect of phase on output power and power added efficiency is observed. As seen in the figure, there are two signal generators. The phase of these generators is swept between 10° and 360°. The power level of signal generators is swept between 20 and 31 dBm. The simulation is done at 3.4 and 3.5 GHz. The simulation result for 3.5 GHz is shown in the Figure 4.27. This graph shows the Pout and drain efficiency according to the phase. The phase is named as 'Phi' in the graph, and it is horizontal axis. The outpower and drain efficiency are shown as blue and pink, respectively.

The simulation results are also shown in the Figure 4.28. These two results are same. The reason why it is shown in Excel is because the measurements to be taken are plotted that way. In Figure 4.28, the horizontal axis shows the output power, and the vertical axis shows the drain efficiency. The phase change is indicated by an arrow. In this figure, the phase difference is not swept up to 360°. The direction of the arrow shows the direction of increase of the phase difference.

The effect of phase is clearly seen in both figures. When the phase differences between the two amplifier circuits reaches the optimum point, the circuits provide good performance compared other phase states. The output power and efficiency are highest point they can reach at the same time. If Figure 4.28 is examined, the optimum point for output power and drain efficiency can be observed. When the phase difference value is 180°, outphasing power amplifier has 43.5 dBm outpower with 50% drain efficiency. Figure 4.31 shows the simulation results of phase difference at the different input power levels. In these results the phase difference is swept up to 360° As can be seen in the figure, phase difference at different input power levels improves the performance of the circuit up to a certain point. After that point, output power and drain efficiency values decrease. The circuit shows the same effect at all input power levels.

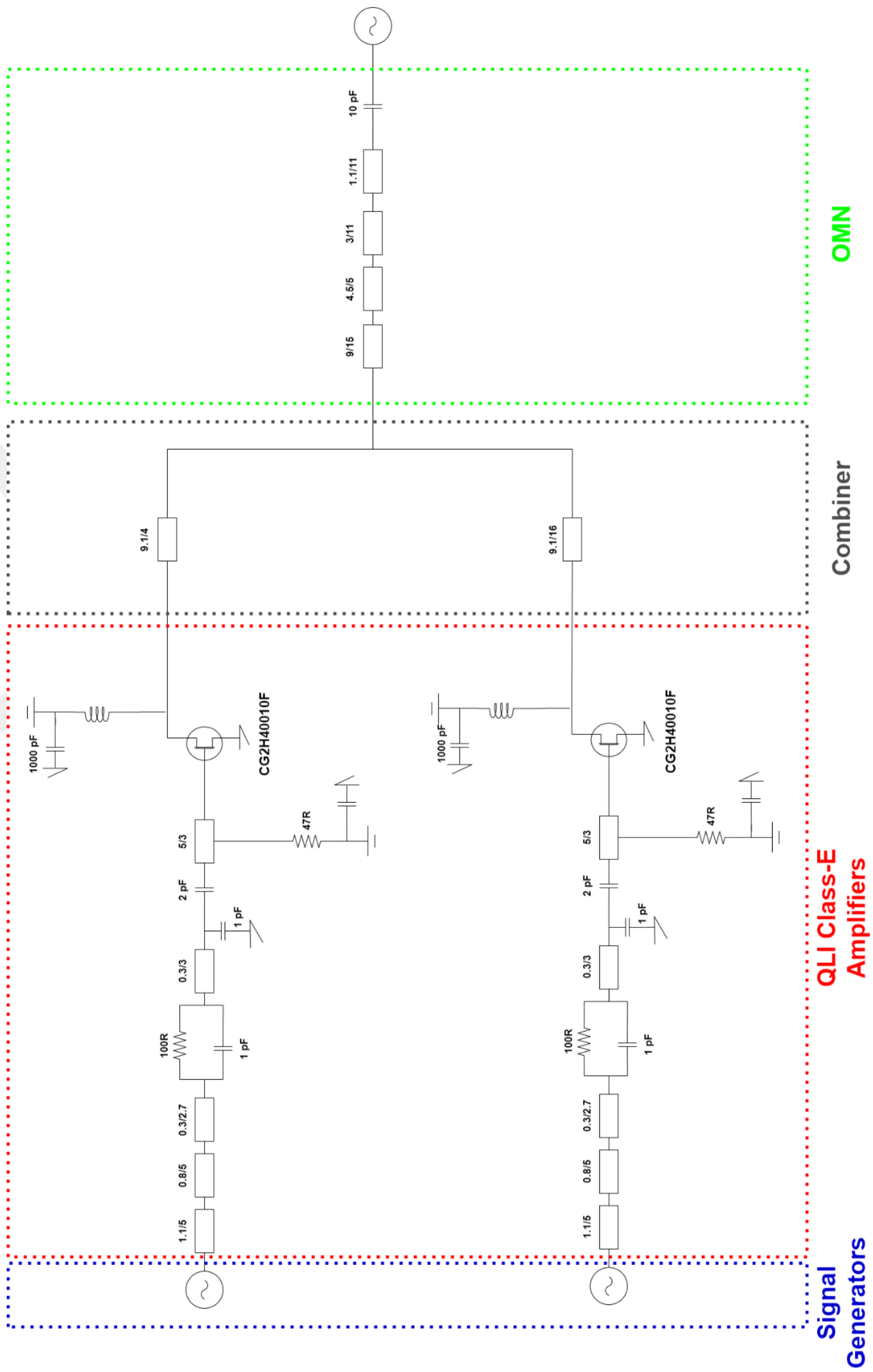

Figure 4.26 QLI Class-E outphasing power amplifier schematic

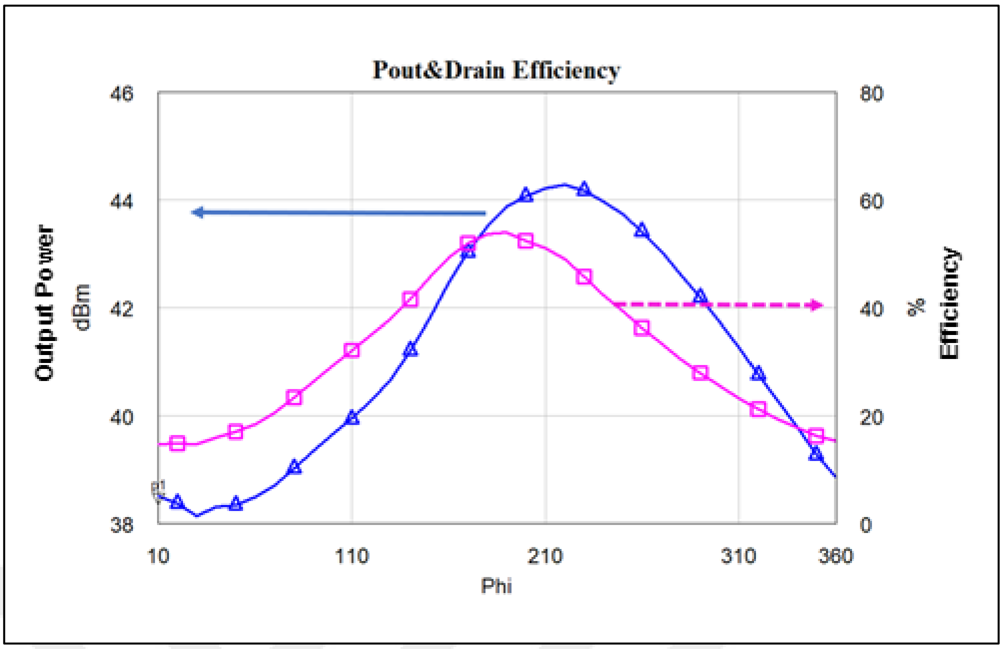

Figure 4.27 Pout and drain efficiency simulation result for 3.5 GHz in CAD

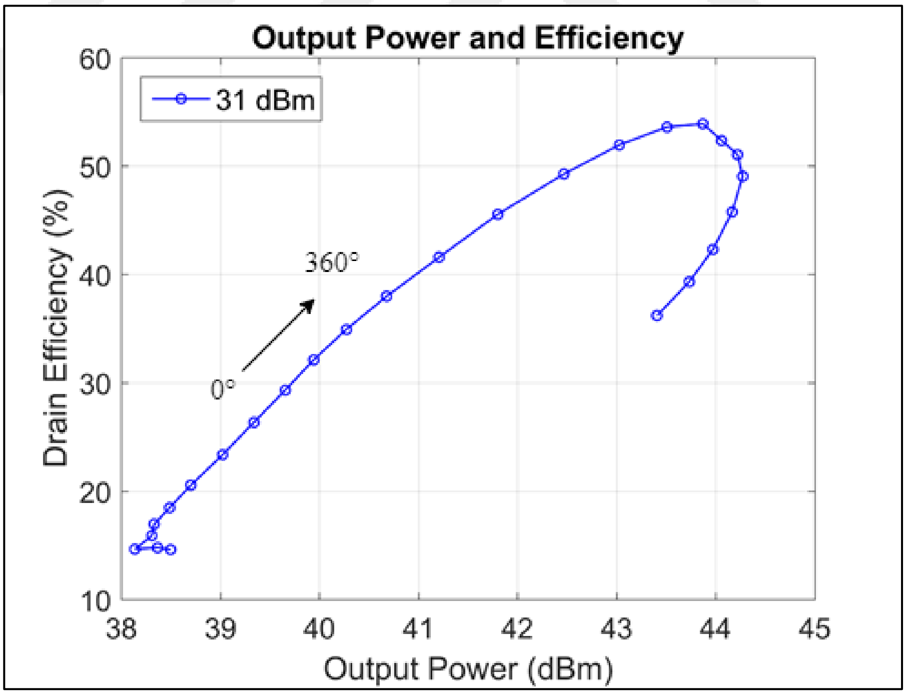

Figure 4.28 Pout and Drain Efficiency simulation result for 3.5 GHz in Matlab

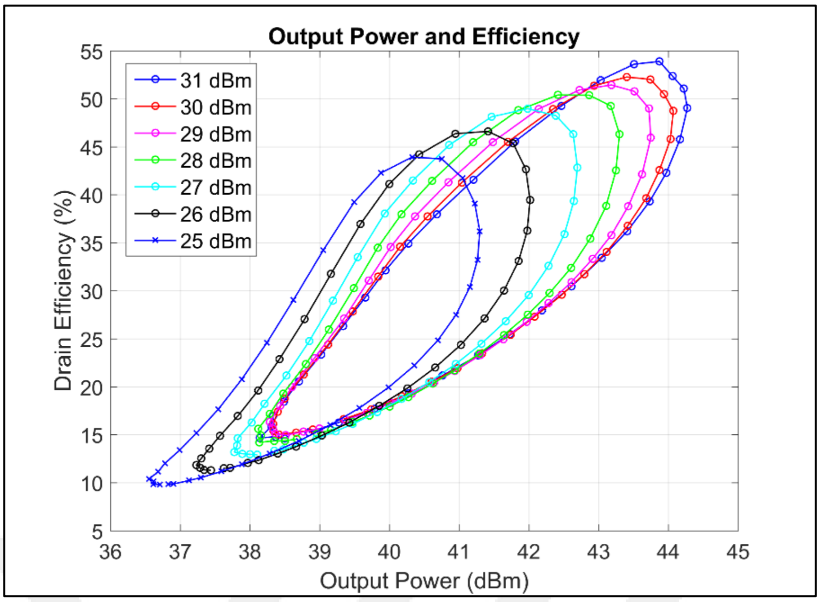

Figure 4.29 Effect of phase change on output power and efficiency according to different input power levels

Figure 4.30 shows the drain efficiency according to the different input power levels at 3.5 GHz. As can be seen in that figure, even though the input power of the circuits drops by 6 dB, the drain efficiency of the circuit remains over 40%.

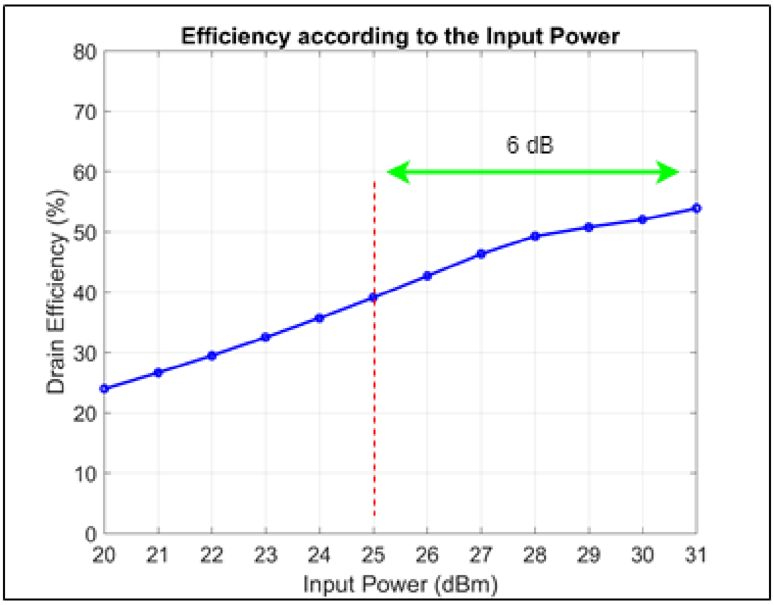

Figure 4.30 Simulation result of drain efficiency according to the input power

The performance of the circuit at different frequencies is shown in the Figure 4.31.

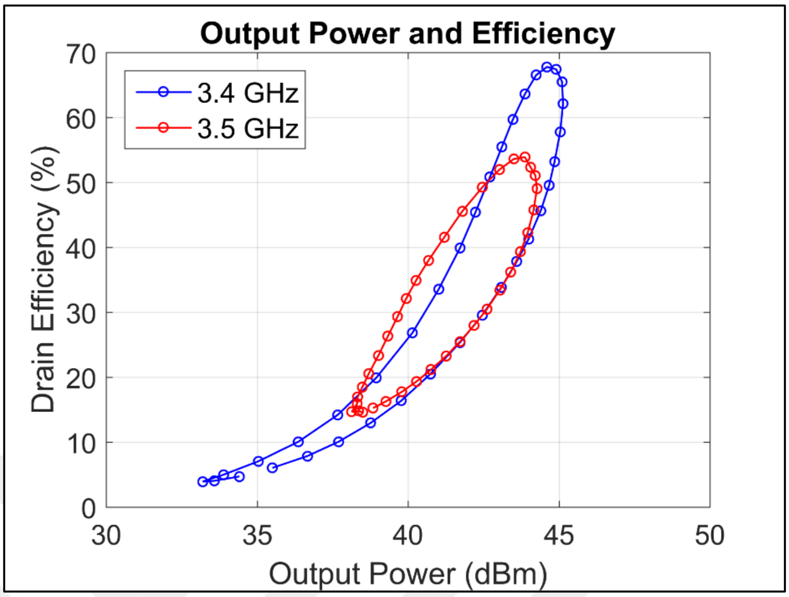

Figure 4.31 Pout and drain efficiency simulation results for 3.4 and 3.5 GHz

The same simulations are repeated by adding the EM simulation results of the combiner and OMN circuit to the outphasing power amplifier circuit. With this study, it is tried to obtain a result closer to the circuit that will be realized. The combiner and OMN circuit are connected as shown in Figure 4.32. Simulation results of outphasing power amplifier obtained by adding the 3D simulation solution result of this block to the circuit are shown in Figure 4.33 and Figure 4.34.

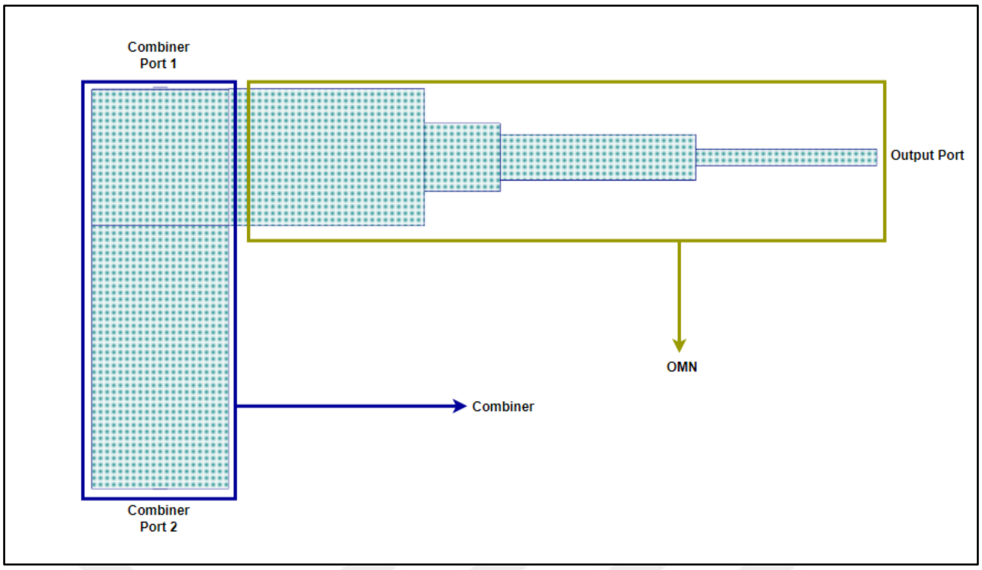

Figure 4.32 Combiner and OMN circutis 2-dimensional representation

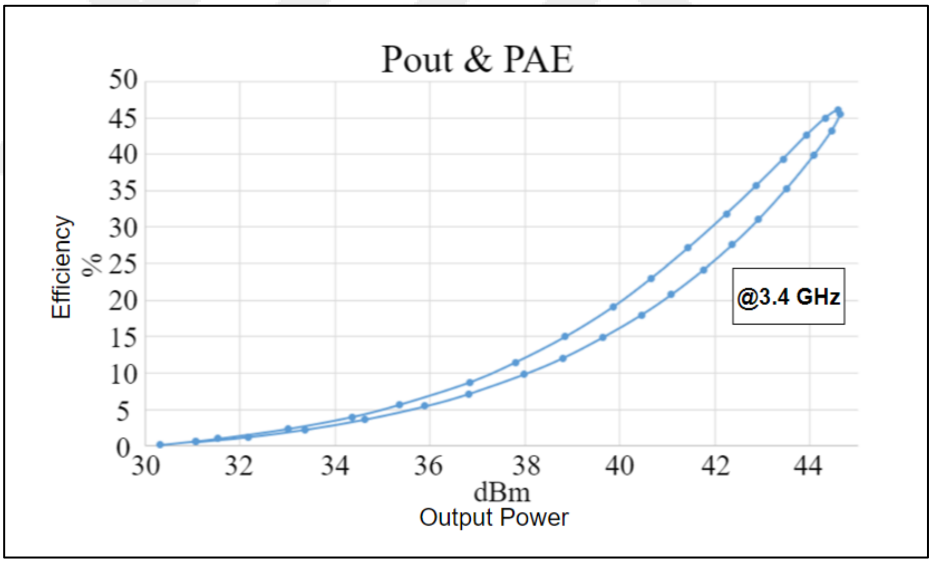

Figure 4.33 Pout and drain efficiency simulation result for 3.4 GHz with EM

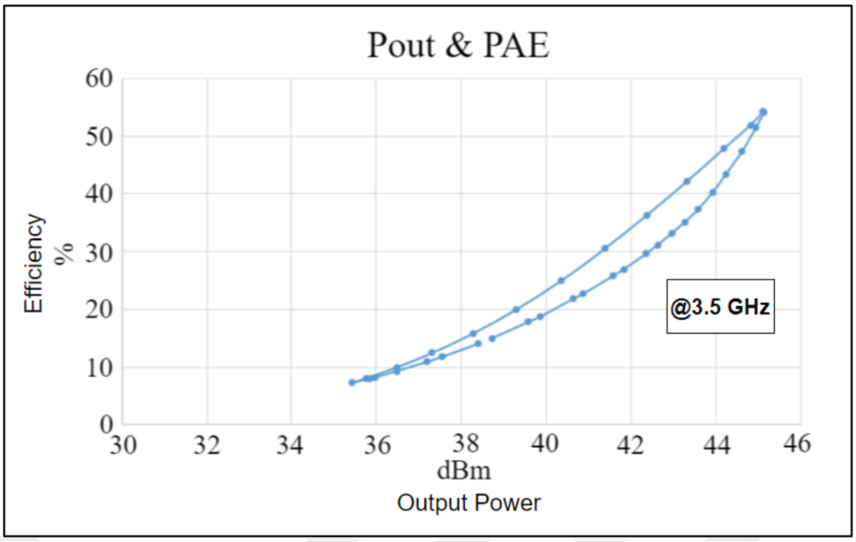

Figure 4.34 Pout and PAE simulation result for 3.5 GHz with EM

4.5. REALIZATION AND MEASUREMENT

The outphasing power amplifier which simulation is performed is fabricated. In this implementation, the PCB of amplifier is drawing with Altium Designer. First, a schematic drawing of this is made according to the simulation schematic and then the PCB drawing is started. Figure 4.35 is the drawn PCB. Combiner and OMN circuits are indicated with blue box. Voltage pads required for the bias of transistor and inputs-output ports are shown in the figure. The PCB shown in the figures is realized in the laboratory environment with Tron Elektronik Sistemler and typesetting is done. The prepared circuit is measured with the facilities of Maury Microwave Corporation.

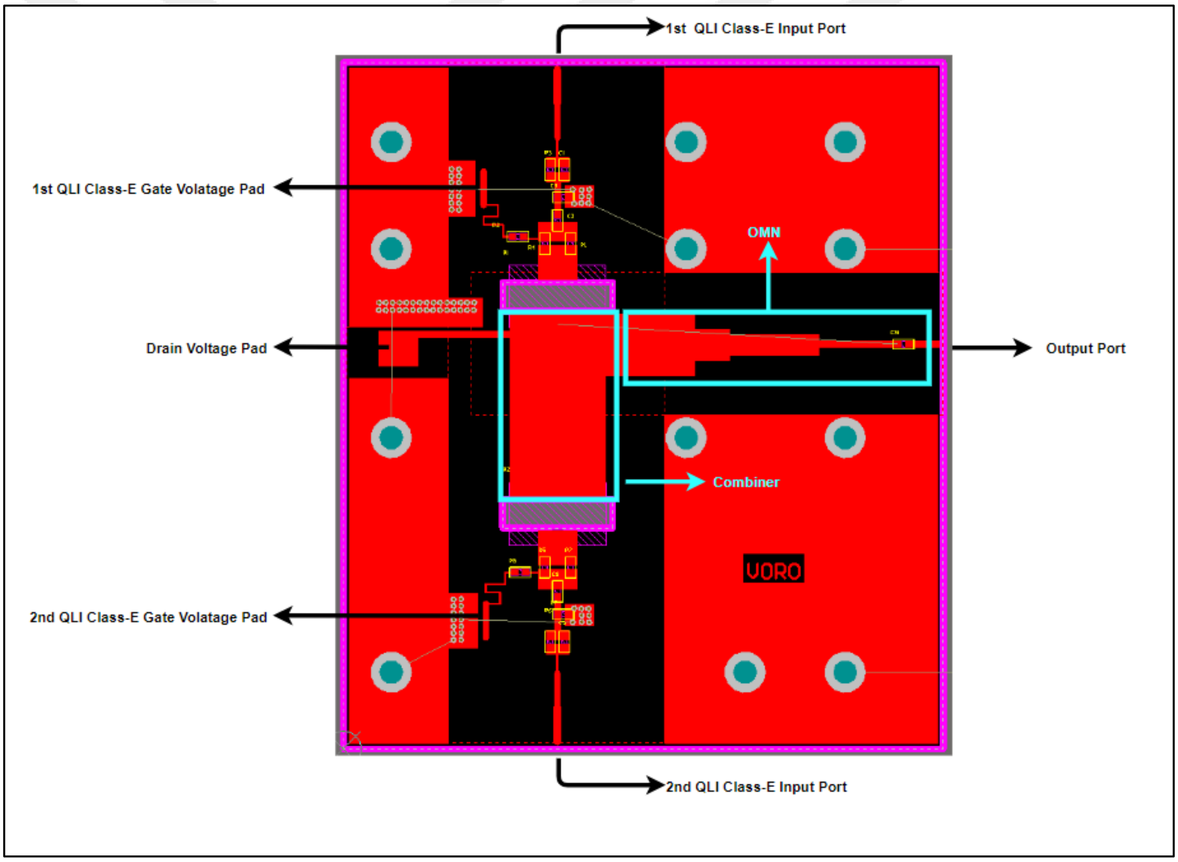

Figure 4.35 2-dimensional PCB drawing of outphasing power amplifier

With the support from Maury Microwave Corporation, a test mechanism that automates the change of phase difference is established and outphasing behaviour of the circuit is measured. To measure this behaviour, two signal generators that can be phase differences are required. When two phase-different signals are created, these signals are amplified to the desired power with the same identical bench type amplifier. These signals are applied separately to the inputs of the designed amplifier. The output power is measured at the output port and drain efficiency is calculated according to the output power. Figure 4.36 is the measurement setup photo and Figure 4.37 is the measurement block diagram. DUT in Figure 4.37 represents the designed outphasing power amplifier. The load tuner at the output provides that the output of the amplifier is transformed to the desired impedance.

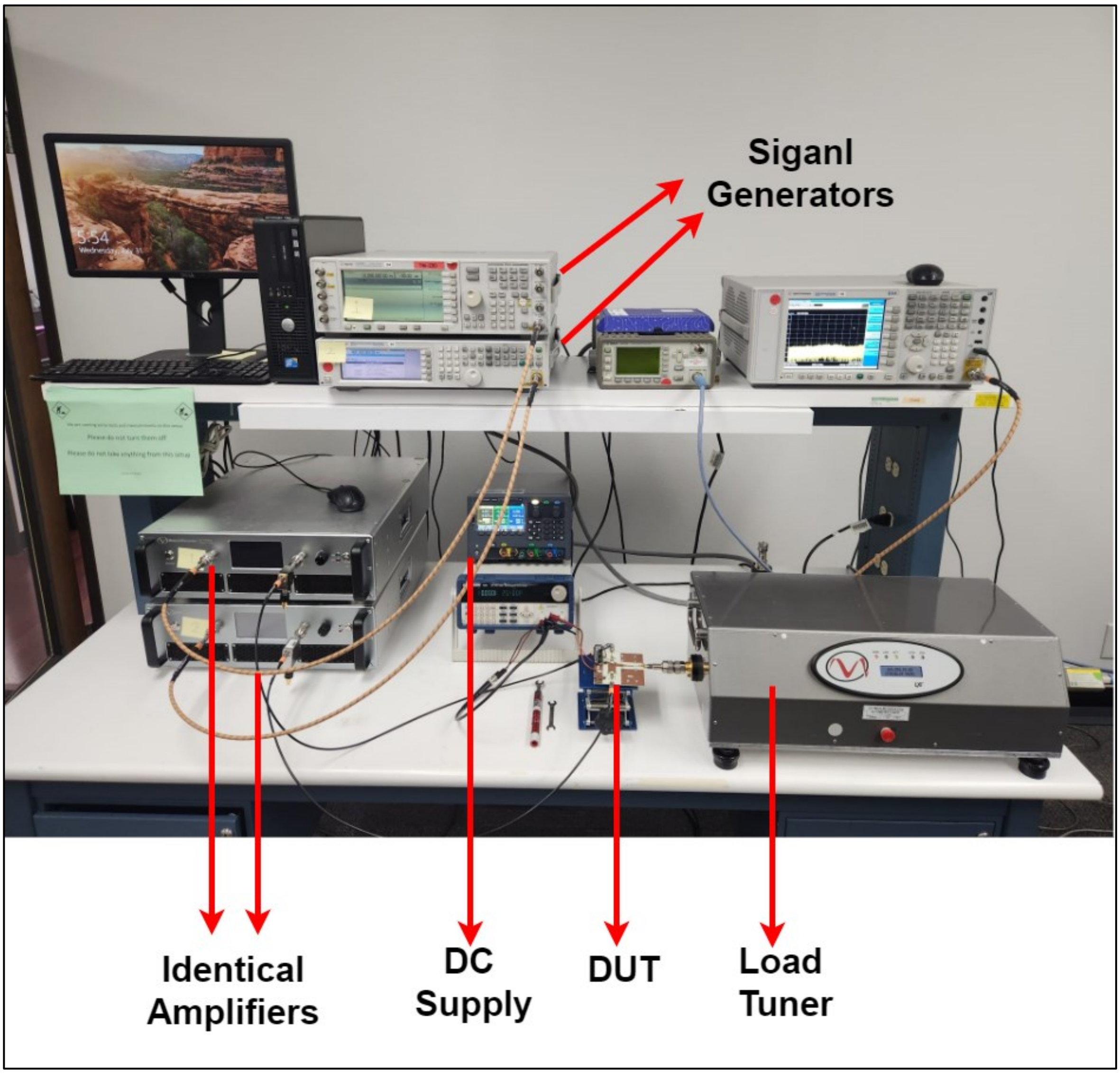

Figure 4.36 Outphasing behavior measurement setup

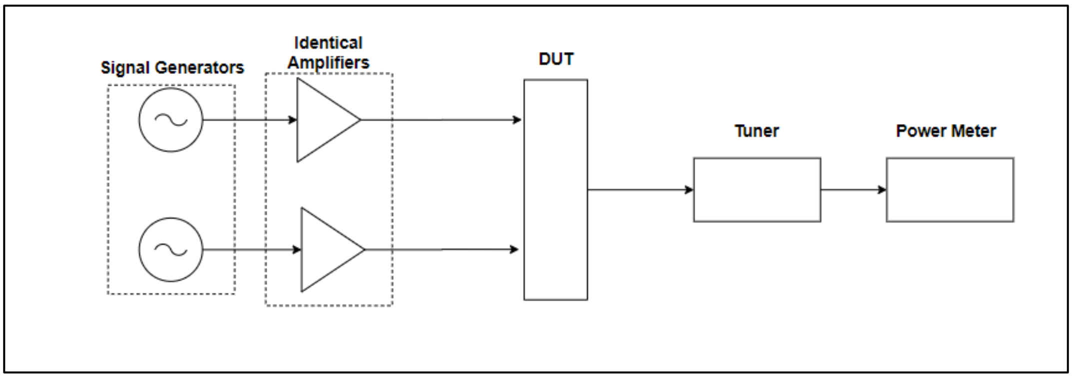

Figure 4.37 Outphasing behavior measurement setup block diagram

Measurement results obtained with this setup are shown between Figure 4.38-Figure 4.41. These measurements were made at 3.5 GHz. Figure 4.38 shows the output power and drain efficiency measurement results when the input power level of the realized circuit is 38 dBm. As can be seen in the figure, the output power and drain efficiency change according to the phase difference of the signal generators. The efficiency of this realized filter is almost 50% when the output power is above 44 dBm.

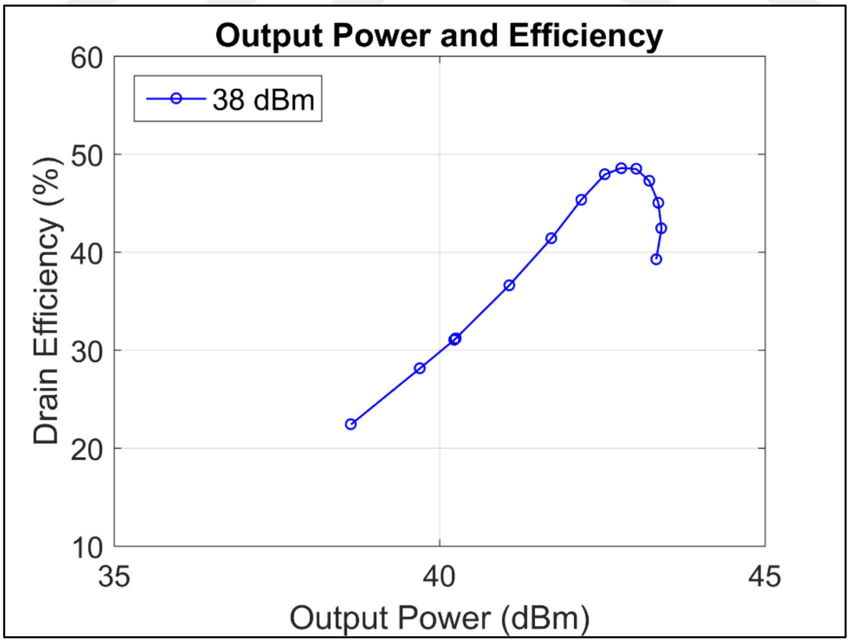

Figure 4.38 Input power 38 dBm measurement results

Figure 4.39 shows the measurement results of the circuit when it is driven different input power levels. The gain value of the circuit is shown in the Figure 4.40 according to these input power levels.

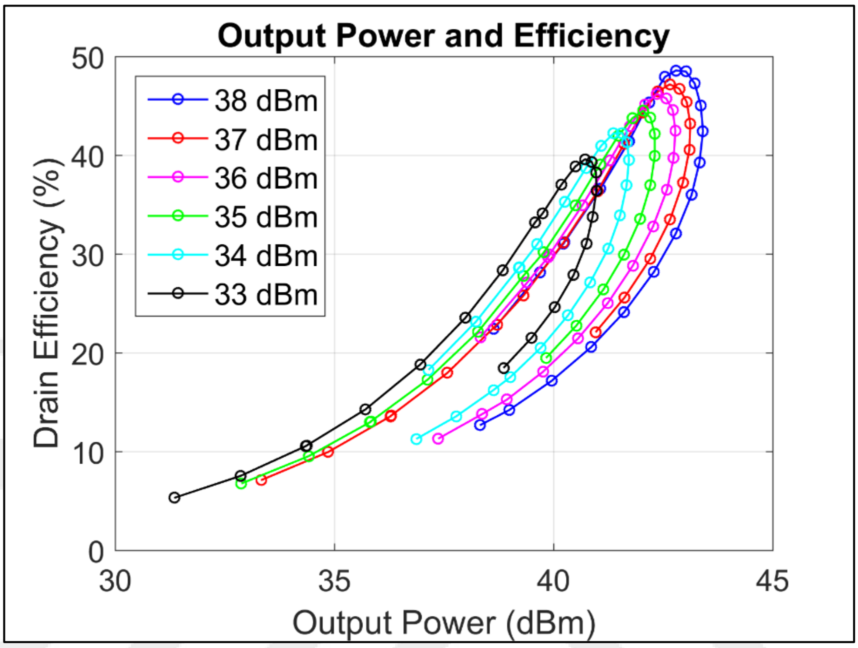

Figure 4.39 Output power and drain efficiency measurement results according to different input power levels

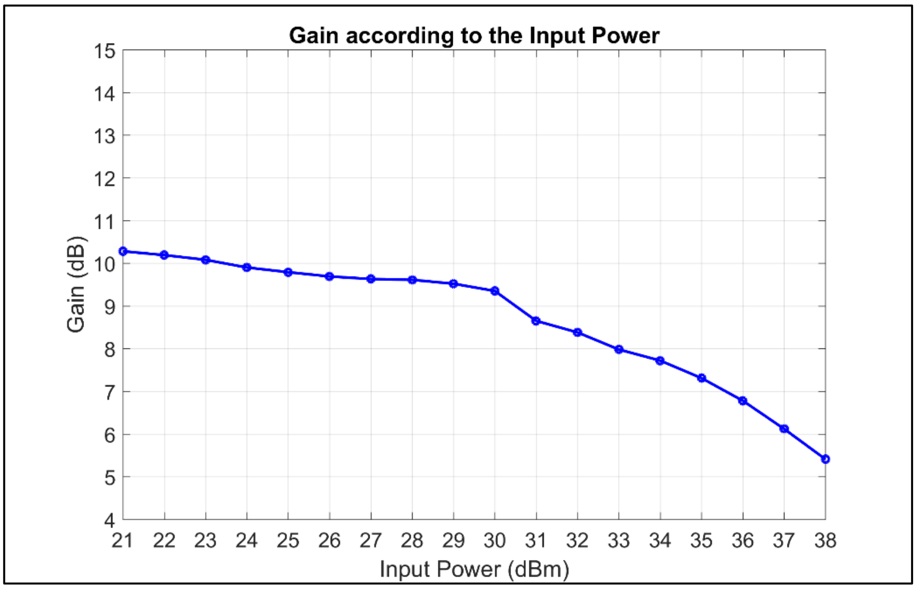

Figure 4.40 Gain according to the input power level

As can be seen in Figure 4.40, the gain value is almost 10 dB when the circuit is driven with 20 dBm input signal. The gain value goes down with increasing input power level. The drain efficiency according to the input power can be seen in Figure 4.41. It is observed that the circuit has an efficiency almost 50% when it driven with 38 dBm.

Figure 4.41 shows the drain efficiency measurement result of realized circuit according to the input power. It can be seen that the drain efficiency remains above 40%, even if the input power drops by 6 dB.

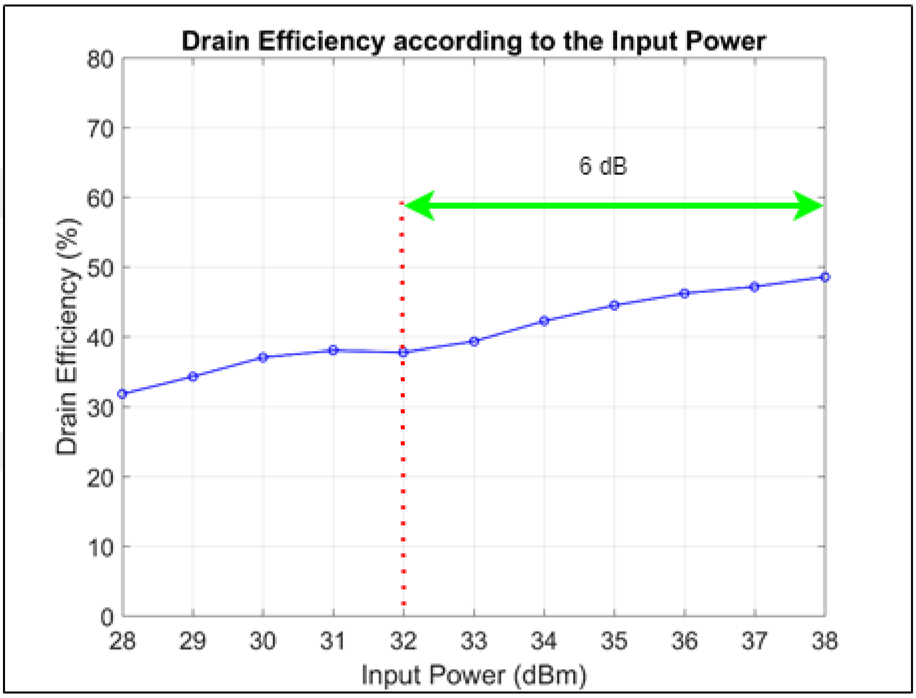

Figure 4.41 Measurement result of drain efficiency according to the input power

5. CONCLUSION

The importance of power amplifiers increases with the development of communication systems. The increasing bandwidth used in communication systems and the development of modulation types make it difficult for single-transistor amplifiers. When the linearity of the signal to be transmitted is desired to preserve, the current drawn by power amplifiers is increased. This causes the system to work inefficiently and generate heat. These disadvantages can be solved with load-modulated amplifiers. Maintaining efficiency, especially in the low power range, can be achieved with load-modulated amplifiers. Doherty, balanced, and outphasing are some of the modulated amplifier topologies. Doherty amplifiers are commonly used in the industry for their ability to achieve high efficiency with modulated signals. However, their complicated output network requirements can limit their use in wideband applications. Balanced amplifiers, while effective, require an extra control source for load impedance and their inherent nonlinearity can pose challenges for wideband signals. The outphasing structure is simpler to realize because the structure is formed by combining two identical amplifiers. These amplifiers process the input signal in different phases to provide power output, reducing energy losses in the process. Thanks to the fast-switching elements used, they can transmit high-quality signals with lower heat generation. This technology is widely used in radio communication and professional audio systems, offering effective performance across a broad frequency range. The outphasing architecture provides significant advantages, especially in applications with high power requirements.

In this thesis, an outphasing structure design is made for sub-6GHz 5G communication systems. The amplifier used in this design is a QLI Class-E. It has been proven that this type of amplifiers is suitable for load modulation. That is why we start with the amplifier design first. Literature studies have determined that the optimal value for load modulation is 1.3 times the 'q' value. With this value, it is observed that the amplifier is not affected even if the load value doubles or is decreased by half. For this reason, an amplifier design with a q value of 1.3 defined in the thesis is made with the selected transistor. The parasitic capacitance of the transistor is used for this and by calculating the appropriate L value, output power and efficiency simulations are done under load change. This L value is added to the circuit as a transmission line and the same analysis is performed again.

Then, the combiner circuit that combines the amplifiers is designed. With this circuit, it is analyzed how the phase change will affect the load. With this design, it is observed that the phase difference of the circuit and the impedance value are brought to the real axis. This circuit is analyzed first according to its electrical length and then its physical length. After these simulations, the 50 Ω impedance matching circuit of the circuit is designed.

All circuits are combined and the change in output power and efficiency according to the phase is observed. Simulations are performed at 3.4 and 3.5 GHz and results are presented. By adding 3D EM solutions of coupling and impedance matching circuits to the circuit, the simulation is made again, and the results are shared. The simulated circuit is produced in a laboratory environment and a mechanism is set up to measure the outphasing behaviour. Measurements are taken according to various input powers and results are shared.

The simulation results show that the output power and efficiency of the designed structure can be controlled with the phase differences between two signal generators. In the simulation results, the designed outphasing amplifier provides 44 dBm output power with 50% drain efficiency at 3.5 GHz. Also, its drain efficiency is higher than 40% even if its input power level is reduced by 6 dB. That means the designed structure has a 6 dB back-off value.

When the designed structure was implemented according to the simulations, 50% drain efficiency was achieved at 44 dBm output power and the same efficiency values can be provided with 6dB back-off value. It is also shown that the output power and efficiency are controlled with the phase difference. In the measurements, it is observed that the realized circuit provides similar curves at different input power levels. The difference between the simulation and measurement results are the input power of the outphasing amplifier. This difference is due the gain value of the realized circuit. It can be concluded that the values will approach each other with the gain.

This study can be improved with taking measurement at different loads, the matching networks can be amended, or these networks can be optimized by taking measurement at various frequencies. The effect of these networks on the outphasing structures can be observed by ignoring these networks. As a continuation of this study, the model of the selected transistor can be created. This allows for a closer approximation to realistic results for simulations and improves the performance of the circuit. In addition, the q value can be selected to have different values and its effects can be investigated.

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