ANKARA YILDIRIM BEYAZIT UNIVERSITY

GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

ACTIVE PACKAGE TO CELL BALANCING BATTERY MANAGEMENT SYSTEM WITH ISOLATED ĆUK CONVERTER AND SWITCH MATRIX

M.Sc. Thesis by

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July, 2024

ANKARA

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A Thesis Submitted to

The Graduate School of Natural and Applied Sciences of

Ankara Yıldırım Beyazıt University

In Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical and Electronics Engineering, Department of Electrical and Electronics Engineering

by

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July, 2024

ANKARA

M.Sc. THESIS EXAMINATION RESULT FORM

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ACKNOWLEDGMENTS

Firstly, I would like to express my sincere gratitude to my supervisor, Prof. Dr. Ahmet KARAARSLAN for his tremendous support and motivation during my study. His immense knowledge and precious recommendations constituted the milestones of this study. His guidance assisted me all the time of my research and while writing this thesis.

2024, 31 July **Alperen UĞURLUOĞLU**

ACTIVE PACKAGE TO CELL BALANCING BATTERY MANAGEMENT SYSTEM WITH ISOLATED ĆUK CONVERTER AND SWITCH MATRIX

ABSTRACT

Battery Management System (BMS) is applied to battery packs to monitor the voltage, current, temperature, and State of Charge (SoC) values of each cell and provide the battery pack to operate in a safe zone. One of the battery problems is that each battery cell in the pack does not contribute energy equally to the entire pack. Li-ion batteries that are used in this paper also suffer from this problem due to their higher energy density than other batteries. Therefore, a balancing operation is needed for the voltage and SoC of each cell.

In this paper, a faster active package-to-cell (P2C) balancing by using a BMS that has an isolated ĆUK converter (IĆC) and a switch matrix is proposed. The proposed BMS draws energy from the entire pack and balances the lower energized cells by converting the energy through a high-power capable IĆC and a cell-selective switch matrix (SWM) that enables the selection of one cell or up to four cells in a row. Due to the isolation, the energy can be transferred from pack to cell, and thanks to the switch matrix, it is possible to reach each cell individually. In addition, the BMS controller has a PI controller for IĆC and a cell-selective algorithm (CSA) for the switch matrix. Also, the proposed study provides a cost-effective and compact solution as compared with other P2C topologies.

Keywords: BMS, cell balancing, package to cell, isolated ĆUK converter, switch matrix

ANAHTAR MATRİKS VE İZOLE ĆUK DÖNÜŞTÜRÜCÜ İLE AKTİF PAKETTEN HÜCREYE DENGELEYEN BATARYA YÖNETİM SİSTEMİ

ÖZ

Batarya Yönetim Sistemi (BMS), her bir hücrenin voltaj, akım, sıcaklık ve Şarj Durumu (SoC) değerlerini izlemek ve batarya paketinin güvenli bölgede çalışmasını sağlamak için batarya gruplarına uygulanmaktadır. Pil problemlerinden biri, paketteki her bir pil hücresinin tüm pakete eşit olarak enerji vermemesidir. Bu makalede kullanılan Li-ion piller de diğer pillere göre daha yüksek enerji yoğunluğu nedeniyle bu sorundan mustariptir. Bu nedenle, her bir hücrenin voltajı ve SoC'si için bir dengeleme işlemine ihtiyaç vardır.

Bu makalede, İzole ĆUK Dönüştürücü (IĆC) ve bir anahtar matrisi kullanarak batarya hücrelerini dengeleyen daha hızlı bir aktif paketten hücreye (P2C) BMS önerilmektedir. Önerilen BMS, tüm paketten enerji çeker ve enerjiyi IĆC aracılığıyla dönüştürerek ve anahtar matrisi ile ilgili hücreleri seçerek daha düşük enerjili hücreleri dengeler. İzolasyon sayesinde enerji paketten hücrelere aktarılabilir ve anahtar matrisi sayesinde her hücreye ayrı ayrı ulaşmak mümkündür. Ek olarak, BMS denetleyicisi, IĆC için PI denetleyicisine ve anahtar matrisi için bir anahtarlama algoritmasına sahiptir. Ayrıca önerilen çalışma, diğer P2C topolojileriyle karşılaştırıldığında uygun maliyetli ve kompakt bir çözüm sunmaktadır.

Anahtar Kelimeler: BMS, hücre dengeleme, paketten hücreye, izole ĆUK dönüştürücü, anahtar matrisi

CONTENTS

NOMENCLATURE

Roman Letter Symbols

A	Current
B	Magnetic Flux Density
C	Capacitance
D	Duty Ratio
f	Frequency
F	Farad
H	Henry
I	Current
k	Kilo
L	Inductance
m	Milli
R	Resistance
T	Period
V	Voltage
Z	Impedance

Greek Letter Symbols

Δ	Difference
ε	State of Charge Difference
ϕ	Magnetic Flux
μ	Magnetic Permeability
μ	Micro
η	Efficiency
$\Re$	Reluctance
Ω	Ohm

Subscripts

max	Maximum
min	Minimum
Sim	Simulation
Exp	Experimental

Acronyms

Ah	Ampere hour
BMS	Battery Management System
C2C	Cell to Cell
C2P	Cell to Pack
CSA	Cell Selective Algorithm
DC	Direct Current
DoD	Depth of Discharge
EV	Electric Vehicle
EN	Enable
EoL	End of Life
ESR	Equivalent Series Resistance
FLC	Fuzzy Logic Controller
GA	Genetic Algorithm
Hz	Hertz
KCL	Kirchoff's Current Law
KF	Kalman Filter
KVL	Kirchoff's Voltage Law
MCU	Micro-Controller Unit
MPC	Model Predictive Control
MOSFET	Metal-Oxide Silicon Field Effect Transistor
NN	Neural Network
OCC	One Cycle Control
OCV	Open Circuit Voltage
IĆC	Isolated ĆUK Controller
P2C	Pack to Cell
PID	Proportion-Integration-Derivation
PWM	Pulse Width Modulation
RC	Resistor-Capacitor
SoC	State of Charge
SoH	State of Health
SMC	Sliding Mode Control
SWM	Switch Matrix
UART	Universal Asynchronous Receiver-Transmitter

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CHAPTER 1

INTRODUCTION

The studies on electrical energy storage systems have great importance. Electric energy storage systems are widely used in the fields of energy, electric vehicles, marine vehicles, aerospace, and industrial areas [1-2]. The rechargeable batteries are massively used to store the electrical energy, and lead, nickel, sodium or lithium electrochemistry is used to produce rechargeable batteries [3]. However, these rechargeable batteries might have some problems if they are not monitored and controlled. In an ideal situation, each battery cell in the pack contributes equally to the entire pack, but not all battery cells are the same in a real situation, as illustrated in Figure 1.1. Even though battery cells have the same physical size, shape, chemistry, and weight, their total capacity, self-discharge rate, internal resistance, and amount of aging can differ [4]. These differences cause the battery packs to perform less than their full capacity and causes a huge challenge to battery cell lifetimes. Therefore, the performance of the battery pack is limited by the lowest capacity cell in the pack, and some of the energy stored in other batteries remains dead energy because once the energy in the weakest cell is depleted, the entire pack is effectively depleted [5].

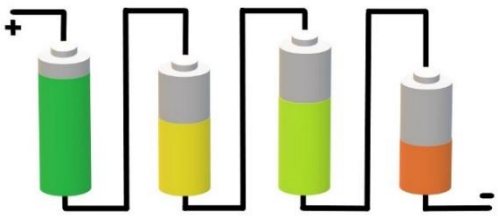


Figure 1.1 Battery charge and capacity

On the other hand, BMS is used to bring battery cells with different capacities and charge-discharge characteristics to a balanced energy level for maximizing battery pack health. Hence, BMS makes voltage, current, and temperature measurements on the battery packs, and if these measurements are above the values determined for the battery operating range, it intervenes to operate the battery pack in the safe

zone. BMS has data monitoring, calculation, protection and optimization features. Battery packs consist of cells connected in series or parallel, so there are different types of BMS for different structures [6].

1.1 Batteries

Lead, nickel, and lithium materials are mostly utilized as electrochemicals to produce rechargeable batteries. However, each material used in a battery cell produces a different cell voltage, energy density, life cycle, efficiency, cost, operating temperature range, capacity, power output, and charge/discharge state. Therefore, Table 1.1 compares these materials and provides further explanations in the next sections.

Table 1.1 Battery types and characteristics

Chemistry	**Cell Voltage (V)**	**Specific Energy (Wh/kg)**	**Life Cycle**	**η (%)**	**Cost ($)**	**Operating Temperature (℃)**
Lead-Acid [7-8]	2.2	20-100	300-400	70-85	Medium	-30 to +60
Ni-Cd [7-8]	1.2	40-100	1300-1600	75-85	High	+15 to +35
Ni-MH [7-8]	1.2	80-140	500-800	75-95	High	+10 to +40
$Li_4Ti_5O_{12}$ (LTO) [9-10]	2.3	140-380	1500	95-99	Medium	-30 to +60
$LiFePO_4$ (LFP) [9-10]	3.25	140-380	2000	95-99	Medium	-20 to +60
$LiCoO_2$ (LCO) [9-10]	3.6	140-380	1000	95-99	Medium	-20 to +60
$LiNiCoAlO_2$ (NCA) [9-10]	3.6	140-380	1500	95-99	Medium	-20 to +60
$LiNiO_2$ (LNO) [9-10]	3.6	140-380	1500	95-99	Medium	-20 to +60

$LiNiMnCoO_2$ $LiMnCoO_2$ (NMC) [9-10]	3.65	140-380	2000	95-99	Medium	-20 to +60
$LiMn_2O_4$ (LMO) [9-10]	3.75	140-380	1500	95-99	Medium	-20 to +60
$LiCoPO_4$ (LCP) [9-10]	4.7	140-380	1500	95-99	Medium	-20 to +60
Li-S [7-10,19]	1.7	200-600	1500	70-95	Low	0 to +80
Li-air [7-10,20]	2.67	340-760	100	-	Low	+10 to +40

1.1.1 Calculation of Battery Parameters

The batteries have the following parameters: OCV, internal resistance, SoC, DoD, SoH, capacity, coulombic efficiency, energy, and specific energy parameters. While charging a battery cell, the OCV and SoC levels increase, and the DoD level decreases. While discharging a battery cell, the OCV and SoC levels decrease, and the DoD level increases. These parameters are calculated with the equations below as described in reference [10] and the standards of IEEE 1625:2008 [11], IEC 60086-4:2019 [12], UL-1642 [13] and UL-2596 [14] for industrial applications, MIL-PRF-81757D [15] and MIL-PRF-29595A [16] for military and DO-293A [17] and DO-311A [18] for aviation.

The OCV of the batteries is simply equal to the measured voltage, $V_{measured}$, minus the magnitude of the voltage drop, as given in equation 1.1.

$$OCV_{cell}[V] = V_{measured}[V] - I_{cell} * R_{internal}[V] \quad \textbf{(1.1)}$$

On the other hand, the internal resistance of the battery cells is not initially known. Therefore, the battery cells can be charged or discharged with two different current values to obtain the value of internal resistance by applying equation 1.2.

$$R_{internal} = (V_1 - V_2\,[V])/(I_1 - I_2\,[A]) \quad \textbf{(1.2)}$$

The SoC value of a battery cell can be obtained by applying the methods that are described in Section 1.4. Equations 1.3 and 1.4 provide a representation of the SoC.

$$SoC_{cell}(\%) = \left(1 - \frac{DoD_{cell}\,[Ah]}{Capacity\,[Ah]}\right) * 100\% \quad \textbf{(1.3)}$$

$$SoC_{cell}(t)[\%] = SoC_{cell}(0)[\%] - \int_0^t \frac{I_{cell}(t)[A]*dt}{Capacity\,[Ah]} * 100[\%] \quad \textbf{(1.4)}$$

The DoD indicates the extent of a battery cell's discharge. Therefore, the DoD value can be experimentally obtained by discharging a cell from its maximum voltage level to its minimum voltage level with a constant current, or it can be calculated by simply using equation 1.5.

$$DoD_{cell}[\%] = 1 - SoC_{cell}[Ah] \quad \textbf{(1.5)}$$

Each battery cell has a rated capacity value in Ah that is defined by the manufacturer. However, the capacity of battery cells drops below the rated capacity during their lives. Finally, the battery cells are counted as dead when the battery capacity reaches a predefined level of end of life (EoL) capacity. Thus, the SoH level of a battery cell is calculated using equation 1.6. Simply put, the maximum storable charge capacity divided by the rated capacity is the SoH value of the battery cell.

$$SoH_{cell}[\%] = \frac{(Capacith_{max} - Capacith_{EoL})[Ah]}{(Capacith_{rated} - Capacith_{EoL})[Ah]} * 100\ [\%] \quad \textbf{(1.6)}$$

The capacity is defined as the magnitude of current output that is constantly obtained for an hour. Therefore, the capacity can be obtained by charging or discharging a cell from its maximum voltage level to its minimum voltage level with a constant current. After the charging or discharging operation is completed, the current times the operation hour give the battery cell capacity, as shown in equation 1.7.

$$Capacity_{cell}[Ah] = Current_{cell}[A] * \text{Time}[h] \quad \textbf{(1.7)}$$

Coulombic efficiency describes how much charge is extracted starting from an initial SoC level, as given in equation 1.8.

$$Coulombic\ Eff_{cell}[\%] = 100[\%] * Charge_{out}[Ah]/Charge_{in}[Ah] \quad \textbf{(1.8)}$$

The energy stored in a battery cell can be calculated using equation 1.9.

$$Energy_{cell}\ [Wh] = V_{cell}[V] * Capacity_{cell}[Ah] \quad \textbf{(1.9)}$$

The specific energy of a battery cell means how much electrical energy can be stored per kg of a cell, as given in equation 1.10.

$$Specific\ Energy_{cell}\ [Wh/kg] = Energy_{cell}\ [Wh] * Mass_{cell}[kg] \quad \textbf{(1.10)}$$

1.1.2 Lead-Acid Batteries

As given in the aviation standard of RTCA DO-293A [17] and the military standard of MIL-PRF-81757D [15], the nominal cell voltage of lead-acid batteries is 2.0 V. Generally, six cells are connected in series for a 12V battery pack. The lead-acid batteries are reliable against thermal runaway. Their energy density is low due to the weight, but the cost is low, as well. They have a medium level life cycle as compared with Ni-Cd and Li-ion [7].

1.1.3 Nickel Based Batteries

As given in the aviation standard of RTCA DO-293A [17] and the military standard of MIL-PRF-81757D [15], Ni-Cd and Ni-MH batteries have nominal a 1.2 V cell voltage. They are reliable against thermal runaway. The energy density is higher than lead-acid, but the cost is high, as well. They have a lower level of life cycle due to the memory effects as compared with Li-ion and Li-S [8].

1.1.4 Lithium Ion (Li-Ion) Batteries

Lithium-ion batteries are the most preferred type because they have important advantages such as high rated voltage, high energy density, long life, and no memory effect. On the other hand, they might have thermal runaway and ignition risks as given in reference [11] and the industrial standards of IEC 60086-4:2019 [12] and UL-1642 [13], the military standard of MIL-PRF-29595A [16], and the

aviation standard of DO-311A [18]. In the literature, there are several types of lithium-ion electrochemistry that are coded as LTO, LFP, LCO, NCA, LNO, NMC, LMO, and LCP. The LCO batteries have medium level of energy density, but their life cycle is the lowest, and the thermal runaway risk is higher among the lithium-ion batteries. The LTO and LMO batteries offer high power, low risk of thermal runaway, and 1500 cycles of life when charged from %20 to %80. However, it has a lower energy density than Li-ion batteries. The LFP batteries provide 2000 cycles of life and a low risk of thermal runaway, but their energy density is lower than the NCA and NMC batteries. The NCA and NMC batteries are the recently introduced methods, so they have the highest energy density, The NCA batteries provide 1500 cycles of life, while the NMC batteries provide up to 2000 cycles of life. Therefore, these batteries dominate EV applications. On the other hand, their thermal runaway risk is moderate [9-10].

1.1.5 Lithium Based Batteries for Future Work

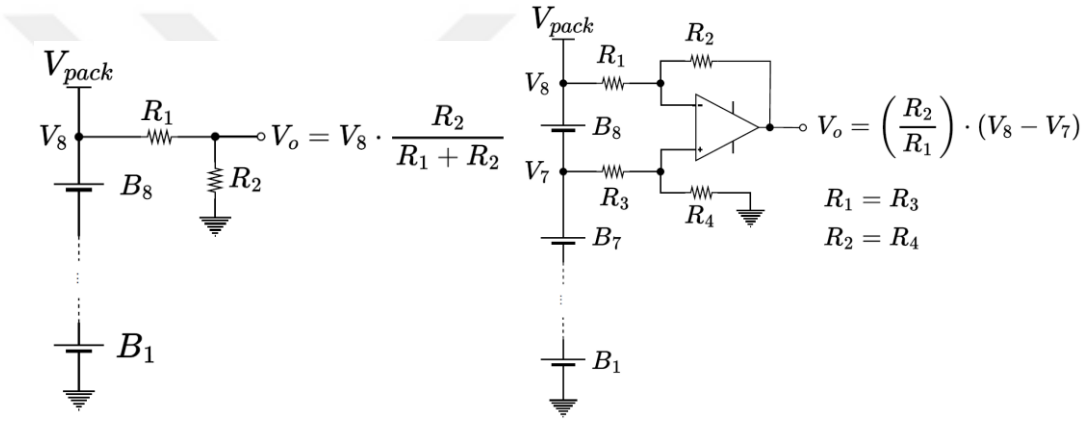
Lithium-sulfur (Li-S) and lithium-air (Li-air) batteries are recently researched types of lithium-based cells in the literature. Their energy density is the highest among all batteries in literature. The Li-S batteries reach up to 600 Wh/kg energy density with a 1.7 nominal voltage, as reported in the literature. The Li-S batteries have almost the same life cycle as Li-ion batteries. The efficiency of these battery types offers an efficiency range of 70-95 %. Moreover, the low cost and higher operating temperature are reported. On the other hand, Lithium-air (Li-air) batteries recorded a much higher energy density of up to 760 Wh/kg with a 2.67 V in the literature. However, 100 cycles of life are achieved at maximum by charging from %20 SoC to %80 SoC and are still the subject of research to advance the life cycle [19-21].

1.2 Cell Monitoring Methods

Monitoring the battery cell voltages, currents, and temperature is crucial for every BMS because the battery health and state of charge are calculated to find out the battery state. Also, the obtained operational temperature of batteries helps to take precautions against the risk of thermal runaway.

1.2.1 Voltage Measurement

In recent studies, the resistive voltage divider circuit and differential voltage measurement circuit have been seen for voltage measurement purposes. The circuits are given in Figure 1.2. The resistive divider circuit is more simple and smaller in size, but the sensitivity gets lower and lower when the high-side battery cell voltages are measured in series connected battery cells [22]. On the other hand, the differential voltage measurement circuits enable high sensitivity while monitoring any cell in a series of connected battery cells. Even if this method is a bit more complex and larger in size, the effectiveness of this circuit is high enough to tolerate these drawbacks [23].



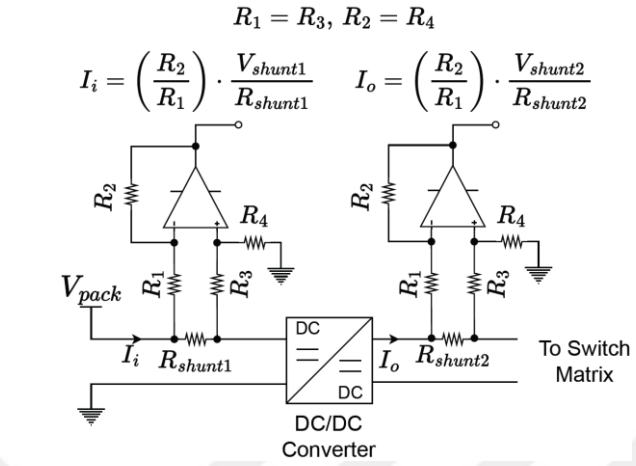
(a) (b)

Figure 1.2 (a) Resistive voltage divider measurement method, (b) differential voltage measurement method

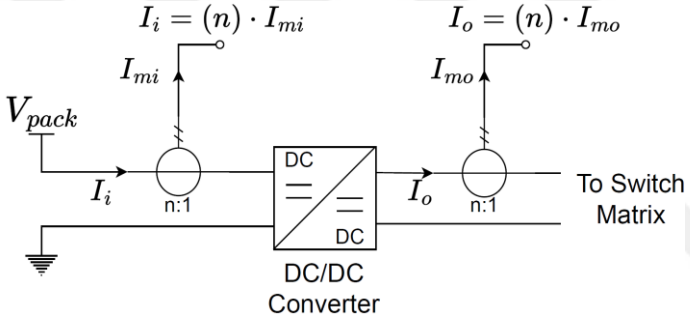
1.2.2 Current Measurement

Since the batteries are charged or discharged on required occasions, current monitoring is required for overcurrent protection and state of charge estimations [24]. The current can be measured by shunt resistors, current transformers, and hall effect based sensors as shown in Figure 1.3. The shunt resistor circuit is used with OPAMP circuits and provides a cheaper and more precise solution. However, this method causes power loss, and no isolation is provided. Another method of current transformers is an isolated and precise sensor, but they are chunky, and their cost is very high, so the current transformers are more effective for high current measurements. The hall effect sensors are isolated, precise, and

simple solution for current measurements. Also, the cost and size are tolerable given the effectiveness of the current measurement in BMS.



(a)



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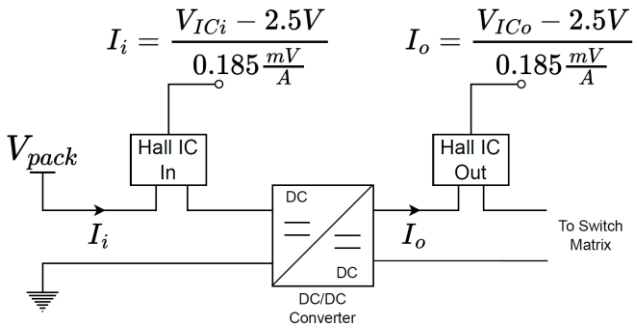


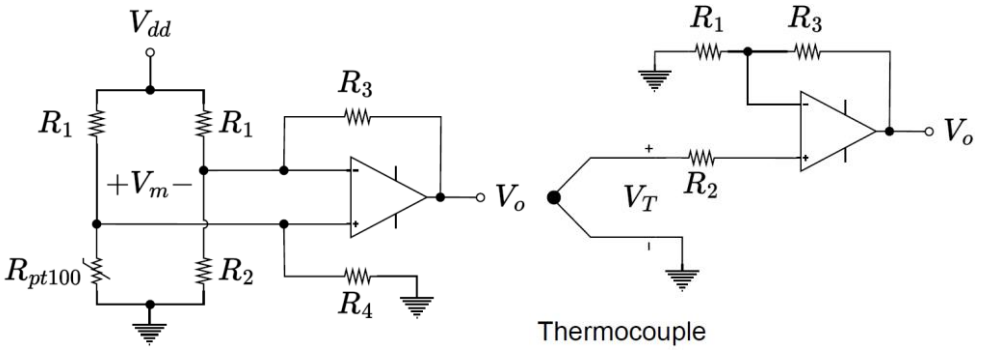
(c)

Figure 1.3 (a) Shunt resistor based current measurement method, (b) current transformer method, (c) hall effect based current measurement method

1.2.3 Temperature Measurement

The temperature of battery cells can be measured with PT100 sensors and thermocouples [25]. PT100 sensors use the change of resistance against temperature change, and thermocouples use the change of voltage against

temperature. Both sensor outputs are measured with OPAMP circuits, and both sensors can be used in BMS topologies. The circuits of the sensors are shown in Figure 1.4.



(a) (b)

Figure 1.4 (a) PT100 measurement method, (b) thermocouple measurement method

1.3 Cell Balancing Methods in Literature

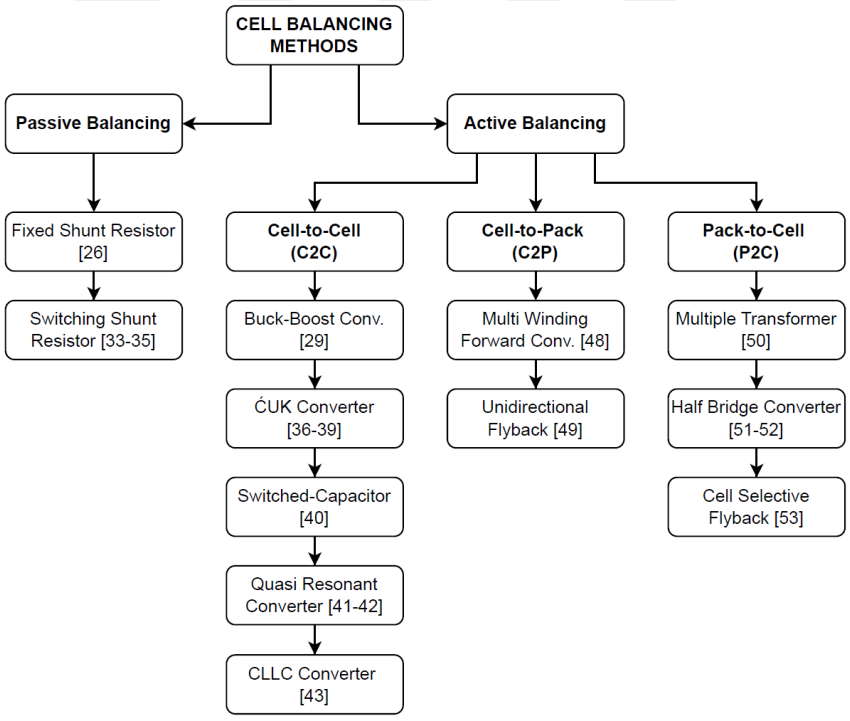


Figure 1.5 Cell balancing methods chart

Cell balancing operation is a process of equalizing the voltage and SoC between the cells of battery packs due to the differences in characteristics between battery cells. The importance of cell balancing is for better battery pack performance and battery health [26-28]. Battery balancing methods are divided into passive

balancing and active balancing. Various methods are introduced and applied to achieve charge balancing between the battery cells. The literature essentially discusses active and passive balancing methods, as represented in Figure 1.5 [29-32].

1.3.1 Passive Cell Balancing

There are fixed shunt and shunt switched resistor topologies as passive balancing methods in the literature [26, 33-35]. The passive cell balancing methods are easy to implement and quite low cost compared to the other active cell balancing methods. With this method, the cells with excess energy are discharged with a bypass resistor, which consumes excess energy as heat until their charge matches that of those with less energy. There is no energy transfer between cells, excess energy is spent on a resistor. Therefore, the efficiency becomes zero, the need for thermal management increases, and the cell balancing takes time to finish.

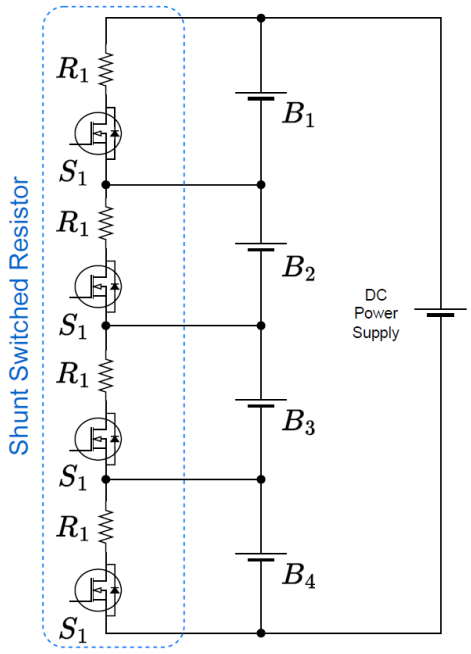


Figure 1.6 Shunt switched resistor topology

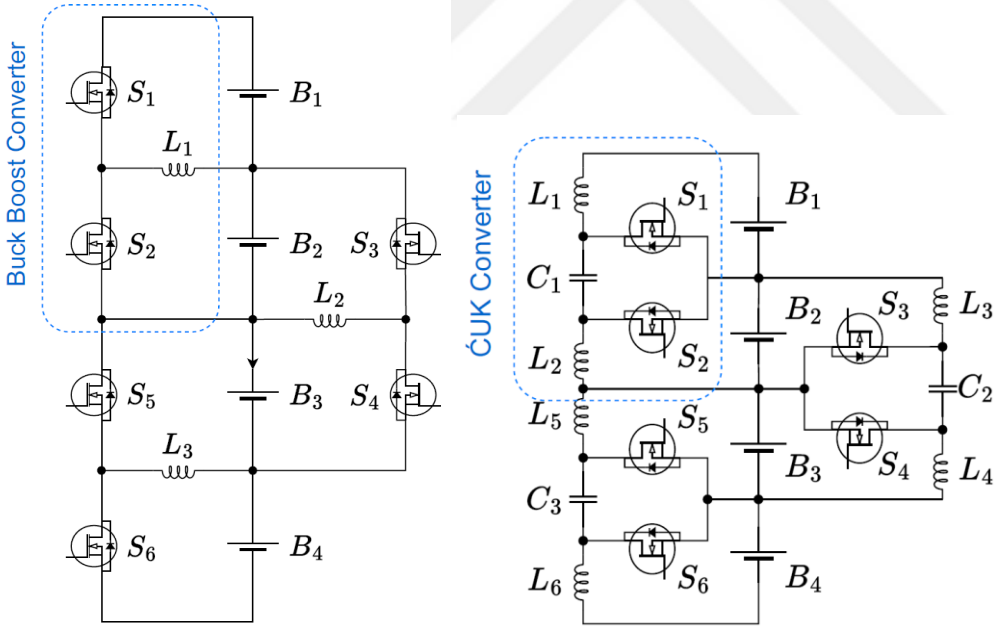
1.3.2 Active Cell Balancing

Active cell balancing techniques use the capacitive or inductive charging method to transfer charge from a high-charged cell to a low-charged cell. So, the active

balancing methods provide faster balancing operations, enhanced efficiency due to charge transfer and reduced heat issues due to the absence of shunt resistors. Active balancing methods are cell-to-cell (C2C), cell-to-package (C2P), and package-to-cell (P2C) in the literature [34].

1.3.2.1 Cell to Cell (C2C)

In the literature, switched capacitor, ĆUK converter, and quasi-resonant converter topologies are examples of C2C studies [29, 36-43]. In C2C studies, the excess charge is transferred from high-charged cells to low-charged cells, such as any-cell to any-cell or adjacent-cells to adjacent-cells. The C2C methods are sufficiently fast and extremely efficient. Nevertheless, the C2C topologies are highly complex due to the large number of switching components and passive elements. Consequently, the cost and size of these topologies increase significantly.



(a) (b)

Figure 1.7 (a) Buck-boost converter topology, (b) ĆUK converter topology

Buck Boost Converter and ĆUK Converter methods are illustrated in Figure 1.7. The converters provide the energy transfer. The low-charged cells are balanced, or the energy of the high-charged cells can be dissipated with the adjacent cells, and vice versa [29, 36-39].

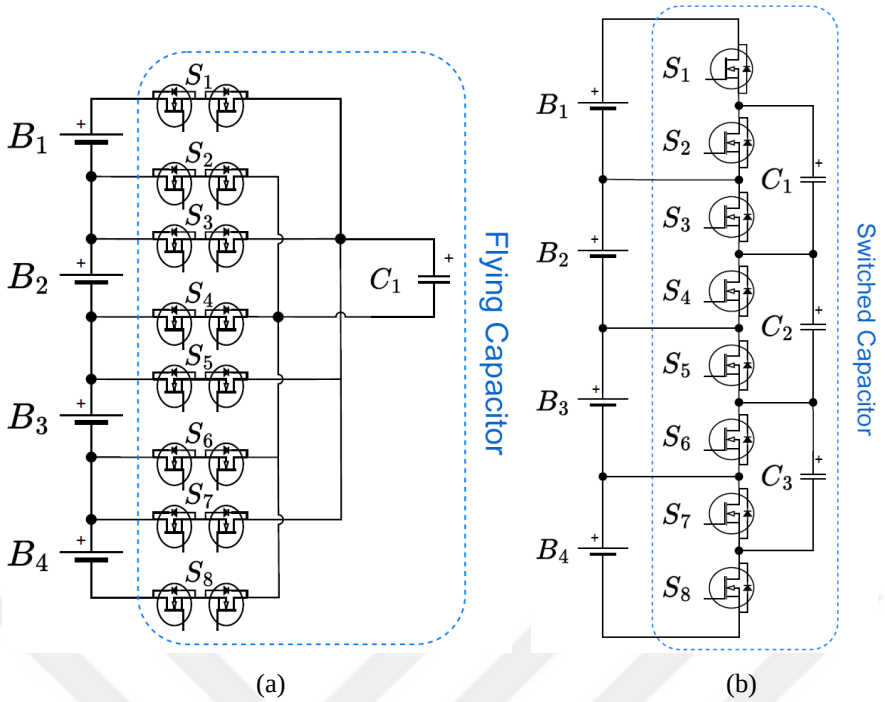


Figure 1.8 (a) Flying capacitor topology, (b) switched capacitor topology

The capacitor based topologies, such as the flying capacitor topology in Figure 1.8 (a) and the switched capacitor topology in Figure 1.8 (b), are also used as C2C methods. The capacitor is first charged from the high-charged cell by switching with the MOSFETs, and then the capacitor is connected to charge the low-charged cell by switching. Flying capacitor topology can be used to charge any low-charged cell from any cell. On the other hand, switched capacitor topology can charge the low-charged cells from its adjacent [40-43].

1.3.2.2 Cell-to-Package (C2P)

In C2P studies in the literature, it is aimed at transferring the energy of high-charged battery cells to the whole battery pack [28, 31, 48-49]. There are several methods, such as the multi-primary based forward converter as seen in Figure 1.9 and the cell-selective unidirectional flyback converter as seen in Figure 1.10. The C2P approaches are less costly and compact compared to other active methods. Nevertheless, the balancing speed at which they achieve balance is less than P2C methods, and their efficiency is moderate. This is mostly due to the presence of a multi-winding transformer and numerous switches, which contribute to their considerable complexity.

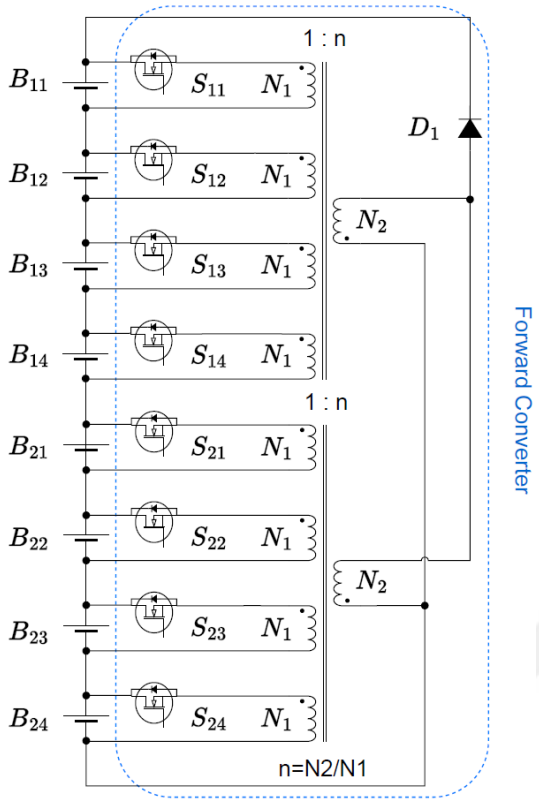


Figure 1.9 Forward converter C2P topology

As shown in Figure 1.9, the primary windings of the multi-primary transformer are connected to each battery cell. The high-charged cells are switched by a forward converter to transfer the excess energy of these cells to the battery pack [48].

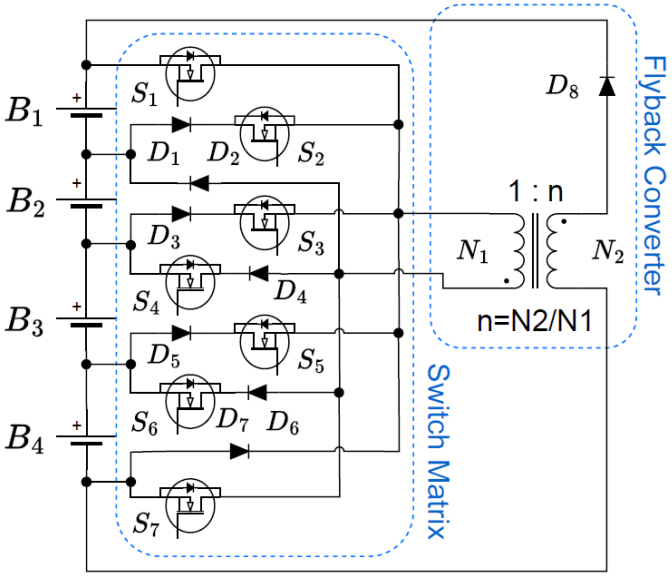


Figure 1.10 Flyback converter C2P topology

As shown in Figure 1.10, each battery cell can be selected with the switch matrix

topology. After the high-charged cells are selected, they are switched by a flyback converter to transfer the excess energy to the battery pack [49].

1.3.2.3 Package-to-Cell (P2C)

BMS balances the low-charged battery cells by transferring the energy of the entire battery pack when the P2C balancing method is applied. The P2C method has the advantages of having the fastest balancing feature among the balancing methods and the applicability of high-power balancing for large battery packages [50-53]. However, the efficiency and cost effectiveness of this study are lower when compared with the C2C and C2P methods. The P2C method, multiple transformers, multi-winding transformers, half-bridge converters and cell-selective converter are some of the topologies that are studied in the literature.

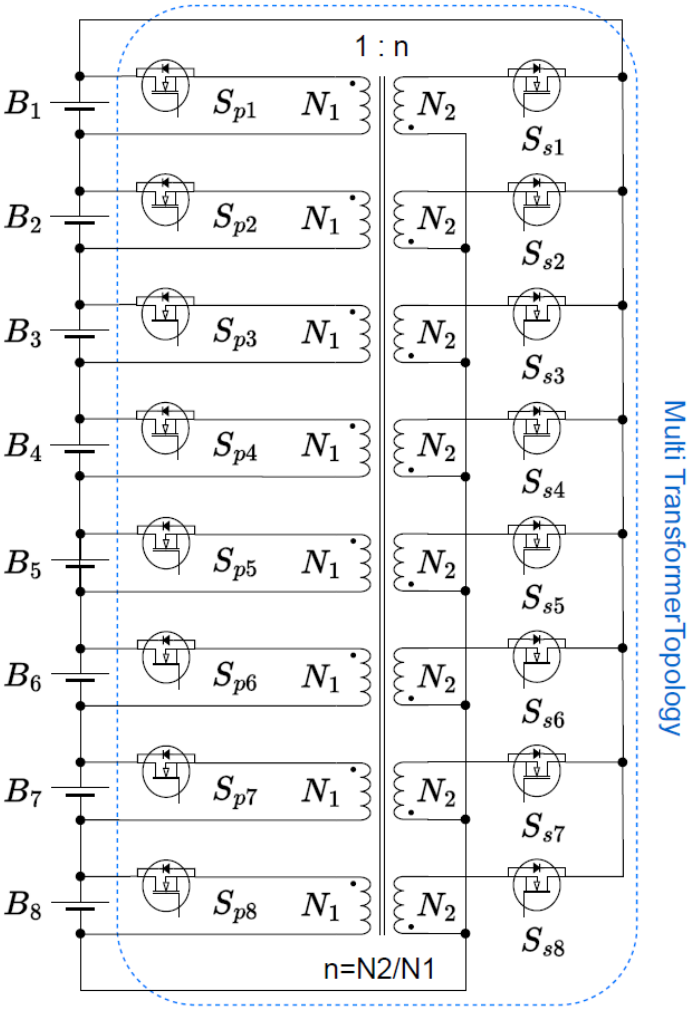


Figure 1.11 Multi-transformer flyback topology

Initially, the multiple transformer topologies are shown in Figure 1.11. In the multiple transformer topology, the primary side of each transformer is connected individually to the battery package. Also, the secondaries are individually connected to the battery cells. Thanks to this method, the packet energy can be contributed directly to the selected cells, thus, the access of batter cells becomes easy. However, each switching element needs to be driven by PWM signals, so the control complexity increases. On the other hand, the utilization of separate transformers for each cell causes an increase in cost and an increase in size [50].

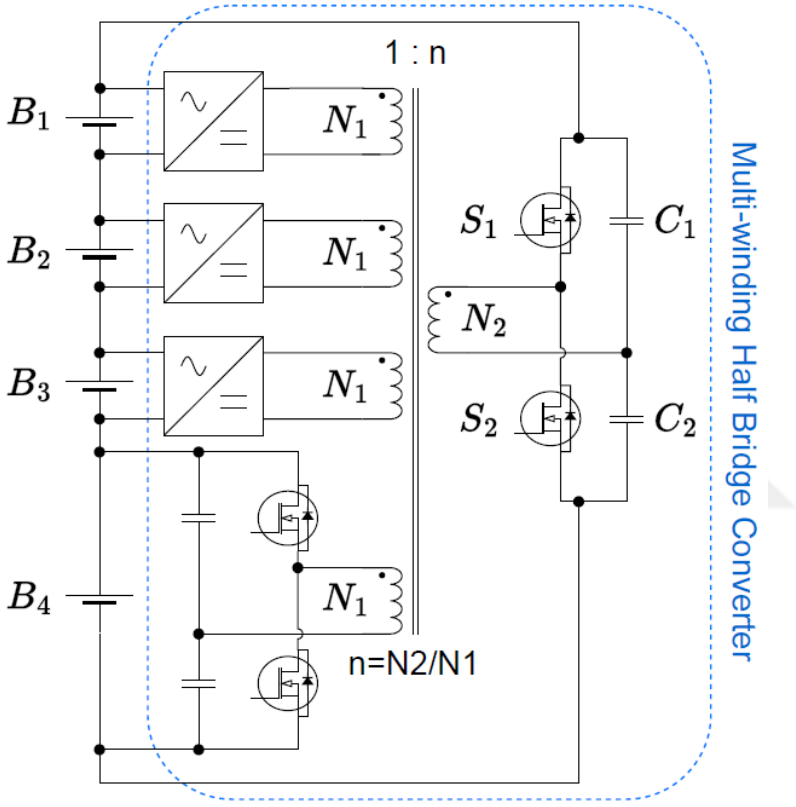


Figure 1.12 Multi-winding transformer with half bridge converter P2C topology

As seen in Figure 1.12, a multi-winding transformer takes the packet energy from a single primary and transfers it to the low-charged ones from one multi-secondary for each cell. In this method, although the least material is used, the size of the multi-winding transformer is large, and a separate controller must be used for each cell [51]. Additionally, the half-bridge converter topology that is based on the multi-winding transformer occupies a greater amount of space as the number of cells increases. These topologies are capable of achieving high balancing speed and efficiency; however, their drawbacks include their high cost, complexity, and large size.

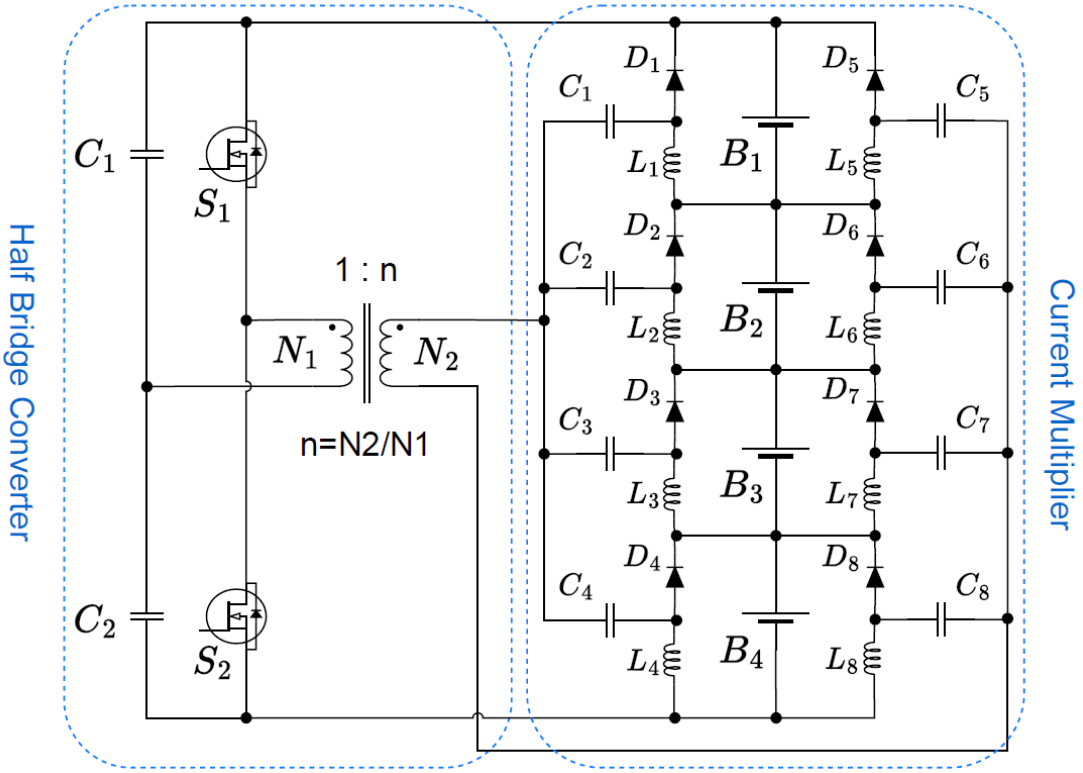


Figure 1.13 Current multiplier based half bridge topology

Another P2C method is the current multiplier based half bridge converter topology, as seen in Figure 1.13. In this topology, the packet energy is connected to a half bridge structure at primary side of a transformer. Also, the secondary side of the transformer is connected to a series of current multipliers that are connected to each cell individually. The half bridge converter supplies a PWM to drive the current multipliers. Thanks to this method, each cell is charged with an equal voltage level, thus, the balancing operation is provided. The advantages of high balance speed, being relatively efficient, and being lower in complexity due to the reduced switch count [52]. Conversely, the amount of passive components is very large, and causes high cost and large size, as well.

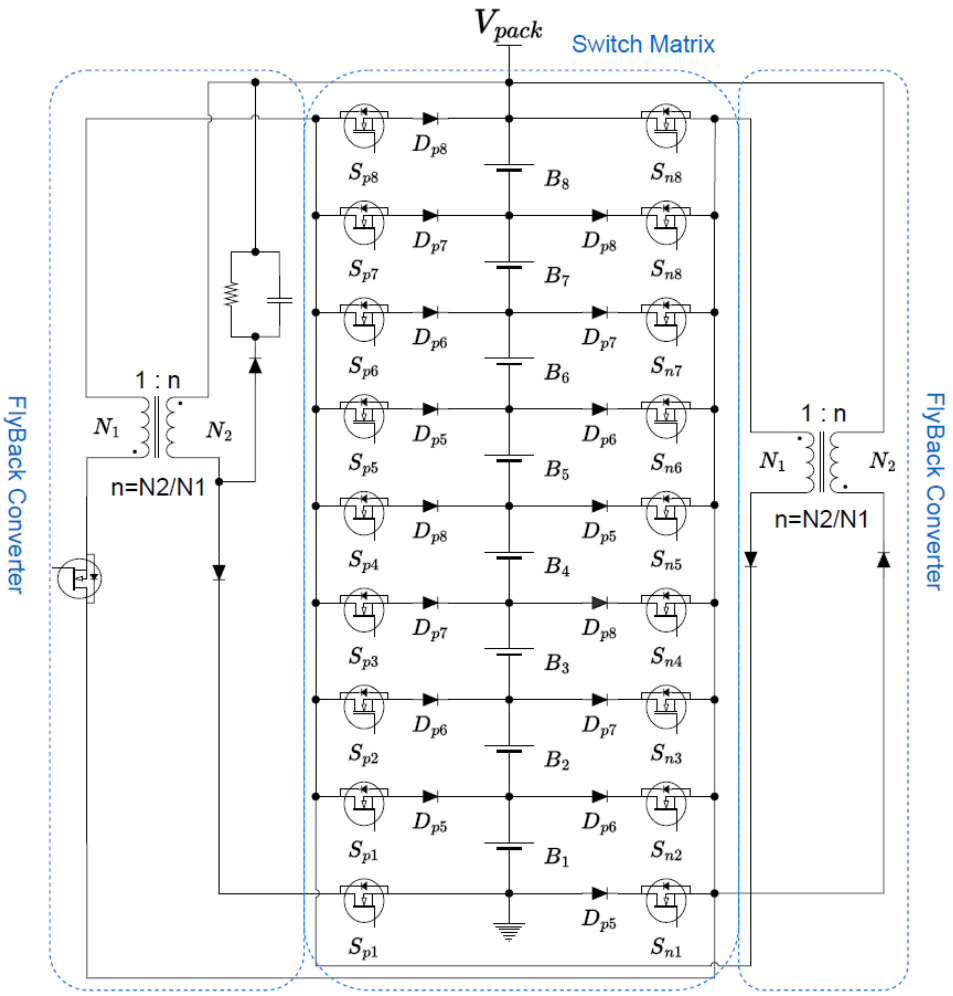


Figure 1.14 P2C Flyback converter with switch matrix topology

1.3.3 Determination of Balancing Topology

Cell-selective converters, on the other hand, transfer the packet energy from the primary to the relevant cells with two transformers and a switch matrix that we can select for each cell, as shown in Figure 1.14. Although the cell selected flyback converter results in a slower balance speed and provides less current as a result of the low power design of the presented study, it is an efficient, moderately simple, cost-effective, and medium-sized topology among the P2C methods [53]. Therefore, the studies in the literature are investigated for high-power dc-dc converters in order to advance the performance of cell selective topology [54]. The push-pull, full bridge, and half bridge converters can achieve high efficiency and high current capability for faster balancing. Nevertheless, they are costly, complex, and large. Consequently, the investigation of efficient and faster

topologies is conducted by also taking into account size, cost, and complexity, and the ĆUK converters are found as another option in that case.

In the latest literature, several studies are found that are related with ĆUK converter and switch matrix. Figure 1.15 (a) illustrates the utilization of an IĆC in conjunction with a SWM [39]. The utilized IĆC is unidirectional, and the secondary side includes a diode. The control of the topology is relatively simpler, but the diode loss is high. On the other hand, the utilized SWM has selection switches for both the input and output sides of the IĆC for a C2C operation. In Figure 1.15 (b), the balancing topology only has a non-isolated ĆUK converter for each adjacent cell [42]. Since there is no SWM in that topology, the cost is low, and the efficiency is high. However, the control difficulty is high due to the number of PWM driven MOSFETs.

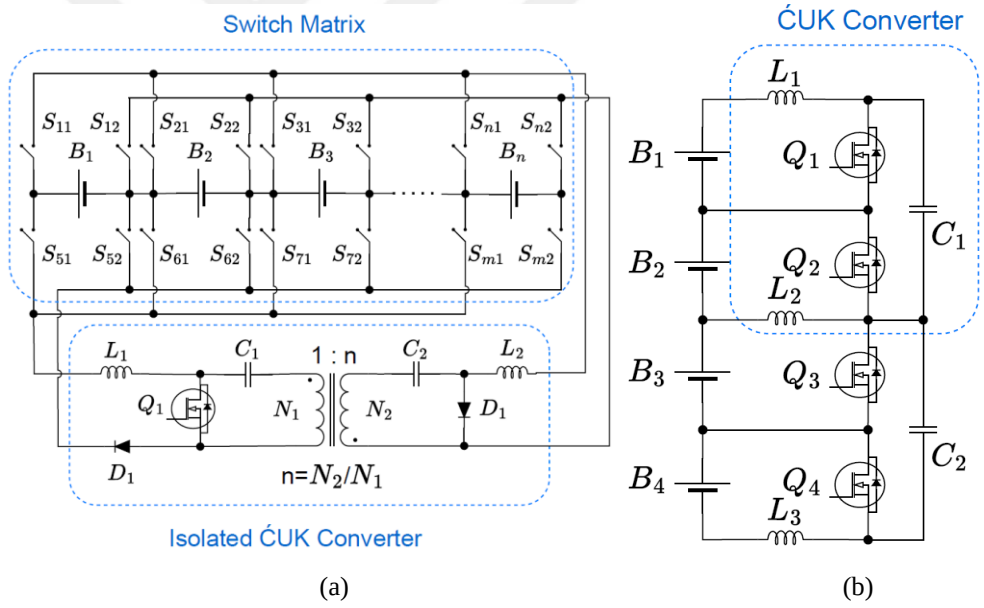


Figure 1.15 (a)C2C isolated ĆUK converter with SWM topology, (b) C2C non-isolated ĆUK converter without SWM

Another topology of a transformerless isolated ĆUK converter with relay SWM is given in Figure 1.16. In this topology, the utilized relay switch matrix and the transformerless IĆC provide low cost and simple control for battery cell selection [37]. Also, high efficiency is provided. However, the size of the topology is large due to the dimensions of the relays and the number of inductors, and the isolation voltage level of the transformerless topology is lower as compared with the transformer design.

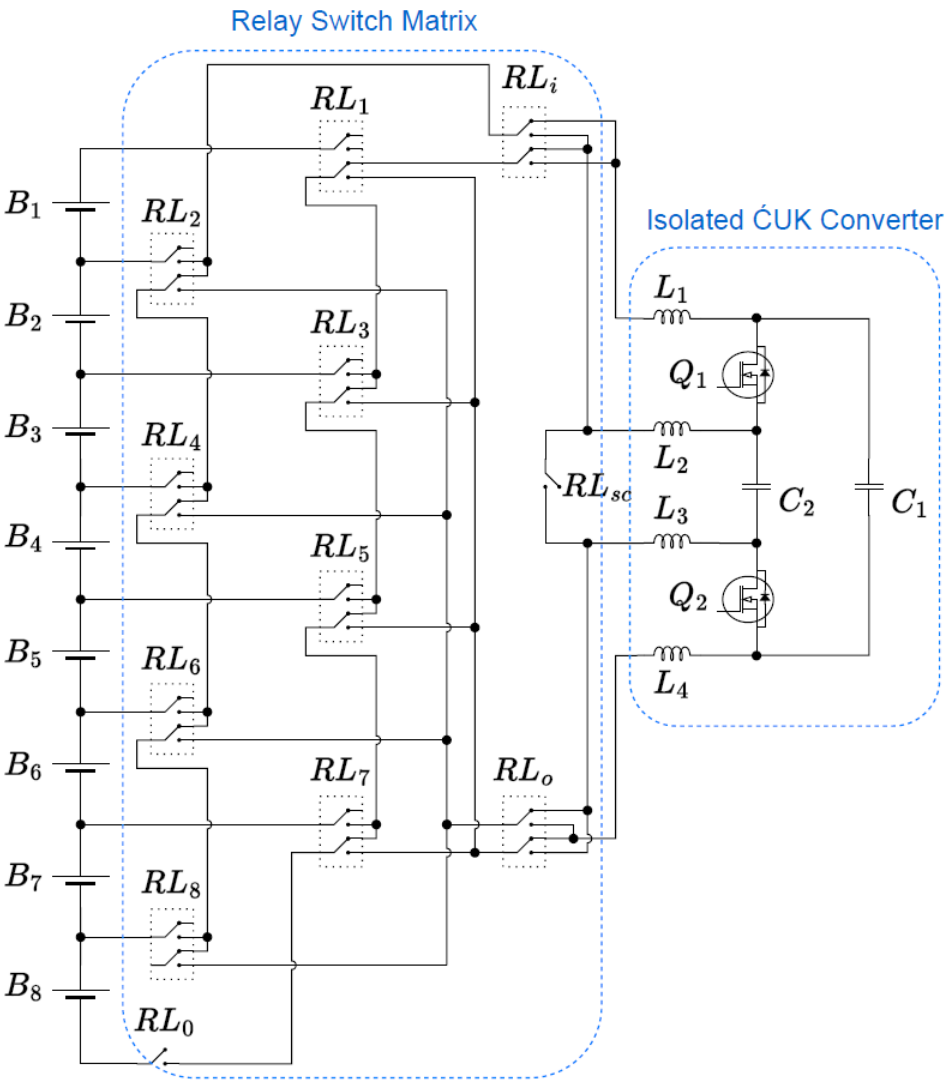


Figure 1.16 C2C transformerless isolated ĆUK converter with relay SWM

In addition, the comparison of the latest studies about the ĆUK converter and switch matrix is compared with the proposed study as given in Table 1.2, and the proposed study is later given in Section 1.6.

Table 1.2 Comparison of latest studies related with ĆUK converter and switch matrix.

Method	**Sim / Exp**	**Topologies**	**Pros**	**Cons**
C2C	Sim	Non-isolated ĆUK with SWM [38]	-No need for isolation -Fast Balancing	- Increased SWM MOSFETs
C2C	Sim	Isolated ĆUK with SWM [39]	-Diode loss in ĆUK converter -Fast Balancing	- Increased SWM MOSFETs - Utilizing Transformer
C2C	Sim	Isolated ĆUK without transformer and SWM [41]	- No need for transformer -Absence of SWM	-Low isolation voltage due to isolation capacitance -Increased PWM driven MOSFETs.
C2C	Sim & Exp	Transformerless Isolated ĆUK with relay SWM [37]	- No need for transformer - Low-cost due to the relays -High efficiency	-Low isolation voltage due to isolation capacitance -Large size due to the relays - Low balancing
C2C	Sim & Exp	Non-isolated ĆUK without SWM [42]	-No need for isolation -Absence of SWM -High efficiency	- Increased PWM driven MOSFETs.
P2C	Sim & Exp	Proposed topology	-Reduced SWM MOSFET -Reduced cost -High current ability -Enhanced balancing speed	-Utilizing Transformer -Efficiency is lower than C2C methods

1.4 SoC Estimation Methods

The BMS completes the balancing process when the voltages and charges of the battery cells are equal. Hence, it is necessary to compute the steady voltages of battery cells and their corresponding charge levels. Nevertheless, the voltage of the battery cells fluctuates during the process of charging or discharging because of the internal resistance of the cells. Therefore, research on SoC estimation methods has been conducted and compiled in Table 1.3 [10, 55-56]. In addition, the chart provides a comparison of their benefits and drawbacks. The initial approach to OCV analysis involves utilizing the OCV vs. SoC graph, which is derived by continuously monitoring the voltage of the battery cells during a long period of rest. The model-based SoC estimate approach requires the use of a battery model, such as an electrochemical model or an equivalent circuit model, to generate an OCV vs. SoC lookup table. The generated lookup table offers real-time SoC estimation during both charging and discharging processes. However, it is important to note that this approach heavily relies on the specific model being used. The internal resistance method utilizes DC voltage and current measurements to determine the internal resistance of batteries, which is then used to estimate the SoC. Nevertheless, the resistance measured is within the milliohm range, enabling precise calculations when the battery is discharged. The following technique is known as coulomb counting. This method relies on the integration of battery currents during charging and discharging over time. The equation 1.4 given in Section 1.1.1 is the base of coulomb counting. Nevertheless, the first evaluation of the SoC is challenging, and the presence of unpredictable disturbances leads to mistakes. On the other hand, Kalman filter (KF) algorithms provide dynamic estimation of SoC in the presence of unknown disturbances and noises. This method utilizes a set of state equations to detect and eliminate deviations and disturbances. In addition, an example of a first order battery model is given in Figure 1.17 for the Kalman filter algorithm. The battery model is later used to obtain the state equations 1.11 and 1.12 for SoC estimation.

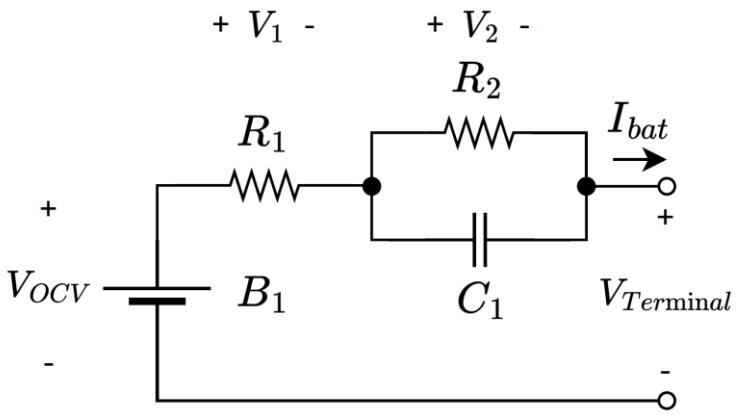


Figure 1.17 First order battery model for Kalman filter

$$\dot{V}_2 = -\frac{V_2}{R_2 * C_1} + \frac{I_{bat}}{C_1} \quad \textbf{(1.11)}$$

$$V_{Terminal} = V_{OCV} - V_2 - I_{bat} * R_1 \quad \textbf{(1.12)}$$

Nevertheless, acquiring the state equations is a highly complicated process. Another approach is the utilization of a neural network (NN). This approach utilizes the battery voltage and temperature as input parameters and generates an estimation of the SoC by applying trained data as given in Figure 1.18.

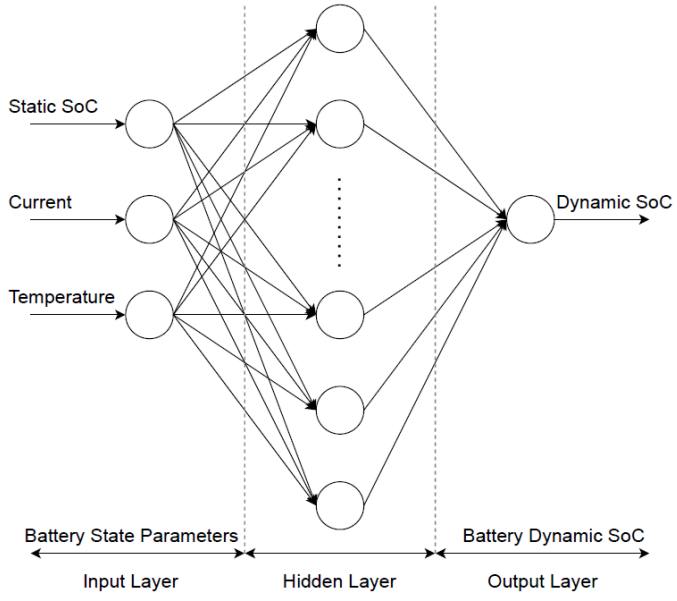


Figure 1.18 SoC estimation schematic of NN algorithm

The controller-based observer methods utilize controllers such as PI, sliding mode, or fuzzy logic to accurately monitor the OCV in order to determine the SoC-OCV relationship.

Table 1.3 Comparison of the SoC estimation methods in the literature [55-56]

SoC Estimation	**Advantages**	**Disadvantages**
Open Circuit Voltage	Easy to Implement, highly precise	Long rest time is required for steady OCV, Therefore, only applicable for the idle state
Model-based SoC estimation	Online and accurate SoC estimation while the charging or discharging of battery	Highly model dependent
Internal resistance	Easy Implementation	High precision is provided for SoC estimation only the end of discharging situation
Coulomb counting	Easy implementation and low power consumption	Inaccurate estimation due to the uncertain disturbances, initial SoC estimation difficulty that causes cumulative effect
Kalman filter (KF)	Accurate SoC estimation in existence of external disturbances	Complex mathematical models are required, Possibility of diverging due to the inaccurate models
Neural Network (NN)	High accuracy, ability of working in noisy or non-linear conditions	Trained data requires very high memory storage and computational effort
Controller Based Observer	Offers high stability, accuracy and robustness for non-linear conditions	Obtaining controller parameters is difficult, high Computational effort
The proposed hybrid model	Easy to implement, high precision, online SoC estimation while charging or discharging	Uncertain disturbance and aging effect dependent while online SoC estimation

The proposed hybrid approach combines both OCV and internal resistance. The OCV method's simplicity and precision are paired with the internal resistance method. Thus, the predicted internal resistance effectively eliminates the changes in cell voltage caused by the internal resistance during the process of charging or

discharging. Next, the lookup table for the OCV-SoC graph is acquired and utilized during the balancing operation. Nevertheless, noise, aging, and temperature dependence remain similar with the OCV technique.

1.5 Control Methods

1.5.1 Battery Balancing Control Strategies

The battery balancing operation requires some variables about the battery cells to determine the amount of imbalance and start the balancing operation. There are three common variables in the literature for battery balancing, which are battery cell capacities, charge levels (SoC), and their terminal voltages, as given in Figure 1.19 [57].

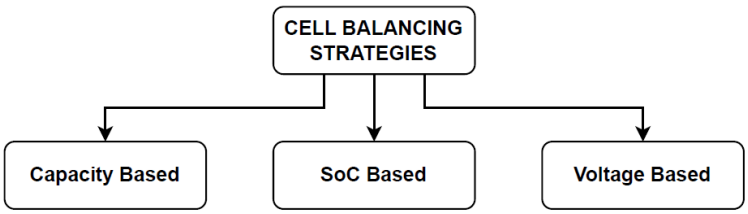


Figure 1.19 The strategies chart for cell balancing

1.5.1.1 Voltage Based Strategy

This method monitors and compares the terminal voltages of battery cells to achieve battery balancing. It is a highly conventional strategy. Practical and simple implementation is offered by this method since only the terminal voltages are monitored and no calculation is required. Mainly, there is a voltage difference threshold level among the battery cells, and the balance operation starts whenever the threshold is exceeded. However, this method might have a balance error because the battery cells might have different internal resistance and capacity as a result of aging factors [58].

1.5.1.2 SoC Based Strategy

This method considers the SoC levels of battery cells for battery balancing. The SoC of the battery cells can be estimated by utilizing the methods described in Section 1.4. After the SoC estimation process, the high-charged cells are

determined to balance the low-charged cells. This method provides robustness against differences due to aging and disturbances due to charging or discharging with a dynamic balancing operation. However, the computational complexity is higher than the voltage-based strategy [59].

1.5.1.3 Capacity Based Strategy

This method utilizes the total capacity of battery cells in a battery pack. Since the battery cells might have different capacities due to aging or other effects, several battery cells can reach their cut-off voltage before the other cells in the pack. Therefore, the residual capacity of the cells that have the highest total capacity is distributed to the battery cells that have a lower capacity while operating the battery. Thus, the energy utilization of the battery pack is maximized. However, the real time operation of this strategy requires a very high computational effort for the BMS [60].

1.5.2 Battery Balancing Algorithms

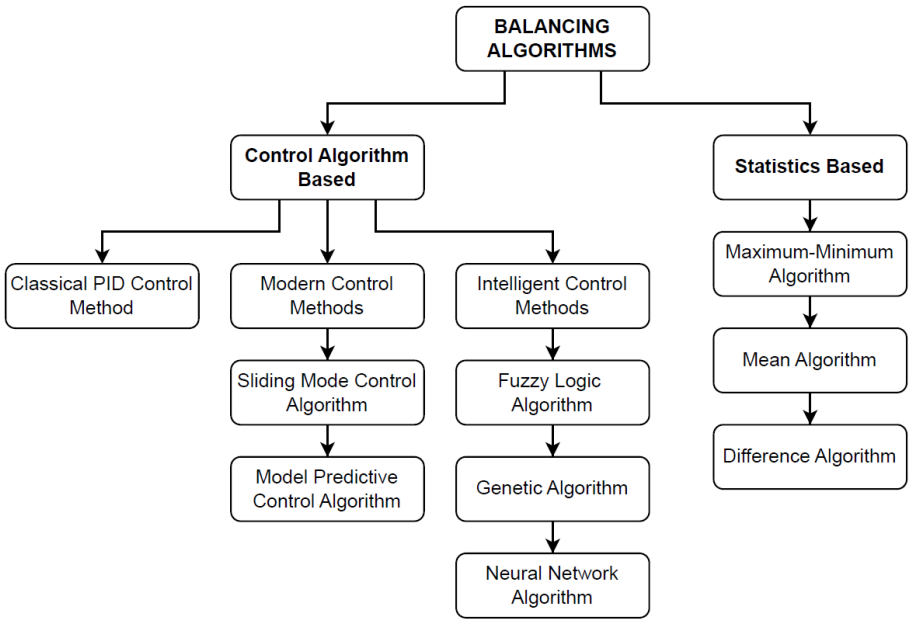


Figure 1.20 The chart of balance algorithms

In the literature, the balance algorithms are divided into three sections: control algorithm based, and statistics based, as seen in Figure 1.20. Balancing algorithms in BMS topologies ensure stable, faster, and more efficient balancing operations while avoiding overbalancing situations [61].

1.5.2.1 Control Algorithm Based Balancing Operation

The control algorithm methods include conventional PID, modern, and intelligent control methods. Also, the modern methods comprise SMC and MPC, while the intelligent methods comprise FLC, GA, and NN.

The PID controller provides easy implementation and a reliable method for battery balancing operations, but its stability becomes weaker as disturbances increase. The PID controller utilization is found with a charge balancing strategy in the literature [38, 62]. The average SoC errors of battery cells and the average SoC reference are taken as input to control the balancing operation. A flowchart example is given in Figure 1.21.

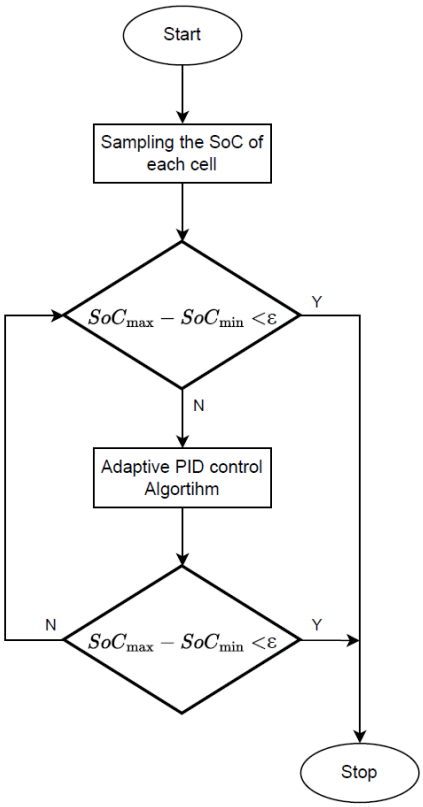
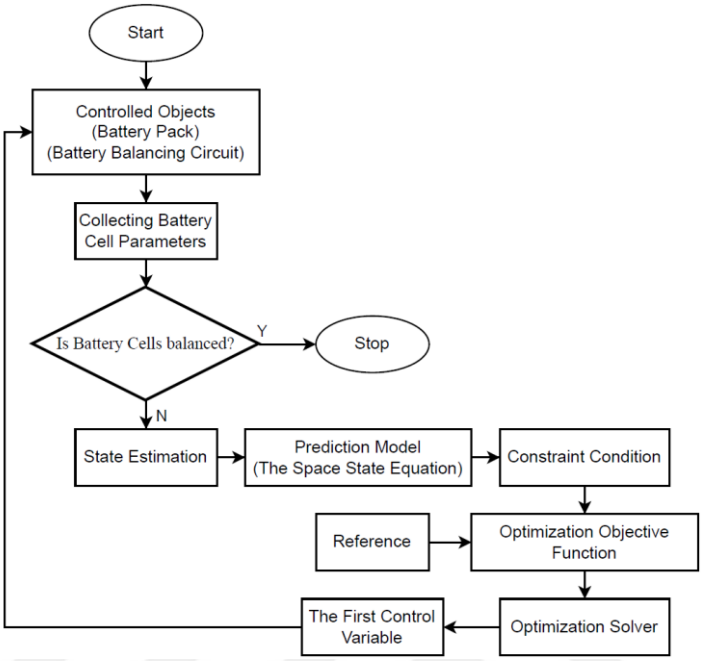


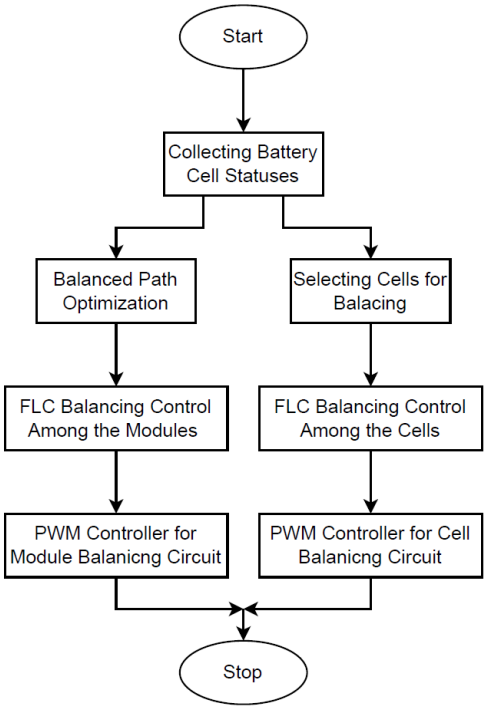
Figure 1.21 Flowchart of adaptive PID algorithm

Modern control algorithms utilize state-space equations to eliminate nonlinear disturbances. The SMC algorithm monitors the charge and discharge currents to obtain the SoC differences among the cells, thus, the balancing current is directed at the battery cells that require balancing [63]. On the other hand, the MPC utilizes battery balance time, current, and voltage for faster equalization and

reduces the energy losses of balancing operations [50]. An example of MPC is also given in Figure 1.22 (a).



(a)



(b)

Figure 1.22 (a) Flowchart of MPC balancing algorithm, (b) flowchart of fuzzy balancing algorithm

The intelligent control algorithms provide an automatic control feature that eliminates human involvement. The complex equations are not needed for these algorithms as modern control methods. The FLC algorithm offers a dynamic balancing strategy by reducing balance time and enhancing balancing efficiency. The algorithm utilizes the voltage and SoC differences and balancing thresholds to carry out the balancing operation [64]. A flowchart example is also given in Figure 1.22 (b). The GA-based algorithms provide less energy consumption and balance time by imitating the evolution of probabilistic optimization methods [65]. Finally, the NN offers dynamic balance operation, reduced balance time, and maximum battery pack capacity. The algorithm imitates the neural network structure of the human brain and learns the information by training with the data and provides optimized output. The algorithm takes the voltage and its derivative as inputs to produce a current output for the balancing operation [66].

1.5.2.2 Statistics Based Balancing Operation

In the statistics based balancing operations, the measured or estimated voltage, SoC, and capacity values are further sorted or compared to determine the imbalance of the battery pack and process the balancing operation. Therefore, statistics algorithms are much simpler and more accurate than controller based algorithms and are used in wide areas.

The statistics based algorithm has three subsections, which are maximum-minimum, mean, and difference methods. In the maximum-minimum algorithm, the observed parameter difference of voltage, SoC, or capacity is compared with the error threshold. Thus, the lower battery cells are discharged, and the higher battery cells are discharged, as shown in Figure 1.23 (a) [67]. In the mean algorithm, the average value of the monitored battery cell parameters of voltage, SoC, or capacity is compared with each battery cell parameter to determine the lower and higher battery cells. Thus, the lower cells are selected for charging, while the higher cells are selected for discharging, as given in Figure 1.23 (b) [68]. In the difference algorithm, the difference of two cell parameters is observed. If the difference value exceeds the determined threshold level, the balance operation proceeds to charge the lower cells with the higher cells, as seen in Figure 1.23 (c) [43].

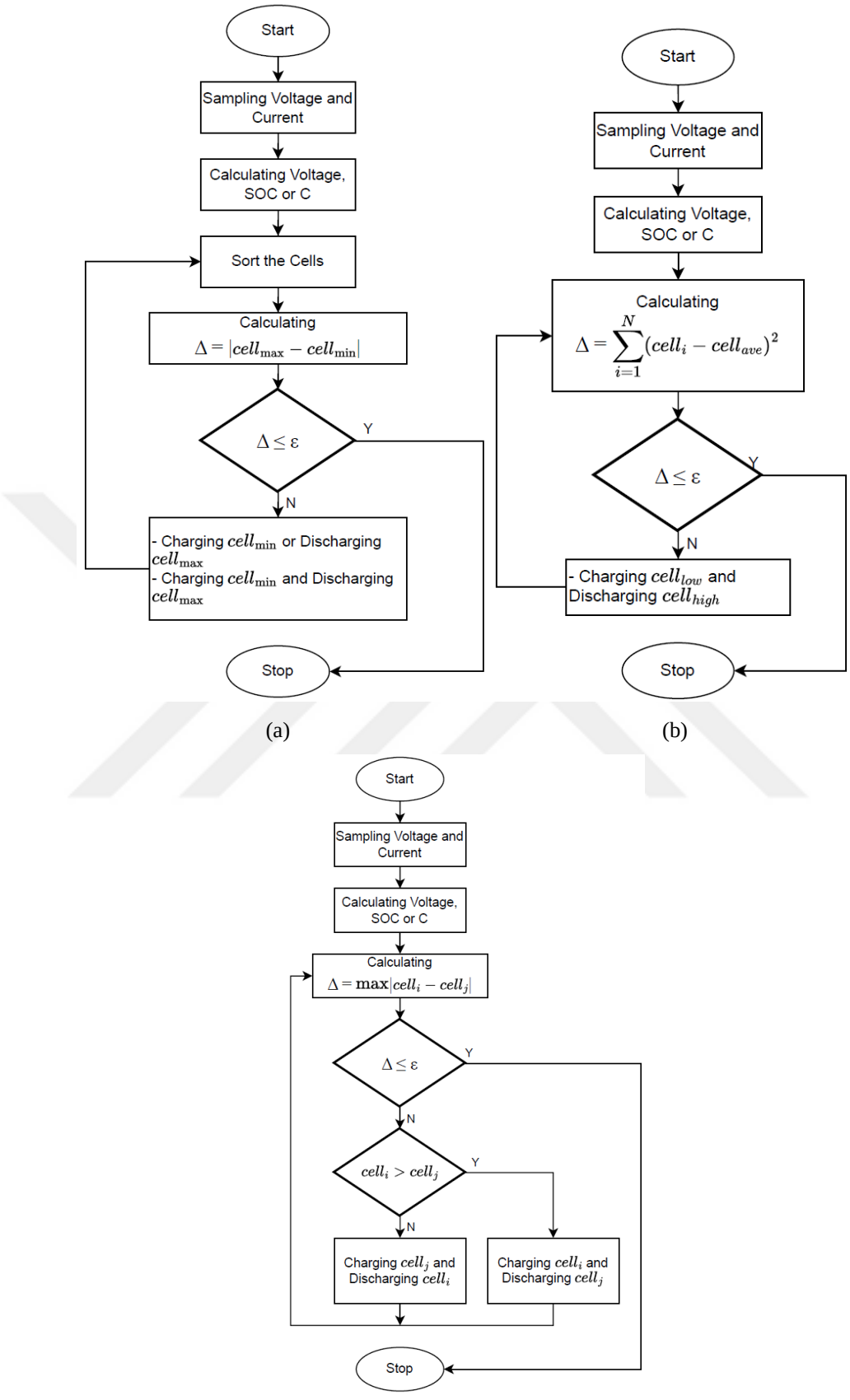


Figure 1.23 (a) The flowchart of maximum-minimum algorithm, (b) the flowchart of mean algorithm, (c) the flowchart of difference algorithm

1.5.3 Control Methods of DC-DC Converters in Balancing Topologies

1.5.3.1 PI Controller

A PID controller continuously calculates an error value, that is, the difference between the desired system state and the current system state [70]. The controller attempts to minimize the error by adjusting the process control input. The PID algorithm controls three fixed parameters to reduce the error value: proportional P, integral I, and derivative D. Intuitively, these values can be interpreted in terms of time, considering the current change;

- P depends on the current error,
- I is the sum of past errors,
- D is an estimate of future errors.

The process controlled by the weighted sum of these three actions is used to set the desired level, as given in equation 1.13.

$$G_{pi} = K_p + \frac{K_i}{s} = \frac{K_p * s + K_i}{s} \quad \textbf{(1.13)}$$

1.5.3.2 One Cycle Control (OCC)

OCC is applied to the switching component of converters [71]. The idea of OCC comes from the average of switched V_s voltage is equal to the output voltage, V_o. Therefore, V_s is integrated into each switching cycle. Then, V_{int} compared with the V_{ref}. Switch becomes on with each clock signal. The switch becomes off when V_{int} and V_{ref} matched. The integrator is reset when V_{int} and V_{ref} match. In addition, an input-output equation 1.14 of a buck converter is given, as an example below [71].

$$V_o = V_s * \frac{Z_{Ld}(s)}{s * L_f + R_{Lf} + Z_{Ld}(s)} \quad \textbf{(1.14)}$$

Where the $Z_{Ld}(s)$ is equal to the equation 1.13.

$$Z_{Ld}(s) = (R_{Ld}(R_{Cf} + \frac{1}{sC_f}))/(R_{Ld} + R_{Cf} + \frac{1}{sC_f}) \quad \textbf{(1.15)}$$

1.5.3.3 Model Predictive Control (MPC)

MPC is based on the logic of estimating the output by applying the control signal calculated within the control horizon along a prediction horizon using the model of the system [72-73]. The model off the system is obtained by applying the state space equation 1.16 and output equation 1.17. The estimation of the output depends on the input (control signal) and measured output values in the past and the input value that is planned to be implemented in the future. The control signal to be applied in the future is calculated to bring the output values closer to the reference value and minimize the determined cost function. The control signal is calculated to the end of the control horizon and is assumed to be constant for the time between the control horizon and the prediction horizon. Only the first of the calculated control signals are sent to the system. In the next time step, new values of the measured output are obtained, the control horizon is shifted one step forward and the same calculations are repeated.

$$x(k+1) = A * x(k) + B * u(k) \quad \textbf{(1.16)}$$

$$y(k) = C * x(k) \quad \textbf{(1.17)}$$

1.5.3.4 Fuzzy Logic Controller (FLC)

The FLC consists of the fuzzifier, inference engine, rule base, and de-fuzzifier. A fuzzifier is the process of converting input information from the system into symbolic values, which are linguistic qualifiers [74-75]. Rule bases characterize the control rules, which are the connections between the input and output defined by the information of the battery balancing process. The inference engine unit operates the fuzzy values with fuzzy rules, then sends the de-fuzzifier to create the actual values as shown in Figure 1.24. FLC has been used commonly in balancing algorithm design because it does not require a mathematical representation of the system and is easy to implement.

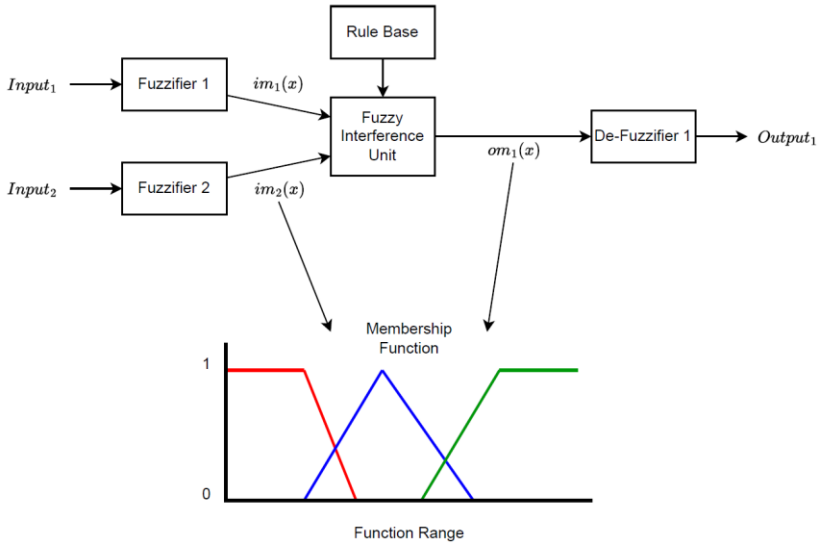


Figure 1.24 Block Diagram of FLC

1.5.3.5 Sliding Mode Control (SMC)

The advantages are robustness against matched external disturbances and unpredictable parameter variations. However, the chattering is a common problem for the method [76].

SMC takes place in two stages;

i)Defining state variables of the system for a stable sliding surface,

ii)Determination of the control signal that will bring the system from any starting point to the sliding surface and keep on it.

In the balancing algorithm scheme, first a state-space representation is obtained to control the state variables of the system. The control signal is obtained on the selected sliding surface, as shown in Figure 1.25. Once the system reaches the sliding surface, it becomes independent of parameter changes and any disturbing effects that may occur.

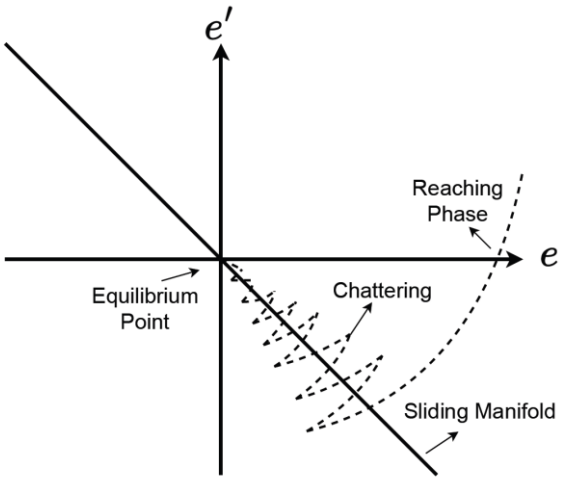


Figure 1.25 Sliding surface graph of SMC

1.5.4 Comparison of Control Algorithms

The balancing algorithms in the literature are further listed in Table 1.4, and their advantages and disadvantages are given. The adaptive PID controller, modern methods, and intelligent methods provide a robust control of nonlinear battery balancing operations and eliminate overbalancing. However, they require complex mathematical models, very high computational effort, or data training. On the other hand, the statistical algorithms of maximum-minimum, mean, and difference algorithms provide easy implementation, less computational effort, and high accuracy. Also, these methods are widely used. However, the statistical algorithms might have some repeated balancing and overbalancing issues. The proposed cell selective algorithm is also given in the table. The proposed algorithm is obtained by modifying the mean algorithm and also has a PI control method for the DC-DC power converter. In the proposed algorithm, the balance operation is limited by the threshold to eliminate overbalancing, and periodical operation is provided as also given in Section 2.4.2 to reduce the repeated balancing issue.

Table 1.4 Comparison of battery balancing algorithms in literature

Algorithms	Advantages	Disadvantages
PID [38, 62]	Easy implementation, reliable, widely used	Requires adaptive methods for nonlinear systems and disturbances
SMC [63]	Robustness for nonlinear systems, applicable for multi input and output systems, fast response	Has a chattering problem that can easily produce balancing error, model dependent
MPC [50]	Able to control Multiple Variables, Robust for both linear and nonlinear systems, avoids over-balancing	Obtaining BMS model is very complex, the computational effort is very high, not used widely
FLC [64]	No need for mathematical model, straightforward, applicable for nonlinear systems	Very high computational effort, flexibility for different battery types is poor
GA [65]	Provides lowest energy consumption	When applied on unlimited balancing operations, unfeasible fitness values are obtained by GA.
NN [66]	Provides maximum battery capacity and minimum balancing time	Training the model is required, due to the lack of experimental data, it is hard to train NN model for every cases.
Maximum-Minimum [67]	Widely used, accuracy is high, simple control	Poor battery pack consistency, repeated balancing and over balancing may occur
Mean [68]	Widely used, simple operation, high battery pack consistency	Requires relatively high effort for computing, repeated balancing and over balancing may occur
Difference [43]	Widely used, easy to implement	Frequently comparison with average voltage, repeated balancing and over balancing may occur
Proposed Algorithm	Simple operation as mean algorithm, reduced probability of repeated equalization and over balancing	Requires relatively high effort for computing, short balancing interruptions due to the periodical operation.

1.6 Proposed Study

This study proposes a BMS that can select individual cells using a switch matrix, transfer power through an IĆC, and balance the battery cells by transferring energy as P2C. The proposed PI controlled IĆC offers a high current capability, leading to fast balancing operations and reduced balancing time [77]. Additionally, the SWM can be programmed to choose a maximum of 4 cells for IĆC, resulting in higher power distribution, enhanced cell control, and simplified cell selection. The CSA monitors the voltage, current, and SoC parameters of each cell and executes an optimal balancing operation when an imbalance is detected. Moreover, the proposed topology is cost-effective when compared to other P2C methods and provides a compact and practical circuit size. A detailed explanation of the working principle, representative figures, and calculations for the proposed study are presented in Chapter 2. The implementation of simulation and experimental studies obtained design performances, and the outcomes of balancing performances are presented in Chapter 3. Finally, Chapter 4 comprises the results and conclusion of the study.

CHAPTER 2

METHODOLOGY

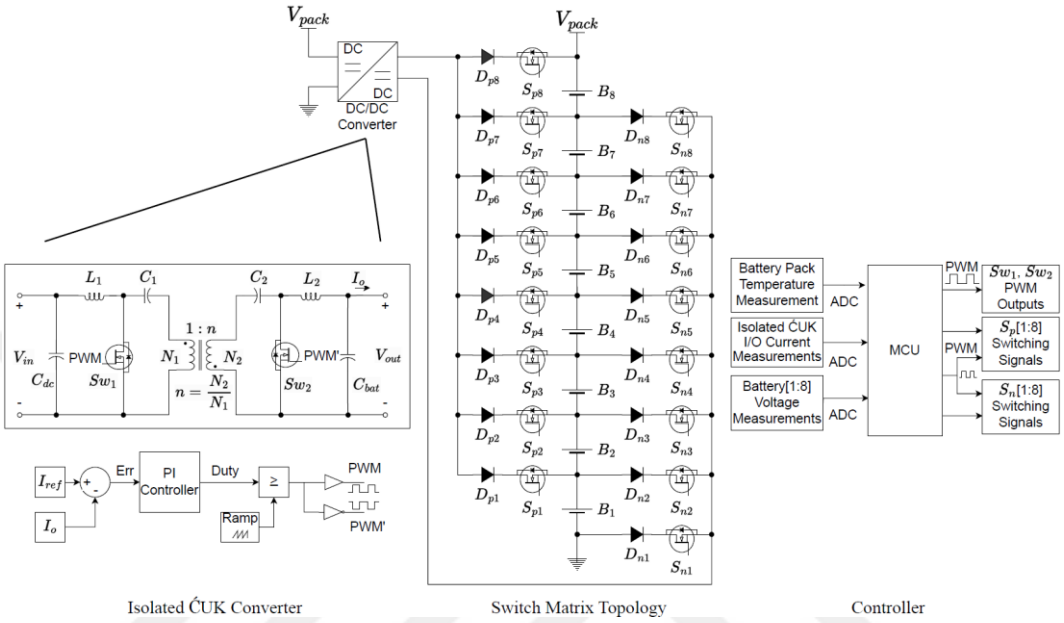


Figure 2.1 Proposed BMS topology

2.1 Battery Package

Because Li-ion batteries have advantages such as high rated voltage, high energy density, long life, and no memory effect, this work utilizes lithium nickel manganese cobalt oxide ($LiNiMnCoO_2$) battery cells that have been enhanced with nickel in their electrochemistry [78]. The battery cells have 18650 packaging. Their charge capacity is 2800 milliampere-hours (mAh), and their voltage range is a maximum of 4.25 V and a minimum of 2.5 V. The detailed information about the utilized battery cells is given in Table 2.1. Also, a battery pack is formed by connecting 8 series and 1 parallel of these battery cells.

Table 2.1 Specifications of utilized battery cells

Battery Parameters	
Package	8S
Part Number	ASPİLSAN INR18650A28
Dimension	18650
Voltage	2.5V Min, 3.65V Nominal, 4.25 Max
Capacity	2800 mAh
Max. Charge Current	4A
Max. Discharge Currents	14A
Operation Temperature	-30 ℃ to +60 ℃
Energy density	230 Wh/kg

2.2 Isolated ĆUK Converter

It is planned to use a single IĆC topology to transfer the energy as a P2C method. As shown in Figure 2.2, L_1, L_2 inductors and C_{dc} and C_{bat} capacitors store the energy and conduct from input to output. C_1, C_2 capacitors protect the transformer from saturation. The transformer is used in this topology to isolate the pack and cell for transferring energy as P2C. The topology has one MOSFET on each side to eliminate diode losses.

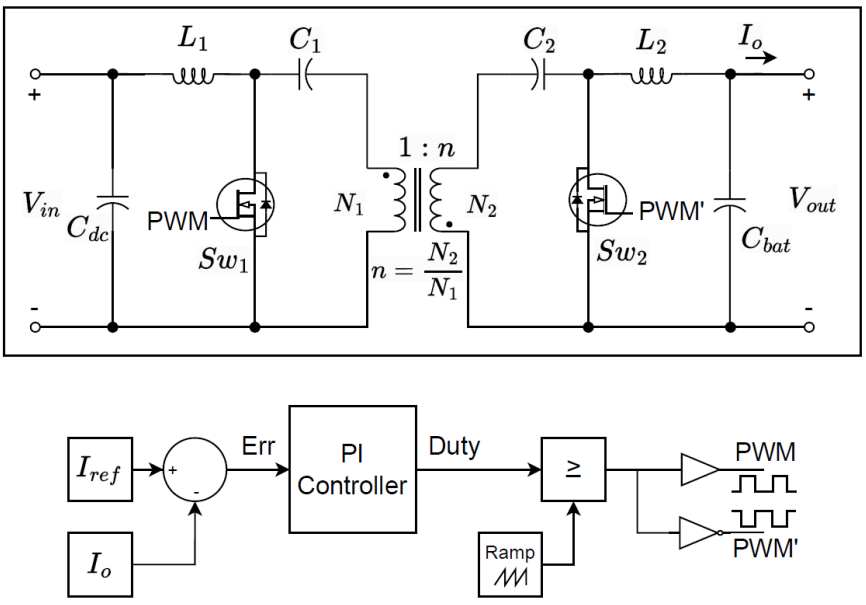


Figure 2.2 Representation of isolated ĆUK converter

2.2.1 Isolated ĆUK Converter Working Principle

The isolated ĆUK converter has state 1 and state 2 operation phases, as shown in Figure 2.3 (a) and (b).

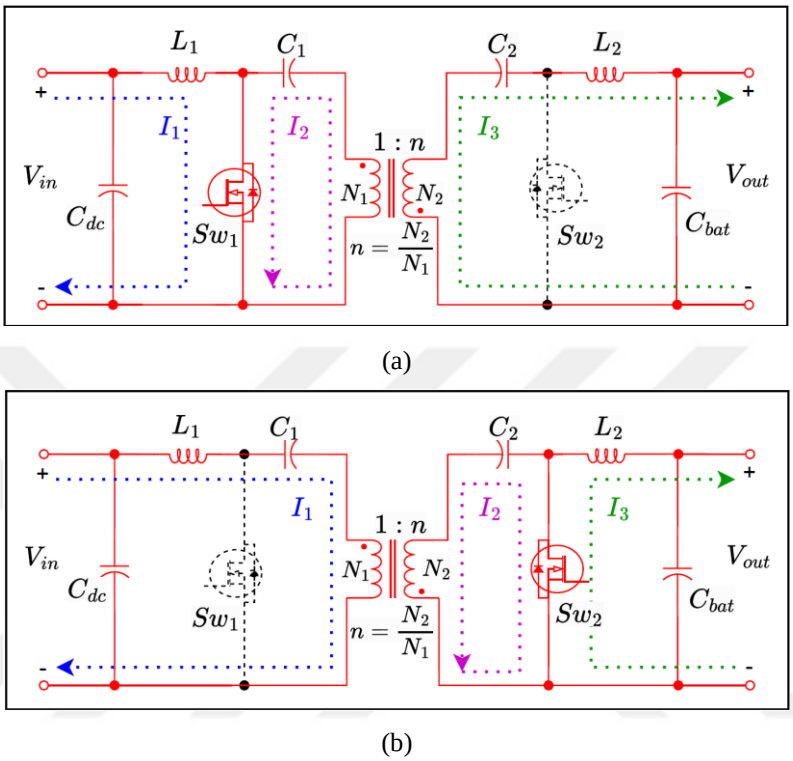


Figure 2.3 (a) On switching state of IĆC, (b) off switching state of IĆC

State 1 of IĆC starts when the Sw_1 is logic high and the Sw_2 is logic low, as seen in Figure 2.3 (a). After Sw_1 is switched to high, the current I_1 flows through L_1 and S_{w1}. Therefore, L_1 is charged by the input voltage source. The current loop I_2 on the primary side of the transformer flows through C_1, Sw_1 and L_m. Because the Sw_2 is switched as logic low, the L_2 inductor is supplied by the transformer. The output is supplied by that passes through the C_{dc} and L_2 components. The current stress on the Sw_1 is ($\imath_{L1}$ + $\imath_{Lm}$), and the voltage stress on the Sw_2 is (n * V_{in} + V_o) where n is the transformer turn ratio of (N_2/N_1).

By switching the Sw_1 as logic low and the Sw_2 as logic high, the IĆC switches from state 1 to state 2, as seen in Figure 2.3 (b). While state 2, the input current I_1 flows through L_1, C_1 and L_m. The voltage stress on the Sw_1 is (V_{in} + V_o/n) and the current stress on the Sw_2 is (I_{L2} + I_{C2}). Because the current direction on the primary side of the transformer is reversed and Sw_2 is switched as high, Sw_2

switch starts conducting the current I_2. Thus, the L_1 inductor charges the C_1, transformer and C_2 components. The output is fed by the current I_3 that passes through L_2 and C_{dc} components.

2.2.2 Isolated ĆUK Converter Calculations

The values of components are computed and implemented in the proposed topology, as indicated in Table 2.2.

Table 2.2 IĆC and SWM parameters

Parameter	Value
Input Voltage (V_{in})	20 V to 33.6 V
Output Voltage (V_{out})	0 V to16.8 V
Max Output Power (P_o)	50.4 W
Switching Frequency (f_s)	50 kHz
Efficiency (η)	81.98 %
IĆC MOSFETs (Sw_1, Sw_2)	BSC070N10NS5ATMA1 100V 80 A
SWM MOSFETs ($S_{p1:8}$, $S_{n1:8}$)	CSD18511Q5AT 40 V 100A
Diodes ($D_{p1:8}$, $D_{n1:8}$)	SVM1045VB 45V 10 A
Micro-controller	DSPIC33FJ16GS502
DC input Capacitance, C_{dc}, ESR_{Cdc}	100 uF, 210mΩ
Primary inductance, L_1, ESR_{L1}	330uH, 326mΩ
Primary capacitance, C_1, ESR_{C1}	100 uF, 210mΩ
Secondary inductance, L_2, ESR_{L2}	330uH, 326mΩ
Secondary capacitance, C_2, ESR_{C2}	680uF, 45mΩ
Output capacitance, C_{bat}, ESR_{Cbat}	100 uF, 6mΩ

The input voltage is calculated from the battery pack specifications, which are eight series and one parallel structure. The maximum output value is determined by how many cells can be balanced at the same time, which is 4 cells. By applying the max balance current of 3 A to the max output value, the required power output has been found to be 50.4 W with a measured efficiency of 81.98% in Section 3.3.

The MOSFETs and diodes are chosen based on their operational zones within the balance circuit. The IĆC MOSFETs operate with 50 kHz PWM signals. A microcontroller is responsible for voltage, current, and temperature measurements while providing PWM outputs for balance topology and UART outputs for the BMS user interface.

While operating the converter in steady state, the average voltage of an inductor is zero. For example, the sum of state 1 and state 2 voltages of L_1 is zero. By applying the theorem, the equation 2.1 is obtained from L_1.

$$V_{in} * D * T + \left(\frac{-V_o}{n} * \ (1 - \mathrm{D}) * \mathrm{T}\right) = 0 \quad \textbf{(2.1)}$$

$$V_o = \frac{n*Vin*D}{1-D} \quad \textbf{(2.2)}$$

After the formula is simplified, the input and output relations of the converter are obtained as equation 2.2. The output voltage, V_o, is equal to the transformer turn ratio, n, times the input voltage, V_{in}, times the duty cycle, D, divided by one minus D. The passive component values are calculated by considering state1 and state 2 of the IĆC, as is shown in Figure 2.3.

$$V = L * \frac{di}{dt} \quad \textbf{(2.3)}$$

$$V_{in} = L_1 * \frac{\Delta i_{l1}}{D*T} \quad \textbf{(2.4)}$$

$$\frac{V_o}{n} = L_1 * \frac{\Delta i_{l1}}{(1-D)*T} \quad \textbf{(2.5)}$$

The inductance values are obtained from equation 2.3. The voltage is equal to the inductance multiplied by the change in current in time. To calculate the value of L_1, either equation 2.4 that is obtained from the state 1 operation of L_1 or equation 2.5 that is obtained from the state 2 operation of L_1 can be used. As seen in equation 2.4, the change rate of current in time can be written as the change of current on L_1, Δi_{l1}, divided by the switching period, T, times the duty ratio, D.

$$L_1 = \frac{V_{in}*D*T}{\Delta i_{l1}} = \frac{V_{in}*D*T}{\Delta i_{in}} \quad \textbf{(2.6)}$$

After the final formula is simplified, the L_1 value is obtained from equation 2.6. In addition, the change in current on L_1, Δi_{l1}, is also equal to the change in input current, Δi_{in}.

$$V_o = L_2 * \frac{\Delta i_{l2}}{(1-D)*T} \quad \textbf{(2.7)}$$

$$L_2 = \frac{V_{out}*(1-D)*T}{\Delta i_{l2}} = \frac{V_{out}*(1-D)*T}{\Delta i_o} \quad \textbf{(2.8)}$$

The inductance value of L_2 is calculated with the same equation 2.3 as well. For the L_2 inductor, state 2 equation 2.7 is used. After the simplification, the equation 2.8 is obtained. In addition, the change of current on L_2, Δi_{l2}, is also equal to Δi_{in}.

$$L_m = \frac{V_{in}*D*T}{\Delta i_{Lm}} = \frac{V_{in}*D}{\Delta(I_{in}+n*I_o)*f_s} \quad \textbf{(2.9)}$$

The simplified equation 2.9 that is needed to calculate the inductance value of L_m is also obtained from the equation 2.3. The change of current on L_m, Δi_{Lm}, is equal to $\Delta(I_{in} + n * I_o)$.

$$\Delta Q = C * \Delta V \quad \textbf{(2.10)}$$

$$\frac{\Delta Q}{\Delta t} = I \quad \textbf{(2.11)}$$

All the capacitance values that belong to the IĆC are obtained with the equations 2.10 and 2.11. The change in charge level, ΔQ, of a capacitor is equal to the capacitance, C, times the change in voltage level, V. On the other hand, the change in charge level, ΔQ, is also equal to the current, I, multiplied by the change in time, Δt.

$$\Delta Q = n * I_o * D * T \quad \textbf{(2.12)}$$

$$\Delta Q = I_{in} * (1 - D) * T \quad \textbf{(2.13)}$$

$$\Delta Q = C_1 * \Delta V_{C1} \quad \textbf{(2.14)}$$

The capacitance of the primary capacitor, C_1, is obtained from the equations 2.12, 2.13 and 2.14. The state 1 equation 2.12 and state 2 equation 2.13 are equal to the equation 2.14, and both state 1 and state 2 equations can be used to calculate capacitance values.

$$C_1 = \frac{n*I_o*D}{\Delta V_{in}*f_s} = \frac{I_{in}*(1-D)}{\Delta V_{in}*f_s} \quad \textbf{(2.15)}$$

The C_1 value is obtained with the simplified equation 2.15. The change in voltage level on C_1, ΔV_{C1}, is equal to the change in input voltage level, ΔV_{in}.

$$\Delta Q = I_o * D * T \quad \textbf{(2.16)}$$

$$\Delta Q = \left(\frac{I_{in}}{n}\right) * (1 - D) * T \quad \textbf{(2.17)}$$

$$\Delta Q = C_2 * \Delta V_{C2} \quad \textbf{(2.18)}$$

$$C_2 = \frac{I_o * D}{\Delta V_o * f_s} = \frac{(I_{in}/n) * (1-D)}{\Delta V_o * f_s} \quad \textbf{(2.19)}$$

The capacitance of the secondary capacitor, C_2, is calculated by simplifying the equations 2.16, 2.17, and 2.18. The simplified equation 2.19 is used to calculate the C_2 value. Also, the change in voltage level on C_2, ΔV_{C2}, is equal to the change in output voltage level, ΔV_o.

$$\Delta Q = \frac{\Delta I_{L2}}{2} * \frac{T}{2} * \frac{1}{2} \quad \textbf{(2.20)}$$

$$\Delta Q = \frac{\Delta I_{L2} * T}{8} \quad \textbf{(2.21)}$$

$$\Delta Q = Cbat * \Delta V_{Cbat} \quad \textbf{(2.22)}$$

$$C_{bat} = \frac{\Delta Q}{\Delta V} = \frac{\Delta I_{L2} * T}{8 * \Delta V_o} \quad \textbf{(2.23)}$$

The capacitance of the output capacitor, C_{bat}, is calculated with the simplified equation 2.23. The simplified equation is obtained from the equations 2.20, 2.21 and 2.22. Also, the change in voltage level on C_{bat}, ΔV_{Cbat}, is equal to the change in output voltage level, ΔV_o.

2.2.3 IĆC Transformer Calculations

The balancing topology is designed to supply a maximum power output of 75W at a maximum battery pack voltage level of 33.6 V. According to the determined power level, a core type is selected initially. The criteria for selecting a proper core are size and magnetic properties. To determine the proper core, a core selection catalogue is used [79]. The ETD29 ferrite core was selected as a proper core according to the datasheet [80-81]. On the other hand, the magnetizing

inductance value, L_m, shall be 116 µH according to the calculations in Section 2.2.2. The foreknowledge of the power output, pack voltage, and magnetizing inductance value determines the basics of the desired transformer. However, the further parameter calculations and design details of a proper transformer are obtained with the help of design handbooks [82-84]. The final parameters of the utilized transformer are given in Table 2.3.

Table 2.3 Transformer parameters

Parameter	**Value**
Transformer Core Type	EPCOS B66359A ETD 29/16/10
Maximum Power Consumption (Pmax)	75W
Turns Ratio (N_p/N_s)	30:30
Primary Inductance (L_p)	116.78 µH
Primary Resistance (R_p)	332 mΩ
Secondary Inductance (L_s)	116.94 µH
Secondary Resistance (R_s)	360 mΩ
Magnetizing Inductance (L_m)	115,56 µH
Leakage Inductance (L_{lk})	1.22 µH
Equivalent coil resistance (R_{eq})	93 mΩ
Coupling Factor (K)	0.9948
Interwinding Capacitor (C_{iw})	2.1 nF

The transformers transfer their energy from the primary winding to the secondary winding by using a magnetic field. When a conductor winding is wrapped around a magnetic core and a current is passed through, a closed magnetic circuit is created, as seen in Figure 2.4. A magnetomotive force, F, is created in this closed magnetic circuit as the magnitude of number of the turns time in the current that passes through (N*I).

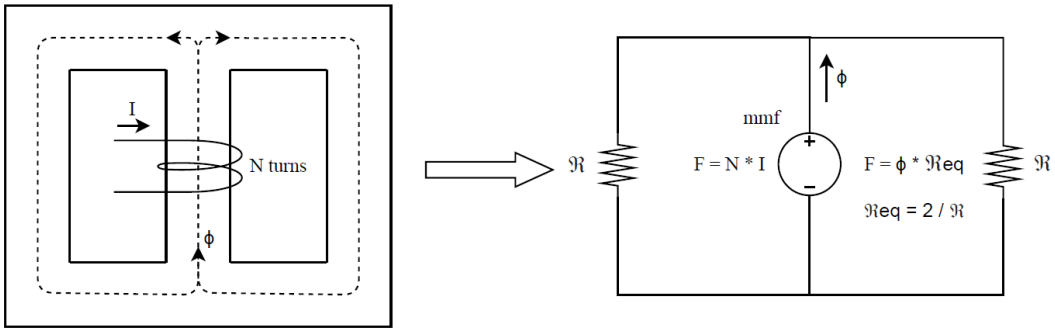


Figure 2.4 Closed loop magnetic circuit of transformer

Moreover, the created magnetomotive force, F, provides a magnetic flux, ϕ, that flows over the magnetic reluctance of the closed magnetic circuit, as shown in Figure 2.4.

$$F = N * I = \phi * \Re_{eq} \quad \textbf{(2.24)}$$

Thus, the magnetomotive force, F, is calculated with the equation 2.24. The equivalent resistance, $\Re_{eq}$, times the magnetic flux, ϕ, is also equal to the number of turns, N, and the current that passes through, I.

$$\phi = N * I / \Re_{eq} \quad \textbf{(2.25)}$$

Furthermore, the equation 2.24 can be rearranged as the equation 2.25 to calculate the magnitude of ϕ. However, the ferrite cores permit only a limited amount of ϕ. The ferrite cores are saturated with the excess amount of ϕ, thus the electrical circuit on the primary and secondary windings becomes short circuited. To prevent an electrical short circuit, the magnetic flux density, B, versus field strength, H, graph (which is also called the B-H curve) is considered.

$$\mu = B / H \quad \textbf{(2.26)}$$

The B-H curve of each ferrite core determines its magnetic property. The magnetic permeability, μ, is also calculated with these parameters, as seen in equation 2.26.

$$B = \frac{\phi}{A} = \frac{N * I}{\Re_{eq} * A} \quad \textbf{(2.27)}$$

The magnetic flux density, B, is kept in a range for operating properly when a transformer is designed. Also, B is calculated with the equation 2.27.

$$\Re = \frac{le}{\mu_0 * \mu_r * Ae} \quad \textbf{(2.28)}$$

The reluctance of the transformer is calculated using equation 2.28. As seen in Figure 2.5, the effective length of the ferrite core, le, is the path that the magnetic flux, ϕ, flows. The effective area of the ferrite core, Ae, is the area where the magnetic flux, ϕ, is concentrated. The magnetic permeability of the free space, μ_0, and the magnetic permeability of the ferrite core, μ_r, are the magnetic factors used to calculate the reluctance.

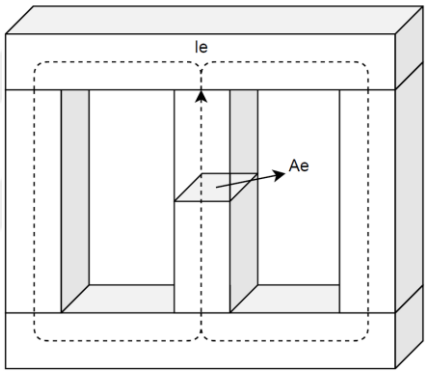


Figure 2.5 Reluctance calculation parameters

The reluctance may also be calculated for each part of the ferrite core. Therefore, the reluctance of the ETD29 ferrite core is calculated by dividing the core into four regions, as seen in Figure 2.6. These regions are the left and right extensions, the top and bottom sides, the middle extension, and the air gap of the ferrite core. Also, the divided regions are l1, l2, l3 and lg if sorted by length. The equivalent reluctance of these regions is used for the further calculations.

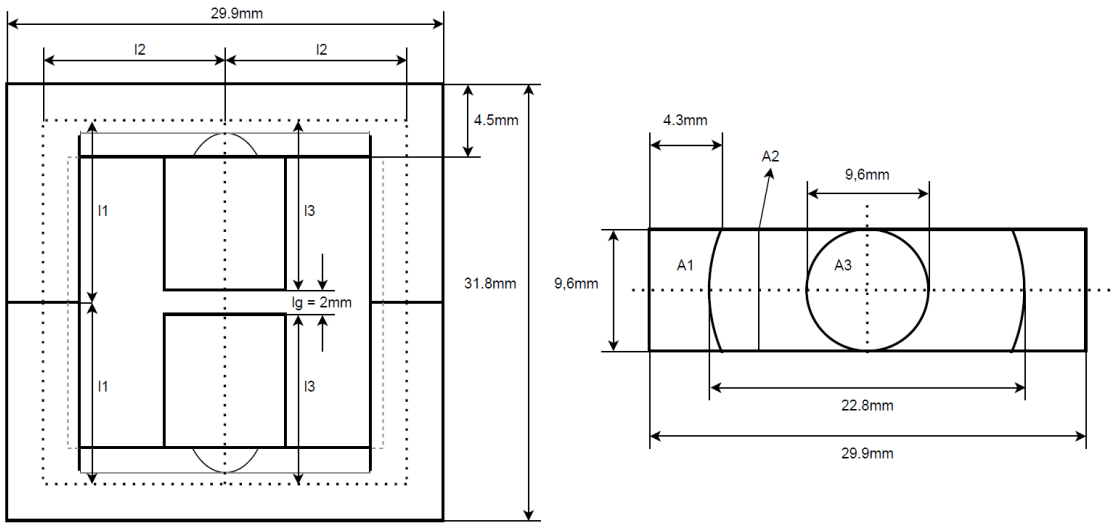


Figure 2.6 The ETD29 ferrite core dimensional specifications

By using the specifications identified in Figure 2.6, the reluctances are calculated with the equations 2.29, 2.30, 2.31 and 2.32. The left and right extensions of the core have the same length, l1, and area, A1. Also, the top and bottom sides of the core have the same length, l2, and area, A2. The middle extension of the core has a length of l3 and an area of A3. The air gap has a length of lg. However, the area of the air gap, Ag, differs from the core area, A3, due to the fringing effect that is also described in the design handbook [83]. The magnetic flux path that flows through the air gap expands in the air, therefore, the Ag becomes greater than A3.

$$\Re_1 = \frac{l1}{\mu_0 * \mu_{rcore} * A1} \quad \textbf{(2.29)}$$

$$\Re_2 = \frac{l2}{\mu_0 * \mu_{rcore} * A2} \quad \textbf{(2.30)}$$

$$\Re_3 = \frac{l3}{\mu_0 * \mu_{rcore} * A3} \quad \textbf{(2.31)}$$

$$\Re_g = \frac{lg}{\mu_0 * \mu_{rair} * Ag} \quad \textbf{(2.32)}$$

The obtained reluctance for each region is positioned into the equivalent magnetic circuit that is shown in Figure 2.7.

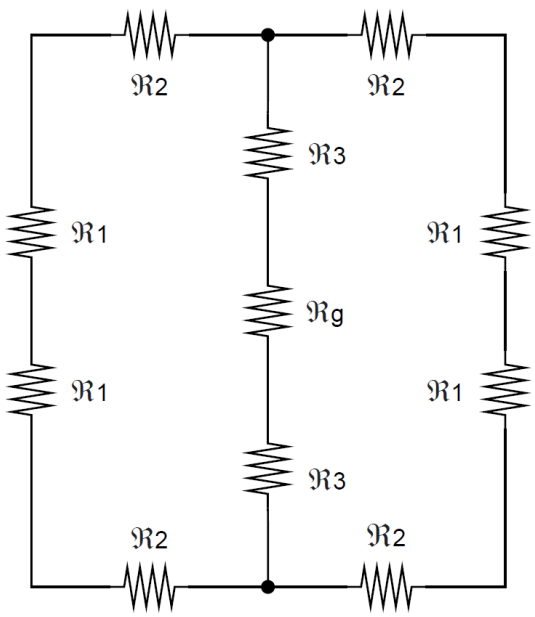


Figure 2.7 The ETD29 ferrite core equivalent reluctance circuit

Because the coils of the transformer will be winded around the middle extension of the core, the equivalent reluctance value is calculated using equation 2.33.

$$\Re_{eq} = 2 * \Re_3 + \Re_g + \left(\frac{1}{2*(\Re_1+\Re_2)} + \frac{1}{2*(\Re_1+\Re_2)}\right)^{-1} \quad \textbf{(2.33)}$$

The sum of $\Re_1$ and $\Re_2$ reluctances of the left and right branches are parallel to each other but serially connected to $\Re_3$ and $\Re_g$ reluctances.

$$AL = \frac{1}{\Re_{eq}} \quad \textbf{(2.34)}$$

The first parameter that is required to calculate the magnetizing inductance value, L_m and the magnetic flux density, B, is the nano Henry per turn square, AL, value. The AL value defines how much the inductance value will increase for each turn that is wrapped around the core. On the other hand, it is obtained by inverting the equivalent reluctance, $\Re_{eq}$, of the ETD29 ferrite core and calculating it with the equation 2.34.

$$L = N^2/\Re \quad \textbf{(2.35)}$$

Inductance can be found with the equation 2.35, and it is equal to the turn square divided by the reluctance.

$$L_m = {N_p}^2 * AL * 10^{-9} \quad \textbf{(2.36)}$$

After AL is found, the magnetizing inductance value, L_m, is obtained from the equation 2.36. The equation is used so that the calculated magnitude of L_m can be found.

$$B = \frac{AL*N_p*I}{Ae} \quad \textbf{(2.37)}$$

Also, the magnetic flux density, B, is obtained from equation 2.37. The B magnitude determines the operation region of the designed transformer whether it is in the saturation region or not.

2.2.4 IĆC Gate Driver Circuit

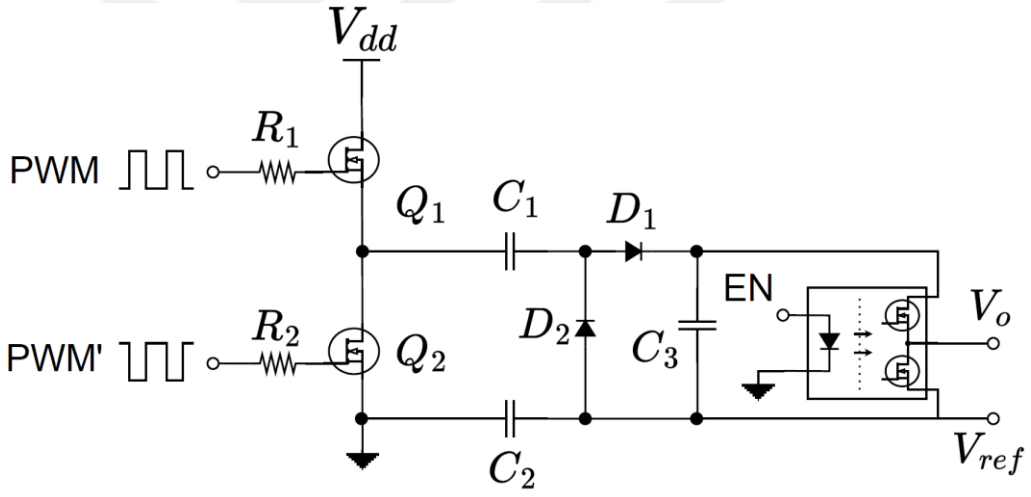


Figure 2.8 IĆC driver circuit

The circuit topology of the IĆC driver is shown in Figure 2.8. The topology includes a modified charge pump circuit and a half bridge circuit [85-86]. The half bridge drives the charge pump circuit with the help of complementary PWM signals. However, the output of the charge pump circuit can only be activated with an EN signal. The EN signal might be a discrete signal for selection purposes and a PWM signal for MOSFET drive purposes. The modified charge pump circuit also provides isolation and floating gate drive.

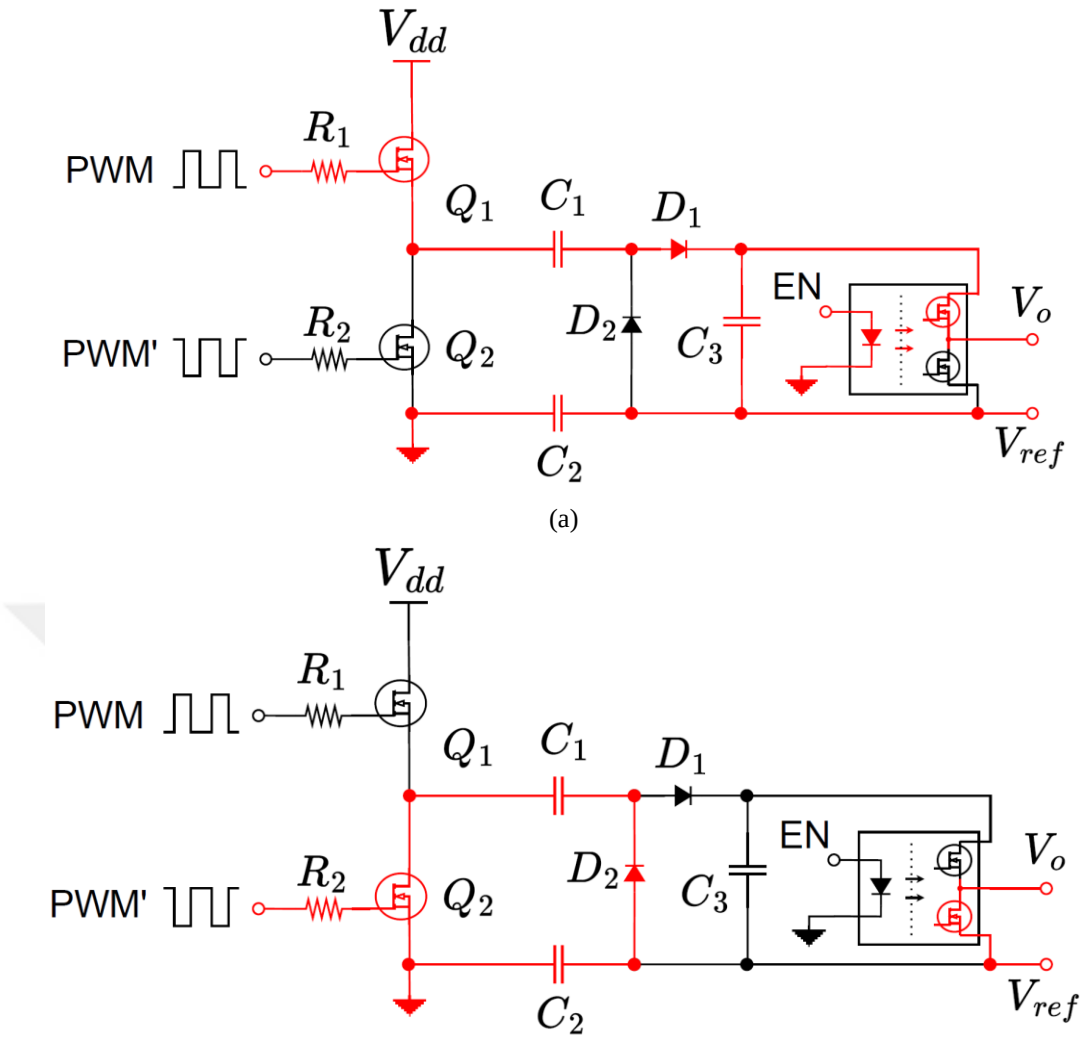


Figure 2.9 (a) State 1 of the IĆC driver, (b) state 2 of the IĆC driver

The State 1 operation of the gate driver is shown in Figure 2.9 (a). When the charge pump is considered in steady state, high side of the half bridge is active and the EN signal is logic high, the output is fed by the C_3 capacitor while the C_1 and C_2 capacitors charge the C_3 capacitor with V_{dd} voltage.

The State 2 operation of the gate driver is shown in Figure 2.9 (b). In this state, the charge pump is considered to be in steady state, low side of the half bridge is active, and the EN signal is logic low. Therefore, the output is grounded thanks to the optocoupler in the charge pump circuit, and the C_1 and C_2 capacitors are discharged with reverse current flow so that the C_3 capacitor can be charged.

State 1 Analysis:

While the Q_1 transistor is active, V_{dd} voltage boosts up the C_1 capacitor, and the C_3 capacitor is charged over the C_1 and C_2 capacitor, as in equations 2.42 and 2.43. The charge equation of C_3 capacitor is given in equation 2.44. On the other hand, the C_2 capacitor provides a GND reference.

$$R_{eq3} = r_{q1} + r_{c1} + r_{d1} + (r_{c3} // R_o) + r_{c2} \quad \textbf{(2.38)}$$

$$\tau_4 = R_{eq3} * C_1 \quad \textbf{(2.39)}$$

$$\tau_5 = R_{eq3} * C_2 \quad \textbf{(2.40)}$$

$$\tau_6 = R_{eq3} * C_3 \quad \textbf{(2.41)}$$

$$V_{C1} = V_{C1o} + (V_{dd} - V_{C1o} - V_{C2o} - V_{C3o} - V_{D1})(1 - e^{-t/\tau_4}) \quad \textbf{(2.42)}$$

$$V_{C2} = V_{C2o} + (V_{dd} - V_{C1o} - V_{C2o} - V_{C3o} - V_{D1})(1 - e^{-t/\tau_5}) \quad \textbf{(2.43)}$$

$$V_{C3} = V_{C3o} + (V_{dd} - V_{C1o} - V_{C2o} - V_{C3o} - V_{D1})(1 - e^{-t/\tau_6}) \quad \textbf{(2.44)}$$

State 2 Analysis:

While the Q_2 transistor is active, the C_2 capacitor is discharged with the C_1 capacitor voltage, and the charging equations are obtained as 2.48 and 2.49.

$$R_{eq1} = r_{c1} + r_{d2} + r_{c2} + r_{q2} \quad \textbf{(2.45)}$$

$$\tau_1 = R_{eq1} * C_1 \quad \textbf{(2.46)}$$

$$\tau_2 = R_{eq1} * C_2 \quad \textbf{(2.47)}$$

$$V_{C1} = (V_{C1o} - (-V_{C2o} + V_{D2} + V_{Q2}))(e^{-t/\tau_1}) \quad \textbf{(2.48)}$$

$$V_{C2} = -V_{C2o} + (V_{C1o} - (-V_{C2o} - V_{D2} - V_{Q2}))(1 - e^{-t/\tau_2}) \quad \textbf{(2.49)}$$

Since the EN signal is logic low, the output is grounded, and the output C_3 capacitor stays charged until the next state.

2.3 Switch Matrix

Thanks to the Switch Matrix, the energy can be transferred to each of the 8 battery cells individually. Each battery has positive and negative switches to direct the energy. Up to 4 cells in series can be balanced with this method. Both the positive and negative switches are composed of a diode and a MOSFET. While balancing, it is also aimed at controlling the temperature, voltage and charge states of the battery cells.

2.3.1 Switch Matrix Working Principle

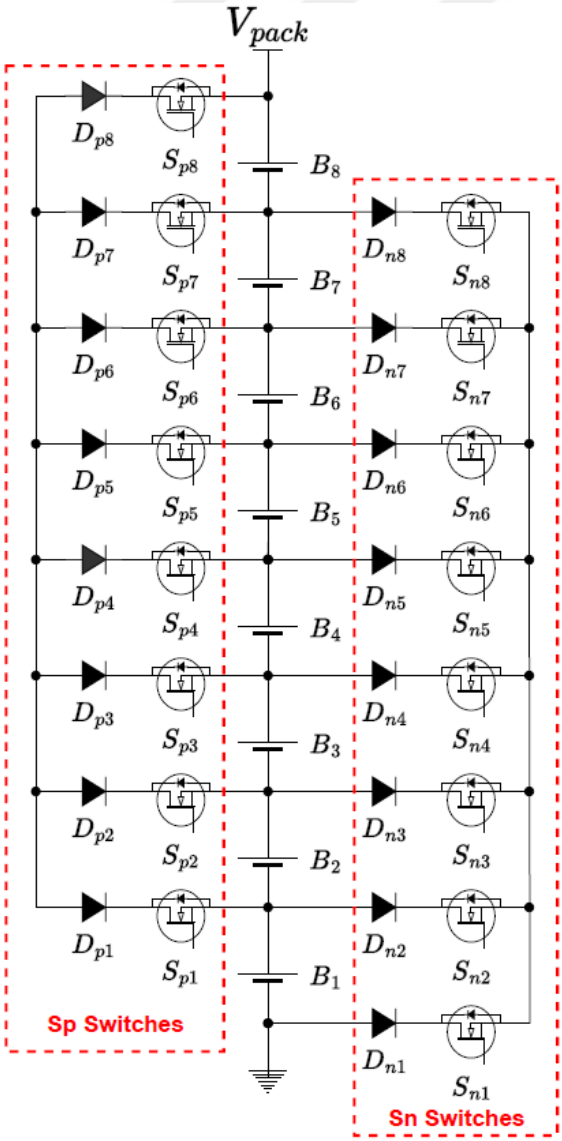


Figure 2.10 Switch matrix topology with battery cells

The SWM is used to select the desired battery cell or cells and create a connection with the IĆC output. As seen in Figure 2.10, the SWM comprises 8 positive switch (Sp) MOSFETs and 8 negative switch (Sn) MOSFETs. The Dp [1:8] and Dn [1:8] diodes are used to prevent short circuits. On the other hand, MOSFETs need a gate driver to be driven, but the source of each MOSFET has a different voltage level, and the gate to source drive voltage, V_{gs} of each MOSFET must be above the source voltage, V_s. That's why, a floating gate driver is required to drive each MOSFET. To produce floating V_{gs} voltages, the charge pump topology that is detailed previously in Section 2.2.4 is also implemented to drive SWM MOSFETs due to its simplicity, low power consumption and cost effectiveness.

2.3.2 Switch Matrix Gate Driver

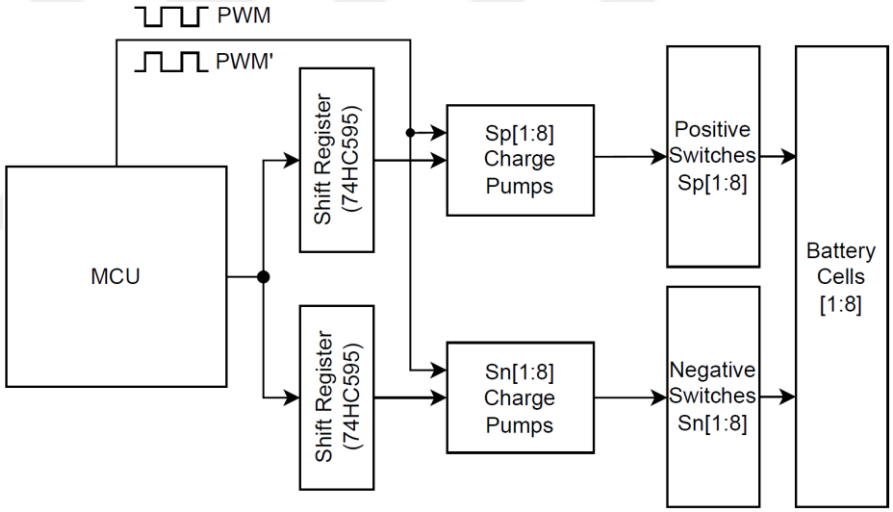


Figure 2.11 The block diagram of the SWM gate driver topology

BMS can select the battery cells that require balancing operation by the Sp and Sn switches that are driven with Sp and Sn charge pumps. The complementary PWM signals that are produced by the MCU charge all charge pumps in the SWM gate driver topology. Thus, the charge pumps become ready to select battery cells. However, selecting the required charge pumps for balancing operations becomes possible by using the 74HC595 shift registers that are commanded by the MCU as seen in Figure 2.11. There are two shift registers, and each of them has 8 outputs that are connected to the enable pins of the Sp and Sn charge pumps, respectively.

2.4 Controller

The BMS controller has three duties. These include monitoring the cells, controlling the converter, and switching the matrix. It is aimed at monitoring the temperature, voltage, current and SoC values of the battery cells. For the control of the IĆC, it is aimed at using PI control. For the switch matrix, an algorithm is planned. The IĆC output is directed to the detected low-charged battery cells.

2.4.1 IĆC Controller

The current input that is measured from the output of the IĆC is compared with the reference current. An error is obtained from the comparison and amplified with a PI controller block. The amplified output is a duty magnitude that will be used to produce a complementary PWM signal pair for S_{w1} and S_{w2} MOSFETs.
To operate IĆC steadily, the proportion, K_p, and integration, K_i, coefficients of the PI controller must be tuned properly. Therefore, the mathematical analysis of the IĆC is done to calculate the PI controller coefficients according to the studies in the literature [87-88]. With the help of mathematical analysis, the transfer function of the IĆC is obtained and used for calculating the optimum PI coefficients.

Table 2.4 Equations of passive components for state 1 and state 2 of IĆC

State 1 Equations	State 2 Equations
$\frac{dI_{L1}}{dt} = \frac{1}{L1}(V_{in})$	$\frac{dI_{L1}}{dt} = \frac{1}{L1}(V_{in} + \frac{V_{C2}}{n} - V_{C1})$
$\frac{dV_{C1}}{dt} = \frac{1}{C1} * (I_{Lm} - n * I_{L2})$	$\frac{dV_{C1}}{dt} = \frac{1}{C1} * (I_{L1})$
$\frac{dI_{Lm}}{dt} = \frac{1}{Lm}(-V_{C1})$	$\frac{dI_{Lm}}{dt} = \frac{1}{Lm}(-\frac{V_{C2}}{n})$
$\frac{dV_{C2}}{dt} = \frac{1}{C2}(I_{L2})$	$\frac{dV_{C2}}{dt} = \frac{1}{C2}\left(-\frac{(I_{L1} - I_{Lm})}{n}\right)$
$\frac{dI_{L2}}{dt} = \frac{1}{L2}(-V_{C2} + n * V_{C1} - V_{Co})$	$\frac{dI_{L2}}{dt} = \frac{1}{L2}(-V_{Co})$
$\frac{dV_{Co}}{dt} = \frac{1}{Co}(I_{L2} - \frac{V_{Co}}{R})$	$\frac{dV_{Co}}{dt} = \frac{1}{Co}(I_{L2} - \frac{V_{Co}}{R})$

On the other hand, a transfer function calculation requires an input state space equation 2.50 and an output state space equation 2.51 [89-92].

$$x^* = A * x + B * u \tag{2.50}$$

$$y = C * x + D * u \tag{2.51}$$

To obtain the state space equations, Kirchoff Voltage Law, KVL, and Kirchoff Current Law, KCL, are applied separately to state 1 and state 2 of the IĆC as shown in Figure 2.3. Thus, the equations of the passive elements in the IĆC are obtained for both state 1 and state 2 operations, as shown in Table 2.4.

State 1 input equation 2.52 and state 2 input equation 2.53 are obtained by transforming the obtained equations in Table 2.4 into matrix format.

$$x^* = A_1 * x + B_1 * u \tag{2.52}$$

$$x^* = A_2 * x + B_2 * u \tag{2.53}$$

The state 1 and state 2 matrix equations are obtained as below.

$$\begin{bmatrix} I_{L1}^* \\ V_{C1}^* \\ I_{Lm}^* \\ V_{C2}^* \\ I_{L2}^* \\ V_{Co}^* \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1/C1 & 0 & -n/C1 & 0 \\ 0 & -1/Lm & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1/C2 & 0 \\ 0 & n/L2 & 0 & -1/L2 & 0 & -1/L2 \\ 0 & 0 & 0 & 0 & 1/Co & -1/(RCo) \end{bmatrix} * \begin{bmatrix} I_{L1} \\ V_{C1} \\ I_{Lm} \\ V_{C2} \\ I_{L2} \\ V_{Co} \end{bmatrix} + \begin{bmatrix} 1/L1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} * V_{in} \tag{2.54}$$

$$\begin{bmatrix} I_{L1}^* \\ V_{C1}^* \\ I_{Lm}^* \\ V_{C2}^* \\ I_{L2}^* \\ V_{Co}^* \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L1} & 0 & \frac{1}{nL1} & 0 & 0 \\ \frac{1}{C1} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{nLm} & 0 & 0 \\ -\frac{1}{nC2} & 0 & \frac{1}{nC2} & 0 & 0 & -\frac{1}{L2} \\ 0 & 0 & 0 & 0 & \frac{1}{Co} & -\frac{1}{RCo} \\ 0 & & 0 & 0 & & \end{bmatrix} * \begin{bmatrix} I_{L1} \\ V_{C1} \\ I_{Lm} \\ V_{C2} \\ I_{L2} \\ V_{Co} \end{bmatrix} +$$

$$\begin{bmatrix} 1/L1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} * V_{in} \tag{2.55}$$

The output equations below are calculated for state 1 and state 2,

$$y = C_1 * x + D_1 * u \quad \textbf{(2.56)}$$

$$y = C_2 * x + D_2 * u \quad \textbf{(2.57)}$$

and the matrix representation of state 1 and state 2 are obtained as below.

$$\begin{bmatrix} V_o \\ I_o \\ I_{in} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} * \begin{bmatrix} I_{L1} \\ V_{C1} \\ I_{Lm} \\ V_{C2} \\ I_{L2} \\ V_{Co} \end{bmatrix} + [0] * V_{in} \quad \textbf{(2.58)}$$

$$\begin{bmatrix} V_o \\ I_o \\ I_{in} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} * \begin{bmatrix} I_{L1} \\ V_{C1} \\ I_{Lm} \\ V_{C2} \\ I_{L2} \\ V_{Co} \end{bmatrix} + [0] * V_{in} \quad \textbf{(2.59)}$$

The obtained input state space and output equations are used to calculate the transfer function of the IĆC, but they are calculated for state 1 and state 2 separately. It is needed to take an average of the obtained input and output state space equations. When the duty ratio of state 1, d, and the duty ratio of state 2, 1-d, are taken into account, the equations 2.60 and 2.61 are used to calculate an averaged input state space equation, while the equations 2.62 and 2.63 are used to calculate an averaged output equation.

$$\mathrm{A} = [A_1 * (d) + A_2 * (1 - d)] \quad \textbf{(2.60)}$$

$$\mathrm{B} = [B_1 * (d) + B_2 * (1 - d)] \quad \textbf{(2.61)}$$

$$\mathrm{C} = [C_1 * (d) + C_2 * (1 - d)] \quad \textbf{(2.62)}$$

$$\mathrm{D} = [D_1 * (d) + D_2 * (1 - d)] \quad \textbf{(2.63)}$$

The equations below are the calculations for IĆC to obtain averaged equations. The average of matrix, A, contains the parameters of the passive elements, and B contains the parameters of the input elements. Also, the average of matrix C contains the relations of passive elements with output elements. Since there is no direct relationship between the input and output elements, the average of matrix D is equal to zero.

$$A = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1/C_1 & 0 & -n/C_1 & 0 \\ 0 & -1/L_m & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1/C_2 & 0 \\ 0 & n/L_2 & 0 & -1/L_2 & 0 & -1/L_2 \\ 0 & 0 & 0 & 0 & 1/C_o & -1/(RC_o) \end{bmatrix} * d$$

$$+ \begin{bmatrix} 0 & -1/L_1 & 0 & 1/(nL_1) & 0 & 0 \\ 1/C_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1/(nL_m) & 0 & 0 \\ -1/(nC_2) & 0 & 1/(nC_2) & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1/L_2 \\ 0 & 0 & 0 & 0 & 1/C_o & -1/(RC_o) \end{bmatrix} * (1-d) \quad \textbf{(2.64)}$$

$$A = \begin{bmatrix} 0 & (d-1)/L_1 & 0 & (1-d)/nL_1 & 0 & 0 \\ (1-d)/C_1 & 0 & d/C_1 & 0 & -dn/C_1 & 0 \\ 0 & -d/L_m & 0 & (d-1)/nLm & 0 & 0 \\ (d-1)/nC_2 & 0 & (1-d)/nC_2 & 0 & d/C_2 & 0 \\ 0 & dn/L_2 & 0 & -d/L2 & 0 & -1/L_2 \\ 0 & 0 & 0 & 0 & 1/C_o & -1/(RC_o) \end{bmatrix} \quad \textbf{(2.65)}$$

$$B = \begin{bmatrix} 1/L_1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} * d + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} * (1-d) \quad \textbf{(2.66)}$$

$$B = \begin{bmatrix} 1/L_1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad \textbf{(2.67)}$$

$$C = C_1 = C_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \mathrm{D} = 0 \quad \textbf{(2.68)}$$

Average matrix models are obtained from the state 1 and state 2 matrix representations by multiplying with the duty ratio, as seen in the equations above. The average matrix representation is shown below.

$$x^* = A * x + B * u \quad \textbf{(2.69)}$$

$$y = C * x + D * u \quad \textbf{(2.70)}$$

The large signal model is obtained by using average matrix models. The values that are used in matrix representations consist of steady state and small signal values. The steady state values are the equilibrium point of the converter, and they

are used to design the converter. On the other hand, the small signal values are the small deviations of the converter, and they are used to design the controller. Both steady state and small signal values are required so that the controller can be designed, and the math model of the converter can be calculated.

Large signal model is calculated with the equation below.

$$\dot{x} = A * x + B * u \tag{2.71}$$

Steady state model is calculated with the equation below.

$$\dot{X} = A * X + B * U = 0 \tag{2.72}$$

Small signal model is calculated with the equation below.

$$\dot{\hat{x}} = A * \hat{x} + B * \hat{u} \tag{2.73}$$

The large signal values can be split into its steady state and small signal components by using the equations given below.

$$\dot{x} = (\dot{X + \hat{x}}) \tag{2.74}$$

$$x = \mathrm{X} + \hat{x} \tag{2.75}$$

$$y = \mathrm{Y} + \hat{y} \tag{2.76}$$

$$u = \mathrm{U} + \hat{u} \tag{2.77}$$

$$d = D + \hat{d} \tag{2.78}$$

After the values are split, the exploded equations are obtained as below. In further steps, these equations will be simplified by using the assumptions below.

$$(\dot{X + \hat{x}}) = [A_1(D + \hat{d}) + A_2(1 - D - \hat{d})] * (\mathrm{X} + \hat{x}) +$$

$$[B_1(D + \hat{d}) + B_2(1 - D - \hat{d})] * (\mathrm{U} + \hat{u}) \tag{2.79}$$

$$(\mathrm{Y} + \hat{y}) = [C_1(D + \hat{d}) + C_2(1 - D - \hat{d})] *$$

$$(\mathrm{X} + \hat{x}) + [0] * (\mathrm{U} + \hat{u}) \tag{2.80}$$

Assumptions:

1- Small signal values are too small when compared with the steady state values ($\frac{\hat{x}}{X} \ll 1$), therefore, multiplication of two small signal ($\hat{x} * \hat{d}$) is neglected.

2- Derivative of the steady state signal ($\frac{dX}{dt} = 0$) is equal to zero because the steady state values are constant.

3- In the steady state analysis, derivative of X is assumed as zero because it is constant. Therefore, the equation below is obtained. The obtained equation is then used to find output value of Y.

$$\dot{X} = A * X + B * U = 0 \quad \textbf{(2.81)}$$

$$A * X = -B * U \quad \textbf{(2.82)}$$

$$\mathrm{X} = -A^{-1} * B * U \quad \textbf{(2.83)}$$

$$Y = C * X + D * U = C * X \quad \textbf{(2.84)}$$

$$Y = -C * A^{-1} * B * U \quad \textbf{(2.85)}$$

By applying the assumptions above, the state space and output equations can be simplified as below. In the output equation, the input parameters are eliminated because D is equal to zero and C_1 is equal to C_2.

$$\dot{\hat{x}} = A * \hat{x} + B * \hat{u} + [(A_1 - A_2)(X) + (B_1 - B_2)(\mathrm{U})\,] * (\hat{d}) \quad \textbf{(2.86)}$$

$$\hat{y} = C * \hat{x} \quad \textbf{(2.87)}$$

In the final situation, the small signal equations of the IĆC are obtained as below. The input parameters of the IĆC can be selected as input voltage and duty ratio, and the output parameters can be selected as output voltage, output current and input current.

$$\begin{bmatrix} \dot{\hat{\imath}}_{L1} \\ \dot{\hat{v}}_{C1} \\ \dot{\hat{\imath}}_{Lm} \\ \dot{\hat{v}}_{C2} \\ \dot{\hat{\imath}}_{L2} \\ \dot{\hat{v}}_{Co} \end{bmatrix} = \begin{bmatrix} 0 & \frac{D-1}{L_1} & 0 & \frac{1-D}{nL_1} & 0 & 0 \\ \frac{1-D}{C_1} & 0 & \frac{D}{C_1} & 0 & -\frac{Dn}{C_1} & 0 \\ 0 & -\frac{D}{L_m} & 0 & \frac{D-1}{nL_m} & 0 & 0 \\ \frac{D-1}{nC_2} & 0 & \frac{1-D}{nC_2} & 0 & \frac{D}{C_2} & -\frac{1}{L_2} \\ 0 & \frac{Dn}{L_2} & 0 & -\frac{D}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_o} & -\frac{1}{RC_o} \end{bmatrix} \begin{bmatrix} \hat{\imath}_{L1} \\ \hat{v}_{C1} \\ \hat{\imath}_{Lm} \\ \hat{v}_{C2} \\ \hat{\imath}_{L2} \\ \hat{v}_{Co} \end{bmatrix} +$$

$$\begin{bmatrix} 1/L_1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_{in} + \begin{bmatrix} (nV_{C1}-V_{C2})/nL_1 \\ (-I_{L1}+I_{Lm}-I_{L2}n)/C_1 \\ (-nV_{C1}+V_{C2})/nL_m \\ (I_{L1}-I_{Lm}+nI_{L2})/nC_2 \\ (nV_{C1}-V_{C2})/L_2 \\ 0 \end{bmatrix} \hat{d} \quad \textbf{(2.88)}$$

$$\begin{bmatrix} \dot{\hat{v}}_o \\ \dot{\hat{\imath}}_o \\ \dot{\hat{\imath}}_{in} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} * \begin{bmatrix} \hat{\imath}_{L1} \\ \hat{v}_{C1} \\ \hat{\imath}_{Lm} \\ \hat{v}_{C2} \\ \hat{\imath}_{L2} \\ \hat{v}_{Co} \end{bmatrix} \quad \textbf{(2.89)}$$

The duty is selected as input and the output current is selected as output for the IĆC system. Later, the transfer function is obtained as below by using the state equations.

$$\frac{\hat{\imath_o}}{\hat{d}} = C * [s * I - A]^{-1} * [B] =$$

$$\frac{1.651e5*s^5+3.504e8*s^4+4.703e12*s^3+1.152e16*s^2+1.651e19*s+9.974e22}{s^6+2515*s^5+8.887e7*s^4+9.039e10*s^3+1.837e15*s^2+5.16e17*s+7.851e21} \quad \textbf{(2.90)}$$

Finally, the P and I coefficients are obtained by using the transfer function above in MATLAB PID toolbox and given in Table 2.5.

Table 2.5 Obtained values of P and I coefficients

Coefficients	Value
P	0.00093639
I	6.3276

2.4.2 CSA Algorithm

The CSA initiates the process by collecting samples of the OCV of the battery cells, as depicted in Figure 2.12. Subsequently, it computes the mean of these cell voltages to facilitate their comparison. The voltage of each battery cell is compared to the average voltage of all the cells. If the voltages of all the batteries are within a specific tolerance of the average voltage, then the cell voltages are considered balanced, and the balancing process becomes passive. In contrast, when an imbalance is noticed, the balancing process is initiated. The measured cell voltages are arranged in ascending order. Hence, the cell with the least charge is identified. Furthermore, the cells that are connected in series with the cell that has the least charge are evaluated to determine if their voltage is lower than the average voltage of all the cells. The cell with the least charge and its series cells that have a voltage below the average are chosen for balancing. Next, the SWM is set up for the chosen cells, and the IĆC is activated to initiate power transmission as P2C. The cell voltages, input current and output current of the IĆC are continuously monitored after the initiation of the balance operation. Following the application of a low-pass filter, the voltage drops across the battery cells are determined and then subtracted from the voltage of each cell in order to estimate the open circuit voltage. The acquired cell voltages are subsequently utilized to determine the SoC levels of the cells and compare them to the mean cell voltage. CSA ends balance operation when the cell voltages are equalized. Otherwise, the balancing procedure proceeds. The time interval for battery balance operation is determined to be 60 seconds, which is considered the optimal value for securely reconfiguring the SWM and reducing computing work. The balance process is periodically paused to evaluate the OCV of each cell, revise the average voltage and reorganize the battery cell voltages for the upcoming SWM configuration, which occurs every 60 seconds. Next, the balance operation proceeds by initiating the IĆC and setting up the SWM configuration.

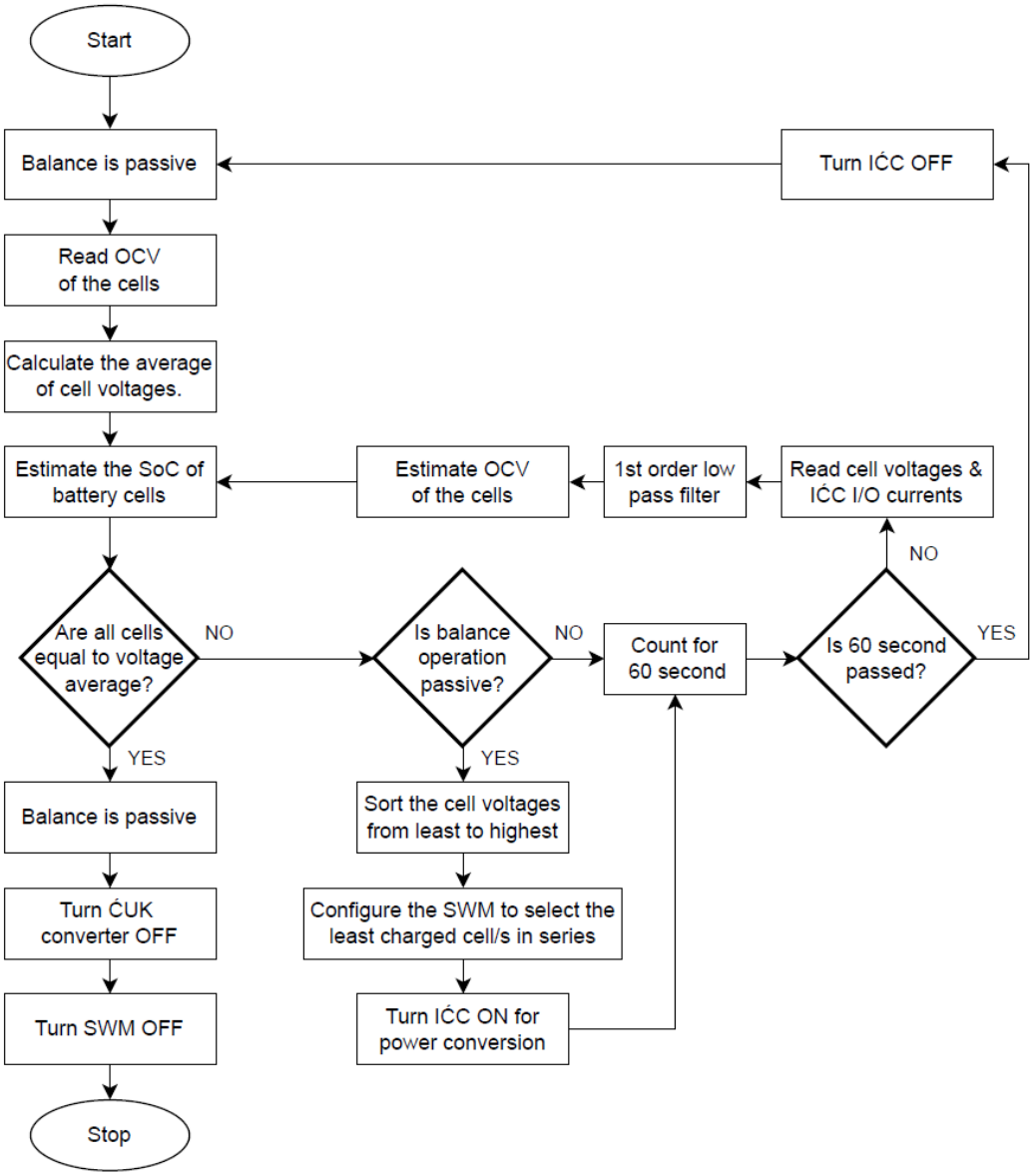


Figure 2.12 Battery balance algorithm of CSA

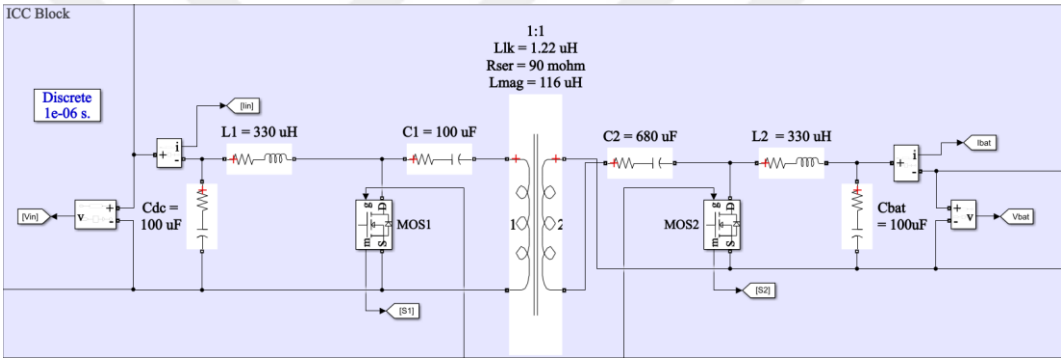
CHAPTER 3

RESULTS & DISCUSSION

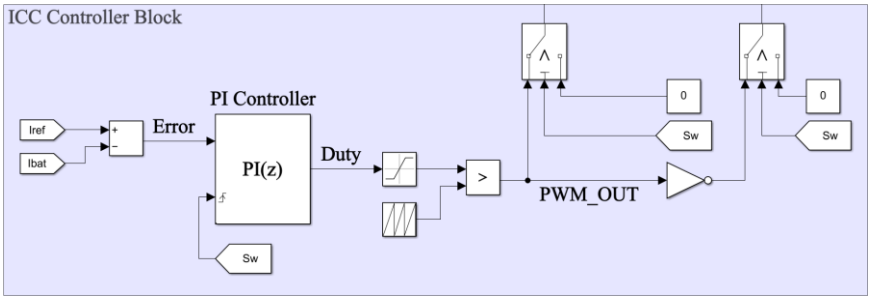
3.1 Simulation & Experimental Implementation

The proposed balance topology is simulated using MATLAB Simulink and then implemented experimentally to validate the simulation results.

3.1.1 Balancing Circuit Implementation



(a)

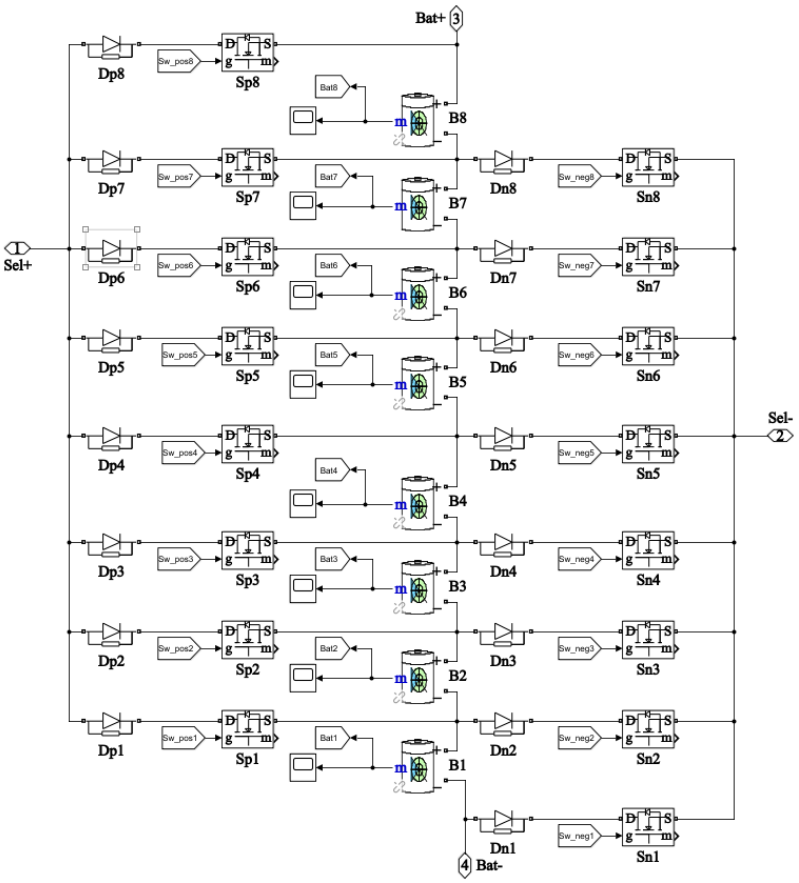


(b)

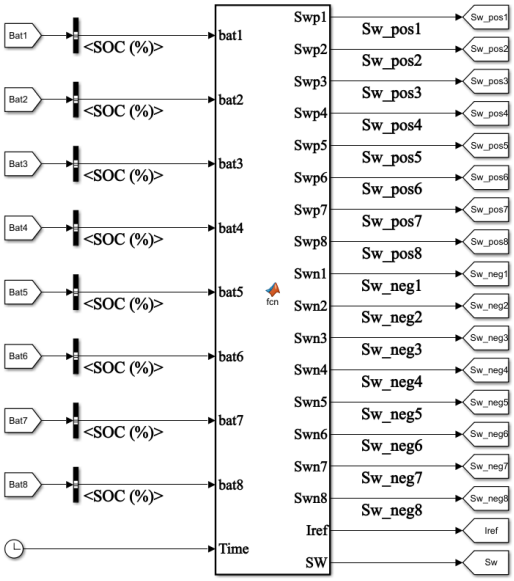
Figure 3.1 (a) The implemented block diagram of IĆC, (b) the implemented block diagram of IĆC controller

Figure 3.1 displays the block diagrams of the IĆC and the simulation parameters. The IĆC topology is controlled by the PI controller, as depicted in Figure 3.1 (b). The PI controller can be activated or deactivated in simulation as required while balancing the cell voltages. Figure 3.2 displays the block schematics of the SWM, BMS controller, and batteries. The batteries are set to

operate at nominal voltage levels of 3.65V and have a capacity of 2.8 Ah. Furthermore, the SWM is coupled to the batteries for the purpose of selection. The BMS controller contains the CSA algorithm, which enables it to control the gate signals of the SWM and IĆC controllers in the presence of a SoC imbalance.



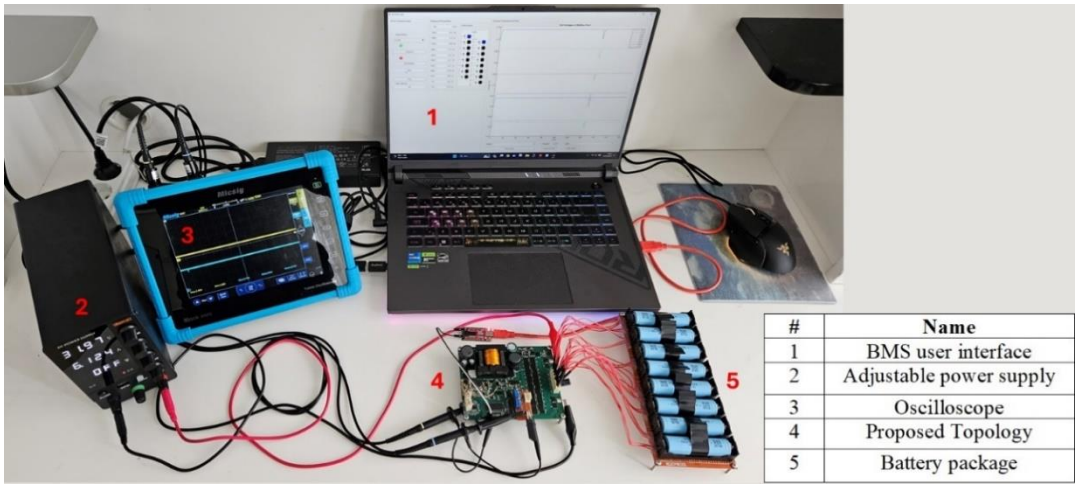
(a)



(b)

Figure 3.2 (a)Block diagrams of the batteries and SWM, (b) block diagram of the BMS controller

Figure 3.3 displays the experimental implementation of the proposed topology. The BMS architecture is powered by a power supply and the battery package. The input and output measurements are acquired through the utilization of an oscilloscope and a BMS user interface.



#	Name
1	BMS user interface
2	Adjustable power supply
3	Oscilloscope
4	Proposed Topology
5	Battery package

Figure 3.3 The experimental setup photograph of the proposed balance topology

As shown in Figure 3.4, the obtained parameters of the proposed BMS topology and the battery pack are monitored in the BMS user interface. Moreover, the monitored data can be saved in the user interface so that it can be analyzed later. A serial communication port connects the proposed BMS circuit board to the user interface. Later, the voltage levels of the battery cells are entered into the graph,

which is named “Cell Voltages of Battery Pack.” The balancing operation outputs of the experimental study are later obtained from that graph in this thesis. Also, the selection configuration of the SWM is visualized in the user interface, thus, the selected battery cells can be distinguished throughout the balance operation. In addition to these features, the user interface monitors the temperatures of battery cells, input current, and output current values. The experimental BMS parameters of the studies in literature are also obtained by using an oscilloscope or a user interface [33,48].

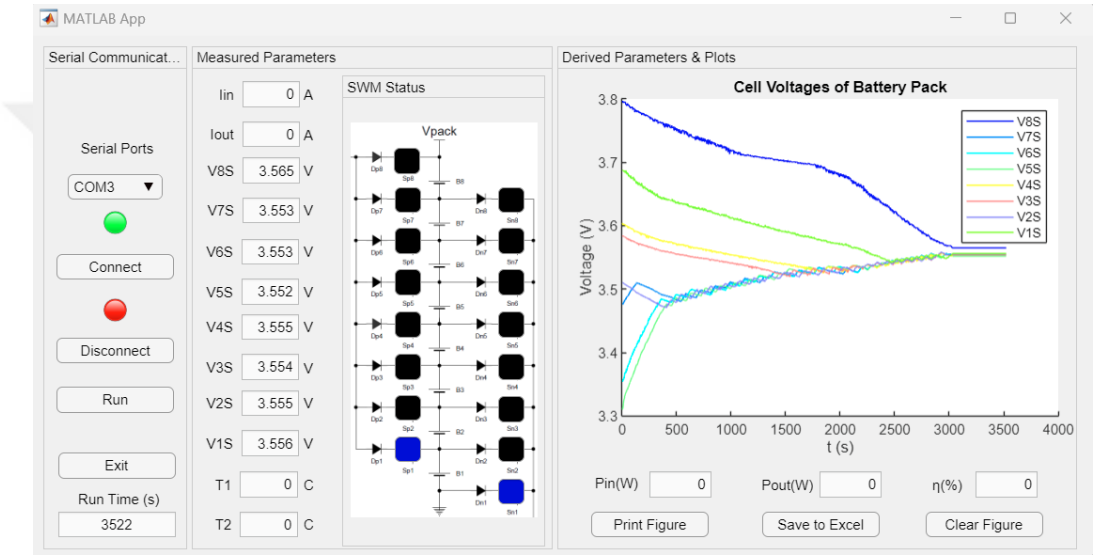
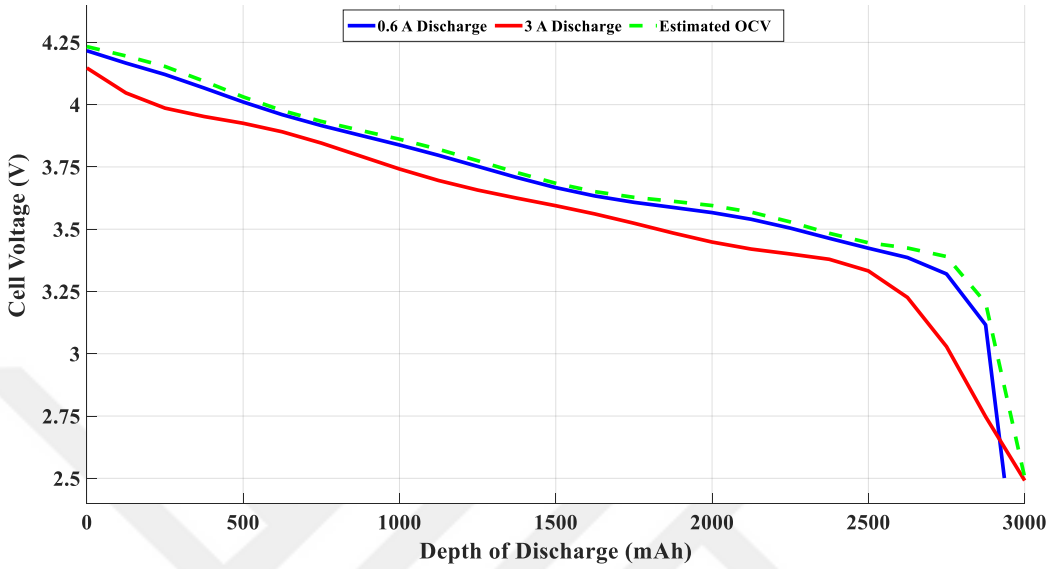


Figure 3.4 BMS user interface

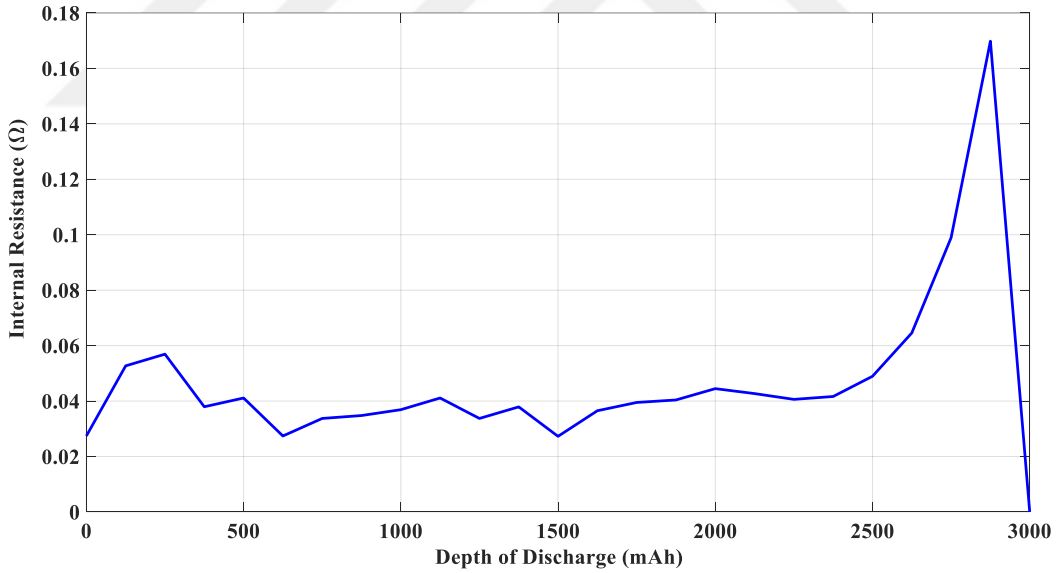
3.2 SoC Estimation

The calculations begin by discharging the battery cells from the highest voltage level of 4.25 V to the lowest voltage level of 2.5 V using current levels of 3A and 0.6A. The discharge curve of the battery cells is determined from the data shown in Figure 3.5. The purpose of these curves is to generate a look-up table that is later used to estimate the SoC level and internal resistance of battery cells. These curves are shown in Figure 3.5 (a) and Figure 3.5 (b). The internal resistance curve is used to determine the OCV of the battery cells during charging or discharging, while proceeding with cell balancing. Thus, the OCV is determined by using the observed cell voltages in equation 1.1. The depth of discharge (DoD) curve points of 3A are used to estimate the DoD level of OCVs utilizing the same formula. So, a projected DoD curve is derived based on the

OCV, as shown in Figure 3.5 (a). Next, the OCV of each cell is determined by using the curves shown in Figure 3.5 (b). The acquired DoD is then used to estimate the SoC percentage of each cell by using equation 1.3.



(a)



(b)

Figure 3.5 (a)The depth of discharge curves that belongs to the battery cells, (b) the calculated internal resistance curve of the battery cells

3.3 Efficiency Calculations

The experimental study is evaluated based on the performance of efficiency in the practical circuitry, as seen in Figure 3.6. The efficiency graph is generated by

modifying the SWM output to select four cells in series. The voltage of each cell is tuned around 3.8V, and the IĆC charges the chosen cells using a current range of 1 A to 3.5A. The MATLAB user interface allows for the sampling of current and voltage measurements on both the input and output sides. Then, these parameters are used to compute efficiency and plot a curve fitted graph of efficiency vs current. As a result, the experimental circuit achieves a maximum efficiency of 81.98% with a balancing current of around 3 A.

After the literature studies are researched, it is seen that there are four methods of efficiency calculation, which are loss analysis, resistive loads, constant battery operation, and balancing operation. The loss analysis method includes the power loss of each component in the BMS topology [69]. The total of the power losses is then used to calculate the efficiency. Since the loss analysis does not have an experimental result, the real efficiency might be different due to the unforeseen disturbances. The efficiency calculation over a resistor at the output gives an experimental result, but that does not belong to a battery operation [52]. Therefore, constant battery operation is used to obtain the efficiency of BMS in existence of batteries [51]. This method is good for the BMS topologies that operate with intervals. On the other hand, efficiency can be calculated while a continuous battery balancing operation exists [43]. This method is a good solution for continuously operating BMS systems. As a result, the efficiency of the proposed topology is calculated with constant battery operation.

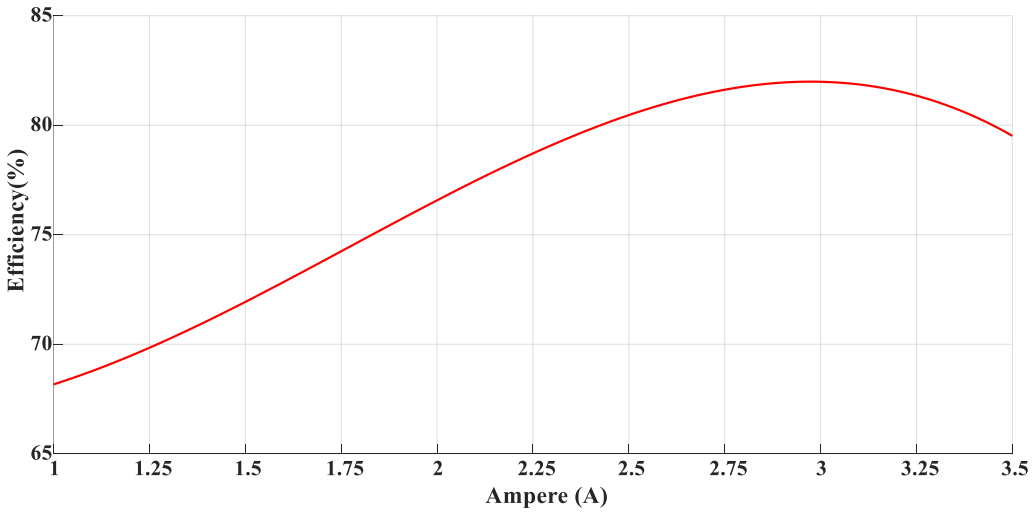
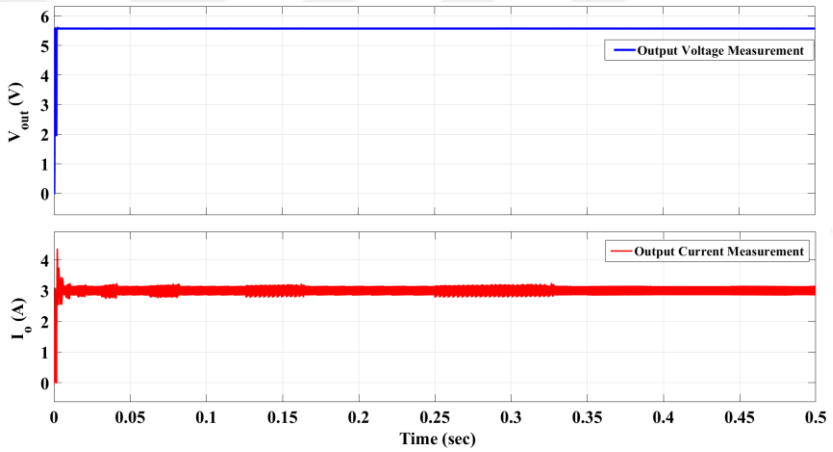


Figure 3.6 Measured efficiency for the proposed balance topology

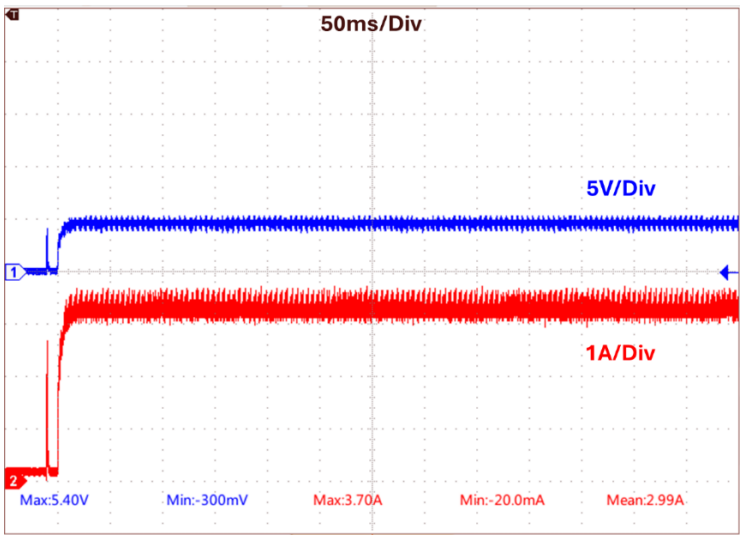
3.4 Simulation & Experimental Results

3.4.1 Operational Outputs of ICC

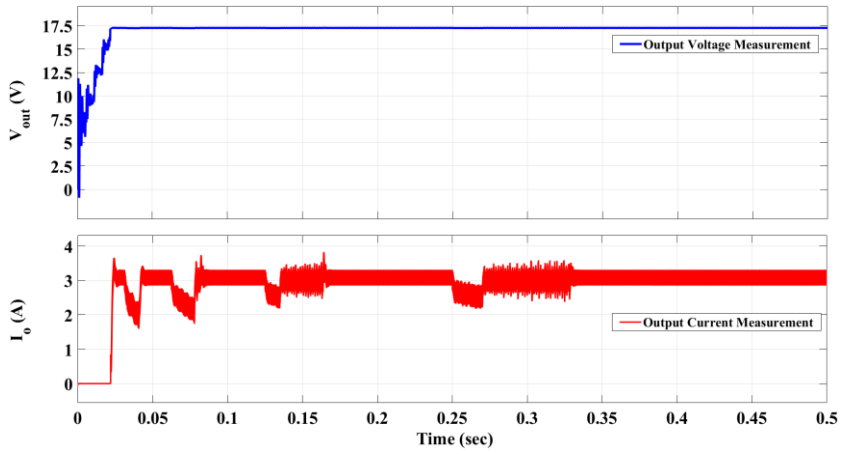
Figure 3.7 displays the voltage and current outputs of the ICC when the battery pack is unbalanced. For the balancing of a single cell, the simulation and experimental data are displayed in Figure 3.7 (a) and Figure 3.7 (b), respectively. The output voltage stays steady at the charging voltage of a single cell, while the balance current is steady at around 3A. During the operation of balancing for four cells in series, the simulation and experimental results are displayed in Figure 3.7 (c) and Figure 3.7 (d), respectively. The current becomes stable at the 3A equilibrium current, while the output voltage settles at the voltage required for charging four cells.



(a)



(b)



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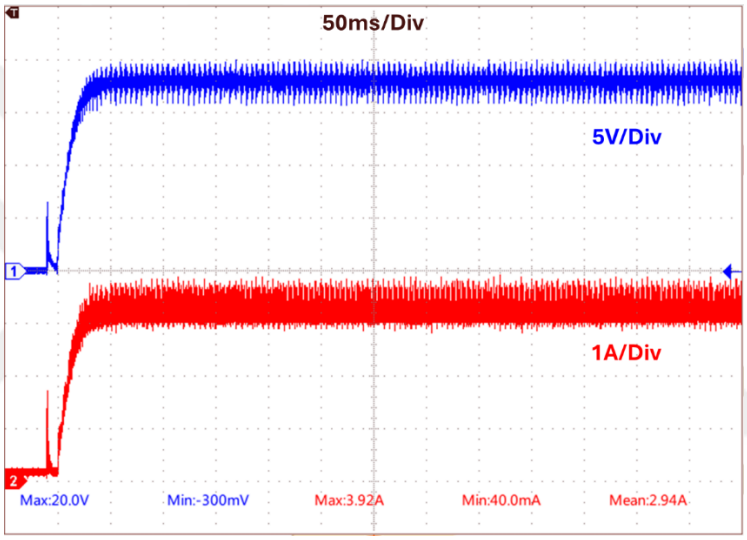
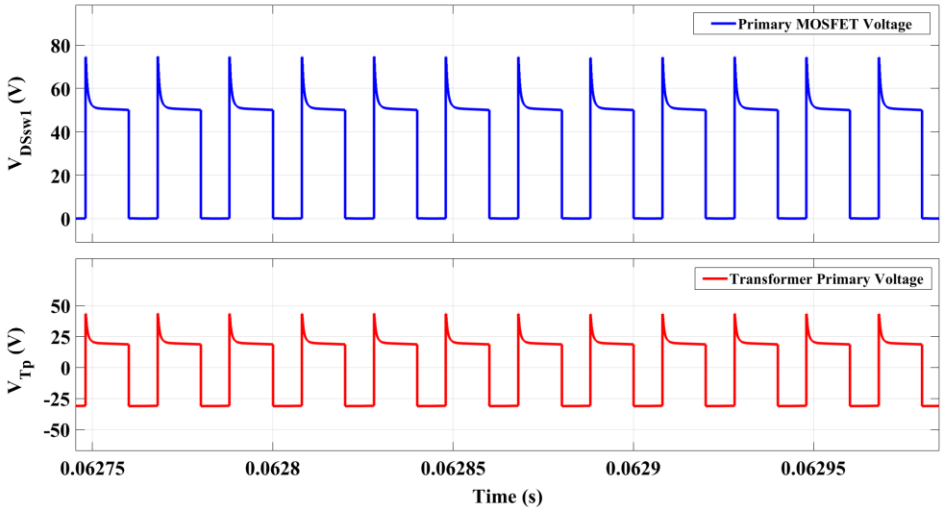


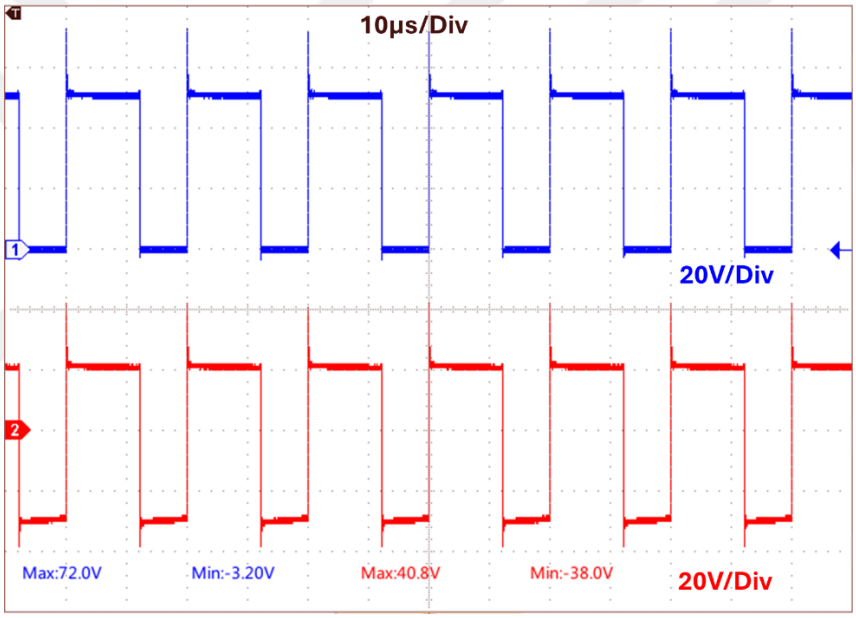
(d)

Figure 3.7 Cell balance outputs for simulation: (a) 1S cell balance, (c) 4S cell balance and cell balance outputs for experiment: (b) 1S cell balance, (d) 4S cell balance

During the operation of the IĆC for balancing four cells in series, the primary MOSFET experiences a voltage stress that is equal to the sum of the input and output voltages. This stress can reach up to 50 V, as depicted in Figure 3.8 (a). However, the voltage level exhibits sudden spikes due to the presence of the primary inductor, L_1, and the inductance of the transformer's magnetizing circuit, L_m. Hence, an RC snubber circuit is implemented to reduce the spikes on MOSFETs, thus, a maximum 75 V spike is observed. The primary voltage of the transformer is equal to the input voltage while in the ON state and equal to the output voltage while in the OFF state. The experimental result depicted in Figure 3.8 (b) is also compatible with the simulation result.



(a)



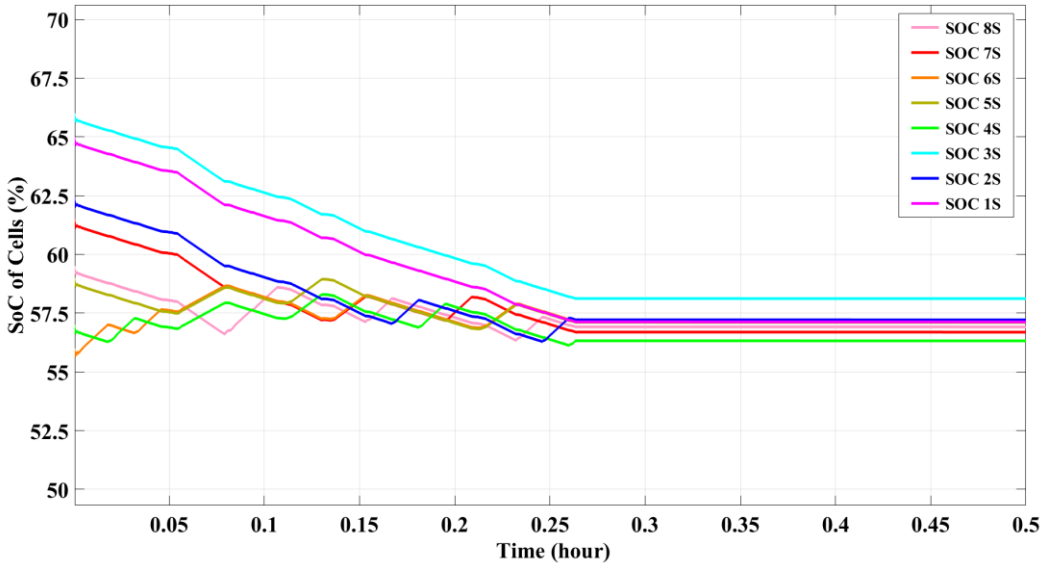
(b)

Figure 3.8 (a) IĆC voltage measurements in simulation, (b) IĆC voltage measurements in experiment

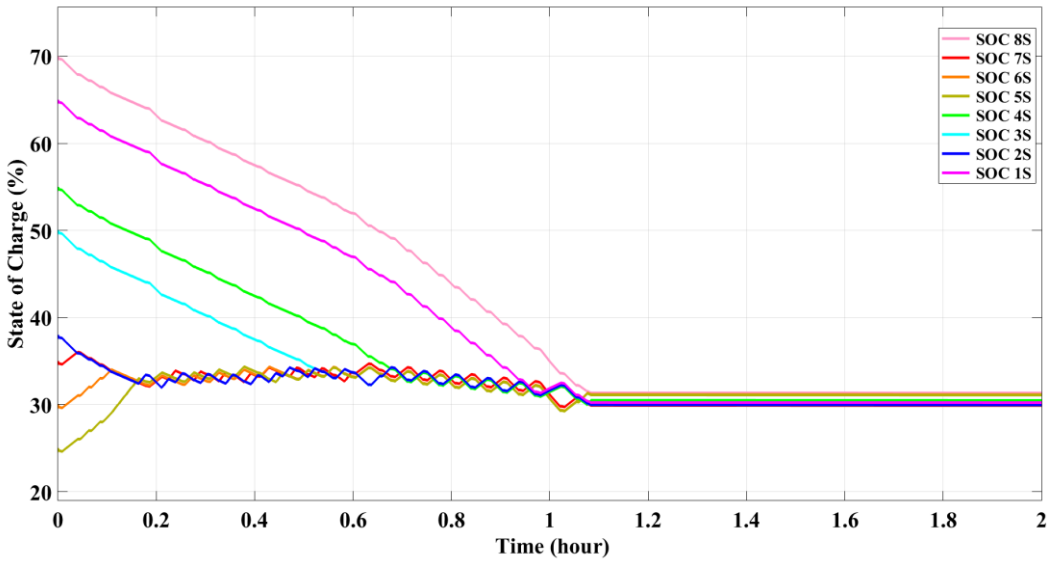
3.4.2 Battery Cell Balancing Results

The balance procedure is simulated using MATLAB Simulink, and the resulting output is depicted in Figure 3.9. Figure 3.9 (a) displays the initial outcome of the battery balance simulation. The SoC levels of the battery cells is initially configured as follows: 59.5%, 61.5%, 56%, 59%, 57%, 66%, 62.5%, and 65%, from the 8th cell to the 1st cell. The maximum SoC imbalance in the current configuration is 10%. Under those circumstances, the balance procedure is

completed within a duration of 15 minutes, equivalent to a quarter of an hour. The resulting SoC levels are 57±1%. Figure 3.9 (b) displays the second attempt. The SoC levels of the battery cells are initially set to 70%, 35%, 30%, 27%, 55%, 50%, 38%, and 65%, respectively. Initially, the SoC difference between the highest and lowest SoC is 43%. The ultimate SoC levels falls within the range of 30% and 32%. The process of balancing required a duration of one hour and six minutes.



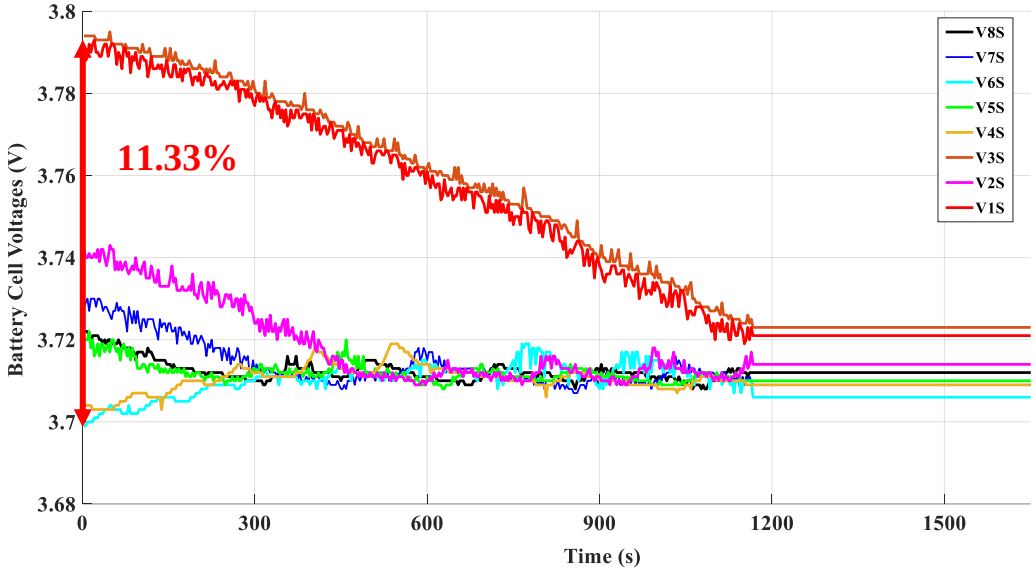
(a)



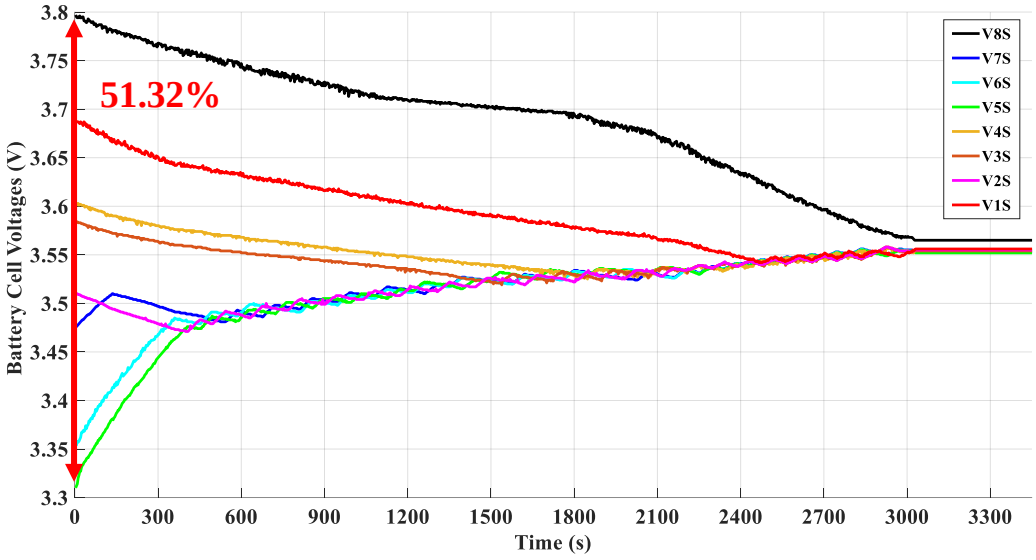
(b)

Figure 3.9 (a) Simulation result of first battery balancing attempt, (b) simulation result of second battery balancing attempt

The BMS user interface, created in MATLAB, collects the balance operation data from the BMS circuit board. The collected data is used later to graph the experimentally executed BMS topological outcomes, as depicted in Figure 3.10. Figure 3.10 (a) displays the initial test of the experimentally applied BMS topology. The initial voltages of the battery cells are 3.722 V, 3.728 V, 3.699 V, 3.720 V, 3.704 V, 3.794 V, 3.742 V, and 3.791 V, starting from the 8th cell and ending with the 1st cell. The calculated SoC imbalance is 11.33% between the cells that are charged the most and the cells that are charged the least. Subsequently, the battery cells complete the balancing process after 1170 seconds, equivalent to 19 minutes and 30 seconds. Upon completion of the balance operation, the voltage levels reach a final measurement of 3.715±0.01 V. Figure 3.10 (b) displays the second attempt. Before starting the balance operation, the cell voltages are adjusted to 3.797 V, 3.476 V, 3.355 V, 3.310 V, 3.604 V, 3.583 V, 3.510 V, and 3.688 V, respectively. The calculated SoC difference between the cell with the greatest voltage and the cell with the lowest voltage is 51.32%. After completion of the balance process, the cell voltages measure 3.559±0.01 V. The duration of the balance process is approximately 3033 seconds, equivalent to 50 minutes and 33 seconds.



(a)



(b)

Figure 3.10 (a) Experimental result of first battery balancing attempt, (b) experimental result of second battery balancing attempt

3.4.3 Comparison with other Studies

Table 3.1 provides a comparison of the P2C studies based on their speed, efficiency, and complexity. The predicted balancing speed parameters are obtained by dividing the stated voltage by the balancing times. Furthermore, the articles that publish the unbalanced amount as a SoC difference are transformed into voltage ranges in order to evaluate their corresponding performances. The proposed topology exhibits superior balancing speed due to the high-power capacity of the PI driven IĆC and the ability of SWM to select up to four cells in a row, while maintaining moderate efficiency. The complexity of the proposed topology is reduced due to the utilization of a single transformer and the absence of PWM-driven cell selection switches.

Table 3.1 Comparisons of balancing speed, efficiency and control difficulty of the proposed study and the topologies in literature

P2C Studies	Balancing Speed	Efficiency	Complexity
Multiple Transformer [47]	7.60 mV/min – Very High	90% - High	Complex
Half Bridge Converter [48]	3.73 mV/min – Medium	90% - High	Complex
Half Bridge Converter [49]	8.33 mV/min – Very High	87% - Medium	Moderate
Cell Selective Flyback [50]	2.51 mV/min – Low	99.9% - Very High	Simple
Proposed Cell Selective IĆC	9.63 mV/min – Very High	81.98% - Medium	Simple

The cost effectiveness and topology sizes that are listed in Table 3.2 are estimated using the analytical approach described in reference [93]. The cost of each component is determined by fixed values provided, and the total cost is derived by considering the amount of components used for only 8 cells. In addition, the size of the topologies is evaluated by taking into account the amount of components utilized and their published dimensions. Due to the use of a single transformer in the IĆC topology, both the cost and size of the topology are significantly lowered. Furthermore, the passive components of IĆC and the semiconductors of SWM prevent the higher costs and larger sizes when compared to other topologies. Consequently, the evaluation of the suggested configuration is more cost-effective and provides a reduced dimension.

Table 3.2 Comparison of cost effectiveness and size of the proposed study and the topologies in literature

Topology	Component Counts for Each 8 Cells							Cost ($)	Size
	M	D	RS	L	C	T	M		
Multiple Transformer [47]	16	0	0	0	0	8	0	56.00	Large
Half Bridge Converter [48]	18	0	0	0	18	0	1	42.40	Large
Half Bridge Converter [49]	4	16	0	16	20	2	0	49.20	Large
Cell Selective Flyback [50]	19	20	1	0	1	2	0	33.90	Medium
Proposed Cell Selective IĆC	18	16	0	2	4	1	0	31.40	Medium

Price per unit of components ($): MOSFET and MOSFET Driver (M) (1), Diode (D) (0.2), Resistor (RS) (0.1), Inductor (L) (1), Capacitor (C) (0.8), Single Transformer (T) (5), Multi Winding Transformer (MT) (10)

CHAPTER 4

CONCLUSION

This study investigates the performance and application of a proposed P2C BMS active balance architecture with a switch matrix and IĆC. The design is simulated via MATLAB Simulink, then verified through experimental implementation. The IĆC and switch matrix are used to enable the transfer of charge from the battery pack to selected cells, operating as expected. The study underlines that P2C active balance systems have the ability to manage higher balance currents, resulting in a faster balancing operation. The SoC curves of cells are estimated by utilizing a combination of the OCV approach, observed DoD curves, and internal resistance estimation methods. The battery balance operation is shown by testing two separate SoC configurations in an idle situation. The initial setup has a deviation of 10% SoC, whereas the second setup involves a 55% SoC deviation. The proposed method appropriately equalizes the low-charged battery cells with the current level of 3 A. The process of balancing takes 1170 seconds to equalize a 10% SoC imbalance and 3033 seconds to equalize a 55% SoC imbalance. The efficiency of the balance operation had been evaluated and found to be 81.98% at around 3A during experiments. The switch matrix is crucial in the process of selecting low-charged cells from 1 cell to 4 cells in a row in order to ensure efficient redistribution of charge. The experimental results confirm the simulation outputs, highlighting the robustness and speed of the proposed active balancing topology. The findings indicate that the suggested P2C BMS topology is an effective way to improve the performance and life cycle of battery systems by ensuring rapid charge balancing. Furthermore, the proposed study offers cost effectiveness, and a compact size compared to other P2C topologies. This research advances the progress of BMS technology, establishing a basis for future advancements focused on increasing battery performance and extending the operational life cycle of battery packs.

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