ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

DESIGN AND IMPLEMENTATION OF PHASE-SHIFTED FULL-BRIDGE CONVERTER WITH A CURRENT DOUBLER FOR HV TO LV BATTERY CHARGER IN ELECTRIC VEHICLES

M.Sc. THESIS

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Department of Electrical Engineering

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ISTANBUL TEKNİK ÜNİVERSİTESİ ★ LİSANSÜSTÜ EĞİTİM ENSTİTÜSÜ

ELEKTRİKLİ ARAÇLARDA YG BATARYADAN AG BATARYAYI ŞARJ EDEN AKIM KATLAYICILI FAZ KAYMALI TAM KÖPRÜ DÖNÜŞTÜRÜCÜNÜN TASARIMI VE GERÇEKLEMESİ

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ŞUBAT 2024

Tevhide DAYIOĞLU YURDAKONAR, a M.Sc. student of ITU Graduate School student ID 504201178, successfully defended the thesis entitled "DESIGN AND IMPLEMENTATION OF PHASE-SHIFTED FULL-BRIDGE CONVERTER WITH A CURRENT DOUBLER FOR HV TO LV BATTERY CHARGER IN ELECTRIC VEHICLES", which she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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To my spouse,

FOREWORD

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January 2024

Tevhide DAYIOĞLU YURDAKONAR
Electrical Engineer

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ABBREVIATION

AC : Alternating Current
ADC : Analog-to-Digital Converter
APM : Auxiliary Power Module
BEV : Battery Electric Vehicles
BSC : Bottom Side Cooled
CDR : Current-Doubler Rectifier
CICDR : Coupled Inductor Current-Doubler Rectifier
CMPSS : Analog Comparator
CPU : Central Processing Unit
CTR : Center-Tap Rectifier
DAC : Digital-to-Analog Converter
DC : Direct Current
EMI : Electromagnetic Interference
ESR : Equivalent Series Resistance
EU : European Union
EV : Electric Vehicle
FCEV : Fuel Cell Electric Vehicle
G2V : Grid-to-Vehicle
GaN : Gallium Nitride
HEMTs : High Electron Mobility Transistors
HEV : Hybrid Electric Vehicles
HV : High-Voltage
ICE : Internal Combustion Engine
IGBT : Insulated-Gate Bipolar Transistor
IMS : Insulated Metal Substrate
IPOP : Input-Parallel-Output-Parallel
IPOS : Input-Parallel-Output-Series
ISOP : Input-Series-Output-Parallel
ISOS : Input-Series-Output-Series
JTAG : Joint Test Action Group

LCO : Lithium Cobalt Oxide
LFP : Lithium Iron Phosphate
Li-Ion : Lithium-Ion
Li-metal : Lithium Metal Batteries
Li-poly : Lithium Polymer
LMO : Lithium Manganese Oxide
LNO : Lithium Nickel Dioxide
LTO : Lithium Titanate
LV : Low-Voltage
MHEV : Mild Hybrid Vehicles
MIMO : Multiple-Input-Multiple-Output
MLT : Mean Length Turn
MOSFET : Metal-Oxide-Semiconductor Field-Effect Transistor
Na-beta : Sodium-Beta Batteries
Na-ion : Sodium-Ion Batteries
NCA : Lithium Nickel Cobalt Aluminum Oxide
Ni-Cd : Nickel-Cadmium
NiMH : Nickel-Metal-Hydride Batteries
NMC : Lithium Nickel Manganese Cobalt Oxide
OBC : On-Board Charger
Pb-acid : Lead acid
PCB : Printed Circuit Board
PCMC : Peak Current Mode Control
PHEV : Plug-In Hybrid Vehicles
PI : Proportional Integral
PRC : Parallel Resonant Converter
PSFB : Phase-Shifted Full-Bridge
PT : Planar Transformer
PWM : Pulse-Width Modulation
RMS : Root Mean Square
SCC : Switch-Controlled-Capacitor
SiC : Silicon Carbide
SIMO : Single-Input- Multiple-Output
SR : Synchronous Rectification
SRC : Series Resonant Converter

SRM **:** Switched Reluctance Motor

SynRMs **:** Synchronous Reluctance Motor

TF **:** Transfer Function

TSC **:** Top Side Cooled

TVS **:** Transient Voltage Suppressor

V2G **:** Vehicle-to-Grid

V2L **:** Vehicle-to-Load

ZCS **:** Zero Current Switching

ZVS **:** Zero Voltage Switching

SYMBOLS

A : Area
A_L : Inductance factor of core
A_p : Area product
B : Flux density
C : Capacitance
D : Diode
D_{eff} : Effective duty cycle
E : Energy
f : Frequency
G : Transfer function
H : Magnetizing force
I : Current
J : Current density
K : Microcontroller's PWM-channel comparator gain
K_f : Waveform factor
K_i : Integral parameter of controller
K_p : Proportional parameter of controller
K_u : Utilization factor
L : Inductance
l : Length
N : Turns number
P : Power
Q : Charge
R : Resistance
R_i : Current sensor gain
R_v : Voltage sensor gain
S : Switch
T : Period
t : Time
TR : Transformer

V **:** Voltage

V_e **:** Effective core volume

W_a **:** Window area

Z **:** Impedance

ΔI **:** Current ripple

ΔV **:** Voltage ripple

Ɛ **:** Skin dept

μ **:** Effective permeability

ρ **:** Copper resistivity

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DESIGN AND IMPLEMENTATION OF PHASE-SHIFTED FULL-BRIDGE CONVERTER WITH A CURRENT DOUBLER FOR HV TO LV BATTERY CHARGER IN ELECTRIC VEHICLES

SUMMARY

Internal combustion vehicles have been widely used for many years. With the increase in population, the usage rate of internal combustion vehicles also increases. This situation causes significant increases in greenhouse gas emissions. Therefore, increasing emission leads to the growth of the global warming problem worldwide. Many protocols such as the Paris Agreement, have been signed between countries in order to solve this issue. Moreover, efforts are made to increase environmental awareness and reduce people's carbon footprint. Electric vehicles (EVs) have recently become widespread within this scope. It is aimed at making the use of electric vehicles more prevalent.

With the extensive use of EVs, different needs have begun to emerge in many different areas. The most prominent of these needs are related to battery systems, power electronic converters, and traction systems. There are two types of batteries in electric vehicles: high-voltage and low-voltage batteries. High voltage batteries have many different types when classified according to their chemical content. The high-voltage battery is used for the traction of the vehicle, and the power is transferred to the electric motor with the inverter, which is one of the power electronic converters in EVs. Another power electronics unit, which is the onboard charger, is required to charge this high-voltage battery. Even though electric vehicles have high voltage battery, low voltage battery is still needed. The low-voltage battery plays a role in feeding the in-vehicle loads. There is another DC-DC converter between this low-voltage battery and the high-voltage battery. A DC-DC converter is a converter that charges the low-voltage battery and supplies all accessories in the EV, such as air conditioner, headlights, sound systems, lighting, electronic control units, wiper, and window system. This converter is used in electric vehicles instead of the belt-driven generator in internal combustion vehicles.

Today, due to the increase in vehicle electrification, accessories, and features, the amount of power demanded from DC-DC converters is also increasing. In order to meet this increase, this DC-DC converter must be able to provide very high currents. High current also brings high transmission losses, so it is essential to design properly with appropriate topology selection. In addition, it is an important criterion that DC-DC converters must be efficient due to continuous operation when the vehicle is in use. This means that a DC-DC converter affects the range or vehicle. In addition to efficiency, the converter must also be suitable for placement in the vehicle in terms of volume, owing to the limited space in the vehicle. Therefore, the DC-DC converter is expected to have a high power density (kW/L). As mentioned, since the DC-DC converter converts power between high-voltage and low-voltage batteries, another important point is that these converters are isolated to ensure safe operation. These are the basic features expected and required from a DC-DC converter to be used for

electric vehicles. This thesis studies the design and implementation of a high power density and efficient isolated DC-DC converter for electric vehicles.

First of all, a short history of EVs from past to present is shared. Brief information about battery electric vehicles, plug-in hybrid electric vehicles, hybrid electric vehicles, and fuel-cell electric vehicles is given. Afterward, high-voltage and low-voltage batteries were mentioned and their properties are shared by classifying them according to their chemical construction. In addition to information about the types and general features of today's EVs, the future of electric vehicles is given.

Isolated and unidirectional converters are investigated and evaluated in terms of power rating, efficiency, cost, volume, power density, input and output voltage, advantages and disadvantages. As a result, a phase-shifted full-bridge converter (PSFB) with a current doubler rectifier (CDR) is selected as a suitable converter. The main reasons for this selection are that PSFB with CDR have a wide voltage gain range operation ability, low output current ripple, and ZVS operation capability with constant switching frequency. Moreover, reduced conduction loss, better thermal performance, simpler transformer structure, and lower ripple load current can be achieved thanks to CDR.

Operating principles of PSFB with CDR converter and related waveforms of each operating mode are given in detail. All analytical calculations about switches, transformer, critical timings, inductors, capacitors and ZVS condition are given. Information on selected components is shared according to calculations. Moreover, design calculations to manufacture the transformer which is a planar transformer and inductors which are output and shim inductor are given.

Another important step, which is the decision on a suitable control method. Voltage mode, average current mode and peak current mode control (PCMC) methods are explained inclusively. PCMC method is selected as a suitable control method. The operating principle and implementation of the selected microcontroller of PCMC are explained. Small-signal model and transfer function of PSFB with CDR converter are obtained. Controller parameters of the PCMC method are determined with the modeled transfer function in MATLAB/Simulink. Open loop and close loop behavior are compared.

Afterwards, the converter is simulated with the real model of selected components, which are provided by the manufacturer, in LTspice. All results and waveforms are obtained for the operation at nominal operating conditions with different load currents. In addition, the clamping diodes effect is evaluated and results are shared.

PSFB with a CDR converter is designed and implemented. General information about the design and parts of the implemented design are shared. Laboratory tests are completed under the nominal operating conditions with different load currents as the simulation. Detailed experimental results and waveforms are shared and compared with simulation results.

As a result of the studies carried out within the scope of this thesis, the efficiency is obtained according to the simulation result at the nominal operating point for 250 A load current as 96.54%. The efficiency obtained from laboratory tests for the same operating point is 93.43%. The reason for this difference in efficiency is conduction losses, which become dominant in the printed circuit board at high currents, and thermal effects, which do not affect the simulation. According to the results of laboratory tests, the highest efficiency is 95.19% at the nominal operating point when

the load current is 150 A. Efficiency decreases for load currents which are higher than 150A because of the more dominant conduction losses. It can be observed that the analytical calculations, simulation, and test results are compatible with each other. Another outcome of the thesis is that the average power density of the different manufacturers' designs is 1.2 KW/L, while the power density of the realized design is 1.87 kW/L.

Finally, improving efficiency and conduction losses at higher currents are shared as future work. Furthermore, in order to adapt to technological developments, the converter can be revised to operate bidirectionally and at input voltages up to 800 V.

ELEKTRİKLİ ARAÇLARDA YG BATARYADAN AG BATARYAYI ŞARJ EDEN AKIM KATLAYICILI FAZ KAYMALI TAM KÖPRÜ DÖNÜŞTÜRÜCÜNÜN TASARIMI VE GERÇEKLEMESİ

ÖZET

İçten yanmalı araçlar uzun yıllardan beri yaygın olarak kullanılmaktadır. Nüfusun artmasıyla birlikte içten yanmalı araçların kullanım oranı da artmaktadır. Bu durum sera gazı salınımlarında ve doğal olarak küresel ısınmada oldukça büyük artışlara sebep olmaktadır. Dolayısıyla artan emisyon dünya genelinde küresel ısınma sorunun büyümesine yol açmaktadır. Bu probleme çözüm üretebilmek adına ülkeler arası Paris sözleşmesi gibi birçok protokol imzalanmaktadır. Dahası çevresel farkındalığın artması ve insanların karbon ayak izinin küçülmesi için çaba gösterilmektedir. Bu kapsamda son zamanlarda elektrikli araç kullanımı oldukça yayınlaşmıştır ve daha da yaygınlaşması hedeflenmektedir.

Elektrikli araçların yaygınlaşması ile birçok farklı alanda farklı ihtiyaçlar oluşmaya başlamıştır. Bu ihtiyaçların içinde en öne çıkanları batarya sistemleri, güç elektroniği çeviricileri ve çekiş sistemleri ile ilgilidir. Elektrikli araçlarda iki tip batarya mevcuttur, bunlar yüksek gerilim ve alçak gerilim bataryadır. Yüksek gerilim bataryaları anot, katot ve kimyasal içeriklerine göre sınıflandırıldığında farklı yapılarda olduğu görülebilir. Yüksek gerilimli batarya aracın çekişi için kullanılır ve güç elektroniği çeviricilerinden biri olan evirici ile elektrik motoruna güç aktarımı sağlanır. Diğer bir güç elektroniği birimi olan onboard charger ise bu yüksek gerilimli bataryanın şebekeden şarj edilmesi için gereklidir. Elektrikli araçlarda yüksek gerilim batarya paketi ile beraber alçak gerilim bataryaya da ihtiyaç duyulmaktadır. Alçak gerilim bataryası ise araç içi yüklerin beslenmesinde rol alır. Bu alçak gerilim batarya ile yüksek gerilim batarya arasında bir DC-DC çevirici vardır. DC-DC çevirici alçak gerilim bataryasının şarj edilmesini ve araç içindeki klima, farlar, ses sistemleri, aydınlatma, elektronik kontrol üniteleri, silecek, cam sistemi gibi tüm aksesuarların beslenmesini sağlar. Elektrikli araçlarda, içten yanmalı araçlardaki akümülatörün yerine bu çevirici kullanılır.

Günümüzde araçlardaki elektrifikasyonun, aksesuarların ve özelliklerinin artması sebebi ile DC-DC çeviricilerden talep edilen güç miktarı da artmaktadır. Bu artışı karşılayabilmek için bu DC-DC çeviricinin oldukça yüksek akımları sağlayabiliyor olması gerekmektedir. Yüksek akım beraberinde yüksek iletim kayıplarını da getirmektedir, bu sebeple uygun topoloji seçimi ile doğru bir şekilde tasarım yapmak oldukça önemlidir. Buna ek olarak, DC-DC çeviricilerin elektrikli araçların kullanımı durumunda sürekli olarak çalışır durumda olması ve yüksek gerilimli bataryadan beslenmesi sebebiyle verimli olması önemli bir kriterdir. Bu durum DC-DC çeviricinin aracın menzilini etkilediği anlamına gelmektedir. Verimin yanı sıra araç içindeki alanının kısıtlı olması sebebiyle, çeviricinin hacimsel anlamda da araç içindeki yerleşime uygun olması gerekmektedir. Dolayısıyla DC-DC çeviricinin yüksek güç yoğunluğuna (kW/L) sahip olması beklenmektedir. Bahsedildiği gibi DC-DC çevirici, yüksek gerilimli ve alçak gerilimli batarya arasında güç dönüşümü yapması sebebiyle

güvenli çalışmayı sağlamak için bu çeviricilerin izoleli olması bir diğer önemli noktadır. Bu bahsedilen özellikler elektrikli araçlar için kullanılacak olan bir DC-DC çeviriciden beklenen ve olması gerek temel özelliklerdir. Bu tezde elektrikli araçlar için yüksek güç yoğunluklu ve verimli izole bir DC-DC çeviricinin tasarımı ve gerçeklenmesi üzerine çalışılmıştır.

Tez kapsamında ilk olarak, geçmişten günümüze elektrikli araçların kısa tarihçesinden bahsedilip bataryalı elektrikli araçlar, şarj edilebilir hibrit elektrikli araçlar, hibrit elektrikli araçlar ve yakıt hücreli elektrikli araçlar hakkında bilgiler verilmiştir. Sonrasında yüksek gerilim ve alçak gerilim bataryalar ele alınarak bunlar kimyasal yapılarına göre sınıflandırılarak temel özellikleri paylaşılmıştır. Günümüzdeki elektrikli araçların tipleri ve genel özelliklerinin yanı sıra elektrikli araçların geleceği hakkında da bilgiler sunulmuştur.

Uygulama gereksinimleri göz önünde bulundurularak izoleli ve tek yönlü çalışan çeviricilerin güç değeri, verim, maliyet, hacim, güç yoğunluğu, giriş ve çıkış gerilimi, avantajları ve dezavantajları incelenerek karşılaştırılmıştır. Bu kapsamda birincil tarafı faz kaydırmalı tam köprü çevirici, ikincil tarafı ise akım katlayıcı doğrultucudan (PSFB-CDR) oluşan çevirici yapısı seçilmiştir. Bu seçimin ana nedenleri, PSFB-CDR, geniş bir gerilim kazanç aralığında çalışma yeteneğine, düşük çıkış akımı dalgalanmasına ve sabit anahtarlama frekansı ile ZVS yapabilme kapasitesine sahip olmasıdır. Ayrıca CDR sayesinde iyileştirilmiş iletim kaybı, daha iyi termal performans, basit transformatör yapısı ve düşük dalgalılığa sahip yük akımı elde edilmiştir.

Seçilen topolojinin çalışma prensibi ve modları detaylı bir şekilde açıklanmış ve ilgili dalga şekilleri verilmiştir. Çeviriciye ait anahtarlara, transformatöre, operasyonu etkileyen kritik zamanlamalara, indüktörlere, kapasitörlere ve ZVS durumuna ait tüm analitik hesaplamalar gerçekleştirilmiştir. Ayrıca, transformatörün ve indüktörlerin üretimine yönelik yapılmış tasarım hesaplamaları paylaşılmıştır.

Bir diğer önemli adım ise uygun kontrol yönteminin seçilmesidir. Gerilim modu, ortalama akım modu ve tepe akım modu kontrolü (PCMC) yöntemleri kapsamlı bir şekilde açıklanıp uygun kontrol yöntemi olarak PCMC yöntemi seçilmiştir. PCMC'nin çalışma prensibi ve seçilen mikrodenetleyici ile uygulanması anlatılmıştır. PSFB-CDR'nin küçük sinyal modeli ve transfer fonksiyonu elde edilmiştir. Seçilen kontrol metoduna göre, çeviricinin transfer fonksiyonu MATLAB/Simulink yazılımı ile modellenerek kontrolcünün parametreleri belirlenip açık döngü ve kapalı döngü davranışı karşılaştırılmıştır.

Çevirici bileşenlerinin netleştirilmesi amacıyla üreticilerden alınmış gerçek komponent modelleri ile birlikte PSFB-CDR LTspice programında benzetişimi gerçekleştirilmiştir. Nominal operasyon koşullarında, farklı yük akımı değerleri için elde edilmiş sonuçlar ve dalga şekilleri incelenerek paylaşılmıştır. Ayrıca kenetleme diyotlarının etkisi değerlendirilmiş ve karşılaştırılmalı sonuçlar paylaşılmıştır.

Benzetişim modellerinin sonrasında PSFB-CDR çevirisi tüm ara birimleri ile tasarlanmış ve gerçeklenmiş tasarım hakkında detaylar paylaşılmıştır. Benzetişimle aynı şekilde, nominal operasyon koşullarında, farklı yük akımı değerlerinde donanımsal ve laboratuvar testleri gerçekleştirilerek tamamlanmıştır. Her bir çalışma koşulunda elde edilen sonuçlar ve dalga şekilleri detaylı bir şekilde verilip benzetişim sonuçları ile karşılaştırılmıştır.

Tez kapsamında yapılan çalışmaların sonuçlarına göre, 250 A yük akımı için nominal çalışma noktasındaki benzetişim sonucuna göre %96.54 verim elde edilmiştir. Aynı çalışma noktası için laboratuvar testlerinden elde edilen verim değeri ise %93.4'tür. Verimdeki bu farklılığın ana sebebi yüksek akımlarda baskı devrede baskın hale gelen iletim kayıplarının ve buna ek olarak termal etkilerin benzetişim modelinde etkisinin görülmemesidir. Laboratuvar testlerindeki sonuçlarına göre en yüksek verim yük akımı 150 A iken nominal çalışma noktasında %95.19 olarak elde edilmiştir. Yük akımı 150 A'in üzerine çıktığında iletim kayıplarının daha baskın olması nedeniyle verim düşmüştür. Yapılan analitik hesaplamalar ile benzetişim ve deneysel sonuçların birbirleri ile uyumlu olduğu görülmüştür. Tezin bir diğer çıktısı ise farklı üreticilerin tasarımlarına bakıldığında ortalama güç yoğunluğunun 1.2 kW/L iken çalışma kapsamında gerçeklenen çevirici tasarımının güç yoğunluğunun 1.87 kW/L olmasıdır.

Tez kapsamında son olarak, verimi ve daha yüksek akımlarda iletim kayıplarını iyileştirmek ilerideki yapılabilecek çalışmalar olarak paylaşılmıştır. Ayrıca teknolojik gelişmelere uyum sağlamak amacıyla dönüştürücü çift yönlü olarak ve 800 V'a kadar giriş gerilimlerinde çalışabilecek şekilde revize edilebileceği yine gelecekteki çalışmalar kapsamında değerlendirilmiştir.

1. INTRODUCTION

Global warming and the depletion of natural resources have become global issues in recent decades, resulting in the need to regulate petroleum-based fuel consumption and carbon dioxide emissions; accordingly, electrification of vehicles has been started with various eco-friendly vehicles such as hybrid electric vehicles (HEV), plugin HEVs (PHEV), mild HEVs (MHEV), and battery electric vehicles (BEV). HEV and PHEV require a rechargeable battery system as a power source for the electric traction system. Electric machines, energy storage devices, and power electronic converters associated with motor drives all play key roles in the continued development of these systems. Among them, HEVs and PHEVs typically require a high-voltage battery to be charged from a public line via the AC–DC converter to drive the vehicle's electric motor; in addition, most of the vehicle's electronic equipment requires a low-voltage battery to be charged [1-2].

In such vehicles, a power electronics-based DC-DC converter takes over the role of the belt-driven generator and supplies low voltage from high voltage battery [3]. This converter is named a low voltage DC-DC converter, auxiliary power module, or accessory power module in literature [4-6]. Auxiliary power modules (APM) are used in this thesis to indicate the converter.

Design optimization of auxiliary loads of the APM significantly impacts vehicle fuel economy and electric range due to continuous operation during vehicle use [7].

In addition to the unidirectional operation of APM, new generation APM is also required to supply power in the reverse direction from the LV to the HV battery for start-up functions and to increase the reliability of the vehicle in case the HV traction battery fails [8].

1.1 Purpose of Thesis

The main objective of this thesis is to design and implementation of PSFB with CDR with high efficiency and high power density for electric vehicles. Firstly, related design calculations are completed. Regarding calculations, magnetic components are

manufactured. Afterward, transfer functions are obtained from the small-signal model of the converter. A suitable control method, which is peak current mode control (PCMC), is implemented in this study. Before the hardware implementation, simulations are completed with real component models in LTspice to observe the result under different load conditions. Finally, PSFB with CDR converter is implemented with selected and manufactured components. Experimental tests are completed at different operating conditions, which are the same as simulations. Eventually, the results obtained from the study are discussed at the end.

1.2 Literature Review

Determination of design parameters, which are power, switching frequency, input and output voltage, is the main starting point for designing the converter. The target application has to be well understood to choose this initial parameter properly. Nominal high-voltage battery and low-voltage battery ratings do not vary dramatically for electric vehicles. Moreover, there are maximum and minimum operating values for both HV and LV batteries. According to with the light of this specification, in [3] input voltage which connects to the HV battery is in the range of 200 to 400V, the LV value is 14 V as the nominal value, the rated power is 2 kW, the maximum output current is 145 A and typical switching frequency is selected as 100 kHz. Another study, which is in [1], is designed to be suitable to 200-250 V input voltage and 12 V rated output voltage, 3 kW, and load current of 250 A. All these electrical specifications also depend on the load profile and used semiconductor. A high switching frequency, which is between 250 kHz and 500 kHz, is selected in [4]. Moreover, input HV and LV ratings are decided between 250 V and 430 V, 9 V and 16 V, respectively. The output current value for this converter is 270 A. In [9], the output current, input, and output voltage range are the same as in [4], yet the differences are switching frequency which is between 260 kHz and 400 kHz, and power rating, which is 3.8 kW.

As similar to the mentioned study, the design parameter in [6] is 220-450 V for input voltage and 6–16 V for output voltage, 2.5 kW. The switching frequency is between 90-200 kHz for this application. Up to that point, all power ratings are given for HV to LV power conversion. However, there is another study in [7] that operates as bidirectional. The power rating of the converter for LV to HV operation, which can be

named boost mode operation, is 1.2 kW, and the power rating of HV to LV operation, which is named buck mode operation, is 2.2 kW.

Another important criterion also is power density. Designing a compact converter for targeted power has great importance. The overall size of the converter is mentioned as 30×18×5 cm with a volume of 2.7 L in [10], the peak power achieved is 7 kW, then the power density is calculated as 2.6 kW/L. The designed converter in [4] has 3.12 kW/L power density value. The calculated power density is 3 kW/L, and the prototype weight is 1.5 kg in [9].

Efficiency is one of the key points for every converter. The HV to LV DC-DC converter has an effect on the range of electrical vehicles since low efficiency causes the use of more power from the HV battery, which is used for traction as well. It is not possible to design a highly efficient converter for all whole operating range; it is important to identify the mostly operated points over the lifetime of the converter. Furthermore, efficiency has a role in heat dissipation issues over the design. Efficiency depends on many things, such as selected topology, semiconductor technology, selected switching frequency. There are several different efficiency values calculated from the designed converter in the literature. In [3], which is the 2 kW rated converter, the highest efficiency, which is 93%, is measured at the lowest specified input voltage, which is 220 V and 40 A load current. Measured peak efficiency and full load efficiency are slightly different from each other in nearly all applications. In [4], The peak efficiency of the converter is measured as 96.7% at 55 A load current and 380V-14 V condition. The full load, which is 270 A efficiency, is above 96% when operating at nominal input and output and above 95.5% for all other cases. In [10], efficiency at laboratory tests is higher than 96%. This converter can also operate in a precharge mode, which means that the input DC-bus capacitor is charged from a low-voltage (LV) battery. The maximum efficiency of the boost mode operation is measured at higher than 94%. As mentioned, used semiconductors have an impact on efficiency. A comparison of the results of this issue can be seen in [6]; system efficiency is calculated from simulation as 97% with synchronous rectification control and 90% without synchronous rectification control. Nevertheless, prototype efficiency is calculated as 93.2% as a maximum value, which is lower than the simulation result. In [7], efficiency reaches above 90% while the converter delivers half power, which is 1.1 kW, and more than half power during buck mode operation. The

efficiency of it during boost mode operation has been measured as 89.5% when delivering 0.976 kW with 9.9 V input voltage and 305.3 V output voltage. In [9], efficiency is higher than 95% over the load ranges. Peak efficiency has been measured as 96.7% at 140 A load, and 95.8% has been measured during full load operation, which is 260 A, 380 V as input voltage, and 14 V as output voltage. In [11], when the output current is greater than 40 A, the converter's efficiency is measured as more than 90% for the whole operating input voltage range. Peak efficiency is 92.5% at 160 V input and 50 A output.

Switching technologies are improving over years so in terms of conduction losses, parasitic components and thermal conductivity. Selected switches for both the primer and seconder side have an impact on determining the switching frequency, which is the major parameter in the design. Efficiency is also affected directly by switch technologies. In [3], primary side switches are selected as IGBT module, which has 650 V, 50 A rating with rapid diode and EasyPACK 2B module package. The part number is F4-50R07W1H3 from Infineon, and 100 kHz is selected as the switching frequency. It is important to realize the achievement of high-frequency switching with IGBT switches. As a result, it seems that remarkable improvement in the turn-off behavior together with satisfying conduction characteristic is visible in its improved high-speed version. The same IGBT module is also used in another study, which is [11]. Seconder side switches are selected as PB180N08S4-02 Silicon (Si) MOSFET from Infineon, which has 80 V, 180 A, and low conduction resistance $R_{ds(on)}$ 2.2 mΩ rating. Another state-of-the-art switch technology is the Gallium Nitride High Electron Mobility Transistor (GaN HEMT). This technology provides to reach high switching frequency which is around 500 kHz. Operation with high switching frequency is also important for resonant converters, since they can operate at in [4] GS66508B from GaN Systems, which has 650 V and 30 A ratings and bottom-side cooling feature. However, the number of automotive qualified, which means qualified to use in automotive application transistor is quite a few. This means that there is still a way to improve this transistor technology. Moreover, there is another study in [9] that also uses GaN HEMTs switches at the primary side.

First of all, galvanic isolation is needed to protect the LV electronic system from the potentially hazardous high voltage as the base topology, so various configurations exist according to this criterion. There are also several parameters, which are operating

current and voltage values, target efficiency, cost, complexity, and power density, to select the suitable topology. In [3] and [11], an IGBT-based zero voltage switching (ZVS) phase-shifted full-bridge (PSFB) with synchronous rectification (SR) DC-DC converter has been implemented. However, the drawback of these application is insufficient energy to charge IGBT parasitic capacitance; ZVS cannot be achieved properly for lagging leg. There are also some designs with a combination of different topologies to eliminate inherent disadvantages of design. The study in [5] recommends an integrated EV charger, which consists with the LLC converter of On-Board Charger (OBC) and the phase-shifted full-bridge (PSFB) converter of APM. The integrated charger shares a switch leg, which is the lagging leg of the PSFB converter. Main purpose is extending the ZVS range of the lagging leg which has non-ZVS behavior during the low load operation, since PSFB has ZVS turn-on characteristic at wide voltage range operation due to lack of the ZVS energy. High power density, low cost, and improved efficiency are other advantages of the proposed integrated charger. There is a shared leg for the integrated EV charger to achieve light load ZVS condition for lagging leg switches. Switches at this shared leg operate to circulate the magnetizing current of the LLC converter's transformer. ZVS for lagging lag has been achieved with the summation of this magnetizing inductance energy and leakage energy. Efficiency is also affected by the secondary side current, which causes dominant power losses because of high current. Thus, several combinations such as interleaved connection has been investigated on the primary and secondary side to find the best configuration. In [1], many configurations of Single-Input-Multiple-Output (SIMO) and Multiple-Input-Multiple-Output (MIMO) topologies and their control strategies have been evaluated in terms of MOSFET switch efficiency drop and cost aspect. Multiple connections which are Input-Parallel-Output-Parallel (IPOP), Input-Parallel-Output-Series (IPOS), Input-Series-Output-Parallel (ISOP), and Input-Series-Output-Series (ISOS) and Single-Input-Multiple-Output (SIMO) have been investigated. Primary MOSFETs' conduction loss, turn-off loss, gate drive loss, and efficiency drops versus cost for Single-Input and Input-Series configurations have been evaluated and reported. Because of the high current at the secondary side, the current doubler makes it more attractive and suitable. Paralleling more switches helps to reduce conduction loss with the drawback of higher cost according to efficiency drop and cost evaluation for the secondary side configuration with MOSFET. As a result of this study, ISOP full-bridge current doubler topology is selected as

suitable to have better performance. Another implemented topology in the literature for the HVLV DC-DC converter is the LLC DC-DC converter. In [9], a three-phase interleaved LLC DC-DC converter has been implemented. Each LLC converter phase can provide 90 A out of 270 A load current. In this study, phase-shedding technology between three phases is used to improve efficiency over a wide range of output current especially at light load. However, there is a trade between the current sharing feature and the efficiency of the interleaved LLC converter. Since, minor tolerance on resonant components which are L_r or C_r will create large impedance difference among different phases which cause unbalanced current sharing, lower efficiency, irregular heating and current stress. The switch-controlled-capacitor (SCC) method, which has been implemented in this study, helps to solve this current sharing problem among phases. Current sharing error between phases is always smaller than 2.5%, which means load current sharing is quite balanced.

The output current at the low-voltage battery side is around a hundred amps. This situation has an impact on the design converter in terms of efficiency, current carrying capability, and thermal issues. In [1], the secondary side current is 250 A. Hence, selecting the most suitable secondary side topology is critical to maximize the conversion efficiency. Two main options have been evaluated in this study for the secondary side, which are the center-tapped rectifier and the current doubler rectifier. It is mentioned that the current doubler with only one secondary winding is more proper than the center-tapped rectifier in terms of transformer structure. Moreover, the current doubler transformer structure provides more parallel windings connection on the secondary to reduce the conduction losses for high current applications. Another solution is mentioned as paralleling more switches helps reduce conduction loss with the drawback of higher cost according to efficiency drop and cost evaluation for the secondary side configuration with MOSFET or Schottky diode. Another point is that rectification with MOSFET has a lower efficiency drop than Schottky diodes for high-current applications. According to this study, all these advantages of the current doubler make it more attractive and suitable. In [2], the secondary side is designed as a current-doubler rectifier (CDR) with a coupled inductor, which can help to reduce the ripple current and losses of the secondary side for high efficiency. Efficiency at different power ratings has been calculated for different rectifier configurations, which are bridge rectifier, center tapped rectifier, CDR, and CICDR. CICDR has much better

efficiency at all calculated power ratings. Another effectual criterion is waveform over switches during turn-on and turn-off, which is affected by selected rectification topology. In [12], three types of rectification stages, which are full wave rectifier, current doubler, and bridge rectifier, have been evaluated in terms of drain-source voltage (V_{ds}) overshoot during turn-off and efficiency. The simulation model has been created for three of them to investigate the V_{ds} overshoot. Moreover, converters have been tested with these rectification stages separately under different input voltage and load current. It was observed that V_{ds} overshoot values are increased with increasing the transformer leakage inductance L_{leak} or the secondary side MOSFETs' output capacitance C_{oss} and reduce the efficiency. Simulation results and experiments have shown that bridge rectifier topology as SR stage has the lowest conduction losses, switch breakdown voltage, V_{ds} overshoot and eliminates the complicated snubber circuit in spite of a higher number of switching components. In addition to the selected configuration, the control method for rectification also has a role in designing a better converter. This effect can be evaluated in [6] and applied control method named as triggering angle tracking SRC (TAT-SRC). This strategy has been applied to the secondary side of the converter to track the target switching instants. Conventional SRC is very easy to operate, but it is unable to control the switching time of the MOSFET precisely, which causes low system efficiency. TAT-SRC is realized as software to determine the exact turn-on and off moments to realize the SRC. This method helps to improve system reliability and make it immune to external noise. These turn-on and turn-off time delays differ with the switching frequency, output power, and battery voltage. The lookup table is generated with device-level simulation in LTSpice and implemented to software. However, an efficiency scan block is used with a lookup table to achieve the best triggering time for the highest efficiency. System efficiency has been calculated from simulation as 97% with SRC and 90% without SRC. Nevertheless, prototype efficiency has been calculated as 93.2% as a maximum value, which is lower than the simulation result. The reason for this difference is that most of the load current flows through the printed circuit board (PCB), which causes additional conduction loss.

The main operating condition of this DC-DC converter is a conversion from high voltage to low voltage side, which is called as buck operation mainly. In addition, there might be a requirement for operating in reverse mode, which is power conversion from

low voltage to high voltage and called as boost or precharge mode. This mode can be used to charge the HV DC-link capacitor to the determined voltage value before connection between this capacitor and the HV battery to prevent discharge current from the HV battery. Moreover, this feature can be used to support the HV battery during cold cranking operation. In [10], the converter topology is an interleaved buck+dc transformer and has a bidirectional operating feature. This means that the converter has a precharge mode, which provides charging to the DC-bus capacitor from the LV battery. Voltage is 14 V for the LV battery and it charges the 2.5 mF capacitor to 400 V within 400 ms with the peak charging current being 80 A in this design. The maximum efficiency of the boost mode operation is measured higher than 94%. Same converter efficiency for buck operation is higher than 96% at laboratory test. Another bidirectional operation is also investigated in [7], which is a phase-shifted full-bridge with a synchronous rectifier at the secondary side. The auxiliary power module (APM), which is a DC-DC converter, provides 1.2 kW during cold cranking as a support to the HV battery with the help of boost mode operation. During buck mode operation, the rated power of APM is 2.2 kW. The efficiency of APM has been measured in buck mode for various output loads. Efficiency reaches above 90% while the APM delivers half power and more than half power during buck mode operation. The output voltage of APM has been set to 13.4 V. Efficiency of APM during boost mode operation has been measured as 89.5% when delivering 0.976 kW with 9.9 V input voltage and 305.3 V output voltage.

1.3 Hypothesis

High efficiency and high power density are desired for high-current applications in electric vehicles. Furthermore, it is required to have a wide voltage gain conversion range because of the wide input and output voltage range operation. Design and implementation of PSFB with CDR converter is proposed to achieve high efficiency, high power density, and wide voltage gain conversion.

2. ELECTRIC VEHICLE TECHNOLOGIES

It is important to understand and have a basic knowledge of many aspects of electric vehicles. This chapter briefly mentions the history of electric vehicles (EVs). Technical overview EVs types, which are battery electric vehicles, plug-in hybrid vehicles, hybrid electric vehicles, and fuel cell electric vehicles are shared. Another important topic, the country's policies on promoting electric vehicles, is also evaluated. Significant components of EVs, which are both high voltage and low voltage batteries, are reported in terms of their existing technologies, pros and cons over each other. Afterward, general information on existing EVs in the market is given. In the end, the future of EVs technologies is evaluated.

2.1 History of Electric Vehicles

The story of EVs started in 1830 with the first experimental lightweight EV in the USA, UK, and Netherlands. The history of EVs can be investigated with three main stages as a summary. First of all, the popularity of EVs increased between about 1890 and 1920. Afterward this popularity has been decreased after 1920. Then, EVs gained their popularity again after 1970.

During the golden age of EVs, three types of cars existed which are steam-powered vehicles, gasoline internal combustion engine (ICE) vehicles, and EVs. EVs became the USA's best-selling road vehicles, capturing 28% of the market in 1900. According to registered nationwide information, 936 gasoline ICE, 1575 electric, and 1681 steam vehicles existed in the 1900s.

Steam-powered vehicles were faster and less expensive; however, they required a long time to fire up and frequently stopped for water. The ICE vehicles were dirtier, more challenging to start working, and more expensive; nonetheless, they could travel longer distances with admissible speed without stopping. EVs were clean and quiet but slow and expensive. The main merits of EVs are that they do not have the vibrations, smell, and rumble compared to other vehicles. The range issue was not a problem during that time since most vehicles were used for urban commuting. With

this increased popularity, the global stock of EVs reached a historical peak of 30,000 in 1912.

After the 1920s, demand for EVs decreased due to several major technical and economic factors. One of the factors is that longer-range vehicles are required with established roads between the cities. Moreover, technical improvements such as hand crank elimination and fuel demand per kilometer descent occurred in time. The price of ICE vehicles also decreased. 15 million Ford Model T were manufactured between 1908 and 1927 at affordable price. However, the price of EVs did not reduce. The same situation existed for the price of gasoline and electricity. Because of all these reasons, EVs disappeared from the market at the end of the 1920s up to the first oil crisis in California in the early 1970s.

EVs were getting on the stage again in the 1980s, since the increasing price of fossil fuel, air pollution, and concern about climate change. Nevertheless, attempts to increase EVs sales remained inconclusive because of the same reasons, which were the high prices of the batteries, inadequate range, insufficient infrastructure, and long charging times as in previous years.

Supportive policies of governments exist to increase the usage of EVs today. The total global stock of rechargeable electric cars was over 180.000, representing 0.02% of total passenger car stock at the end of 2012 [13].

Major milestones in the history of EVs are given in Figure 2.1.

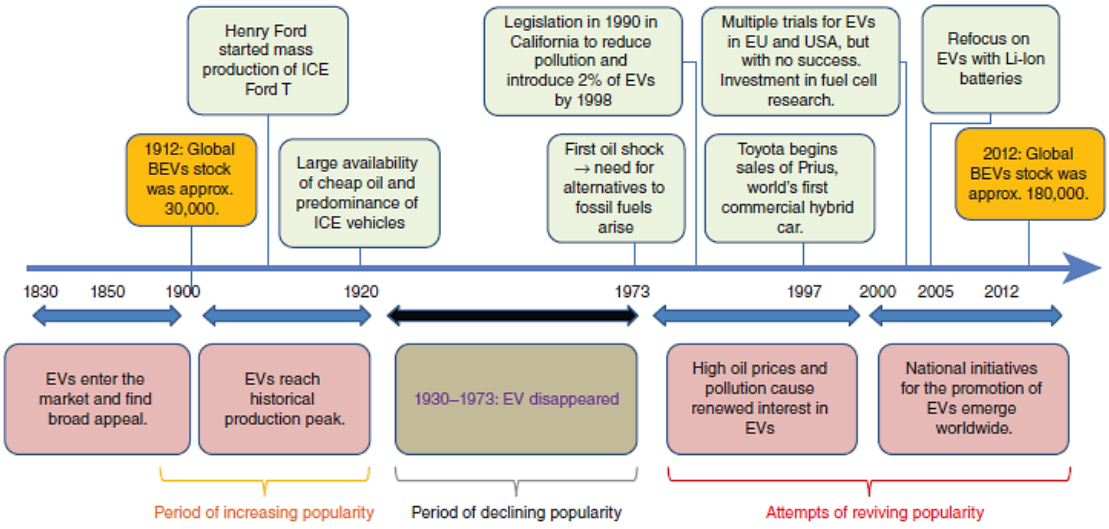

Figure 2.1 : General Major milestones in the history of EVs representation of the flyback converter [13].

2.2 Types of Electric Vehicles

Today, several types of EVs exist in the market. These are classified as battery electric vehicles (BEVs), plug-in hybrid vehicles (PHEV), hybrid electric vehicles (HEVs), and fuel cell electric vehicles (FCEVs).

Battery electric vehicles (BEVs) do not require an ICE or liquid fuel. They have only one storage system, which is a battery that provides all of the power for vehicles [13,14].

The general representation of EVs with their sub-components is given in Figure 2.2.

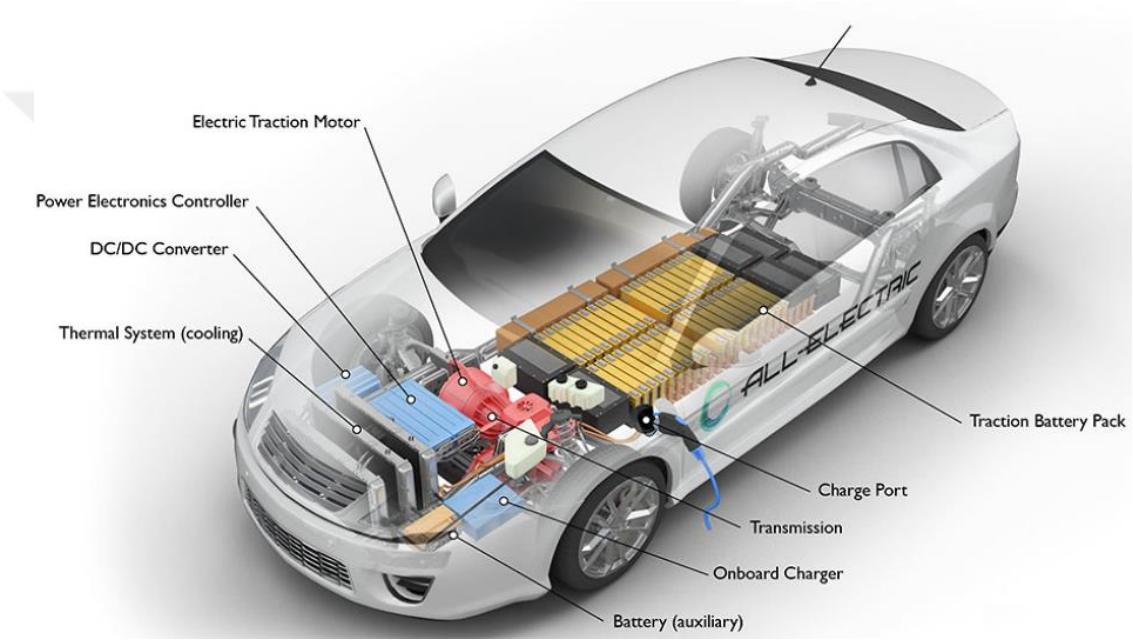

Figure 2.2 : General view of BEVs with sub-components [15].

PHEVs have almost the same powertrain as HEVs. However, PHEVs have rechargeable batteries through an external electricity supply, contrary to HEVs. In addition, the battery can be charged through regenerative braking. PHEVs have a larger battery than HEVs, which makes it possible to have a higher driving range and use electricity alone [13].

The ICE and the battery are powered HEVs. When the battery is dead, the petrol engine is used to both operate and charge the vehicle. ICE is the system's primary source, and the electric motor is used to support the vehicle for short distances or the ICE. The battery of HEVs is charged only with the energy recuperation of the braking process. HEVs are less efficient than PEVs. HEVs are usually categorized based on powertrain architecture, such as series hybrid electric, parallel hybrid electric, series-parallel

hybrid electric, and complex hybrid electric. The fuel and electric modules are connected in series with the electric motor in the series hybrid electric architecture. The ICE charges a battery that delivers power to the wheels [13,16,17]. In parallel hybrid electric architecture, multiple sources, which are the battery and fuel tank are connected in parallel to operate the vehicle. This means the energy sources operate separately or together to power the engine. A series-parallel electric topology allows switching between series and parallel modes. The sources can be utilized in different combinations to have enhanced efficiency. A complex hybrid electric architecture is similar to the series-parallel hybrid. Nevertheless, the critical difference is the bidirectional power flow of the electric motor in the complex hybrid, whereas the power flow is unidirectional in the series-parallel hybrid [16,17].

Architecture of different HEV types are given in Figure 2.3.

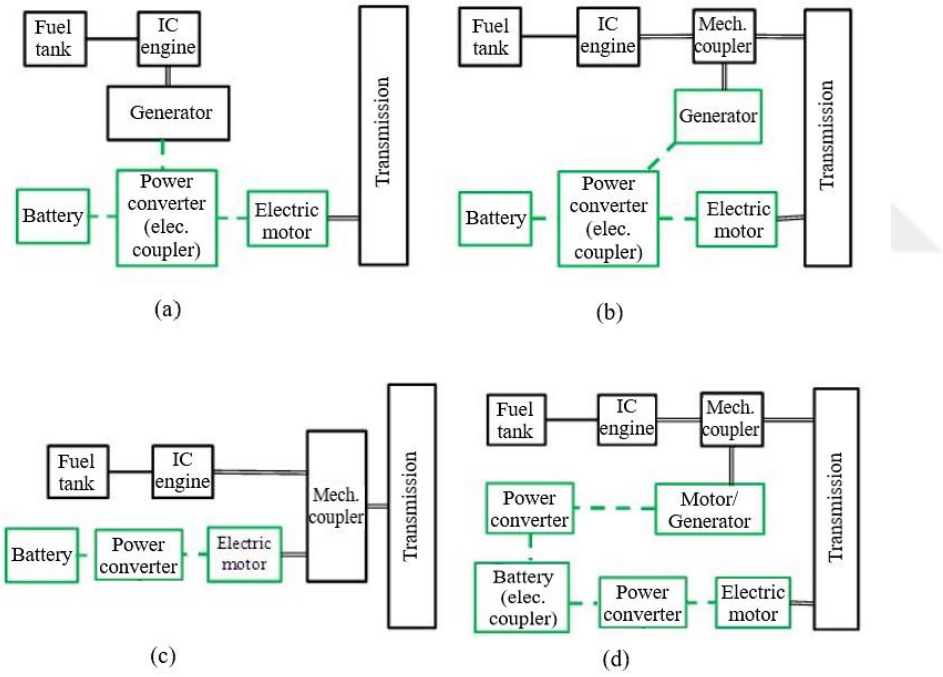

Figure 2.3 : Architecture of a) series hybrid electric configuration, b)series-parallel hybrid electric configuration, c) parallel hybrid electric configuration, and d) complex hybrid electric configuration [17].

FCEVs are another zero-emission vehicle. Hydrogen is the essential source of FCEV. Electricity which is the main energy, is generated by fuel source in fuel cell vehicles. The main features of FCEVs over BEVs is long driving range, the refiling time of the vehicle, which is just a few minutes [13]. Moreover, energy density and specific energy of the hydrogen fuel cell system are higher than battery systems. This means that

higher space and weight are required for battery systems when compared with the hydrogen fuel cell system which provides the same energy. Nevertheless, efficiency of FCEVs is lower than BEVs [18].

General architecture of BEVs, PHEVs, HEVs, and FCEVs is given in Figure 2.4.

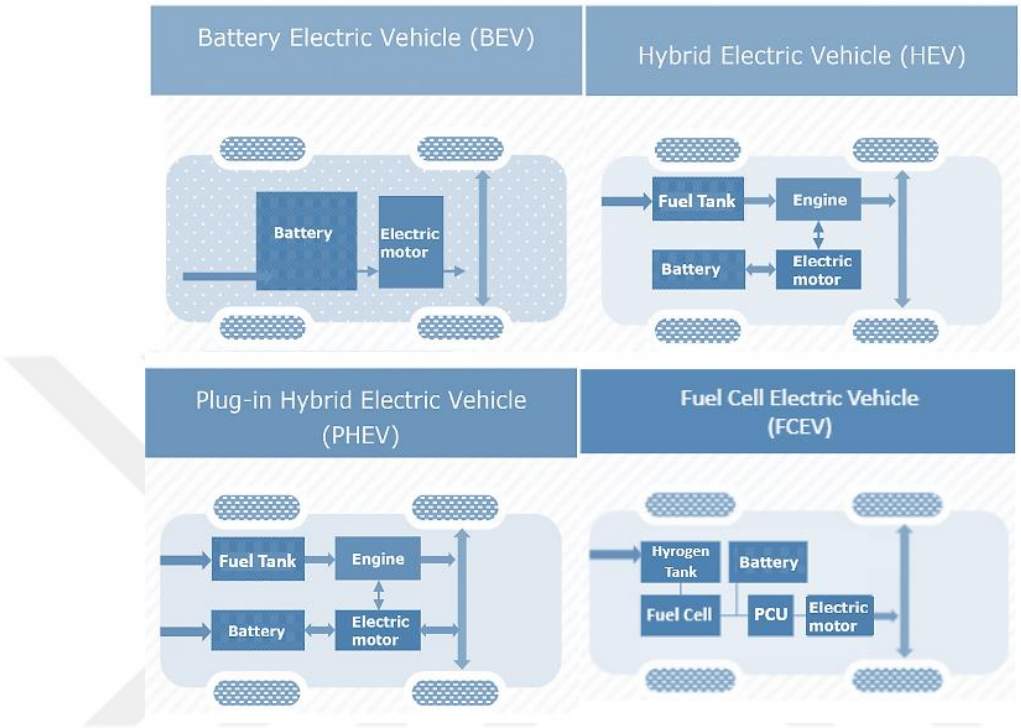

Figure 2.4 : Architecture of BEV, PHEV, HEV and FCEV [19].

When ICE vehicles and EVs are compared with each other, there are several prominent features. First of all, EVs are more comfortable with smoother acceleration, deceleration, and reduced center of gravity. Moreover, they intrinsically generate less noise pollution. Even though EVs have an enormous initial investment cost, relatively less maintenance cost can compensate for this issue thanks to significantly fewer moving components than ICE vehicles. Having fewer and simpler components also contributes to reliability. Moreover, powering the vehicle with electricity rather than petroleum is less expensive. The ability to regeneratively brake also contributes to generating energy.

EVs have disadvantages as well as advantages. The cost of EVs is high when compared with ICE vehicles. Other points are limited range per charge and long charging time. Furthermore, the electrical infrastructure of cities and the number of charging stations is insufficient [14,16].

A brief comparison between ICE vehicles and EVs is given in Table 2.1.

Table 2.1 : Comparison between ICE vehicles and EVs [20].

Characteristic	ICE Vehicles	EVs
Moving parts	More	Less
Vibrations	Medium	Low
Emission of gasses	More	Less
Reliability	Low	High
Efficiency	30% to 40%	More than 90%
Regenaration	Not possible	Possible
Torque at zero speed	Zero	Maximum torque

2.3 Policies of the Promotion of Electric Vehicles

Many countries apply different supporting policies to promote the widespread use of EVs. Even though EVs currently have higher costs than conventional vehicles and some less favorable characteristics.

Most European cities have several subsidies and exemptions or reductions for EVs, which are given below.

- Road taxes,
- Annual circulation tax,
- Company car tax,
- Registration tax,
- Fuel consumption tax,
- Congestion charges,
- Free parking spaces,
- Possibility for EVs drivers to use bus lines,
- Permission for EVs to enter city centers and zero emission zones [13].

Furthermore, many countries declare the electrification target in their countries. This means that only EVs will be sold, even banning ICE vehicle usage. Some countries' plans for the electrification of vehicles are given in Figure 2.5.

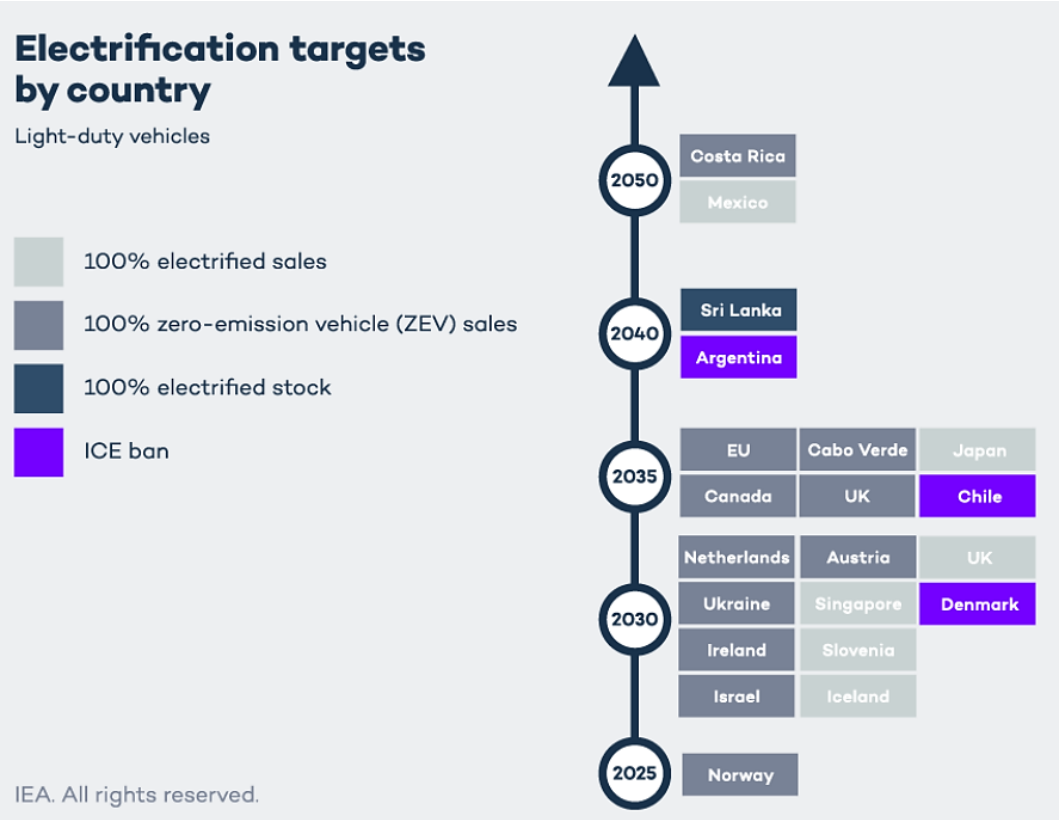

Figure 2.5 : Electrification target by countries over the years [21].

2.4 Battery Technologies

There are two different electrical systems in EVs. One of them is a high voltage system, which is commonly at 400 V. Moreover, some suppliers have begun to use an 800 V in their new model EVs. The Hyundai Ioniq 5 and Porsche Taycan 4S have 800 V HV battery [22]. The second one is a low voltage system, which is 12 V, such as the electrical systems used in ICE vehicles for decades. However, Tesla switches from 12 V to 48 V as a LV battery in Cybertruck. This transformation makes the wires thicker, lighter, and cheaper. Moreover, efficiency increases because of the current reduction by a factor of four, compared to 12 V systems [23].

Many different batteries which have different chemical contents and features exist. Finding the best suitable battery is quite crucial for EVs. Since there are several parameters, which are safety, performance, cost, range, thermal profile, reliability, and lifecycle have to be considered [24]. Especially the cost of EVs depends on the battery because the battery cost is a significant portion of the cost. The battery cost of the Tesla Model S is 13.6% of the total cost of EVs. Similarly, a battery of Ford Mustang

Mach E Standard is 16% of the total cost of EVs. In addition, the cost of Volkswagen ID.4 Standard battery is 23.4% of the EV's overall cost [25].

High-voltage and low-voltage batteries are evaluated in detail regarding various battery chemicals to better understand the battery technologies.

2.4.1 High voltage batteries

High-voltage batteries are the primary source of EVs that enable movement. This requires high-voltage batteries to handle high energy capacity and high power within limited weight and space at an affordable price. As a result, selecting the proper battery technologies is critical.

The most outstanding batteries are lithium polymer, lithium-ion, nickel-cadmium, and nickel-metal-hydride for EVs application. Detailed information on these battery technologies is given.

2.4.1.1 Lithium polymer batteries

Lithium polymer (Li-poly) batteries consist of lithium metal and oxide for negative and positive electrodes, respectively. A thin solid polymer instead of a liquid electrolyte is used as an electrolyte, which provides improved safety and flexibility during design.

Li-poly batteries have a higher specific energy. Thus, they are suitable for weight-critical applications, such as portable devices. However, higher manufacturing cost is the major drawback of Li-poly batteries. They are the prominent battery technologies for future generations of high-performance applications [16,24].

2.4.1.2 Lithium-ion batteries

Lithium-ion (Li-Ion) batteries are composed of carbon or silicon-carbon material for the negative electrode instead of metallic lithium and a metal oxide for the positive electrode. Li-Ion batteries have a higher voltage because their typical cell voltage is 3.0 to 4.5 V. Moreover, they have a long-life cycle, low self-discharge rate, more remarkable performance in high temperatures, and higher energy density. Because of these advantages, the Li-Ion batteries are used as the most promising batteries for EVs. The essential challenge of Li-Ion batteries was that they affected performance during operation under certain temperatures in the past.

Several types of Li-Ion batteries depend on the chemical combinations. These are lithium nickel manganese cobalt oxide (NMC), lithium nickel cobalt aluminum oxide (NCA), lithium iron phosphate (LFP), lithium manganese oxide (LMO), and lithium titanate (LTO), lithium nickel dioxide (LNO), lithium cobalt oxide (LCO). Cobalt-based lithium-ion batteries have higher specific energy and energy density; nevertheless, their costs and discharge rate are high. Manganese-based lithium-ion batteries are considerably the lowest in cost and specific energy.

The NMC Li-Ion batteries are preferable for EVs due to their superior lifespan and better overall performance. Another type, the NCA Li-Ion battery, is used in long range models of Tesla. However, Tesla switching to LFP Li-Ion batteries for their standar range models. LFP is a good option for cost-oriented manufacturers. LFP, which is a cobalt-free battery, is easier to build and cheaper. Moreover, LFP batteries are less likely to be exposed to thermal runaway that causes a fire. LTO Li-Ion batteries are also newer and popular option, which ensure a much higher surface area per gram. This means that LTO Li-Ion batteries enable higher power density [16,22,24].

Comparison of Li-Ion batteries with different chemical contents and the electric vehicle models in which they are used are given in the Table 2.2.

Table 2.2 : A comparison between Li-Ion batteries with different chemical options [16,22,26].

Battery Name	Nominal Voltage (V)	Lifespan (hrs)	Specific Energy (Wh/kg)	Vehicle Model
LFP	3.2~3.3	1000~2000	90~130	Tesla 3 (standard range) BYD Atto 3 MG ZS EV
LNO	3.6~3.7	>300	150~200	
LMO	3.7~5.0	300~700	100~150	Chevy Volt Escape PHEV
NMC	3.8~5.0	1000~2000	150~220	Nissan Lead Kia e-Soul Volkswagen e-Golf BMW i3 Peugeout e-208
LTO	2.3~2.5	3000~7000	70~85	Mitsubishi i-MiEV Honda Fit EV

Table 2.2 (continued) : A comparison between Li-Ion batteries with different chemical options [16,22,26].

Battery Name	Nominal Voltage (V)	Lifespan (hrs)	Specific Energy (Wh/kg)	Vehicle Model
NCA	3.6~3.65	500	200~260	Tesla X, S, 3 (long range), Y
LCO	3.7~3.9	500~1000	150~200	

2.4.1.3 Nickel-cadmium batteries

Nickel-cadmium (Ni-Cd) batteries have more energy density; however, this battery is old-fashioned because of its lower life span and durability. Moreover, cadmium is a heavy metal that harms the environment and human and animal health. As a result, European Union (EU) directives are applied to limit the use of Ni-Cd batteries. Because of these disadvantages, nickel-metal-hydride batteries (NiMH) are substituted for Ni-Cd batteries [14,27].

2.4.1.4 Nickel-metal-hydride batteries

The manufacturing technology and operation of NiMH batteries are similar to Ni-Cd batteries. NiMH batteries have a 40% higher specific energy than Ni-Cd batteries. Moreover, NiMH batteries have a reasonable operation and storage temperature range from 0 ℃ to 50 ℃ and longer life. However, NiMH batteries have lower energy storage capacity and a high self-discharge coefficient when compared to Li-Ion batteries. Other challenges are the heat generation at high temperatures, and required additional control systems to control losses.

NiMH battery is usually used in HEV, EV, and fuel cell EVs due to their longer life cycle than lead acid batteries, and safer operation. Toyota RAV4 EV, as a hybrid model, is one of the EVs with a Ni-MH battery [14,16,22,28].

2.4.2 Low voltage batteries

A low-voltage battery, which is 12 V, is required to start an ICE and the entire electric subsystem of ICE vehicles. EVs changed everything about the propulsion systems in the vehicle, yet everything on the inside as subsystems are the same. Similar to ICE vehicles, EVs also need a 12 V battery to power all electric subsystems. Eliminating the 12 V battery in an EVs might sound possible and ordinary; however, there are valid

reasons to keep this voltage level and LV battery in the vehicle. Developing and manufacturing new parts for HV batteries would be inconvenient and costly in the case of removing LV battery. Furthermore, redesigning a vehicle's auxiliary loads is complicated since automotive qualification can take years to complete. Most of the auxiliary loads connected to low-voltage systems are very close to the passengers. Powered by these loads with 400 V or even 800 V batteries is unsafe for the passengers. In addition, the idea of using high-voltage to power auxiliary requires high-voltage wiring in the car, making it hazardous to service. Another significant safety-related reason is that a HV battery has to be disconnected via a contactor during an accident. This contactor is driven by a 12 V battery [29-31].

Most of the typical LV auxiliary loads of EVs are represented in Figure 2.6.

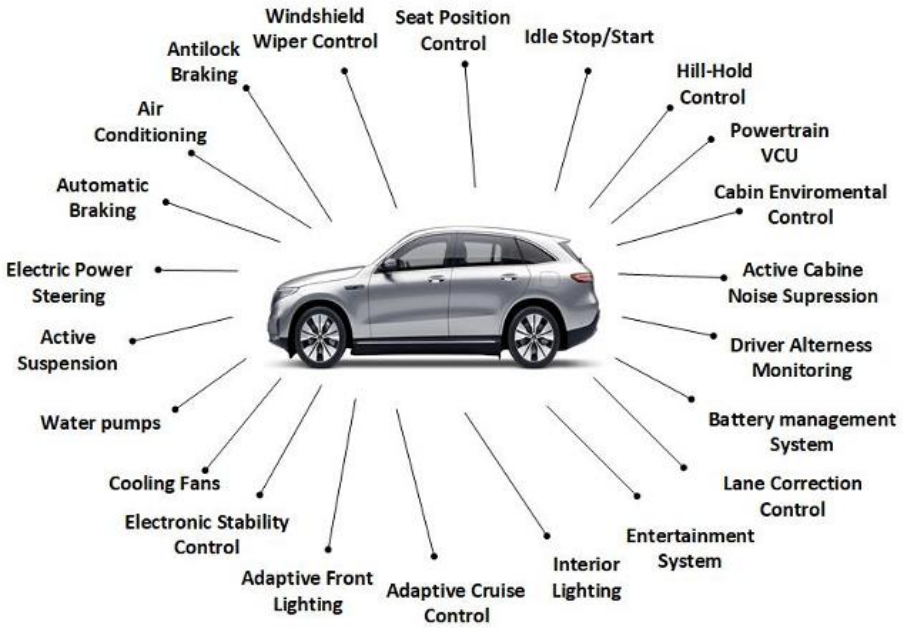

Figure 2.6 : EVs LV auxiliary loads [8].

Lead acid (Pb-acid) batteries are the oldest and most commonly used rechargeable batteries, invented in 1859. Pb-acid batteries are still the most common batteries worldwide.

Pb-acid batteries are inexpensive, easy to manufacture (minimal effort per watt-hour), reliable, tolerant of overcharging, and available in many brands. Moreover, they have high discharge current and good performance at low and high temperatures. Although there are several advantages of Pb-acid batteries, environmental concerns, corrosion

issues, acid fumes, and sulfation are the major negative sides to utilizing such batteries [14, 16].

2.5 Electric Vehicles in the Market

The usage of EVs worldwide is increasing. Many automotive manufacturers have at least one EVs model today. Even companies that only manufacture EV have been established. Moreover, some manufacturers declare that ICE vehicle development will stop in the future. Several countries also announced some sanctions on using ICE vehicles in the following years. Evaluation of EV car stock in China, Europe, the USA, and the remaining countries between 2010 and 2022 can be observed in Figure 2.7. According to observed data, China is the country that has the most usage of both BEVs and PHEVs [32].

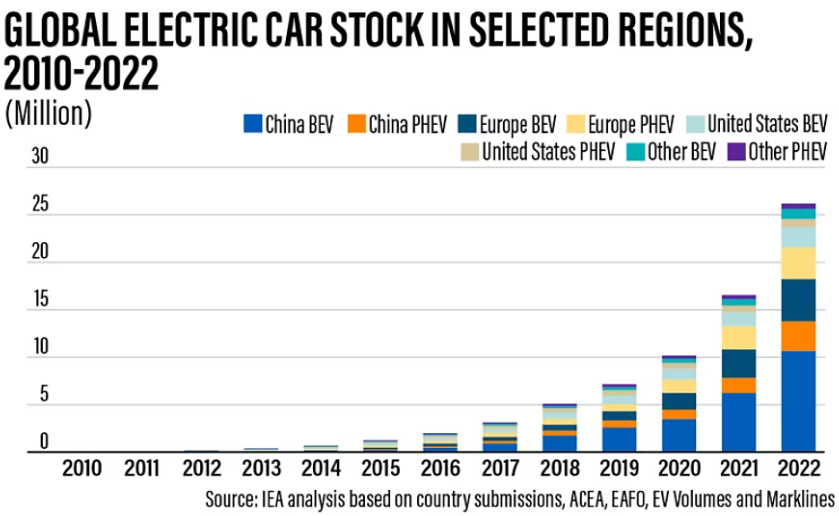

Figure 2.7 : Global electric vehicle stock in selected region between 2010 and 2022 [32].

Existing models of BEVs, PHEVs, and FCEVs are shared with battery charge capacity and range information in Table 2.3.

Table 2.3 : Existing models of BEVs, PHEVs, and FCEVs in the market [20,22].

EV model	Type	Battery Capacity (kWh)	Driving Range (km)
Chevrolet Volt	PHEV	18.4	85
Mitsubishi Outlander	PHEV	20	84
Volvo XC40	PHEV	10.7	43
Toyota Prius Prime	PHEV	8.8	40
Nissan Leaf Plus	BEV	64	480
Tesla Model S	BEV	100	620

Table 2.3 (continued) : Existing models of BEVs, PHEVs, and FCEVs in the market [20,22].

EV model	Type	Battery Capacity (kWh)	Driving Range (km)
Tesla Model X	BEV	100	500
Tesla Model 3	BEV	82	580
Kia Niro-SUV	BEV	64	460
Lexus UX 300e	BEV	54.3	320
Ford Mustang	BEV	70	400
Jaguar ev400	BEV	90	450
Renault Zoe	BEV	52	390
BMW i3	BEV	42.2	310
Chevrolet Bolt	BEV	65	402
Honda e	BEV	35.5	220
Porsche Taycan	BEV	79.2	410
Volkswagen e-Golf	BEV	35.8	230
Volkswagen ID.4	BEV	82	500
Mercedes-EQA	BEV	66.5	420
Audi e-tron	BEV	95	400
BMW iX3	BEV	80	460
Skoda Enyaq iv	BEV	62	412
Volvo XC40 Recharger	BEV	78	414
Polestar 2	BEV	78	470
Togg T10X-Long Range	BEV	88.5	523
Jaguar I-PACE	BEV	90	470
Toyota Mirai	FCEV	1.6	647
Hyundai Nexo	FCEV	40	570
Honda Clarity	FCEV	25.5	550

2.6 Future of Electric Vehicles

EVs have multiple advantages with several deficiencies that have to be improved in the future. According to the Department of Energy roadmap, EVs will reach a power density of 33 kW/L, 480.000 km or 15-year lifetime, and 100 kW electric drive capacity in 2025 [22]. The main bottleneck is the battery in terms of cost, charging time, and limited range. Ongoing development and search show that sodium-beta batteries (Na-beta), sodium-ion batteries (Na-ion), metal-air batteries, lithium metal batteries (Li-metal) (solid-state) type batteries have the potential to be future batteries for EVs. Another critical point is cost. Battery cost decreased over time; however, this is not sufficient. The average cost change per kWh of the main types of batteries that are used in EVs is given in Figure 2.8. Li-based batteries' cost is related to used

minerals, difficulty accessing, and manufacturing processes. Research and development continue because of all these reasons about high voltage batteries [24].

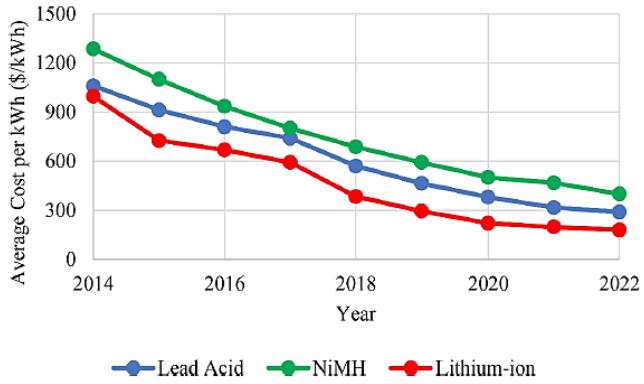

Figure 2.8 : Average cost change per kWh of different types of batteries between 2014 and 2022 [16].

Moreover, generating an alternative to LV batteries, which are mostly Pb-acid batteries, is another topic for the next generation of EVs. High current delivery is required for the ICE vehicle to start the engine. A Pb-acid battery is suitable to demand this. However, there is no need for this high current amount for EVs. Furthermore, Pb-acid batteries are heavy, and replacing them with Li-Ion batteries reduces the vehicle's weight with increasing efficiency. Li-Ion batteries are used as LV batteries for Tesla Model S and X models. In the future, Pb-acid batteries can be replaceable with different kinds of batteries [30].

EVs consist not only of batteries; there are several power conversion units such as inverter, OBC, and HV to LV DC-DC converter. The overall architecture of EVs is given in Figure 2.9. Unsurprisingly, efficiency, size, weight, and cost are the critical parameters for units. Replacing silicon switches with wide bandgap power electronic devices, which are mainly SiC and GaN, are enabled to increase in switching frequency without efficiency and thermal problems. Since the material properties of these switches have high thermal conductivity, wide bandgap, and high electron drift velocity. Moreover, usage of these switches leads to smaller dimensions and high-power density [20,22].

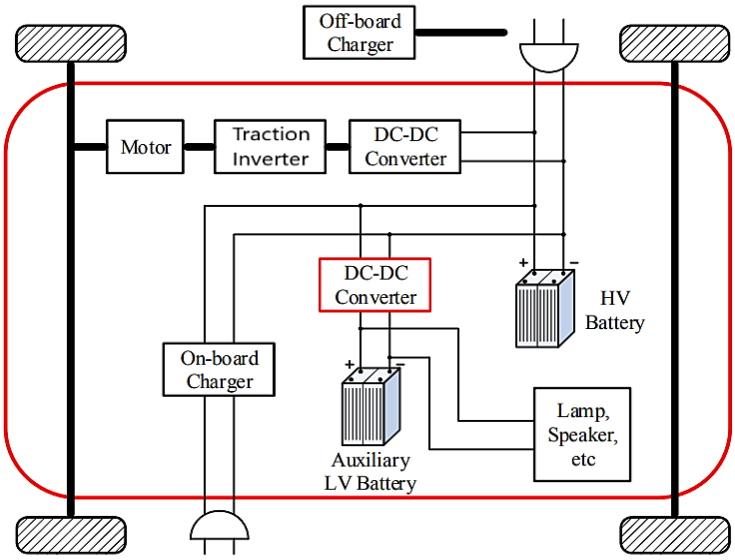

Figure 2.9 : The overall architecture of EVs [4].

The operating direction of the converters is another point of the future EV technology. Most OBCs in the market operate as unidirectional, which means that power conversion only from grid-to-vehicle (G2V) due to simplicity, reliability, low cost, and simple control strategy. Nevertheless, today, power conversion vehicle-to-grid (V2G) or vehicle-to-load (V2L) are expected. There are only a few manufacturers that have bidirectional OBCs in the market [20,22]. Ford F-150 lightning, Genesis GV60, Hyundai Ioniq 5, Hyundai Ioniq 6, Kia EV6, Kia Niro, Mitsubishi Outlander PHEV, Nissan Leaf and Volkwagen ID.4 have bidirectional OBC [33]. This feature will be the default characteristic of OBC in the future. Several studies are going on to generate policy on the grid side. Bidirectional operation also becomes widespread for HV to LV DC-DC converter. During the start-up of the EVs, DC-link capacitors of the inverter have to be charged up to a specified voltage level to prevent the huge inrush current from the HV battery. This is achieved with charging through external components, which are contactor with connected series resistor. To eliminate this component and have a more controllable charge current, bidirectional operation for the HV to LV DC-DC converter will be an ordinary feature.

Another open improvement point of EVs is the electric motors, which provide traction. EVs. Proper selection of electric motors makes the design and packaging of the powertrain components easier due to the size and lack of thermal limitations. The main issue for electric motors of EVs is rare earth magnets (NdFeB). For cost reduction, removing the rare earth magnets that are used also eliminates the reliance on this

essential component. Tesla uses alternating current (AC) induction motors in the Model S as an exemption. However, the necessity for higher specific power and power density makes induction motors no longer a good choice. The switched reluctance motor (SRM) and synchronous reluctance motor (SynRMs) are good candidates for alternative permanent magnet electric motors. Both machines feature a simple design with rotors made entirely of thin steel laminations. SRM controls are difficult and costly. SynRMs are robust, efficient, have minimum torque ripple, and are simple to control. However, they have a limitation on power factor and a limited constant power speed range. Studies have continued to find suitable and optimum electric motors for the future generation of EVs [34].

The combination of power electronics units, electric motor and transmission is a rising trend to reduce the space occupied by these components. This combined solution is named as e-axle. BorgWarner Inc., Continental AG, Dana Incorporated, Robert Bosch GmbH, and ZF Friedrichshafen are the outstanding companies for e-axle solutions in the market. This idea leads to a reduction in the number of parts, shortened cable runs and busbars, lower electromagnetic interference, and cost savings. Integrated structure may increase power density by at around 10% and diminish manufacturing and installation costs between 30% and 40%. However, thermal management can be challenging for this kind of combined solution [34,35]. The sub-system of the e-axle solution is given in Figure 2.10.

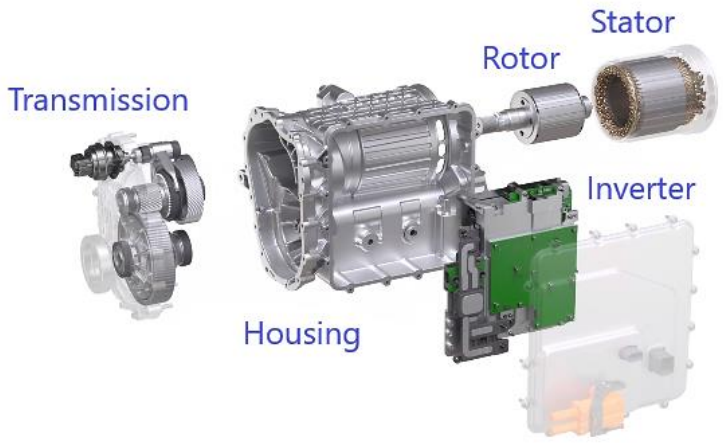

Figure 2.10 : Sub-systems of e-axle [36].

3. TOPOLOGY SELECTION AND COMPARISON FOR HV TO LV BATTERY CHARGER IN EVs

There are several types of DC-DC converters in power electronic circuits. These can be classified as isolated and non-isolated DC-DC converter. HV to LV DC-DC converter has to be isolated for EV applications in terms of safety and to satisfy the required voltage gain [9]. Another numerous criterion have to be considered for the selection of the suitable topology based on the application requirements. These are power level, efficiency, cost, volume, power density, input and output voltage, and durability. Moreover, the operating direction, which is unidirectional or bidirectional, also affects the converter topology selection.

Isolated topology is a must for HV to LV DC-DC converters for EV applications as mentioned. Therefore, unidirectional isolated DC-DC converters are evaluated and compared with each other in terms of suitability of the stated application basically.

One of the basic isolated converters is a flyback converter. Flyback is an outstanding converter in terms of cost, since it is a simple structure and has no additional inductor to the transformer. The voltage stress of the primary side switch is higher than the input voltage because of the reflected output voltage. This means that switch selection for high-voltage applications is critical. Flyback is suitable for low-power applications, thus it is not appropriate for the application evaluated in this thesis. However, transformer utilization is inadequate. Extra capacitors are required because of the high input and output current ripple. A controlled switch can be used instead of a diode for the rectification [8, 37]. The general representation of the flyback converter is shown in Figure 3.1.

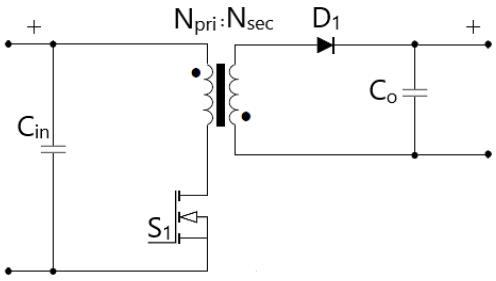

Figure 3.1 : General representation of the flyback converter.

Another basic isolated converter is a forward converte which is suitable for medium power applications. There is a transformer utilization issue similar to a flyback converter. In addition, there is a duty cycle limitation due to resetting the transformer. Voltage stress over the switch is twice the input voltage. Thus, a forward converter is not the best solution for high-voltage applications. A controlled switch can be used instead of a diode for the rectification [8, 37]. The general representation of the forward converter is shown in Figure 3.2.

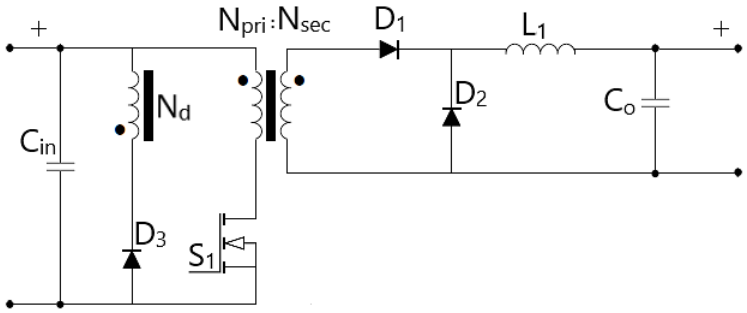

Figure 3.2 : General representation of the forward converter.

The push-pull converter is also one of the isolated converters. This converter uses the two quadrants of the BH curve on the contrary of the flyback and forward converter. This also provides that, higher power density can be achieved because of the full utilization of the transformer. Rectification can be configured as a center-tap rectifier or full-bridge rectifier and a controlled switch instead of a diode. This causes poor usage of the window area of the core. Furthermore, voltage stress over the primary side switch is two times the input voltage [8, 37]. The general representation of the push-pull converter is shown in Figure 3.3.

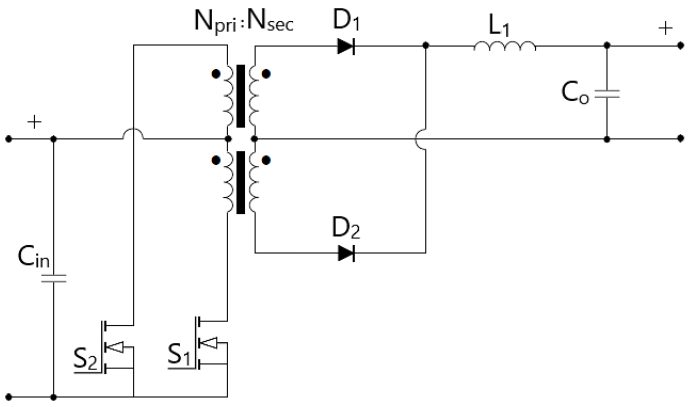

Figure 3.3 : General representation of the push-pull converter**.**

A half-bridge converter is another option. A transformer of the half-bridge converter also uses the two quadrants of the BH curve which is similar to the push-pull converter. Moreover, there is only one primary side winding which, provides better utilization of the core. Rectification can be configured as a center-tap rectifier or full-bridge rectifier and a controlled switch instead of a diode. Voltage stress over primary side switches does not exceed the input voltage. The capacitor connection behaves as a voltage divider. Thus, the primary side transformer voltage equals half of the input voltage. These capacitors can be bulky and costly depending on the input voltage. Current mode control is not feasible for a half-bridge converter because of these two capacitors at the input side [8, 37]. The general representation of the half-bridge converter is shown in Figure 3.4.

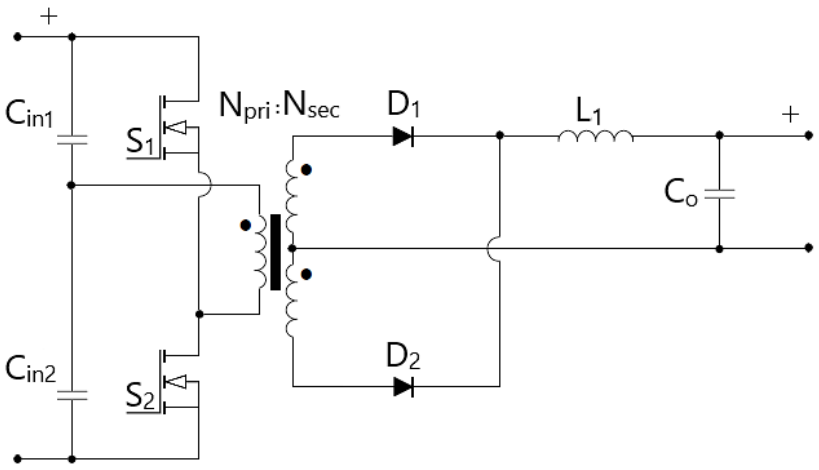

Figure 3.4 : General representation of the half-bridge converter.

A full-bridge converter is also a commonly selected isolated converter for high-power applications. A transformer of the full-bridge converter also uses the two quadrants of

the BH curve. Core utilization is good as a result of single primary side winding. Rectification can be configured as a center-tap rectifier or full-bridge rectifier and, a controlled switch instead of a diode. Voltage stress over primary side switches does not exceed the input voltage. Primary side transformer voltage equals the input voltage. The primary side current of the full-bridge transformer is half of the half-bridge transformer current owing to the doubling voltage at the primary side of the transformer. This means that full-bridge converter efficiency is higher than half-bridge converter because of reduced current. The disadvantage of a full-bridge converter is the usage of four primary switches which increases the driving complexity [1]. The general representation of the full-bridge converter is shown in Figure 3.5.

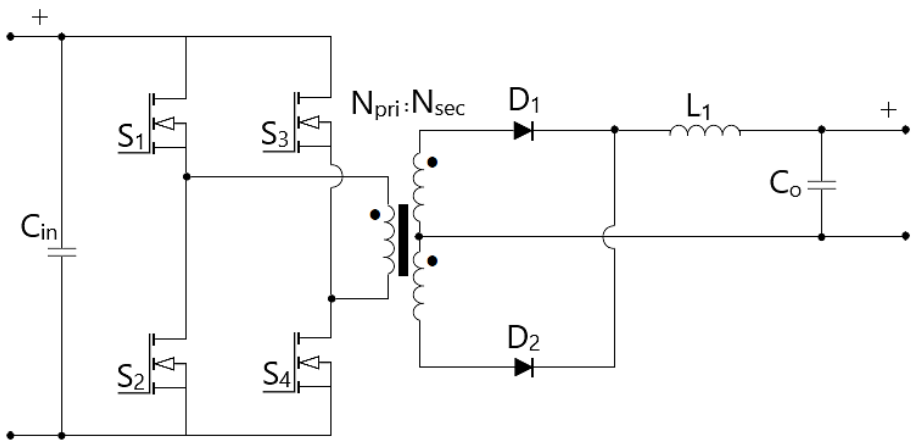

Figure 3.5 : General representation of the full-bridge converter.

A full-bridge converter can be operated as a phase-shifted full-bridge (PSFB) converter with a suitable switching method. This converter is commonly used for medium and high-power applications. PSFB converter can achieve zero-voltage switching (ZVS) during the turn-on transition. This feature provides common usage of the PSFB converter at high input voltage and power with high efficiency [1]. Moreover, ZVS can be accomplished with constant switching frequency. To extend the ZVS range for a light load operation, an external inductor is added in series with the primary side of the transformer. This inductor is named as shim inductor. Rectification can be configured as a center-tap rectifier (CTR), full-bridge rectifier, or current doubler rectifier (CDR) with a controlled switch instead of a diode. Nevertheless, conduction losses at the primary side are increased because of freewheeling operation interval. The general representation of the PSFB converter is shown in Figure 3.6.

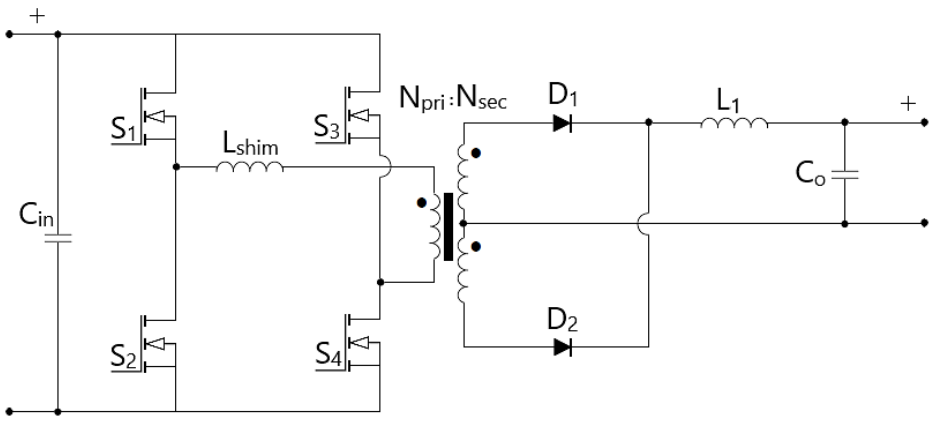

Figure 3.6 : General representation of the PSFB converter.

A series resonant converter (SRC) is configured with a series-connected capacitor to the primary side of the transformer. Voltage gain is the controller with a changing switching frequency. This requires a complex control design when compared with the other isolated converters. SRC is capable of achieving ZVS and zero current switching (ZCS). However, frequency has to sweep in a wide range to regulate the output voltage. Another issue is that a high switching frequency is needed for the regulation of light-loaded condition. Since the load has a high impedance compared to the resonant network impedance. Higher switching frequency causes a higher resonant tank impedance, which causes higher conduction losses [8, 37]. The series representation of the parallel resonant converter is shown in Figure 3.7.

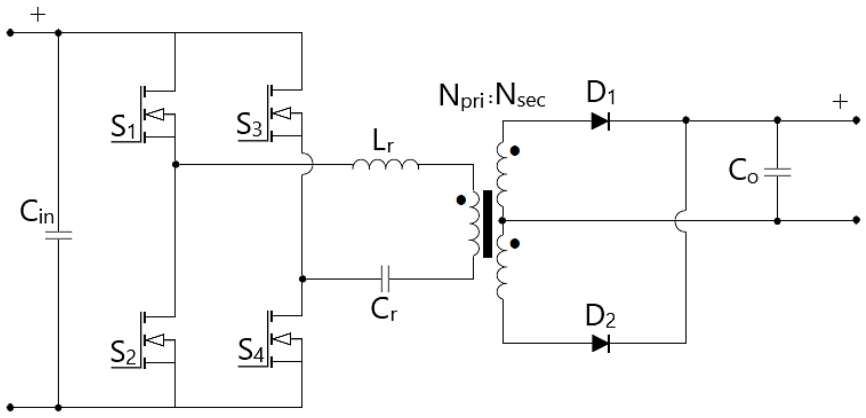

Figure 3.7 : General representation of the series resonant converter

A parallel resonant converter (PRC) is configured with a parallel connected capacitor primary side of the transformer. The voltage gain control method is the same as the series resonant converter. PRC is capable of achieving ZVS and ZCS. Moreover, the problem of the light load regulation does not occur for PRC. Nevertheless, high

circulation current in light-loaded conditions is the main drawback of PRC. This directly affects efficiency in a negative manner [8, 37]. The general representation of the parallel resonant converter is shown in Figure 3.8.

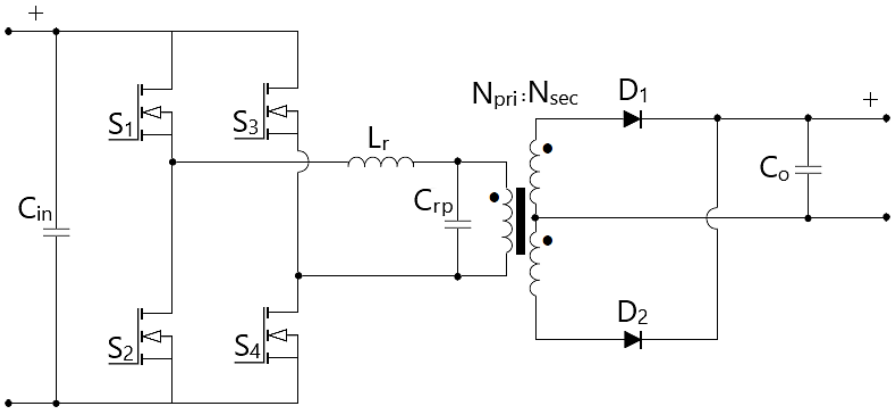

Figure 3.8 : General representation of the parallel resonant converter.

Another outstanding converter is the LLC resonant converter. The converter has to operate on the negative slope side of the gain curve to utilize the soft switching behavior of the LLC resonant converter. The relation between input and output voltage is adjusted with frequency change, as mentioned previously. The highest efficiency can be achieved during operation at resonant frequency. ZCS is also achieved during operation at the below resonant frequency. This feature provides to reach high efficiency. For the above resonance operation, only ZVS is accomplished. High power density is achievable for LLC resonant converter thanks to high-frequency operation capability [8, 37]. Furthermore, the LLC resonant converter provides the ZVS at very light load conditions or even no-load conditions [38]. LLC resonant converter can be configured as interleaved to have higher current capability and lower voltage ripple at the output. Nevertheless, additional components are required to have proper current sharing and parallel operation. This causes a more complicated design and control [8,37]. The general representation of the LLC resonant converter is shown in Figure 3.9.

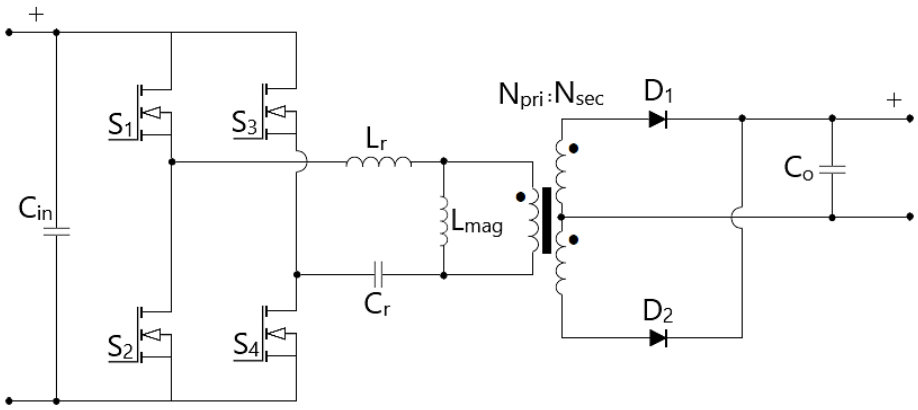

Figure 3.9 : General representation of the LLC resonant converter.

3.1 Selection of Suitable Converter for HV to LV Battery Charger in EVs

The input and output voltage range is quite wide for the HV to LV DC-DC converter for EVs application. Input voltage can be any value between 240 V and 475 V; output voltage can be any value between 10.9 V and 14 V. This means that the converter has to ensure the operation with a wide voltage gain range. Output current, which is 250 A as nominal value, is very high. Moreover, the converter operates in a unidirectional mode in this study. According to these basic operating requirements;

- Converter has a soft-switching feature to achieve highly efficient operation and low electromagnetic interference (EMI).
- Converter has to be configured as that voltage stress over primary side switches should not exceed input voltage because of high input voltage.
- Converter has to provide the operation with a wide voltage gain range.
- Converter has to be configured to carry high output current.
- Converter has to be feasible in terms of size and power density.

The PSFB converter, which is one of the most used topologies for HV to LV DC-DC converters for EV applications, is the best suitable converter to satisfy all these requirements and criteria. LLC converter is not feasible because of the wide voltage gain range requirement. Lower magnetizing inductance is required to have a wider gain range in LLC. This causes high magnetic currents and high conduction losses. Moreover, the LLC converter has to operate below the resonant frequency to achieve ZVS and ZCS, otherwise switching losses will be considerably high due to high-frequency operation. However, the converter has to operate at the above resonant frequency region to acquire a wide voltage gain range. Regarding to this, a wide

voltage gain range necessity is obtained with changing over frequency widely. This causes a loss of the advantage on the size of passive components, especially for magnetics. Since, the design of components has to be considered according to the lowest switching frequency. Output inductor contributes to having less output current ripple. Thus lower amount of output DC-link capacitors is required than an LLC converter [12].

To prevent the saturation of the transformer is a critical issue for the PSFB converter. Series capacitor to transformer can be used to eliminate the possible DC-bias current. However, this is not a good solution, since it is hard to find a capacitor that can satisfy the required rating. Furthermore, this kind of capacitor brings additional cost and lower efficiency. Peak current mode control (PCMC) is a better solution to extinguish this DC-bias current. More detailed information is given in chapter 4.3.

There are three options for the secondary side of the converter which are center-tap, full-bridge, and current double rectifier. They are given in Figure 3.10.

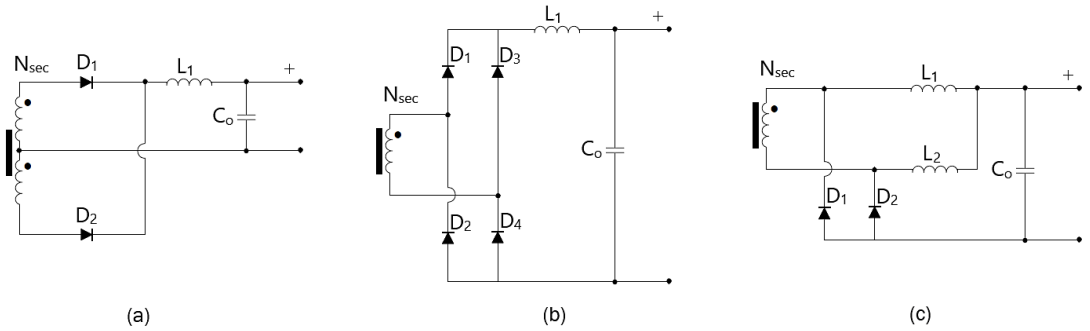

Figure 3.10 : a) Center-tap rectifier, b) full-bridge rectifier, c) current double rectifier as secondary side configuration.

The rectification side of the converter is selected as CDR as a consequence of the high output current. Output current flows over two switches in a full-bridge rectifier. Thus conduction loss will be two times when compared with CTR and CDR. Transformer utilization is poor for CTR. Only one of two windings is used at the same time. Output current splits into two when CDR is used as the secondary side. This is the major benefit of CDR, since conduction loss is correlated with the square of current. CDR requires two output inductors which help to decrease the current ripple in half when compared with other rectifier options [1]. Less output capacitors can be used thanks to this current ripple reduction behavior. Having two inductors instead of one bulk inductor has an advantage on thermal performance. The disadvantage of CDR is that the voltage stress of secondary side switches is higher than the output voltage.

CDR configuration can be implemented as a diode or synchronous rectifier. A diode rectifier is not a suitable option when the output voltage is low, since diode voltage drop becomes dominant. Moreover, the conduction resistance of the synchronous rectifier is lower than the diode rectifier. This provides that a synchronous rectifier can achieve higher efficiency during high current operation. However, the synchronous rectifier requires additional gate drive circuits.

As a result, PSFB with CDR converter provides high-efficiency thanks to ZVS operation and reduction by half of the high output current operation. High power density can be achievable with high switching frequency. In addition, the converter is capable of regulating a wide input and output voltage. With the help of the full-bridge configuration at the primary side, voltage stress over primary side switches does not exceed input voltage.

3.2 Analysis of the PSFB with CDR Converter

The PSFB with CDR converter has several different operating modes. It is important to evaluate deeply in terms of general information and operating principles to the design converter properly. In this chapter, general information about PSFB with CDR converter topology, phase-shifted pulse-width modulation (PWM) switching methodology and operating modes are given in detail.

PSFB with CDR converter is highly suitable for APM applications because of ZVS operation due to the simplicity of both hardware and software. Moreover, CDR enables it to operate with high current. PSFB with CDR combination circuit schematic is shown in Figure 3.11.

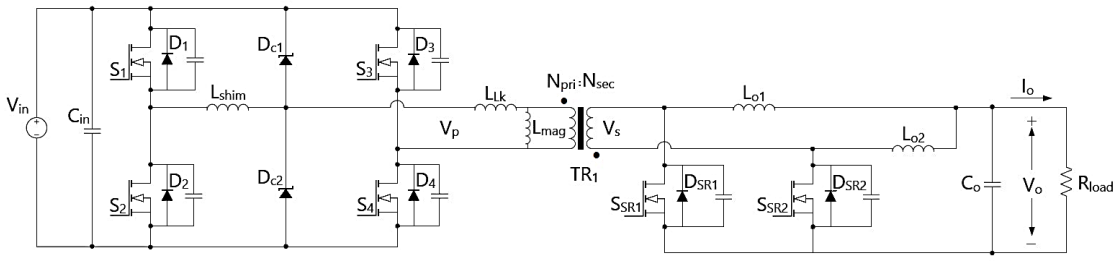

Figure 3.11 : Schematic of PSFB-CDR converter.

Primary side switches which are S_1, S_2, S_3, and S_4 which are identified as MOSFET in Figure 3.11, conduct almost 50% fixed-duty cycle. However, an effective duty cycle is generated by the overlapped of S_1 and S_4 and S_2 and S_3. D_1, D_2, D_3, D_4, D_{SR1}, and

D_{SR2} are the body diode of related switches. Deadtime has to be applied between S_1 and S_2, and S_3 and S_4 to prevent short circuit. ZVS could be achieved during this deadtime with the help of resonance between output capacitances of S_1, S_2, S_3, S_4 and stored energy in shim inductor L_{shim} which helps to achieve ZVS operation for light load condition and transformer leakage inductance L_{lk}. Shim inductor causes an increase in the number of components; however, increases the overall efficiency of the converter. The same situation could be obtained with increasing L_{lk}, yet that option causes an increase of voltage overshoot on the secondary side switches and decreases efficiency. L_{shim} also contributes to voltage overshoot on the secondary side switches. Nevertheless, D_{c1} and D_{c2}, which are the clamping diodes, could overcome this problem by clamping this overshoot. Detailed analysis of this issue was evaluated in [39, 40].

L_{mag} is the magnetizing inductance of the transformer. S_{SR1} and S_{SR2}, which are identified as MOSFET, are the switches in the CDR at the secondary side in Figure 3.11. These two switches are switched in relation of the primary side switches state. L_{o1} and L_{o2} are the output inductors. C_o and C_{in} are output and input DC-link capacitor respectively.

3.2.1 Phase-shifted PWM switching methodology

The switching method is quite critical in a PSFB with CDR converter; thus, it has to be understood exhaustively. PWM waveforms V_{gs1}, V_{gs2}, V_{gs3}, V_{gs4}, V_{gSR1}, V_{gSR2} are belong to S_1, S_2, S_3, S_4, S_{R1} and S_{R2} respectively. Duty cycle time is 50% for S_1, S_2, S_3, S_4 ideally, yet this time is less than 50% because of deadtime. S_3 and S_4 are leading leg switches; S_1 and S_2 are lagging leg switches. V_{gSR1} and V_{gSR2} are generated compatibly with the turn-on and turn-off time of primary side switches.

Power transfer happens when V_{gs1} and V_{gs4}; V_{gs2} and V_{gs3} overlap each other. These times which are t_1-t_2 and t_6-t_7, are named as effective duty cycle in Figure 3.12.

There is a time interval where there is not any PWM between switches at the same leg. These time intervals which are t_2-t_3, t_4-t_5, t_7-t_8 and t_9-t_{10} are named as deadtime in Figure 3.12. This interval is needed to prevent a shoot-through situation during switching transaction at the same leg. Moreover, this time is necessary to achieve the ZVS condition.

Another critical time interval is also named as duty cycle loss time which are t_o-t_1 and t_5-t_6 in Figure 3.12. Primary current I_p changes its direction during this time interval. Primary voltage V_p is equal to input voltage V_{in} theoretically. It can can be practically observed that there is an oscillated voltage on the transformer primary side. The reason for this oscillating waveform is the resonation between primary side inductance and the parasitic capacitor of primary side switches. The corresponding waveforms are given in the simulation and experimental results sections. However secondary voltage V_s is equal to zero. Thus, there is no power transfer at this interval. Efficiency is getting lower with higher duty cycle loss time. Moreover, this time interval limits the maximum achievable effective duty cycle time.

3.2.2 Operating principle of the PSFB with CDR converter

There are several operating modes which are changing according to the applied PWM situation. In this section, what is change in the converter and how it behaves are explained. Several waveforms are given in Figure 3.12. These are PWM waveforms V_{gs1}, V_{gs2}, V_{gs3}, V_{gs4}, V_{gSR1}, V_{gSR2}, primary and secondary voltage V_p and V_s respectively, primary current I_p, clamping diodes current I_{Dc1} and I_{Dc2}, output inductors voltage V_{Lo1} and V_{Lo2}, output inductors current I_{Lo1} and I_{Lo2}, leading leg switch which is I_{S3} current, lagging leg switch which is I_{S1} current, secondary side switch current I_{SR1}.

There are four main modes of operation of the PSFB with a CDR converter: duty cycle loss mode, power delivery mode, ZVS mode, and freewheeling mode. All these modes are explained in detail and schematics which show that active circuit parts are shared for each time interval.

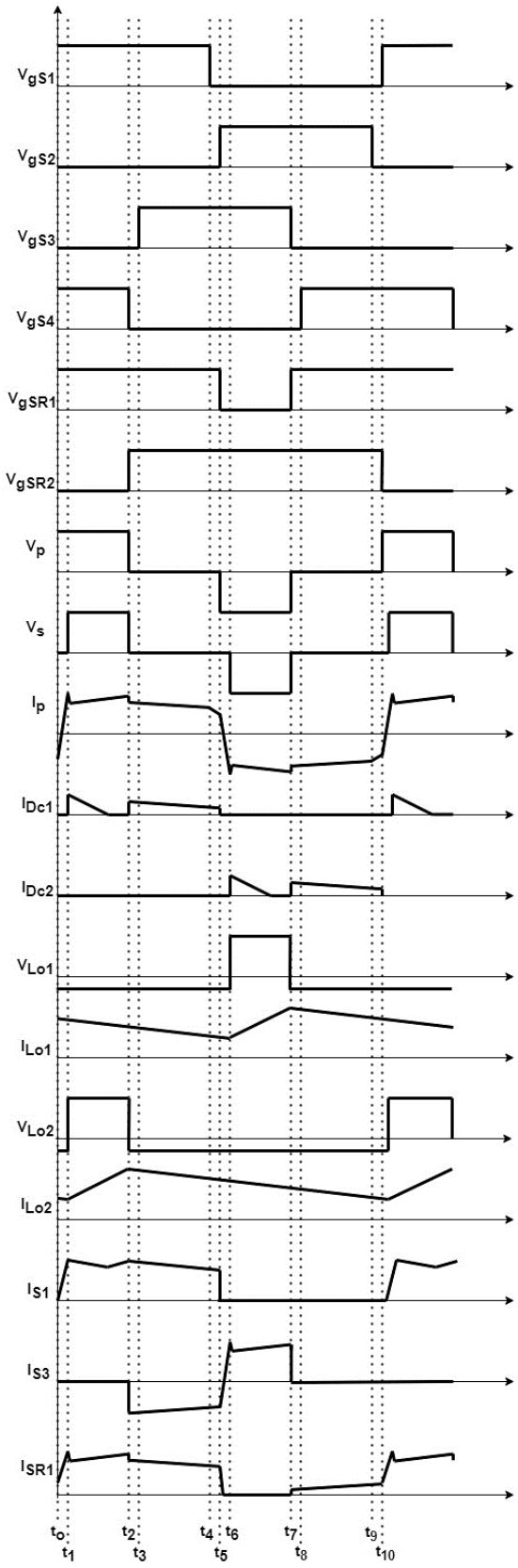

Figure 3.12 : Waveforms of PSFB-CDR converter during specific time intervals.

Mode 1: Duty Cycle Loss Mode (t_0-t_1)

This mode is named duty cycle loss mode since no power is delivered to the output in this mode. Switch S_1 is turned on with ZVS (as a following state of Mode 10, which is mentioned below) at t_0. Both secondary side switches, S_{SR1} and S_{SR2}, conduct current, although S_{SR2} is gated off. Not only output inductor L_{o1} but also other output inductor L_{o2} are discharging. The voltage of the transformer primary side V_p is equal to the supply voltage V_{in} theoretically. However, the voltage of the transformer secondary side V_s remains zero until the primary side current of transformer I_p reverses its direction and reaches the reflected output inductor current at t_1. I_p rises with a slope which depends on the V_{in} and both shim inductor L_{shim} and leakage inductor of transformer L_{lk}. The operation of the PSFB-CDR converter between t_0-t_1 is given in Figure 3.13.

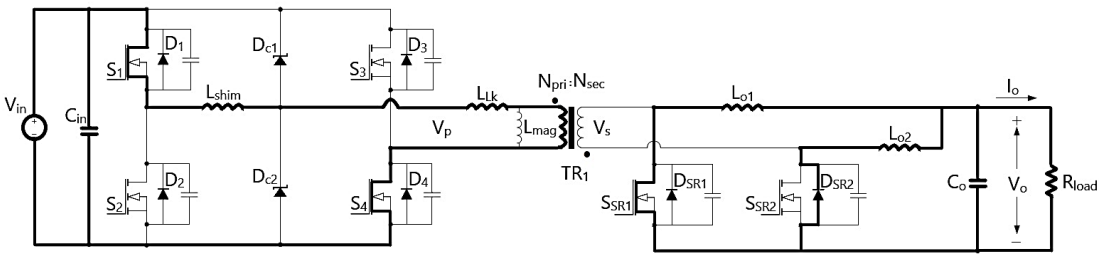

Figure 3.13 : Operation of PSFB-CDR converter between t_0-t_1.

Mode 2: Power Delivery Mode (t_1-t_2)

Power is delivered at this time interval and effective duty cycle ph_{eff} time interval starts at t_1 and ends at t_2. V_p is equal to supply voltage V_{in}. V_s is equal to the multiplication of V_{in} with transformer turns ratio (N_{pri}: N_{sec}) at t_1. Only S_{SR1} is on and carries both inductors current. L_{o2} is charging; however, L_{o1} is discharging. I_p is equal to the reflected output inductor current with respect to the transformer turns ratio.

S_{SR2} is turned off, this means that the switch output charge Q_{oss} and body diode reverse recovery charge Q_{rr} are charged. This energy is provided by the primary side of the converter. Additional current flows over L_{shim} and L_{lk} and stored energy is increased. D_{c1} starts conduction when the current through the L_{shim} rises above the I_p due to the charge of the rectifier's Q_{oss} and Q_{rr} at the start of the power transfer [41]. D_{c1} stops conduction at the point that the current of L_{shim} is equal to I_p. The operation of the PSFB-CDR converter between t_1-t_2 is given in Figure 3.14 and Figure 3.15.

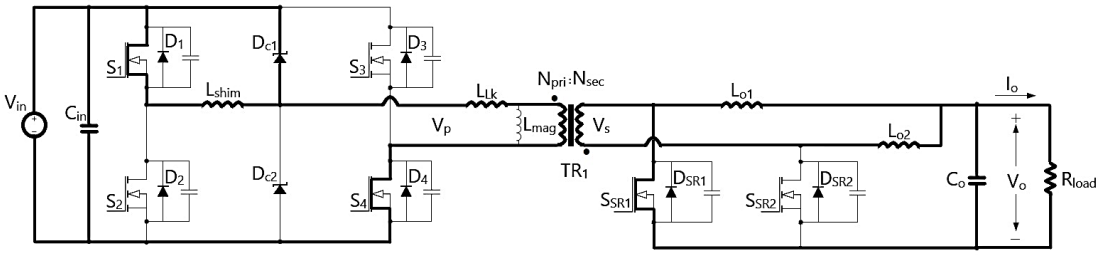

Figure 3.14 : Operation of PSFB-CDR converter between t_1-t_2-1.

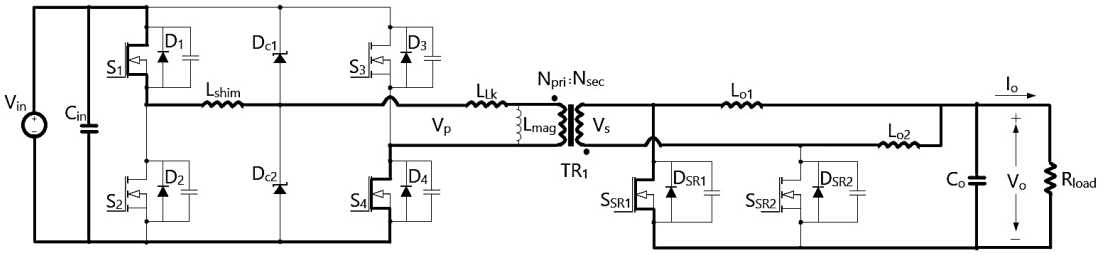

Figure 3.15 : Operation of PSFB-CDR converter between t_1-t_2-2.

Mode 3: Switch S_3 ZVS Mode (t_2-t_3)

At t_2, switch S_4 is turned off, the capacitance of S_4 is charged, and the capacitance of S_3 is discharged. When switch S_3 is discharged to zero, its body diode conducts to achieve ZVS condition. V_p and V_s become zero. Both S_{SR1} and S_{SR2} are conducting. L_{o1} and L_{o2} are discharging.

During this operating mode, the voltage at the primary side of the transformer suddenly decreases from V_{in} to zero. This situation leads to a decrease in the current with a steep slope. However, L_{shim} does not face this kind of voltage change over itself. Thus the current of L_{shim} does not change as transformer primary side current. This difference is that current flows through the diode, which is D_{c1} [42]. The operation of the PSFB-CDR converter between t_2-t_3 is given in Figure 3.15 and Figure 3.16.

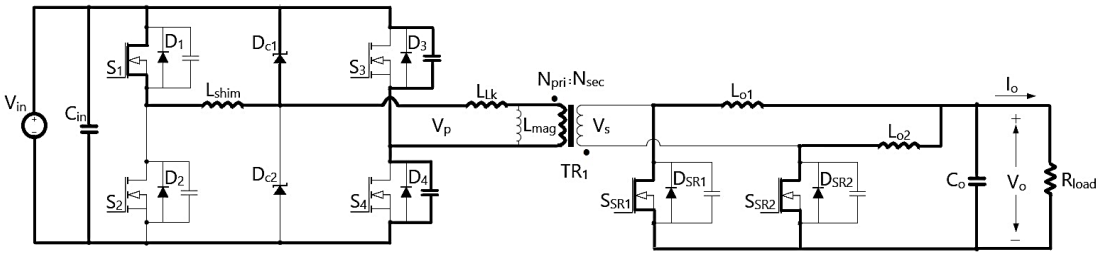

Figure 3.16 : Operation of PSFB-CDR converter between t_2-t_3-1.

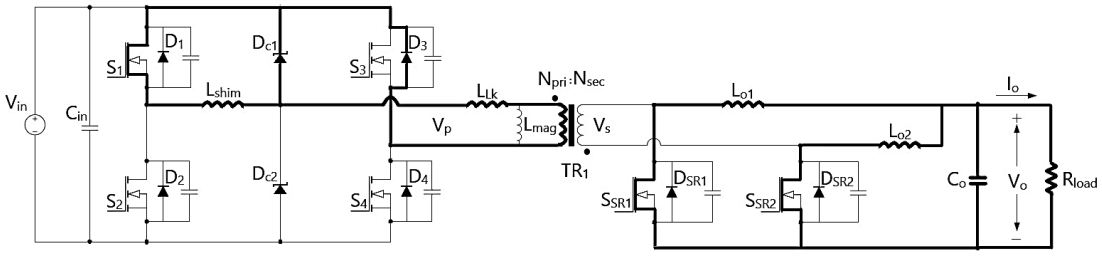

Figure 3.17 : Operation of PSFB-CDR converter between t_2-t_3-2.

Mode 4: Freewheeling Mode (t_3-t_4)

This time interval is named as freewheeling mode since I_p recirculates over high-side switches. There is not any power transfer during this mode. At t_3, switch S_3 is turned on with ZVS. V_p and V_s are zero. L_{o1} and L_{o2} are discharging.

D_{c1} is still conducting because of the mentioned voltage change at transformer primary side suddenly which causes a current difference between I_p and the current of L_{shim}. The operation of the PSFB-CDR converter between t_3-t_4 is given in Figure 3.18.

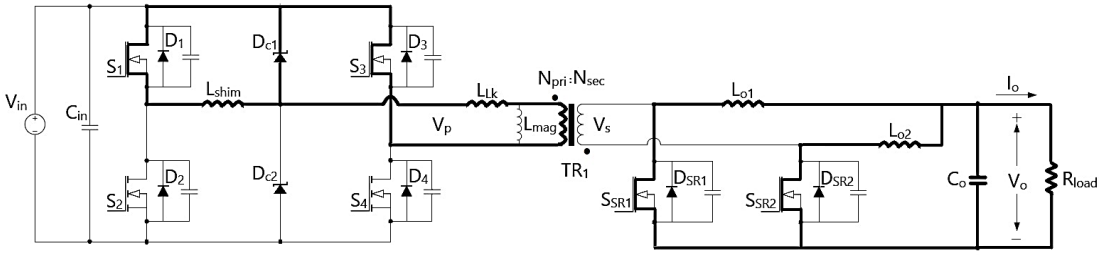

Figure 3.18 : Operation of PSFB-CDR converter between t_3-t_4.

Mode 5: Switch S_2 ZVS Mode (t_4-t_5)

At t_4, switch S_1 is turned off, the capacitance of S_1 is charged, and the capacitance of S_2 is discharged. When switch S_2 is discharged to zero, its body diode conducts to achieve ZVS condition. V_p and V_s become zero. Both S_{SR1} and S_{SR2} are conducting. L_{o1} and L_{o2} are discharging. The operation of the PSFB-CDR converter between t_4-t_5 is given in Figure 3.19 and Figure 3.20.

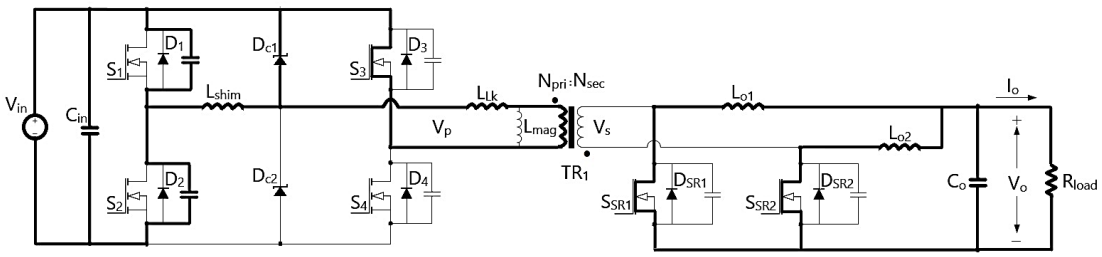

Figure 3.19 : Operation of PSFB-CDR converter between t_4-t_5-1.

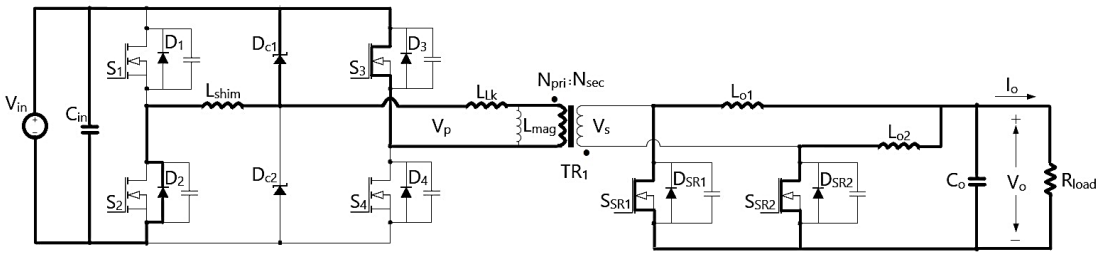

Figure 3.20 : Operation of PSFB-CDR converter between t_4-t_5-2.

Mode 6: Duty Cycle Loss Mode (t_5-t_6)

At t_5, switch S_2 is turned on with ZVS. No power is delivered to the output in this mode. Both secondary side switches, S_{SR1} and S_{SR2}, conduct current, although S_{SR1} is gated off. Not only output inductor L_{o1} but also other output inductor L_{o2} are discharging. The voltage of the transformer primary side V_p is equal to the supply voltage V_{in} theoretically. However, voltage of the transformer secondary side V_s remains zero until the primary side current of transformer I_p reverses its direction and reaches the reflected output inductor current at t_6. I_p rises with a slope which depends on the V_{in} and both shim inductor L_{shim} and leakage inductor of transformer L_{lk}. The operation of the PSFB-CDR converter between t_5-t_6 is given in Figure 3.21.

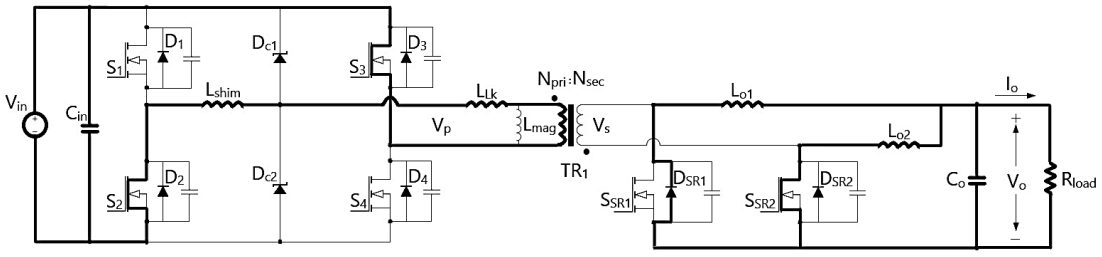

Figure 3.21 : Operation of PSFB-CDR converter between t_5-t_6.

Mode 7: Power Delivery Mode (t_6-t_7)

Power is delivered at this time interval and effective duty cycle ph_{eff} time interval starts at t_6 and ends at t_7. V_p is equal to supply voltage V_{in}. V_s is equal to the multiplication of V_{in} with transformer turns ratio (N_{pri}: N_{sec}) at t_6. Only S_{SR2} is on and carries both inductors current. L_{o1} is charging; however, L_{o2} is discharging. I_p is equal to the reflected output inductor current with respect to the transformer turns ratio.

S_{SR1} is turned off; this means that the switch output charge Q_{oss} and body diode reverse recovery charge Q_{rr} are charged. This energy is provided by the primary side of the

converter. Additional current flows over L_{shim} and L_{lk} and stored energy is increased. D_{c2} starts conduction when current through the L_{shim} rises above the I_p due to the charge of the rectifier's Q_{oss} and Q_{rr} at the start of the power transfer [41]. D_{c2} stops conduction at the point that the current of L_{shim} is equal to I_p. The operation of the PSFB-CDR converter between t_6-t_7 is given in Figure 3.22 and Figure 3.23.

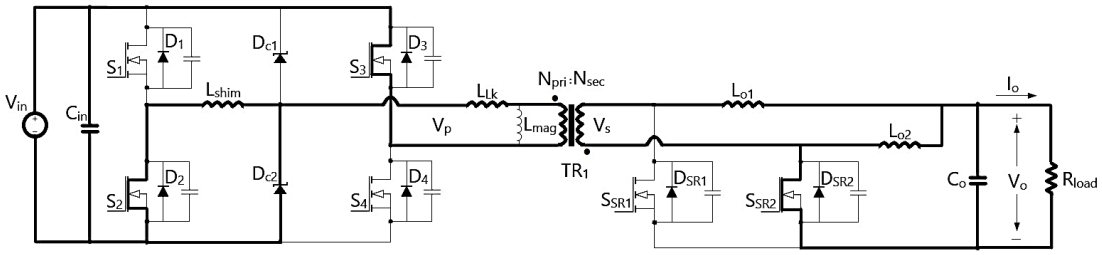

Figure 3.22 : Operation of PSFB-CDR converter between t_6-t_7-1.

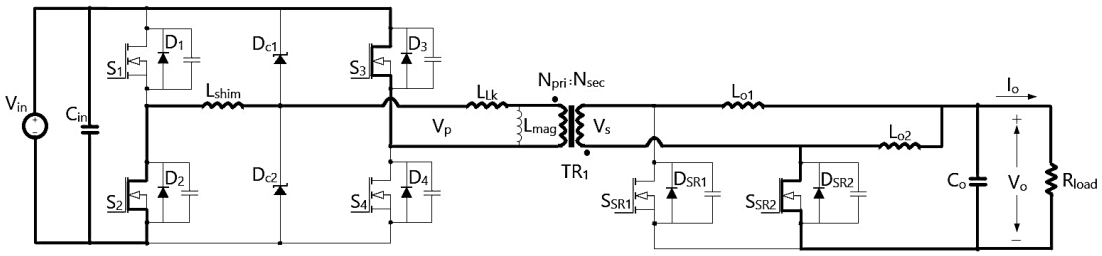

Figure 3.23 : Operation of PSFB-CDR converter between t_6-t_7-2.

Mode 8: Switch S_4 ZVS Mode (t_7-t_8)

At t_7, switch S_3 is turned off, the capacitance of S_3 is charged, and the capacitance of S_4 is discharged. When switch S_4 is discharged to zero, its body diode conducts to achieve the ZVS condition. V_p and V_s become zero. Both S_{SR1} and S_{SR2} are conducting. L_{o1} and L_{o2} are discharging.

During this operating mode, the voltage at the primary side of the transformer suddenly decreases from $-V_{in}$ to zero. This situation leads to a decrease in the current with a steep slope. However, L_{shim} does not face this kind of voltage change over itself. Thus the current of L_{shim} does not as change as transformer primary side current. This difference is that current flows through the diode, which is D_{c2} [42]. The operation of the PSFB-CDR converter between t_7-t_8 is given in Figure 3.24 and Figure 3.25.

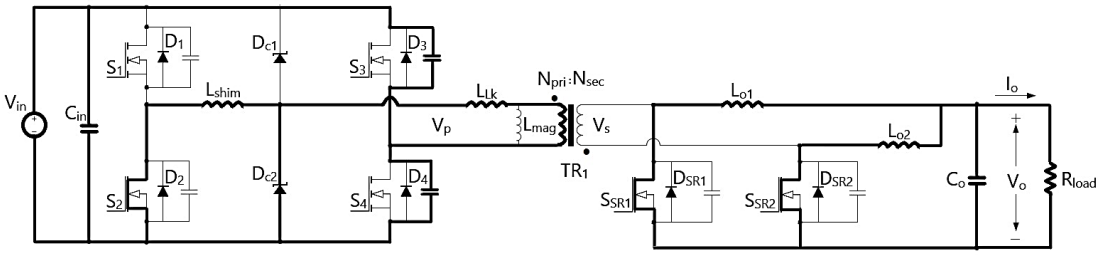

Figure 3.24 : Operation of PSFB-CDR converter between t_7-t_8-1.

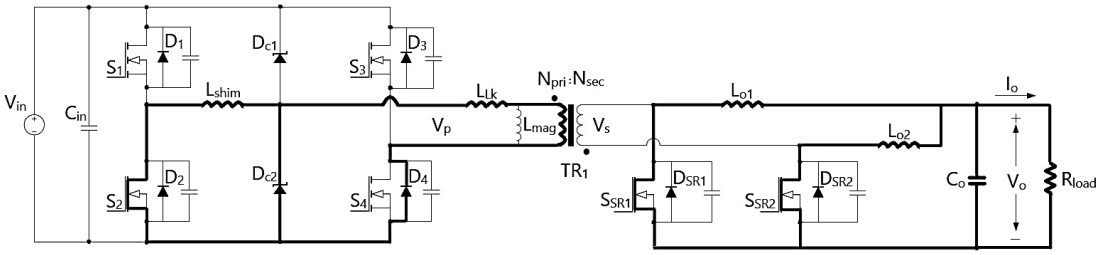

Figure 3.25 : Operation of PSFB-CDR converter between t_7-t_8-2.

Mode 9: Freewheeling Mode (t_8-t_9)

At this time duration, which is the freewheeling mode, I_p is recirculating over low-side switches. There is not any power transfer during this mode. At t_8, switch S_4 is turned on with ZVS. V_p and V_s are zero. Both S_{SR1} and S_{SR2} are conducting. L_{o1} and L_{o2} are discharging.

D_{c2} is still conducting because of mentioned voltage change at transformer primary side suddenly which causes a current difference between I_p and the current of L_{shim}. The operation of the PSFB-CDR converter between t_8-t_9 is given in Figure 3.26.

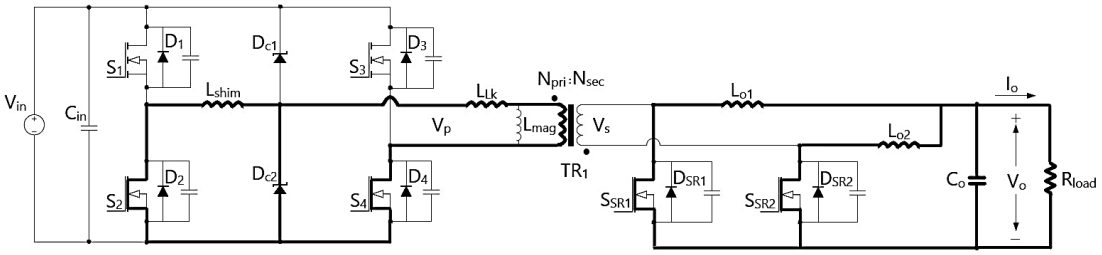

Figure 3.26 : Operation of PSFB-CDR converter between t_8-t_9.

Mode 10: Switch S_1 ZVS Mode (t_9-t_{10})

At t_9, switch S_2 is turned off, the capacitance of S_2 is charged, and the capacitance of S_1 is discharged. When switch S_1 is discharged to zero, its body diode conducts to achieve the ZVS condition. V_p and V_s become zero. Both S_{SR1} and S_{SR2} are conducting.

L_{o1} and L_{o2} are discharging. The operation of the PSFB-CDR converter between t_9-t_{10} is given in Figure 3.27 and Figure 3.28.

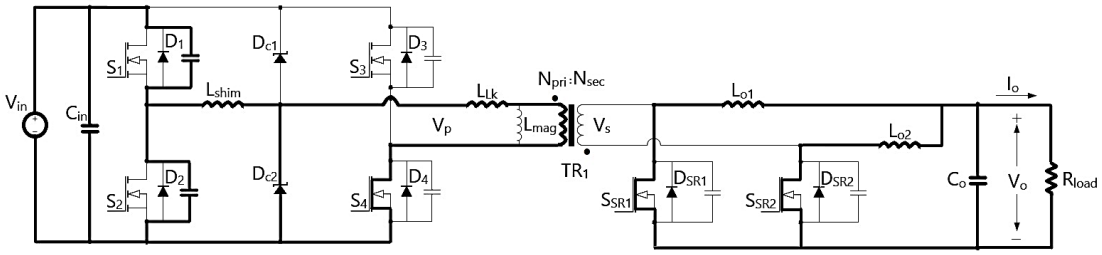

Figure 3.27 : Operation of PSFB-CDR converter between t_9-t_{10}-1.

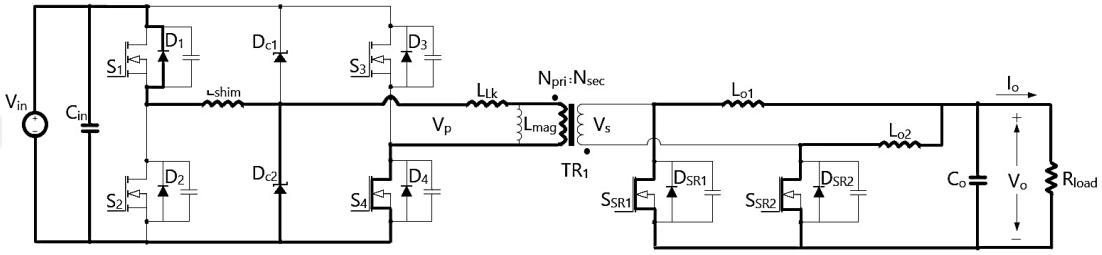

Figure 3.28 : Operation of PSFB-CDR converter between t_9-t_{10}-2.

4. DESIGN OF THE PSFB WITH CDR CONVERTER

In this chapter, the analytical calculation to design PSFB with CDR has been given step by step. Additionally, the parameters of all the magnetic components of the converter are calculated. Detailed information on the manufactured magnetics components is also shared. It is quite important to select the proper turns ratio of the transformer to satisfy the duty cycle limitation of topology and also the target operation range. Moreover, calculated values, especially for magnetic components and capacitors has to be manufacturable and exist in the market.

One of the major criteria is also to achieve ZVS behavior with leakage inductance of the transformer and parasitic output capacitance of switches for determined output current. Additional inductance can be considered according to the calculation to achieve and extend this ZVS boundary. On the other hand, it has a side effect of decreasing the resonant frequency during voltage transition. Thus increased deadtime is required, which is not desired in high-switching frequency applications. For that reason, it is logical to reduce the capacitive energy in the circuit rather than increase the inductive energy. This implies the necessity of low MOSFET output capacitance for this converter and other ZVS topologies in general. Schematic of the PSFB-CDR converter is given in Figure 4.1.

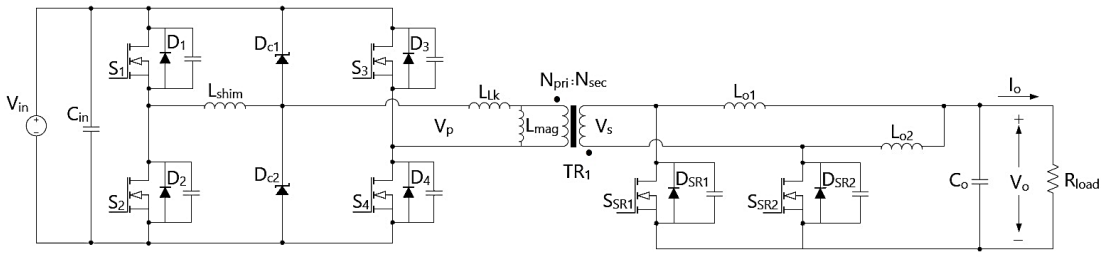

Figure 4.1 : Schematic of PSFB-CDR converter.

4.1 Design Calculations of Power Stage of the PSFB with CDR Converter

All analytical calculations will be given step by step, yet some specifications have to be identified which are given in Table 4.1 before starting the calculation. Each

calculation has been done at each operating condition point to provide working functionally.

The nominal operating condition of the converter is 400 V as the input voltage, 12 V as the output voltage and 250 A as the output current.

Table 4.1 : Operating points specification

Power rating (P_o):	3 kW
Input voltage (V_{in}):	240 V – 475 V
Output voltage (V_o):	10.9 V – 14 V
Output current (I_o):	214 A – 275 A
Target efficiency:	95%
Direction:	Unidirectional
Switching frequency (f_{sw}):	100 kHz

4.1.1 Calculation of switches

The calculation of the current of primary switches requires roughly knowing the turns ratio as a first step. If the maximum effective duty cycle $D_{m\text{-}eff}$ is assumed as 45%, the turns ratio, which is the primary side turns N_{pri} over the secondary side turns N_{sec}, is calculated as around 7. Primary side switches root mean square (RMS) current $I_{pri,rms}$ and secondary side switches RMS current $I_{SR,rms}$ are calculated using equation 4.1 and equation 4.2 [43]. $I_{pri,rms}$ and $I_{SR,rms}$ are calculated as in Table 4.2 and Table 4.3, respectively.

$$I_{pri,rms} = \frac{I_0}{2} \cdot \frac{N_s}{N_p} \sqrt{\frac{1}{2}} \tag{4.1}$$

Table 4.2 : Primary side switches RMS current value.

Operating Conditions	$I_{pri,rms}$ (A)
V_{in}:240 V, V_o:14 V, I_o:214 A	10.82
V_{in}:475 V, V_o:14 V, I_o:214 A	10.82
V_{in}:475 V, V_o:10.9 V, I_o:275 A	13.90
V_{in}:240 V, V_o:10.9 V, I_o:275 A	13.90

The current which flows over the secondary side switch is quite high and causes high losses. Thus the rectification stage, which is the secondary side is designed as CDR with two parallel switches for each operating cycle. The calculated value of $I_{SR,rms}$ belongs to each paralleled switch. D_{eff} is an effective duty cycle, which is explained in the following calculation.

$$I_{SR,rms} = \frac{I_o}{2}\sqrt{D_{eff} + \frac{1}{4}} \tag{4.2}$$

Table 4.3 : Secondary side switches RMS current value.

Operating Conditions	$I_{SR,rms}$ (A)
V_{in}:240 V, V_o:14 V, I_o:214 A	87.54
V_{in}:475 V, V_o:14 V, I_o:214 A	72.66
V_{in}:475 V, V_o:10.9 V, I_o:275 A	88.64
V_{in}:240 V, V_o:10.9 V, I_o:275 A	104.68

Maximum voltage stress on the primary side equals to input voltage V_{in}, which is 475 V. Primary side switch is selected as SiC MOSFET AIMDQ75R040M1H from Infineon. The voltage stress on the secondary side $V_{SR,stress}$, which depends on output voltage V_o and D_{eff}, is calculated as in equation 4.3 [43]. According to the calculation $V_{SR,stress}$ is found in Table 4.4.

$$V_{SR,stress} = \frac{V_o}{D_{eff}} \tag{4.3}$$

Table 4.4 : Voltage stress on the secondary side.

Operating Conditions	$V_{SR,stress}$ (V)
V_{in}:240 V, V_o:14 V, I_o:214 A	33.53
V_{in}:475 V, V_o:14 V, I_o:214 A	66.69
V_{in}:475 V, V_o:10.9 V, I_o:275 A	66.08
V_{in}:240 V, V_o:10.9 V, I_o:275 A	33.17

With consideration of the calculated values, the secondary side switch is selected as Si MOSFET IAUTN12S5N018T from Infineon. Both of these switches have top side-cooled feature to have low thermal resistance, which leads to better cooling performance.

In addition to the calculated current and voltage values, the primer switches have low output capacitance C_{oss} for extended ZVS range and short deadtime designs. Moreover, its body diode has a fast reverse recovery value. The secondary switch has to low R_{dson}, C_{oss}, and reverse recovery charge Q_{rr} to keep switching and conduction losses as low as possible.

According to datasheet information of selected both primer and seconder switches, voltage drops are calculated as in equation 4.4. V_{in} is the input voltage. $V_{Rdson\text{-}pri}$ is the

primary side switch voltage drop and $V_{Rdson\text{-}SR}$ is the secondary side switch voltage drop. Calculated values are given in Table 4.5 and Table 4.6, respectively.

$$V_{Rdson} = I_{rms} \cdot R_{dson} \tag{4.4}$$

Table 4.5 : Primary side switch voltage drop.

Operating Conditions	$V_{Rdson\text{-}pri}$ (V)
V_{in}:240 V, V_o:14 V, I_o:214 A	0.43
V_{in}:475 V, V_o:14 V, I_o:214 A	0.43
V_{in}:475 V, V_o:10.9 V, I_o:275 A	0.56
V_{in}:240 V, V_o:10.9 V, I_o:275 A	0.56

Table 4.6 : Secondary side switch voltage drop.

Operating Conditions	$V_{Rdson\text{-}SR}$ (V)
V_{in}:240 V, V_o:14 V, I_o:214 A	0.13
V_{in}:475 V, V_o:14 V, I_o:214 A	0.11
V_{in}:475 V, V_o:10.9 V, I_o:275 A	0.13
V_{in}:240 V, V_o:10.9 V, I_o:275 A	0.16

Turn-on switching loss is zero for the primary side switches, since it is a ZVS converter.

It is important to know the turn-off delay time $t_{d(off)}$ and fall time t_f for turn-off switching loss $P_{pri,off}$ calculation. These values, which are 20 ns and 8 ns, respectively, are taken from the datasheet of primary MOSFET. The summation of $t_{d(off)}$ and t_f is mentioned as t_{off}, which is 28 ns. Detailed calculation of $I_{Lo,max}$, which is the maximum value of output inductor current, is given in equation 4.22. $P_{pri,off}$ is calculated as in equation 4.5. Calculated values are given in Table 4.7.

$$P_{pri,off} = \frac{1}{6} \cdot I_{Lo,max} \cdot \frac{N_s}{N_p} \cdot V_{in} \cdot t_{off} \cdot f_{sw} \tag{4.5}$$

Table 4.7 : Switching loss of the primary side switches.

Operating Conditions	$P_{pri,off}$ (W)
V_{in}:240 V, V_o:14 V, I_o:214 A	1.97
V_{in}:475 V, V_o:14 V, I_o:214 A	4.09
V_{in}:475 V, V_o:10.9 V, I_o:275 A	4.93
V_{in}:240 V, V_o:10.9 V, I_o:275 A	2.42

Switching loss calculation of the secondary side switches $P_{SR,sw}$ is calculated as in equation 4.6. Output capacitance value C_{oss} changes according to voltage value. This

value can be observed from the datasheet of the selected switch. Calculated values are given in Table 4.8.

$$P_{SR,sw} = 0.5 \cdot V_{in}{}^2 \cdot C_{oss} \cdot f_{sw} \tag{4.6}$$

Table 4.8 : Switching loss of the secondary side switches.

Operating Conditions	$P_{SR,sw}$ (W)
V_{in}:240 V, V_o:14 V, I_o:214 A	0.22
V_{in}:475 V, V_o:14 V, I_o:214 A	0.44
V_{in}:475 V, V_o:10.9 V, I_o:275 A	0.44
V_{in}:240 V, V_o:10.9 V, I_o:275 A	0.22

Another main loss of switches is conduction losses P_{cond}. For both primary and secondary conduction losses are calculated according to equation 4.7. On resistance values R_{on} are obtained from the datasheet. Calculated values are given in Table 4.9 and Table 4.10. for primary and secondary switches conduction losses $P_{P,cond}$, $P_{SR,cond}$ respectively.

$$P_{cond} = I_{rms}{}^2 \cdot R_{on} \tag{4.7}$$

Table 4.9 : Conduction loss of the primary side switches.

Operating Conditions	$P_{P,cond}$ (W)
V_{in}:240 V, V_o:14 V, I_o:214 A	4.68
V_{in}:475 V, V_o:14 V, I_o:214 A	4.68
V_{in}:475 V, V_o:10.9 V, I_o:275 A	7.73
V_{in}:240 V, V_o:10.9 V, I_o:275 A	7.73

Table 4.10 : Conduction loss of the secondary side switches.

Operating Conditions	$P_{SR,cond}$ (W)
V_{in}:240 V, V_o:14 V, I_o:214 A	11.49
V_{in}:475 V, V_o:14 V, I_o:214 A	7.92
V_{in}:475 V, V_o:10.9 V, I_o:275 A	11.79
V_{in}:240 V, V_o:10.9 V, I_o:275 A	16.44

Gate losses P_{gate} occur while switches are switching. This loss depends on gate voltage V_g, gate charge Q_g, and f_{sw}. Primary switch V_g is +15, -5V and secondary switch V_g is 10V. Q_g values are obtained from datasheets. P_{gate} of primary and secondary switches are calculated as in equation 4.8, and results are 68 mW and 111 mW for each switch, respectively.

$$P_{gate} = V_g \cdot Q_g \cdot f_{sw} \quad (4.8)$$

The overall loss, which is summation switching, conduction, and gate losses, is given in Table 4.11 for each primary side switch and Table 4.12 for each secondary side switch.

Table 4.11 : Total loss of the primary side switches.

Operating Conditions	$P_{P,\,total}$ (W)
V_{in}:240 V, V_o:14 V, I_o:214 A	6.73
V_{in}:475 V, V_o:14 V, I_o:214 A	8.85
V_{in}:475 V, V_o:10.9 V, I_o:275 A	12.73
V_{in}:240 V, V_o:10.9 V, I_o:275 A	10.23

Table 4.12 : Total loss of the secondary side switches.

Operating Conditions	$P_{SR,\,total}$ (W)
V_{in}:240 V, V_o:14 V, I_o:214 A	11.83
V_{in}:475 V, V_o:14 V, I_o:214 A	8.47
V_{in}:475 V, V_o:10.9 V, I_o:275 A	12.33
V_{in}:240 V, V_o:10.9 V, I_o:275 A	16.77

4.1.2 Calculation of transformer

The turn ratio has been roughly calculated as seven in the previous calculation. However, it has to be validated with consideration of voltage drop-over switches. Maximum effective duty cycle $D_{m\text{-}eff}$ value is decided as 47%, since deadtime and duty cycle loss time have to be considered. The turn ratio of the transformer is calculated as seven according to equation 4.9 [44]. Calculated values are given in Table 4.13.

$$\frac{N_p}{N_s} = \frac{(V_{in} - 2 \cdot V_{Rdson-pri}) \cdot D_{eff}}{V_O + V_{Rdson-SR}} \quad (4.9)$$

Table 4.13 : Turn ratio of the transformer.

Operating Conditions	N_p/N_s
V_{in}:240 V, V_o:14 V, I_o:214 A	7.06
V_{in}:475 V, V_o:14 V, I_o:214 A	7.05
V_{in}:475 V, V_o:10.9 V, I_o:275 A	7.08
V_{in}:240 V, V_o:10.9 V, I_o:275 A	7.09
N_p/N_s (selected)	7

Magnetizing inductance of transformer L_{mag} is another important parameter of the transformer. It has to be sufficient to enable proper converter operation. On the other hand, wrong-selected transformer in terms of L_{mag} causes efficiency drop and control

problem. L_{mag} is calculated in equation 4.10 [44]. The output inductors current ripple is ΔI_{Lo1}. Calculated values are given in Table 4.14 and selected as 1.5 mH as a result of the calculation.

$$L_{mag} \geq \frac{V_{in} \cdot (1 - D_{eff})}{\frac{\Delta I_{Lo1} \cdot 0.5}{\frac{N_p}{N_s}} \cdot f_{sw}} \tag{4.10}$$

Table 4.14 : Magnetizing inductance value of transformer.

Operating Conditions	L_{mag} (mH)
V_{in}:240 V, V_o:14 V, I_o:214 A	0.6
V_{in}:475 V, V_o:14 V, I_o:214 A	1.19
V_{in}:475 V, V_o:10.9 V, I_o:275 A	1.53
V_{in}:240 V, V_o:10.9 V, I_o:275 A	0.77
L_{mag} (selected)	1.5

This selected L_{mag} value is shared with the manufacturer and discussed about producibility, then L_{mag} value is decided as 1.08 mH according to the final decision with the manufacturer. Magnetizing inductor current ripple ΔL_{mag} is calculated as equation 4.11 [44]. Calculated values are given in Table 4.15.

$$\Delta I_{Lmag} = \frac{V_{in} \cdot D_{eff}}{L_{mag} \cdot f_{sw}} \tag{4.11}$$

Table 4.15 : Magnetizing inductor current ripple value of transformer.

Operating Conditions	ΔI_{Lmag} (A)
V_{in}:240 V, V_o:14 V, I_o:214 A	0.93
V_{in}:475 V, V_o:14 V, I_o:214 A	0.93
V_{in}:475 V, V_o:10.9 V, I_o:275 A	0.73
V_{in}:240 V, V_o:10.9 V, I_o:275 A	0.73

The primary side current of transformer $I_{TR\text{-}pri,rms}$ and secondary side current of the transformer $I_{TR\text{-}sec,rms}$ have to be known to design the proper transformer during the prototyping stage. These values are calculated by equation 4.12 and equation 4.13 [43]. Calculated values are given in Table 4.16 and Table 4.17.

$$I_{TR-pri,rms} = \frac{I_o}{2} \cdot \frac{N_s}{N_p} \tag{4.12}$$

Table 4.16 : Primary side RMS current value of transformer.

Operating Conditions	$I_{TR\text{-}pri,rms}$ (A)
V_{in}:240 V, V_o:14 V, I_o:214 A	15.31
V_{in}:475 V, V_o:14 V, I_o:214 A	15.31
V_{in}:475 V, V_o:10.9 V, I_o:275 A	19.66
V_{in}:240 V, V_o:10.9 V, I_o:275 A	19.66

$$I_{TR-sec,rms} = I_o \sqrt{D_{eff}} \tag{4.13}$$

Table 4.17 : Secondary side RMS current value of transformer.

Operating Conditions	$I_{TR\text{-}sec,rms}$ (A)
V_{in}:240 V, V_o:14 V, I_o:214 A	138.46
V_{in}:475 V, V_o:14 V, I_o:214 A	98.18
V_{in}:475 V, V_o:10.9 V, I_o:275 A	111.78
V_{in}:240 V, V_o:10.9 V, I_o:275 A	157.77

Peak current $I_{TR\text{-}pp}$ and minimum current $I_{TR\text{-}pm}$, which flows over the primary side of the transformer, are calculated as in equation 4.14 and equation 4.15, respectively [44]. Calculated values are given in Table 4.18 and Table 4.19.

$$I_{TR-pp} = \left(\frac{P_{out}}{V_o \cdot \eta} + \frac{\Delta I_{Lo1}}{2}\right) \cdot \frac{N_s}{N_p} + \Delta I_{Lmag} \tag{4.14}$$

Table 4.18 : Primary side peak current value of transformer.

Operating Conditions	$I_{TR\text{-}pp}$ (A)
V_{in}:240 V, V_o:14 V, I_o:214 A	19.11
V_{in}:475 V, V_o:14 V, I_o:214 A	19.94
V_{in}:475 V, V_o:10.9 V, I_o:275 A	23.82
V_{in}:240 V, V_o:10.9 V, I_o:275 A	23.31

$$I_{TR-pm} = \left(\frac{P_{out}}{V_o \cdot \eta} - \frac{\Delta I_{Lo1}}{2}\right) \cdot \frac{N_s}{N_p} - \Delta I_{Lmag} \tag{4.15}$$

Table 4.19 : Primary side minimum current value of transformer.

Operating Conditions	$I_{TR\text{-}pm}$ (A)
V_{in}:240 V, V_o:14 V, I_o:214 A	13.11
V_{in}:475 V, V_o:14 V, I_o:214 A	12.29
V_{in}:475 V, V_o:10.9 V, I_o:275 A	17.57
V_{in}:240 V, V_o:10.9 V, I_o:275 A	18.08

4.1.3 Calculation of critical timings

D_{eff} has to be checked to see whether it satisfies the limit of $D_{m\text{-}eff}$, which is selected as 47% with the selected transformer turns ratio for operating condition intervals. Effective duty cycle means that power transfer exists during this time interval. I_o is output current. Maximum D_{eff} value is calculated as 41.7% for 240 V as V_{in}, 14 V as V_o, and 214 A as I_o by equation 4.15 [44]. Calculated values are given in Table 4.20.

$$D_{eff} = \frac{\frac{N_p}{N_s} \cdot (V_O + V_{Rdson-SR})}{(V_{in} - 2 \cdot V_{Rdson-pri})} \tag{4.15}$$

Table 4.20 : Effective duty cycle.

Operating Conditions	D_{eff} (%)
V_{in}:240 V, V_o:14 V, I_o:214 A	41.7
V_{in}:475 V, V_o:14 V, I_o:214 A	20.99
V_{in}:475 V, V_o:10.9 V, I_o:275 A	16.49
V_{in}:240 V, V_o:10.9 V, I_o:275 A	32.86

Deadtime t_{dead} is critical to achieve ZVS and high efficiency. Resonant period T_r is the limitation for t_{dead} as in equation 4.16 [43]. L_k is the summation of L_{shim} and L_{lk}. L_{lk} value is 1.8 µH which belongs to the designed transformer with the manufacturer. C_{TR} is transformer parasitic capacitance which could be neglected, since it is quite small when compared with time-related output capacitance of primer switches $C_{pri\text{-}coss(tr)}$. Resonant frequency f_r is calculated by equation 4.17 [14]. Pursuant to these calculations, t_{dead} is selected as 100 ns. Related parameters are given in Table 4.21.

$$t_{dead} \geq {}^{T_r}/_{4} \tag{4.16}$$

$$f_r = \frac{1}{2 \cdot \pi \cdot \sqrt{L_k \cdot \left(2 \cdot C_{pri-coss(tr)} + C_{TR}\right)}} \tag{4.17}$$

Table 4.21 : Deadtime with related parameters.

$C_{pri\text{-}coss(tr)}$	136 pF
L_k	3.3 µH
f_r	5.29 MHz
T_r	47.23 ns
t_{dead} (selected)	100 ns

Duty cycle loss time t_{loss} is the time interval in the duty cycle which does not provide power delivery. t_{loss} could be observed at each half switching cycle during the

commutation of current. This time is calculated as equation 4.18 [43]. Calculated values are given in Table 4.22.

$$t_{loss} = I_o \cdot \left(\frac{N_s}{N_p}\right) \cdot \frac{L_k}{V_{in}} \cdot f_{sw} \quad (4.18)$$

Table 4.22 : Duty cycle loss time.

Operating Conditions	t_{loss} (µs)
V_{in}:240 V, V_o:14 V, I_o:214 A	0.42
V_{in}:475 V, V_o:14 V, I_o:214 A	0.21
V_{in}:475 V, V_o:10.9 V, I_o:275 A	0.27
V_{in}:240 V, V_o:10.9 V, I_o:275 A	0.54

As mentioned, there is a duty cycle limitation, which is 50% for phase-shifted full-bridge topology inherently. The target is that not to exceed 47% because of the safety margin. D_{max} is the summation of D_{eff}, t_{dead}, and t_{loss}. Selected D_{max} is satisfied, as seen in Table 4.23.

Table 4.23 : Maximum duty cycle.

Operating Conditions	D_{max} (%)
V_{in}:240 V, V_o:14 V, I_o:214 A	46.9
V_{in}:475 V, V_o:14 V, I_o:214 A	23.1
V_{in}:475 V, V_o:10.9 V, I_o:275 A	19.2
V_{in}:240 V, V_o:10.9 V, I_o:275 A	38.3

4.1.4 Calculation of inductors

First of all, target current ripple values on the output inductors ΔI_{Lo1} and ΔI_{Lo2} have to be selected to calculate the suitable inductance value for output inductors L_{o1} and L_{o2} as given in equation 4.19 [43]. The target ripple value is chosen as 30%. Calculated values are given in Table 4.24. Afterwards, L_{o1} and L_{o2} are calculated by equation 4.20 [43]. T is the period of switching. Calculated values are given in Table 4.25.

$$\Delta I_{Lo1} = \Delta I_{Lo2} = \%Ripple \cdot \frac{I_o}{2} \quad (4.19)$$

Table 4.24 : Target current ripple of output inductor.

Operating Conditions	ΔI_{Lo1}, ΔI_{Lo2} (A)
V_{in}:240 V, V_o:14 V, I_o:214 A	32.14
V_{in}:475 V, V_o:14 V, I_o:214 A	32.14
V_{in}:475 V, V_o:10.9 V, I_o:275 A	41.28
V_{in}:240 V, V_o:10.9 V, I_o:275 A	41.28

$$L_{o1} = L_{o2} = \frac{1}{\Delta I_{Lo1}} \cdot V_o \cdot (1 - D_{eff}) \cdot T \quad (4.20)$$

Table 4.25 : Inductance value of output inductor.

Operating Conditions	L_{o1}, L_{o2} (µH)
V_{in}:240 V, V_o:14 V, I_o:214 A	2.54
V_{in}:475 V, V_o:14 V, I_o:214 A	3.44
V_{in}:475 V, V_o:10.9 V, I_o:275 A	2.2
V_{in}:240 V, V_o:10.9 V, I_o:275 A	1.77
L_{o1}, L_{o2} (selected)	2.5

The inductance value is calculated as 3.44 µH. When producibility is considered, available space on the designed PCB is not enough to have an inductor which has this current rating and inductance value. Thus, the inductance value is selected as 2.5 µH. According to the selected output inductance value, which is 2.5 µH, ΔI_{Lo1}, and ΔI_{Lo2} are recalculated as current value and percentage in Table 4.26.

Table 4.26 : Current ripple for selected output inductance value.

Operating Conditions	ΔI_{Lo1}, ΔI_{Lo2} (A)
V_{in}:240 V, V_o:14 V, I_o:214 A	32.62
V_{in}:475 V, V_o:14 V, I_o:214 A	44.24
V_{in}:475 V, V_o:10.9 V, I_o:275 A	36.41
V_{in}:240 V, V_o:10.9 V, I_o:275 A	29.27

To design a proper inductor, it is important to know the RMS current value and maximum and minimum current value. The RMS current rating of L_{o1} and L_{o2} ($I_{Lo1,RMS}$, $I_{Lo2,RMS}$) is half of the output current as in equation 4.21, since the rectification side configuration is a current doubler [43]. Calculated values are given in Table 4.27.

$$I_{Lo1,RMS} = I_{Lo2,RMS} = \frac{I_o}{2} \quad (4.21)$$

Table 4.27 : RMS current value of output inductor.

Operating Conditions	$I_{Lo1,RMS}$, $I_{Lo2,RMS}$ (A)
V_{in}:240 V, V_o:14 V, I_o:214 A	107.14
V_{in}:475 V, V_o:14 V, I_o:214 A	107.14
V_{in}:475 V, V_o:10.9 V, I_o:275 A	137.61
V_{in}:240 V, V_o:10.9 V, I_o:275 A	137.61

According to the selected L_{o1} and L_{o2}, maximum and minimum current values $I_{Lo,max}$, $I_{Lo,min}$, which flow through that component, are calculated as below in equation 4.22

and equation 4.23, respectively [43]. P_o is output power. Calculated values are given in Table 4.28 and Table 4.29. of $I_{Lo,max}$ and $I_{Lo,min}$.

$$I_{Lo,max} = \frac{P_o}{2 \cdot V_o} + \frac{\Delta I_{Lo1}}{2} \tag{4.22}$$

Table 4.28 : Maximum current value of output inductor.

Operating Conditions	$I_{Lo,max}$ (A)
V_{in}:240 V, V_o:14 V, I_o:214 A	123.45
V_{in}:475 V, V_o:14 V, I_o:214 A	129.27
V_{in}:475 V, V_o:10.9 V, I_o:275 A	155.82
V_{in}:240 V, V_o:10.9 V, I_o:275 A	152.25

$$I_{Lo,min} = \frac{P_o}{2 \cdot V_o} - \frac{\Delta I_{Lo1}}{2} \tag{4.23}$$

Table 4.29 : Minimum current value of output inductor.

Operating Conditions	$I_{Lo,min}$ (A)
V_{in}:240 V, V_o:14 V, I_o:214 A	90.83
V_{in}:475 V, V_o:14 V, I_o:214 A	85.02
V_{in}:475 V, V_o:10.9 V, I_o:275 A	119.41
V_{in}:240 V, V_o:10.9 V, I_o:275 A	122.98

Shim inductance is another critical component to extend the ZVS range; on the other hand, inductance value directly affects the duty cycle loss interval. $C_{pri\text{-}coss(er)}$ is the energy-related output capacitance of primer switches. According to the calculation in equation 4.24 [44]. The required inductance value is calculated based on the required amount of inductive energy to achieve ZVS at the specified load condition. This inductive energy has to deplete the capacitive energy of the switches in the switching node. Calculated values are given in Table 4.30, and the shim inductance value L_{shim} is selected as 1.5 µH.

$$L_{shim} \geq 2 \cdot C_{pri-coss(er)} \cdot \frac{V_{in}^2}{\left(\frac{I_{TR-pp}}{2} - \frac{\Delta I_{Lo1}}{2 \cdot \frac{N_p}{N_s}} \right)^2} \tag{4.24}$$

Table 4.30 : Inductance value of shim inductor.

Operating Conditions	L_{shim} (µH)
V_{in}:240 V, V_o:14 V, I_o:214 A	0.21
V_{in}:475 V, V_o:14 V, I_o:214 A	0.92
V_{in}:475 V, V_o:10.9 V, I_o:275 A	0.5
V_{in}:240 V, V_o:10.9 V, I_o:275 A	0.12
L_{shim} (selected)	1.5

Moreover, the inductance value of the manufactured shim inductance is 1.5 µH.

4.1.5 Calculation of capacitors

Input capacitance C_{in} is selected pursuant to the decided minimum input voltage V_{drop} that the converter could operate during the holdup time t_{hold} as in equation 4.25 [44]. $V_{in,min}$ is the minimum input voltage, which is 240 V. C_{in} is selected as 6.6 µF when V_{drop} is 220 V, and t_{hold} is 10 µs. The number of paralleled capacitors is determined according to the RMS current delivered from the C_{in} that is mentioned as $I_{Cin\text{-}rms}$ by equation 4.26 [43]. Calculated values are given in Table 4.31.

Two paralleled 3.3 µF capacitors, which are B32774P7335K from TDK Electronics, are selected.

$$C_{in} \geq \frac{2 \cdot P_o \cdot t_{hold}}{\left({V_{in,min}}^2 - {V_{drop}}^2\right)} \tag{4.25}$$

$$I_{Cin-rms} = \sqrt{2 \cdot D_{eff} \cdot \left(\frac{I_o}{2} \cdot \frac{N_{sec}}{N_{pri}} - \frac{P_o}{V_{in}}\right)^2 + 2 \cdot (0.5 - D_{eff}) \left(\frac{P_o}{V_{in}}\right)^2} \tag{4.26}$$

Table 4.31 : RMS current of input capacitor.

Operating Conditions	$I_{Cin\text{-}rms}$ (A)
V_{in}:240 V, V_o:14 V, I_o:214 A	5.68
V_{in}:475 V, V_o:14 V, I_o:214 A	7.54
V_{in}:475 V, V_o:10.9 V, I_o:275 A	9.24
V_{in}:240 V, V_o:10.9 V, I_o:275 A	9.33

Output load current ripple ΔI_o before the DC-link capacitor is calculated as in equation 4.27 [43]. Calculated values are given in Table 4.32. Afterward, RMS current value of output DC-link capacitor $I_{co\text{-}rms}$, which is critical to deciding the number of paralleled capacitors, is obtained. $I_{co\text{-}rms}$ is calculated in equation 4.28, and calculated values are given in Table 4.33. Another crucial parameter is the voltage rating of the selected capacitor. The voltage rating is selected as 50 V capacitor since the maximum voltage value is 14V at the connected power rail. The amount of output voltage ripple ΔV_o is

decided as 2% of output voltage. As a result of calculation equation 4.29 [43], the total output capacitance value C_o is selected as 90 µF. This capacitance value is achieved with paralleled nine pieces 10 µF capacitors, which are MCJCU32MLB7106KPPDT1 from Taiyo Yuden.

$$\Delta I_o = 2 \cdot \frac{V_o \cdot \left(0.5 - D_{eff}\right) \cdot 10^{-5}}{L_{o1}} \tag{4.27}$$

Table 4.32 : Output load current ripple.

Operating Conditions	ΔI_o (A)
V_{in}:240 V, V_o:14 V, I_o:214 A	9.24
V_{in}:475 V, V_o:14 V, I_o:214 A	32.49
V_{in}:475 V, V_o:10.9 V, I_o:275 A	29.22
V_{in}:240 V, V_o:10.9 V, I_o:275 A	14.95
C_o (selected)	90

$$I_{Co-rms} = \sqrt{\frac{1}{12} \cdot \Delta I_o^2} \tag{4.28}$$

Table 4.33 : RMS current of output capacitor.

Operating Conditions	$I_{Co\text{-}rms}$ (A)
V_{in}:240 V, V_o:14 V, I_o:214 A	2.66
V_{in}:475 V, V_o:14 V, I_o:214 A	9.38
V_{in}:475 V, V_o:10.9 V, I_o:275 A	8.43
V_{in}:240 V, V_o:10.9 V, I_o:275 A	4.31

$$C_o = \frac{V_o \cdot \left(1 - 2 \cdot D_{eff}\right) \cdot T^2}{16 \cdot L_{o1} \cdot \Delta V_o} \tag{4.29}$$

Table 4.34 : Total output capacitance value.

Operating Conditions	C_o (µF)
V_{in}:240 V, V_o:14 V, I_o:214 A	20.62
V_{in}:475 V, V_o:14 V, I_o:214 A	72.52
V_{in}:475 V, V_o:10.9 V, I_o:275 A	83.76
V_{in}:240 V, V_o:10.9 V, I_o:275 A	42.85
C_o (selected)	90

Output voltage ripple is recalculated regarding the selected output DC-link capacitor value, which is 90 µF for each operating point as voltage value in Table 4.35.

Table 4.35 : Output voltage ripple.

Operating Conditions	ΔV_o (V)
V_{in}:240 V, V_o:14 V, I_o:214 A	0.064
V_{in}:475 V, V_o:14 V, I_o:214 A	0.226
V_{in}:475 V, V_o:10.9 V, I_o:275 A	0.203
V_{in}:240 V, V_o:10.9 V, I_o:275 A	0.104

4.1.6 Calculation of ZVS condition

PSFB converter has limitation to achieve ZVS since insufficient energy until converter reaches the suitable operating condition. This situation is solved by using a clamping diode and shim inductor in this study. Equation 4.30 has to be verified to achieve the ZVS condition [43].

$$Inductive\ Energy\ E_L \geq Capacitive\ Energy\ E_C \tag{4.30}$$

Inductive energy depends on the switching legs, which are lagging and leading. Their inductive energy is calculated as in equation 4.31 and equation 4.32, respectively [43]. S_1 and S_2, which are lagging leg switches, and S_3 and S_4, which are leading leg switches. Capacitive energy is calculated by equation 4.33 [43]. C_{TR} could be neglected because of the explained reason in the calculation of deadtime. Circulating current over clamping diode on lagging leg switches has to be considered. $I_{clampd,min}$ and $I_{clampd,max}$ are the minimum and maximum current of the clamping diode during the freewheeling period correspondingly. $I_{mag,peak}$ is the maximum magnetizing current. $I_{Lo1,min}$ and $I_{Lo1,max}$ are the minimum and maximum current of the output inductor respectively.

$$\begin{aligned} E_{L-lagging} &= 0.5 \cdot L_{lk} \cdot \left(I_{mag,pk} + I_{Lo1,min} \cdot \frac{N_{sec}}{N_{pri}} \right)^2 \\ &+ 0.5 \cdot L_{shim} \cdot \left(I_{clampd,min} + I_{mag,pk} + I_{Lo1,min} \cdot \frac{N_{sec}}{N_{pri}} \right)^2 \end{aligned} \tag{4.31}$$

$$\begin{aligned} E_{L-leading} &= 0.5 \cdot L_{mag} \cdot {I_{mag,pk}}^2 + 0.5 \cdot L_{o1} \cdot \left(\frac{N_{pri}}{N_{sec}} \right)^2 \\ &\cdot \left(I_{Lo1,max} \cdot \frac{N_{sec}}{N_{pri}} \right)^2 \\ &+ 0.5 \cdot L_{lk} \cdot \left(I_{mag,pk} + I_{Lo1,max} \cdot \frac{N_{sec}}{N_{pri}} \right)^2 \\ &+0.5 \cdot L_{shim} \cdot \left(I_{clampd,max} + I_{mag,pk} + I_{Lo1,max} \cdot \frac{N_{sec}}{N_{pri}} \right)^2 \end{aligned} \tag{4.32}$$

$$E_c = 0.5 \cdot (2 \cdot C_{pri-coss(er)} + C_{TR}) \cdot V_{in}^2 \quad (4.33)$$

4.2 Design and Calculations of Magnetic Component of PSFB with CDR Converter

Magnetics are one of the critical components that directly affect the converter efficiency, volume, and weight. Owing to these critical roles, calculating the parameters and design are crucial. Detailed calculations that belong to the planar transformer, shim inductor, and output inductor are given in this chapter. Information on manufactured magnetics is shared besides the calculations.

4.2.1 Calculation and design of planar transformer

The planar transformer is implemented in this PSFB-CDR converter since several advantages. A lower profile, lighter weight, flatter transformer is a better option for mounting the PCBs. High efficiency and power density are also important. Planar transformer is prominent in terms of all these features. Repeatability of performance, electrical and magnetic specifications is also another outstanding characteristic of planar transformers.

The main difference between traditional and planar transformers (PT) is core geometry and winding structure. PT has flat copper lead frames and flat copper spirals instead of the wire wound winding structure of traditional transformers. Flat copper provides the operation with high current and high frequency. In addition, flat copper as winding helps to increase the utilization factor up to 60%. Furthermore, PT mostly has lower-profile magnetic cores, which are E, PQ or RM cores. The core of a traditional transformer is more like a cube; however, the core surface of PT is wider. This provides to have better thermal performance since heat is dissipated over the surface area of the core.

Another advantage of PT over a traditional one is the implementation to PCB. The transformer can be dislocated due to its heavy weight and bulk structure when shock and vibration happen. However, PT is more sensitive to break under mechanical and thermal stress by virtue of its thinner structure.

Manufacturability of the transformer is essential. PT has eligibility in terms of manufacturability, since PT can be assembled automatically. This eliminates the

variation between manufactured transformers and increases reliability. It is crucial to have the same specification for resonant converters. Less leakage inductance is better for a PSFB converter. PT ensures the minimization of the leakage inductance with interleaving structure between primary and secondary windings [45, 46].

It is critical to design the transformer properly, which is one of the main components of the converter. There is dimension limitation in terms of width, length, and height, since there is limited space in the designed board. According to dimension limitation, suitable cores are evaluated, and calculations which are given below are repeated to select the best proper core. As a result of several iterations, the transformer core is selected from Ferroxcube 14.8/32-3C96. Calculations that are used to design planar transformer are shared step by step.

Skin dept (Ɛ) is an important parameter to size the conductor. This value is calculated regarding to selected switching frequency f_{sw}, which is 100kHz in equation 4.34. Relative permeability μ_r is 0.999994 for copper, permeability constant μ_0 is $4\pi10^{-7}$ H/m and resistivity of the material ρ is $1.72x10^{-8}$ Ωm for copper. Conductors thickness for primary and secondary are selected as two times Ɛ, which is 0.418 mm, to prevent the skin effect issue during high switching frequency operation.

$$\varepsilon = \sqrt{\frac{\rho}{\pi \cdot \mu_r \cdot \mu_0 \cdot f_{sw}}} \tag{4.34}$$

The conductors' width is decided as 8 mm according to the available core window area width. Conductor cross-sections A_{wp} and A_{ws} are calculated as 3.344 mm^2.

Current densities of conductors for both primary J_{pri} and secondary side J_{sec} are calculated as equation 4.35 and equation 4.36.

$$J_{pri} = \frac{I_{TR-pri,rms}}{A_{wp}} \tag{4.35}$$

$$J_{sec} = \frac{I_{TR-sec,rms}}{A_{ws}} \tag{4.36}$$

Primary and secondary winding can be paralleled to optimize the current density value. In this transformer design the primary side winding has two parallel windings, and the secondary side has six parallel windings. As a result of the existing planar transformer, which has nearly the same power rating and current values, the current density for both windings is selected. Moreover, selected current density values are evaluated with the

manufacturer regarding producibility and thermal issues. The current density of primary winding for maximum current is obtained as 2.936 A/mm^2. The same parameter is obtained as 7.82 A/mm^2 for the secondary winding.

The number of turns for primary N_{pri} is calculated as in equation 4.37. Saturation flux density B_{sat} of the selected core is 340 mT. Thus the maximum flux density B_m is decided as 200 mT. The effective area A_e of the selected core is 201 mm^2.

$$N_{pri} = \frac{V_{in} \cdot D_{eff}}{2 \cdot B_m \cdot A_e \cdot f_{sw}} \tag{4.37}$$

The result of the calculation is 12.45 turns; this value is rounded up to 14 as turns number of primary winding. Turns number of secondary winding N_{sec} has to be 2.

Utilization factor K_u has to be reasonable and applicable. K_u is calculated in as equation 4.38 in regard to selected conductors cross-section, number of paralleled conductor NPC_{pri}, NPC_{sec} and turns number. K_u is obtained obtained as 0.69.

$$K_u \cdot W_a = N_{pri} \cdot NPC_{pri} \cdot A_{wp} + N_{sec} \cdot NPC_{sec} \cdot A_{ws} \tag{4.38}$$

Area product A_p is another critical parameter to select a suitable magnetic core. The power handling capability of the core is associated with A_p. W_a is the window area of the core, which is 194.832 mm^2. A_e is an effective magnetic cross-section area of the core, which is 201 mm^2. A_p value of the core is calculated as in equation 4.39. Required A_p value is also calculated in equation 4.40 regarding to converter. V_{pri} is the voltage at the primary side of transformer, and V_{sec} is the voltage at the secondary side of the transformer. K_f is the waveform factor, and its value is 4 for square of the waveform. The results of equation 4.39 and equation 4.40 are 3.917 cm^4 and 3.67 cm^4, respectively.

$$A_p = A_e \cdot W_a \tag{4.39}$$

$$A_p = \frac{V_{pri} \cdot 10^4}{K_f \cdot K_u \cdot B_{sat} \cdot f_{sw}} \cdot \frac{I_{TR-pri,rms}}{J_{pri}} + \frac{V_{sec} \cdot 10^4}{K_f \cdot K_u \cdot B_{sat} \cdot f_{sw}} \cdot \frac{I_{TR-sec,rms}}{J_{sec}} \tag{4.40}$$

Resistance of winding for both primary R_{pri} and secondary R_{sec} side is calculated as in equation 4.41 and equation 4.42, respectively. Windings material is copper. The resistivity of copper ρ is 1.72x10^{-8} Ωm as mentioned before. The mean length per

turn is 75.4 mm. l_{pri} is the length of each primary winding and l_{sec} is the length of each secondary winding.

$$R_{pri} = \frac{\rho \cdot l_{pri}}{A_{wp}} \tag{4.41}$$

$$R_{sec} = \frac{\rho \cdot l_{sec}}{A_{ws}} \tag{4.42}$$

R_{pri} and R_{sec} are obtained as 5.42 mΩ and 0.78 mΩ, respectively. Since there are two parallel primary winding and six parallel secondary winding, the equivalent R_{pri} is 2.71 mΩ, and the equivalent R_{sec} is 0.13 mΩ.

Copper losses of primary side $P_{con\text{-}pri}$ and secondary side $P_{con\text{-}sec}$ are calculated in equation 4.43 and equation 4.44, respectively. $R_{pri\text{-}eq}$ is the equivalent value of R_{pri}, and $R_{pri\text{-}sec}$ is the equivalent value of R_{sec}. Maximum $P_{con\text{-}pri}$ and $P_{con\text{-}sec}$ are obtained as 1.05 W and 3.2 W, respectively.

$$P_{con-pri} = I_{TR-pri,rms}^2 \cdot R_{pri-eq} \tag{4.43}$$

$$P_{con-sec} = I_{TR-sec,rms}^2 \cdot R_{sec-eq} \tag{4.44}$$

Core loss P_{core} is calculated in equation 4.45 and obtained as 6.624 W. V_e is the effective core volume, which is 18.4 cm^3. Temperature (Temp) is taken as 100 °C.

$$P_{core} = \left(\frac{(0.00018 \cdot Temp^2 - 0.0366 \cdot Temp + 2.827)}{10^6} \cdot 0.0827 \cdot (f_{sw})^{1.72} \cdot (B_m)^{2.80} \right) \cdot V_e \tag{4.45}$$

L_{mag} of the transformer is calculated in equation 4.46 and obtained as 1.078 mH. A_L value of the selected core is 5500 nH/N^2.

$$L_{mag} = A_L \cdot N_{pri} \tag{4.46}$$

The leakage inductance of transformer L_{lk} depends on winding construction and manufacturer capability. This transformer winding structure, which is optimized by the manufacturer, is shared in Figure 4.2. According to this structure, L_{lk} is 1.8 µH.

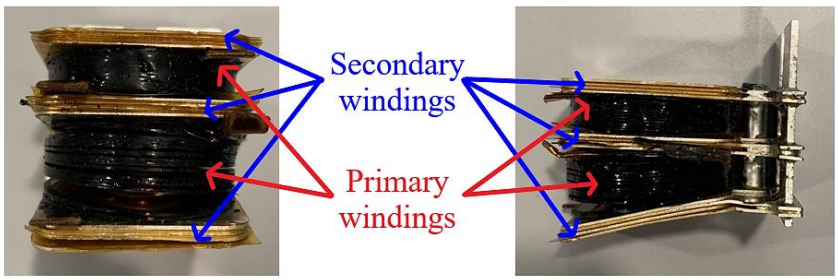

Figure 4.2 : Planar transformer winding structure.

Calculated windings size and selected core information are shared with the manufacturer. The manufactured transformer is given in Figure 4.3. Primary and secondary side winding are also shared in Figure 4.4.

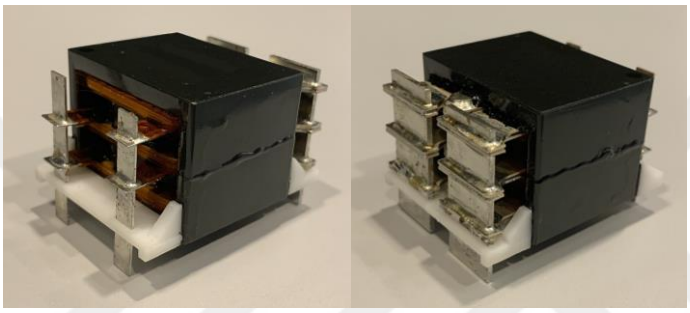

Figure 4.3 : Manufactured planar transformer.

Figure 4.4 : Windings of planar transformer.

The primary side winding thickness is configured as 0.4 mm by the manufacturer. The secondary side winding thickness is also configured as 0.5 mm because of the high current at the secondary side. Primary side and secondary side resistance are measured as 3.7 mΩ and 0.2 mΩ, respectively. L_{mag} is measured as 1.08 mH. L_{lk} is measured as

1.8 µH. The overall dimension of the transformer is 40.64x52.8x29.6 mm as width x length x height.

4.2.2 Calculation and design of shim inductor

The shim inductor is an additional inductor to the leakage inductor of the transformer for extending the ZVS range. It is important to implement and size this inductor to converter, since there is limited space in the designed board. According to size limitation and several calculations iterations, the shim inductor core is selected from TDK EQ 20/6.3/14-N87.

The winding diameter is selected as 2 mm and consists of 260 pieces paralleled by a 0.1 mm litz wire. Since, this winding is common in the market and provides optimum solution in terms of current carrying capability and winding utilization. Cross-section of winding $A_{w\text{-}shim}$ is calculated as 3.142 mm^2. Moreover, the transformer primary side current and shim inductor current I_{shim} can be considered as same when clamping diode operation is neglected. The current densities of shim inductor J_{shim} is calculated equation 4.47 and obtained as 6.25 A/mm^2.

$$J_{shim} = \frac{I_{shim}}{\mathrm{A}_{w-shim}} \tag{4.47}$$

The number of turns N is calculated as in equation 4.48. Saturation flux density B_{sat} of selected core is 390 mT, thus maximum flux density B_m is decided as 200 mT. ΔI_{shim} is peak to peak value of the shim inductor current which can be considered as same as the primary side of the transformer. Effective permeability µ is 1520. Magnetic path length MPL is 33.2 mm.

$$N = \frac{B_m \cdot MPL}{0.4 \cdot \pi \cdot \frac{\Delta \mathrm{I}_{shim}}{2} \cdot \mu \cdot 10^{-4}} \tag{4.48}$$

N has to be 0.14 which is not applicable according to equation 4.45. If N is one at least, B_m will be 1.37 T. Thus, air gap is needed to the shim inductor. EQ 20/6.3/14-N87 core has several air gapped options as finished product. A suitable and available option is found in the core portfolio when N is three. Used equation to calculate the necessary amount of gap l_g as in equation 4.49. Effective magnetic cross-section A_e is 59.8 mm^2. Target shim inductance value L_{shim} is 1.5 µH. Calculated l_g is 0.45mm.

$$l_g = \frac{0.4 \cdot \pi \cdot N^2 \cdot A_e \cdot 10^{-8}}{L_{shim}} \quad (4.49)$$

Effective permeability changes with adding air gap to the core. New effective permeability μ_{new} is calculated in equation 4.50 and obtained as 70.36.

$$\mu_{new} = \frac{\mu}{1 + \mu \cdot \frac{l_g}{MPL}} \quad (4.50)$$

Moreover, A_L changes with adding air gap to core. New A_L which is $A_{L\text{-}new}$ is calculated as equation 4.51 and obtained as 159.26 nH/N^2. μ_o is permeability of air which is 4 x π x 10^{-7}.

$$\frac{1}{A_{L-new}} = \frac{l_g}{\mu_0 \cdot A_e} + \frac{MPL}{\mu_0 \cdot \mu \cdot A_e} \quad (4.51)$$

Equation 4.52. is used to understand whether the target inductance value is achieved with calculated $A_{L\text{-}new}$ and N. L_{shim} is obtained as 1.44 µH which is slightly less than the target according to calculation.

$$L_{shim} = A_{L-new} \cdot N \quad (4.52)$$

Furthermore, flux density has to be verified with μ_{new} as in equation 4.53. B_m is obtained as 190 mT.

$$B_m = \frac{0.4 \cdot \pi \cdot N \cdot \frac{\Delta l_{shim}}{2} \cdot \mu_{new} \cdot 10^{-4}}{MPL} \quad (4.53)$$

K_u is calculated in as equation 4.54 with consideration of selected conductor cross-section and window area W_a of the selected core. W_a is 21.074 mm^2. K_u is obtained as 0.447.

$$K_u \cdot W_a = N \cdot A_w \quad (4.54)$$

A_p value of the core is calculated as equation 4.55. In addition, the required A_p value is calculated as equation 4.56. Voltage over the shim inductor V_{shim} is 2 V which is retrieved from the simulation. K_f is the waveform factor and its value is 4 for square waveform. Result of equation 4.55 and equation 4.56 are 0.126 cm^4, 0.009 cm^4 respectively.

$$A_p = \mathrm{A}_e \cdot \mathrm{W}_a \tag{4.55}$$

$$A_p = \frac{V_{shim} \cdot I_{shim} \cdot 10^4}{K_f \cdot K_u \cdot B_{sat} \cdot \mathrm{f}_{sw} \cdot J_{shim}} \tag{4.56}$$

The mean length turn (MLT) for each turn is 42.1 mm, total MLT which is indicated as l_{shim} is 126.3 mm for 3 turns. Resistance of winding R_{shim} is calculated as in equation 4.57 and obtained as 0.69 mΩ.

$$R_{shim} = \frac{\rho \cdot \mathrm{l}_{shim}}{\mathrm{A}_w} \tag{4.57}$$

Copper losses of winding $P_{con\text{-}shim}$ is calculated as equation 4.58 and obtained as 0.27 W.

$$P_{con-shim} = \mathrm{I}_{shim}^2 \cdot R_{shim} \tag{4.58}$$

Core loss P_{core} is calculated in equation 4.59 and obtained as 0.57 W. V_e is the effective core volume which is 1500 mm^3.

$$P_{core} = 0.036 \cdot \left(\frac{\mathrm{f}_s}{10^3}\right)^{1.64} \cdot (10 \cdot B_m)^{2.68} \cdot V_e \cdot 10^3 \tag{4.59}$$

Calculated windings size and selected core information are shared with the manufacturer. The manufactured shim inductor is given in Figure 4.5. Overall dimension of the inductor is 20x20x12 mm as width x length x height.

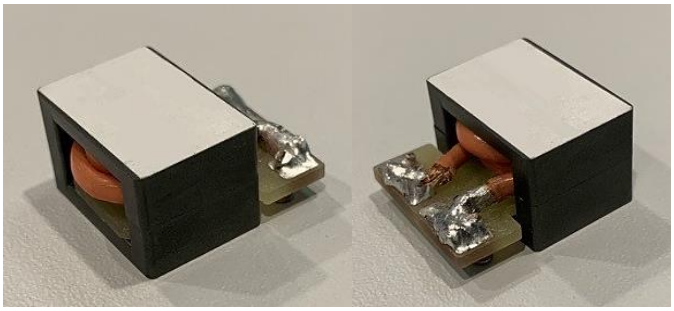

Figure 4.5 : Manufactured shim inductor.

Winding is configured with 260 pieces paralleled 0.1mm litz wire by the manufacturer. Winding resistance is measured as 1.01 mΩ. L_{shim} value is measured as 1.51 µH. Obtained inductance value is slightly higher than calculation because of A_L value tolerance.

4.2.3 Calculation and design of output inductor

The output inductor is one of the main components because of the nature of the PSFB converter. The secondary side is configured as CDR in this design; thus, two output inductors are necessary. Output inductor current is quite high, this is the main challenge of design. The current which flows over the output inductor is DC. Available space on the board is limited, therefore core and winding sizing have to be evaluated carefully. High current density and copper losses are expected, this means that cooling of the designed board comes into prominence.

As a result of several calculations iterations, the output inductor core is selected from Micrometals EQHF-265190124- 060.

The cross-section of winding $A_{w\text{-}Lout}$ is sized as 9 mm^2. According to this, the current densities of the output inductor J_{Lout} is calculated as equation 4.60 and obtained as 15.29 A/mm^2.

$$J_{Lout} = \frac{I_{Lo,RMS}}{A_{w-Lout}} \tag{4.60}$$

The required number of turns N depends on the A_L value to achieve the targeted inductance value L_{out} which is 2.5 µH. A_L changes with ampere x turns value which can be seen in Figure 4.6. Detailed information could be found appendix A. After a few iterations, targeted L_{out} is obtained when N is six. Ampere x turns is equal to 825 and A_L is 70 nH/N^2.

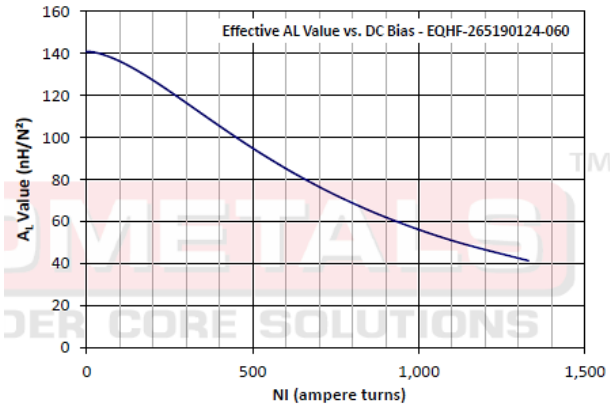

Figure 4.6 : Relation between A_L and DC current.

DC magnetizing force H is calculated as in equation 4.61 and obtained as 162.24 Oe. MPL is 6.39 cm. $I_{Lo,RMS}$ is calculated in Table 4.27.

$$H = \frac{0.4 \cdot \pi \cdot N \cdot I_{Lo,RMS}}{MPL} \tag{4.61}$$

Initial permeability μ which is 60, is decreased with respect to H, since the selected core is powder core. Equation which indicates the amount of decrease of μ in 4.62. The result of the calculation is 47.34% which means that new initial permeability μ_{new} is 47.34% of the μ. Regarding this result, μ_{new} is obtained as 28.4.

$$\mu\% = \frac{1}{0.01 + 2.64 \cdot 10^{-6} \cdot H^{1.64}} \tag{4.62}$$

AC flux density B_{ac} which is generated by ripple current over DC current, is calculated as equation 4.63. ΔI_{Lo} is calculated in Table 4.24. B_{ac} is obtained as 74 mT.

$$B_{ac} = \frac{0.4 \cdot \pi \cdot N \cdot \frac{\Delta I_{Lo}}{2} \cdot \mu_{new} \cdot 10^{-4}}{MPL} \tag{4.63}$$

DC flux density B_{dc} which is generated by DC current, is calculated as equation 4.64. B_{dc} is obtained as 461 mT.

$$B_{dc} = \frac{0.4 \cdot \pi \cdot N \cdot I_{Lo,RMS} \cdot \mu_{new} \cdot 10^{-4}}{MPL} \tag{4.64}$$

K_u is calculated as equation 4.65 and obtained as 0.607. W_a of the selected core is 88.9 mm^2.

$$K_u \cdot W_a = N \cdot A_w \tag{4.65}$$

A_p value of the core and the required A_p value are calculated as equation 4.66 and equation 4.67 respectively. A_e is 1.20 cm^2. $I_{Lo,max}$ is given in Table 4.28. B_m is the summation of B_{ac} and B_{dc}. Results of calculations are 1.07 cm^4, 1.07 cm^4 respectively. These values show that the inductor design is the limit during worst-case operation.

$$A_p = A_e \cdot W_a \tag{4.66}$$

$$A_p = \frac{L_{out} \cdot I_{Lo,max} \cdot I_{Lo,RMS} \cdot 10^4}{K_u \cdot B_m \cdot J_{Lout}} \tag{4.67}$$

MLT for each turn is 5.39 cm. Total MLT which is indicated as l_{Lout} is 32.34 cm for six turns. Resistance of winding R_{Lout} is calculated as in equation 4.68 and obtained as 0.62 mΩ.

$$R_{Lout} = \frac{\rho \cdot l_{Lout}}{A_w} \tag{4.68}$$

Copper losses of winding $P_{con\text{-}Lout}$ is calculated as equation 4.69 and obtained as 11.7 W.

$$P_{con-Lout} = I_{Lout}^2 \cdot R_{Lout} \tag{4.69}$$

Core loss P_{core} is calculated in equation 4.70 and obtained as 4.39 W. V_e is 7.66 cm^3. Unit of B_{ac} is gauss in this equation.

$$P_{core} = \left(\frac{f_{sw}}{\frac{8.19 \cdot 10^8}{{B_{ac}}^3} + \frac{7.4 \cdot 10^8}{{B_{ac}}^{2.3}} + \frac{2.97 \cdot 10^6}{{B_{ac}}^{1.65}} + 3.59 \cdot 10^{-14} \cdot {B_{ac}}^2 \cdot {f_{sw}}^2} \right) \cdot V_e \tag{4.70}$$

Calculated windings size and selected core information are shared with the manufacturer. The manufactured output inductor is given in Figure 4.7. Overall dimension of the inductor is 26.5x25x22.5 mm as width x length x height.

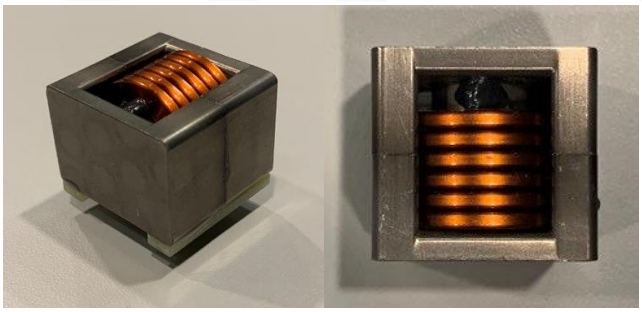

Figure 4.7 : Manufactured output inductor.

Winding is configured with 4.5x2 mm copper conductor by the manufacturer. Winding resistance is measured as 0.6 mΩ. L_{out} value is measured as 2.56 µH.

4.3 Control Methods of PSFB with CDR Converter

Control of the power converters is as important as designing and selecting electronic components. There are two main control methods which are voltage mode and control mode control basically. The designer selects the proper control method according to design requirements and converter type.

Voltage mode control measures the output voltage that would like to be controlled and compares this measurement with the reference voltage value. The error signal is generated as a result of this comparison. The voltage mode controller generates a control reference signal from the error signal. Then, control signal is obtained with the comparison between this control reference signal and the generated sawtooth signal.

Voltage mode control has a single control loop. Thus design, analysis, and implementation are simpler than the current mode control method. In additional, response time is slower than the current mode control method. The block diagram of voltage mode control is shown in Figure 4.8.

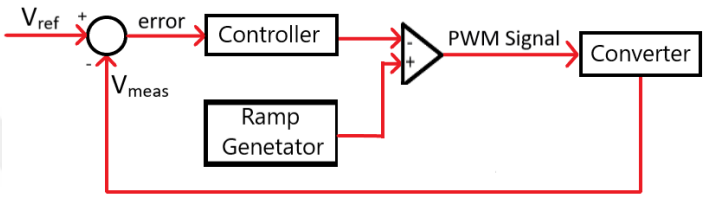

Figure 4.8 : The block diagram of voltage mode control.

Another control method is current mode control. On the contrary of voltage mode control, the duty cycle is controlled with measured current. There are two control loops, which are voltage mode control loop as the outer loop and the current mode control loop as the inner loop. Current mode control is faster than voltage mode control. This means that the outer loop bandwidth is smaller than the inner loop bandwidth. With the help of a higher bandwidth of peak current mode control, the bandwidth of the voltage loop can be increased to use bandwidth efficiently and have a faster controller. However, the controller is more sensitive to noise at that condition. This problem is solved by adding an additional digital filter and averaging the monitored signals in this thesis.

Moreover, current mode control is divided into two, one of them is average current mode control and the other one is the peak current mode control. Peak current mode control monitors the peak current value of the inductor, and average current control mode monitors the average value of the controlled current [47]. Block diagrams of the average current mode control and the peak current mode (PCMC) are shown in Figure 4.9 and Figure 4.10, respectively.

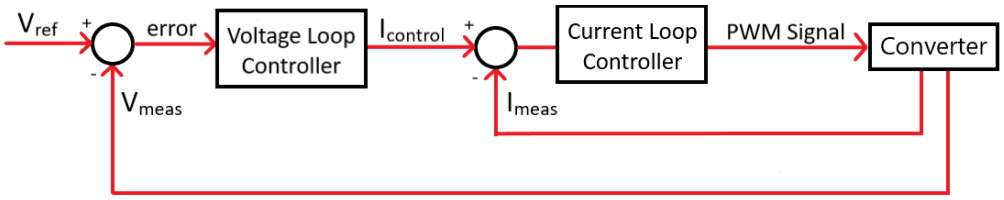

Figure 4.9 : The block diagram of average current mode control.

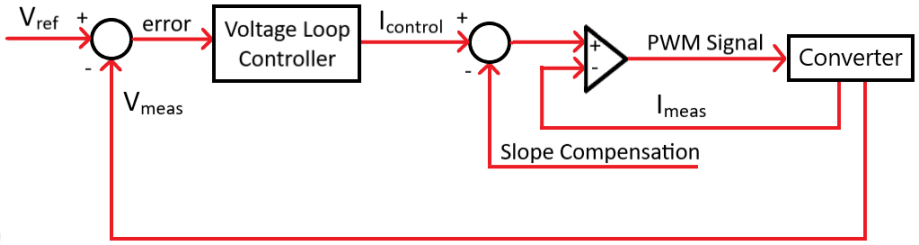

Figure 4.10 : The block diagram of peak current mode control.

In this thesis, PCMC is selected as the control method. First of all, peak current mode control can provide cycle-by-cycle current protection, which is a very useful feature. However, sub-harmonic oscillation and instability occur when the duty cycle exceeds 50%. Thus, slope compensation has to be implemented to prevent problem. Slope compensation can also be added if the duty cycle is less than 50% to ensure better noise immunity [47].

One of the main advantages of PSFB converters is the operation in the 1st and 3rd quadrants of the BH curve [48]. An important point is that the transformer has to achieve a volt-second balanced operation to avoid core saturation and current runaway [49]. There are several reasons for the current offset in the transformer, which causes core instability. Nonequal conduction resistance between power switches, gate drivers, and PCB design are the main reasons [48].

The conventional solution to this imbalance problem is adding a blocking capacitor to eliminate the DC component of the current. However, this solution is unreasonable for a high-power converter, since it is hard to find a capacitor that can satisfy the required rating. Furthermore, this kind of capacitor brings additional cost and lower efficiency [48, 49]. As a result of the pros and cons evaluation, PCMC control is a better option to solve the current balancing problem.

4.3.1 PCMC implementation

PCMC is digitally implemented to PSFB with a CDR converter. It is essential to generate precise timed PWM waveforms. TMS320F280048 is selected from the C2000 family of Texas Instruments. The selected microcontroller has a 32-bit central processing unit (CPU), 256 KB flash memory, and several peripherals on the chip, which are an analog comparator (CMPSS), digital-to-analog converter (DAC), PWM modules, 12-bit analog-to-digital converter (ADC) basically.

Sensed current from the primary side, which is HV current, by a current transformer and output voltage by voltage divider resistor is connected to the ADC pins of the microcontroller. The sensed output voltage value is compared with the set value and the output of this comparison is used in current mode controller. The generated error signal is combined with the slope compensation signal, which is generated in the microcontroller. Slope value has to ensure stability. If the slope is high, the duty cycle will be limited; if the slope is low, sub-harmonic oscillation might occur. The produced control reference signal with slope compensation is connected to the DAC module within the microcontroller. The newly formed analog signal from the digital signal is compared with the sensed primary side current in the CMPSS module. Then, a reset signal is generated when the sensed current signal reaches the control reference signal. After determining deadtime, a set signal is generated for other switches at the same leg. These set and reset signals are processed into the PWM module for PWM generation [50, 51]. The software block diagram for PCMC is given to help visualize and better understand in Figure 4.11.

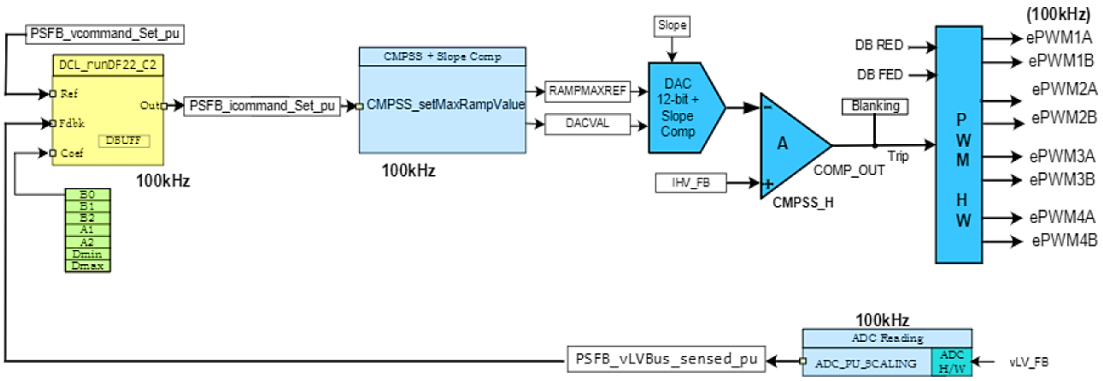

Figure 4.11 : The block diagram of software implementation for PCMC [50].

All these ADC conversions, control loop process, and PWM generation have to be completed within the selected interrupt time, which is 100 kHz in this thesis. Deadtime

is selected as 100 ns. Thus PWM on time is 4.9 µs for each primary side switches. The power transfer interval is ended by leading leg switches. This means that the set and reset signals which are generated by the CMPSS module affect the leading leg switches. PWM of secondary side switches are also generated regarding to primary side switch state. The correlation of all these signals is given in Figure 4.12. Switch names are referred to Figure 3.11.

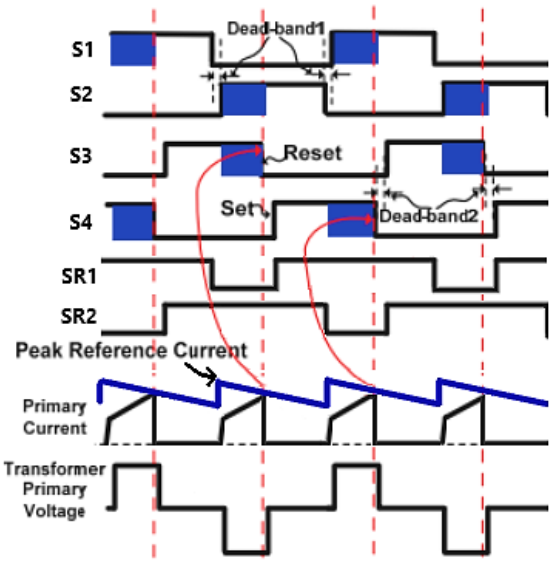

Figure 4.12 : Correlation PMW generation for PCMC.

The main advantage of PCMC is that it provides flux balancing. Therefore, the important point is ensuring the same peak reference current for both halves of the switching cycle during controller implementation.

4.3.2 Small signal analysis and transfer function

PSFB with CDR converter has ZVS feature, since high switching frequency operation is suitable. Reliable and high-frequency operation requires a suitable controller. It is important to properly obtain a small-signal model to observe open-loop and closed-loop behavior.

There are some challenges to model PSFB with a CDR converter for PCMC. One of them is having the CDR stage, since there are two current loops at the seconder side. This causes the cross-coupling issue for PCMC. Another difficulty is sensing the primary side current two times of switching frequency. This requirement makes it mandatory to use a higher bandwidth current sensor. In this design, the current transformer is selected with a high bandwidth feature [52].

It is important to evaluate the operating states of the converter when a linearized small-signal model is obtained. The open loop transfer function is derived from this obtained model. The small-signal equivalent circuit model is given in Figure 4.13. Power switches are modeled as a three-port network model. R_{deq} is equivalent resistance due to the duty cycle loss operation and the conduction loss of the output inductors. R_{deq} depends on the transformer turns ratio (N_s/N_p), leakage inductance and shim inductance, if exists, L_{lk}, switching frequency f_{sw}, and the output inductor resistance R_L. L_{eq} is the half of the inductance of the output inductor, C is the capacitance of the output capacitor, R_c is the ESR of the output capacitor, and R is the resistance of the load.

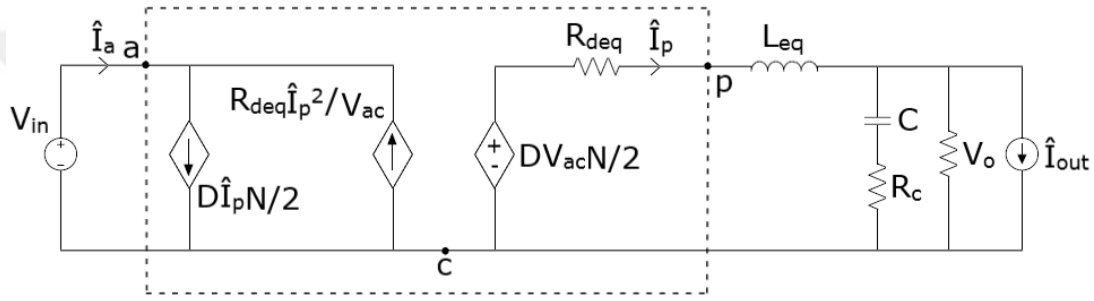

Figure 4.13 : The small-signal equivalent circuit model of PSFB with CDR converter.

$$R_{deq} = 2 \cdot N^2 \cdot L_{lk} \cdot f_{sw} + \frac{R_L}{2} \tag{4.71}$$

The small-signal model of the CDR side for PCMC has to be considered as two paralleled buck converters. Inductors current peak values are controlled separately by the controller. A small-signal model of PSFB with CDR converter is given in Figure 4.14. D_1 and D_2 are suppositional duty ratios of the parallel connected buck converters.

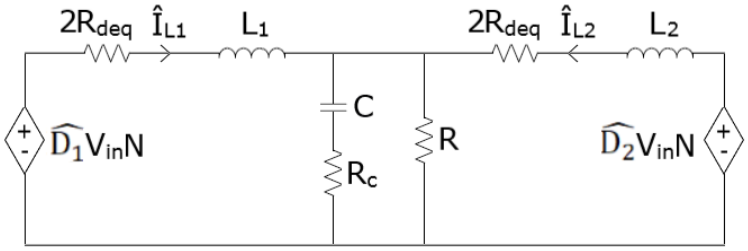

Figure 4.14 : The small-signal equivalent circuit model of PSFB with CDR converter for PCMC.

According to obtained small-signal models of PSFB with CDR converter, open-loop transfer functions have been derived. The equivalent impedance (Z_{eq}) is calculated

with the output DC-link capacitor and the load resistor in equation 4.72. Control to output voltage (G_{vd}), control to output inductor current (G_{id}), line feed-through (G_{vg}), and the output impedance (Z_{out}) transfer functions are derived as in equation 4.73, equation 4.74, equation 4.75, and equation 4.76, respectively.

$$Z_{eq} = \mathrm{R} \parallel \left(R_c + \frac{1}{sC}\right) = \frac{(R \cdot R_C \cdot C)s + R}{(R \cdot C + R_C \cdot C)s + 1} \tag{4.72}$$

$$G_{id}(\mathrm{s}) = \frac{i_L(s)}{D(s)} = \frac{NV_{ac}}{2\left(R_{deq} + L_{eq}s + Z_{eq}\right)} \tag{4.73}$$

$$= \frac{NV_{ac}[(RC + R_cC)s + 1]}{2L_{eq}C(R + R_c)s^2 + 2\left(R_{deq}RC + R_{deq}R_cC + L_{eq} + RR_cC\right)s + 2\left(R + R_{deq}\right)}$$

$$G_{vd}(\mathrm{s}) = \frac{V_o(s)}{D(s)} = \frac{NV_{ac}Z_{eq}}{2\left(R_{deq} + L_{eq}s + Z_{eq}\right)} \tag{4.74}$$

$$= \frac{NV_{ac}(RR_cCs + R)}{2L_{eq}C\left[(R + R_c)s^2 + \left(\frac{R_cR_{deq} + RR_{deq} + RR_c}{L_{eq}} + \frac{1}{C}\right)s + \frac{\left(R + R_{deq}\right)}{L_{eq}C}\right]}$$

$$G_{vg}(\mathrm{s}) = \frac{V_o(s)}{V_{in}(s)} = \frac{ND_{DC}Z_{eq}}{2\left(R_{deq} + L_{eq}s + Z_{eq}\right)} \tag{4.75}$$

$$= \frac{ND_{DC}(RR_cCs + R)}{2L_{eq}C\left[(R + R_c)s^2 + \left(\frac{R_cR_{deq} + RR_{deq} + RR_c}{L_{eq}} + \frac{1}{C}\right)s + \frac{\left(R + R_{deq}\right)}{L_{eq}C}\right]}$$

$$Z_{out}(\mathrm{s}) = \frac{V_o(s)}{I_{out}(s)} = Z_{eq} \parallel \left(L_{eq}s + R_{deq}\right) \tag{4.76}$$

$$= \frac{RR_cCL_{eq}s^2 + \left(R_{deq}RR_cC + RL_{eq}\right)s + RR_{deq}}{L_{eq}C\left[(R + R_c)s^2 + \left(\frac{R_cR_{deq} + RR_{deq} + RR_c}{L_{eq}} + \frac{1}{C}\right)s + \frac{\left(R + R_{deq}\right)}{L_{eq}C}\right]}$$

V_{ac} is considered as equal to V_{in} for G_{vg} calculation. The output current disturbance $\hat{I}_{out}$ is ignored for all transfer function calculations. Equivalent series resistance (ESR) of the output capacitor R_c is neglected, since its value is relatively small when compared with load resistor R. As a result of this ignoration, G_{id}, G_{vd}, G_{vg}, and Z_{out} are

simplified as in equation 4.77, equation 4.78, equation 4.79, and equation 4.80 respectively.

$$G_{id}(s) = \frac{i_L(s)}{D(s)} = \frac{NV_{ac}(RCs+1)}{2L_{eq}CR\left[s^2 + \left(\frac{R_{deq}+R_c}{L_{eq}} + \frac{1}{RC}\right)s + \frac{1}{L_{eq}C}\left(1 + \frac{R_{deq}}{R}\right)\right]} \quad (4.77)$$

$$G_{vd}(s) = \frac{V_o(s)}{D(s)} = \frac{NV_{ac}(R_cCs+1)}{2L_{eq}C\left[s^2 + \left(\frac{R_{deq}+R_c}{L_{eq}} + \frac{1}{RC}\right)s + \frac{1}{L_{eq}C}\left(1 + \frac{R_{deq}}{R}\right)\right]} \quad (4.78)$$

$$G_{vg}(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{ND_{DC}(R_cCs+1)}{2L_{eq}C\left[s^2 + \left(\frac{R_{deq}+R_c}{L_{eq}} + \frac{1}{RC}\right)s + \frac{1}{L_{eq}C}\left(1 + \frac{R_{deq}}{R}\right)\right]} \quad (4.79)$$

$$Z_{out}(s) = \frac{V_o(s)}{I_{out}(s)} = \frac{R_cCL_{eq}s^2 + \left(R_{deq}RR_cC + L_{eq}\right)s + R_{deq}}{L_{eq}C\left[s^2 + \left(\frac{R_{deq}+R_c}{L_{eq}} + \frac{1}{RC}\right)s + \frac{1}{L_{eq}C}\left(1 + \frac{R_{deq}}{R}\right)\right]} \quad (4.80)$$

G_{id} transfer function cannot be used for PCMC, since the two paralleled buck converter structure behavior of CDR. Another additional transfer function, which is the control to output inductor current (G_{iL}), derived from Figure 4.14. According to the small-signal equivalent circuit model in Figure 4.14, the controlled voltage source $D_1V_{in}N$ has an effect on the currents in both output inductors, which are named as L_1 and L_2. Similarly, $D_2V_{in}N$ has the same influence. This means that two transfer functions are derived for each control variables, D_1 and D_2. One of them is named as the forward gain transfer function, which is the ratio between $i_{L1}(s)$ and $D_1(s)$, $i_{L2}(s)$ and $D_2(s)$. Another one is named as the cross-coupled transfer function, which is the ratio between $i_{L1}(s)$ and $D_2(s)$ or $i_{L2}(s)$ and $D_1(s)$. The forward gain and crossed-coupled transfer functions are calculated as in equation 4.81 and equation 4.82, respectively. Re_1 and

Re_2, which are used as parameters in calculations, as in equation 4.83 and equation 4.84.

$$G_{iL11}(s) = \frac{i_{L1}(s)}{D_1(s)} = G_{iL22}(s) = \frac{i_{L2}(s)}{D_2(s)}$$
$$= \frac{NV_{in}\left(LCs^2 + \left(\frac{L}{R} + R_{e2}C\right)s + 1\right)}{2L\left(s + \frac{R_{deq}}{L}\right)\left(\frac{LC}{2}s^2 + \left(\frac{R_{e1}C}{2} + \frac{L}{2R}\right)s + 1\right)} \quad (4.81)$$

$$G_{iL12}(s) = \frac{i_{L1}(s)}{D_2(s)} = G_{iL21}(s) = \frac{i_{L2}(s)}{D_1(s)}$$
$$= \frac{NV_{in}(R_cCs + 1)}{2L\left(s + \frac{R_{deq}}{L}\right)\left(\frac{LC}{2}s^2 + \left(\frac{R_{e1}C}{2} + \frac{L}{2R}\right)s + 1\right)} \quad (4.82)$$

$$R_{e1} = R_{deq} + 2R_c \quad (4.83)$$

$$R_{e2} = R_{deq} + R_c \quad (4.84)$$

Relying on the obtained open-loop transfer functions, G_{vd}, G_{iL11}, G_{iL12}, G_{iL22} and G_{iL21} the closed-loop control model for PCMC of the PSFB with CDR converter is acquired as in Figure 4.15. G_{cs} is the slope compensator, which is essential to ensure stability; R_i and R_v are the current sensor and voltage sensor gains, respectively. K is the microcontroller's PWM-channel comparator gain.

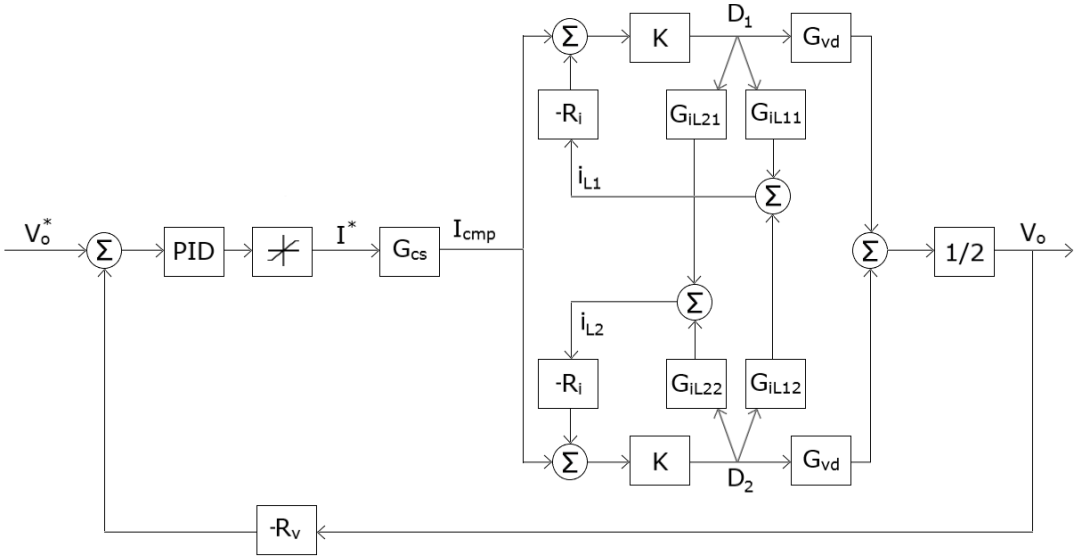

Figure 4.15 : The closed-loop control model for PCMC of the PSFB with CDR converter.

4.3.3 PCMC design for PSFB with CDR converter

According to the calculated transfer function (TF) in the previous section, blocks of TF are implemented to MATLAB/Simulink as given in Figure 4.18. Two different steps as input and scaled output voltage, as the response of step change can be seen in Figure 4.16 and Figure 4.17, respectively.

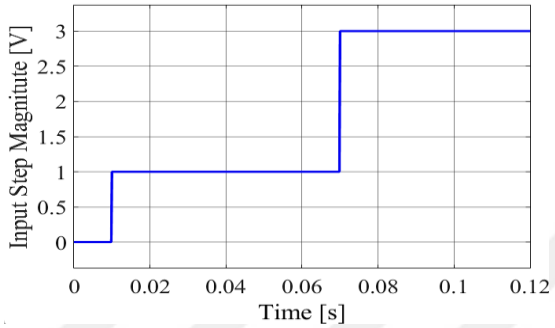

Figure 4.16 : Applied step input signal as reference input.

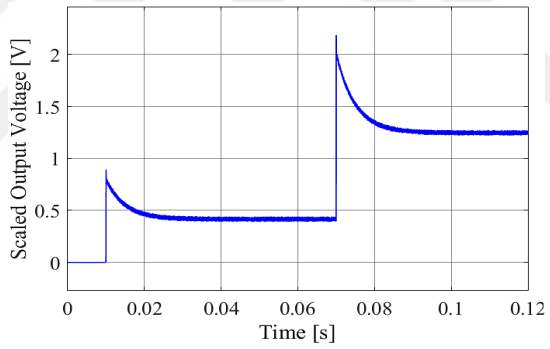

Figure 4.17 : Step response of open loop operation.

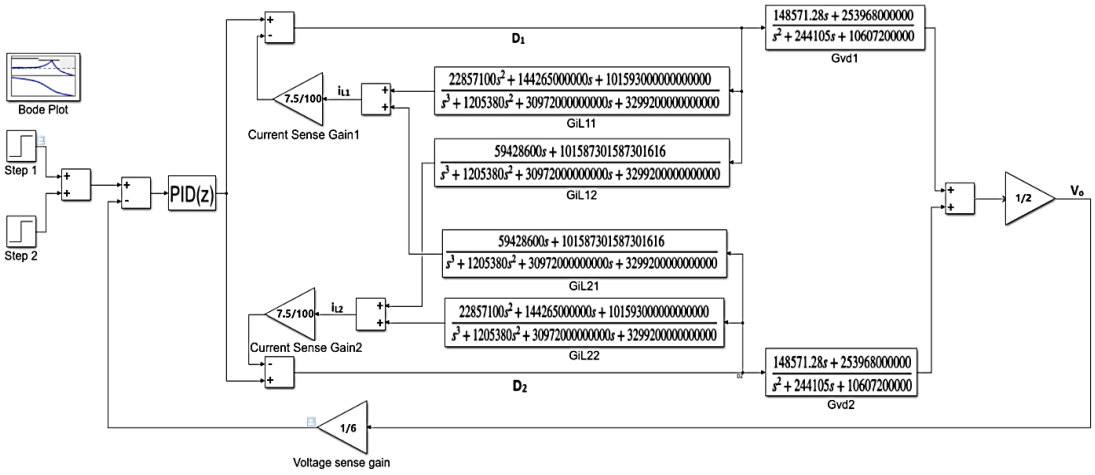

Figure 4.18 : Model of close loop transfer function PSFB with CDR converter in MATLAB/Simulink.

Bode diagram of open loop operation is shown in Figure 4.19.

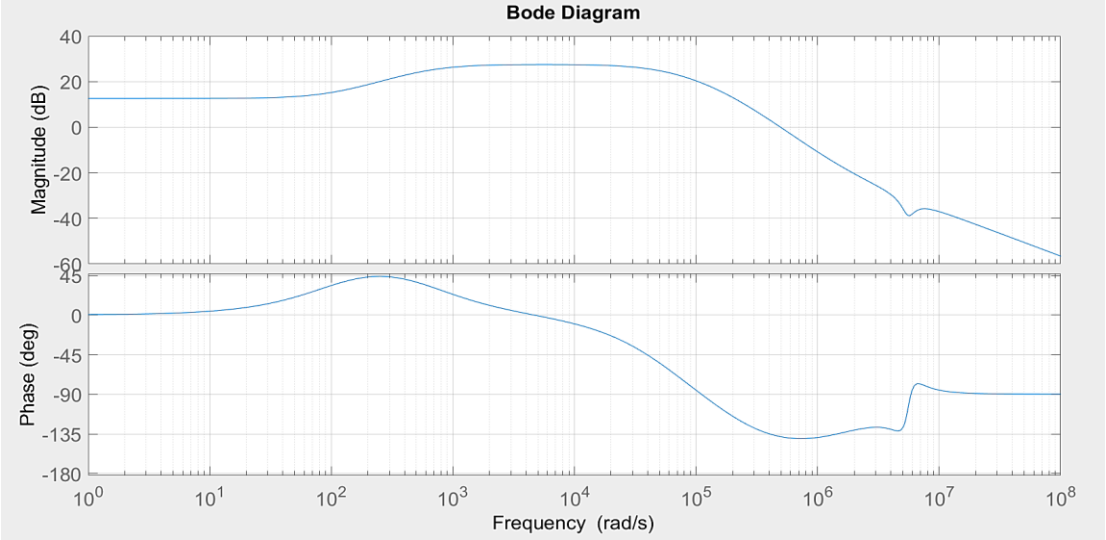

Figure 4.19 : Bode diagram of open loop operation.

Proportional-integral (PI)-type controller is selected to control the converter due to its simple structure, ease of use, and suitable performance [47]. Compensator parameters are found with the help of Simulink's response optimizer tool. Compensator parameters are selected with consideration of settling time and overshoot behavior, which can be observed in the response optimizer tool. As a result, these parameters, which are proportional (K_p) and integral (K_i), are implemented as 0.002856 and 1031.58, respectively. The bode diagram of the close loop operation is shared in Figure 4.20. Phase margin is 60° and the gain margin is 17.7dB.

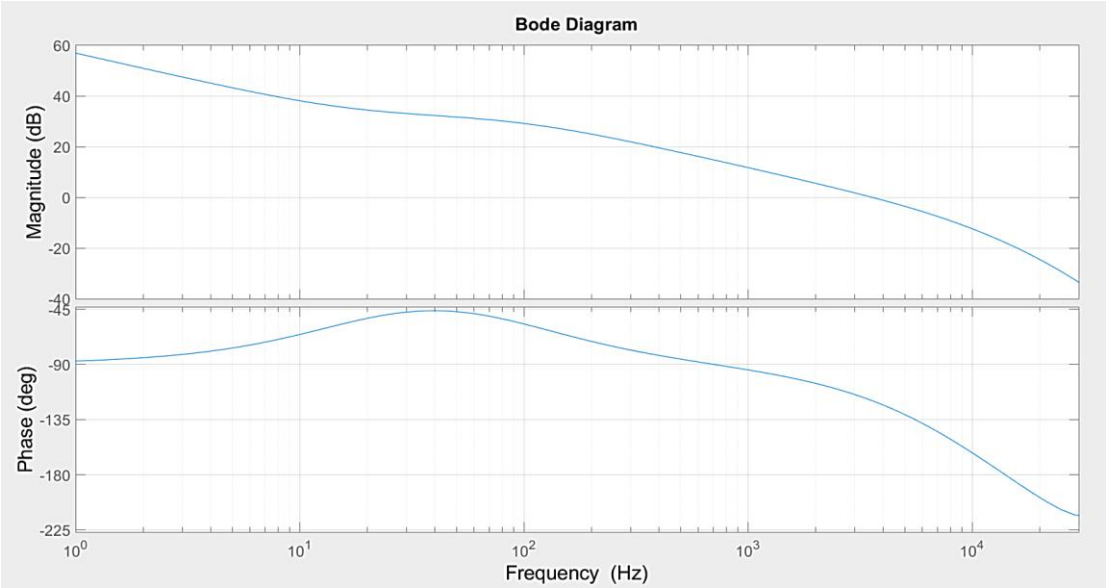

Figure 4.20 : Bode diagram of close loop operation.

The scaled output voltage response regarding step change with the designed controller can be seen in Figure 4.21. The output can able to follow the input step, which is considered as a reference to the output.

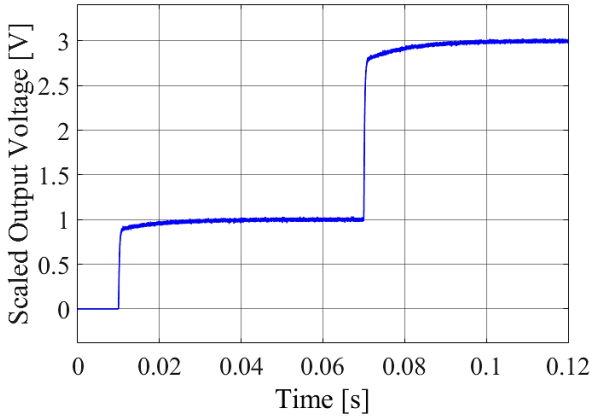

Figure 4.21 : Step response of close loop operation.

The mentioned K_p and K_i values are in the s-domain. The transformation from the s-domain to the z-domain is necessary since the microcontroller is used to control the converter. There are several types of transformation methods, which are Forward Euler, Backward Euler, and Trapezoidal methods (Bilinear or Tustin transformation). The transformation map for each method is given in Table 4.36. T_s is switching period.

Table 4.36 : Transformation map from s-domain to z-domain [53].

Transformation Methods	Transformation s-domain to z-domain
Forward Euler	$s = \frac{z-1}{T_s}$
Backward Euler	$s = \frac{z-1}{T_s \cdot z}$
Trapezoidal/Bilinear/Tustin	$s = \frac{2}{T_s} \cdot \frac{z-1}{z+1}$

The Tustin method is selected in this controller transformation. Regarding the Tustin method transformation, controller transfer function H(z) in the z-domain is obtained.

4.4 Simulation Circuit and Simulation Results

Simulation is an essential step in designing the converter before the implementation. Well-modeled simulation provides accurate information about the converter behavior. Each component has to be modeled as closely as possible to real components to have real-like results. In this chapter, PSFB with CDR converter is simulated with real

component models, which are obtained from the manufacturer in LTspice. Simulation results are observed for different output load currents.

4.4.1 Modelling of PSFB with CDR converter

Detailed design calculations and information on selected components are shared in the previous chapter. In this chapter, a simulation model of the converter is designed with selected component and their calculated values. PSFB with CDR converter simulated in LTspice.

It is important to implement accurate component models to obtain more accurate results. One of the main advantages of LTspice is that it enables the usage of real component models which are generated by the manufacturer. Model of primary and secondary side switches, clamping diodes, input and output DC-link capacitors, transient voltage suppressor (TVS) at the secondary side, and gate drivers are implemented as real models to simulation. Switches models are selected as level 1, which has the transient behavior effect of MOSFET. This is important to observe switching losses, especially [54]. Other selected and manufactured critical magnetic components are modeled according to their datasheets. HV battery is modeled as DC supply; a load of LV battery side is modeled as a resistive load. Simulation is designed as open mode; thus, the duty cycle is controlled manually according to the analytically calculated duty cycle. The simulation diagram, which is generated in LTspice, is seen in Figure 4.22.

Simulation results are given at nominal operating condition for different load current values. Nominal operating conditions in terms of voltage values are that input voltage as 400 V, output voltage as 12 V. Maximum power rating is 3 kW as mentioned in the previous chapter, yet simulation results are shared for different output current ratings.

Both voltage and current waveforms of the transformer, output load, leading and lagging leg switch are given. In addition, current waveforms of shim inductor, output inductors, and clamping diodes are shared. Clamping diode effects are observed in terms of voltage waveforms and efficiency.

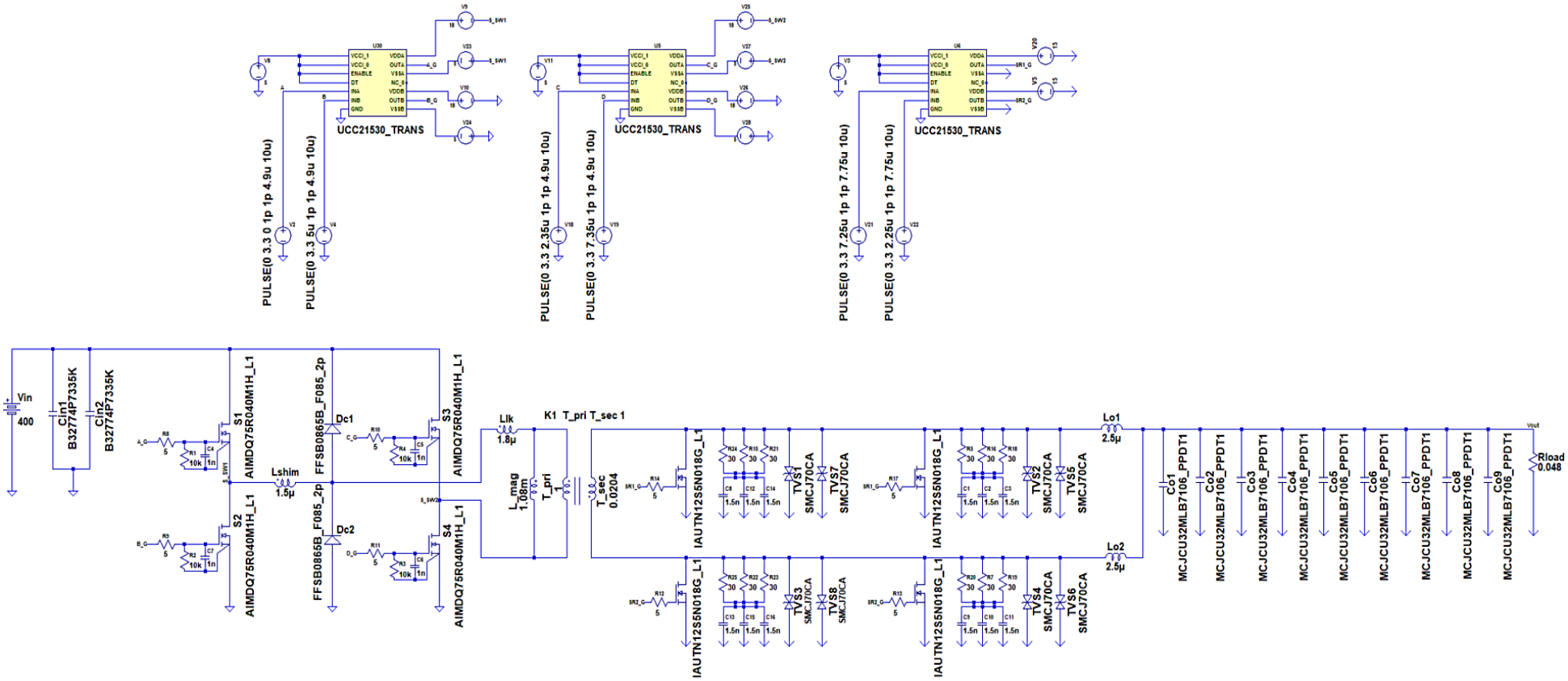

Figure 4.22 : Simulation diagram of PSFB with CDR converter in LTspice**.**

4.4.2 Simulation results at different load

It is important to have information about the behavior, performance, and waveform of the converter with changing loads. Several simulations are given to see and evaluate the performance of the converter at different load conditions. Input voltage is 400 V, and output voltage is 12 V for all simulations. Related waveforms are shared in the following sections.

4.4.2.1 Simulation results at 50 A load current

The simulation results of the operation with a 50 A load have been shared. Transformer voltage and current waveforms for both the primary and secondary sides can be seen in Figure 4.23. It can be seen that the duty cycle loss mode, which is the secondary side voltage is 0 V, however primary side voltage is not. Moreover, this interval can be detected with a change in the primary side current direction. There is an oscillation at primary side voltage during the duty cycle loss time, since resonation between primary side inductance and parasitic capacitor of primary side switches.

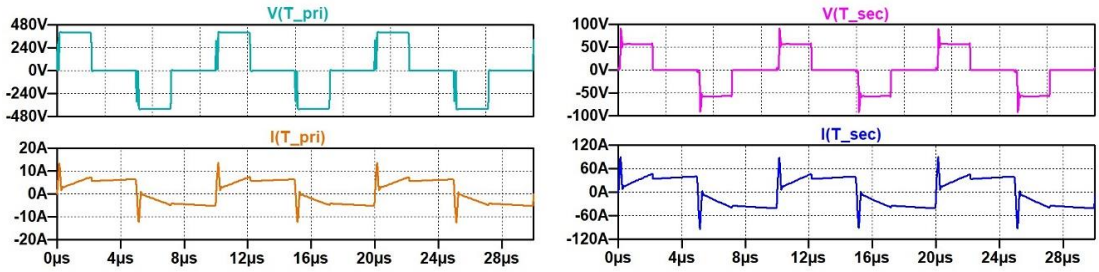

Figure 4.23 : Transformer primary and secondary side voltage V_{T_pri}, V_{T_sec} and current waveforms I_{T_pri}, I_{T_sec} at 50 A load current.

Output inductors current, output load current and voltage waveforms are shown in Figure 4.24.

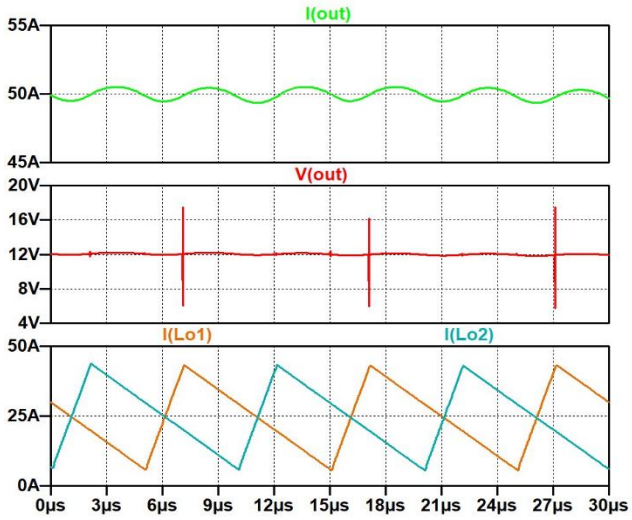

Figure 4.24 : Output load current I_{out} and voltage V_{out}, output inductors current I_{Lo1}, I_{Lo2} at 50 A load current.

Another critical issue is to achieve ZVS condition. The current waveform of clamping diode D_{c1}, voltage and current waveforms of S_1, which is the lagging leg switch, and S_4, which is the leading leg switch, are given in Figure 4.25. Moreover, it can be noticed that the current waveform of leading leg and lagging leg are different from each other because of the clamping diode operation.

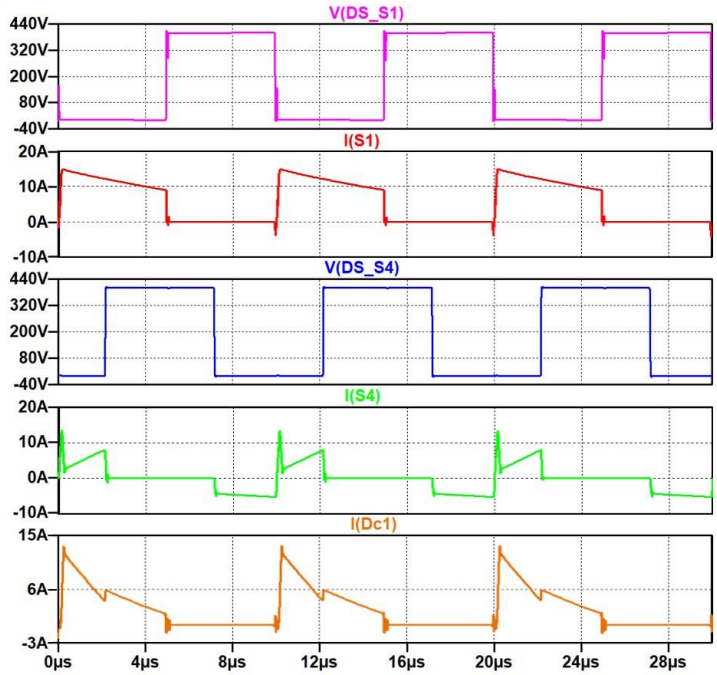

Figure 4.25 : Primary side switch S1 and S4 voltage V_{DS_S1}, V_{DS_S4} and current I_{S1}, I_{S4} waveform; clamping diode D_{c1} current waveform I_{Dc1} at 50 A load current.

Voltage and current waveform which belong to the secondary side switch S_{SR1} shown in Figure 4.26.

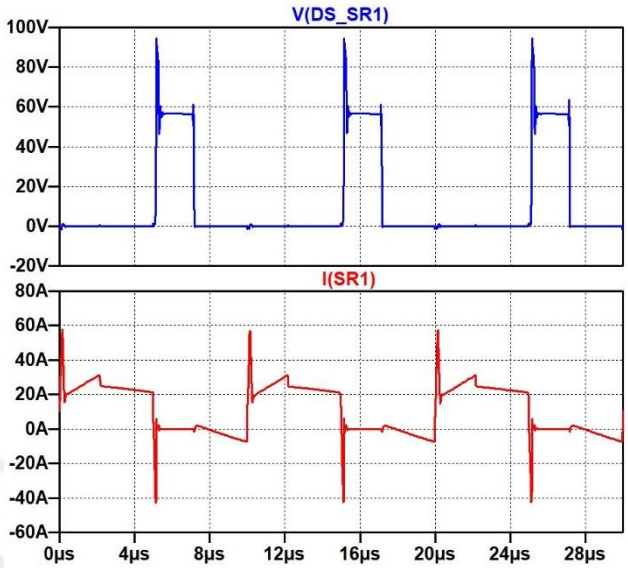

Figure 4.26 : Voltage V_{DS_SR1} and current I_{SR1} waveform of secondary side switch S_{SR1} at 50 A load current.

A zoomed view of waveforms that belong to S_1 and S_4 and their PWM waveforms are also given for better observation of ZVS event in Figure 4.27.

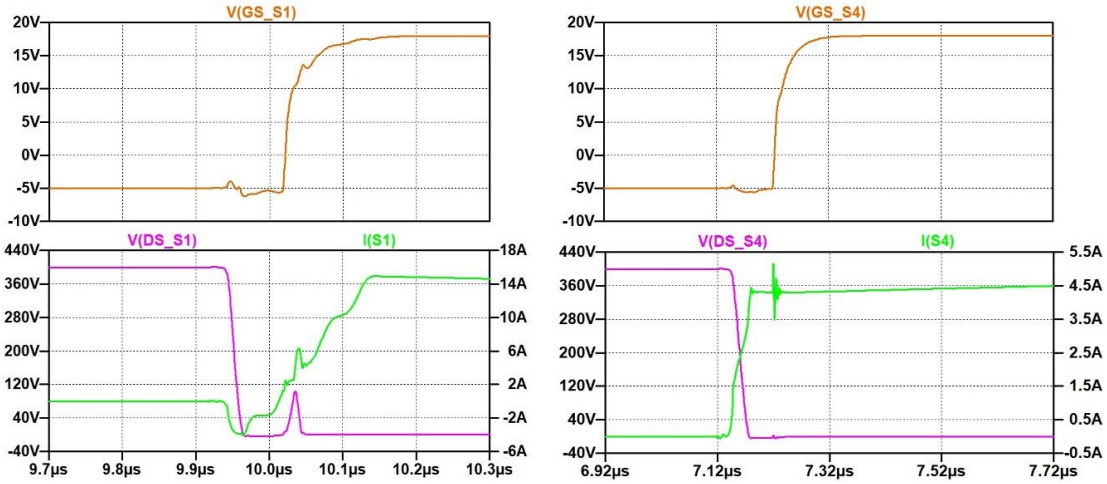

Figure 4.27 : ZVS event of primary side switches S_1 and S_4 at 50 A load current.

It can be seen that ZVS is achieved both leading and lagging leg switch. However, there is a peak at the V_{DS_S1} because of fixed deadtime which is 100 ns. Solution of this issue is to apply adaptive deadtime, which changes regarding to load current.

Efficiency is calculated as 82.56%.

4.4.2.2 Simulation results at 100 A load current

The simulation results of the operation with a 100 A load have been shared. Transformer voltage and current waveforms for both the primary and secondary sides can be seen in Figure 4.28. Duty cycle loss mode can be observed when the primary side current direction changes.

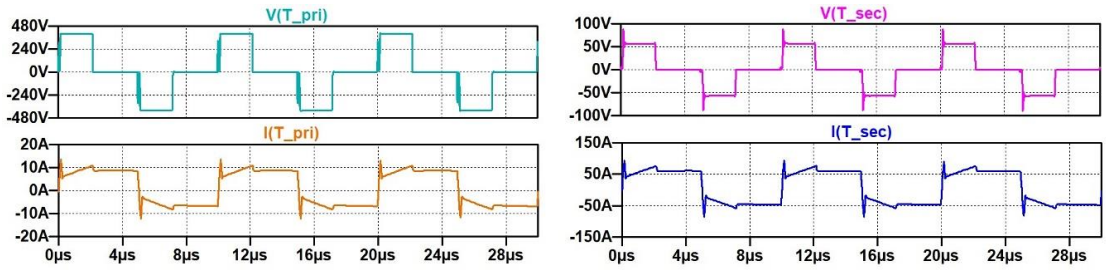

Figure 4.28 : Transformer primary and secondary side voltage V_{T_pri}, V_{T_sec} and current waveforms I_{T_pri}, I_{T_sec} at 100 A load current.

Output inductors current, output load current and voltage waveforms are shown in Figure 4.29.

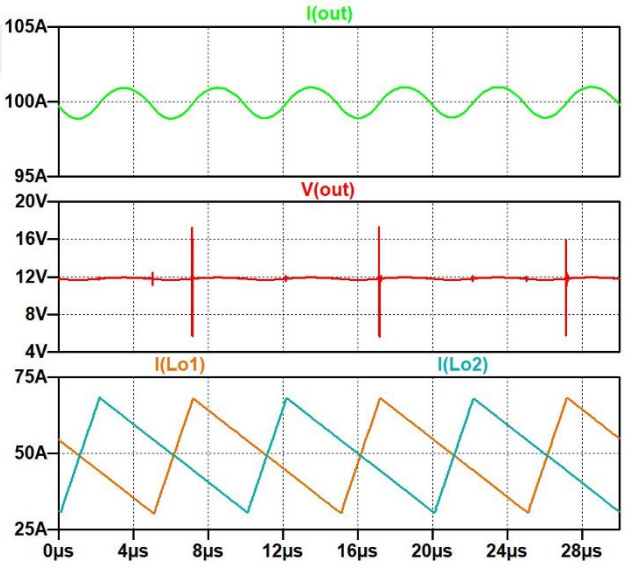

Figure 4.29 : Output load current I_{out} and voltage V_{out}, output inductors current I_{Lo1}, I_{Lo2} at 100 A load current.

The current waveform of clamping diode D_{c1}, voltage and current waveforms of S_1, which is the lagging leg switch, and S_4, which is the leading leg switch, are given in Figure 4.30. In addition, the voltage and current waveform, which belong to the secondary side switch S_{SR1} are also shared in Figure 4.31.

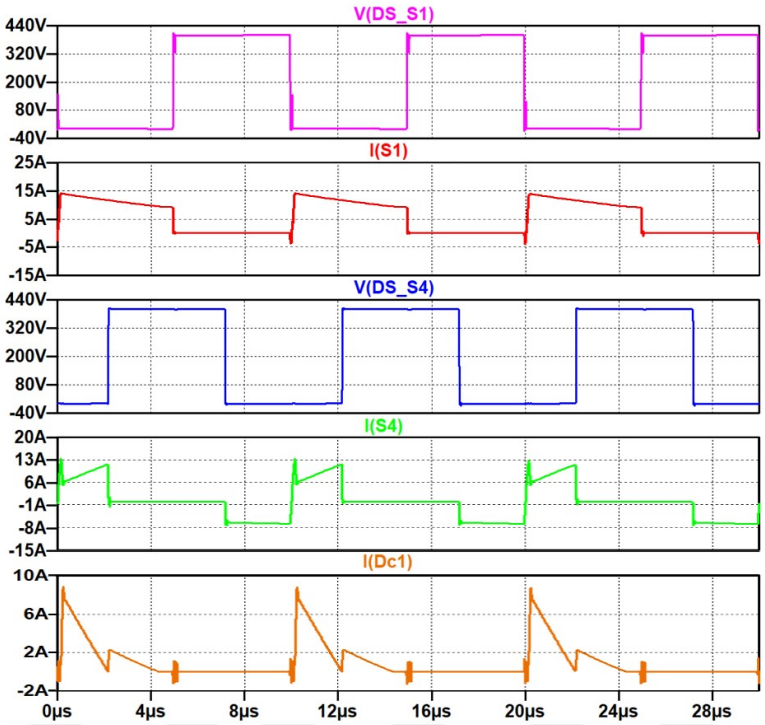

Figure 4.30 : Primary side switch S1 and S4 voltage V_{DS_S1}, V_{DS_S4} and current I_{S1}, I_{S4} waveform; clamping diode D_{c1} current waveform I_{Dc1} at 100 A load current.

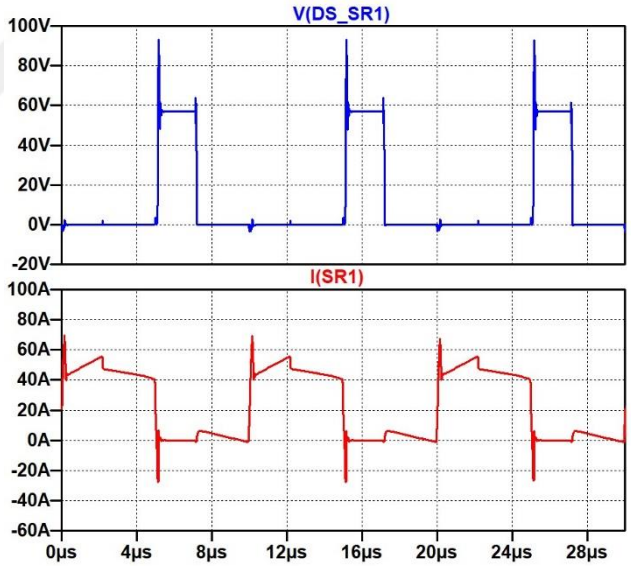

Figure 4.31 : Voltage V_{DS_SR1} and current I_{SR1} waveform of secondary side switch S_{SR1} at 100 A load current.

A zoomed view of waveforms that belong to S_1 and S_4 and their PWM waveforms are also given for better observation of the ZVS event in Figure 4.32.

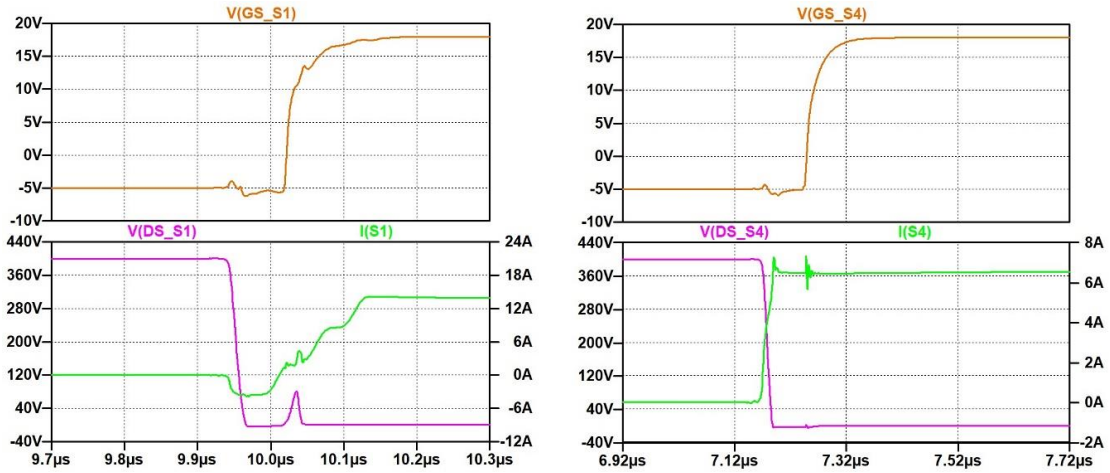

Figure 4.32 : ZVS event of primary side switches S_1 and S_4 at 100 A load current.

It can be seen that ZVS is achieved both leading and lagging leg switch.

Efficiency is calculated as 92.42%.

4.4.2.3 Simulation results at 150 A load current

The simulation results of the operation with a 150 A load have been shared. Transformer voltage and current waveforms for both the primary and secondary sides can be seen in Figure 4.33. Duty cycle loss mode can be observed when the primary side current direction changes.

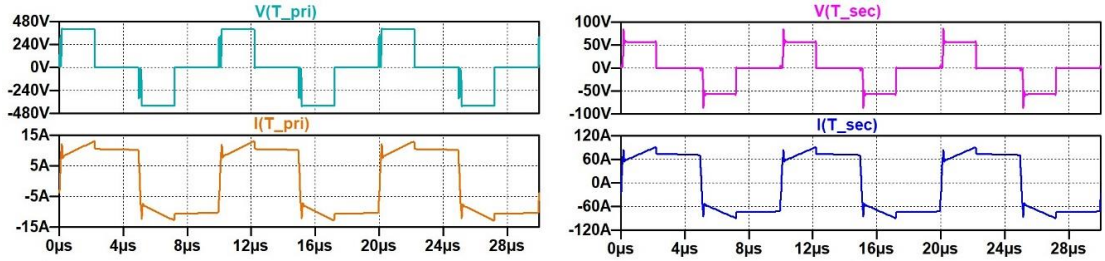

Figure 4.33 : Transformer primary and secondary side voltage V_{T_pri}, V_{T_sec} and current waveforms I_{T_pri}, I_{T_sec} at 150 A load current.

Output inductors current, output load current, and voltage waveforms are shown in Figure 4.34.

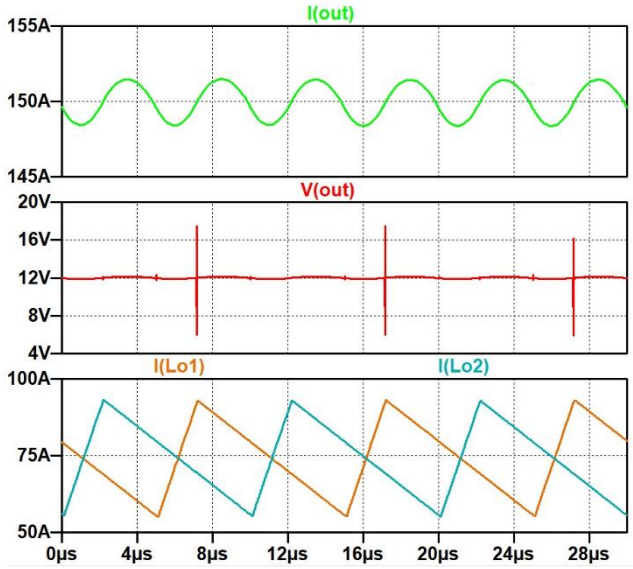

Figure 4.34 : Output load current I_{out} and voltage V_{out}, output inductors current I_{Lo1}, I_{Lo2} at 150 A load current.

The current waveform of clamping diode D_{c1}, voltage and current waveforms of S_1, which is the lagging leg switch and S_4, which is the leading leg switch, are given in Figure 4.35. Additionally, the voltage and current waveform, which belong to the secondary side switch S_{SR1} is also shared in Figure 4.36.

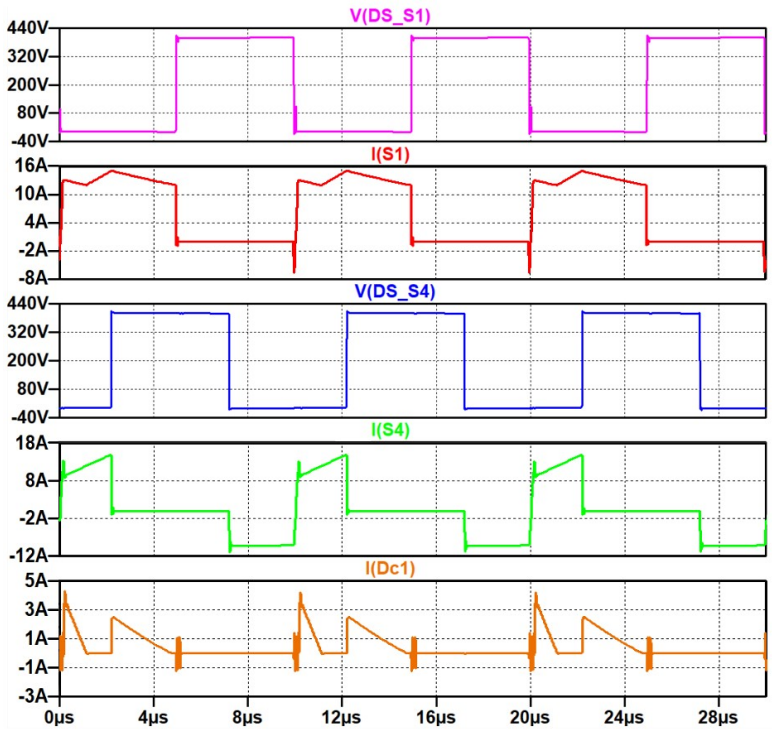

Figure 4.35 : Primary side switch S_1 and S_4 voltage V_{DS_S1}, V_{DS_S4} and current I_{S1}, I_{S4} waveform; clamping diode D_{c1} current waveform I_{Dc1} at 150 A load current.

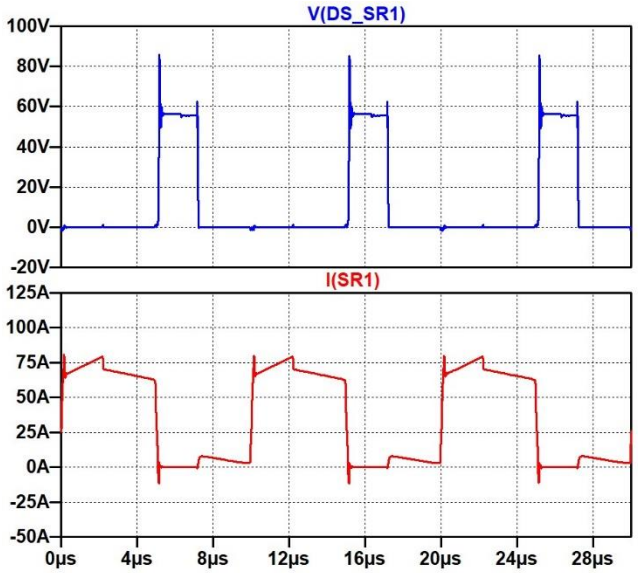

Figure 4.36 : Voltage V_{DS_SR1} and current I_{SR1} waveform of secondary side switch S_{SR1} at 150 A load current.

Zoomed view of waveforms that belong to S_1 and S_4 and their PWM waveforms are also given for better observation of the ZVS event in Figure 4.37.

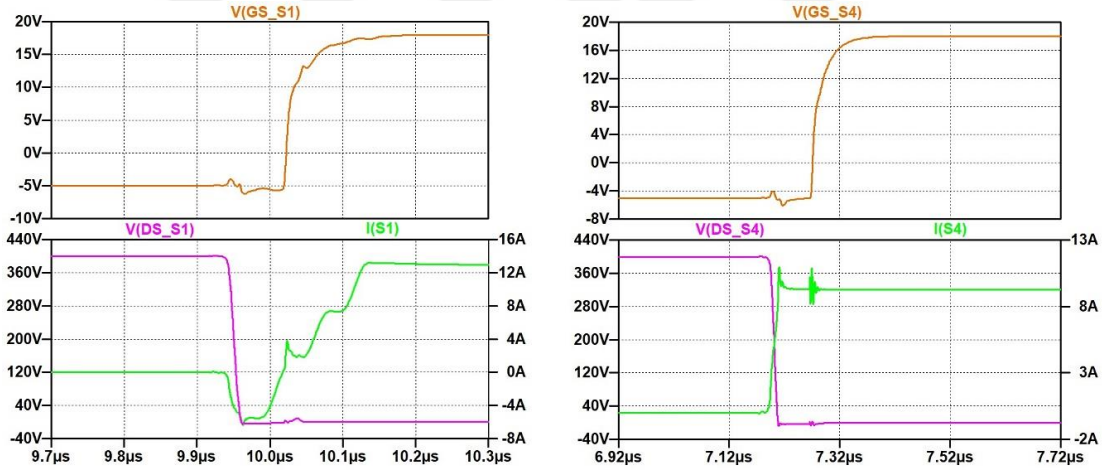

Figure 4.37 : ZVS event of primary side switches S_1 and S_4 at 150 A load current.

It can be seen that ZVS is achieved both leading and lagging leg switch.

Efficiency is calculated as 95.54%.

4.4.2.4 Simulation results at 200 A load current

The simulation results of the operation with a 200 A load have been shared. Transformer voltage and current waveforms for both the primary and secondary side

can be seen in Figure 4.38. Duty cycle loss mode can be observed when the primary side current direction changes.

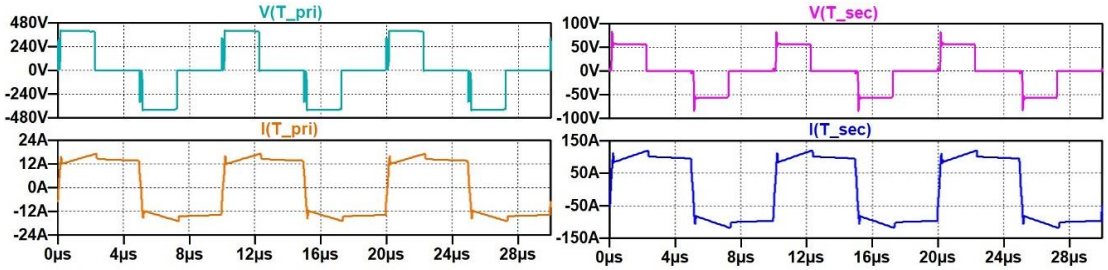

Figure 4.38 : Transformer primary and secondary side voltage V_{T_pri}, V_{T_sec} and current waveforms I_{T_pri}, I_{T_sec} at 200 A load current.

Output inductors current, output load current and voltage waveforms are shown in Figure 4.39.

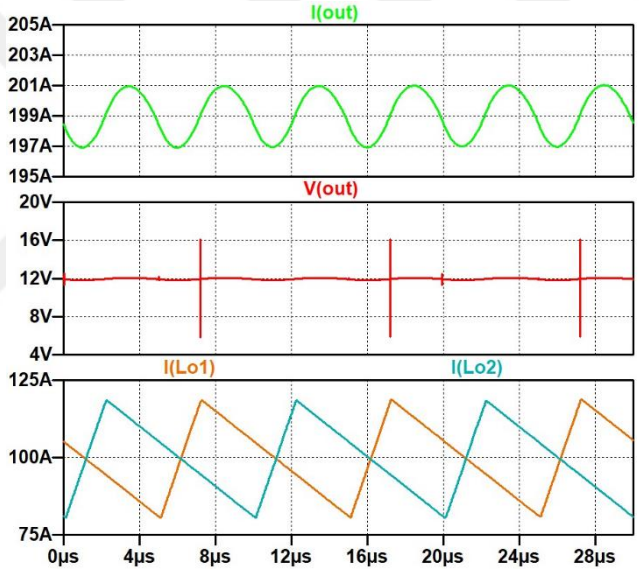

Figure 4.39 : Output load current Iout and voltage V_{out}, output inductors current I_{Lo1}, I_{Lo2} at 200 A load current.

The current waveform of clamping diode D_{c1}, voltage and current waveforms of S_1, which is the lagging leg switch and S_4, which is the leading leg switch, are given in Figure 4.40. Additionally, the voltage and current waveform, which belong to the secondary side switch S_{SR1} are also shared in Figure 4.41.

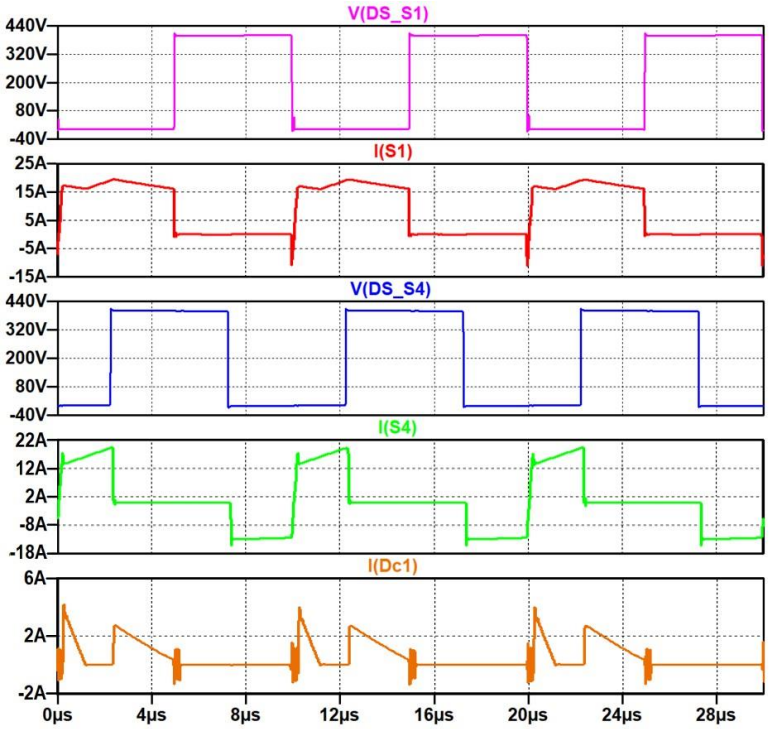

Figure 4.40 : Primary side switch S_1 and S_4 voltage V_{DS_S1}, V_{DS_S4} and current I_{S1}, I_{S4} waveform; clamping diode D_{c1} current waveform I_{Dc1} at 200 A load current.

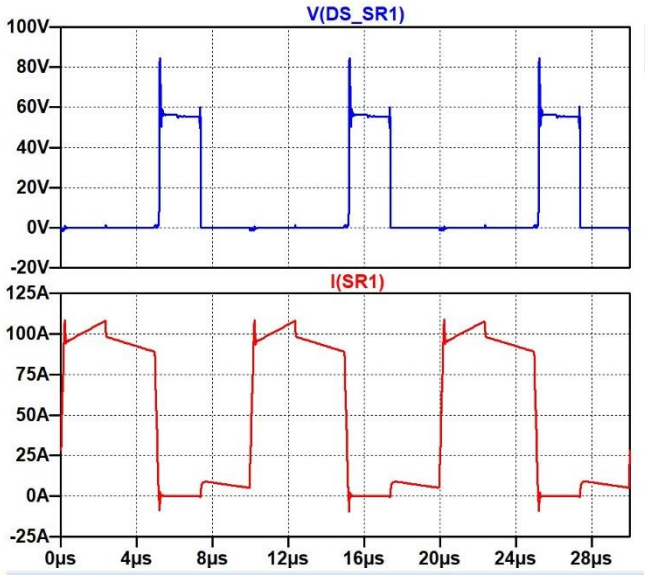

Figure 4.41 : Voltage V_{DS_SR1} and current I_{SR1} waveform of secondary side switch S_{SR1} at 200 A load current.

A zoomed view of waveforms that belong to S_1 and S_4 and their PWM waveforms are also given for better observation of the ZVS event in Figure 4.42.

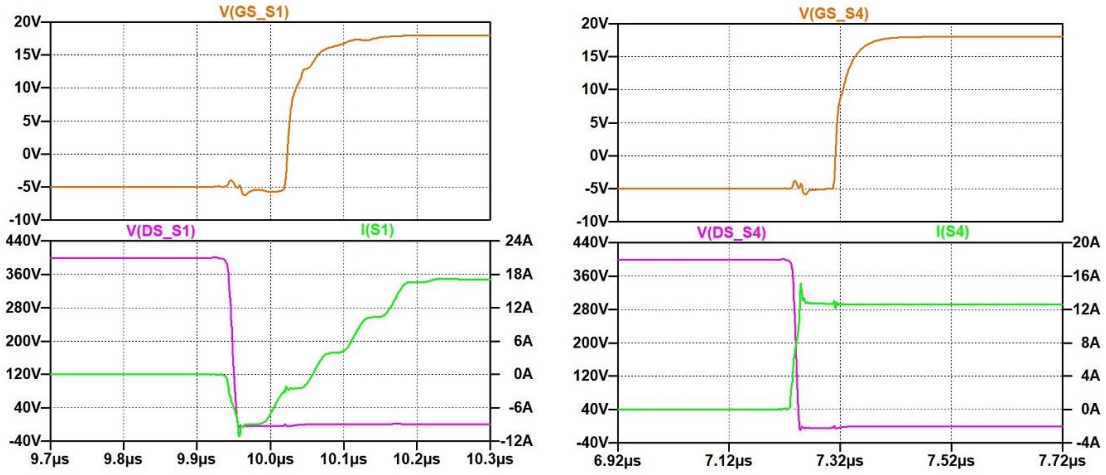

Figure 4.42 : ZVS event of primary side switches S_1 and S_4 at 200 A load current.

It can be seen that ZVS is achieved both leading and lagging leg switch.

Efficiency is calculated as 96.59%.

4.4.2.5 Simulation results at 250 A load current

The simulation results of the operation with a 250 A load have been shared. Transformer voltage and current waveforms for both the primary and secondary sides can be seen in Figure 4.43. Duty cycle loss mode can be observed when the primary side current direction changes.

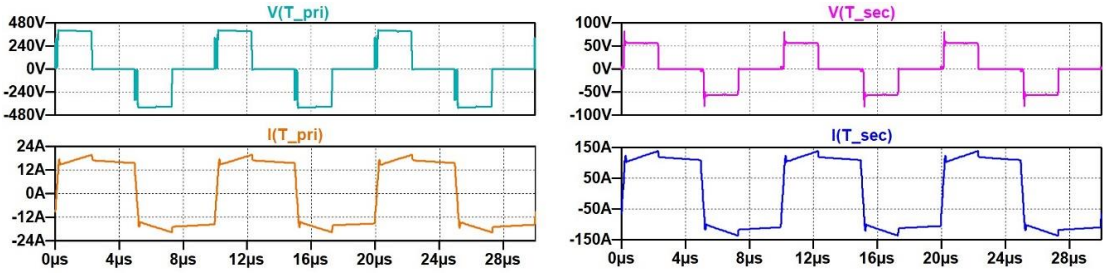

Figure 4.43 : Transformer primary and secondary side voltage V_{T_pri}, V_{T_sec} and current waveforms I_{T_pri}, I_{T_sec} at 250 A load current.

Output inductors current, output load current and voltage waveforms are shown in Figure 4.44.

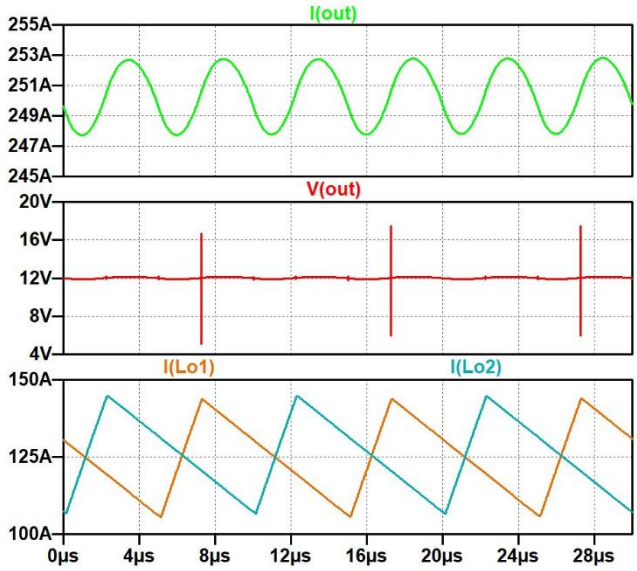

Figure 4.44 : Output load current I_{out} and voltage V_{out}, output inductors current I_{Lo1}, I_{Lo2} at 250 A load current.

The current waveform of clamping diode D_{c1}, voltage and current waveforms of S_1, which is the lagging leg switch and S_4, which is the leading leg switch, are given in Figure 4.45. Additionally, the voltage and current waveform which belong to the secondary side switch S_{SR1} are also shared in Figure 4.46.

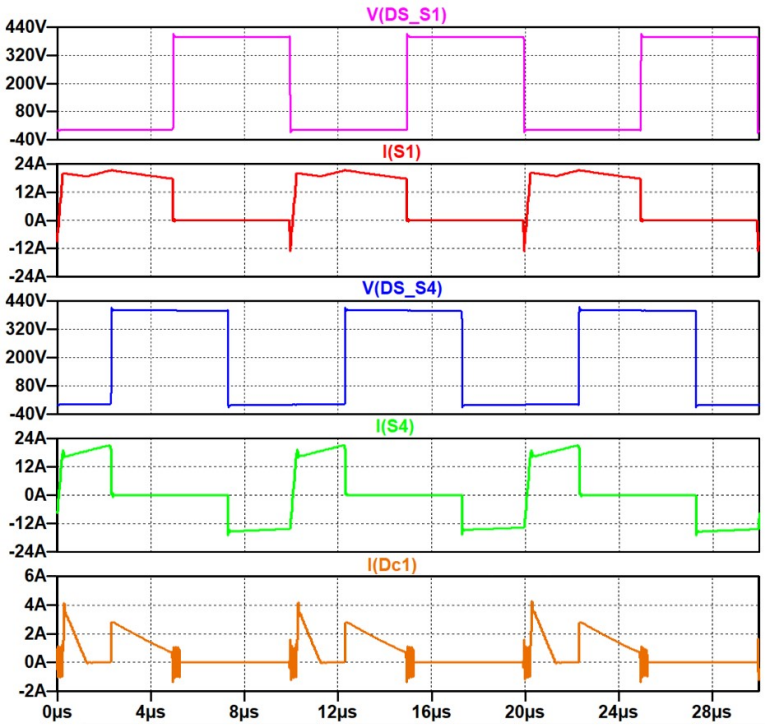

Figure 4.45 : Primary side switch S1 and S4 voltage V_{DS_S1}, V_{DS_S4} and current I_{S1}, I_{S4} waveform; clamping diode D_{c1} current waveform I_{Dc1} at 250 A load current.

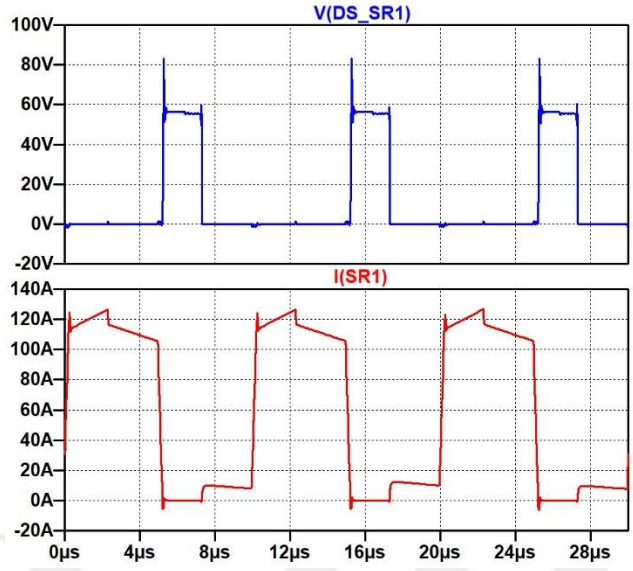

Figure 4.46 : Voltage V_{DS_SR1} and current I_{SR1} waveform of secondary side switch S_{SR1} at 250 A load current.

A zoomed view of waveforms that belong to S_1 and S_4 and their PWM waveforms are also given for better observation of the ZVS event in Figure 4.47.

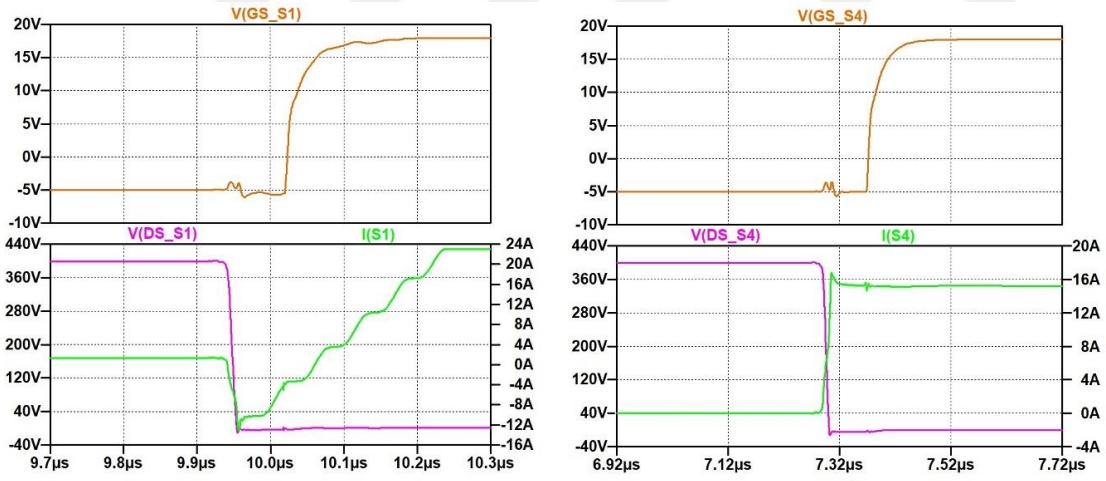

Figure 4.47 : ZVS event of primary side switches S_1 and S_4 at 250 A load current.

It can be seen that ZVS is achieved both leading and lagging leg switch.

Efficiency is calculated as 96.54%.

4.4.3 Effect of clamping diodes

The clamping diodes eliminate the voltage overshoot at the primary side because of output charge Q_{oss} and body diode reverse recovery charge Q_{rr} of secondary side

switches. Moreover, the externally added inductor, which is a shim inductor to extend the ZVS operation range for the leading leg, contributes to this phenomenon. Due to the action of the primary side clamping diodes, the stored energy in L_{shim} is recirculated on the primary side of the converter. This stored energy does not contribute to the secondary side commutation resonance. However, voltage overshoot because transformer leakage inductance can not be clamped [55,56].

Voltage waveforms of the primary and the secondary side of transformer can be observed at the operating condition, which is with and without clamping diode in Figure 4.49. To better understanding of the plotted voltage waveform, measured voltage nodes are indicated with the related color of waveforms in Figure 4.48.

It can be seen that the voltage overshoot generated by L_{shim} is clamped to supply voltage. Peak voltage values between nodes, which are indicated with blue and turquoise, are 530 V and 81.57 V, respectively while clamping diodes exist during the operation at 400 V input voltage and 250 A load current. The transformer L_{Lk} overshoot cannot be clamped as mentioned. These values are measured as 592 V and 84.57 V while clamping diodes do not exist. A higher voltage spike causes stress and higher power loss over the primary side switches.

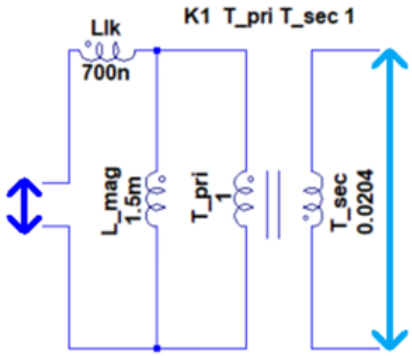

Figure 4.48 : Measurement points of voltage waveforms of primary and secondary side.

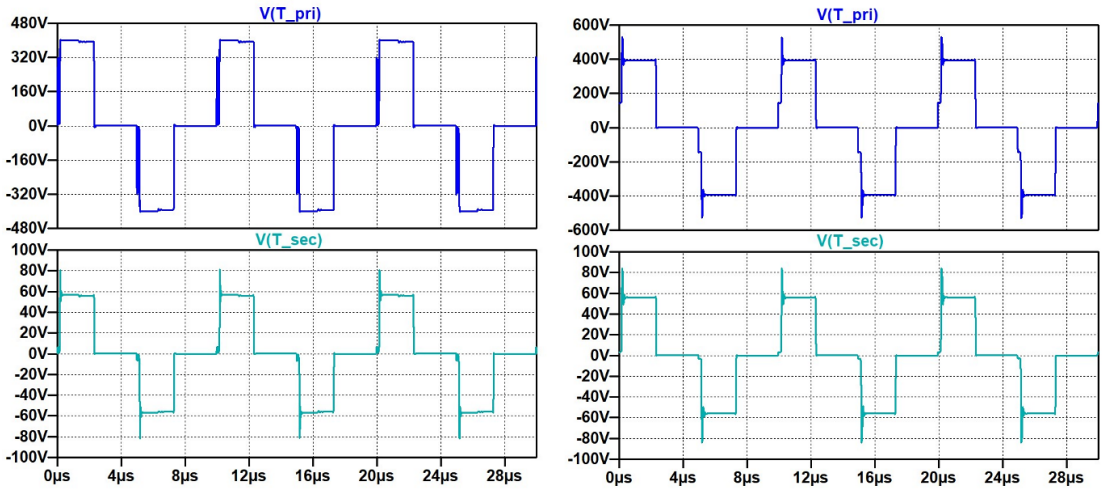

Figure 4.49 : Voltage waveforms of primary and secondary side (left one with clamping diode, right one without clamping diode).

Efficiency is another parameter affected by clamping diode usage.

L_{shim} provides additional energy to achieve ZVS for the lagging switches. Clamping diodes provide the path for circulating current to have higher inductive energy, which is used during the turn-on time of lagging leg switches. Higher inductive energy improves the ZVS ability for the light load operation [55,56]. This situation directly affects the efficiency, as shown in Figure 4.50.

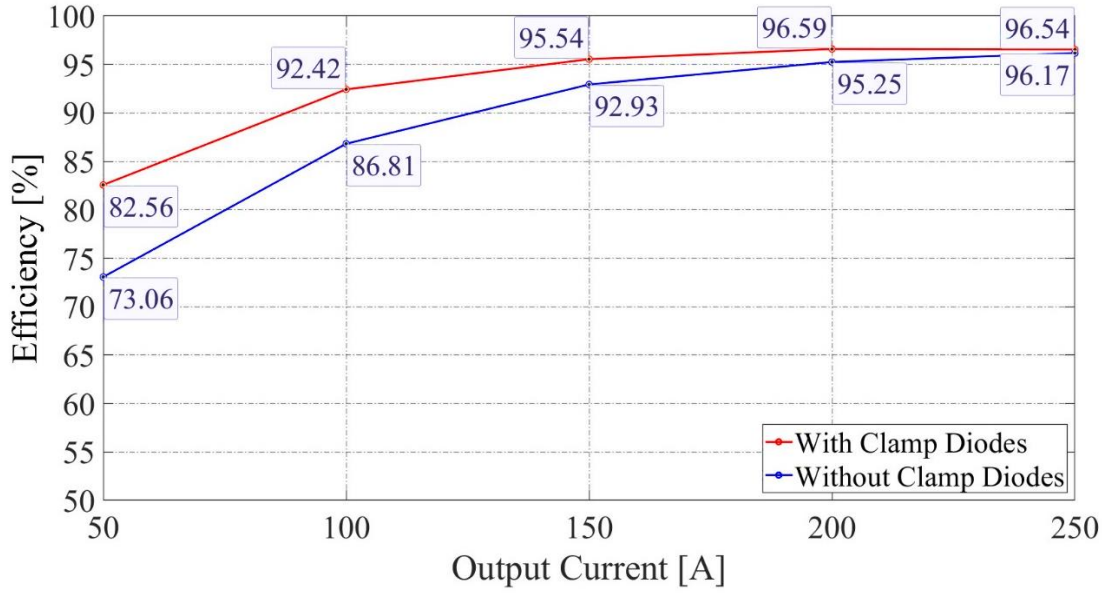

Figure 4.50 : Efficiency for operating with and without clamping diodes.

5. IMPLEMENTATION AND EXPERIMENTAL RESULTS OF PSFB WITH CDR CONVERTER

General test setup information, experimental results, and several waveforms obtained are given in this chapter. Detailed observations of leading and lagging switches, and rectification side switches are shared. Voltage of transformer primary side and secondary side, and primary side transformer current are evaluated. Moreover, efficiencies are measured according to shared input, output voltage, and current. PSFB with CDR converter is tested at nominal input and output voltage with changing load currents, which are 50 A, 100 A, 150 A, 200 A, and 250 A.

As a result of the experimental results, efficiencies which are obtained from the simulation and experiment are compared.

5.1 Hardware Implementation

PSFB with CDR converter consists of four discrete SiC top side cooled (TSC) N-Channel MOSFET at the primary side. The secondary side of the converter is also designed with four discrete Si TSC N-Channel MOSFETs, which two of them are paralleled to each other. The connection of both side switches is shared in Figure 3.11. TSC technology is state-of-the-art technology which is preferred to have better thermal conductivity instead of the bottom side cooled (BSC) packaged switch. More reliable and efficient operation can be achieved.

Application example of BSC approach on FR4 PCB, BSC approach on insulated metal substrate (IMS) board and TSC approach with applied gap filler for D2PAK-7L package are shared in Figure 5.1. Junction to case thermal resistances $R_{th,j\text{-}c}$ of each configuration are given in Figure 5.2.

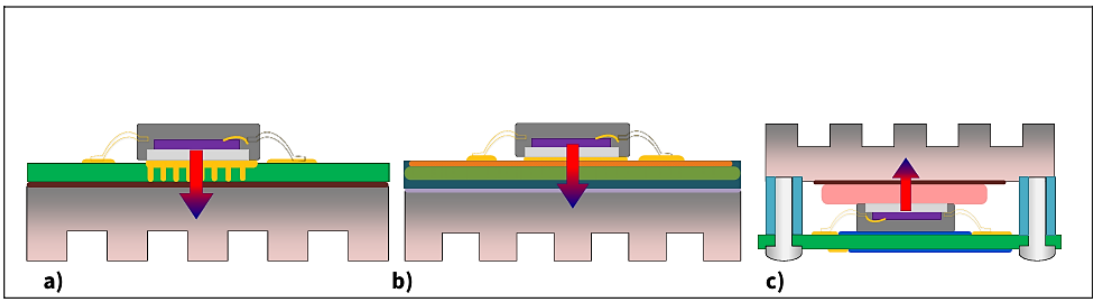

Figure 5.1 : Application of a) BSC approach on FR4 PCB, b) BSC approach on IMS board and c) TSC approach with applied gap filler for D2PAK-7L package [57].

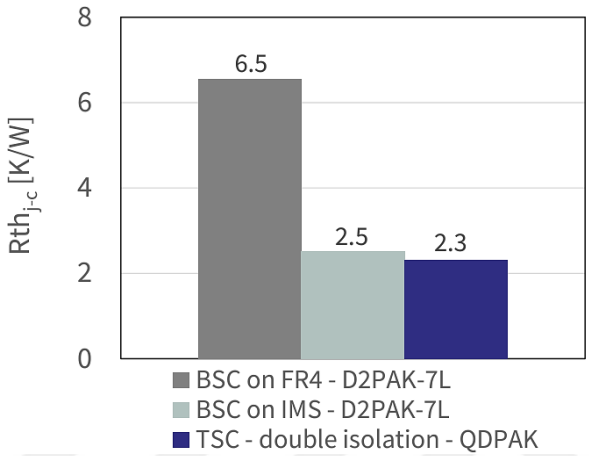

Figure 5.2 : $Rth_{j\text{-}c}$ of BSC approach on FR4 PCB, BSC approach on IMS board and TSC approach with applied gap filler for D2PAK-7L package [57].

Two dual-channel isolated gate drivers are used for the primary side switches; one is used for the secondary side switches. The primary side gate driver voltage is between +15 V and -5 V to prevent self-turn-on phenomena. The secondary side gate driver voltage is between +10 V and 0 V. Supply voltages of gate driver circuits are generated with a half-bridge converter internally.

PCMC, which is a control method of the converter, is executed by a microcontroller. The current at the primary side is sensed with the current transformer. The sensed signal is measured and evaluated by the microcontroller. Furthermore, input and output voltage are also sensed and evaluated by the microcontroller. These measurement signals are used for both the control loop and protection.

Routing of the high di/dt path is especially designed carefully to prevent unexpected voltage spikes and oscillations. The placement of the transformer, magnetics and also switches is decided with considering this.

All magnetics and switches are cooled with a liquid-cooled plate which is given in Figure 5.3.

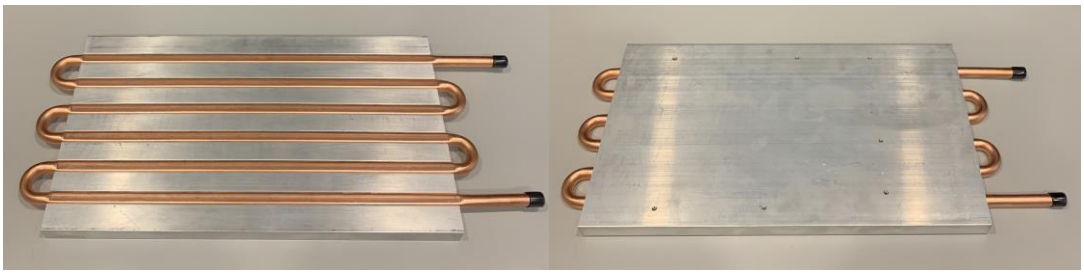

Figure 5.3 : Liquid cooled plate.

Designed and implemented PSFB with CDR converter is given in Figure 5.4. Main parts of the design are indicated with numbers. One is the input DC-link capacitor; two is the primary side switch; three is the shim inductor; four is the planar transformer; five is the seconder side switch; six is the output inductor; seven is the gate driver; eight is the gate driver supply; nine is microcontroller; 10 is a current transformer; 11 is output DC-link capacitor.

Power density of the converter is 1.87 kW/L.

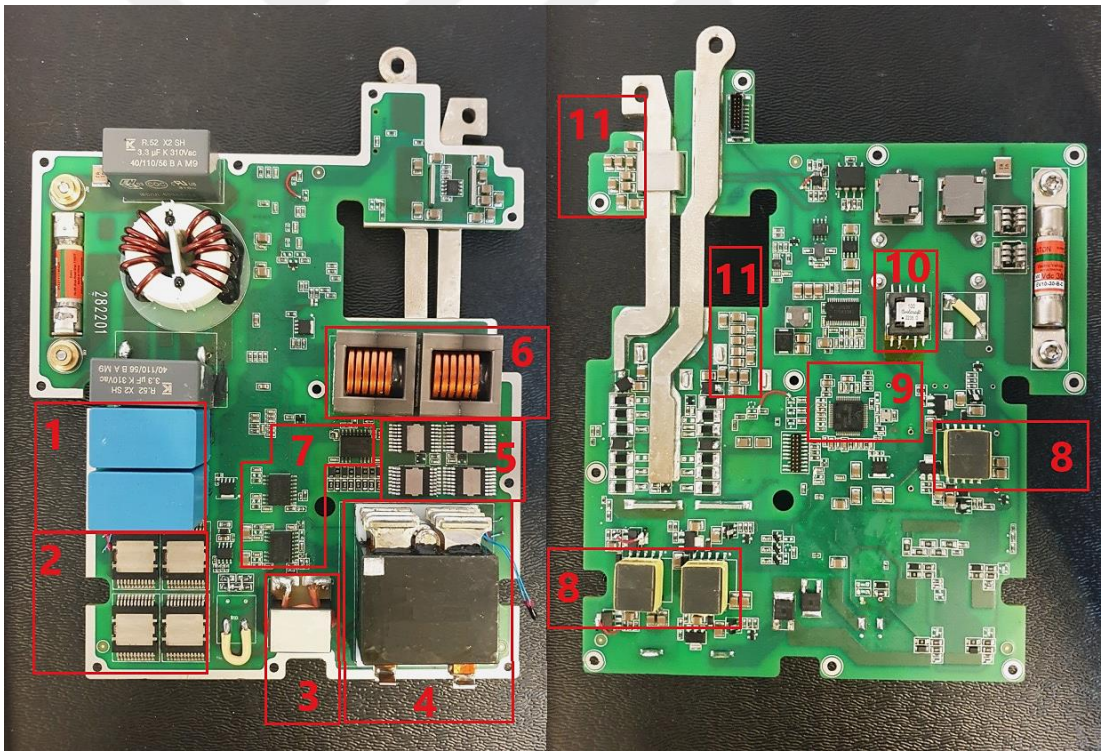

Figure 5.4 : Designed and implemented PSFB with CDR converter.

5.2 Experimental Results

Several equipments that are used to test PSFB with a CDR converter are necessary. First of all, HV power supply is needed to emulate the HV battery. Electronic load is used as an output load and LV battery. LV power supply is used to provide an internal

12 V supply which will be converted to different voltage levels. Joint test action group (JTAG) board is required to flash the code to the microcontroller in the PCB. An oscilloscope is another main equipment for observation of the converter's waveforms. The setup view with all essential devices is shared in Figure 5.5.

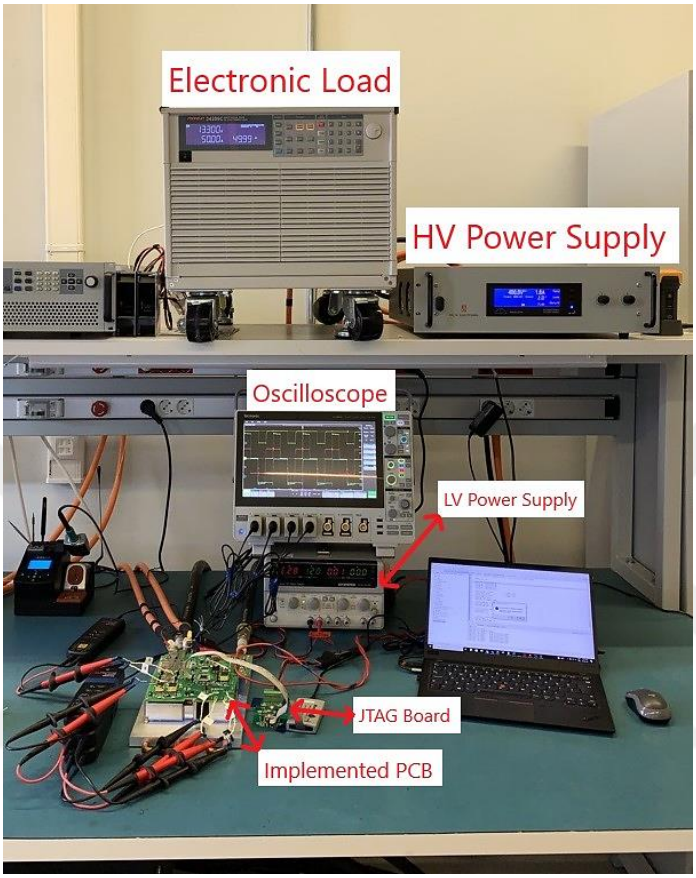

Figure 5.5 : Setup view for PSFB with CDR converter.

Designed board is tested at nominal input voltage as 400 V, nominal output voltage as 12 V, and different load currents, which are 50 A, 100 A, 150 A, 200 A, and 250 A. The converter is tested at maximum operating power rating as 3 kW when the load current is 250 A.

PWM waveforms are considerably critical for the proper operation of PSFB with a CDR converter. The correlation of PWM waveforms with each other is explained in detail in chapter 3.2.2. Obtained PWM waveforms for both primary and secondary side switches from the oscilloscope are given in Figure 5.6. The amount of phase shift changes according to operating conditions to reach the required output voltage and current.

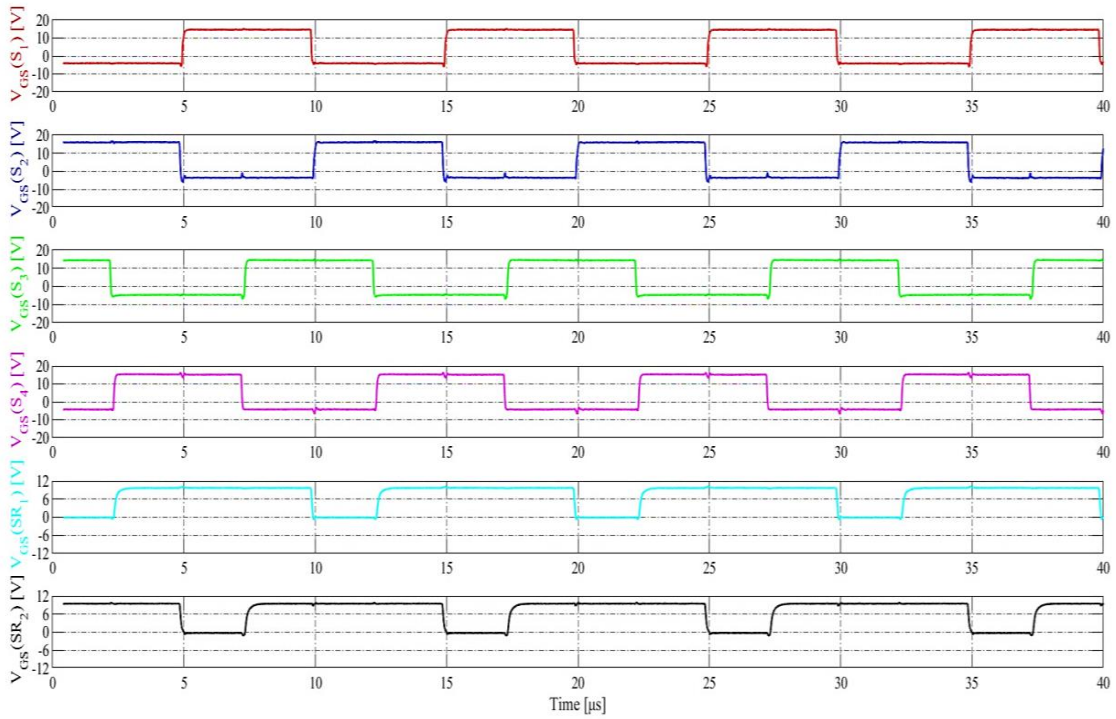

Figure 5.6 : PWM waveforms of S_1 in red, S_2 in blue, S_3 in green, S_4 in purple, S_{SR1} in turquoise, S_{SR2} in black.

Several waveforms are observed at each operating point. Drain to source voltage V_{DS} waveforms with related switch gate signals V_{GS} are observed for S_1, which is one of the leading leg switches, and S_4, which is one of the lagging leg switches. The same waveforms are also monitored for S_{SR1}, which is one of the secondary switches. These waveforms make it possible to evaluate the soft switching behavior of switches.

Moreover, transformer primary and secondary side voltage and primary side current waveforms are observed. Input voltage and current, output voltage and current waveforms which are obtained from the test, are shared. Efficiencies are calculated at each operating point.

Detailed waveforms of output voltage and duty cycle loss phenomena are observed at 250 A output load.

All waveforms are drawn in MATLAB with obtained data sets from the oscilloscope.

5.2.1 Experimental results at 50 A load current

The experimental results which indicate the performance of designed and implemented PSFB with CDR converter, are shared for 50 A load current operation.

First of all, V_{DS} waveforms with V_{GS} of S_1 are shared in Figure 5.7. Zoomed waveforms of V_{DS} and V_{GS} can be seen in Figure 5.8 during the turn-on transition. It can be observed that ZVS cannot be achieve 50 A load current, yet. However, S_1 starts to conduction when V_{DS} is less than half of the input voltage. This situation also leads to improvement the switching loss.

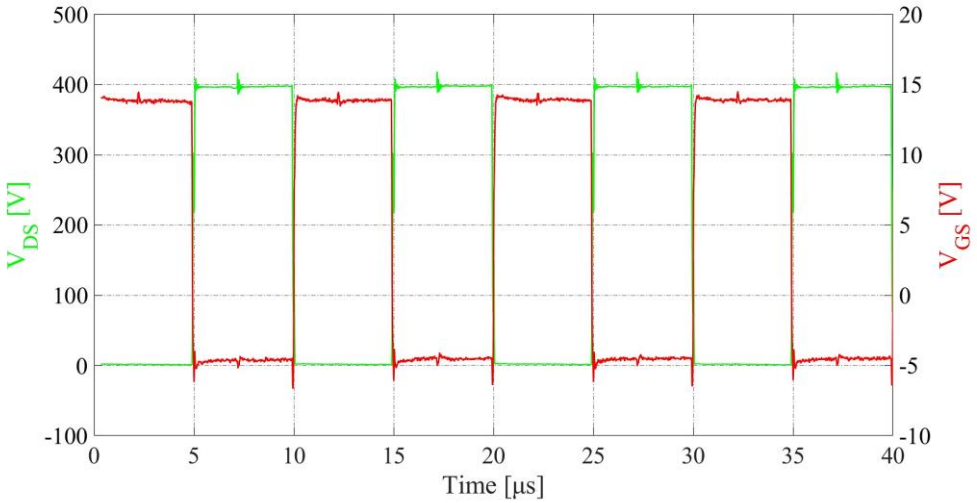

Figure 5.7 : V_{DS} in green and V_{GS} in red of leading leg switch S_1 at 50 A load current.

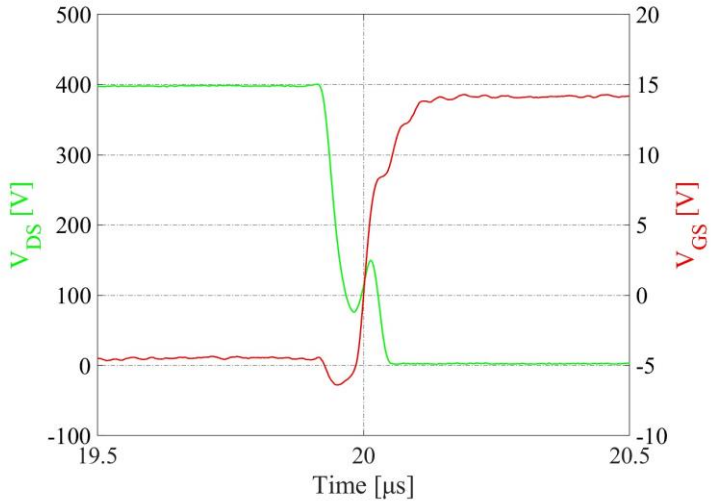

Figure 5.8 : Zoomed view of V_{DS} in green and V_{GS} in red of leading leg switch S_1 at 50 A load current during turn-on.

As same as the S_1, V_{DS} waveforms with V_{GS} of S_4 are shared in Figure 5.9. Zoomed waveforms of V_{DS} and V_{GS} can be seen during the turn-on transition in Figure 5.10. It can be observed that ZVS can be achieve 50 A load current. Since, lagging leg switches can achieve the ZVS even at light load conditions, on the contrary of leading leg switches.

Spikes which are at the V_{DS}, happen at the end of the power transfer and freewheeling operating periods.

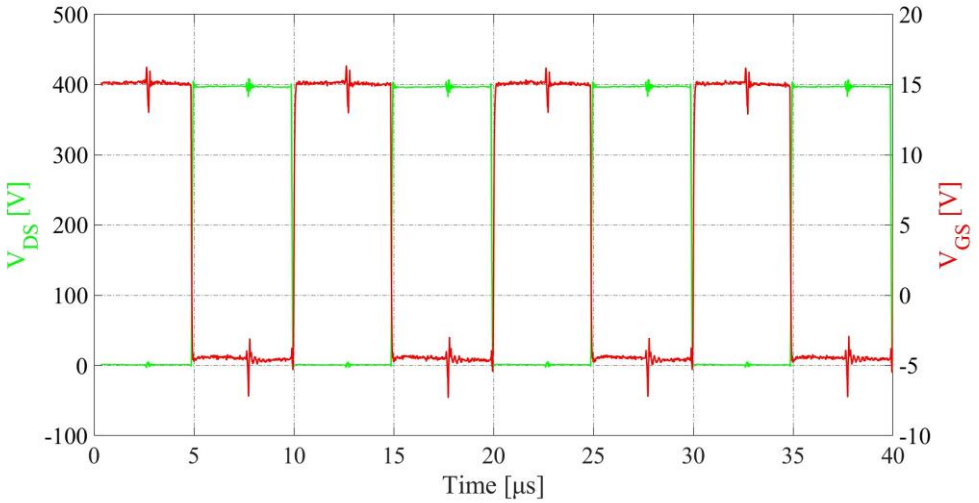

Figure 5.9 : V_{DS} in green and V_{GS} in red of lagging leg switch S_4 at 50 A load current.

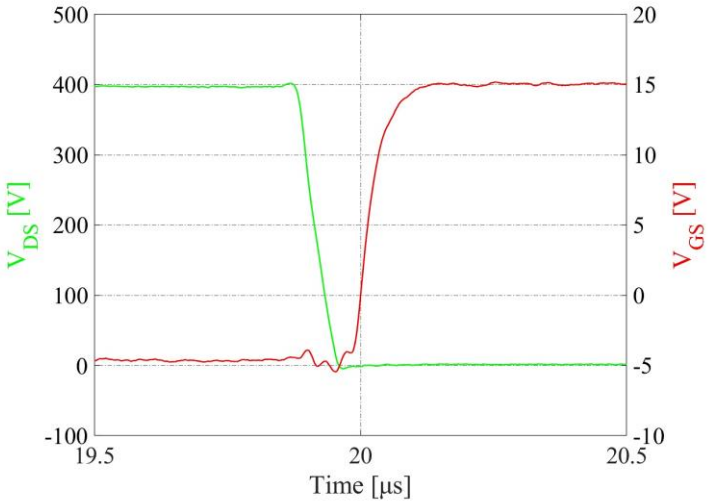

Figure 5.10 : Zoomed view of V_{DS} in green and V_{GS} in red of lagging leg switch S_4 at 50 A load current during turn-on.

V_{DS} waveforms with V_{GS} of S_{SR1} are shared in Figure 5.11. Zoomed waveforms of V_{DS} and V_{GS} can be seen during the turn-off transition in Figure 5.12. It can be observed that ZCS can be achieve. The body diode of S_{SR1} starts to conduct after V_{GS} is low because of the duty cycle loss operation mode.

The reason of the spikes which are at the V_{DS}, is the resonation between transformer leakage inductance and output capacitance of the secondary side switch.

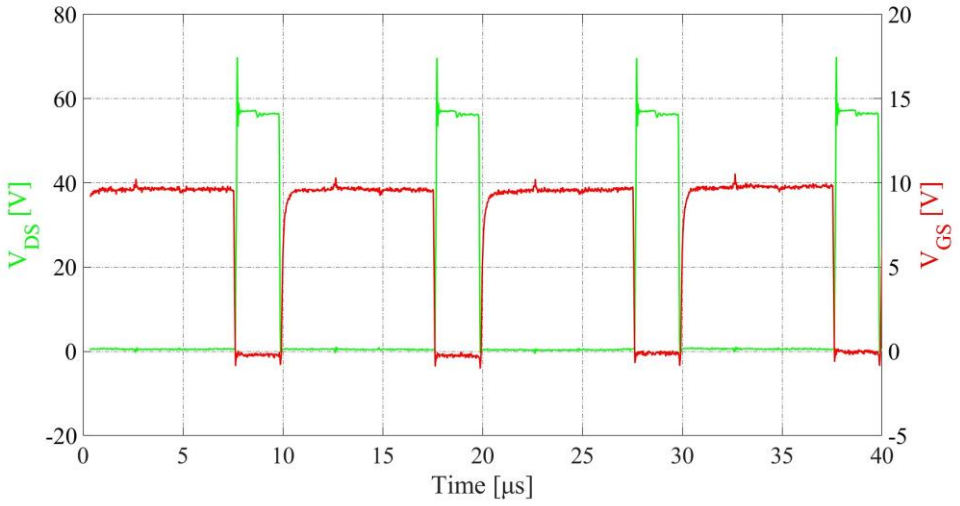

Figure 5.11 : V_{DS} in green and V_{GS} in red of S_{SR1} at 50 A load current.

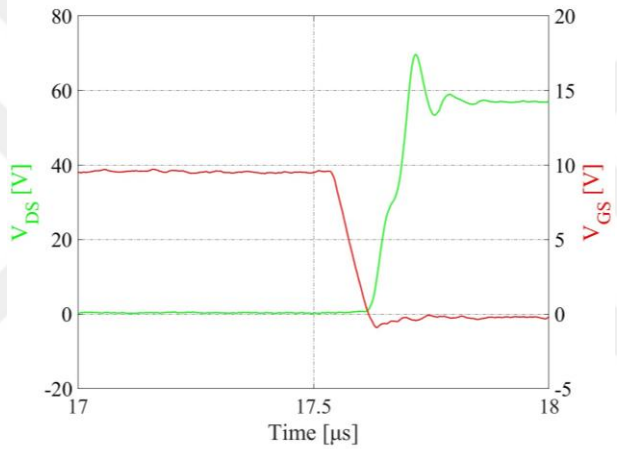

Figure 5.12 : Zoomed view of V_{DS} in green and V_{GS} in red of S_{SR1} at 50 A load current during turn-off.

Transformer primary V_{pri} and secondary side voltage V_{sec} waveform, and primary side current I_{pri} are shared in Figure 5.13. It is important to achieve zero mean for the current to prevent the saturation of the transformer. PCMC becomes prominent according to this requirement. It is observed that PCMC works properly.

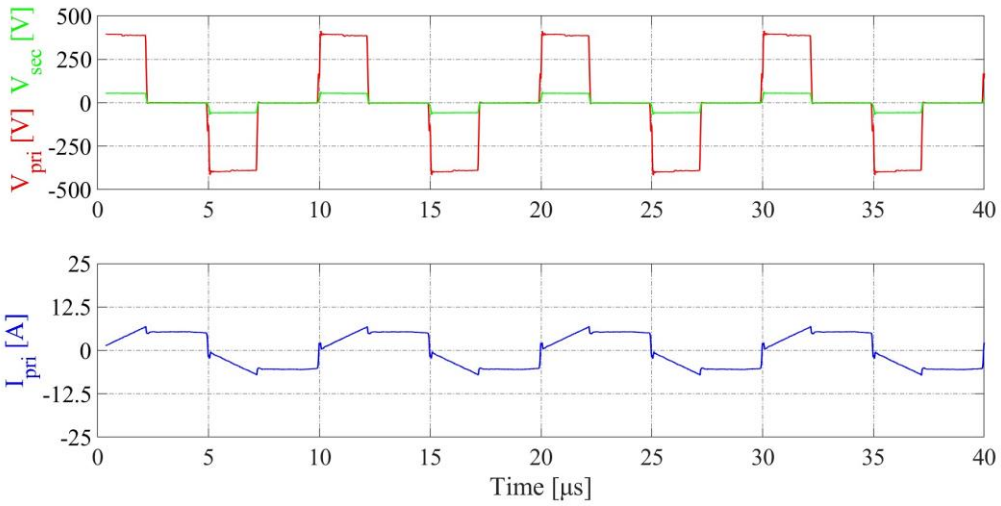

Figure 5.13 : V_{pri} in red, V_{sec} in green and I_{pri} in blue at 50 A load current.

Waveforms of input voltage V_{in} and current I_{in} are given in Figure 5.14. V_{in} is measured as 398.6 V since a regulation error of power supply and current I_{in} is measured as 1.685 A from the oscilloscope.

Waveforms of output voltage V_{out} and current I_{out} are given in Figure 5.15. V_{out} is measured as 12.3 V because of controller and measurement circuits error of power supply and current I_{out} is measured as 47.57 A from the oscilloscope.

According to this measurement, efficiency is calculated as 87.12% for this operating condition.

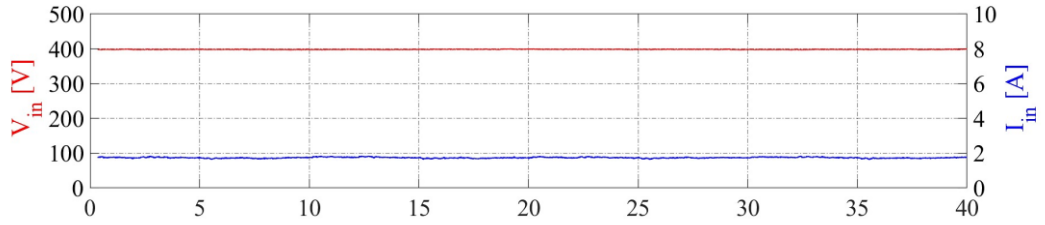

Figure 5.14 : V_{in} in red and I_{in} in blue at 50 A load current.

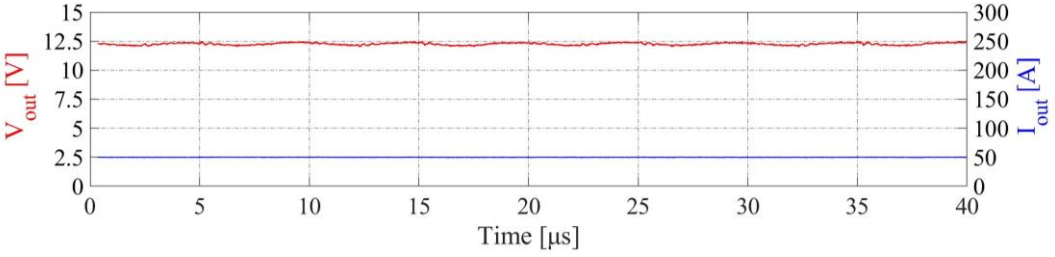

Figure 5.15 : V_{out} in red and I_{out} in blue at 50 A load current.

5.2.2 Experimental results at 100 A load current

The experimental results of designed and implemented PSFB with CDR converter, are shared for 100 A load current operation.

Initially, V_{DS} waveforms with V_{GS} of S_1 are shared in Figure 5.16. Zoomed waveforms of V_{DS} and V_{GS} can be seen during turn-on transition in Figure 5.17. It can be observed that ZVS starts at 100 A load current. A slight voltage spike can be seen in at V_{DS} during turn-on. The reason of this is that PSFB with CDR converter is required to change deadtime with changing load current. Deadtime is 100 ns and fixed in this converter. Because of the safety reason, deadtime is not decreased less than 100 ns in this study. Because of this non-adaptive deadtime, oscillation occurs between primary side leakage inductances and output capacitance of switches [38].

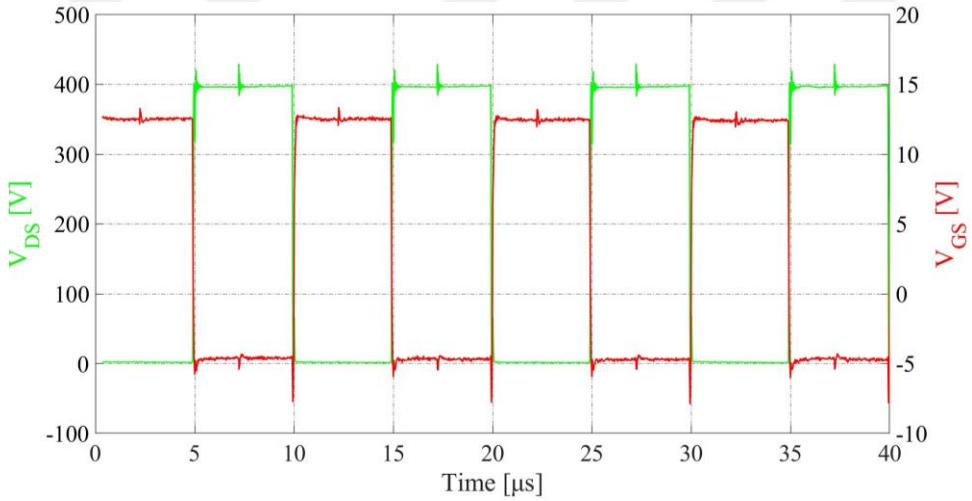

Figure 5.16 : V_{DS} in green and V_{GS} in red of leading leg switch S_1 at 100 A load current.

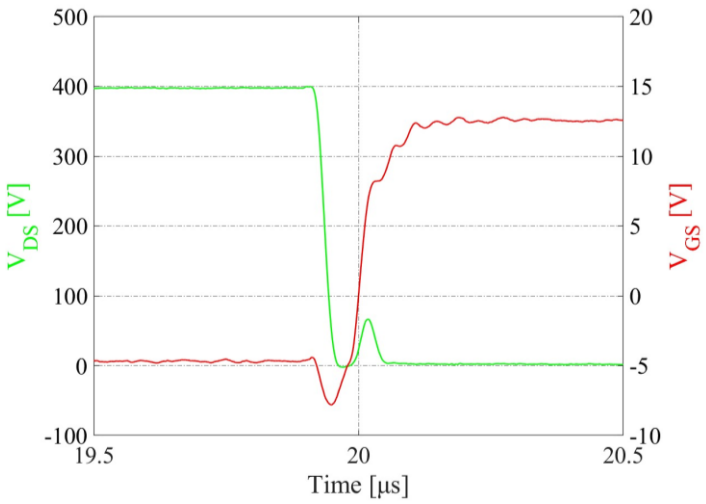

Figure 5.17 : Zoomed view of V_{DS} in green and V_{GS} in red of leading leg switch S_1 at 100 A load current during turn-on.

V_{DS} waveforms with V_{GS} of S_4 are shared in Figure 5.18. Zoomed waveforms of V_{DS} and V_{GS} can be seen during the turn-on transition in Figure 5.19. It can be observed that ZVS can be achieve 100 A load current. The reason of spikes which are at the V_{DS}, is explained previously.

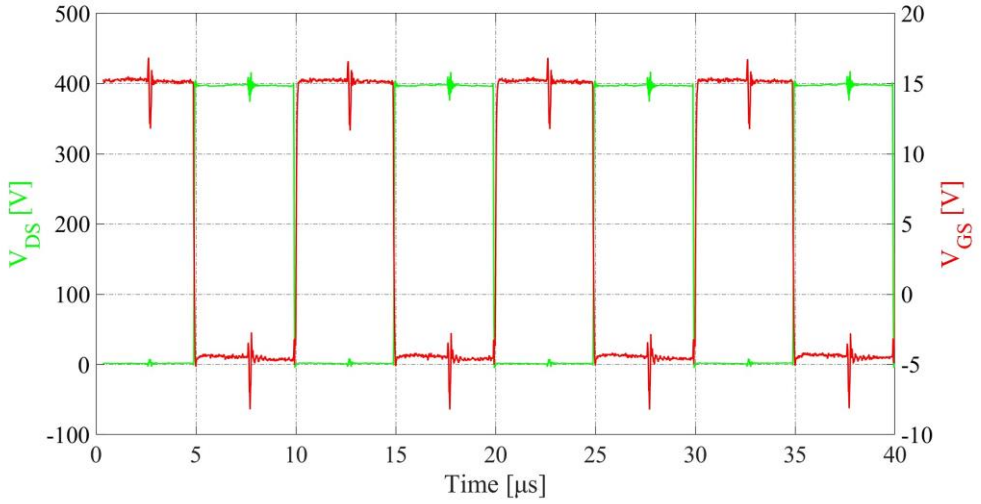

Figure 5.18 : V_{DS} in green and V_{GS} in red of lagging leg switch S_4 at 100 A load current.

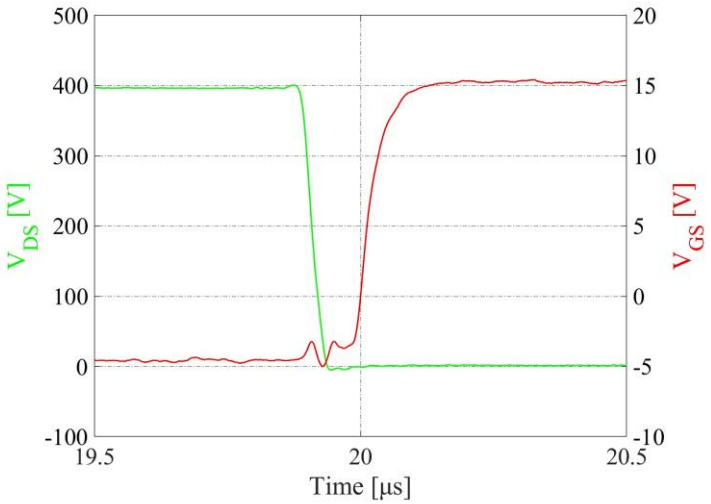

Figure 5.19 : Zoomed view of V_{DS} in green and V_{GS} in red of lagging leg switch S_4 at 100 A load current during turn-on.

V_{DS} waveforms with V_{GS} of S_{SR1} are shared in Figure 5.20. Zoomed waveforms of V_{DS} and V_{GS} can be seen during the turn-off transition in Figure 5.21. It can be observed that ZCS can be achieve.

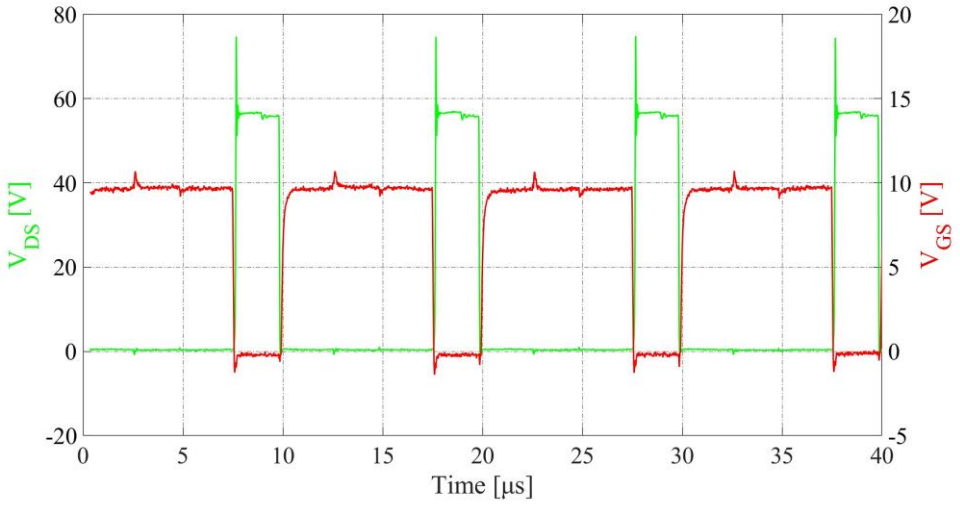

Figure 5.20 : V_{DS} in green and V_{GS} in red of S_{SR1} at 100 A load current.

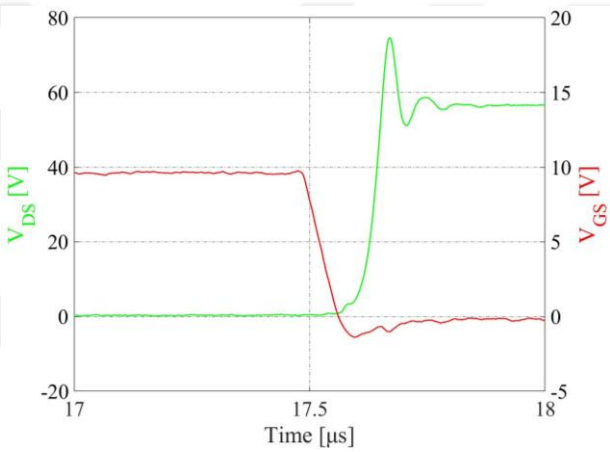

Figure 5.21 : Zoomed view of V_{DS} in green and V_{GS} in red of S_{SR1} at 100 A load current during turn-off at right.

Transformer primary V_{pri} and secondary side voltage V_{sec} waveform, and primary side current I_{pri} are shared in Figure 5.22.

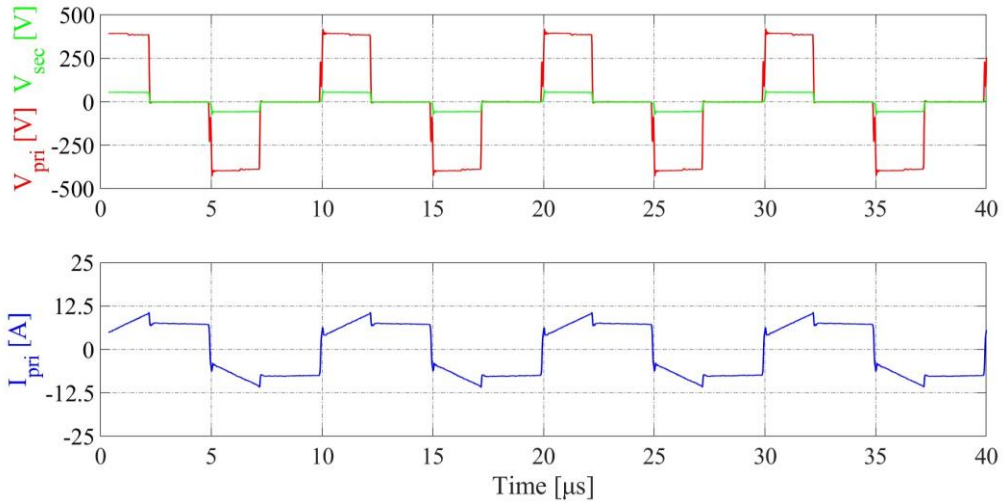

Figure 5.22 : V_{pri} in red, V_{sec} in green and I_{pri} in blue at 100 A load current.

Waveforms of input voltage V_{in} and current I_{in} are given in Figure 5.23. V_{in} is measured as 397.7 V and I_{in} is measured as 3.272 A from the oscilloscope.

Waveforms of output voltage V_{out} and current I_{out} are given in Figure 5.24. V_{out} is measured as 12.33 V and I_{out} is measured as 98.69 A from the oscilloscope.

According to this measurement, efficiency is calculated as 93.51% for this operating condition.

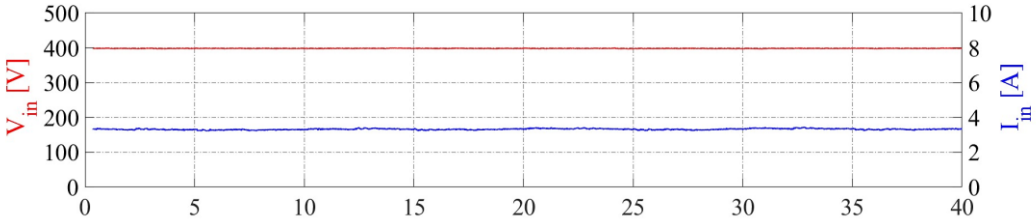

Figure 5.23 : V_{in} in red and I_{in} in blue at 100 A load current.

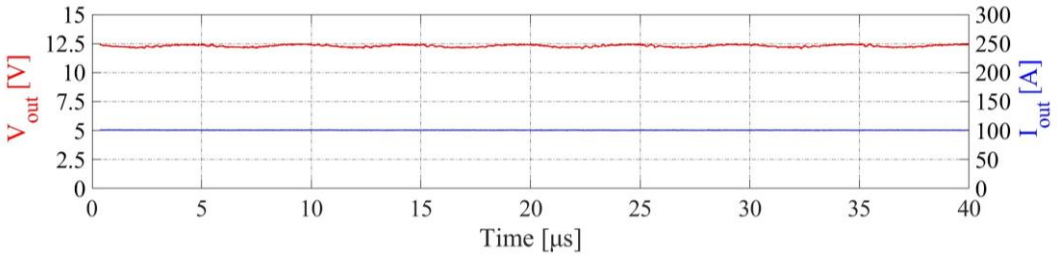

Figure 5.24 : V_{out} in red and I_{out} in blue at 100 A load current.

5.2.3 Experimental results at 150 A load current

The experimental results of designed and implemented PSFB with CDR converter, are shared for 150 A load current operation.

V_{DS} waveforms with V_{GS} of S_1 are shared in Figure 5.25. Zoomed waveforms of V_{DS} and V_{GS} can be seen during the turn-on transition in Figure 5.26. It can be observed that ZVS happens at 150 A load current.

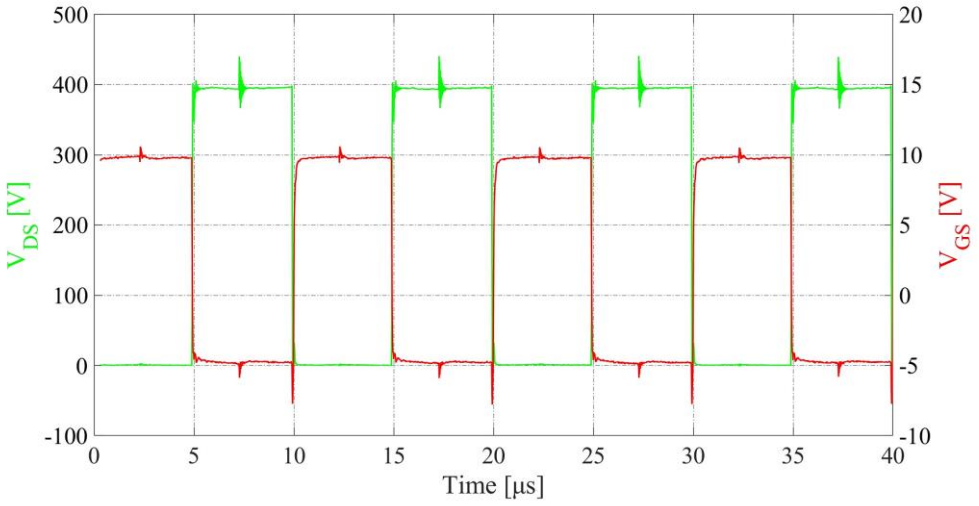

Figure 5.25 : V_{DS} in green and V_{GS} in red of leading leg switch S_1 at 150 A load current.

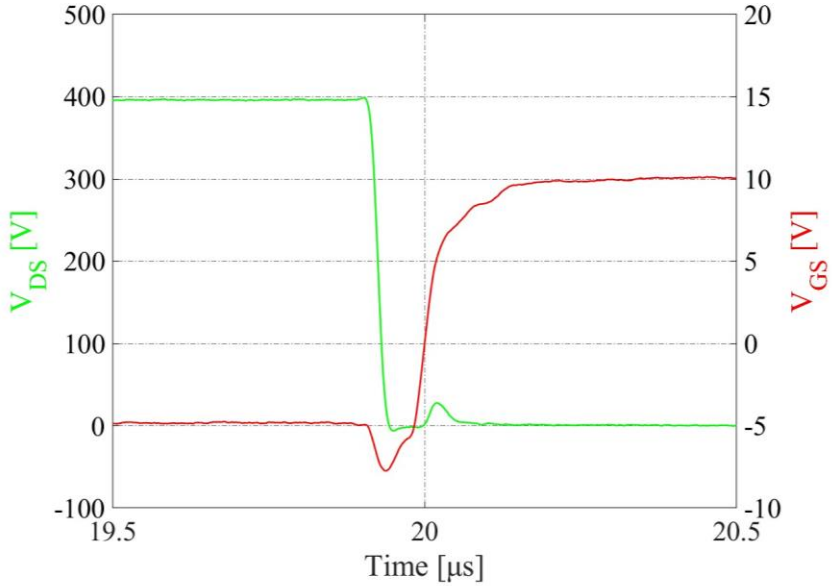

Figure 5.26 : Zoomed view of V_{DS} in green and V_{GS} in red of leading leg switch S_1 at 150 A load current during turn-on.

V_{DS} waveforms with V_{GS} of S_4 are shared in Figure 5.27. Zoomed waveforms of V_{DS} and V_{GS} can be seen during the turn-on transition in Figure 5.28. It can be observed that ZVS can be achieved 150 A load current.

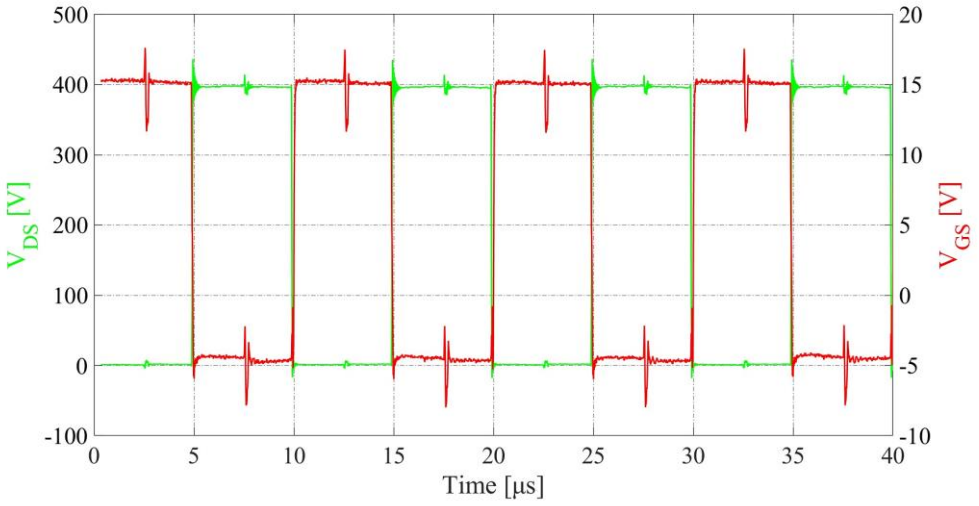

Figure 5.27 : V_{DS} in green and V_{GS} in red of lagging leg switch S_4 at 150 A load current.

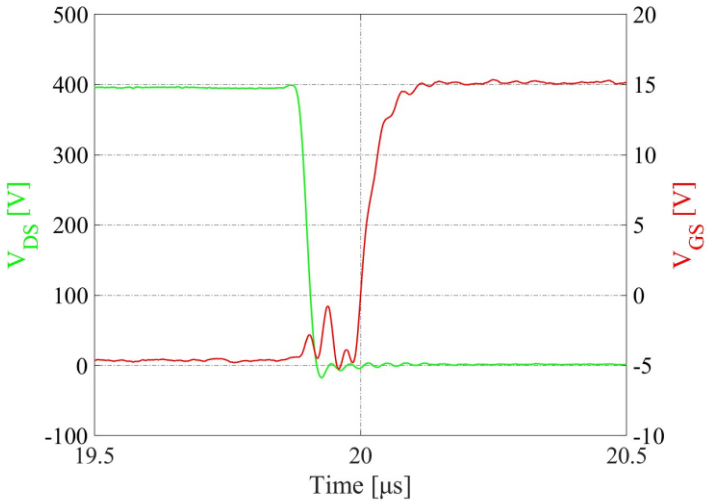

Figure 5.28 : Zoomed view of V_{DS} in green and V_{GS} in red of lagging leg switch S_4 at 150 A load current during turn-on.

V_{DS} waveforms with V_{GS} of S_{SR1} are shared in Figure 5.29. Zoomed waveforms of V_{DS} and V_{GS} can be seen in Figure 5.30 during the turn-off transition. It can be observed that ZCS can be achieve.

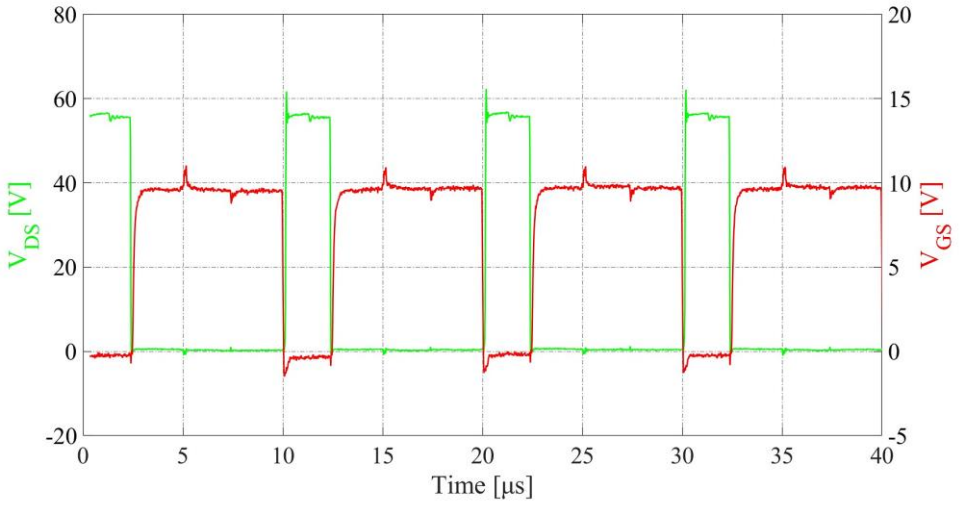

Figure 5.29 : V_{DS} in green and V_{GS} in red of S_{SR1} at 150 A load current.

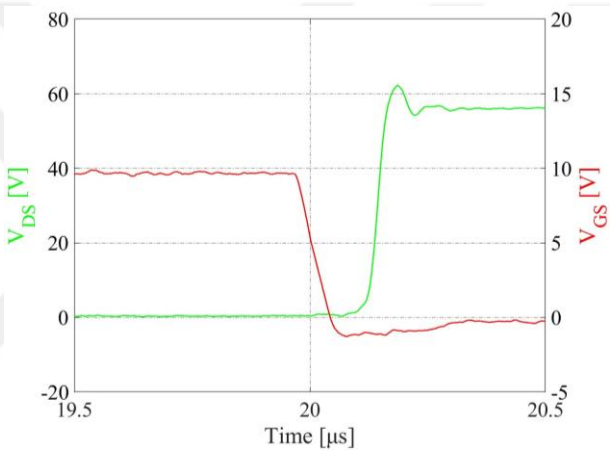

Figure 5.30 : Zoomed view of V_{DS} in green and V_{GS} in red of S_{SR1} at 150 A load current during turn-off.

Transformer primary V_{pri} and secondary side voltage V_{sec} waveform, and primary side current I_{pri} are shared in Figure 5.31.

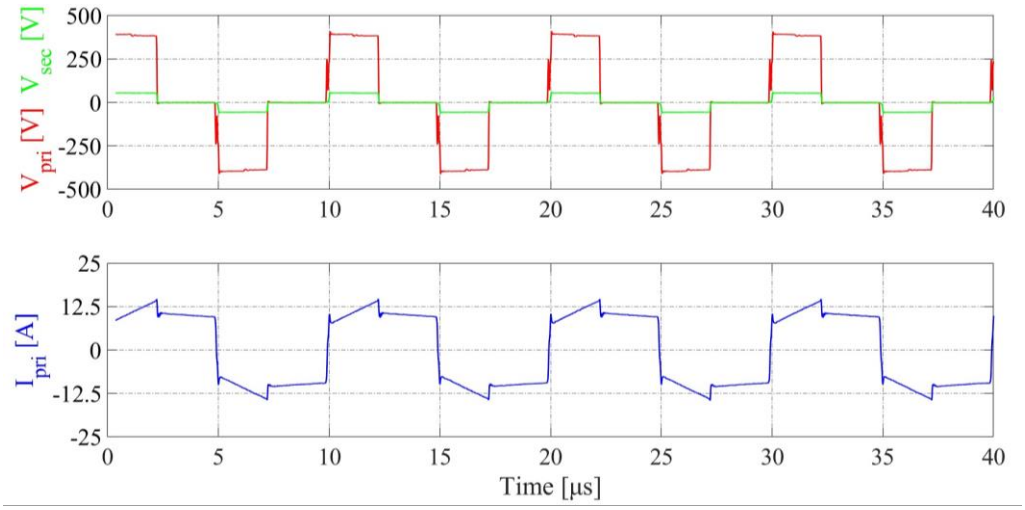

Figure 5.31 : V_{pri} in red, V_{sec} in green and I_{pri} in blue at 150 A load current.

Waveforms of input voltage V_{in} and current I_{in} are given in Figure 5.32. V_{in} is measured as 397.2 V and I_{in} is measured as 4.909 A from the oscilloscope.

Waveforms of output voltage V_{out} and current I_{out} are given in Figure 5.33. V_{out} is measured as 12.39 V amd I_{out} is measured as 149.8 A from the oscilloscope.

According to this measurement, efficiency is calculated as 95.19% for this operating condition.

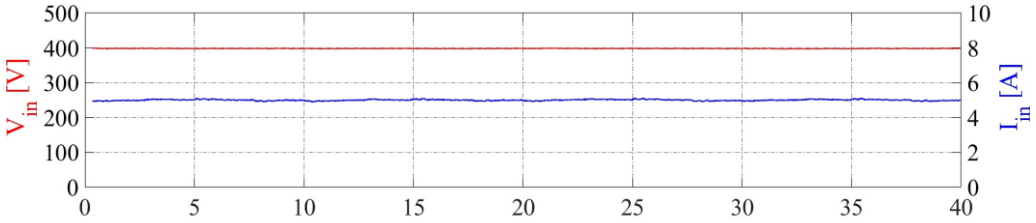

Figure 5.32 : V_{in} in red and I_{in} in blue at 150 A load current.

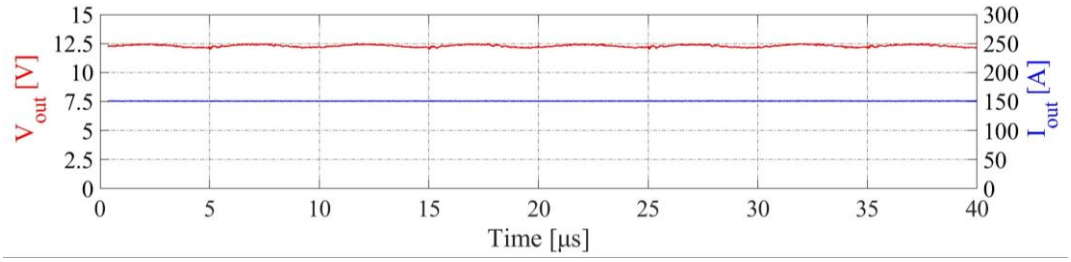

Figure 5.33 : V_{out} in red and I_{out} in blue at 150 A load current.

5.2.4 Experimental results at 200 A load current

The experimental results of designed and implemented PSFB with CDR converter, are shared for 200 A load current operation.

V_{DS} waveforms with V_{GS} of S_1 are shared in Figure 5.34. Zoomed waveforms of V_{DS} and V_{GS} can be seen during turn-on transition in Figure 5.35. It can be observed that ZVS at 200 A load current. V_{GS} is decreased to -10 V because of a sudden voltage change at the source of S_1. Switch can be able to overcome this situation according to datasheet information.

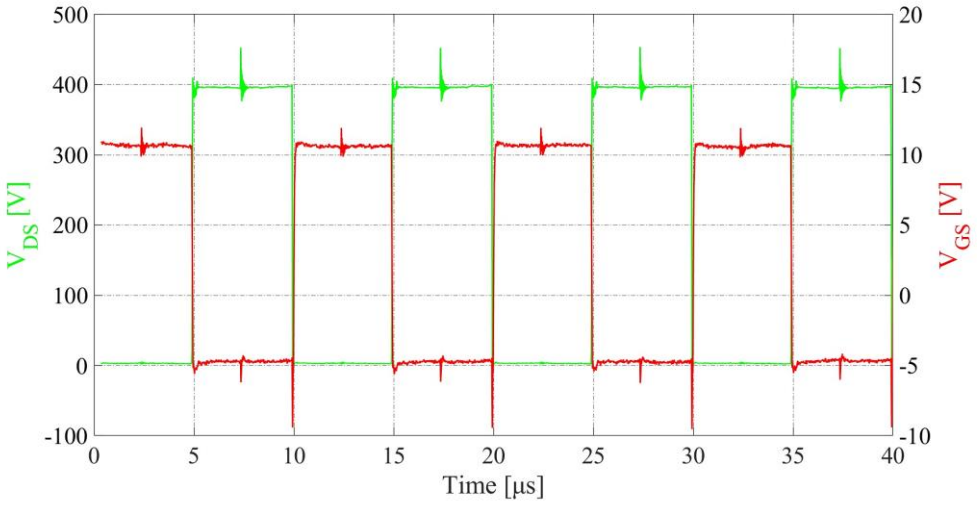

Figure 5.34 : V_{DS} in green and V_{GS} in red of leading leg switch S_1 at 200 A load current.

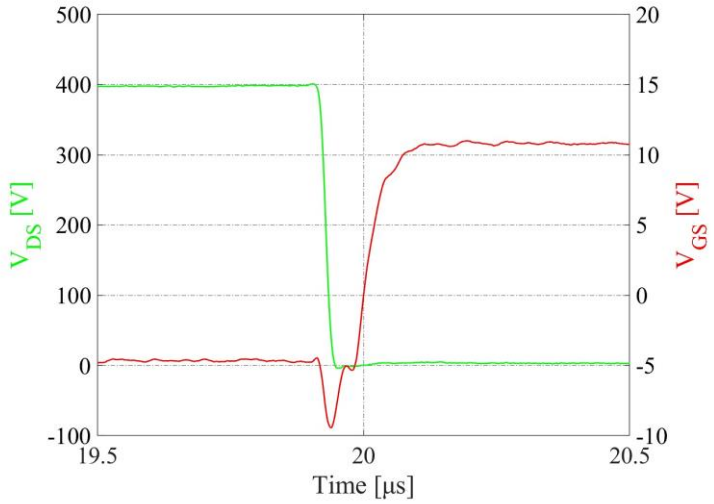

Figure 5.35 : Zoomed view of V_{DS} in green and V_{GS} in red of leading leg switch S_1 at 200 A load current during turn-on.

V_{DS} waveforms with V_{GS} of S_4 are shared in Figure 5.36. Zoomed waveforms of V_{DS} and V_{GS} can be seen during the turn-on transition in Figure 5.37. It can be observed that ZVS at 200 A load current.

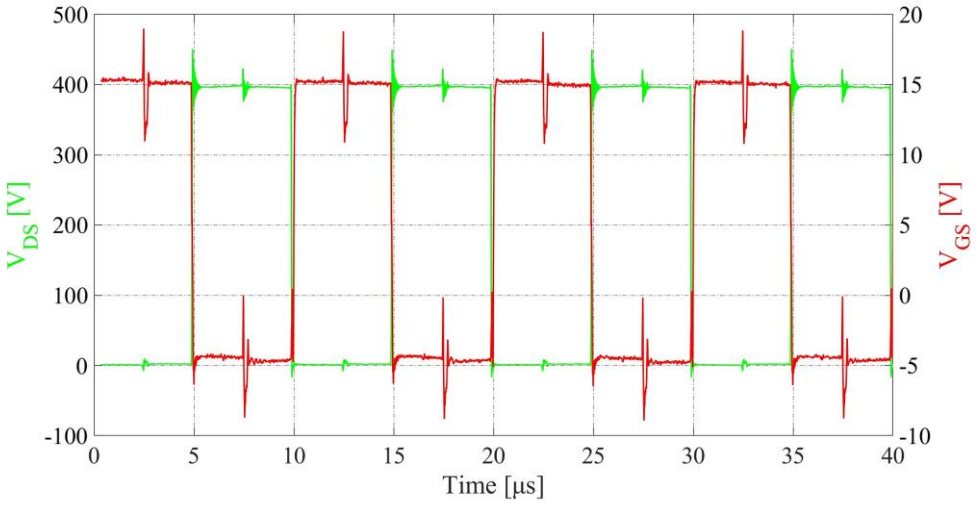

Figure 5.36 : V_{DS} in green and V_{GS} in red of lagging leg switch S_4 at 200 A load current.

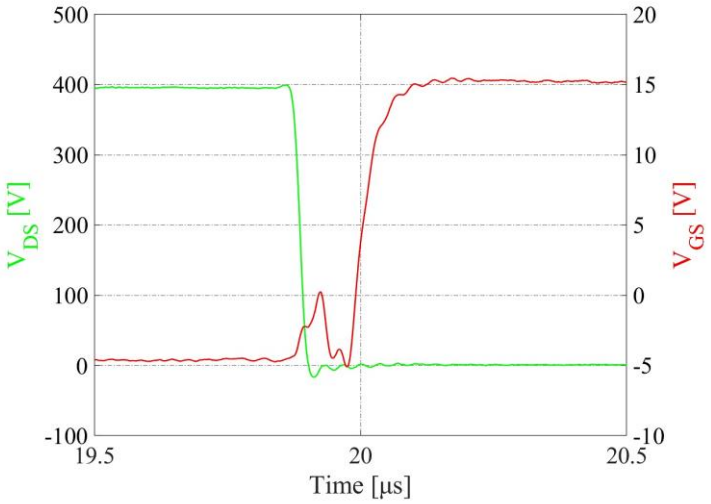

Figure 5.37 : Zoomed view of V_{DS} in green and V_{GS} in red of lagging leg switch S_4 at 200 A load current during turn-on.

V_{DS} waveforms with V_{GS} of S_{SR1} are shared in Figure 5.38. Zoomed waveforms of V_{DS} and V_{GS} can be seen during the turn-off transition in Figure 5.39. It can be observed that ZCS can be achieve.

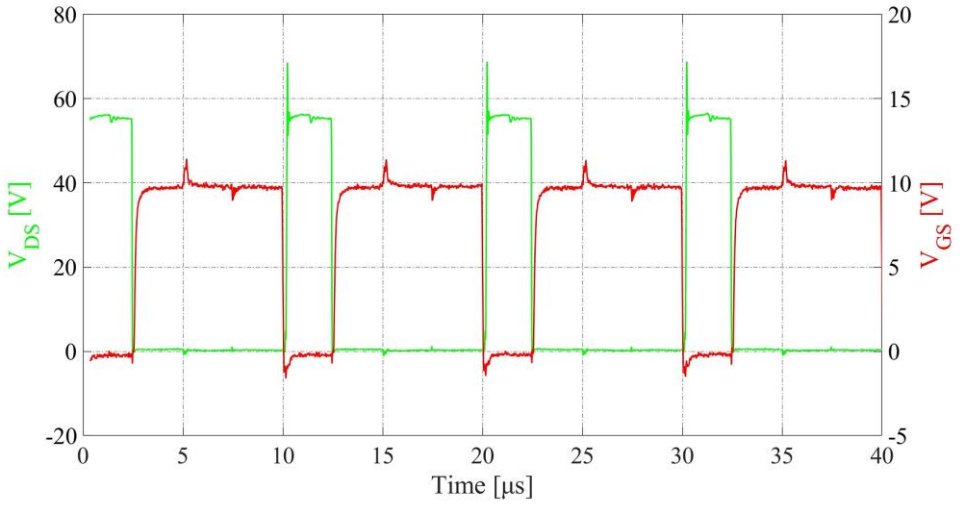

Figure 5.38 : V_{DS} in green and V_{GS} in red of S_{SR1} at 200 A load current.

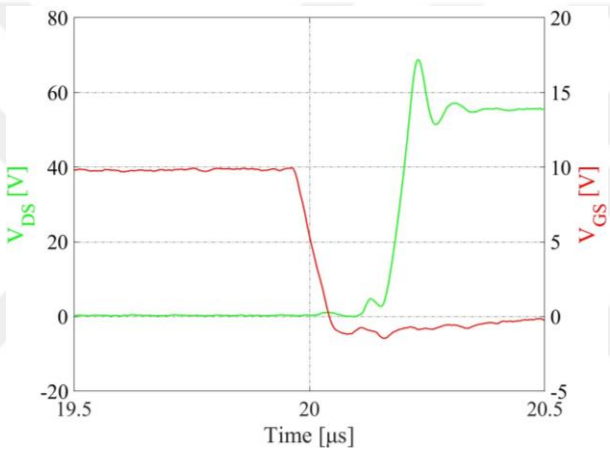

Figure 5.39 : Zoomed view of V_{DS} in green and V_{GS} in red of S_{SR1} at 200 A load current during turn-off.

Transformer primary V_{pri} and secondary side voltage V_{sec} waveform, and primary side current I_{pri} are shared in Figure 5.40.

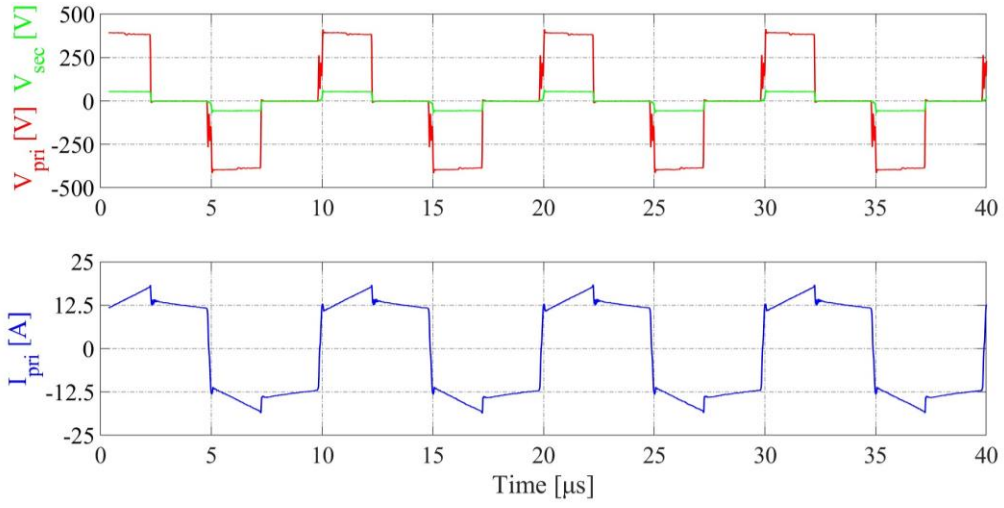

Figure 5.40 : V_{pri} in red, V_{sec} in green and I_{pri} in blue at 200 A load current.

Waveforms of input voltage V_{in} and current I_{in} are given in Figure 5.41. V_{in} is measured as 398.4 V and I_{in} is measured as 6.568 A from the oscilloscope.

Waveforms of output voltage V_{out} and current I_{out} are given in Figure 5.42. V_{out} is measured as 12.35 V and I_{out} is measured as 200.8 A from the oscilloscope.

According to this measurement, efficiency is calculated as 94.77% for this operating condition.

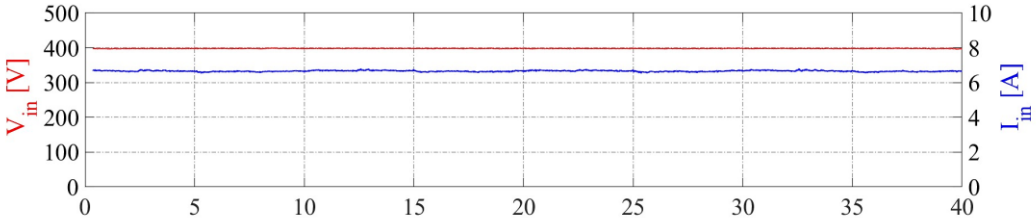

Figure 5.41 : V_{in} in red and I_{in} in blue at 200 A load current.

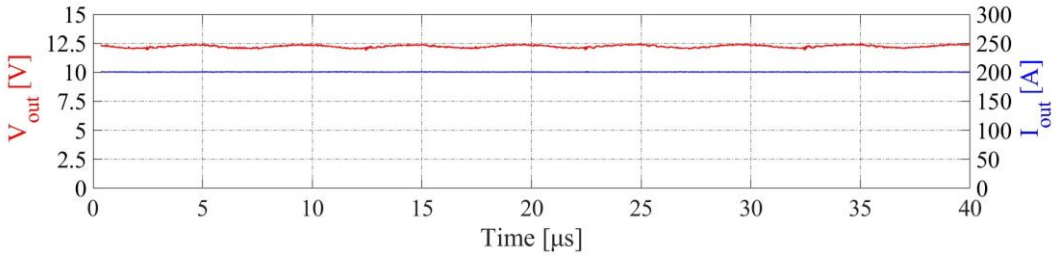

Figure 5.42 : V_{out} in red and I_{out} in blue at 200 A load current.

5.2.5 Experimental results at 250 A load current

The experimental results of designed and implemented PSFB with CDR converter, are shared for 250 A load current operation.

V_{DS} waveforms with V_{GS} of S_1 are shared in Figure 5.43. Zoomed waveforms of V_{DS} and V_{GS} can be seen during the turn-on transition in Figure 5.44. It can be observed that ZVS at 250 A load current. In addition, the zoomed waveform of V_{DS} and V_{GS} can be seen during the turn-off transition in Figure 5.45. Moreover, hard switching can be monitored because of the miller region existence at this operating point especially.

The maximum peak value of V_{DS} is observed as 460.3 V. The breakdown voltage rating of the primary side switches are 750 V, thus this peak value is not a problem at this operating point which is the worst case.

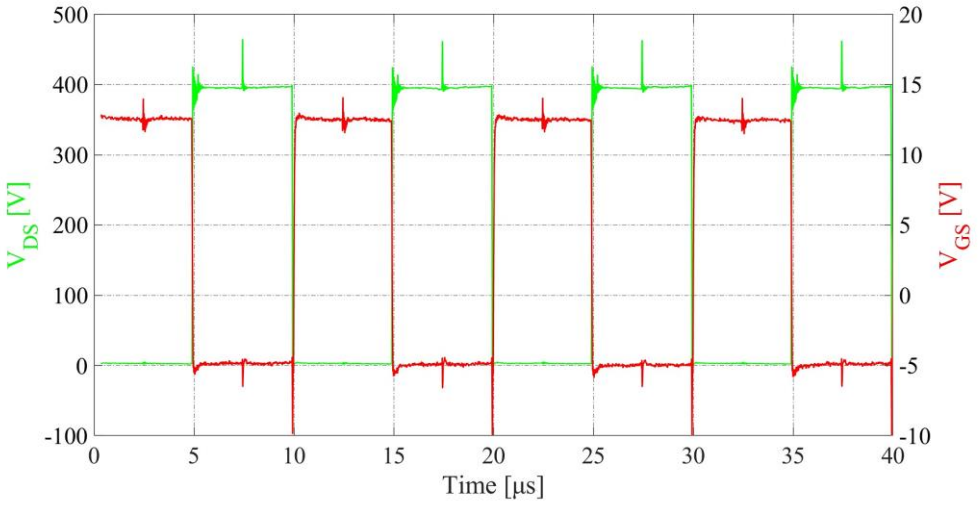

Figure 5.43 : V_{DS} in green and V_{GS} in red of leading leg switch S_1 at 250 A load current.

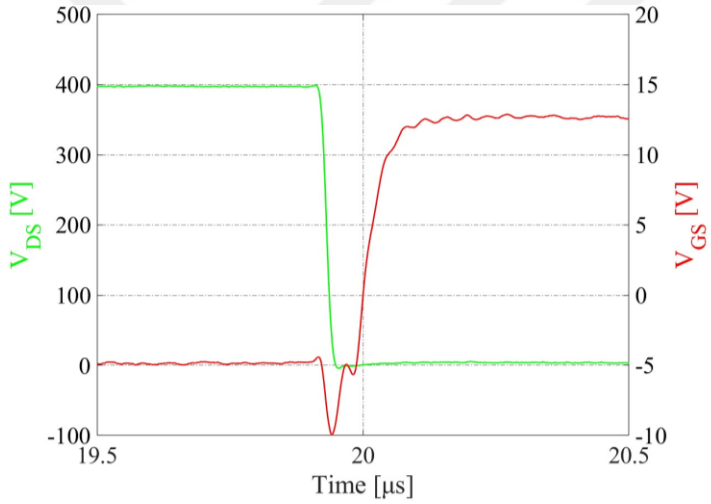

Figure 5.44 : Zoomed view of V_{DS} in green and V_{GS} in red of leading leg switch S_1 at 250 A load current during turn-on.

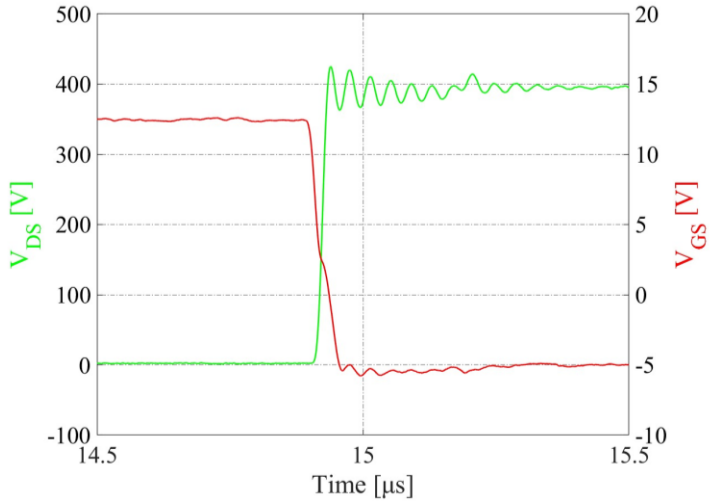

Figure 5.45 : Zoomed view of V_{DS} in green and V_{GS} in red of leading leg switch S_1 at 250 A load current during turn-off.

V_{DS} waveforms with V_{GS} of S_4 are shared in Figure 5.46. Zoomed waveforms of V_{DS} and V_{GS} can be seen during the turn-on transition in Figure 5.47. It can be observed that ZVS at 250 A load current.

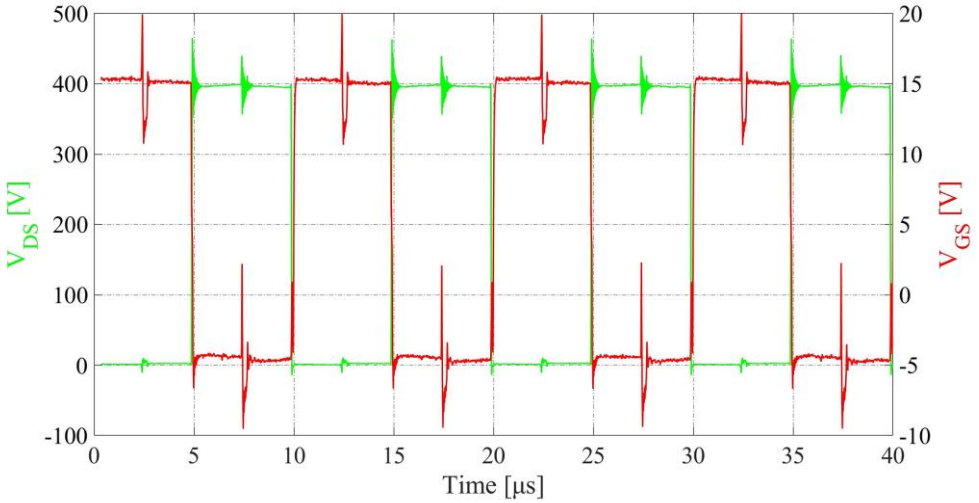

Figure 5.46 : V_{DS} in green and V_{GS} in red of lagging leg switch S_4 at 250 A load current.

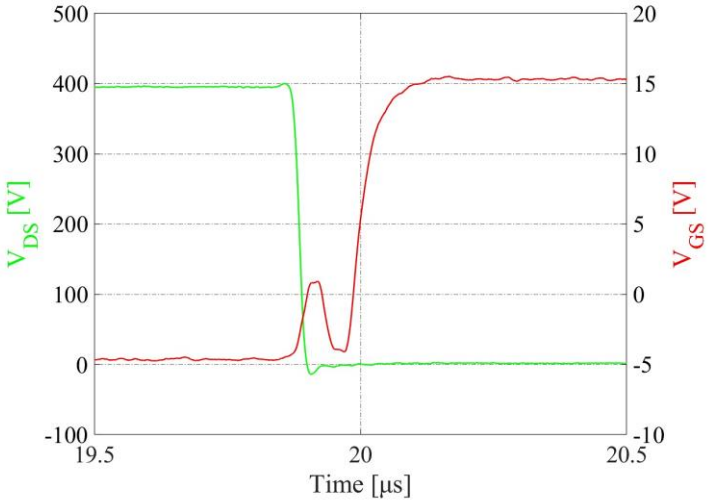

Figure 5.47 : Zoomed view of V_{DS} in green and V_{GS} in red of lagging leg switch S_4 at 250 A load current during turn-on.

V_{DS} waveforms with V_{GS} of S_{SR1} are shared in Figure 5.48. Zoomed waveforms of V_{DS} and V_{GS} can be seen during the turn-off transition in Figure 5.49. It can be observed that ZCS can be achieve.

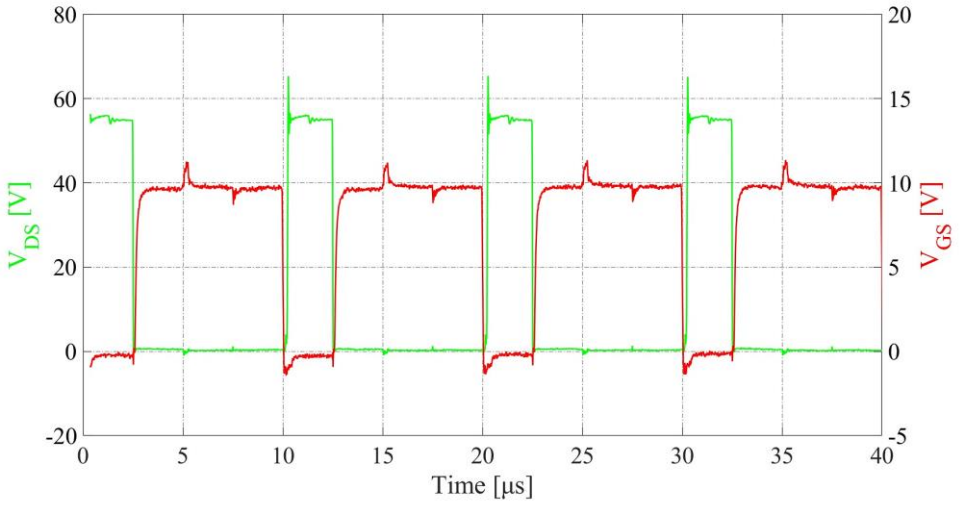

Figure 5.48 : V_{DS} in green and V_{GS} in red of S_{SR1} at 250 A load current.

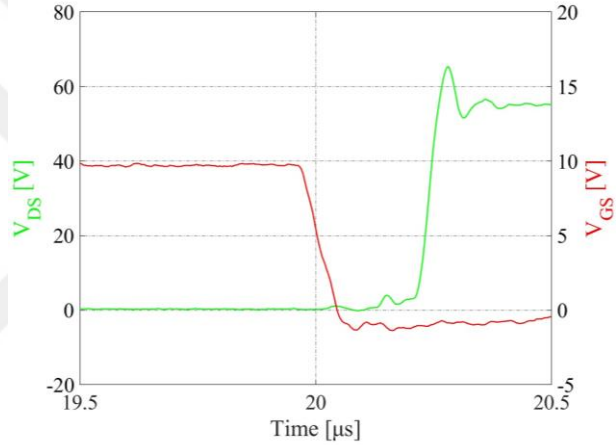

Figure 5.49 : Zoomed view of V_{DS} in green and V_{GS} in red of S_{SR1} at 250 A load current during turn-off

Transformer primary V_{pri} and secondary side voltage V_{sec} waveform, and primary side current I_{pri} are shared in Figure 5.50. Moreover, duty cycle loss which is explained in chapter 3.2.2 in detail, can be observed in Figure 5.51. Voltage of the transformer secondary side is zero during direction change of transformer primary side current, on the contrary of voltage of transformer primary side. Duty cycle loss time is measured as 250 ns.

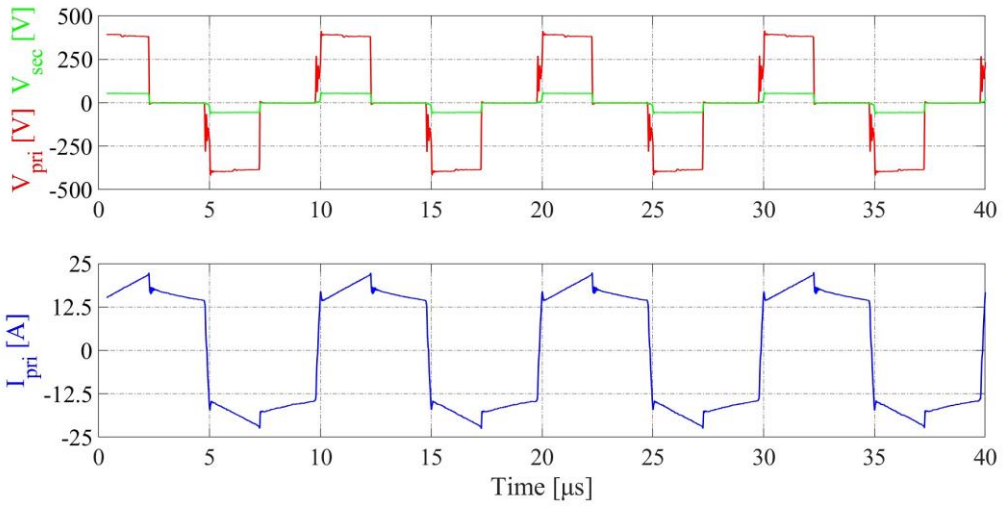

Figure 5.50 : V_{pri} in red, V_{sec} in green and I_{pri} in blue at 250 A load current.

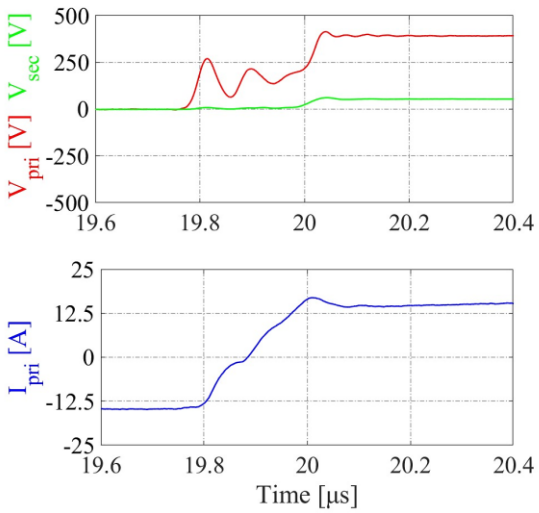

Figure 5.51 : Zoomed view of V_{pri} in red, V_{sec} in green and I_{pri} in blue at 250 A load current duty cycle loss.

Waveforms of input voltage V_{in} and current I_{in} are given in Figure 5.52. V_{in} is measured as 398 V and I_{in} is measured as 8.296 A from the oscilloscope.

Waveforms of output voltage V_{out} and current I_{out} are given in Figure 5.53. V_{out} is measured as 12.28 V and I_{out} is measured as 251.2 A from the oscilloscope.

According to this measurement, efficiency is calculated as 93.43% for this operating condition.

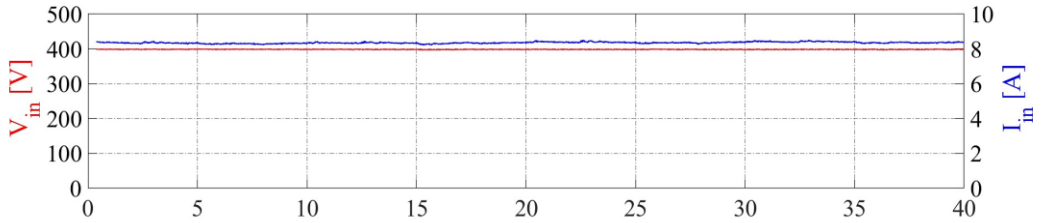

Figure 5.52 : V_{in} in red and I_{in} in blue at 250 A load current.

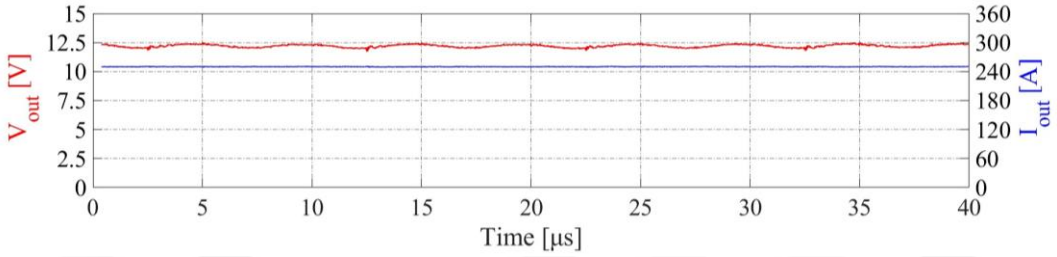

Figure 5.53 : V_{out} in red and I_{out} in blue at 250 A load current.

Zoomed output voltage ripple is shared to observe the amount of ripple in Figure 5.54. Output voltage ripple is measured as 315.719 mV from the oscilloscope. This value is higher than calculation, since the capacitance value of ceramic capacitor is changed according to the DC bias value. The capacitance value of the selected capacitor decreases down to 43.9% of its initial value.

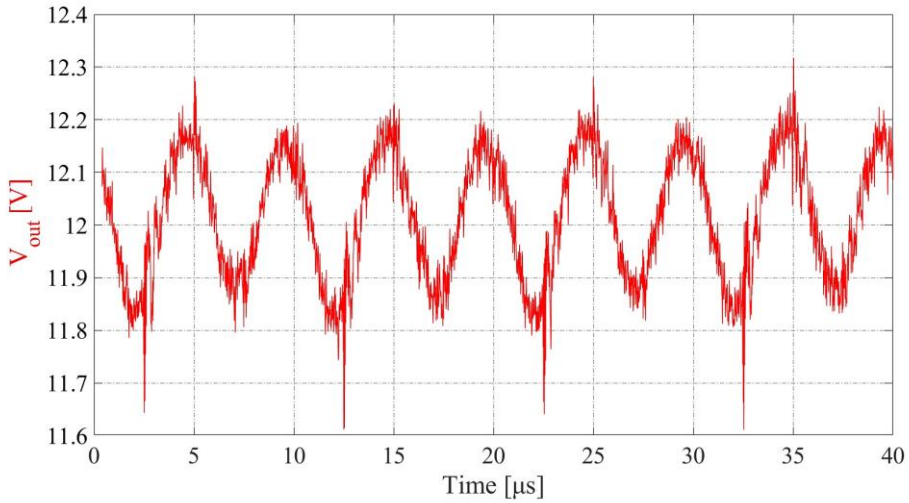

Figure 5.54 : Zoomed view of output voltage at 250 A load current.

5.3 Evaluation of Experimental Results of PSFB with CDR Converter

In this section, the obtained results at each operating point are evaluated.

It can be observed that V_{DS} and V_{GS} spikes of all switches during the end of the power transfer and freewheeling operating periods are increased with increasing load current.

The reason for this issue is that the di/dt ratio over traces inductance increases with increasing load current.

Another slight voltage peak is monitored during the turn-on state of leading leg switches. This does not mean that ZVS does not occur for this operating point. Different deadtime value is required for different load currents for PSFB with a CDR converter as a solution to this phenomenon. Less deadtime is necessary for less loaded conditions. When the load current is increased, this peak disappears. However, deadtime is fixed in this study.

It can be seen that ZVS for both leg switches is achieved after 100 A. The effect of starting ZVS can be observed in the efficiency.

Duty cycle loss time is increasing with increasing load current. It can be observed from primary and secondary voltage waveforms. Maximum duty cycle loss time is measured as 250 ns at 250 A load operation.

In addition, the output voltage ripple is measured as 315.719 mV at 250 A load operation. This ripple value is higher than the analytic calculation due to a drop in capacitance value with applied voltage over capacitors.

Efficiencies at each test operating point from simulation and experimental results are shared in Figure 5.55. Maximum efficiency is 95.19% at the 150 A load current condition. Minimum efficiency is 87.12% at the 50 A load current condition since ZVS can not be achieved in the leading leg. Moreover, the losses are dominant in the total power rating.

Efficiency at the maximum load current, which is 250 A, is measured as 93.43%. Efficiency decreases with increasing load current after 150 A load current since conduction losses increase with the square of load current.

When the results are compared with similar studies in the literature, maximum efficiency is 95.5% at the half-loaded condition with the same converter topology in [58]. However, efficiency is 90.4% at maximum load operation, which is 1.2 kW. In another converter, which has the same topology in [59], the maximum efficiency is 94% at the 70% loaded condition. Efficiency is 93.2% at 2 kW full-loaded operation. In [60], the maximum efficiency of PSFB with a CDR converter is 93.5% at 60% loaded condition. Moreover, efficiency is 93% at 2 kW, which is the maximum power rating of the converter.

Efficiency difference is seen between simulation and experimental results. The measured efficiency from the simulation at higher load current values is higher tthan the experimental results due to neglected conduction losses in PCB and thermal effects on the components. Moreover, reason of efficiency difference at lighter load operating condition is that component tolerances and inductance changes depend on the current values can not be modelled in simulation.

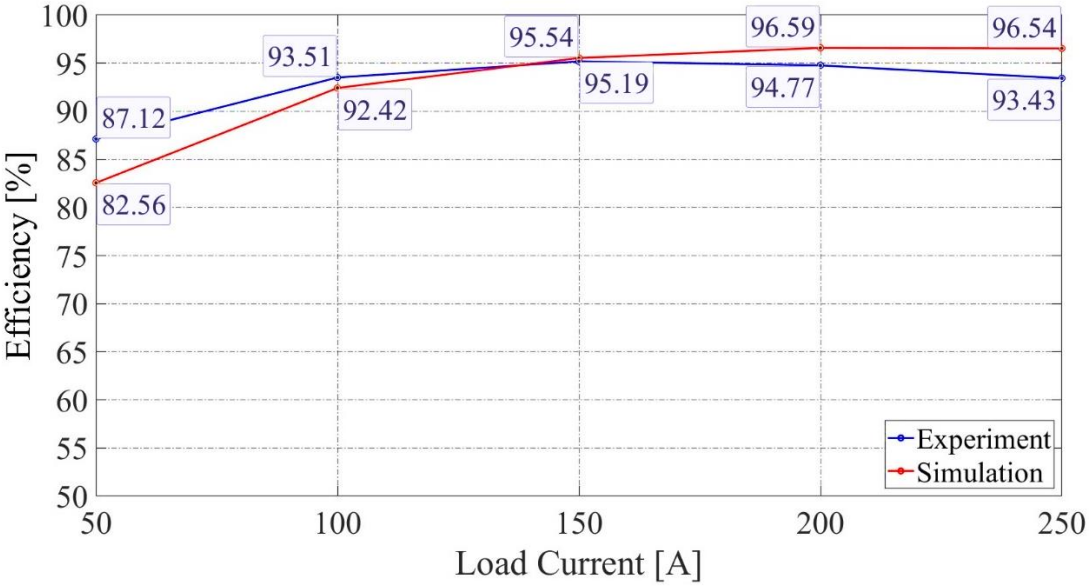

Figure 5.55 : Measured efficiency curve of PSFB with CDR converter from experiment and simulation.

6. CONCLUSIONS AND RECOMMENDATIONS

In this thesis, several unidirectional isolated converters and rectification configurations are evaluated in terms of the suitability of the HV to LV battery charger requirement in EV applications. The selected converter has to provide soft-switching operations, operate with a wide voltage gain range, carry high output current, and be feasible in size and power density. A phase-shifted full-bridge with a current doubler converter is selected as the most convenient option due to having a wide voltage gain range, low output current ripple, operation with constant switching frequency, and ZVS capability without any additional auxiliary components features. Moreover, CDR provides conduction loss reduction, thermal management improvement, simpler transformer structure, and ripple current cancellation capability to the converter.

The operating principle of PSFB with CDR converter and its operating modes related to the switching sequences are explained in detail. The PWM method is quite critical for converter operation and accomplishment of the ZVS. Detailed waveforms which belong to each operating mode are shared.

Comprehensive analytical calculations to design PSFB with CDR converter are shared. Calculations are given about the main components which are primer and seconder side switches, transformer, shim and output inductor, and input and output capacitor according to specified operating conditions. Moreover, calculations that affect the operation of the converter such as effective duty cycle, deadtime, duty cycle loss time, and ZVS condition are shared. Detailed design and calculations are also given about magnetic components. Regarding the obtained results, components are selected, sized, and manufactured if needed to ensure the proper operation of the converter.

Another essential part of the converter design is the control method. The selected control method has to be convenient for the converter operation principle. In this thesis, peak current mode control is applied as the control method to have cycle-by-cycle current protection and prevent transformer saturation. PCMC is digitally implemented with a microcontroller, which is TMS320F280048, from the C2000 family of Texas Instruments. Detailed information about the implementation of

PCMC to the microcontroller is given. The transfer function of PSFB with CDR converter is obtained with the small signal analysis. Acquired transfer functions are implemented in MATLAB/Simulink to design the controller, which is selected as PI. Compensator parameters are identified with the help of the response optimizer tool of MATLAB/Simulink. Both open-loop and closed-loop responses and bode diagrams are given. Moreover, the transformation of compensator parameters from the s-domain to the z-domain is applied to make it suitable for microcontroller implementation.

PSFB with CDR converter is simulated in LTspice with the implemented model of the selected component and their calculated values. Simulation is done with the nominal operating condition which is the input voltage as 400 V and output voltage as 12 V. Output load is changed step by step from 50 A to 250 A. Current waveforms of shim inductor, output inductors and clamping diodes; voltage and current waveforms of the transformer, output load, and leading and lagging leg switch are given in detail. Efficiencies are measured and given for each operating condition. Moreover, the effect of the clamping diode over voltage waveforms and efficiency is evaluated and observed. The efficiency difference between operating with and without clamping diode is given.

As a following step, technical details of the designed and implemented PSFB with CDR converter are given. Setup information for experimental tests is also shared. Experimental tests are completed at the nominal operation points which is input voltage as 400 V, nominal output voltage as 12 V. Tests are executed at varied load currents which are 50 A, 100 A, 150 A, 200 A, and 250 A. All waveform data sets are obtained from an oscilloscope and drawn in the MATLAB. Several waveforms that belong to PWM, transformer, primary and secondary side switch, input, and output are given in detail for each operating condition. Waveforms that enable the observation of ZVS behavior are also shared. Waveforms which related to the duty cycle loss and output voltage waveform ripple are given at 250 A loaded condition. The efficiency of each operating point is calculated.

The efficiency from the simulation is measured as 96.54% at the nominal operating point at maximum power. As a result of the experiment, efficiency is measured as 93.43% at the same operating condition. The reason for the efficiency difference between the simulation and experiment at a higher load current is that conduction losses in PCB and thermal effects on the components are disregarded in the simulation.

Peak efficiency is measured as 95.19% at 150 A load current from the experiment. It can be observed that efficiency decreases with increasing load current after 150 A load current, since conduction losses become more dominant than light-loaded operation. The high compatibility of waveforms and their values from simulation and experiment is observed. Moreover, analytical calculations are coherent with the simulation and experimental results. Another important output in this thesis is power density, which is 1.87 kW/L. This value is high and quite satisfactory when compared with the 1.2 kW/L, which is the average power density value of 13 different manufacturers' converters [8]. The reasons for achieving this high power density are use of appropriately sized busbars for high output current and the planar transformers. In addition, the use of top side cooled switches provides better thermal performance and therefore minimizes the need for parallel switch usage.

Overall; all analytical calculations, control method, simulation model and results, implemented design details, and experimental results are given for PSFB with CDR converter in this thesis. Results provide useful technicality not only for electric vehicle applications but also for these kinds of applications such as required wide voltage gain, high efficiency, high power density, and capability to carry high current.

As a future work, adaptive deadtime, which changes with load current, can be implemented to achieve high efficiency. Moreover, new PCB can be designed to increase efficiency at higher currents with lower conduction losses. According to technological advances and demands of the automotive industry, the bidirectional operation can be evaluated for future design. In addition, input voltage can be increased up to 800 V for the next generation of HV battery architecture for EVs.

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APPENDICES

APPENDIX A: Datasheets

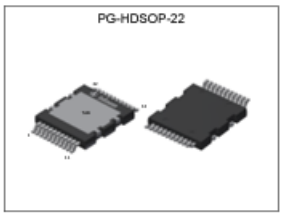
APPENDIX A

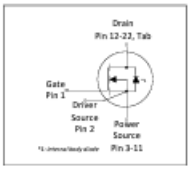
AIMDQ75R040M1H

MOSFET

CoolSiC™ Automotive Power Device 750 V G1

The 750 V CoolSiC™ is built over the solid silicon carbide technology developed in Infineon in more than 20 years. Leveraging the wide bandgap SiC material characteristics, the 750V CoolSiC™ MOSFET offers a unique combination of performance, reliability and ease of use. Suitable for high temperature and harsh operations, it enables the simplified and cost effective deployment of the highest system efficiency.





Features

- Highly robust 750V technology, 100% avalanche tested
- Best-in-class $R_{DS(on)}$ x Q_{fr}
- Excellent $R_{DS(on)}$ x Q_{oss} and $R_{DS(on)}$ x Q_G
- Unique combination of low C_{rss}/C_{iss} and high $V_{GS(th)}$
- Infineon proprietary die attach technology
- Cutting edge top side cooling package (QDPAK)
- Driver source pin available

Benefits

- Enhanced robustness and reliability for bus voltages beyond 500 V
- Superior efficiency in hard switching
- Higher switching frequency in soft switching topologies
- Robustness against parasitic turn on for unipolar gate driving
- Best-in-class thermal dissipation
- Reduced switching losses through improved gate control

Potential applications

Uni- and bidirectional On Board Chargers and HV-LV DCDC converters:
- hard switching half bridges
- soft switching topologies

AEC Qualified RoHS

Product validation

Qualified according to AEC Q101

Please note: The source and driver source pins are not exchangeable. Their exchange might lead to malfunction.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DSS} over full $T_{j,range}$	750	V
$R_{DS(on),typ}$	40	mΩ
$R_{DS(on),max}$	52	mΩ
$Q_{G,typ}$	34	nC
$I_{DM,max}$	134	A
$Q_{oss,typ}$ @ 500 V	68	nC
$E_{oss,typ}$ @ 500 V	12.2	µJ

Type / Ordering Code	Package	Marking	Related Links
AIMDQ75R040M1H	PG-HDSOP-22	75A040M1	see Appendix A

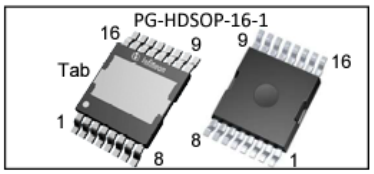
Figure A.1 : Datasheet of AIMDQ75R040M1H.

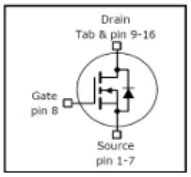
IAUTN12S5N018T

Automotive MOSFET

OptiMOS™ 5 Power-Transistor

RoHS Infineon Automotive Quality AEC Qualified





Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – enhancement mode – normal level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% avalanche tested
- Very low reverse recovery charge (Q_{rr})

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.

Product Summary

V_{DS}	120	V
$R_{DS(on)}$	1.8	mΩ
I_D (chip limited)	309	A

Type	Package	Marking
IAUTN12S5N018T	PG-HDSOP-16-1	5N12N018

Figure A.2 : Datasheet of IAUTN12S5N018T.

B32774P

MKP DC link – 125 °C series up to 50 µF

Ordering codes and packing units (lead spacing 27.5 mm)

C_R [1] µF	Max. dimensions w × h × l mm	Ordering code (composition see below)	$I_{RMS,max}$ [2] 85 °C 10 kHz A	ESR_{typ} 10 kHz mΩ	ESL_{typ} [3] nH	tan δ max. 1 kHz 10^{-3}	tan δ max. 10 kHz 10^{-3}	Untaped pcs./ MOQ
$V_{R,85\,°C}$ = 630 V DC								
1.5	11.0 × 19.0 × 31.5	B32774P6155+000	3.5	22.3	13.2	0.5	3.5	1280
2.2	12.5 × 21.5 × 31.5	B32774P6225+000	4.7	15.5	14.5	0.5	3.5	1120
3.0	14.0 × 24.5 × 31.5	B32774P6305+000	6.0	11.5	16.1	0.5	3.5	1040
4.7	18.0 × 27.5 × 31.5	B32774P6475+000	8.2	7.6	18.7	0.5	3.7	800
6.8	21.0 × 31.0 × 31.5	B32774P6685+000	10.4	5.4	21.3	0.6	3.9	720
8.0	22.0 × 36.5 × 31.5	B32774P6805+000	12.0	4.5	24.0	0.6	4.0	640
$V_{R,85\,°C}$ = 700 V DC								
1.5	11.0 × 19.0 × 31.5	B32774P7155+000	3.6	20.3	18.4	0.5	3.2	1280
2.0	12.5 × 21.5 × 31.5	B32774P7205+000	4.7	15.3	19.8	0.5	3.2	1120
3.3	18.0 × 27.5 × 31.5	B32774P7335+000	7.3	9.6	22.9	0.5	3.3	800
4.7	19.0 × 30.0 × 31.5	B32774P7475+000	9.0	6.9	25.8	0.5	3.4	720
7.0	22.0 × 36.5 × 31.5	B32774P7705+000	11.8	5.0	31.2	0.5	3.7	640
$V_{R,85\,°C}$ = 840 V DC								
1.0	11.0 × 19.0 × 31.5	B32774P8105+000	3.3	25.2	18.3	0.5	2.7	1280
1.5	12.5 × 21.5 × 31.5	B32774P8155+000	4.4	17.2	20.2	0.5	2.7	1120
3.0	18.0 × 27.5 × 31.5	B32774P8305+000	7.5	9.1	25.6	0.5	2.8	800
5.0	22.0 × 36.5 × 31.5	B32774P8505+000	12.5	5.8	31.6	0.5	3.0	640

MOQ = Minimum Order Quantity, consisting of 4 packing units.
Intermediate capacitance values are available on request.

Composition of ordering code

+ = Capacitance tolerance code:
K = ±10%
J = ±5%

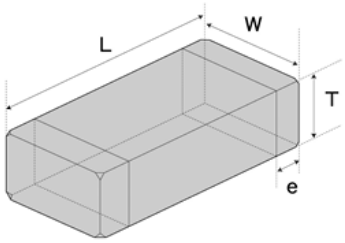
Packing code:
000 = untaped (lead length 6 – 1 mm)
Other lead lengths available upon request

Figure A.3 : Datasheet of B32774P7335K.

Spec Sheet

Soft Termination Multilayer Ceramic Capacitors for Automotive Body & Chassis and Infotainment

MCJCU32MLB7106KPPDT1 (Previous PN: UMJ325KB7106KMHP)



Features

- Item Summary
  10uF±10%, 50V,
  X7R, 1210/3225 (EIA/JIS)
- Lifecycle Stage
  Mass Production (Preferred)
- AEC-Q200 qualified
- Standard packaging quantity (minimum)
  Taping Embossed 1000pcs

Products characteristics table

Capacitance	10 uF ± 10 %
Case Size (EIA/JIS)	1210/3225
Rated Voltage	50 V
tan δ (max)	10 %
Temperature Characteristic (EIA)	X7R
Operating Temp. Range (EIA)	-55 to +125 ℃
Insulation Resistance (min)	100 MΩ·μF
RoHS Compliance (10 subst.)	Yes
REACH Compliance (235 subst.)	Yes
Halogen Free	Yes
Soldering	Reflow

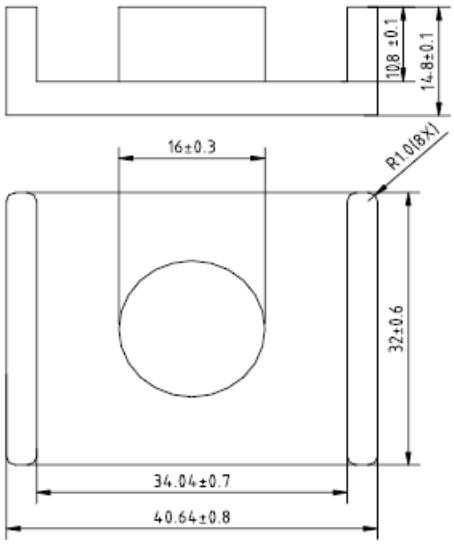
External Dimensions

Dimension L	3.2 ±0.50 mm
Dimension W	2.5 ±0.30 mm
Dimension T	2.5 ±0.30 mm
Dimension e	0.60 +0.4/-0.3 mm

Figure A.4 : Datasheet of MCJCU32MLB7106KPPDT1.

FERROXCUBE

Product Drawing and Specification



Magnetic dimensions according to IEC 60205

Ae : 221mm²	Amin : 201mm²	Le : 83.2	Ve :18400 mm³	Weight≈g/pcs

Electrical Specifications

Property	Specification	Unit	Test Conditions			
			Frequency (kHz)	Induction (mT)	Temperature (°C)	Field strength (A/m)
A_L	**5500±25%**	nH/N²	10	0.1V	25±3	----
Bs	**≥340**	mT	25	----	100	250
Pv	**≤8.832**	W/Set	100	200	100	----

Note:AL is measured with Ferroxcube standard bobbin 10turns Φ0.65mm.

ROUGHNESS	UNIT	SCALE	PROJ EUROP	UN-D 28	TOLERANCES: UNLESS OTHERWISE STATED DIMENSION: ACC. TO DIN 406 TEIL 4	UN-D 603
	mm	2:1		Ra in mikron(µm)		

CORE- FAMILY ER41/14.8/32-3C96	434101110121	V1	2022/1/12

Name:Jinqin Zeng	Check:	Approve:	110 - 02	010	SH 1	A 4

Revision:003 No.:FXC-F-0168

Figure A.5 : Datasheet of Ferroxcube 14.8/32-3C96.

TDK

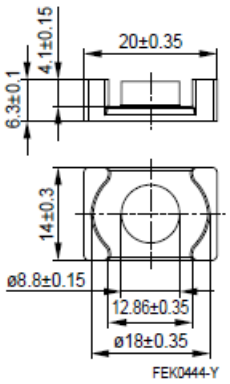
EQ 20/6.3/14

Core **B66483**

Core set EEQ 20
Combination: EQ 20/6.3/14 with EQ 20/6.3/14

- To IEC 63093-9
- Optimized cross section
- Small overall footprint (core and winding)
- Less EMI
- Minimized winding length
- Delivery mode: single units

EQ 20/6.3/14



Magnetic characteristics (per set)

$\Sigma l/A$ = 0.56 mm^{-1}
l_e = 33.2 mm
A_e = 59.0 mm^2
A_{min} = 55.0 mm^2
V_e = 1960 mm^3

Approx. weight 11 g/set

Ungapped

Material	A_L value nH	μ_e	P_V W/set	Ordering code
PC200[1)]	1400 ±25%	630	< 0.90 (50 mT, 1000 kHz, 100 °C) < 1.10 (30 mT, 2000 kHz, 100 °C)	B66483G0000X608
N49	2600 ±25%	1160	< 0.51 (50 mT, 500 kHz, 100 °C)	B66483G0000X149
N92	2600 ±25%	1160	< 1.80 (200 mT, 100 kHz, 100 °C)	B66483G0000X192
N87	3400 ±25%	1520	< 1.10 (200 mT, 100 kHz, 100 °C)	B66483G0000X187
N97	3500 ±25%	1560	< 1.00 (200 mT, 100 kHz, 100 °C)	B66483G0000X197
N95	4100 ±25%	1840	< 1.05 (200 mT, 100 kHz, 100 °C) < 1.20 (200 mT, 100 kHz, 25 °C)	B66483G0000X195

[1)] Preliminary data

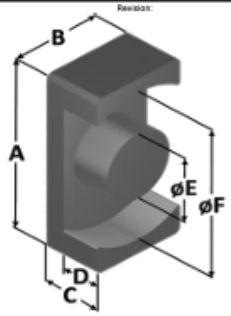
Other A_L values/air gaps and materials available on request – see chapter Processing notes in General Technical Information.

Figure A.6 : Datasheet of TDK EQ 20/6.3/14-N87.

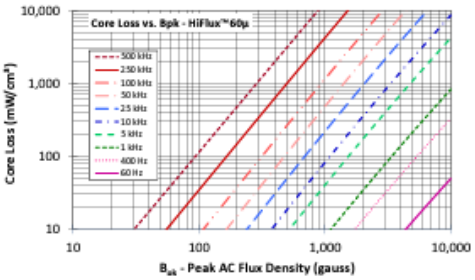
MICROMETALS™
POWDER CORE SOLUTIONS

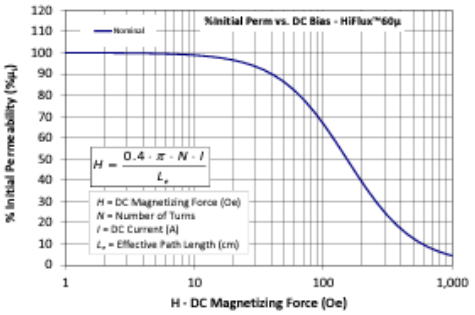
Part Number: EQHF-265190124-060

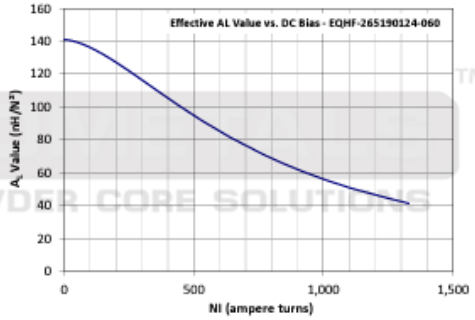
Revision: 2023-Dec-06

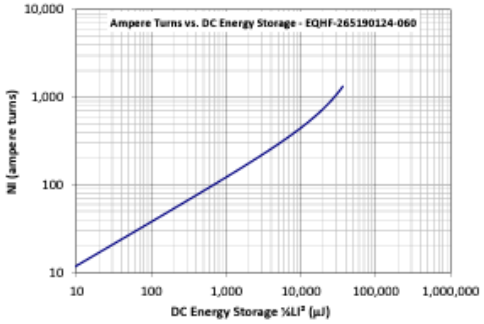


A	26.50 ± 0.30 mm	1.043 ± 0.012 in
B	19.00 ± 0.20 mm	0.748 ± 0.008 in
C	12.40 ± 0.203 mm	0.488 ± 0.008 in
D	8.800 mm (min.)	0.346 in (min.)
E	12.00 ± 0.20 mm	0.472 ± 0.008 in
F	22.30 mm (min.)	0.878 in (min.)
Mass	(approximate)	26 grams/half
Magnetic Dimensions	A_e - Eff. Mag. Cross Section	1.20 cm²
	L_e - Eff. Mag. Path Length	6.39 cm
	V_e - Eff. Core Volume	7.66 cm³
	WA - Min. Eff. Window Area	0.889 cm²
	sa - Surface Area	33.4 cm²
	mlt - mean length per turn	5.39 cm
Inductance	μ(reference)	60
	A_L value (nominal)	141 nH/N²
	Test Winding	N=20, #20 AWG
	Frequency	10 kHz
	Voltage on Agilent 4284A	0.11 V
	A_L tolerance	±12%
Core Loss	Core Loss(mW/cm³)= $\frac{f}{\frac{a}{Bpk^{a}}+\frac{b}{Bpk^{2.3}}+\frac{c}{Bpk^{1.65}}}+d\cdot Bpk^{2}\cdot f^{2}$	
	where B_{pk} expressed in gauss, f expressed in hertz, and:	
	a=8.195E+08, b=7.405E+08, c=2.965E+06, d=3.593E-14	
	B_{pk}	1000 G
	frequency	50 k Hz
	Core Loss (nominal)	483 mW/cm³
	Core Loss (maximum)	555 mW/cm³
DC Saturation	$\%\mu_i = \frac{1}{a+b\cdot H^{c}}+d$	
	where H expressed in oersteds, and:	
	a=1.000E-02, b=2.637E-06, c=1.639, d=0.000	
	H_{DC}	150 Oe
	Percent Initial Perm(nom.)	50.7 %
	Percent Initial Perm(min.)	43.3 %
Coating/Pkg	Coating Type:	None
	Voltage Breakdown (min.)	N/A
	Limit	N/A
	Package Quantity	400 Halves/Box









Winding Table													
Wire Size	AWG	14	16	18	20	22	24	26	28	30	32	34
	mm	1.600	1.250	1.000	0.800	0.630	0.500	0.400	0.315	0.250	0.200	0.160
Full Winding	Turns	18	27	43	66	102	158	244	378	585	905	1,401
	Rdc(Ω)	8.0 m	19.1 m	48.5 m	118.3 m	290.8 m	716.4 m	1.8	4.3	10.7	26.3	64.6

Figure A.7 : Datasheet of Micrometals EQHF-265190124- 060.

CURRICULUM VITAE

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PUBLICATIONS, PRESENTATIONS AND PATENTS ON THE THESIS:

- **Dayioglu Yurdakonar, T.,** Yilmaz. M. 2023. Design and Implementation of Phase-Shifted Full-Bridge Converter with a Current Doubler for HV to LV Battery Charger in EVs, *International Conference - ELECO 2023*, November 30-December 2, 2023 Bursa, Turkey

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- **Dayioglu Yurdakonar, T.,** Gulbahce, M.O., Lordoglu, A. and Kocabas, D.A. 2023. Design of a High-Efficiency Micro-Inverter with TO-220 Packaged Gallium Nitride-High-Electron-Mobility Transistors, *Electrica 2023*.