

ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

**DESIGN AND ANALYSIS OF TOPOLOGIES AND CONTROL ALGORITHMS
USED IN EV FAST CHARGING SYSTEMS**



M.Sc. THESIS

Özgür Can MİLLETSEVER

Department of Electrical Engineering

Electrical Engineering Master Programme

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**Özgür Can MİLLETSEVER
(504191089)**

Department of Electrical Engineering

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Thesis Advisor: Assoc. Prof. Dr. Murat YILMAZ

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**ELEKTRİKLİ ARAÇ HIZLI ŞARJ SİSTEMLERİNDE KULLANILAN
TOPOLOJİLER VE KONTROL ALGORİTMALARININ ANALİZİ VE
TASARIMI**

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**Özgür Can MİLLETSEVER
(504191089)**

Elektrik Mühendisliği Anabilim Dalı

Elektrik Mühendisliği Yüksek Lisans Programı

Tez Danışmanı: Doç. Dr. Murat YILMAZ

NİSAN 2023

Özgür Can MİLLETSEVER, a M.Sc. student of ITU Graduate School, student ID 504191089, successfully defended the thesis entitled “DESIGN AND ANALYSIS OF TOPOLOGIES AND CONTROL ALGORITHMS USED IN EV FAST CHARGING SYSTEMS”, which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

Thesis Advisor: Assoc. Prof. Dr. Murat YILMAZ
Istanbul Technical University

Jury Members: Asst. Prof. Dr. Deniz YILDIRIM
Istanbul Technical University

Asst. Prof. Dr. Nihan ALTINTAŞ
Yıldız Technical University

Date of Submission : 30 December 2022
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To my family



FOREWORD

I would like to thank my thesis advisor Assoc. Prof. Dr. Murat Yılmaz at Istanbul Technical University, for all the support and valuable advices. Finally, I would like to thank my dear family for always being there for me.

April 2023

Özgür Can MİLLETSEVER
(Electrical Engineer)





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ABBREVIATIONS

EV	: Electric Vehicle
THD	: Total Harmonic Distortion
PFC	: Power Factor Correction
THDi	: Total Harmonic Distortion of Current
DC	: Direct Current
DES	: Distributed Energy Sources
WBG	: Wide-Band Gap
DAB	: Dual Active Bridge
HIL	: Hardware-in-the-Loop
G2V	: Grid-to-Vehicle
V2G	: Vehicle-to-Grid
ZVS	: Zero Voltage Switching
ZCS	: Zero Current Switching
HEV	: Hybrid Electric Vehicle
IM	: Induction Machine
CCS	: Combined Charging System
BMS	: Battery Management System
SOC	: State-of-Charge
SOH	: State-of-Health
CV	: Constant Voltage
CC	: Constant Current
CP	: Constant Power
HFTR	: High-Frequency Transformer
PSFB	: Phase-Shifted Full Bridge
NPC	: Neutral Point-Clamped
ANPC	: Active Neutral Point-Clamped
EMI	: Electromagnetic Interference
FB	: Full-Bridge
ESR	: Equivalent Serial Resistance
PCB	: Printed Circuit Board

ZVT: : Zero-Voltage-Transition
PI : Proportional and Integral
PWM : Pulse Width Modulation
PLL : Phase-Locked Loop
RRF : Rotating Reference Frame
PF : Power Factor



SYMBOLS

I_{sc}	: Short Circuit Current
$I_{nom-load}$	: Total Load Current
TDD_i	: Total Demand Distortion of Current
THD_i	: Total Harmonic Distortion of Current
I_n	: n^{th} Current Harmonic
L	: Inductance Value
C	: Capacity Value
L_i	: Grid Side Inductance Value
L_o	: Rectifier Side Inductance Value
L_t	: Trap Filter Inductance Value
C_t	: Trap Filter Capacitance Value
R	: Damping Resistor Value
f_{tune}	: Tuning Frequency
L_1, L_2, L_3	: Phase Connections
D_x	: x^{th} Diode
Q_x	: x^{th} Switch
L_{bx}	: x^{th} Boost Inductance
C_{dc}, C_{dcx}	: x^{th} DC/DC Converter Output Capacitor
V_{fb}	: Output Voltage of Full Bridge
V_{NPC}	: Output Voltage of Neutral Point-Clamped Rectifier
f	: Frequency
Z_L	: Impedance of Inductance
P_{o-max}	: Maximum Power of Each Full-Bridge
I_L	: Phase Current
V_{L-L}	: Line Voltage
P_{grid}	: Grid Power
V_{o-min}	: Minimum Output Voltage
I_{o-max}	: Maximum Current at Maximum Power
I_o	: Output Power
I_{Lo}	: Output Inductance Current

I_{Lo-min}	: Minimum Value of Output Inductance Current
I_{Lo-max}	: Maximum Value of Output Inductance Current
I_{pr}	: Transformer Primary Current
I_s	: Transformer Secondary Current
R_{DS-on}	: Drain-Source On Resistance
I_{D-nom}	: Nominal Drain Current
I_{DRM}	: Repetitive Peak Drain Current
V_{pr}	: Transformer Primary Voltage
V_s	: Transformer Secondary Voltage
P_{tr}	: Transformer Power
f_{sw}	: Switching Frequency
$WaAc$	: Product of Window Area and Core Area
B_{max}	: Maximum Flux Density
A_L	: Inductance Factor
μ_e	: Relative Effective Permeability
P_v	: Maximum Core Loss per Set
P_{c-max}	: Maximum Core Loss
l_e	: Effective Core Length
A_c	: Effective Core Cross Section Area
V_e	: Core Volume
B_{sat}	: Saturation Flux Density
B_m	: Selected Maximum Flux Density
L_{mag}	: Magnetization Inductance
ΔI_{Lo-pp}	: Maximum Current Ripple on the Output Inductance
H	: Magnetic Field Strength
P_{core}	: Core Losses
P_{cu}	: Copper Losses
V_o	: Output Voltage
I_o	: Output Current
V_i	: Input Voltage
V_{ref}	: Output Reference Voltage
K_{pi}	: Current Gain
$V_{CE(sat)}$	: Saturation Collector-Emitter Voltage
I_{C-nom}	: Nominal Collector Current
θ_{grid}	: Instantaneous Phase Angle of the Grid

V_{q-grid}	: Grid q-Axis Voltage
V_{d-grid}	: Grid d-Axis Voltage
V_{dc}	: DC Link Voltage of Neutral Point-Clamped Rectifier
V_{dc-ref}	: DC Link Voltage Reference of Neutral Point-Clamped Rectifier
I_{d-ref}	: Reference d-Axis Current
I_{0-ref}	: Reference Zero-Axis Current
I_{abc}	: Rectifier Currents
I_{q-ref}	: Reference q-Axis Current
V_{d-ref}	: d-Axis Reference Voltage
V_{q-ref}	: q-Axis Reference Voltage
V_{0-ref}	: Zero-Axis Reference Voltage
Z_{f-max}	: Maximum Filter Impedance
Z_f	: Filter Impedance
f_{grid}	: Grid Frequency
C_{min}	: Lowest Filter Capacitance Value
C_{mix}	: Highest Filter Capacitance Value
Z_c	: Capacitor Impedance
OD	: Outer Diameter
ID	: Inner Diameter
HT	: Height



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DESIGN AND ANALYSIS OF TOPOLOGIES AND CONTROL ALGORITHMS USED IN EV FAST CHARGING SYSTEMS

SUMMARY

Because of rising carbon emissions, there is a growing trend toward alternative fuels for vehicles instead of gasoline and diesel fuel. Different studies have been conducted, such as on full electric vehicles with batteries as the main powertrain, hydrogen-fueled vehicles, and hybrid vehicles with both an internal combustion engine and an electric motor. Today, many automotive manufacturers such as Renault, Volkswagen, Citroen and Porsche have released electric variants of some of their models, while some manufacturers have produced electric vehicles with new model names. There are also companies, such as Tesla, that were established just for the production of electric vehicles.

Each vehicle has its own on-board charging system for charging the battery packs in each vehicle. However, due to limited space inside the vehicle, this charging system is typically low-powered, and charging the battery packs in a low state of charge takes a very long time. Fast charging stations, which we can think of as fuel stations for charging in a short time, have been developed. On-board charging systems usually have power below 20 kW due to size constraints. However, because the size of the fast-charging station is larger, there are charging stations with power greater than 300 kW. Rather than designing the structure with a single high-power system, many manufacturers prefer a modular structure. The charging station's wide output voltage range is also one of the criteria considered in its design.

Over time, with the increase in studies on electric vehicles and charging stations, different standards, such as CHAdeMO and CCS, have emerged in different regions. Even if each standard differs from the other in certain aspects, some standards are globally applicable. The IEEE 519 standard is a general standard for grid-connected power electronic devices, while the IEC 61851 standard is the general standard for conduction charging. In the sub-sections of this standard, rules are also set for different issues such as DC charging stations, insulation types, and communication protocols.

First, the structures of various DC fast charging systems and the configurations used are examined in this thesis. The topologies and structures that can be used for each subsystem are then compared, and the DC fast charging system is designed in the topologies of the chosen structure. The design is for the one module that will be located in a modular charging station. A three-level neutral point clamped rectifier topology is chosen as the rectifier. In the grid-connection filter, an LCL filter with a damping resistor and a trap filter tuned to the switching frequency is designed. Isolation between the grid and the vehicle battery pack is provided by a high frequency transformer in the DC/DC converter. A phase-shifted full bridge DC/DC converter is used in this part. However, in order to reduce the switching losses, improve system performance, and increase efficiency, design modifications have been made to the topology for switching at zero voltage transition. In addition, switching and conduction losses are reduced by using SiC semiconductors. By using SiC semiconductor, the switching frequency is increased and the size of the high frequency transformer is reduced. In order to optimize the transformer size and be more flexible in semiconductor sizing, two parallel phase-shifted full bridge DC/DC converters are used in the DC/DC converter section. These two circuits are linked in parallel by the same DC link, and their outputs are also linked in parallel to transfer energy to the battery pack.

In the design phase, mathematical models of the selected topologies were first derived and modeled with ideal elements. The PLECS package program, which is specialized for power electronics, was used in all modeling and simulations. With the ideal model, the elements were selected according to the simulation results, and the ideal model prepared according to the design was modified into a full physical model with the addition of magnetic and thermal characteristics.

The switching frequency of the DC/DC converter was chosen to be 40 kHz since a low switching frequency would increase the transformer size. SiC MOSFETs are used to reduce switching and conduction losses, and the topology is modified for zero voltage switching. In the rectifier stage at the output of the phase-shifted full-bridge DC/DC converter, a full-wave bridge diode structure is used due to the high power. Since Si diodes have high reverse recovery energy and time, SiC diodes are used to increase the efficiency. At the rectifier, 16 kHz of switching frequency is selected. The reason of that is the losses of the rectifier is less than the DC/DC converter. Si IGBTs are used for the neutral point clamped rectifier. A 3-level topology is selected for the increasing

the DC-link voltage. With a higher DC-link voltage it is possible to reaching higher DC output voltage. Also, 3-level rectifier has a less amount of total harmonic distortion of current when operating.

As a result of the modeling and simulations, it is seen that the losses are reduced with the changes made. At a constant 80°C heatsink temperature, the highest junction temperature is 112°C and the efficiency is above 95%. When the current waveform drawn from the grid is analyzed, it is seen that it complies with IEEE 519 standards. The experimental results of the designed system are consistent with the simulation results. The experimental peak efficiency of the system was measured at 97.52%. The measurement results and waveforms obtained from the experimental studies are similar to the simulation results.

The whole system power density is equal to 0.82 kW/L. Using SiC MOSFETs and SiC diodes is the most affective reason of high amount of power density. With the increasement of the switching frequency of DC/DC converter, it is possible to use a smaller transformer. SiC MOSFET usage decreased the losses by 76.41%.



ELEKTRİKLİ ARAÇ HIZLI ŞARJ SİSTEMLERİNDE KULLANILAN TOPOLOJİLER VE KONTROL ALGORİTMALARININ ANALİZİ VE TASARIMI

ÖZET

Artan karbon emisyonu nedeniyle, ulaşım araçlarında benzin ve mazot yerine alternatif yakıtlara yönelim artmıştır. Ana güç kaynağı bataryalar olan tam elektrikli araçlar, hidrojen yakıtlı araçlar ve hem içten yanmalı motora hem de elektrik motoruna sahip hibrid araçlar gibi farklı çalışmalar yapılmıştır. Hibrid araçlar, konvansiyonel araçlar gibi içten yanmalı motora sahip fakat bunun yanında bir de elektrik motoru bulunduran yapılardır. Bu içten yanmalı motor araç hareketine katkı sağlayabileceği gibi, sadece elektrik üretilmesinde de rol oynayabilir. Bunun dışında hidrojen yakıtlı araçlar da bazı çalışmalarda denenmiştir. Fakat bunlar arasındaki en popüler olanı, üzerine en çok çalışma yapılanı ve ticari olarak en tercih edileni tam elektrikli araçlar olmuştur.

Günümüzde Renault, Volkswagen, Citroen ve Porsche gibi birçok otomotiv üreticisi bazı modellerinin elektrikli varyasyonlarını çıkarırken, bazı üreticiler ise yeni model adıyla elektrikli araçlar üretmiştir. Volkswagen Golf modelinin bir varyantı olarak e-Golf'ü tasarlarken, Renault ise Zoe modelini sadece elektrikli olarak tasarlamıştır. Ayrıca Tesla gibi sadece elektrikli araç üretimi için kurulmuş şirketler de vardır. Her bir üretici, kendi modellerinde farklı tipte elektrik motorunu ve batarya paketlerini tasarlamıştır. Renault Zoe klasik uyarma sargılı klasik senkron motora sahipken, Tesla markası genellikle araçlarında asenkron motor ve mıknatıslı motorları tercih etmektedir. Fakat genel eğilim sürekli mıknatıslı senkron motor kullanımına yöneliktir.

Her araç içinde bulunan batarya paketlerinin şarjı için her bir araç kendi içinde araç üstü şarj sistemini bulundurur. Fakat araç içindeki yer kısıt ve maliyetinden dolayı bu şarj sistemi genellikle düşük güçlüdür ve düşük şarj durumundaki batarya paketlerini şarj etmeleri çok uzun sürer. Gün içi kullanımlar için, akşamdan sabaha kadar geçen süredeki şarj yeterli olabilirken uzun yol durumları veya yolcu ve yük taşımacılığı durumları için bu kadar uzun süreler problem yaratabilmektedir. Bu amaçla akaryakıt

istasyonlarına benzetebileceğimiz ve bataryayı hızlı bir şekilde şarj edebilme yeteneğine sahip hızlı şarj istasyonları ortaya çıkmıştır. Araç üstü şarj sistemleri, şebekeden alternatif gerilim ile beslenir ve kendi içinde doğrultucu ve DC/DC çevirici bulundurulur. Bu doğrultucu ve DC/DC çevirici yardımıyla enerjiyi istenen gerilim ve güçte batarya paketine ulaştırırlar. Fakat hızlı şarj istasyonları, kendi içinde doğrultucu ve DC/DC çevirici içerdikleri için, araca ve bataryaya doğrudan doğru gerilim ile enerjiyi aktarırlar. Araç üstü şarj sistemleri, boyut kısıtı gibi sebeplerden genellikle 20 kW altında güce sahiptirler. Fakat hızlı şarj istasyonunda kullanılabilecek boyut daha büyük olduğu için 300 kW üzeri güce sahip şarj istasyonları bulunmaktadır. Tritium markasının PK350 modeli 350 kW çıkış gücüne sahiptir. Günümüzde bu değerler 900 kW değerlerine (GB/T, ChaoJi) ulaşmış durumdadır. Tek bir yüksek güçlü sistem ile yapıyı tasarlamaktansa birçok üretici, modüler bir yapı tercih etmektedir. Bir diğer konu ise hızlı şarj istasyonunun çıkış gerilim aralığıdır. Farklı araç modelleri, farklı batarya paketi gerilimlerine sahip oldukları için şarj istasyonunun geniş bir çıkış gerilim aralığına sahip olması önemlidir.

Zamanla elektrikli araçlar ve şarj istasyonları üzerine yapılan çalışmaların artmasıyla, farklı standartlar ortaya çıkmıştır. CHAdeMO, CCS, GB/T gibi farklı standartlar farklı bölgelerde ortaya çıkmıştır. Her bir standart belli konularda birbirinden ayrılabilir bazı standartlar küresel çapta geçerlidir. IEEE 519 standardı, şebekeye bağlı güç elektroniği cihazları için genel bir standarttır ve şebekeden çekilen akımın harmonik sınırlarını ve cihazın, bağlantı noktasında yarattığı gerilim harmoniği sınırlarını belirlemektedir. IEC 61851 standardı ise iletim yoluyla yapılan şarj işlemleri için genel standarttır. Bu standardın alt başlıklarında DC şarj istasyonları, izolasyon tipleri ve haberleşme protokolleri gibi farklı konular için de kurallar belirlenmiştir.

Bu tez kapsamında, öncelikle farklı DC hızlı şarj sistemlerinin yapıları ve kullanılan konfigürasyonlar incelenmiştir. Daha sonra her bir alt sistem için kullanılabilecek topoloji ve yapılar karşılaştırılmış ve seçilen yapıda bulunan topolojilerdeki DC hızlı şarj sistemi tasarlanmıştır. Tasarım kriterleri olarak IEEE 519 standartlarına uyumluluğa ve birçok araç modelinin batarya paketini şarj edilebilecek bir konfigürasyon seçilmiştir. Yapılan tasarım, modüler yapıdaki bir şarj istasyonunda bulunacak bir modülün tasarımıdır. Doğrultucu olarak üç seviyeli olan nötr noktası kenetlemeli doğrultucu topolojisi seçilmiştir. Bunun nedeni, bu topolojinin üç seviyeli olması nedeniyle dengeli ve diğer topolojilere kıyasla daha yüksek bir DC bara

gerilimi elde edilebilmesidir. Ayrıca IEEE 519 standartlarına uyumluluk için akım harmoniğinin düşük olması gereklidir ve üç seviyeli topolojiler, iki seviyeli topolojilere kıyasla bu konuda daha başarılıdır. Şebeke bağlantı filtresinde ise sönümlleme direncine ve anahtarlama frekansına akort edilmiş yakalayan filtreye sahip bir LCL filtre tasarımı yapılmıştır. Diğer filtre topolojileri ile yapılan kıyaslama sonucu boyut avantajı, tasarım kolaylığı ve performans açısından öne çıkmaktadır. Şebeke ve araç batarya paketi arasındaki izolasyon, DC/DC çeviricide bulunan yüksek frekans transformatörü yardımıyla sağlanmıştır. Bu kısımda faz kaydırmalı tam köprü DC/DC çevirici yapısı kullanılmıştır. Fakat anahtarlama kayıplarını azaltmak, sistem performansını iyileştirmek ve verimi yükseltmek için sıfır gerilim geçişinde anahtarlama yönelik topoloji üzerinde tasarım değişiklikleri yapılmıştır. Ayrıca SiC yarıiletken kullanımı ile anahtarlama ve iletim kayıpları azaltılmıştır. Si yarıiletkenlere göre daha yüksek frekanslarda çalışabilen SiC yarıiletken ile anahtarlama frekansı da arttırılmıştır. Artan anahtarlama frekansı ile kullanılacak yüksek frekans transformatörünün boyutu küçültülmüştür. Transformatör boyutunu en iyileştirebilmek ve yarıiletken boyutlandırmasında daha esnek olmak için DC/DC çevirici kısmında iki adet paralel çalışan faz kaydırmalı tam köprü DC/DC çevirici kullanılmıştır. Bu iki devre aynı DC baradan paralel olarak beslenmekte ve çıkışları tekrar paralel olarak bağlanarak batarya paketine gerekli enerjiyi aktarmaktadır.

Tasarım aşamasında seçilen topolojilerin öncelikle matematiksel modelleri çıkarılmış ve ideal elemanlar ile modellemeleri yapılmıştır. Yapılan bütün modelleme ve simülasyonlarda güç elektroniği için özelleşmiş olan PLECS paket programı kullanılmıştır. Bu paket program, manyetik ve termal modellemeye de izin verdiği için sistem modeli, tasarım aşamalarına paralel olarak adım adım idealden gerçekte fiziksel sisteme yaklaştırılmıştır. İlk başta hazırlanan ideal model oluşturulduktan sonra, elde edilen simülasyon sonuçlarına göre devre elemanlarının seçimi ve boyutlandırılması yapılmıştır. Eleman seçimi ve tasarım sonuçlarına göre hazırlanan ideal model, manyetik ve termal karakteristiklerin de eklenmesi ile tam fiziksel modele dönüştürülmüştür.

Tasarım sonucunda bir adet 16 kHz anahtarlama frekansına, 22 kW güce sahip üç fazlı nötr noktası kenetlemeli doğrultucu; bu doğrultucunun şebeke bağlantısını sağlayacak üç fazlı, sönümlleme direncine ve anahtarlama frekansına akort edilmiş yakalayan filtreye sahip bir LCL filtre ve 40 kHz anahtarlama frekansına, 11 kW güce sahip sıfır

gerilim geçişinde anahtarlama faz kaydırmalı tam köprü DC/DC çevirici elde edilmiştir. Tasarımı yapılan sıfır gerilim geçişinde anahtarlama faz kaydırmalı tam köprü DC/DC çeviricilerden iki tanesinin giriş ve çıkış kısımları paralel bağlanarak 22 kW güce sahip bir modül elde edilmiştir.

Tasarım aşamasında doğrultucunun kayıplarının düşük olması nedeniyle Si IGBT kullanılmış ve anahtarlama kaybı bu sayede düşük tutulabilmiştir. Fakat DC/DC çeviricinin anahtarlama frekansının düşük seçilmesi, transformatör boyutunu arttıracak için 40 kHz anahtarlama frekansı bu devre için seçilmiştir. Bu durumdaki anahtarlama ve iletim kayıplarının yüksek olduğunun görülmesi nedeniyle, SiC MOSFET kullanımı ile anahtarlama ve iletim kayıplarının azaltılması için çalışılmış ve sıfır gerilimde anahtarlama için topoloji üzerinde gerekli değişiklikler yapılmıştır. Faz kaydırmalı tam köprü DC/DC çeviricinin çıkışında bulunan doğrultucu kademesinde, gücün yüksek olması nedeniyle tam dalga köprü diyot yapısı kullanılmıştır. Si diyotların ters toparlanma enerjileri ve süreleri yüksek olduğu için SiC diyot kullanımı ile verimi arttırmaya yönelik çalışmalar gerçekleştirilmiştir.

Yapılan modelleme ve koşturulan simülasyonlar sonucunda, yapılan değişiklikler ile kayıpların azaldığı görülmüştür. DC/DC çeviricide bulunan diyotların, anahtarlama kayıpları ihmal edilebilecek kadar küçük seviyelerdedir. Ayrıca tam köprü yapısının iletim kayıpları, SiC MOSFET kullanımı ile azaltılabilmektedir. Sabit 80°C soğutucu sıcaklığında, en yüksek jonksiyon sıcaklığının 112°C ve verimin %95 üzerinde olduğu görülmüştür. Şebekeden çekilen akım dalga formu incelendiğinde ise, IEEE 519 standartlarına uyumlu olduğu sonucuna varılmıştır. Bu kriterler ışığında, tasarlanan sistemin tasarım parametreleri ile uyumlu olduğu görülmüştür.

Tasarlanan sistemin deneysel sonuçları, simülasyon sonuçları ile karşılaştırılmış ve tutarlı olduğu görülmüştür. Sistemin deneysel verimi %97,52 olarak ölçülmüştür. Deneysel çalışmalar sonucu elde edilen ölçüm sonuçları ve dalga şekilleri simülasyon sonuçlarına benzerdir. Arada oluşan verim farkının en büyük nedeni, sistemin çalışırken sabit 80°C soğutucu sıcaklığında olmayışıdır.

SiC MOSFET kullanımı ile DC/DC çevirici kayıpları %76,24 oranında azaltılabilmiş ve sistemin toplam güç yoğunluğu 0,82 kW/L seviyesine çıkarılabilmektedir. DC/DC çeviricide SiC MOSFET yerine Si IGBT kullanmak, anahtarlama frekansının daha düşük seçilebilecek olmasından dolayı transformatör boyutunda yaklaşık iki katı bir

büyükölük getirecektir. Ayrıca gerekli yarı iletkenleri soğutmak için gerekli soğutucu boyutu da kayıplar nedeniyle yaklaşık iki kat artacağından, güç yoğunluğu yaklaşık olarak iki katına çıkarılabilmekmiştir.





1.INTRODUCTION

The use of electric vehicle (EV) chargers has increased with the increasing number of EVs. Fast charging units are becoming more widespread over time, and the areas where they are installed worldwide are growing. Manufacturers first determine the voltage and frequency range in which the product can operate safely. Some manufacturers give a percentage range, while others specify the lowest and highest voltages. Generally, designs are made to operate at a 50/60 Hz frequency and a 208-480 V voltage range.

EV charging units are power electronics-based systems. According to the standards, the output must be isolated from the input. In conventional designs, this isolation can be achieved by feeding the system through an isolation transformer connected to three phases on the input side. These structures are realized by using a rectifier unit on the secondary side of the isolation transformer. This structure causes both a low power factor and a high total harmonic distortion (THD). The new generation products are fed by a power factor correction (PFC) stage, and the isolation process is realized by an isolated DC/DC converter on the output side, not by an isolation transformer on the input side. This allows the system to be realized in smaller sizes while achieving a high-power factor and low total harmonic distortion of current (THDi). With this new structure, the power factor is usually above 0.99 and THDi is below 5% in charging units [1].

Fast direct current (DC) charging systems can be unidirectional or bidirectional in energy flow. In the industry, low-cost solutions are unidirectional structures. However, there is an increasing trend towards methods that provide bidirectional energy flow. Systems that allow bidirectional energy flow act as distributed energy sources (DES), allowing the energy in the batteries of EVs to be transferred to the grid. In this way, EVs can provide support to the grid on demand.

Fast DC charging systems can be of various power levels. Chargers above 20 kW are classified as fast chargers, and their power can reach several hundred kilowatts. Such high-power systems can be realized with a single high-power inverter or by connecting

many low-power modules in parallel. Modular systems have many advantages. First of all, modular systems are suitable for power increases by adding additional modules at any time. These systems provide redundancy so that even if one or more of the modules are disabled due to failure, maintenance, etc., the rest of the system continues to operate [2].

In remote areas where charging stations will be installed, a significant installation cost is required for the energy infrastructure. The stations need to be fed from the medium-voltage grid through a separate distribution transformer. This medium-voltage line needs to be connected to the station and meet the energy requirements of the charging stations, which can reach hundreds of kilowatts. In weak grids, energy quality problems occur due to the dynamic power flow that is required by the charging stations. Charging units must be able to operate even in grids with energy quality problems.

1.1.Purpose of Thesis

Within the scope of the thesis, different charging unit structures were analyzed and compared. As a result of the comparisons, suitable structures were determined for the design of a high efficiency charging unit, and a 22 kW system was designed for the selected structure. While designing, attention was given to the standards' suitability and industrial usability was emphasized.

For a high efficiency system design, high efficiency topologies and control algorithms for the rectifier and DC/DC converter are preferred. Appropriate modulation techniques have been selected to reduce losses. Proper thermal design has been made for the system to operate under suitable conditions.

With the wide-band gap (WBG) switching devices usage, the switching frequency can be increased and the sizes of necessary filter elements and transformer can be reduced. Additionally, the losses of WBG switching devices are smaller than the Si switching devices. Because of that, the efficiency will be much higher and the necessary cooling requirements will be much smaller. With a smaller heat sink and smaller filter elements, the power density of the system will be increased. Also, the necessary fan size will be decreased.

1.2.Literature Review

In the study for DC fast charging in electric busses, thermal modeling of a DC fast charger with an output power of 150 kW was performed. In this study, a single-stage design is preferred. An isolation transformer operating at grid frequency and an LCL filter are used in the grid connection. The voltage rectified by a six-switch boost PFC rectifier is applied directly to the battery [3]. Figure 1.1 shows the structure used in this study.

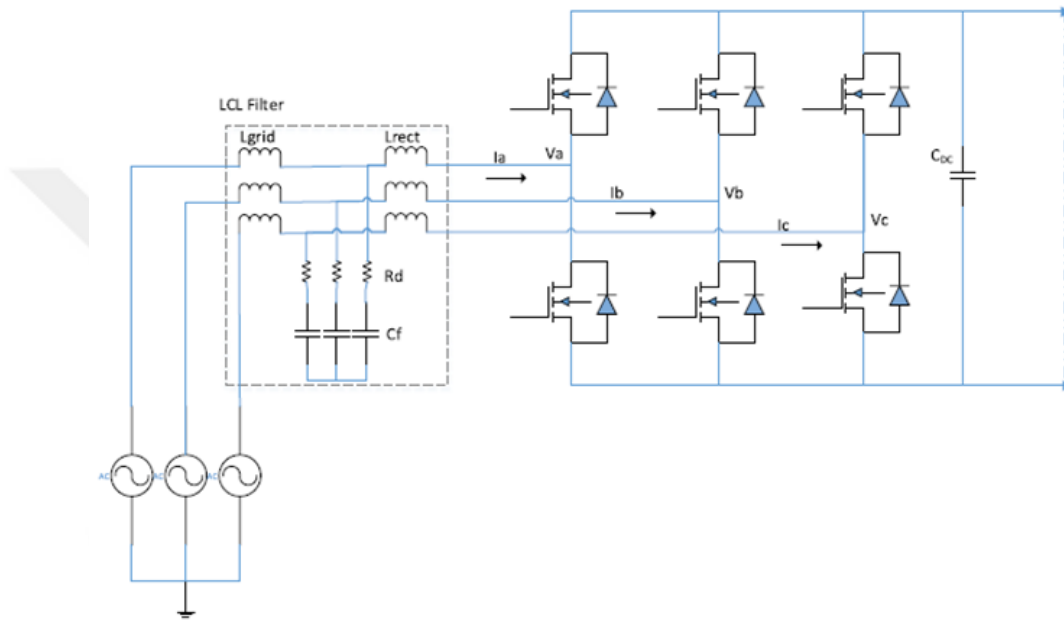


Figure 1.1 : Topology studied for DC fast charger in electric busses [3].

In this study, only simulations were performed. In the simulations, switching frequency was chosen as 40 kHz. At an output power of 175 kW, the efficiency was above 96%. In addition, the THDi was below 3% and the power factor was above 99%, in accordance with the standards. The system can be designed in a smaller size by using SiC MOSFETs [3].

In a different study using an isolation transformer operating at grid frequency, a two-stage design was used. A constant DC-link voltage was obtained by using two parallel six-switch boost PFC rectifiers with an L filter at the input. This DC-link voltage is then applied to the battery via a bidirectional, 3-level asymmetrical converter. The topology used in this study is as shown in Figure 1.2. The designed system has an output voltage between 200 V and 500 V and an output power of 40 kW. As a result of the experimental studies, the system operates with a THDi below 3% and a power factor of 0.99 when operating at full load [4].

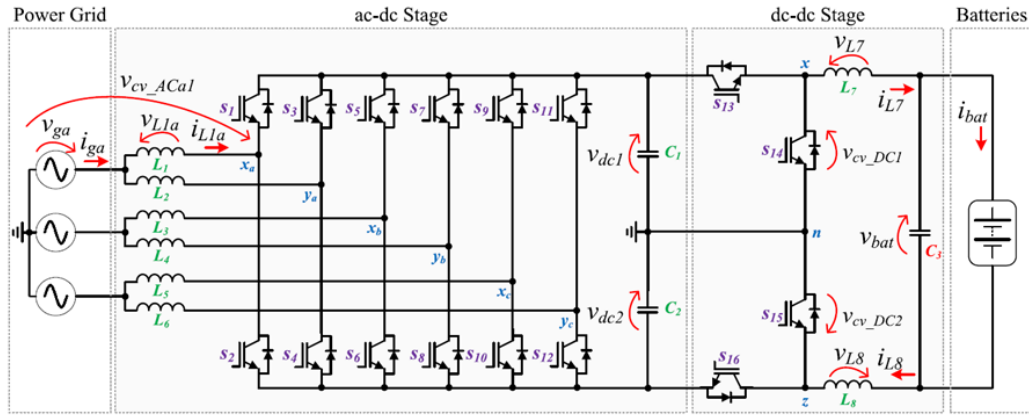


Figure 1.2 : Two-stage system with grid side isolation transformer [4].

In these two studies, isolation between the battery and the grid was provided with isolation transformers operating at grid frequency. The system in the first study is a single-stage system, and in applications where such a system will be used, the isolation transformer should be located at the grid connection point. In the second study, the application was realized in this way because the DC/DC converter does not have an isolated type of structure. Nowadays, the more preferred structure is the one where the DC/DC converter is realized with an isolated topology. In this way, the size of the transformer can be reduced by increasing switching frequency. The structures that will continue to be analyzed are those with such topologies.

In a study using a six-switch boost PFC rectifier and a dual active bridge (DAB) converter, the voltage applied to the battery was controlled via a six-switch boost PFC rectifier. The DAB converter used in the study operates at 50% duty cycle with single phase-shift modulation. The voltage applied to the battery can be controlled by adjusting the rectified DC link voltage. In the structure shown in Figure 1.3, switching frequency of DAB converter is selected as 50 kHz. The experimental results show an output power of 3.3 kW at an output voltage between 290 V and 400 V. With this control strategy, the current stress on the switching devices used in the DAB converter is reduced. In addition, the system can operate in a more optimized way by reducing the reactive power requirement of the system [5].

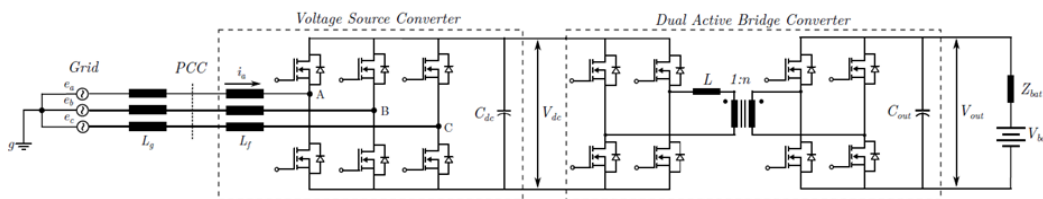


Figure 1.3 : Topology used in variable DC bus control strategy study [5].

In the study on a 50 kW bidirectional EV DC fast charger, 6-switch boost PFC rectifier and three-level DAB converter topologies were used. Simulations and real-time hardware-in-the-loop (HIL) tests were performed for the structure shown in Figure 1.4. The switching frequency of the rectifier is 25 kHz and the switching frequency of the three-level DAB converter is 50 kHz. The output voltage range of the system is between 50 V and 500 V [6].

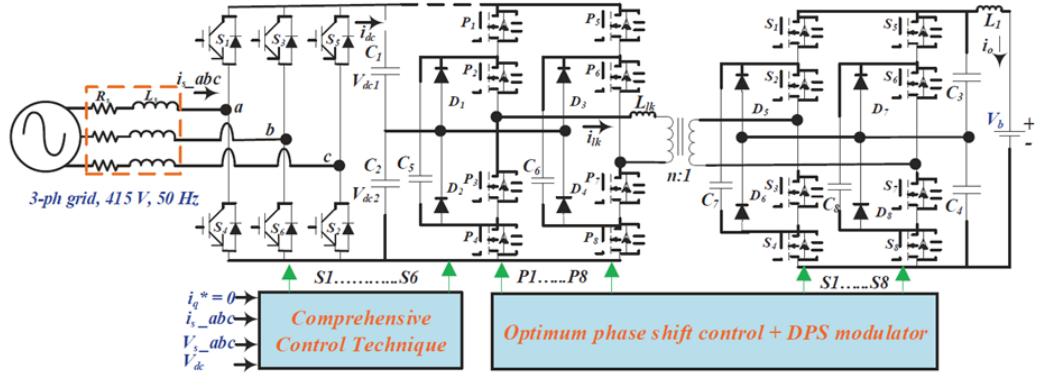


Figure 1.4 : System with six-switch boost PFC rectifier and three-level dual active bridge converter [6].

As a result of HIL tests, it draws 72 A at 415 V grid voltage while operating in grid-to-vehicle (G2V) mode under a 50 kW load at 500 V output voltage. THDi is 1.41%, and efficiency is 96.6%. Under a load of 7.5 kW at an output voltage of 50 V in G2V mode, it draws 12 A of current from the grid with a THDi value of 1.19%. The efficiency in this case is 87%. As expected, the efficiency is lower at lower power and higher current. In vehicle-to-grid (V2G) mode, when 44.6 kW of active power is supplied to the grid with a battery voltage of 450 V, the system efficiency is 99% and THDi is 1.9%. During V2G operation at low power, 6.5 kW of active power could be delivered to the grid with 86.3% efficiency and 3.69% THDi [6]. As seen in this study, efficiency decreases at low power or high current. The most important reason for this is that a certain amount of energy is consumed regardless of the output power. It is also seen that THDi increases when the grid current decreases. THDi in G2V mode is lower than V2G mode under the same conditions.

It is seen that two-level rectifier topologies are used in many studies. The most popular topology is the six-switch boost PFC rectifier. However, the biggest disadvantages of two-level rectifiers are the difficulty of finding capacitors with high withstand voltage and the increase in system size when the DC link voltage at the rectifier output is

desired to be kept high. With the use of multi-level rectifiers, bipolar DC link voltage can be obtained. In addition, since the voltage on the capacitors is reduced, the realization of the system becomes easier. Another advantage of multi-level rectifiers is that they have a lower THDi. In the rest of the chapter, DC/DC converter topologies used in different studies will be analyzed.

In a study on battery energy storage systems and DC fast charging systems, a semi-DAB with a power of 10 kW was designed. The design, which can be supplied with a variable DC link voltage between 350 V and 550 V, is shown in Figure 1.5. 100 kHz was selected as the switching frequency. According to the experimental results, the peak efficiency of the structure with an output voltage between 150 V and 450 V was measured at 97.6% [7].

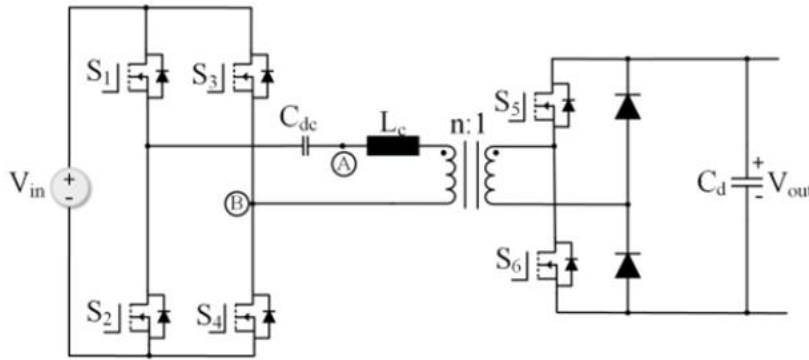


Figure 1.5 : Semi-DAB converter topology [7].

The semi-DAB converter topology is one of the preferred topologies due to the small number of controlled switching elements. This makes control simpler. It also reduces the cost. On the other hand, there may be some decrease in efficiency according to the use of controlled switching devices. For this, techniques such as zero voltage switching (ZVS) or zero current switching (ZCS) can be added to the topology to optimize its efficiency.

A study was carried out to compare the performance of CLLC converters and DAB converters designed with GaN switching devices, which are WBG semiconductors on on-board chargers. For this purpose, a 3.7 kW CLLC converter and a DAB converter were designed. The same GaN MOSFETs were used in both designs. Figure 1.6 (a) shows the topology of the designed CLLC converter, and Figure 1.6 (b) shows the topology of the designed DAB converter. A variable switching frequency between 110 kHz and 300 kHz is used to control the CLLC converter. The main reason for this is the need to adjust switching frequency according to the load to reduce the switching

losses with the resonant tank. In the DAB converter, a fixed switching frequency of 500 kHz was chosen. The experimental results show that the peak efficiency of the DAB converter is 98.6% at 390 V output voltage under a 3 kW load. However, the efficiency of the CLLC converter is 97% at 370 V output voltage under a 3.6 kW load [8]. One of the reasons for this efficiency difference is that the DAB converter allows ZVS and ZCS on the primary and secondary sides, depending on the load. In addition, the losses of the passive components used to create a resonant tank in the CLLC converter also affect its efficiency.

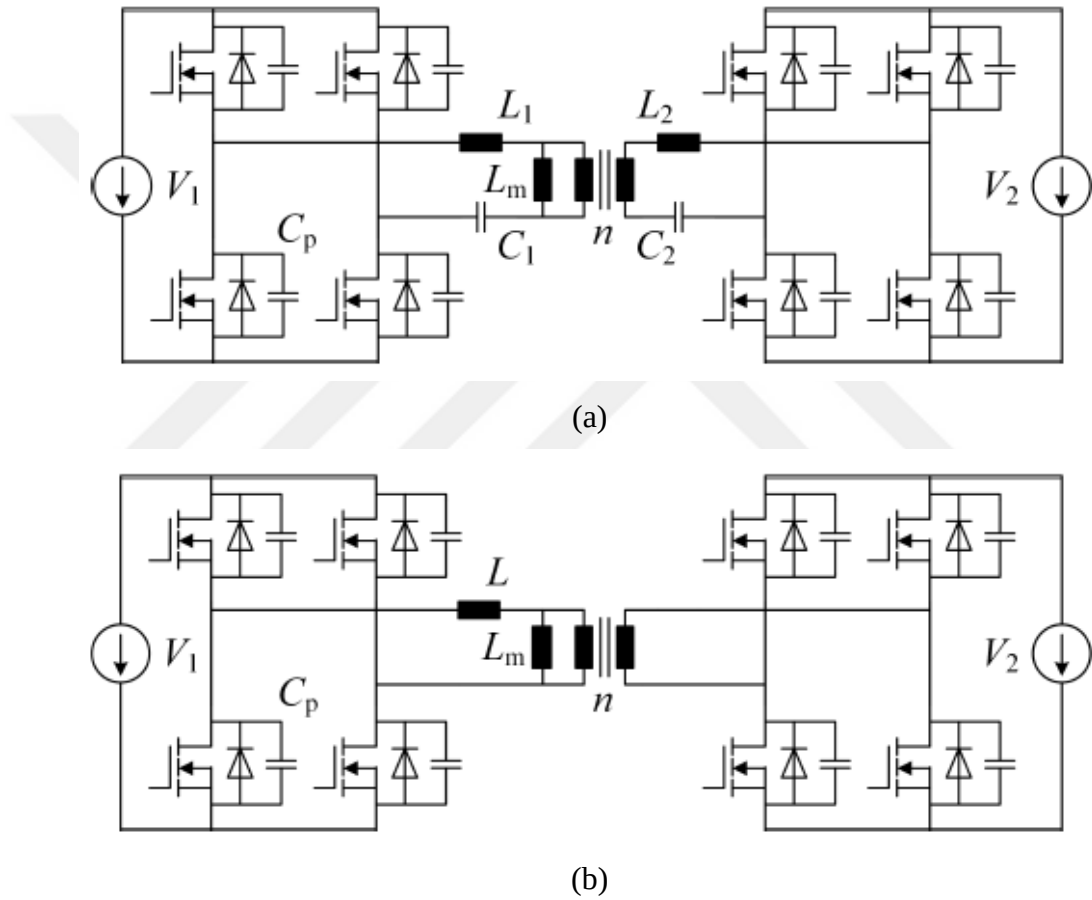


Figure 1.6 : CLLC converter topology (a) and DAB converter topology (b) [8].

In addition to single-stage DC/DC converters, two-stage DC/DC converter designs have also been preferred. Such designs usually consist of an isolated DC/DC converter followed by a non-isolated DC/DC converter. The structure shown in Figure 1.7 is realized with the use of an LLC converter followed by a buck converter.

In this study, a two-stage DC/DC converter with a power of 20 kW and an output voltage between 50 V and 650 V was designed by using an LLC converter and a buck converter together. The switching frequency of the LLC converter is 120 kHz, the

switching frequency of the buck converter is 50 kHz, and the whole LLC circuit operates in ZVS mode. It is also observed that all diodes also perform ZCS. Furthermore, the efficiency is increased above 97% when SiC MOSFETs are used [9].

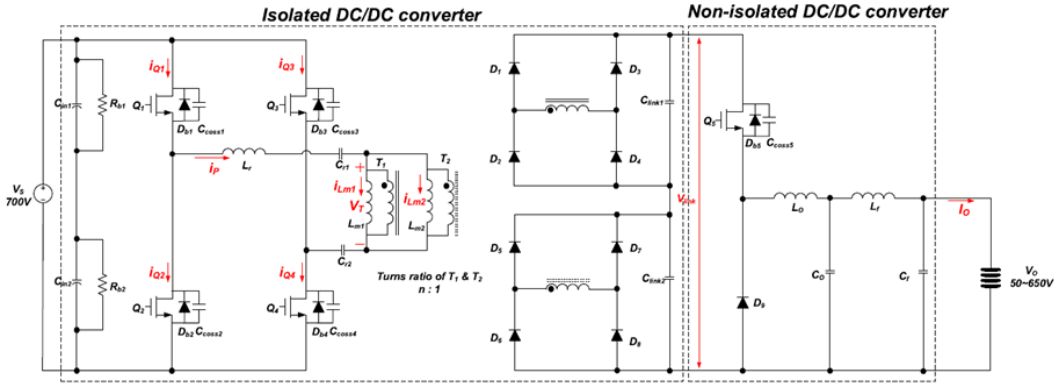


Figure 1.7 : Two-stage DC/DC converter topology [9].

The biggest advantage of this type of structure is that a topology such as LLC goes further from the ZVS state depending on the load, and its efficiency decreases. With the help of the buck converter used after the LLC converter, the desired voltage can be applied to the battery. In this way, the output voltage of the LLC converter can be adjusted according to the output power, allowing switching under the most optimum conditions. This increases the efficiency and performance of the LLC converter.

DC fast chargers and normal speed DC chargers can be used together in charging station installations. With this type of structure, more than one EV can be charged at the same time. The structure shown in Figure 1.8 can be used in hybrid charging stations.

In a study on hybrid charging stations, the structure shown in Figure 1.8 was used. With a 5 kW modular structure, an output voltage between 200 V and 400 V can be obtained on both sides. The fast-charging side can output up to 9 A, while the slow charging side has a maximum current of 3 A. With a power density of 2.7 kW/L, the system has a peak efficiency of 98.2% [10]. In addition to the studies on rectifiers and DC/DC converters, some studies have also been carried out on the grid connection filter. IEEE 519 standards have been generally considered as the performance criteria in the design of the filter part.

The operating conditions of a filter designed for a 50 kW 3-level rectifier are as given in Table 1.1. In a study on LCL filter design, which is one of the filter topologies to be discussed in detail in the next section, it is stated that the resonant frequency should be

at least 10 times larger than the grid frequency and smaller than half of switching frequency. In addition, the reactive power at no-load operation should be less than 10% of the nominal power, and the power factor at minimum load should be above 0.995 [11].

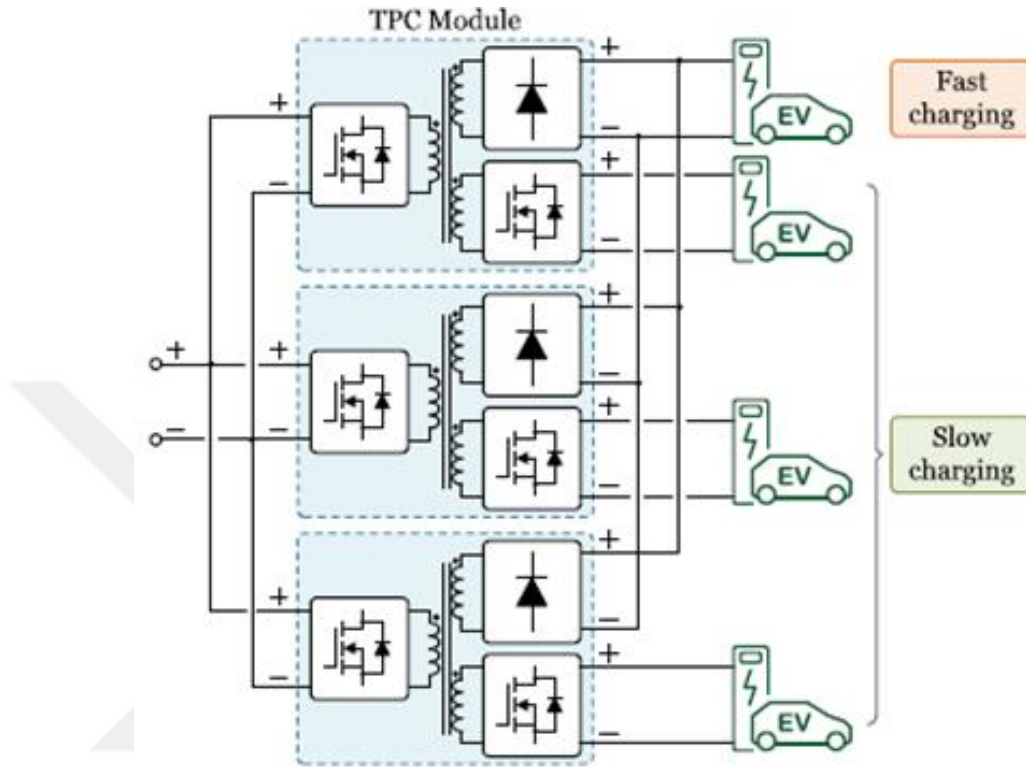


Figure 1.8 : Hybrid charging station structure [10].

Table 1.1 : Operating conditions of LCL filter [11].

Parameter	Value
Grid frequency (Hz)	50
Nominal output power (kW)	50
No-load reactive power (kVAr)	< 5
Phase voltage (V)	230
Phase current (A)	72.5
Power factor	> 0.995
DC-link voltage (V)	650
Switching frequency (kHz)	20

1.3. Standards for EVs Charging

Power grids, in general, have minimal source impedance and well-regulated voltage. They can withstand large disturbances, including harmonic currents, outside of continuous grid frequency loads without creating severe voltage distortion. The

resulting voltage distortion will be quite minor for a given quantity of harmonic current flow [12]. According to IEEE 519 standards, limit values are defined for current and voltage harmonics at multiples of the grid frequency. In addition, the maximum total harmonic distortion that can occur in total is also determined. For grids with voltages of 1 kV and below, each of the first 50 voltage harmonics must be below 5% and the total voltage harmonic distortion must be below 8% [13]. For systems with a voltage between 120 V and 69 kV, the limit values for current harmonics depend on the short circuit current (I_{sc}) and total load current ($I_{nom-load}$) of the system. In the standards, total demand distortion of current (TDD_i) is mentioned instead of THD_i for current harmonics. While equation 1.1 is used to calculate THD, TDD is calculated as in equation 1.2. Table 1.2 shows the limit values set by IEEE 519 standards for current harmonics.

$$THD_i = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \quad (1.1)$$

$$TDD_i = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_{nom-load}} \quad (1.2)$$

Table 1.2 : Maximum harmonic current distortion in percent of $I_{nom-load}$ [13].

$I_{sc}/I_{nom-load}$	$2 \leq n \leq 11$	$11 \leq n < 17$	$17 \leq n < 23$	$23 \leq n < 35$	$35 \leq n$	TDD
<20	4	2	1.5	0.6	0.3	5
20-50	7	3.5	2.5	1	0.5	8
50-100	10	4.5	4	1.5	0.7	12
100-1000	12	5.5	5	2	1	15
>1000	15	7	6	2.5	1.4	20

IEC 61851 is one of the standards for conductive charging systems. Different charging modes are defined in this standard. Modes 1, 2, and 3 are defined for AC charging modes. Mode 4 is defined for both AC and DC charging [14]. The detailed standard for DC charging stations is IEC 61851-23. This standard is used for many vehicles, such as electric scooters and electric buses. According to this standard, the output voltage range of the EV DC charging station according to the application is given in Table 1.3.

Table 1.3 : Voltage levels for different vehicle types according to IEC 61851-23 [15].

Mode	Minimum Voltage (V)	Maximum Voltage (V)
Electric scooters	18	60
Electric passenger vehicles	50	500
Electric passenger vehicles	200	500
Electric busses	400	800

IEC 61851-23 specifies the structures that should be used. According to this standard, Figure 1.9 (a) shows a typical insulated system, Figure 1.9 (b) shows a typical non-isolated system, and Figure 1.9 (c) shows a DC grid system.

IEC 61851-24 deals with the communication between the DC fast charger and the EV. The data to be transmitted in this communication are current and voltage requests, the maximum voltage and current of the DC fast charger, and the maximum voltage and minimum current limit of the EV [15].

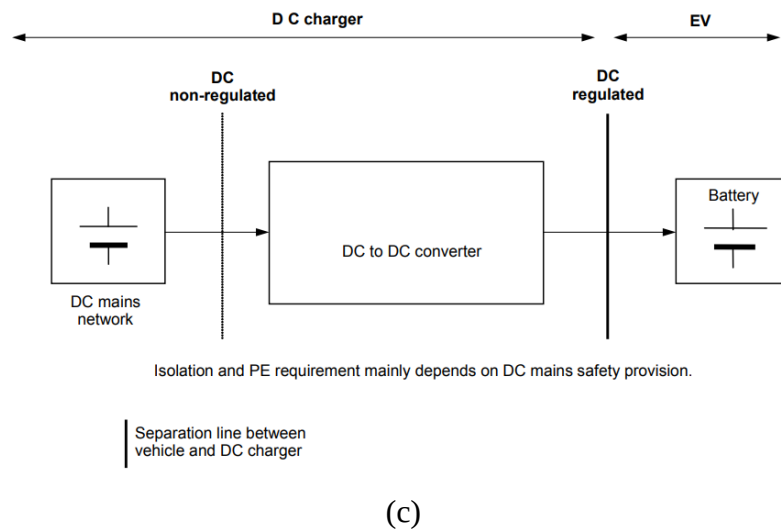
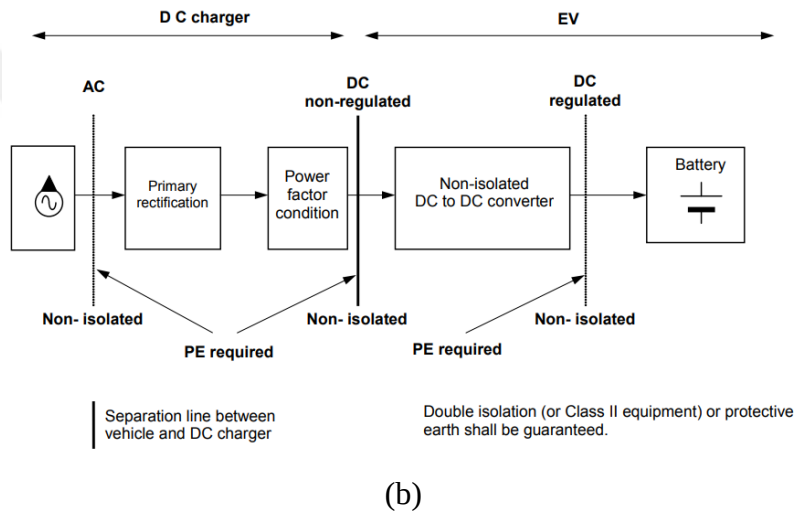
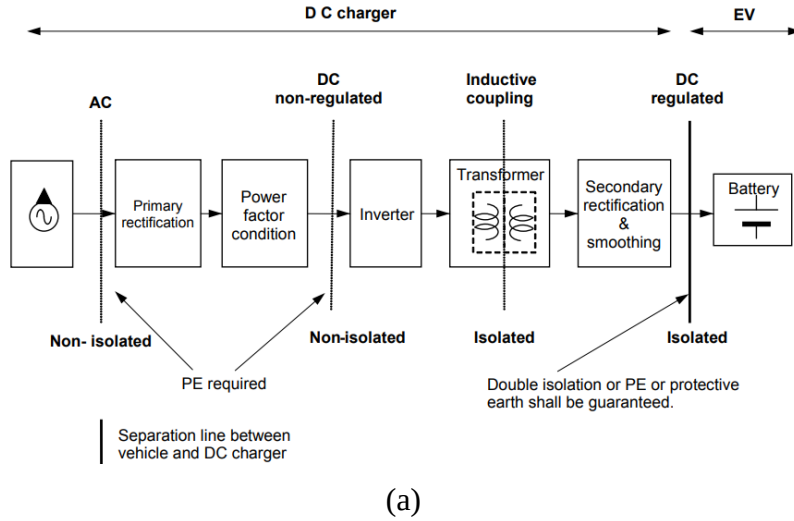


Figure 1.9 : Diagram of typical isolated system (a), typical non-isolated system (b), and system with DC grid (c) [16].

2.ELECTRIC VEHICLES AND CHARGING SYSTEMS

2.1.Electric Vehicles

Due to the limited amount of fossil fuels and the damage they cause to the environment, the use of EVs and hybrid electric vehicles (HEVs) is increasing. According to the IEA, more than 10 million EVs and plug-in HEVs will be in use by the end of 2020. Although the largest share of this number is in vehicles for individual use, the increase in the number of vehicles such as buses and trucks used for commercial purposes should not be ignored. Even in 2020, when vehicle sales declined due to the pandemic, EV and HEV sales volumes has increased, especially in Europe [17]. Over time, many brands have focused on EV production and released models. Each brand has used electric motors with different features and battery packs with different features in their models. Although Tesla uses induction machines (IMs) in its vehicles, most brands prefer the use of permanent magnet motors. Renault uses a wound-rotor synchronous motor in the Zoe model. Each brand has developed battery groups suitable for the characteristics of its own vehicle. Vehicle ranges vary according to these battery groups, with different capacities and voltage. Table 2.1 shows the battery voltages, usable battery capacities, energy consumptions and ranges of different EVs.

Table 2.1 : Battery voltage, usable battery capacity, vehicle energy consumption and vehicle range of some EVs.

Model	Battery Voltage (V)	Usable Capacity (kWh)	Energy Consumption (Wh/km)	Range (km)
Volkswagen e-Golf [18]	323	32	168	190
Kia Niro EV [19]	327	64.8	171	380
Tesla Model X Plaid [20]	350	95	207	460
Audi e-Tron GT RS [21]	400	85	210	405
Renault Zoe ZE50 R135 [22]	400	52	168	310
Ford Mustang Mach-E GT [23]	450	91	214	425
Porsche Taycan [24]	800	71	173	410

As seen in Table 2.1, many different brands have EV models with different segments and features. The Volkswagen e-Golf model in the C-segment is given in Figure 2.1. Although it has a low battery capacity, the range of 190 km is sufficient, as the vehicles in the C-segment are generally intended for family use. In addition, its low energy consumption is the reason why this vehicle is preferred in this segment.



Figure 2.1 : Volkswagen e-Golf [25].

It has been observed that brands not only produce EVs in specific segments, but also in all segments to meet all demands. For example, the Porsche Taycan model in the E-segment, which is referred to as the luxury segment, is shown in Figure 2.2. As seen in Table 2.1, this vehicle has higher battery voltage, energy capacity, and consumption than the Volkswagen e-Golf.



Figure 2.2 : Porsche Taycan [26].

2.2.Charging Stations for EVs

Charging systems used to charge EV batteries can have different structures. Charging systems are divided into two categories according to the location of the charging unit; on-board and off-board. On-board charging systems are connected directly to the mains voltage with a suitable plug and provide one or three-phase AC to the voltage level suitable for the battery with the help of a rectifier and DC/DC converter inside the EV. Among on-board chargers, chargers with an output power of 2 kW or below

are classified as Level-1. Level-1 chargers have an AC single-phase supply and are commonly seen in household use. Chargers up to 20 kW power level are classified as Level-2, and although they usually have a three-phase supply, there are also those with a single-phase supply. They are usually used in places such as buildings and workplaces. The charging system, classified as Level-3, is in the off-board class. In these systems, the rectifier and DC/DC converter are located outside the EV, and the energy transfer via the plug is made directly to the battery in the EV. Since there is no space limitation in this system, charging can be done at higher power. Level-3 chargers, also called DC-Fast chargers, have an output power of between 50 and 900 kW. Since they are connected directly to the battery, their output voltage range is wide, and they are usually at 300-800 VDC levels. They are installed in public areas such as gas stations. They bring the battery above a certain charge level in a very short time so that EV batteries can be charged, especially on long roads. The parameters for the comparison of the charging stations are given in Table 2.2.

Table 2.2 : Comparison of charging stations [27].

Station Type	Charger Power (kW)	Supply Voltage (V)	Supply Current (A)	Charging Time for 20-50 kWh EV (h)
Level-1 (AC)	1.44-1.92	120/230 (AC)	12-16	11-36
Level-2 (AC)	3.1-19.2	208/240 (AC)	15-80	2-6
Level-3 (DC Fast)	50-350	300-600 (DC)	400 (Max.)	0.5

Although on-board chargers are usually designed and manufactured by automotive manufacturers, DC fast charger units are usually designed by different manufacturers. The biggest reason for this is the impact on the overall design of the vehicle, as on-board chargers are located on the EV. In addition, some manufacturers are working on bidirectional on-board chargers. The comparison of bidirectional on-board chargers produced by some manufacturers is given in Table 2.3.

Table 2.3 : Comparison of some bidirectional on-board chargers [28].

Manufacturer	Output Power (kW)	Output Voltage (V)	Input Voltage (V)	Efficiency
Texas Instruments	6.6	250-450	208-240	97%
Delta-q	6.6	250-450	85-265	96%
Current Ways	6.6	250-425	97-265	96%
Eaton	22	225-500	110-240	> 95%

The bidirectional on-board charger produced by Texas Instruments is shown in Figure 2.3. In order to increase the power density of on-board chargers, the use of WBG semiconductors is often preferred [29].

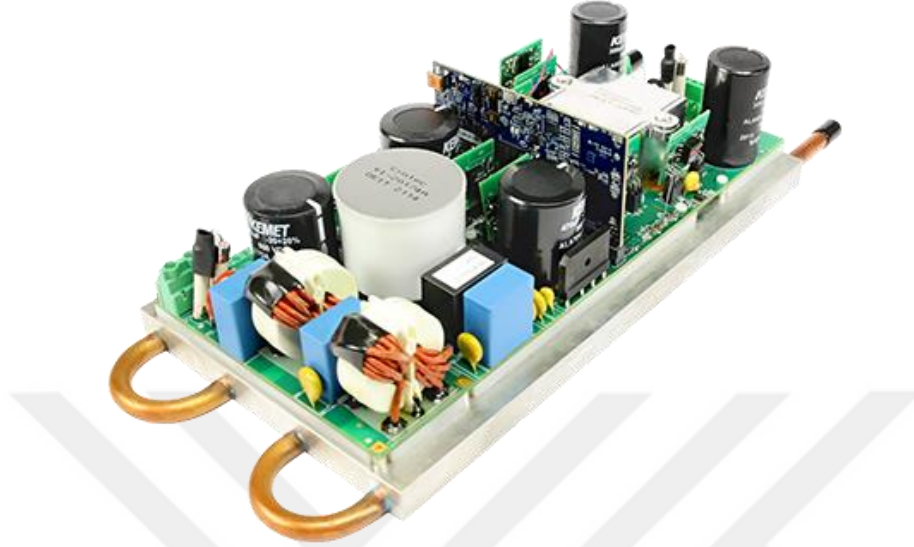


Figure 2.3 : Bidirectional on-board charger developed by Texas Instruments [29].

DC fast chargers, which are off-board chargers, are not directly connected to the vehicle as they are in the form of a separate station. Table 2.4 shows the DC fast charger models of different manufacturers.

Table 2.4 : Specifications of some DC fast chargers.

Model	Output Power (kW)	Output Voltage (V)	Output Current (A)	Supply Voltage (V)	Power Factor	THD	Efficiency
ABB Terra 54HV UL [30]	50	200-920	125	480±10%	>0.96	5%	95%
Wallbox Supernova [31]	60	150-500	150	400±10%	>0.98	5%	97%
Siemens VersiCharge Ultra 175 [32]	175	200-920	350	380-480	>0.99	<5%	98.5%
Tritium PK350 [33]	350	920	500	480	0.99	<5%	>98%

As can be seen in Table 2.4, there are DC fast chargers from many different manufacturers with different output powers. ABB Terra 54HV UL, with the widest output voltage range, is shown in Figure 2.4 (a), and Tritium PK350, with the highest output power, is shown in Figure 2.4 (b).



Figure 2.4 : (a) ABB Terra 54HV UL and (b) Tritium PK350 [30, 33].

On-board chargers and off-board chargers differ from each other in many ways. On-board chargers are supplied with AC voltage from the grid, rectify it in the vehicle, and apply it to the battery. Off-board chargers, on the other hand, have a rectifier and DC/DC converter. Off-board chargers apply DC voltage directly to the vehicle battery. The differences in the structure of on-board and off-board chargers are given in Figure 2.5.

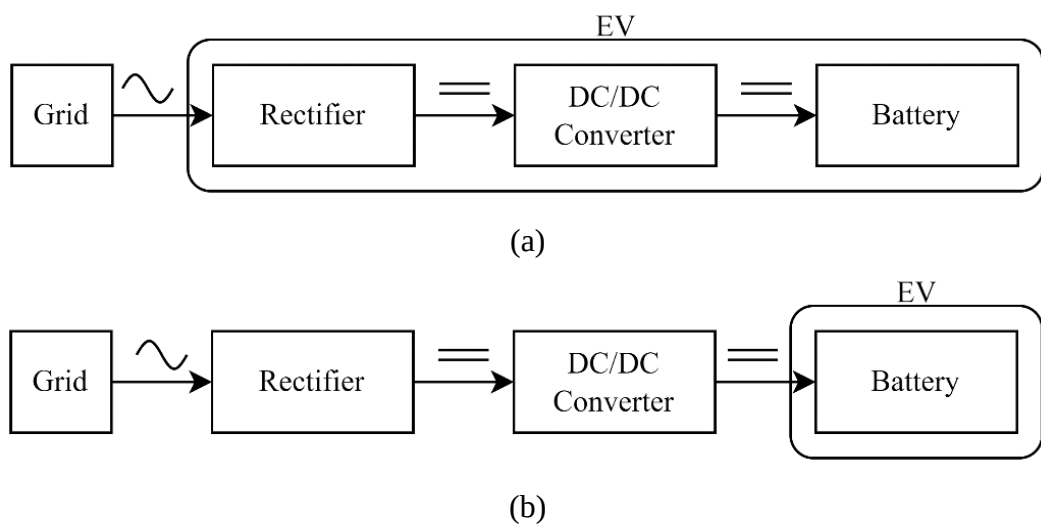


Figure 2.5 : Structures of (a) on-board and (b) off-board charger.

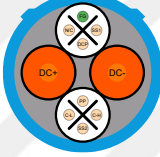
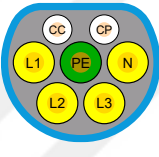
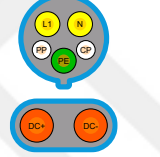
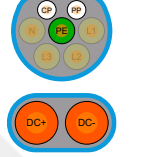
As seen in Table 2.1, different EVs have different battery voltages. The Volkswagen e-Golf has a battery voltage of 323 V, while the Porsche Taycan has a battery voltage of 800 V. Among the chargers given in Table 2.4, all of them except Wallbox Supernova are able to charge all the EVs given in Table 2.1. Wallbox Supernova, on the other hand, is not capable of charging Porsche Taycan due to its low output voltage. Therefore, when designing EV DC fast chargers, it is necessary to have a wide output voltage range and pay attention to the highest output voltage level.

As seen in Table 2.4, the general tendency is to have an output voltage range between 200 V and 900 V and a supply voltage range between 380 V and 480 V. A high power factor means that the reactive current to be drawn from the grid will be reduced and a lower conductor cross-section can be selected. Reducing the cooling requirement with high system efficiency provides a dimensional advantage and increases power density. High efficiency, high power density, low cost, low weight and small volume are the desired features of an EV charger. Battery lifetime and charging time are related to the chargers. THD must be very low to mitigate power quality issues [27].

Topologies where the direction of energy flow is in one direction are classified as unidirectional. In EV chargers designed using these topologies, the direction of energy flow is only from G2V. Many charging stations in use today are of this type. However, one of today's trends is to support the grid by providing energy flow from V2G. Bidirectional chargers are critical components of smart grid infrastructure, allowing peak load shaving, grid frequency, and grid voltage support. A charger capable of bidirectional power flow can be used in a smart grid to conduct grid support functions like as peak load levelling in V2G mode [34]. Unidirectional on-board chargers are popular due to their minimal battery deterioration and inexpensive hardware requirements. However, the current state of EV research has revealed its promise as a mobile energy source. On-board chargers can accomplish V2G capability by returning electrical energy to the grid, which might be useful during peak power needs. Many firms have shown an interest in producing bidirectional on-board chargers. Nissan, for example, has created vehicle-to-home capabilities for its 2013 Leaf model, and all next-generation Leaf vehicles will be capable of V2G functionality. Tesla and Chinese EV company BYD Tang established vehicle-to-load and vehicle-to-vehicle features in 2019. Most on-board chargers can attain 6 kW to 10 kW power levels in 2020, with some reaching up to 22 kW, like in the Renault Zoe [28].

According to the IEC 69196 standard, four different sockets with different characteristics are defined for DC fast chargers. In addition, these sockets also comply with some standards published by different organizations. The specifications of these sockets are as given in Table 2.5. The CHAdeMO socket is a Japan-based Toyota-led organization with the same name as the socket, which has set standards for this type of socket. Today, its use in Europe has also increased and many brands are compatible with this inlet. GB/T sockets are the ones that comply with the standards developed by China and are not common outside of China. The Combined Charging System (CCS), which has two different types, is the most common type used in North America and Europe. Apart from the IEC 69196 standard, Tesla has a charging system called Supercharger for its own EVs [35].

Table 2.5 : EV DC fast charger sockets according to IEC 69196 [36].

Standard	CHAdeMO	GB/T	CCS Type 1	CCS Type 2
Socket				
Maximum Voltage (V)	1000	1000	600	1000
Maximum Power (kW)	400	120	150	175

2.3.Batteries for EVs

Many different battery types have been used in EVs in the past and are still used today. Some of them are technologically older but are still preferable due to their cost. Lead-acid batteries are the type used in today's conventional vehicles and were used in the first EVs. Although their technology is mature, installation costs are low and self-discharge is low, they are weak in terms of specific energy and power. They also have long charging times and short cycle life [37].

NiMH batteries are characterized by their reasonable installation cost and satisfying specific energy and power ratings. Another advantage is their fast-charging capability. However, their major disadvantages are their high self-discharge rate and average cycle time. NiCd batteries are a technology with a low installation cost and average fast charging support and self-discharge rate. However, they have low specific energy

and power ratings [37]. Li-ion batteries, one of today's trending topics, have impressive specific energy and power, are generally fast rechargeable and have long cycle times. However, their major disadvantages are high installation costs and the need for a complex battery management system (BMS). The price of a Li-ion battery has dropped from 1,000 \$/kWh to 120 \$/kWh during the previous 20 years, while the energy density has increased from 90 Wh/kg to 300 Wh/kg [38]. The C-rate of Li-ion batteries should also be mentioned. C-rate is a measure of the current that can be withdrawn or transferred from the battery to the nominal current. It can be used to calculate the charging or discharging time of the battery. The higher the C-rate, the shorter the charging or discharging time.

One of the reasons why Li-ion batteries are preferred for use in EVs is their charging efficiency of over 99% [39]. Li-ion batteries can be found in many different structures. Each of these structures has its own advantages and disadvantages. Table 2.6 shows the comparison of the specific energy, specific power, cost, and lifespan of different Li-ion batteries. LiCoO₂ represents lithium cobalt oxide, LiMn₂O₄ represents lithium manganese oxide, LiFePO₄ represents lithium iron phosphate, NMC represents lithium nickel manganese cobalt oxide, NCA represents lithium nickel cobalt aluminum oxide, and Li₄Ti₅O₁₂ represents lithium titanate.

Table 2.6 : Comparison of Li-ion battery types [39].

Battery Type	Specific Energy	Specific Power	Cost	Lifespan
LiCoO ₂	High	Low	Medium	Low
LiMn ₂ O ₄	Medium	Medium	Medium	Low
LiFePO ₄	Low	High	Medium	High
NMC	High	Medium	Medium	Medium
NCA	High	Medium	Low	Medium
Li ₄ Ti ₅ O ₁₂	Low	Medium	Lowest	High

The most preferred Li-ion battery types in Table 2.6 are NMC, LiFePO₄ and LiMn₂O₄ [39]. LiFePO₄ is characterized by its long life and high specific power. NMC, on the other hand, has optimized characteristics in every aspect.

One of the issues that should be mentioned in batteries is State-of-Charge (SOC), which shows how much energy the battery is currently charged with, and State-of-Health (SOH), which shows how much energy the battery can store compared to its initial state. SOC is expressed as a percentage and is an indication of how much of the

available energy is charged. Different methods, such as Coulomb counting, can be used to determine SOC. SOH is an indicator of the available capacity of the battery compared to the energy capacity for which the battery was originally designed. Methods such as the change in the internal resistance of the battery can be used in its calculation. For sufficient performance and longer battery life, it is desired that the SOC not fall below 20%. In addition, batteries with a SOH level of below 80% usually do not provide the desired performance.

There are three basic methods for charging EV batteries. These are constant voltage (CV), constant current (CC), and constant power (CP) charging. Table 2.7 shows a comparison of these methods. CV charging provides a long battery life, while charging is done more slowly. While CC charging provides fast charging, battery life is shorter than with CV charging. There are also methods called CV-CC combined charging and multistage charging where these methods are used together. With CP charging, CV-CC combined charging, and multistage charging, a more optimized battery life, thermal performance, and charging time can be achieved. The main disadvantage of CP and multistage charging is that they have complex control algorithms [40].

Table 2.7 : Comparison of charging modes.

Mode	CV	CC	CP	CV-CC
Voltage	Constant	Variable	Variable	Variable
Current	Variable	Constant	Variable	Variable
Power	Variable	Variable	Constant	Variable

The most widely used method in EV batteries today is the CV-CC combined charge mode. The reason for this preference is that it uses an easier control method compared to CP and multistage charging and optimizes battery life and charging time. In this method, CC is first performed up to a certain SOC, and then the charging process is completed with CV [40]. Multistage charging is a similar process. In addition to CV-CC charging, it also includes a stimulating charge and a balancing charge at the end. Figure 2.6 shows the charging characteristics of a battery in CV-CC combined charge mode. As can be seen, the voltage applied to the battery is increased continuously in the charging process, which initially starts in CC mode. After the SOC reaches a certain level in a linear way, it is switched to CV mode. In CV mode, the current decreases over time depending on the SOC. When the SOC reached 100%, the charging process was over.

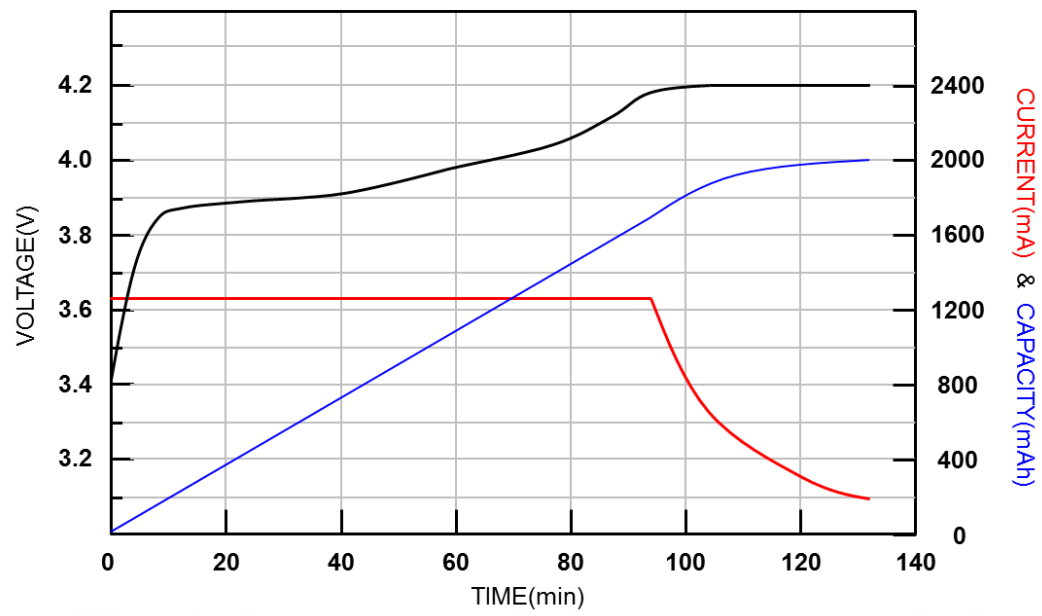


Figure 2.6 : CV-CC combined charging characteristic [41].

3.TOPOLOGIES USED IN ELECTRIC VEHICLE DC FAST CHARGERS

EV DC fast chargers consist of a connection filter, a three-phase rectifier, and a DC/DC converter. The general structure is as given in Figure 3.1. For safety purposes, there must be isolation between the battery and the grid. This isolation can be provided by an isolation transformer on the grid side or by an isolated DC/DC converter [35]. An isolation transformer on the grid side is disadvantageous in terms of size since it will operate at the grid frequency. However, the isolation provided on the DC/DC converter provides a great dimensional advantage since it is provided with the help of a transformer operating at a high frequency. The advantage of the transformer used on the grid side is the use of a smaller grid connection filter.

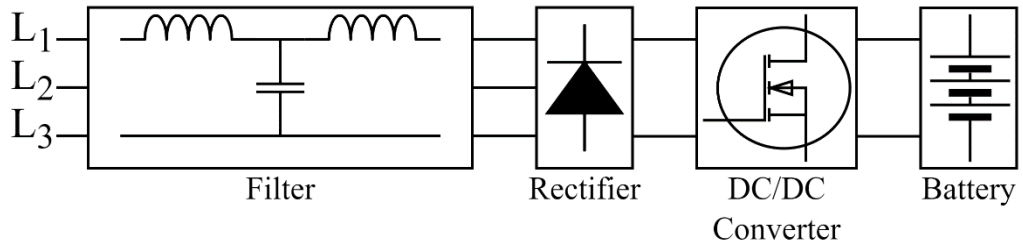


Figure 3.1 : General structure of DC fast charger.

The structure of the isolation transformer on the grid side is shown in Figure 3.2. The output of the isolation transformer is rectified by passing through a filter. The generated DC-link voltage is converted to a suitable level for the battery with the help of a DC/DC converter and applied to the battery. In these types of structures, it is common to use simpler topologies such as buck converters as well as DC/DC converter topologies.

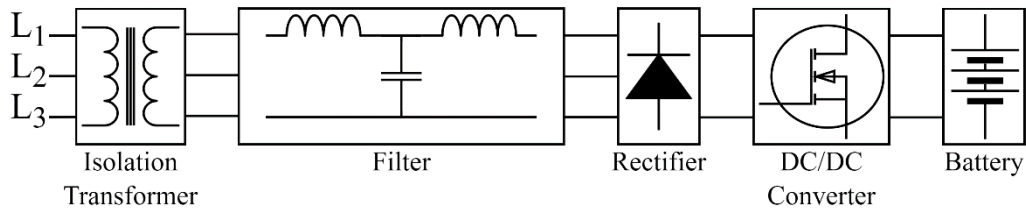


Figure 3.2 : Structure with grid side isolation transformer.

Figure 3.3 shows the structures where the isolation is done on the DC/DC converter side. After passing through the filter, the rectified voltage is converted to high frequency AC. The voltage at the output of the high-frequency transformer (HFTR) is rectified again with the help of a rectifier and applied to the battery. It is common to use phase-shifted full-bridge (PSFB), DAB, etc. in such structures.

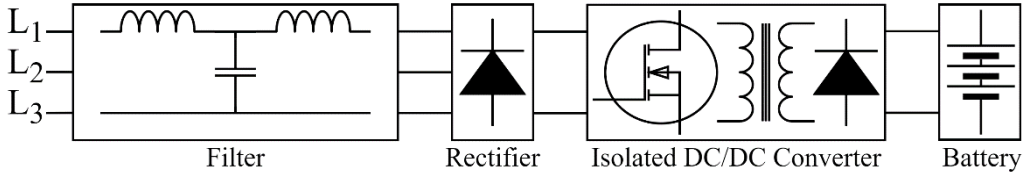


Figure 3.3 : Structure with isolated DC/DC converter.

Since it can be difficult to reach high power levels with a single unit, modular structures are often used. In this way, high-power stations can be built by connecting lower-power charger modules in parallel. An example of this is the Tesla Supercharger. Tesla Supercharger has a 135 kW station with the combination of 12 11.25 kW modules [42].

3.1.Filter Topologies for EV DC Fast Chargers

In grid-connected systems, different filter topologies are used to reduce the harmonics and noise generated by the system on the grid. The major source of issues with connected loads or sensitive equipment is harmonics generated on the power conversion device switching. During the systems design stage, the cost of filters and THD are key factors to take into account. Due to price increases and poor dynamic responses, high inductance values make it more challenging to implement useful filters. Filter topologies such as L, LC, and LCL are frequently used. Each has different advantages and disadvantages. For example, although LCL filters are very successful in filtering high frequency harmonics, they generate a resonance risk at some frequencies [43].

Figure 3.4 shows the structure of different filter topologies. Figure 3.4 (a) shows an L filter with only a single inductor, (b) an LC low-pass filter, (c) an LCL filter, (d) an LCL filter with a damping resistor, and (e) an LCL filter with a trap filter and a damping resistor tuned to a specific frequency. In this section, the characteristics and frequency responses of each topology will be analyzed and compared. The advantages

and disadvantages of topologies and the systems in which they should be preferred will be discussed. The modeling used to compare the topologies was done in PLECS, a specialized package program for power electronic circuits.

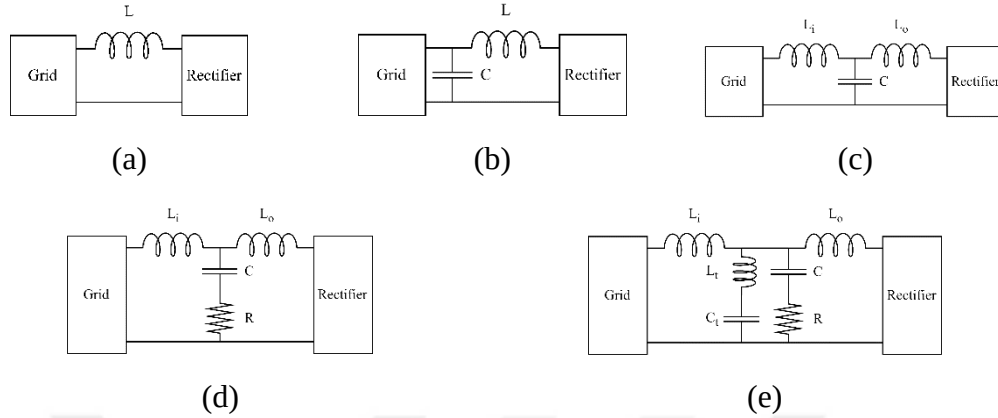


Figure 3.4 : (a) L filter, (b) LC filter, (c) LCL filter, (d) LCL filter with damping resistor and (e) LCL filter with a trap filter and damping resistor.

3.1.1.L filter

It is the simplest and first order filter structure. It has a damping performance of 20 dB/decade at all frequencies. They are usually used in systems with very high frequencies, and the inductance value must be chosen high for better damping performance. Therefore, they reduce the system response. They are generally easier to design. The transfer function is given in equation 3.1. L represents the inductance value. The model and frequency response are given in Figure 3.5 (a) and (b).

$$\frac{I_{\text{grid}}(s)}{V_r(s)} = \frac{1}{sL} \quad (3.1)$$

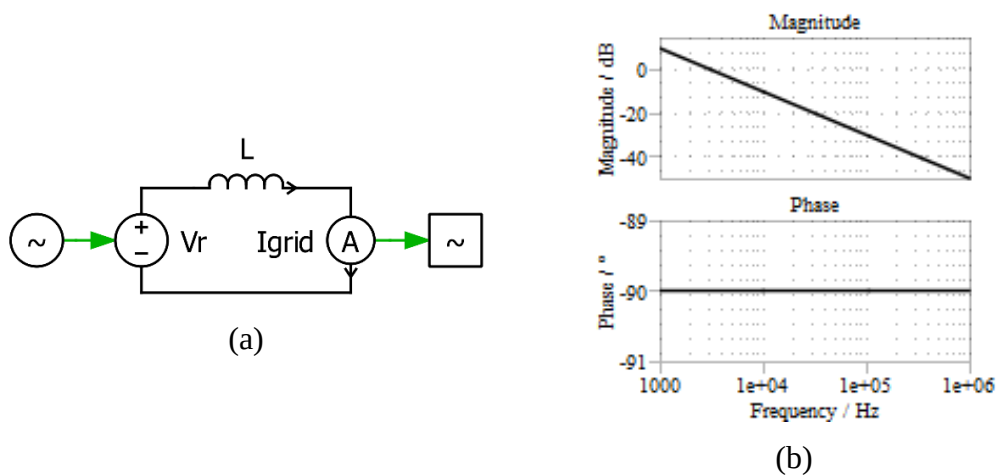


Figure 3.5 : L filter (a) simulation model and (b) frequency response.

3.1.2.LC filter

The LC filter, a second-order filter type, has better damping performance than the L filter. They are also known as low-pass filters. Its design is simple due to the simplicity of its structure. They usually operate trouble-free with good performance. The structure has no gain at frequencies below the resonant frequency and has a damping performance of 12 dB/decade at frequencies above resonant frequency [43]. The simulation model of the LC filter, whose transfer function is given in equation 3.2, is shown in Figure 3.6 (a), and the frequency response is shown in Figure 3.6 (b). L represent the inductance value, and the C represents the capacity of capacitor. For performing the simulations, a damping resistor (R) is added to grid side of the filter.

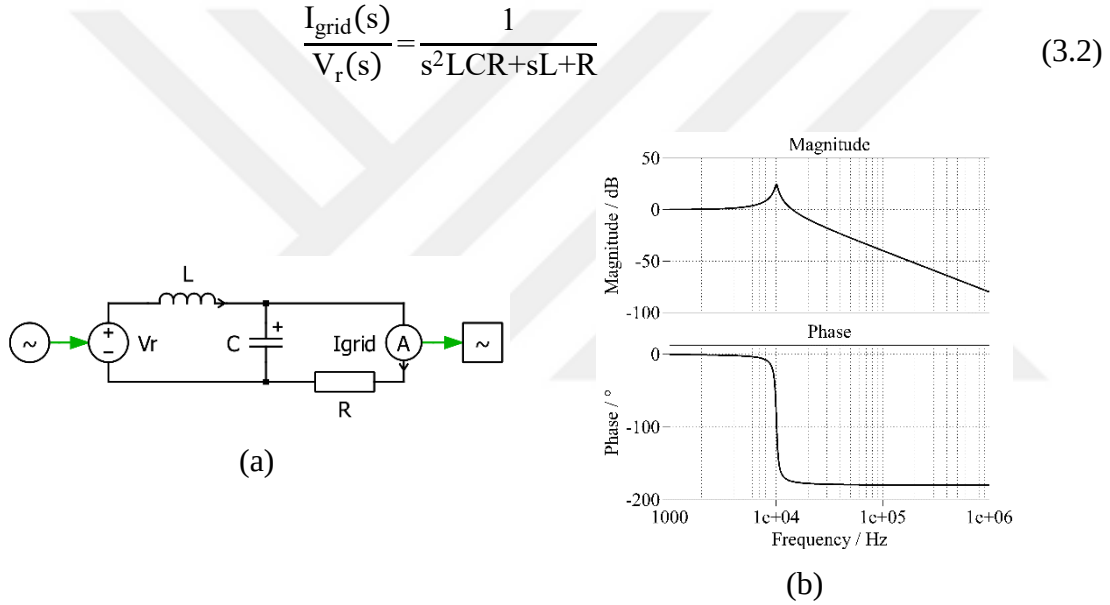


Figure 3.6 : LC filter (a) simulation model and (b) frequency response.

The high capacitance of the capacitor improves the voltage quality, while resonant frequency can be adjusted to the desired value with a high inductance value. The biggest disadvantage of this structure is that it has a filtering characteristic that depends on the grid inductance. Therefore, it causes some difficulties in practice [43].

3.1.3.LCL filter

The LCL filter, which is the preferred one in many applications, is much more successful than the L and LC filter, especially at low switching frequency with a damping performance of 60 dB/decade. By selecting a lower switching frequency, the switching losses on the switching circuit can be reduced. In addition, with lower

switching frequency, the DC-link capacitors of the power circuit are less stressed and their lifetime is extended. Considering that the losses of the cores used in inductance designs also increase in proportion to the frequency, it is a great advantage to provide great flexibility in the selection of switching frequency. Figure 3.7 (a) shows the simulation model of the LCL filter, and Figure 3.7 (b) shows the frequency response. L_i is the grid side inductance and L_o is the rectifier side inductance.

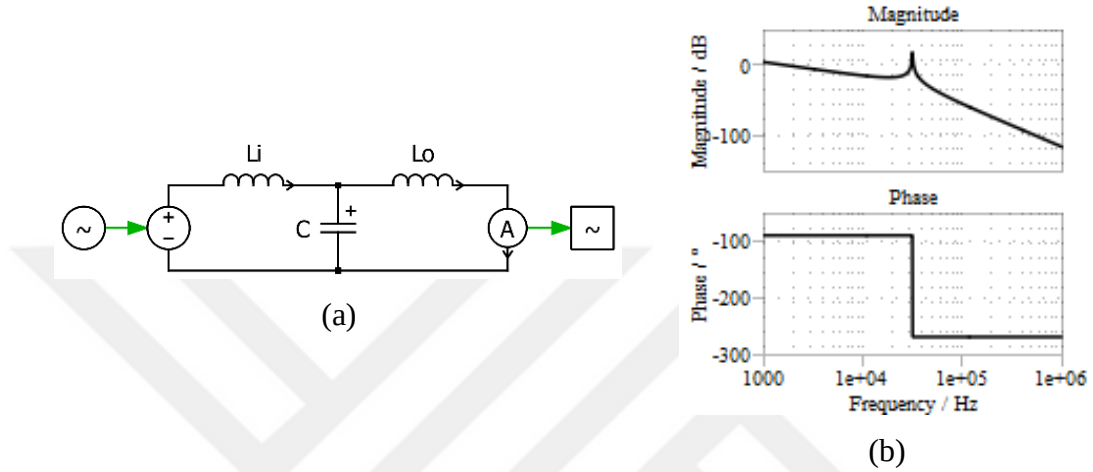


Figure 3.7 : LCL filter (a) simulation model and (b) frequency response.

As seen in Figure 3.7 (b), the frequency response has a peak at a specific frequency. The frequency value of the peak here is resonant frequency and depends on the inductors and capacitance. This frequency value can be found with equation 3.3.

$$f_{\text{res}} = \frac{1}{2\pi} \sqrt{\frac{L_i + L_o}{L_i L_o C}} \quad (3.3)$$

It is necessary to select switching frequency far away from resonant frequency to avoid any problems in the operation of the system. Resonance is a problem when building the LCL filter because it can disrupt the system. This problem may be solved by passive and active damping methods based on resistors, as well as a controller. The design process is iterative, requiring concern about the resonant frequency, voltage drop, maximum output current ripple, THD, and damping technique [44].

3.1.4. LCL filter with damping resistance

It shows similar characteristics to the LCL filter mentioned in the previous section. The simplest solution is to use a damping resistor as a method of damping the amplitude of the resonance point. With the help of a damping resistor connected in

series to the capacitor, the peak at resonant frequency can be damped depending on R. Although the added damping resistor slightly reduces the damping effect at high frequencies, it provides a simple and satisfactory solution. Figure 3.8 (a) shows the simulation model and Figure 3.8 (b) shows the frequency response. Compared to Figure 3.7 (b), it can be seen that the peak at resonant frequency is reduced.

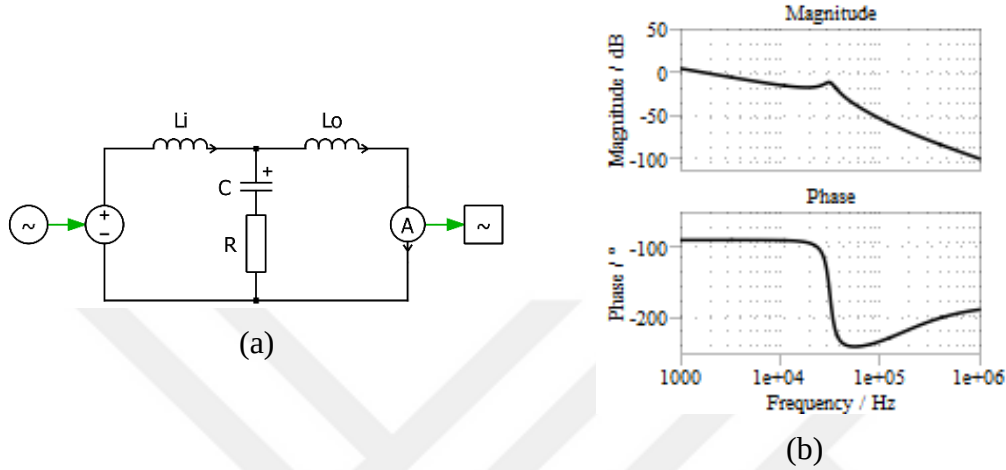


Figure 3.8 : LCL filter with damping resistance (a) simulation model and (b) frequency response.

The choice of the damping resistor to be used is important. Because while it should be able to damp the peak at the appropriate level, it should not reduce the high frequency damping characteristic. According to a research, damping resistor values (R) can be selected as in equation 3.4 depending on C and resonant frequency [43]. However, when designing this filter topology, it is important to use an iterative method and test the iterations with analysis programs to arrive at the final design.

$$R = \frac{1}{6\pi f_0 C} \quad (3.4)$$

In the next section, one more branch will be added to the LCL filter with a damping resistance topology, and the change in filtering performance with the trap filter tuned to a specific frequency will be analyzed.

3.1.5.LCL filter with damping resistance and trap filter

Inductance and capacitance connected in series with each other create a resonance point. By connecting the branches formed in this way in parallel to C, the frequency at this point is filtered. This branch is called a trap filter. Figure 3.9 (a) shows the L_t trap inductance and C_t trap capacitor in the simulated topology. The frequency response of

this topology is depicted in Figure 3.9 (b). As can be seen from the frequency response, the trap filter can filter the frequency at which it is tuned at a very high level. However, there is an additional resonance point in the system. This peak is not very high and can be reduced by adjusting the damping resistor value.

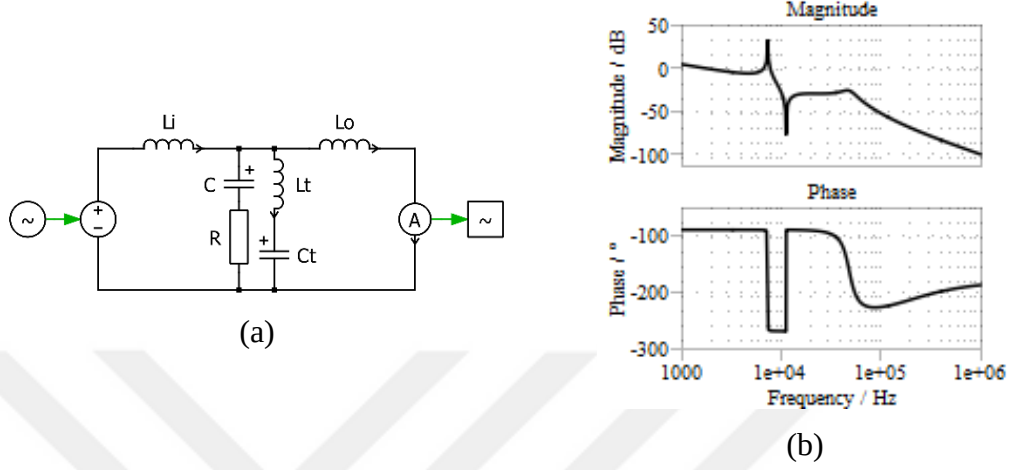


Figure 3.9 : LCL filter with damping resistance and trap filter (a) simulation model and (b) frequency response.

The tuning frequency (f_{tune}) of the trap filter can be calculated as in equation 3.5. By adjusting the values of L_t and C_t , the amplitude and width of the damping at the resonance point can be changed. Increasing the inductance reduces the damping performance but improves the filtering performance at nearby frequencies.

$$f_{\text{tune}} = \frac{1}{2\pi\sqrt{L_t C_t}} \quad (3.5)$$

More than one trap filter can be added to the topology according to the need. Since each trap filter will have a different f_{tune} , different frequencies can be filtered in this way. In particular, it is common to use trap filters tuned to switching frequency and twice the switching frequency according to the need. If the damping performance of the LCL filter at these frequencies is sufficient, there is no need to use a trap filter and it can only cause extra loss in the system.

3.2.Rectifier Topologies for EV DC Fast Chargers

EV DC fast chargers need a rectifier after the grid connection filter. With the rectifier, the grid voltage is rectified and then energy is transferred to the battery with the DC/DC converter. Although structures such as bridge diode rectifiers are the easiest

structures to use, the THD values of the current they draw from the grid are very high. In addition, since their output voltage drops depending on the load, it is quite problematic to obtain a constant DC-link voltage. Therefore, topologies that can control the output voltage and do not cause THD problems are used.

Obtaining a constant DC-link voltage is essential for the DC/DC converter to operate efficiently and with good performance. In addition, it has been mentioned in the previous sections that the effects of the system on the grid must comply with the standards. For this purpose, it is necessary to use a topology that can control the output voltage with PFC capability. Rectifier topologies can be divided into two categories: unidirectional and bidirectional. If the energy flow direction will be both G2V and V2G, bidirectional topologies should be chosen. It can also be classified as a 2-level topology or a multilevel topology according to the output voltage level. The output voltages of 2-level topologies have only negative and positive terminals. Multilevel topologies have different levels of output voltages according to their level. 3-level topologies have zero-level output in addition to positive and negative terminals.

2-level topologies are easy to control and can be realized with a lower number of switching elements. As the level of multilevel topologies increases, the number of switches increases and control becomes more difficult. However, they have a much better current and voltage regulation capability. The most widely used type of multilevel topology in applications is the 3-level topology. Compared to 2-level topologies, 3-level topologies also have higher output voltage.

In the following part of this chapter, the rectifier topologies that can be used will be discussed. Since 2-level topologies and 3-level multilevel topologies are the most commonly used ones, only these structures will be evaluated. Among the one-level rectifiers, the boost PFC rectifier, six-switch boost PFC rectifier, buck type PFC rectifier, and Swiss rectifier are the first topologies to be examined. Then the chapter will be concluded with the 3-level topologies of T-type, neutral point-clamped (NPC), and active neutral point-clamped (ANPC) rectifiers.

3.2.1. Boost PFC rectifier

This topology is a boost converter topology following a diode three-phase bridge rectifier structure. The biggest advantage of this topology is that it can be implemented with a single controlled switching element. However, it cannot reduce the THD

sufficiently compared to many other topologies. The topology shown in Figure 3.10 consists of six diodes and one controlled switch. The inductance at the entrance of the topology symbolizes the grid connection filter. The inductance after the bridge diodes is for boost purposes. It increases the voltage and brings it to the desired level. This topology is a unidirectional topology and can be used for just V2G operation.

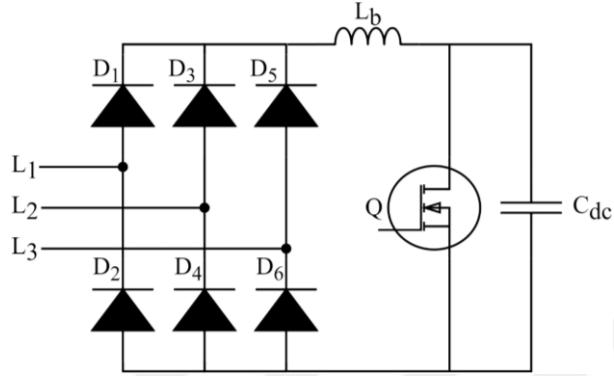


Figure 3.10 : Boost PFC rectifier topology.

3.2.2. Six-switch boost PFC rectifier

This 2-level topology works similar to a boost converter. The structure shown in Figure 3.11 can be realized using six switching devices. It is the simplest PFC rectifier topology to construct and control. It allows bidirectional energy flow. The output voltage in this topology can be adjusted to the desired level. The inductance shown in Figure 3.11 represents the boost inductance. Usually, the inductance of the grid connection filter is used for this purpose. The main advantage of this topology is that it is especially efficient at low frequencies due to the small number of switching elements. In addition, successful results can be achieved with the help of a simple controller. However, the output voltage is lower compared to multilevel topologies.

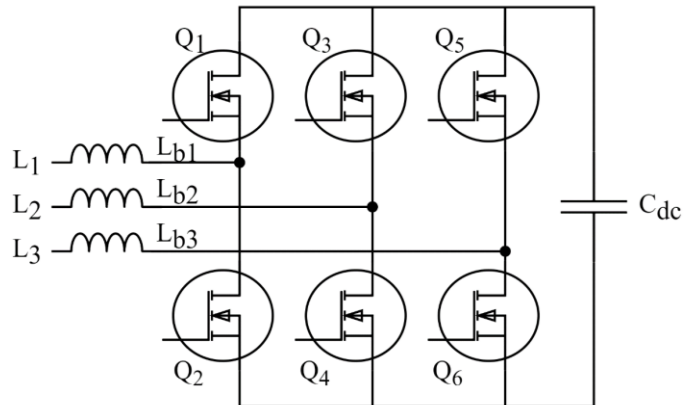


Figure 3.11 : Six-switch boost PFC rectifier topology.

3.2.3. Buck type PFC rectifier

This unidirectional and 2-level topology is similar to the 6-switch boost PFC rectifier. While the six-switch boost PFC rectifier increases the DC link voltage, in the buck type PFC rectifier the output voltage is lower. On the grid connection side, a filter is still required, but the structure is different. The topology is shown in Figure 3.12. This topology can be realized by using six diodes and six controlled switching elements. Like other 2-level topologies, the THD ratio is higher than multilevel topologies.

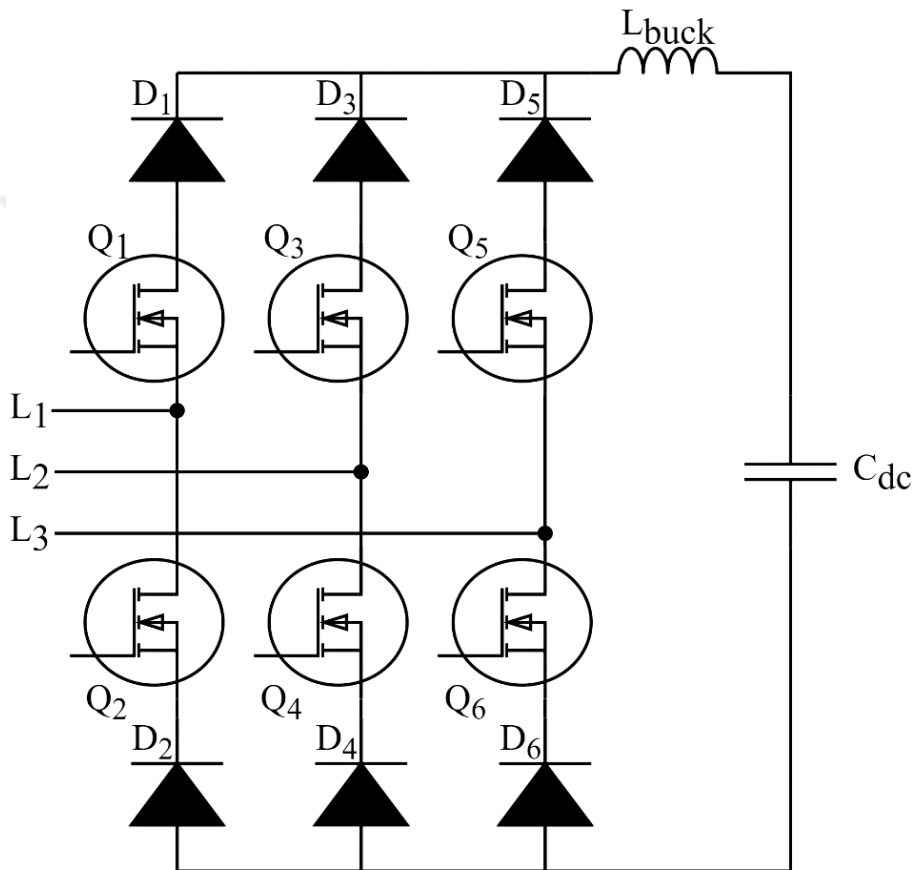


Figure 3.12 : Buck type PFC rectifier topology.

3.2.4. Swiss rectifier

This topology is a unidirectional, 2-level topology. The high number of switching elements is one of its major disadvantages. It can be realized using eight diodes and eight controlled switching elements. Therefore, its control is more complex than other 2-level topologies. However, one of its advantages is that it offers a better THD ratio. Figure 3.13 shows this topology. The high number of switching elements causes high conduction losses and switching losses.

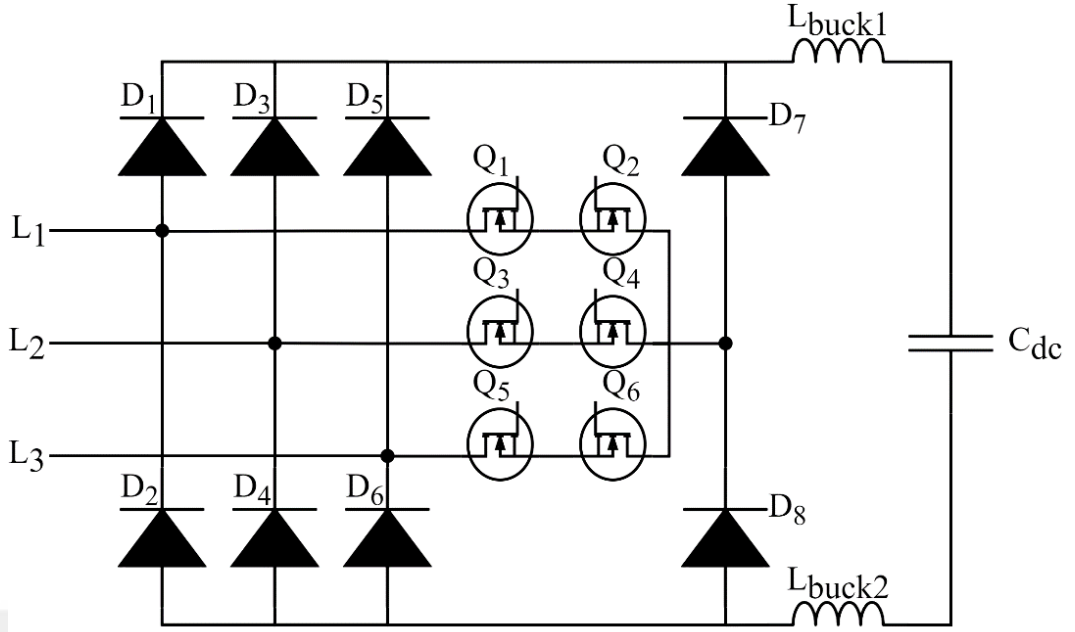


Figure 3.13 : Swiss rectifier topology.

The topologies mentioned up to this point are 2-level topologies, and in general, their biggest disadvantages are that they cannot obtain a DC link voltage of sufficient magnitude and that the THD of the current they draw from the grid is high. But despite this, they are generally simpler and easier to control. Therefore, the 6-switch boost PFC rectifier is one of the most preferred topologies. In the rest of the rectifier topologies, 3-level rectifiers will be discussed. Since these topologies are also used in grid-connected inverters, the THD of the grid current is lower and they can provide much better voltage regulation.

3.2.5. Vienna rectifier

Vienna rectifier was patented in 1994 by John W. Kolar [45]. This topology, which is increasing in popularity and use today, is a 3-level topology. It is easier to control than other 3-level topologies because it uses fewer controlled switching elements than other 3-level topologies. The topology shown in Figure 3.14 can be realized with eighteen diodes and three controlled switching devices. While the diodes perform the rectification functions, the controlled switching elements stabilize the bipolar voltage at the output of the DC link and reduce the THD of the current drawn from the grid.

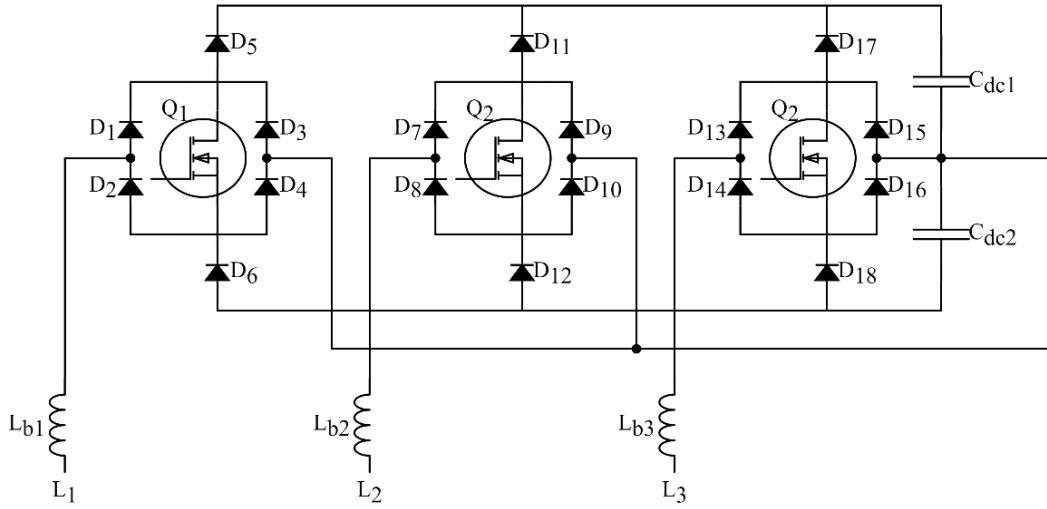


Figure 3.14 : Vienna rectifier topology.

3.2.6. T-type rectifier

The biggest disadvantage of this topology, which can be realized with twelve controlled switching devices, is the high voltage stress on the switching devices. Like the Vienna rectifier, it has a bipolar and balanced output voltage, and the THD of the current drawn from the grid is low. Due to the high voltage stress on the switching elements, the switching losses are also high. Therefore, it is not preferred to be used with high switching frequency. The topology is given in Figure 3.15.

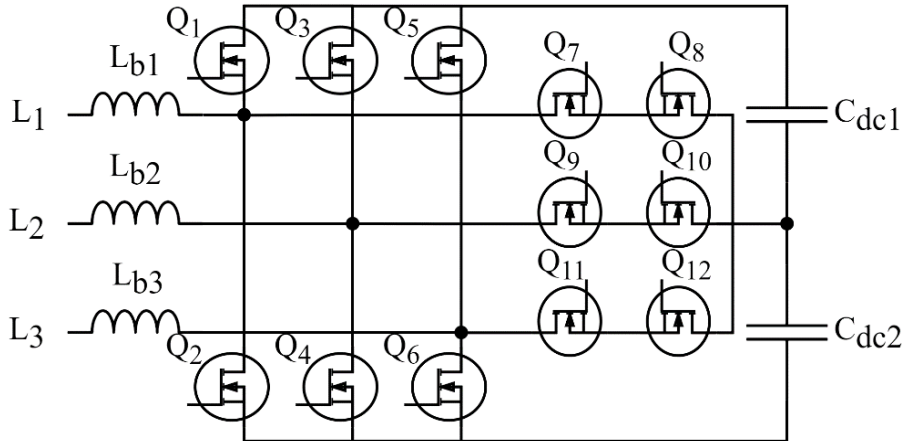


Figure 3.15 : T-type rectifier topology.

3.2.7. Neutral point-clamped rectifier

The NPC rectifier is a boost-type converter. This 3-level topology allows for the use of devices with lower voltage ratings, which can give fewer switching losses at a reasonable cost. According to some reports on a 30 kW EV charger prototype with an NPC rectifier that delivers low THD input current. Another benefit of utilizing an NPC

rectifier is that it produces a bipolar DC link expressly [35, 46]. NPC rectifier topology can be realized with six diodes and twelve controlled switching devices. As can be seen in the topology shown in Figure 3.16, the switching devices are connected in series with each other. This reduces the voltage stress on the switching devices by half compared to the T-type rectifier. In this way, higher switching frequency can be achieved. It has a bipolar and balanced output voltage and the THD of the current drawn from the grid is low.

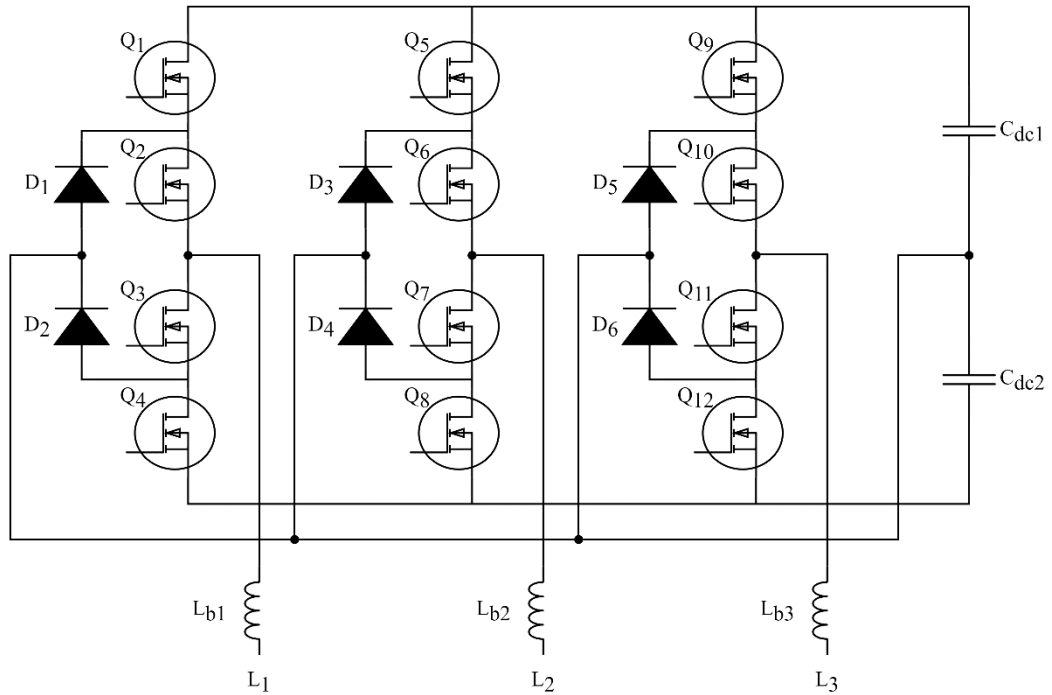


Figure 3.16 : NPC rectifier topology.

3.2.8. Active neutral point-clamped rectifier

ANPC rectifier topology is the replacement of the six diodes in the NPC rectifier topology with controlled switching devices. In this way, lower conduction losses can be achieved with controlled switching devices instead of high conduction losses due to the voltage drops of the diodes. In addition, higher switching frequency can be achieved by reducing the switching losses caused by the reverse recovery charge of the diodes. The topology can be realized with eighteen controlled switching elements as shown in Figure 3.17.

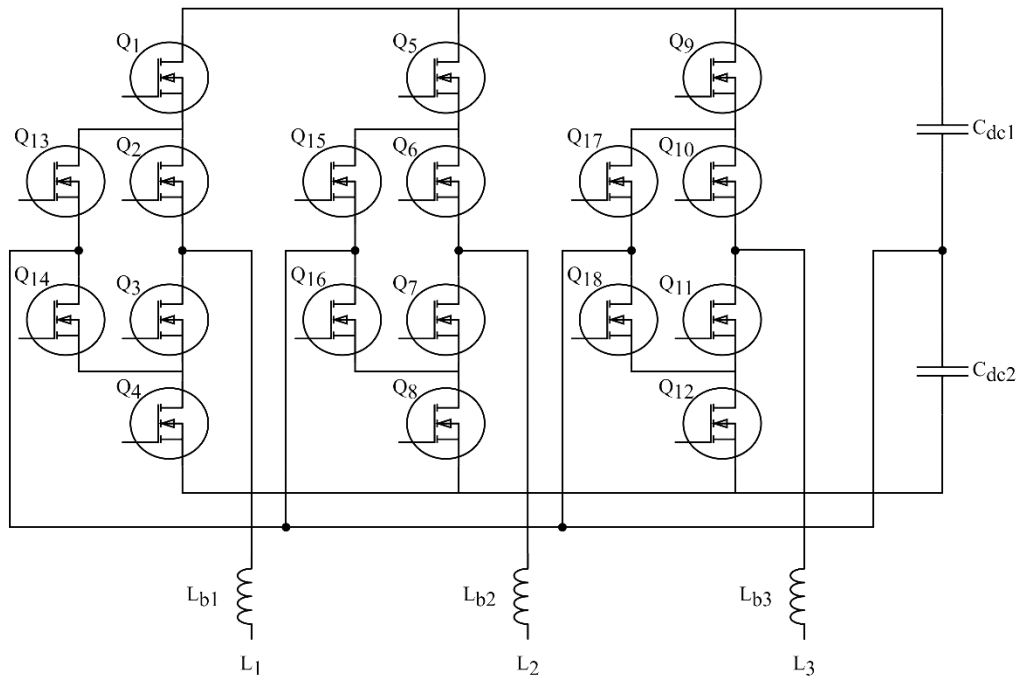


Figure 3.17 : ANPC rectifier topology.

Depending on the control method in ANPC rectifier topology, some switching devices can be made to switch at grid voltage. In this way, the efficiency of the rectifier can be increased by reducing the switching losses generated by these switching devices. Low switching losses at higher switching frequency can be achieved by using WBG switching devices in other switching devices. Higher switching frequency reduces the size of the magnetic components to be used and increases the capacitor life.

A summary of rectifier topologies is given in Table 3.1. As can be seen, in topologies where bidirectional energy flow is possible, the number of controlled switching devices is also higher. In addition, topologies with bipolar DC link voltages also increase the number of switching devices. Topologies with a high number of controlled switching devices are generally more complex to control and require more measurements and calculations. Generally, these topologies have lower THD values. One of the most important criteria in selecting a rectifier topology is to determine whether the direction of energy flow is unidirectional or bidirectional. Then, considering the DC/DC converter topology and the system structure, the requirement for the bipolar DC link voltage should be considered. Accordingly, the choice of the optimum topology affects both system efficiency and cost.

Table 3.1 : Summary of rectifier topologies.

Topology	Controlled Switching Devices	Diodes	Bidirectional	Bipolar DC Link Voltage	THD	Conduction Loss	Switching Loss	Efficiency	Cost	Power Density
Boost PFC rectifier	1	6	No	No	Highest	Highest	Lowest	Low	Low	Low
Six-switch boost PFC rectifier	6	0	Yes	No	High	Low	High	Low	Low	Low
Buck type PFC rectifier	6	6	No	No	High	High	Low	Low	Mid	Low
Swiss rectifier	8	8	No	No	Low	High	Mid	Mid	Mid	Mid
Vienna rectifier	3	18	No	Yes	Very Low	High	Mid	High	Mid	High
T-type rectifier	12	0	Yes	Yes	Very Low	Mid	Mid	High	Mid	High
NPC rectifier	12	6	Yes	Yes	Very Low	High	Low	Very high	High	Higher
ANPC rectifier	18	0	Yes	Yes	Very Low	High	Low	Highest	High	Higher

3.3. DC/DC Converter Topologies for EV DC Fast Chargers

The battery connection converter is a DC/DC converter that supplies the necessary DC voltage to the battery while maintaining high efficiency, soft-switching capabilities, and minimal ripple and electromagnetic interference (EMI). The voltage output ripple can be reduced by increasing the converter's switching frequency or filter size. To reduce switching losses, soft switching strategies like as ZVS and ZCS are used [47]. Galvanic isolation is critical to keep the isolation between the grid and the battery so that the battery protection continues untouched by the charger since the EV's battery must not be grounded at all times. This is possible with an isolated DC/DC converter [35].

One of the most desirable features of a DC/DC converter is a wide output voltage range. As mentioned in the previous sections, EV batteries have different voltages. Also, depending on the charging strategy, higher voltages need to be provided by the DC/DC converter. In addition, for a high power density system design, a highly efficient topology should be used to minimize losses. For this purpose, isolated DC/DC converters used in EV fast DC chargers will be analyzed. Within the scope of this study, topologies with a full-bridge (FB) structure on the input side will be discussed.

In several situations, the number of active devices in a topology is reduced. Using the half-bridge equivalents of the converters is one approach to do this. Because half-bridge converters require only four active switches, they are less expensive. When compared to the FB configuration, the applied voltage is half of the DC link voltage. When operated in medium voltage applications, this property benefits the HFTR design. However, the active device's current stress is doubled, and the variables available for converter control are decreased [35].

3.3.1. Phase-shifted full-bridge converter

PSFB converter is one of the most popular topologies. The main reasons for this are the simplicity of the topology as well as the ease of control. The topology with unidirectional energy flow is shown in Figure 3.18. Depending on the situation, it can be realized with a center-tapped transformer and rectifier instead of a FB rectifier. At the battery end, a PSFB converter consists of a FB converter followed by a HFTR and

a rectifier. To balance the flux in a transformer core, peak current mode control or voltage mode control is performed [47].

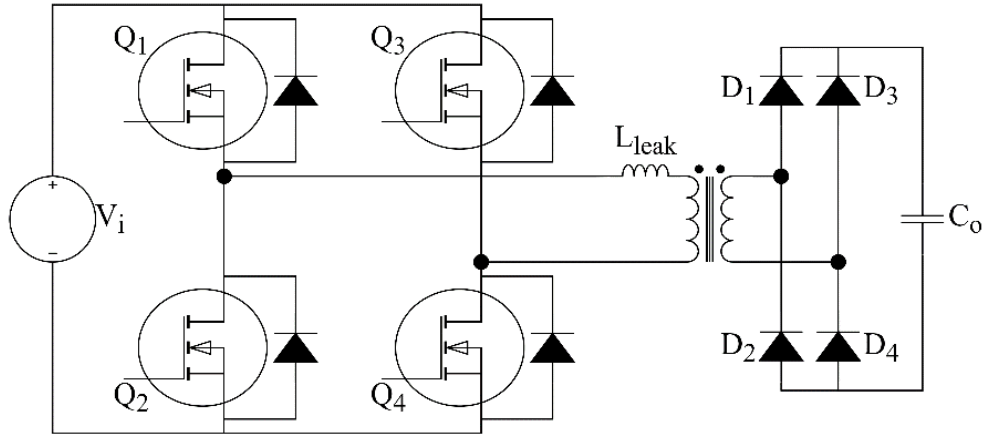


Figure 3.18 : Phase-shifted full-bridge converter topology.

3.3.2.LLC resonant converter

Another widely used unidirectional topology is the LLC resonant converter. Although it has better efficiency than the PSFB converter, it is more difficult to control. Low turn-off losses and low transformer losses are produced as a result of the LLC converter's use of the magnetizing current to accomplish ZVS. By adjusting the switching frequency, the impedance ratio of the resonant tank to equivalent load is changed, hence controlling the converter output voltage. Its limited capacity to regulate light loads' power and the possibility that the ZVS state won't persist throughout a large working range, however, have an adverse effect on efficiency [35]. Figure 3.19 shows the topology. According to PSFB, one capacitor is added to the input of the transformer. Usually, the leakage inductance is used in the resonant tank, but if it is insufficient, an additional inductance can be added.

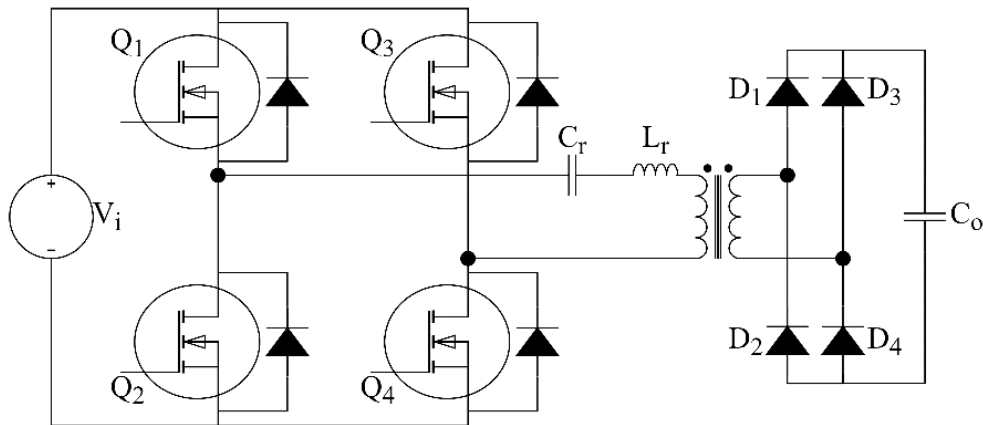


Figure 3.19 : LLC resonant converter topology.

Operating at high efficiency over a wide output voltage range is one of the disadvantages of this topology. The performance over a wide output voltage range and under light load situations is improved using a number of techniques. Different modulation techniques are suggested to constrain the operating frequency range while expanding the output range. Another disadvantage is that the capacitor in the resonant tank is under high voltage stress [35]. One of the reasons why this topology is not preferred is the difficulty of finding a capacitor that can withstand high voltage stress and has a high current capacity, or the difficulty of designing a suitable capacitor group.

3.3.3. Dual active bridge converter

It is a topology obtained by connecting two FBs through one HFTR. This topology, shown in Figure 3.20, allows bidirectional energy flow. DAB converter can be used with different controller structures and modulation techniques and thus has many advantages. Due to its ability to soft switch, DAB converter is widely utilized. The transformer's leakage inductance can also be collected by the resonant inductance. With ZVS, switching losses can be reduced and efficiency can be increased [48].

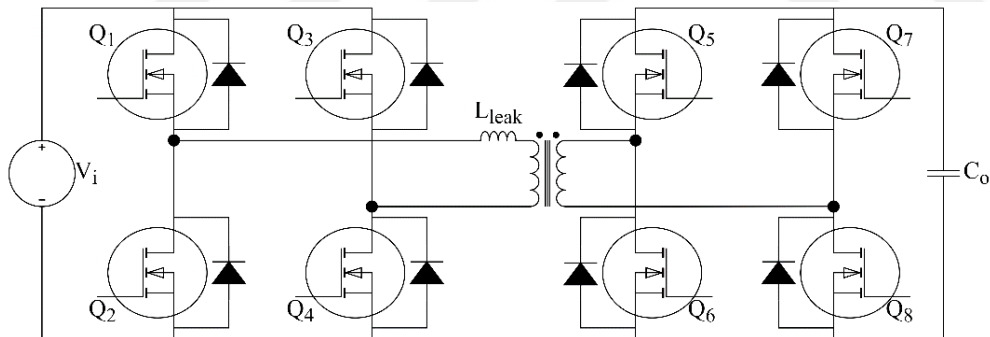


Figure 3.20 : Dual active bridge converter topology.

With different modulation techniques, different output power ranges and different current values for the same operating point can be operated under different switching losses. By combining different modulation techniques, the DAB converter can offer optimum performance with high efficiency and an operating range [49].

3.3.4. CLLC resonant converter

The CLLC resonant converter is a topology constructed with capacitors added to the input and output side of the transformer in the DAB converter. The CLLC resonant converter topology shown in Figure 3.21 is suitable for use in applications where

bidirectional energy flow is required, such as a DAB converter. The leakage inductance required for the CLLC resonant tank is significantly smaller than that required for the LLC resonant converter due to its symmetrical circuit. Furthermore, as compared to the LLC resonant converter, the CLLC resonant converter divides two resonant capacitors on both sides of the transformer, which helps decrease resonant capacitor voltage stress. The leakage inductance required for the CLLC resonant tank is less than that required for the DAB converter [35].

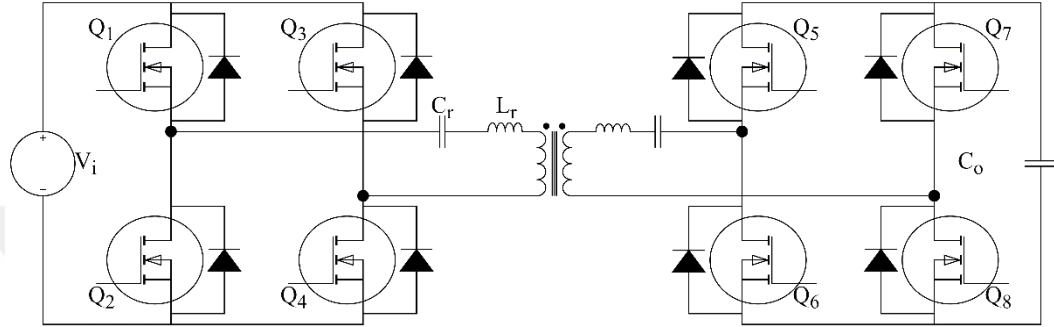


Figure 3.21 : CLLC resonant converter topology.

A summary of different DC/DC converter structures is given in Table 3.2. It can be seen that topologies with bidirectional energy flow require more controlled switching devices. Also, the control algorithm of the DC/DC converter becomes more complex with an increasing number of controlled switching devices. In addition, if ZVS or ZCS is applied to increase the efficiency, the number of passive elements can increase the cost.

Table 3.2 : Summary of DC/DC converter topologies.

Topology	Controlled Switching Devices	Diodes	Bidirectional	Efficiency	Cost
Phase-shifted full bridge converter	4	4	No	Lowest	Lowest
LLC resonant converter	4	4	No	Low	Low
Dual active bridge converter	8	0	Yes	High	High
CLLC resonant converter	8	0	Yes	Highest	Highest



4.CHARGER SYSTEM MODELLING AND SIMULATION

Before the design process can begin, the topologies and structures in the system must be selected. System parameters and design criteria should be determined according to the result of this selection. For this purpose, mathematical models were first determined and waveforms were characterized with ideal simulations. For this purpose, starting with the DC/DC converter at the output of the system and the rectifier are analyzed, respectively. In this way, the operation of each structure with the following structure can be seen. Table 4.1 shows the design parameters of the system.

Table 4.1 : System design parameters.

Parameter	Value
Input Voltage (V)	380-480
Maximum Input THDi	< %5
Power Factor	> 0.99
Output Voltage Range (V)	200-750
Maximum Output Power (kW)	22
Target System Efficiency	> %97

EV fast chargers generally achieve high power by connecting low-power modules in parallel. Another advantage of this structure is that it allows the design of stations with the desired power. The values in the Table 4.1 belong to one module. It is aimed at designing a station with a power of 150 kW by connecting 7 of these modules in parallel.

4.1.DC/DC Converter Modelling and Simulation

On the DC/DC converter side, the PSFB topology was chosen due to its low cost and ease of control. Since the efficiency of this topology is low, methods to increase the efficiency by reducing losses will be investigated in the design phase. Since the system output power of 22 kW with a single FB would increase the transformer size, the system will be realized by connecting the inputs and outputs of two 11 kW FBs in

parallel. For this purpose, the analysis in this section will be done for a system with a power of 11 kW.

4.1.1. Mathematical modelling

The four switches in the FB topology have a total of 16 different switching states. However, switches on the same branch will short-circuit the DC link, thus creating a forbidden switching state. Also, since the circuit cannot be completed with a single switching device, there are actually only four switching states. Figure 4.1 shows the names of the switching devices and diodes.

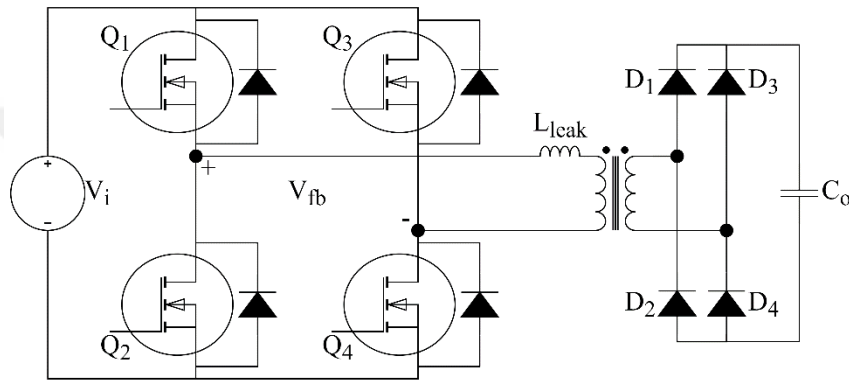


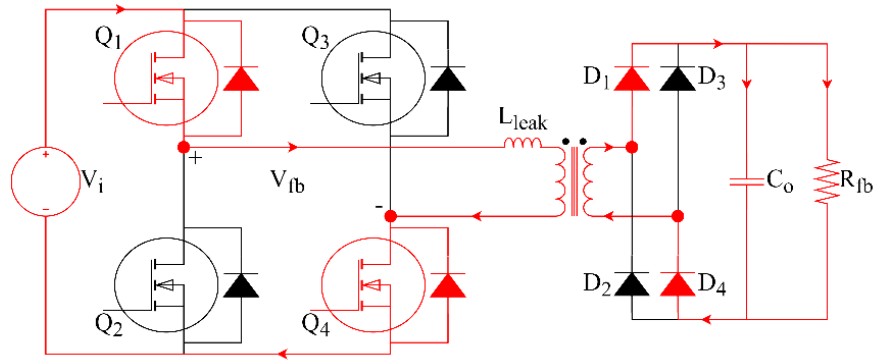
Figure 4.1 : Names of switching devices and diodes in phase-shifted full bridge converter topology.

According to the naming in the given topology, the conduction states of the controlled switching element and diodes and the voltage applied to the FB output (V_{fb}) in these states are as given in Table 4.2.

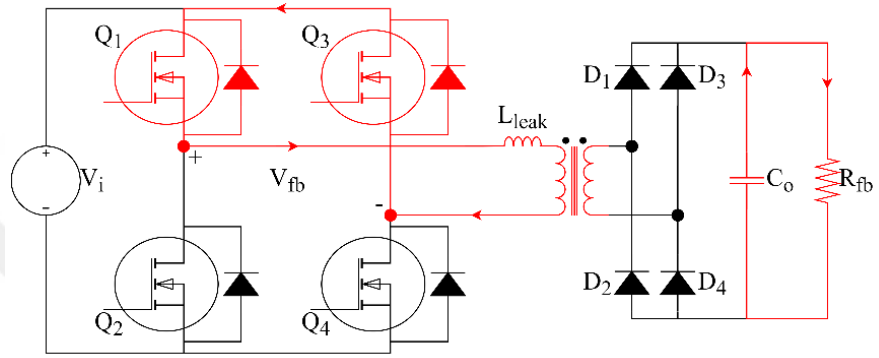
Table 4.2 : Switching sequences of phase-shifted full bridge converter topology.

Number of State	Q_1	Q_2	Q_3	Q_4	D_1	D_2	D_3	D_4	V_{fb}
1	1	0	0	1	1	0	0	1	V_i
2	1	0	1	0	0	0	0	0	0
3	0	1	1	0	0	1	1	0	$-V_i$
4	0	1	0	1	0	0	0	0	0

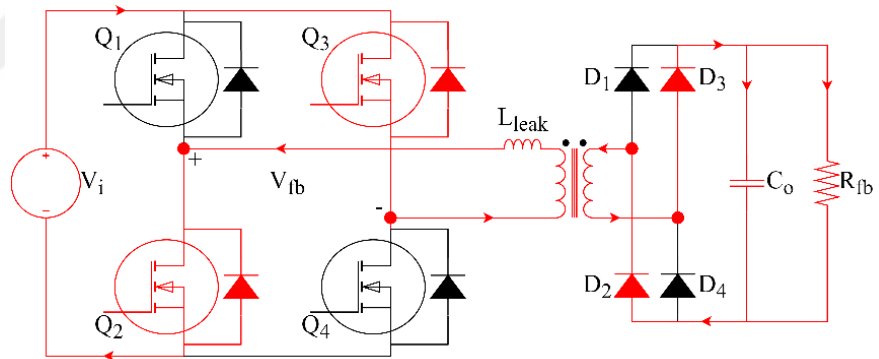
Current paths and conducting switches of the switching states given in Figure 4.1 and Table 4.2 are shown in red in Figure 4.2. Figure 4.2 (a) is the current paths for state 1, Figure 4.2 (b) for state 2, Figure 4.2 (c) for state 3 and Figure 4.2 (d) for state 4 in Table 4.2. In the next section, ideal modelling and simulations of the PSFB converter will be performed.



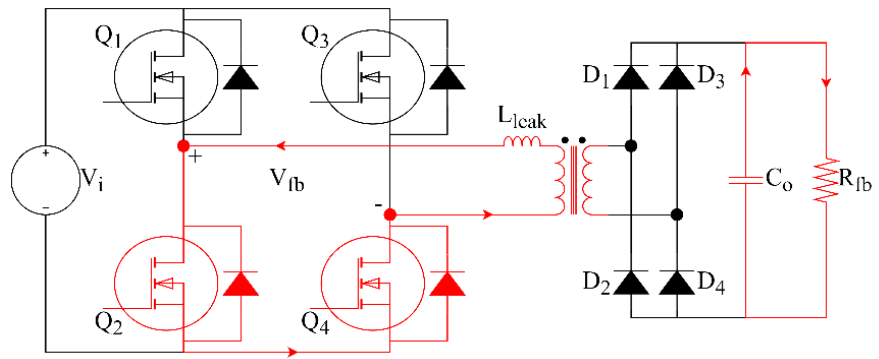
(a)



(b)



(c)



(d)

Figure 4.2 : Current paths and conducting switches for (a) state 1, (b) state 2, (c) state 3 and (d) state 4.

4.1.2.Simulation

Power output of 11 kW PSFB is modeled and simulated on the PLECS platform. The system behavior will be observed as a result of simulations with ideal switching devices. The leakage inductance of the transformer and the equivalent serial resistance (ESR) of the capacitor are added to the model since they are effective on the system behavior. Figure 4.3 shows the PSFB model.

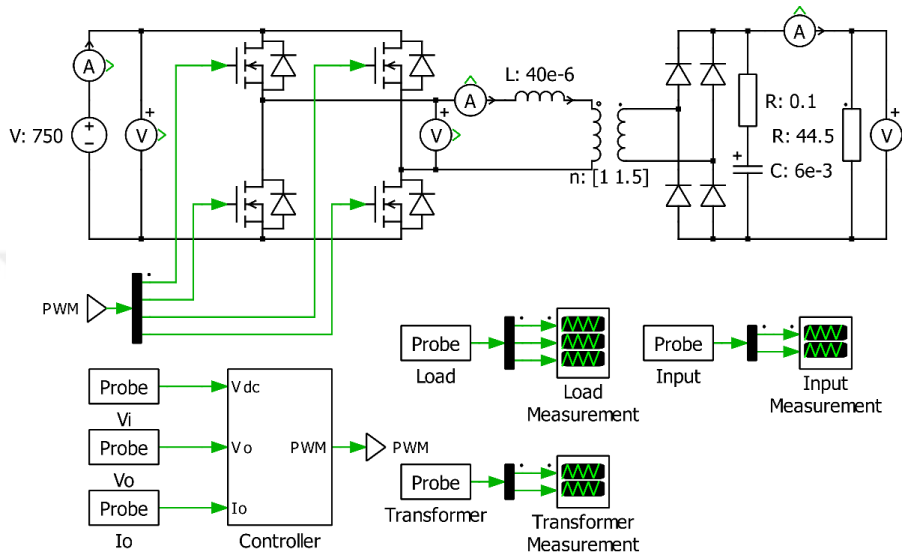


Figure 4.3 : Phase-shifted full bridge converter model in PLECS.

The controller block diagram of the PSFB converter is given in Figure 4.4 (a) and (b). Figure 4.4 (a) is the general controller schema. The calculated phase-shift angle is then converter the PWMs with the phase-shift PWM block given in Figure 4.4 (b).

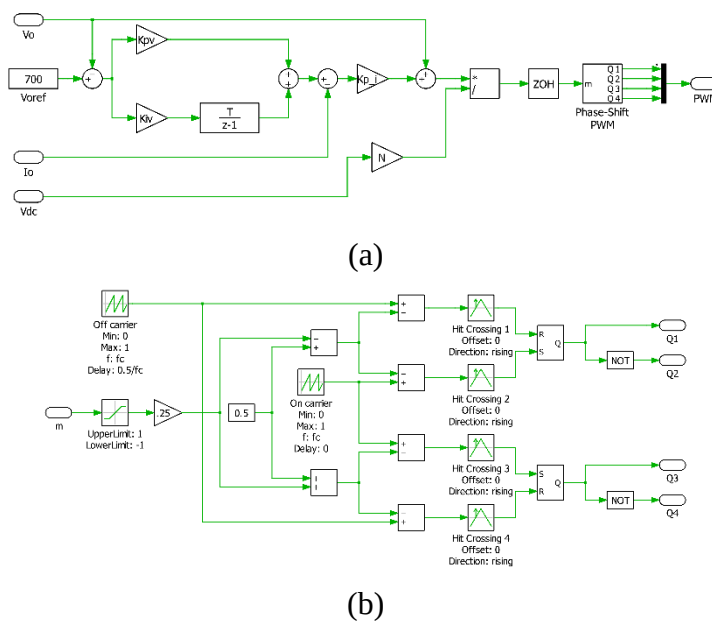


Figure 4.4 : General controller schema (a) and phase-shift PWM block (b).

The simulation of the model given in Figure 4.3 was run. 700 V was entered as the controller reference and a resistive load was used as the load. The input current under this condition are as given in Figure 4.5 (a) and the output voltage, current, and power are as given in Figure 4.5 (b). A constant voltage source with a voltage of 750 V was used as the input voltage. The input current under this condition is in the form of a triangle with a peak value of 50.3 A and an average value of 14.8 A. The output voltage has an average value of 709 V. The output current has an average value of 15.9 A.

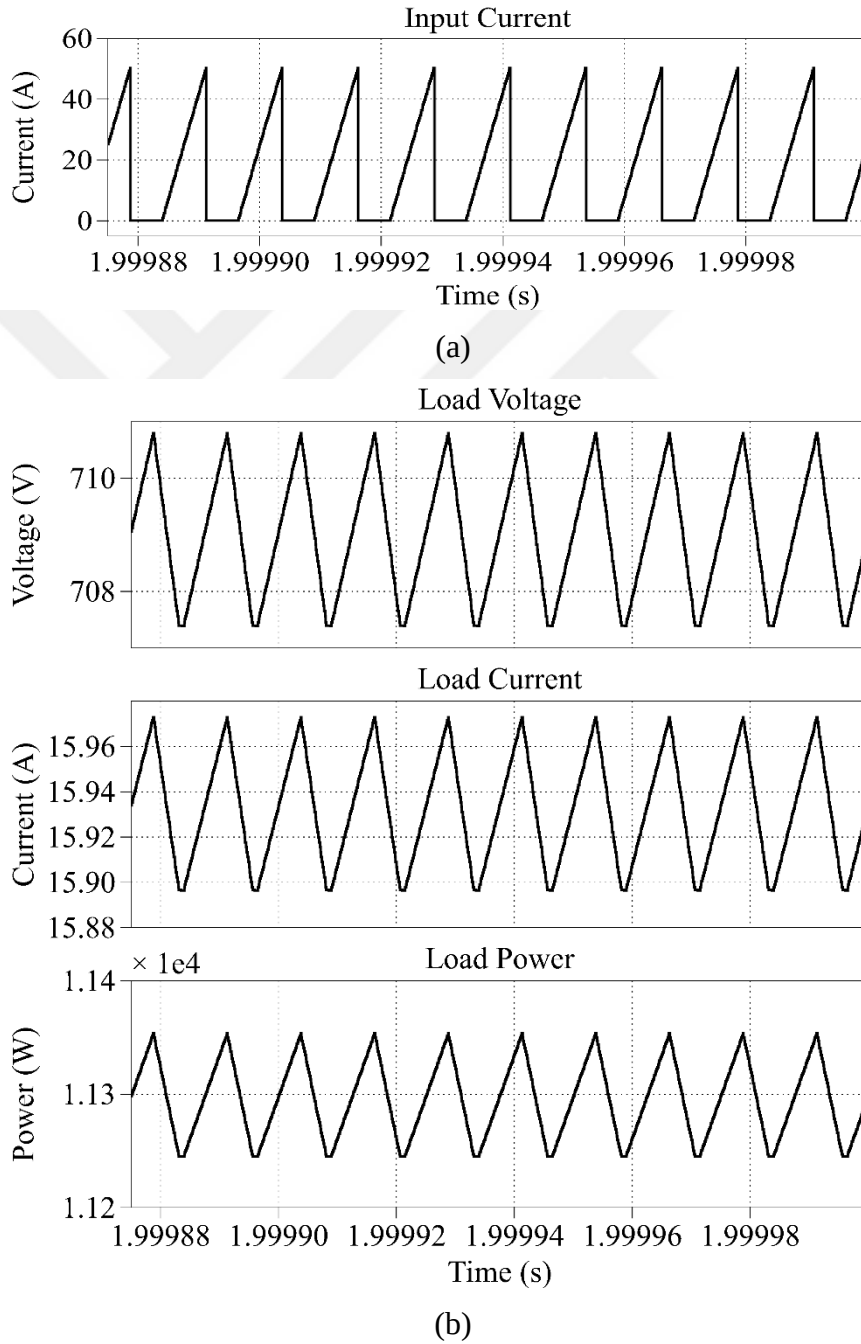


Figure 4.5 : Waveforms of (a) input and (b) output of ideal phase-shifted full bridge simulation.

For the design of the transformer at the output of FB, the waveform of voltage and current is as given in Figure 4.6. The voltage applied to the terminals of the transformer has an RMS value of 576.1 V.

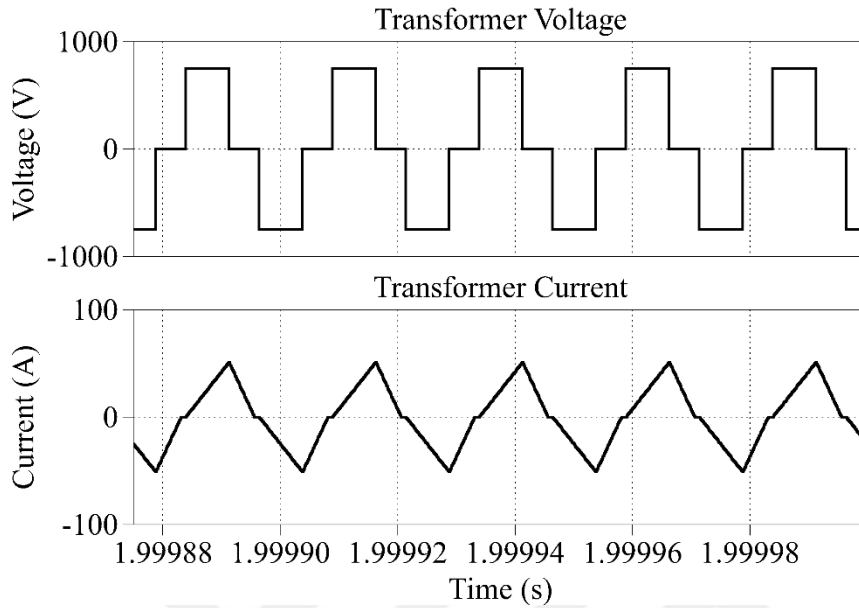


Figure 4.6 : Voltage and current waveforms of the transformer.

4.2.Rectifier Modelling and Simulation

The NPC rectifier topology was chosen because of its low THDi and high efficiency compared to most other topologies. Another advantage is the high DC link voltage at its output.

4.2.1.Mathematical modelling

With a total of four controlled switching elements per phase, the topology has a total of 16 switching states per phase. However, only 3 of these switching states are usable. The other states may cause a DC-link short circuit or damage the switching device. Figure 4.7 shows the names of the switching devices.

Different switching sequences can be observed for positive and negative sequences of the grid voltage. Switch Q_2 is fully conducting at positive grid voltage, while switches Q_1 and Q_3 are switching in reverse. When Q_1 and Q_2 are conducted at the same time, $V_{dc}/2$ is applied to the NPC output. When Q_2 and Q_3 switches are in conduction, 0 voltage is applied to the output. The case with negative grid voltage is similar. Q_3 switch is always in conduction. When Q_4 switch is in conduction, $-V_{dc}/2$ voltage is applied to the NPC output, and when Q_2 switch is in conduction, 0 voltage is applied

to the output. Table 4.3 shows the switching states and Figure 4.8 shows the reference voltage and gate signals.

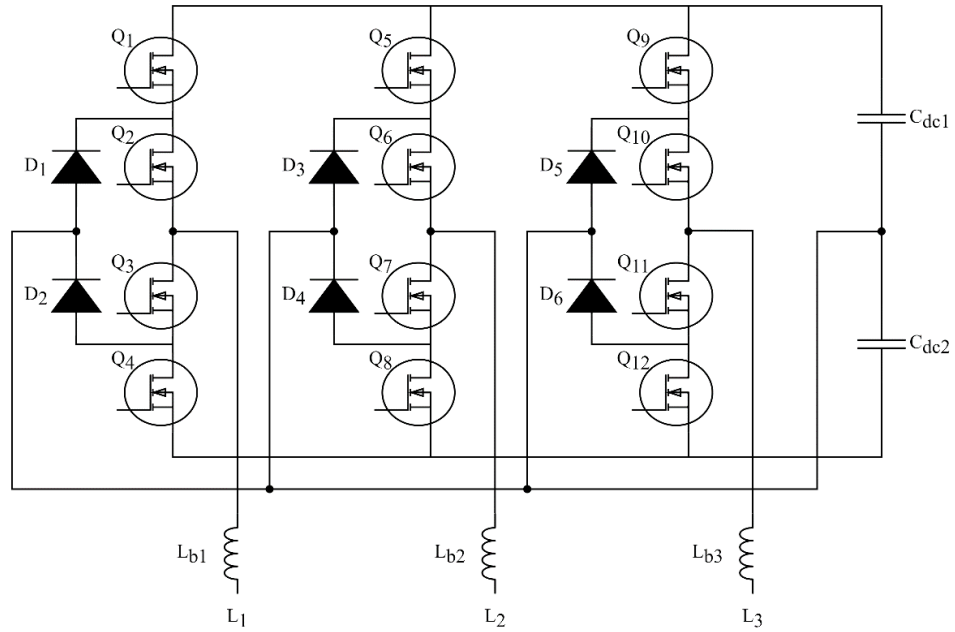


Figure 4.7 : Names of switching devices and diodes in neutral point-clamped rectifier topology.

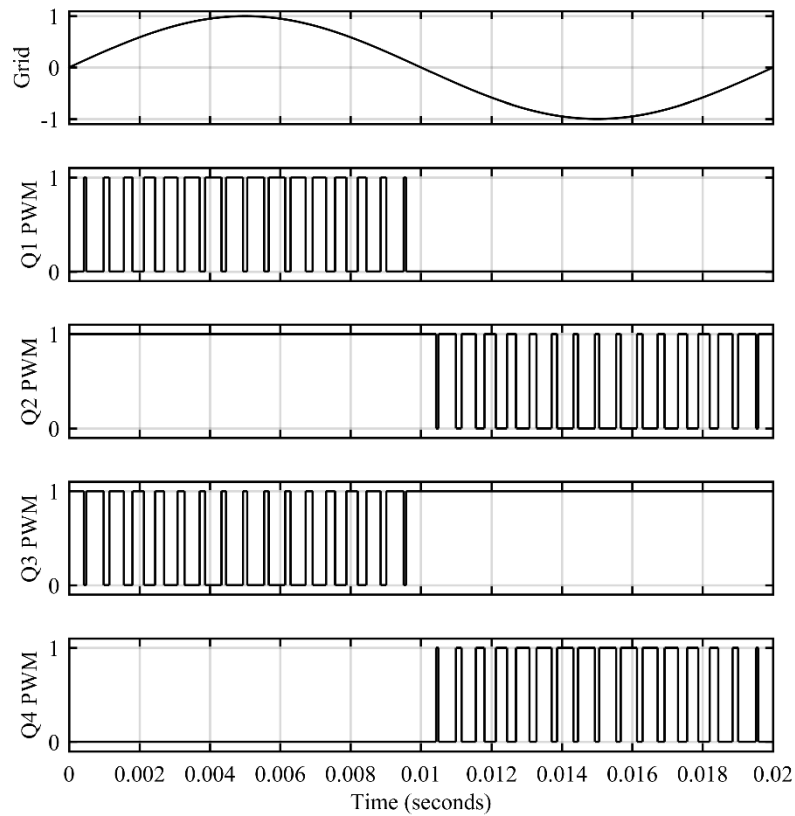


Figure 4.8 : Switching waveforms of NPC rectifier.

Table 4.3 : Switching sequences of neutral point-clamped rectifier topology.

Voltage State	Q1	Q2	Q3	Q4	V_{NPC}
P	1 (s)	1	0 (s)	0	$V_{dc}/2$
0+	0 (s)	1	1 (s)	0	0
0-	0	1 (s)	1	0 (s)	0
N	0	0 (s)	1	1 (s)	$-V_{dc}/2$

4.2.2.Simulation of the NPC Rectifier

The ideal modeling and simulation of the NPC topology to be used for the rectifier was performed on the PLECS platform. Figure 4.9 shows the simulation model. For the DC-link voltage, 750 V was entered as the reference value. A pure resistance load was used as the load.

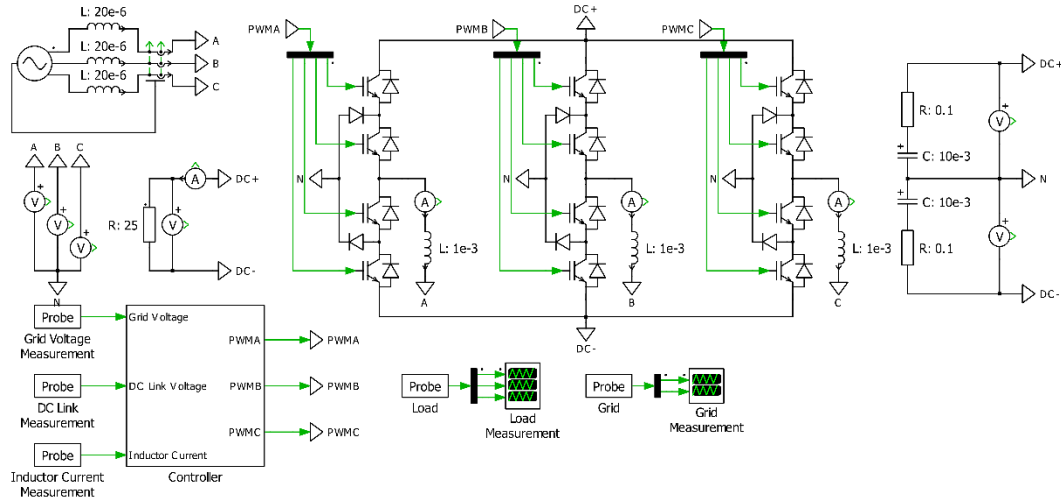


Figure 4.9 : Neutral point-clamped rectifier model in PLECS.

The inside of the controller block is given in Figure 4.10. After the reference signals are calculated, the necessary PWMs are generated according the reference signals.

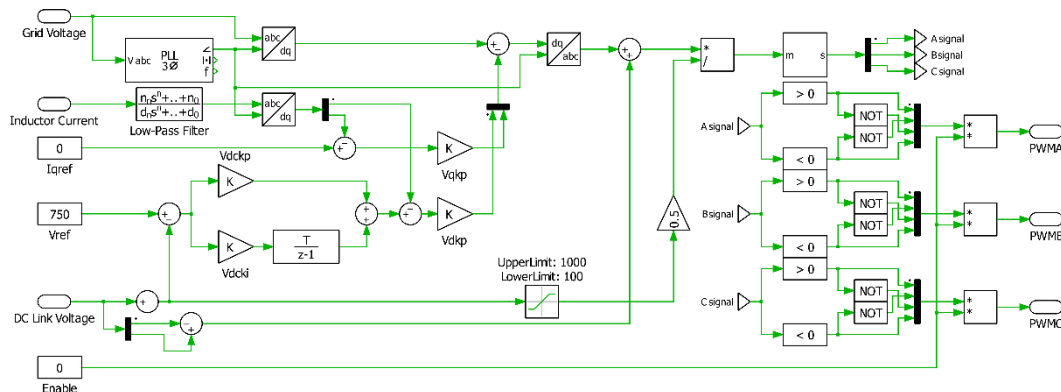


Figure 4.10 : NPC controller block.

The simulation of the model given in Figure 4.9 is run. The grid voltage and current under this condition are as given in Figure 4.11 (a) and the load voltage, current and power are as given in Figure 4.11 (b).

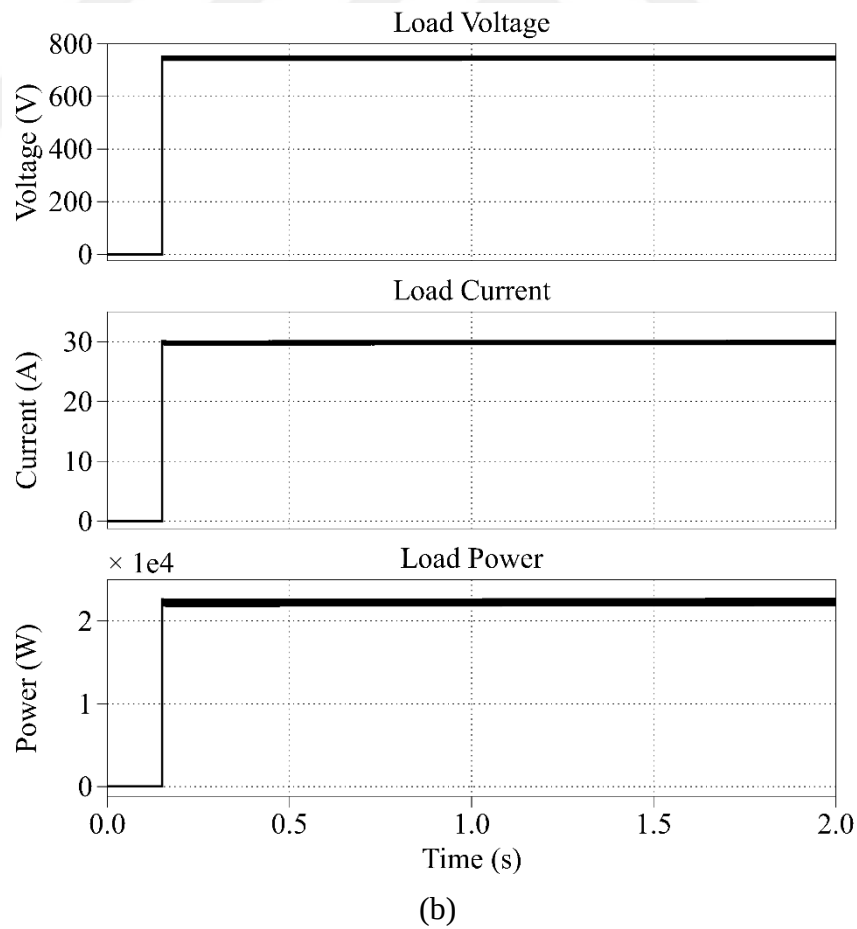
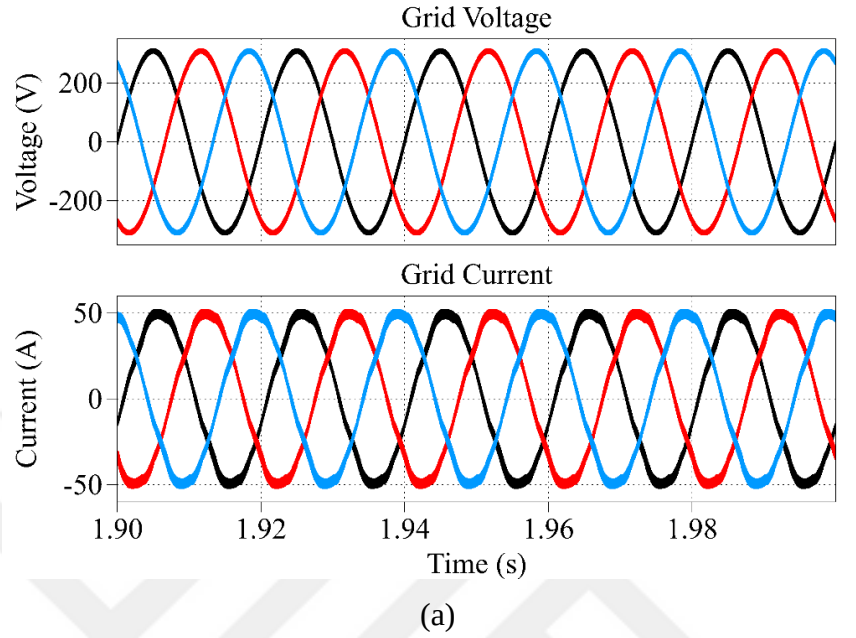


Figure 4.11 : Waveforms of (a) grid line to neutral voltage and currents, and (b) load voltage, current and power of ideal neutral point-clamped rectifier simulation.

The input current under this condition is 35.4 A and has a THDi of 4.09%. As shown in Figure 4.11 (a), there is a phase difference between voltage and current. This difference is due to the inductance used for grid connection, which slows down the response of the controller. The output voltage is 745 V. The load current under this condition is 29.8 A and the output power is 22.2 kW.

4.3. Overall System Simulation

After the structures other than the grid connection filter were modeled separately, these models were combined to create the ideal model of the whole system. The reason for not modeling the topology to be used in the grid connection filter is that the topology will be decided during the design phase of the NPC rectifier. For this reason, a high-value inductance was used in this modeling phase. The model is shown in Figure 4.12. The grid in the model is the same as the one used in the rectifier modeling. The rectifier model was added to the system in the same way. In PSFB modeling, one of the modules to be used in parallel was modeled. At this stage, the inputs and outputs of two PSFB models were connected in parallel. During the parallel connection of the PSFB modules, which act as a current source due to the diodes on their outputs, one inductance was placed at the outputs before the capacitor group. If necessary, the use of these inductances will be reviewed during the design phase. The battery model used at this stage is modeled with a pure resistive load. In the controller block, there are three sub control block. One of them is used for controlling of NPC rectifier and can be seen in Figure 4.10. The other two is used for parallel connected PSFB converters and can be seen in Figure 4.4.

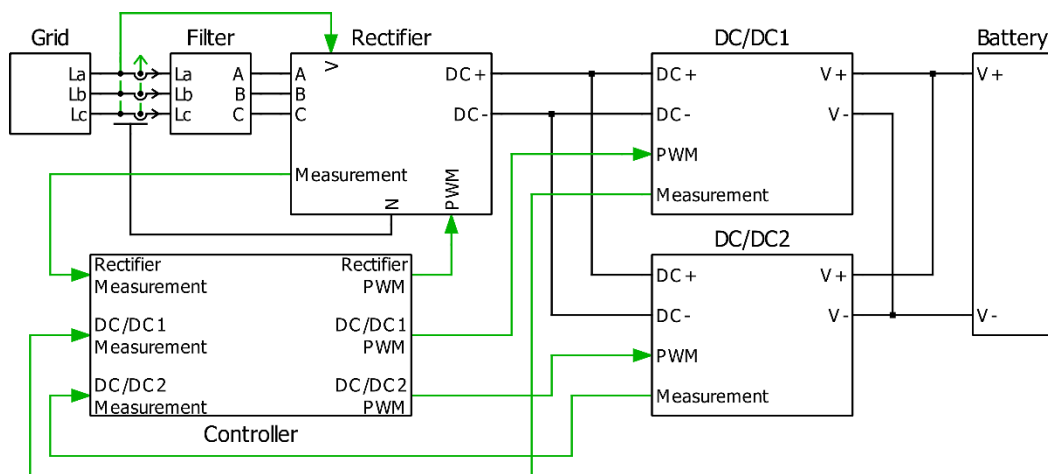


Figure 4.12 : System model in PLECS.

The simulation of the model given in Figure 4.12 is run. The steady states of the grid voltage and current under this condition are as shown in Figure 4.13. The steady state input current is 35.6 A and has a THDi of 4.05%. The system output voltage and current are as given in Figure 4.14. The DC/DC converter is activated at 0.2 s of the simulation. The load voltage in this condition has an average value of 742.8 V. The load current is 29.7 A.

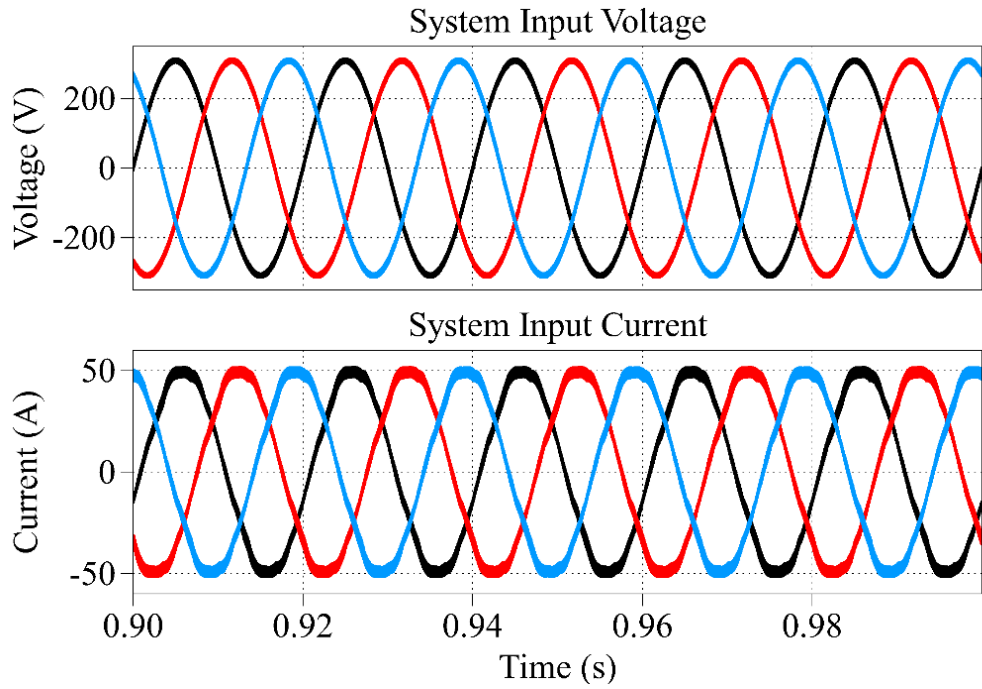


Figure 4.13 : System simulation grid voltage and current waveforms

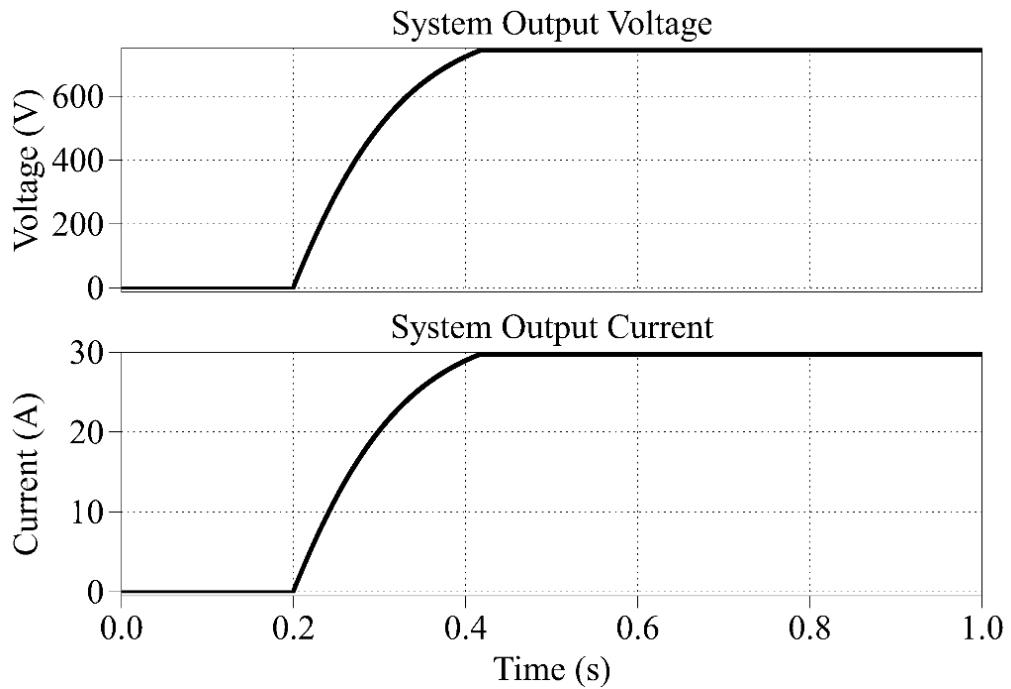


Figure 4.14 : System simulation load voltage and current waveforms.

As a result of the system simulation, the output power is 22.1 kW. The power drawn from the grid is calculated to be 23.4 kVA. The active power drawn from the grid is not calculated exactly. This is due to the phase difference caused by the grid connection inductance. The system design will be started in the next section. In the following section, components will be selected and designed with the help of modeling and simulations.



5.DESIGN, COMPONENT MODELLING AND SIMULATION

In this section, starting with the DC/DC converter, the design and material selection of the rectifier and grid connection filter will be made, respectively. Then, the system design will be made by combining the designs. The system design will start with the system modeling and simulation phase, and then designs for printed circuit boards (PCBs) will be made. The last step will be the design of the cooling system, and the chapter will be completed. The system structure under design is given in Figure 5.1.

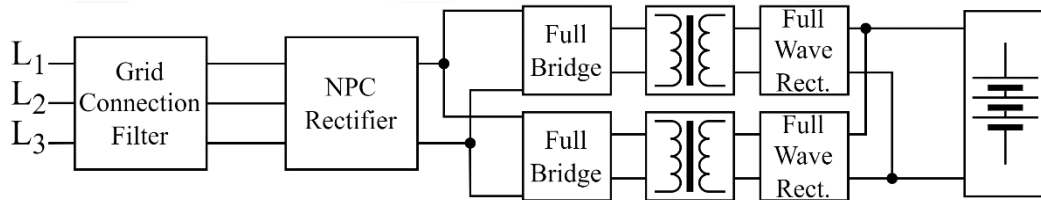


Figure 5.1 : System structure under design.

5.1.DC/DC Converter

In the previous section, it was said that PSFB was chosen as the topology. In this section, the design of the power circuit will be done first. By analyzing the waveforms, the power module to be used will be selected, and then the design of the transformer will be completed. After the power circuit is designed, the gate driver and controller will be designed. After these steps, the DC/DC converter will be modeled and the simulation results will be compared with the design criteria.

5.1.1.Power circuit design

One PSFB converter cell to be designed will have an output power of 11 kW and will be able to operate in the output voltage range between 200 V and 750 V. To increase the power output to 22 kW, the outputs of two of these designed cells will be connected in parallel. For this purpose, in the parallel connection of the outputs of two PSFB converters, inductance must be connected to the output stage of each PSFB converter. Inductance was added to the modeling to be connected to the output of the PSFB converter. Due to the added inductance, a capacitor is added to the output of the FB

before the transformer in order to reset the transformer flux and perform ZVS. Also, an inductance will be added before the transformer to ensure the ZVS condition. In this way, the PSFB zero-voltage-transition (ZVT) structure will be built. Waveforms for this topology will be analyzed to characterize the topology. Figure 5.2 shows the PSFB ZVT topology. In this topology, the capacitor used for ZVT is denoted by C_r and the inductance is denoted by L_r . The filter inductance at the output side is L_{FB} and the output voltage is V_o . FB output voltage is V_{fb} . Transformer primary current is I_{pr} and secondary current is I_s .

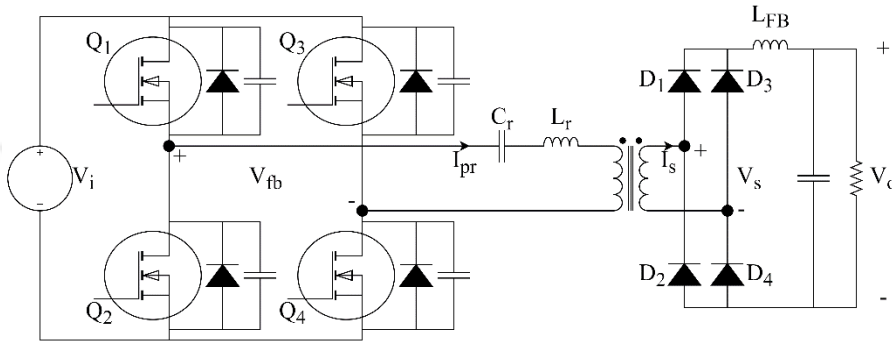


Figure 5.2 : Phase-shifted full bridge zero-voltage-transition converter.

The workings of the topology can be divided into six intervals for an operating period. Figure 5.3 shows the FB output voltage, primary current, and transformer secondary voltage during one period. The V_i' here is the voltage obtained by multiplying the voltage V_i by the conversion ratio. C_r will be neglected when analyzing waveforms.

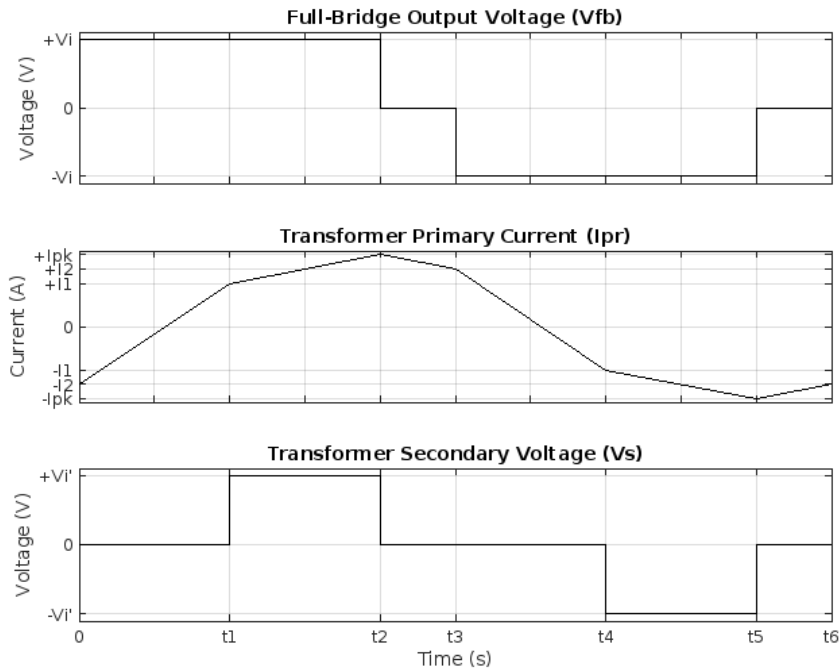


Figure 5.3 : Phase-shifted full bridge zero-voltage-transition converter waveforms.

The first operating interval is $0-t_1$. In this interval, Q_1 and Q_4 switches are conducting, and V_{fb} is equal to V_i . Since the output inductance current starts to decrease and the voltage across the inductance is negative in this case, all diodes in the output rectifier are in conduction. As a result, the transformer's secondary voltage is equal to zero. In this interval, equation 5.1 shows the change of I_{pr} . I_{pr} is equal to $-I_2$ at the start of interval and, reaches I_1 . The current paths are as given in Figure 5.4.

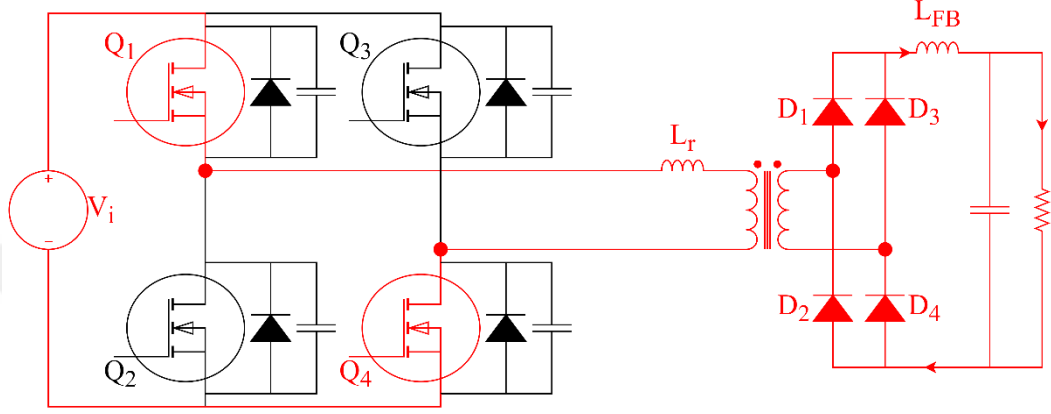


Figure 5.4 : $0-t_1$ interval operation.

$$\frac{dI_{pr}}{dt} = \frac{V_i}{L_r} \quad (5.1)$$

After the freewheeling stage on the secondary side is over, we start to see the V_i' voltage on the secondary side. Equation 5.2 shows the change in I_{pr} . The voltage V_o' is the primary-reduced output voltage, and L_{FB}' is the primary-reduced output inductance. At the end of this interval, I_{pr} reaches I_{pk} and Q_1 is turned off and Q_2 is turned on. The current paths in the interval t_2-t_3 are as given in Figure 5.5.

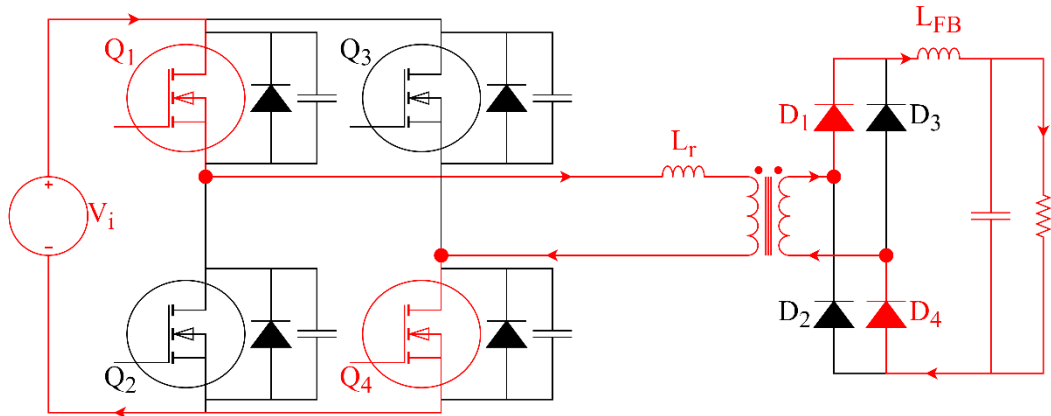


Figure 5.5 : t_1-t_2 interval operation.

$$\frac{dI_{pr}}{dt} = \frac{V_i - V_o'}{L_r + L_{FB}'} \quad (5.2)$$

In the interval t_2 - t_3 , when switches Q_2 and Q_4 are in conduction, V_{fb} is equal to zero. The change in I_{pr} is given in equation 5.3. I_{pr} , which has I_{pk} value at t_2 , decreases to I_2 at t_3 . At time t_3 , switch Q_4 is turned off and switch Q_3 is turned on. The current paths are given in Figure 5.6.

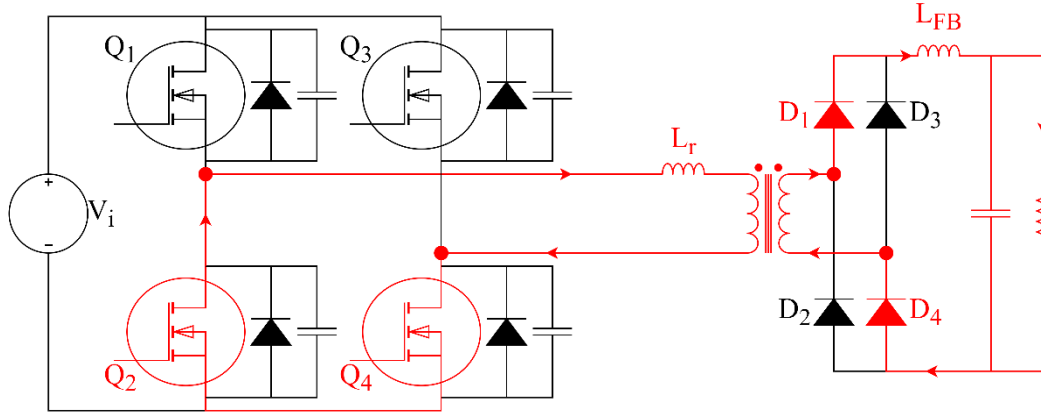


Figure 5.6 : t_2 - t_3 interval operation.

$$\frac{dI_{pr}}{dt} = \frac{-V_o'}{L_{FB}'} \quad (5.3)$$

In the intervals up to this point, a positive input voltage was applied to the primary of the transformer. The following switching intervals can be considered the inverse of the previously mentioned switching intervals. At time t_3 , V_{fb} is equal to $-V_i$ with the help of switches Q_3 , which has been turned on, and Q_2 , which is still conducting. As in the interval 0 - t_1 , all diodes on the rectifier side are conducting and freewheeling. The change of I_{pr} in the time interval t_3 - t_4 is as given in equation 5.4. The current paths are as shown in Figure 5.7 with red lines. Since the current changes direction within this interval, the direction of the current is not represented by arrows. After the end of the freewheeling phase at time t_4 , I_{pr} will reach $-I_1$. Diodes D_1 and D_4 in the rectifier will be reverse polarized and turned off, and the conduction will be provided by diodes D_2 and D_3 .

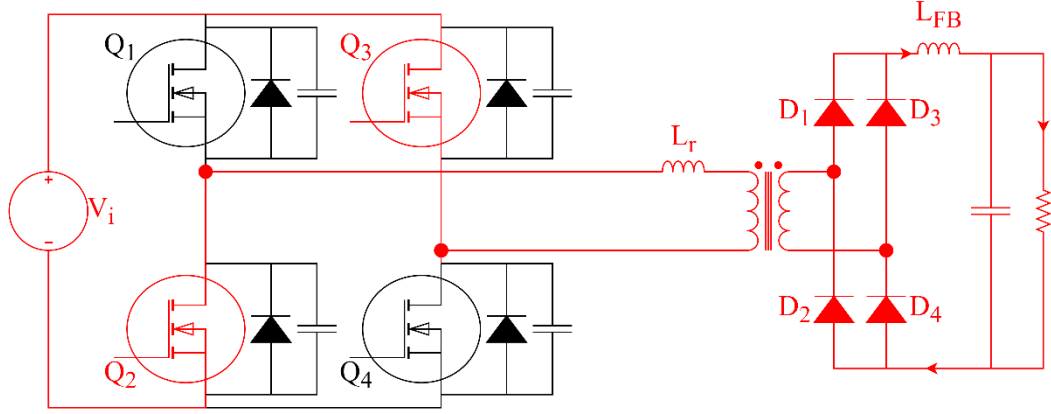


Figure 5.7 : t_3 - t_4 interval operation.

$$\frac{dI_{pr}}{dt} = -\frac{V_i}{L_r} \quad (5.4)$$

The current paths for the t_4 - t_5 interval after freewheeling ends are as given in Figure 5.8. At t_5 I_{pr} reaches $-I_{pk}$. The change in I_{pr} is as given in equation 5.5. At t_5 , Q_2 will be turned off and Q_1 will be turned on.

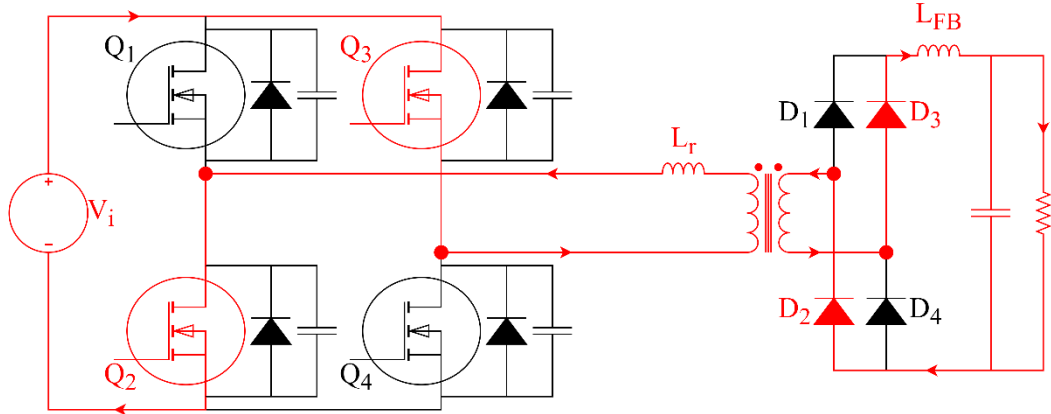


Figure 5.8 : t_4 - t_5 interval operation.

$$\frac{dI_{pr}}{dt} = -\frac{V_i - V_o'}{L_r + L_{FB}} \quad (5.5)$$

Q_1 and Q_3 were in conduction during the last switching interval. V_{fb} is equal to zero. I_{pr} has increased from $-I_{pk}$ to $-I_2$. Equation 5.6 shows the change in I_{pr} . The time t_6 and the time 0 are the same instant. After this phase, the same switching intervals will repeat. The current paths in the t_5 - t_6 switching interval are as shown in Figure 5.9.

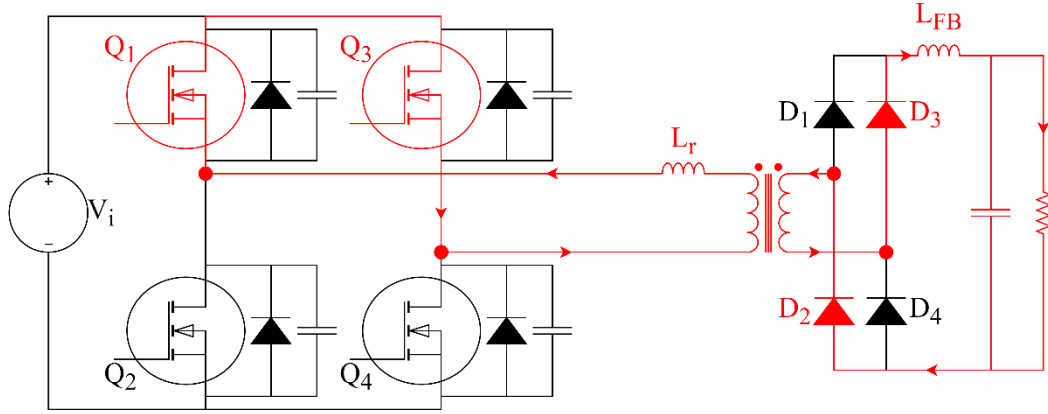


Figure 5.9 : t_5 - t_6 interval operation.

$$\frac{dI_{pr}}{dt} = \frac{V_o'}{L_{FB}} \quad (5.6)$$

The model prepared with these changes has been updated and the simulation has been repeated. The newly created model is as given in Figure 5.10. The controller block in Figure 5.10 is the same controller block given in Figure 4.4.

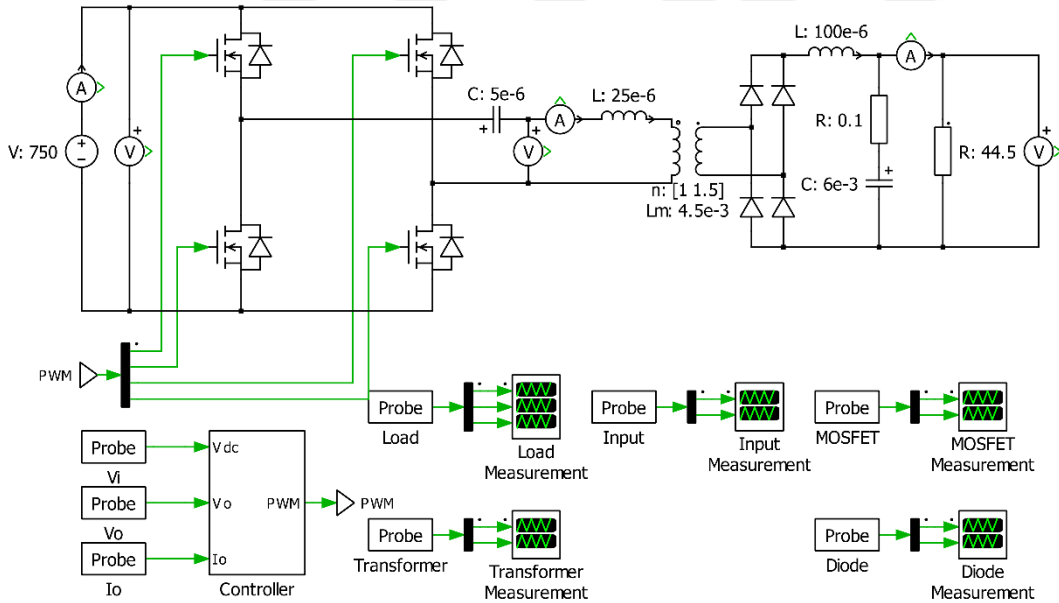


Figure 5.10 : Phase-shifted full bridge zero-voltage-transition converter model in PLECS.

When the model given in Figure 5.10 is run, the waveforms of the output voltage, current, and power are as given in Figure 5.11.

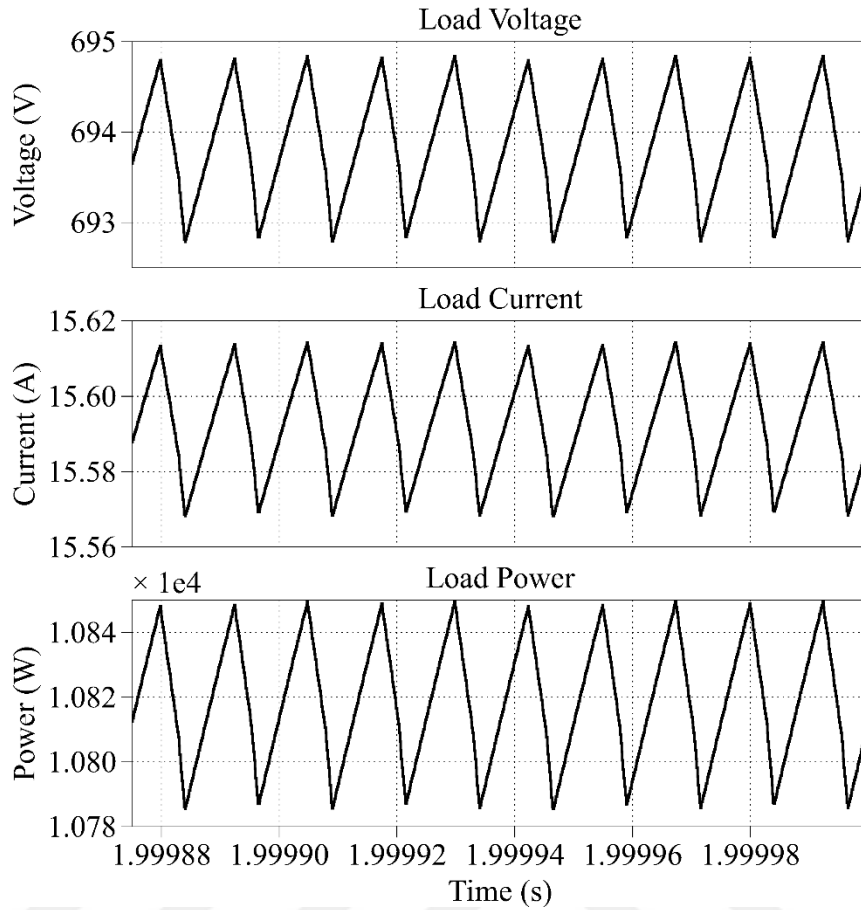


Figure 5.11 : Output voltage, current and power of ideal phase-shifted full bridge zero-voltage-transition simulation.

As seen in Figure 5.11, the inductance placed at the output side causes a voltage drop. With increasing frequency (f), the impedance of the inductance (Z_L) increases as given in equation 5.7, and the output voltage decreases due to the increasing impedance. Here, L represents the inductance value.

$$Z_L = 2\pi fL \quad (5.7)$$

As seen in equation 5.7, Z_L increases with increasing f . Choosing too high a switching frequency will increase the Z_L even though it will reduce the size of the magnetic materials. Increasing Z_L will increase the voltage drop across the inductor, making it difficult to regulate the output voltage.

5.1.1.1. Module selection

The switching frequency must first be determined before selecting the appropriate module. As seen in the studies examined in the literature review, different switching frequencies were selected for different topologies. In the study on the semi-DAB

converter, it is seen that 100 kHz of switching frequency is selected at 10 kW power. However, V_i and V_o values are lower in this study [7]. In the study where an LLC converter and buck converter are used together, it is seen that the LLC converter has 120 kHz switching frequency at 20 kW power. However, the buck converter has a switching frequency of 50 kHz [9]. In addition, in many studies, SiC or GaN switching devices are preferred to keep the switching frequency high or to design systems with better thermal performance and efficiency at lower switching frequency values.

The modules F4-50R12KS4 and F4-23MR12W1M1_B76 have similar maximum ratings. The difference between them is that, the F4-50R12KS4 has four Si IGBTs and the F4-23MR12W1M1_B76 has four SiC MOSFETs inside the module. According to datasheet of F4-50R12KS4, each Si IGBT of that module has 6 mJ of turn-on energy and 2.5 mJ of turn-off energy for the standardized test condition and has a 3.2 V saturation collector-emitter voltage, when 50 A current flows through it at 25°C [50]. Each SiC MOSFET of the module F4-23MR12W1M1_B76 has 0.43 mJ of turn-on energy and 0.11 mJ of turn-off energy for the same conditions and has a 22.5 m Ω drain-source on resistance, when 50 A current flows through it at 25°C [51]. According to these parameters, for the same switching frequency, the module F4-50R12KS4 has a loss, which is more than 15 times the switching losses of the module F4-23MR12W1M1_B76. Also, switching frequency of Si IGBTs cannot be high as SiC MOSFETs. Mostly, the switching frequency is chosen below 20 kHz, when Si IGBTs are used. A system with SiC MOSFETs can be reach over 50 kHz of switching frequency. The conduction loss of F4-50R12KS4 is equal to 160 W per IGBT for given test conditions and the conduction loss of F4-23MR12W1M1_B76 is equal to 56.25 W per MOSFET. That means each Si IGBT of module F4-50R12KS4 has conduction loss of nearly 3 times of the each SiC MOSFET of the module F4-23MR12W1M1_B76. If we use Si IGBT at 20 kHz of switching frequency, we can see that each IGBT has 170 W of switching losses and 160 W of conduction losses. For the each SiC MOSFET of the module F4-23MR12W1M1_B76 has 27 W of switching losses at 50 kHz of switching frequency and 56.25 W of conduction losses. To sum up, Si IGBTs have total losses of nearly 4 times of SiC MOSFETs even the switching frequency of SiC MOSFET was selected as 2.5 times of Si IGBTs.

The module F4-50R12KS4 has 180 g of weight and 76.92 mL of volume [50]. The module F4-23MR12W1M1_B76 has 24 g of weight and 21.5 mL of volume [51]. Both

of modules can be reach up to 11 kW of power. According to the parameters, the module with Si IGBTs has a 143.01 kW/mL and 61.11 W/g of power density. But, the module with SiC MOSFETs has a 511.7 kW/mL and 458.33 W/g of power density. Just for comparing the power densities of the modules, we can see that module with SiC MOSFETs make the system 72.05% smaller and 86.67% lighter. Additionally, the heat sink sizes will be much smaller if the module with SiC MOSFETs are used even with higher switching frequency and also, the sizes of the magnetic materials will be smaller, too.

The switching frequency of the DC/DC converter in the system to be designed in this thesis is selected as 40 kHz. In this way, magnetic material sizes can be optimized and switching losses can be kept at desired levels. In addition, WBG semiconductors will be used for their high efficiency and power density.

In order to select the FB module, the current in the FB circuit must first be calculated. Since the maximum power of each FB (P_{o-max}) module is 11 kW and the minimum output voltage (V_{o-min}) is 200 V, the maximum current at maximum power (I_{o-max}) is calculated as 55 A according to equation 5.8.

$$I_{o-max} = \frac{P_{o-max}}{V_{o-min}} \quad (5.8)$$

In the case where the capacitor current is neglected, output current (I_o) is equal to the output inductance current (I_{Lo}). The relationship between the number of primary turns N_1 , the number of secondary turns N_2 , and the turns ratio “n” is as given in equation 5.9. The relationship between I_{pr} and I_s is given in equation 5.10. Accordingly, the relationship between the minimum value (I_{Lo-min}) and maximum value (I_{Lo-max}) of the output inductance current and I_{pr} is given in equations 5.11 and 5.12.

$$n = \frac{N_2}{N_1} \quad (5.9)$$

$$I_s = \frac{I_{pr}}{n} \quad (5.10)$$

$$I_{Lo-min} = \frac{I_{pr-1}}{n} \quad (5.11)$$

$$I_{Lo-max} = \frac{I_{pr-pk}}{n} \quad (5.12)$$

Based on similar studies, 600 V DC link voltage was preferred in a study using a three-port DC/DC converter [10]. In another study using a semi-DAB converter, a variable DC-link voltage between 350 V and 550 V was preferred. However, the output voltage in this study is between 150 V and 450 V [7]. Accordingly, it is aimed to keep the current flowing through the FB low by choosing a DC link voltage is selected as 750 V in the system to be developed. The drain-source voltage that should be used at this level should be 1200 V. Furthermore, it is intended to keep stray inductance low by using power modules rather than disassembled semiconductors. According to this, manufacturer, manufacturer code, drain-source on resistance (R_{DS-on}), nominal drain current (I_{D-nom}), and repetitive peak drain current (I_{DRM}) values of SiC switching devices that can be used in the research are as given in Table 5.1.

Table 5.1 : Parameters of different SiC FB MOSFET modules [51–53].

Manufacturer	Manufacturer Product Code	R_{DS-on} (m Ω)	I_{D-nom} (A)	I_{DRM} (A)
Infineon	F4-45MR12W1M1_B76	45	25	50
Infineon	F4-23MR12W1M1_B76	22.5	50	100
Semikron	SK45MH120TSCp	45	40	90

As seen in Table 5.1, there are three different SiC FB MOSFET modules with 1200 V drain-source voltage currently in production. Among these three modules, Infineon's F4-45MR12W1M1_B76 has the lowest nominal drain current and repetitive peak drain current values. Semikron's SK45MH120TSCp has a nominal drain current value of 40 A. The disadvantage of this module is that the drain-source on resistance is 45 m Ω [53]. Therefore, the SiC MOSFET module with the code F4-23MR12W1M1_B76 from Infineon is the best choice. The appearance of the module is as shown in Figure 5.12 and the datasheet of module is given in Appendix A.



Figure 5.12 : F4-23MR12W1M1_B76 SiC FB MOSFET module [51].

After selecting the FB module, it is necessary to select the full-wave rectifier module in the DC/DC converter. Since I_o is calculated as 55 A, the rectifier module to be used must be selected accordingly. Accordingly, the SiC full-wave rectifier module must be able to withstand this current. Furthermore, the voltage withstand must be at least 1200 V, as in the SiC FB module. The only SiC full-wave rectifier module that meets these requirements and is still in production is Infineon's DDB2U60N12W1RF_B11. The appearance of the module is same as F4-23MR12W1M1_B76 SiC FB MOSFET module. The voltage drop of each diode in the module is 1.85 V at maximum junction temperature [54]. The datasheet of module is given in Appendix B.

5.1.1.2. Transformer design

Primary voltage (V_{pr}), secondary voltage (V_s), transformer power (P_{tr}), and switching frequency (f_{sw}) can be taken as transformer design parameters. When C_r is not taken into account, V_{pr} equals V_{fb} . First of all, a core selection should be made. In such applications, it is common to use ferrite cores. The main reasons for this are the low core losses up to 1 MHz frequency and the fact that many manufacturers are active in the market. Accordingly, core sizing can be done according to equation 5.13 [55]. The product of window area and core area ($WaAc$) is the reference value used in the tables shared by the manufacturers for core selection. In the calculation of $WaAc$, FB topology comes in at 140 as a coefficient [55]. Furthermore, $WaAc$ depends on the maximum flux density (B_{max}) in Tesla, f_{sw} in kHz, and current density (J) in A/mm².

$$WaAc = 140 \frac{P_{tr}}{B_{max} f_{sw} J} \quad (5.13)$$

To allow for instantaneous higher powers, the P_{tr} used in the design is set to 16.5 kW. According to equation 5.13, $WaAc$ is calculated as 96.25 cm⁴ when P_{tr} is 16.5 kW, B_{max} is 0.2 T, switching frequency is 40 kHz, and J is 3 A/mm². Accordingly, the appropriate core will be selected from the area product distribution chart of the Magnetics Company in Appendix D. The general tendency in such applications is to use toroid or E-core. However, toroid cores are less preferred because they have sharper saturation characteristics than E-cores. Depending on the material properties, ferrite cores are classified as N87 or N97. N87 ferrite cores are for general use. N97 cores are a material family with lower loss. According to the area product distribution chart, 96.25 cm⁴ $WaAc$ can be achieved with different configurations. The

configurations that can be used are given in Table 5.2. This table shows the inductance factor (A_L), relative effective permeability (μ_e), maximum core loss per set (P_v) of cores and maximum core loss (P_{c-max}) of these configurations.

Table 5.2 : Usable core configurations [56–61].

Core Code	Material Name	Number of Sets	A_L (nH)	μ_e	P_v (W/set)	P_{c-max} (W)
E80/38/20	N87	3	4500	1680	< 6.5	< 19.5
E80/38/20	N97	3	4700	1770	< 6.2	< 18.6
E70/33/32	N87	4	9700	1700	< 9.5	< 38
E70/33/32	N97	4	10000	1740	< 8.6	< 34.4
E65/33/27	N87	4	7900	1700	< 6.7	< 26.8
E65/33/27	N97	4	7900	1730	< 6.3	< 25.2

Among the configurations in Table 5.2, the one with E70/33/32 has the highest P_{c-max} . Although E80/38/20 has the lowest P_{c-max} , due to its low A_L , it needs to have a higher number of turns for the same inductance value. Therefore, E65/33/27 was chosen as the most optimized core. Since the loss difference between N87 and N97 materials is below 6.5%, the N87 type will be used in the design for cost optimization. The core dimensions are given in Figure 5.13; the effective core length (l_e), effective core cross section area (A_c), core volume (V_e), and saturation flux density (B_{sat}), A_L and μ_e required for the design are given in Table 5.3.

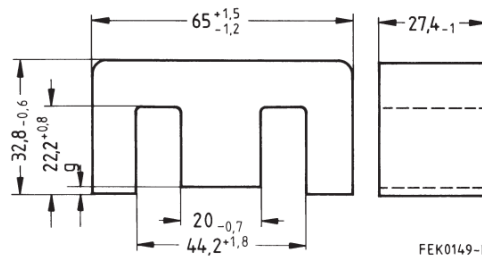


Figure 5.13 : E65/33/27 core dimensions in cm [60].

Table 5.3 : E65/33/27 core parameters [60].

Parameter	Value
l_e (cm)	14.7
A_c (cm ²)	5.35
V_e (cm ³)	78.65
B_{sat} (T)	0.32
A_L (nH)	7900
μ_e	1700

The calculation of N_1 will be done according to equation 5.14 [62]. The selected maximum flux density (B_m) in the formula is 0.18 T. Accordingly, N_1 is calculated as 12.

$$N_1 = \frac{V_{pr}}{4B_m f_{sw} A_c} \quad (5.14)$$

n is chosen as 1.5, and according to equation 5.9, N_2 is calculated as 18. I_{pr} is calculated as 14.67 A according to equation 5.15 and I_s is calculated as 9.78 A according to equation 5.10.

$$I_{pr} = \frac{P_{tr}}{V_i} \quad (5.15)$$

J was taken as 4 A/mm² during core selection. Since the effective cross-section may decrease due to the skin effect at high frequencies, Litz wire was preferred. The skin depth (δ) is depended on the resistivity of conductor, frequency of current and permeability of conductor. Copper conductor is used for magnetic design. The resistivity of copper (ρ_{Cu}) is equal to 1.72 $\mu\Omega$ cm and permeability of copper (μ_{Cu}) is equal to 1.2566 $\times 10^{-6}$ H/m. Accordingly equation 5.16, the skin depth is calculated as 0.33 mm at 40 kHz frequency.

$$\delta = \sqrt{\frac{\rho_{Cu}}{\pi f \mu_{Cu}}} \quad (5.16)$$

If usage of copper conductor with diameter less than 0.33 mm, the skin effect does not occur and the whole conductor can be used for current carrying. For this purpose, Litz wire with diameter of 0.2 mm is preferred for conductor. In core selection, the max current density of transformer is selected as 4 A/mm². In this situation the minimum cross section to be used in the primary was calculated as 3.67 mm² according to equation 5.17, and the minimum cross section to be used in the secondary was calculated as 2.45 mm². There is 96 parallel 0.2 mm Litz wire bundle can be found in industry and it is practically used. This one bundle has 3.015 mm² of cross section. According to this, two of these bundles can be paralleled for primary winding of transformer and 192 parallel of 0.2 mm Litz wires can be used in the primary winding. Usage of 192 parallel of 0.2 mm Litz wire has 6.03 mm² of cross-sectional area. For

secondary winding, one bundle can be used and that 96 parallel of 0.2 mm Litz wires has 3.015 mm² of cross-sectional area. According to equation 5.16, the primary and secondary current densities are calculated 2.43 A/mm² and 3.24 A/mm², respectively.

$$J = \frac{I}{q} \quad (5.17)$$

The magnetization inductance (L_{mag}) of the designed transformer is calculated as 4.55 mH according to equation 5.18. Since there is no air gap, the leakage inductance will be low. The leakage inductance ratio is taken as 0.1% and accepted as 4.55 μ H.

$$L_{mag} = N_1^2 A_L \quad (5.18)$$

5.1.1.3. Output inductor design

The maximum current ripple on the output inductance (ΔI_{Lo-pp}) is defined in equation 5.19. Choosing a high inductance ripple reduces the inductance value and core size required. It also improves system response. It does, however, increase core losses and output voltage ripple. The increased output voltage ripple necessitates the use of a larger capacitor value. EMI is higher at high ripple values. As a result, the current ripple is set to 30%. When ΔI_{Lo-pp} is chosen as 30% of I_{Lo} , I_{Lo-min} and I_{Lo-max} are calculated as 46.75 A and 63.25 A, respectively, according to equations 5.20 and 5.21.

$$\Delta I_{Lo-pp} = I_{Lo-max} - I_{Lo-min} \quad (5.19)$$

$$I_{Lo-min} = I_{Lo} - \frac{\Delta I_{Lo-pp}}{2} \quad (5.20)$$

$$I_{Lo-max} = I_{Lo} + \frac{\Delta I_{Lo-pp}}{2} \quad (5.21)$$

L_o is selected at 100 μ H accordingly. The target parameters for the inductance design are nominal current 55 A, ripple current 16.5 A and ripple frequency 80 kHz. Therefore, it is necessary to select a core with low loss at high frequencies. XFlux type core with code 0078189A7 from Magnetics Company was selected accordingly. A structure combining two of these cores will be used. The parameters of a single core are as given in Table 5.4.

Table 5.4 : 0078189A7 core parameters [63].

Parameter	Value
l_e (cm)	12.5
A_c (cm ²)	2.29
V_e (cm ³)	28.6
A_L (nH)	92
μ_e	40

The magnetic field strength (H) is as given in equation 5.22, and the saturation characteristic of the core is as given in equation 5.23. N represents the number of turns. The coefficients a, b, and c given in the equation depend on the material and geometry. For the selected core, these parameters are as given in Table 5.5. According to equation 5.23, the value of rectifier side inductance under the current should be at the desired value. For this purpose, the number of turns was calculated as 23 with a single iteration. B_{max} in this case is 0.211 T. In addition, μ_e is 96.4%.

$$H = \frac{NI}{l_e} \quad (5.22)$$

$$\% \mu_e = \frac{1}{a + b(4\pi H)^c} \quad (5.23)$$

Table 5.5 : 0078189A7 core saturation characteristic coefficients [64].

Parameter	Value
a	0.01
b	1.843e-8
c	2.358

Core loss (P_{core}) is calculated according to equation 5.24. The coefficients a, b, and c used here are given in Table 5.6. The B_{max} is equal to 0.211 T, f is equal to 80 kHz and V_e is equal to 57.2 cm³ because of the usage of two cores. The result of equation 5.24 is in unit of mW. According to this, P_{core} is equal to 268 W.

$$P_{core} = dB_{max}^e f^g V_e \quad (5.24)$$

Table 5.6 : 0078189A7 core loss characteristic coefficients [64].

Parameter	Value
d	581.54
e	2.015
g	1.194

When $J = 7 \text{ A/mm}^2$ is taken for the conductor cross section to be used in the winding, q is 7.86 mm^2 according to equation 5.17. If two parallel strands with a diameter of 2.3 mm are used for this purpose, q is 8.31 mm^2 . In this case, current density is found to be 6.62 A/mm^2 . The copper losses consist of two parts in this inductor. One of these depends on the DC component and other depends on ripple current. The DC component of current equals to 55 A and for calculating DC resistance of inductor, it is necessary to calculate the length of the conductor. According to the datasheet of 0078744A7 given in Appendix E, the outer diameter (OD) of core is equal to 57.15 mm, the inner diameter (ID) of core is equal to 26.39 mm and the height (HT) of the core is equal to 15.24 mm. The length of one turn (l_{turn}) of the winding is equal to 91.72 mm according to equation 5.25.

$$l_{\text{turn}} = 4\text{HT} + \text{OD} - \text{ID} \quad (5.25)$$

The total length of the one conductor (l_{cond}) is equal to 2.11 m. For a safety 10% higher length will be used in calculations. According to equation 5.26 the total DC resistance (R_{DC}) is calculated as $4.81 \text{ m}\Omega$.

$$R_{\text{DC}} = \frac{\rho_{\text{Cu}} l_{\text{cond}}}{nq} \quad (5.26)$$

According to 55 A DC component and $4.81 \text{ m}\Omega$ of DC resistance, the DC component of copper losses is equal to 14.55 W. For ripple current component of copper losses is depend on the skin depth in the ripple frequency. According to equation 5.16, the skin depth can be found 0.23 mm. Because of the skin depth, the effective conductor cross-sectional area decreased to 1.52 mm^2 . That means the resistance at the 80 kHz is equal to $13.15 \text{ m}\Omega$. The ripple current is equal to 16.5 A. The copper losses at the ripple frequency are equal to 3.58 W. The total copper losses (P_{cu}) in this case are calculated as 18.13 W. The maximum total loss of the output inductance is equal to 286.13 W.

5.1.2. Gate driver design

The gate drive voltage of the module is between -10 V and 20 V [51]. In order to guarantee that the MOSFETs are at turn-off, the use of a totem-pole driver structure is preferred. The output voltages of the totem-pole driver must be obtained from an isolated source. For this purpose, the QA151M isolated DC/DC converter module with a 15 V input voltage is used in the gate driver. The module has output voltages of -5 V and 15 V [65]. These voltage levels are applied to each MOSFET via the totem-pole driver shown in Figure 5.14.

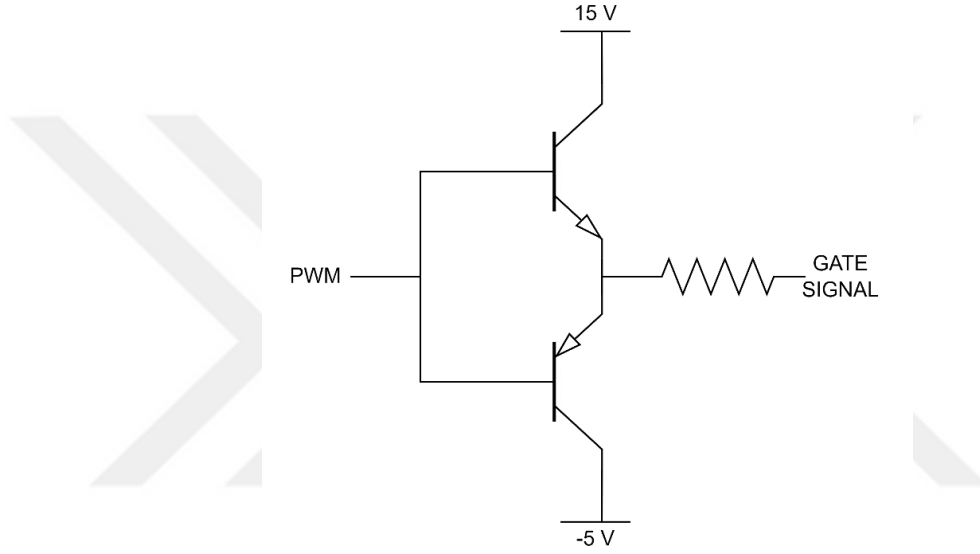


Figure 5.14 : SiC FB MOSFET module gate driver equivalent circuit.

5.1.3. Controller design

In order to control the PSFB ZVT, it is necessary to measure the output voltage (V_o), output current (I_o), and input voltage (V_i). V_i and V_o are measured using voltage dividers, while I_o is measured using a LEM hall effect current sensor. The controller shown in Figure 5.15 includes voltage and current control loops. After finding the error between the output reference voltage (V_{ref}) and V_o , it is passed through a classical proportional and integral (PI) controller. The reference current obtained at the output of the PI controller is then subtracted from I_o to find the current error. To generate the appropriate phase-shift angle, multiply the current error by the current gain (K_{pi}) and added to V_o . The result of the sum is divided by the secondary reduced V_i . Suitable pulse width modulations (PWM) signals will be generated using this phase-shift angle. Equation 5.27 shows the mathematical expression of the generated phase-shift angle.

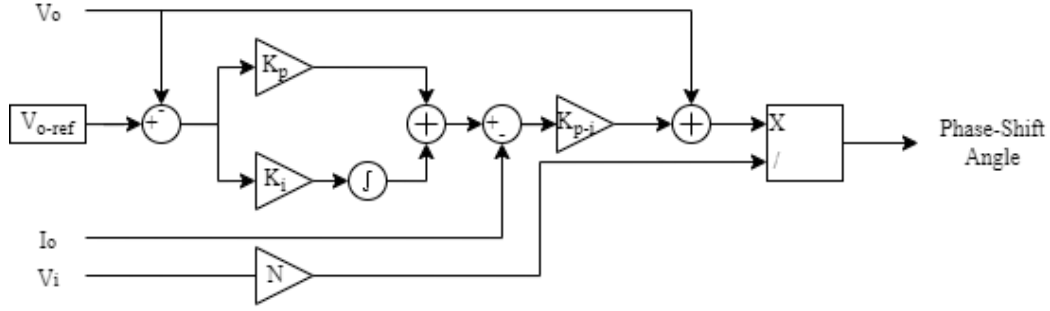


Figure 5.15 : PSFB ZVT controller.

$$\phi = \frac{V_o + K_{p-i} [K_p (V_{o-ref} - V_o) + K_i \int (V_{o-ref} - V_o) - I_o]}{N V_i} \quad (5.27)$$

5.1.4. Modelling and simulation

The ideal simulation model was created using the values obtained as a result of the design. The created model is given in Figure 5.16. The controller block in Figure 5.16 is same as the Figure 4.4. Simulations of the model at maximum output voltage (V_{o-max}), under P_{o-max} , and at V_{o-min} , under P_{o-max} , were performed.

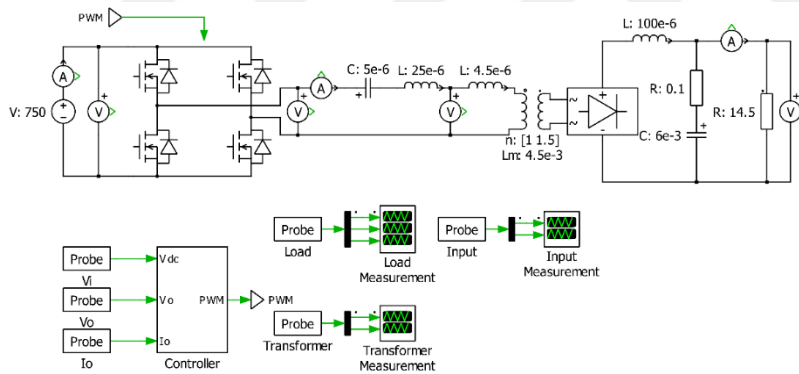


Figure 5.16 : Ideal simulation model with designed parameters.

The model operates at 11 kW when V_i is equal to 750 V and V_{ref} is equal to 700 V. The average value of the current drawn from the DC-link in this case is 14.9 A, and the average power is 11.175 kW. Since V_o is 699.5 V and I_o is 15.7 A, P_o is calculated as 10.982 kW. Figure 5.17 shows the output voltage and current.

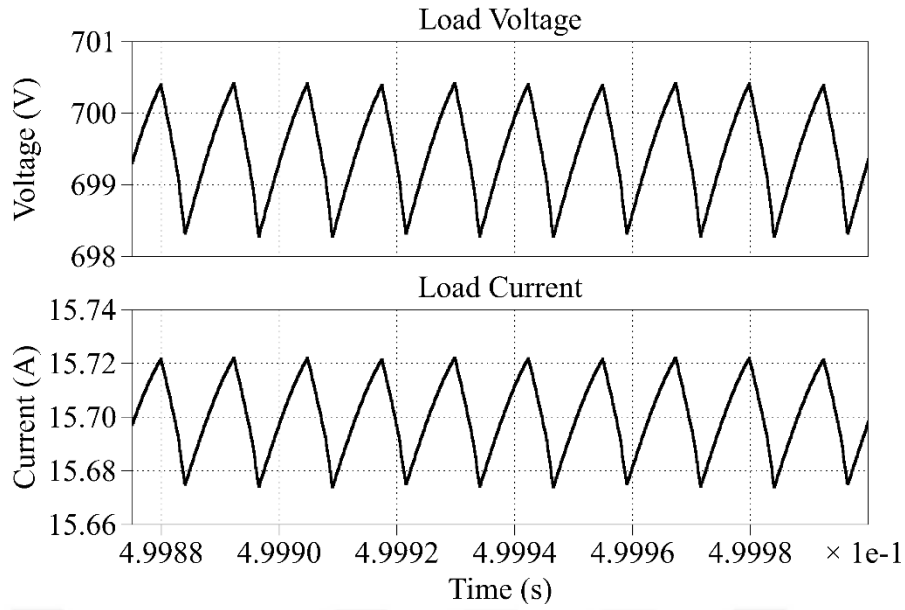


Figure 5.17 : Output voltage and current waveforms when system operates in P_o 11 kW and V_{ref} 750 V.

The RMS value of the transformer voltage in this case is 537.5 V. Also, the RMS current of the transformer is 26.2 A. As can be seen from the waveforms of transformer voltage and current given in Figure 5.18, the peak transformer current is 40.1 A.

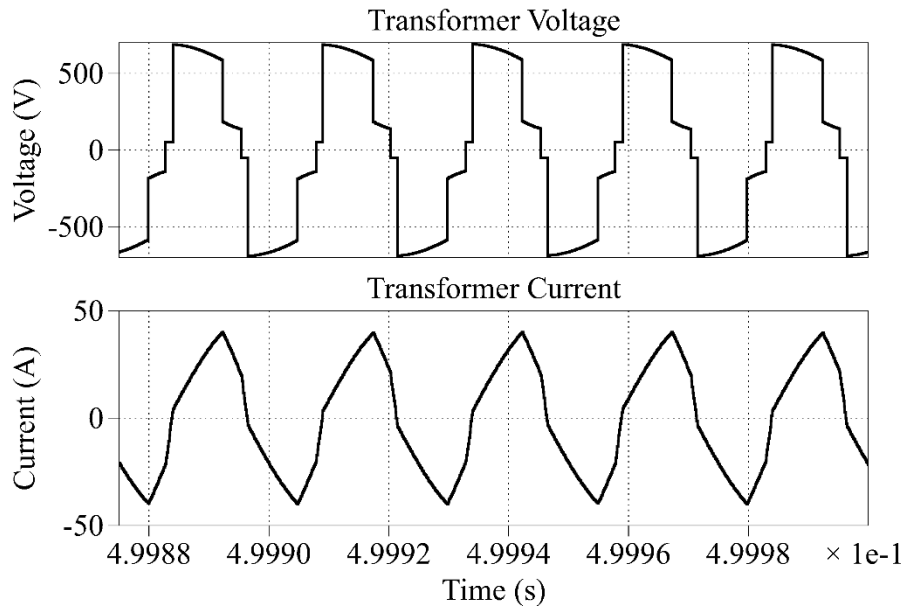


Figure 5.18 : Transformer voltage and current waveforms when system operates in P_o 11 kW and V_{ref} 750 V.

The simulations were run again for P_o 11 kW with V_i 750 V and V_{ref} 200 V. Accordingly, the average value of the current drawn from the DC link is 15.2 A, and the average power is 11.4 kW. Since V_o is 197.3 V and I_o is 54.2 A, P_o is calculated as 10.694 kW. Figure 5.19 shows the output voltage and current.

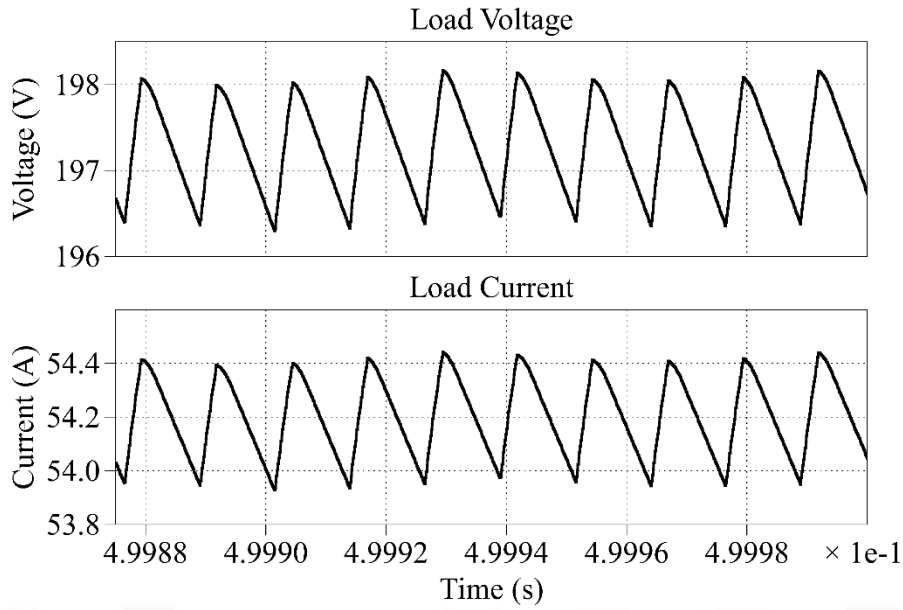


Figure 5.19 : Output voltage and current waveforms when system operates in P_o 11 kW and V_{ref} 200 V.

The RMS value of the transformer voltage in this case is 281 V. Also, the RMS current of the transformer is 71.1 A. As can be seen from the waveforms of transformer voltage and current given in Figure 5.20, the peak transformer current is 95.5 A.

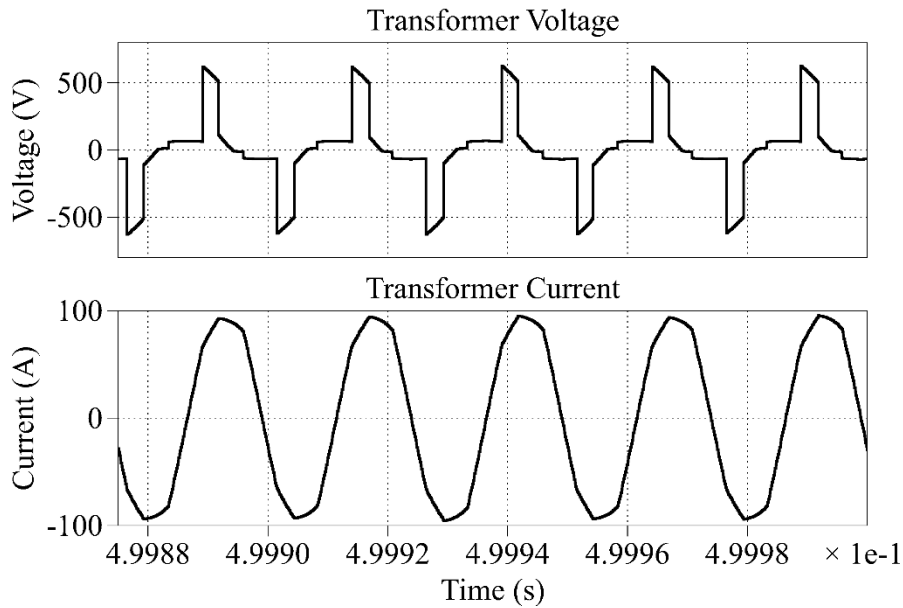


Figure 5.20 : Transformer voltage and current waveforms when system operates in P_o 11 kW and V_{ref} 200 V.

5.2.NPC Rectifier

In the previous section, NPC topology was chosen as the rectifier topology. The main advantages of this topology are low THDi and high efficiency. In this section, the

design of the power circuit will be done first. By analyzing the waveforms, semiconductor selection and power circuit design will be done. After the power circuit is designed, the gate driver and controller will be designed. At final, the NPC rectifier will be modeled and the simulation results will be compared with the design criteria.

5.2.1.Power circuit design

As shown in Figure 4.11 (a), the current waveform of the NPC rectifier operating at 22 kW is given. In this case, where the grid voltage is 380 V, the calculation of the current drawn from each phase is as given in equation 5.28. P_{grid} represents the power drawn from the grid, $V_{\text{L-L}}$ represents the line voltage, and I_{L} represents the phase current.

$$I_{\text{L}} = \frac{P_{\text{grid}}}{\sqrt{3}V_{\text{L-L}}} \quad (5.28)$$

Using equation 5.28, the current drawn from each phase of the NPC rectifier operating at 380 V line voltage and 22 kW output power is 33.42 A. The peak value of this current is calculated as 47.26 A. The junction temperature of a semiconductor will also increase due to losses during operation. Therefore, these criteria should be considered when selecting the semiconductor. Since the use of discrete semiconductor will increase the stray inductance, the use of modules is mostly preferred in industrial applications. In this design, such a choice will be made.

The use of IGBTs is generally preferred in grid-connected, high voltage, and high power applications. Therefore, the Si IGBT module was preferred in the NPC rectifier design. In applications where the grid line voltage is between 380 V and 480 V, modules with a collector-emitter voltage above 600 V are preferred. In addition, in order to react quickly to changes, the system will be allowed to draw current up to 1.5 times the nominal current. Under these conditions, the module to be used must withstand at least 50.13 A RMS. Table 5.7 lists the modules available from Infineon and Semikron, along with their saturation collector-emitter voltage ($V_{\text{CE(sat)}}$) and nominal collector current ($I_{\text{C-nom}}$).

Table 5.7 : Parameters of different Si NPC IGBT modules [66–72].

Manufacturer	Manufacturer Product Code	$V_{CE(sat)}$ (V)	I_{C-nom} (A)
Infineon	F3L75R07W2E3_B11	1.45	75
Infineon	F3L100R07W2H3_B11	1.68	100
Infineon	F3L100R07W2E3_B11	1.45	100
Semikron	SK75MLI066T	1.45	75
Semikron	SK75MLI07S5TD1E1	1.42/1.10	75
Semikron	SKiP 26MLI07E3V1	1.45	75
Semikron	SK100MLI066T	1.45	100
Semikron	SK100MLI07F3TD1p	1.85/1.45	100
Semikron	SK100MLI07S5TD1E2	1.35	100
Semikron	SKiP 27MLI07E3V1	1.45	100

Infineon's F3L100R07W2H3_B11 is not preferred because it has a higher saturation collector-emitter voltage than other Infineon modules. Since F3L100R07W2E3_B11 has a higher I_{C-nom} F3L75R07W2E3_B11, its internal thermal design will be better [66–68]. When Semikron's equivalent modules are compared, SK100MLI07S5TD1E2 has a lower saturation collector-emitter voltage, but its size is larger [73]. It will not be preferred because it may complicate the mechanical design of the system and reduce the power density. Likewise, SK100MLI066T also remains large in size [72]. The SKiP 27MLI07E3V1 module, on the other hand, is both large in size and difficult to design due to its contact structure [74]. Therefore, the NPC module from Infineon brand F3L100R07W2E3_B11, which is given in Figure 5.21, will be used on the rectifier side.

**Figure 5.21 :** F3L100R07W2E3_B11 Si NPC IGBT module [68].

5.2.2. Gate driver design

The gate drive voltage of the module is between -20 V and 20 V [68]. In order to guarantee that the IGBTs are at turn-off, the use of a totem-pole driver structure is

preferred like PSFB ZVT gate driver. The output voltages of the totem-pole driver must be obtained from an isolated source. For this purpose, the QA151 isolated DC/DC converter module with a 15 V input voltage is used in the gate driver. The module has output voltages of -8 V and 15 V [75]. These voltage levels are applied to each IGBT via the totem-pole driver shown in Figure 5.22.

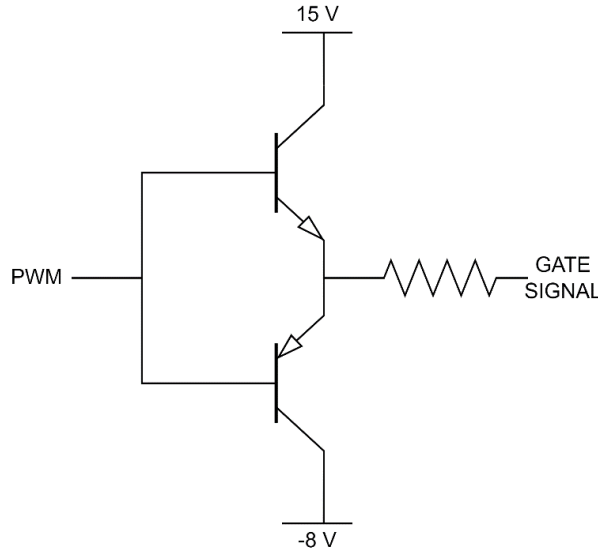


Figure 5.22 : Si NPC IGBT module gate driver equivalent circuit.

5.2.3. Controller design

The control of the NPC rectifier consists of four main parts: the phase-locked loop (PLL) algorithm, the DC-link controller, the current controller and voltage controller. With the help of PLL, the phase angle of the grid voltage is determined and synchronization to the grid is provided. The three phase currents and voltages are converted to a rotating reference frame (RRF) with Clarke-Park transformations and then they are processed in the RRF. DC-link voltage regulation is performed with the d-axis component in the RRF. For a normal operating mode, the q-axis current component reference can be taken as 0, and the power factor (PF) can be 1. If there is a different operating condition, the required reference current command can be entered as a reference. With the help of the current controller, the references generated in the RRF are converted into current commands. Reference signals are generated by making appropriate transformations to these current commands. With the help of reference signals, appropriate PWM signals are transmitted to the power circuit.

With the PLL algorithm given in Figure 5.23, the instantaneous phase angle of the grid (Θ_{grid}) is determined and synchronization to the grid is provided. For this purpose, the grid voltages at the RRF are calculated using the Clarke-Park transformation given in equation 5.29. Phase voltages represent here with V_A , V_B , and V_C . The grid q-axis voltage ($V_{q\text{-grid}}$) is set to zero with the help of a PI controller. The Θ_{grid} is calculated by taking the integral of the output of the PI controller. Since the Θ_{grid} is also used in Clarke-Park transformations, this controller is a closed loop in itself. The grid d-axis voltage ($V_{d\text{-grid}}$), $V_{q\text{-grid}}$, and Θ_{grid} obtained at the output of this controller are used again in other blocks.

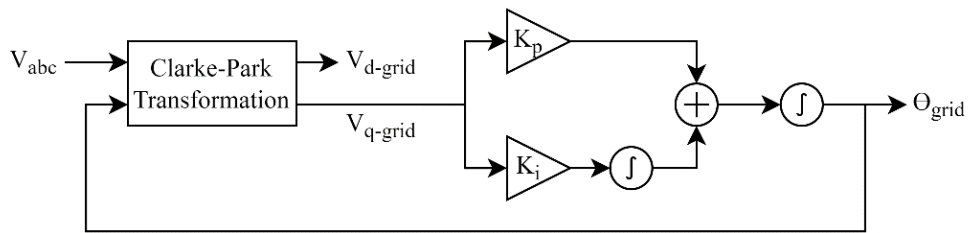


Figure 5.23 : PLL algorithm.

$$\begin{bmatrix} V_{d\text{-grid}} \\ V_{q\text{-grid}} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta_{\text{grid}}) & \cos\left(\theta_{\text{grid}} - \frac{2\pi}{3}\right) & \cos\left(\theta_{\text{grid}} + \frac{2\pi}{3}\right) \\ \sin(\theta_{\text{grid}}) & \sin\left(\theta_{\text{grid}} - \frac{2\pi}{3}\right) & \sin\left(\theta_{\text{grid}} + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} \quad (5.29)$$

In the DC-link controller, the DC link voltage measurements (V_{dc1} and V_{dc2}) are used. The DC-link consists of two parts; the voltages after the measurement are summed with each other and subtracted from the DC-link reference voltage ($V_{\text{dc-ref}}$) to find the DC-link voltage error. The DC-link voltage error is converted to reference d-axis current ($I_{d\text{-ref}}$) with the help of the PI controller. Also, in order to make V_{dc1} and V_{dc2} balanced, they are subtracted from each other to calculate the reference zero-axis current ($I_{0\text{-ref}}$). The DC-link controller is as shown in Figure 5.24.

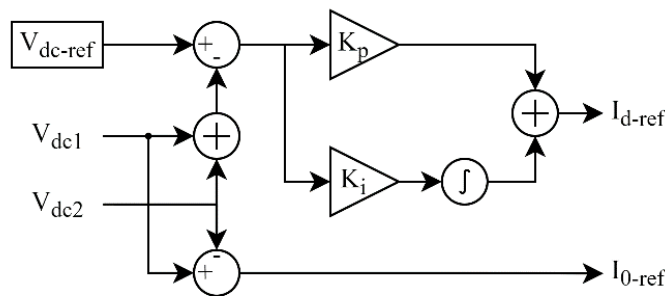


Figure 5.24 : DC-link controller.

Using the measured rectifier currents (I_{abc}) and the Θ_{grid} obtained in the PLL algorithm, the rectifier currents are converted to RRF by equation 5.30. Current errors are found by subtracting the d-axis component from $I_{d\text{-ref}}$ and the q-axis component from the reference q-axis component ($I_{q\text{-ref}}$). $I_{q\text{-ref}}$ is taken as 0 in the case where the power factor is 1. The obtained current errors and $I_{0\text{-ref}}$ component are multiplied by the gains and converted to reference voltages at the RRF, as shown in Figure 5.25. The d-axis reference voltage ($V_{d\text{-ref}}$), q-axis reference voltage ($V_{q\text{-ref}}$), and 0-axis reference voltage ($V_{0\text{-ref}}$) are sent to the voltage controller.

$$\begin{bmatrix} I_{d\text{-rect}} \\ I_{q\text{-rect}} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta_{\text{grid}}) & \cos\left(\theta_{\text{grid}} - \frac{2\pi}{3}\right) & \cos\left(\theta_{\text{grid}} + \frac{2\pi}{3}\right) \\ \sin(\theta_{\text{grid}}) & \sin\left(\theta_{\text{grid}} - \frac{2\pi}{3}\right) & \sin\left(\theta_{\text{grid}} + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \quad (5.30)$$

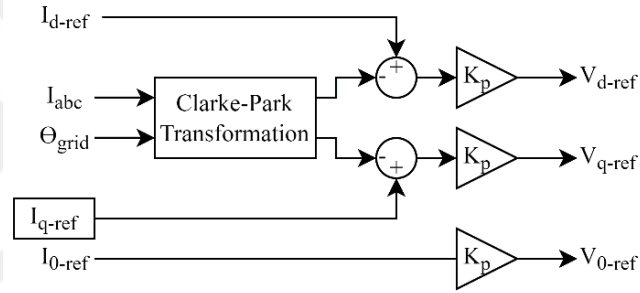


Figure 5.25 : Current controller.

$V_{d\text{-grid}}$ obtained in the PLL algorithm is summed with $V_{d\text{-ref}}$ obtained in the current controller, and $V_{q\text{-grid}}$ obtained in the PLL algorithm is summed with $V_{q\text{-ref}}$ obtained in the current controller. The inverse Clarke-Park transformation is applied according to equation 5.31 with the Θ_{grid} calculated in the PLL algorithm. By adding $V_{0\text{-ref}}$ to the values obtained as a result of the transformation and dividing by half the sum of the DC link voltage, modulation signals for three phases are generated as given in Figure 5.26.

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta_{\text{grid}}) & \sin(\theta_{\text{grid}}) \\ \cos\left(\theta_{\text{grid}} - \frac{2\pi}{3}\right) & \sin\left(\theta_{\text{grid}} - \frac{2\pi}{3}\right) \\ \cos\left(\theta_{\text{grid}} + \frac{2\pi}{3}\right) & \sin\left(\theta_{\text{grid}} + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \quad (5.31)$$

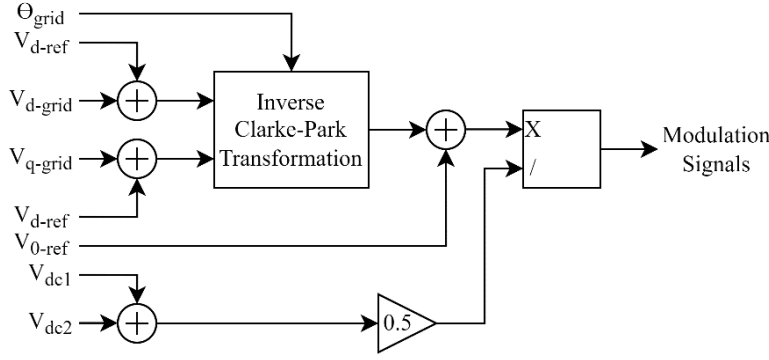


Figure 5.26 : Voltage controller.

The modeling and simulation of the rectifier are not done in this chapter since they will not give correct results without the design of the grid connection filter. In the next section, after the design of the grid connection filter, the modeling and simulation of the rectifier and the filter will be performed together.

5.3.Grid Connection Filter

According to the IEEE 519 standard, the limits of the TDD values of the current to be drawn from the grid were given in the standards section [13]. It was also mentioned that the LCL filter has the best damping performance when analyzing filter topologies. According to these, the LCL filter was selected as the grid connection filter topology to be used. After analyzing the damping performance of the LCL filter to be designed, the use of damping resistance and a trap filter will be studied if necessary.

5.3.1.Design

In the LCL filter topology given in Figure 5.27, V_{grid} represents the grid voltage, V_r represents the rectified DC-link voltage, I_{grid} represents the grid current, I_c represents the filter capacitor current, and I_r represents the rectifier current. Accordingly, the transfer function of the relationship between V_r and I_r is given in equation 5.32. Equation 5.33 shows the transfer function of the relationship between V_r and I_{grid} .

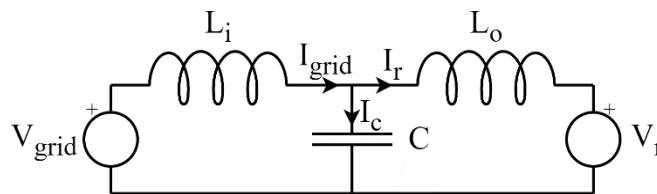


Figure 5.27 : LCL filter topology equivalent circuit.

$$\frac{I_r(s)}{V_r(s)} = \frac{1}{sL_o} \frac{s^2 + \frac{1}{C(L_i + L_o)}}{s^2 + \frac{L_i + L_o}{CL_i L_o}} \quad (5.32)$$

$$\frac{I_{grid}(s)}{V_r(s)} = \frac{1}{sCL_i L_o} \frac{1}{s^2 + \frac{L_i + L_o}{CL_i L_o}} \quad (5.33)$$

5.3.1.1.LCL filter

The voltage drop across the LCL filter is chosen to be less than 2% of the grid voltage at full load. In this way, the losses on the LCL filter can be minimized. The maximum filter impedance (Z_{f-max}) is calculated as 131 mΩ according to equation 5.34.

$$Z_{f-max} = \frac{V_{L-L}^2}{P_o} 0.02 \quad (5.34)$$

When capacitor current is neglected, the filter impedance (Z_f) depends on L_i and L_o . Therefore, the maximum sum of L_i and L_o is calculated as 417 μH according to equation 5.35. Here, f_{grid} represents the grid frequency.

$$Z_f = 2\pi f_{grid}(L_i + L_o) \quad (5.35)$$

If the ratio between L_i and L_o is 3, and the total inductance is chosen to be 400 μH, then L_i is 100 μH and L_o is 300 μH. Since rectifier side inductance also contains switching noise, there is a component at switching frequency in the current flowing through it. It will be designed with the assumption that this component will be 20% of the current. Since grid side inductance has a filtered current, it has a single component at the rated current at grid frequency.

Since the inductance at the PSFB ZVT output is close to the inductance parameters in the grid connection filter, the same core structure will be used. This will make material supplies easier. L_i was chosen as the 100 μH. Since the core saturation characteristic is the same as equation 5.25 and the coefficients are the same as Table 5.5, the current dependents H , B_{max} , and P_{core} are calculated again. In the case where the number of turns was chosen as 23, B_{max} was calculated as 0.391 T and P_{core} as 0.14 W at 33.42 A, which is the current at full load. In this case, L_i is 92.5 μH when saturated at full load.

For L_o , the same core structure will be preferred. However, the ripple current in the switching frequency should be considered here. According to this, the target inductance can be reached in 46 turns. $B_{\max}$ at full load is 0.544 T, and P_{core} is 10.7 W. The inductance in the saturated condition is 307 μH . The reasons for the increase in P_{core} are the increases in H and $B_{\max}$ due to the number of turns. Also, the high-frequency component is also shown in the P_{core} .

For the choice of C , it is necessary to pay attention to the resonant frequency of the filter given in equation 3.2. As a result of the studies, resonant frequency should be at least 10 times greater than f_{grid} and less than half of switching frequency [11]. Accordingly, the resonant frequency should be higher than 500 Hz and lower than 8 kHz. The lowest filter capacitor value ($C_{\min}$) that can be selected is 5.28 μF according to equation 5.36, and the highest filter capacitor value ($C_{\max}$) that can be selected is 1.35 mF according to equation 5.37.

$$C_{\min} = \frac{L_i + L_o}{\pi^2 f_{\text{sw}}^2 L_i L_o} \quad (5.36)$$

$$C_{\max} = \frac{L_i + L_o}{400\pi^2 f_{\text{grid}}^2 L_i L_o} \quad (5.37)$$

Since the C range that can be selected has been determined, frequency analyses were performed for different C values. As seen in Figure 5.28, the resonant frequency decreases with increasing C values. It can also be observed that the damping performance at high frequencies increases with a higher C selection. The main reason for this is that the capacitor impedance (Z_c) decreases with increasing frequency (f) and increasing C , as given in equation 5.38. Therefore, using a high C value can filter high frequencies better. However, I_c can reach very high values. In addition, high- C selection has the risk of resonance with other devices connected to the grid.

$$Z_c = \frac{1}{2\pi f C} \quad (5.38)$$

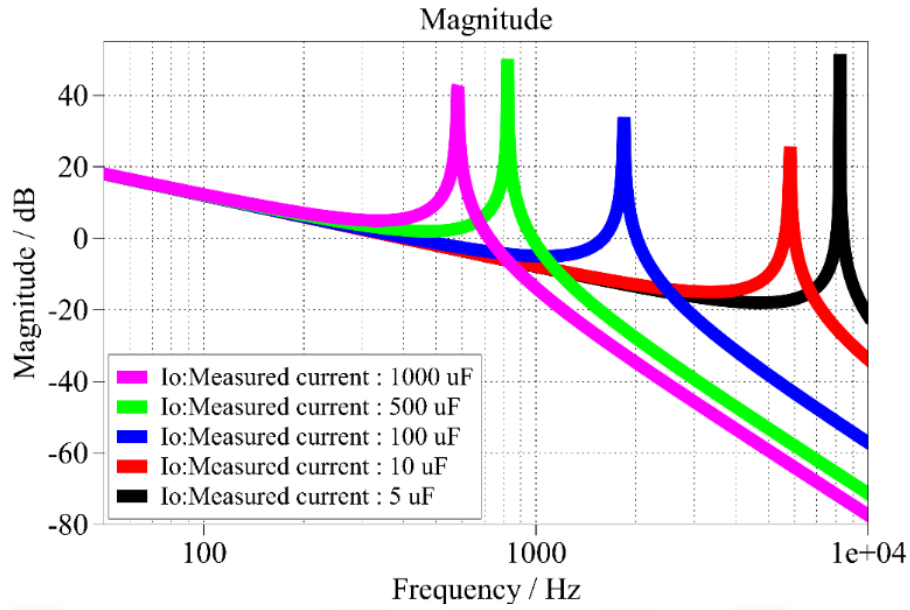


Figure 5.28 : Frequency responses of different C values.

Considering the frequency analysis, a small C value will be preferred to avoid the risk of resonance. Accordingly, the most appropriate value within the limits was found to be 5 μF , and was chosen. The frequency of filtering high frequencies and the amplification effect at the resonance point when C is 5 μF are as shown in Figure 5.29.

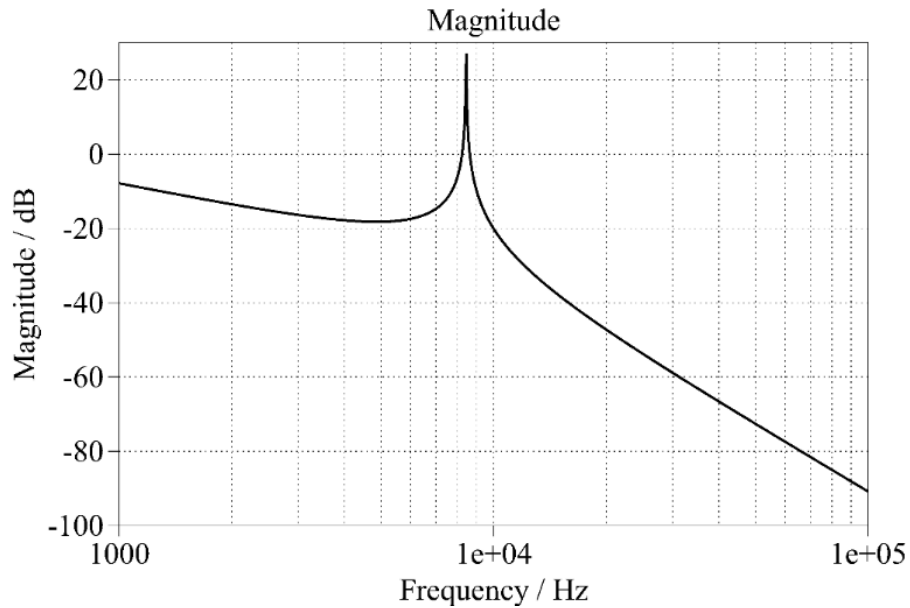


Figure 5.29 : Frequency response of C selected as 5 μF .

As can be seen from the frequency response, there is a 27 dB amplification effect at the resonance point of 8.5 kHz and a 40 dB attenuation at switching frequency. Since the amplification effect at the resonance point can be risky, active damping, passive damping, or both are necessary. Active damping will not be preferred as it requires

modification of the controller and the number of measurements will increase. For this purpose, passive damping will be used by connecting a damping resistor in series to C. In a study, it was found that the selection of damping resistor should be made depending on C and resonant frequency [76]. The calculated R was 1.25 Ω , according to equation 5.39. When the frequency response shown in Figure 5.30 is examined again after the damping resistor is added, it is seen that the amplification effect at the resonant frequency changes from 40 dB to 16 dB of damping. However, the damping resistor also reduced the damping effect at high frequencies.

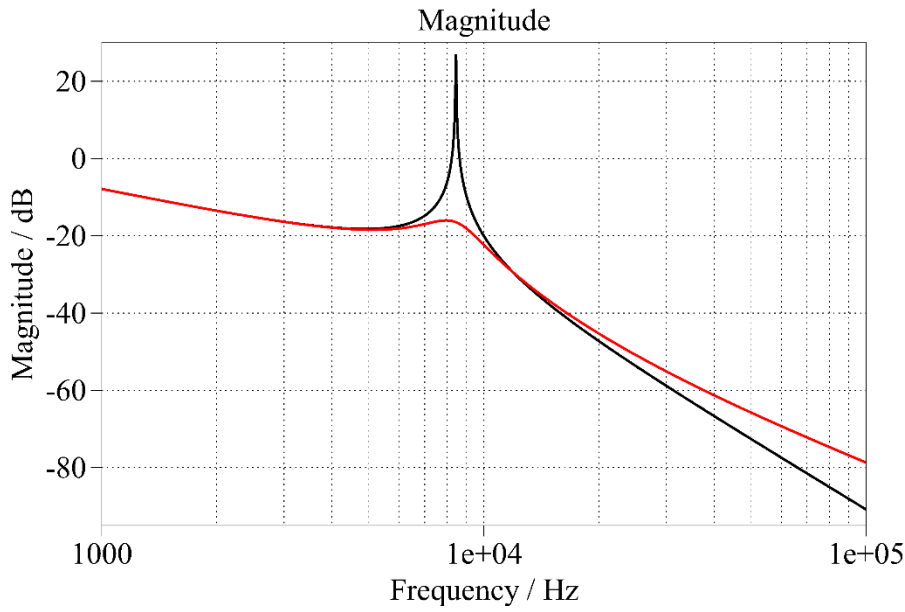


Figure 5.30 : Frequency response of filter without damping resistor (black) and with damping resistor (red).

$$R = \frac{1}{6\pi f_{\text{res}} C} \quad (5.39)$$

5.3.1.2. Trap filter

For a trap filter, L_t and C_t values must be selected. According to equation 5.40, the product of L_t and C_t is found to be 98.9e-12 HF. The damping performance of trap filter for different L_t and C_t values is given in Figure 5.31.

$$L_t C_t = \frac{1}{4\pi^2 f_{\text{sw}}^2} \quad (5.40)$$

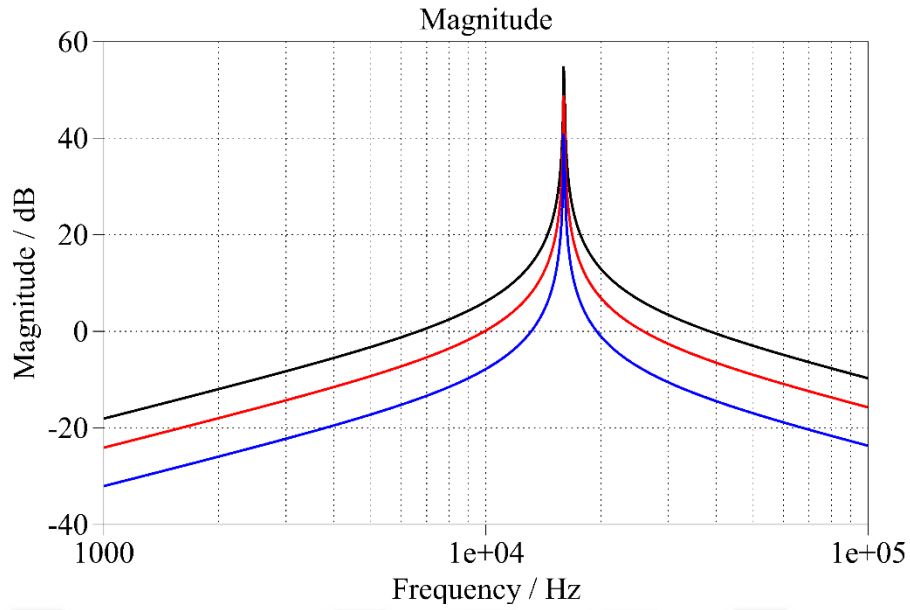


Figure 5.31 : Trap filter filtering performance for 5 μH with 19.8 μF (black), 10 μH with 9.9 μF (red) and 25 μH with 3.96 μF (blue).

As seen in the frequency response, a low L_t value has a higher damping effect at the frequency at which it is tuned. But it reduces the damping effect at other frequencies. However, since the damping difference at the tuned frequency does not change much, it is preferable to choose a high value of L_t . Therefore, 24.7 μH is selected as L_t and 4 μF is selected as C_t for trap filter design. Sendust-type Micrometal cores are preferred for magnetic elements operating directly at high frequencies. For these power levels and applications, MS-157026-2 core is preferred. The outer diameter (OD), inner diameter (ID), height (HT), l_e , A_c , V_e , A_L , and μ_e values of the core are given in Table 5.8 [77].

Table 5.8 : MS-157026-2 core parameters [77].

Parameter	Value
OD (mm)	40.69
ID (mm)	23.32
HT (mm)	15.37
l_e (cm)	9.85
A_c (cm ²)	1.07
V_e (cm ³)	10.5
A_L (nH)	35
μ_e	26

The saturation characteristic of the core is the same as Magnetics and is given in equation 5.25. The coefficients to be used here are as given in Table 5.9.

Table 5.9 : MS-157026-2 core saturation characteristic coefficients [77].

Parameter	Value
a	0.01
b	2.061e-7
c	1.995

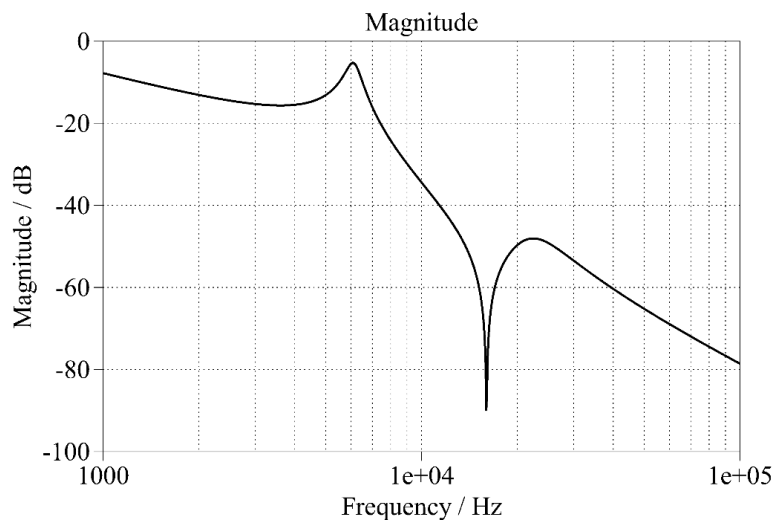
The core loss density characteristic is given in equation 5.41 [77]. The coefficients to be used here are as given in Table 5.10.

$$P_{core} = \frac{f}{\frac{d10^{12}}{B^3} + \frac{e10^{9.2}}{B^{2.3}} + \frac{g10^{6.6}}{B^{1.65}}} + hB^2f^210^{-8} \quad (5.41)$$

Table 5.10 : MS-157026-2 core loss characteristic coefficients [77].

Parameter	Value
d	1e6
e	4.969e8
g	3.993e6
h	2.867e-14

In the given characteristics, the appropriate trap inductance was designed. Accordingly, the desired target value was achieved with 27 turns. In this case, B_{max} is 0.1 T and P_{core} is 1.6 W. The frequency analysis of the whole designed grid connection filter is given in Figure 5.32. According to this, the amplification effect at the resonance point can be dampened. Also, the damping performance at switching frequency is 90 dB.

**Figure 5.32 :** Designed grid connection filter frequency analysis.

5.3.2. Modelling and simulation

The modeling of the filter and rectifier design is given in Figure 5.33. The controller block used in the Figure 5.33 is same as the Figure 4.10. At this stage, ideal elements without magnetic and thermal modeling were used.

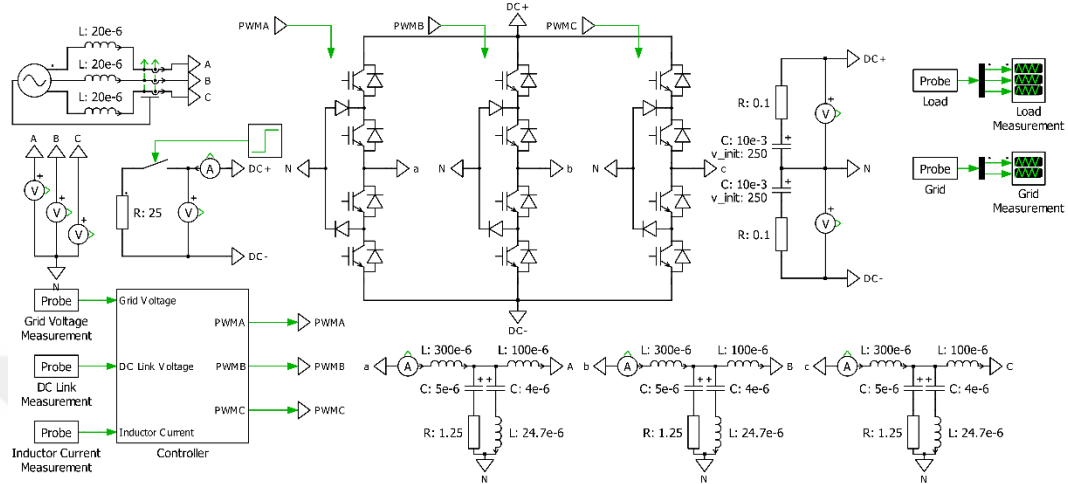


Figure 5.33 : Rectifier and grid connection filter simulation model.

The model was run with a 22 kW load. The grid voltage and current are given in Figure 5.34. When V_{L-L} is 380 V, the current drawn from the grid is 34.7 A. It can also be seen that there is no phase difference between voltage and current. THDi is 2.7% and complies with the IEEE 519 standard.

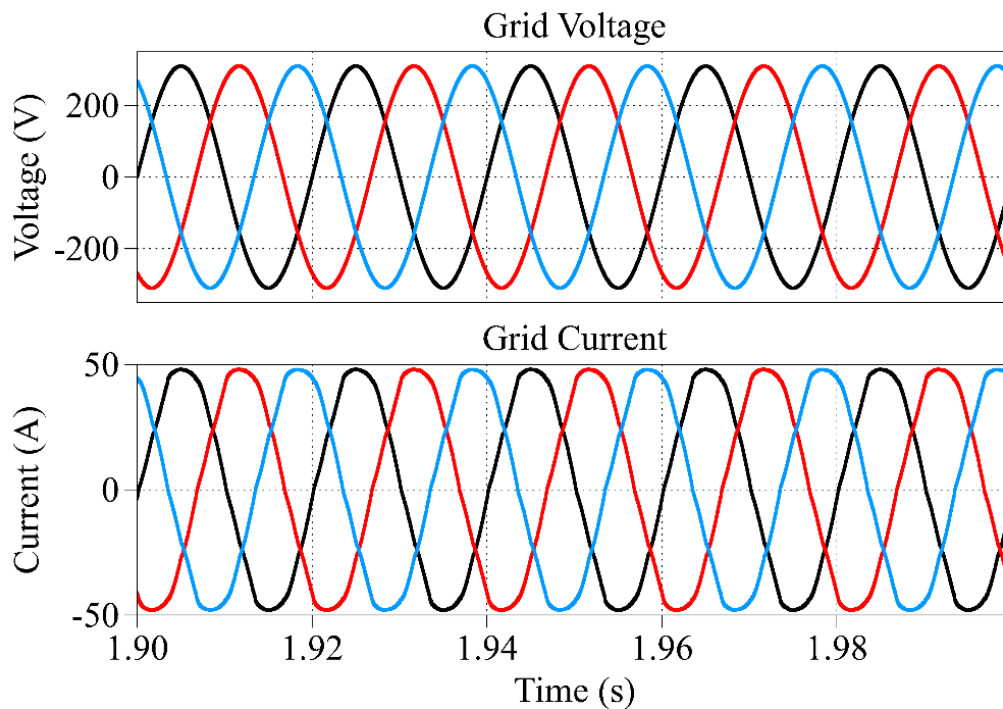


Figure 5.34 : Grid voltage and current at 22 kW load.

Under the given operating condition, the DC link voltage can be stabilized at 746 V and oscillates between 740 V and 752 V. Figure 5.35 shows the voltage, current, and power of the load connected to the DC-link.

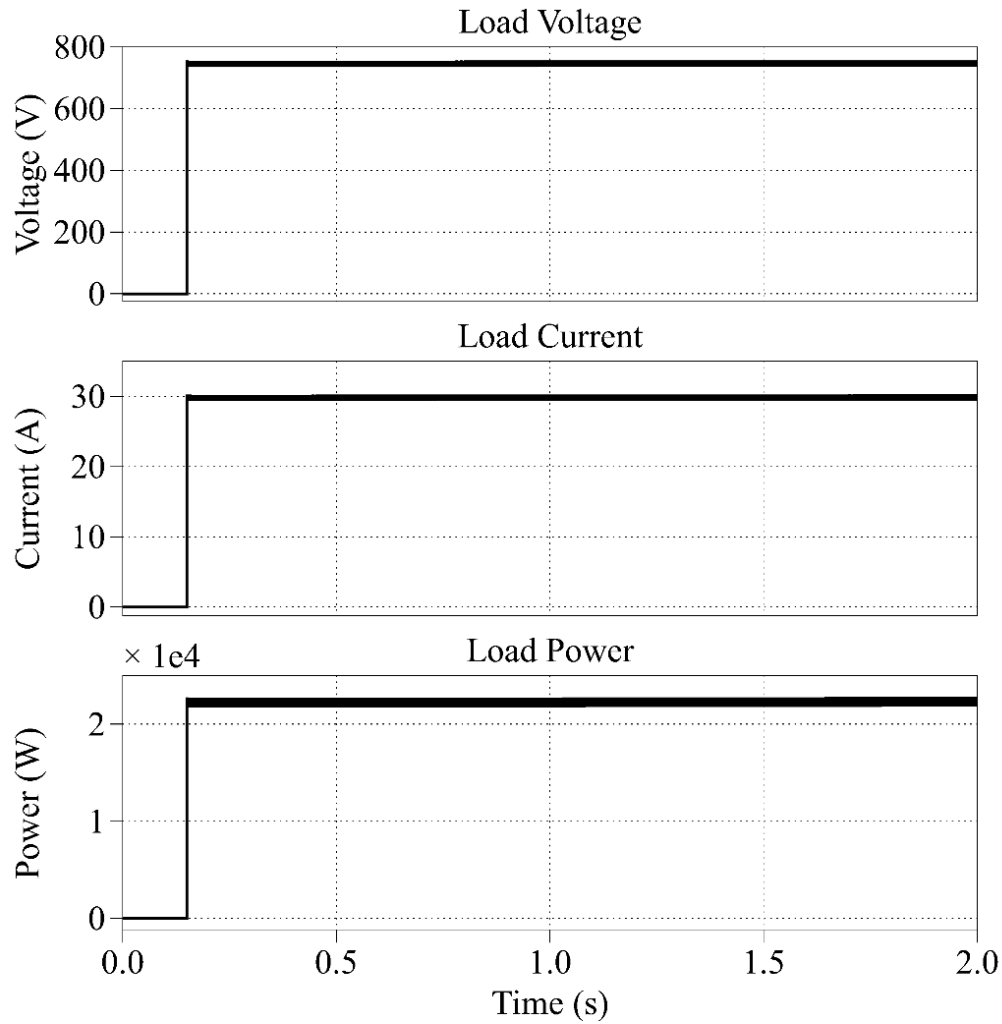


Figure 5.35 : Load voltage, current, and power at 22 kW load.

In addition, the inductance on the rectifier side has a current of 35 A and contains a component of 2.7 A in switching frequency. The current of this inductance is given in Figure 5.36.

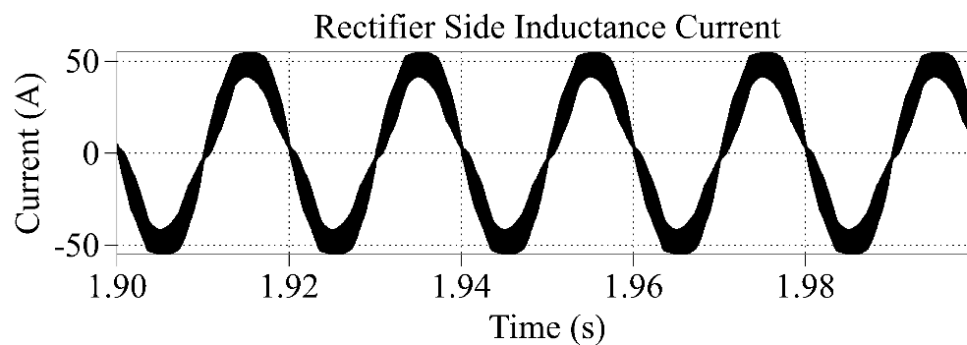


Figure 5.36 : Rectifier side inductor current waveform.

The current of the capacitor and trap filter in the grid connection filter is as given in Figure 5.37. There is 1.6 A of current flowing through the capacitor line and 4.3 A of current flowing through the trap line.

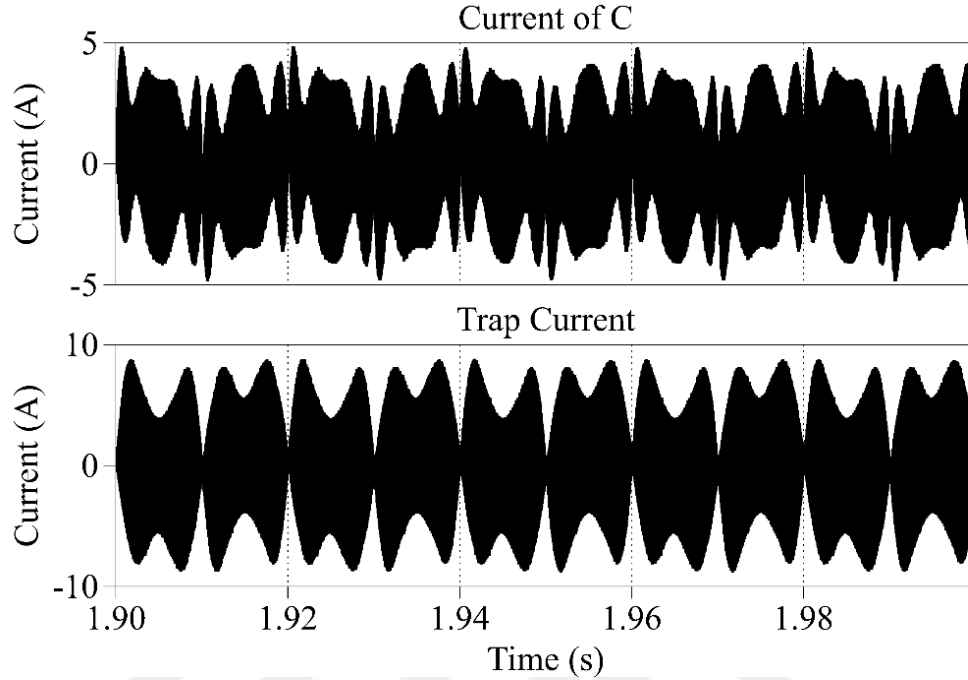


Figure 5.37 : Current waveforms of capacitor and trap line.

5.4.System Design

After the designs of the NPC rectifier, grid connection filter, and DC/DC converter are completed, the system will be modeled and simulated. After thermal modeling of semiconductor modules and magnetic modeling of magnetic materials, the models will be run. The cooling system design will be realized according to the simulation results. In addition, PCB designs will be made and experimental studies will be carried out. Electrical modeling will not be discussed in this section as it is done in the design stage of modeling.

5.4.1.System modelling and simulation

All modeling and simulations will be performed in the PLECS package program, which is specialized for power electronics. This package program contains four different domains in which simulations are performed. These domains are the electrical domain, the magnetic domain, the thermal domain, and the mechanical domain. In this study, except for the mechanical domain, the other three domains will be used. Electrical models made during the design phase will be combined at this stage. In

addition, for the analysis of the losses of semiconductor modules, the characteristics of the modules will be modeled. The obtained loss values will be transferred to the thermal domain, and temperatures will be analyzed. In addition, the characteristics of the magnetic materials to be used will be transferred to the program, and their operating conditions under current will be observed in the magnetic domain.

5.4.1.1. Thermal modelling

Turn-on energies, turn-off energies, conduction losses, and thermal impedances were modeled using the datasheets of the modules. The characteristics of each IGBT and body diode in the NPC module are the same. However, the characteristics of the clamping diodes are different from the body diodes. For this purpose, it is necessary to model one IGBT and two diodes. The conduction losses of the IGBT in the module is given in Figure 5.38.

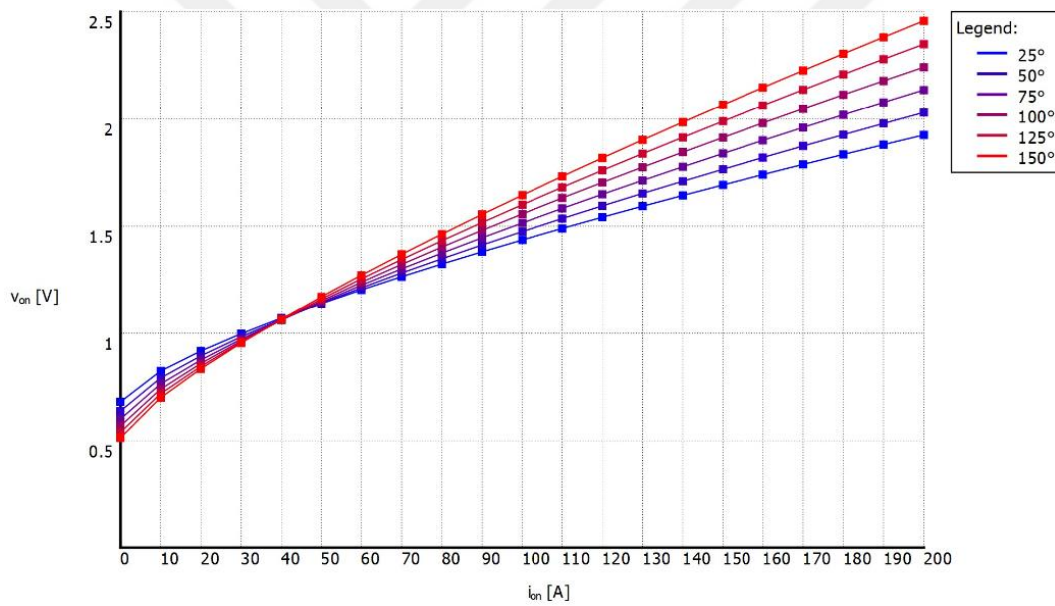


Figure 5.38 : Conduction loss characteristic of IGBT in F3L100R07W2E3_B11.

The turn-on energy characteristic of the IGBT in the module is given in Figure 5.39 (a), and the turn-off energy characteristic is given in Figure 5.39 (b). The parameters of the Cauer thermal equivalent circuits of the IGBTs in the module are given in Table 5.11.

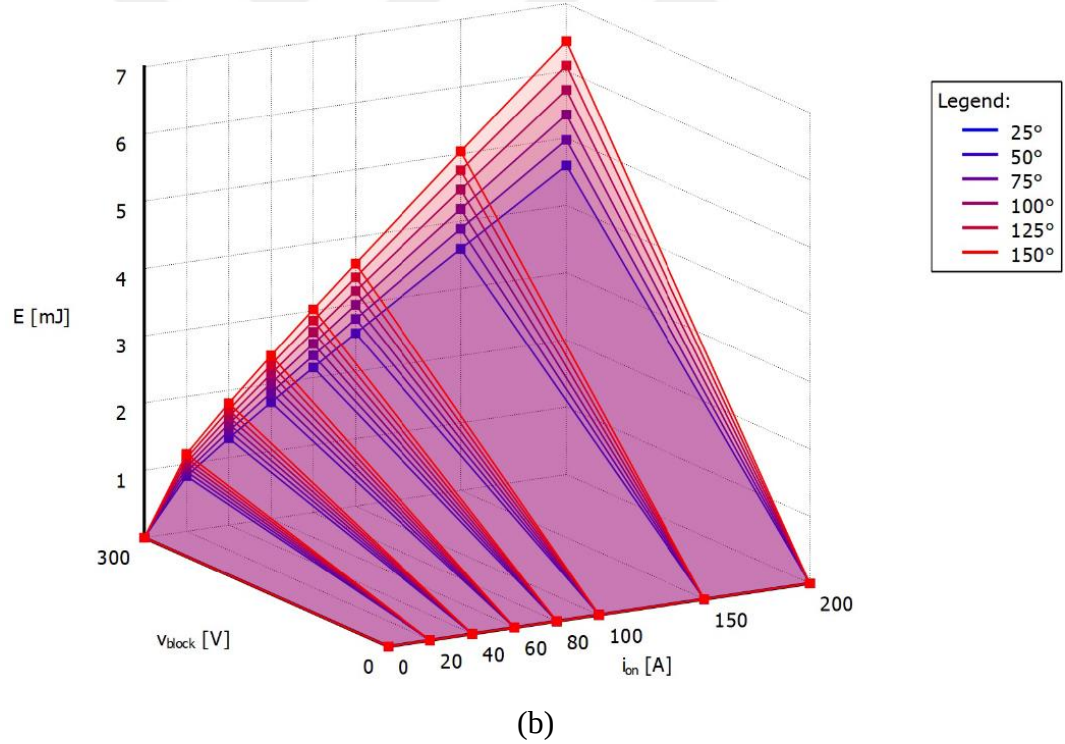
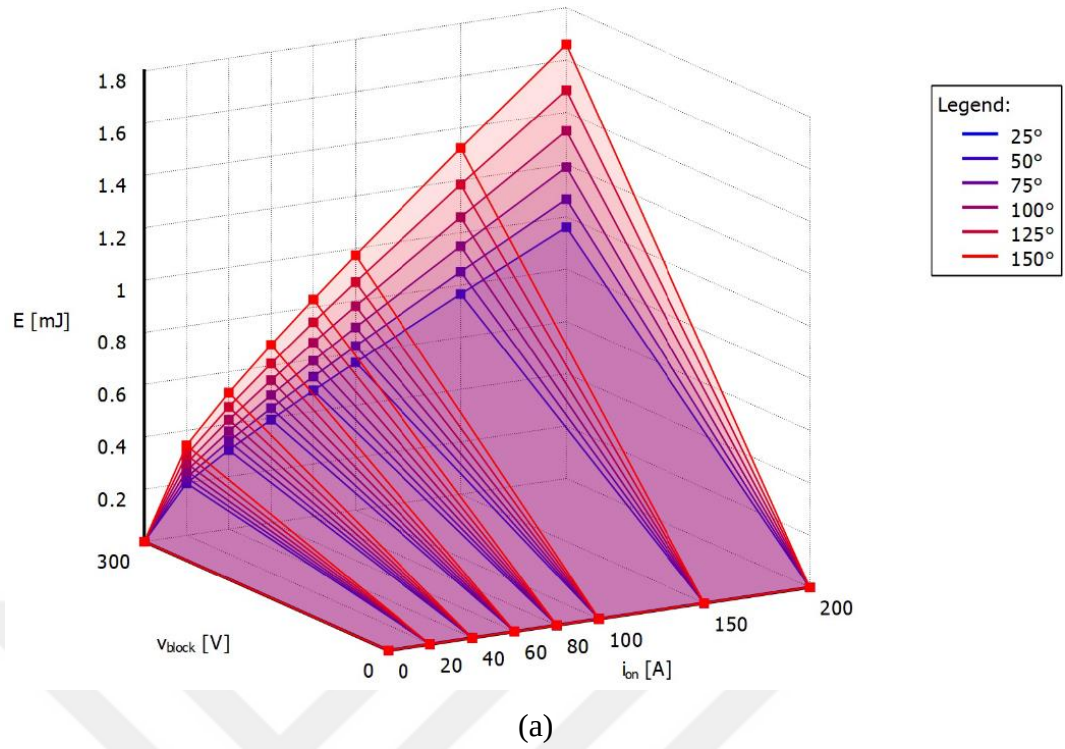


Figure 5.39 : Turn-on energy (a), and turn-off energy (b) characteristics of IGBT in F3L100R07W2E3_B11.

Table 5.11 : Cauer equivalent circuit parameters of IGBT in F3L100R07W2E3_B11.

Element	1	2	3	4
R (K/W)	0.06493	0.1747	0.4749	0.2365
C (J/K)	0.01009	0.03549	0.08364	0.6552

The turn-on energies of the body diodes and clamping diodes in the module are not published by the manufacturer. The main reason for this is that the turn-on energies of the diodes are negligibly small compared to the turn-off energies and conduction losses. The conduction loss characteristic of the body diodes in the module is given in Figure 5.40, and the turn-off energy characteristic is given in Figure 5.41. The parameters of the Cauer thermal equivalent circuits of the body diodes in the module are given in Table 5.12.

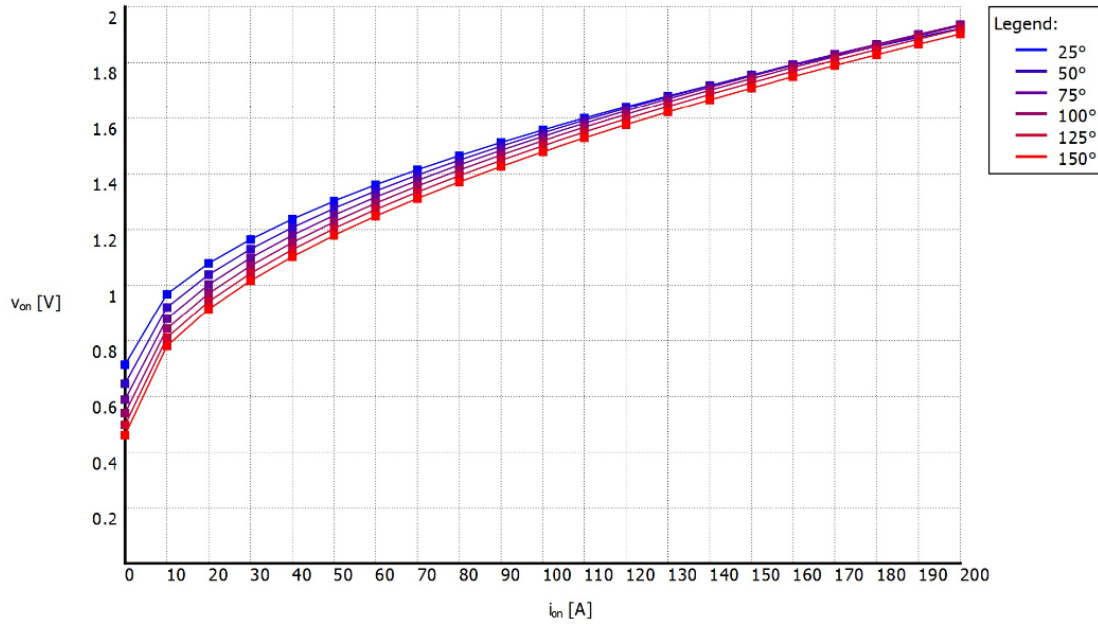


Figure 5.40 : Conduction loss characteristic of body diode in F3L100R07W2E3_B11.

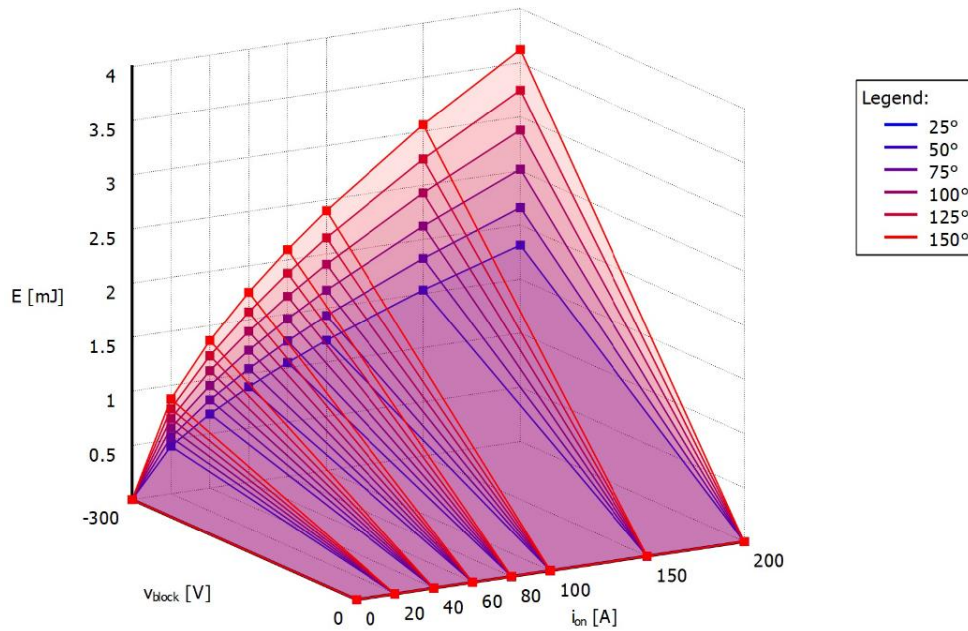


Figure 5.41 : Turn-off energy characteristic of body diode in F3L100R07W2E3_B11.

Table 5.12 : Cauer equivalent circuit parameters of body diodes in F3L100R07W2E3_B11.

Element	1	2	3	4
R (K/W)	0.1253	0.2736	0.6042	0.2469
C (J/K)	0.005133	0.01984	0.07144	0.6722

Finally, the characteristics of the clamp diodes in the NPC module are modeled. The conduction loss characteristic is shown in Figure 5.42, and the turn-off energies are shown in Figure 5.43. The parameters of the Cauer thermal equivalent circuits of the clamping diodes in the module are given in Table 5.13.

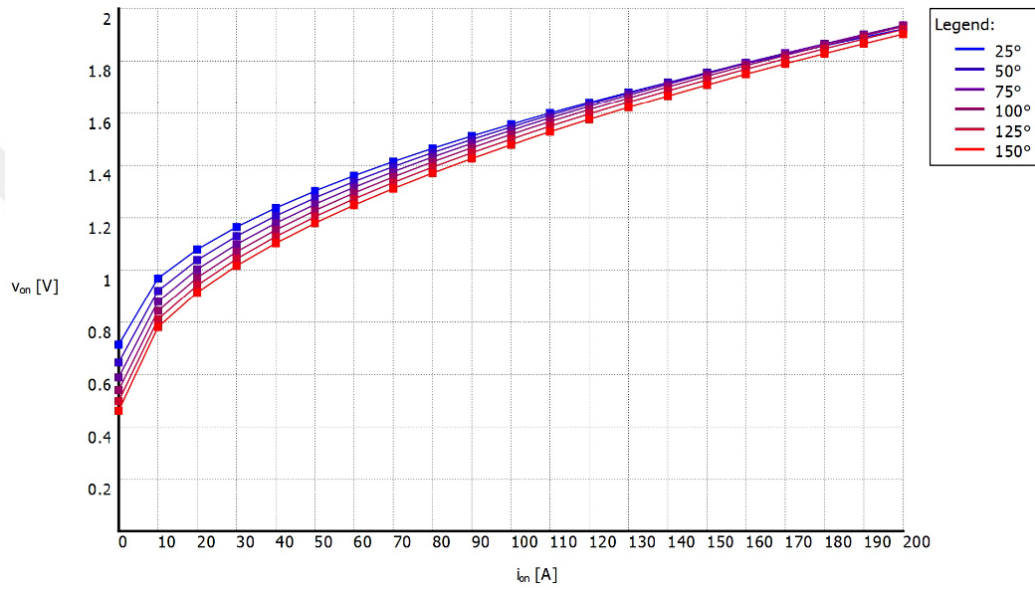


Figure 5.42 : Conduction loss characteristic of clamping diode in F3L100R07W2E3_B11.

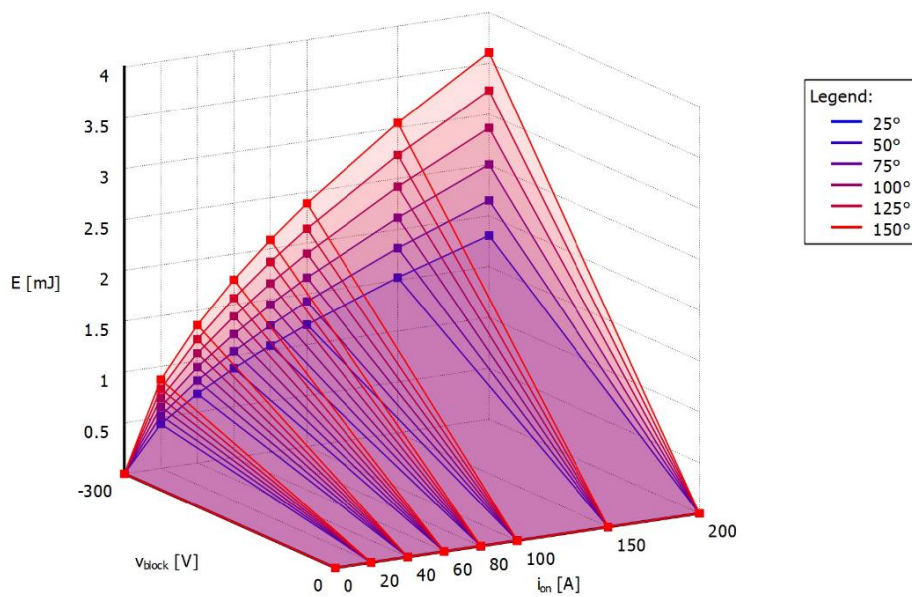


Figure 5.43 : Turn-off energy characteristic of clamping diode in F3L100R07W2E3_B11.

Table 5.13 : Cauer equivalent circuit parameters of clamping diodes in F3L100R07W2E3_B11.

Element	1	2	3	4
R (K/W)	0.106	0.2372	0.534	0.2217
C (J/K)	0.006093	0.02301	0.08032	0.7454

After the thermal model of the NPC module was prepared, the modeling of the FB module was started. The conduction losses of the MOSFETs in the FB module are given in Figure 5.44.

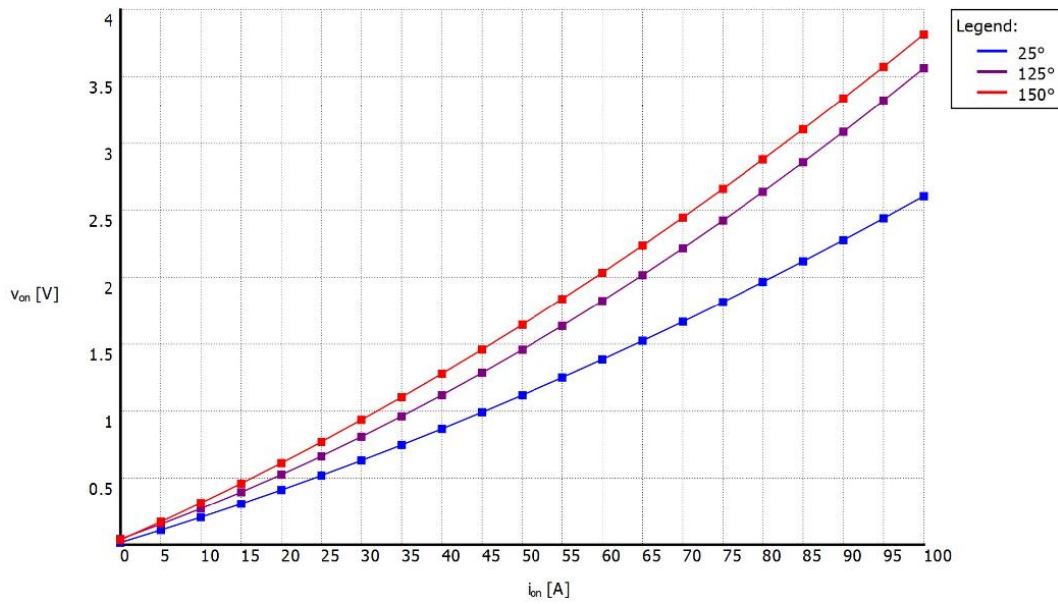


Figure 5.44 : Conduction loss characteristic of MOSFETs in F4-23MR12W1M1_B76.

Since the switching losses of SiC semiconductors are very low, the turn-on and turn-off energies of MOSFETs are modeled only at 150°C. Figure 5.45 (a) shows the turn-on and Figure 5.45 (b) shows the turn-off energies. The parameters of the Cauer thermal equivalent circuit of MOSFETs are as shown in Table 5.14.

Finally, in the FB module, the losses of the body diodes will be modeled. Only conduction losses will be used in this modeling. Figure 5.46 shows the conduction losses of the body diodes in the FB module, the parameters of the Cauer thermal equivalent circuit is same as the MOSFETs.

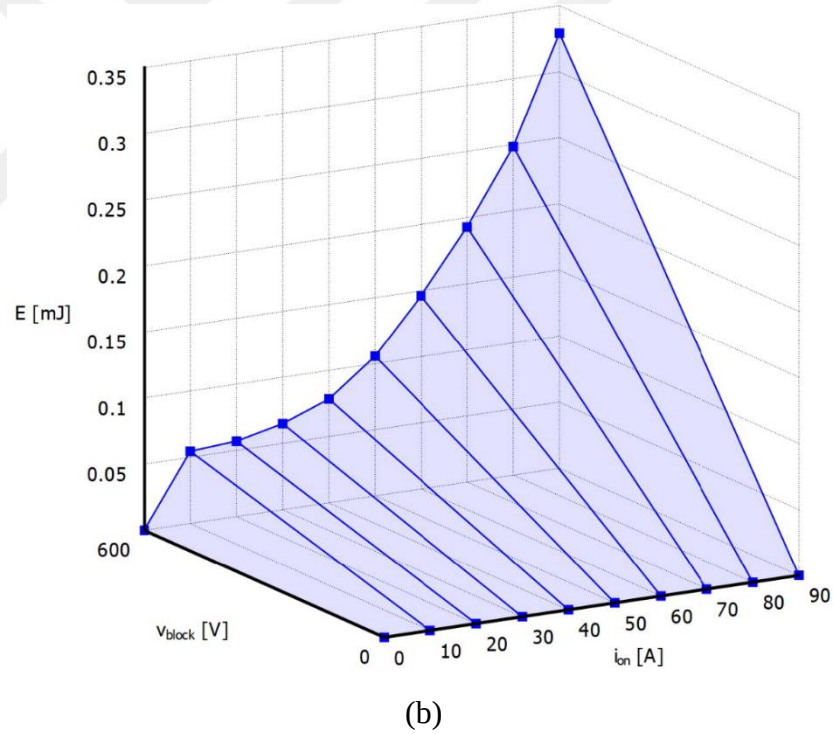
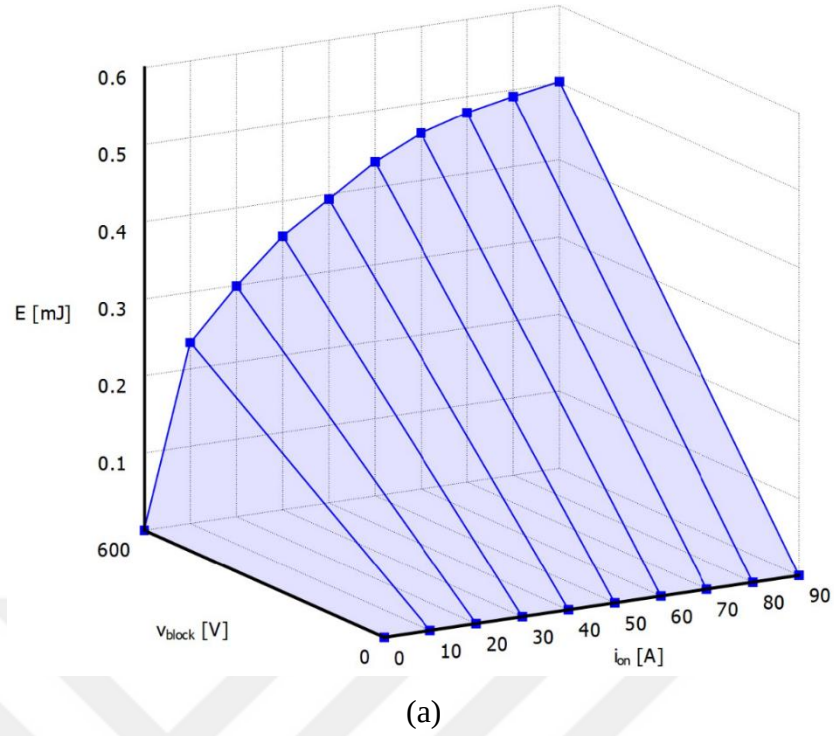


Figure 5.45 : Turn-on energy (a), and turn-off energy (b) characteristics of MOSFETs in F4-23MR12W1M1_B76.

Table 5.14 : Cauer equivalent circuit parameters of MOSFETs in F4-23MR12W1M1_B76.

Element	1	2	3	4
R (K/W)	0.06947	0.1978	0.2667	0.3661
C (J/K)	0.01187	0.02762	0.08891	0.2611

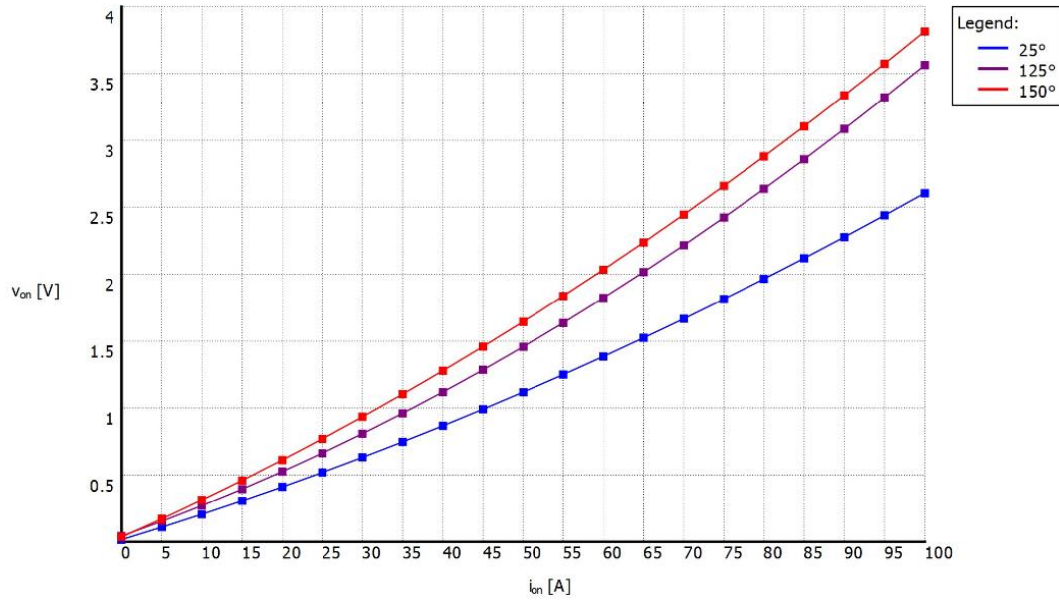


Figure 5.46 : Conduction loss characteristic of body diodes in F4-23MR12W1M1_B76.

Lastly, the SiC diode module at the output of the DC/DC converter will be modeled. Since the switching loss of the module is very low, only conduction losses are modeled and given in Figure 5.47. Also, the parameters of the Cauer thermal equivalent circuit of the diodes are given in Table 5.15.

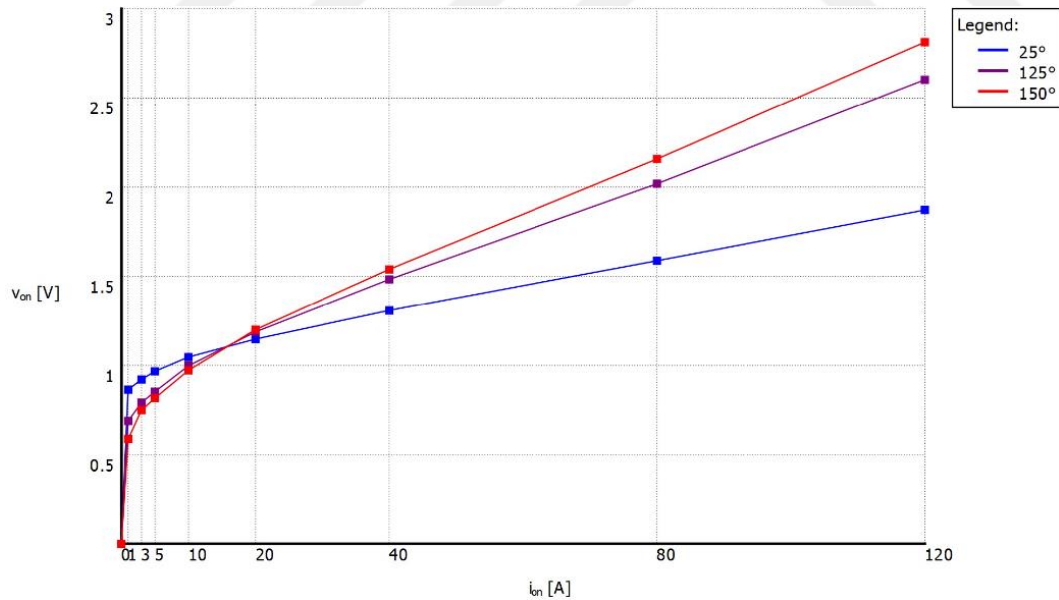


Figure 5.47 : Conduction loss characteristic of diodes in DDB2U60N12W1RF_B11.

Table 5.15 : Cauer equivalent circuit parameters of diodes in DDB2U60N12W1RF_B11.

Element	1	2	3
R (K/W)	0.07596	0.2391	0.3979
C (J/K)	0.01255	0.05347	0.2514

Thermal modeling ended at this stage. The required parameters of all semiconductors have been modeled. These parameters will be taken into consideration in the design of the cooling system.

5.4.1.2. Magnetic modelling

For magnetic modeling, it is necessary to determine the physical parameters and saturation characteristics of the core to be used. In the PLECS package program, saturation characteristics can be defined as two different functions. These functions are as in equations 5.42 and 5.43.

$$B = \frac{2}{\pi} B_{\text{sat}} \tan^{-1} \left(\frac{\pi H}{2a} \right) + \mu_{\text{sat}} H \quad (5.42)$$

$$B = B_{\text{sat}} \left(\coth^{-1} \left(\frac{3H}{a} \right) - \frac{a}{3H} \right) + \mu_{\text{sat}} H \quad (5.43)$$

The values of B_{sat} and μ_{sat} given in the equations are the parameters to be used in the model for the saturation characteristic and parameter a is given in equation 5.44. In order to find out which function is more appropriate; a curve fitting script was written in Matlab. The model parameters of all inductances are given in Table 5.16.

$$a = \frac{B_{\text{sat}}}{\mu_{\text{unsat}} - \mu_{\text{sat}}} \quad (5.44)$$

Table 5.16 : Magnetic modelling parameters of magnetic components.

Parameter	L_i	L_o	L_t	L_{FB}
Number of turns	23	46	27	23
Fitting function	atan	atan	coth	atan
A_c (cm ²)	4.58	4.58	1.07	4.58
l_e (cm)	12.5	12.5	9.85	12.5
$\mu_{\text{r-unsat}}$	40	40	26	40
$\mu_{\text{r-sat}}$	0	0	1	0
B_{sat} (T)	1.125	0.893	1.027	1.097

The parameters required in magnetic modeling are as given in the Table 5.16. Modeling was done for each magnetic material. The magnetic modeling of the transformer was done directly with the parameters shared in the datasheet. This is because the saturation characteristics of ferrite cores are more linear.

5.4.1.3.Simulation results

All thermal and magnetic characteristics are modeled and the generated model is as shown in Figure 5.48. 380 V_{L-L} fed system is rectified with NPC rectifier after passing through the grid connection filter. The obtained 750 V DC link is applied to the battery at the desired level with the help of two parallel PSFB-ZVT circuits.

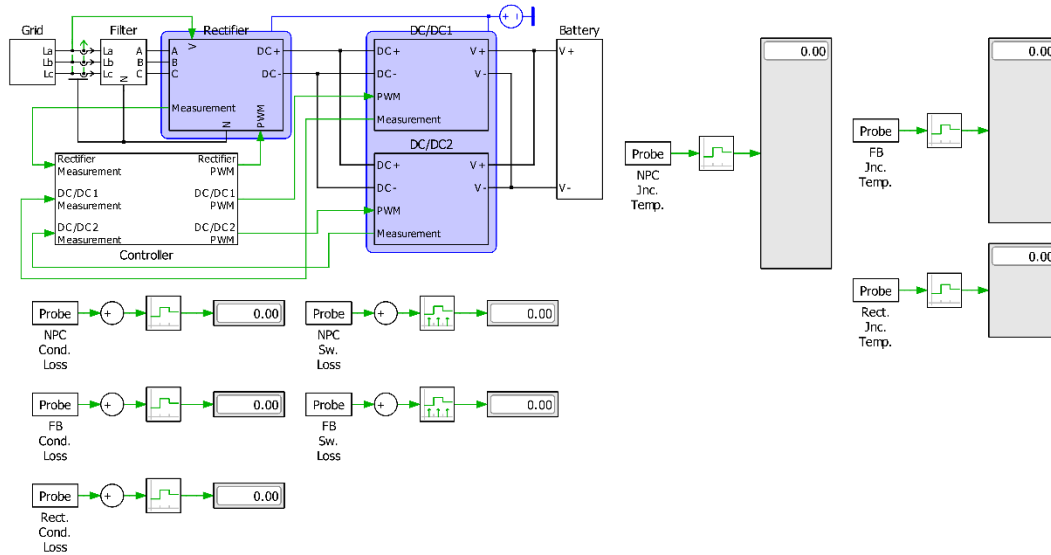


Figure 5.48 : Full model of the system.

When the prepared model was run with a 22 kW load for 700 V battery voltage, the grid voltage and current were as shown in Figure 5.49. The current drawn from the grid has an RMS value of 34.4 A. THDi is 3.1%. The power drawn from the grid is 22.6 kW.

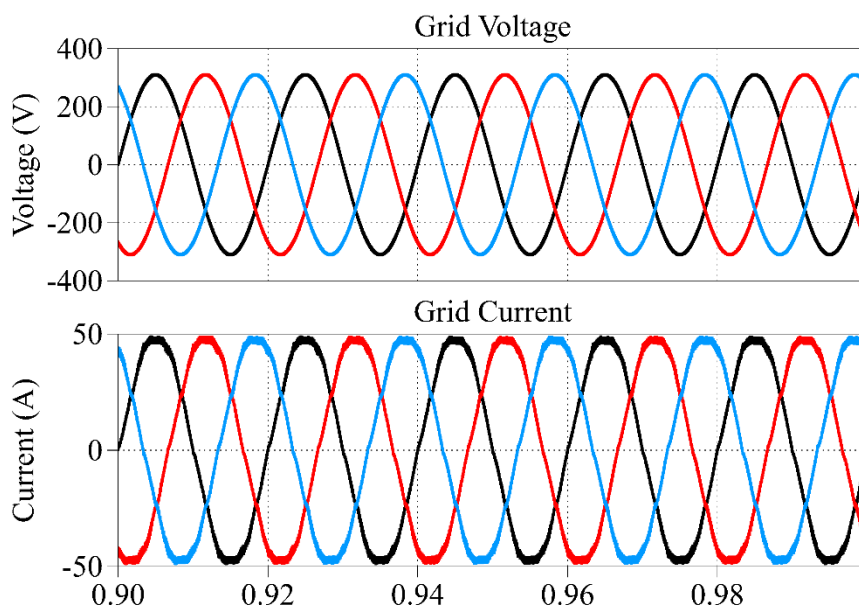


Figure 5.49 : Grid voltage and current.

The output voltage and current in the same condition are given in Figure 5.50. The output voltage is between 693 V and 695 V with an average value of 693 V. The output current is 31.12 A. The output power in this case is 21.55 kW. The efficiency of the system is 95.4%.

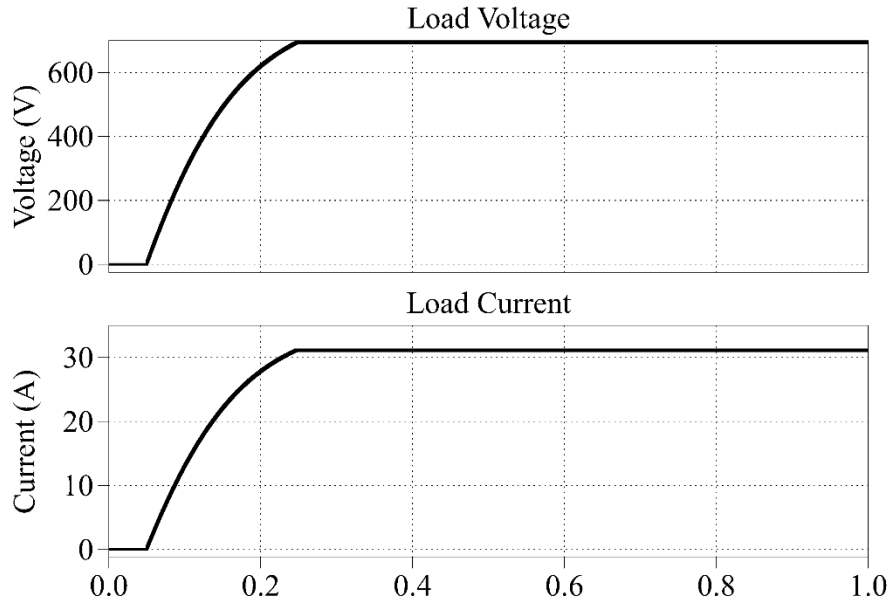


Figure 5.50 : Load voltage and current.

The simulations were run at a constant heatsink temperature of 80°C. The simulated losses are given in Table 5.17.

Table 5.17 : Losses of the system.

Circuit	Switch	Conduction Losses (W)	Switching Losses (W)	Loss Per Module (W)	Total Loss (W)
NPC Rectifier	Outer IGBTs (Q ₁ & Q ₄)	0.01	0.29	140.74	422.22
	Inner IGBTs (Q ₂ & Q ₃)	6.2	20.06		
	Outer Body Diodes (D ₁ & D ₄)	11.5	13.54		
	Inner Body Diodes (D ₂ & D ₃)	11.69	0.05		
	Clamping Diodes (D ₅ & D ₆)	6.84	0.15		
PSFB DC/DC Converter	MOSFETs (Q ₁ , Q ₂ , Q ₃ & Q ₄)	10.01	3.67	54.72	109.44
	Rectifier Diodes (D ₁ , D ₂ , D ₃ & D ₄)	9.49	0	37.96	75.92

The junction temperatures of NPC rectifier obtained from the simulation results are given in Table 5.18, and the junction temperatures of DC/DC converter are given in Table 5.19.

Table 5.18 : Rectifier maximum junction temperatures.

Device	Maximum Junction Temperature (°C)
Outer IGBTs (Q ₁ & Q ₄)	112.04
Inner IGBTs (Q ₂ & Q ₃)	96.99
Outer Body Diodes (D ₁ & D ₄)	80.34
Inner Body Diodes (D ₂ & D ₃)	80.02
Clamping Diodes (D ₅ & D ₆)	97.3

Table 5.19 : DC/DC converter maximum junction temperatures.

Device	Maximum Junction Temperature (°C)
MOSFETs (Q ₁ , Q ₂ , Q ₃ & Q ₄)	94.95
Rectifier (D ₁ , D ₂ , D ₃ & D ₄)	86.63

According to these results, the system can operate without any problem when the highest heatsink temperature is 80°C. When designing the cooling system, a design will be made so that the highest heatsink temperature stays below 80°C.

5.4.2. Printed circuit board design

In the system to be designed, there are grid connection filter PCB, protection PCB, controller PCB, power circuit PCB and gate driver PCBs. The protection PCB contains fuses and relays to be used against high-current protection. The grid connection filter contains capacitors, inductances, and resistors. Since there are no special considerations in the design of these PCBs, their design is not mentioned in this thesis. The controller PCB is also outside the scope of this thesis.

5.4.2.1. Power circuit printed circuit board design

The energy from the protection PCB and the grid connection PCB goes to the power circuit PCB. All rectifier and DC/DC converter circuits are located on this PCB. The transformers in the DC/DC converters are located outside the PCB. Figure 5.51 shows the schematic of the rectifier and the mutual DC-link. At the left side, the gate resistors and protection diodes can be seen. At the top right, the mutual DC-link is drawn. The gate drivers are shown in the middle of the bottom.

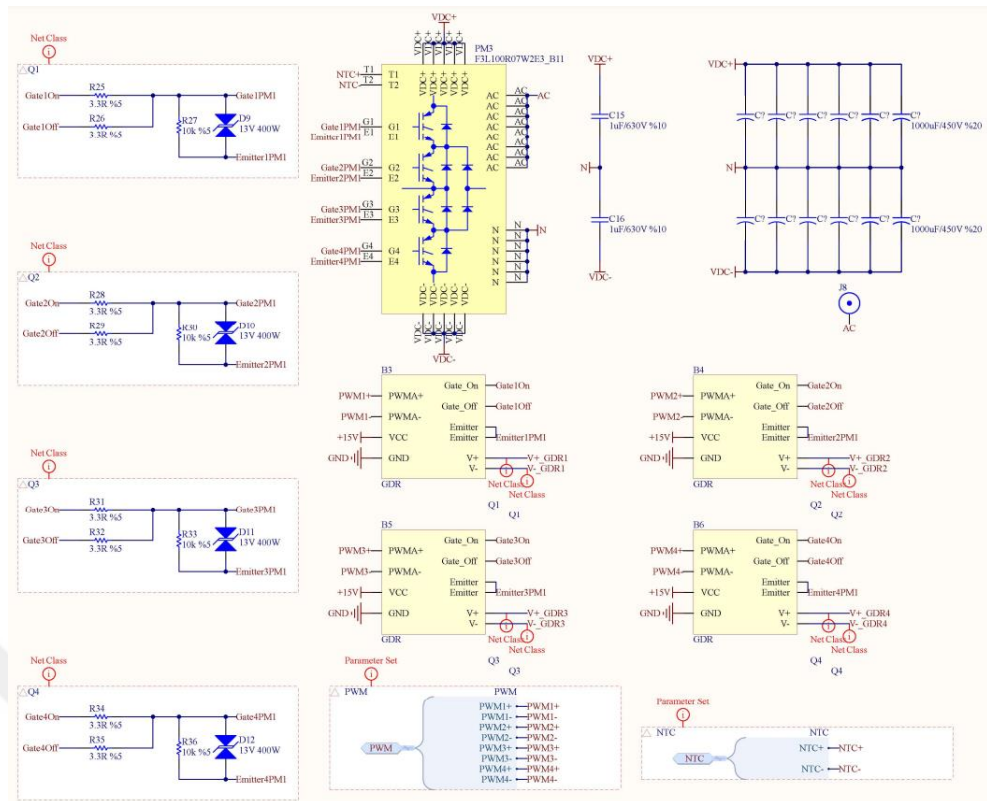


Figure 5.51 : The schematic of rectifier and mutual DC-link.

After the mutual DC-link one cell of the full-bridge is given in Figure 5.52. The transformer is located outside of the PCB and the terminals shown in the Figure 5.52. At the top left the snubber capacitors can be seen. Bottom of the snubber capacitors, the gate drive PCB is given. At the right side the gate resistors and protection diodes can be seen. At the output of the full-bridge module, the inductor and capacitors are located. After the capacitors, the transformer terminals can be seen.

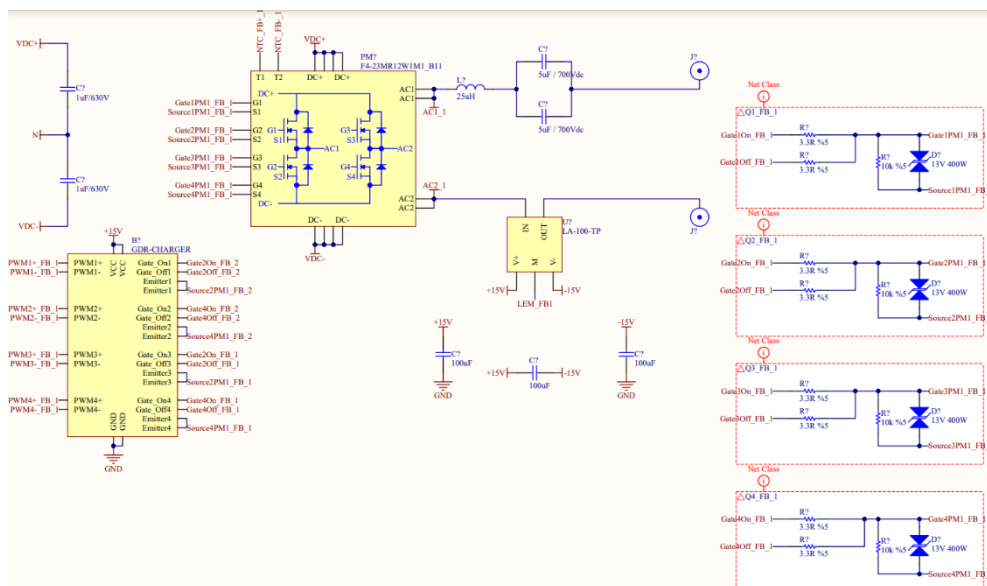


Figure 5.52 : The schematic of one cell of the full-bridge modules.

The secondary side of the transformer is connected to full wave bridge rectifier via terminals. After the full wave bridge rectifier module, the output inductor can be seen. The output current is measured via the current sensor located after the inductor. Also, the isolated output voltage measurement circuit is shown at the right side. The Figure 5.53 shows the schematic of one cell of the output stages.

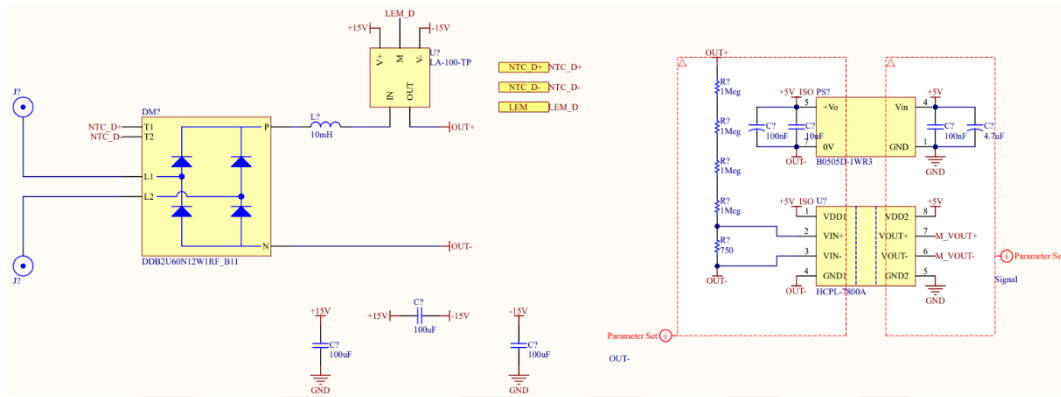


Figure 5.53 : The schematic of one cell of the output stages.

The power is transferred to the transformer through the terminals, and from the secondary side, it is transferred to the PCB through the terminals. Figure 5.54 shows the power PCB. That PCB includes the NPC rectifier circuit, PSFB circuit, mutual and output DC-links. Also, the current sensors, isolated output voltage measurement circuit are located. The different parts of the PCB are given with numbers. The number 1 shows the gate drivers of Si IGBT modules. The number 2 shows the Si IGBT NPC rectifiers. The number 3 shows the mutual DC-link capacitors and snubber capacitors. The number 4 shows the PSFB circuit. At the number 5, the gate drivers of SiC MOSFET modules are given.

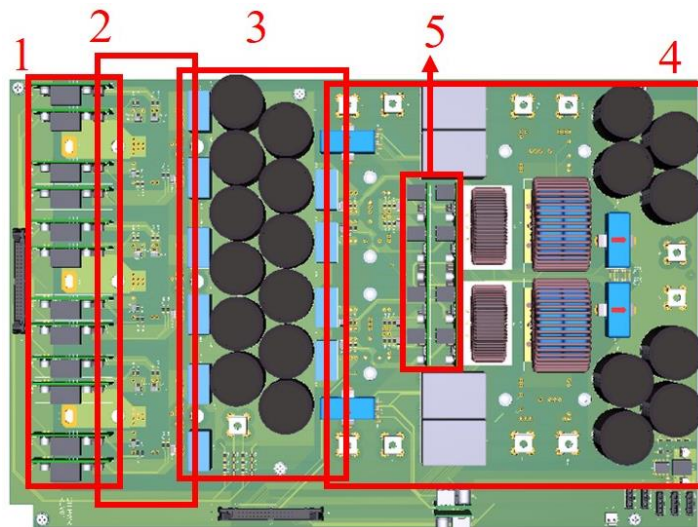


Figure 5.54 : Power circuit PCB.

In the design of this PCB, special attention was paid to the thickness of the high-current tracks. In addition, the gate signals are routed away from the high-current paths to avoid noise. A snubber is used to prevent stray inductance due to its high frequency. An isolated measurement structure is designed so that switching noise does not affect the measurement of the output voltage.

5.4.2.2.Rectifier gate driver printed circuit board design

Si IGBT gate drivers and SiC MOSFET gate drivers have same schematic design. The difference between these two is the isolated DC/DC converter. The gate driver of the Si IGBT has output voltages of -8 V and 15 V. The gate driver of the SiC MOSFET has output voltages of -5 V and 15 V. Each gate in the rectifier has its own gate driver PCB. In this way, it is easier to draw the paths on the power circuit PCB. In Figure 5.55 the schematic design of the gate driver circuits can be seen. At the top left, the bypass capacitors of the isolated DC/DC converter can be seen. Top middle is the location of the isolated DC/DC converter. At the top right, the output and bypass capacitors of the output of the isolated DC/DC converter can be seen. At the bottom middle, the gate drive circuit is located. As can be seen in Figure 5.55, the indicator light emitting diodes are located.

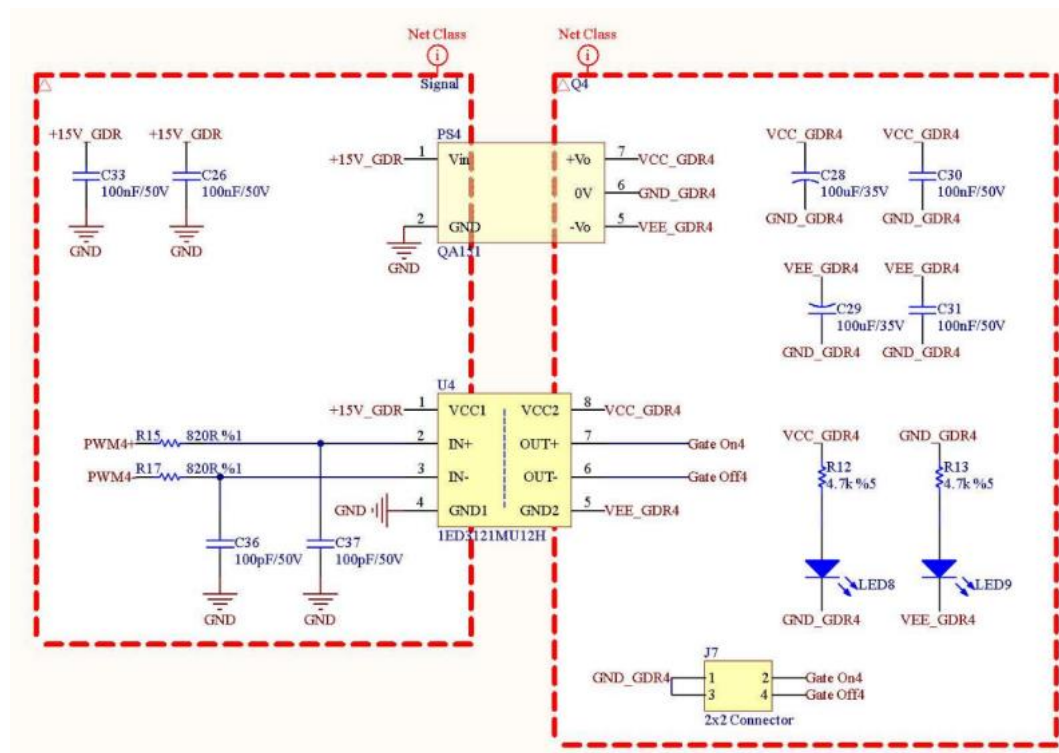


Figure 5.55 : The schematic design of the gate driver circuits.

After the schematic design of the gate driver, one of the points to be considered on the PCB is the isolation between the signals going to the power circuit PCB and the signals coming from the controller PCB. This was taken into consideration in the design of the PCB shown in Figure 5.56. In addition, the impedance between the gate signals is as equal as possible to minimize the delay.

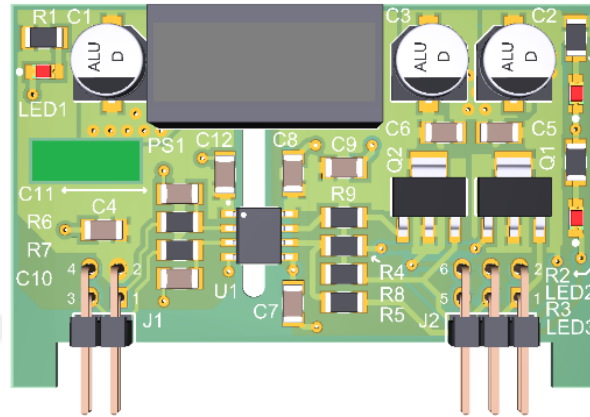


Figure 5.56 : Rectifier gate driver PCB.

5.4.2.3.DC/DC converter gate driver printed circuit board design

The DC/DC converter gate driver has a same schematic structure of the rectifier gate driver given in Figure 5.55. The issues mentioned for the gate driver of the rectifier are also valid for this PCB shown in Figure 5.57. The only difference here is that the gate signals in each module are on a single PCB. Since the frequency in this part is higher, by-pass capacitors have been added in suitable places to reduce the noise. In this way, high-frequency noise can be filtered.

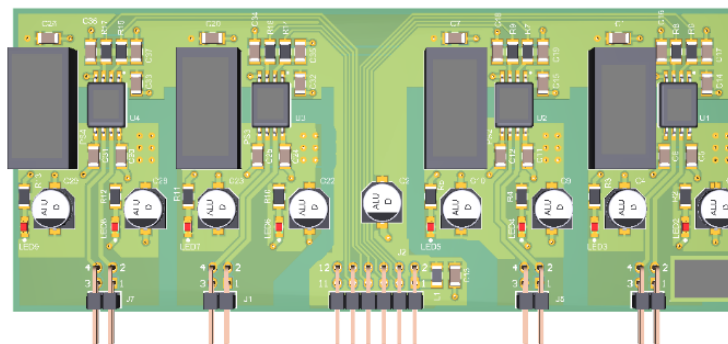


Figure 5.57 : FB gate driver PCB.

5.4.3.Cooling system design

As a result of the simulations, the losses of each module in the system were calculated. In this section, using these loss values, a design will be realized in which the heatsink temperature will not exceed 80°C.

5.4.3.1.Heatsink design

The R-Tools web-based program was used for heatsink sizing. Accordingly, the loss of each module is defined according to the layout. The obtained results, when the targeted maximum heatsink size, maximum allowable temperature, target pressure drop and flow rate are entered into the program, are shown in the Figure 5.58. According to this, the heatsink size in the selected configuration is shown in Table 5.20. The maximum allowable pressure drop for the fan block is 35.22 Pa, and the flow rate in this case is 4.3 m³/min.

Table 5.20 : Size of heatsink.

Parameter	Dimension (mm)
Weight	262
Height	77.9
Length	350

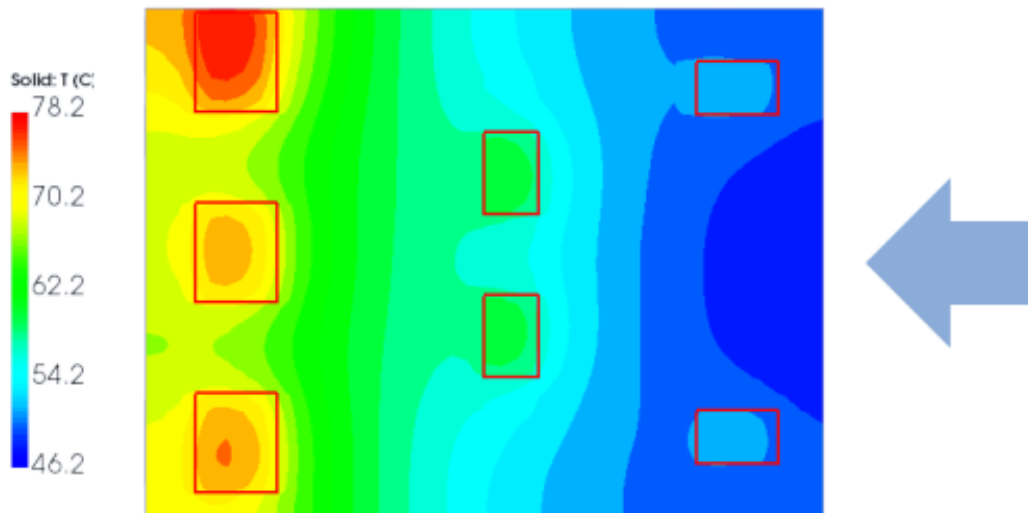


Figure 5.58 : Temperature map of heatsink.

5.4.3.2.Fan block design

The flow rate in the fan block targeted for design is 4.3 m³/min, and the maximum allowable pressure drop is 35.22 Pa. Accordingly, it is suitable to use 4 of the 9G0624P4S001 coded fans with dimensions of 60x60x24 mm. Figure 5.59 shows the characteristics of the selected fan.

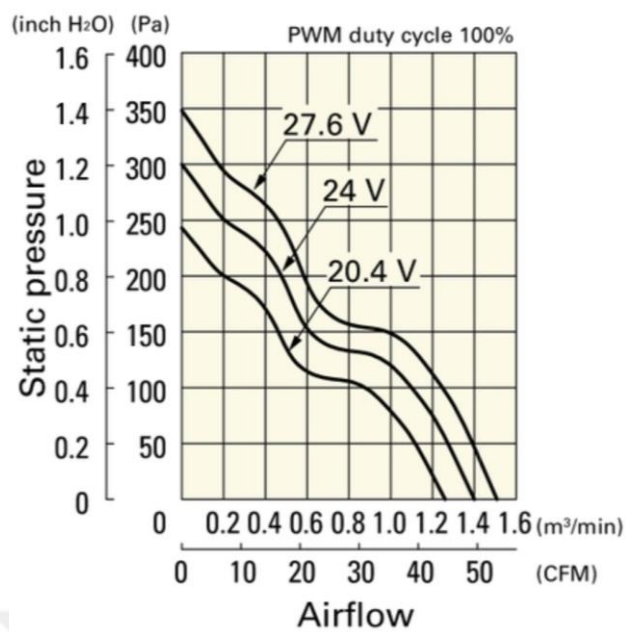


Figure 5.59 : Characteristic of 9G0624P4S001 [78].

6.EXPERIMENTAL STUDIES AND RESULTS

After the design and simulation stage ended, the experimental studies are performed for validation of the design.

6.1.Experimental Setup

The schematic of experimental setup is given in Figure 6.1 and the experimental setup is given in Figure 6.2. To measure the voltage and current drawn by the grid, PW3390 power analyzer of Hioki is used. For measuring the output voltage, Fluke 114 digital multimeter is used. The waveforms are taken with oscilloscope model name of RT06 and manufactured by Rohde & Schwarz. For loading the system, pure resistive load bank is used. The load bank has 40 resistances. Each of them is $25\ \Omega$ and maximum power capability of 2.5 kW. With parallel and serial connections, needed resistance value can be obtained. The bottom view of the EV DC fast charger is given in Figure 6.3.

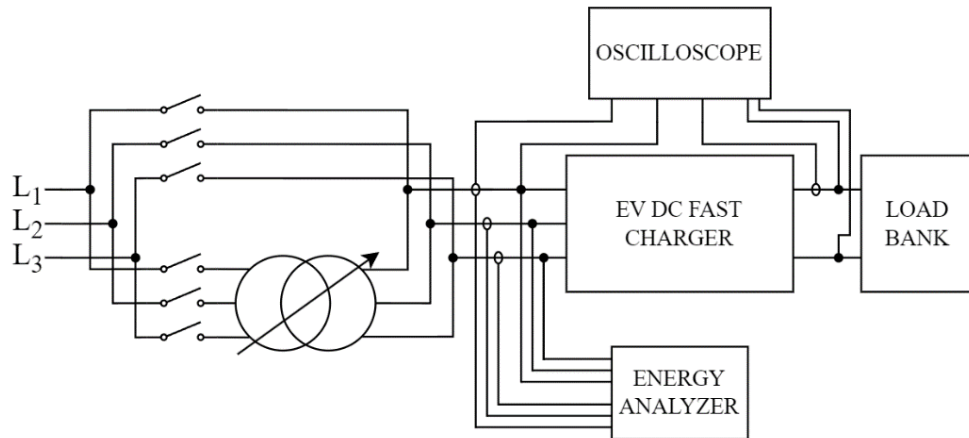


Figure 6.1 : Schematic of experimental setup.

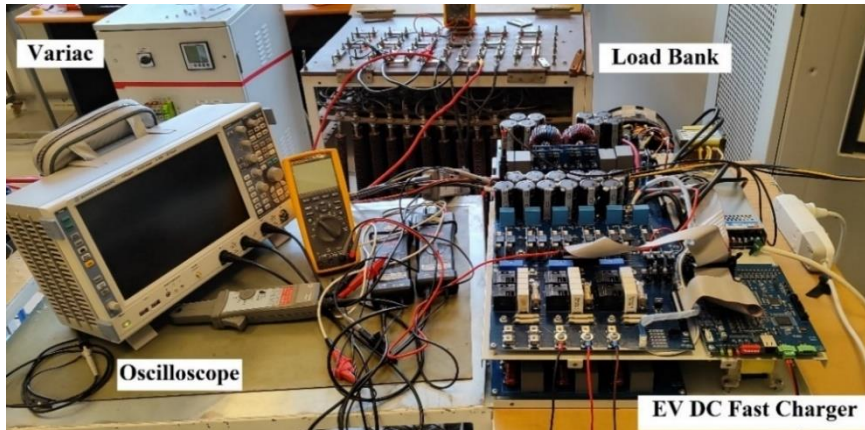


Figure 6.2 : Experimental setup.

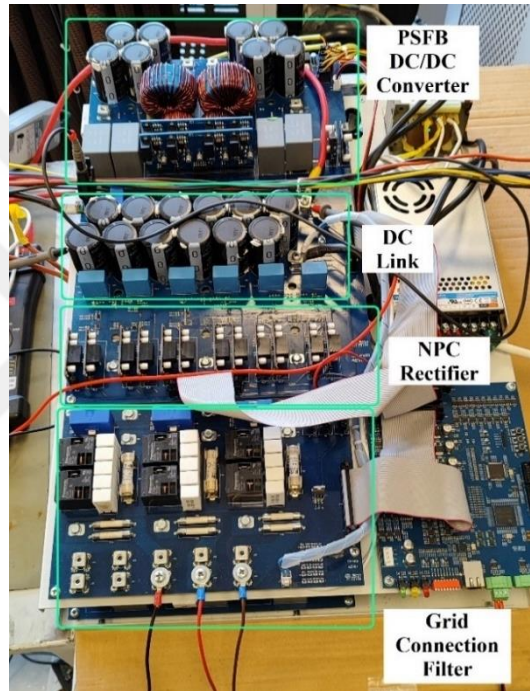


Figure 6.3 : Top view of EV DC fast charger.

6.2.Experimental Results

After the experimental setup is installed, the experiments are started. First of all, system is started without load, and no-load operation results are taken for different output voltages of 500 V, 600 V, 700 V and 800 V. The current measurements show the 10% of the actual values. The reason for that is the multiplier of the oscilloscope cannot set for actual values. Figure 6.4 shows the no-load grid voltage, and current drawn by grid and output voltage when the V_{ref} is given 500 V. As seen in Figure 6.4, the input voltage is equal to 217.41 V and the current drawn from the grid is equal to 2.74 A. According to these values, the no-load power is equal to 1.79 kW. Also, the output voltage is equal to 499.15 V.

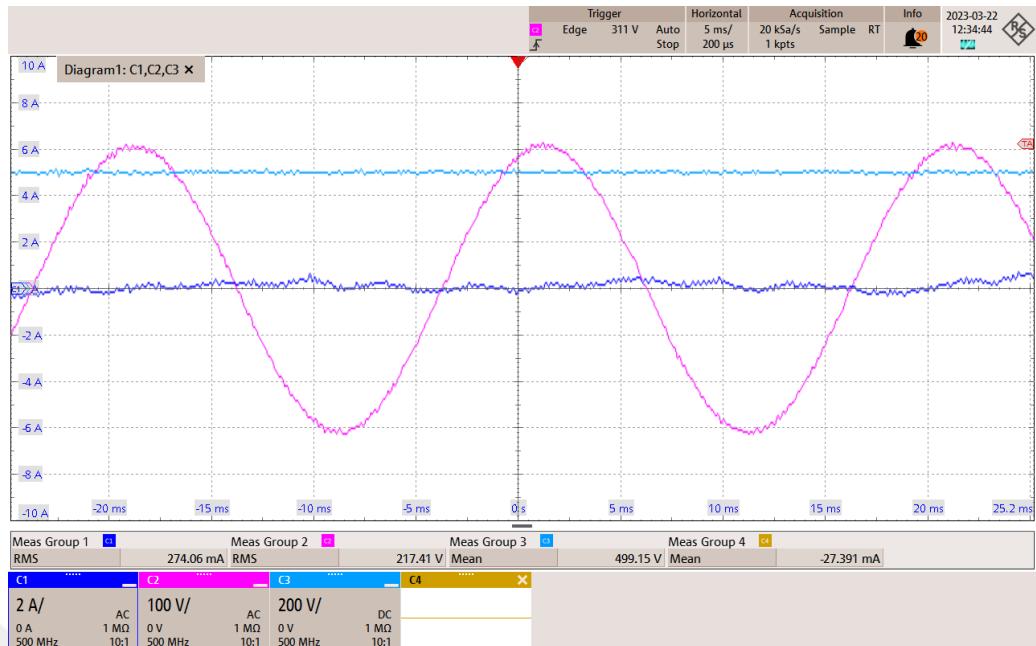


Figure 6.4 : Waveforms of grid voltage and current drawn by grid and output voltage at no-load operation when the V_{ref} is given 500 V.

Figure 6.5 shows the no-load grid voltage, and current drawn by grid and output voltage when the V_{ref} is given 600 V. As seen in Figure 6.5, the input voltage is equal to 217.57 V and the current drawn from the grid is equal to 2.87 A. According to these values, the no-load power is equal to 1.87 kW. Also, the output voltage is equal to 595.88 V.

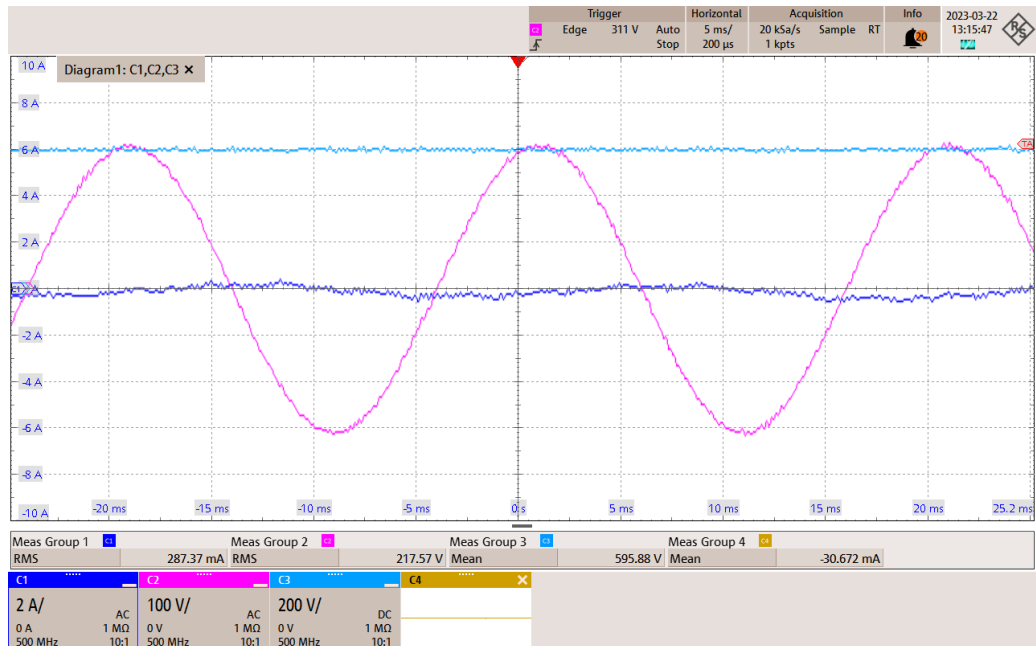


Figure 6.5 : Waveforms of grid voltage and current drawn by grid and output voltage at no-load operation when the V_{ref} is given 600 V.

Figure 6.6 shows the no-load operation for 700 V of V_{ref} . The grid voltage is equal to 216.5 V and the current drawn from the grid is 2.33 A. According to these values, the no-load power is equal to 1.51 kW. Also, the output voltage is equal to 695.68 V.

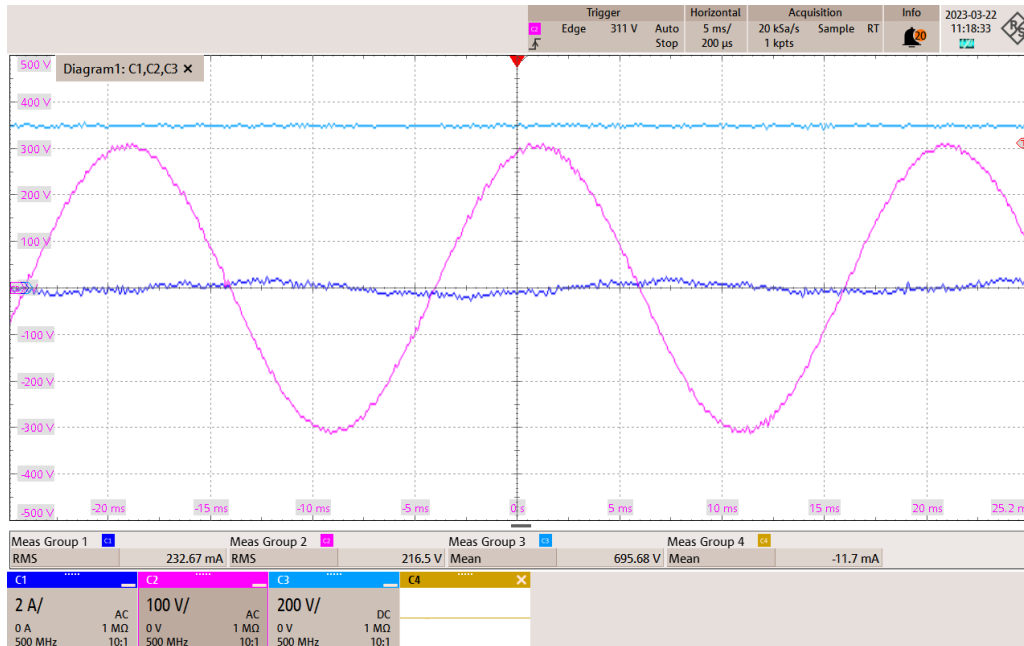


Figure 6.6 : Waveforms of grid voltage and current drawn by grid and output voltage at no-load operation when the V_{ref} is given 700 V.

Figure 6.7 shows the no-load operation for 700 V of V_{ref} . The grid voltage is equal to 217.93 V and the current drawn from the grid is 2.24 A. According to these values, the no-load power is equal to 1.46 kW. Also, the output voltage is equal to 796.75 V.

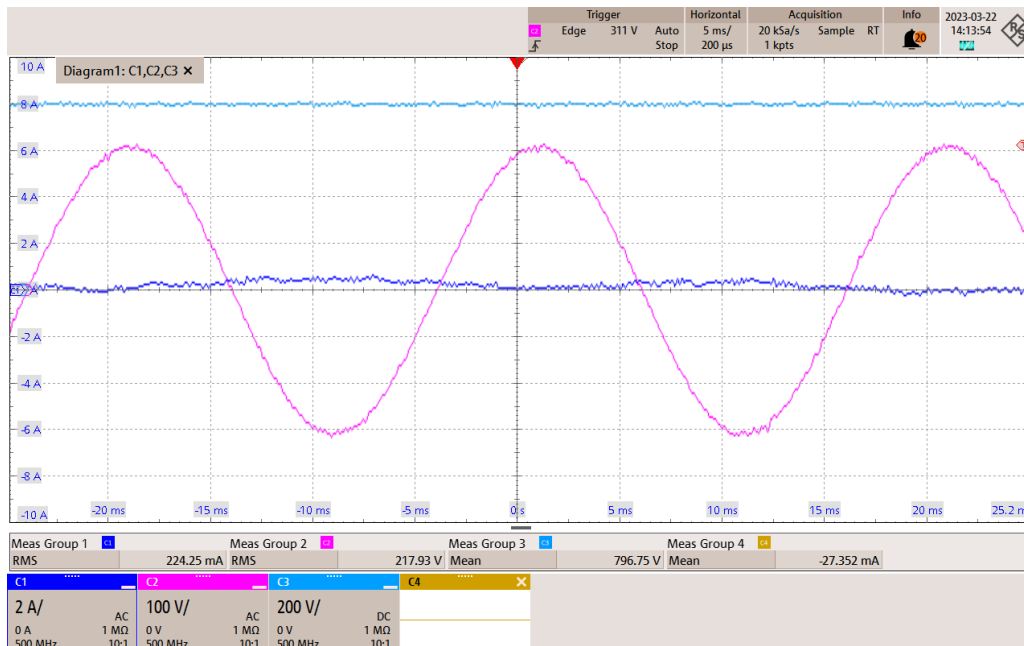


Figure 6.7 : Waveforms of grid voltage and current drawn by grid and output voltage at no-load operation when the V_{ref} is given 800 V.

As seen in the Figure 6.4-6.7, the output voltage of the system can be stabilized at the desired values. No-load operation currents drawn from the grid are between 2.24 A and 2.87 A. No-load operation powers drawn from the grid are between 1.46 kW and 1.87 kW.

After the no-load results, system is worked under different load conditions. At the tests, the V_{ref} is selected as 500 V, 600 V, 700 V and 800 V. Also, the results are taken for the 25%, 50%, 75% and 100% of rated power. The input voltages, currents drawn from the grid, output voltages, output currents, input powers, output powers and efficiencies can be seen in Table 6.1 for the V_{ref} is equal to 500 V.

Table 6.1 : Test results for V_{ref} is equal to 500 V.

Load Condition (%)	Input Voltage (V)	Input Current (A)	Output Voltage (V)	Output Current (A)	Input Power (kW)	Output Power (kW)	Efficiency (%)
25%	218.2	8.87	501.86	10.33	5.59	5.18	92.77%
50%	218.7	17.35	501.59	20.93	11.18	10.5	93.89%
75%	218.6	22.7	500.02	27.85	14.61	13.92	95.31%
100%	218.7	33.84	499.46	41.79	21.76	20.87	95.91%

Figure 6.8 shows the full-load operation for 500 V of V_{ref} . The grid voltage is equal to 218.68 V and the current drawn from the grid is 33.83 A.

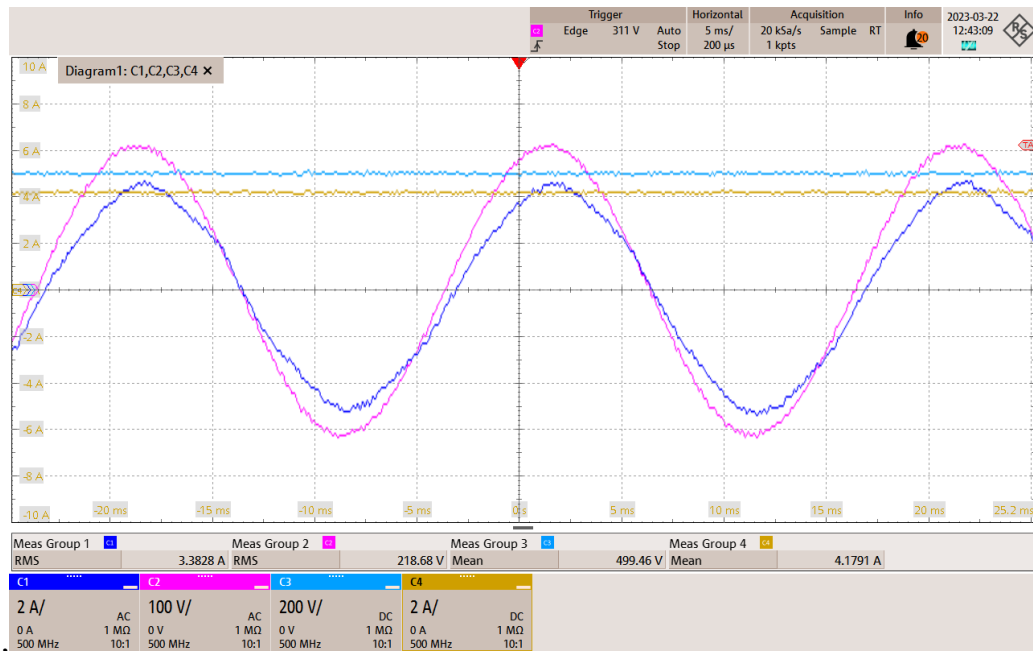


Figure 6.8 : Waveforms of grid voltage and current drawn by grid, output voltage and current at full-load operation when the V_{ref} is given 500 V.

The input voltages, currents drawn from the grid, output voltages, output currents, input powers, output powers and efficiencies can be seen in Table 6.2 for the V_{ref} is equal to 600 V. Figure 6.9 shows the full-load operation for same working conditions. The grid voltage is equal to 217.71 V and the current drawn from the grid is 35.21 A.

Table 6.2 : Test results for V_{ref} is equal to 600 V.

Load Condition (%)	Input Voltage (V)	Input Current (A)	Output Voltage (V)	Output Current (A)	Input Power (kW)	Output Power (kW)	Efficiency (%)
25%	217.3	9.38	595.87	8.95	5.66	5.33	94.12%
50%	217.4	18.15	596.21	18.28	11.38	10.9	95.74%
75%	217.3	23.81	595.75	24.32	15.04	14.49	96.32%
100%	217.3	35.22	596.35	36.78	22.53	21.93	97.34%

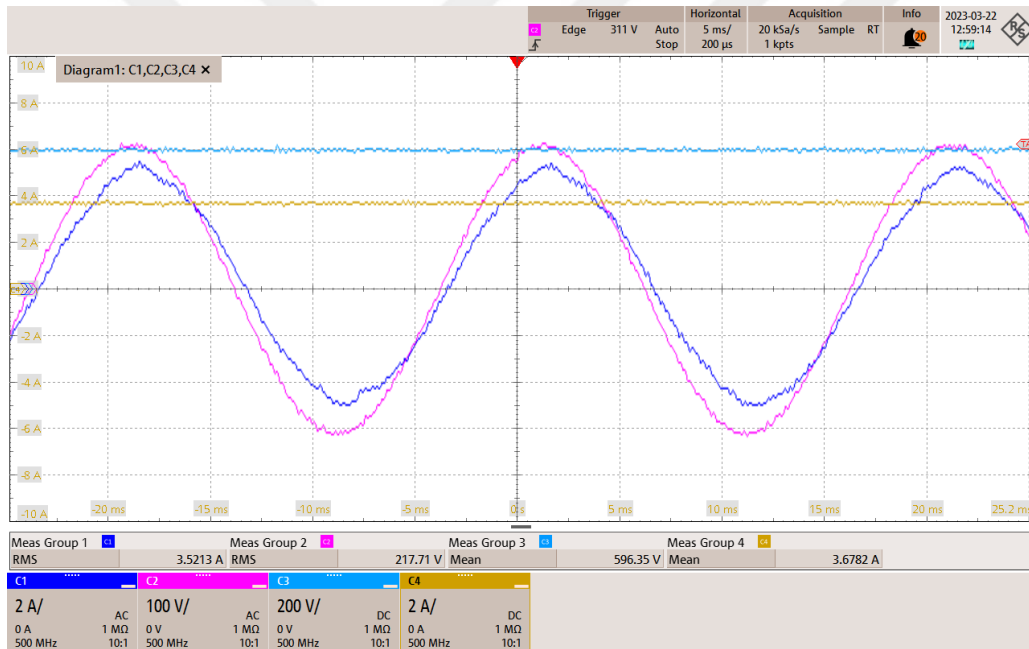
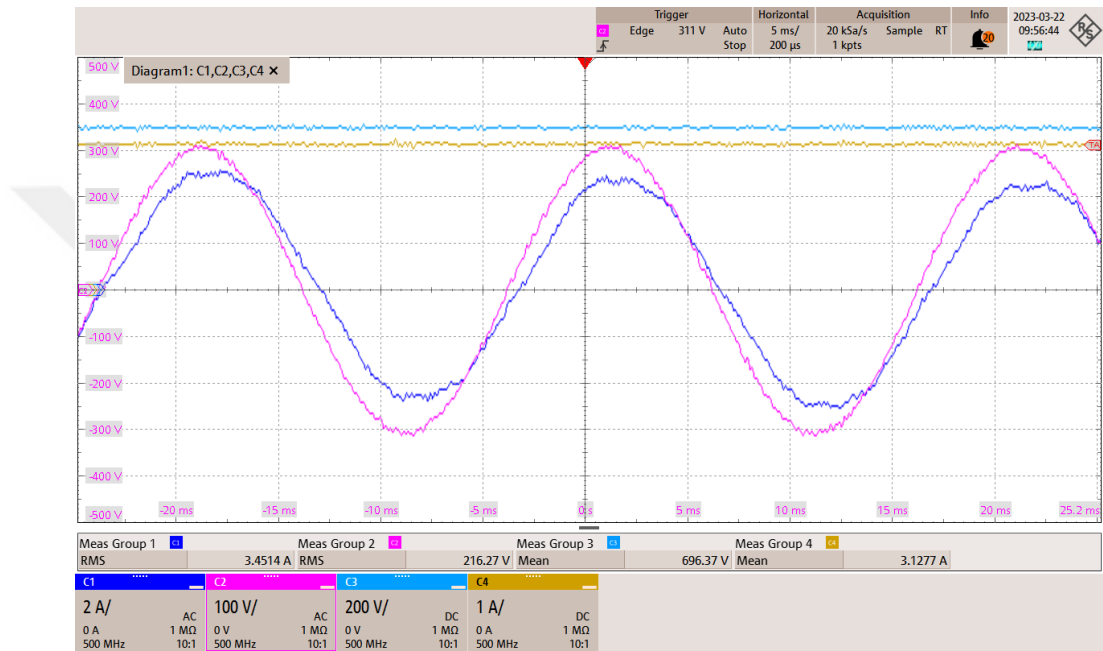


Figure 6.9 : Waveforms of grid voltage and current drawn by grid, output voltage and current at full-load operation when the V_{ref} is given 600 V.

The input voltages, currents drawn from the grid, output voltages, output currents, input powers, output powers and efficiencies can be seen in Table 6.3 for the V_{ref} is equal to 700 V. Figure 6.10 shows the full-load operation for same working conditions. The grid voltage is equal to 216.27 V and the current drawn from the grid is 34.51 A.

Table 6.3 : Test results for V_{ref} is equal to 700 V.

Load Condition (%)	Input Voltage (V)	Input Current (A)	Output Voltage (V)	Output Current (A)	Input Power (kW)	Output Power (kW)	Efficiency (%)
25%	215.9	9.61	696.15	7.8	5.78	5.43	93.99%
50%	216	18.05	696.23	15.65	11.38	10.9	95.78%
75%	217.3	23.42	696.34	20.84	15.05	14.5	96.44%
100%	216.2	35.02	696.37	31.28	22.35	21.78	97.44%

**Figure 6.10 :** Waveforms of grid voltage and current drawn by grid, output voltage and current at full-load operation when the V_{ref} is given 700 V.

The input voltages, currents drawn from the grid, output voltages, output currents, input powers, output powers and efficiencies can be seen in Table 6.4 for the V_{ref} is equal to 800 V. Figure 6.11 shows the full-load operation for same working conditions. The grid voltage is equal to 216.91 V and the current drawn from the grid is 31.3 A.

Table 6.4 : Test results for V_{ref} is equal to 800 V.

Load Condition (%)	Input Voltage (V)	Input Current (A)	Output Voltage (V)	Output Current (A)	Input Power (kW)	Output Power (kW)	Efficiency (%)
25%	218.2	9.27	796.51	6.61	5.59	5.26	94.13%
50%	217.6	18.29	796.8	13.62	11.33	10.85	95.82%
75%	217.7	23.92	796.52	18.36	15.11	14.62	96.8%
100%	217.2	32.73	795.3	25.1	20.47	19.96	97.52%

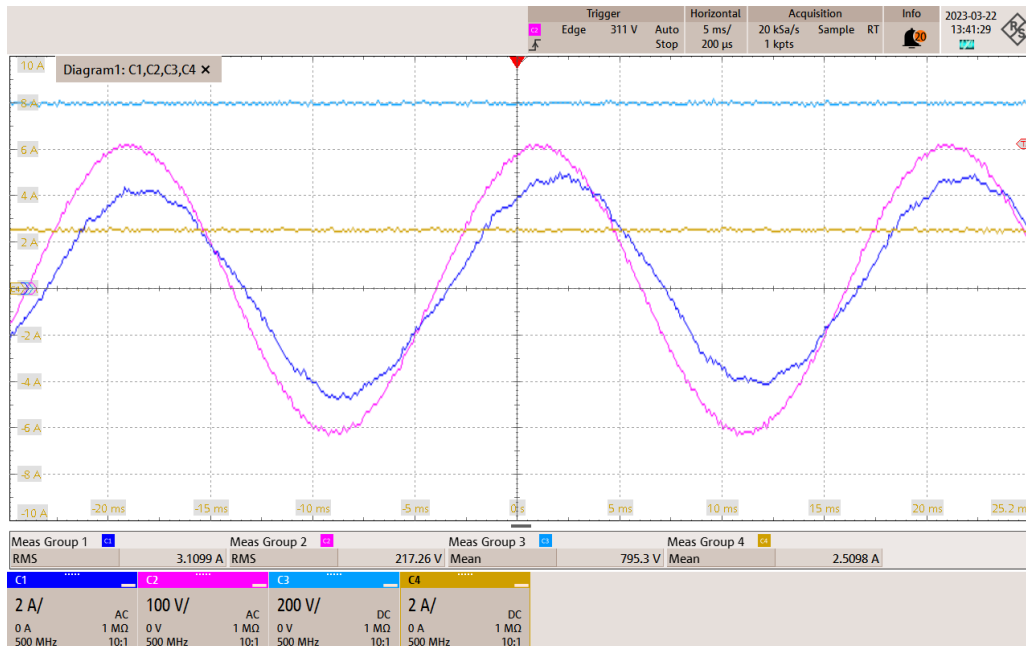


Figure 6.11 : Waveforms of grid voltage and current drawn by grid, output voltage and current at full-load operation when the V_{ref} is given 800 V.

The efficiency of the system according to loading percentage is given in Figure 6.12. based on this characteristic the efficiency is increased with the increased output voltage at full-load. But, when the system is in the lower loading, the lower output voltage values have higher efficiencies.

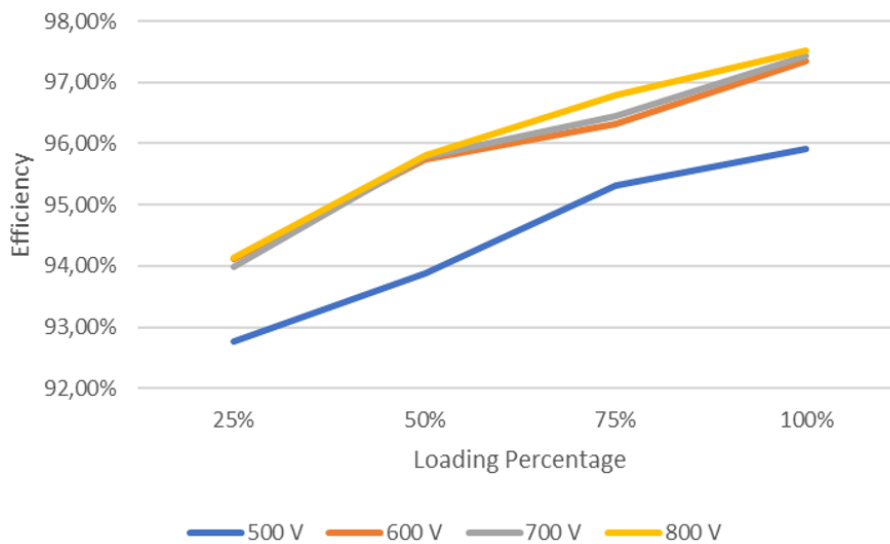


Figure 6.12 : Efficiency characteristics of system depend on the loading percentage.

As seen in the results, the efficiency is depended on the output voltage and power. The reason for that is some losses are not depended on the load condition. With higher current operations the losses are more increased comparing to higher voltages. The core and copper losses occur in the magnetic are increased with the current. The

conduction losses of SiC MOSFETs are depended on the square of current. At high currents the conduction losses are increased. The peak efficiency of the system is measured as 97.52% at the full-load condition with output voltage of 800 V. The dimensions of the designed system are 640 mm, 420 mm and 100 mm. the volume of the system is equal to 26.88 L. The power density of the system is equal to 0.82 kW/L.

In a similar study, a system with 5 kW of output power is designed. This system has a peak efficiency of 98.2%. But the designed system is not a fully fast charging system. The system has also slow charging output. The power density of the system is equal to 2.74 kW/L [10]. In the system designed for thesis has 0.82 kW/L of power density. The biggest reason of that difference is the power differences between the system.

According to performed simulation results, the system has a 95.4% efficiency when the output voltage is equal to 693 V and output power is equal to 21.55 kW. This simulation is performed for the constant 80°C heat sink temperature. After the experimental studies performed, the efficiency of the system is equal to 97.52% for the same conditions. The output voltage is equal to 696.37 V and the output power is equal to 21.78 kW. According to experimental results, it is seen that the system has higher efficiency. The reason of that is the heat sink temperature is selected as a constant value of 80°C, but in the experimental studies, the heat sink temperature is not equal to constant 80°C. There are points that have less than 80°C of heat sink temperature, and because of that the losses are less than the simulation results.

At the peak working point of the system, system has 795.3 V of output voltage with the output power of 19.96 kW according to experimental results when the desired output voltage is equal to 800 V. At this point the efficiency of the system is equal to 97.52%. Also, the peak efficiency point of the system is this working point. In a similar study, it is seen that the efficiency is lower when the output power is lower and the current is higher. The system, which is studied in this study, has 96.6% efficiency under the 50 kW load at 500 V output voltage, according to HiL test results [6].



7.CONCLUSION

7.1.Summary

The structures of various DC fast charging systems and the configurations used are examined in this thesis. The topologies and structures that can be used for each subsystem are then compared, and the EV DC fast charging system is designed in the topologies of the chosen structure. The design is for the one module that will be located in a modular charging station. A three-level neutral point clamped rectifier topology is chosen as the rectifier.

The switching frequency of the rectifier is chosen as 16 kHz and the switching frequency of DC/DC converter is chosen as 40 kHz since a low switching frequency would increase the transformer size. At the rectifier stage, the switching frequency is selected lower than the switching frequency of DC/DC converter. The reason for that is the selection of module with Si IGBTs. SiC MOSFETs are used to reduce switching and conduction losses, and the topology is modified for zero voltage switching. In the rectifier stage at the output of the phase-shifted full-bridge DC/DC converter, a full-wave bridge diode structure is used due to high power. Since Si diodes have high reverse recovery energy and time, SiC diodes are used to increase the efficiency.

As a result of the modelling and simulations, it is seen that the losses are reduced with the changes made. At a constant 80°C heatsink temperature, the highest junction temperature is 112°C and the efficiency is above 95%. When the current waveform drawn from the grid is analyzed, it is seen that it complies with IEEE 519 standards.

According the given values in datasheet of the module with Si IGBTs, the switching losses are higher more than 15 times than the module with SiC MOSFETs. Additionally, the conduction loss of the module with Si IGBT is nearly 3 times of the conduction loss of the module with SiC MOSFETs. It is clear that the Si IGBTs can work with lower switching frequency than the SiC MOSFETs. If we use the module with Si IGBTs at the DC/DC converter part at the 20 kHz of switching frequency, the total losses of the semiconductors are 4 times bigger. With a usage of module with SiC

MOSFETs, the total semiconductor losses can be reduced 76.41%. Also, with a switching frequency of 40 kHz, the sizes of the magnetics can be halved compared to the Si IGBT with 20 kHz.

The experimental results of the designed system are consistent with the simulation results. The experimental peak efficiency of the system was measured at 98.03%. the simulation results are taken with the output power of 22 kW with output voltage of 700 V. According to simulation results, the efficiency of the system was 95.4% for the fixed 80°C heatsink temperature. The experimental results taken with the same conditions show that the efficiency is 97.44%. That shows us the maximum heatsink temperature is much lower than the simulated system.

According to literature review, many designed systems have wide-band gap semiconductors at the DC/DC converter. The reason of that is the increasing the switching frequency to design smaller transformer. At the rectifier stage, most preferred topologies are 2-level topologies. In the system, designed for this study, neutral-point clamped rectifier is selected. Neutral-point clamped rectifier is a 3-level topology and with a 3-level topology, the DC-link voltage can be increased compared to DC-link voltage of 2-level topologies. With this increased DC-link voltage, DC/DC converter works wider output power and wider output voltage. The whole system has a power density of 0.82 kW/L. At some researches, the power density of 2.74 kW/L can be seen. The reason of that is the designed systems have less power and uses fast chargers and slow chargers together.

7.2.Future Work

For future works, it is possible to changing the rectifier topology and semiconductors of the rectifier. At the ANPC rectifier topology, the diodes of the NPC rectifier topology are replaced with fully controlled switching devices like MOSFET and IGBT. MOSFETs and IGBTs have less conduction losses than the diodes. Also using only SiC MOSFETs decreases the switching losses, too. It is possible using hybrid structure with Si IGBTs and SiC MOSFETs together. The switching devices, that have a switching frequency equal to grid frequency, can be selected as Si IGBT. If WBG semiconductors are used in the rectifier, the switching frequency can be increased. With a higher switching frequency, smaller grid connection filter usage is possible.

The rectifier diodes of the PSFB converter can be replaced with fully controlled switching devices. With that change, the losses of the DC/DC converter can be reduced. If the controller structure is modified, the system can be work as a bidirectional charger.





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APPENDICES

APPENDIX A: Datasheet of F4-23MR12W1M1_B76

APPENDIX B: Datasheet of DDB2U60N12W1RF_B11

APPENDIX C: Datasheet of F3L100R12W2H3_B11

APPENDIX D: Area Product Distribution (WaAc) Chart of Magnetics

APPENDIX E: Datasheet of Core 0078189A7

APPENDIX F: Datasheet of Core MS-157026-2

APPENDIX G: Datasheet of QA151

APPENDIX H: Datasheet of QA151M

APPENDIX A: Datasheet of SiC Full Bridge Module F4-23MR12W1M1_B76

F4-23MR12W1M1_B76 EasyPACK™ module



Preliminary datasheet

EasyPACK™ module with CoolSiC™ Trench MOSFET and PressFIT / NTC

Features

- Electrical features
 - $V_{DSS} = 1200\text{ V}$
 - $I_{DN} = 50\text{ A} / I_{DRM} = 100\text{ A}$
 - Low switching losses
 - High current density
 - Low inductive design
- Mechanical features
 - Integrated NTC temperature sensor
 - PressFIT contact technology
 - Rugged mounting due to integrated mounting clamps



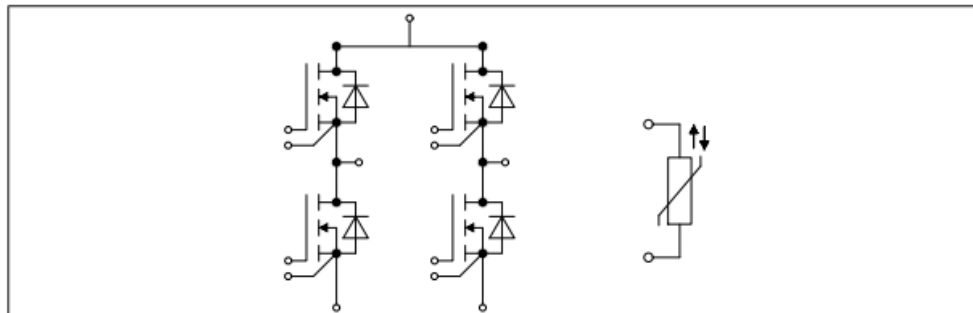
Potential applications

- Welding
- DC charger for EV
- DC/DC converter
- High Frequency Switching application

Product validation

- Qualified for industrial applications according to the relevant tests of IEC 60747, 60749 and 60068

Description



APPENDIX B: Datasheet of SiC Diode Module DDB2U60N12W1RF_B11

DDB2U60N12W1RF_B11 EasyBRIDGE module



EasyBRIDGE module with CoolSiC™ Schottky diode and PressFIT / NTC

Features

- Electrical features
 - $V_{CES} = 1200\text{ V}$
 - $I_{C\text{ nom}} = 60\text{ A} / I_{CRM} = 120\text{ A}$
 - CoolSiC™ Schottky diode gen 5
 - High dynamic robustness
 - $T_{vj\text{ op}} = 150\text{ °C}$
- Mechanical features
 - Compact design
 - Rugged mounting due to integrated mounting clamps
 - PressFIT contact technology
 - Integrated NTC temperature sensor
 - Al_2O_3 substrate with low thermal resistance



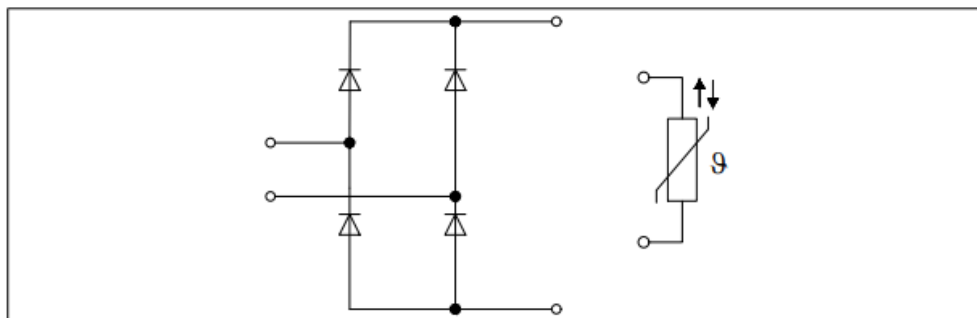
Potential applications

- DC charger for EV

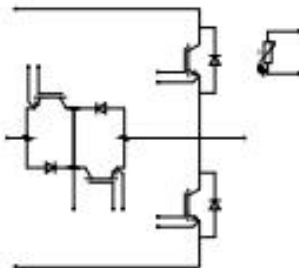
Product validation

- Qualified for industrial applications according to the relevant tests of IEC 60747, 60749 and 60068

Description



APPENDIX C: Datasheet of Si IGBT NPC Module F3L100R12W2H3_B11

Technische Information / Technical Information			
IGBT-Modul IGBT-Module		F3L100R12W2H3_B11	
EasyPACK Modul mit aktiver "Neutral Point Clamp 2" Topologie und PressFIT / NTC EasyPACK module with active "Neutral Point Clamp 2" topology and PressFIT / NTC			
Vorläufige Daten / Preliminary Data			
 Typical Appearance		 $V_{CES} = 1200V$ $I_{C\,nom} = 50A / I_{CRM} = 100A$	
Typische Anwendungen • 3-Level-Applikationen • Solar Anwendungen		Typical Applications • 3-Level-Applikationen • Solar Applications	
Elektrische Eigenschaften • High Speed IGBT H3 • Niedrige Schaltverluste • $T_{vj\,op} = 150^{\circ}C$		Electrical Features • High Speed IGBT H3 • Low Switching Losses • $T_{vj\,op} = 150^{\circ}C$	
Mechanische Eigenschaften • PressFIT Verbindungstechnik • RoHS konform		Mechanical Features • PressFIT Contact Technology • RoHS compliant	
Module Label Code			
Barcode Code 128	 0000012345600000000000	Content of the Code	Digit
		Module Serial Number	1 - 5
		Module Material Number	6 - 11
		Production Order Number	12 - 19
		Datecode (Production Year)	20 - 21
		Datecode (Production Week)	22 - 23
DMX - Code			
prepared by: CM	date of publication: 2015-02-03		
approved by: AKDA	revision: 2.3	LIL approved (E83335)	

APPENDIX D: Core Selection Chart of Magnetics Company

Area Product Distribution (WaAc) Chart

WaAc (cm ²)	RS, DS, HS	E	EC, EER, EFD, ETD	EP, RM	ER	Planar	Pot	PQ	TC	U, UR
<0.001									40200 TC 40301 TC 40502 TC	
0.001									40401 TC 40402 TC 40503 TC 40601 TC	
0.002		40904 EE					40704 UG			
0.003					40906 EE		40905 UG		40603 TC	
0.004			41009 EFD		41126 EE					
0.005				40707 EP						
0.006					41308 EI		41107 UG			
0.008						41434 EI			40705 TC	
0.01			41212 EFD	41010 EP 41110 RM	41308 EE 41426 EE	41425 EE	41109 UG		41003 TC	41106 UI
0.02	41408 RS DS HS	41203 EE	41515 EFD	41510 RM		41434 EE	41408 UG		41005 TC	41106 UI
0.03		41205 EE 41707 EE		41313 EP	41826 EE	42107 EI 41805 EI			40907 TC	
0.04						41805 EI			41303 TC 41435 TC	
0.05	41811 HS			41812 RM	42313 EE				41206 TC 41304 TC 41405 TC 41407 TC 41506 TC	
0.06				41717 EP 41912 RM		42107 EE	41410 UG		41305 TC	
0.07	41811 RS DS				42014 EI	42107 EE 41805 EE	41811 UG	42610 UG	41306 TC 41406 TC	
0.08	42311 DS HS	41808 EE			42517 EI				41450 TC	
0.09			42019 EFD				41814 UG			
0.1	42311 RS	41810 EE			42014 EE	42216 EI			41605 TC	
0.2	42318 RS DS HS	42510 EE 42515 EI	42523 EFD	42013 RM 42120 EP 42316 RM	42517 EE 43021 EI	42214 EI	42213 UG	42016 UG 42020 UG 42614 UG	41606 TC 41607 TC 41410 TC 41610 TC	
0.3	42616 RS DS HS	42513 EE	43030 EFD		42521 EE 43225 EE	43618 EI 42216 EE 42214 EE		43214 UG	41809 TC 42106 TC	42515 UI
0.4		42526 EE		42819 RM		42217 EE 43208 EI 44008 EI	42616 UG	42620 UG	42109 TC 42206 TC	
0.5		42520 EE 43007 EE	42814 EER		43021 EE				42207 TC	
0.6	43019 DS HS	42515 EE 43009 EE				43618 EE	42823 UG	42625 UG		42220 UI 42515 UI
0.7	43019 RS	42530 EE	42929 EFD 42817 EER			43208 EE	43019 UG		42507 TC	
0.8			43517 EC			44008 EE		43220 UG	42506 TC 42212 TC	42512 UI
0.9						43808 EI			42508 TC	

Area Product Distribution (WaAc) Chart

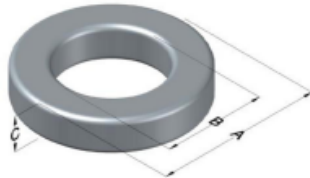
WaAc (cm ²)	RS, DS, HS	E	EC, EER, EFD, ETD	EP, RM	ER	Planar	Pot	PQ	TC	U, UR
<1	43622 RS DS HS	43515 EE 44011 EE 44020 EI	43434 ETD	43723 RM		44308 EI			42712 TC 42908 TC	42530 UU
2		44016 EE 44317 EE 43520 EE	43521 EER 43939 ETD 44013 EER 44119 EC	44230 RM		44310 EI 43808 EE	43622 UG	43230 UG	42915 TC 43113 TC 43806 TC	
3	44229 RS DS	44721 EE	44216 EER 44818 EER			43809 EE 44308 EE		43535 UG	43610 TC 43813 TC	44119 UR 44121 UR
4		44020 EE 44022 EE	44444 ETD 44821 EER 45224 EC 45418 EER			44310 EE	44229 UG		43615 TC	44125 UR
5						45810 EI		44040 UG	43620 TC 44416 TC	44130 UR
6		44033 EE 46016 EE	44949 ETD			46410 EI			44419 TC	
7		45724 EE							43825 TC 44015 TC	
8						45810 EE		45050 UG	44715 TC	
9			45454 ETD						44920 TC	45716 UR
10		45528 EE								
11						46410 EE			44916 TC	
12		45530 EE								
13			47035 EC						44925 TC	
14			45959 ETD							45917 UR
15		47228 EE								
16									46013 TC 46113 TC	
21		46022 EE							44932 TC	
22										46420 UU
23		47133 EE					43428 UG			
24		46527 EE								
25									46019 TC 47313 TC	
34		48020 EE							46325 TC 46326 TC	
46									48613 TC	49316 UI
51						49938 EE			47325 TC	
61										49925 UI
70									48619 TC	
91		49928 EE							48625 TC 48626 TC 49715 TC	49316 UU
106									49718 TC	
121										49925 UU
171									49725 TC	
286										49920 UU
372									49740 TC	

APPENDIX E: Datasheet of Core 0078189A7



0078189A7

110 Delta Drive
Pittsburgh, PA 15238
NAFTA Sales: (1)800-245-3984
HK Sales: (852)3102-9337
magnetics@spang.com
www.mag-inc.com

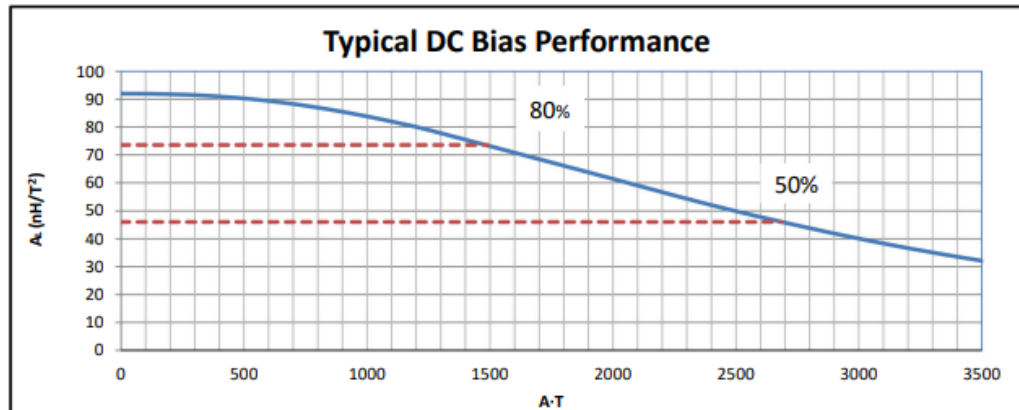


XFLUX Permeability (μ)	A_L (nH/T ²)	Core Marking			Coating Color
		Lot Number	Part Number	Inductance Grade	
40	92 $\pm$ 8%	XXXXXX	78189A7	N/A	Brown

Dimensions	Uncoated		Coated Limits		Packaging
	(mm)	(in)	(mm)	(in)	
OD (A)	57.15	2.250	58.04	2.285	Cardboard cut-outs Box Qty= 80 pcs
ID (B)	26.39	1.039	25.58	1.007	
HT (C)	15.24	0.600	16.13	0.635	

Electrical Characteristics			Physical Characteristics						
Watt Loss @ 50 kHz, 100mT max(mW/cm ²)	DC Bias min (oersteds)		Voltage Breakdown wire to wire min (V _{ac})	Break Strength min (kg)	Window Area W _A (mm ²)	Cross Section A _e (mm ²)	Path Length L _e (mm)	Volume V _e (mm ³)	Weight (g)
850	80%	50%	3000	274	514	229	125	28,600	200
	120	230							

Winding Information					Temperature Rating	
Winding Length Per Turn				Wound Coil Dimensions (mm)		Curie Temp: 700°C
Winding Factor	(mm)	Winding Factor	(mm)	40% Winding Factor	OD	62.0
					HT	
				Completely Full Window	Max OD	75.7
					Max HT	
0%	64.6	40%	77.8	Notes:		
20%	71.2	45%	79.8			
25%	72.9	50%	81.6	Surface Area (mm²)		
30%	74.1	60%	85.6			
35%	76.3	70%	90.1			
				Unwound Core	8,500	
				40% Winding Factor	12,000	



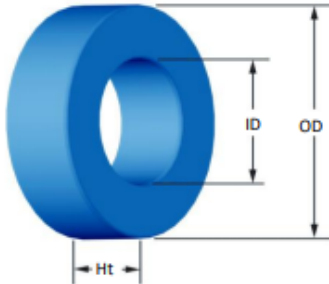
Revision 10/6/2021

APPENDIX F: Datasheet of Core MS-157026-2



Part Number: **MS-157026-2**

Revision 2021-Dec-01 - Generated 2021-Dec-01



(If coated, Max./Min. includes coating)

OD	(nom. - bare core) (max.)	39.88 mm 40.69 mm	1.570 in 1.602 in
ID	(nom. - bare core) (min.)	24.13 mm 23.32 mm	0.950 in 0.918 in
HT	(nom. - bare core) (max.)	14.48 mm 15.37 mm	0.570 in 0.605 in

Mass	(approximate)	54 grams
A_e - Eff. Mag. Cross Section		1.07 cm ²
L_p - Eff. Mag. Path Length		9.85 cm
V_p - Eff. Core Volume		10.5 cm ³
W_A - Min. Eff. Window Area		4.27 cm ²
S_A - Surface Area		60.2 cm ²
m_{lt} - mean length per turn		5.98 cm

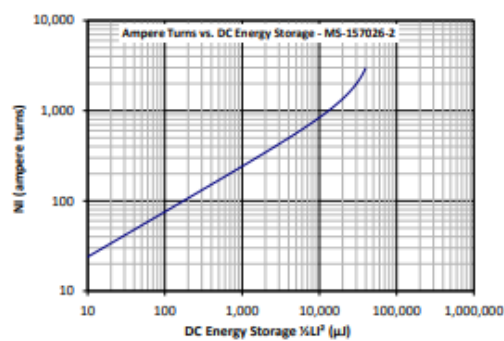
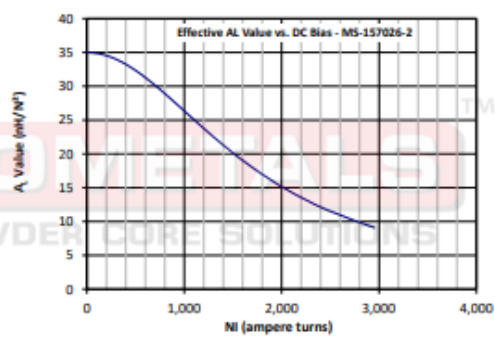
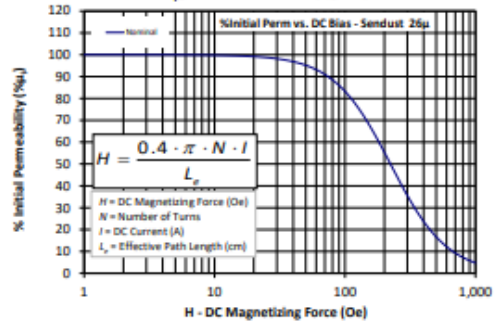
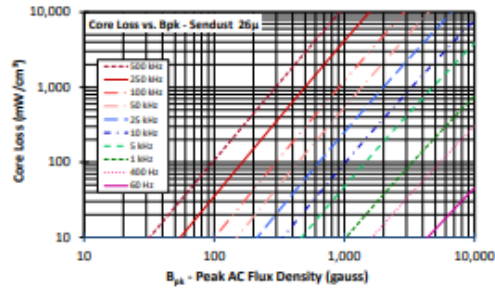
Inductance		
μ (reference)		26
A_L value (nominal)		35 nH/N ²
Test Winding	N=70, #20 AWG	
Frequency	10 kHz	
Voltage on Agilent 4284A	0.33 V	
AL tolerance		±8%

Core Loss		
Core Loss(mW/cm ³) _{pk}	$\frac{a}{B_{pk}^2} + \frac{b}{B_{pk}^{1.5}} + \frac{c}{B_{pk}^{1.85}} + d \cdot B_{pk}^2 \cdot f^2$	
	where B_{pk} expressed in gauss, f expressed in hertz, and: $a=1.000E+06$, $b=4.969E+08$, $c=3.993E+06$, $d=2.867E-14$	
B_{pk}	500 G	
frequency	100 kHz	
Core Loss (nominal)	295 mW/cm ³	
Core Loss (maximum)	339 mW/cm ³	

DC Saturation		
μ_i	$\frac{1}{a + b \cdot H^c} + d$	
	where H expressed in oersteds, and: $a=1.000E-02$, $b=2.061E-07$, $c=1.995$, $d=0.000$	
H_{dc}	200 Oe	
Percent Initial Perm(nom.)	55.4%	
Percent Initial Perm(min.)	46.3%	

Coating/Pkg		
Coating Type:	Blue Epoxy	
Voltage Breakdown (min.)	1000 Vrms	
Limit	0.1 mA, 5 s	
Package Quantity	216 Pcs/Box	

Winding Table	Wire Size	8	10	12	14	16	18	20	22	24	26	28
	AWG	3.150	2.500	2.000	1.600	1.250	1.000	0.800	0.630	0.500	0.400	0.315
	mm	3.150	2.500	2.000	1.600	1.250	1.000	0.800	0.630	0.500	0.400	0.315
	Turns	17	22	28	35	45	56	70	88	111	138	173
	Single Layer	Rdc(Ω)	2.1 m	4.3 m	8.7 m	17.3 m	35.4 m	70.0 m	139.2 m	278.3 m	558.3 m	1.1
		Turns	22	35	54	83	128	199	307	476	736	1,139
	Full Winding	Rdc(Ω)	2.7 m	6.8 m	16.8 m	41.0 m	100.6 m	248.8 m	610.5 m	1.5	3.7	9.1
		Turns	22	35	54	83	128	199	307	476	736	1,139
		Rdc(Ω)	2.7 m	6.8 m	16.8 m	41.0 m	100.6 m	248.8 m	610.5 m	1.5	3.7	9.1



APPENDIX G: Datasheet of QA151

DC/DC Converter for IGBT Driver QAxx1 Series

MORNSUN®

DC/DC Converter for IGBT driver



Patent Protection



RoHS

FEATURES

- High efficiency up to 81%
- Ultra compact SIP package
- I/O Isolation test voltage 3kVAC
- Max. Capacitive Load: 1000uF
- Ultra low isolation capacitance
- Operating ambient temperature range: -40°C to +105°C
- No-load operation allowed

QAxx1 series are DC-DC converters for IGBT drivers. The ultra low isolation capacitance can improve the capability of anti-interference. The built-in common-ground mode of the unique asymmetric voltage output mode reduces the driver loss of IGBT driver. It features short-circuit protection, auto-recovery and can be widely used in:

1. General inverter
2. AC servo drive system
3. Electric welding machine
4. Uninterruptible power supply (UPS)

Selection Guide

Certification	Part No.	Input		Output		Full Load Efficiency (%) Min./Typ.	Capacitive Load (uF) Max.
		Input Voltage(VDC) Nominal (Range)	Input Current(mA, Typ.) full load/no-load	Voltage(VDC) +Vo/-Vo	Current(mA) +Io/-Io		
EN	QA121	12 (11.4-12.6)	280/40	+15/-8.0	+120/-120	78/81	1000
-	QA151	15 (14.25-15.75)	230/35				
-	QA241	24 (22.8-25.2)	144/30				

Input Specifications

Item		Operating Conditions	Min.	Typ.	Max.	Unit
Surge Voltage (1sec. max.)	QA121	DC	-0.7	—	14	VDC
	QA151	DC	-0.7	—	16	
	QA241	DC	-0.7	—	26	
Input Filter			Capacitance Filter			
Hot Plug			Unavailable			

Output Specifications

Item	Operating Conditions		Min.	Typ.	Max.	Unit	
Output Voltage	QA121	+Vo Vin=12VDC, Pin6 & Pin7 +Io= +120mA	14.10	14.81	15.60	VDC	
		-Vo Vin=12VDC, Pin5 & Pin6 -Io= -120mA	-6.24	-7.84	-9.44		
	QA151	+Vo Vin=15VDC, Pin6 & Pin7 +Io= +120mA	14.10	14.81	15.60		
		-Vo Vin=15VDC, Pin5 & Pin6 -Io= -120mA	-6.24	-7.84	-9.44		
	QA241	+Vo Vin=24VDC, Pin6 & Pin7 +Io= +120mA	14.10	14.81	15.60		
		-Vo Vin=24VDC, Pin5 & Pin6 -Io= -120mA	-6.24	-7.84	-9.44		
Voltage Accuracy		10% -100% load	See output regulation curve (Fig. 2, Fig. 3)			%	
Linear Regulation		Input voltage range	Positive output	-	±1.1	±1.2	-
			Negative output	-	±1.1	±1.2	
Load Regulation		10%-100% load	Positive output	-	8	15	%

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APPENDIX H: Datasheet of QA151M

MOSFET SiC Driver Dedicated Power Supply QA151M

MORNSUN®

MOSFET SiC driver dedicated power supply



Continuous Short
Circuit Protection

FEATURES

- High efficiency up to 80%
- SIP package
- I/O isolation test voltage: 3.5k VAC
- Ultra low isolation capacitor
- Operating ambient temperature range: -40°C to +105°C
- Continuous short-circuit protection
- Industry standard pin-out

Patent Protection RoHS

QA151M is DC-DC module power supply designed for MOSFET SiC driver requiring two set of isolation power supply. The mode uses two common ground output modes to better provide energy for SiC turn-on and turn-off. Output short-circuit protection and self-recovery capabilities are also provided. General application includes:

1. Universal converter
2. AC servo drive systems
3. Electric welding machines
4. Uninterruptible power supplies (UPS)

Selection Guide

Part No.	Input Voltage (VDC)	Output		Full Load Efficiency(%) Min./typ.	Max. Capacitive Load*(μ F)
	Nominal (Range)	Voltage (VDC) +Vo/-Vo	Current (mA) +Io/-Io		
QA151M	15 (13.5-16.5)	+15/-5	+100/-100	76/80	220

Note: *The specified maximum capacitive load value for positive and negative output is identical.

Input Specifications

Item	Operating Conditions	Min.	Typ.	Max.	Unit
Input Current (full load / no-load)	15V Input	—	162/15	—	mA
Surge Voltage (1sec. max.)		-0.7	—	21	VDC
Input Filter		Capacitor filter			
Hot Plug		Unavailable			

Output Specifications

Output specifications						
Item	Operating Conditions		Min.	Typ.	Max.	Unit
Output Voltage	Vin=15VDC, Pin6 & Pin7 +Io=+100mA	+Vo	14.4	15	15.9	VDC
	Vin=15VDC, Pin5 & Pin6 -Io=-100mA	-Vo	-4.75	-5	-5.75	
Voltage Accuracy	Vin=15VDC, Pin6 & Pin7 +Io=+100mA	+Vo	-4% to +6%			
	Vin=15VDC, Pin5 & Pin6 -Io=-100mA	-Vo	-8% to +15%			
	10%-100% load		See output regulation curve(Fig. 1)			
Linear Regulation	Input voltage change: ±1%		--	±1.1	--	--
Load Regulation	10%-100% load	+Vo	--	7	--	%
		-Vo	--	9	--	
Ripple & Noise*	20MHz bandwidth	+Vo	--	120	--	mVp-p
		-Vo	--	80	--	
Temperature Coefficient	100% load		--	±0.02	--	%/℃
Short-circuit Protection			Continuous, self-recovery			
Note: *the "parallel cable" method is used for ripple and noise test, please refer to DC-DC converter application notes for specific information.						

Note: *The "parallel cable" method is used for ripple and noise test, please refer to DC-DC converter application notes for specific information.

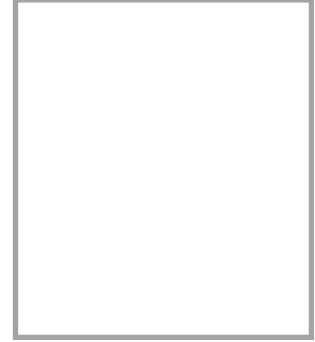
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CURRICULUM VITAE



Name Surname : Özgür Can MİLLETSEVER



EDUCATION :

- **B.Sc. :** 2020, Istanbul Technical University, Faculty of Electrical and Electronics Engineering, Electrical Engineering

PROFESSIONAL EXPERIENCE AND REWARDS:

- 2019-2020 R&D Intern-Mercedes-Benz Türk
- 2020-2020 Project Engineer-Elkon Elektrik
- 2020-2023 R&D Engineer Elektra Elektronik
- 2022 Best Paper Award at PEMC 22

PUBLICATIONS, PRESENTATIONS AND PATENTS ON THE THESIS:

- **O. C. Milletsever**, V. T. Buyukdegirmenci and M. Yilmaz, "Controller Design of Dual Active Bridge Converter for Electric Vehicle Fast DC Charger Applications," 2022 IEEE 20th International Power Electronics and Motion Control Conference (PEMC), Brasov, Romania, 2022, pp. 81-86, doi: 10.1109/PEMC51159.2022.9962874.

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- V. T. Buyukdegirmenci, A. Sozuer, **O. C. Milletsever**, O. F. Kozarva, T. Oz and A. M. Hava, "Considerations for Inverter Topology Selection and Limitations in Active Power Filtering Applications," 2022 IEEE Power and Energy Conference at Illinois (PECI), Champaign, IL, USA, 2022, pp. 1-6, doi: 10.1109/PECI54197.2022.9744007.

- V. T. Buyukdegirmenci, O. F. Kozarva, **O. C. Milletsever** and A. M. Hava, "Design Trade-offs and Considerations for Improving the PCB Current Carrying Capacity in High Power Density Power Electronics Applications," 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), Houston, TX, USA, 2022, pp. 1678-1685, doi: 10.1109/APEC43599.2022.9773486.

