DESIGN, FABRICATION, AND CHARACTERIZATION OF NORMALLY-OFF GAN HEMTS

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By
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ABSTRACT

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GaN-based high-electron-mobility transistors (HEMTs) have been developing rapidly from the time when they were first demonstrated in the 1990s. They have consistently been presented as a displacement technology to silicon based power devices owing to the superior material properties of GaN such as high-electric breakdown field, high-electron saturation velocity, and high mobility. Normally-off GaN HEMT devices are particularly significant in power electronics applications.

In this thesis, a comprehensive study of normally-off high-electron-mobility transistors is presented, including theoretical background review, theoretical analysis, physically-based device simulations, device fabrication and optimization and electrical characterization. p-GaN gate InAlN/GaN HEMT and recessed AlGaN/GaN MISHEMT devices have been successfully demonstrated.

Keywords: HEMT, GaN, InAlN, normally-off, power electronics, threshold voltage, atomic layer deposition, alumina, recess etch, fluorine treatement, p-GaN.

ÖZET

NORMALDE KAPALI YEMT AYGITLARIN TASARIM, FABRİKASYON VE KARAKTERİZASYONU

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GaN tabanlı yüksek-elektron-mobiliteli transistörleri 1990'lı yılların başında ortaya çıktıklarından beri yoğun bir şekilde çalışılan ve GaN malzemesinin yüksek kırılma alanı, yüksek satürasyon hızı ve yüksek mobilitesi sayesinde düzenli olarak silikon tabanlı güç transistörlerine rakip olarak gösterilen aygıtlar olmuşlardır. Normalde kapalı olan GaN YEMT cihazları, güç elektroniği uygulamalarında özellikle önemlidir.

Bu tez, teorik arkaplan incelemesi, teorik analiz, fiziksel temelli aygıt simülasyonları, aygıt üretimi ve optimizasyonu ve elektriksel karakterizasyonu dahil olmak üzere normalde kapalı yüksek elektronlu mobil transistörlerin kapsamlı bir çalışmasını sunar. Kapı bölgesinde p-GaN katmanı içeren InAlN/GaN YEMT ve gömme kapı aşındırması içeren AlGaN/GaN metal-yalıtkan-yarıiletken MYY-YEMT aygıtları başarıyla gösterilmiştir.

Anahtar sözcükler: YEMT, GaN, InAlN, normalde kapalı, güç elektroniği, eşik voltajı, atomik katman biriktirme, alümina, gömme kapı aşındırması, flor implantasyonu, p-GaN.

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Chapter 1

Introduction

The semiconductor industry has been dominated by silicon technologies for decades on account of its well established CMOS process. The growth of the industry has been majorly driven by scaling, with smaller node technologies being developed, as predicted by Moore's Law. However, silicon based power semiconductor devices are approaching their limits determined by fundamental material properties. It is predicted that further scaling will reach its limits in the next few decades and the scaling is trying to be extended for more technology generations with multigate field effect transistors [1]. In addition to the limitations of scalability, silicon, with its relatively low band gap energy, is not always able to meet the need for high-power and high-frequency devices required in military applications and wireless communications. Thus new material technologies for use in devices must be explored in order to address the limitations. Wide bandgap materials, such as gallium nitride (GaN) and silicon carbide (SiC) have properties that are suitable for power electronic applications.

Wide band-gap, high breakdown voltage, and high thermal conductivity are the most critical characteristics for power device applications. Furthermore, for high speed response characteristics high electron mobility, high hole mobility, high saturation velocity, and low dielectric constant are of importance. The semiconductor materials utilized for such applications are Si, GaAs, GaN and 4H-SiC, for which power

devices have begun to be available commercially, β-Ga_2O_3, which has recently gained increasing interest, and diamond, which is a promising material still in the research stage.

Table 1.1 Semiconductor material properties [2],[3],[4].

MATERIAL	**Si**	**GaAs**	**Diamond**	**GaN**	**4H-SiC**	**β-Ga_2O_3**
Bandgap E_g (eV)	1.1	1.4	5.45	3.42	3.26	4.8
Electron Mobility μ_e ($cm^2/V\cdot s$)	1400	8500	2200	900	1000/850	~300
Hole Mobility μ_h ($cm^2/V\cdot s$)	600	400	1600	150	115	
Breakdown Field E_c (MV/cm)	0.3	0.4	10	3.3	2.5	8
Saturation Velocity v_{sat} (10^7 cm/s)	1	2	2.7	2.7	2.2	
Intrinsic Carrier Concentration n_i (cm^{-3})	1.5×10^{10}	1.8×10^{6}	1.6×10^{-27}	1.9×10^{-10}	8.2×10^{-9}	
Thermal Conductivity λ (W/Cm·K)	1.5	0.5	20	2	4.9	0.14
Relative Dielectric Constant ε	11.8	12.8	5.5	9	9.7	10
Bulk Material (Substrate)	Commercial	Commercial	Research	Research	Commercial	Commercial
Band Structure	Indirect	Direct	Indirect	Direct	Indirect	Direct
Baliga FOM $E\cdot\mu\cdot E_C^3$	1.0	15.6	4110	650	130	3444
Johnson FOM $E_c\cdot V_{sat}/2\pi$	1	7.1	2540	760	180	

In comparison to other materials such as Si, GaAs, and SiC, GaN-based power transistors demonstrate greater potential as a result of the superior material properties of GaN, as summarized in Table 1.1. GaN-based technologies, therefore possess a competitive advantage. The impact of material properties on the performance of semiconductor devices are assessed with figures of merit. One such merit is the Johnson figure of merit, which is given by the product of the breakdown electric field and saturation velocity and is used to assess the suitability of a material for high-power high-frequency applications. Another figure of merit is the Baliga figure of merit, which is given by the product of relative dielectric constant, mobility, and breakdown electric field and determines the material parameters required to minimize the conduction losses in power devices [5]. The Baliga figure of merit and Johnson figure of merit are also given in Table 1.1. By comparing the figures of merit, it can be seen that GaN is a promising material choice. Smaller devices can be achieved due to the high power per unit width, enabling easier manufacture and higher impedance, which further allows easier matching, whereas this can be difficult to achieve with other materials such as GaAs. Operation of GaN-based devices at higher voltages is enabled by the high breakdown voltage, which leads to a lessening in the necessity for voltage conversion, a decrease in power requirements, and simplification in cooling needs. Additionally, GaN posseses a direct bandgap energy, which is important in light-emitting diode technologies and the utilization of this overlap in technologies can help drive down development costs. The advantages of GaN and the enabling material properties are summarized in Table 1.2.

Table 1.2 Comparative advantages of GaN based devices [6].

NEED	ENABLING FEATURE	PERFORMANCE ADVANTAGE
High Power/Unit Width	Wide band gap, high field	Compact, ease of matching
High Voltage Operation	High breakdown field	Eliminate/reduce step down
High Linearity	HEMT technology	Optimum band allocation
High Frequency	High electron velocity	Bandwidth l-wave/mm-wave
High Efficiency	High operating voltage	Power saving, reduced cooling
Low Noise	High gain, high velocity	High dynamic range receivers
High Temperature Operation	Wide band gap	Rugged, reliable, reduced cooling needs
Thermal Management	SiC substrate	High power devices with reduced cooling needs
Technology Leverage	Direct band gap, enabler for lighting	Driving force for technology low cost

The typical uses of power electronic systems are to process and control the flow of electric power. The aim of a power electronic system is providing a user load with the optimum form of power. The power switching device is the key component of a power electronic system and the characteristics of the power switching devices are the determining factors of the frequencies and power levels at which operation of the power electronic system is possible. GaN based devices are normally-on and are suitable for low-voltage and high frequency applications. However, normally-off devices are required in power switching applications in order to simplify the gate driver configuration and ensure safe operation. Normally-off operation can be obtained with GaN based devices through two approaches, which are to combine a low-voltage silicon MOSFET and high-voltage normally-on GaN HEMT in cascode configuration or to use a true normally-off GaN device. The benefit of using a cascode configuration is the similar gate control to conventional silicon MOSFETs, whereas

a true normally-off GaN device is advantageous in that off-chip or on-chip gate driver circuits can be used to directly drive the device which is helpful for safe operation and reducing ringing noises. Different approaches such as gate recess, surface treatments, or various capping layers (InGaN, p-GaN, p-AlGaN etc.) can be utilized in order to realize normally-off GaN HEMTs.

In this thesis the simulation, fabrication, and characterization of normally-off GaN devices are carried out. The studied devices are p-GaN gate InAlN/GaN HEMTs and recessed gate AlGaN/GaN MISHEMTs with fluorine treatment. The effect of various device parameters on normally-off operation is investigated using device simulation. The optimum devices determined from device simulation are fabricated and characterized.

Chapter 2 provides background information on GaN HEMTs. III-N semiconductors and their crystal, electrical, and elastic properties are introduced. Polarization in III-N materials and the resulting two-dimensional-electron gas (2DEG) are described. Finally, HEMT devices, their operating principles, and the approaches to obtain normally-off operation are explained.

Chapter 3 deals with the simulation of HEMT devices. Physical device simulation is briefly introduced and the simulation methodology and models are described. Conduction band and threshold voltage simulations for p-GaN gate InAlN/GaN HEMTs and recessed gate AlGaN/GaN MISHEMTs with fluorine treatment are carried out.

Chapter 4 describes the device fabrication. The different steps used in the fabrication of HEMT devices are explained. Studies carried out for the development of the fabrication process are detailed and the process steps for the studied devices are given.

Chapter 5 presents the electrical characterization results of the fabricated HEMT devices. Various DC transistor measurements are conducted. Parameters such as the

threshold voltage, drain current density, leakage current density, and breakdown voltage are extracted and analyzed.

Chapter 6 consists of the concluding remarks.

Chapter 2

Theoretical Background for HEMTs

This chapter provides a brief summary on III-V semiconductors and more specific background information on the material properties of GaN and its implementation in high electron mobility transistors (HEMTs). In Section 2.1 the physical properties of GaN are described. Section 2.2 describes polarization in III-N semiconductors and Section 2.3 describes the formation of 2DEG in heterostructures. Section 2.4 presents the AlGaN/GaN HEMT and explains the operating principles. Section 2.5 outlines HEMT devices based on the InAlN/GaN heterostructure. In Section 2.6 normally-off devices and their operation is studied.

2.1 Material Properties of GaN

Group III-V semiconductors are comprised from the combination of group III elements (Al, Ga, In) and group V elements (N, P, As, Sb), which corresponds to a possibility of 12 combinations, the most common being GaAs, InP GaP and GaN. The group III-V semiconductors form crystals in either the diamond lattice structure, referred to as zincblende (β-phase) or in a hexagonal lattice structure, referred to as wurtzite (α-phase), shown in Figure 2.1. The rocksalt (NaCl) lattice structure may also be induced under very high pressures for GaN, AlN, and InN. For GaN, the thermodynamically stable phase is the hexagonal lattice structure. The hexagonal unit cell is defined by two lattice constants, namely, c and a, and contains 6 atoms of each type. The wurtzite structure contains two interpenetrating Hexagonal Close Packed (HCP) sublattices, such that each sublattice contains one type of atom, which are

offset along the *c* axis by 5/8 of the cell height (5*c*/8). Four nitrogen atoms surround each gallium atom and similarly, each nitrogen atom is surrounded by four gallium atoms. The stacking sequence of the (0001) plane in the ⟨0001⟩ direction is ABABAB. Hexagonal wurtzite structure GaN has a molecular weight of 83.728 gm/mol and lattice parameters of a_0 = 3.1892 ± 0.0009 Å and c_0 = 5.1850 ± 0.0005 Å at room temperature.

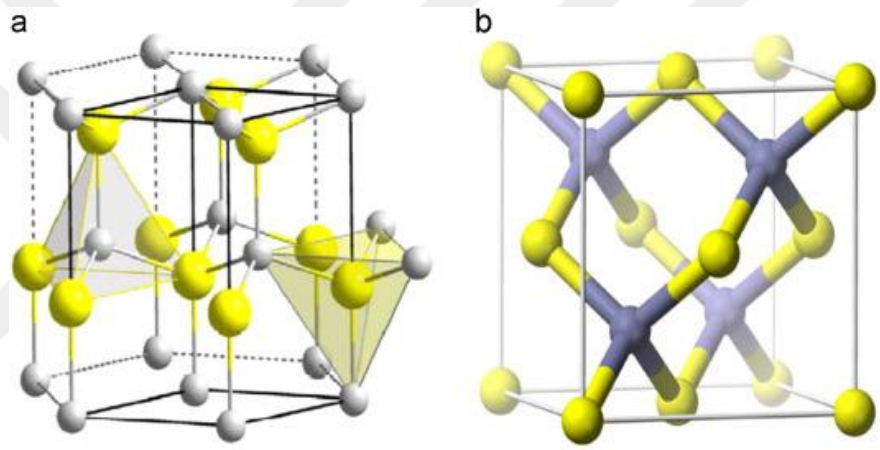


Figure 2.1 Crystal structure of (a) wurzite GaN and (b) zinc-blende GaN [7].

In Group III-nitrides epitaxial layers, hexagonal and cubic phases can coexist since only the stacking arrangement of nitrogen and metal atoms (polytypes) differ between the α- and β-phases of Group III-nitrides, which can occur in cases like the existence of stacking faults. Three parameters define the hexagonal crystal structure of Group III-N semiconductors. These are the edge length of the basal hexagon a_0, the height of the hexagonal prism c_0, and the bond length between the anion–cation along the (0001) axis which is denoted by *u*. GaN, AlN, and InN possess different cations and ionic radii (Al^{3+}: 0.39 Å, Ga^{3+}: 0.47 Å, In^{3+}: 0.79 Å), so their lattice constants, bandgap energies, and binding energies are different as shown in Table 2.1 [8].

Table 2.1 Lattice constants and binding energies of hexagonal GaN, AlN and InN [8].

WURTZITE, 300 K	**AlN**	**GaN**	**InN**
a_0 (Å)	3.112	3.189	3.54
c_0 (Å)	4.982	5.185	5.705
c_0/a_0 (EXP.)	1.6010	1.6259	1.6116
c_0/A_0 (CALC.)	1.6190	1.6336	1.6270
u_0	0.380	0.376	0.377
a_{BOHR} (Å)	5.814	6.04	6.66
E_B (M–N)$^+$	2.88	2.20	1.98

$^+$ M = In, Ga or Al, N = Nitride

Since its synthesis in 1932 by Johnson et al. [9], it has been widely observed that GaN is an exceedingly chemically stable and significantly hard compound. The chemical stability at elevated temperatures in combination with its hardness made GaN an advantageous compound for use as protective compounds. Most GaN research, however, is focused on semiconductor device applications, owing to the compounds wide energy bandgap, which makes it excellent for devices operating in high temperatures and caustic environments.

GaN has a bandgap energy of 3.42 eV [10], AlN has a bandgap energy of 6.13 eV [10], and InN has a bandgap energy reported in the range of 0.7 eV – 1.9 eV [11]. The large bandgap energies in GaN and AlN lead to high breakdown electric fields of 3.3 MV/cm in GaN and 11.7 MV/cm in AlN [12]. Compared to the breakdown field of 0.3 MV/cm in Si, these fields are very high, and in combination with their high thermal conductivities, GaN and AlN become preferable materials for high-power and high-temperature applications. They can also operate at high frequencies owing to their high saturation velocities and are good candidates for optical applications as they are direct bandgap semiconductors.

GaN-based devices mostly are composed of heterostructures. Some of the alloys used in heterosructures are AlGaN, InAlN, InGaN, and InAlGaN. The properties of the alloys such as bandgap energy, electron and hole effective masses, and the dielectric constant are dependent on the alloy composition. Ternary and quaternary nitride compounds form a continuous range of bandgap energies which makes bandgap engineering possible. The interpolation of the bandgap energy is not linear and can be approximated with a parabolic model that employs a bowing parameter b. The energy bandgap model is given by

$$E_g(A_xB_{1-x}N) = xE_g(AN) + (1-x)E_g(BN) - b_{ABN}x(1-x) \qquad (2.1)$$

The values of the bowing parameter b for some alloys are as follows: -0.8 eV for AlGaN, -3.4 eV for InAlN and -1.4 eV for InGaN [12]. The InAlN alloy has the additional advantage of being able to be lattice-matched to GaN.

2.2 Polarization in III-Ns

Device operation in III-Ns is largely determined by the polarization material property. Dipoles may form due to the asymmetry of bonding in low symmetry compound crystals, in which the center of negative charge (electrons) is shifted away from the center of the positive charge (nuclei), forming a polarized atom with a dipole moment [13]. Under this condition, the material will show a built-in spontaneous polarization, defined as P_{sp}. Mechanical deformation caused by a lack of center of symmetry will cause piezoelectric polarization P_{pz}. Highly pronounced polarization effects are observed in Group III-V nitride semiconductors. Group III-V semiconductors mostly crystallize in the cubic zincblende or wurtzite structures, both of which meet the condition of noncentrosymmetricity for piezoelectric polarization. The lack of inversion symmetry leads to piezoelectric effects in nitride semiconductors when strained in the ⟨0001⟩ direction. Even in the absence of strain, wurtzite GaN exhibits spontaneous polarization, due to its unique axis, which manifests as a polarization

charge at heterointerfaces. Zincblende possess a three-fold rotational symmetry axes and an inversion axis, thus the condition for spontaneous polarization is not met [14]. Piezoelectric polarization is composed of two components: strain from lattice mismatch and thermal strain arising from the difference in thermal expansion coefficient between the epitaxial layers and substrate. AlGaN/GaN based heterostructures exhibit relatively larger spontaneous polarization than piezoelectric polarization. InGaN/GaN heterostructures exhibit relatively small spontaneous polarization since in GaN and InN the spontaneous polarization is close to one another, whereas strain induced piezoelectric polarization is more significant. If defects are present in the films that act to reduce strain, there will be a reduction in the strength of piezoelectric polarization. The band structures of the heterostructures are affected by spontaneous and piezoelectric polarization.

Polarization depends on the polarity of the crystal, that is, whether the bonds along the c-direction are from cation sites to anion sites or from anion sites to cation sites. For GaN the accepted convention is that the [0001] axis points from the face of the N plane towards the Ga plane and denotes the positive *z-direction*. Thus, the polarity is said to be the Ga polarity when the bonds along the *c-direction* are from cation (Ga) to anion (N) atoms, and the direction of the bonds from Ga atoms to N atoms along the *c-direction* is accepted to be the +*z-direction*. Conversely, the polarity is said to be the N polarity when the direction of the bonds in the *c-direction* are from anion (N) to cation (Ga) atoms and the direction of the bonds along the *c-direction* is taken as the –*z-direction*. As a result, due to the lack of inversion symmetry along the *c-axis* (also called the pyroelectric axis), the [0001] and [000$\bar{1}$] are not equivalent, as shown in Figure 2.2 [9].

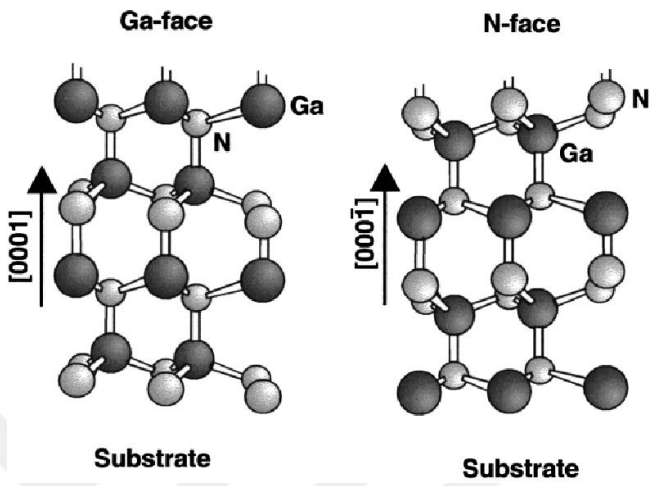


Figure 2.2 Ga- and N- faces of GaN [15].

In nitride semiconductors, the electric dipole is in the direction from the N atom to the Ga (or Al or In) atom resulting in a negative polarization value. Polarization is a bulk property, so the polarity of the crystal is not dependent on the termination of the surface layer, but is dependent only on the crystal structure direction. Nitride semiconductors are grown in either the $[0001]$ or $[000\bar{1}]$ direction and an abrupt change in the polarization at heterostructure interface may be exploited for device operation [9].

Nitride films are often grown on substrates which do not possess the wurtzite symmetry of nitride semiconductors. As a result, uniformity of the polarity of films across a substrate may not be ensured, as depicted in Figure 2.3, where the portion on the left is Ga polar whereas the portion on the right is N polar. Such regions are referred to as inversion domains and the boundary between these domains are referred to as inversion-domain boundaries. The alternating nature of anion-cation bonds cannot be maintained when inversion domains are present and can lead to flipping piezoelectric fields when combined with the strain in nitride films. Flipping fields can lead to an increase in scattering of carriers in the c-plane [9].

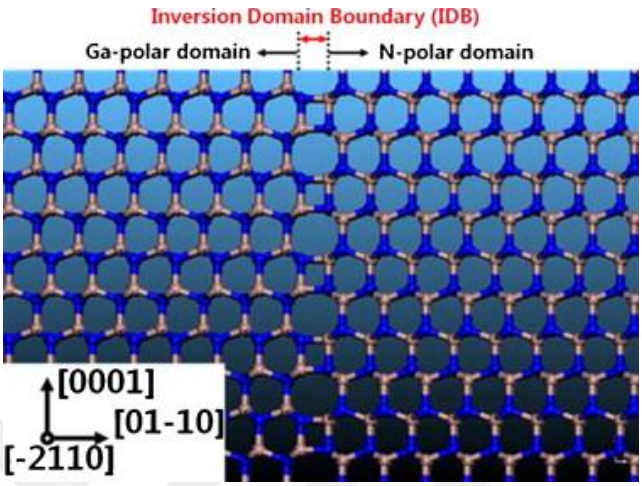


Figure 2.3 A schematic representation of inversion-domain boundary. The pink represent the gallium atoms and the blue represent the nitrogen atoms [16].

The anisotropy which gives rise to piezoelectric polarization may additionally cause pyroelectric effects, which is a considerable phenomenon in nitride-based devices as they operate at high junction temperatures. Thus, a thermally induced electric field is also likely to be present with similar consequences to that of polarization effects [9].

The physical properties of Group III-N materials are influenced by the spontaneous and piezoelectric polarization. The carrier distribution inside nitride semiconductors and shape of the band edges are influenced by the electric fields; the radiative recombination in light-emitting devices or the electrical properties of transistors can be influenced by spontaneous and piezoelectric polarization, therefore the polarization properties are important for device applications [8].

The highest symmetry compatible with the existence of spontaneous polarization occurs in the wurtzite structure. The piezoelectric tensor of the wurtzite structure possesses three nonzero components, thus, wurtzite structures possess both spontaneous (**P_{SP}**) and a piezoelectric (**P_{PE})** components. Spontaneous polarization is closely dependent on the structural parameters of the materials, so the polarization for the different nitride materials is quantitatively different. From GaN to InN to AlN

the nonideality of the crystal structure increases (u_0 increases and c_0=a_0 decreases as shown in Table 1), corresponding to an increase in spontaneous polarization. If there are no external electric fields present, the macrosopic polarization **P** will be given by the summation of the spontaneous polarization $\mathbf{P_{SP}}$ in the equilibrium lattice and the strain-induced piezoelectric polarization $\mathbf{P_{PE}}$, given as $\mathbf{P} = \mathbf{P_{SP}} + \mathbf{P_{PE}}$ [8].

Most growth of heterostructures, epitaxial films, and standard bulk materials is carried out along the (0001) axis, hence polarizations along this axis will be considered. The polarity determines the direction of the spontaneous polarization which is given by $\mathbf{P_{SP}} = \mathbf{P_{SP}}\mathbf{z}$ along the *c-axis*. Both the polarity and whether compressive or tensile strain is applied to the material determine the direction of the piezoelectric polarization [9].

The piezoelectric tensor, obtained from the differentiation of the polarization with respect to strain, is the starting point for the quantitative study of piezoelectric polarization. The displacement vector in a dielectric is represented as

$$\boldsymbol{D} = \epsilon \boldsymbol{E} + \boldsymbol{P} \tag{2.2}$$

where **E** is the electric field vector and **P** is the polarization vector. When only the piezoelectricity is considered the polarization vector is represented as

$$\boldsymbol{P} = d \cdot T \tag{2.3}$$

where d is the piezoelectric tensor and T is the stress tensor. Due to the symmetry of the wurtzite structure, only three of the components of d are independent, given by e_{15}, e_{31}, and e_{33}, where the index of 3 gives the direction of the c-axis [9]. From the piezoelectric coefficients, the piezoelectric polarization can be calculated as

$$P_{PE} = e_{33}\varepsilon_z + e_{31}(\varepsilon_x + \varepsilon_y) \tag{2.4}$$

The piezoelectric coefficients are given in Table 2.2. ε_z is the strain in the *c-axis* direction and is defined as $\varepsilon_z = (c - c_0)/c_0$. ε_x and ε_y are the in-plane strain and are assumed to be isotropic, given by $\varepsilon_x = \varepsilon_y = (a - a_0)/a_0$. a_0 and c_0 represent the equilibrium lattice parameter values. e_{15} is the third independent component of the piezoelectric tensor and represents the shear strain induced polarization [8].

Table 2.2 Spontaneous polarization, piezoelectric, dielectric constants and other electromechanical properties of AlN, GaN and InN [8], [14].

WURTZITE	**AlN**	**GaN**	**InN**
P_{SP} ($C \cdot m^{-2}$)	-0.090	-0.034	-0.042
e_{33} ($C \cdot m^{-2}$)	1.50	0.67	0.81
e_{31} ($C \cdot m^{-2}$)	-0.53	-0.34	-0.41
e_{15} ($C \cdot m^{-2}$)	-0.35	-0.17	-0.11
ε_{11}	9.0	9.5	
ε_{33}	10.7	10.4	
d_{31} ($pm \cdot V^{-1}$)	-1.9	-1.3	-3.3
	-2.1	-1.0	-3.5
d_{33} ($pm \cdot V^{-1}$)	5.4	2.7	9.3
		1.9	7.6
d_{15} ($pm \cdot V^{-1}$)	2.9	1.8	5.5
	3.6	3.1	
C_{11} (GPa)	496	367	223
		390	
C_{12} (GPa)	137	135	115
		145	
$C_{11} + C_{12}$ (GPa)	506	413	266
C_{13} (GPa)	94	68	70
	108	103	92
		106	
C_{33} (GPa)	377	354	205
	373	405	224
		396	
C_{44} (GPa)	116	95	48
		105	

The additional parameters relating to piezoelectricity in crystals and the relations of these parameters are visualized in Figure 2.4. The standardized method to calculate the fixed charge at a heterointerface is to focus on the direct piezoelectric effect and ignore the converse piezoelectric effect. From the figure it can be seen that it is possible to represent the piezoelectric polarization is several ways, in addition to the form involving the piezoelectric coefficients:

$$P_{PE} = \sum_{jk} d_{ijk}\sigma_{jk} = \sum_{jk} d_{ijk}\left(\sum_{lm} C_{jklm}\varepsilon_{lm}\right) = \sum_{lm} e_{ilm}\varepsilon_{lm} = \sum_{lm} e_{ilm}\left(\sum_{lm} S_{lmjk}\sigma_{jk}\right) \tag{2.5}$$

This representation also demonstrates the relationships between the variables and properties of piezoelectricity, i.e., the relationship between the piezoelectric constants ($\mathrm{e} = \mathrm{d} \cdot \mathrm{C}$), piezoelectric moduli ($\mathrm{d} = \mathrm{e} \cdot \mathrm{S}$), elastic constants (stiffness) C and elastic compliance ($\mathrm{S} = \mathrm{C}^{-1}$). The piezoelectric polarization $\mathbf{P_{PE}}$, electric field **E**, stress σ, and resulting strain ε are dependent on external conditions, thus can possess different forms. The crystal structure of the material determines the internal properties of the crystal, namely, the piezoelectric constants e, piezoelectric moduli d, compliance tensor S, and elastic constants C. The values of the piezoelectric and elastic constants of Group III nitrides is a source of considerable disagreement; some reported values for these properties is given in Table 2.2.

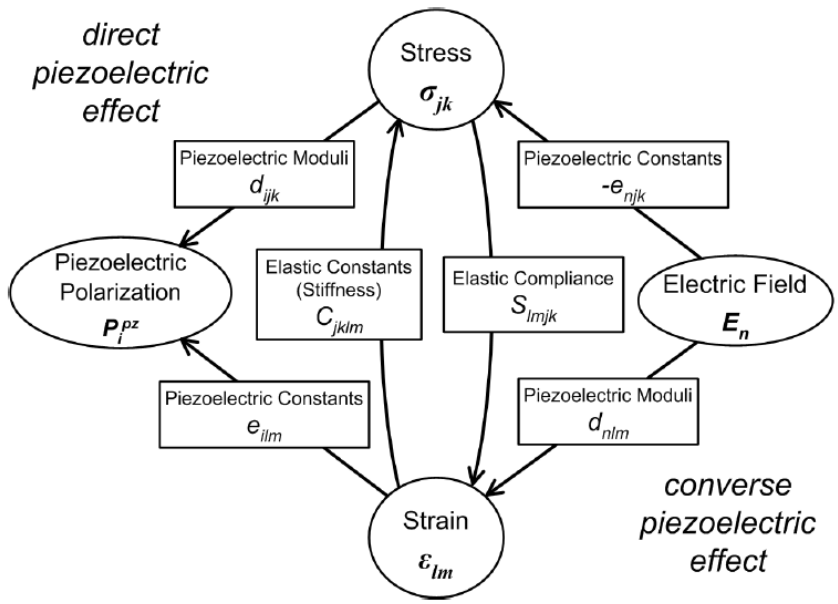


Figure 2.4 Schematic demonstrating the relations of the electrical and mechanical properties of a crystal [14].

For ternary alloys, the linear interpolation of piezoelectric and elastic constants of two binary compounds is used. Piezoelectric moduli depend on alloy composition nonlinearly, due to their dependency on the piezoelectric and elastic constants. Spontaneous polarization also relates nonlinearly to the alloy composition, as the internal parameter *u* has a nonlinear dependence on alloy composition. For Group III nitrides, the spontaneous polarization $P_{SP}(A_xB_{1-x}N)$ can be described using the parabolic model as [17]

$$P_{SP}(A_xB_{1-x}N) = xP_{SP}(AN) + (1-x)P_{SP}(BN) - b_{ABN}x(1-x) \qquad (2.6)$$

where $P_{SP}(AN)$ and $P_{SP}(BN)$ are the spontaneous polarization of the bulk binaries and b_{ABN} is the bowing parameter. The bowing parameter is defined as

$$b_{ABN} = 4P_{SP}(A_{0.50}B_{0.50}N) - 2P_{SP}(AN) - 2P_{SP}(BN) \qquad (2.7)$$

and takes on the values of 0.019 C/m^2 for AlGaN, 0.071 C/m^2 for InAlN, and 0.038 C/m^2 for InGaN [18].

2.3 Heterostructures and 2DEG

A heterojunction is defined as the interface that occurs between two dissimilar crystalline semiconductors having unequal bandgaps, as opposed to a homojunction, which refers to the junction between only one type of semiconductor with regions of different doping. A structure that employs a heterojunction is referred to as a heterostructure. One determining factor for the electrical behavior of a semiconductor is the bandgap energy; in a heterostructure both materials have different bandgap energies and the band structure obtained as a result determines the heterostructure device. Additionally, the difference in polarization between the two materials and the bound charge due to this difference effects the band diagram in III-Ns. The type of metal-semiconductor contact employed is another determining factor of the band structure. Ohmic contacts, non-rectifying metal-semiconductor contacts, have nearly no barrier between the metal and the semiconductor, therefore the device is supplied with carriers utilizing a low-resistance junction which is used to make up the source and drain terminals of the transistor. On the other hand, the gate contact, is made up of a rectifying metal-semiconductor contact referred to as a Schottky contact. A barrier defined by the difference of the work-function of the metal and the affinity of the semiconductor is present between the conduction band of the semiconductor and metal, which impacts the resulting band diagram of the device.

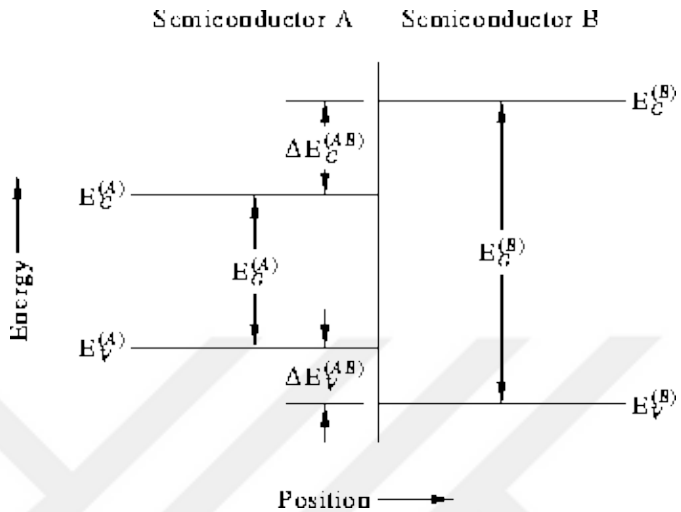


Figure 2.5 A heterojunction formed from two semiconductors with different bandgap energies [19].

In the heterostructure formed from two semiconductors, the bandgap energy of one semiconductors will be wider than the other, as shown in Figure 2.5. For the $Al_xGa_{1-x}N/GaN$ heterostructure, GaN has the smaller bandgap energy and $Al_xGa_{1-x}N$ has the wider bandgap energy. A bandgap discontinuity represented by ΔE_g will form at the interface of these two semiconductors. The bandgap discontinuity is given by the difference in the bandgap energy of the two semiconductors and is described by the conduction band offset and valence band offset as $\Delta E_g = \Delta E_c + \Delta E_v$. For the case of general semiconductors, the bands bend when one of the semiconductors contains doping. For III-Ns, due to the high polarization fields a high electron density arises at the interface without any additional doping. The polarization difference of the semiconductors produces a bound charge at the interface. For example, for an AlGaN/GaN heterostructure with growth in the (0001) direction, at the interface a positive charge and at the heterostructure surface a negative charge is produced.

The heterostructures that make up nitride devices generally consist of a ternary nitride alloy grown on bulk GaN. For the consideration of polarization in a heterostructure an $Al_xGa_{1-x}N/GaN$ heterostructure can be assumed without the loss of generality.

III-N compounds, that is, GaN, AlN, and InN, possess different unstrained lattice constants. When a ternary alloy is grown on a binary alloy its lattice must be strained to match the lattice constant of the binary alloy. If the *c-axis* of the crystal is referred to as the *z-axis* and the {0001} plane of the crystal is referred to as the *xy-plane*, the direction of growth of III-N semiconductor will be either parallel or antiparallel to the direction of the *c-axis*. The *c-axis* is orthogonal to the {0001} basal plane, so, the side of the hexagonal base *a* corresponds to the lattice constant that must match. The six-fold rotational symmetry of the wurtzite structure in the direction of the *c-axis* requires that the strain is identical in the *x* and *y* directions. In the basal plane the strain takes on the form of

$$\varepsilon_1 = \frac{a - a_0}{a_0} \tag{2.8}$$

where a_0 and a respectively refer to the unstrained/relaxed and strained lattice constants. The AlGaN layer thickness is on the order of nanometers in HEMT devices; the GaN layer thickness is usually several orders of magnitudes larger, therefore, it can be assumed that that the AlGaN layer is strained whereas the GaN layer is fully relaxed. Thus, in the equation for strain *a* will refer to the lattice constant of the unstrained GaN layer and a_0 will refer the lattice constant of the unstrained AlGaN layer that must fit to match the lattice constant. The strain can then be written as

$$\varepsilon_1 = \frac{a(0) - a(x)}{a(x)} \tag{2.9}$$

where *a(x)* refers to the lattice constant of unstrained $Al_xGa_{1-x}N$ and *x* refers to the Al concentration.

When the $Al_xGa_{1-x}N$ layer is being grown, forces are acting only on the topmost layer in the *xy-plane*; no shear stresses or strains, or forces acting in the *z-direction* are

present. The z-component of the polarization vector becomes the only component that does not vanish in the absence of shear strains, with the form of

$$P_{PE} = 2e_{31}\varepsilon_1 + e_{33}\varepsilon_3 \tag{2.10}$$

In the direction of growth, using the relationships between the strain, stress, and elastic stiffness, the expression of the strain along the polar axis (ε_3) and in the basal plane (ε_1) can be obtained as

$$\varepsilon_3 = -2\frac{C_{13}}{C_{33}}\varepsilon_1 \tag{2.11}$$

which can be combined with expression for piezoelectric polarization to obtain the piezoelectric polarization in the strained $Al_xGa_{1-x}N$ layer as

$$P_{PE} = 2\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right)\varepsilon_1 = 2d_{31}\left(C_{11} + C_{12} - 2\frac{{C_{13}}^2}{C_{33}}\right)\varepsilon_1 \tag{2.12}$$

In the three III-Ns used in electronic devices the piezoelectric polarization depends negatively on strain for all $Al_xIn_yGa_{1-x-y}N$, where $0 \leq x \leq 1$ and $0 \leq y \leq 1 - x$. Thus, negative (positive) piezoelectric polarization is caused by tensile (compressive) strain, that is, $\varepsilon_1 > 0$ ($\varepsilon_1 < 0$). This means that the piezoelectric polarization vector is parallel (antiparallel) to the spontaneous polarization, pointing towards the N-face (group III-face), so that the polarization is increased (reduced). Different scenarios of strain and the resulting polarization vectors are shown in Figure 2.6. The lattice constants of AlN (InN) are smaller (larger) than the lattice constants of GaN. Therefore, AlGaN on top of GaN has tensile strain, while InGaN on GaN has compressive strain. For InAlN on GaN the type of strain is dependent on the composition.

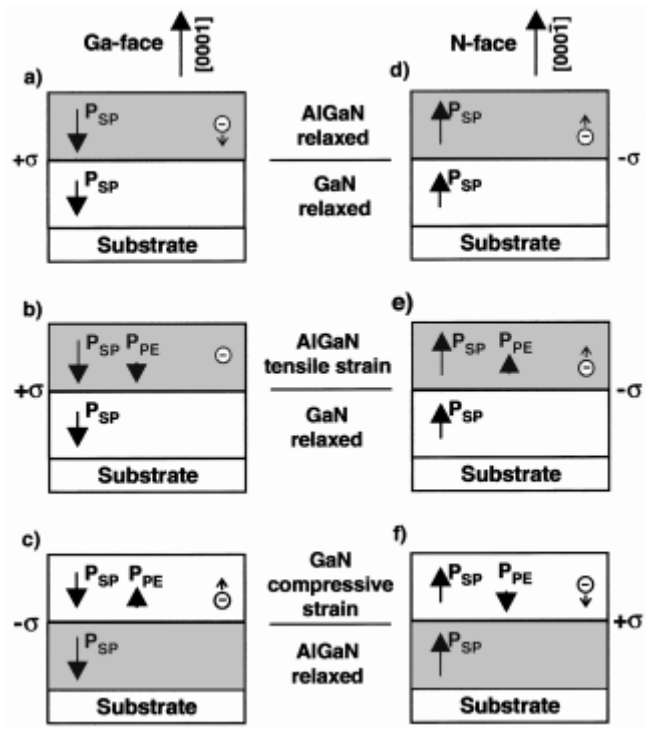


Figure 2.6 Schematic for Ga- and N-face strained and relaxed AlGaN/GaN heterostructures demonstrating the directions of the spontaneous and piezoelectric polarization and the corresponding polarization induced sheet charge densities [20].

The linear dependence of the piezoelectric polarization on the strain only holds for small strains. The nonlinearity of the piezoelectric polarization for binary alloys can be modeled by a second-order polynomial [17]:

$$
\begin{aligned}
P_{PE}^{AlN} &= -1.808\varepsilon_1 + 5.624{\varepsilon_1}^2 \quad for\ \varepsilon_1 < 0 \\
P_{PE}^{AlN} &= -1.808\varepsilon_1 - 7.8884{\varepsilon_1}^2 \quad for\ \varepsilon_1 > 0 \\
P_{PE}^{GaN} &= -0.918\varepsilon_1 + 9.541{\varepsilon_1}^2 \\
P_{PE}^{InN} &= -1.373\varepsilon_1 + 7.559{\varepsilon_1}^2
\end{aligned}
\tag{2.13}
$$

where ε_1 is the strain of the binary alloy in the basal plane in terms of alloy composition. The piezoelectric polarization for a ternary alloy can modeled as:

$$P_{PE}^{A_xB_{1-x}N} = -xP_{PE}^{AN}\big(\varepsilon(x)\big) + (1-x)P_{PE}^{BN}\big(\varepsilon(x)\big) \tag{2.14}$$

In a heterointerface there will be a discontinuity in the polarization. A bound charge density (ρ_b) is associated with changes in the polarization field (**P**) in space, which is given by

$$\rho_b = -\nabla \cdot \boldsymbol{P} \tag{2.15}$$

The direction of polarization is always along the *c-axis* for wurtzite III-nitrides and is orthogonal to the heterostructure interface. Therefore a bound sheet charge (σ_b) forms at the heterojunction, which is assumed to be abrupt and planar, that is given by [20]

$$\sigma_b = P_{tot,layer1} - P_{tot,layer2} = (P_{SP} + P_{PE})_{layer1} - (P_{SP} + P_{PE})_{layer2} \tag{2.16}$$

For a Ga-facing AlGaN/GaN interface the bound charge is found as

$$\begin{gathered} \sigma_b = P_{GaN} - P_{AlGaN} = P_{SP}^{GaN} + P_{PE}^{GaN} - P_{SP}^{AlGaN} - P_{PZ}^{AlGaN} \\ \sigma_b = P_{SP}(0) + P_{PE}(0) - P_{SP}(x) - P_{PE}(x) \end{gathered} \tag{2.17}$$

where x is the alloy composition of $Al_xGa_{1-x}N$. The piezoelectric polarization will be zero as the GaN layer is assumed to be relaxed, i.e., $P_{PE}(0) = 0$. All non-zero terms will be negative and the spontaneous polarization of AlGaN is greater than that of GaN, therefore a positive bound charge will exist at the interface of AlGaN/GaN. Typically in device applications, at the surface of AlGaN there is a material that does not possess polarization, such as air or a passivation layer, which leads to a negative bound charge at the device surface. For a N-face heterostructure the situation will be reversed, with a negative charge at the interface and a positive charge at the surface.

Theoretically, polarization charge is expected at the bottom GaN interface as well, however, due to screening effects in the GaN layer by impurities, defects and traps the induced electric field is presumed to be negligible [21]. The bound sheet charge can be calculated for any Al alloy composition by interpolating the values of the parameters of AlN and GaN.

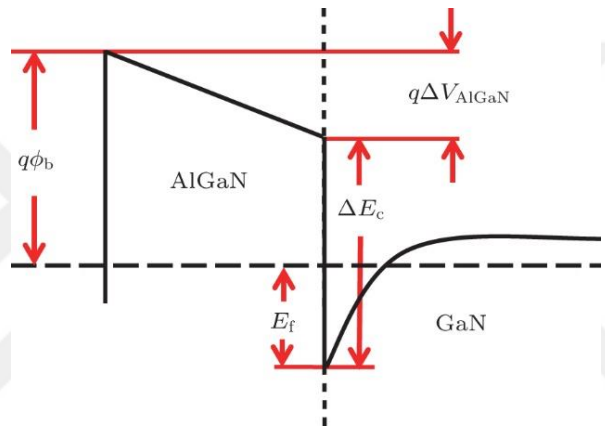


Figure 2.7 Schematic showing the conduction band of an AlGaN/GaN heterostructure [22].

The bound charge produced from the difference in polarization leads to a high electron sheet density n_s. Free electrons compensate the high positive polarization induced sheet charge. These electrons accumulated close to the interface in the GaN layer in a triangular shaped potential well, forming a two-dimensional electron gas (2DEG), in which the confined electrons are free to move parallel to the interface. The confined electrons have an increased mobility compared to electrons in the bulk. The maximum sheet carrier concentration is given by [20]

$$n_s(x) = \frac{+\sigma(x)}{e} - \left(\frac{\epsilon_0 \epsilon(x)}{de^2}\right)[e\phi_b(x) + E_F(x) - \Delta E_C(x)] \qquad (2.18)$$

where d represents the thickness of the $Al_xGa_{1-x}N$ barrier, $e\phi_b$ represents the Schottky barrier height of the gate contact, E_F represents the Fermi level with respect to the conduction band of GaN, and ΔE_C represents the conduction band offset at the

AlGaN/GaN interface, as shown in Figure 2.7. The following values are used in the calculation of the polarization induced sheet charge density:

dielectric constant:

$$\epsilon(x) = -0.5x + 9.5 \tag{2.19}$$

Schottky barrier height:

$$e\phi_b = (1.3x + 0.84)\ eV \tag{2.20}$$

Fermi energy:

$$E_F(x) = E_0(x) + \frac{\pi\hbar^2}{m^*(x)} n_s(x) \tag{2.21}$$

where $E_0(x)$ is the ground subband level of the 2DEG given by

$$E_0(x) = \left\{\frac{9\pi\hbar e^2}{8\varepsilon_0\sqrt{8m^*(x)}}\frac{n_s(x)}{\epsilon(x)}\right\}^{2/3} \tag{2.22}$$

with effective electron mass $m^*(x) \approx 0.22m_e$

band offset:

$$\Delta E_C = 0.7[E_g(x) - E_g(0)] \tag{2.23}$$

2.4 AlGaN/GaN HEMTs

The amplification or switching of electronic signals are the main purposes of a transistor. A Field Effect Transistor (FET) contains a source terminal, a drain terminal, and a channel through which current flows from the source and drain terminals (ohmic contacts). Modulation of the channel conductance is made possible

by an electric field perpendicular to the surface, which is produced with the application of a voltage between the source and gate terminals. In the High Electron Mobility Transistor (HEMT), a potential well is created by utilizing a heterostructure. The potential well is perpendicular to the heterointerface and contains confined electrons that are free to move in the direction parallel to the interface, which forms a 2DEG. Traditional HEMT devices were based on GaAs, however, spontaneous polarization does not exist in Arsenide III-Vs and the piezoelectric constants are smaller by an order of magnitude compared to the piezoelectric constants of nitride semiconductors, which makes doping necessary to induce a 2DEG. A 2DEG density around 2×10^{12} cm^{-2} can be achieved with conventional GaAs based HEMTs with doping, whereas for GaN based devices, 2DEG densities on the order of 10^{13} cm^{-2} can be achieved without any doping due to the high polarization properties.

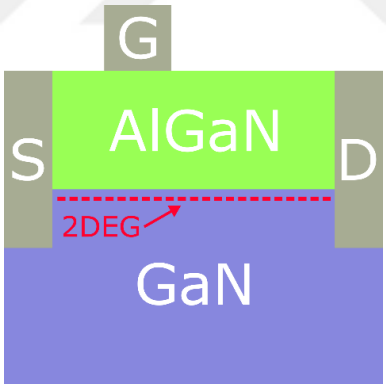


Figure 2.8 Schematic of an AlGaN/GaN high-electron-mobility transistor.

A schematic representation of an AlGaN/GaN HEMT is shown in Figure 2.8. The device consists of a source, drain, and asymmetrically placed gate terminal. High drain voltages can produce a high peak electric field at the drain side edge of the gate, hence, it is preferred to place the gate further away from the drain contact to minimize the electric field peak and maximize the obtainable breakdown voltage. However, an increased separation between the gate and drain leads to deterioration in the high

frequency performance of the devices, particularly in a reduction of the cut-off frequency.

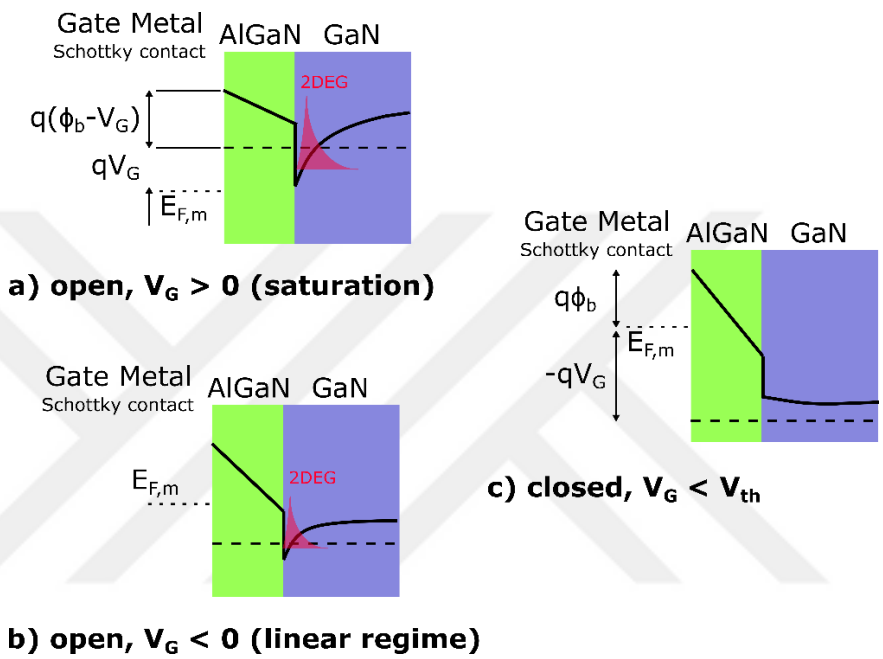


Figure 2.9 Operation modes of a normally-on AlGaN/GaN HEMT.

In HEMT devices the gate voltage V_G applied to the Schottky gate contact modulates the channel conductance. The gate voltage modifies the expression for the electron sheet density such that

$$n_s(x,d) = \frac{\sigma(x)}{e} - \left(\frac{\epsilon_0 \epsilon(x)}{de^2}\right)[e(\phi_b(x) - V_G) + E_F(x) - \Delta E_C(x)] \qquad (2.24)$$

The three possible modes of operation according the applied gate voltage are the off-mode, linear regime, and saturation regime. The conduction band diagrams for these cases are shown in Figure 2.9. In the off-mode the channel is closed and there are no free electrons to conduct current. In the linear regime, the gate voltage is close to the threshold voltage so the 2DEG density is small. In the saturation regime, the 2DEG density in the channel is high. GaN transistors require a negative gate voltage not to conduct current, making them depletion mode or normally-on devices.

2.5 InAlN/GaN HEMTs

AlGaN based HEMT devices have a limitation in drain-source current densities due to the tensile strain in the AlGaN barrier that ultimately leads to plastic relaxation for large Al contents above a critical thickness. InAlN/GaN heterostructures, compared to AlGaN/GaN heterostructures, have the advantages of higher 2DEG density as a result of higher spontaneous polarization fields, and less strain and crystal defects due to the lattice match between $In_{0.17}Al_{0.83}N$ and GaN [23]. Even when the piezoelectric polarization component vanishes due to the absence of strain, at the heterointerface a high polarization induced sheet charge density can be achieved. An InAlN barrier with about 14.5% indium content on GaN as thin as 6 nm can achieve a 2DEG density up to $1.7\pm0.1 \times 10^{13}$ cm^{-2} [24].

2.6 Normally-Off HEMTs

HEMTs are intrinsically normally-on devices due to the presence of the 2DEG at the heterointerface. In power electronics applications, however, normally-off operation is required for the simplification of driver circuitry and circuit safety reasons. Different approaches such as gate recess, fluorine treatment, InGaN cap, p-GaN or p-AlGaN gate, piezo-neutralization layer, and cascode HEMTs are available to achieve normally-off operation. The aim is to cause the depletion of the 2DEG in at least the gate region in the absence of an applied gate voltage. When a positive gate bias is applied the sheet carrier density should be able to be completely restored for optimum device operation in terms of maintaining R_{ON}, it is preferred that the depletion of the 2DEG channel is localized in the gate region.

Low access resistance, which requires normally-on access regions and a normally-off channel is needed for high performance normally-off HEMTs. As a consequence, conversion of the channel from normally-on to normally-off using post-epitaxy threshold voltage control techniques that can be applied locally is the preferred approach for normally-off HEMTs. Fluorine treatment, p-type gate, gate recess

combined with a MISHEMT structure, and the cascode configuration are the most studied approaches for normally-off operation. In this chapter, these four approaches will be studied. The fluorine treatment method consists of fluoride-based plasma treatment of the gate region in AlGaN/GaN HEMTs. The negatively charged fluorine ions can be effectively incorporated into the AlGaN barrier with the plasma treatment and lead to a positive shift the threshold voltage. In the p-type gate approach, a p-GaN (or p-AlGaN) layer is added under the gate contact. The p-type layer acts to raise the conduction band above the Fermi level, resulting in the depletion of the 2DEG channel by the p-n junction even when no external bias is applied. This method is utilized in commercially available normally-off GaN HEMT devices. In the recessed MISHEMT method the region under the gate contact region is etched and a gate dielectric is used. By reducing the 2DEG density only under the gate electrode the threshold voltage can be positively shifted with this structure. The depth of the recess etch can be used to control the gate threshold voltage. The MISHEMT configuration is combined with this approach to obtain lower gate leakage current. The fluorine implantation method has the advantages of low leakage current and controllability of the threshold voltage. The challenge of this method is the stability of the doped fluorine. The p-type gate method also has the advantage of controllability of the threshold voltage, also, it is a reliable method. The disadvantages are that the obtainable threshold voltages are relatively low and the gate leakage is larger. The recessed MISHEMT approach is advantageous due to its lower leakage current, lower ON resistance, and controllability of the threshold voltage. The challenges are damage caused by etching, stability of the semiconductor/insulator interface, and controllability of the recess depth, spacing, and uniformity [25]. The cascode configuration is a direct approach to obtaining normally-off operation in which a normally-on GaN transistor is connected with a normally-off Si MOSFET. The advantages of this approach are that a high threshold voltage is achievable and that the gate drive is compatible with that for Si devices. The disadvantages are that the

fabrication is costly and difficult to integrate and that there is limited driving speed [26].

2.6.1 Fluorine Implantation

One robust method of fabricating normally-off GaN transistors is fluorine implantation. A large positive threshold shift is observed when fluorine ions are incorporated into the gate region using a fluorine-based plasma. The intrinsic III-nitride crystal structure and the strong electronegativity of the fluorine element are the reason for the effectiveness of this technique. AlGaN/GaN heterostructures consist of a very tight lattice structure, with an in-plane lattice constant of around 3.2 Å. Implanted F ions are repelled by neighboring atoms (Al, Ga or N), and, due to the tight lattice structure, stabilize in interstitial sites. Being the most electronegative element among all chemical elements, the implanted F ions are able to capture a free electron, becoming a fixed negative charge, and thus modulating the local potential and depleting the 2DEG channel [27], as shown in Figure 2.10.

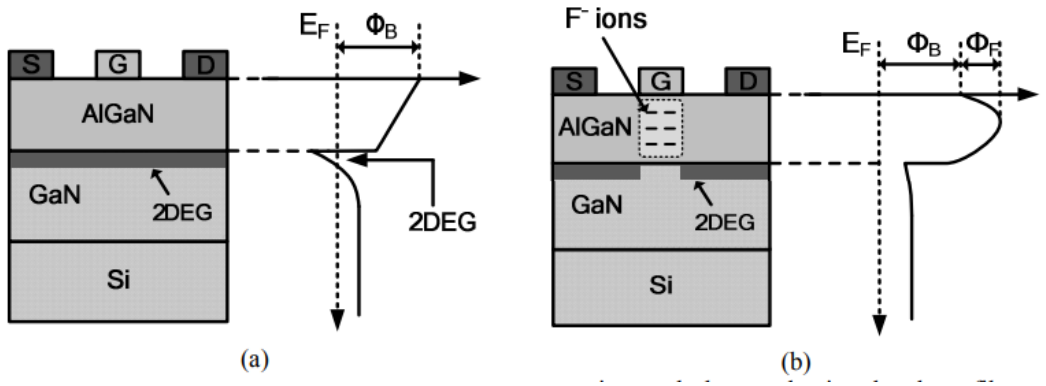


Figure 2.10 Cross sectional schematic and conduction band diagrams of a) normally-on and b) fluorine implanted normally-off AlGaN/GaN HEMTs [27].

The factors controlling the amount of threshold voltage shift are the implantation time and the RF plasma power. With an increase in treatment time, the positive shift in the threshold voltage also increases up to a point after which the obtainable positive

threshold voltage remains the same. The RF plasma power must be above a lower bound, dependent on the systems used, to be able to introduce a significant threshold voltage shift; however, this power must also be kept as low as possible to minimize the number of F ions that penetrate into the 2DEG channel region and plasma induced lattice damages [28]. The threshold voltage characteristics for an AlGaN/GaN HEMT devices treated with different CF_4 plasma power and durations are shown in Figure 2.11. Greater positive shift of V_{th} is possible with higher plasma powers and longer treatment durations. More fluorine ions implant into the barrier layer when the plasma time is increased, reducing the electron density in the channel, which shifts V_{th} in the positive direction. Increased plasma power leads to fluorine ions possessing a higher energy that reach depths closer to the 2DEG channel. The fluorine atoms can deplete the 2DEG more effectively the closer they are to the channel, and a greater shift in V_{th} is attained. However, ICP induced damages and the defects produced from this damage causes an increase in gate-leakage current [29].

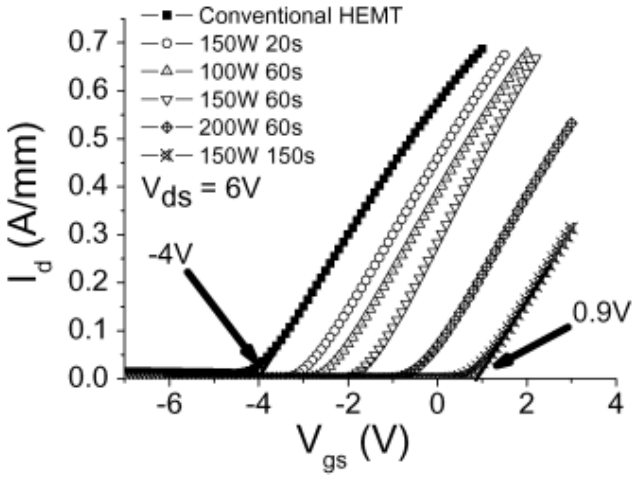


Figure 2.11 I_d-V_{gs} characteristics of fluorine treated AlGaN/GaN HEMT for different CF_4 plasma-treatment process parameters [29].

Annealing at various temperatures has been demonstrated to reduce plasma induced damages. Nonetheless, as a result of the nature of the implantation process, some

amount of F ions will be present in the channel that may behave like impurities and lead to a degradation of 2DEG mobility of up to 10-20% [27].

2.6.2 p-type Gate HEMTs

This approach incorporates a p-GaN (or p-AlGaN) layer on the heterostructure under the gate contact. The p-GaN layer depletes the 2DEG even when no applied gate bias is present by lifting up the band diagram. High 2DEG density is preserved in the access regions where the p-type layer is not present, hence low ON-resistance and high current density are achievable in addition to normally-off operation. The p-GaN gate method is utilized in commercially available normally-off GaN HEMT devices [30].

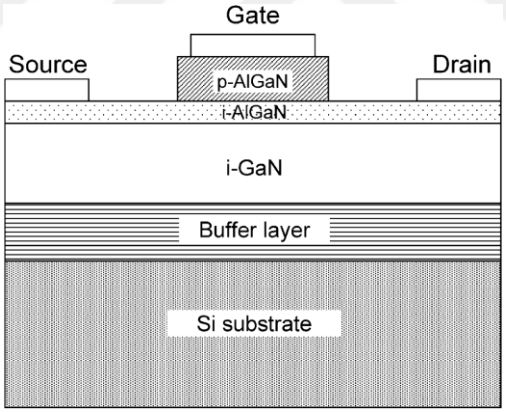


Figure 2.12 Cross sectional schematic of a p-type gate AlGaN/GaN HEMT device [31].

Figure 2.12 shows the schematic of the cross section of a p-AlGaN gate AlGaN/GaN HEMT. The high-potential barrier of the p-(Al)GaN depletes the 2DEG under the gate by lifting the conduction band above the Fermi level. When the gate bias is zero the channel under the gate is depleted fully, enabling normally-off operation, as demonstrated in Figure 2.13. The potential at the 2DEG controls the drain current and as the gate voltage is increased to reach the built-in voltage of the p-n junction making up the gate the 2DEG begins to form [31].

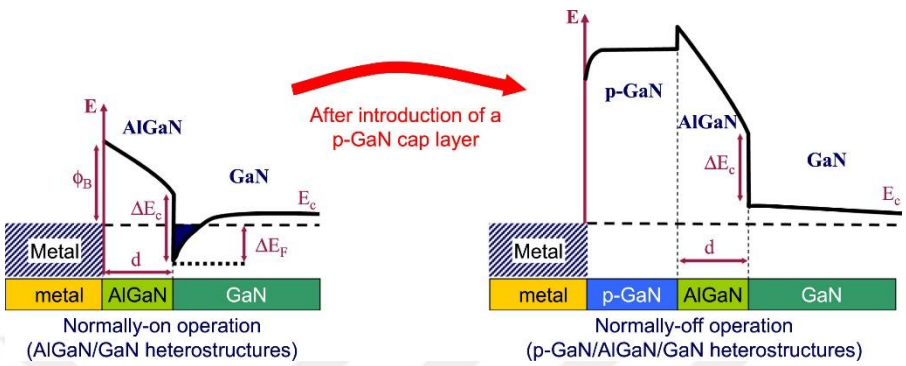


Figure 2.13 Schematic of the conduction band demonstrating the operation principle of the p-GaN gate normally-off HEMT [32].

The threshold voltage achievable with a p-type capping layer in GaN based devices depends on various heterostructure properties, namely, acceptor concentration of p-GaN, thickness and molar fraction of the barrier layer, and residual donor concentrations in the barrier and GaN channel layers. A p-type cap layer with high acceptor concentration is desired facilitate 2DEG depletion at $V_G = 0$. Magnesium doping is used to obtain p-GaN, typically achieving an acceptor concentration of about 3×10^{19} cm^{-3}. Higher p-GaN densities are not preferred since incorporation of the required amount of magnesium could deteriorate the crystal quality. In Figure 2.14 the conduction bands for two different Al-concentrations for a given barrier thickness and two different barrier thicknesses for a given Al-concentration in a p-GaN/AlGaN/GaN heterostructure are shown, demonstrating that the operation of the heterostructure can be either normally-on or normally-off depending on the choice of parameters. For a higher Al-content barrier layer, the p-GaN layer raises the conduction band increasing the threshold voltage, but is not sufficient for normally-off operation. A thinner AlGaN barrier thickness enables the conduction band to be raised above the Fermi level, forming a suitable heterostructure to obtain normally-off operation. Based on the barrier layer molar fraction and thickness there is a border seperating heterostructures appropriate for normally-off or normally-on operation [32].

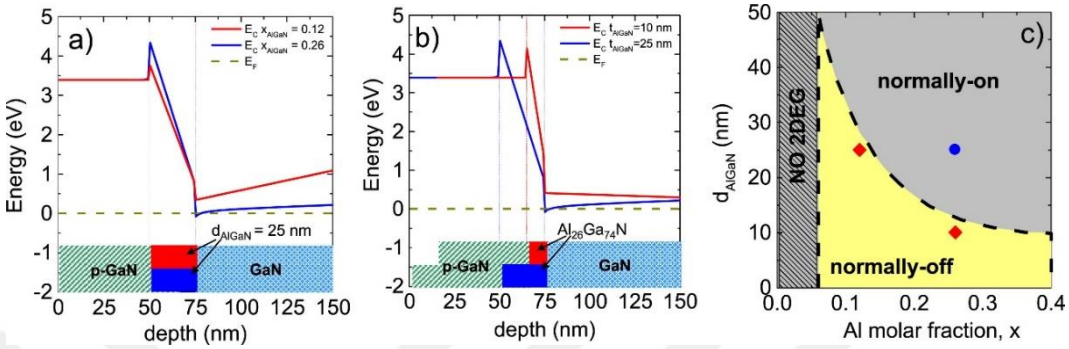


Figure 2.14 Simulated conduction band diagrams of a p-GaN/AlGaN/GaN heterostructure, for a) different values of Al-content, b) different values barrier thickness, and c) based on simulations, the border between normally-on and normally-off operation mode for different Al-contents and barrier thicknesses in p-GaN/AlGaN/GaN heterostructures [32].

2.6.3 Recessed MISHEMTs

In this method the region under the gate contact region is etched and additionally a gate dielectric can be used. The threshold voltage is increased with this structure by reducing the 2DEG density only under the gate electrode. Controlling the depth of the recess etch allows control of the threshold voltage. The tradeoff between the breakdown voltage characteristics and the on-resistance is maintained at the same level as normally-on HEMTs.

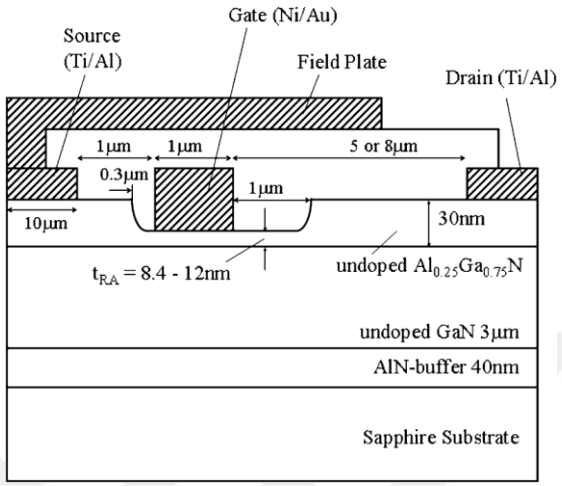


Figure 2.15 Cross sectional schematic of a recess gate AlGaN/GaN HEMT [33].

Figure 2.15 shows the cross sectional view of a gate recessed AlGaN/GaN HEMT device (with a source connected field plate, unrelated to normally-off operation). The 2DEG is selectively reduced in the gate region by performing an etch to thin the barrier in this region only. Reduction of the AlGaN thickness increases the threshold voltage. The 2DEG density is reduced in the gate region while it remains the same in other channel regions, leading to only a small increase in the on-resistance. The threshold voltage increases directly with increasing etch depth [33]. The AlGaN layer in the gate region can be removed completely for the complete removal of the inherent positive polarization charges in the gate region. A thin barrier layer (thickness < 1.5 nm) may be left to maintain the high mobility in the gate controlled channel for the purpose of low R_{on}, typically at the cost of a smaller positive V_{th}.

Gate recess used on its own leads to an increases in the ON-state gate leakage current and a decrease in gate voltage swing. To combat this, recessed normally-off devices are frequently combined with the metal-insulator-semiconductor (MIS) approach [34]. In this approach, the barrier layer is either partially or fully removed and replaced with an insulating dielectric layer to improve gate leakage currents. The MIS-gate additionally enables a large forward gate voltage swing [30].

2.6.4 Cascode Configuration

The cascode configuration achieves an effective normally-off high-voltage device by combining a normally-off high-voltage GaN HEMT with a low voltage Si MOSFET device, as shown schematically in Figure 2.16. The gate-source voltage of the GaN HEMT is connected to the drain-source voltage of the Si MOSFET.

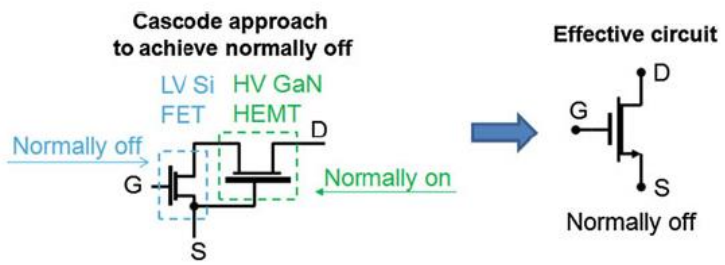


Figure 2.16 Schematic of the cascode normally-off GaN HEMT [35].

The operation of the GaN+Si cascode configuration is shown in Figure 2.17. At zero gate voltage, the Si MOSFET turns off leading to an increase in its drain to source voltage (V_{DS1}). The drain to source voltage of the Si HEMT equals the gate-source voltage (V_{GS2}) of the GaN HEMT, which turns off as the voltage becomes less than its threshold voltage. The HEMT achieves high voltage operation (>600 V) by blocking the high off-state voltage (V_{DS2}). The Si MOSFET turns on at a positive gate voltage ($>V_{TH1}$), which causes a reduction in V_{DS1}. V_{GS2} acquires a value close to zero; the gate to source voltage of the GaN HEMT becomes higher than its negative threshold voltage, thus the HEMT turns on. To be able to effectively turn off the GaN HEMT in all the different conditions the chosen Si MOSFET should have an off-state voltage that is more negative than the threshold voltage of the GaN HEMT [35].

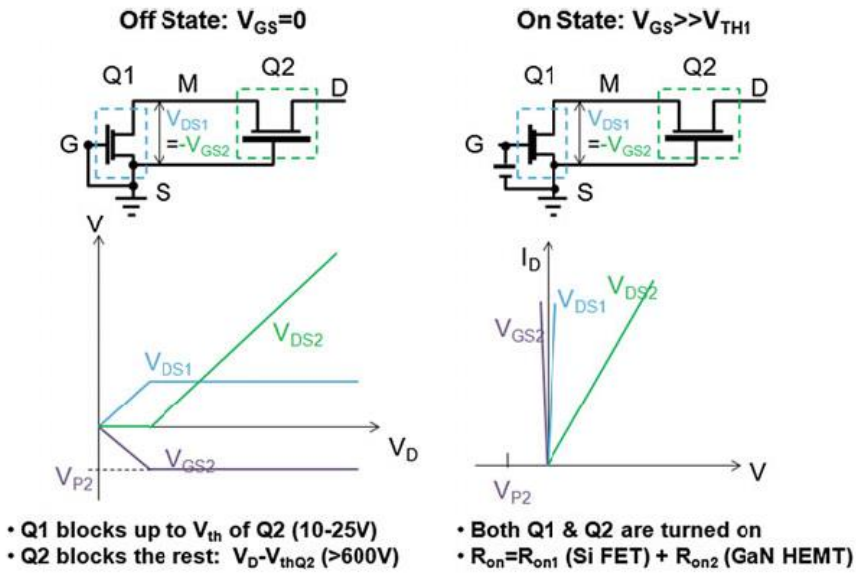


Figure 2.17 On and off operation of the cascode configuration where Q1 represents the Si MOSFET and Q2 represents the GaN HEMT [35].

Chapter 3

Simulation Methodology

3.1 Numerical Device Modelling

The simulation of the electrical response of semiconductor devices is made possible with physical models and numerical methods. Device simulations aim to describe the physical processes that occur inside device structures and to provide an understanding of the underlying physics. Semiconductor device simulation is classified as two parts: process simulation and device simulation. The fabrication process of semiconductor devices, for instance transistors, is modelled in semiconductor process simulations. Modelling the steps in a process flow to obtain the dopant and stress profiles is the main purpose of semiconductor process simulation. Device simulation consists of modelling device electrical characteristics. In device simulators the electrical characteristics are predicted for specified physical structures under specified bias conditions through the utilization of physically-based modelling. Physically-based modelling differs from empirical modelling, in which it is aimed to approximately fit existent data with analytic formulas, with minimum complexity and good accuracy. In physically-based modelling, DC, AC or transient modes of operation of a device is modelled by the approximation of the operation of the device onto a grid (either two or three dimensional) and the application a group of differential equations derived from Maxwell's equations, to simulate carrier transport through the structure. To carry out device simulation the physical structure is defined, the physical models are chosen, and the bias conditions to be simulated are specified. Physically-based simulations are advantageous in that they provide insight, are predictive, and are able to capture and visualize theoretical knowledge. The drawbacks are that relevant physics and numerical procedures must be incorporated into the simulation.

3.2 Silvaco Atlas Simulation Methodology

The Silvaco Atlas TCAD tool has been used in this thesis to carry out electrical simulations to study normally-off GaN HEMT devices. Physically-based two (2D) and three-dimensional (3D) simulation capabilities are provided with the Silvaco Atlas software. Solutions are produced for DC, AC small-signal, and transient modes through the application of a set of differential equations derived from Maxwell's equation onto a two or three dimensional grid that approximates the operation of a device [36].

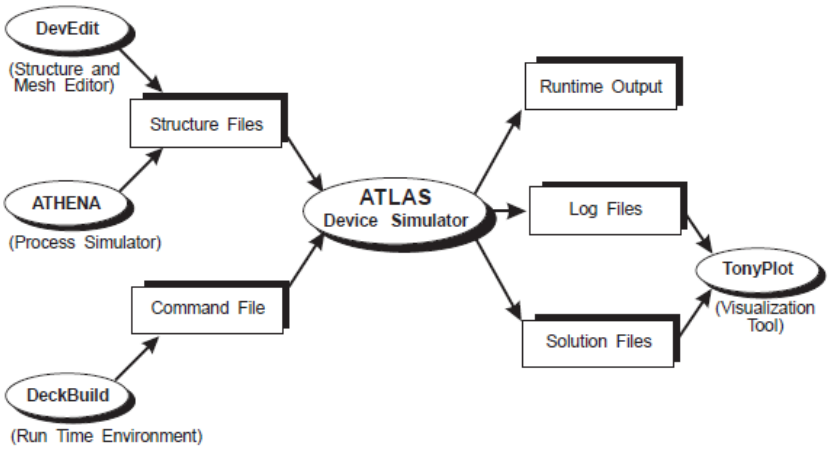


Figure 3.1 Inputs and outputs of the Atlas device simulator [36].

The inputs and outputs of the Atlas simulator are shown in Figure 3.1. A file containing the commands to be executed by Atlas and a file defining the structure to be simulated are the required inputs. In turn, Atlas will produce run-time output showing the progress as the simulation proceeds and any error or warning messages, a log file containing the produced terminal voltages and currents, and a solution file storing the 2D and 3D data related to the solution variable values inside the device for given bias points.

Group	Statements
1. Structure Specification	MESH REGION ELECTRODE DOPING
2. Material Models Specification	MATERIAL MODELS CONTACT INTERFACE
3. Numerical Method Selection	METHOD
4. Solution Specification	LOG SOLVE LOAD SAVE
5. Results Analysis	EXTRACT TONYPLOT

Figure 3.2 Atlas command groups and principal statements of each group [36].

In the Atlas input, possible statements are divided into five groups that must appear in a specified order, as shown in Figure 3.2. The device structure to be simulated must first be defined using the mesh, region, electrode, and doping statements, in order. The material definitions and physical models to be used must be specified and a numerical method must be selected. Finally statements regarding the solutions to be logged and displayed must be included.

3.3 Basic Semiconductor Equations

A mathematical model called Stanford University PISCES-II, which has been used for the derivation of other device simulators, has been developed as a result of years of device physics research. Stanford University PISCES-II consists of a set of fundamental equations linking the electrostatic potential and the carriers together within a simulation domain and can be used to operate on any semiconductor device [37]. These equations consist of Poisson's Equation, the continuity equations, and the transport equations and have been derived from Maxwell's equations. Any general purpose device simulator solves these equations. Poisson's equation relates changes in electrostatic potential and local charge densities. The continuity equations and the

transport equations define in which manner electron densities and hole densities vary in response to transport properties, generation processes, and recombination processes. To enable to application of these equations to the finite grid used in the representation of the simulation domain, the equations are discretized.

3.3.1 Poisson's Equation

The relationship of variations in electrostatic potential and the space charge density is described by Poisson's Equation as follows

$$div(\epsilon \nabla \psi) = -\rho \tag{3.1}$$

The electrostatic potential is represented by ψ, the local permittivity is given by ϵ, and the local space charge density is given by ρ. There are several possible definitions of the reference potential; in Atlas the Fermi potential ψ_i is used as the reference. All mobile and fixed charges, including electrons, holes, and ionized impurities compose the local space charge density. The gradient of the potential gives the electric field:

$$\boldsymbol{E} = -\nabla \Psi \tag{3.2}$$

3.3.2 Continuity Equations

The following equations define the continuity equations for electrons and holes

$$\begin{aligned} \frac{\partial n}{\partial t} &= \frac{1}{q} div \boldsymbol{J}_n + G_n - R_n \\ \frac{\partial p}{\partial t} &= \frac{1}{q} div \boldsymbol{J}_p + G_p - R_p \end{aligned} \tag{3.3}$$

where n and p are the electron and hole concentrations. $\boldsymbol{J}$ is the current density, G is the generation rate, and R is the recombination rate, where the subscripts n and p in the equations refer to electrons and holes, respectively. q refers to the magnitude of the electric charge carried by a single electron.

In Atlas the continuity equations for both electrons and holes are included by default, however, in some cases solving for only one of the carriers is sufficient, hence, it is possible to selectively turn off the one of the continuity equations.

3.3.3 Transport Equations

Poisson's Equations and the continuity equations provide the general framework for device simulation. For the specification of particular physical models for $\boldsymbol{J}_n$, $\boldsymbol{J}_p$, G_n, G_p, R_n, and R_p secondary equations are required. The charge transport models, or current density equations are obtained as a result of approximations and simplifications of the Boltzmann Transport Equation. According to the assumptions made numerous different transport models may be obtained such as the drift-diffusion model, the hydrodynamic model, or the Energy Balance Transport Model. The chosen charge transport model is a major influence in the choice of generation and recombination models. The simplest charge transport model is the drift-diffusion model as apart from ψ, n, and p, no additional independent variables are introduced. According to Boltzmann transport theory based derivations, a drift-diffusion model can approximate the current densities in the continuity equations. The current densities are expressed in terms of electron and hole mobilities and quasi-Fermi levels. Two Boltzmann approximations are used to link these to the carrier concentrations and the potential. The conventional form of the drift-diffusion equations is given as

$$\begin{aligned} \boldsymbol{J}_n &= qn\mu_n \boldsymbol{E}_n + qD_n \nabla n \\ \boldsymbol{J}_p &= qp\mu_p \boldsymbol{E}_p - qD_p \nabla \mathrm{p} \end{aligned} \tag{3.4}$$

where n and p are the electron and hole concentrations, μ is the mobility, $\boldsymbol{E}$ is the effective electric field, and D is the diffusion constant, where the subscripts n and p refer to electrons and holes, respectively.

The drift-diffusion model was sufficient for almost all technologically feasible devices until recently, however, is becoming less accurate for decreasing feature sizes. For the simulation of deep submicron devices more advanced energy balance and hydrodynamic models can be preferred.

3.4 Silvaco Physical Models

The physical models to be used by Atlas during device simulation must be chosen. The physical models are divided into five groups: mobility, recombination, carrier statistics, impact ionization, and tunneling. The models used in this thesis will be briefly explained in this section.

3.4.1 Mobility Models

Electrons and holes are accelerated by electric fields, but they undergo a loss of momentum caused by of various scattering processes, such as lattice vibrations (phonons), impurity ions, material imperfections, or other carriers or surfaces. These microscopic phenomena manifest as local electric field, doping concentration, lattice temperature, etc. dependent macroscopic mobilities. Mobility modeling can be grouped into four, namely, low-field, high field, bulk semiconductors and inversion regions. Low electric field carriers and the lattice are almost in equilibrium and the mobility is characterized by a low-field value ($\mu_{n0,p0}$). This low-field value depends on phonon and impurity scattering, which have decreasing effects on the low-field mobility.

As a low field mobility model, the Albrecht Model is used. The Albrecht Model develops transport parameters for electron conduction in GaN from electron transport Monte Carlo simulations, based on the analytical representation of the lowest conduction bands of wurtzite bulk GaN [38]. The mobility is a function of lattice temperature and doping, given by

$$\frac{1}{\mu(N,T_L)} = \frac{AN.ALBRCT \cdot N}{N0N.ALBRCT}\left(\frac{T_L}{T0N.ALBRCT}\right)^{-3/2} ln\left[1 + 3\left(\frac{T_L}{T0N.ALBRCT}\right)^2\left(\frac{N}{N0N.ALBRCT}\right)^{-2/3}\right] + BN.ALBRCT\left(\frac{T_L}{T0N.ALBRCT}\right)^{3/2} + \frac{CN.ALBRCT}{e^{T1N.ALBRCT/T_L} - 1} \quad (3.5)$$

where N represents the total doping concentration and T_L represents the lattice temperature. The remaining variables are user-specifiable parameters. A similar expression applies for holes. This model is called *albrct* for short in Atlas.

3.4.2 Recombination Models

If a semiconductor material is disturbed from equilibrium, it will attempt to return to equilibrium through carrier generation and recombination processes. A steady state balance given by

$$n_0 p_0 = n_i^2 \quad (3.6)$$

exists for a homogeneously doped semiconductor with equilibrium carrier concentrations of n_0 and p_0. However, semiconductor materials are continuously undergoing excitations whereby the carrier concentrations n and p are disturbed from their equilibrium values. If light shines on a p-type semiconductor, for example, electron-hole pairs will be generated which disturbs the minority carrier concentration, resulting in a net recombination in an attempt to return to equilibrium. Generation-recombination causing processes are grouped into six: photon transitions, phonon transitions, surface recombination, Auger transitions, impact ionization, and tunneling.

Shockley-Read-Hall (SRH) Recombination

The Shockley-Read-Hall Recombination process, process first derived by Shockley and Read [39] and then by Hall [40], is a two-step that analyzes the recombination of electrons and holes in semiconductors with a model in which the mechanism of trapping results in recombination, such that traps or defects within the semiconductor bandgap lead to phonon transitions. It is assumed that the energy level of the trap in the energy gap is such that its charge can take on either of two values that differ by one electronic charge. The following equation is models the Shockley-Read-Hall recombination:

$$R_{SRH} = \frac{pn - n_{ie}^2}{TAUP0[n + n_{ie}e^{ETRAP/kT_L}] + TAUN0[p + n_{ie}e^{-ETRAP/kT_L}]} \tag{3.7}$$

ETRAP represents the difference of the trap energy and intrinsic Fermi level, the lattice temperature in Kelvin is represented by T_L, and electron and hole lifetimes are represented by *TAUN0* and *TAUP0*. The Shockley-Read-Hall Recombination model is activated through the *srh* statement.

SRH Concentration-Dependent Lifetime Model

In the SRH recombination model the carrier lifetimes are constant; the constant carrier lifetimes can be expressed as a function of impurity concentration as [41-43]

$$R_{SRH} = \frac{pn - n_{ie}^2}{\tau_p[n + n_{ie}e^{ETRAP/kT_L}] + \tau_n[p + n_{ie}e^{-ETRAP/kT_L}]} \tag{3.8}$$

where the concentration dependent lifetimes are given as

$$\tau_n = \frac{TAUN0}{AN + BN\left(\frac{N_{total}}{NSRHN}\right) + CN\left(\frac{N_{total}}{NSRHN}\right)^{EN}} \tag{3.9}$$

$$\tau_p = \frac{TAUP0}{AP + BP\left(\frac{N_{total}}{NSRHP}\right) + CP\left(\frac{N_{total}}{NSRHP}\right)^{EP}}$$

N refers to the total local impurity concentration and the remaining parameters are user definable parameters. This model is shortly referred to as *consrh*.

<u>Auger Recombination</u>

Auger generation/recombination processes involve three particle transitions in which either the capture or emission of a mobile carrier occurs. The particles involved are either two holes and an electron or two electrons and a hole. The underlying physics partial processes involved in Auger recombination are yet unclear and only more or less qualitatively understood [44]. Auger recombination can be expressed as

$$R_{Auger} = AUGN(pn^2 - nn_{ie}^2) + AUGP(np^2 - pn_{ie}^2) \tag{3.10}$$

where *AUGN* and *AUGP* are user definable parameters. To activate this model the statement *auger* should be used.

3.4.3 Carrier Statistics Models

For a temperature T_L, electrons in a semiconductor lattice at thermal equilibrium obey Fermi-Dirac statistics. The probability *f(E)* of an available electron state with a given energy *E* to be filled with an electron is given by

$$f(E) = \frac{1}{1 + e^{\frac{E - E_F}{kT_L}}} \tag{3.11}$$

where E_F is the Fermi level and *k* is Boltzmann's constant.

An approximation of this expression can be given as

$$f(E) = e^{\frac{E-E_F}{kT_L}} \tag{3.12}$$

in the limit where $E - E_F >> kT_L$.

Statistics based on the simplified form are called Boltzmann statistics. In semiconductor device theory, using Boltzmann statistics is typically justified as it simplifies calculations compared to using Fermi-Dirac statistics. Nevertheless, in order to model certain properties of very highly doped semiconductors Fermi-Dirac statistics are necessary. This model is called *fermi* shortly.

3.4.4 Polarization in Wurtzite Materials

Polarization modeling is one of the most critical aspects in the simulation of GaN based devices. The polarization, composed of spontaneous polarization (P_{sp}) and piezoelectric polarization (P_{pi}) components, is calculated automatically. The total polarization P_t is expressed

$$P_t = PSP + P_{pi} \tag{3.13}$$

where *PSP* is a user definable parameter specifying the total spontaneous polarization. The piezoelectric polarization is given by

$$P_{pi} = 2\frac{a_s - a_0}{a_0}\left(E31 - \frac{C13}{C33}E33\right) \tag{3.14}$$

where *E31* and *E33* represent the piezoelectric constants, and *C13* and *C33* represent the elastic constants, all user specifiable. a_0, which can also be specified, represents the lattice constant of the material layer in consideration and a_s represents the mean value of the lattice constants of the layers above and below the layer in consideration. A positive and negative fixed charge placed at the top and bottom of the layer in

question is used to model the polarization. The *POLAR.SCALE* parameter can be specified to modify the magnitude of this charge, which is multiplied by the total polarization to obtain the applied charge.

3.5 Simulation Studies

Typically, device simulation begins with calibration of the simulator to reproduce the measured IV characteristics or other dependences of a real device. In this thesis, the aim of the simulation work was to model the conduction band diagrams of various normally-off structures and gain insight into the threshold voltage ranges achievable with these structures. To this extent, a detailed calibration procedure was not carried out and the simulations were calibrated to typical 2DEG densities in the literature, the simplest forms of the epitaxial structures were used, and ideal devices were assumed (e.g. self-heating effects were not taken in account).

Various parametric simulations were carried out for p-GaN gate InAlN/GaN HEMTs and recessed AlGaN/GaN MIS-HEMTs, the results are presented in this section.

3.5.1 p-GaN Gate InAlN HEMTs Simulations

Conduction band and threshold voltage simulations were carried out for a p-GaN gate InAlN/GaN HEMT. The base parameters used for the simulation are shown in Figure 3.3. A simplified epitaxial structure consisting of 20 nm p-GaN with $N_A = 3\times10^{17}$ cm^{-3}, an InAlN barrier layer, and 1.5 µm GaN channel layer was used and the interface charge was calibrated to be 2×10^{13} cm^{-2} for an InAlN barrier thickness of 8 nm. The drain to source distance L_{ds} was taken 6 µm, the gate to source distance L_{gs} was taken as 2 µm, and the gate width L_g was taken as 2 µm. The source and drain contacts were set to be ohmic contacts by defining a high concentration n-type doping and the gate contact was set to be Schottky. The *consrh* model is used to account for the doping of the p-type layer. The *albrct* mobility model is used with separate definitions for electrons and holes for the same purpose. The conduction bands and I_D vs V_G characteristics are simulated for various different epitaxial

parameters. The threshold voltages are extracted as the linear extrapolation at maximum transconductance.

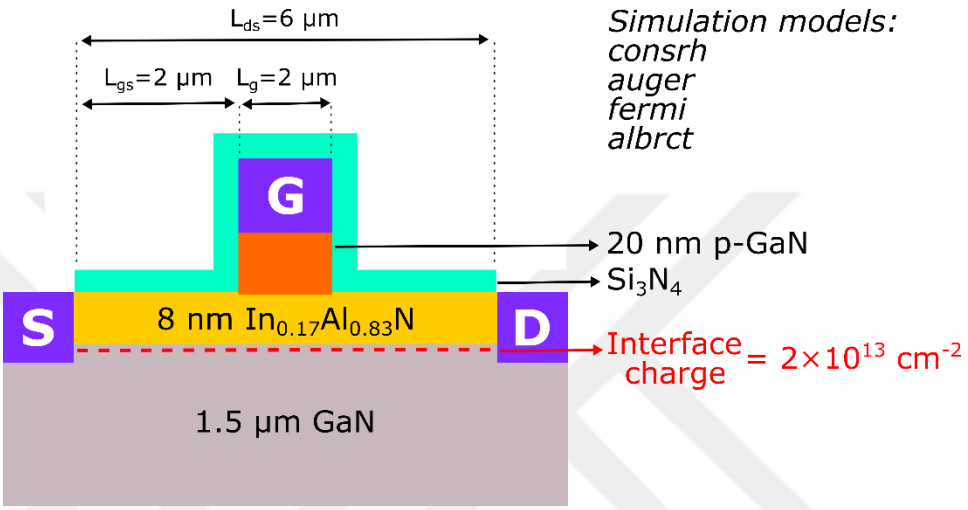


Figure 3.3 Schematic demonstrating the base parameters used in the simulations for p-GaN gate InAlN/GaN HEMT structures.

The first parameter studied is the InAlN barrier thickness. The thicknesses used are 4 nm, 6 nm, 8 nm, and 10 nm. The simulated conduction band and I_D vs V_G characteristics are shown in Figure 3.4 and Figure 3.5, respectively. For and barrier thickness of 10 nm InAlN some 2DEG still forms even with the p-GaN present. As the barrier thickness decreases, the conduction band can be lifted further above the Fermi level and begins to form with positive biasing of the gate contact. Thus the threshold voltage increases as the barrier layer thickness decreases and this increase is observed to be non-linear. Also, a tradeoff between the threshold voltage and the drain current density is observed; as the barrier layer thickness decreases higher threshold voltages can be obtained but this comes with a decrease in the achievable drain current density.

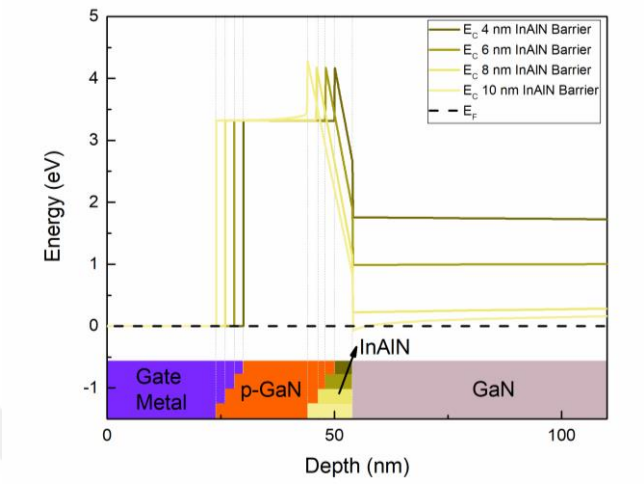


Figure 3.4 Simulated conduction band for increasing InAlN barrier thicknesses for the p-GaN/InAlN/GaN structure.

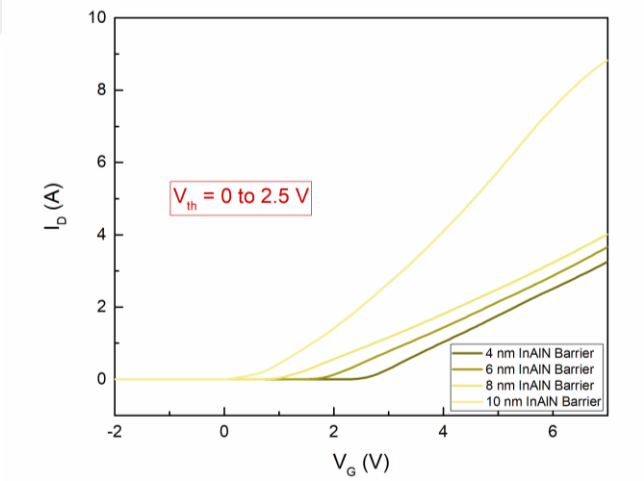


Figure 3.5 Simulated I_D vs V_G characteristic for increasing InAlN barrier thicknesses for the p-GaN/InAlN/GaN structure.

An AlGaN buffer or back-barrier is often used to further increase the threshold voltage in normally-off structures. The AlGaN buffer increases the threshold voltage by acting as a virtual p-type doping and also has the advantage of mitigating the buffer leakage current by providing effective confinement of the electrons in the 2DEG region [45]. A simulation comparing the structure without and with an AlGaN buffer

is carried out and the resulting energy bands are shown in Figure 3.6. For the same p-GaN and InAlN parameters, the AlGaN buffer results in a conduction band that is lifted up further in the gate region, indicating a higher threshold voltage. In the access region, the 2DEG forms as usual for both structures.

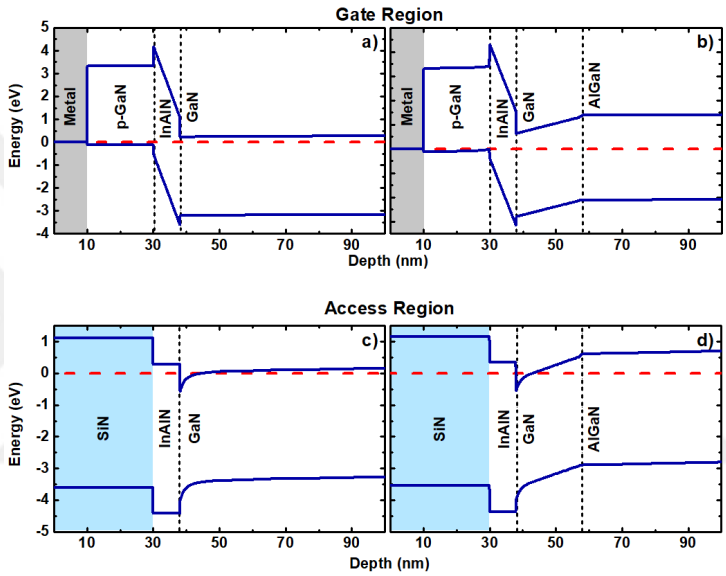


Figure 3.6 Comparison of simulated energy band diagrams for the p-GaN/InAlN/GaN and p-GaN/InAlN/GaN/AlGaN structures in the gate region (a and b) and in the access region (c and d).

Various parameters of the p-GaN/InAlN/GaN/AlGaN heterostructure are investigated for a constant InAlN barrier thickness of 8 nm. The first parameter studied is the Al-content of the AlGaN buffer. The obtained simulation results are shown in Figure 3.7 and Figure 3.8. It is observed that as the concentration of aluminum in the AlGaN buffer increases the conduction band is lifted higher up, owing to the increasing bandgap energy of AlGaN. Thereby, the threshold voltages that are achieved are higher than those that can be achieved without the AlGaN buffer. For the p-GaN/InAlN/GaN structure a 4 nm InAlN barrier is required to achieve a threshold voltage of 2.5 V, whereas this threshold voltage can be achieved with an

8 nm InAlN barrier with an $Al_{0.15}Ga_{0.85}N$ buffer, which may be preferable in terms of epitaxial growth due to difficulties associated with growing thin layers uniformly.

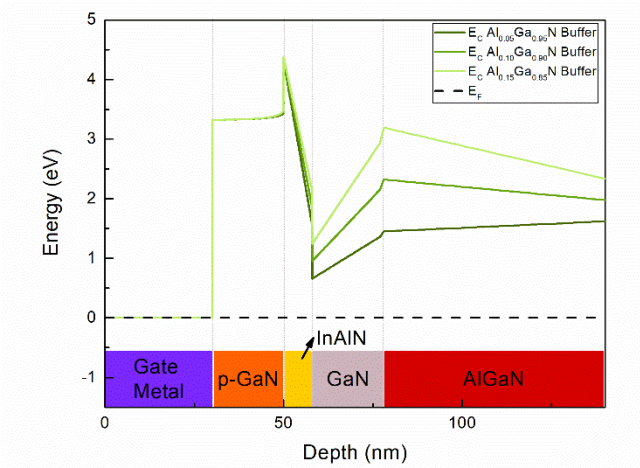


Figure 3.7 Simulated conduction band for increasing AlGaN buffer concentrations for the p-GaN/InAlN/GaN/AlGaN structure.

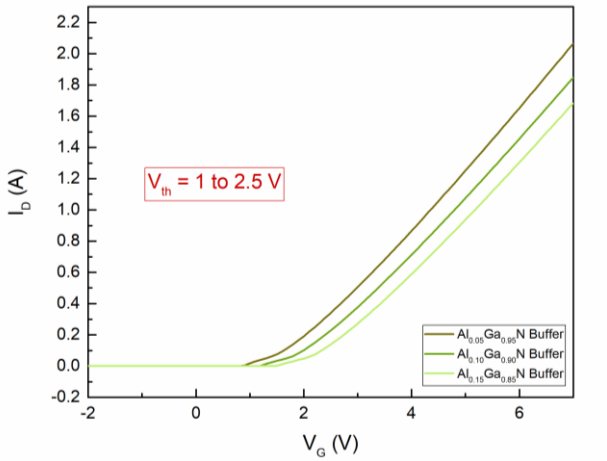


Figure 3.8 Simulated I_D vs V_G characteristic for increasing AlGaN buffer concentrations for the p-GaN/InAlN/GaN/AlGaN structure.

The effect of the thickness of the AlGaN buffer is also simulated and the results are shown in Figure 3.9 and Figure 3.10. It is observed that increasing the AlGaN buffer thickness leads to an increase in the conduction band notch between GaN/AlGaN

which may provide better confinement for electrons leading to decreased leakage. However, the change in the conduction band at the InAlN/GaN interface is minimal, leading to no significant effect on the threshold voltage.

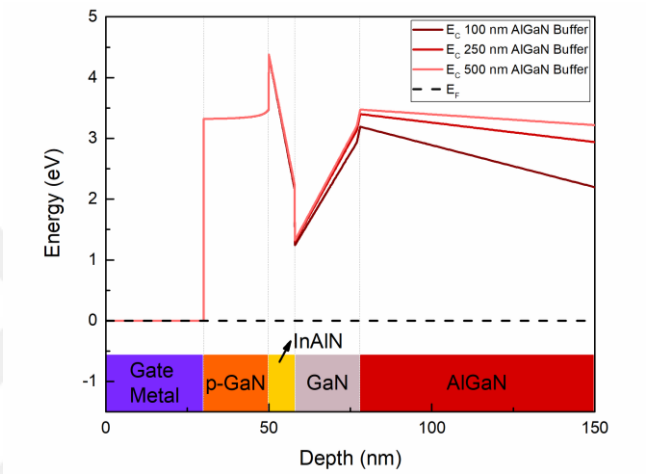


Figure 3.9 Simulated conduction band for increasing AlGaN buffer thicknesses for the p-GaN/InAlN/GaN/AlGaN structure.

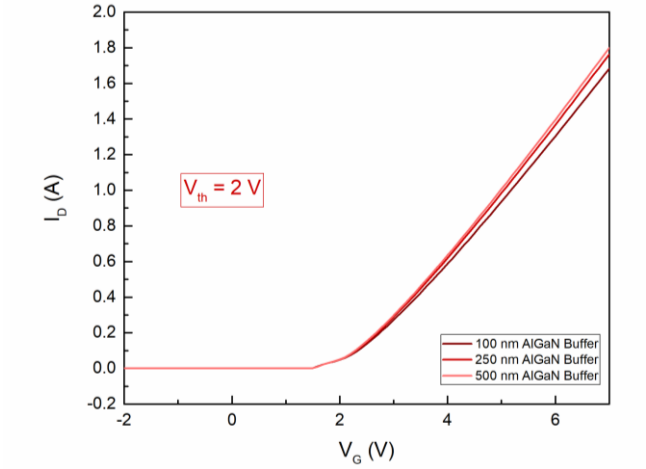


Figure 3.10 Simulated I_D vs V_G characteristic for increasing AlGaN buffer thicknesses for the p-GaN/InAlN/GaN/AlGaN structure.

The final parameter investigated for the p-GaN/InAlN/GaN/AlGaN structure is the thickness of the GaN channel layer. The obtained conduction band and I_D vs V_G

diagrams are given in Figure 3.11 and Figure 3.12. It is observed that as the thickness of the GaN channel decreases the conduction band at the InAlN/GaN interface is lifted leading to higher threshold voltage, but the conduction band notch between GaN/AlGaN decreases leading to poorer confinement of electrons. Thus there is a tradeoff between increasing the threshold voltage and decreasing buffer leakage.

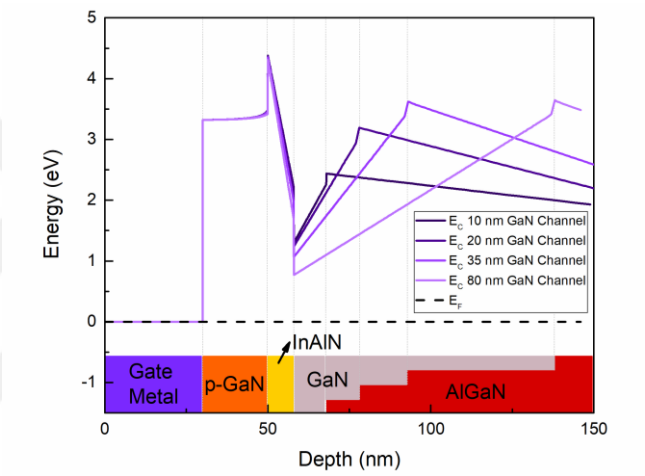


Figure 3.11 Simulated conduction band for increasing GaN channel thicknesses for the p-GaN/InAlN/GaN/AlGaN structure.

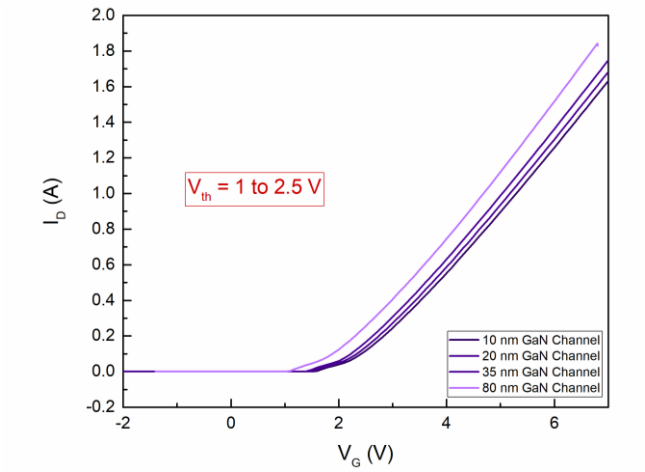


Figure 3.12 Simulated I_D vs V_G characteristic for increasing GaN channel thicknesses for the p-GaN/InAlN/GaN/AlGaN structure.

3.5.2 Recessed MIS-HEMTs Simulations

Conduction band and threshold voltage simulations were also carried out for an AlGaN/GaN MIS-HEMT. The base parameters used for the simulation are shown in Figure 3.13. A simplified epitaxial structure consisting of an AlGaN barrier layer, and 1.2 µm GaN channel layer was used and the interface charge was calibrated to be 1×10^{13} cm^{-2} for an AlGaN barrier thickness of 25 nm. The drain to source distance L_{ds} was taken 9 µm, the gate to source distance L_{gs} was taken as 2 µm, and the gate width L_g was taken as 2 µm. The source and drain contacts were set to be ohmic contacts by defining a high concentration n-type doping and the gate contact was set to be Schottky with a workfunction of 5.5 eV. The *srh*, *Fermi*, and *albrct* models are used. The conduction bands and I_D vs V_G characteristics are simulated for various recess depths and gate dielectrics and the effects of fluorine treatment are modelled. The threshold voltages are extracted as the linear extrapolation at maximum transconductance.

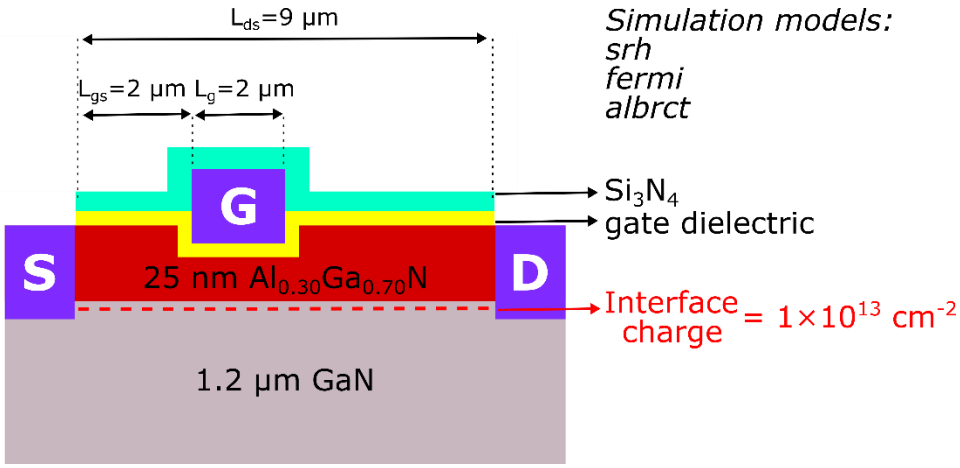


Figure 3.13 Schematic demonstrating the base parameters used in the simulations for MISHEMT structures.

First, the effect of the recess depth was studied for a structure without the gate dielectric. The simulated conduction band diagram is shown in Figure 3.14 and the corresponding I_D vs V_G characteristics are shown in Figure 3.15 for recess depths

between 0 nm (no recess) and 24 nm (1 nm AlGaN remaining). From the conduction band diagram it is observed that as the AlGaN thickness under the gate decreases with increasing recess depth the 2DEG depletes, but the conduction band is not fully raised above the Fermi level until the recess depth is such that only a few nanometers of AlGaN remain. This observation is also confirmed in the I_D vs V_G plot, which shows that the threshold voltage increases as the recess depth increases but does not become positive until only a few nanometers of AlGaN remain under the gate. By controlling the recess depth, it is possible to tune the threshold voltage to a desired value. This plot also reveals that as the recess depth increases and the threshold voltage increases, on the other hand the current density and the transconductance degrades. The trend for the threshold voltage V_{th} as the recess depth increases is shown in Figure 3.16. It can be seen that the relationship between the threshold voltage and the recess depth is not linear.

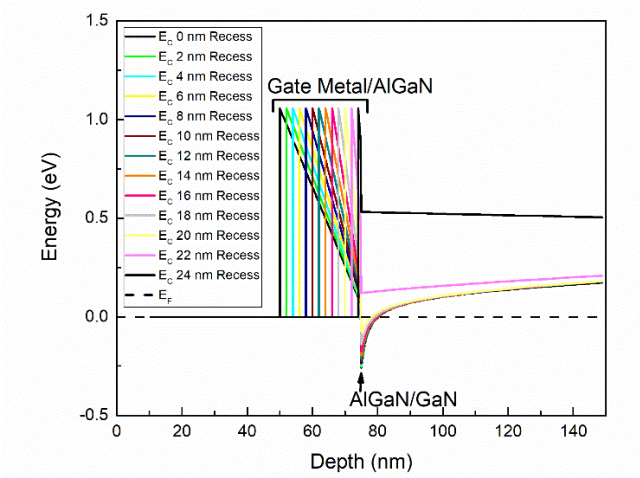


Figure 3.14 Simulated conduction band for increasing recess depth for the AlGaN/GaN structure.

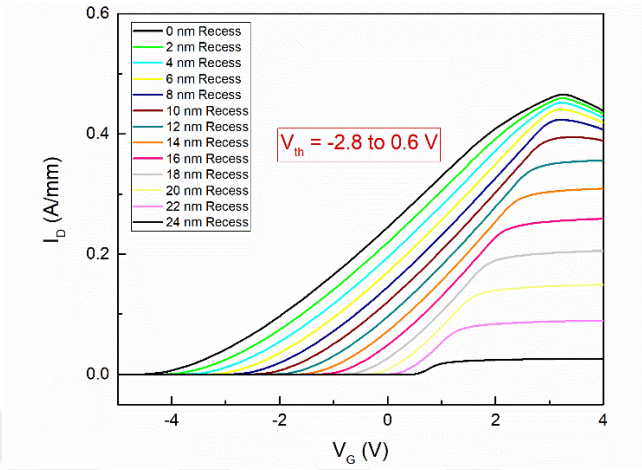


Figure 3.15 Simulated I_D vs V_G characteristic for increasing recess depth for the AlGaN/GaN structure.

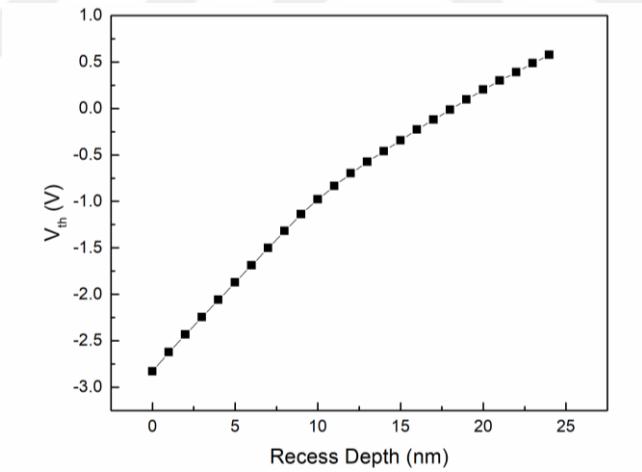


Figure 3.16 Extracted V_{th} trend for increasing recess depth.

If the barrier is fully recessed, a degradation in channel mobility and increased channel resistance will occur, leading to low current densities and large on-resistance [46], [47]. Hence, a partial recess, where a thin barrier layer will remain, is often preferred at the cost of a lower threshold voltage. When only gate recess is used the ON-state gate leakage current increases and the gate voltage swing decreases; thus, for normally-off devices fabrication gate recess and metal-insulator-semiconductor

(MIS) approaches are commonly combined [48], [34]. Four structures are simulated to compare such structures: a standard normally-on AlGaN/GaN structure, a partially recessed AlGaN/GaN structure, a partially recessed structure employing a gate dielectric (SiO_2/AlGaN/GaN), and a deep recessed structure employing a gate dielectric (SiO_2/AlGaN/GaN).

The conduction band and I_D vs V_G characteristics for the normally-on HEMT are shown in Figure 3.17 and Figure 3.18. The 2DEG is formed as expected. A threshold voltage of -3 V is obtained for this structure.

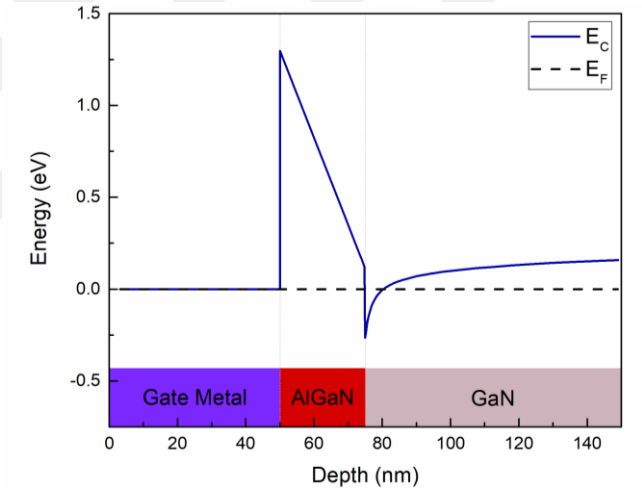


Figure 3.17 Simulated conduction for standard normally-on AlGaN/GaN structure.

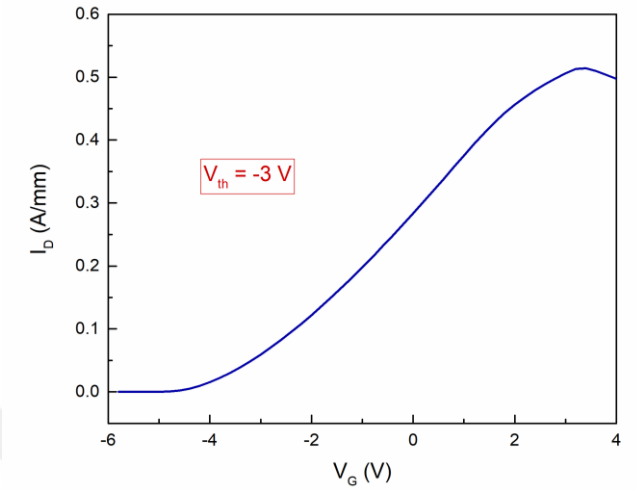


Figure 3.18 Simulated I_D vs V_G characteristic for standard normally-on AlGaN/GaN structure.

The simulation results for the partially recessed structure are shown in Figure 3.19 and Figure 3.20. The recess depth is 20 nm so that 5 nm of the AlGaN barrier remains. The 2DEG is partially depleted in the gate region and the corresponding threshold voltage obtained with the linear extrapolation at maximum transconductance method is obtained as 0.2 V. However, the increased threshold voltage comes at a cost of decreased drain current density.

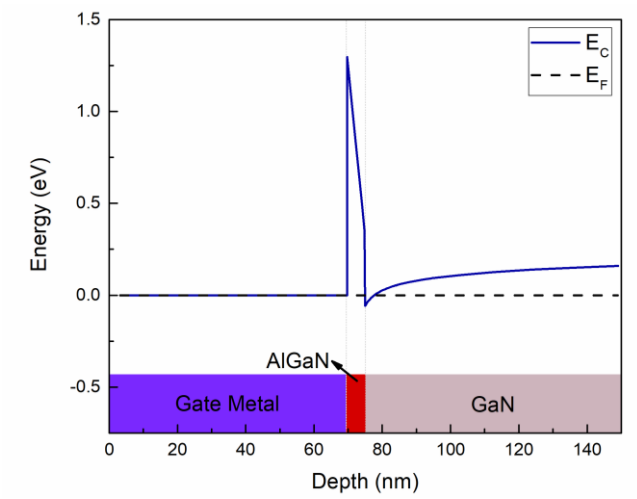


Figure 3.19 Simulated conduction band for recessed AlGaN/GaN gate stack structure.

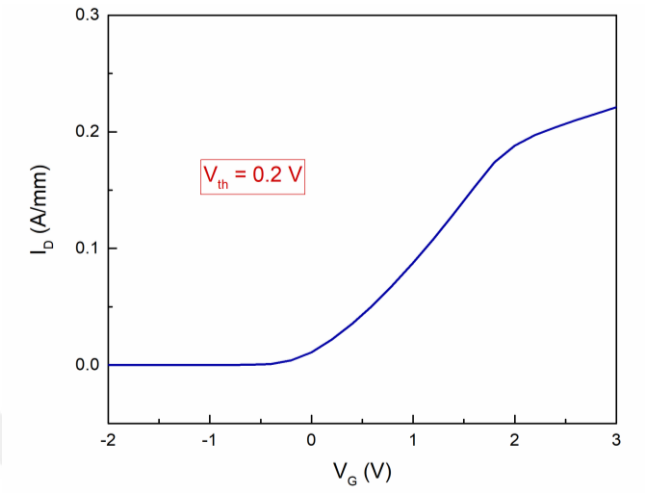


Figure 3.20 Simulated I_D vs V_G characteristic for recessed AlGaN/GaN gate stack structure.

The simulated conduction band and I_D vs V_G characteristics for a partially recessed structure employing a gate dielectric (SiO_2/AlGaN/GaN) are shown in Figure 3.21 and Figure 3.22. The recess depth is 20 nm and the gate dielectric used is a 20 nm SiO_2 layer. Compared to the normally-on AlGaN/GaN structure, the 2DEG is partially depleted, however, the threshold voltage obtained is more negative (V_{th} = -8.2 V). The gate dielectric used to suppress the gate leakage, has the advantages of improving the 2DEG transport characteristics and device stability, but it leads to a decrease in the threshold voltage due to lower gate capacitance as a result of the increased gate-to-channel spacing and the existence of positive interface charges and positive oxide bulk charges.

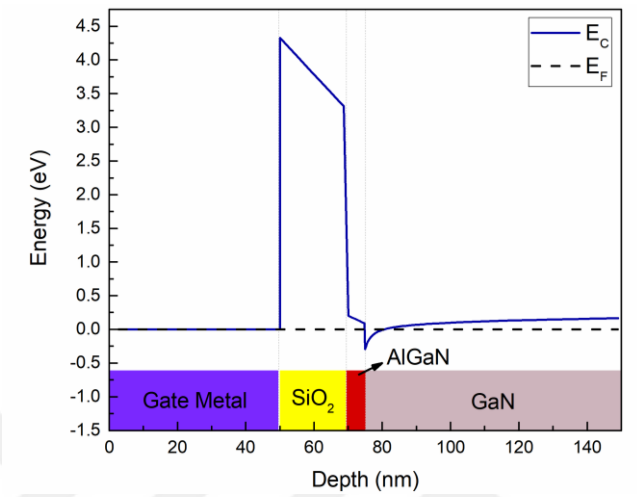


Figure 3.21 Simulated conduction band for recessed SiO_2/AlGaN/GaN gate stack structure.

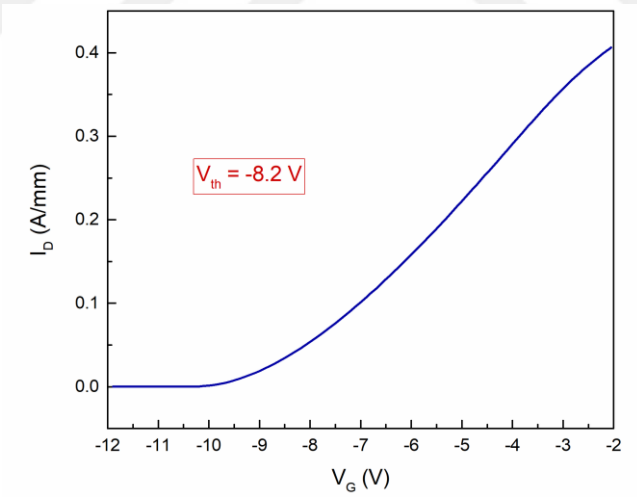


Figure 3.22 Simulated I_D vs V_G characteristic for recessed SiO_2/AlGaN/GaN gate stack structure.

In the deep recess approach, the AlGaN barrier is fully recessed in the gate region so that no 2DEG forms at all (Figure 3.23). Out of the four structures compared, this structure results in the highest threshold voltage of V_{th} = 2 V (Figure 3.24). This comes at the cost of a severely decreased drain current density, due to the absence of the 2DEG in the gate region.

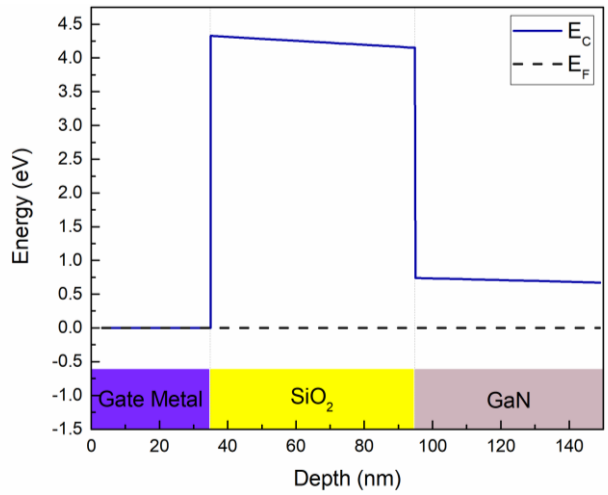


Figure 3.23 Simulated conduction band for deep recessed SiO_2/GaN gate stack structure.

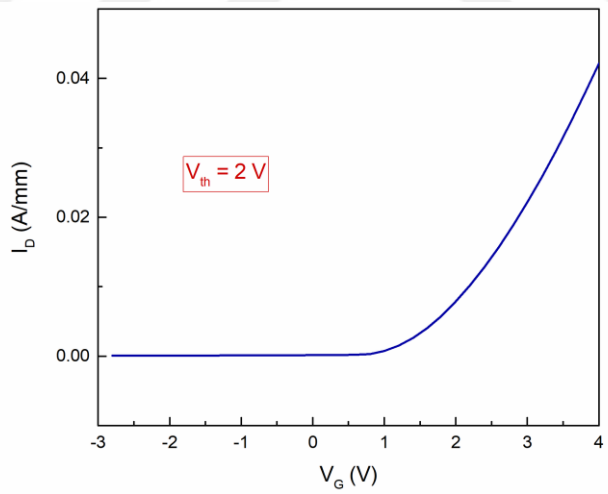


Figure 3.24 Simulated I_D vs V_G characteristic for deep recessed SiO_2/GaN gate stack structure.

Comparing the four simulated structures, a partial recess and deep recess results in a positive shift in the threshold voltage, whereas a partial recess with a gate dielectric results in a negative shift in the threshold voltage. Fluorine treatment is commonly used to further increase the threshold voltage in recessed MIS-HEMT structures. A

practical concern arising from both the recess etch and fluorine treatment methods is increased gate leakage due to surface damage from these processes. An approach to provide decreased gate leakage is to use a high-*k* material as the gate dielectric [49]. Al_2O_3 is an attractive and frequently used high-*k* gate dielectric because of its high conduction-band offset on GaN (2.1 eV), high breakdown field (5–10 MV/cm), and high dielectric constant (9.0) [50].

AlGaN/GaN HEMTs with an Al_2O_3 gate dielectric and fluorine treatment are investigated. The epitaxial structure of the simulated devices consist of a 3 nm GaN cap/18 nm $Al_{0.26}Ga_{0.72}N$ barrier/1.2 µm GaN channel. The effects of the gate dielectric and fluorine treatment are modelled in the simulation as an interface charge at the oxide/semiconductor interface ($Q_{Al2O3/GaN}$) and a bulk oxide charge (n_{ox}) [51]. Both of these charges are positive in the case when there is no fluorine treatment and are negative when there is fluorine treatment, as it is assumed that fluorine acts to compensate the positive charges. The parameters used in the simulation to study the effect of Al_2O_3 thickness and fluorine treatment time are given in Table 3.1.

Table 3.1 Simulation parameters used to model the Al_2O_3 gate dielectric and fluorine treatment. A more negative oxide/semiconductor interface charge $Q_{Al2O3/GaN}$ corresponds to increasing fluorine treatment.

	Fluorine Treatment	**Total Oxide/Semiconductor Interface Charges $Q_{Al2O3/GaN}$ (cm^{-2})**	**Average Bulk Oxide Charge n_{ox} (cm^{-3})**
(1)	No fluorine treatment	7.08×10^{12}	1.1×10^{18}
(2)	↓ Increasing fluorine treatment	-3.46×10^{12}	-7.1×10^{18}
(3)		-4.12×10^{12}	-7.1×10^{18}
(4)		-4.78×10^{12}	-7.1×10^{18}

First, the effect of the Al_2O_3 thickness is studied for a non-recessed structure. The parameters used in this simulation correspond to **(1)** from Table 3.1. The conduction band and I_D vs V_G characteristics are shown in Figure 3.25 and Figure 3.26. As the gate dielectric thickness increases, the threshold voltage becomes more negative.

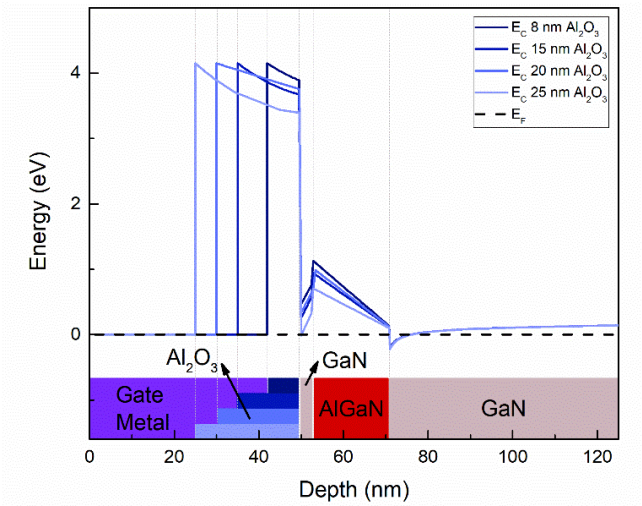


Figure 3.25 Simulated conduction band for different Al_2O_3 thicknesses.

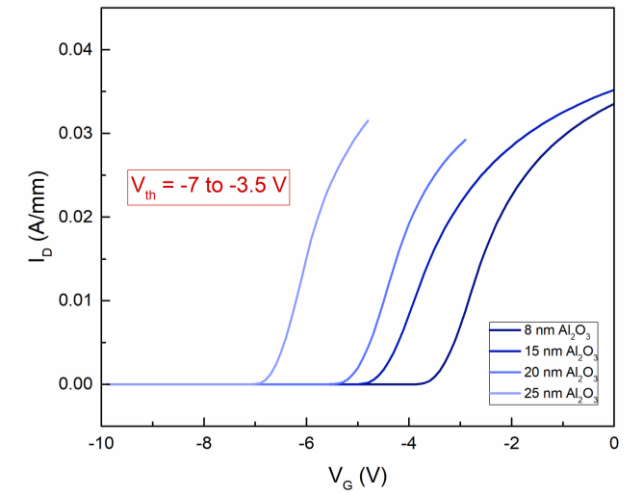


Figure 3.26 Simulated I_D vs V_G characteristics for different Al_2O_3 thicknesses.

Fluorine treatment is modeled for varying gate dielectric thicknesses using the parameters of **(2)** from Table 3.1. The positive interface and oxide charges for the

Al_2O_3 are assumed to be compensated by fluorine treatment and hence become negative. The obtained simulation results are given in Figure 3.27 and Figure 3.28. The threshold voltage increases with increasing Al_2O_3 thickness for the fluorinated structure.

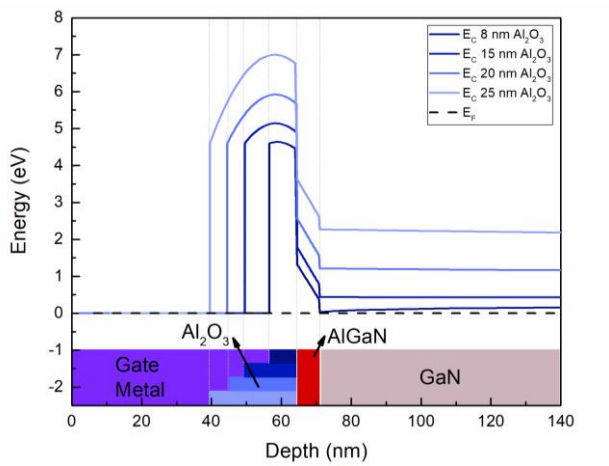


Figure 3.27 Simulated conduction band for different Al_2O_3 thicknesses for a single n_{ox} value, corresponding to a single fluorine treatment time.

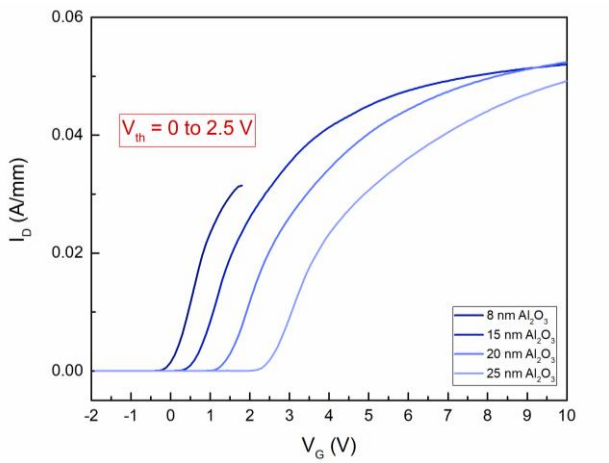


Figure 3.28 Simulated I_D vs V_G characteristics for different Al_2O_3 thicknesses for a single n_{ox} value, corresponding to a single fluorine treatment time.

Finally, the effect of increasing fluorine treatment time is modeled as more negative $Q_{Al2O3/GaN}$ values. The simulation is carried out for a constant Al_2O_3 thickness of 25 nm and the parameters used in the simulation correspond to **(2), (3),** and **(4)** from Table 3.1. It is observed that increasing fluorine treatment time leads to more depletion of the 2DEG and thereby a more positive threshold voltage.

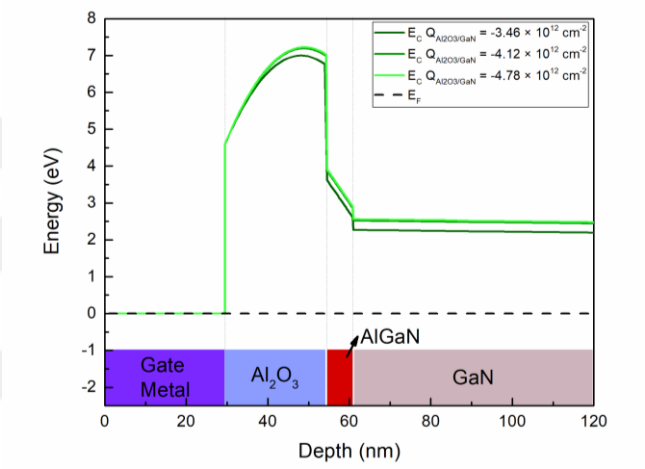


Figure 3.29 Simulated conduction band for different n_{ox} values, corresponding to different fluorine treatment times.

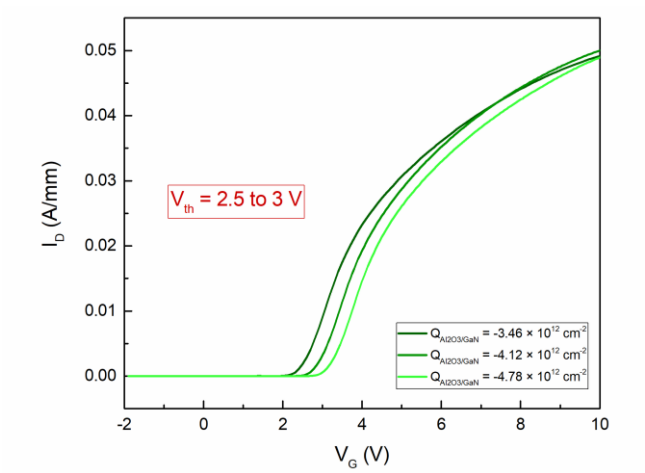


Figure 3.30. Simulated I_D vs V_G characteristics for different n_{ox} values, corresponding to different fluorine treatment times.

Chapter 4

Device Fabrication

This chapter describes the fabrication steps of the normally-off transistors. The fabrication processes have been developed and carried out at the nanofabrication facilities at Bilkent University Nanotechnology Research Center (NANOTAM).

4.1 Epitaxial Growth

GaN compounds contain a large amount of dislocations and when multilayer structures are grown further defects occur due to strain [52]. High quality GaN epilayer growth must be achieved for successful HEMT fabrication. Device quality GaN epilayers can be grown using Metal Organic Chemical Vapor Deposition (MOCVD). MOCVD is a technique for growing crystalline layers and is used to deposit layers of atoms onto a wafer. Simply, the growth process works by injecting ultra-pure gases into a cold wall reactor under thermal and compositional gradient, and under the right conditions, through surface reactions crystal growth is obtained. These gases used are metalorganic compounds and hydride gases. The gaseous hydrides and metalorganic vapors react in a pyrolysis reaction and the decomposed atoms can then adsorb to the surface [53].

The electron mobility and the sheet carrier density of the 2DEG are important physical parameters that determine the HEMT properties and performance. The 2DEG properties are influenced by the composition of the barrier layer, barrier thickness, AlN spacer thickness if a spacer layer is present, GaN cap thickness if a cap layer is present, and the impurity level in the GaN layer, all of which are parameters dependent on the growth conditions. The wafer growth is carried out on 4-in Si (111) wafers. Commonly, a nucleation layer is introduced first to overcome

the lattice mismatch between the substrate and GaN. A buffer layer is grown to improve the crystallinity of the GaN films and obtain a smooth GaN surface. For the AlGaN/GaN structure a GaN buffer is used; for the InAlN/GaN structure an additional graded AlGaN buffer is used before the GaN buffer. After the buffer layer unintentionally doped or intrinsic channel GaN layer is grown. Next, for the InAlN/GaN structure the InAlN barrier layer and the p-GaN capping layer is grown, and for the AlGaN/GaN structure an AlN spike layer, the AlGaN barrier layer, and a GaN cap layer is grown.

4.2 Cleanroom Fabrication

In this section the fabrication steps to make a normally-off transistor will be described. The fabrication recipes for p-GaN gate devices and MISHEMT devices follow the same basic recipes with some differing specialized steps. The general methods required for the fabrication of a HEMT are as follows:

Step 1: Wafer Cleaving

Step 2: Surface Cleaning

Step 3: Optical Lithography

Step 4: Oxygen Plasma Treatment

Step 5: Contact Deposition

Step 6: Lift-off

Step 7: Rapid Thermal Annealing

Step 8: Dry Etching

Step 9: Dielectric Deposition

4.2.1 Wafer Cleaving

The 4-in wafers are cleaved into 12×12 mm pieces to make the fabrication processes easier and make it possible to carry out more than one process. The wafer is split into the smaller pieces by mechanical sawing using a dicing saw. The wafer to be diced is spin-coated with a layer of photoresist to keep wafer clean from dust. The wafer is suspended by tape in the machine. A high-speed spindle with a diamond blade divides the wafer into the desired size. Water flows over the blade for cooling purposes. The diced samples are dried and removed from the tape and will be cleaned next.

4.2.2 Surface Cleaning

In HEMT devices the surface of the group III nitride semiconductor is an important factor and can be the cause of unwanted effects such as RF-DC dispersion. Thus, for an optimized, reproducible and reliable process the physical and chemical properties of the surface of the nitride must be controlled [54].

Organic particles are cleaned from the surface by rinsing with acetone. The acetone solvent is removed with an isopropyl alcohol (IPA) rinse which is in turn removed by rinsing with deionized water (DI water). The samples are dried with a nitrogen spray gun and the surfaces of the samples are inspected for any remaining impurities with an optical microscope. In the case of remaining impurities the samples are cleaned in an ultrasonic bath in acetone, followed by an IPA and DI water rinse. For stubborn organic particles mechanical cleaning with cleanroom swabs is carried out before sonication. These steps are repeated until a satisfactorily clean sample surface is achieved.

4.2.3 Optical Lithography

Optical photolithography with 1 µm resolution is used for the patterning of the samples. Both direct and reverse lithography are used for various steps. Contact lithography with the Karl Suss MA6 Mask Aligner is used for patterning. For most of the steps AZ5124E type image reversal photoresist is used. This resist is preferred

to obtain negative sidewall profiles for easier liftoff [55]. The resist is spincoated at 6000 rpm for 60 seconds with a 4 second ramp time for most steps. The revolutions per minute can be varied to obtain thinner or thicker resist for certain steps, such as the gate lithography where higher revolutions per minute are used to obtain a thinner resist thickness since good resolution is more critical. After the spincoat a soft bake at 110°C for 1 minute is done to evaporate residual solvents. Edge bead removal is carried out with a cleanroom swab and acetone. Alignment and exposure is done with the Karl Suss MA6 Mask Aligner. For direct lithography a single exposure is done. For reverse lithography after a first exposure a reversal bake at 110°C for 2 minutes is done to crosslink the exposed areas and flood exposure without a mask is done.

The exposed samples are developed using AZ400K diluted with water with a ratio of 1:4. The developed samples are rinsed with DI water and dried with nitrogen. Finally, optical microscope inspections for the critical dimension, resolution, and alignment mismatches are done.

4.2.4 Oxygen Plasma Treatment

Oxygen plasma treatment is used to remove organic impurities and contaminants from the surface. The Glow Research AutoGlow Plasma System is used. This treatment is carried out before contact depositions and after mesa etching to ensure that any photoresist residue is removed. First a 5 minute purge is carried out at a pressure of 2 Torr. Next 50 W RF plasma at 2 Torr pressure for 1 minute for before metal deposition treatments, and 110 W RF plasma at 2 Torr pressure for 5 minutes for after mesa etch treatments is applied.

4.2.5 Contact Deposition

For contact deposition electron beam (e-beam) evaporation is used. The Oerlikon Leybold Univex 350 E-Beam Evaporator System is used. Ti/Al/Ni/Au is used for ohmic contacts, Ni/Au is used for gate contacts and Ti/Au for the interconnect layer.

4.2.6 Lift-off

The image reversal resist processed in the negative mode produces a reproducible undercut so that the sidewalls of the resist are not coated and a straightforward liftoff process is possible. The samples are soaked in a solvent, typically acetone (NMP for interconnect), for at least 30 minutes. If necessary, ultrasonic treatment is used to assist the lift-off process. The samples are then rinsed with acetone and isopropyl alcohol.

4.2.7 Rapid Thermal Annealing

After ohmic metallization rapid thermal annealing is applied to improve the contact resistances. The Surface Science Integration Solaris 150 Rapid Thermal Processing System is used for annealing. The samples are annealed in nitrogen gas at varying temperatures and durations.

4.2.8 Dry Etching

Both wet etch and dry etch methods are possible for GaN fabrication, but in this study dry etching is preferred due to its anisotropy. Inductively coupled plasma reactive ion etching (ICP-RIE) is used with the Sentech SI 500 Dry Etching System and Samco RIE-140iP systems. ICP-RIE systems use a plasma generated with an RF powered magnetic field. The produced plasma is chemically reactive so that both chemical reactions and ion-induced etching occur. The Sentech system is used for mesa etching, recess etching, and p-GaN etching while the Samco system is used for the dielectric opening etch.

4.2.9 Dielectric Deposition

Dielectric deposition is used for device passivation and for the gate dielectric. For passivation purposes SiN_x is deposited by plasma enhanced chemical vapor deposition (PECVD) using the Sentech SI PPD Plasma Enhanced Chemical Vapor Deposition System and Samco PD-220Nl systems. SiN_x passivation is used to

improve the device performance and reliability by decreasing the density of surface states available that can lead to electron trapping [56].

As a gate dielectric ALD grown Al_2O_3 is used. A Cambridge Nanotech Savannah S100 ALD System was employed to perform the Al_2O_3 dielectric deposition. The deposition was carried out at a temperature of 200 °C. The precursors used were $Al(CH_3)_3$ solution as the aluminum precursor and water as the oxygen precursor. The pulse duration was 0.015 s and the purge duration was 10 s. The deposition rate was 1 Å/cycle. Gate dielectrics are used to decrease gate leakage and prevent RF current collapse [57].

4.3 Fabrication Recipes

The p-GaN gate HEMTs and recessed MISHEMTs have been fabricated with similar procedures using the methods described in the previous sections. The fabrication recipes will be described in detail this section.

4.3.1 p-GaN Gate HEMTs

This section describes the fabrication studies carried out for the fabrication of the normally-off transistors. Mask design, and studies for ohmic contacts to InAlN, selective etch for p-GaN/InAlN structures were carried out. The recipe used is described.

<u>Mask Design</u>

A photomask consisting of one and two finger transistors with gate width W_g of 100 µm was developed. Some of the important parameters to take into consideration in the design of a transistor are the gate length L_g, drain to source spacing L_{ds}, gate to source spacing L_{gs}, and gate to drain spacing L_{gd}. Typically, short L_g is preferred as the cutoff frequency f_T ($f_T = v_{sat}/2\pi L_g$) and drain current are inversely proportional with L_g (W_g/L_g). For high power operations, the drain to source spacing should be minimized and the gate should be placed closer to the source than drain to improve

the breakdown characteristics. The purpose of this study was to study normally-off operation, so a gate width that can be achieved with optical lithography of 2 µm was chosen. Various drain to source spacings up to 7 µm were used and the gates were placed symmetrically. The transistor layout in the photomask is shown in Figure 4.1.

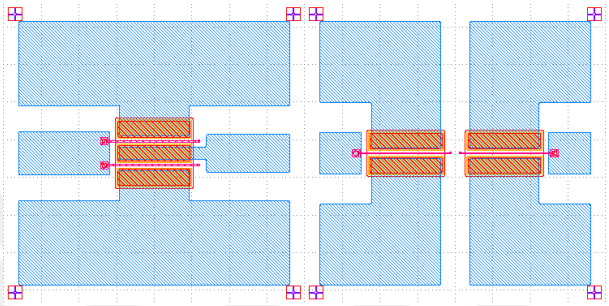


Figure 4.1 Normally-off HEMT photomask transistor layout.

The mask contains patterns to monitor different aspects of the fabrication process (Figure 4.2) and alignment markers for lithography. Transmission line method (TLM) patterns are used to determine the ohmic contact resistance. Greek cross patterns are used to determine resistivity. Patterns to characterize the leakage are included. Alignment markers are used to align different lithography steps to each other and resolution markers are used to determine the critical dimension (minimum feature size).

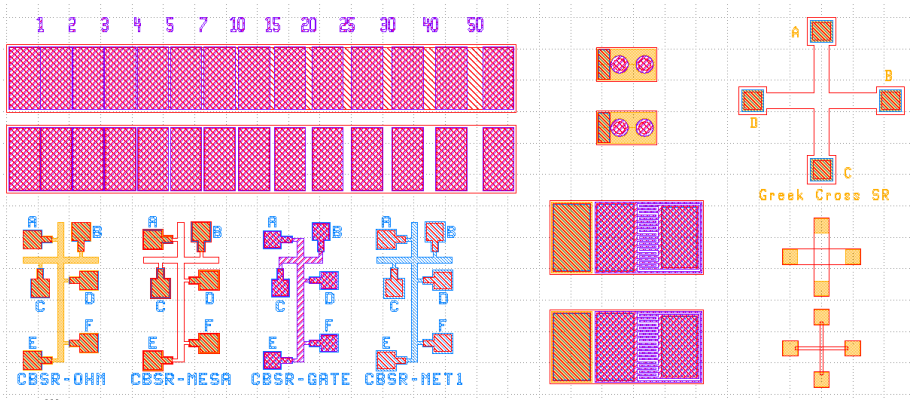


Figure 4.2 Test patterns photomask layout.

Ohmic contact formation

Ohmic contacts are patterned with AZ nLOF 2020 resist spun at 4000 rpm for 40 seconds with a 6 second ramp. HMDS is spincoated using the same parameters before the photoresist in order to promote adhesion. Edge bead removal cleaning is done and the samples are baked at 110°C for 1 minute to dry the photoresist. Using a photomask the samples are exposed with 66 mJ/cm^2 UV light. The samples are baked at 105°C for 1 minute and 15 seconds and are then developed using AZ 826MIF for 35 seconds to obtain a 1 µm undercut and are checked under an optical microscope. Plasma Asher Descum operation is done to remove any photoresist residues in the drain and source regions.

Before the ohmic contact deposition the 100 nm p-GaN layer in the drain and source regions must be removed with dry etching. This is achieved in two steps with two different etch recipes. The parameters for these recipes are given in Table 4.1 and Table 4.2. The first recipe uses BCl_3 and Cl_2 gases and is used to thin the p-GaN layer. The process duration for this recipe is 65 seconds. The second recipe uses Cl_2 and O_2 gases and is used to achieve selective etching of p-GaN over InAlN. The process duration of this recipe is 15 minutes and is chosen such to include an overetch time to ensure the complete removal of the p-GaN layer.

Table 4.1 p-GaN etch process conditions utilizing ICP RIE.

BCl_3 (sccm)	Cl_2 (sccm)	ICP Power (W)	RF Power (W)	Pressure (Pa)	Etch Rate (nm/s)
35	5	100	50	0.6	1

Table 4.2 Selective p-GaN/InAlN etch process conditions utilizing ICP RIE.

Cl_2 (sccm)	O_2 (sccm)	ICP Power (W)	RF Power (W)	Pressure (Pa)	Etch Time (min)
35	3.5	100	30	0.6	15

The same lithography used to etch the samples will also be used for the metallization step, therefore it is not possible to measure and confirm the etch depth of the process samples. For this purpose, another sample is prepared to check the etch depth. Figure 4.3 displays the SEM image of a p-GaN/InAlN sample etched with the selective etch recipe. The etch depth is obtained as approximately 100 nm as expected.

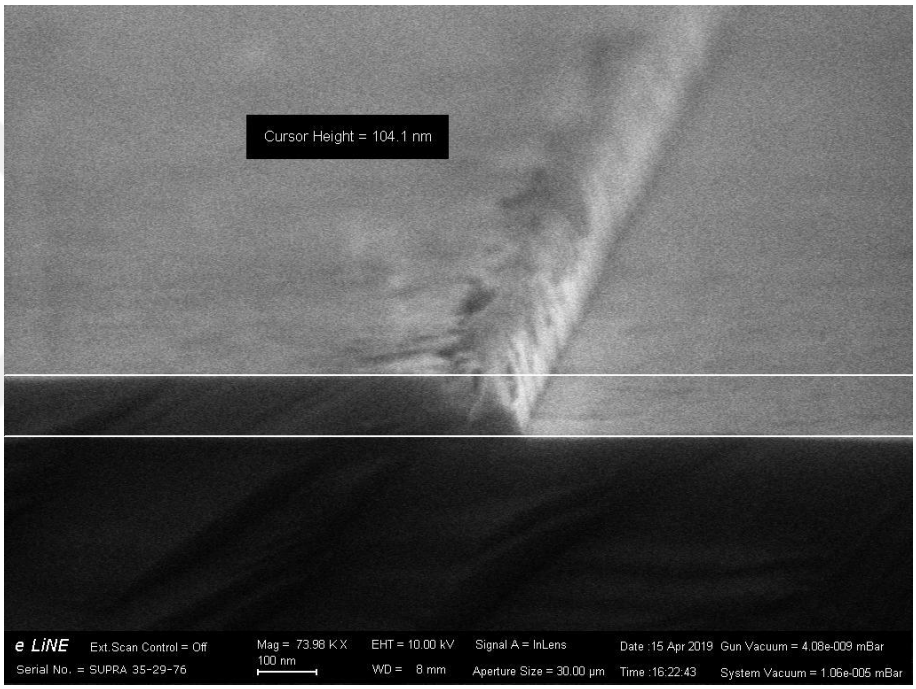
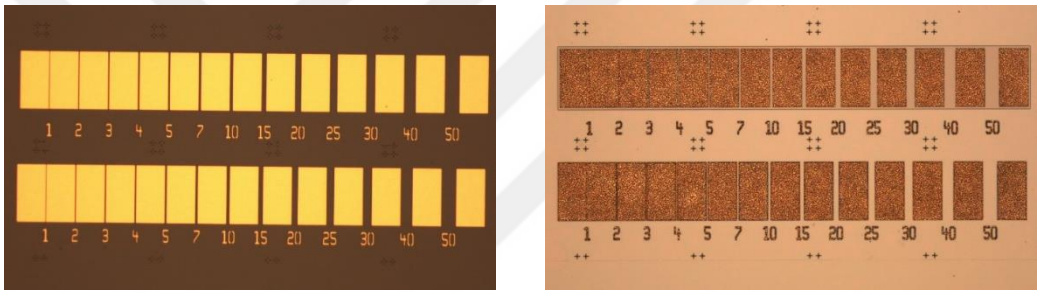


Figure 4.3 SEM image of selectively etched 100 nm p-GaN over InAlN.

After the p-GaN is etched the ohmic contacts will be prepared by evaporation of multilayered Ti/Al/Ni/Au. The formation of ohmic contacts to InAlN is more challenging compared to AlGaN due to the high Al-content. Additionally, there exists a tradeoff for the annealing temperature to attain low contact resistance, as a significant degradation of mobility accompanied by a decrease in sheet carrier density occurs as the annealing temperature increases [58].

Studies are carried out to optimize the contacts to the InAlN/GaN heterostructure. TLM structures with contact length of 100 µm and contact width of 200 µm are utilized to characterize the contacts. The distances between contact pads are 5 µm,

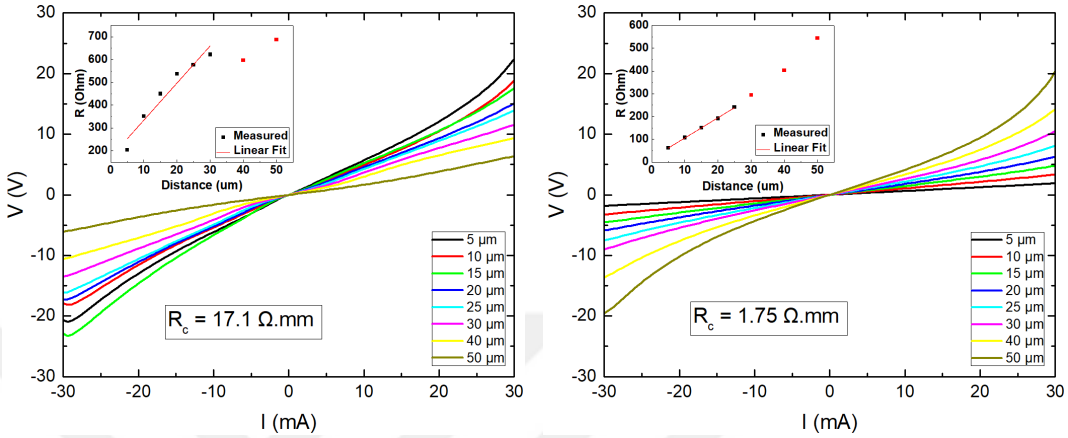
10 µm, 15 µm, 20 µm, 25 µm, 30 µm, 40 µm and 50 µm. The TLM patterns are fabricated by defining the contact areas with optical lithography using a negative photoresist. Ti/Al/Ni/Au (35/100/40/50nm) metal stack [59] is deposited with e-beam evaporation and liftoff in acetone is carried out. Then the samples are annealed under three different conditions to determine the optimum process conditions. Annealing is carried out in N_2 gas ambient at 850°C for 30 seconds, 60 seconds, and 120 seconds. Figure 4.4 displays the fabricated TLM patterns before and after annealing.



(a) **(b)**

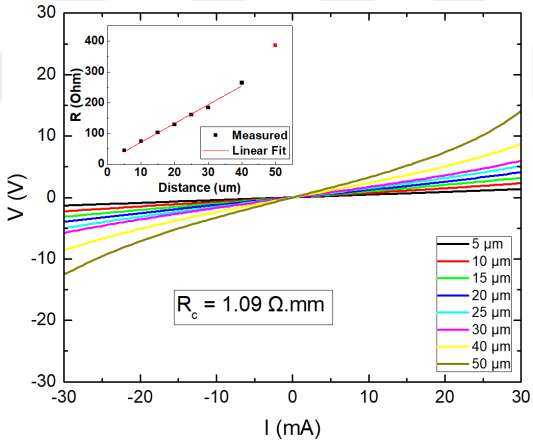
Figure 4.4 Optical microscopy image of the TLM patterns after (a) ohmic metallization and (b) after rapid thermal annealing.

The IV curves obtained from the measured TLM patterns and the resulting resistances, the fitting of the resistances and finally the calculated contact resistances for each of the annealing durations are shown in Figure 4.5. For the sample annealed at 850°C for 30 seconds the contacts show slightly rectifying behavior, even for smallest distance between the contact pads. Analogously, the highest contact resistance is obtained for this sample. For the 60 second and 120 second annealed samples the contact behavior is linear for the smaller contact spacings and starts to become slightly rectifying for the larger contact spacings.



(a)

(b)



(c)

Figure 4.5 TLM measurement results of sample annealed at 850°C for (a) 30 seconds, (b) 60 seconds, and (c) 120 seconds.

The R_C and R_{SH} values obtained from the TLM measurements are summarized in Table 4.3. For the 30 second annealed sample a very high contact resistance of 17.3 Ω·mm is obtained. For the 60 second annealed sample the contact resistance decreases to the more reasonable value of 1.75 Ω·mm. For the 120 second annealed sample the lowest contact resistance of 1.09 Ω·mm is obtained. Additionally, for increasing annealing time, the sheet resistance R_{SH} does not increase, which indicates

that no degradation has occurred. Thus, the optimum annealing condition to obtain the best contact is 120 second at 850°C in N_2 ambient.

Table 4.3 R_C and R_{SH} values for different annealing durations.

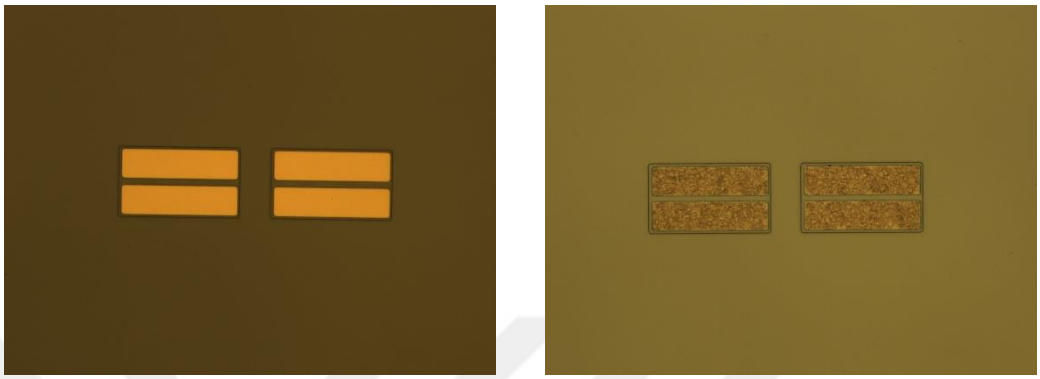
Duration (sec)	R_C (Ω·mm)	R_{SH} (Ω/sq)
30	17.1	3262
60	1.75	1774
120	1.09	1220

Thus, the ohmic metallization of the process samples is formed by e-beam evaporation of Ti/Al/Ni/Au (35/200/40/50 nm). The titanium, nickel and gold metals are deposited in tungsten crucibles while aluminum is deposited in an elemental carbon crucible. The deposition parameters are shown in the table below.

Table 4.4 Deposition thickness and rate for ohmic metallization.

Material	Deposition Thickness (nm)	Deposition Rate (Å/sec)
Ti	35	2
Al	200	2
Ni	40	1
Au	50	3

Lift-off is done by soaking in acetone and then the samples are cleaned by rinsing with acetone and isopropanol alcohol. After lift-off, in order to improve the contact resistances, the samples are annealed at 850°C for 120 seconds in a nitrogen environment. The microscope images of the samples before and after annealing are given in Figure 4.6.



(a) **(b)**

Figure 4.6 Optical microscope view of the drain and source patterns after (a) ohmic metallization and (b) after rapid thermal annealing.

Mesa Isolation

Individual devices are isolated from one another with mesas defined using positive mode resist. The active regions of the devices are defined and the electric field effects between the devices are minimized by etching from the top layer to a depth below the 2DEG in the GaN channel layer. To define the mesa patterns AZ5214E resist is spincoated at 6000 rpm for 60 seconds with a 4 second ramp, the samples are baked at 110°C for 1 minute, edge bead removal cleaning is done, and using a photomask the samples are exposed with 216 mJ/cm^2 UV light. The samples are developed in diluted AZ400K for 32 seconds, rinsed with DI water and dried with the N_2 gun. Development of the lithography is checked using an optical microscope.

Mesa etching is done with the Sentech ICP-RIE system using a Bl_3 and Cl_2 gas mixture. The samples are etched for a duration of 190 seconds to etch away to 100 nm p-GaN layer and obtain a mesa depth greater than 75 nm. The etch process parameters are shown in the table below.

Table 4.5 Mesa etch process conditions utilizing ICP RIE.

BCl_3 (sccm)	Cl_2 (sccm)	ICP Power (W)	RF Power (W)	Pressure (Pa)	Etch Rate (nm/s)
35	5	100	50	0.6	1

After device isolation 4 point probe TLM measurements can be performed to characterize the ohmic contact quality. The ohmic contact resistance is obtained as 2.50 Ω·mm. The higher contact resistance is due to the p-GaN on the surface.

Gate formation

Gate contacts are patterned with AZ5214E resist spun at 9000 rpm for 60 seconds with a 6 second ramp, then baked at 110°C for 1 minute to dry the photoresist. Edge bead removal is done using a photomask so that better resolution can be obtained for the gates. Then, using a photomask the samples are exposed with 108 mJ/cm^2 UV light, baked at 110°C for 2 minutes and exposed with 216 mJ/cm^2 UV light without the photomask so that the gate regions are soluble and the remaining regions are inert. The samples are developed using diluted AZ400K for 33 seconds. Plasma Asher Descum operation is done to remove any photoresist residues.

The gate metallization is formed by e-beam evaporation using Ni/Au (50/300 nm). The deposition parameters are shown in the table below.

Table 4.6 Deposition thickness and rate for gate metallization.

Material	Deposition Thickness (nm)	Deposition Rate (Å/sec)
Ni	50	0.8
Au	300	1.8

Lift-off is done by soaking in acetone and then the samples are cleaned by rinsing with acetone and isopropanol alcohol.

Dry etching of p-GaN regions

At this point, the p-GaN layer between the source and drain contacts remains and must be removed so that it is present only under the gate to be able to achieve good transistor characteristics. The samples are not patterned with photolithography; the ohmic and gate metallizations act as a protective layer and all remaining regions are etched. The Sentech ICP-RIE system is used to decrease the thickness of the p-GaN layer. Ideally, the p-GaN layer would completely be removed, however, the selective etch recipe used in the ohmic contact step cannot be used here as it damages the metal contacts on the sample. Instead a BCl_3 gas based recipe with low selectivity is used to achieve a slow etch rate that can be used to thin the p-GaN layer. At an RF power of 30 W; an etch rate of 4 nm/min is obtained. The samples are etched for 23 minutes. The table below shows p-GaN etch process conditions utilizing ICP RIE.

Table 4.7 p-GaN etch process conditions utilizing ICP RIE.

BCl_3 (sccm)	**ICP Power (W)**	**RF Power (W)**	**Pressure (Pa)**	**Etch Rate (nm/min)**
20	50	30	7.5	4

Dielectric Deposition and Opening

The SiN_x passivation layer is deposited using the Samco PD-220Nl Plasma Enhanced Chemical Vapor Deposition System. 250 nm of SiN_x was deposited using silane (SiH_4), ammonia (NH_3), and nitrogen (N_2) as source gases. The process time was 7 minutes and 35 seconds. The recipe parameters are shown in the Table 4.8.

Table 4.8 SiN_x deposition process utilizing PECVD.

SiH_4 (sccm)	NH_3 (sccm)	N_2 (sccm)	RF Power (W)	Temperature (°C)	Pressure (Pa)	Deposition Rate (nm/s)
140	6	500	130	275	75	0.55

The dielectric in the region of the metal contacts must be removed to be able to make electrical connections to the contacts. The dielectric openings are patterned with the same procedure as the mesa step.

The dielectric etching was done using the Samco ICP RIE system using SF_6 and Ar gases. The process time was 3 minutes and 45 seconds. The process parameters are given in the table below. The sample after the SiN_x etch is shown in Figure 4.7.

Table 4.9 SiN_x opening etch process utilizing ICP RIE.

SF_6 (sccm)	Ar (sccm)	ICP Power (W)	RF Power (W)	Pressure (Pa)	Etch Rate (nm/min)
300	300	60	40	0.6	100

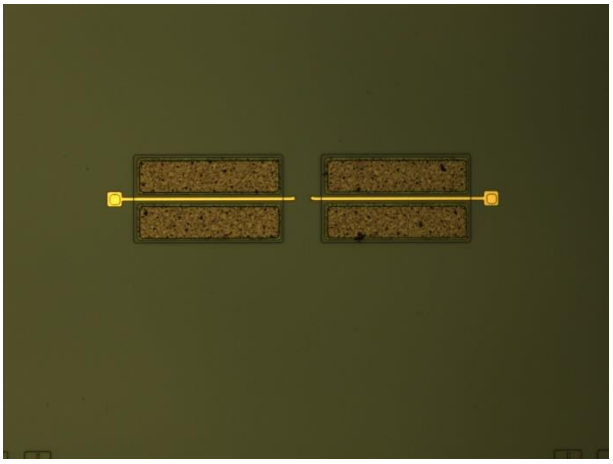


Figure 4.7 Optical microscope image of the sample following the passivation and opening etch steps.

Interconnect

Interconnect metallization is carried out to from metal pads suitable for electrical measurements. The samples are patterned with AZ5214E resist spun at 6000 rpm for 60 seconds with a 4 second ramp. The samples are baked at 110°C for 1 minute to dry the photoresist and edge bead removal cleaning is done. Using a photomask the samples are exposed with 108 mJ/cm^2 UV light. The samples are baked at 110°C for 2 minutes and exposed with 216 mJ/cm^2 UV light without the photomask so that the interconnect regions are soluble and the remaining regions are inert and therefore protected. The development in diluted AZ400K takes 40 seconds. Similarly to the previous contact deposition steps, oxygen plasma treatment is done.

Ti/Au (50/350 nm) metallization is formed by e-beam evaporation with the parameters shown below.

Table 4.10 Deposition thickness and rate for interconnect metallization.

Material	Deposition Thickness (nm)	Deposition Rate (Å/sec)
Ti	**50**	**2**
Au	**350**	**2**

Lift-off is done by soaking in acetone and then the samples are cleaned by rinsing with acetone and isopropanol alcohol. At this stage the devices are ready for electrical measurements. The finished devices are shown in Figure 4.8.

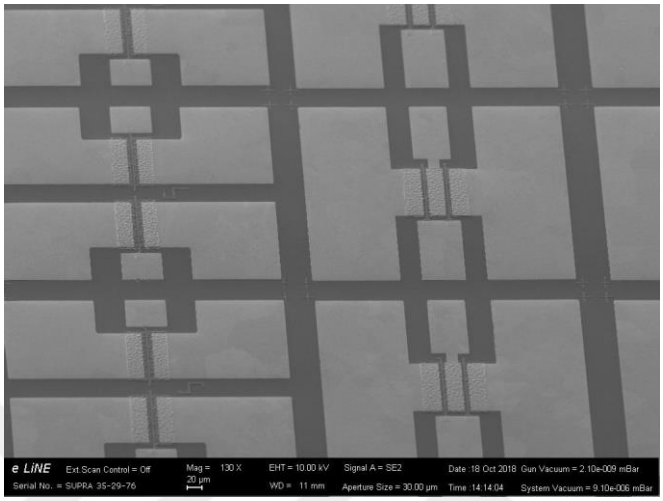


Figure 4.8 SEM image of the sample after the interconnect metallization and liftoff.

4.3.2 Recessed MISHEMTs

This section describes the fabrication studies carried out for the fabrication of the normally-off MISHEMTs. Studies for recess etching and fluorine treatment were carried out. The recipe used is described.

<u>Mesa formation</u>

The recessed MISHEMT fabrication begins with mesa formation. AZ5214E resist is spun onto the samples at 6000 rpm for 60 seconds with a 10 second ramp. Soft bake is done for 1 minute at 110°C. After edge bead removal, using a photomask the mesa patterns are exposed with a 200 mJ/cm^2 dose. The samples are developed in diluted AZ400K for 37 seconds. Optical microscope checks for resolution, critical dimension, and alignment mismatch are done.

The mesa etch is done with the Sentech ICP RIE system. The samples are etched for 75 seconds. The process parameters are given in Table 4.11. The sample after mesa isolation is shown in Figure 4.9.

Table 4.11 Mesa etch process conditions utilizing ICP RIE.

BCl_3 (sccm)	Cl_2 (sccm)	ICP Power (W)	RF Power (W)	Pressure (Pa)	Etch Rate (nm/min)
35	3	100	50	0.6	1

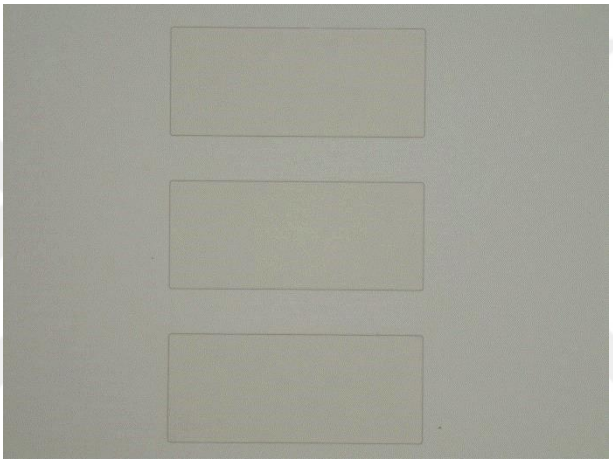


Figure 4.9 Optical microsope image after mesa isolation step.

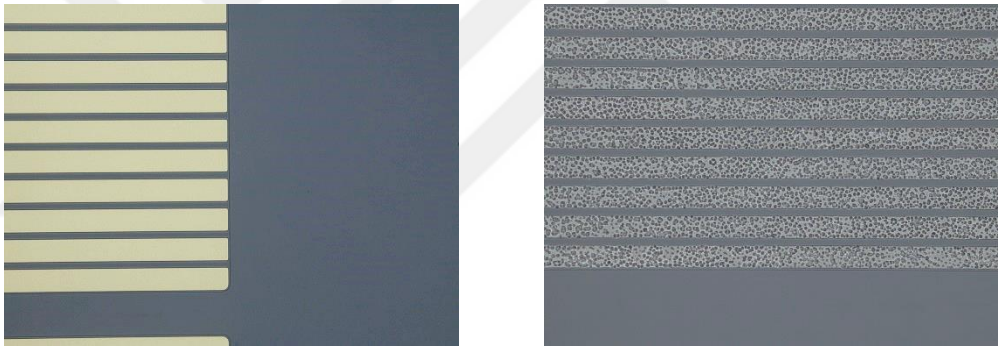
Ohmic contact formation

AZ5214E resist is spin-coated at 6000 rpm for 60 seconds with a 10 second ramp. The samples are baked for 1 minute at 110°C and edge bead removal is done. The samples are exposed with a photomask to 100 mJ/cm^2 UV light, baked for 2 minutes at 110°C, and exposed without the photomask with 200 mJ/cm^2 UV light. The photolithography is developed in diluted AZ400K for 34 seconds. Oxygen plasma treatment is applied.

Ohmic metallization consists of Ti/Al/Ni/Au (12/120/35/65 nm). Ti, Al, and Ni are deposited in carbon crucibles; Au is deposited in a molybdenum crucible. The deposition parameters are given in Table 4.12. The optical microscopy image is given in Figure 4.10.

Table 4.12 Deposition thickness and rate for ohmic metallization.

Material	Deposition Thickness (nm)	Deposition Rate (Å/sec)
Ti	12	2
Al	120	2
Ni	35	2
Au	65	3



(a) **(b)**

Figure 4.10 Optical microscopy image after (a) ohmic metallization and (b) after rapid thermal annealing

Liftoff is achieved by soaking the samples in acetone overnight. The samples are cleaned with acetone and isopropanol alcohol and are annealed for 30 seconds at 830°C. A three step annealing recipe in nitrogen environment is used. The annealing process starts with a 60 second purge, ramps up to 400°C and waits for 180 seconds, ramps up to 700°C and waits for 40 seconds, and then finally ramps up to 830°C for 30 seconds.

After annealing, 4 point TLM measurements can be carried out. The contact resistance was measure as 0.67 Ω·mm.

Gate Formation

Gate recess regions are patterned with AZ5214E resist spun at 9999 rpm for 60 seconds with a 10 second ramp to achieve thinner resist and therefore better resolution. The samples are baked for 1 minute at 110°C. Edge bead removal is done with a photomask. The gates are patterned with a photomask at 120 mJ/cm^2, baked for 2 minutes at 110°C, and exposed without a photomask at 200 mJ/cm^2. The samples are developed in diluted AZ400K for 44 seconds. The developed samples are inspected under an optical microscope.

Recess etch processes are carried out using ICP-RIE. In recess etch processes the most important factor is precise control of the remaining AlGaN layer thickness, as this directly determines threshold voltage of the device. It is typically desired that a few nanometers of the barrier layer remains in order to achieve low ON-resistance. Additionally, uniform etching across the sample or wafer is desired to ensure that the obtained threshold voltages stay within an acceptable range. For this purpose, super slow etching is used by minimizing the RF power. The thickness of the barrier layer that will remain is determined by the etch duration when very slow etching is carried out. However, the etch rate is difficult to control as the etch rate varies because of byproducts in the reaction chamber. Slow etching is also required to minimize plasma damage and thus obtain smooth surfaces. Any ICP induced damages may lead to defects and an increased in gate leakage current. The gate recess is formed by dry etching with the Sentech ICP-RIE system. The recess depth is 10 nm. The process parameters are given in the table below.

Table 4.13 Gate recess etch process conditions utilizing ICP RIE.

BCl_3 (sccm)	Cl_2 (sccm)	ICP Power (W)	RF Power (W)	Pressure (Pa)	Etch Rate (nm/sec)
20	20	300	5	0.6	0.27

Subsequently, the fluorine plasma treatment is carried out. Fluorine treatment is also carried out using ICP-RIE using fluorine containing gases such as CF_4, SF_6 and is another process that must be carefully optimized. Low plasma power must be used to prevent etching from occurring during the treatment process. In addition to causing a positive shift in the threshold voltage, fluorine plasma treatment has the advantages of decreased gate leakage current and increased breakdown voltage. However, plasma induced surface damages may be introduced and fluorine ions that are implanted too deep into the sample can cause degradation of 2DEG mobility. A low power plasma treatment using the Samco ICP-RIE system is utilized for the fluorine implantation. SF_6 gas is used as the source for fluorine ions and the treatment time is 10 minutes. The detailed parameters are shown below.

Table 4.14 Fluorine plasma treatment conditions utilizing ICP RIE.

SF_6 (sccm)	**ICP Power (W)**	**RF Power (W)**	**Pressure (Pa)**	**Process Time (min)**
20	0	10	0.6	10

The surface properties of samples with recess etching and fluorine treatment were investigated using XPS measurements. Three AlGaN/GaN heterostructure samples were prepared such that one sample had no treatment, one sample had recess etching applied, and the final sample had both recess etching and fluorine treatment applied. Figure 4.11 shows compares the obtained XPS spectra for the three samples. After the fluorine treatment, it can be observed that a peak corresponding to F 1s appears, confirming that the ICP-RIE treatment is successful for implanting fluorine ions into the gate region. There are also changes in the oxygen and carbon peaks with the application of the treatments, indicating that surface damage leading to changes in surface contamination occurs.

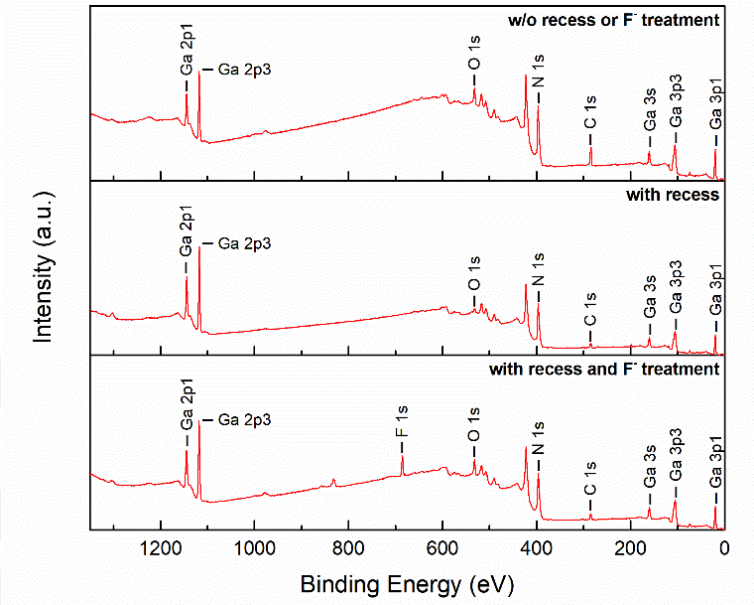


Figure 4.11 XPS spectra for an AlGaN/GaN heterostructure without recess of fluoine treatment (bare sample), with recess, and with recess and fluorine treatment, with some of the major peaks labeled.

AFM surface roughness measurements were carried out investigate the effects of the recess and fluorine treatments on the surface. Figure 4.12 shows the AFM measurement for a bare AlGaN/GaN sample structure. Apart from a few big peaks that are considered to be errors caused from the AFM tip, qualitatively, the surface appears smooth when compared to Figure 4.13, which shows the AFM measurement for an AlGaN/GaN sample with recess etching applied. Figure 4.14 shows the surface for an AlGaN/GaN sample with both recess etching and fluorine treatment applied and it can be seen that the surface after the fluorine treatment is similar to that after recess etching. Thus, it is confirmed that recess etching and fluorine treatment leads to increased surface damage.

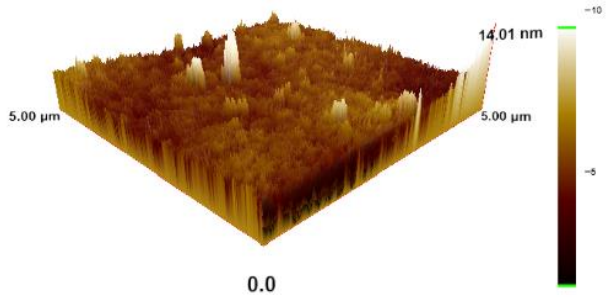


Figure 4.12 3D AFM measurement of an AlGaN/GaN heterostructure without recess or fluoine treatment (bare sample).

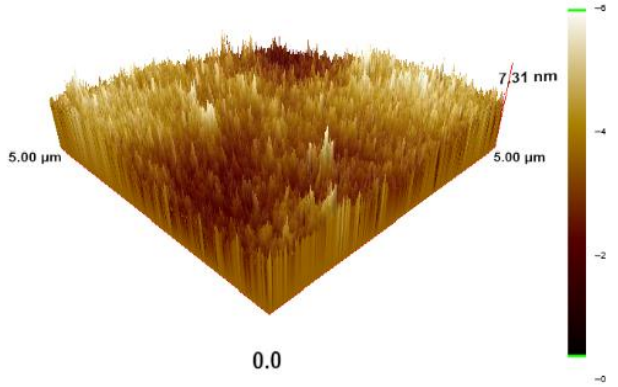


Figure 4.13 3D AFM measurement of an AlGaN/GaN heterostructure with recess.

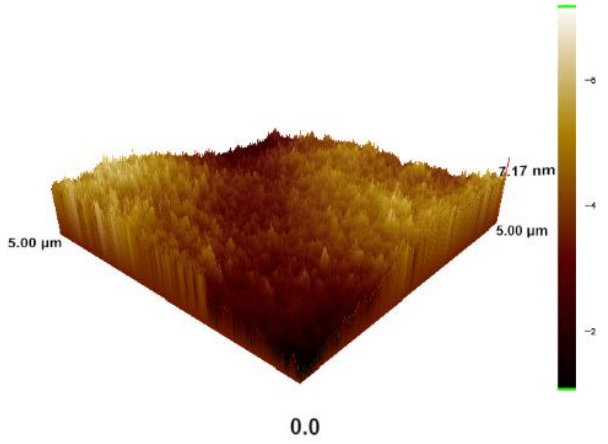


Figure 4.14 3D AFM measurement of an AlGaN/GaN heterostructure with recess and fluorine treatment.

After the fluorine treatment is completed the samples are cleaned in preparation for the gate dielectric deposition. Acetone and isopropanol alcohol rinse and oxygen plasma treatment are used. 10 nm Al_2O_3 is deposited with ALD. 100 cycles at a rate of 1 Å/cycle are utilized to deposit 10 nm of Al_2O_3.

After the gate dielectric deposition the gate lithography is repeated to form the patterns for the gate contacts. Ni/Au (50/300 nm) is evaporated using e-beam evaporation. The metallization parameters are shown below.

Table 4.15 Deposition thickness and rate for gate metallization.

Material	Deposition Thickness (nm)	Deposition Rate (Å/sec)
Ni	50	0.8
Au	300	1.8

Liftoff is done with acetone and the samples are cleaned. The image of the sample after liftoff is shown in Figure 4.15.

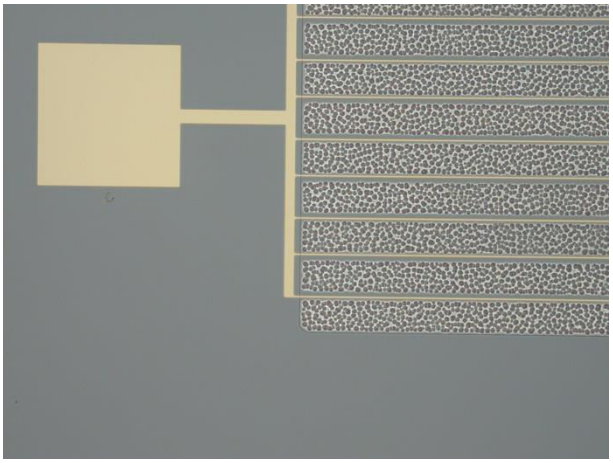


Figure 4.15 Optical microscope image of the sample after gate formation.

Dielectric Deposition and Opening

SiN_x passivation layer is deposited using the Sentech SI PPD Plasma Enhanced Chemical Vapor Deposition System. 240 nm of SiN_x was deposited using silane (SiH_4), ammonia (NH_3), and argon (Ar) as source gases. The recipe parameters are shown in the table below.

Table 4.16 SiN_x deposition process utilizing PECVD.

SiH_4 (sccm)	**NH_3 (sccm)**	**Ar (sccm)**	**RF Power (W)**	**Temperature (°C)**	**Pressure (Pa)**	**Deposition Rate (nm/min)**
300	15	300	50	300	80	10

The dielectric in the region of the metal contacts must be removed to be able to make electrical connections to the contacts. The gate dielectric in the contact regions is also removed in this step. The dielectric openings are patterned with the same procedure as the mesa step.

The dielectric etching was done using the Samco ICP RIE system using SF_6 and Ar gases. The process time was calculated for a 150% overetch to ensure the complete removal of the SiN_x layer and the duration was 3 minutes 45 seconds. The process parameters are given in the table below. The sample after passivation and the opening step is displayed in Figure 4.16.

Table 4.17 SiN_x opening etch process utilizing ICP RIE.

SF_6 (sccm)	**Ar (sccm)**	**ICP Power (W)**	**RF Power (W)**	**Pressure (Pa)**	**Etch Rate (nm/min)**
300	300	60	40	0.6	100

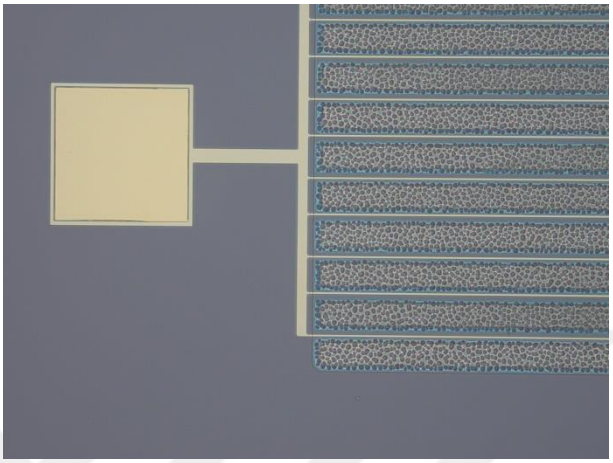


Figure 4.16 Optical microscope of the sample after the passivation and opening etch steps.

Air Bridge

The transistors in this fabrication have multiple fingers so air bridges must be formed before the interconnect deposition. First the samples are cleaned by sonication in acetone and rinsing with alcohol. A dehydration bake is done at 200°C for 5 minutes. HMDS is spin-coated at 2000 rpm for 40 seconds with a 10 second ramp to promote adhesion. S1828 positive mode photoresist is then spin-coated at 6000 rpm for 40 seconds with a 10 second ramp. After edge bead removal the samples are patterned with a photomask and exposed with 141 mJ/cm^2 of UV light. The samples are developed with AZ 326MIF for 5 minutes. Photoresist reflowing is achieved by baking the samples for 5 minutes at 200°C to obtain rounded photoresist structures. The thermal softening and roundening (reflow) of the air bridge posts is checked using an optical microscope.

Interconnect

The photolithography for the interconnect step is carried out using AZnLOF 2070 photoresist. The thickness of the metal to be deposited for the interconnection layer, close to 2 µm, is greater than the previous metal depositions so a greater photoresist

thickness is required, which is achieved with AZnLOF 2070. The resist is spin-coated at 4000 rpm for 40 seconds with a 10 second ramp. The coated samples are baked for 7 minutes at 100°C. After edge bead removal the samples are patterned using a photomask with a 200 mJ/cm^2 dose of UV light. A 1 minute reversal bake at 110°C is carried out and then the samples are flood exposed with a 1000 mJ/cm^2 dose of UV light. The patterned samples are developed using AZ 826MIF. The development takes 80 seconds. The resolution, critical dimension, and alignment mismatch are checked with an optical microscope. Oxygen plasma treatment is applied before the metal deposition.

Ti/Au (200/2000 nm) is evaporated with the e-beam system. The deposition rate for Ti begins at 2 Å/sec and is then increased to 3 Å/sec and then to 4 Å/sec. The Au layer is deposited at five different increasing rates. The parameters can be seen in the table below.

Table 4.18 Deposition thickness and rate for interconnect metallization.

Material	Deposition Thickness (nm)	Deposition Rate (Å/sec)
Ti	50	2
	50	3
	100	4
Au	200	2
	200	4
	200	6
	200	8
	1200	10

Liftoff is done using NMP as a solvent. The samples are soaked overnight. The liftoff process can be assisted with a syringe or sonication if necessary.

The final step in the fabrication is to remove the air bridge posts. This is achieved by soaking the samples in AZ100 solution on hot plate at 120°C for 3 hours. After 3 hours the samples are removed and rinsed with water. The samples are rinsed with acetone and isopropanol alcohol. Sonication and oxygen plasma treatment can be used if deemed necessary for cleaning. The optical microscope image of fabricated devices is shown in Figure 4.17.

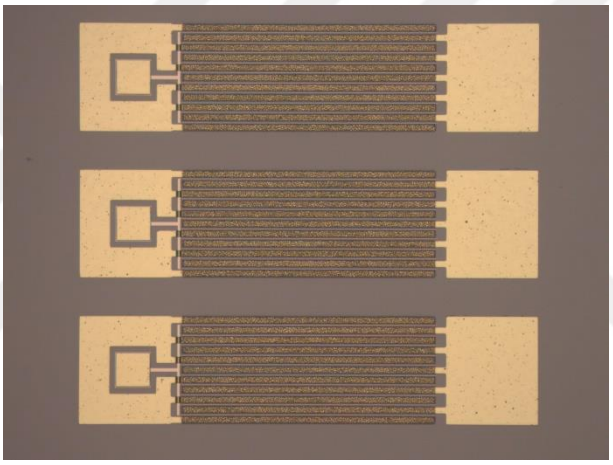


Figure 4.17 Optical microscope image of the fabricated MISHEMT devices.

Chapter 5

Electrical Characterization and Discussion

This chapter focuses on the electrical characterization of the fabricated HEMT devices and discussion. In order to characterize the fabricated devices, detailed measurements are conducted. Various DC and leakage measurements are carried out and the threshold voltage, drain current density, breakdown voltage and leakage characteristics are extracted in order to analyze device performance parameters.

5.1 Measurement Setups

The measurements were carried out using a Keysight B1500A Semiconductor Device Analyzer and probe station. Three probe transistor measurements are carried out to characterize the fabricated devices. Different parameters of the transistors are extracted from the measurements.

Transfer characteristics (I_d-V_{gs}) measurements are carried to extract the threshold voltages (V_{th}) of the fabricated devices. In the transfer characteristic measurement the drain voltage is held constant at V_d = 10 V. The drain current is measured as the gate voltage is varied. From the obtained measurement the threshold voltage is obtained as the gate voltage of the intersection of the linear extrapolation at maximum slope (maximum transconductance). The drain leakage current density is also extracted from the transfer characteristics measurements. The drain leakage current density ($I_{d,leak}$) is defined as the drain current density at a gate voltage V_{gs} where the transistor

is fully pinched off, for example, at a gate voltage of V_{gs} = -6 V for a transistor with a threshold voltage of V_{th} = -3 V. These definitions are demonstrated in Figure 5.1.

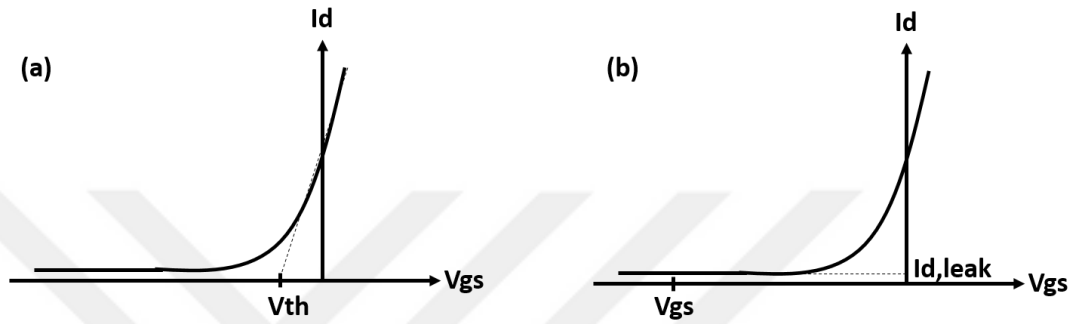


Figure 5.1 Definition of the (a) threshold voltage (V_{th}) and (b) drain leakage current density ($I_{d,leak}$) extracted from the transfer characteristics measurements.

Output characteristic (I_d-V_{ds}) measurements are carried out to extract the saturated drain current density (I_{dss}). For the output characteristic measurement the drain voltage is varied for constant gate voltage and the measurement is repeated for increasing gate voltages. The saturated drain current density is extracted as the maximum drain current density for a gate voltage of V_{gs} which corresponds to the turn-on voltage of the gate-source diode (Figure 5.2).

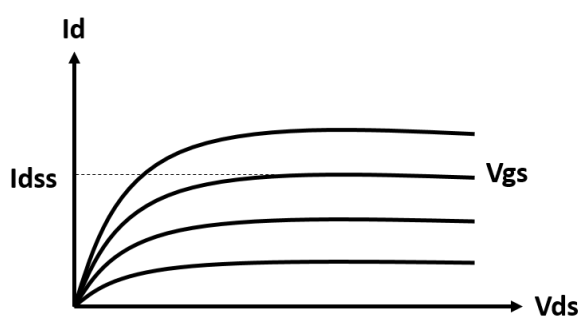


Figure 5.2 Definition of the saturated drain current density extracted from the output characteristics measurements.

The gate leakage current density is determined by measuring the gate current for varying gate-source voltages (Figure 5.3). In this measurement the drain is left

floating, voltage is applied between the gate and the source and the gate current is measured. The gate leakage current density is then extracted as the gate current at a gate voltage V_{gs} where the transistor is fully pinched off, for example, at a gate voltage of V_{gs} = -6 V for a transistor with a threshold voltage of V_{th} = -3 V.

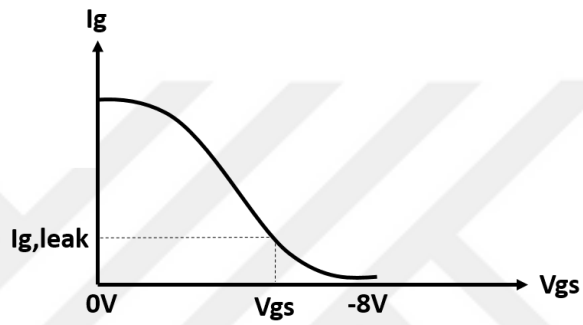


Figure 5.3 Definition of the gate leakage current density extracted from I_g-V_{gs} measurements.

The off-state breakdown voltage is measured by sweeping the drain voltage while the gate voltage is held constant at a voltage where the transistor is fully pinched off. A drain current compliance value is set, typically according to the size of the transistor being measured. When the measured current reaches the set compliance value the corresponding drain voltage is extracted as the breakdown voltage. This definition is demonstrated in Figure 5.4.

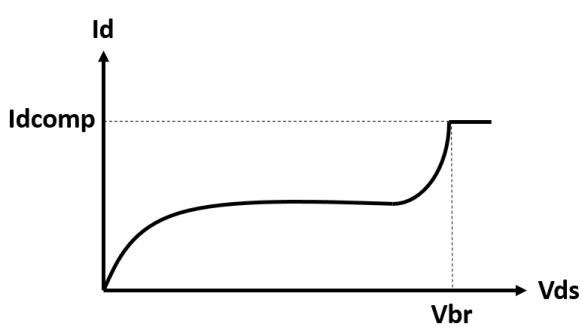


Figure 5.4 Definition of the off-state breakdown voltage.

5.2 Results and Discussion

5.2.1 p-GaN Gate HEMTs

InAlN/GaN HEMTs possess a high 2DEG density and therefore large negative threshold voltage; the p-GaN gate is expected to shift the threshold voltage towards the positive side, however reaching a positive threshold voltage is challenging. The transfer characteristics are measured from V_{gs} = -6 V to 4 V and the obtained result in shown in Figure 5.5. The threshold voltage extracted from the device is obtained as -16 mV, which is significantly higher than the threshold voltage obtained from devices without p-GaN. The I_d-V_{gs} plot displays two regions with different slopes, which corresponds to 2 peaks in the transconductance; this is a result of the p-GaN gate. The drain leakage current density is extracted at a gate voltage of V_{gs} = -6 V and is obtained as 277 µA/mm.

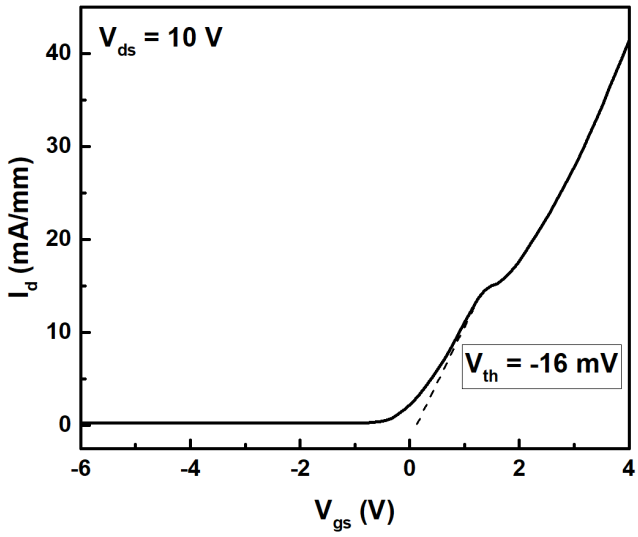


Figure 5.5 Measured transfer characteristics of the fabricated p-GaN gate InAlN/GaN HEMT.

Figure 5.6 displays the measured output characteristics. The IV measurements are carried out for gate voltages between -1 V and 4 V and the drain voltage is varied from 0 V to 10 V. The saturated drain current density is obtained at a gate voltage of

V_{gs} = 3 V as 26.6 mA/mm. Due to the depletion of the 2DEG by the p-GaN layer, the drain current density is lower than what can be achieved for InAlN/GaN transistors.

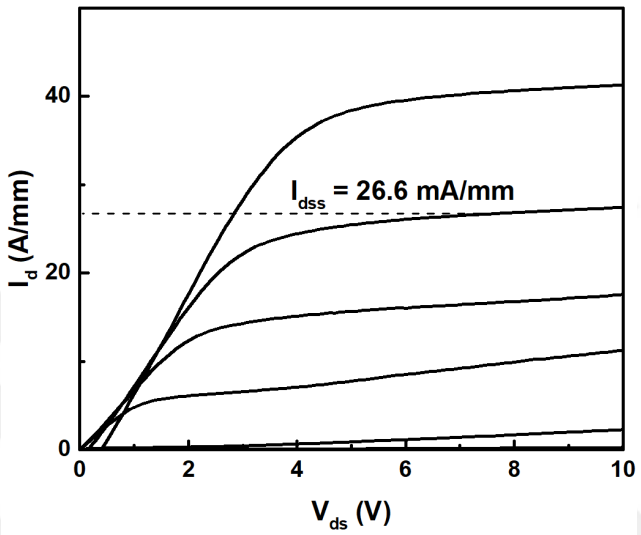


Figure 5.6 Measured output characteristics of the fabricated p-GaN gate InAlN/GaN HEMT.

The measured I_{gs}-V_{gs} characteristics are given in Figure 5.7. The measurement is carried out from a gate voltage of -8 V to 6 V with the drain pad floating. The gate leakage current density is obtained as 0.46 µA/mm at a gate voltage of -6 V.

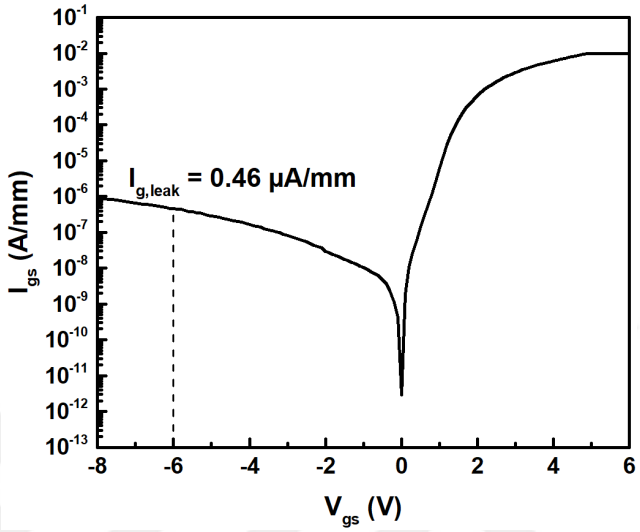


Figure 5.7 Measured I_{gs}-V_{gs} characteristics of the fabricated p-GaN gate InAlN/GaN HEMT.

The off-state breakdown measurement is carried out at a gate bias of V_{gs} = -4 V and the drain voltage is swept from 0 V to 150 V. The obtained result is shown in Figure 5.8. The breakdown voltage is extracted as 35 V using the criteria of I_d = 1 mA/mm. The breakdown voltage can be improved by decreasing the leakage currents.

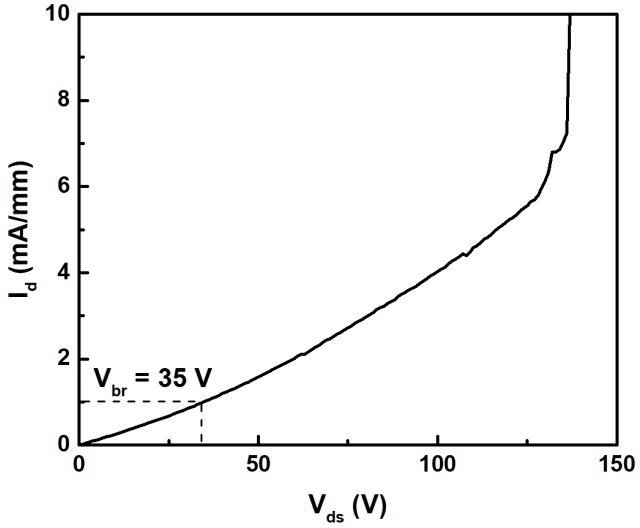


Figure 5.8 Measured off-state breakdown characteristics of the fabricated p-GaN gate InAlN/GaN HEMT.

The leakage currents of the p-GaN gate InAlN/GaN HEMT device are further analyzed by measurements taken from a leakage test pattern. The leakage test pattern consists of three metal contacts, ohmic, guard, and gate, and enables the measurement of the bulk (I_{bulk}) and surface (I_{surf}) leakage components separately [60]. Figure 5.9 shows the measurement result and the inset shows the optical microscope image of the leakage test pattern. The measurement results show that the surface leakage current is greater than the bulk leakage current component. Typically, in passivated HEMTs the bulk leakage current is greater than the surface leakage current. In the fabricated p-GaN gate InAlN/GaN HEMT the reverse is observed, indicating that the major component of the leakage in this device is due to the remaining p-GaN in the regions between the gate and source or drain.

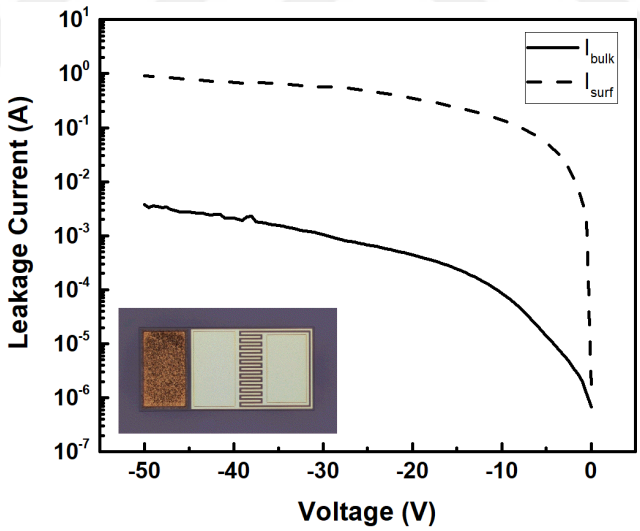


Figure 5.9 Measured bulk and surface leakage current characteristics of the fabricated p-GaN gate InAlN/GaN HEMT and the leakage test pattern (inset).

5.2.2 Recessed MISHEMTs

The fabricated MISHEMTs contain 10 nm recess etch and fluorine treatment so it is expected that the threshold voltage will be shifted to the positive side. The transfer characteristics are measured from V_{gs} = -4 V to 8 V and the obtained result in shown in Figure 5.10. The threshold voltage extracted from the device is obtained as 2.84 V.

The drain leakage current density is extracted at a gate voltage of Vgs = -1 V and is obtained as 9.61 µA/mm.

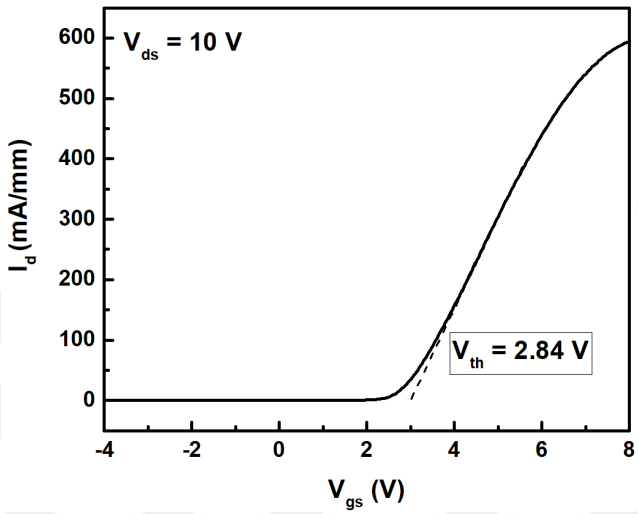


Figure 5.10 Measured transfer characteristics of the fabricated recessed AlGaN/GaN MISHEMT.

The measured output characteristics are given in Figure 5.11. The gate voltage is varied from -2 V to 6 V. The drain voltage is swept from 0 V to 12 V. From this graph, the normally-off operation can also be seen. For the gate voltages below 2 V the transistor is off and only leakage current is present. For gate voltages above 3 V the transistor turns on, indicating that the threshold voltage is between 2 V and 3 V, which is in agreement with the result obtained from the transfer characteristic measurement. The drain current density is extracted at a gate voltage of 6 V and is obtained as 415 mA/mm. This drain current is expected to be lower than that which can be achieved for a normally-on device, due to the decrease in the 2DEG density caused by the gate recess and fluorine treatments. Thus, the normally-off operation leads to a tradeoff between the achievable threshold voltage and drain current density.

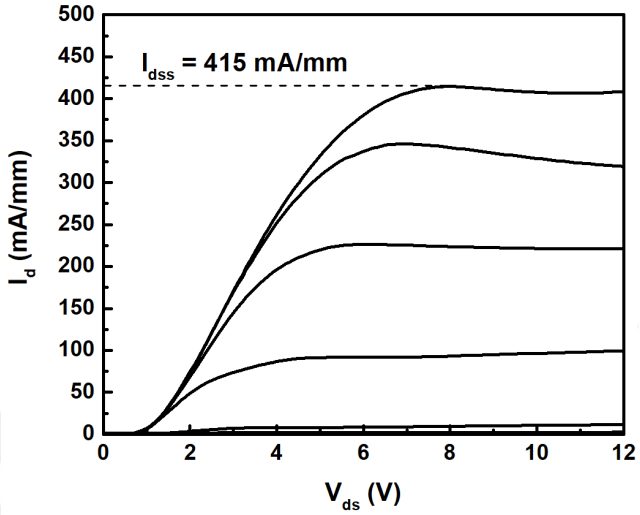


Figure 5.11 Measured output characteristics of the fabricated recessed AlGaN/GaN MISHEMT.

The measured I_{gs}-V_{gs} characteristics are shown in Figure 5.12 in semi-log scale. The gate leakage current density is extracted at a gate voltage of V_{gs} = -6 V and obtained as 16.7 µA/mm. In typical Schottky gate AlGaN/GaN HEMT devices large reverse leakage current is a disadvantage of the Schottky gate that leads to difficulty in achieving efficiency. Inductively coupled plasma etching methods that are used for gate recess processes of AlGaN/GaN HEMTs also cause plasma-induced damage which in turn causes surface roughening which eventually results in device performance degradation. The MISHEMT approach with the introduction of a of high dielectric constant (high-κ) material as a gate dielectric leads to reduction in gate leakage current, thus a reverse gate leakage current on the order of µA's can be obtained.

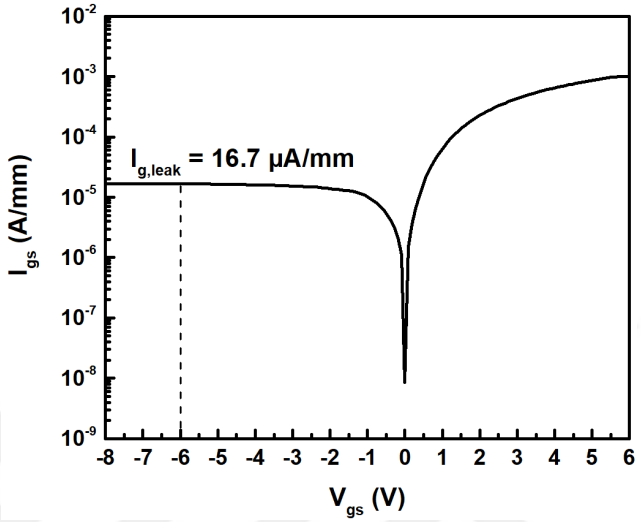


Figure 5.12 Measured I_{gs}-V_{gs} characteristics of the fabricated recessed AlGaN/GaN MISHEMT.

Figure 5.13 shows the off-state breakdown voltage of the MISHEMT device, measured at a gate bias of V_{gs} = -6 V and drain current criteria of 1 mA/mm, obtained as 63 V. A high breakdown voltage is desired for power electronic applications; this can be achieved through the introduction of field plates or buffer engineering.

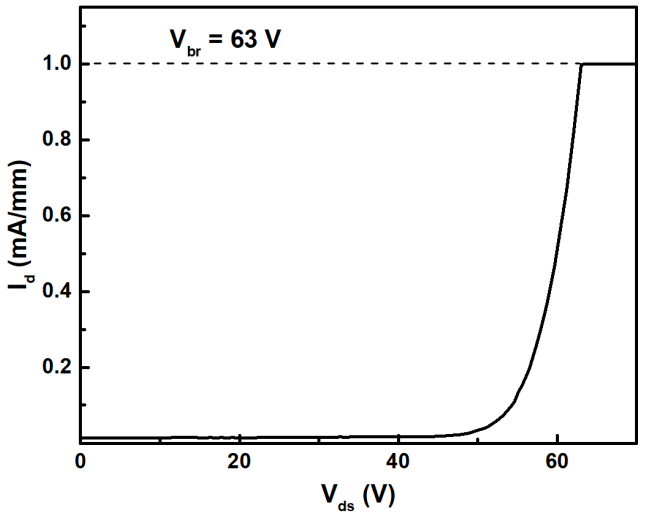


Figure 5.13 Measured off-state breakdown characteristics of the fabricated recessed AlGaN/GaN MISHEMT.

Chapter 6

Conclusion

Normally-off GaN HEMT devices are promising devices that are emerging as a superior alternative to silicon based power MOSFETs. GaN HEMTs are inherently normally-on devices and require additional device technologies to realize normally-off operation. Modulation of the 2DEG in the gate region only through the use of p-type layers, recess etching, or fluorine treatments can achieve normally-off operation without sacrificing too much of the advantages gained from the superior material properties of GaN.

In this thesis, normally-off HEMTs have been studied in detail through device simulations, fabrications, and electrical characterizations. Theoretical background review, theoretical analysis, physically-based device simulations, device fabrication and optimization and electrical characterization has been carried out.

The purpose of this work was to study normally-off HEMT devices for power electronics applications. Two different approaches have been studied to this end: the p-GaN gate HEMT and recessed MISHEMT. InAlN/GaN HEMTs have been studied as an alternative to AlGaN/GaN heterostructures. For the p-GaN gate InAlN/GaN HEMT, a threshold voltage of -16 mV was obtained, which may not be enough for normally-off operation, but corresponds to a great positive shift in threshold voltage by the p-GaN layer when it is considered that typical threshold voltages for standard InAlN devices can range from -8 V to -12 V. The threshold voltage can be further increased through optimizations of the epitaxial structure; by decreasing the thickness

of the barrier layer or including an AlGaN backbarrier, for example. The obtained saturation drain current density of 26.6 mA/mm is also low compared to the expectation for InAlN devices (possibly up to 1 or 2 A/mm can be achieved for standard InAlN HEMTs). The drain current is believed to be diminished by the p-GaN layer that remains in the access regions of the device. The gate leakage current density is extracted as 0.46 µA/mm, which is a good value, however, the breakdown voltage is extracted as 35 V, which is low for power electronic applications, due to high off-state leakage currents, indicating that there is room for improvement in the leakage current performance. A detailed analysis of the bulk and surface leakage currents carried out through measurements from a specialized test pattern reveal that the dominating leakage component is the surface leakage current. Generally, for SiN_x passivated devices the bulk leakage current is the dominant factor, which is the opposite of what is obtained for the p-GaN gate InAlN/GaN HEMT. The high surface leakage current is attributed to the remaining p-GaN layer in the access regions. Thus, for the p-GaN gate HEMT approach with the InAlN/GaN heterostructure, a shift in the threshold voltage towards to positive side has been demonstrated, however, the full potential of the advantages of the InAlN/GaN system have not been achieved due to fabrication challenges relating to the selective etching of p-GaN. As the p-GaN etch recipe with high selectivity ($BCl_3/Cl_2 + Cl_2/O_2$) also etches metals, it cannot be after the gate contact formation to etch the p-GaN in the access regions. On the other hand, the gentler BCl_3 based etching recipe can be used even when there are metal contacts on the sample owing to its slow etch rate, however, the selectivity of this recipe is low, hence, in order to guarantee that the InAlN barrier layer is not damaged, the p-GaN layer in the access layer cannot be fully etched but only made thinner. The most straightforward method to address the issues relating to the etching of the access region p-GaN layer would be to redesign the photomask and/or process flow such that the sample surface can be protected by photoresist during the access region p-GaN etch or the etch can be carried out before the contact deposition steps.

For the recessed MISHEMT approach with the AlGaN/GaN heterostructure, normally-off operation with a threshold voltage 2.84 V, and moderate drain current density, gate leakage current density, and breakdown voltage of 415 mA/mm, 16.7 µA/mm, and 63 V, respectively, has been realized. A threshold voltage of 1.5 V is typically considered as the minimum required threshold voltage for safe normally-off operation, thus, reliable normally-off operation is achieved with this design. Further improvements can be made to this design by tuning the recess depth and fluorine treatment parameters to the optimal values such that the tradeoff between threshold voltage and drain current density gives maximum values for both characteristics. The breakdown voltage can be improved further through the additions of field plate structures.

The detailed analysis of the p-GaN gate HEMT and recessed MISHEMT devices reveals advantages and challenges for both devices. The p-GaN gate approach to obtaining normally-off operation is a reliable method with good uniformity in the obtained threshold voltages. However, the device fabrication is more challenging compared to the recessed MISHEMT structure and does not allow for compromises in the fabrication. The recessed MISHEMT structure provides more controllability of the threshold voltage through the process parameters of the recess depth, fluorine treatment, gate dielectric thickness, however, this can also lead to homogeneity issues across samples (i.e. if the recess etch process has poor uniformity etc.).

In power electronics applications normally-off devices are desired to guarantee a safe operation, reliability, and a simple gate drive configuration. GaN-based materials have excellent figures of merit to be utilized electron devices such as power transistors. For GaN-based technologies to become a replacement for silicon power MOSFETs rather than being a niche technology like GaAs technology, it must enable significant new applications, be easy to use, be cost effective to the user and be reliable. In the voltage range up to 650 V, devices that are competitive in terms of switching speed, size, cost, and reliability have already been achieved for

commercially available devices. GaN research programs into the next level technologies are continuing with no shortage, with special interest in electric cars and photovoltaic applications.

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