TWO-STAGE BROADBAND CLASS-AB HIGH POWER AMPLIFIER DESIGN USING GAN HEMT TECHNOLOGY

A Thesis

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Dedicated to My Family

ABSTRACT

Modern radio systems need broadband, high power, high efficiency power amplifiers to cover a wide frequency spectrum with reliable system performance. Linearity is another critical parameter in power amplifier design and there is a trade-off between linearity and efficiency. Class-AB design presents a compromise in terms of linearity and efficiency for the radio frequency systems. In this thesis, a two-stage broadband high power amplifier design using GaN HEMT technology is presented. Simulations and measurements are based on transistor models provided by the manufacturer. The design has minimum of 43% power added efficiency (PAE) and 47.3 dBm output power over 0.5 - 2.5 GHz operating frequency.

ÖZETÇE

Modern radyo sistemleri, güvenilir sistem performansıyla geniş bir frekans spektrumunu kapsamak için geniş bantlı, yüksek güçlü, yüksek verimli güç yükselteçlerine ihtiyaç duyar. Lineerlik güç yükselteci tasarımında diğer bir kritik parametredir ve lineerlik ve verim arasında bir ödünleşim vardır. AB sınıfı tasarım radyo frekansı sistemleri için lineerlik ve verimlilik yönünden bir uzlaşma sunmaktadır. Bu tezde GaN HEMT teknolojisini kullanan iki aşamalı geniş band yüksek güçlü yükselteç tasarımı sunulmaktadır. Simülasyonlar ve ölçümler üretici tarafından sağlanan transistör modellerine dayanmaktadır. Tasarım 0.5 - 2.5 GHz çalışma bandında minimum 43% güç eklemeli verimlilik ve 47.3 dBm çıkış gücüne sahiptir.

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CHAPTER I

INTRODUCTION

A Power amplifier (PA) is one of the most important devices for radar, guidance, radio communication and electronic warfare systems. It is the most dominant component determining overall power consumption and heat dissipation of such systems. Having highly efficient and wideband PAs leads to not only reducing power consumption and self-heating but also improves reliability of modern RF transmitters. Complexity of modern RF systems continues to increase in pursuit of very high data rates which necessitate transceivers capable of broadband operation while maintaining high spectral efficiency. High spectral efficiency requires linear operation of RF transmitters such that their impact on complex modulation schemes (such as quadrature amplitude modulation) is minimized. Therefore, output power, linearity and efficiency of PA are crucial in modern radio frequency systems [1], [2] [3].

There are various technologies to build power amplifiers. Microwave Power Module (MPM), Traveling Wave Tube Amplifier (TWTA) and Solid-State Power Amplifier (SSPA) are three essential power amplifier technologies. Among the solid-state technologies, Gallium-Nitride (GaN) High-Electron Mobility transistors (HEMT) comes to the forefront for high power microwave applications with their high power density, high breakdown voltage, high saturated electron mobility, good thermal conductivity, low turn-on resistance and compact footprint [4], [5].

In this thesis, two-stage broadband Class-AB high power amplifier using GaN HEMT technology and operating from 0.5 to 2.5 GHz is presented. Figure 1 demonstrates the block diagram of the two-stage design. Two-stage power amplifier consists

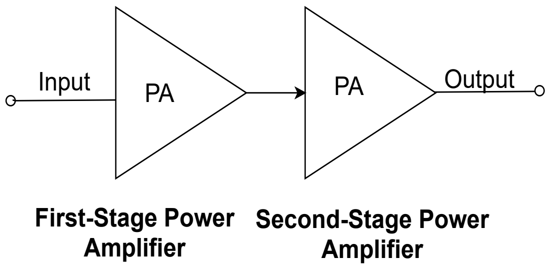


Figure 1: Block diagram of the two-stage PA

of the first- and second-stage power amplifiers. First- and second-stage power amplifiers are first designed individually, then optimized together and finally fabricated. Two-stage design has minimum of 43% power added efficiency (PAE) and 47.3 dBm output power over the 0.5 - 2.5 GHz operating frequency.

In Chapter II, fundamentals of power amplifiers are explained. Chapter III investigates design and measurements of the first-stage PA and Chapter IV presents the second-stage PA design and characterization. Cascaded two-stage, broadband amplifier design and measurements are provided in Chapter V. Finally, concluding remarks and comments on future direction are given in Chapter VI.

CHAPTER II

FUNDAMENTALS OF POWER AMPLIFIERS

2.1 Definition

Power amplifiers are among the fundamental devices in transmitter chains of wireless communication and radar systems. They comprise the last amplification stage before the antenna in transmitters and are designed with different goals depending on the application, such as high efficiency, high output power and flat gain in the operating band.

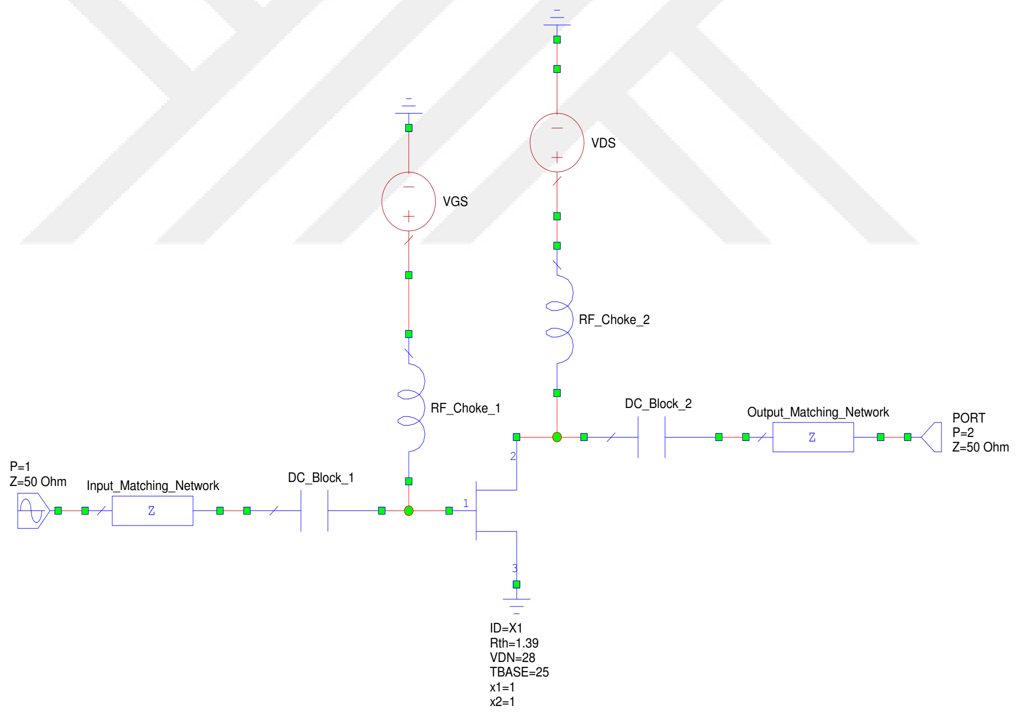


Figure 2: General power amplifier topology

Power amplifiers nominally operate in large-signal region wherein RF voltage amplitude is large enough to affect operating DC bias point of the amplifier. Changing DC operating point results in non-linearity which is an important metric in PA performance assessment. Since the dissipated power level by the power amplifiers is relatively high, they have an important role in determining thermal performance of the system [6]. Therefore, efficiency and linearity are crucial parameters for power amplifiers. Stability is another important parameter for the power amplifier to continue operating in the desired function unaffected by other conditions.

2.2 Efficiency

Power amplifier is the most dominant component determining overall power consumption and, consequently, heat dissipation of transmitters. Power amplifiers with high efficiency are required to reduce DC power consumption and self-heating. This results in operating cost reduction and improved reliability.

Efficiency of a power amplifier is a measure of how effectively it converts DC power to RF power. There are various different definitions of efficiency [7]. Drain efficiency is calculated as ratio of RF output power to DC power:

$$\eta = \frac{P_{out}}{P_{DC}} \tag{1}$$

Drain efficiency does not take into account RF input power which can be non-negligible in many cases. Power added efficiency (PAE), on the other hand, accounts for the input RF power and as such is widely used to characterize PA performance [8]. It is defined in equation 2:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2}$$

2.3 Gain Compression

Amplifiers nominally have constant gain with increasing input RF power level when operated in the small-signal region. However, as amplitude of the input signal increases, amplifiers begin to saturate and gain decreases. Input (output) 1-dB compression point P_{1dB} is an important measure of an amplifier's linearity. It is the input (output) power level at which amplifier gain is 1 dB below its small-signal value.

2.4 Stability

Stability is frequency dependent and an amplifier is said to be unconditionally stable if it is stable for all frequencies without being affected by the input and output load conditions. For an amplifier, either input reflection coefficient, $|\Gamma_{in}| > 1$ or the output reflection coefficient, $|\Gamma_{out}| > 1$, results in negative impedance, thus leads to oscillation also known as instability. Stability analysis can be formed graphically by using stability circles or calculated analytically. In this thesis, stability analysis is satisfied analytically by using the two-parameter test criterion (K-Δ Test) [9].

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{3}$$

and

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{4}$$

Amplifier is conditionally stable if below conditions are satisfied:

$$K > 1 \tag{5}$$

$$|\Delta| < 1 \tag{6}$$

If an amplifier is not stable, placing a resistor at input or output of the amplifier ensures unconditional stability. A resistor at amplifier input increases noise and reduces gain, while a resistor at the output degrades output power and efficiency. For PAs, noise is usually of secondary importance and resistors are placed at the input, if needed.

2.5 Power Amplifier Classes

Linear amplifiers and switching-mode amplifiers are two fundamental groups of amplifiers. Because this study aims to design a Class-AB power amplifier, only linear amplifiers are investigated in depth. There are four sub-classes of linear amplifiers: Class-A, Class-AB, Class-B and Class-C.

DC bias point determines which class amplifier operates in. Time the transistor is conducting is expressed as the conduction angle that changes between 0° and 360°. The conduction angle differs from the class of amplifiers. Table 1 presents comparison of the linear amplifier classes in terms of conduction angle and bias condition [7].

Table 1: Conduction angle and bias condition comparison for linear power amplifier classes

Amplifier Class	Conduction Angle	Bias Condition
A	2π (360°)	Middle of the Saturation and Cut-off
B	π (180°)	Cut-off
AB	$> \pi$ (180°)	Above Cut-off
C	$< \pi$ (180°)	Below Cut-off

2.5.1 Class-A Power Amplifiers

Class-A power amplifiers are the most linear amplifiers because they operate in always ON region. Conduction angle of Class-A power amplifiers is 360° and quiescent current of this class of amplifiers is half of the maximum drain current. Theoretical maximum efficiency is 50 % for Class-A power amplifiers [10]. Although linearity is the main advantage of these classes of amplifiers, they have the lowest efficiency.

2.5.2 Class-B Power Amplifiers

Class-B power amplifiers are biased at cut-off voltage and they amplify input signal for only half cycle. Conduction angle of the Class-B power amplifier is 180° and its quiescent current is zero. Maximum theoretical efficiency is 78.5 % for Class-B power amplifiers [11]. The transistor turns on and off for every half cycle of the input signal and this is the cause of nonlinear behavior of Class-B power amplifiers.

2.5.3 Class-C Power Amplifiers

Class-C power amplifiers conduct less than half cycle of the input signal. Their bias voltage is below the cut-off voltage to acquire a higher efficiency level than Class-B power amplifier. Conduction angle of Class-C power amplifiers is less than 180°. As a result, this class of PAs is the most non-linear resulting in distortion of input waveform. This type of amplifier is preferred in applications that can tolerate non-linearity, such as constant envelope systems [7].

2.5.4 Class-AB Power Amplifiers

Class-AB power amplifiers conduct for more than half cycle of the input signal and their bias voltage is above cut-off voltage; therefore, conduction cycle of Class-AB power amplifiers is between 180° and 360°. Class-AB is between Class-A and Class-B in terms of efficiency and linearity. Theoretical efficiency of this class of PAs is between 50 % and 78.5 % [12].

From Class-A to Class-C, conduction angle decreases and efficiency increases. On the other and, linearity and gain of the power amplifier decrease. Class-AB power amplifiers are one of the most preferred power amplifiers in modern RF systems since they offer a compromise between efficiency and linearity. In this thesis, design of a Class-AB, high power amplifier is pursued to achieve high efficiency with good linearity.

2.6 Simulation Techniques Used

All designs presented herein are simulated in Cadence AWR Design Environment [13].

Scattering parameters (S-parameters) are used to represent linear, small-signal behavior of microwave components [8]. Wolfspeed device libraries model transistors' small-signal performance as a function of DC bias point.

Large-signal simulations of active microwave devices are more complicated than small-signal simulations using S-parameters. Large-signal device models are a must to be able to design a power amplifier. These models not only enable prediction of network parameters (gain, input & output reflection coefficients) under large-signal stimulation but also enable efficiency and non-linearity calculations. Wolfspeed device libraries model large-signal behavior of the transistors as a function of DC bias point.

2.6.1 Load-pull and Source-pull Simulations

Maximum power transfer theorem states that load impedance must be equal to complex conjugate of source impedance to obtain maximum power transfer from source to load. However, maximum power transfer and conjugate termination notions are valid only for small-signal conditions and does not apply to power amplifiers [14]. Instead, there is a mathematical dependency between output power and output match. This situation is one of the principal differences between linear amplifier design and power amplifier design. In addition, some transistors, i.e. bipolar transistors, have remarkable relation between output power and input match [7]. Due to this dependence, transistors provide maximum output power only for a specific input and output impedance values. The goal of load- & source-pull simulations is to determine these specific impedance points. Using harmonic balance tuner, input and output impedance points are swept and resulting output power, large-signal gain, PAE are calculated.

CHAPTER III

DESIGN & MEASUREMENTS OF FIRST-STAGE BROADBAND CLASS-AB HIGH POWER AMPLIFIER

In this chapter, design and measurements of the first-stage power amplifier are described in detail. This stage is used to drive the 48 dBm second-stage PA and employs Wolfspeed's CGH40010F GaN HEMT device in class-AB operation. Primary design goals are summarized in Table 2. All simulations are carried out using large-signal model of the CGH40010F transistor in Cadence AWR Design Environment.

Table 2: Design goals of the first-stage of the broadband Class-AB high power amplifier

Output Frequency Range	0.5 - 2.5 GHz
Output Power	$>$ 40 dBm
PAE	$>$ 50%

3.1 Transistor Choice

The first step in power amplifier design is to select a proper transistor that can meet design specifications. It is necessary to use a transistor that can operate over the desired frequency range with acceptable gain and PAE. In this work, Wolfspeed's CGH40010F GaN HEMT device is selected for the first-stage due to its broadband gain and PAE performance and, equally importantly, its large-signal model availability.

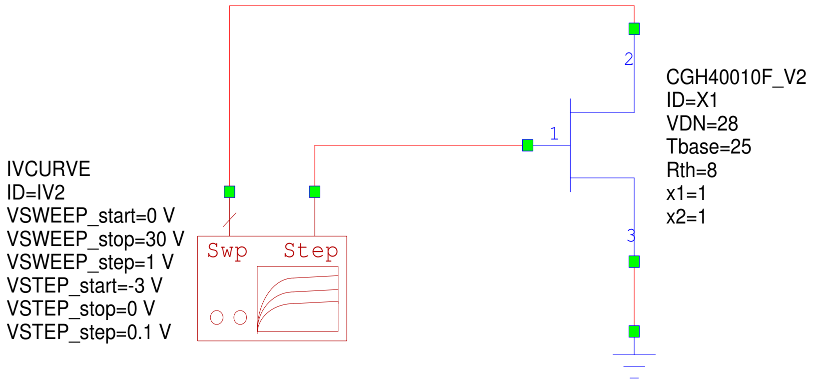


Figure 3: Schematic of circuit used in Cadence AWR Microwave Office for I-V curve analysis of CGH40010F

3.2 Bias Point Selection

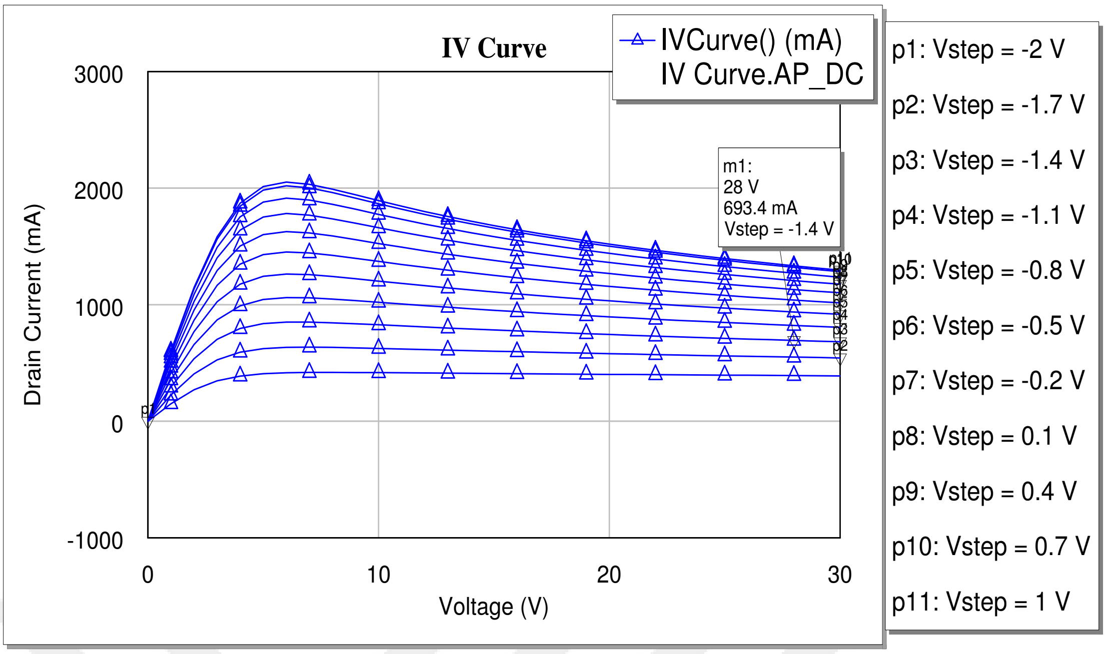
Next step after device selection is determining a proper DC operating point for the transistor to meet P_{out}, PAE, gain and harmonic suppression specifications. DC bias point determines which class amplifier operates in. Figure 3 presents circuit schematic used to generate I-V curves of the transistor.

For Class-A design, quiescent current I_{DQ} is half of the maximum drain current which is 1.34 A for CGH40010F, while zero quiescent current indicates Class-B operation. It is observed that $V_{GS} = -1.4$V is Class-A biasing point from Figure 4a. In order to better understand the Class-B point, Figure 4b can be used. It is seen that Class-B point is $V_{GS} = -3$V for CGH40010F.

The transistor is driven at Class-AB biasing point by adjusting gate voltage between these two values. In this thesis, biasing point is selected as V_{DS} = 28 V, V_{GS} = -2.1 V, I_{DQ} = 336 mA for Class-AB operation.

3.3 DC Biasing Network

A DC bias network, consisting of RF chokes and DC blocks, is designed to operate the transistor at the desired bias point with minimum impact on RF performance (match, noise, gain). Figure 5 shows the most common DC bias topology for power amplifiers.



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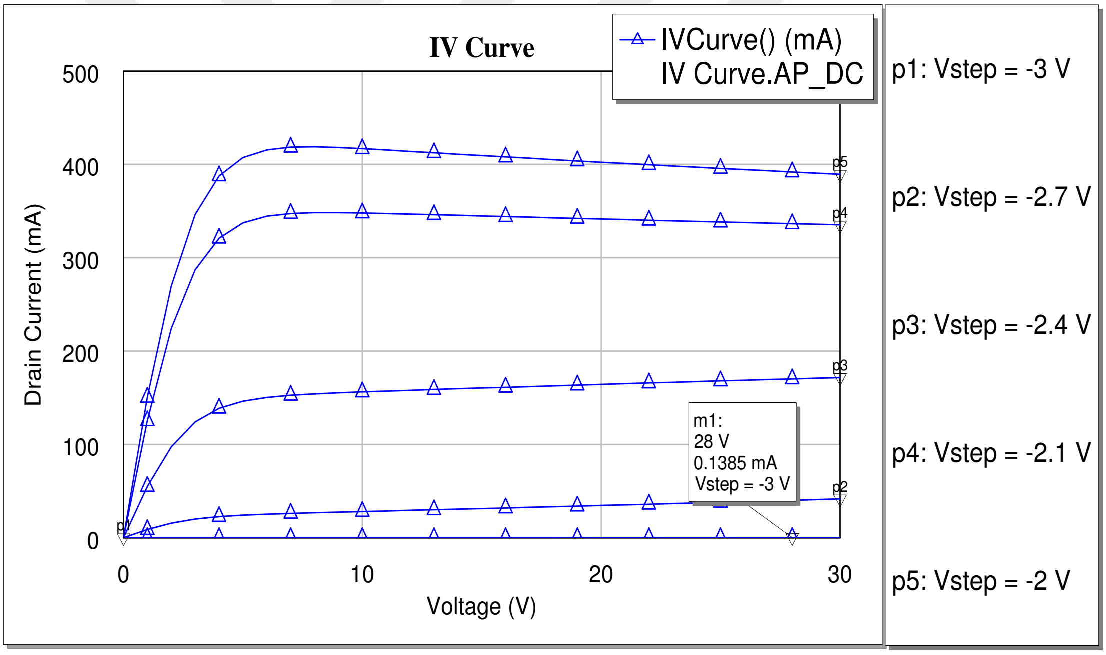


(b)

Figure 4: (a) I-V curves of CGH40010F, (b) close up of class-AB operation region

RF chokes have high impedance for high frequency signals, while capacitors have zero impedance at DC. Three important considerations pertaining to RF choke must be taken into account while designing a DC bias network with chokes:

- Impedance of the RF choke must be high enough at low frequencies to prevent

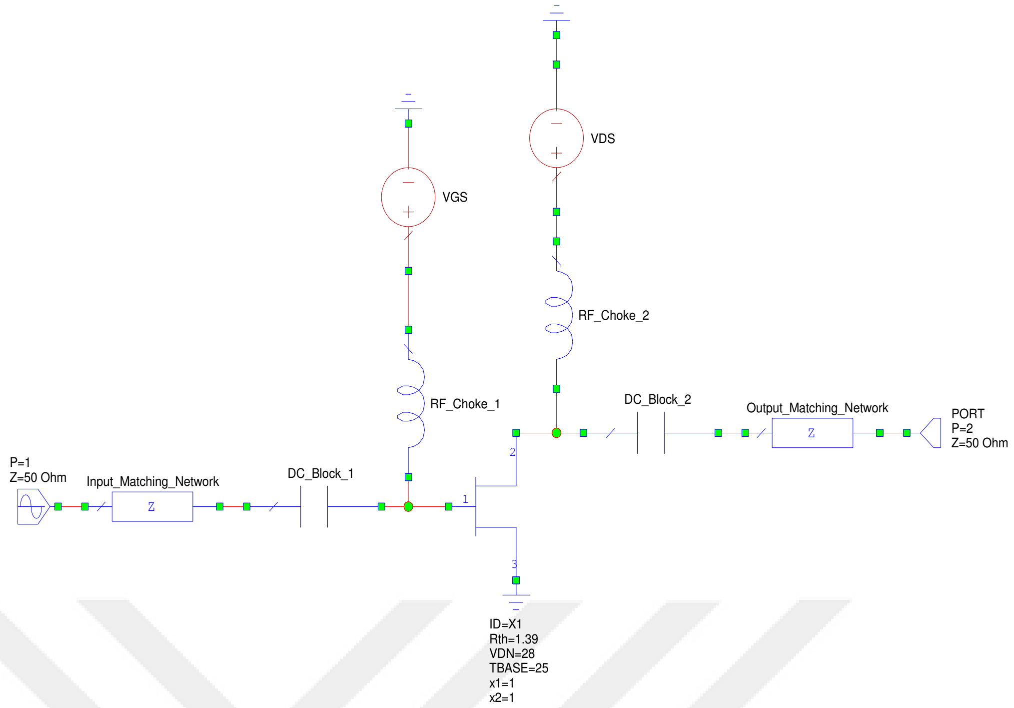


Figure 5: DC biasing network for the PA

RF leakage into DC lines;

- Real inductors have parasitic effects causing them to exhibit capacitive impedance beyond a certain frequency. Therefore, one must ensure the selected RF choke behaves as close to an inductor as possible within the desired frequency range;
- Transistor drain current flows through the RF choke necessitating chokes with large current handling capability.

In this thesis, Coilcraft 0603LS-241XJE is used as RF choke for both gate and drain lines. ATC 700A331JW is used as DC block capacitors at both input and output.

3.4 Load-pull and Source-pull Analyses

As explained in detail in section 2.6.1, load- & source-pull analyses are used in PA design wherein load and source impedance presented to a transistor are varied. Transistor's gain, efficiency and output power are calculated for each load and source

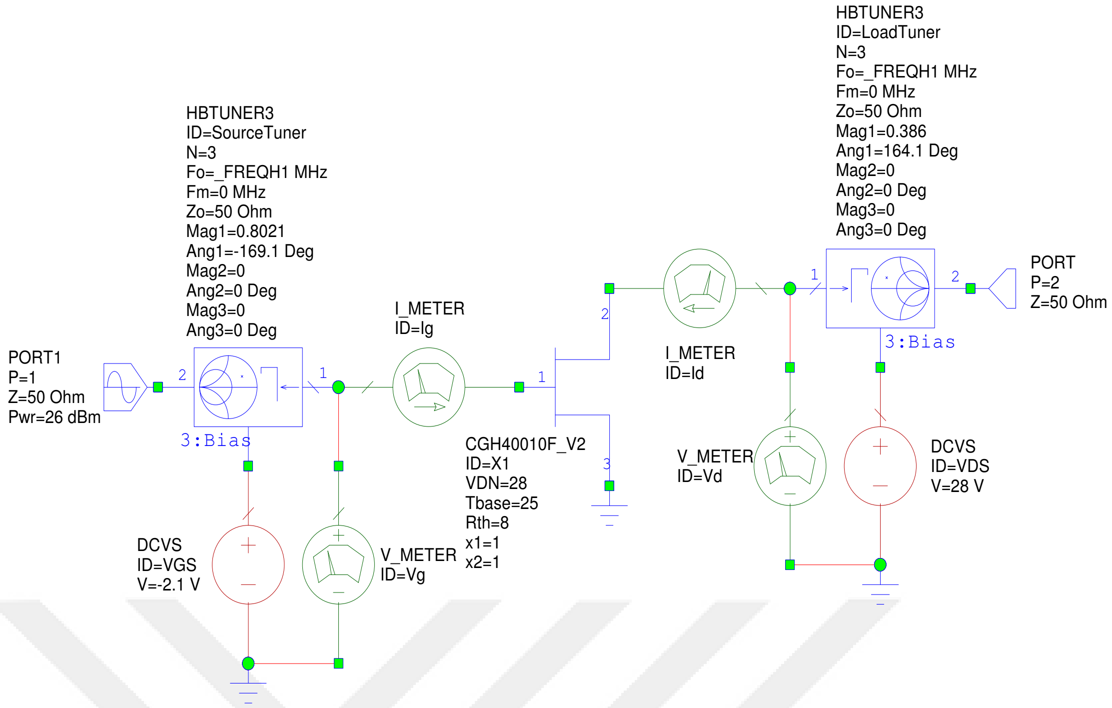


Figure 6: Load- & source-pull circuit for CGH40010F

impedance point to find those values which extract the most performance from the device. Analysis results are usually displayed on the Smith chart for each frequency.

Figure 6 shows the circuit schematic used to perform load- & source-pull analyses of CGH40010F while Figures 7-11 present load and source contours obtained at 0.5, 1, 1.5, 2 and 2.5 GHz. It is clearly observed that there is a compromise between maximum P_{out} and maximum PAE because power and PAE contours reach their maximum at different load impedance points on the Smith chart. The challenge of broadband design is to find the best compromise to achieve desired performance over a large frequency range. Impedance of the final input and output matching networks are also shown with red diamonds on each Smith chart.

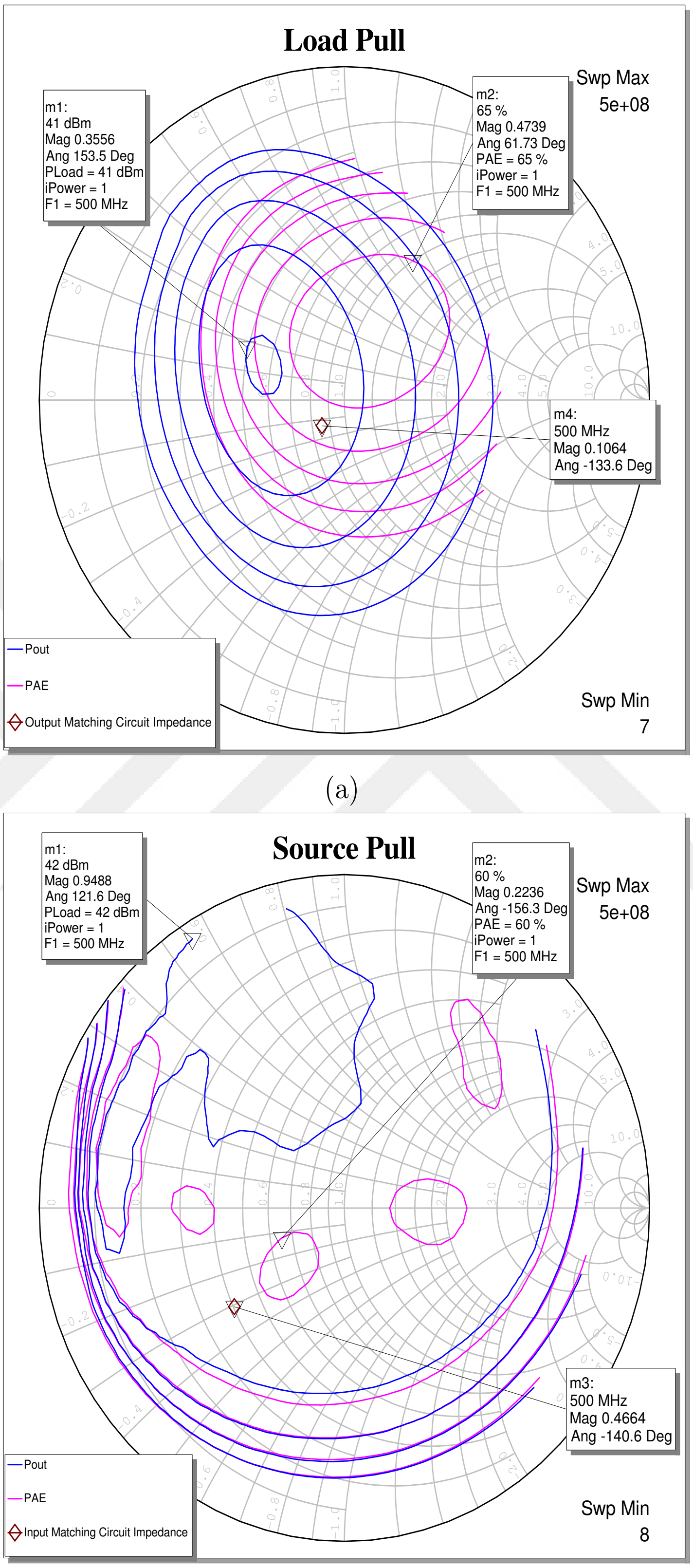
Load- & source-pull analyses are executed in an iterative fashion. First, the analyses are performed to obtain Γ_L (load reflection coefficient) and Γ_S (source reflection coefficient) by using power vs. efficiency contours on the Smith chart. Then, the process is repeated using reflection coefficients from first iteration as the new load and source impedance values, until desired P_{out} and PAE are simultaneously achieved in simulations.

It is also important to note that in non-linear operation, a transistor's input and output impedance depend strongly on input power level and bias voltage. Thus, load- & source-pull simulations must be conducted for a specific input power level and bias point to obtain proper impedance values. In this thesis, input power level and biasing conditions are chosen as 26 dBm and -2.1V/28V respectively for the load- & source-pull simulations.

3.5 Input and Output Matching Network Design

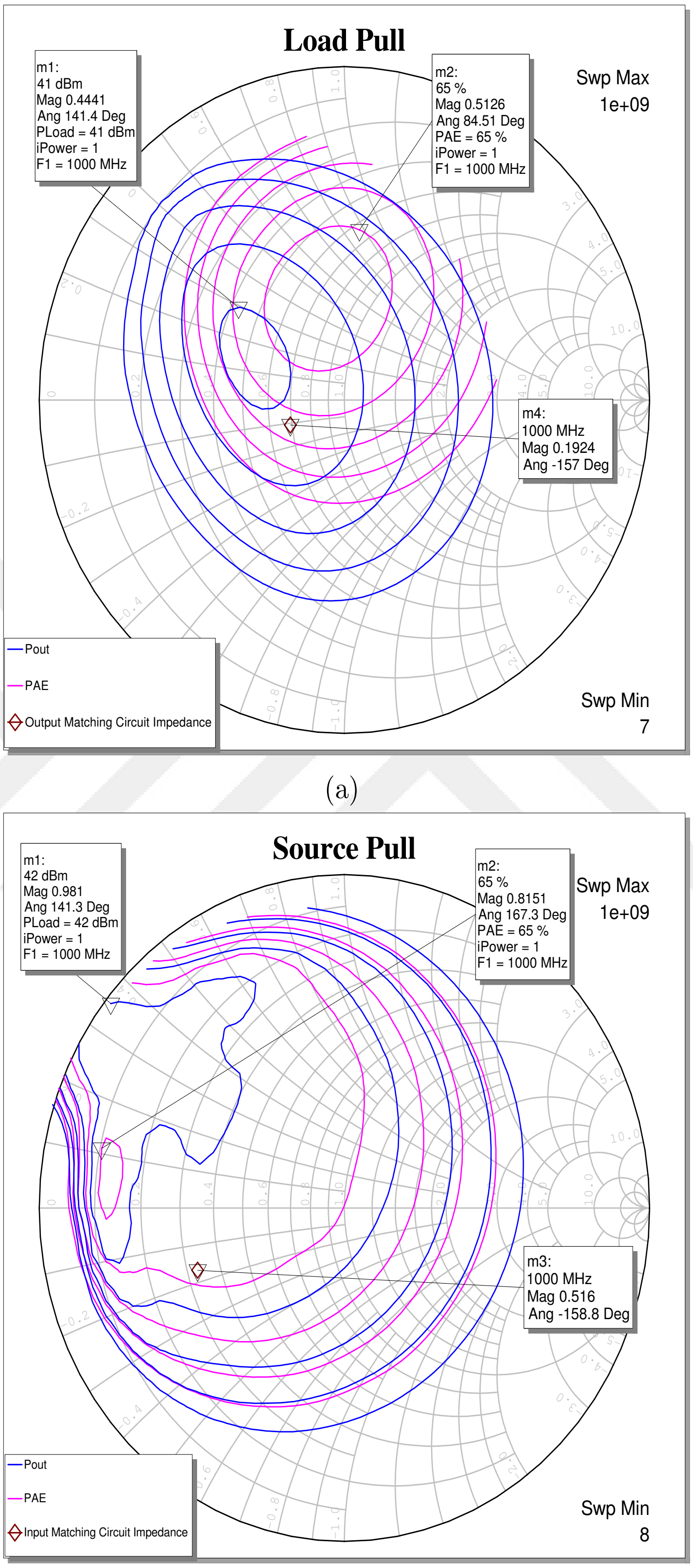
Once desired load and source impedance values are determined, next step is to design broadband input and output matching networks to transform 50 Ω to these values. It would not be an exaggeration to state that matching network ultimately determines PA performance as any deviation from desired performance degrades P_{out}, PAE, gain and/or harmonic suppression.

When designing a narrowband power amplifier, it is possible to design an input matching circuit by using conjugate of input impedance of the transistor in the middle of the frequency band. Load-pull is then conducted to maximize output power and PAE. However, determining input and output matching points is much more complex for broadband power amplifier design. In this thesis, network synthesis tool in Cadence AWR Design Environment is used as a first step in matching network design. It uses impedance values obtained from source- & load-pull analyses. Designs are then further refined manually to optimize performance. Microstrip matching is preferred due to ease of fabrication and less parasitic effects. Final designs of the matching networks of the first-stage PA are shown in Figure 12.



(b)

Figure 7: (a) Load- and (b) source-pull contours of CGH40010F at 0.5 GHz



(a)

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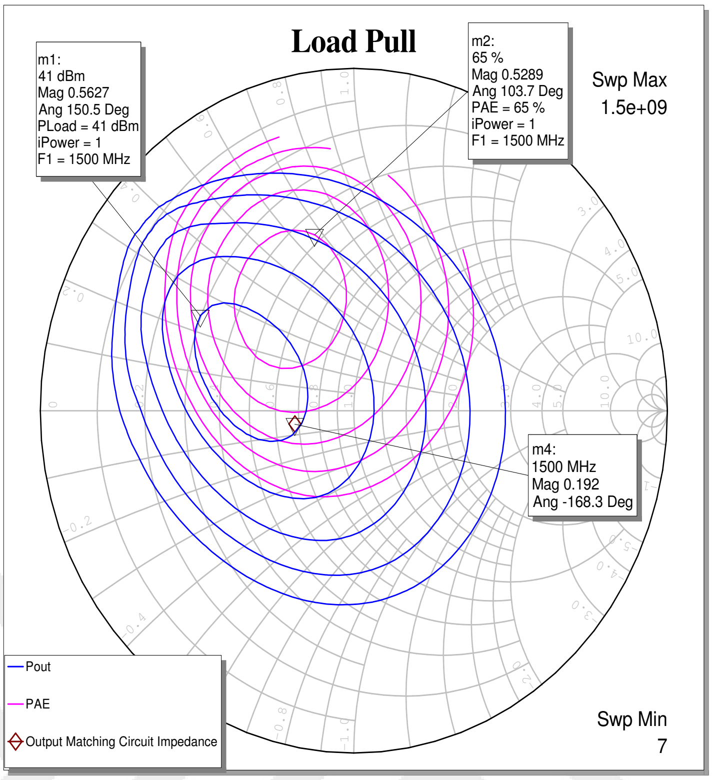
Figure 8: (a) Load- and (b) source-pull contours of CGH40010F at 1 GHz



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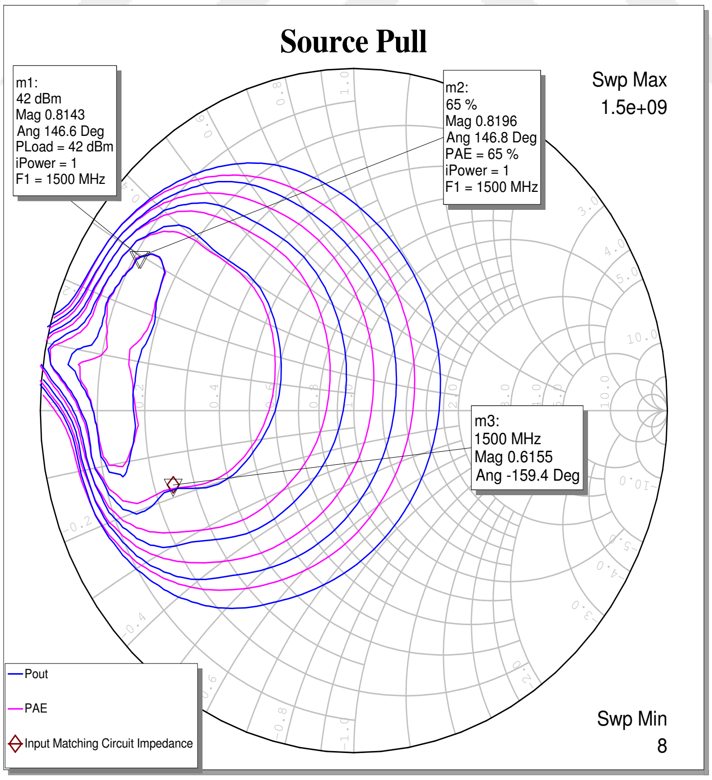

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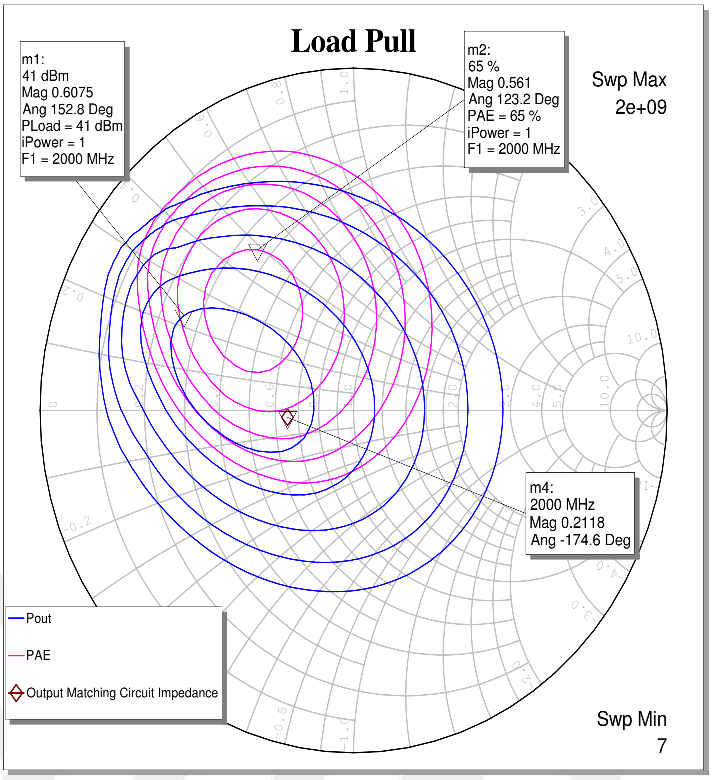
Figure 9: (a) Load- and (b) source-pull contours of CGH40010F at 1.5 GHz



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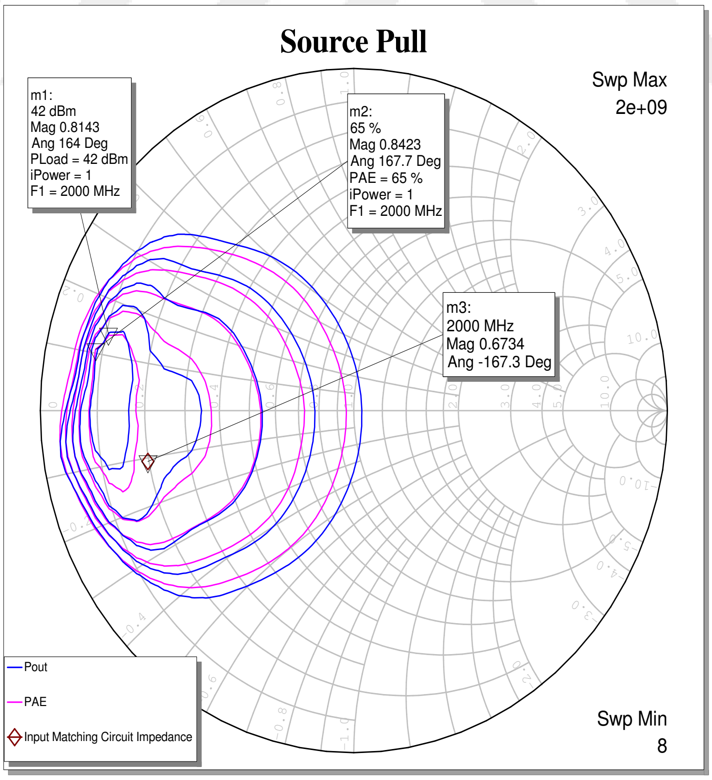

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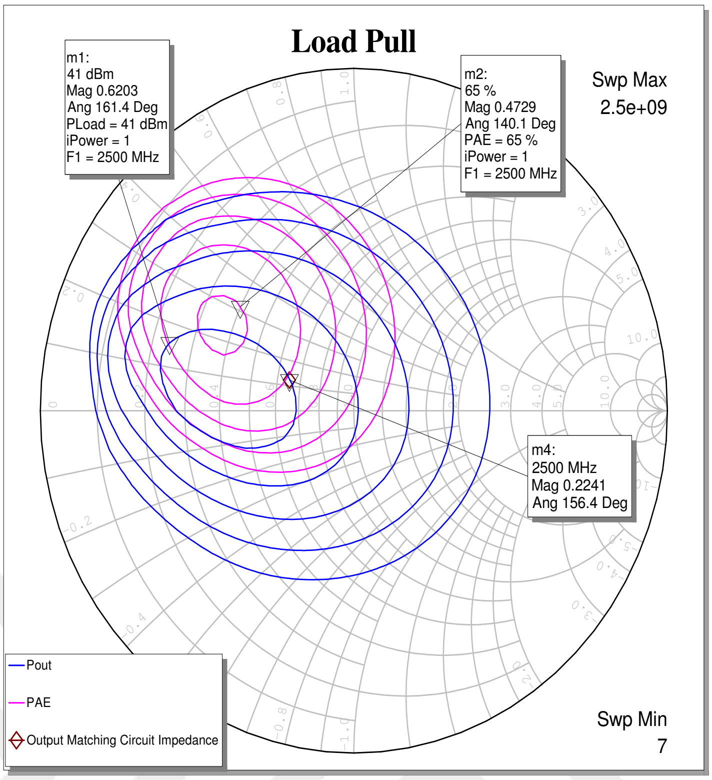
Figure 10: (a) Load- and (b) source-pull contours of CGH40010F at 2 GHz



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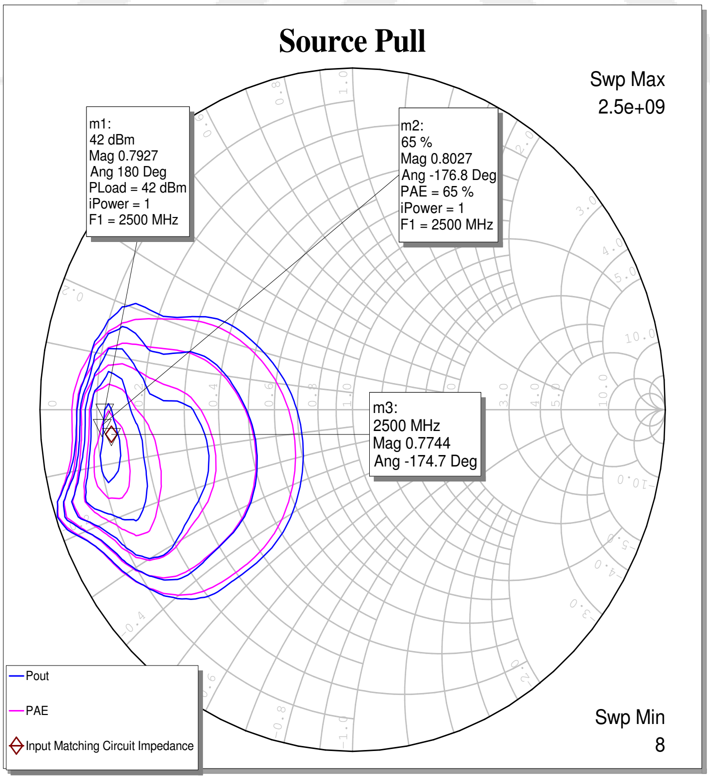
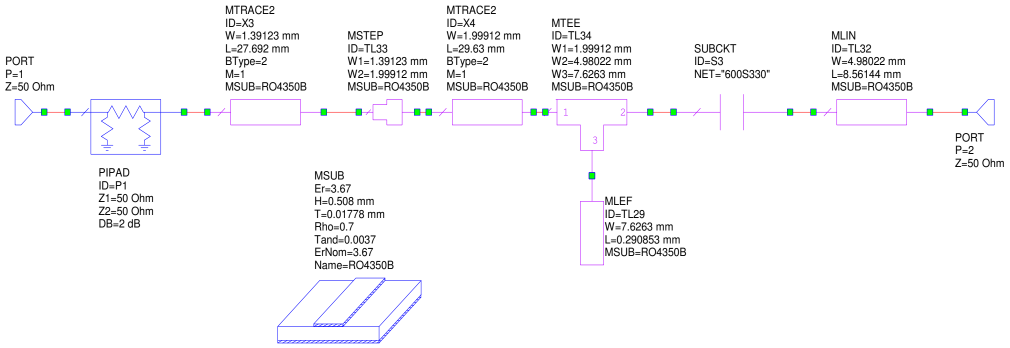


(b)

Figure 11: (a) Load- and (b) source-pull contours of CGH40010F at 2.5 GHz



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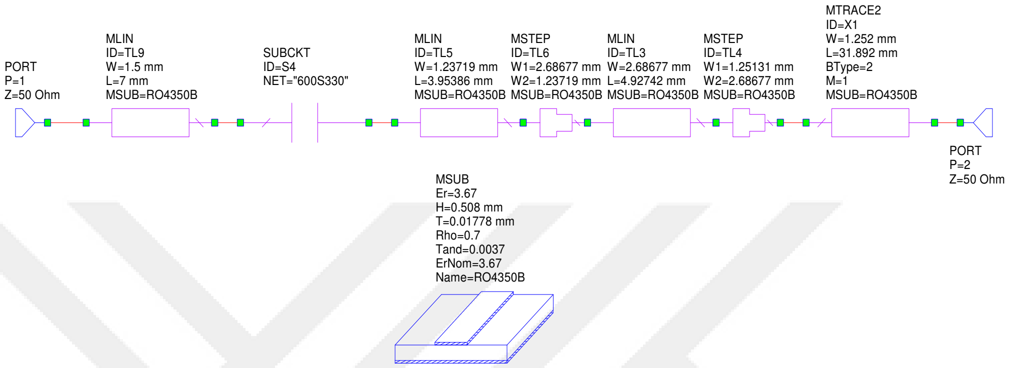


(b)

Figure 12: (a) Input and (b) output matching networks of the first-stage PA

3.6 Final Circuit and Stability Analysis

The amplifier design is completed and ready for fabrication with addition of DC blocks and RF chokes. Stability analysis conducted with the final design to ensure the design is stable. The analysis is conducted from 0.1 to 6 GHz and the proposed power amplifier is observed to be unconditionally stable. Figure 13 shows the B1 and K stability plots.

75 Ω stabilization resistor is used in the gate bias line to meet Rollet's stability condition [9]. Its impact on input impedance, P_{out} and PAE is analyzed and seen to be minimal up to 1.8 GHz. Beyond this frequency, it begins to have an impact on input impedance and beyond 2.4 GHz, gain and efficiency degrade; however, unconditional stability is a must for this work and therefore performance is compromised slightly to achieve this target. The final circuit is presented in Figure 14.

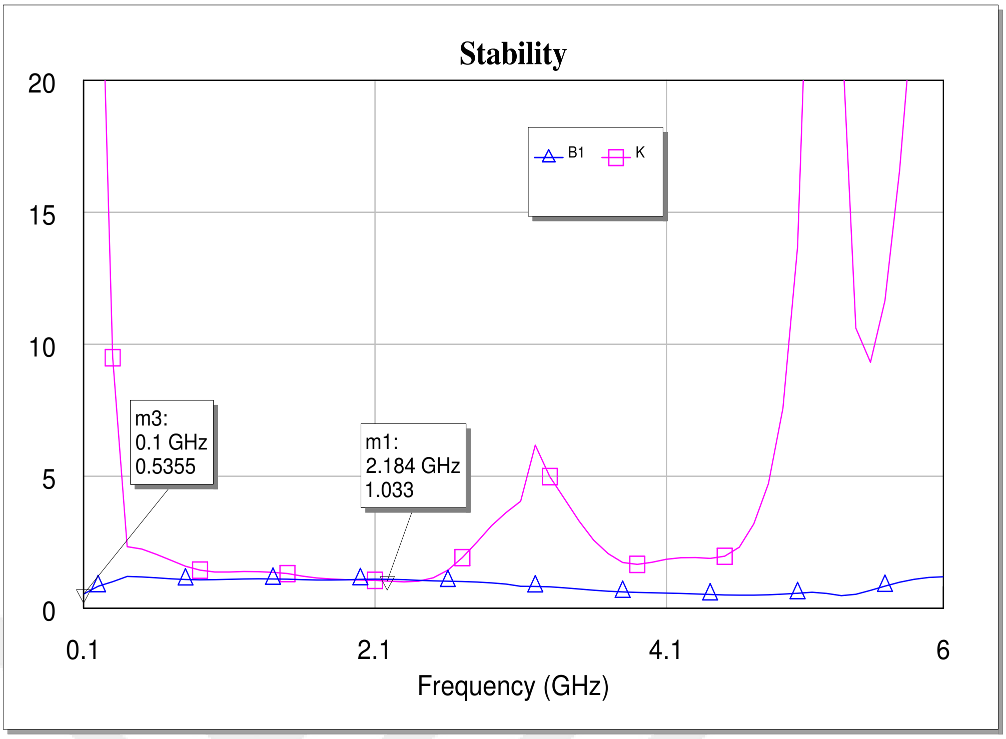


Figure 13: B1 and K stability for first-stage PA

3.7 Simulation Results of First-Stage Power Amplifier

Simulated small-signal results are presented in Figure 15. S_{11} varies between -4.5 - -6.5 dB, while S_{21} fluctuates between 16.5 - 19.8 dB. Figure 15 shows S_{22} whose maximum value is seen to be -9.6 dB at 2.1 GHz.

Simulated large-signal gain, large-signal input return loss, P_{out} and PAE graphs are given in Figure 15. Simulations are conducted at 26 dBm input power level with swept frequency. Output power and PAE are greater than 40.2 dBm and 54.1%, respectively, throughout the band.

Power and efficiency versus input power plots for different frequencies are presented in Figure 16, Figure 17 and Figure 18.

3.8 Measurements of First-Stage Power Amplifier

In this section, measurement results of the first-stage power amplifier are described in detail. Test setup used in large-signal measurements is also presented. Figure 19

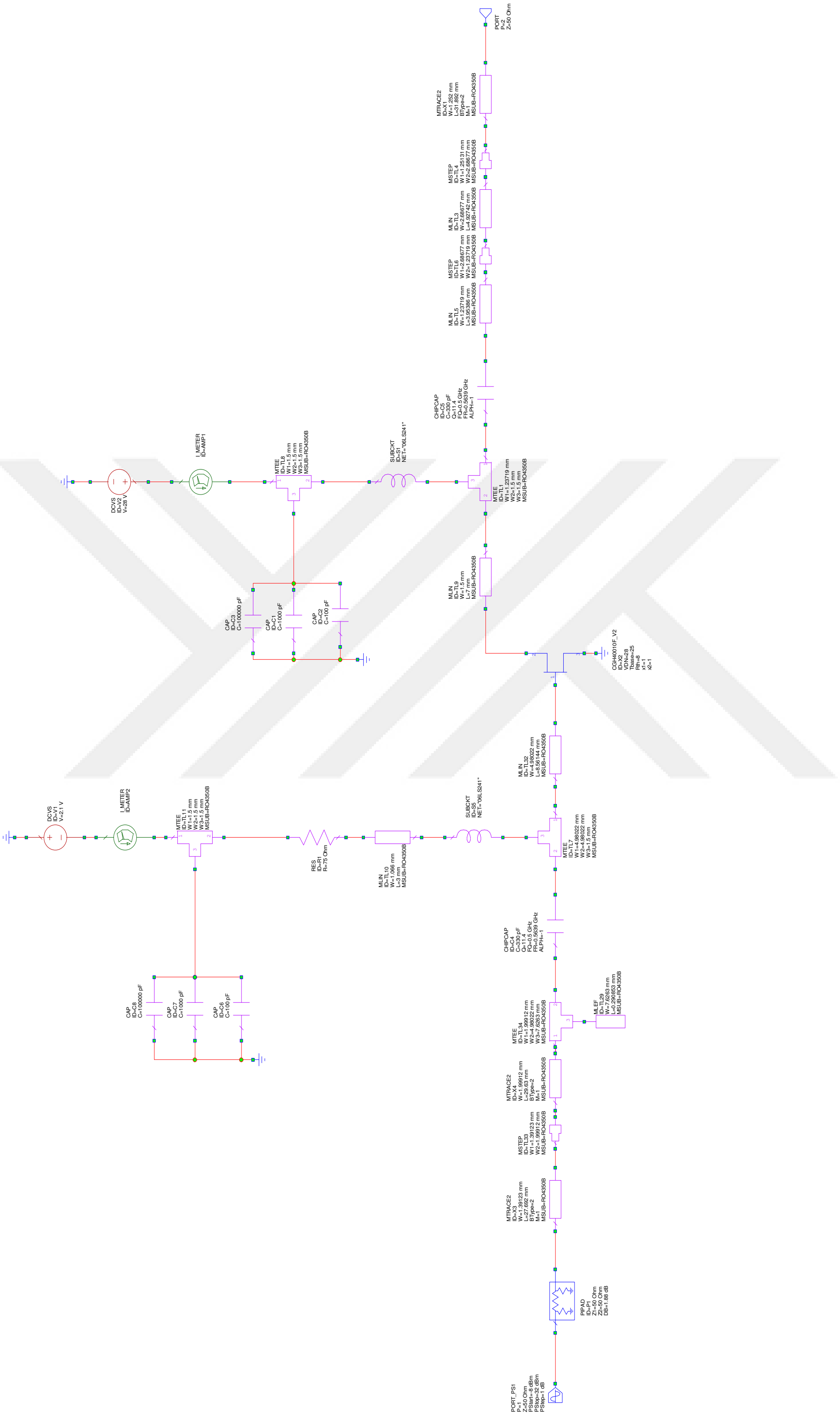
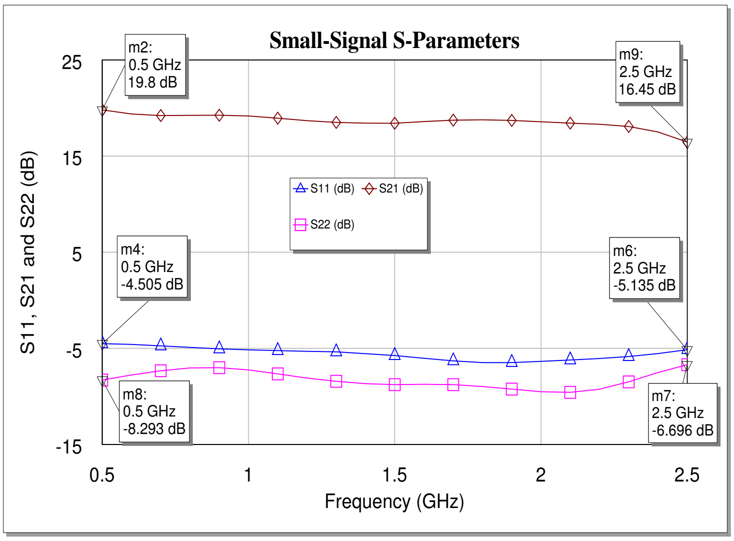
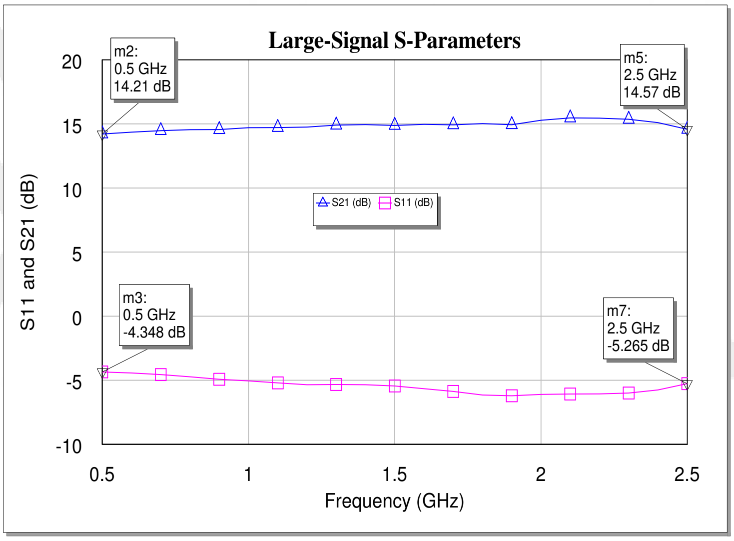


Figure 14: Final first-stage PA circuit



(a)



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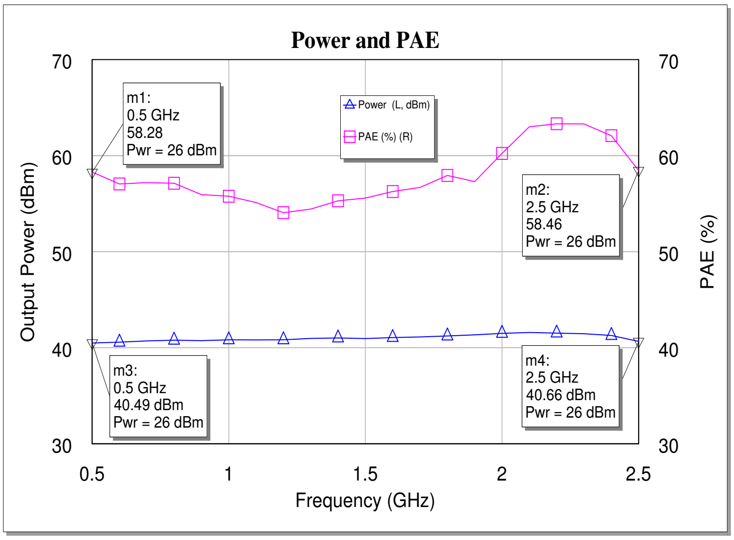
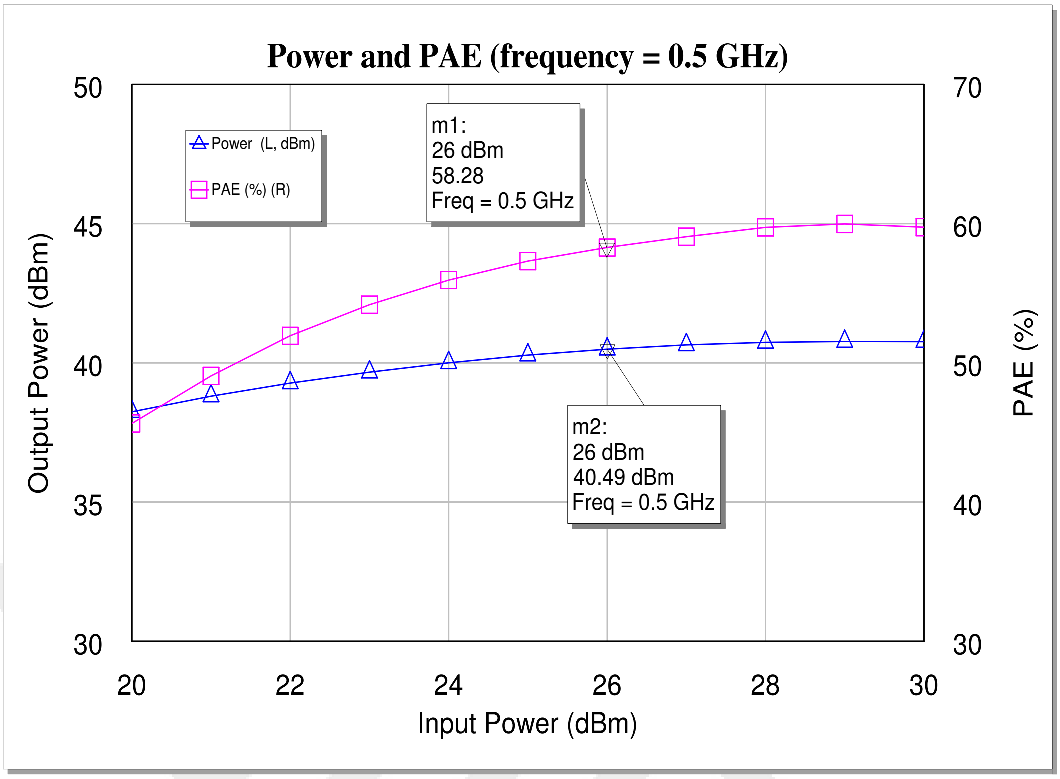


(c)

Figure 15: Simulated (a) small- and (b) large-signal S-parameters, (c) P_{out} and PAE of the first-stage PA



(a)

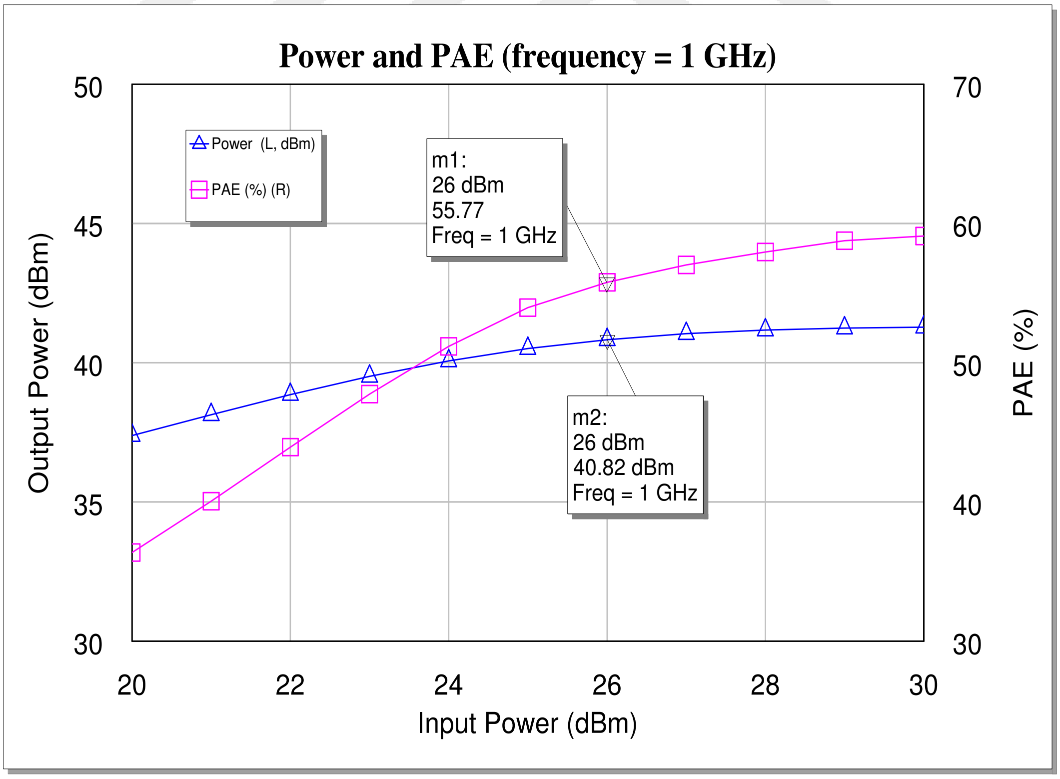


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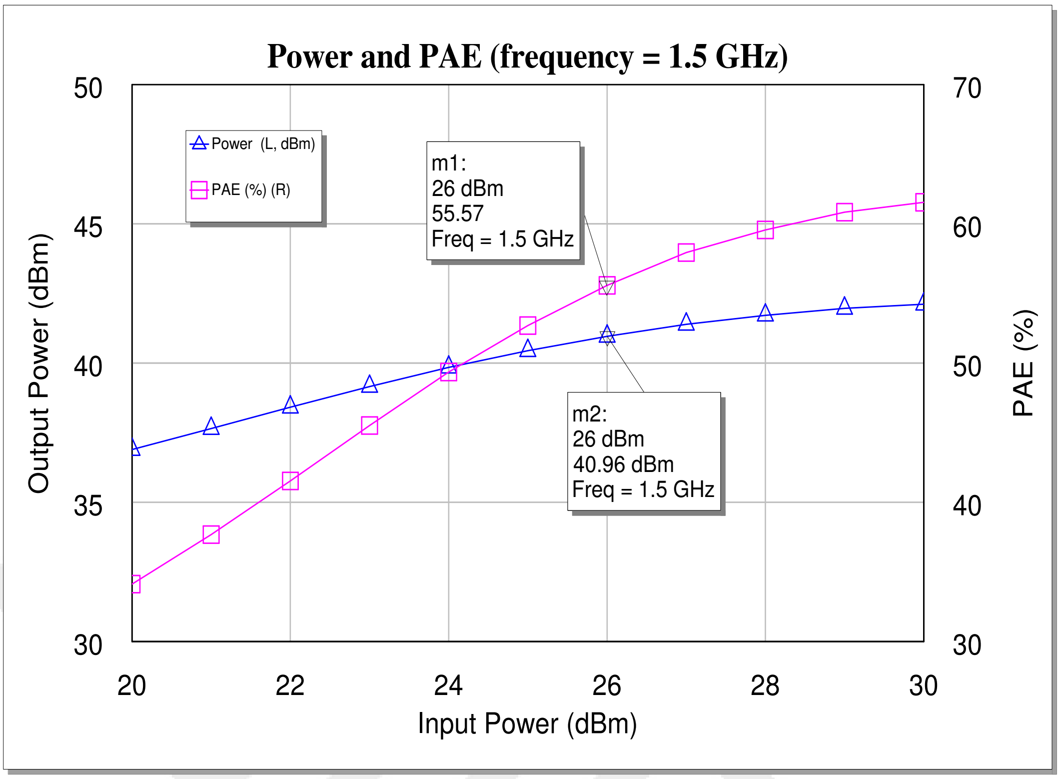
Figure 16: Simulated P_{out} and PAE vs P_{in} for the first-stage PA at (a) 0.5 GHz and (b) 1 GHz



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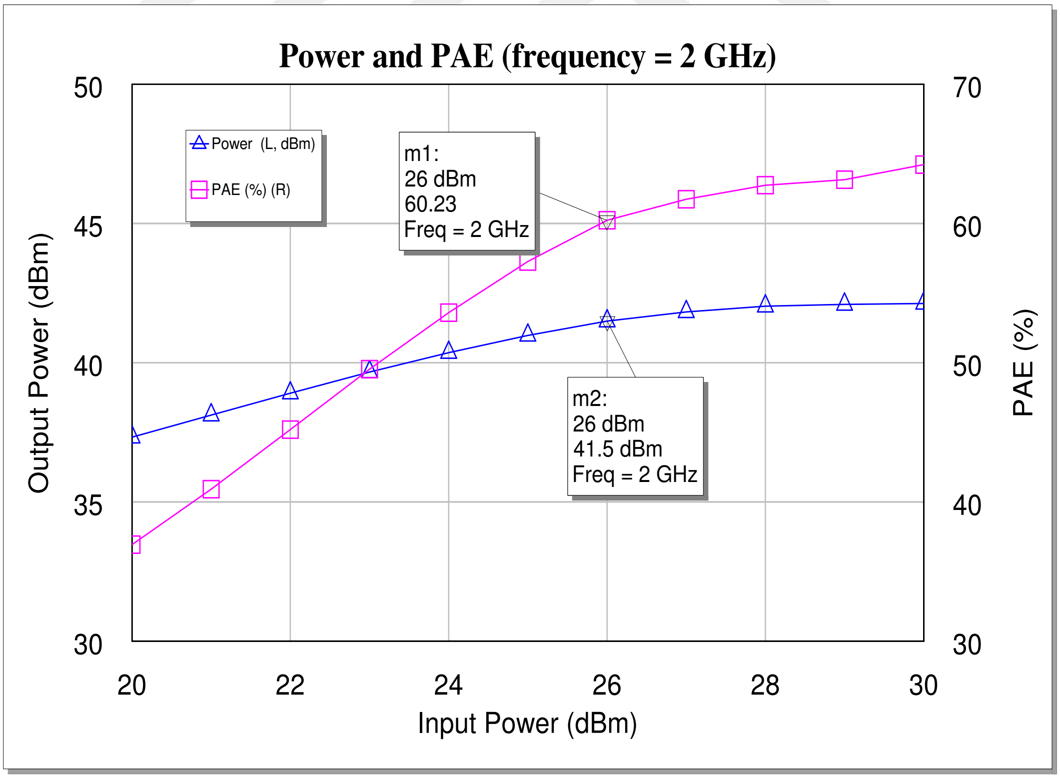

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Figure 17: Simulated P_{out} and PAE vs P_{in} for the first-stage PA at (a) 1.5 GHz and (b) 2 GHz

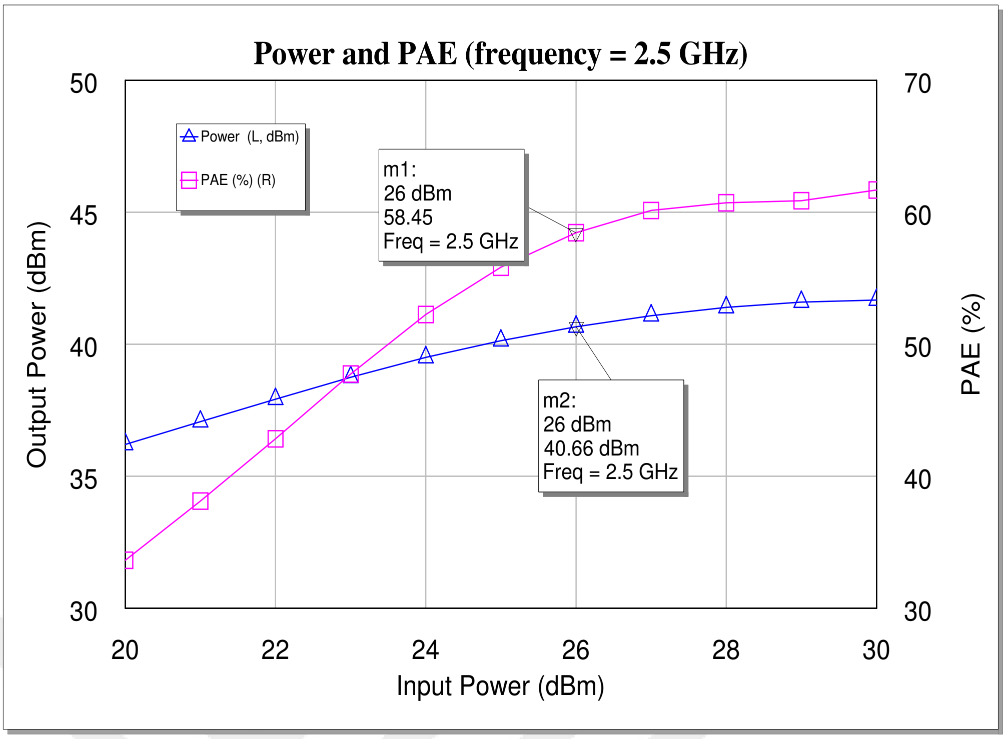
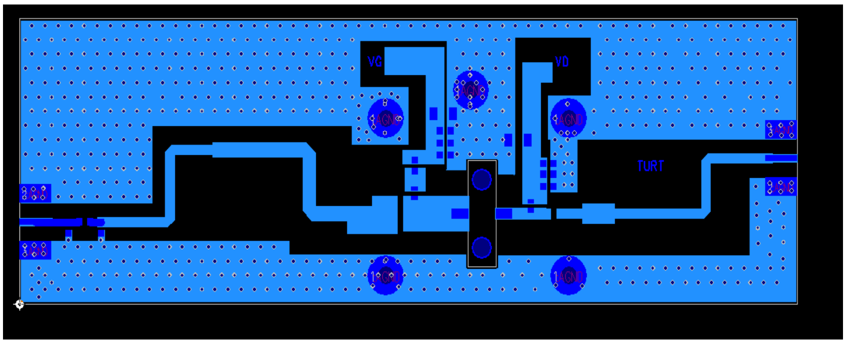


Figure 18: Simulated P_{out} and PAE vs P_{in} for first-stage PA at 2.5 GHz

displays layout of the first-stage PA and the realized circuit. The design is fabricated on 0.508 mm thick Rogers RO4350B substrate with $\epsilon_r = 3.66$. Final PCB dimensions are 120 mm x 40 mm. Mentor Pads software [15] is used for layout of the printed circuit board.

Small-signal analyses and measurements are carried out first. Simulated and measured small-signal S_{11}, S_{21} are provided in Figure 20. Simulated S_{11} varies between -4.5 - -6.5 dB, while measurements show better than -4.8 dB input reflection throughout the band which is in good agreement with simulations. On the other hand, small-signal gain, S_{21}, exhibits slight divergence between simulations and measurements. While the measured gain is higher at the low end of the band (0.5 - 1.2 GHz), it is lower than simulations in the upper half by as much as 2 dB.

Block diagram and photo of the large-signal measurement setup are illustrated in Figure 21. Agilent E8257D [16] signal generator is used to provide continuous-wave (CW) excitation. However, because it cannot provide 26 dBm output power,



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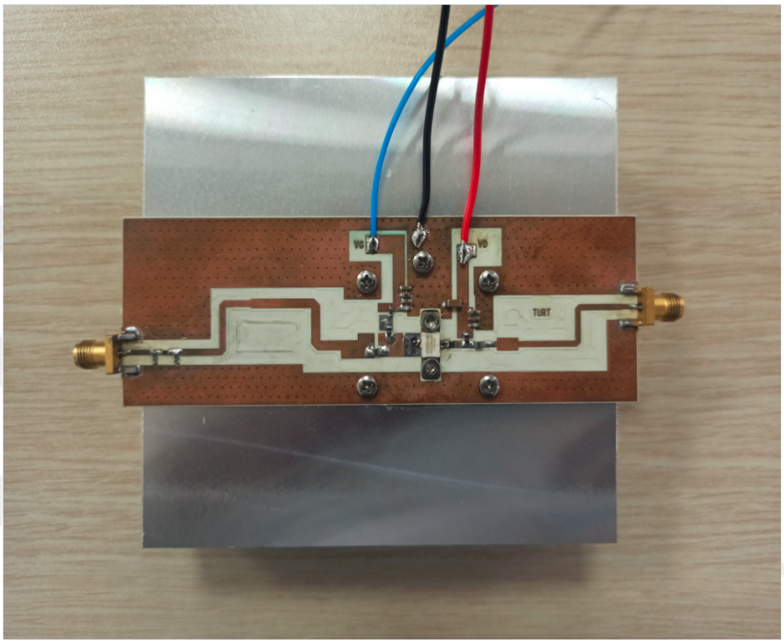


(b)

Figure 19: (a) Layout and (b) photo of the realized first-stage PA

a COTS power amplifier JA0530P52 [17] is used to amplify signal generator output for large-signal measurements. For the first-stage power amplifier, bias conditions are determined as V_{DS} = 28 V, V_{GS} = -2.1 V, I_{DQ} = 336 mA for class AB operation. JA0530P52 is supplied with 20 V by using Keysight E3631A [18] DC power supply. Keysight E3631A and Keysight 6032A [19] DC power supplies are used to supply gate and drain voltages of the first-stage power amplifier, respectively. Large-signal power measurements are conducted by using Keysight E4417A [20] power meter. Since the maximum input power level is 20 dBm for E4417A, a 40 dB attenuator is used. The attenuator is characterized over the frequency range of interest and its loss is

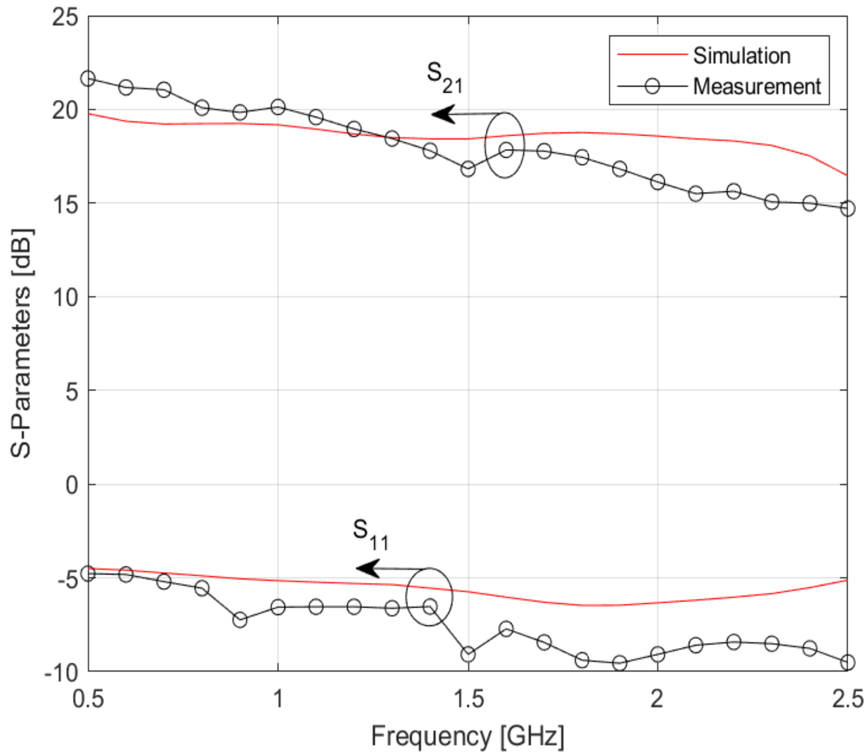
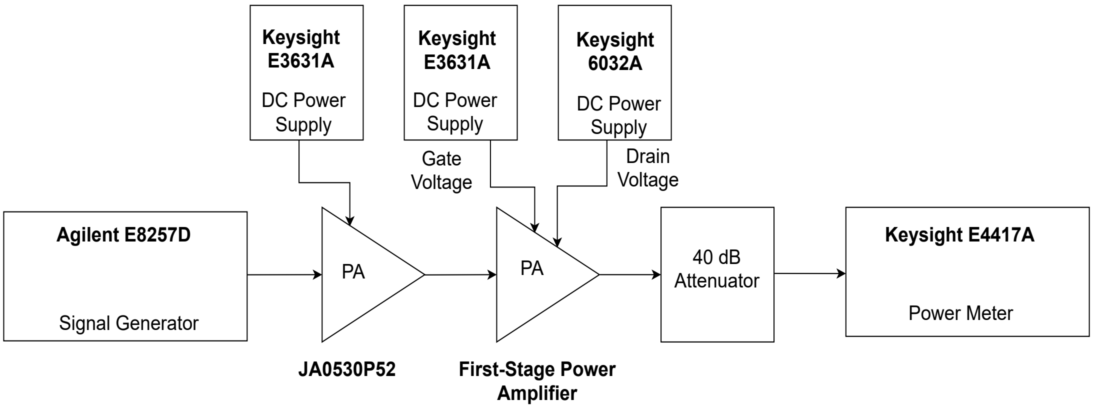


Figure 20: Measured and simulated small-signal S-parameters of the first-stage PA

de-embedded in results presented herein.

Output power, gain and PAE are analyzed for the fabricated and simulated systems under CW stimulation with swept frequency from 0.5 to 2.5 GHz. Signal generator and COTS amplifier are configured to provide a constant 26 dBm input drive to the first-stage PA. Figure 22 presents the measured output power, gain and PAE versus simulation over the band. The measured output power is between 39.6 - 40.9 dBm and measured PAE is between 45.9 % - 61.4 % over the band.

The simulated output power is between 40.2 - 41.5 dBm and simulated PAE is between 54.1 % - 63.3 % over the band. For output power, PAE and gain, measured results are better than simulations at most points between 0.5 - 1.3 GHz; however, beyond this point, there is a drop in measured results compared to simulated results. Large-signal gain of the fabricated system varies between 13.6 - 14.9 dB, while it is between 14.2 - 15.5 dB in simulations.



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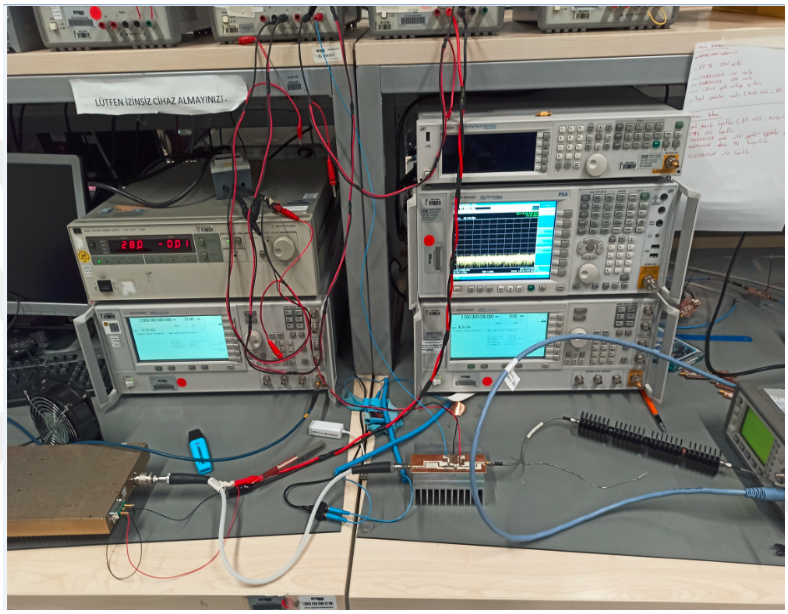
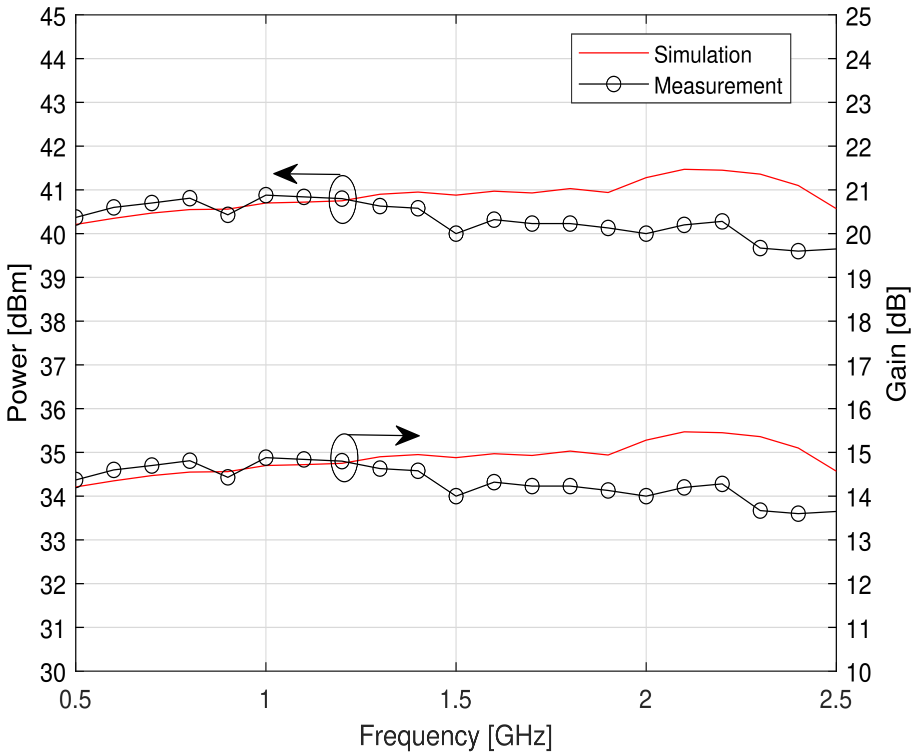


(b)

Figure 21: (a) Block diagram and (b) photo of the large-signal measurement setup

During design of the first-stage PA, a trade-off between gain and input match is noticed. In order to achieve broadband performance, gain is prioritized over input match. As a result, both simulations and measurements show relatively poor input match.

Simulations are conducted for an input power level of 26 dBm with 50 Ω terminated source. During measurements, on the other hand, it is difficult to present a perfect 50 Ω source impedance to the PA. In order to alleviate the impact this may have on measurements, a 3 dB attenuator is used at the input of the first-stage PA. Figure 22 presents the measured output power and PAE versus simulated results



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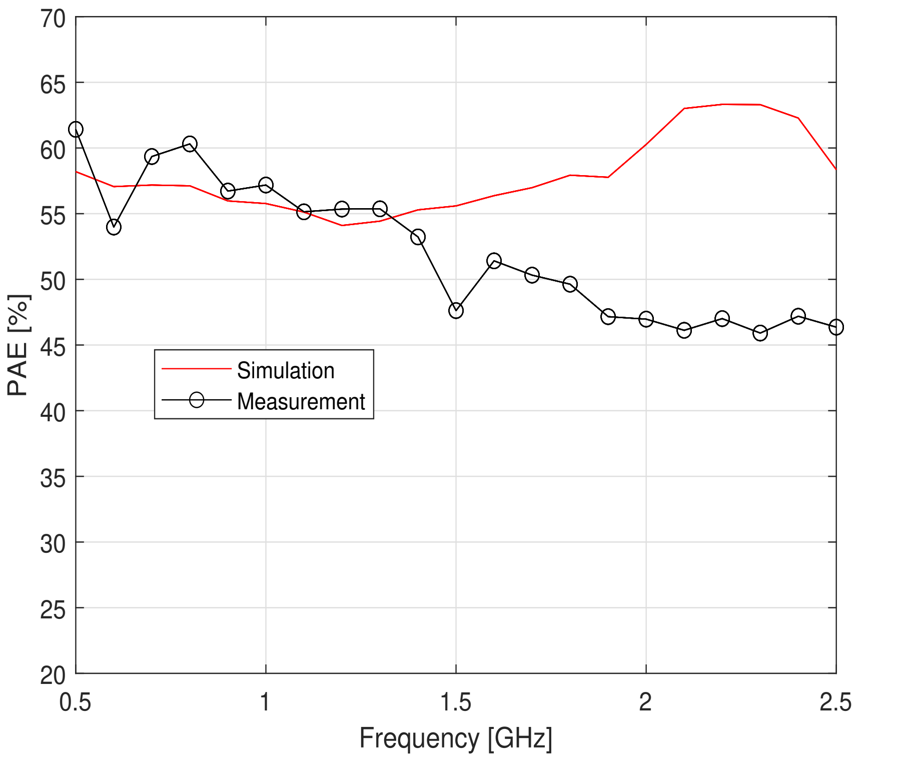
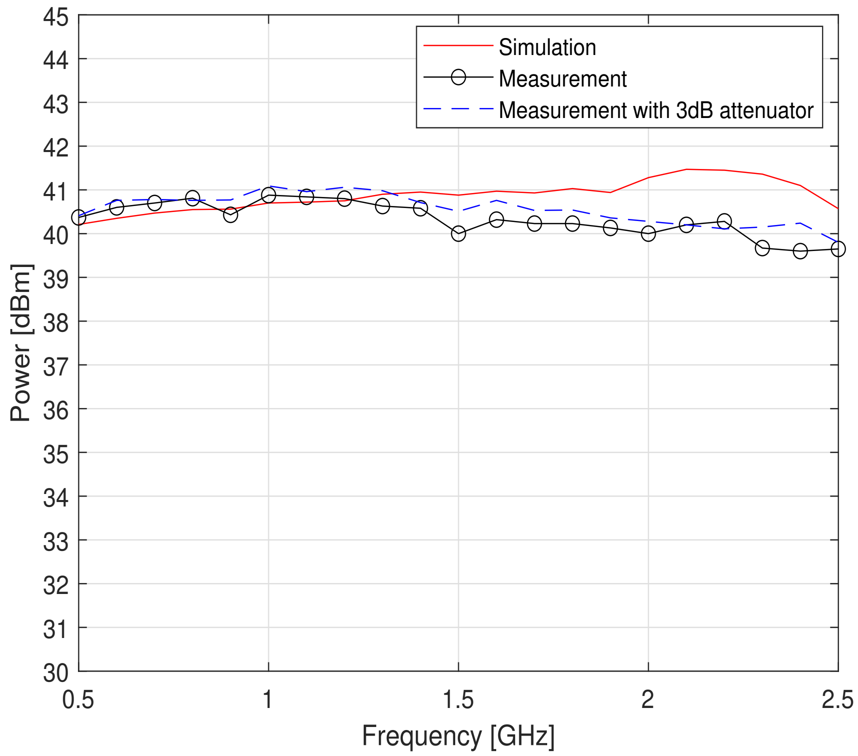


(b)

Figure 22: Measured and simulated (a) output power, large-signal gain and (b) PAE of the first-stage PA



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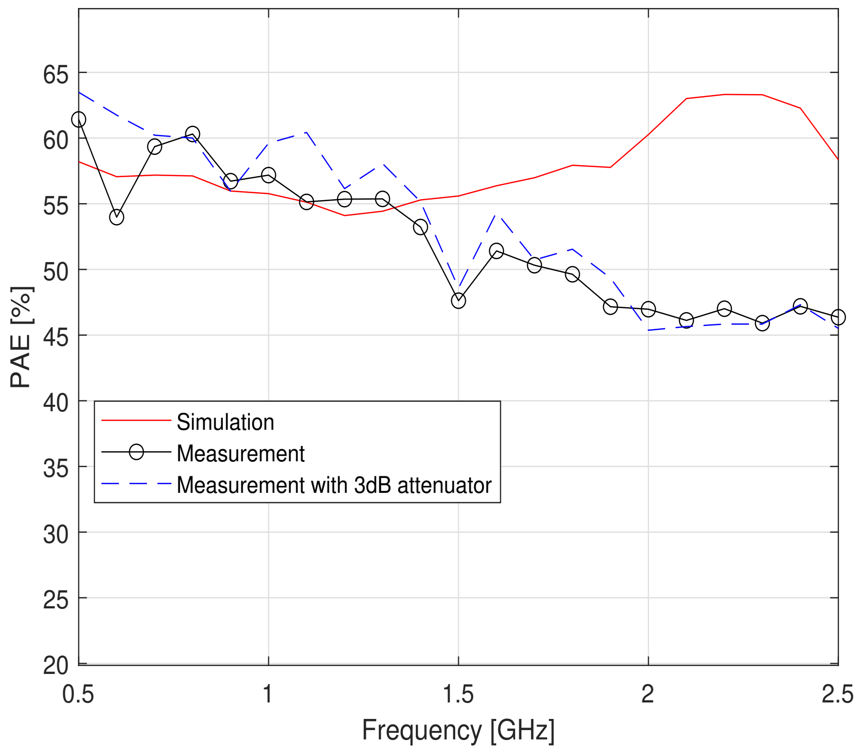


(b)

Figure 23: Measured, measured with 3 dB and simulated (a) output power and (b) PAE of the first-stage PA

versus frequency. Figure 23 compares output power and PAE with and without the 3 dB attenuator along with simulated results. It is observed that use of the 3 dB attenuator improves the output power ever so slightly at the lower half of the band while having no discernible impact on higher frequency performance. Therefore, it is concluded that divergence of PAE and P_{out} in measurements versus simulations in the upper half of the band is not due to source impedance mismatch.

While simulations employ manufacturer's transistor model, microstrip line models and S-parameters of lumped components where available, two components could not be modelled accurately. First, discontinuity due to subminiature-A (SMA) RF connectors could not be taken into account due to lack of S-parameters. Secondly, manufacturer's S-parameters of the RF choke is given up to 0.5 GHz. Beyond this frequency, RF choke model is based on extrapolated curves. Combined with fabrication imperfections,these factors are thought to be main culprits of the difference between simulated and measured results in the high end of the band.

CHAPTER IV

DESIGN & MEASUREMENTS OF SECOND-STAGE BROADBAND CLASS-AB HIGH POWER AMPLIFIER

In this chapter, design and measurements of second-stage of broadband class AB high power amplifier using Wolfspeed's CG2H40120F GaN HEMT device are presented. The primary goals are to achieve higher than 50 % PAE and 48 dBm output power from 0.5 to 2.5 GHz. Table 3 summarizes these goals.

Second-stage PA design approach mirrors that of the first-stage presented in the previous chapter. Consequently, followings sections only highlight differences briefly.

Table 3: Design goals of second-stage of broadband Class-AB high power amplifier

Output Frequency Range	0.5 - 2.5 GHz
Output Power	>48 dBm
PAE	>50 %

4.1 Transistor Choice & DC Operating Point

Similar to the first-stage PA, a Wolfspeed transistor is selected, CG2H40120F, for the second stage due its broadband performance and large-signal model availability.

To meet specifications on output power, PAE, gain and harmonic suppression, suitable DC bias point needs to be determined by drawing I-V curves. Figure 24 represents the circuit which is used to draw I-V curves.

Maximum drain current of CG2H40120F is 11 Amperes. This corresponds to $V_{GS} = -1.8$ V for Class-A operation as seen in Figure 25a. Class-B operation with

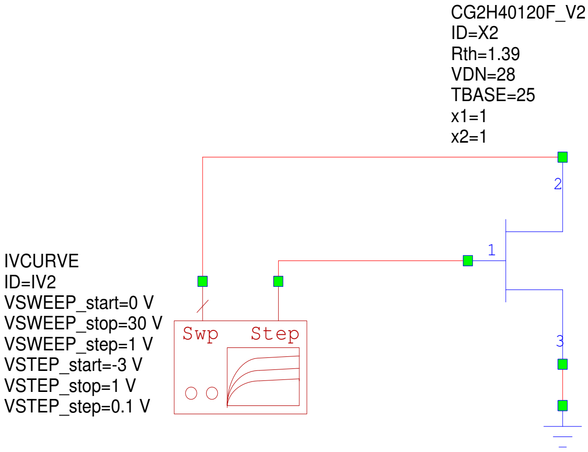


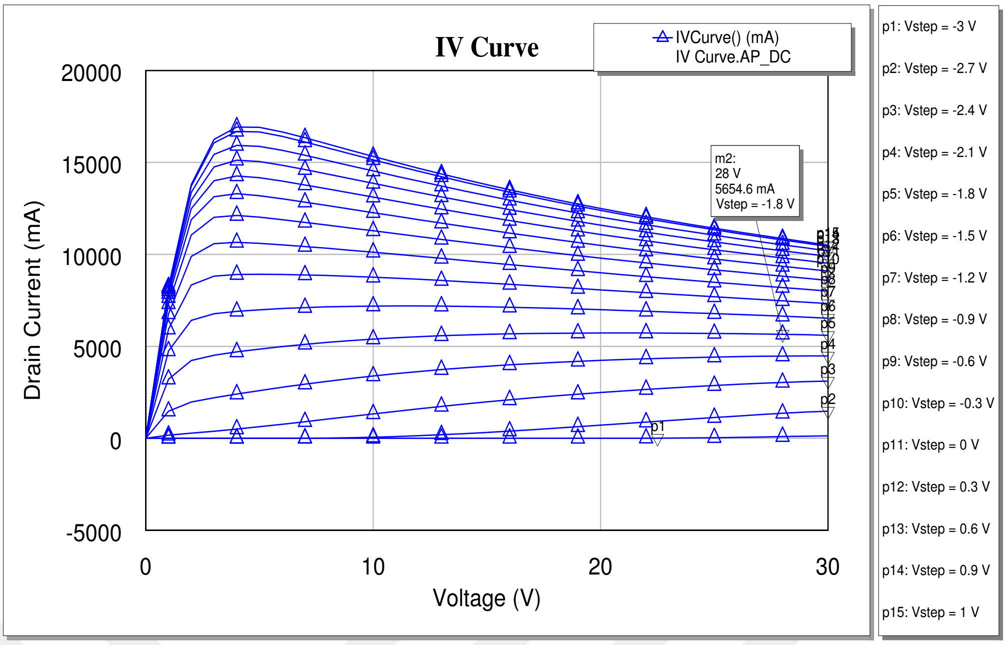
Figure 24: Schematic of circuit used in Cadence AWR Microwave Office for I-V curve analysis of CG2H40120F

zero quiescent current is achieved at $V_{GS} = -3$ V as shown in Figure 25b. By adjusting gate voltage between these two values, the transistor is operated in Class-AB. In this work, DC operating point is selected as V_{DS} = 28 V, V_{GS} = -2.2 V, I_{DQ} = 4 A for Class-AB operation.

ATC 700A101JW capacitor is used as DC block at both input and output of the transistor. Unlike the first-stage design, a quarter-wave transmission line is used as an RF choke to eliminate parasitic effects of surface-mount inductors. Simulations are used to determine the frequency at which the transmission line is quarter wavelength long to ensure broadband performance which showed 2 GHz achieved the best performance.

4.2 Load- & Source-pull Analyses

Load- & source-pull analyses are already discussed in detail in previous chapters. Same processes are repeated for CG2H40120F herein. Figures 27-31 present load- & source-pull contours of the device along with the impedance points of the final input and output matching networks at 0.5, 1, 1.5, 2 and 2.5 GHz. For these analyses, input power to CG2H40120F is 39 dBm and DC bias voltages are -2.2V/28V.



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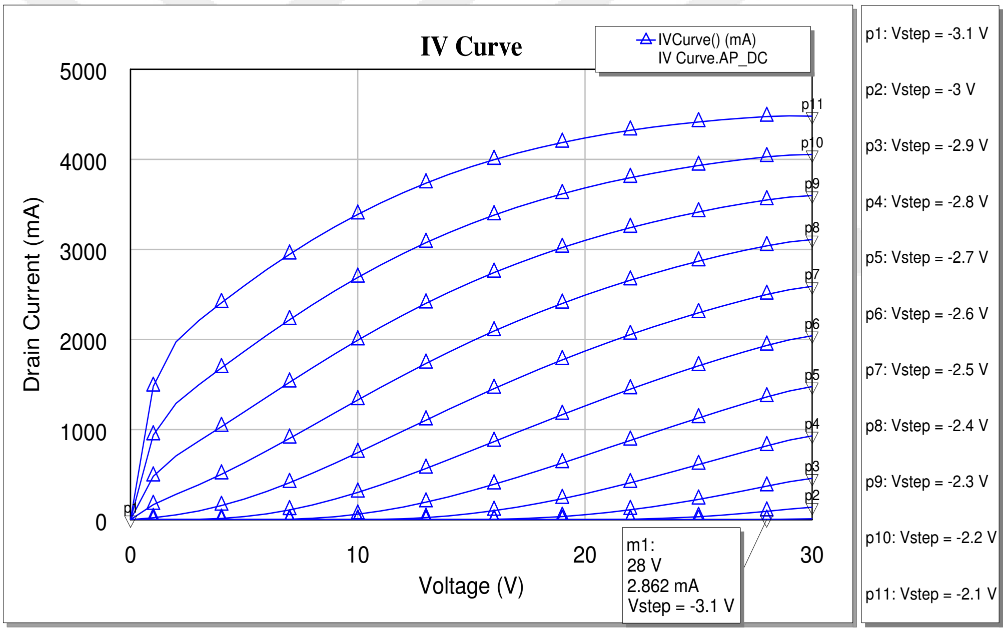


(b)

Figure 25: (a) I-V curves of CG2H40120F, (b) close up of class-AB operation region

4.3 Input and Output Matching Network Design

The same design procedure is followed as the first-stage to design input and output matching networks for the second-stage power amplifier. Network synthesis tool of Cadence AWR Design Environment is used to provide a starting point for the iterations, followed by manual optimization. Figure 32 displays the final input and output

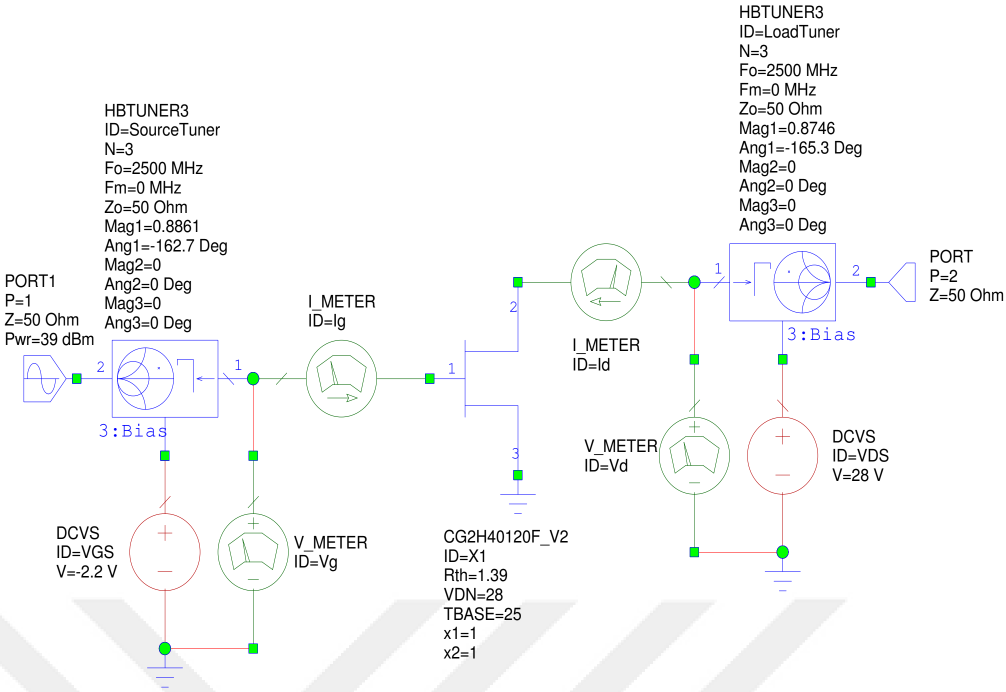


Figure 26: Load- & source-pull circuit for CG2H40120F

matching networks for the second-stage power amplifier.

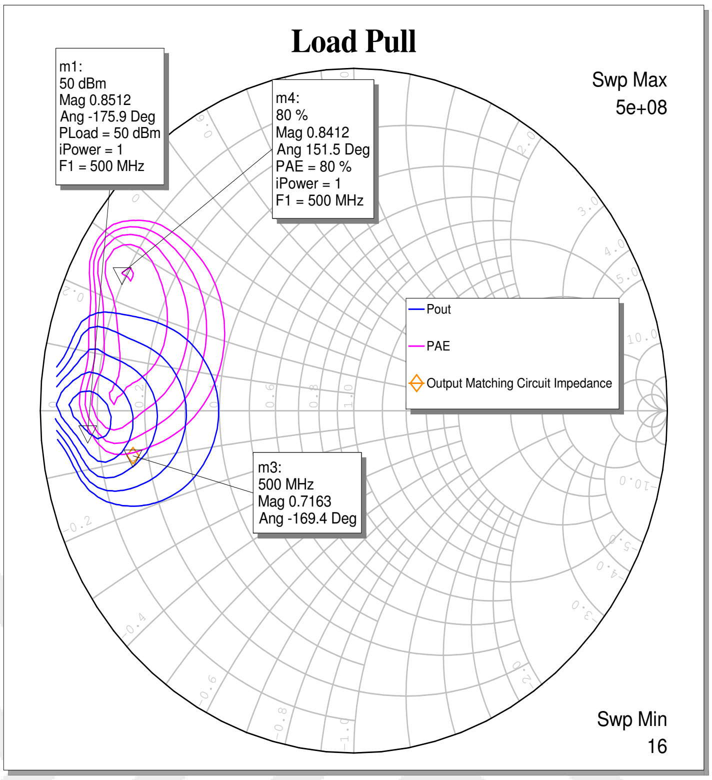
4.4 Final Circuit and Stability Analysis

In this section, DC blocks and biasing circuits are added to design thereby obtaining the final circuit. Stability analysis is conducted between 0.1 - 6 GHz and it is observed that the proposed power amplifier is unconditionally stable. Figure 33 shows the B1 and K stability plots.

In order to ensure unconditional stability,

- an RC stabilization circuit, consisting of 8.2 pF capacitor and 20 Ω resistor, is employed at the input RF line,
- A 5.6 Ω resistor is added to the gate bias line.

Both stability circuits are designed to quench potential oscillations, especially at low frequencies. Final schematic of the second-stage power amplifier is provided in Figure 34.



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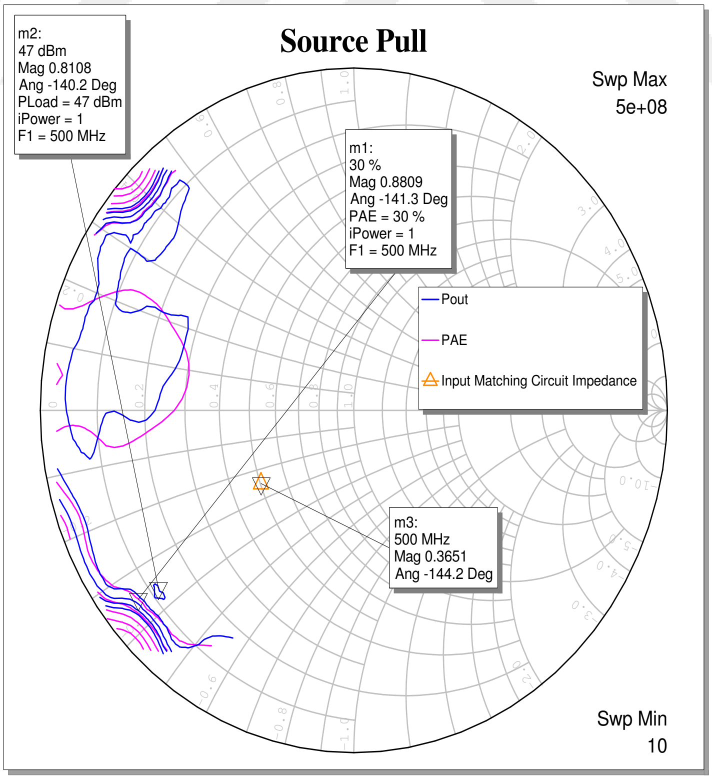
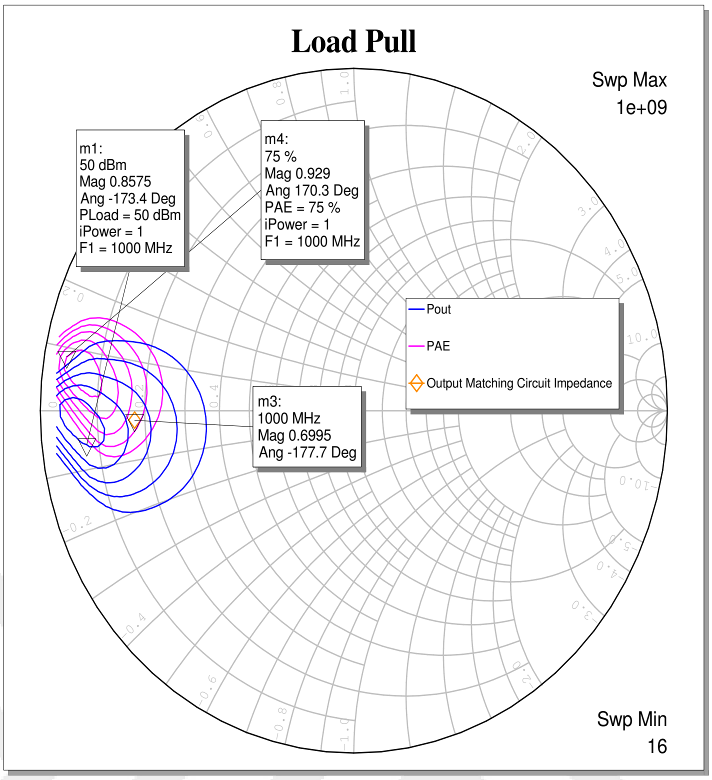
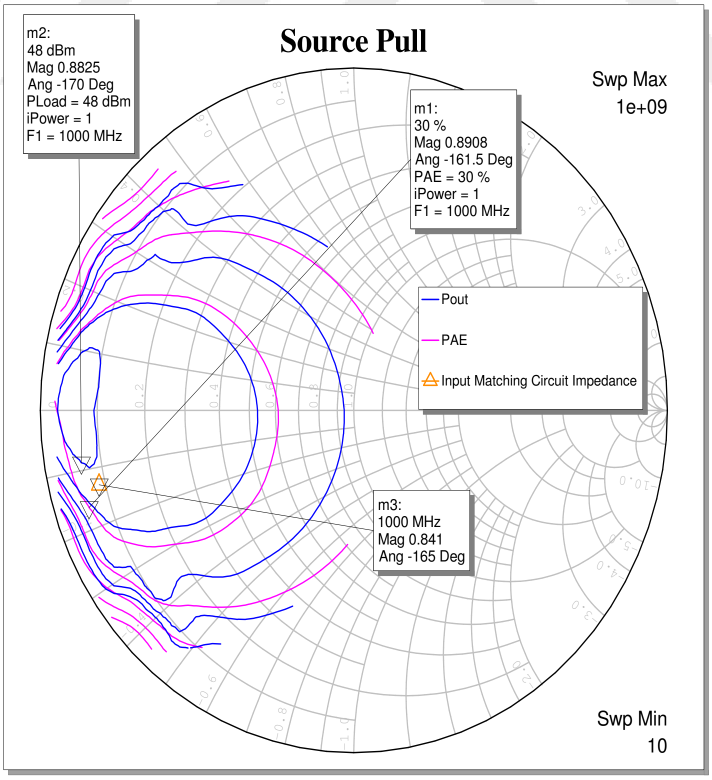


(b)

Figure 27: (a) Load- and (b) source-pull contours of CG2H40120F at 0.5 GHz

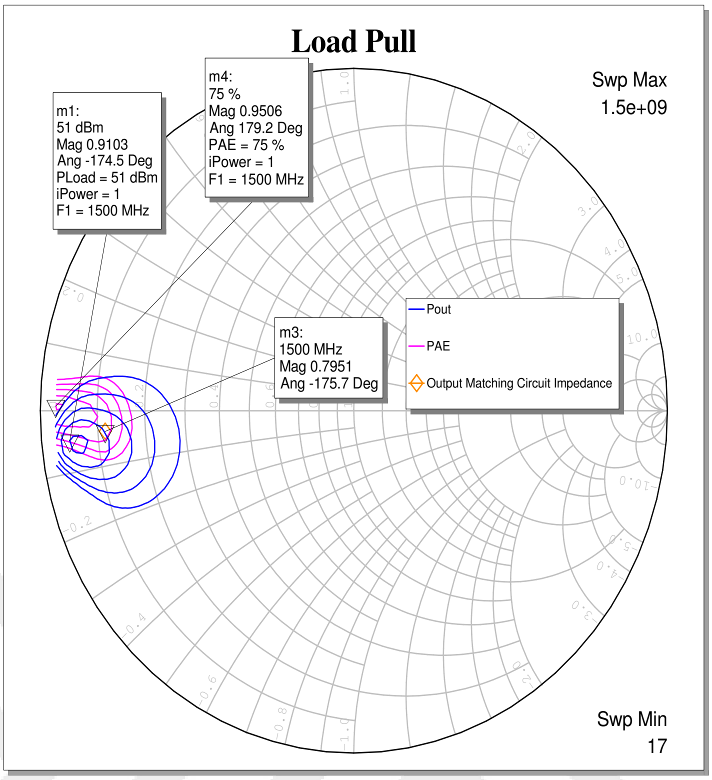


(a)

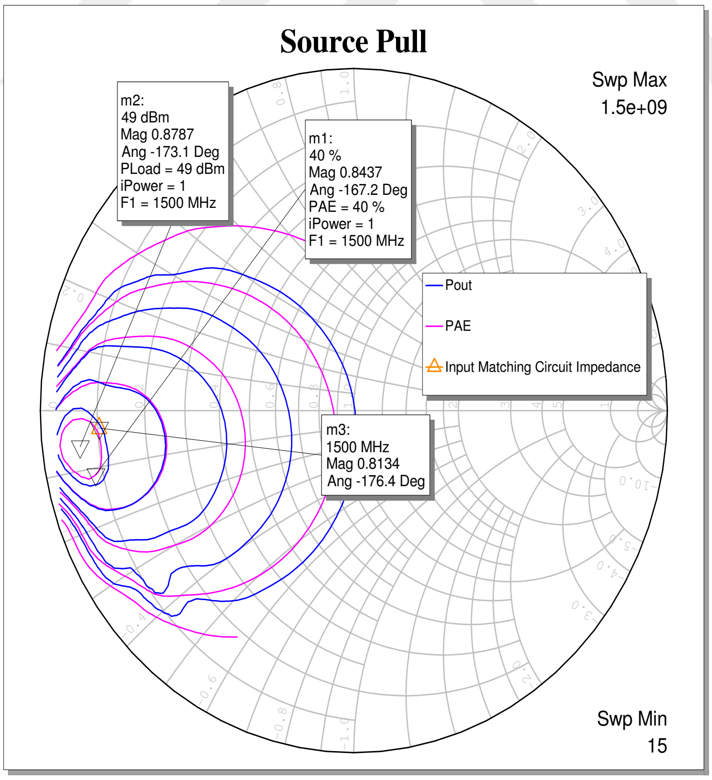


(b)

Figure 28: (a) Load- and (b) source-pull contours of CG2H40120F at 1 GHz

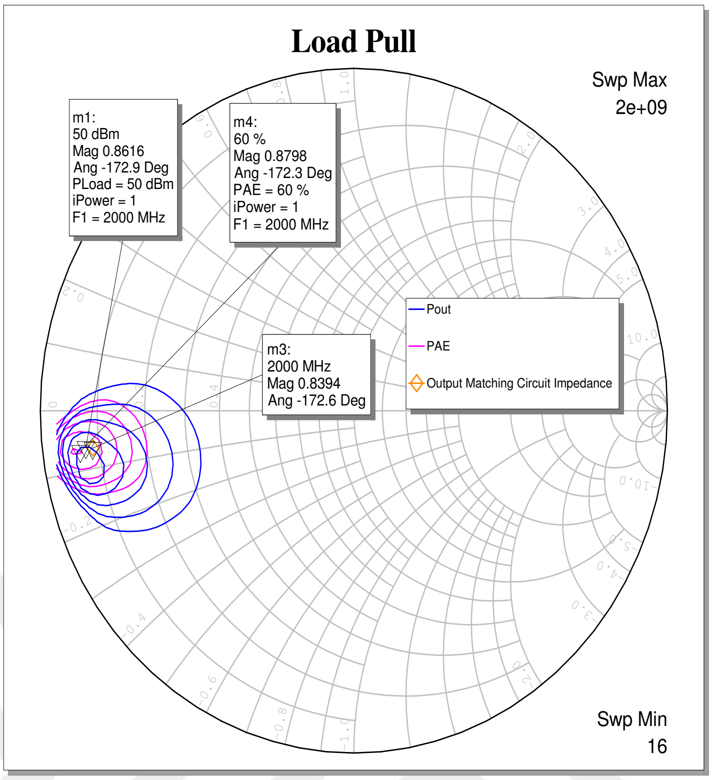


(a)



(b)

Figure 29: (a) Load- and (b) source-pull contours of CG2H40120F at 1.5 GHz



(a)

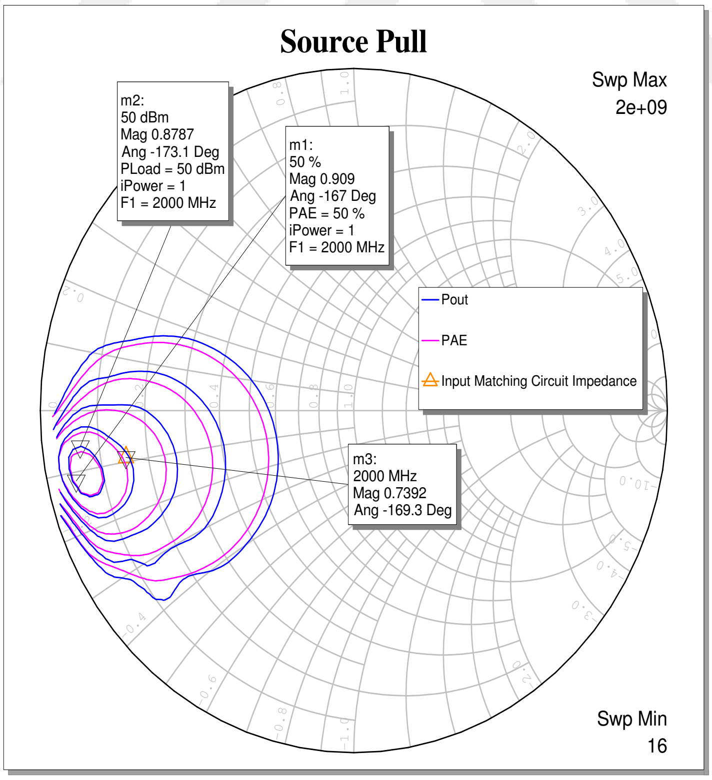


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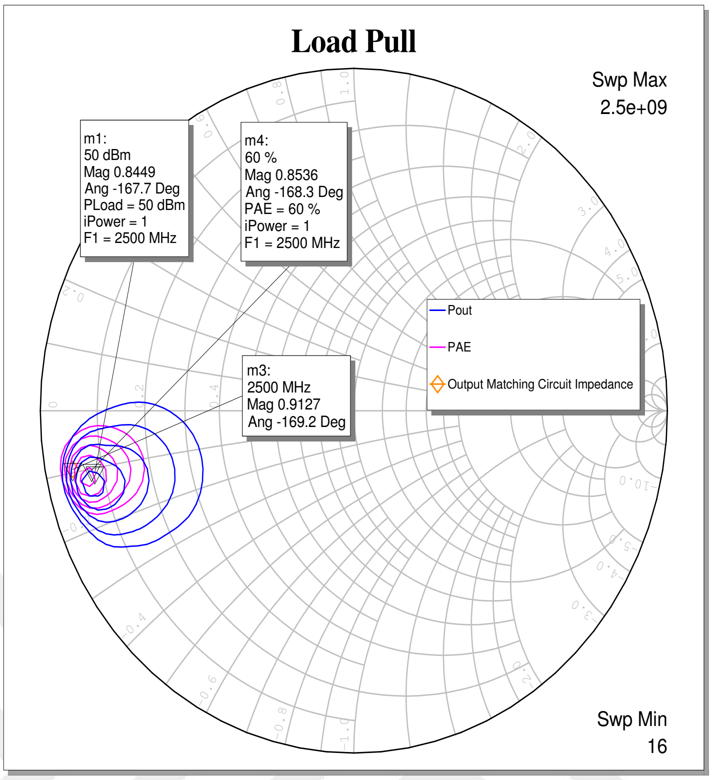
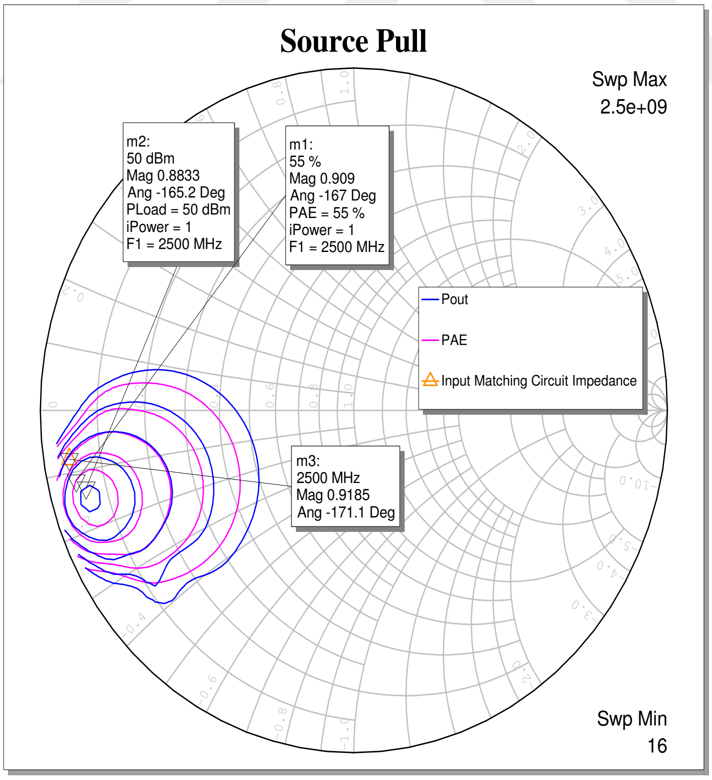
Figure 30: (a) Load- and (b) source-pull contours of CG2H40120F at 2 GHz

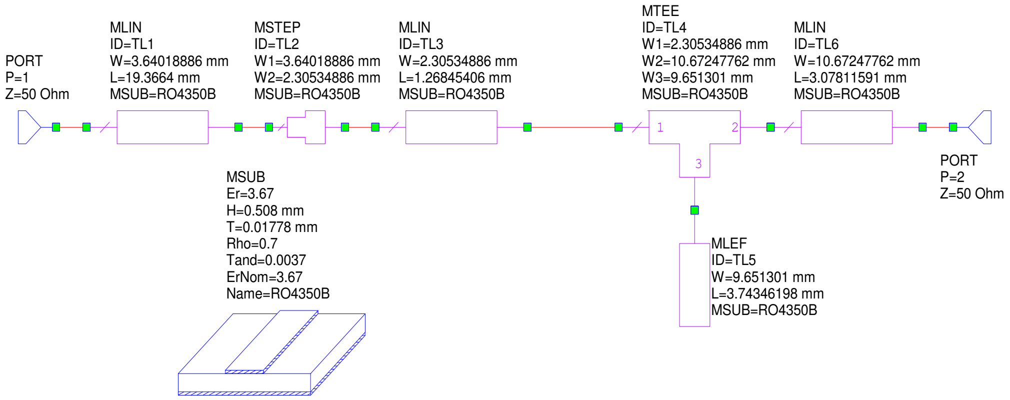


(a)

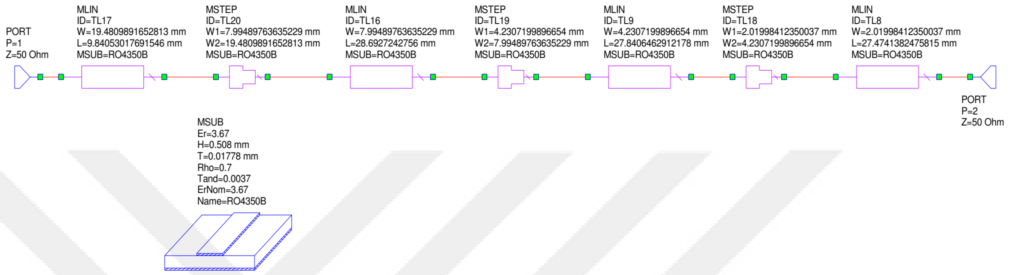


(b)

Figure 31: (a) Load- and (b) source-pull contours of CG2H40120F at 2.5 GHz



(a)



(b)

Figure 32: (a) Input and (b) output matching networks of the second-stage PA

4.5 Simulation Results of Second-Stage Power Amplifier

Simulated small-signal results for second-stage power amplifier are displayed in Figure 35. S_{11} varies between -3.2 - -6.6 dB, while S_{21} is between 10.3 - 18.3 dB. Figure 35 shows S_{22} which is better than 8 dB in the frequency band of interest.

Simulated large-signal gain, large-signal input return loss, output power and PAE graphs are provided in Figure 35. Simulations are conducted with an input power level of 39 dBm with swept frequency. Minimum 48.1 dBm of output power and 53.4% of PAE are obtained in large-signal simulations.

Power and efficiency versus input power are plotted for different frequencies and shown in Figure 36, Figure 37 and Figure 38.

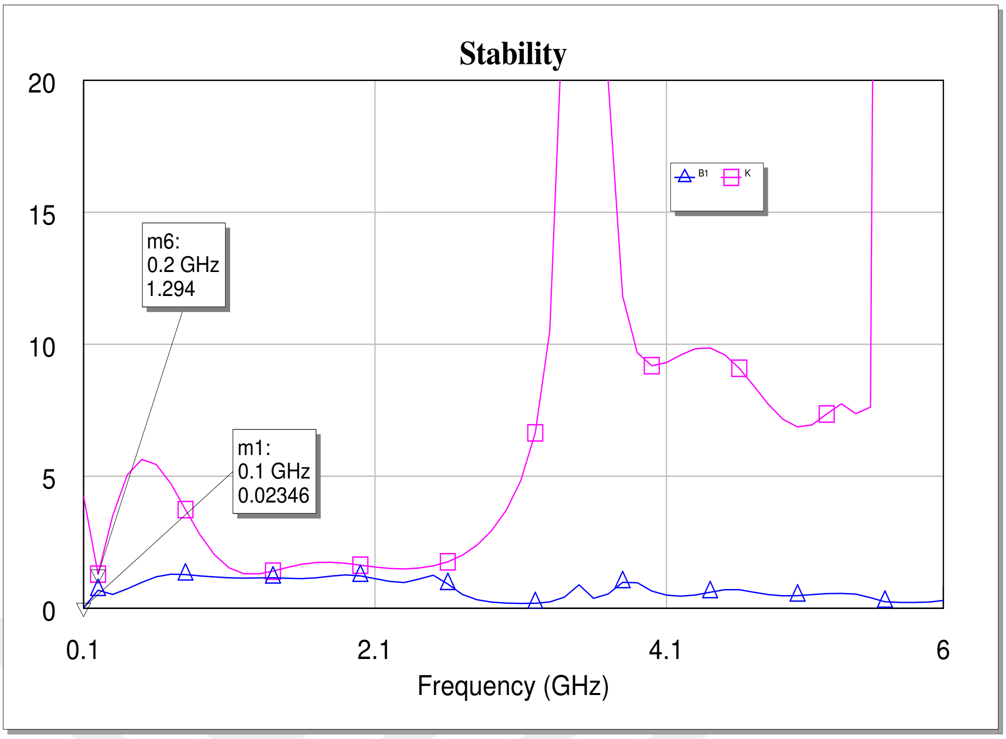


Figure 33: B1 and K Stability for second-stage PA

4.6 Measurements of Second-Stage Broadband Class-AB High Power Amplifier

In this section, measurement results of the second-stage power amplifier are detailed. Test setup used to obtain the measurements, albeit being similar to that of the first-stage, is also described.

Figure 39 presents layout and photo of the fabricated second-stage power amplifier. The design is fabricated on 0.508 mm thick Rogers RO4350B substrate with $\epsilon_r = 3.66$. Final dimensions of the fabricated circuit are 150 mm x 50 mm.

Block diagram and photo of the small-signal test setup are illustrated in Figure 40. Two different Keysight E3631A DC power supplies are used to supply gate and drain voltages for the second-stage power amplifier. Small-signal S-parameters are collected by using Agilent N5222A PNA Microwave Network Analyzer [21].

Simulated and measured small-signal S_{11}, S_{21} are provided in Figure 41. In general, the fabricated amplifier performs better than simulations. Input match is, once

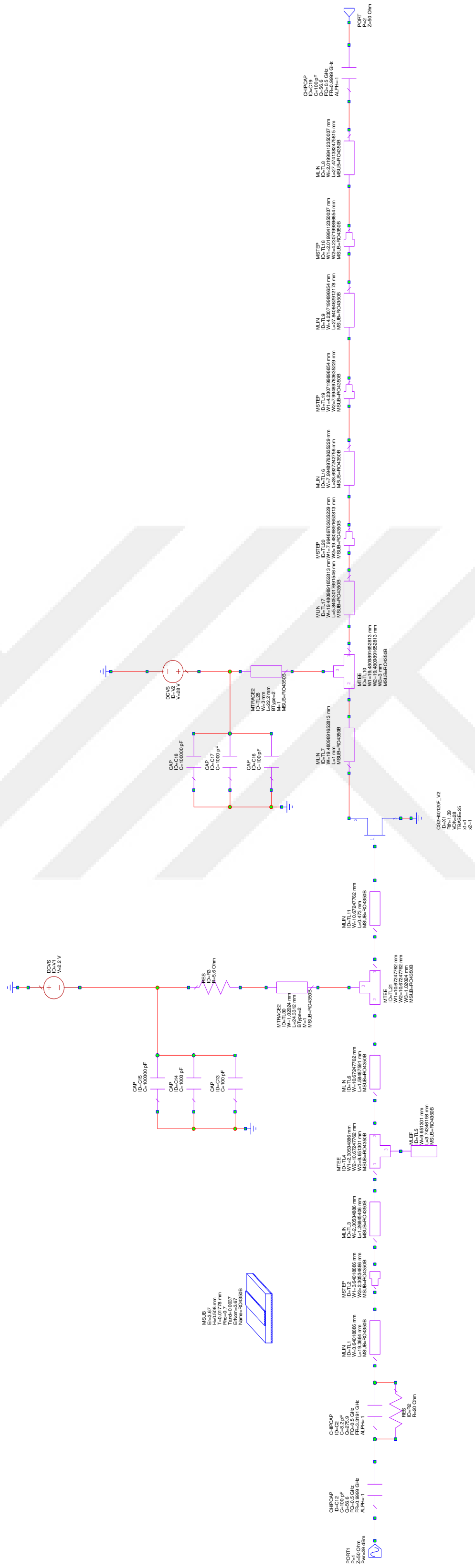
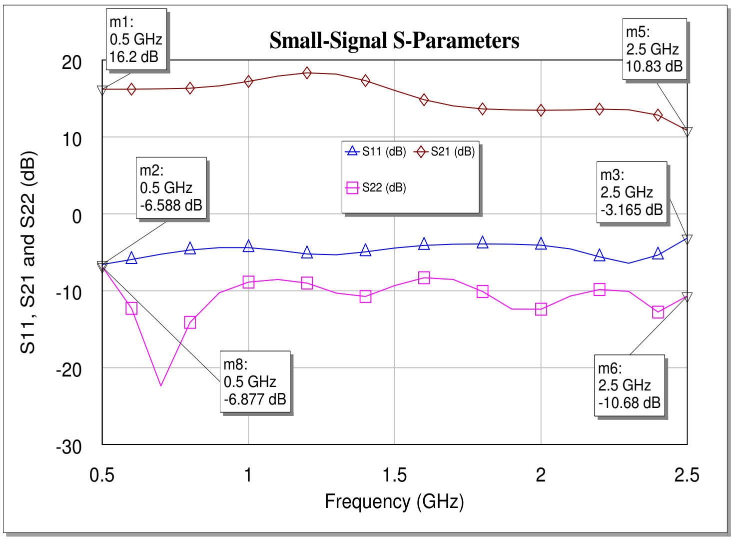


Figure 34: Final second-stage PA circuit



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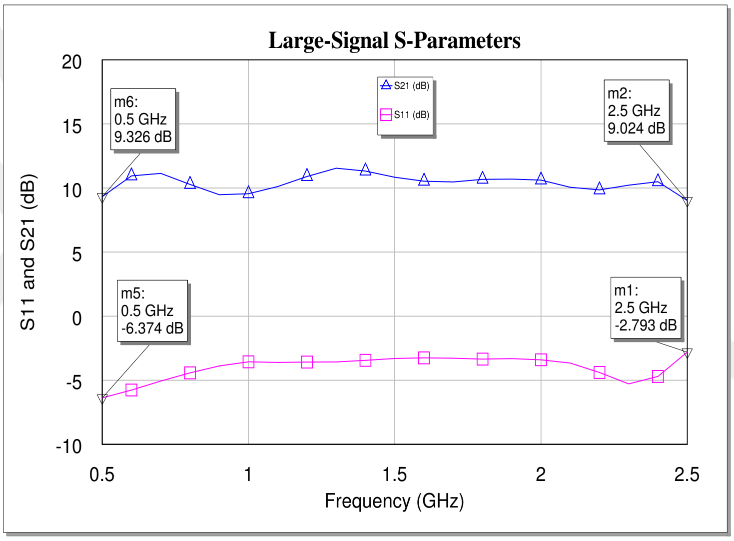

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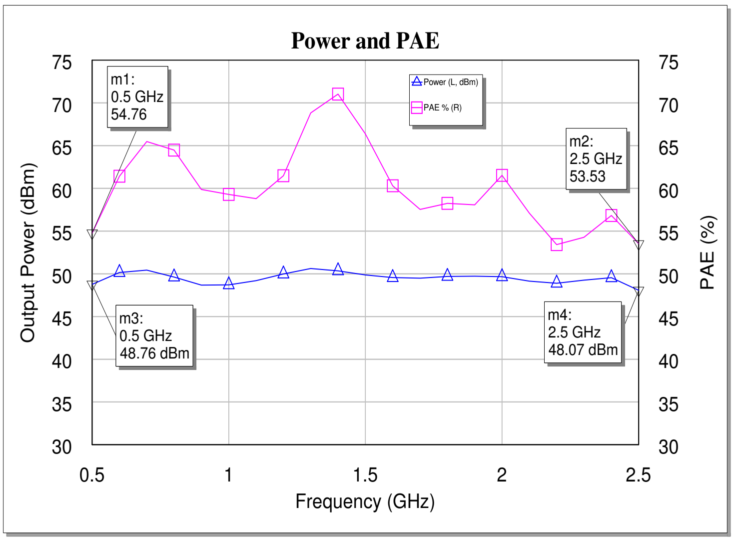
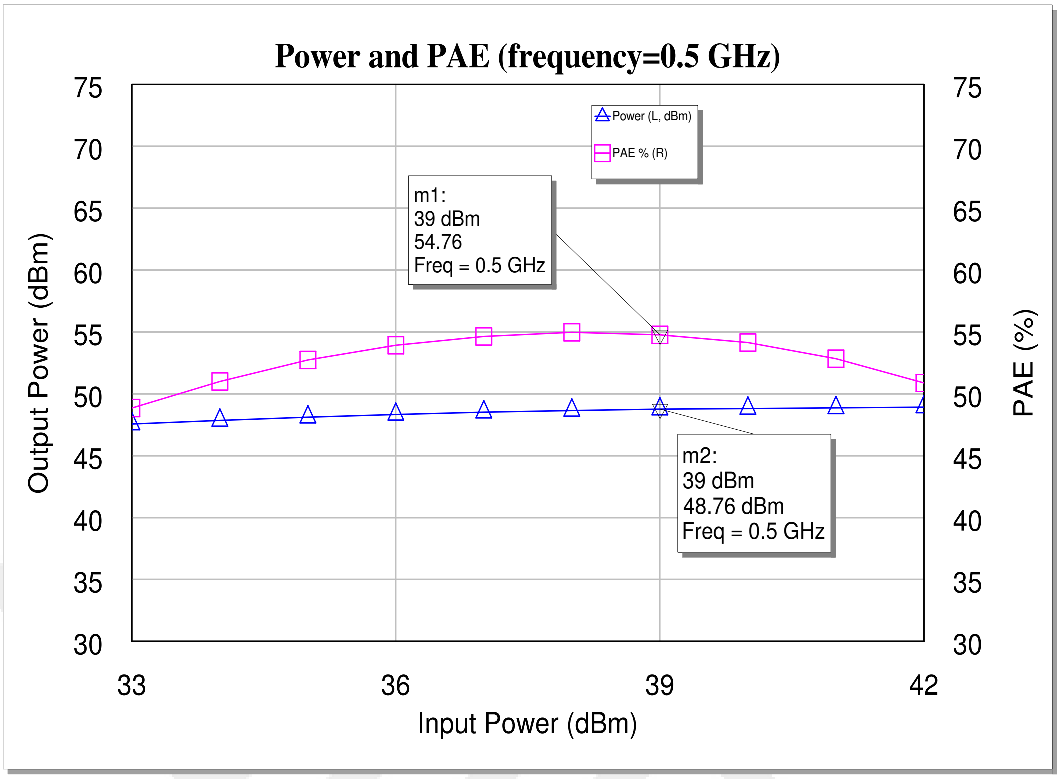


(c)

Figure 35: Simulated (a) small- and (b) large-signal S-parameters, (c) P_{out} and PAE of the second-stage PA



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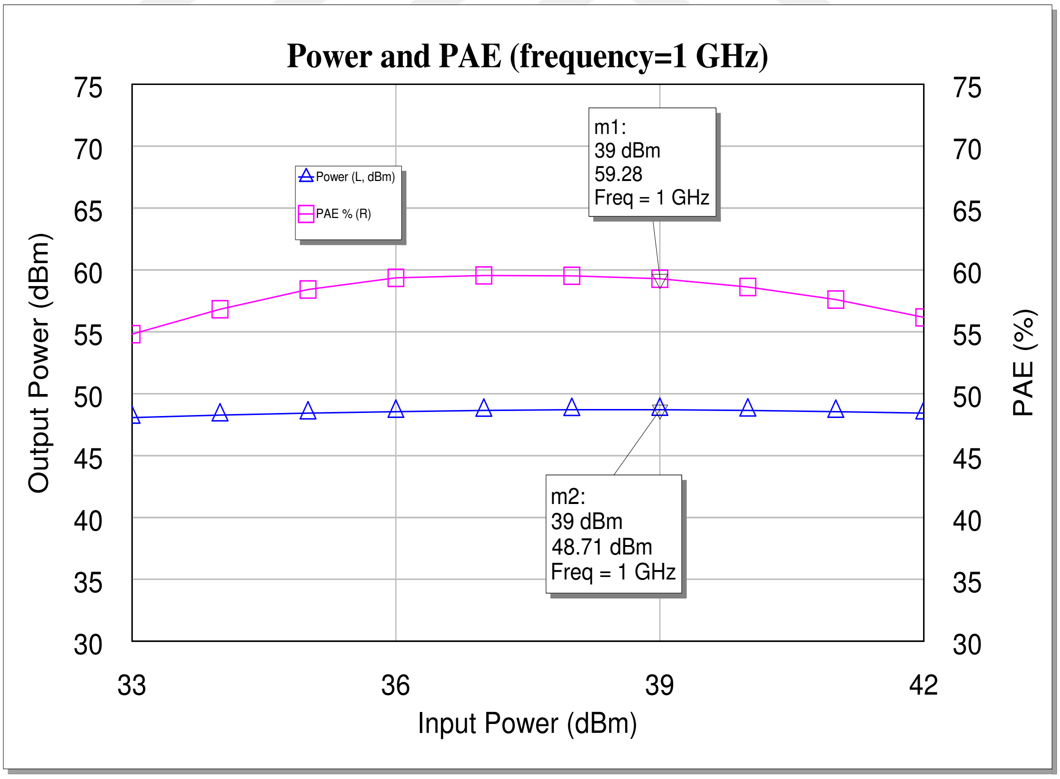
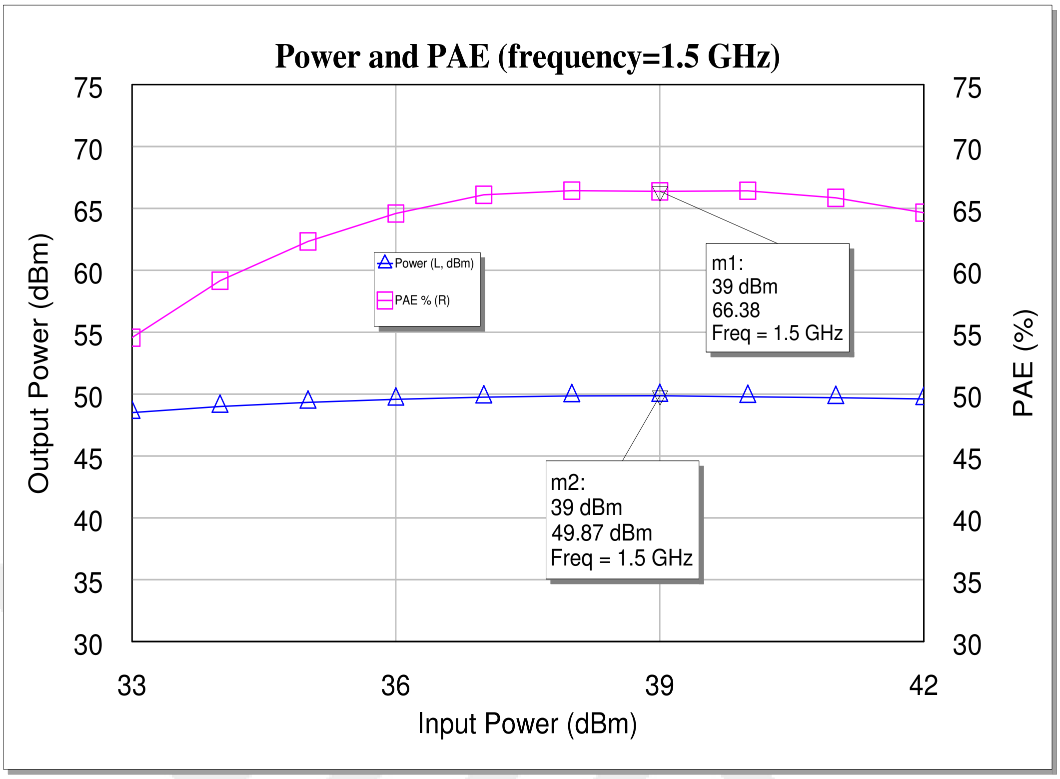


(b)

Figure 36: Simulated P_{out} and PAE vs P_{in} for the second-stage PA at (a) 0.5 GHz and (b) 1 GHz



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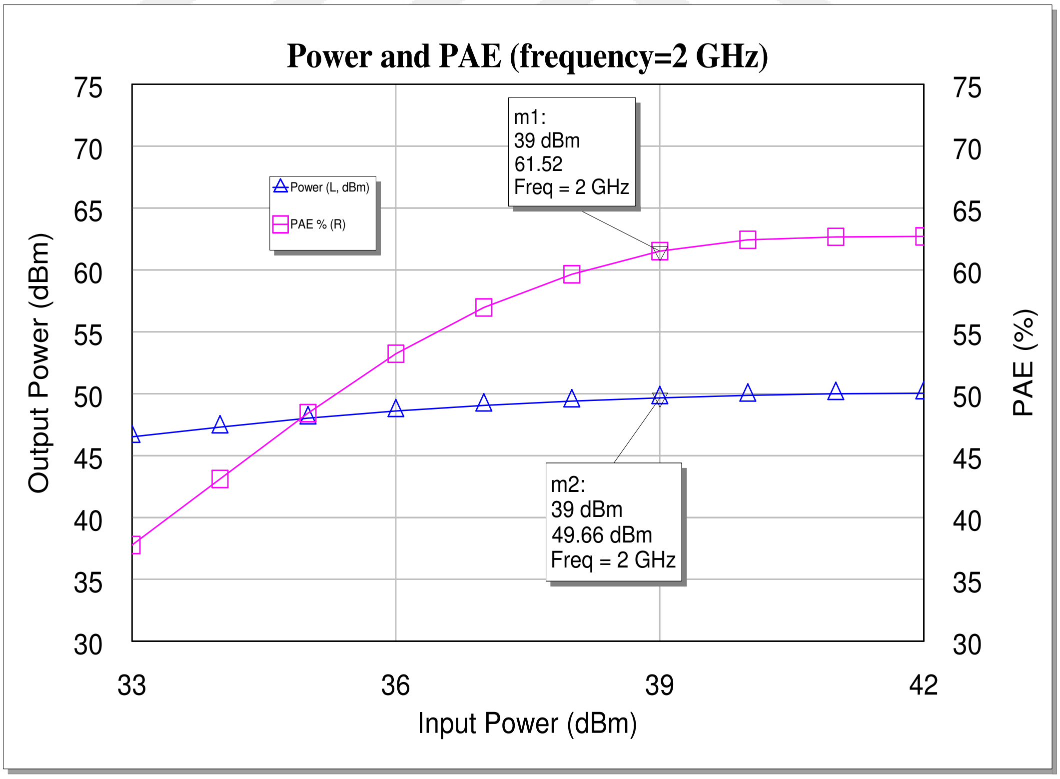

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Figure 37: Simulated P_{out} and PAE vs P_{in} for the second-stage PA at (a) 1.5 GHz and (b) 2 GHz

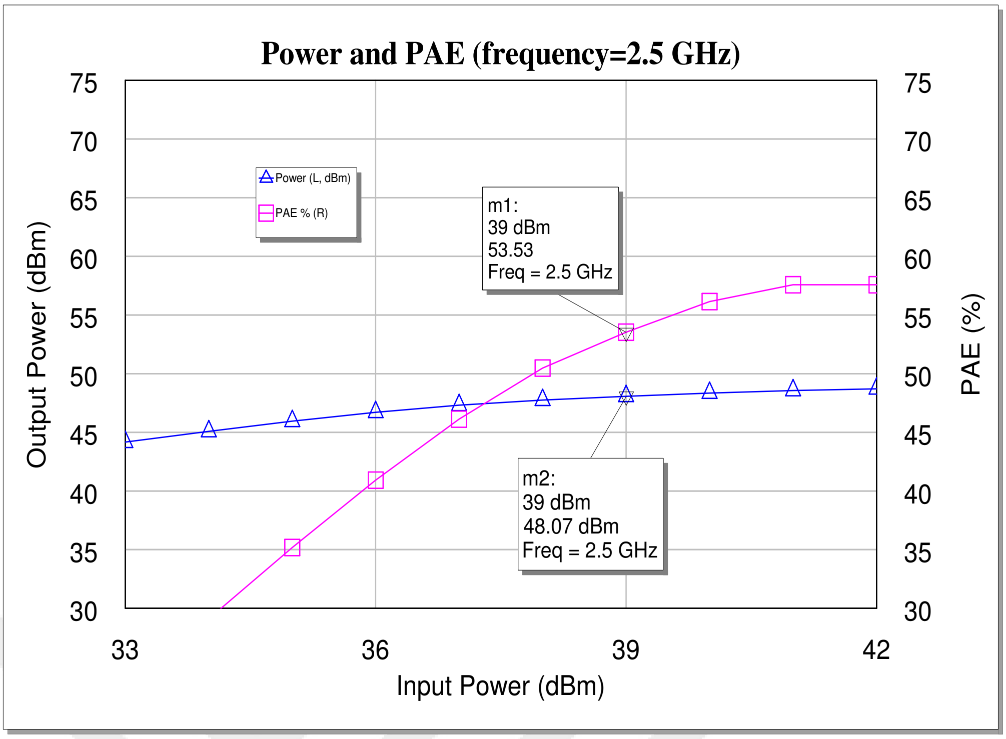
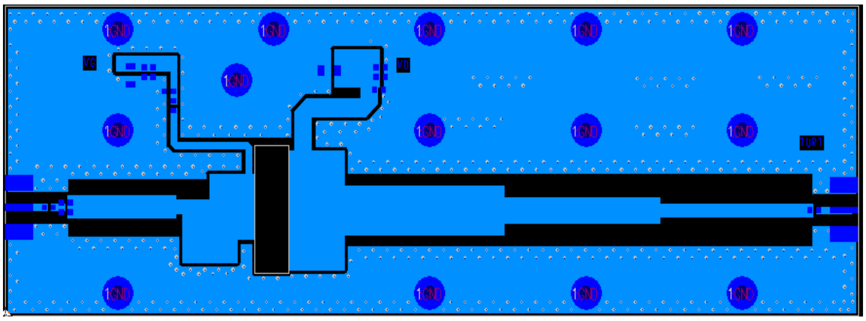


Figure 38: Simulated P_{out} and PAE vs P_{in} for the second-stage PA at 2.5 GHz

again, sacrificed in favor of better gain and this is clearly observed in both simulations and measurements. Small-signal gain of the simulated and implemented designs are in very good agreement across the frequency band with a minimum measured small-signal gain of 11.69 dB.

Block diagram and photo of the large-signal measurement setup for the second-stage power amplifier are illustrated in Figure 42. COTS power amplifier JA0530P52 is used to boost power from signal generator Agilent E8275D to drive the second-stage PA at 39 dBm. Keysight E3631A and 6032A DC power supplies are used to supply gate and drain voltages of -2.2 and 28 V, respectively. Large-signal power is measured using Keysight E4417A power meter with a 40 dB attenuator. For second and third harmonic measurements, Keysight N9030A PXA Signal Analyzer [22] is employed.

Figure 43 presents the measured output power, gain and PAE overlaid with simulated results. Large-signal gain comparison between simulated and fabricated design is also given in Figure 43. The measured P_{out} is higher than 47.1 dBm while the



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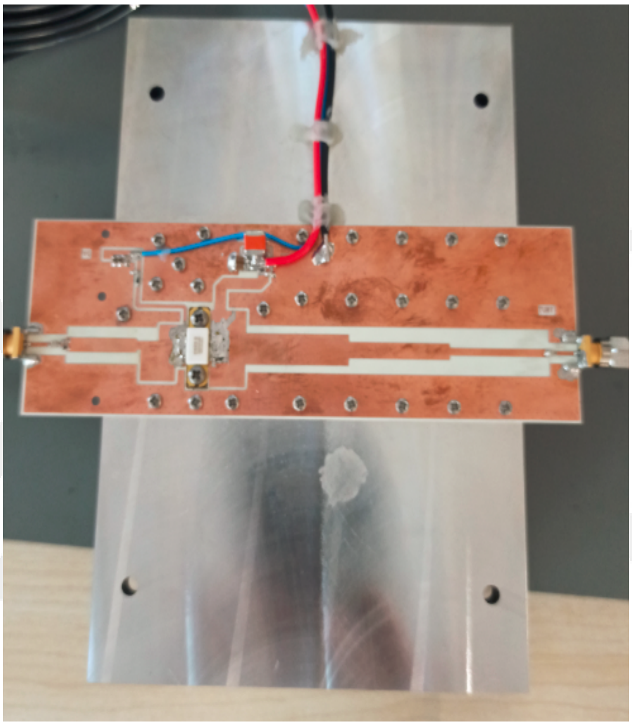
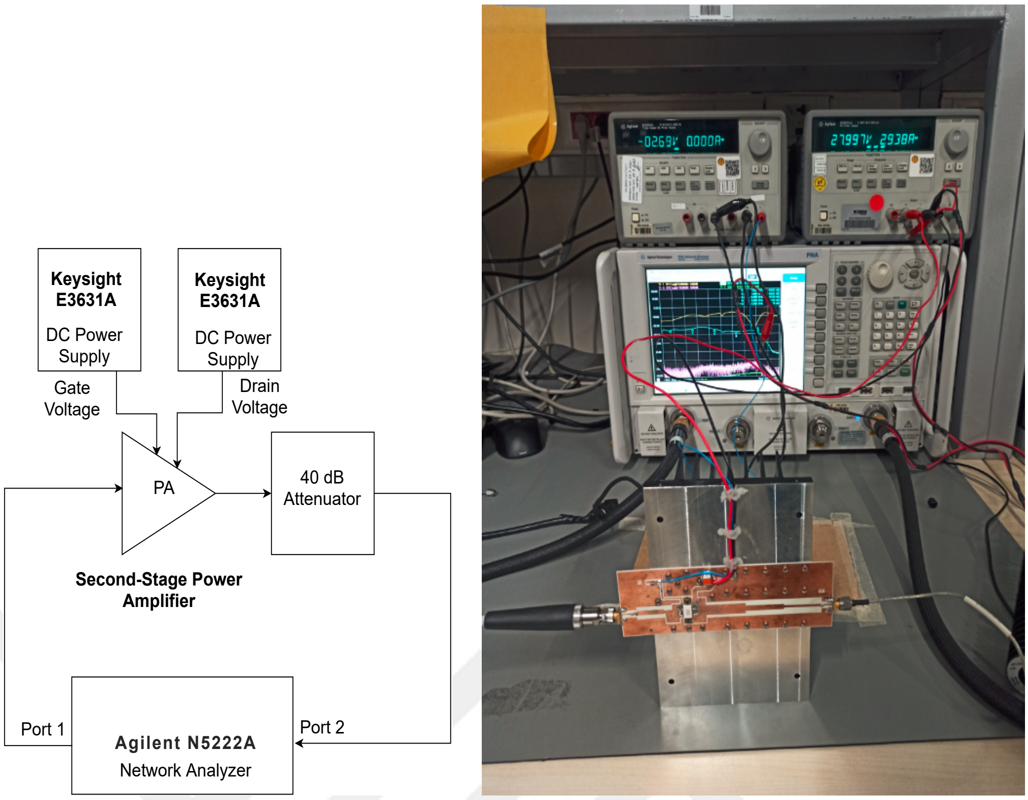


(b)

Figure 39: (a) Layout and (b) photo of the realized second-stage PA

measured PAE is between 45.3 and 70.6%. On the other hand, the simulated output power is between 48.1 - 50.6 dBm and simulated PAE is between 53.4 - 71% over the band. It is noted that while output power is at most 1 dB worse than simulations, measurements reveal a somewhat larger discrepancy in PAE. Large-signal gain of the fabricated system varies between 8.1 - 11.2 dB, while it is between 9.1 - 11.6 dB in simulations.

Harmonic levels of the second-stage PA is measured. Comparison of simulated and measured power in harmonic products is provided in Figure 44 which shows levels



(a) (b)

Figure 40: (a) Block diagram and (b) photo of the small-signal measurement setup

of the fundamental tone, second and third harmonic products. The lowest measured second harmonic level is 12.3 dBc at 0.6 GHz and the lowest measured third harmonic level is 10.4 dBc at 0.5 GHz. The second and third harmonic performance of the fabricated system is better than the simulated at most points.

For output power, gain, PAE, second and third harmonic level parameters, fabricated second-stage power amplifier shows similar performance to simulated design at most points. 90° transmission lines are used as RF chokes for the second-stage power amplifier design. In this way, parasitic effects caused by the use of RF inductors are eliminated. In the first and second-stage lab tests, it is noticed that metal heatsink under the transistor must have very good contact with PCB to ensure reliable operation. The metal heatsink must be conductive and must not have paint on it. Also, indium foil is used between transistor case and metal heatsink to facilitate cooling. There is a cut-out on the PCB to ensure good contact between the transistor and the

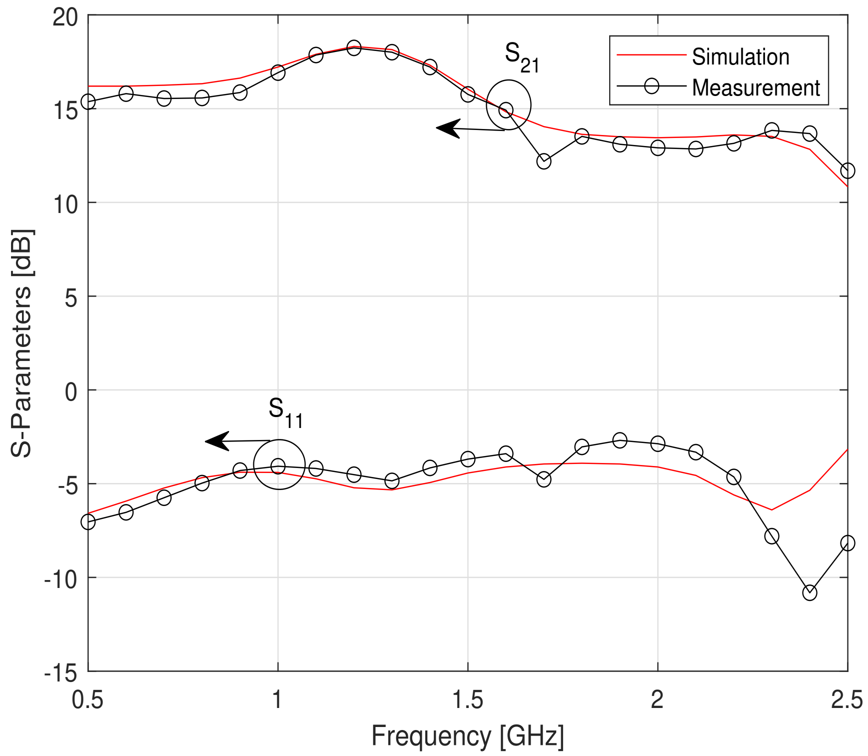
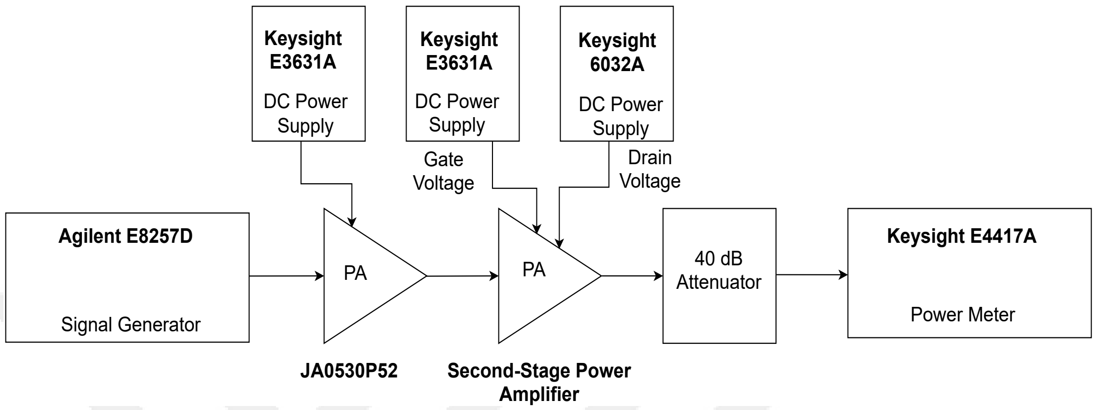
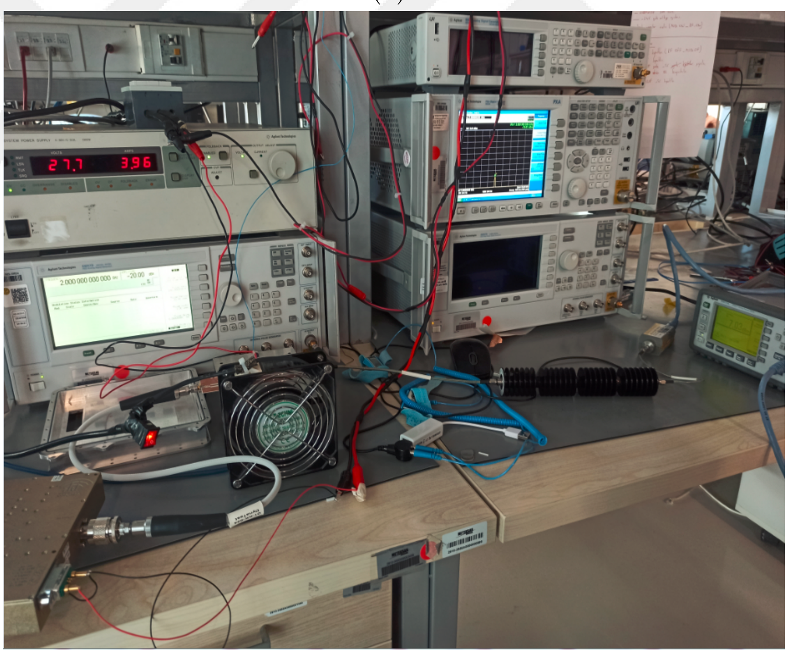


Figure 41: Measured and simulated small-signal S-parameters of the second-stage PA

metal case. The width of the cut-out should be as small as possible. As the width of the cut-out increases, the RF return path becomes longer, resulting in a mismatch in impedance. Screws are placed around the transistor on the PCB to achieve solid contact. These factors played an important role in achieving good agreement between measurements and simulations. Fairly small discrepancies observed in measurements could be attributed to SMA connectors and fabrication imperfections.



(a)



(b)

Figure 42: (a) Block diagram and (b) photo of the large-signal measurement setup

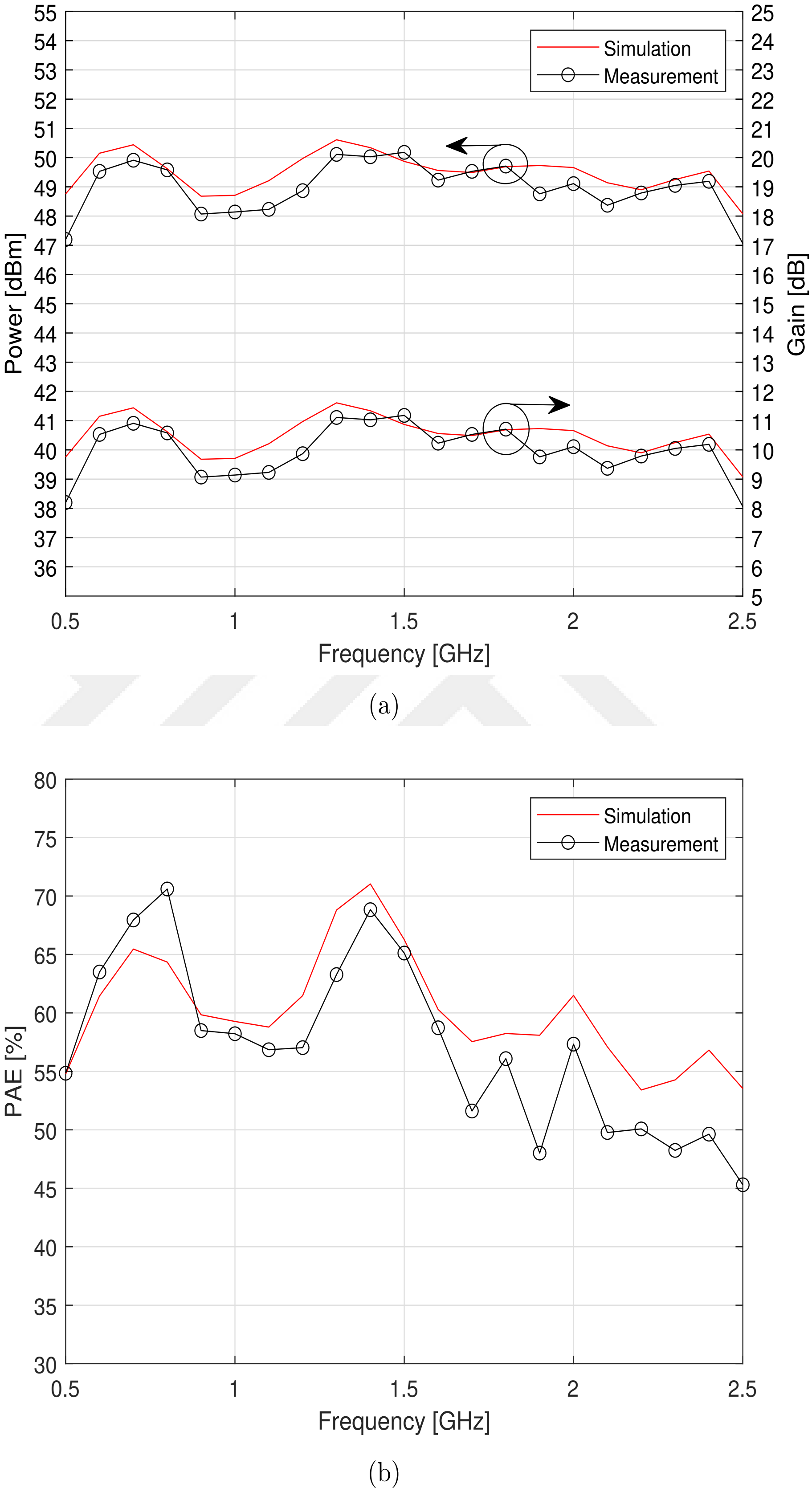
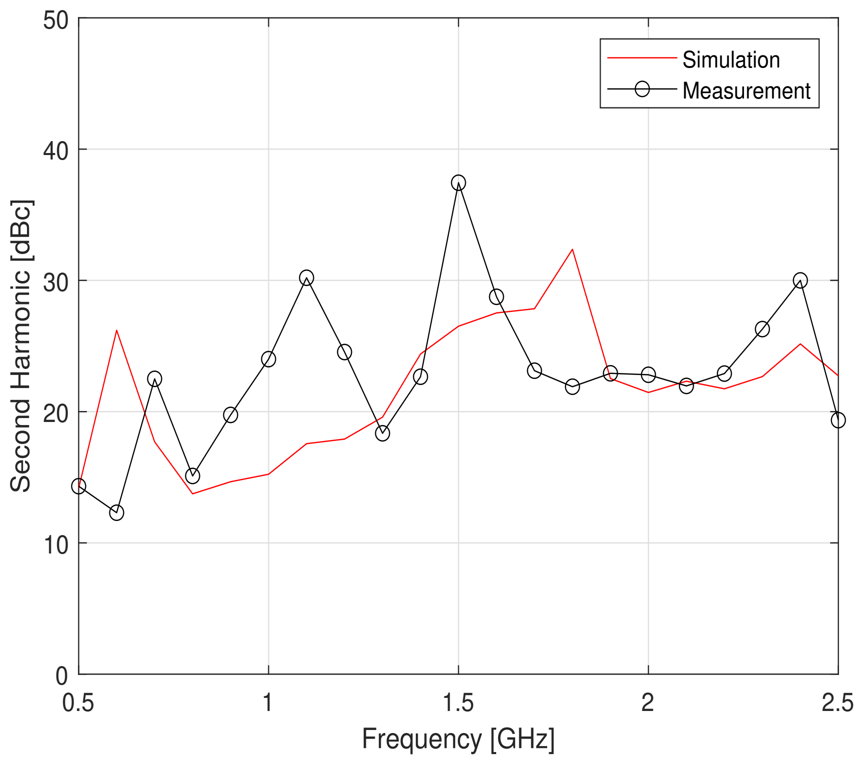
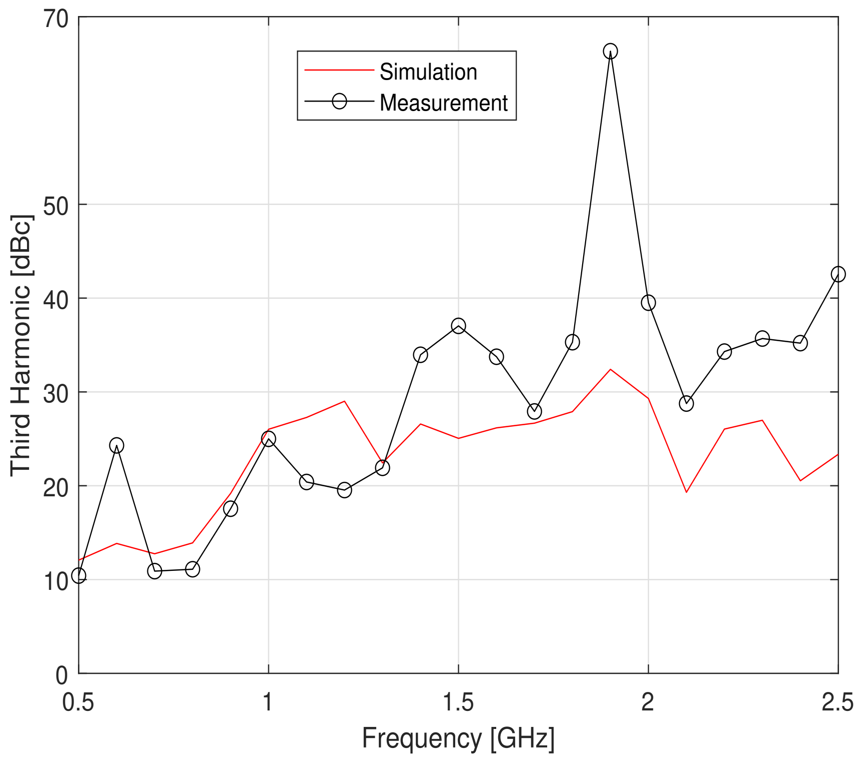


Figure 43: Measured and simulated (a) large-signal gain and P_{out}, and (b) PAE of the second-stage PA



(a)



(b)

Figure 44: Measured and simulated (a) second and (b) third harmonic levels of the second-stage PA

CHAPTER V

DESIGN & MEASUREMENTS OF TWO-STAGE BROADBAND CLASS-AB HIGH POWER AMPLIFIER

In this chapter, simulation and measurement results of the two-stage broadband Class-AB high power amplifier are described. Two-stage broadband Class-AB high power amplifier consists of the combination of the first and second-stage power amplifiers. After designs of individual stages are completed, they are combined at schematic level, and further optimization of inter-stage and output matching networks is performed. The individual stages are fabricated after this step of combined optimization. Table 4 summarizes the design goals of the cascaded two-stage amplifier.

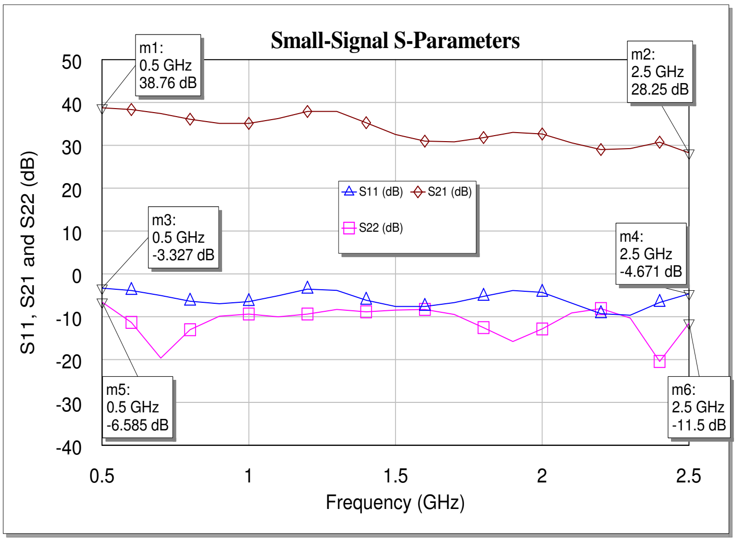
Table 4: Design goals of two-stage of broadband Class-AB high power amplifier

Output Frequency Range	0.5 - 2.5 GHz
Output Power	>48 dBm
PAE	>50 %

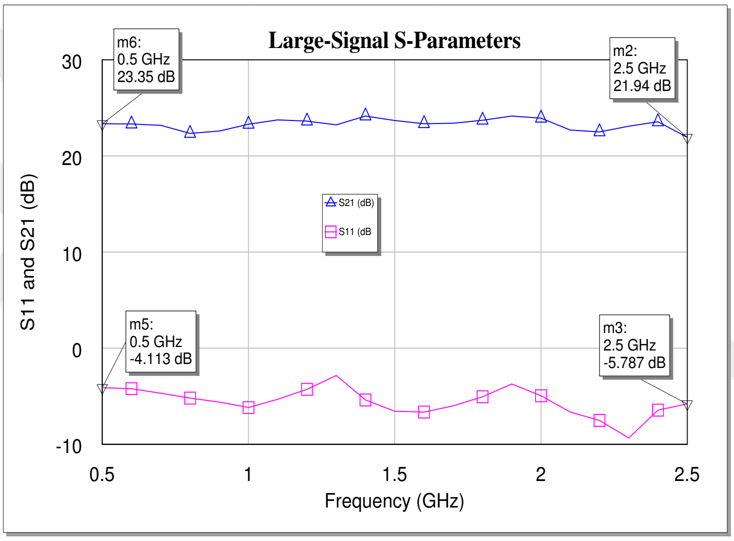
Simulated small-signal results are given in Figure 45. S_{11} varies between -3.3 - -9.7 dB, while S_{21} fluctuates between 28.2 - 38.8 dB. Also, Figure 45 depicts the S_{22} and minimum value of the S_{22} is -20.5 dB at 2.4 GHz.

Simulated large-signal gain, large-signal S_{11}, output power and PAE graphs are given in Figure 45. Simulations are conducted for an input power level of 26 dBm with swept frequencies. Minimum 48 dBm of output power and 50% of PAE is obtained as a result of the large-signal simulations.

Power and efficiency versus input power plots for different frequencies are present in Figure 46, Figure 47 and Figure 48.



(a)



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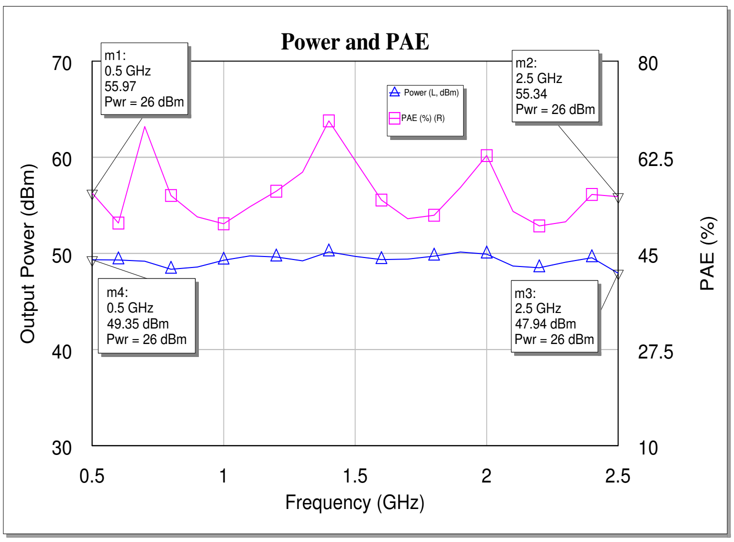
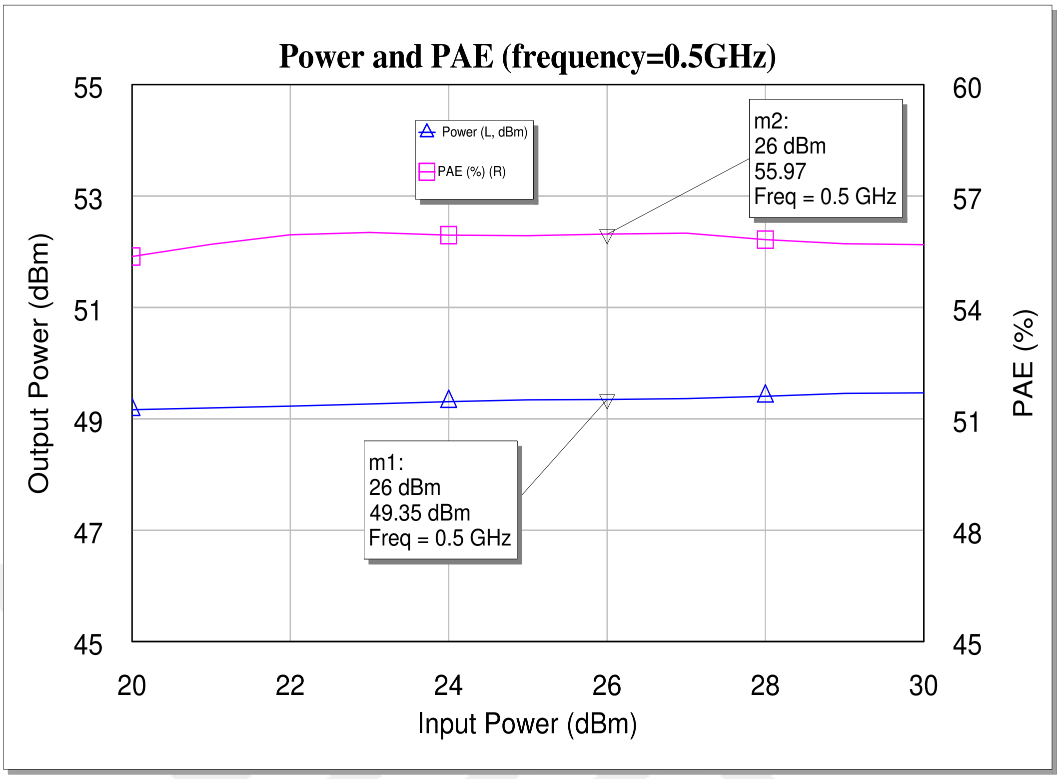
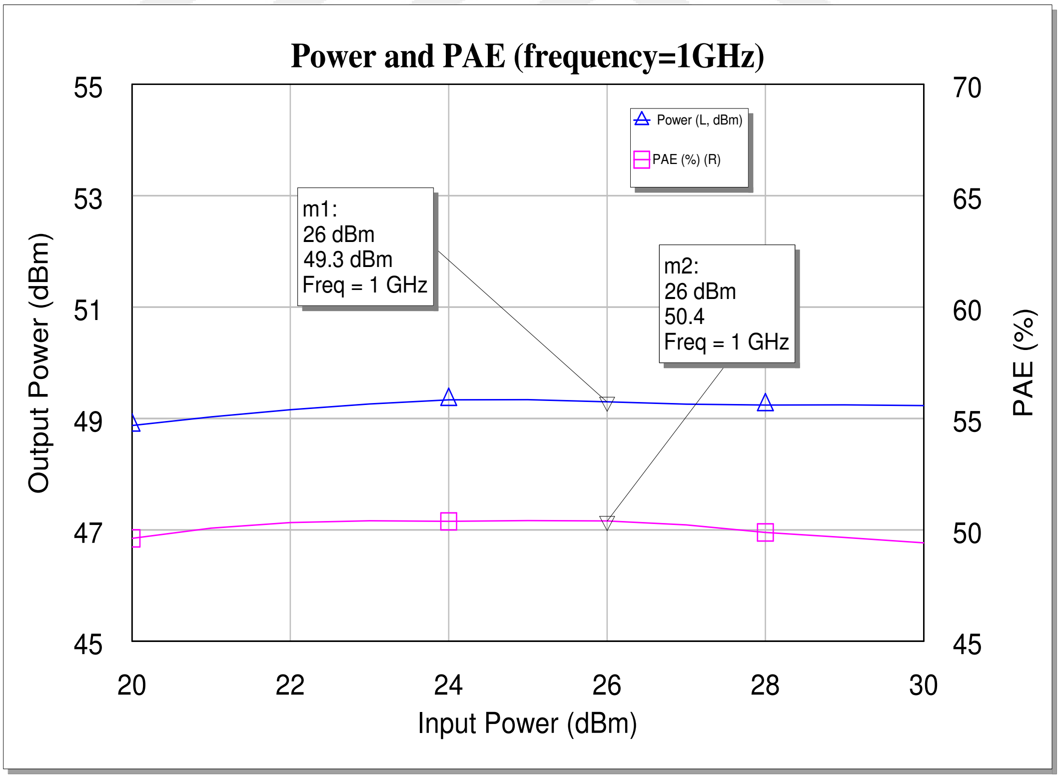


(c)

Figure 45: Simulated (a) small- and (b) large-signal S-parameters, (c) P_{out} and PAE of the two-stage PA

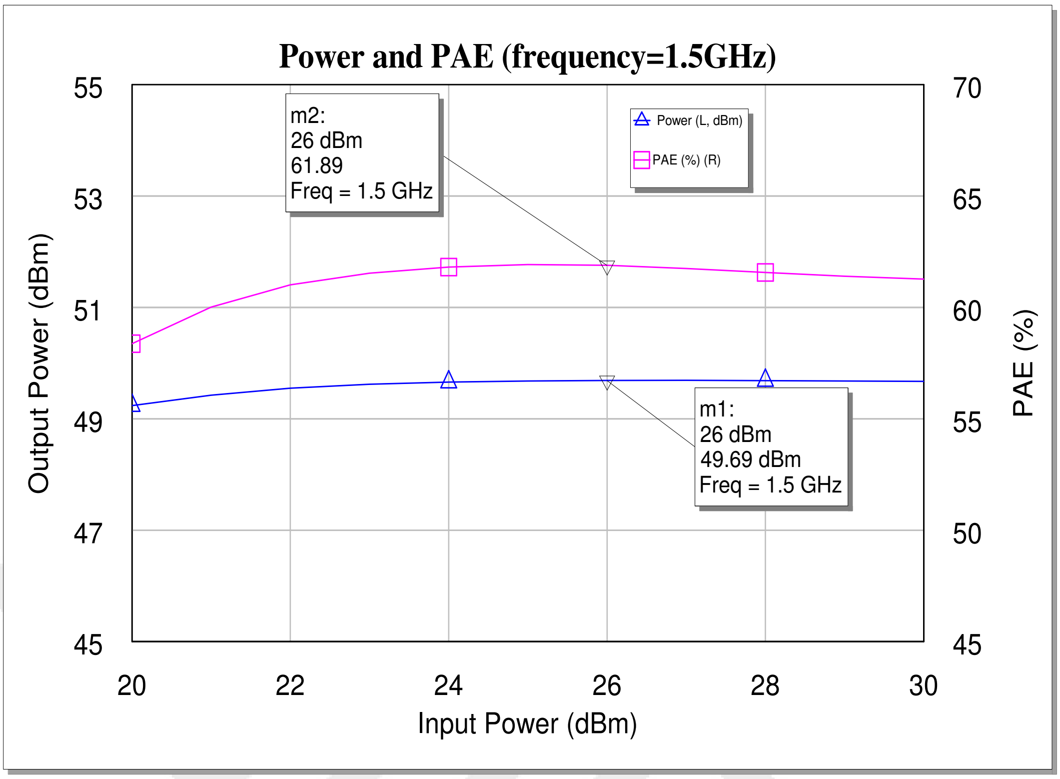


(a)

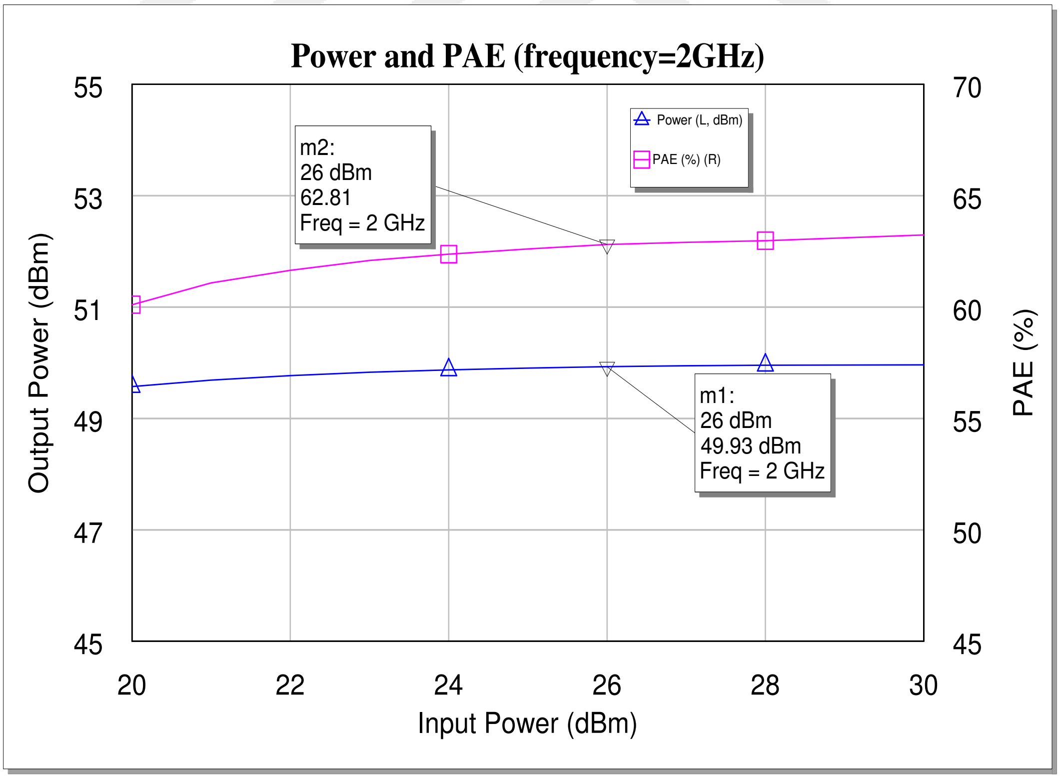


(b)

Figure 46: Simulated P_{out} and PAE vs P_{in} for the two-stage PA at (a) 0.5 GHz and (b) 1 GHz



(a)



(b)

Figure 47: Simulated P_{out} and PAE vs P_{in} for the two-stage PA at (a) 1.5 GHz and (b) 2 GHz

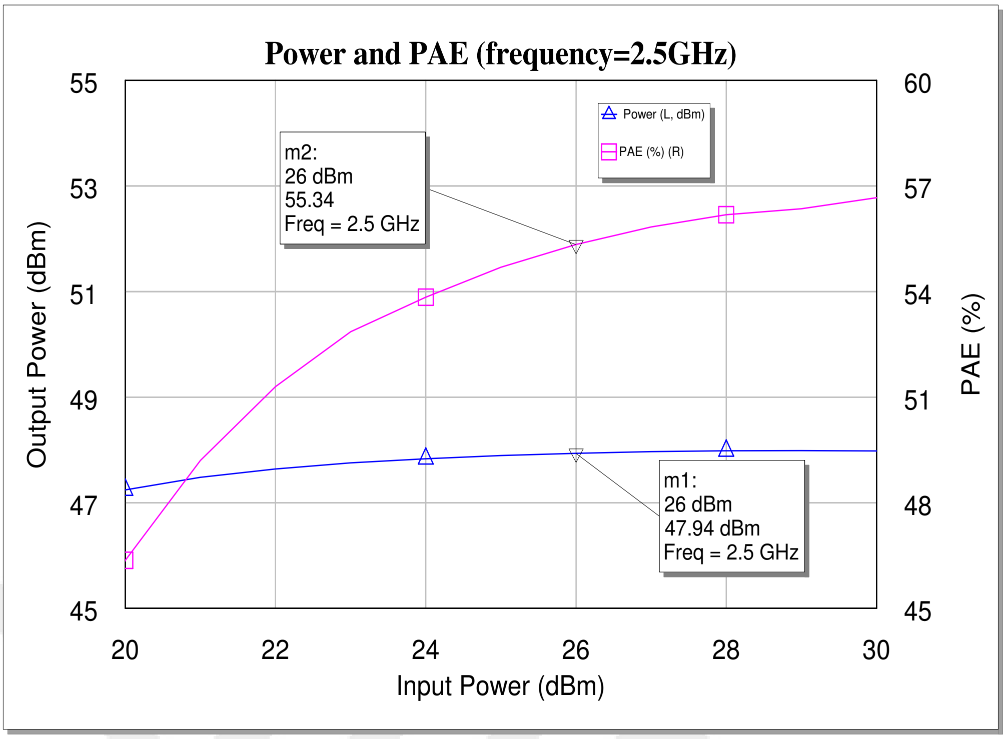


Figure 48: Simulated P_{out} and PAE vs P_{in} for the two-stage PA at 2.5 GHz

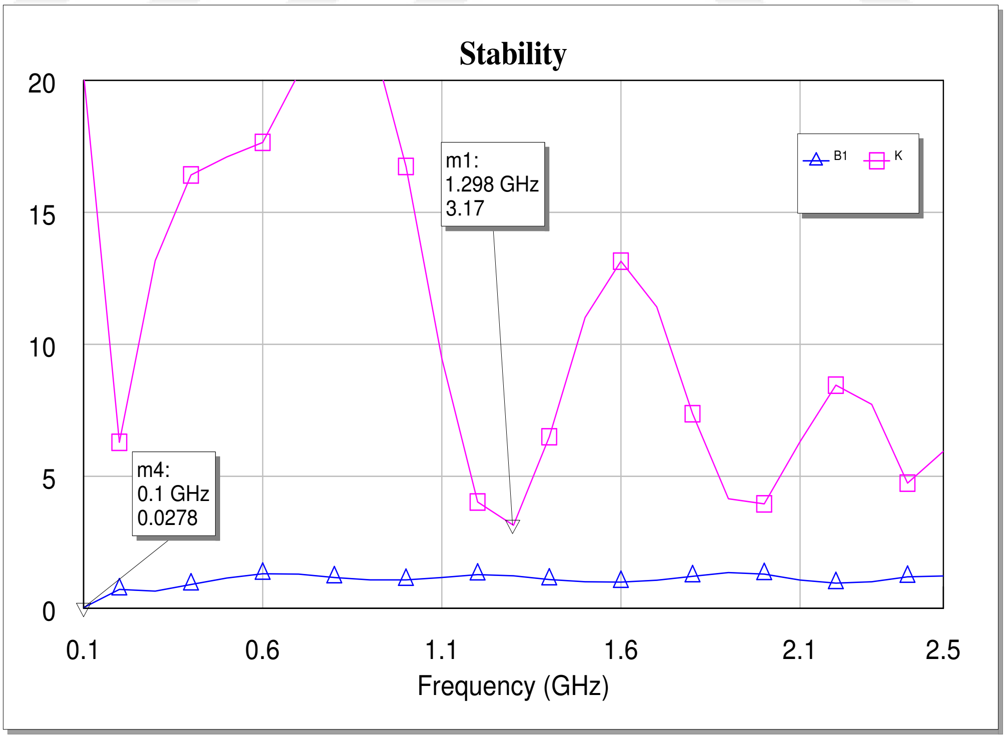


Figure 49: B1 and K stability for two-stage PA

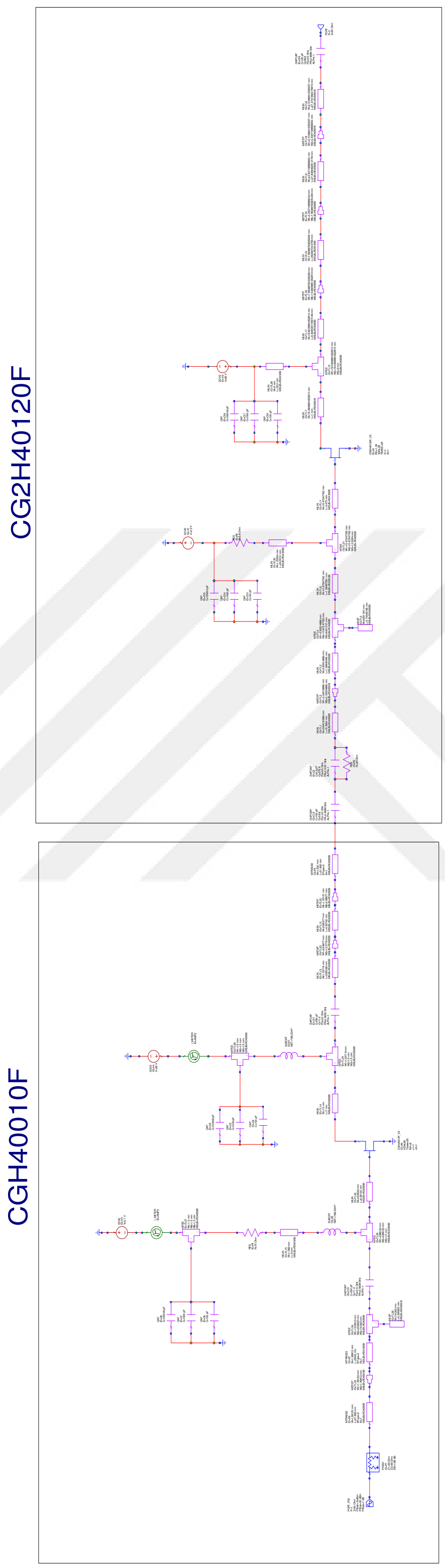


Figure 50: Final two-stage PA circuit

Stability analysis is conducted between 0.1 - 6 GHz and it is seen that the two-stage power amplifier is unconditionally stable. Figure 49 shows the B1 and K stability plots. Final two-stage power amplifier circuit is given in Figure 50.

5.1 Measurement Results of Two-Stage Broadband Class-AB High Power Amplifier

Large-signal analysis is performed for the proposed system from 0.5 to 2.5 GHz. For the large signal analysis, output power, gain and PAE, second and third harmonic levels are analyzed for the fabricated and simulated systems under CW input signals. Measurements are conducted for an input power level of 39 dBm with swept frequencies. Figure 53 presents the measured output power, gain and PAE versus simulation over the band. The measured output power is between $47.3-50.2$ dBm and measured PAE is between $43-65.6\%$ over the band.

On the other hand, the simulated output power is between $48-50.2$ dBm and simulated PAE is between $50-69.1\%$ across the frequency band. Large-signal gain comparison between simulated and fabricated design is also given in Figure 53. Large-signal gain of the fabricated system is greater than 21.3 dB, while it is between 22 - 24.2 dB in simulations.

Levels of the simulated higher harmonic products are provided to reveal large-signal analysis in depth. Figure 54 shows the levels of the fundamental tone, second and third harmonic products. The lowest second harmonic level is 8.2 dBc at 0.5 GHz and the lowest third harmonic level is 13.3 dBc at 0.8 GHz. The second and third harmonic performance of the fabricated system is better than the simulated at most points.

Two tone linearity test is carried out for OIP3 measurement. The gap between two tones is 10MHz. Figure 55 represents simulated and measured OIP3 results. As seen from the Figure 55, measured and simulated values are close to each other. The simulated OIP3 is between 53.28 - 64.8 dBm and measured OIP3 is between 56.5 -

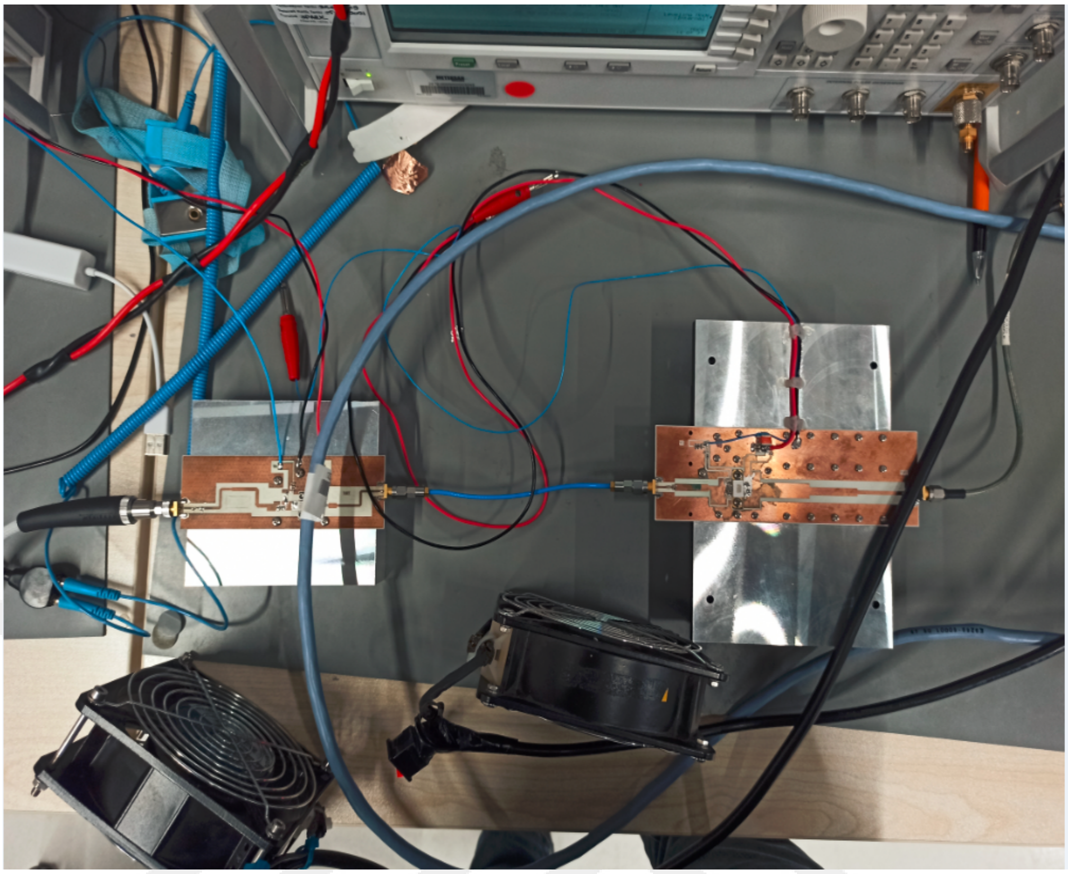
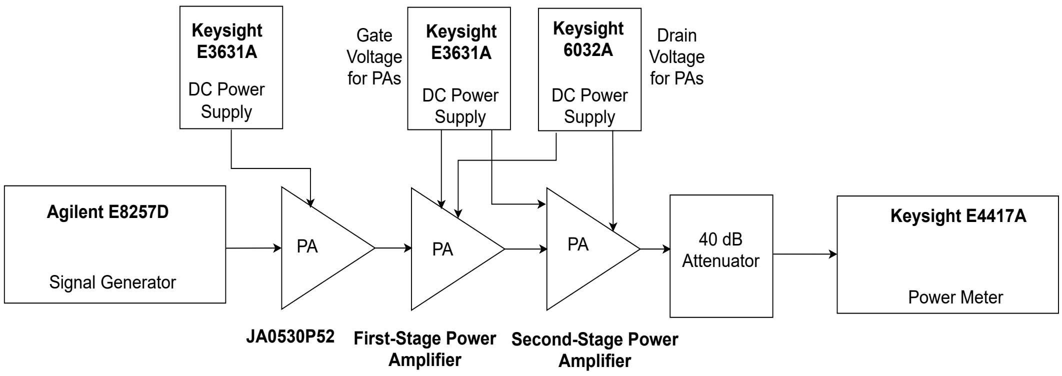


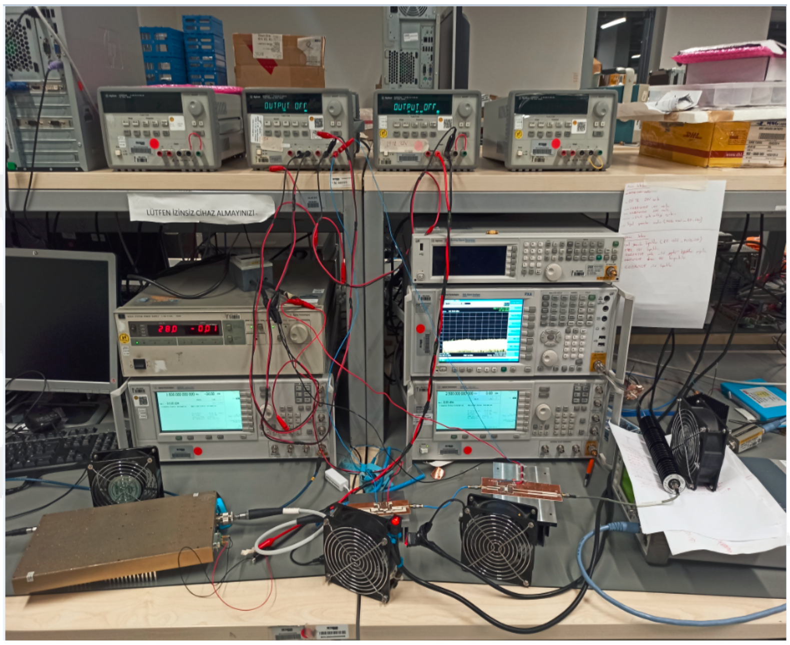
Figure 51: Implemented two-stage PA

66.6 dbm over the the band.

For output power, gain, PAE, second and third harmonic level parameters, fabricated second-stage power amplifier shows close performance to simulated design at most points. 50 Ω RF cable is used between the first-stage and second-stage power amplifiers during the lab tests. RF cable behaves like a transmission line and creates an impedance mismatch between power amplifiers. Apart from that, simulations are carried out with 50 Ω terminated source. Since there is no signal generator with an output power of 26 dBm in the laboratory, another power amplifier is added in front of the signal generator in the measurements, and a power level of 26 dBm is obtained. The output impedance of the ready-product power amplifier is not 50 Ω. In addition to this, RF connectors that are used at the input and output of the RF lines are not available. All of these factors mentioned above lead to impedance mismatch and



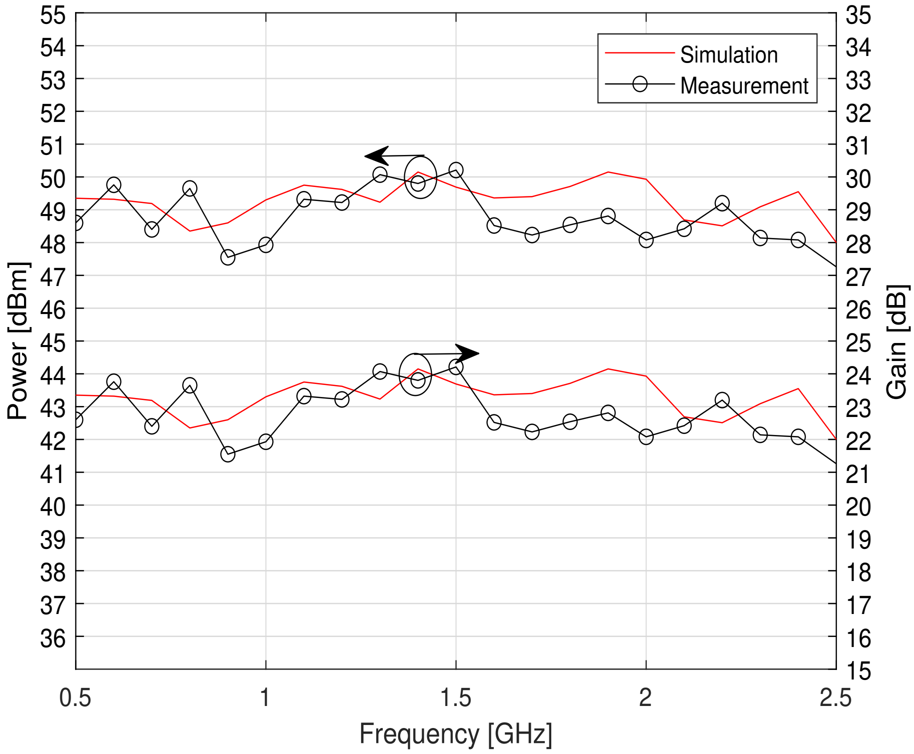
(a)



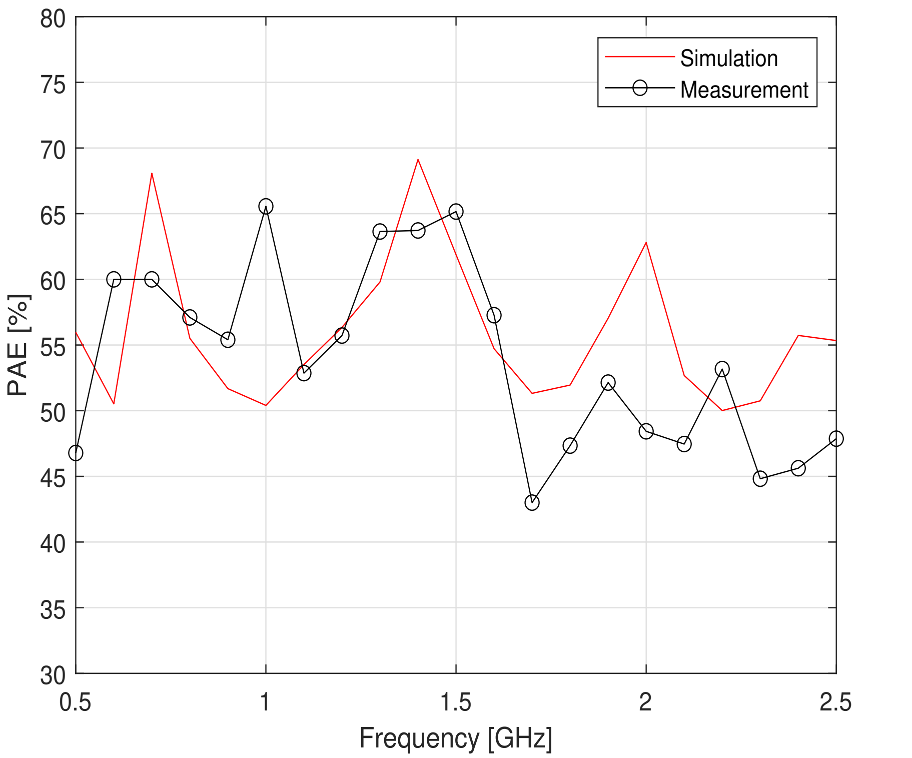
(b)

Figure 52: (a) Block diagram and (b) photo of the large-signal measurement setup

decrease output power, gain and PAE at some points.

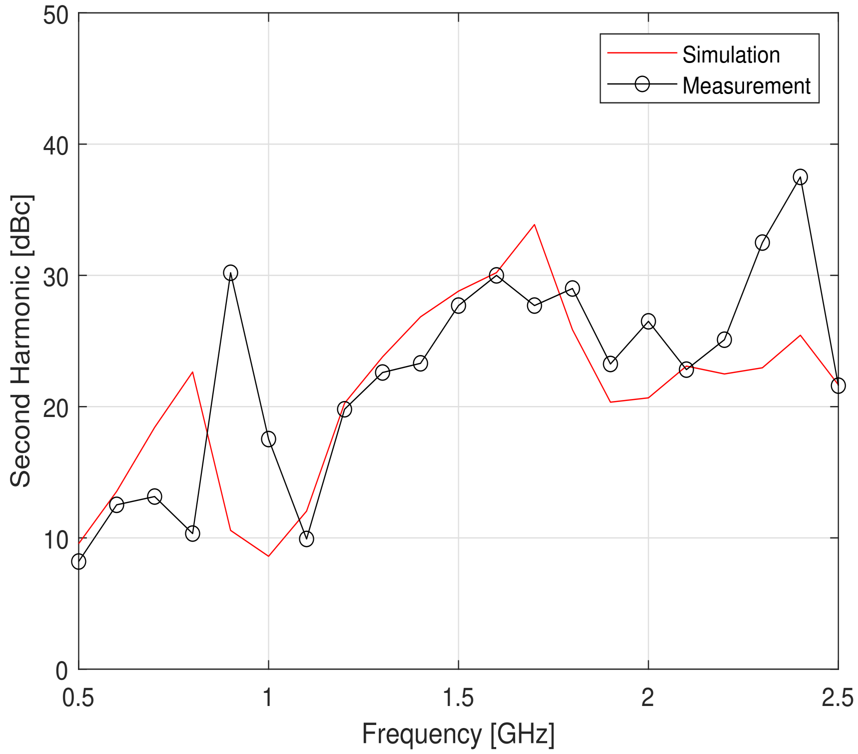


(a)

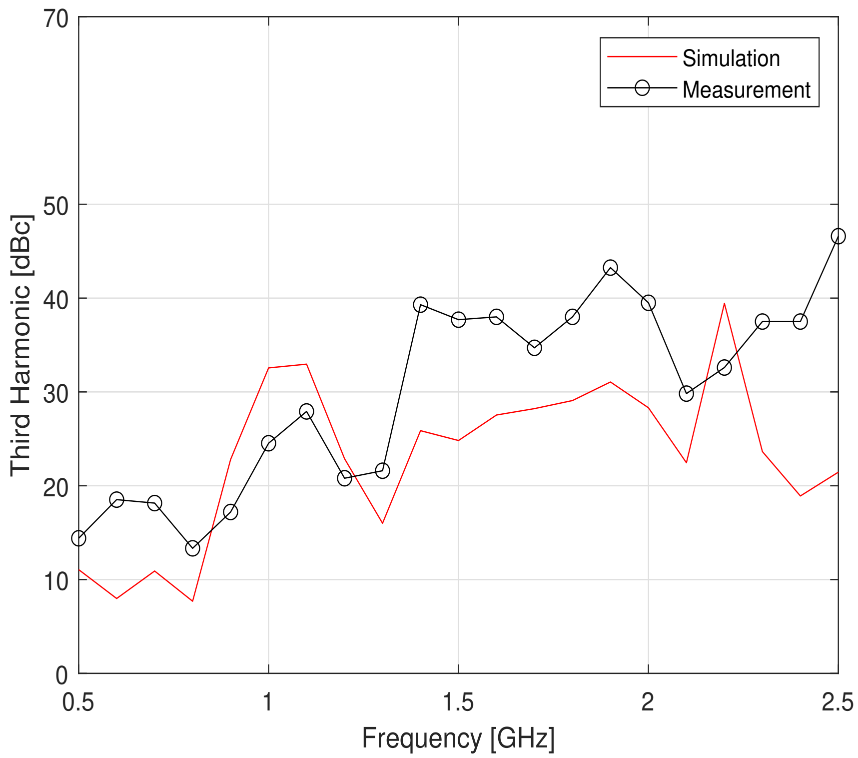


(b)

Figure 53: Measured and simulated (a) large-signal gain and P_{out}, and (b) PAE of the two-stage PA



(a)



(b)

Figure 54: Measured and simulated (a) second and (b) third harmonic levels of the two-stage PA

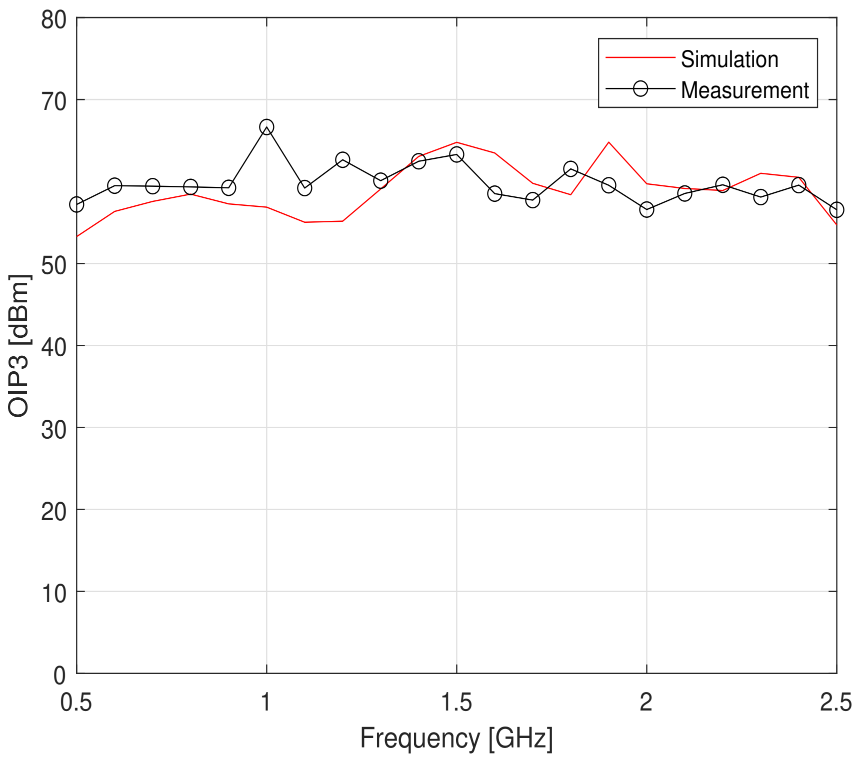


Figure 55: Measured and simulated OIP3 results of the two-stage PA

CHAPTER VI

CONCLUSION

This thesis presents design and measurements of two-stage broadband, high power, high efficiency power amplifier using GaN HEMT technology working over 0.5 - 2.5 GHz. The amplifier provides > 50 Watt output power and achieves 43% power-added efficiency. The amplifier could be useful in radio systems, radars and electronic warfare systems.

Two-stage power amplifier consists of the first- and second-stage power amplifiers. After designs of individual stages are completed, they are combined at schematic level, and further optimization of inter-stage and output matching networks is performed. These PAs are then fabricated and characterized separately. Then, these amplifiers are cascaded and characterized. Wolfspeed CGH40010F and CG2H40120F are used to design first-stage and second-stage PAs, respectively. The first-stage amplifier is designed to achieve higher than 50% PAE and 40 dBm output power. Measurements reveal minimum output power and minimum PAE of 39.6 dBm and 45.9%, respectively. The second-stage power amplifier is designed to obtain better than 50% PAE and 48 dBm output power. Measured minimum output power and PAE are 47.1 dBm and 45.3%, respectively. For the combined amplifier, the design goals are 50% PAE and 48 dBm output power while minimum output power and minimum PAE are measured to be 47.3 dBm and 43%, respectively.

For the first-stage, second-stage and two-stage power amplifier designs, simulation and measurement results are in fairly good agreement over much of the frequency range. For the first-stage power amplifier, results are better than simulations at most points between 0.5 - 1.3 GHz; however, beyond this point, there is a drop in measured results compared to simulated results. It is thought that the use of RF inductor as RF choke has an important role in this decrease due to its parasitic effects. Thus, it is decided to use 90° transmission lines as RF chokes for the second-stage power amplifier design. The measurement results of the second-stage power amplifier are much closer to the simulation results compared to the first-stage amplifier. In laboratory tests, it is observed that heatsink on which the transistor is placed must have very good contact with the PCB. The metal heatsink surface must be very conductive and must not have any paint on it. Use of indium foil facilitates heat transfer from the transistor case to the heatsink. SMA connectors, inter-stage RF cable not taken into account in simulations and parasitics are other factors believed to contribute differences between measurements and analyses.

For further development of this power amplifier, re-design of the first-stage PA to employ transmission lines instead of RF chokes on DC lines could help improve efficiency and output power of the amplifier in the upper half of the frequency range.

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