REPUBLIC OF TURKEY
YILDIZ TECHNICAL UNIVERSITY
GRADUATE SCHOOL OF SCIENCE AND ENGINEERING

GENETIC ALGORITHM BASED DELAY OPTIMIZATION FOR SWITCHLESS ARINC 664 NETWORK TOPOLOGIES

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MASTER OF SCIENCE THESIS
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A thesis submitted by Bekir GÜL in partial fulfillment of the requirements for the degree of **MASTER OF SCIENCE** is approved by the committee on 17.02.2022 in Department of Avionics Engineering, Program of Avionics Engineering.

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Bekir GÜL

Signature

Dedicated to my family

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Bekir GÜL

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LIST OF SYMBOLS

$\alpha(t)$	Arrival Curve
S_n	Burst of Flow
η	Crossover Rate
μ	Elite Ratio
f_n	Flow of n^{th}
J	Jitter
D_m	Maximum Delay
L_{max}	Maximum Frame Size
$\alpha^*(t)$	Modified Arrival Curve
$1-\eta-\mu$	Mutation Rate
P_{VL}	Path of VL
r_n	Rate of Flow
R_m	Service Capacity
$\beta(t)$	Service Curve
T_m	Technological Latency

LIST OF ABBREVIATIONS

AFDX	Avionics Full-Duplex Switched Ethernet
ARINC	Aeronautical Research Incorporated
BE	Best Effort
CM	Compression Master
COTS	Commercial off-the-shelf
ES	End System
GA	Genetic Algorithm
IMA	Integrated Modular Avionics
LRU	Line Replaceable Units
NC	Network Calculus
OS	Operating System
PCP	Priority Code Point
RC	Rate Constrained
SC	Synchronization Client
SM	Synchronization Master
SW	Switch
SWaP	Size Weight and Power
TSN	Time Sensitive Network
TT	Time Triggered
VLAN	Virtual Local Area Network
VL	Virtual Link

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ABSTRACT

Genetic Algorithm Based Delay Optimization for Switchless ARINC 664 Network Topologies

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Department of Avionics Engineering
Master of Science Thesis

Supervisor: Asst. Prof. Muhammet GARİP
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The necessity of modern avionics systems that require more complicated capabilities is emerging as the technology develops. The Integrated Modular Avionics (IMA) concept in next-generation avionics systems provides significant advantages in terms of size, weight, and power consumption. A new architecture with improved flexibility, extensibility, and functional complexity is required. That approach requires the use of deterministic network technology. The ARINC-664 protocol is a prominent embedded communications technology in civil and military aircraft. Ethernet-based ARINC-664 deterministic network technology has been widely used to meet IMA systems' high-speed data communication requirements. In this thesis, the delay performance of the ARINC-664 network architecture, which separates the end system and switches elements, the ring network, and the switchless network topology, which integrates the network switch functions into the end system, is compared. The number of possible VL routes starts to rise as the number of ES ports increases in switchless ARINC-664 network topologies. To calculate the lowest latency limitations, all combinations of these VL routes must be examined in the corresponding network topology. As a result, there are a huge number of different routing configurations in the network topologies. Therefore, we utilize GA-based delay optimization for these network topologies. The results of the worst-case delay analysis calculated with the Network Calculus approach show that the average and maximum delay values are always smaller in the switchless network topology. Furthermore, the average and maximum delay values decrease as the number of ports in the end system increases.

In future work, it is aimed to decrease the memory usage rate, which increases in proportion to the number of ES ports.

Keywords: ARINC-664, network calculus, deterministic network, avionics systems

ÖZET

Anahtarsız ARINC 664 Ağ Topolojileri için Genetik Algoritma Tabanlı Gecikme Optimizasyonu

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Yüksek Lisans Tezi

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Eş-Danışman: Dr. İbrahim HÖKELEK

Modern aviyonik sistemler, teknoloji geliştikçe daha karmaşık hale gelen fonksiyonel özellikleri kullanmayı gerektirir. Yeni nesil aviyonik sistemleri kullanan uçaklar için Entegre Modüler Aviyonik (EMA) konsepti boyut, ağırlık ve güç tüketimi açısından avantajlar sağlamaktadır. Gelişmiş esneklik, genişletilebilirlik ve fonksiyonel karmaşıklık ile yeni bir mimari gereklidir. Bu aviyonik mimariyi uygulamak için deterministik ağ teknolojilerini kullanmak gerekmektedir. ARINC-664 protokolü, sivil ve askeri uçaklarda kullanılan gömülü iletişim teknolojisidir. EMA sistemlerinde yüksek hızlı veri haberleşmesi ihtiyacını karşılamak için Ethernet tabanlı ARINC-664 gerekirci ağ teknolojisi kullanılmaktadır. Bu tezde, ARINC-664 sistemleri için uç sistem ve ağ anahtarı elemanlarının ayrık olduğu referans ağ topolojisi ile, halka ağı ve ağ anahtar fonksiyonlarının uç sisteme taşındığı anahtarsız topolojilerin gecikme karşılaştırılması yapılmaktadır. Anahtarsız ARINC-664 ağ topolojilerinde Uç Sistem (US) port sayısı arttıkça olası Sanal Bağlantı (SB) rotalarının sayısı artmaya başlar. En düşük gecikme sınırlamalarını hesaplamak için bu SB yollarının tüm kombinasyonları ilgili ağ topolojisinde incelenmelidir. Sonuç olarak, ağ topolojilerinde çok sayıda yönlendirme yapılandırması vardır. Bu ağ topolojilerinin SB gecikmelerini iyileştirmek için Genetik algoritma tabanlı gecikme optimizasyonunu kullanılmaktadır. Ağ Hesabı(Network Calculus) yaklaşımı ile hesaplanan en kötü durum gecikme analizi sonuçlarına göre ortalama ve en büyük gecikme değerlerinin anahtarsız topolojide her zaman daha küçük olduğu görülmektedir. Aynı zamanda, ortalama ve en büyük gecikme değerleri uç sistemdeki kapı sayısıyla ters orantılı olarak azalmaktadır.

Gelecek çalışmalarda kapı sayısı ile orantılı olarak artan hafıza kullanım oranın düşürülmesi hedeflenmektedir.

Anahtar Kelimeler: ARINC-664, ağ hesabı, gerekirci ağ, aviyonik sistemler

1
INTRODUCTION

1.1 Literature Review

The electronics of aircraft are defined as "avionics," which is derived from the words aviation and electronics. The term avionics was originally used in the United States in the early 1950s, and has since achieved widespread acceptance and usage [1]. Avionics systems are crucial for performing the aircraft's mission safely and efficiently. Traditionally, an aircraft's avionics consisted of federated systems including radar, navigation, communication, and cockpit display, all connected by dedicated cables. The sensors and instrument structure in aircraft have been becoming increasingly complex in parallel with the development of next-generation aircraft. With the widespread usage of digital technology, the number of devices, which require information exchange, has been significantly increased. This need for communication increased the number of cables within the aircraft, resulting in increased power consumption and weight. The use of busses was introduced in aviation, and this helped to reduce the number of wiring and simplify the overall design, as well as maintenance [1].

The traditional avionics network architecture was developed by a federated architecture, where the functions of each device in the aircraft are independent. As technology evolves, modern avionics systems require more functions that are becoming more complex. Therefore, the federated architecture is not appropriate for modern avionics systems [2]. There is a need for a new architecture that provides flexibility, extensibility, and increased functional complexity. The concept of Integrated Modular Avionics (IMA) has been proposed to address these challenges. The IMA aims to utilize common hardware and software modules for different applications. Compared to federated systems using application-specific devices, the IMA concept offers significant advantages in terms of size, weight, and power consumption (SWaP). In addition, the ARINC 651 standard for IMA architecture and the ARINC 653 standard for the underlying operating system were needed to avoid operational breakdowns and interruption between tasks. The partition paradigm offers a safe mechanism for separating functions and preventing interference. Consequently, it is enabled that new partitions to be added without affecting other modules [3].Undoubtedly, IMA will improve software implementation and validation. Avionic designers conclude that the transition from federated architecture to IMA occurs because of these encouraging features. The federated and IMA architectures are shown in Figures 1.1 and 1.2, respectively.

The Integrated Modular Avionics concept is used to meet the high-speed data processing requirements of the next generation of aircraft. The IMA concept requires high-speed and deterministic networks, modularity, rapid reconfiguration, and an open common modular architecture. As shown in Figure 1.1, federated architectures do not share components, information timesharing between subsystems in the avionics suite. In contrast, IMA architectures allow supporting multiple functions on the same components [4].

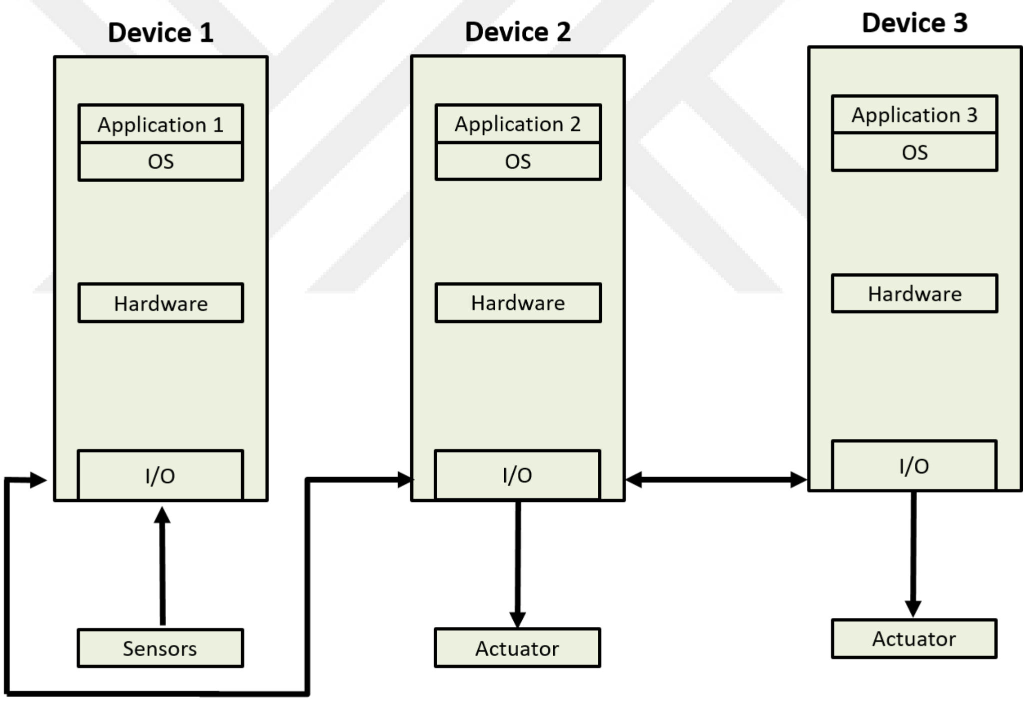

Figure 1.1 Federated avionics architecture [5]

The ARINC-664 standard has been developed to address high-speed communications requirements in IMA systems. ARINC-664 is used to provide deterministic data transfer between modules within IMA systems, as shown in Figure 1.2. ARINC-664 supports minimal interconnections between network nodes and can provide robust and reliable connectivity to the interconnected system in the event of a failure. In avionics systems, deterministic network technologies are used to keep delay and jitter values below a certain limit so that safety-critical applications can communicate with each other. Although widely used communication standards such as ARINC 429

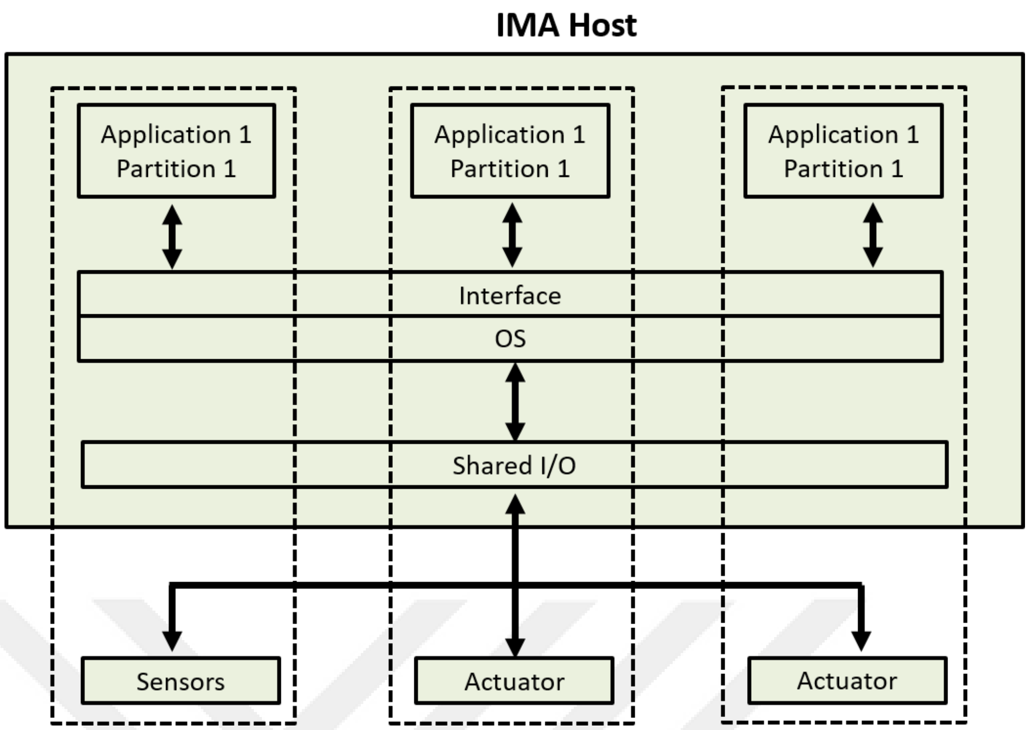

Figure 1.2 Integrated modular avionics architecture [5]

and MIL-STD 1553 are deterministic, they are insufficient to meet new generation applications' high data rate requirements. Since there is no Ethernet protocol (IEEE 802.3) regulation that supports high data rates, the latency and jitter values are unpredictable in congestion situations.

The ARINC-664 protocol, which is developed as a profile of the IEEE 802.3 standard, allocates bandwidth between applications according to a predetermined network schedule. The ARINC-664 network, widely used in modern avionics systems, defines a deterministic high-speed network structure. ARINC-664 Part 7 is the standard for this technology. This standards' goal is to create a deterministic network by ensuring foreseeable delay and jitter [6]. A centralized switch including a star topology and switchless point-to-point structure within network topology can be used to implement an ARINC-664 deterministic communication network. Each node in the switchless design could contain many terminals. In the conventional ARINC-664 solution, ES and SW elements are separated to provide high-speed communications between network elements. Thanks to the shortage of physical switches in the switchless ARINC-664 topology developed by shifting the switch structure to ES, there is a reduction in SWaP. In addition, switchless architecture can potentially improve latency performance due to its inherent load balancing feature. Note that in the switchless architecture, when the number of ports for each ES is higher than two, in comparison to a star topology, a mesh network architecture offers higher availability and robustness in the case of link failure. Adaptive router could be used in a mesh topology to reduce network interference, packet loss, and latency by dynamically rerouting communications across other channels. To meet the needs of deterministic high-speed networks, either static or dynamic routing can be used. Switchless ARINC-664 network topologies have been gaining attention in the literature [7]. In this thesis, we study switchless ARINC-664 network topology as a promising approach for IMA architectures since it provides a significant advantage in terms of SWaP and delay bounds.

1.2 Objective of the Thesis

In this thesis, three different avionics networks architectures, including star, ring, and mesh topologies, are studied, and their delay performances are reported using the Network Calculus tool. While traditionally, the star network topology is constructed using ARINC-664, mesh network topologies have gained significant attention due to their SWaP advantages. This thesis aims to compare and contrast the delay and jitter performances of switchless ARINC-664 network topology against conventional ARINC-664 star topology, and ring network.

1.3 Hypothesis

In this thesis, the delay analysis of switchless ARINC 644 topologies, ring network, and the reference star network topology is performed by using Network Calculus. As the number of ES ports increases, the number of possible routes of VLs also increases. These VL routes in any combination must be taken into consideration in the respective network topology to determine the lowest delay bounds. There are many different routes to choose from configurations in network topologies. Therefore, we use GA based on route optimization for switchless ARINC-664 network topologies. 10 ESs and 11 VLs are used for both scenarios. In the switchless topology, the worst-case latency analysis is calculated using GA based network calculus approach by changing the number of ports in an ES. The numerical results indicate that mean and the maximum worst-case delay values of all VLs are always smaller in the switchless ARINC-664 topology. It is observed that the mean and maximum delay values decrease with the increase in the number of ports in the ES.

2
OVERVIEW OF AVIONICS NETWORKS

The technological development of avionics networks is briefly discussed in this chapter. With the advent of the fly-by-wire notion, the widespread use of information exchange in avionics systems led to the definition of safety-critical communication protocols. Avionics networks have gained interest due to the increasing demand for higher reliability, security, and performance associated with communications in avionics systems [6]. Modern avionics flight control systems are designed with digital interfaces that allow components of an avionics system can be interconnected. For example, flight control and central control computers are connected to sensors and actuators using point-to-point connections. Two of the most common avionics data bus standards are ARINC 429 for commercial aircraft and MIL-STD -1553B for military aircraft. The broadcast communication standard can be used instead of a point-to-point architecture to achieve high data rates and reduce SWaP for aircraft. As an example, the avionics systems on the C130J military transport aircraft, which previously used separate cabling, were converted to the bidirectional bus MIL-STD -1553B. This upgrade resulted in significant weight savings. However, the use of the bus has become more complex. In addition, improved versions of these standards have been developed to satisfy the performance requirements of modern avionics systems [4]. Reliable buses developed for the automotive industry, such as CAN(Controller Area Network) and Time-Triggered Protocol, are adapted to avionics equipment used in the aviation industry. There is an increasing need for data networks in aircraft, driven by the increasing amount of information flowing through inter-system communication and general-purpose operating systems. Avionics data transmission systems have evolved into information-centric networks. As a result of these developments, high-speed, reliable, and low-cost networks have been required. Therefore, there is a tendency to use COTS networking technologies in aerospace equipment. The high-speed IEEE802.3 standard, which has received considerable interest in the aerospace industry [5]. However, the Ethernet standard is not directly used in aviation due to the inherent non-determinism. Therefore, it is mandatory that the Ethernet standard is extended to meet the requirements of the aviation industry. In this framework, the AFDX protocol was created and is utilized in the Airbus A380, as well as the A350 and B787 [6]. TTEthernet is an IEEE 802.3 Ethernet-based variant of such protocols that defines time-triggered services for Ethernet networks as a quality of service enhancement, with fault-tolerant time synchronization.

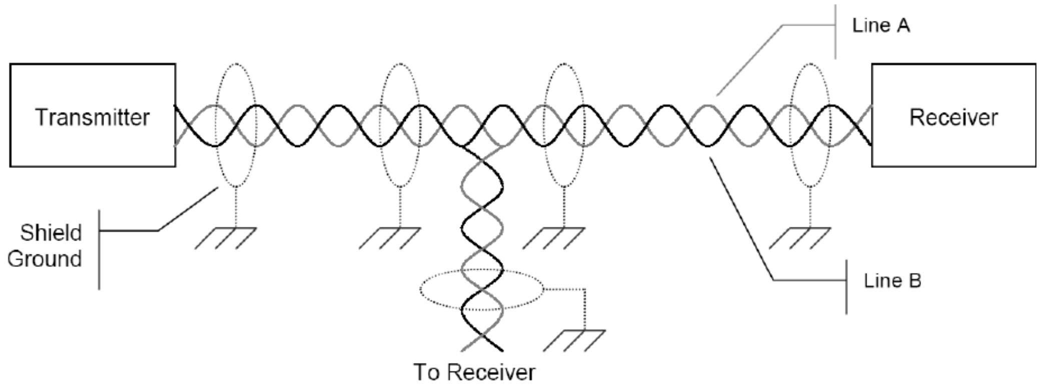

Figure 2.1 ARINC 429 cabling [4]

2.1 ARINC 429

ARINC 429 is one of the most widely used data exchange protocols for commercial and military aircraft, developed in 1988. The ARINC 429 specification defines standard requirements for digital data transmission between aircraft avionics systems. ARINC 429 specifications include a constant packet size, dedicated point-to-point connections, and a fixed transmission rate. The ARINC 429 specification was designed to assure the interoperability of LRU-based sensors and devices [8]. The first problem with the ARINC 429 specification is the physical layer properties. A twisted 78-ohm shielded cable is used to connect the nodes. The shields have to be grounded at both ends and each junction, as shown in Figure 2.1. A only one transmitter and approximately 20 receivers are connected by a twisted couple of wires. Communication between the nodes is unidirectional; while the transmitter is talking, the receiver is not relaying information for data exchange. A device may include many transmitters and receivers to communicate with components via separate buses. Therefore, fault isolation is provided at each transmitter/receiver to ensure that faults in one transmitter/receiver do not cause faults in a variety of different transmitters/receivers. As a result, fault-tolerant communication mechanism is achieved by using this architecture.

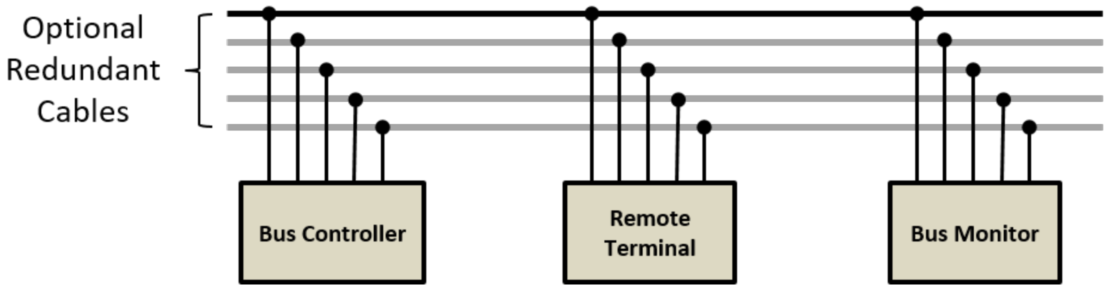

Figure 2.2 MIL-STD-1553

2.2 MIL-STD-1553

MIL-STD -1553 is a military standard that defines the characteristics of the bus implemented in military and aerospace platforms. It is also known as the Digital Time Division Response/Command Multiplexed Bus. MIL-STD -1553 was designed for military aircraft, but it is also widely used in civil aviation and other sectors are like railway systems. Just like ARINC 429, the transfer bit rate of the MIL-STD -1553 frame is defined at 1 Mbps and has a constant configuration. As shown in Figure 2.2, the MIL-STD-1553 standard provides three types of terminals that are connected to the interface. These terminals are bus monitor, remote terminal, and bus controller [9]. The Bus Controller commences all transfers on the bus, and data exchange is accomplished under command mode. There can be more than one bus controller on the same bus, but one is enabled at any time. Depending on its response, it sends a command to one or more remote terminals. The remote terminal connects sensors and subsystems on the data bus MIL-STD -1553. It can be installed on subsystems and independent devices. There are 31 remote terminals on the data bus, and each one of the remote terminals can communicate with other terminals. Bus Monitor is a device that listens to the data on the bus, and its primary function is to detect system errors and troubleshoot.

2.3 TTEthernet

TTEthernet implements time-triggered communication mechanisms to offer a deterministic communication service over Ethernet. It can execute deterministic communication using mature fault tolerance and real-time mechanisms of time-triggered technology based on Ethernet standards. These time-triggered mechanisms establish and maintain a global time that establishes a globally uniform clock in the network system. TTEthernet divides the various traffic streams into three classes: time-triggered, rate-constrained, and best-effort traffic to support mixed-criticality applications on a single network. The three traffic classes are adopted to the standard Ethernet frame format, and types are created for these classes. The type field of the TT frame is 0×88d7, that of the RC frame is 0×0888, and that of the BE frame is 0×0800.

The TT traffic is sent and routed at defined points in time and therefore has highly deterministic timing characteristics and minimal jitter. The path and timing of each frame are determined by the programs configured in the transmitter and switch the channel. Therefore, each end system has a transmit schedule, and each switch has a receive and transmit schedule. The switch accepts frames from the transmitter only if they are received within a certain time window (i.e., if they comply with the reception schedule). Otherwise, they are discarded. It is suitable for communication applications with low jitter and deterministic delay [10].

Rate Constrainted similarly to ARINC-664, traffic is delivered with low latency and jitter, and each TTEthernet transmitting node is assigned a particular capacity. When determinism and real-time requirements are less rigorous than for time-triggered communication, RC messages are utilized.

Best-Effort messages implement the conventional switched Ethernet approach. There is no guarantee as to whether or when these messages will be sent. The remaining network bandwidth is utilized by BE messages, and these have a lower priority than other message types.

2.3.1 TTEthernet Clock Synchronization Service

Time-triggered solutions enhance the development of mixed-criticality distributed systems. TTEthernet is a synchronized protocol that performs timing along with the system. Global timing issue must be maintained for TTEthernet networks. The Protocol Control Frame is used by TTEthernet as the synchronized message.

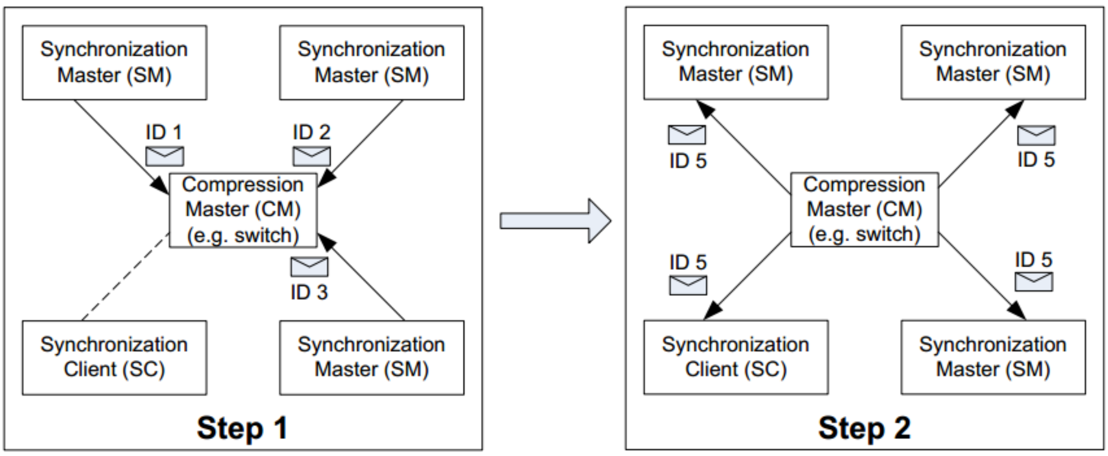

Figure 2.3 Two-step synchronization approach [11]

Two-step synchronization is achieved by TTEthernet, as depicted in Figure 2.3. The TTEthernet protocol consists of three components, namely the synchronization master, the synchronization client, and the compression master, to achieve synchronization [11]. To initiate, all of the SMs in the network transmit a protocol control frame to the CM. Then, the compression masters compute a configurable average or median value based on the arrival times of these protocol control frames. Then, the newly calculated protocol control frames (PCF) are sent to SCs and SMs. Depending on the system architecture, the devices in the network are SC, CM, and SM. The ES can be configured as SC, CM, or SM; also, SW can be configured in this way. In the TTEthernet network, a redundancy mechanism is used to increase the fault tolerance capacity [12].

2.4 Time Sensitive Network

TSN presents a set of IEEE standards to facilitate time-critical network communication. TSN provides real-time communication with network latency and jitter that are deterministically bounded. TSN standards are utilized as an open standard in the industrial, automotive, and audio-video bridge industries. TSN employs distributed device scheduling to enable deterministic communication. TSN defines a timing technique for controlling access to outgoing queues at switch ports by triggering switches over time. Other scheduling techniques, such as credit-based shapers and priority queuing, can be implemented across the network in addition to time-triggered scheduling [13].

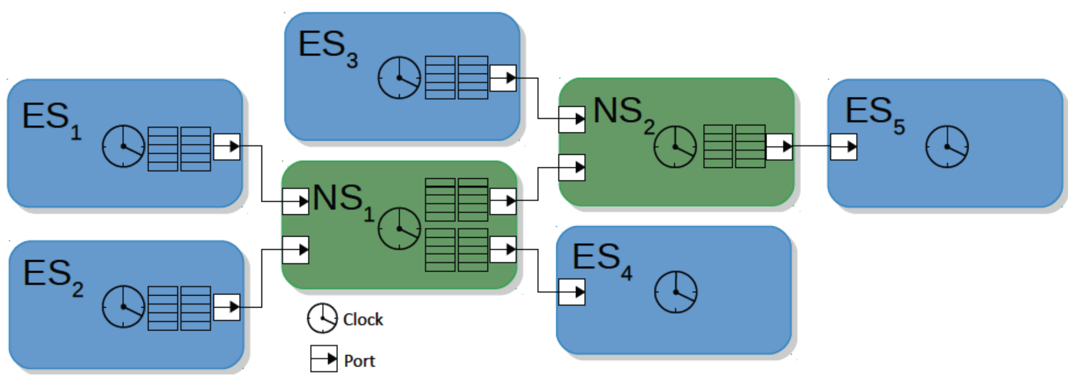

Figure 2.4 TSN network architecture example [14]

The network includes network switches and end systems. End systems can only receive and send data; they can not relay data. On the other hand, network switches do not consume, create, or process data; they only relay it. The output port is used to connect to other nodes. Therefore, there can be more than one output port for each node in the network. Send and receive ports can be different from each other. The insertion of a clock inside the node is one of the most essential characteristics of TSN. It is used to synchronize the gate times between the nodes. General topology is shown in Figure 2.4. The other nodes should receive all data which are sent. This eliminates the prioritization that must be implemented in the output port [14]. In addition, TSN provides robustness and reliability with a seamless redundancy and frame avoidance mechanism that provides the ability to interrupt frames that are already in transmission.

Furthermore, TSN eliminates the requirement for critical and non-critical networks to be physically separated. There can be different traffic classes on the network without delay and jitter. One can add new data streams to the network without distorting existing traffic and without the need to reconfigure all networks. Consequently, this situation leads to creating a complex network structure transporting both time-critical and non-critical traffic in one network [15].

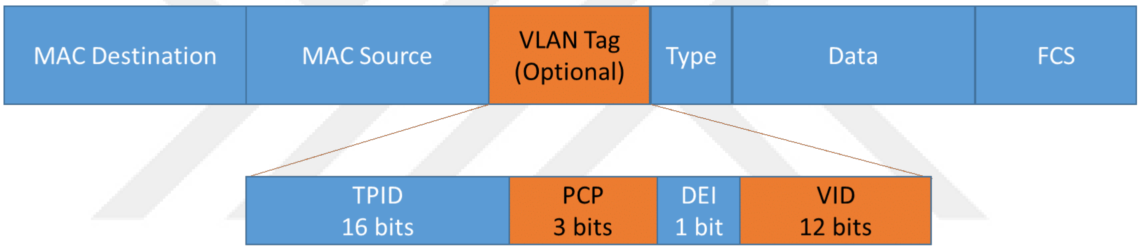

Figure 2.5 TSN frame

2.4.1 Time Sensitive Network Flow

The TSN stream is identified by the Priority Code Point (PCP) field and the Virtual Local Area Network (VLAN) ID (VID) in the 802.1Q VLAN tag in the Ethernet header. The structure of the TSN frame is shown in Figure 2.5. The Tag Protocol Identifier (TPID) is a fixed 16-bit value defined by the standard. This indicates to the switch that this frame is a VLAN tag and that the switch needs to read further to find the Ether Type field. Priority Code Point (PCP) is a 3-bit value indicating the frame's priority, ranging from 0 to 7, with 0 as the lowest priority. Input mechanisms use the Drop Proper Indicator (DEI) bit in switches to flag frames that violate configuration constraints. VLAN Identifier (VID) is a 12-bit identifier for a VLAN [15].

2.4.2 Time Synchronization

Timing and synchronization are crucial in order to achieve deterministic communication within TSN. IEEE 802.1 AS is a profile of the IEEE 1588 Precision Time

Protocol. The clock synchronization allows network devices to operate consistently and perform critical operations at a given time. This standard defines the protocol and procedures which are used to synchronization requirements are met for time-sensitive applications. The Best Master algorithm is employed to find a grandmaster device for time synchronization. Then the Generalized Precision Time Protocol, which uses the PDelay mechanism, is used for two-way time transaction [16].

2.4.3 Traffic Scheduling

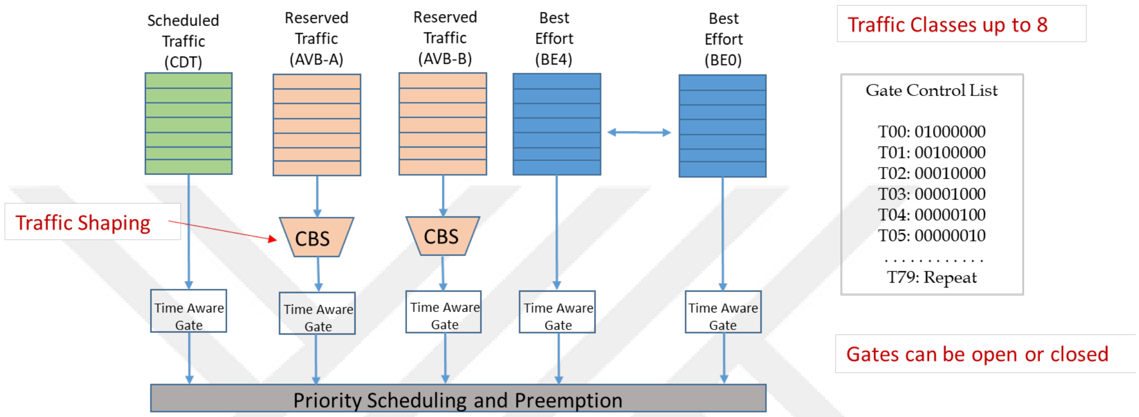

Figure 2.6 TSN gating mechanism [17]

The aim of scheduling and traffic shaping is to allow different traffic classes to coexist in the same network. These traffic classes have different priorities, bandwidths, and end-to-end delays. Scheduling is the main concept of TSN in order to avoid interfering traffic. Time scheduling of TSN defines time-dependent queue-draining procedures. The schedule is created and distributed among the participating network devices according to the shared global time. Time-gated egress queues transmit one at a time based on a precise time slot schedule and directly time the release of packets to avoid congestion and provide a deterministic delay. VLAN tag-encoded priority values are allocated to allow simultaneous support of scheduled traffic, credit-based traffic shaping, and other bridged traffic over Local Area Networks (LANs). Networks which are employed scheduled transmissions can check out real-time processes. Figure 2.6 depicts the TSN time-aware gating mechanism, were at a time within the time interval "T00", the second gate program entry is applied, i.e., the gate (AVB-A) is open only for reserved traffic. In addition, the traffic of queues 2 and 3 is shaped using the credit-based shaper. IEEE802.1Q specifies eight different types of traffic that can be useful for traffic classification according to QoS requirements, as shown in Table 2.1. The default traffic is considered Best Effort traffic. Also, the default PCP is 0, which represents Best Effort traffic.

Table 2.1 Traffic classes

PCP	Priority	Traffic Class
1	0(lowest)	Background
0(default)	1	Best Effort
2	2	Excellent Effort
3	3	Critical Application
4	4	"Video"<100 ms latency and jitter
5	5	"Voice"<10 ms latency and jitter
6	6	Internetwork control
7	7(Highest)	Control Data Traffic

2.5 ARINC-664

New-generation aircraft require high data rates and reliable communication due to the aircraft's increasing number of integrated functions. These aircraft requirements cannot be met by other types of networks such as ARINC 429, ARINC 825. Due to the limitations in protocols, system integrators felt the need to develop a new aircraft data network. Avionics Full Duplex Switched Ethernet technology was developed by Airbus for the A350, A380, and A400M aircraft and is standardized in ARINC-664 Part 7, a constrained and profiled version of the IEEE 802.3 network. ARINC-664 Aircraft Data Network specifies the electrical characteristics and protocol recommended for avionics. AFDX is a full-duplex Ethernet-based deterministic switched network protocol which provides redundant communication. Furthermore, the reliability of this network is achieved by applying a redundant comumunication mechanism. The full-duplex communication used in AFDX avoids collisions and tighter deterministic timing performance. These properties enable AFDX to offer reliable network communication, guaranteed QoS, high performance, and determinism [18].

2.5.1 End System

The logical unit is connected to the physical AFDX network via AFDX ES, which is part of an avionics system or avionics subsystem. ES performs a variety of duties in the AFDX networks, including transmitting and receiving frames. Another critical role of ES is to provide guaranteed services and secure data exchange among avionics applications. Each ES in this network is connected to the redundant switches, as shown in Figure 2.7. The switch connections are configured in a cascaded star architecture for network scalability. The switch is considered to be capable of parallel processing. As a consequence, packets routed to different switch output ports do not interfere with each other [19].

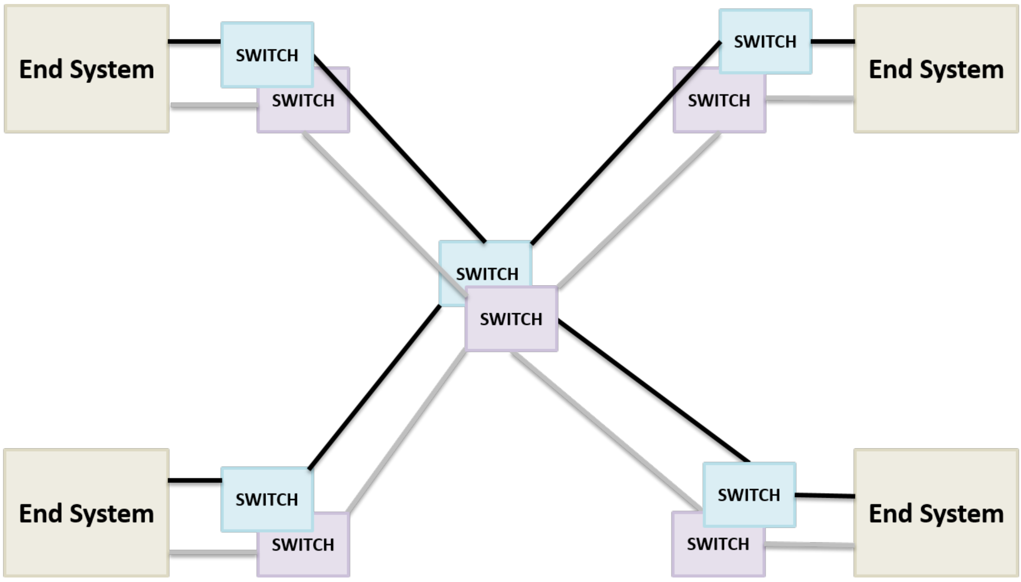

Figure 2.7 Sample AFDX network

2.5.2 Concept of Virtual Link

The concept of VL comes from the ARINC 429 protocol. AFDX achieves deterministic communication using the VL concept, which specifies a logical, unidirectional connection from a source ES to one or more destination ESs. Each VL has an unique 16-bit Virtual Link Identifier (VL ID) whose value varies from 0 to 65535. The routing of VL is defined statically to offer a guaranteed performance.

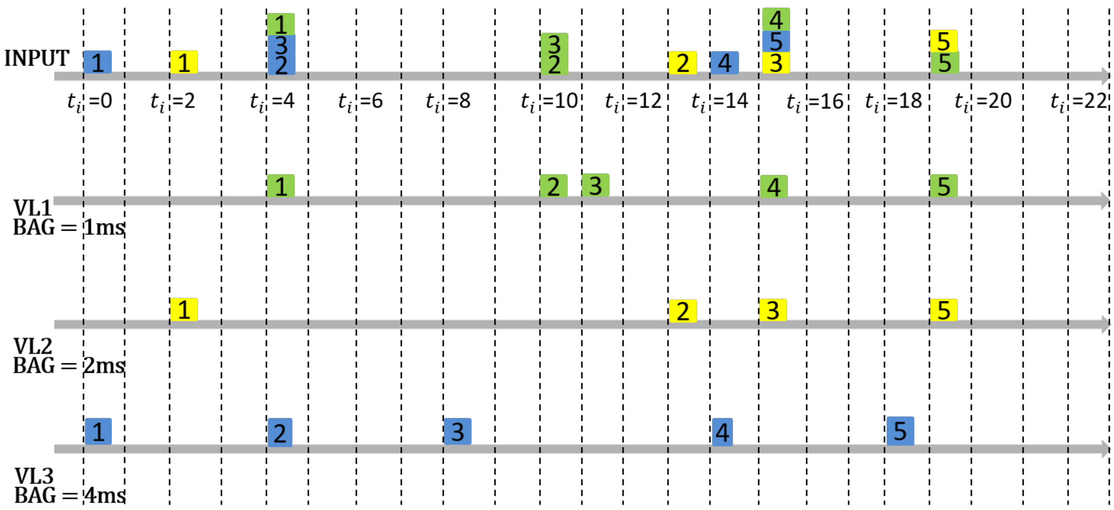

Figure 2.8 Regulation of VL flow

The maximum allowed bandwidth of each VL is determined by two parameters namely, maximum frame size, and bandwidth allocation gap (BAG). The maximum frame size should be between 64 bytes and 1518 bytes. The BAG specifies the minimum amount of time between the start bits of two consecutive frames required to ensure that the bandwidth usage of a VL never exceeds its allocated bandwidth. According to the

AFDX standard, the valid range for the values is from 1 to 128 ms in powers of 2. The regulation mechanism is used as shown in Figure 2.8 to ensure that the BAG is maintained for each VL in the source ESs. The regulator regulates the related VL with respect to the BAG. Therefore, the periodic or non-periodic frame input is arranged according to the predefined configuration [20].

2.5.3 The Virtual Link Frame Structure

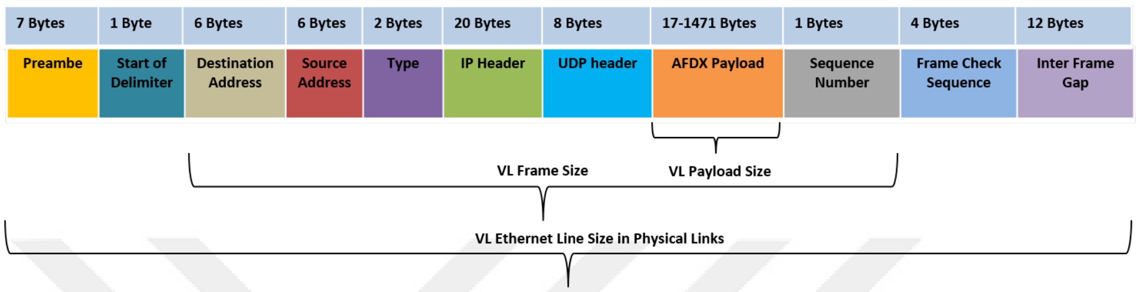

Figure 2.9 AFDX frame structure

VLs are used to transfer frames within AFDX networks. Each VL consists of a 6-byte MAC destination address, 6-byte MAC source address, a 2-byte type field, AFDX payload whose length is between 17 and 1471 bytes, 20-byte IP header, 8-byte UDP header, and 1-byte sequence number, as shown in Figure 2.9. The MAC destination address is used for routing VL within switches. Since the VL identification is inserted in the MAC destination address, the end system and switch employ VL, a predetermined configuration table. The MAC source address of the AFDX frame must comply with IEEE 802.3, and this address determines which network path the AFDX frame to which it belongs should follow. The type field is a consistent value, which is 0x0800 for AFDX. The IP header is defined to specify the information used for multicast or multicast transmission. The IP header should comply with the IPv4 format since IPv4 is used in AFDX. The total length of AFDX is excluded from the sequence number. Padding bytes are appended if the AFDX payload is less than 17 bytes. The sequence number is added by the AFDX network and used for integer checking and redundancy management mechanism. The Frame Check Sequence field is controlled by SW to ensure the validity of the frame. Seven bytes of Preamble, 1 byte of Start of Delimiter, 4 bytes of Frame Check Sequence, and 12 bytes of Inter Frame Gap are added to the frames during transmission over the physical links [21].

2.5.4 Transmitting and Receiving Function of End Sytem

The structure of a transmitting ES is shown in Figure 2.10, which includes a traffic regulator per VL, a VL scheduler, and a redundancy manager. Each regulator module

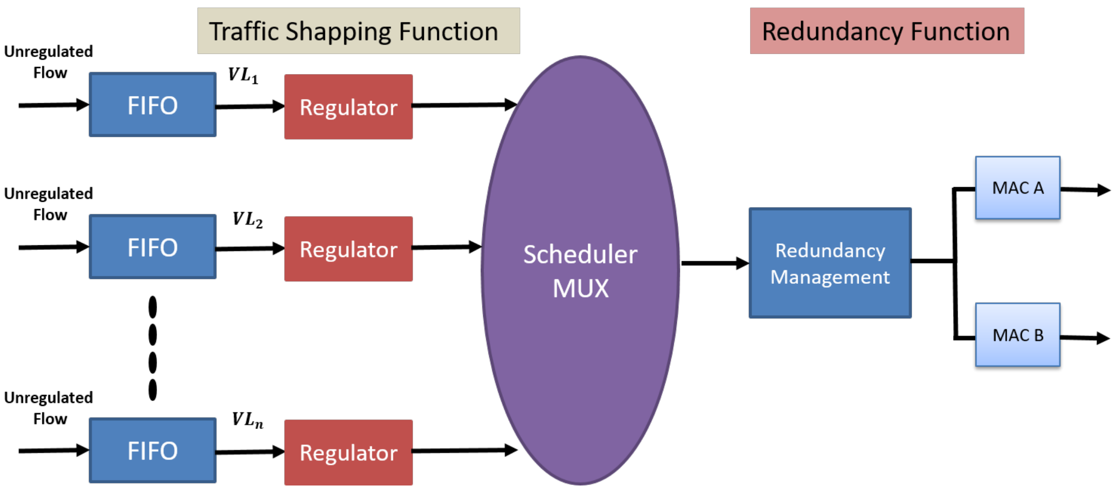

Figure 2.10 AFDX transmitting ES

shapes the corresponding VL traffic to limit the frame rate of the VL using its BAG value. The VL scheduler multiplexes the several VL streams coming from the regulators and sends the selected frame to redundancy management. The Redundancy management module for network forwarding. The VL scheduler can specify a certain amount of deviation, limited to a maximum value, so frames can appear at the scheduler's output within a time window defined by this deviation. The frame from the VL scheduler assigns a sequence number to each copy depending on VL, ranging from 0 to 255, and passes each copy to the appropriate MAC interface for transmission to the network layer through the PHY. The receiving ES can detect redundant copies of the same frame using this approach. For each subsequent frame, one VL increases the sequence number. The sequence number is rolled back to 1 in the following frame after reaching 255 in the previous transmitted frame. Upon reset or initialization of the transmitter ES, it is set to 0 in the next frame. The redundancy management module can also forward non-redundant VLs whose frames are forwarded over only one of the same networks, not both [22].

$$J_{max} \leq 40\mu s + \frac{\sum_{i=1}^{N}(20 + L_{max}) \times 8}{BW} \tag{2.1}$$

$$J_{max} \leq 500\mu s \tag{2.2}$$

The maximum jitter allowed for any VL at the output of an ES, i.e., J_{max}, is bounded by the upper limits given in the equations 2.1 and 2.2 and N (total number of VLs originating from ES), $Lmax$ (in bytes), and BW (MAC in bits per second) physical bandwidth capacity of the interface). The 20-byte total term in the numerator and the time duration of 40 μs indicate the minimum technological jitter and Ethernet overhead from the interframe gap (IFG), preamble, and start of frame limiter (SFD). The change in the delay is required to process one frame when ES is not processing another frame. Equation 2.2 defines a strict limit for outgoing traffic, i.e., the upper limit specified by Equation 2.1 should never exceed 500 μs. This limit was chosen to be half of the minimum BAG, i.e., 1 ms, to avoid possible traffic bursts in the network. It is the responsibility of the network designer to ensure that the ES configuration and ES implementation never cause jitter in excess of 500 μs [6].

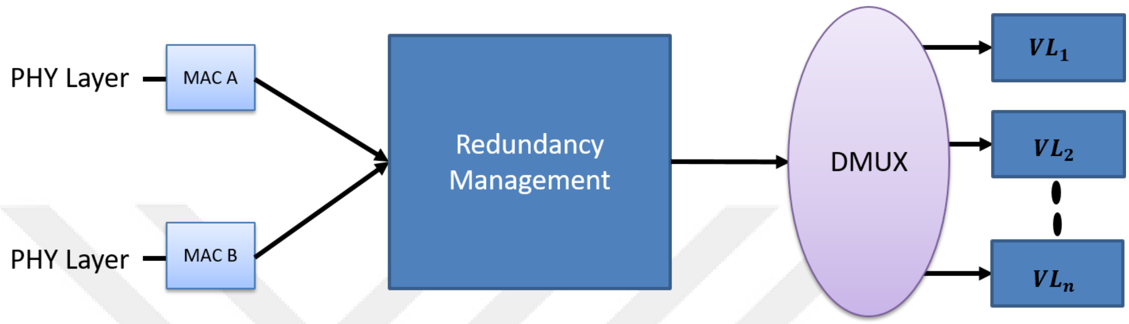

Figure 2.11 AFDX receiving ES

The receive side of the redundancy management module is responsible for the primary functionality of a receiver ES, as shown in Figure 2.11. This module detects and eliminates invalid and unnecessary frames. The elimination of invalid frames, i.e., integrity check, is performed based on sequence numbers if the sequence number of the currently received frame does not fit into the range [PSN+1, PSN+2], where PSN indicates the previous received sequence number. The frame that was previous received has been categorized as invalid. To eliminate redundant frames, sequence numbers and the tunable parameter SkewMax are employed. A frame is classified as redundant if it is received from one of the redundant networks within a SkewMax time after another frame with the same sequence number is received from the other network. Otherwise, it is defined as a new frame and allowed to pass through the upper protocol layers by parsing (DMUX) the incoming frames into their corresponding VLs (DMUX) [23].

2.5.5 Switch

The AFDX switch is the primary network element, connecting the ES to other ES. The functional blocks of an AFDX switch, such as traffic filtering, traffic monitoring, and switching, influence its capacity to transfer data and, as a result, have a direct impact on end-to-end latency in an AFDX network. It performs the configuration and monitoring, configuration, and network management tasks that are the other functional blocks of the switch. The data forwarding channel for incoming traffic is

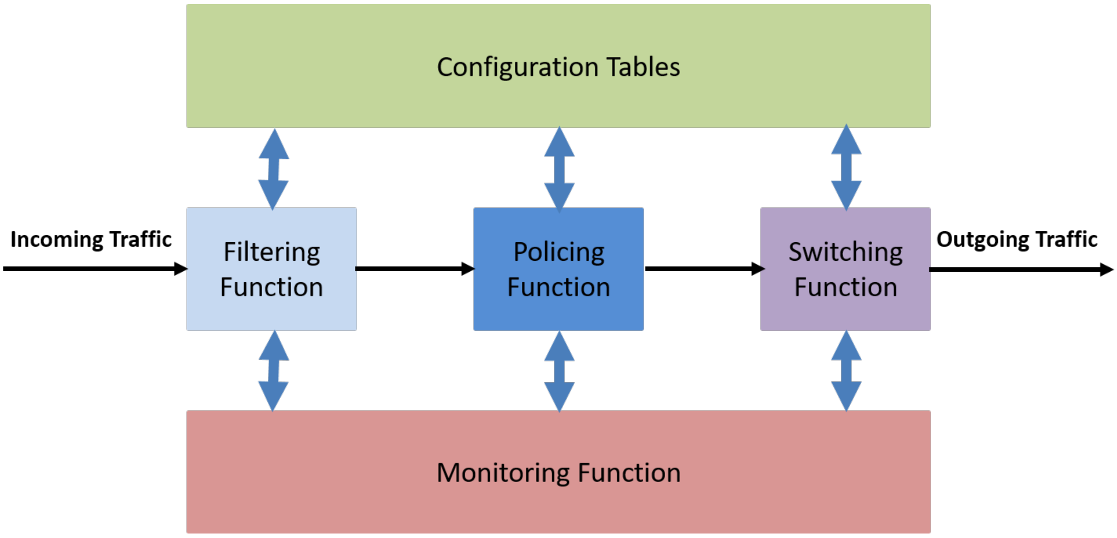

Figure 2.12 Functional blocks of AFDX switch

shown in Figure 2.12. Parameters including BAG, J_{switch}, S_{max}, and S_{min}, which must be specified on a VL basis within the switch, are required for the filtering and monitoring functionalities to work. The J_{switch} represents the time window during which a frame arriving at a switch port is guaranteed. Each incoming frame is assessed for size and integrity, the destination address and port are verified, and the frame is discarded if the network configuration is violated. The policing function guarantees that each VL's assigned bandwidth is used by discarding any VL packets that are incompatible with the BAG configuration.

$$S_{max} \times \frac{1 + J_{switch}}{BAG} \tag{2.3}$$

While the AFDX standard allows policing for multiple VL, policing is performed based on VL in an avionics platform. There are two forms of policing available in an AFDX switch: byte-based and frame-based. Byte-based and frame-based policing discards VL frames if the VL bandwidth in bits or frames per second violates the network configuration. The policing mechanism maintains an account for each VL with the maximum credit specified in equation 2.3. It transmits a VL frame as long as the account in question has sufficient credit or discards the frame otherwise. The J_{switch} in equation 2.3 should be configured to match the maximum possible jitter value for incoming traffic, which must be determined by theoretical analysis or simulation. Any inconsistency between the actual and configured values of J_{switch} may result in unexpected packet loss, which may not be tolerated in deterministic communication. Whether byte-based or frame-based checking is employed, each arriving frame updates a VL account balance in a different way [22].

2.6 Avionics Network Topologies

Communication occurs between network nodes using a switch-centered star or a switchless mesh or ring topology in IMA systems. Switching functions are performed by a high-performance processing unit with high-speed communication interfaces while communicating through a central switch. In the case of the ring topology, each node should be connected with at least two other nodes, and in the case of the mesh topology, each node should be connected with at least three other nodes. Alternative IMA topologies for deterministic communication are briefly described in this section [24].

2.6.1 Star

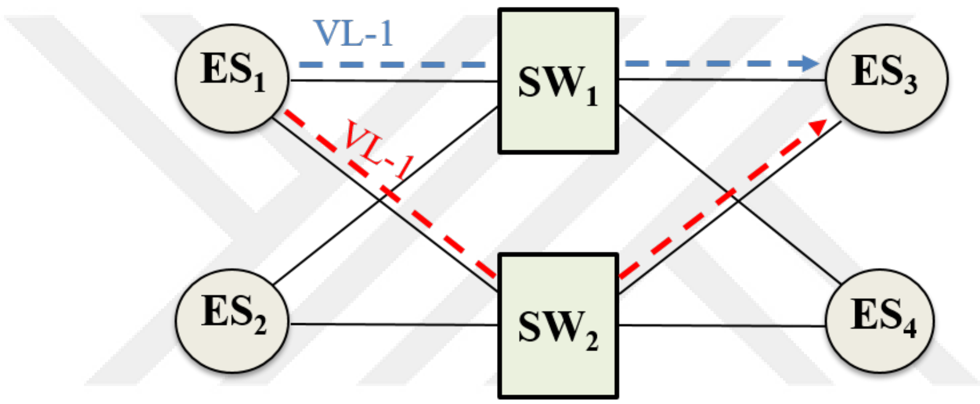

Figure 2.13 Star network topology

Figure 2.13 illustrates a star topology in which communication between modules is handled by a central switch. Each ES node is connected to two switches via a deterministic peer-to-peer network interface. The primary switch is Switch A, while the secondary switch is Switch B, which is utilized for redundancy management. A dedicated VL can be constructed between any two communicating nodes because each ES has a physical communication path through the primary switch. The amount of traffic injected by each node is managed by a flow control system running on each VL, and traffic that exceeds average and peak rates is shaped [25]. Since the entire communication center runs via the switch, one technological difficulty is facilitating the exchange of enormous amounts of deterministic data over the switch. When dealing with time-critical traffic that demands a specified flow rate and quality of service criteria like low latency and jitter, things get a little more challenging. The switch must be deterministic and meet timing and policy constraints [26]. This network topology is highly suited to enable avionics system communications in the context of Integrated Modular Avionics (IMA), either through basic data flow or virtual link management and separation. The star topology has the advantage of providing the shortest path between nodes when compared to ring and network topologies, which increases data communication possibilities. New nodes can be placed with minimum configuration, and existing nodes can be eliminated without impacting the rest of the network. In the event of a failure, the network may rapidly reorganize its responsibilities in a planned manner, allowing traffic to be redirected from the main link to the redundant link via the redundant switch. The star topology's main drawback is its technological reliance on the central switch, which must be capable of switching large amounts of deterministic traffic. Another disadvantage is the SWaP, in which switching operations occupy two slots and increase the system's total weight. Another difficulty is scalability since the switch gets more complicated and costly as the number of modules rises. The number of nodes that may be placed is limited by the capacity of the switch [27].

2.6.2 Mesh

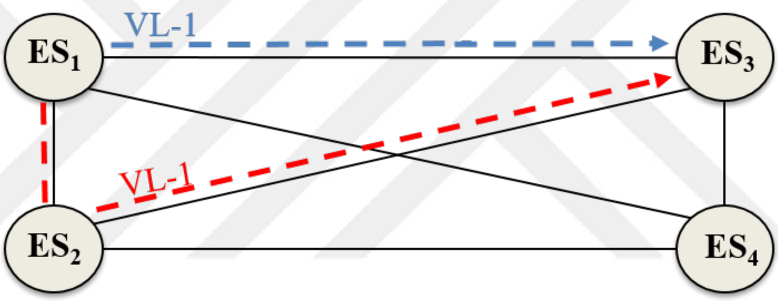

Figure 2.14 Mesh network topology

The concept of integrated modular avionics in next-generation avionics systems aims to share hardware and software components among different applications. Compared to federated systems using application-specific devices, the IMA concept offers significant advantages in terms of Size, Weight, and Power (SWaP). The ARINC-664 solution, which separates the ES and SW units, is utilized in IMA systems to address the need for high-speed communications between nodes. In the mesh network topology constructed by transferring the SW structure to ES, the SWaP is expected to be reduced by eliminating the physical switches, and the latency performance is improved by load balancing. The mesh network topology, which eliminates the switch, is a promising alternative to interconnect the modules in the networks. As illustrated in Figure 5.2, each module in this network architecture has at least three interfaces to create a mesh network topology. In comparison to star and ring topologies, mesh network topologies give better robustness and redundancy mechanisms. The mesh topology enables ESs, whose forwarding capabilities are limited, to communicate with other ESs throughout the network by using the relaying concept. QoS methods can be used to provide traffic with lower latency a higher priority. The amount of Ethernet traffic can be controlled via a flow control mechanism [28].

2.6.3 Ring

All nodes in the in-ring topology are connected to form a closed network. The modules are interconnected by a ring topology as shown in Figure 5.3. Each node is connected to the network through its two adjacent nodes. Thus, data will be exchanged between remote modules through a ring network with relay functionality. Central switching modules connected to other modules are not needed. A redundant ring is used to establish fault tolerance by transmitting the frames through alternative path. The destination ES takes the packet from both primary and redundant paths and always drops the redundant one in normal operation. If the primary ring encounters an error, the duplicated packet is received instead. The VL concept may be used to segregate data flow between pairs of network nodes while still satisfying speed, latency, and jitter requirements. Before data communication starts, bandwidth resources are assigned utilizing resource reservation protocol. The quantity of traffic injected by each node is managed thanks to a traffic shaping system. Only if resources are available after other flows have fulfilled the QoS requirements is traffic exceeding average and peak rates accepted. Since each ring network has its communication path, the ring architecture includes natural support for redundancy.

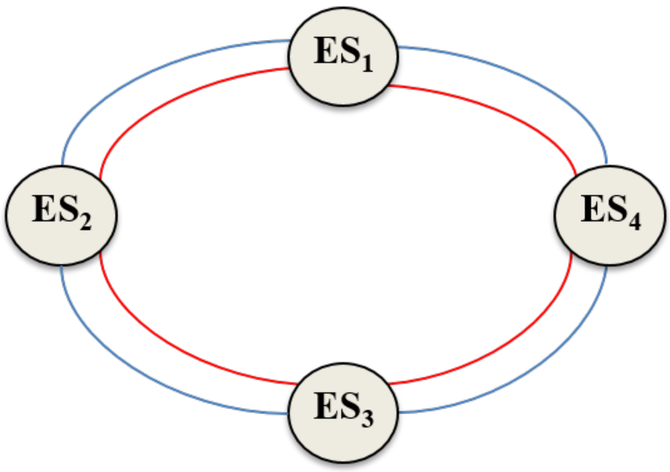

Figure 2.15 Ring network topology

On the other hand, ring network topologies have longer routing paths than start and mesh topologies, resulting in lower bandwidth capacity if the number of communication paths are same. When the same number of physical interfaces are used. Data transmission on the network will continue to flow even if a link fails but across more extended channels. A successive connection failure on the redundant ring will bring the entire network to a deadlock [29].

3
DELAY ANALYSIS USING NETWORK CALCULUS

Real-time communication performance is a vital issue for avionics networks inside aircraft. Therefore, the upper bound of the delay, which is transmitted packets, is needed for the certification process. It performs a critical function in assessing whether or not real-time necessities are being met [30]. The worst-case delay bound on the network is measured by using the Network Calculus (NC) approach. In this section, the NC, which will be utilized for overall performance evaluation and design optimization, is overviewed [31].

3.1 Network Calculus for ARINC-664

NC theory is a queuing system that first appeared in the 1990s and is presently the most widely used as a network performance tool for the research in time-critical applications. NC provides in-depth analysis of streaming issues in networking. The mathematical theory of Min-Plus algebra is the foundation of NC. Using the NC, we can analyze integrated service networks, flow control, scheduling, and delay [32].

3.1.1 The Concept of Arrival and Service Curve

The input and output flows of the network nodes are modeled by using two main concepts in NC; the arrival curve and the service curve.

The arrival curve is a technique for limiting the amount of data emitted by sources. $\alpha(t)$ be a wide-sense increasing function which is for $t \geq 0$. The flow $R(t)$ is bounded by $\alpha(t)$ only if $s \leqslant t$.

$$R(t) - R(s) \leqslant \alpha(t-s), \tag{3.1}$$

where $\alpha(t)$ denote the arrival curve.

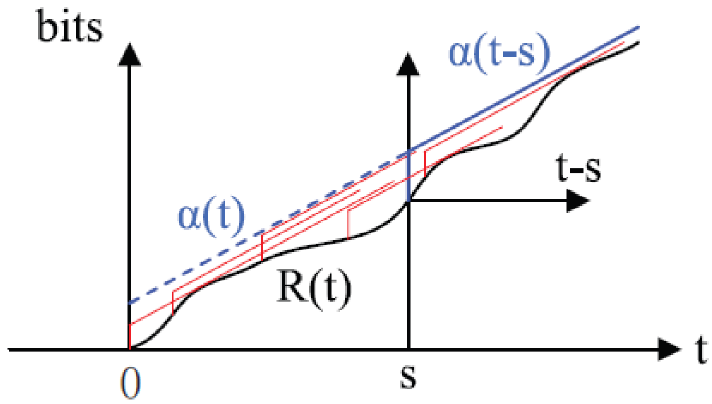

Figure 3.1 An example representation of the arrival curve [6]

Figure 3.1 provides an example of arrival curve where $\alpha(t)$ can be described as the upper bound of bit accumulation of $R(t)$ in any given time interval. As seen in this figure, there are many sets of curves which are met this equation. The aim is to find the tightest one that describe the best traffic characteristic among all the arrival curves. The affine and staircase are arrival curves that are the most used in the network performance analysis for NC approach [33]. The AFDX standard proposes affine arrival curve for VL traffic model. Therefore, we will use the affine arrival curve to analyze our system model. In this study, bandwidth allocation gap, maximum packet size and flow are the parameters used for n^{th} VL data traffic generated in ES, BAG_n, L_n and f_n, respectively. The leaky-bucket method is used by the traffic regulator function in the ES to regulate traffic flows. Therefore, there is no congestion situation that is sent flows by ES, and we need to calculate the equation of SW for congestion cases. When n^{th} VL data traffic generated in ESs is expressed by f_n, the time (t) dependent arrival curve for f_n at input SW can be expressed as equation 3.2:

$$\alpha_n(t) = \begin{cases} \alpha_n(t) = r_n t + s_n, & t > 0 \\ 0, otherwise \end{cases} \tag{3.2}$$

The burst of the n^{th} flow are expressed by $s_n = L_{max,n} + 160$ and rate of the n^{th} flow is given by equation 3.3.

$$r_n = \frac{s_n}{BAG_n} \tag{3.3}$$

For $t \geq 0$ where $\beta(0) = 0$, $\beta(t)$ be a wide-sense increasing function. The input and output functions are present in the flow that passes through a system $R(t)$ and $R^*(t)$, respectively. Therefore, $\beta(t)$ can be described as the service curve provided by the model only if $s \leqslant t$.

$$R^{*}(t) \geqslant inf[R(s)+\beta(t-s)], \quad 0 \leq s \leq t \tag{3.4}$$

Furthermore, the 3.4 Equation may be expressed using the min-plus convolution operator ($\bigotimes$).

$$R^{*}(t) \geqslant [R \otimes \beta](t) \tag{3.5}$$

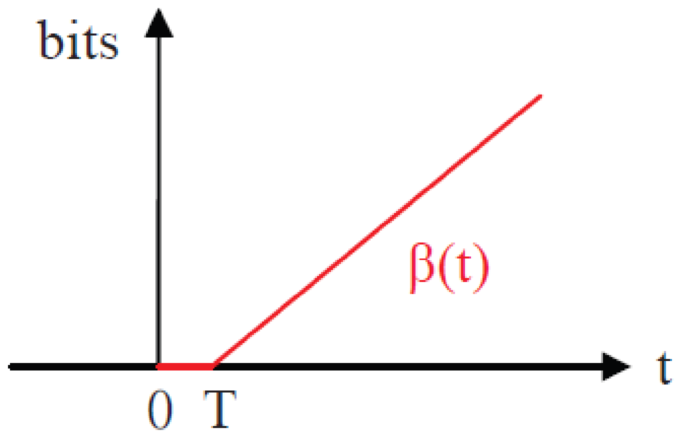

Figure 3.2 An example representation of the service curve [6]

The service curve equation can be written by using Figure 3.2 in practical analysis. The service capacity at the output port of m^{th} SW is indicated by R_m and the technological latency T_m. Technological latency (T_m) is defined as the time it takes for a packet to be accepted, processed, and served while no other operations are being performed on the SW. Thus, the time-dependent equation of the service curve can be described as:

$$\beta_m(t) = R_m(t - T_m)^{+}, \tag{3.6}$$

where $(.)^{+}$ denotes the max$(.,0)$ function. In the case of a single network flow (f_n) at the output port of m^{th} SW, the maximum delay for f_n is expressed as follows:

$$D_m^{f_n} = \frac{s_n}{R_m} + T_m \tag{3.7}$$

The $\alpha_n^{*}(t) = \alpha_n(t) \oslash \beta_m(t)$ function is used to compute the Modified arrival curve after f_n traffic flow passes m^{th} SW. For $\alpha_n(0) = 0$, $\beta_m(0) = 0$, $\oslash$ denotes the min-plus deconvolution operator. The closed-form formulation of the modified arrival curve can be described as follows:

$$\alpha_n^*(t) = r_n t + s_n + r_n T_m \tag{3.8}$$

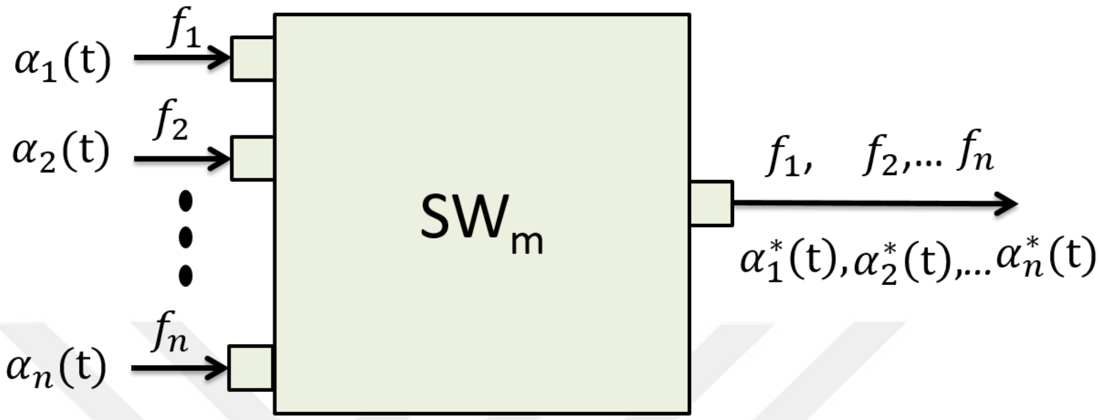

Figure 3.3 Multiple flow cross at switch

The maximum delay of each VL that utilizes the same output port of the switch can be calculated using the residual service curve [32], as illustrated in Figure 3.3.

Suppose that $I_m^{f_n} = f_1, f_2, ...f_{n-1}, f_{n+1}, ...$ displays the flows list that utilize the same port as flow f_n on the m^{th} switch. The service curve may be described as follows in case of the First-In-First-Out (FIFO) service element:

$$\beta_m^{f_n}(t) = (R_m - \sum_{i \in I_m^{f_n}} r_i)[t - \frac{R_m T_m + \sum_{i \in I_m^{f_n}} s_i}{R_m}]^+ \tag{3.9}$$

After implantation Equation (3.9) into Equation (3.7), the maximum latency bound of f_n can be written as:

$$D_m^{f_n} = \frac{s_n}{R_m - \sum_{i \in I_m^{f_n}} r_i} + \frac{R_m T_m + \sum_{i \in I_m^{f_n}} s_i}{R_m - \sum_{i \in I_m^{f_n}} r_i} \tag{3.10}$$

Equation 3.11 represents the modified arrival curve when many VLs use the same SW port.

$$\alpha_n^*(t) = r_n t + s_n + r_n \frac{R_m T_m + \sum_{i \in I_m^{f_n}} s_i}{R_m - \sum_{i \in I_m^{f_n}} r_i} \tag{3.11}$$

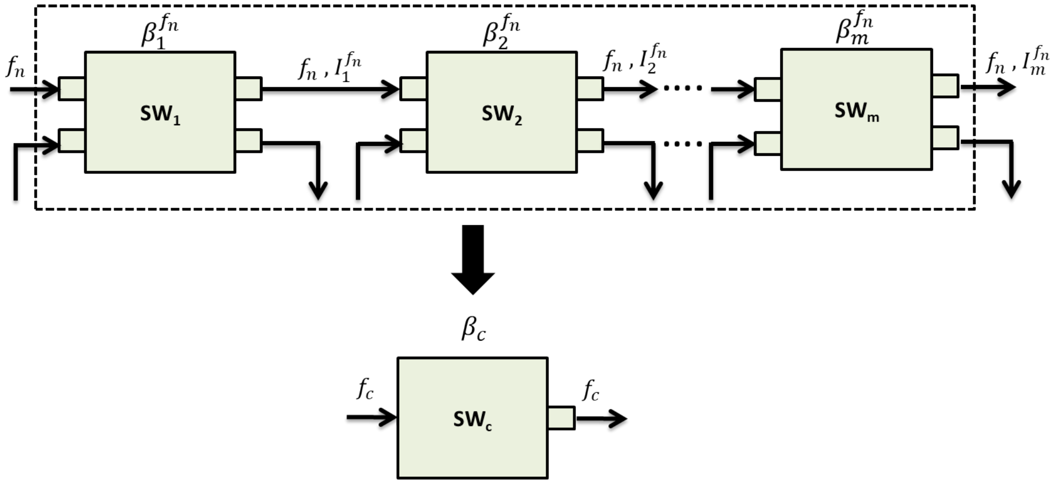

Figure 3.4 Residual service curve concatenation approach

The aggregate of the individually determined worst-case delay values at each switch gives a looser delay constraint when a traffic flow crosses many cascaded switches as illustrated in Figure 3.4. The Pay-Burst-Only-Once (PBOO) approach can achieve better worst-case delay limitations in cascaded SW conditions. The first SW in the PBOO approach regulates the incoming unregulated traffic arrivals to the second SW, eliminating the need for further delay at next SWs.

In the designed network configuration, the worst-case delay NC limits are calculated for each network flow (VL), and the suitability of the network planning is checked. When the network planning is done correctly, it is expected that the calculated NC limits for each VL within the deterministic network will be equal to or less than the BAG parameter for the worst-case delay of ES [32].

3.2 Network Calculus for Switchless ARINC-664

This section will perform a network calculus analysis for an ARINC-664 network consisting exclusively of ESs and there is no central ARINC-664 switches. In these network types, ESs with a restricted number of ports perform ARINC-664 switching in addition to other ES functions including traffic regulator, redundancy management, and scheduling. Network Calculus analysis is solely utilized in networks with no cyclic dependency between communication flows. In these topologies, flows can create cyclic dependencies, making it challenging to show the determinism of a network. The NC approach, which was originally designed for feedforward networks, has to be expanded to include cyclic-dependent mesh networks. We need to solve cyclic dependencies to perform worst-case delay analysis for Switchless ARINC-664. Several techniques have been offered in the literature to solve this problem. Among these approaches, we have applied an approach known as Time Stopping Method. We offer an example of the network topology, which are formed the cyclic dependency concept in Section 3.2.1. Then, in Section 3.2.2, we apply the Time Stopping Method (TSM) to solve cyclic dependency.

3.2.1 Cyclic Dependency

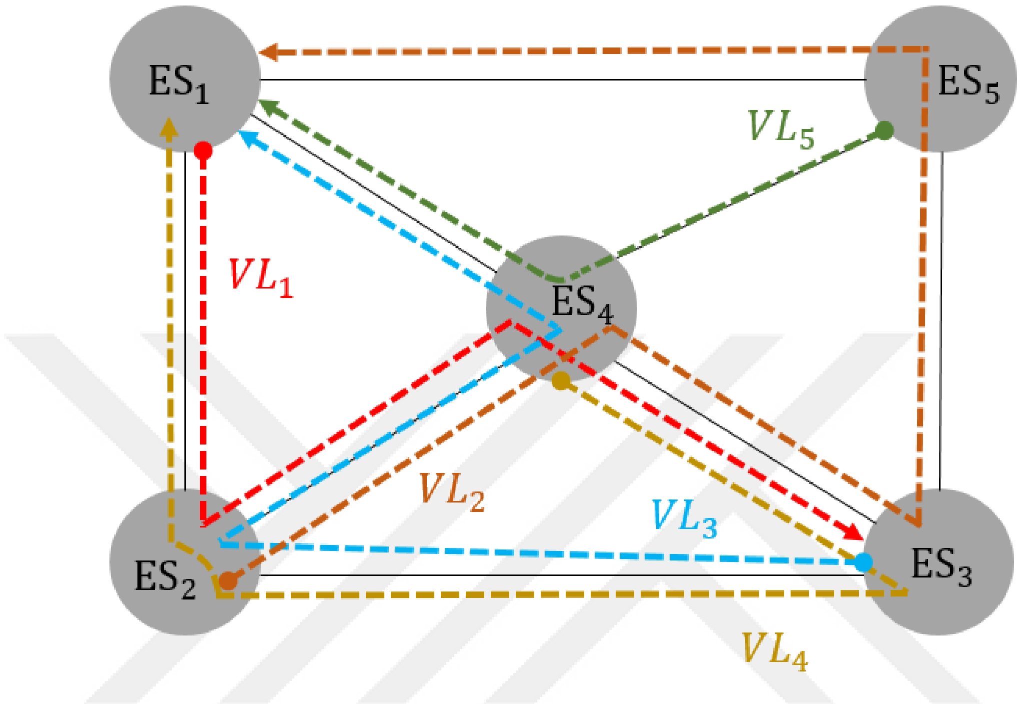

Figure 3.5 A cyclic dependency situation with five VLs

The cyclic dependence problem is demonstrated using a mesh network topology composed of five ESs, as illustrated in Figure 3.5. Five VLs have already been introduced to communicate between ES nodes. VL frames from ES_1 to ES_3, for example, are forwarded the use of VL_1 where ES_2 and ES_4 used to transmit packets. In another words, the route VL_1 is represented as $P^1_{VL_1} = (ES_1, ES_2, ES_4, ES_3)$. The delay analysis of VL_1 requires the arrival curves of other VLs which shares the same port with itself. In ES_1, VL_1 no longer shares the port with rest of the VLs. On the other hand, in ES_2, VL_1 utilizes the same port as VL_2 and VL_3. Thus, the modified arrival curves of VL_2 and VL_3, which are incoming ES_4, need to determine the worst-case delay of VL_1. In addition, given that VL_3 shares the same port with VL_4 in ES_3, the modified arrival curve of VL_3 which is received by ES_4 relies upon on the modified arrival curve of VL_4 to ES_2. Likewise, the modified arrival curve of VL_4 to ES_2 relies upon on the modified arrival curves of VL_1 and VL_2 to ES_3. In addition to, arrival curve of VL_5 relies upon on the modified arrival curve of VL_3 at ES_4. The cyclic dependency problem is a recursive dependence on modified arrival curves of individual VLs to determine the worst-case delay. To effectively fulfill the delay limitations of the VLs, this cyclic dependence issue must be handled.

3.2.2 Time Stopping Method

When network calculus equations are written for Switchless ARINC-664, it creates cyclic dependency, so we need to use a approach referred to as Time Stopping to resolve this situation. This section briefly explains the Time Stopping Method, which is described in detail at [34]. TSM's goal is to find NC equations for each port and flow that connect bursts and delays. Let r_n and s_n^{mp} present the rate at which f_n (ie VL_n) enters node m and the burst at which f_n enters node m. s_n^m indicates the burst port of f_n at node m^{th}.

$$s_n^m = s_n^{mp} + r_n \frac{R_m T_m + \sum_{i \in I_m^{f_n}} s_i^{mp}}{R_m} \tag{3.12}$$

where s_i^{mp} denotes the burst of f_i that enters node m^{th} Equation (3.12) is a set of equations that may be expressed in matrix form [34] as:

$$C \cdot X = D \tag{3.13}$$

where each C input represents the flows' output bursts port at the associated node through which the flow passes. The output bursts of the flows' necessary to determine the NC delay limits specified in Equation (3.11) are represented by X. It is worth noting that solving this equation provides the answer to the cyclic dependence problem.

4
DELAY OPTIMIZATION FOR SWITCHLESS ARINC-664 USING GENETIC ALGORITHM

Metaheuristic algorithms are widely employed in a variety of sectors, including economics, engineering, politics, and management, to solve challenging real-world problems. Metaheuristic algorithms rely heavily on condensation and diversity. The biological evolutionary process is used to inspire the majority of metaheuristic algorithms. The GA algorithm is a well-known metaheuristic algorithm that is used in the biological evolution process [35]. The exhaustive search approach in all possible paths of all VLs can be used to perform the worst-case latency value of VLs in the switchless ARINC-664 network topologies. When the number of possible VL paths increases, the search area grows exponentially, making an exhaustive search strategy too costly to explore. Figure 4.1 shows an example of switchless network topologies, which are composed of 10 ESs. The number of ports each ES is varied from 3 to 6 depending on the chosen topology. The total number of VLs is 11. For these network topologies, the number of possible paths for each port number is demonstrated in Figure 4.2. As the number of ES ports increases, the number of possible routes of VLs also increases. To identify the network VL route with the lowest latency limits, these VLs route in any combination must be investigated in the corresponding network topology. As a result, network topologies have a vast number of different route configurations. Therefore, for most practical networking scenarios, a specific search strategy is computationally prohibitive. The GA technique is used to efficiently derive the NC delay limits in this case.

4.1 Chromosome Structure and Initialization

The flowchart of GA, a powerful heuristic for exploring enormously vast search spaces, is shown in Figure 4.3. The genetic algorithm's implementation principle starts with a (usually random) population of chromosomes. GA, a population-based search algorithm, employs the survival of the fittest principle. The iterative employment of

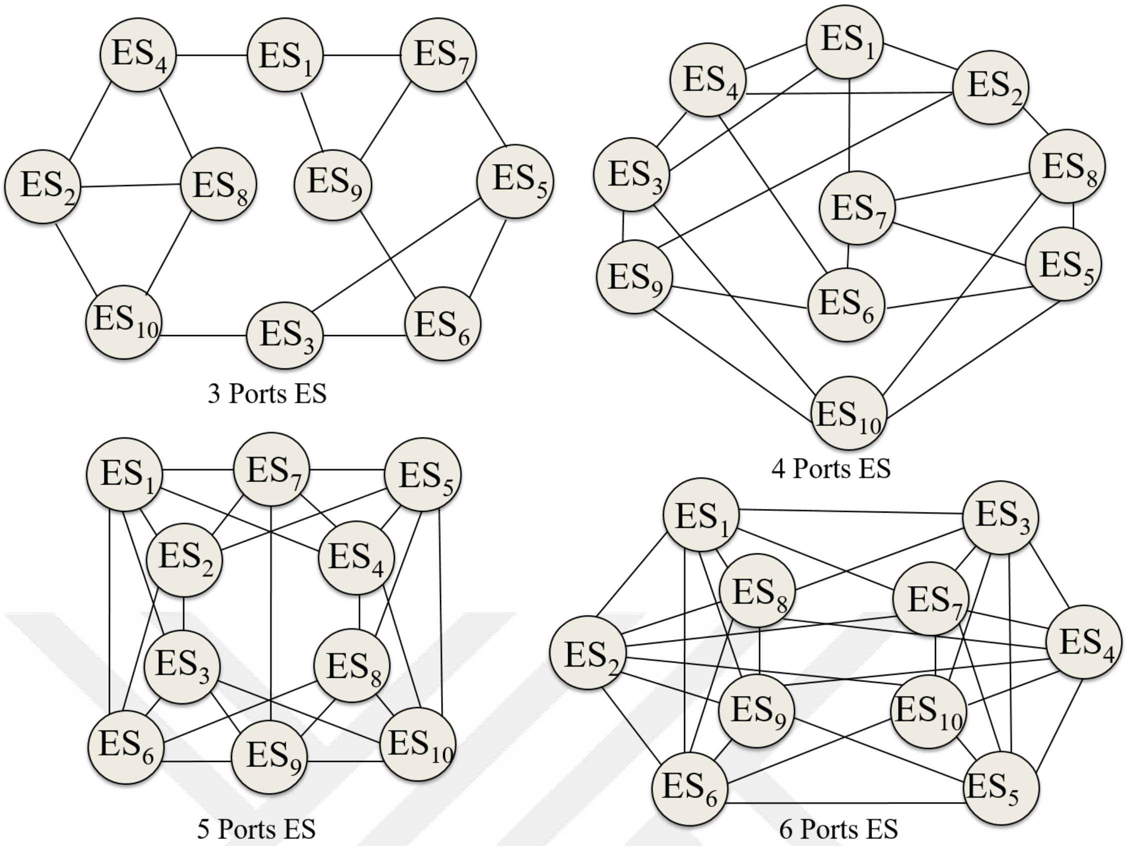

Figure 4.1 Switchless ARINC-664 topologies for different port numbers

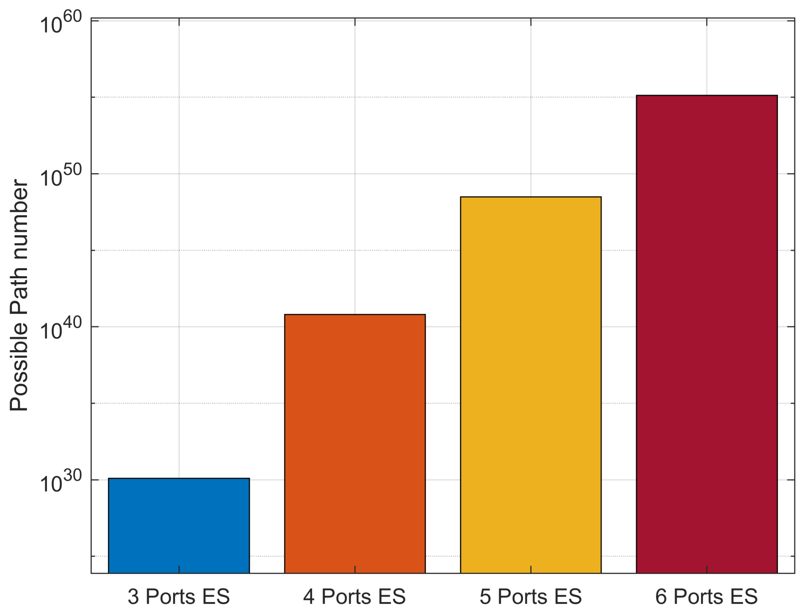

Figure 4.2 Possible paths for different port numbers

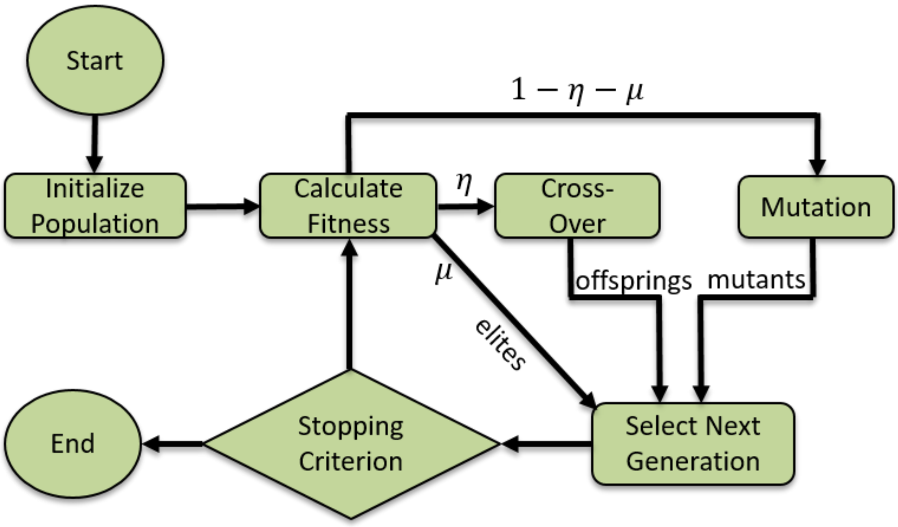

Figure 4.3 Flow chart of GA

genetic operators on individuals in the population generates new populations. GA requires the representation of chromosomes, selection, crossover, mutation, and the calculation of fitness functions. The GA procedure is as follows. As a first candidate solution, the GA generates K random chromosomes. The method then uses crossover and mutation operations to update the chromosomes regularly till the stopping condition is satisfied. The cost value of the previous generation, which includes every chromosome, is computed at each step, and the elites are transferred to the next generation. The elite proportion is defined by μ. Mutation and crossover operations are used to create population diversity. In our application, the GA chromosomal structure corresponds to path of VL alternatives [36]. For instance, each VL's chosen path corresponds to one gene on the chromosome, as illustrated in Figure 4.5.

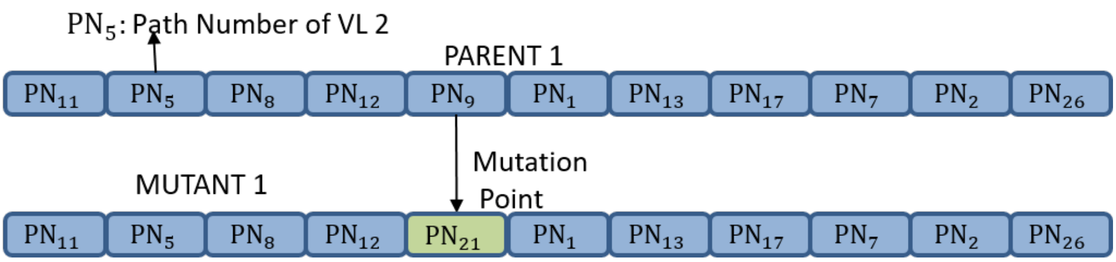

Figure 4.4 GA mutation operation

As demonstrated in Figure 4.5, the crossover operation is performed with the parent K_η randomly selected from the population. The crossover rate (η) parameter determines how many individuals are selected by the parents in the crossover. The crossover process produces offspring, which are handed on to the next generation.

As shown in Figure 4.4, a genetic operator (the mutation operation) is employed to ensure that the variety of the genetics is maintained among the generations. The

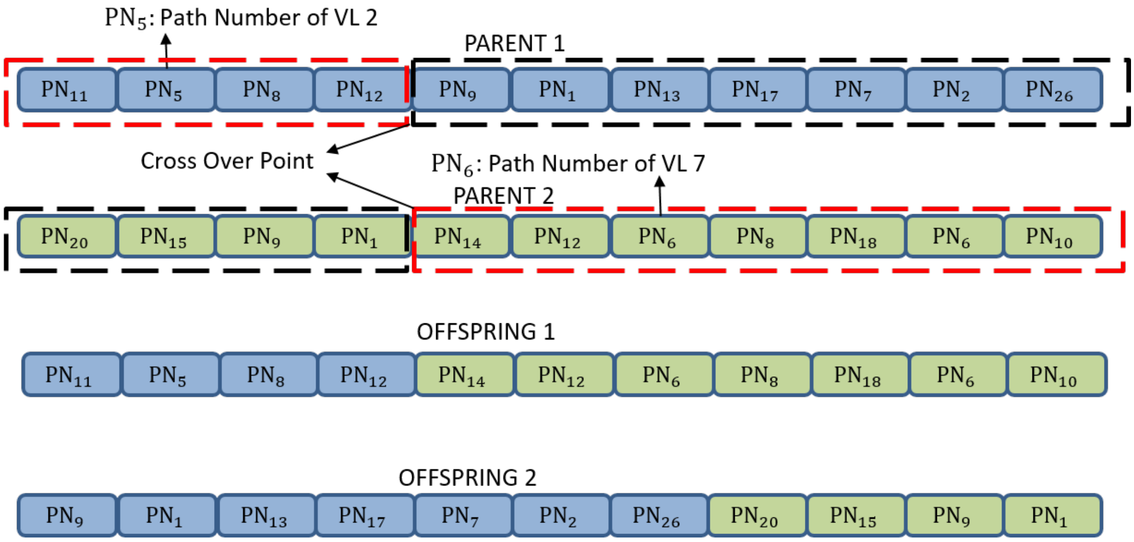

Figure 4.5 GA crossover operation

number of mutants created throughout the mutation process is determined by the parameter (1-η-μ). In this study, the one with the highest number among all the iterations was used to determine the stopping criteria.

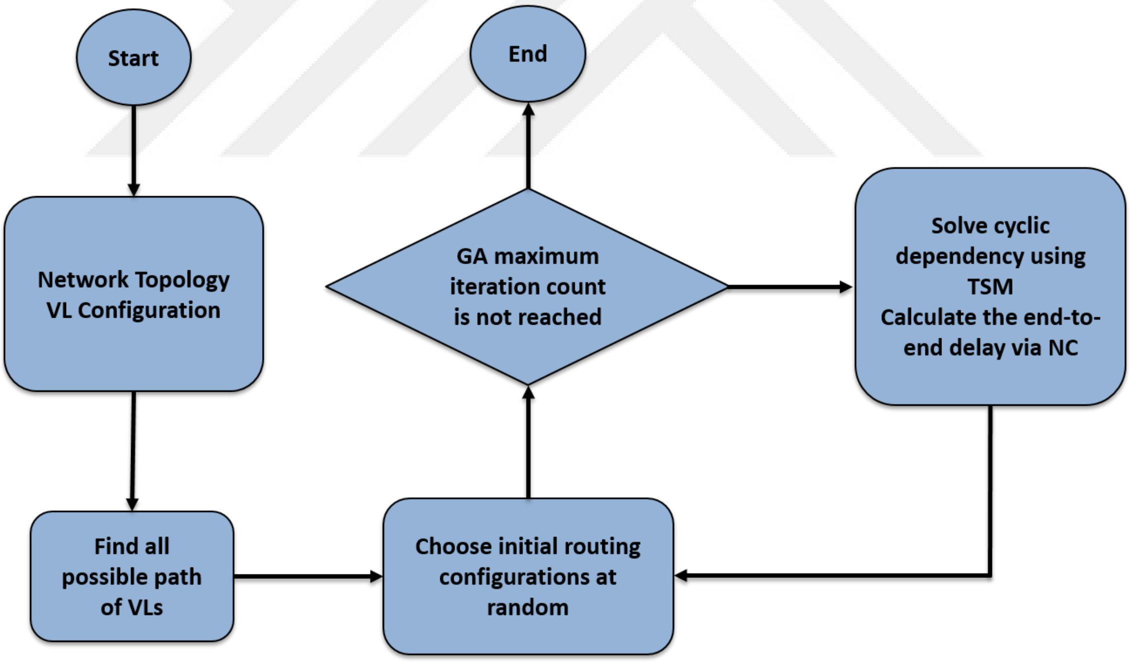

Figure 4.6 Algorithm of VL delay analysis

The proposed algorithm determines each VL's possible paths of the related network topology. The first K chromosomes are chosen randomly. Later, until the highest number among all the iterations is achieved, GA searches for alternative route configurations. The cost value of each chromosome is computed at each GA iteration, as shown Figure 4.6, by solving the TSM cyclic dependency equations in Section 3.2.2 and applying the NC delay equations in Section 3.1. The elite routing configuration, which does not need any crossover and mutation processes, can be transferred to the next generation. After crossover and mutation procedures have been applied, the ones which survives among all the chromosomes are used to produce new chromosomes. The VL chromosome with the minimum worst-case delay limit is chosen as the best option when the highest number among all the iterations is achieved.

5
NUMERICAL EXPERIMENTS

The numerical results are shown in this section utilizing the GA-based route optimization technique for switchless ARINC-664, ring network, and reference ARINC-664 network topologies of worst-case delay analysis. 5 SW, 10 ES, and 11 VL shown in Figure 5.1, the worst-case delay analysis were performed to transmit an end-to-end packet for each VL using the reference ARINC-664 network topology. The service capacity for each output port of SW in the reference topology ($R_m, m \in \{1, 2, ..\}$) and the technological latency ($T_m, m\ in\ 1, 2, ..$) the parameters are selected as 1 Gbps and 16 μs respectively. All of the VLs in the network have the BAG and L_{max} parameters set to 1 ms and 1500 bytes, respectively. The worst-case delay for each VL, an average of the worst delay values of VLs, and the maximum VL delay has been reported for all scenario.

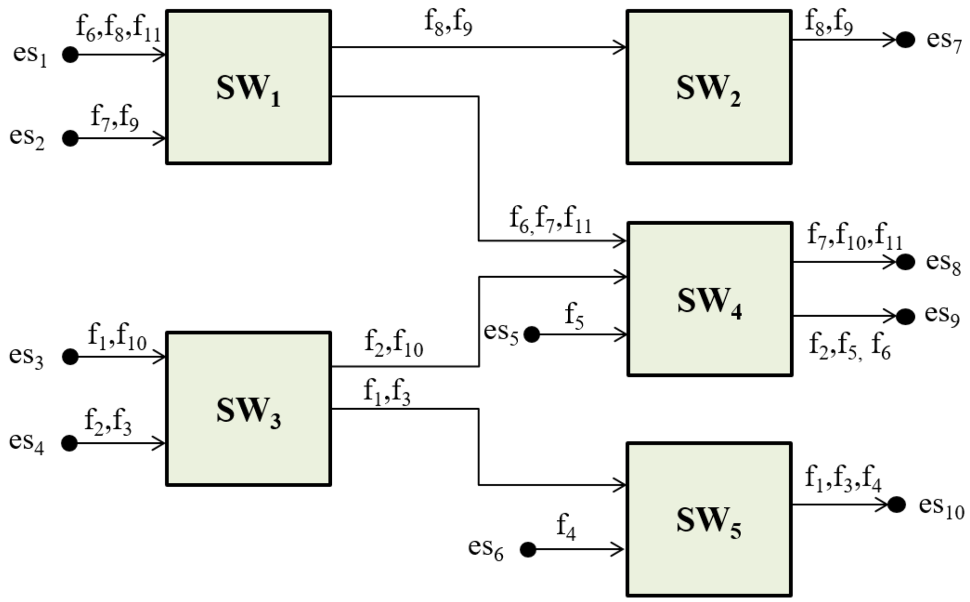

Figure 5.1 ARINC-664 reference network topology [37].

The switchless network topology in which the network switch functions are integrated into the end system is created 3,4,5, and 6 ports ES as shown in Figure 5.2. These topologies is formed by using ARINC-664 reference network topology as shown in

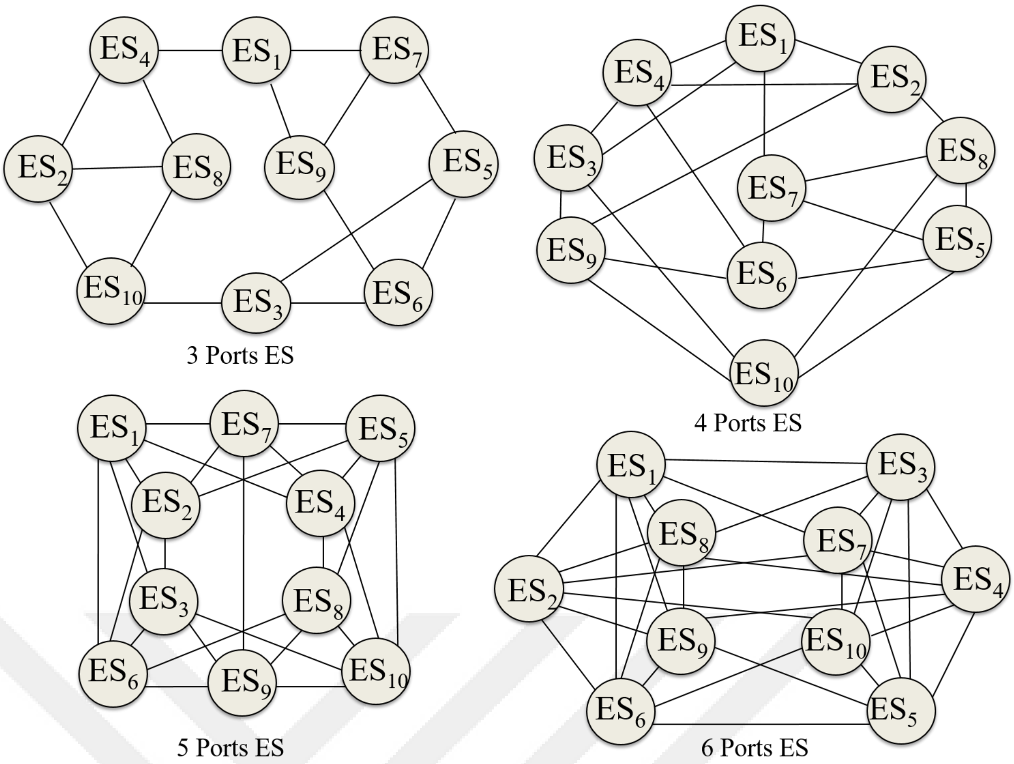

Figure 5.2 Switchless ARINC-664 topologies for different output port.

Figure 5.1 in which the end system and switch elements are separated without changed source and destination of VL. The other network topology that is shown in Figure 5.3, which is named ring network topology, is created by using reference network topology.

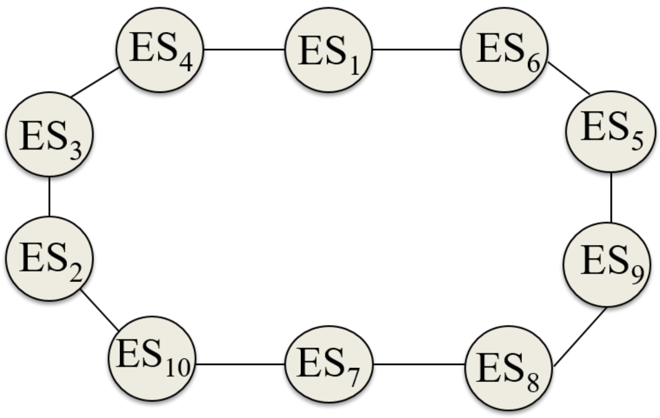

Figure 5.3 The Ring network topology

The destination and source table for each VL is shown in Table 5.1. The worst-case delay analysis is performed using network calculus for each VL in switchless topologies. The delay of VL average worst-case and the maximum delay values was calculated using network calculus and reported. These results is compared to the reference network topology results, ring network topology, and switchless ARINC-664 network topologies. Path optimization is required for switchless ARINC-664 topologies, as each VL has many possibly many alternative paths. As the number of ES ports increases, so does the number of possible routes of the VLs. All combinations of these VL paths must be regarded in the respective network topology to decide the network configuration with the lowest latency limits. This leads to an enormous range of alternative routing configurations in network topologies. Thus, a comprehensive search technique is computationally expensive for practical network topologies. Therefore, we use the GA-based route optimization for switchless ARINC-664 topologies to derive the NC delay limits computationally efficiently. Switchless ARINC-664 network topologies have a many possible path for different output ports. When the output port of ESs' has a maximum port, the possible path configuration is reached the maximum count. GA parameter is selected according to the maximum number of possible paths of VL's for switchless ARINC-664 network topologies.

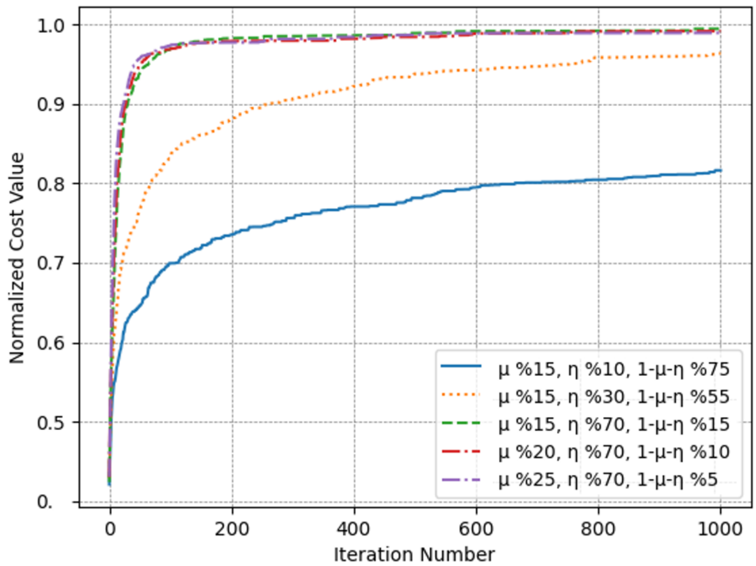

Figure 5.4 Optimization of the GA parameters

In the figure above, the impact of the GA parameters on worst-case delay is examined. When the and the cross-over rate is increased from 10% to 70% and elite ratio (μ) is set as 15%, lower delay bounds are achieved. These results indicate that the exploration of the search space gets faster as the cross-over rate increases. No noticeable effect on the delay-bound can be seen if the cross-over rate is fixed at 70% and the mutation rate is increased from 5% to 15%. The elite, cross-over, and mutation rates are set to 25%, 70%, and 5%, respectively, for the rest of the experiments in this thesis.

Figure 5.7 shows the worst-case delay results obtained using network calculus for each

Table 5.1 The source and destination ESs for each VL

VL ID	*Source - Destination*
VL ID 1	ES3-ES10
VL ID 2	ES4-ES9
VL ID 3	ES4-ES10
VL ID 4	ES6-ES10
VL ID 5	ES5-ES9
VL ID 6	ES1-ES9
VL ID 7	ES2-ES8
VL ID 8	ES1-ES7
VL ID 9	ES2-ES7
VL ID 10	ES3-ES8
VL ID 11	ES1-ES8

VL in different topologies. Higher latency values are obtained for each VL in the ring network topology. The reason is that VLs in this network topology share the same path with other VLs as there are only two paths they can go to on their destination routes.

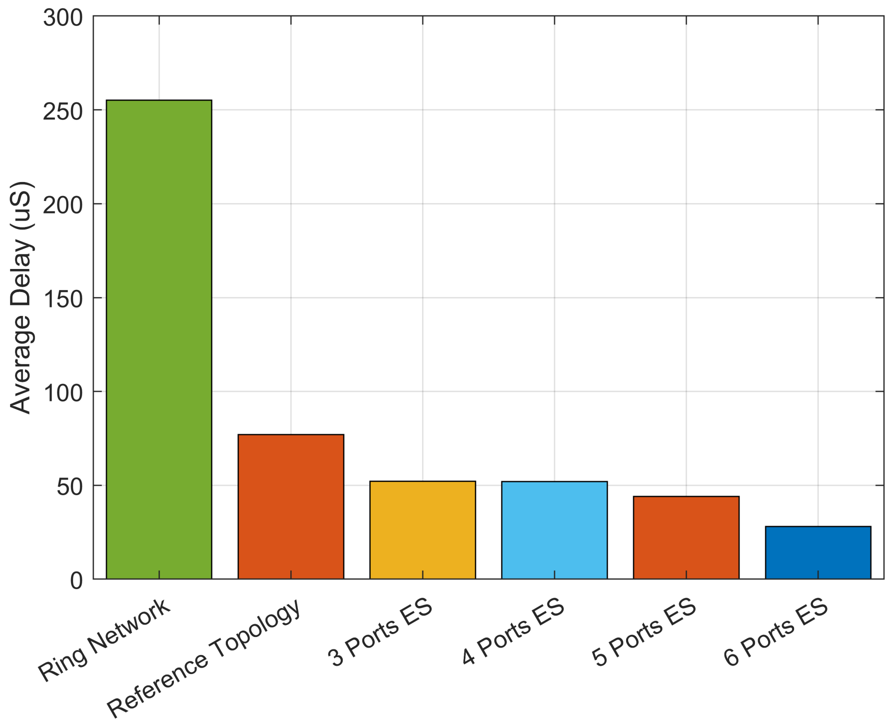

Figure 5.5 The average delay

Therefore, the delay values are higher compared to other network topologies. Figure 5.5 and Figure 5.6 show the results of the mean worst-case delay and the largest VL delay of the VLs for all topologies. It is observed that as the number of ports in ESs increases, the average and maximum delay values decrease depending on the number

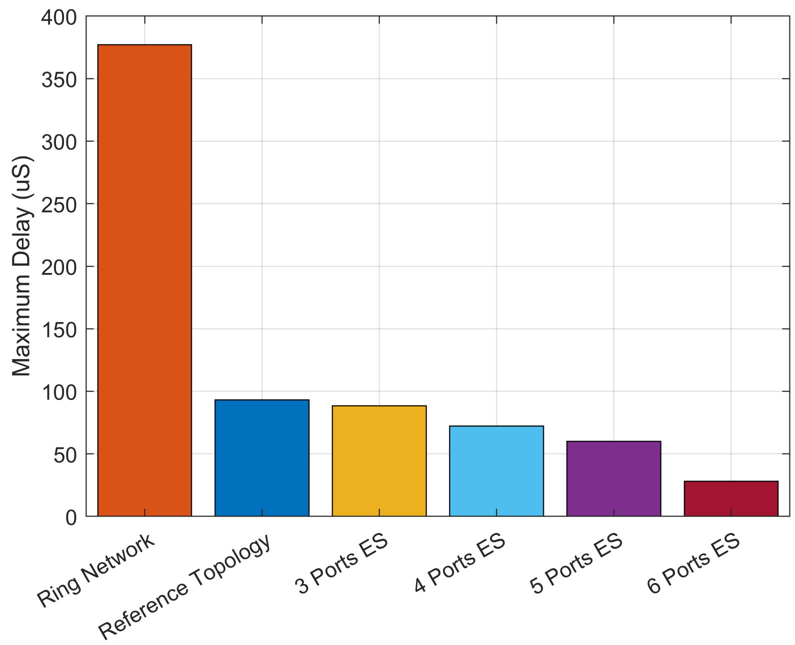

Figure 5.6 The maximum delay

of ports. In addition, since the source and destination ESs are directly connected in the switchless topology where 6-port ES is used, it has been observed that the average and maximum delay values are equal to each other and 28 μs.

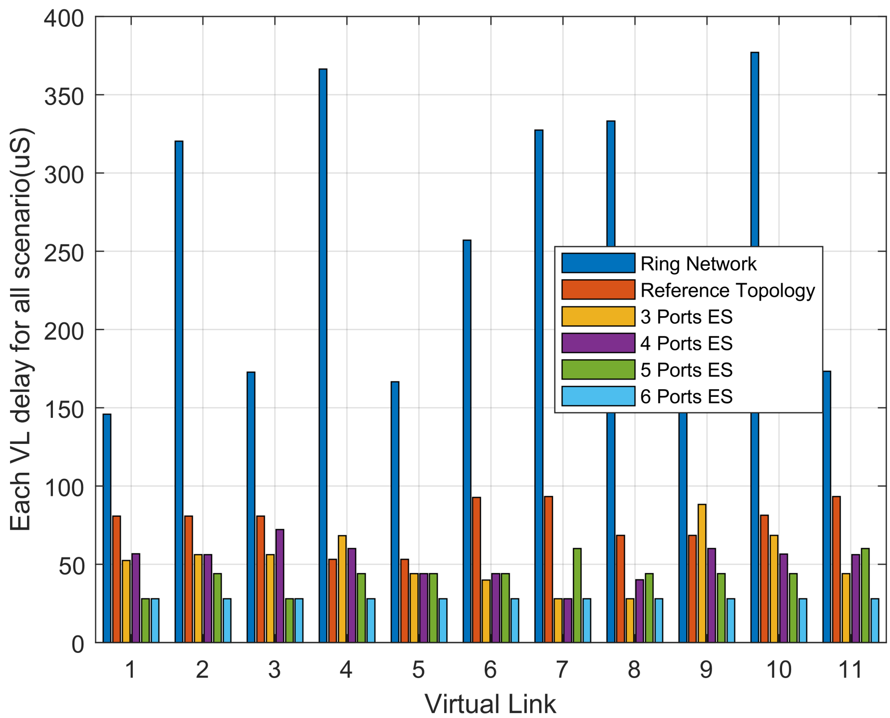

Figure 5.7 The delay of each VL

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RESULTS AND DISCUSSION

The ARINC-664 protocol is a prominent embedded communications technology in civil and military aircraft. The main features of ARINC-664 are high transmission rate, guaranteed bandwidth for data, redundancy mechanism, and determinism. These improvements let the IMA architecture use the ARINC-664 protocol. The IMA concept offers considerable size, weight, and power savings in next-generation avionics systems. Deterministic network technologies are required for that concept. Ethernet-based ARINC-664 deterministic network technology has been widely employed to fulfill the high-speed data communication requirements of IMA systems. In this thesis, the Network Calculus technique compares the delay performance of the ARINC-664 network topology, which separates the end system and switch elements, the ring network, and the switchless network topology, which integrates the network switch functions into the end system. For switchless ARINC-664 network topologies, as the number of ES ports increases, the number of possible routes of VLs also increases. All of the VL path combinations must be taken into account in the respective network topology to determine the lower delay bounds. This causes to an enormous number of alternative routing configurations in network topologies. Thus, we utilize GA-based VL route optimization for switchless ARINC-664 topologies. For all scenarios, 10 ESs and 11 VLs are used. The worst-case delay analysis of the ARINC-664 system with reference, switchless, and ring topologies is carried out with the network calculus approach. Experimental results show that the average and maximum latency values for network switchless topologies are smaller than for reference and ring network topologies. It has been observed that as the number of ports in ESs increases, the latency values in network switchless topologies decrease. In future work, we will investigate the disadvantages of increasing the number of ports in terms of memory usage. A model network will be proposed about how many ports the ES should have for a given topology.

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PUBLICATIONS FROM THE THESIS

Conference Papers

1. B. Gül, M. Garip, et al., “Latency analysis of switchless arinc 664 using network calculus,” in 2021 29th Signal Processing and Communications Applications Conference (SIU), IEEE, 2021, pp. 1–4.