ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

GAN BASED HIGH EFFICIENCY CLASS AB POWER AMPLIFIER DESIGN FOR SUB-6GHZ 5G TRANSMITTER SYSTEMS

M.Sc. THESIS

Kudret ÜNAL

Department of Electronics and Communication Engineering

Electronics Engineering Programme

FEBRUARY 2021

ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

GAN BASED HIGH EFFICIENCY CLASS AB POWER AMPLIFIER DESIGN FOR SUB-6GHZ 5G TRANSMITTER SYSTEMS

M.Sc. THESIS

Kudret ÜNAL
(504171211)

Department of Electronics and Communication Engineering

Electronics Engineering Programme

Thesis Advisor: Assoc. Prof. Mustafa Berke YELTEN

FEBRUARY 2021

İSTANBUL TEKNİK ÜNİVERSİTESİ ★ LİSANSÜSTÜ EĞİTİM ENSTİTÜSÜ

6 GHZ ALTI 5G VERİCİ SİSTEMLERİ İÇİN GAN TABALI YÜKSEK VERİMLİLİĞE SAHİP AB SINIFI GÜÇ KUVVETLENDİRİCİSİ TASARIMI

YÜKSEK LİSANS TEZİ

Kudret ÜNAL
(504171211)

Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

Elektronik Mühendisliği Programı

Tez Danışmanı: Doç. Dr. Mustafa Berke YELTEN

ŞUBAT 2021

Kudret ÜNAL, a M.Sc. student of İTU Graduate School student 504171211, successfully defended the thesis/dissertation entitled "GAN BASED HIGH EFFICIENCY CLASS AB POWER AMPLIFIER DESIGN FOR SUB-6 GHZ 5G TRANSMITTER SYSTEMS", which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

Thesis Advisor :	**Assoc. Prof. Mustafa Berke YELTEN** İstanbul Technical University	....
Jury Members :	**Assoc. Prof. Metin YAZGI** Istanbul Technical University	....
	Asst. Prof. Okan Zafer BATUR Istanbul Bilgi University	....

Date of Submission : 22 January 2021
Date of Defense : 16 February 2021

To my spouse,

FOREWORD

First, I would like to thank my advisor, Mustafa Berke YELTEN, for his help and guidance for this project and for his mentorship over the past five years. His guidance and contributions have a lot of impact on widening my engineering perspective. I would like to express my gratidute all members of ITU RF Electronics Laboratory and ITU VLSI Laboratory for their valuable knowledge, guidance, and support.

I would like to thank the commitee members Assoc. Prof. Metin YAZGI and Asst. Prof. Okan Zafer BATUR for their valuable time and their comments on this project.

I would like to thank my family for their conditnued support, dedication, and encouragement during my whole education. Lastly, greatest of the thanks is belong to my spouse, Kadriye, who is always by my side to support me. There are no words to describe her great support and faith in me.

February 2021

Kudret ÜNAL
(Electronics Engineer)

TABLE OF CONTENTS

Page

ABBREVIATIONS

1G	**:** 1st Generation
2G	**:** 2nd Generation
3G	**:** 3rd Generation
4G	**:** 4th Generation
5G	**:** 5th Generation
CDMA	**:** Code Division Multiple Access
dB	**:** decibell
dBm	**:** decibell miliwatt
DC	**:** Direct Current
DSP	**:** Digital Signal Processing
DUT	**:** Device Under Test
EM	**:** Electromagnetic
eV	**:** Electron Volt
FDMA	**:** Frequency Division Multiple Access
GaAs	**:** GaAs
GaN	**:** Gallium Nitride
Gbps	**:** Gigabit per second
GHz	**:** Gigahertz
HD	**:** High Definition
kbps	**:** kilobit per second
Mbps	**:** Megabit per second
MHz	**:** Megahertz
MIMO	**:** Multiple Input Multiple Output
mW	**:** miliwatt
P1dB	**:** 1 dB Compression Point
PA	**:** Power Amplifier
PAE	**:** Power Added Efficiency
PHEMT	**:** Pseudomorphic High Electron Mobility Transistor
PSTN	**:** Public Swithed Telephone Network
Si	**:** Silicon

SiC **:** Silicon Carbite

TDMA **:** Time Division Multiple Access

W **:** Watt

WWWW **:** World Wide Wireless Web

SYMBOLS

G	: Gain
$\mathbf{I_D}$	: Drain Current
$\mathbf{I_{DD}}$	: Drain Supply Current
$\mathbf{P_G}$	: Power Gain
$\mathbf{P_{in}}$	: Input Power
$\mathbf{P_{out}}$	: Output Power
$\mathbf{R_L}$	: Load Resistance
$\mathbf{V_{DD}}$	: Drain Supply Voltage
$\mathbf{V_{GS}}$	: Gate Supply Voltage
$\mathbf{V_{in}}$	: Input Voltage
$\mathbf{V_{out}}$	: Output Voltage
η	: Efficiency
η_{PAE}	: Power Added Efficiency

LIST OF TABLES

Page

LIST OF FIGURES

Page

GAN BASED HIGH EFFICIENCY CLASS AB POWER AMPLIFIER DESIGN FOR SUB-6 5G TRANSMITTER SYSTEMS

SUMMARY

Wireless data transfer was first performed at the end of the 19th century as the result of the theoretical and practical studies of Maxwell, Marconi, Hertz, and Tesla. At the beginning of the 20th century, with the rapidly developing radio technology, wireless communication started to become widespread. With each passing day, the need to deliver more data to more people has increased and the communication frequency used has increased in parallel with the increasing amount of data.

The first mobile phone call was made by Martin Cooper in 1973 and marked the beginning of a new era. The first-generation cellular network technology, called 1G, entered our lives in the late 70's and in the following years, it has come to the present day with 2G, 3G, 4G and 5G. From the first to the fifth generation, it is aimed to increase data rate and use frequency band more effectively. With the need for bandwidth brought by the high data transfer requirement, the communication frequency has increased continuously. The data transfer rate of 2.4kbps in the first generation is planned to be 20 Gbps in the fifth generation. For 5G New Radio, two different frequency spectrums are defined as below 6 GHz and above 24 GHz.

The power amplifiers that are the subject of this study are used as the last circuit element before the antenna in the transmitting parts of communication systems. Power amplifiers provide high power output signal by amplifying the signal on their inputs using DC power. As with every active electronic element, high power amplifiers are also desired to have high efficiency. Since the highest power consuming element in transmitter systems is the power amplifier, the efficiency of the power amplifier has an important share in the total transmitter efficiency.

Power amplifiers are divided into two main groups as linear (current source) and switched power amplifiers. Linear power amplifiers are divided into four as Class A, Class B, Class AB, and Class C with the bias point of the transistor. Gate bias determines the conduction angle of the transistor.

Class A power amplifiers are biased to have a high drain current compared to the input signal, and the transistor continuously flows current regardless of the input signal power. DC power consumption is high due to high quiescent current and their maximum theoretical drain efficiency is 50%. Class A power amplifiers are the most linear power amplifier type because it is in conduction at all angles of the input signal.

As a solution to the low efficiency of class A power amplifiers, class B power amplifiers are biased at the cutoff point of the transistor and transistor is in conduction only half the period of the input signal and the conduction angle is 180 degrees. Since the overlapping portions of the current and voltage curves of the transistor are reduced compared to Class A, DC power consumption is lower than Class A power amplifiers and the theoretical drain efficiency is calculated as 78%.

The bias point of the Class C power amplifiers is selected below the cut-off voltage, so that the conduction angle is smaller than 180 degrees. Transistor conducts current for only a small portion of the input signal and DC power consumption is the lowest among the linear power amplifier classes. Theoretically, as the conduction angle approaches zero, drain efficiency approaches 100%.

The bias point of class AB power amplifiers is chosen between class A and class B, and the conduction angle of the transistor is between 180 degrees and 360 degrees. Theoretical drain efficiency is between 50% and 78%.

Conduction angle is directly related to the linearity of the amplifier. As the conduction angle decreases, the efficiency increases, but the efficiency of the transistor decreases. For this reason, class AB power amplifiers is a good power amplifier class in terms of efficiency / linearity balance.

In this study, a Class AB power amplifier having high gain, high efficiency and delivering 10W output power at 3 dB suppression point was designed for 5G Sub-6 GHz applications. 3.3 GHz - 3.6 GHz frequency range has been chosen as the design frequency. Since it gives much better results compared to other materials at high output power and frequencies, it was decided to use GaN (gallium nitride) transistor in the design and QPD1009 model of Qorvo was chosen for this purpose.

The nonlinear model of the QPD1009 transistor was provided by Modelithics Qorvo GaN Library Student Support Program and imported to the AWR Microwave Office design program.

First, the transistor was biased with ideal design elements and DC-IV curves were created and a bias point suitable for Class AB operation was determined. Accordingly, the point where the transistor has 59 mA drain current for 50V source voltage was selected.

Load-pull analysis was performed to determine the load and source impedances at 3 dB compression point which satisfies the design goals at specified frequency interval.

Input-output supply circuit are designed to show high impedance at the operating frequency of the transistor. To ensure the transistor's stability in a wide frequency range, resistors are added on the gate feed line and on the input line. In this way, unwanted oscillation of the transistor is prevented.

In order to realize the simulation results made with ideal elements, the substrate selection was made, and it was decided to use the 0.762 mm thick Rogers 4350B substrate which is a well-known and widely used substrate in high frequency designs. Load impedance values determined by load-pull analysis were designed with the drain feed line. The input matching circuit has been designed and the entire design has been combined. With a few iterations on input and output circuitry, PAE, gain and output power were improved.

By making electromagnetic simulation of the designed circuit, the characteristic behavior of microstrip lines in the real environment was examined and small adjustments were made in the line sizes. Final simulations were made for output power, gain, efficiency with added power and second and third harmonic components of the main signal.

As a result of the simulations, it was seen that the designed circuit provided 10W output power in the 3.3 GHz - 3.6 GHz band, a gain of more than 55% and a linear gain of about 19 dB, and the design of the power amplifier was completed.

Designed amplifier was manufactured and assembled for the measurements. As a result of the measurements made, it was observed that the circuit provided the expected gain, but the output power was 38-38.5 dBm and the power added efficiency was measured around 50%. It was determined that the difference might be related with the output impedance difference of the transistor in simulation and relatity, and it was decided to replace the output stage impedance matching elements with different values and to compare the measurement results with the previous results and to find a better output impedance point.

6 GHZ ALTI 5G VERİCİ SİSTEMLERİ İÇİN GAN TABALI YÜKSEK VERİMLİLİĞE SAHİP AB SINIFI GÜÇ KUVVETLENDİRİCİSİ TASARIMI

ÖZET

Kablosuz veri aktarımı ilk olarak Maxwell, Marconi, Hertz ve Tesla'nın teorik ve Pratik çalışmalarının birikimi sonucu 19. yüzyılın sonlarında gerçekleştirilmiştir. 20. Yüzyılın başlarında hızla gelişen radyo teknolojisi ile telsiz haberleşme ve yaygınlaşmaya başladı. Her geçen gün daha fazla verinin, daha fazla kişiye ulaştırılması ihtiyacı yükselmiş ve kullanılan haberleşme frekansı artan veri miktarına paralel olarak yükselmiştir.

İlk cep telefonu görüşmesi 1973 yılında Martin Cooper tarafından yapılmış ve yeni bir dönemin başlangıcı olmuştur. 1G olarak adlandırılan birinci nesil hücresel ağ teknolojisi 70'li yılların sonunda hayatımıza girmiş ve ilerleyen yıllarda 2G,3G, 4G ve 5G ile günümüze gelinmiştir. Birinci nesilden beşinci nesle kadar veri artırım hızı ve frekans bandının daha efektif bir şekilde kullanılması hedeflenmiştir. Yüksek veri aktarım ihtiyacının getirdiği bant genişliği ihtiyacı ile haberleşme frekansı sürekli olarak artmıştır. Birinci nesilde 2.4kbps olan veri aktarım hızının beşinci nesilde 20 Gbps seviyesinde olması planlanmaktadır. 5G Yeni Radyo için 6 GHz altı ve 24 GHz üstü olmak üzere iki farklı frekans spektrumu tanımlanmaktadır.

Bu çalışmanın konusu olan güç kuvvetlendiricileri, haberleşme sistemlerinin verici kısımlarında antenden önceki son devre elemanı olarak kullanılır. Güç kuvvetlendiricileri, DC güç kullanarak girişlerindeki işareti güçlendirerek yüksek güce sahip çıkış işareti sağlarlar. Her aktif elektronik elemanda olduğu gibi yüksek güç kuvvetlendiricilerinin de yüksek verimliliğe sahip olması istenir. Verici sistemlerindeki en yüksek güç tüketen eleman güç kuvvetlendirici olduğu için güç kuvvetlendiricisinin verimliliği toplam verici verimliğinde önemli bir yer tutar.

Güç kuvvetlendiricileri lineer (akım kaynağı) ve anahtarlamalı güç kuvvetlendiricileri olarak iki ana gruba ayrılır. Lineer güç kuvvetlendiricileri kapı (gate) kutuplamalarına göre A Sınıfı, B sınıfı, AB Sınıfı ve C sınıfı olmak üzere dörde ayrılır. Kapı kutuplamaları tranzistorun giriş işaretinin iletimin açısını belirler.

A sınıfı güç kuvvetlendiricileri giriş işareti ile karşılaştırıldığında yüksek bir savak akımına sahip olacak şekilde kutuplanır ve transistor giriş işaretinin büyüklüğünden bağımsız olarak sürekli olarak akım akıtır. DC güç tüketimleri yüksek kutuplama noktası sebebi ile yüksektir ve teorik savak verimliliği en fazla %50'dir. Tranzistor giriş işaretininin tüm açılarında iletimde olduğu için A sınıfı güç kuvvetlendiricileri en doğrusal güç kuvvetlendirici çeşididir.

A sınıfı güç kuvvetlendiricilerinin düşük verimliliğine çözüm olarak B sınıfı güç kuvvetlendiricileri tranzistorun kesim noktasında kutuplanır ve tranzistor giriş işaretinin yalnızca yarım periyodunda iletimdedir ve iletim açısı 180 derecedir. Tranzistorun akım ve gerilim eğrilerinin kesişim noktaları A sınıfına göre

azaltıldığından DC güç tüketimleri A sınıfı güç kuvvetlendiricilerine oranla daha düşüktür ve teorik savak verimliliği %78 olarak hesaplanmaktadır.

C sınıfı güç kuvvetlendiricilerinin kutuplama noktası kesim geriliminin de altında seçilerek iletim açısının 180 dereceden daha küçük olması sağlanır. Tranzistor giriş işaretinin yalnızca küçük bir kısmında iletimdedir ve DC güç tüketimi lineer güç kuvvetlendiriciler arasındaki en düşük sınıftır. Teorik olarak iletim açısı sıfıra yaklaştıkça savak verimliliği %100'e yaklaşır.

AB sınfı güç kuvvetlendiricilerinin kutuplama noktası A sınıfı ile B sınıfı arasında seçilir ve transiztorun iletim açısı 180 derece ile 360 derece arasındadır. Teorik savak verimlilikleri %50 ile %78 arasındadır.

İletim açısı kuvvetlendiricinin doğrusallığı ile doğrudan ilişkilidir. İletim açısı azaldıkça verimlilik artmakta ancak transiztorun verimliliği de azalmaktadır. Bu sebeple AB sınıfı güç kuvvetlendiricileri verimlilik/doğrusallık dengesi açısından dengeli bir güç kuvvetlendiricisi sınıfıdır.

Bu çalışmada 5G 6 GHz altı frekans bandı için yüksek kazançlı, 3 dB bastırma noktasında yüksek verimliliğe ve 10W çıkış gücüne sahip AB sınıfı bir güç kuvvetlendiricisi tasarımı hedeflenmiştir. Tasarım frekansı olarak 3.3 GHz- 3.6 GHz frekans aralığı seçilmiştir.

Diğer yarıiletkenler ile karşılaştırıldığında GaN (Galyum Nitrür) yüksek bant aralığı, yüksek kırılma gerilimi, yüksek electron doygunluk hızı ve SiC (Silikon Karbür) tabanlar ile kullanıldığında yüksek ısıl iletkenliğe sahip olması sebebiyle yüksek frekans, yüksek güç uygulamaları için uygun bir adaydır. Yüksek güç yoğunluğu ile aynı miktarda çıkış gücü GaN tabanlı transistörler ile daha küçük bir alanda sağlanabilir.

Yüksek çıkış güç ve frekanslarında diğer materyallerle karşılaştırıldığında çok daha iyi sonuçlar vermesi sebebi ile AB Sınıfı Güç Kuvvetlendiricisi tasarımda GaN tabanlı bir transistor kullanılmasına karar verilmiş ve bu amaçla Qorvo firmasına ait QPD1009 tranzistör modeli seçilmiştir.

QPD1009 transistorunun doğrusal olmayan modeli Modelithics firmasının Qorvo GaN kütüphanesi öğrenci destek programı ile edinilmiş ve AWR Microwave Office tasarım programına aktarılmıştır.

Transistor ilk olarak ideal tasarım elemanları ile kutuplanmış ve DC-IV eğrileri oluşturularak AB Sınıfı çalışmaya uygun bir kutuplama noktası belirlenmiştir. Buna göre transistorun 50V kaynak gerilimi için 59 mA savak akımına sahip olduğu nokta seçilmiştir.

Güç kuvvetlendiricisinin istenilen 3 dB bastırma noktasında istenilen güç eklenmiş verim, kazanç ve çıkış gücünü sağlamsı için gereken yük ve kaynak empedansları yükle-çek analizi ile 3.3 GHz, 3.4 GHz, 3.5 GHz ve 3.6 GHz frekanslarında belirlenmiştir.

Giriş-çıkış besleme hatları transistorun çalışma frekansında yüksek empedans gösterecek şekilde tasarlanmıştır. Transistorun geniş frekans aralığında kararlılık göstermesi için kapı besleme hattı üzerine ve giriş hattı üzerine direnç eklenmiştir. Bu sayede transistorun istenmeyen salınım yapması engellenmiştir.

İdeal elemanlar ile yapılan benzetim sonuçlarının gerçeklenmesi için taban seçimi yapılmış ve 0.762 mm kalınlığında Rogers 4350B tabanın kullanılmasına karar verilmiştir. Yükle-çek analizi ile belirlenen yük empedans değerleri savak besleme hattı ile birlikte tasarlanmıştır.

Çıkış katının tasarımının ardından giriş uyumlama devresi tasarlanmıştır ve tüm tasarım tasarım parçaları birleştirilmiştir. Birkaç tekrarlama ile giriş çıkış katı uyumlaması, PAE, kazanç ve çıkış gücü iyileştirilmiştir.

Tasarlanan devrenin elektromanyetik benzetimi yapılarak gerçek ortamda mikro şerit hatların karakteristik davranışları incelenmiş ve hat boyutlarında küçük ayarlamalar yapılmıştır. Çıkış gücü, kazanç, güç eklenmiş verimlilik ve ana işaretin ikinci ve üçüncü harmonik bileşenleri için son benzetimler yapılmıştır.

Yapılan benzetimler sonucu tasarlanan devrenin 3.3 GHz – 3.6 GHz bant aralığında 10W çıkış gücü, %55'ten daha yüksek güç eklenmiş kazanç, yaklaşık 19 dB doğrusal kazanç sağladığı görülmüştür. Elektromanyetik benzetimin ardından devrenin AWR tasarım programında serimi tamamlanmış ve üretime gönderilmiştir. Üretimin ardından devrenin montajı yapılmıştır.

Küçük işaret analizi ölçümleri Vektörel Network Analizörü ile yapılmıştır. Giriş yansımasının tasarımdan farklı olduğu görülmüş ve istenen frekans bandına taşımak için giriş hattı üzerine bakır bant eklenmiştir.

Çıkış gücü, kazanç ve yük eklenmiş verimlilik ölçümleri için kullanılan elemanların frekans ve güç bağımlı etkilerini ortadan kaldırmak adına ölçüm düzeneği oluşturuldu ve zayıflatıcı, kablo, konektör kayıpları için kalibrasyon yapıldı.

Yapılan ölçümler sonucu devrenin beklenen kazancı sağladığı gözlemlendi, ancak çıkış gücü 38-38.5 dBm, güç eklenmiş verimlilik %40 civarında ölçülmüştür. Aradaki farkın transistorun çıkış empedansının tasarımda ve gerçekteki farklılıktan kaynaklanabileceği belirlendi ve çıkış katı empedans uyumlama elemanlarının farklı değerler ile değiştirilerek ölçüm sonuçlarının önceki sonuçlarla karşılaştırılması ve daha iyi bir çıkış empedans noktası bulunmasına karar verildi.

1. INTRODUCTION

The need for communication has been one of the foremost human needs throughout history. This need increased tremendously with the growth in population year by year. Starting with telegram followed by the invention of cable phone was revolution for the transferring data/message from point to point. As a result of the studies on wireless data transfer with radio frequencies, first wireless transfer is achieved at the end of 19th century. Studies on wireless data transfer continued and developed exponentially with tens of milestones [1].

Studies on communication systems brought us today with very complicated transceiver systems. A typical superheterodyne transceiver system is given in Figure 1.1 [2]. In modern transceiver systems, receiver and transmitter are implemented together with a single antenna.

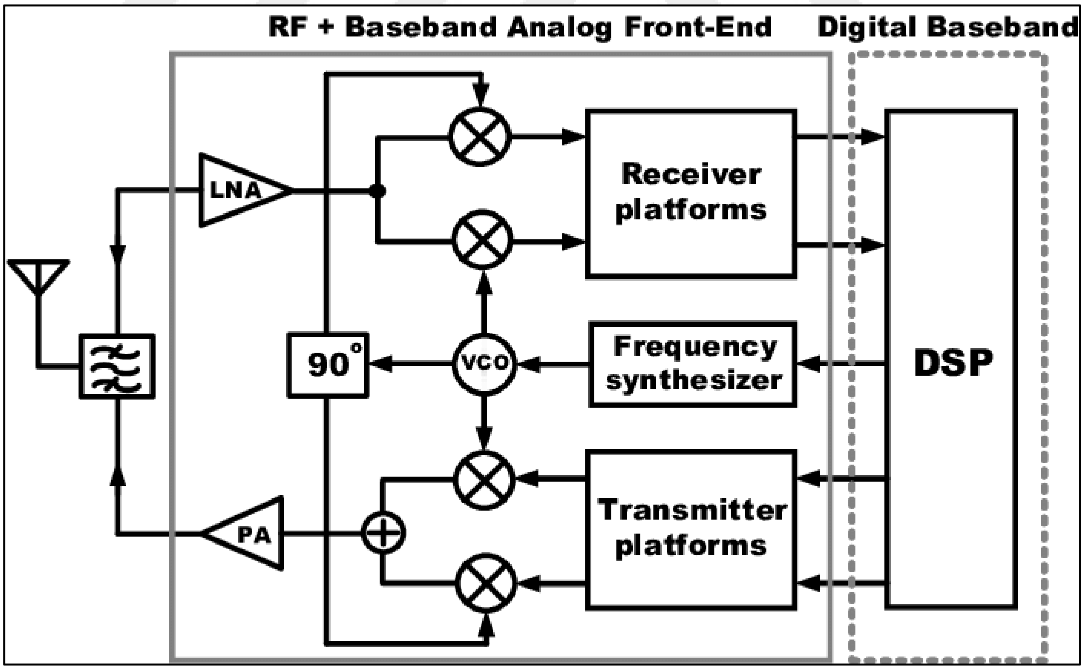

Figure 1.1: Typical superheterodyne tranceiver structure.

This study will be focusing on the power amplifier part of the given heterodyne transceiver system. Throughout this study, fundamentals of power amplifiers, power amplifier classes will be shared. After going over theoretical information, GaN Based

Class AB Power Amplifier design steps will be studied, and measurement results of manufactured circuit will be shared and compared with the simulation.

1.1 Power Amplifier Fundamentals

Power amplifiers are the last element in a transmitter system just before the antenna. As being the last active element, they need to handle the highest power in the system. Like all other electronic components and circuit blocks, there are certain comparison parameters for power amplifiers. Fundamental parameters to define a power amplifier are gain, output power, efficiency, and P1dB.

Gain of an amplifier is defined as the measure of how much input signal is amplified and presented at the output of the amplifier. It is the ratio of output amplitude to input amplitude as given in equation (1.1). Considering the power amplifiers, it is more common to talk in logarithmic scale. Giving input power and output power in logarithmic scale, gain of the amplifier is the difference between output power and input power as given in equation (2.2).

$$\mathbf{G} = \frac{\mathbf{V_{out}}}{\mathbf{V_{in}}} \tag{1. 1}$$

$$\mathbf{P_G} = \frac{\mathbf{P_{out}}}{\mathbf{P_{in}}} \tag{1. 2}$$

Output power is another important parameter to define a power amplifier. Transmitter systems require wide range of output power for a specific application ranging from a few milliwatts to tens-hundreds of watts. Selecting the right power transistor which can handle the required output power is important.

Like every other electronic component, power amplifiers consume DC power. Comparing with other electronic circuit components, power consumption of power amplifiers is usually the highest consumption in a communication system since they are the one handling the highest signal power in the system. Efficiency of power amplifiers are defined as the ratio of their output power to their DC power consumption which is also called Drain Efficiency. DC power consumption is the multiplication of DC current that drawn from the source and supply voltage as given in equation (1.3)

$$\mathbf{P_{DC}} = \mathbf{I_{DD}} * \mathbf{V_{DD}} \tag{1. 3}$$

Efficiency of a power amplifier is defined as the ratio of its output power and DC power consumption as given in equation (1.4)

$$\eta = \frac{P_{out}}{P_{DC}} \tag{1.4}$$

Since the power amplifiers are mostly defined with high input and output power, input power become considerably high in most of the cases and should be accounted in the efficiency calculation. More common efficiency definition for power amplifiers which subtract the input power is called Power Added Efficiency and defined as given in equation (1.5). The difference between the consumed DC power and delivered output power is dissipated as heat.

$$\eta_{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} \tag{1.5}$$

Gain of the transistor is defined as the ratio of output and input signal power amplitude. In ideal, as input is increased output is expected to increase linearly and gain should be constant for all input power levels. However, this is not possible in practice due to the current capability of the transistor and other non-linear effects. Output power will begin to saturate even if input power is increased linearly, consequently gain will begin to fall. The point where output power is saturated to 1 dB lower than its ideal value for a given input power is called 1 dB Compression Point and interpreted in Figure 1.2[3].

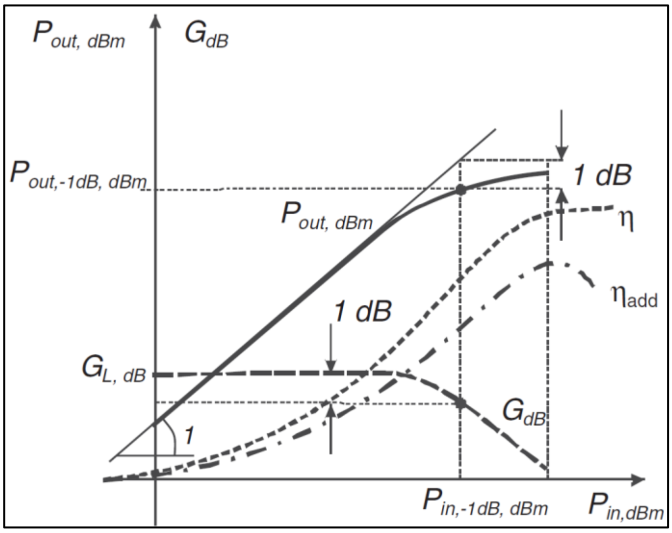

Figure 1.2: 1 dB compression point.

1.2 Gallium Nitride

First silicon transistor is developed in 1944 in Bell Laboratories and made a breakthrough in electronics. As a better solution for high frequency electronics, GaAs (Gallium Arsenide) transistor is developed in 1961. Even if operating frequency and output power of the Si and GaAs transistors were developed in years, their output capacitances and breakdown voltages are the main restrictions of them to be widely used in the applications which require high output power [4].

Consequently, first GaN (Gallium Nitride) transistor was developed in 2004 and in a short time it become a key player in the high-power RF applications [4].

Gallium Nitride (GaN) is a chemical compound of gallium from group 3A and nitrogen from group 5A. Gallium Nitride is a very popular semiconductor device in electronics and its popularity increases day by day in different applications such as optoelectronics, high power switches, high frequency/high power amplifiers [5].

Bandgap voltage is defined as the required amount of energy to move a valance band electron to conduction band. GaN is called wide bandgap semiconductor with its bandgap of 3.4 eV. Comparing with GaAs which has bandgap of 1.4 eV and silicon which has bandgap of 1.1 eV, more energy is required to excite an electron in valance band to conduction band in GaN [5].

Gallium nitride is grown in high temperature with different techniques on various substrates. Silicon Carbide (SiC) is the most common substrate used in development of GaN devices with its very good thermal conductivity. GaN on SiC devices provides very good both RF and thermal performance on power applications with the combination of high-power density of GaN and thermal conductivity of SiC [5].

The reason of GaN on SiC substrate devices being very good in high power RF applications can be investigated with their three main properties [5].

- Breakdown Voltage: As it is indicated above, GaN devices have large bandgap 3.4 eV. This feature makes GaN devices to have high breakdown voltages comparing with other semiconductor devices. Under high electric field chemical bonds can be broken and this phenomenon called impact ionization. Thanks to their wide bandgap GaN devices can operate at high voltages without degradation.

• Saturation Velocity: The speed of electrons in GaN devices under high electric fields are very high comparing with other semiconductors. Having high saturation velocity provides higher current values under same electric field comparing with a semiconductor having lower saturation velocity. This provides that GaN devices can provide same current in a smaller area. Combining high breakdown voltage and high current density, it can be concluded that GaN devices have high power density than other semiconductor devices.

• Thermal Conductivity: Thanks to the outstanding thermal conductivity of SiC substate, GaN on SiC devices can work on high powers and temperatures. Dissipated power on device is converter into heat and this makes the device to get hotter. High thermal conductivity of SiC substrate enables the removal of heat from the device and keeps the device cool.

All these features enable GaN to be most appropriate semiconductor for high frequency high power applications. Comparison of different semiconductors for their operating frequency and power level is given in Figure 1.3 [6].

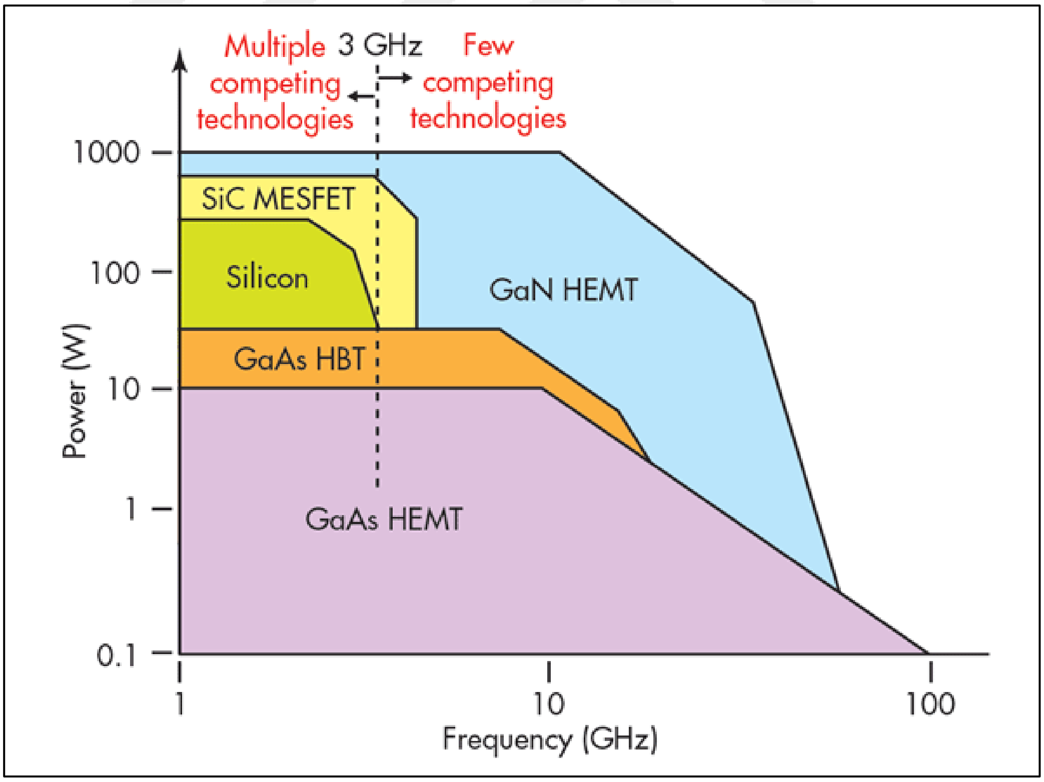

Figure 1.3: Performance comparison of different semiconductors.

1.3 5G New Radio

As it is experienced by everyone, the need for more and faster data transfer has increased tremendously. Today we cannot wait while a video or a webpage is loading, whereas it was more than enough to hear a few kilobytes of voice around 40 years ago. Wireless communication technology also changed and developed over the years to keep up with this need. Before going into details of the fifth generation of mobile communication system, it would be good to go over the preceding generations and see the development through the years.

First generation is firstly introduced in early 1980s. It was using analog modulation and it allows only voice transfer. As a result of analog modulation and no encryption, anyone can interfere to the communication. With a channel bandwidth of 30 kHz, quality and capacity was very poor [7].

Second generation was a big development over the first generation consisting of digital system and was introduced in 1990s. Data services is provided in 2G along with the voice, but it was very limited. Second generation is improved with GPRS having 150 Kbps and and EDGE having 384 Kbps. GPRS and EDGE is known as the transition from 2G to 3G [7].

Third generation introduced in 2000s and aim was to improve voice services, data throughput and high quality of service. With the increase in data transfer rate up to 2 Mbps, SMS, MMS, video conferencing were become available and the noise problem in first and second generation was highly improved [7].

Fourth generation was launched in 2010 with important improvements comparing with third generation. Most important change of fourth generation is that core network and switching type is internet. Peak data rate reaches up to 1Gbps and it uses spectrum more efficiently comparing with preceding generations [7].

Although 4G provides very good performance, high handoff speed, MIMO technology, HD voice, global roaming and so on, it is not sufficient for future applications. Fifth generation is introduced as solution to higher data rate, higher capacity, wider coverage and most importantly to decrease latency [7].

Peak data rate of 5G is more than 20 Gbps and average data rate is more than 100 Mbps. Core network is enhanced comparing with fourth generation and based on internet and cloud computing [8].

Latency is expected to be less than 1 ms which was 10 ms in fourth generation. User capacity will be 100 times higher than fourth generation which will increase the numbers of connected wearable devices and IoT devices. With the wide usage of fifth generation, faster speed for much more user with more efficient and reliable communication will be available. The number and variety of the connected devices will increase, and everything will become “smart”. Cloud computing, telemedicine, virtual reality, 4k streaming, real-time full HD video calls, smart transportation, drone delivery, car-to-car communication and much more will be the features and applications that will be widely used with 5G [7][8].

Comparison table from 1G to 5G is given in Table 1. 1 [9].

Table 1. 1: 1G to 5G Technology Comparison

Technology	1G	2G/2.5G	3G	4G	5G
Bandwidth	2 kbps	14-64 kbps	2 Mbps	200 Mbps	>1 Gbps
Technology	Analog cellular	Digital cellular	Broadbandwidth/ CDMA/ IP Technology	Unified IP and seamless combo of LAN/WAN/WLAN	4G+WWWW
Service	Mobile telephony	Digital voice, short messaging	Integrated high quality audio, video, and data	Dynamic information access, variable devices	Dynamic information access, variable devices with AI
Multiplexing	FDMA	TDMA/CDMA	CDMA	CDMA	CDMA
Switching	Circuit	Circuit/circuit for access network and air interface	Packet except air interface	All packet	All packet
Core Network	PSTN	PSTN	Packet Network	Internet	Internet
Handoff	Horizontal	Horizontal	Horizontal	Horizontal& Vertical	Horizontal& Vertical

5G is designed to use existing frequency spectrum below 6 GHz at early stages. To improve channel bandwidth and speed mentioned above, 5G will use cmWave (6-30 GHz) and mmWave (30-300) GHz frequency band [8].

The aim of this study is to design a power amplifier for 5G sub-6 GHz applications centered around 3.5 GHz.

2. POWER AMPLIFIER CLASSES

Power amplifier is a system component which is designed to increase the power level of an input signal for a specific frequency range and deliver a certain output power [3]. Power amplifiers are the last element on a transmitter circuitry before the antenna. So, they have to handle the highest power in a transmitter system. Comparing with the rest of the transmitter components, they are the one which holds a great percentage on the systems overall DC power consumption. Delivering high output power along with the low DC power consumption is the key point of power amplifiers. [10]

High output power requirement of the power amplifiers differs them from the traditional small signal amplifiers. Small signal amplifiers can be design with traditional amplifier design techniques since they are working in the linear region of the transistor. However, power amplifiers work with relatively high input power and output power, so their operating region is mostly non-linear and non-linear effects of the transistor itself become significantly important. In this manner, traditional small signal amplifier design techniques do not apply for power amplifier design [11].

Power amplifiers can be divided into two main category as current source or linear and switching power amplifiers. Current source amplifiers are divided into sub-classes as Class A, Class B, Class AB, and Class C. Classification is determined according to the bias point of the transistor. Gate bias point determines the conduction angle of the transistor and decreases from Class A to Class C. Details of each class will be discussed in following sections. Switching type amplifiers is classified as Class D, Class E, Class G, Class H and Class S. There is also another class called Class F which lies between current source and switching type [3]. Since the purpose of this study is to design a Class AB power amplifier, only details of current source type power amplifiers will be investigated deeply.

Current source amplifiers are driven with sinewave inputs and output signal is a relatively linear function of the input signal. Bias point selection determines the transistors conduction interval. Transistor can conduct current full cycle, half cycle, more than half cycle or lower than half cycle as it is given in Table 1. 2 [3]. Output current waveform of different classes are also given graphically in Figure 2. 1 [3].

Table 1. 2: Comparison of power amplifier operating classes.

Operating Class	Current Conduction Angle	Drive Level Dependence	Bias
Class A	2 π (360°)	No	Middle of Pinch-off and Saturation
Class B	π (180°)	No	Pinch-off
Class AB	> π (180°)	Yes	Above Pinch-off
Class C	< π (180°)	Yes	Below Pinch-off

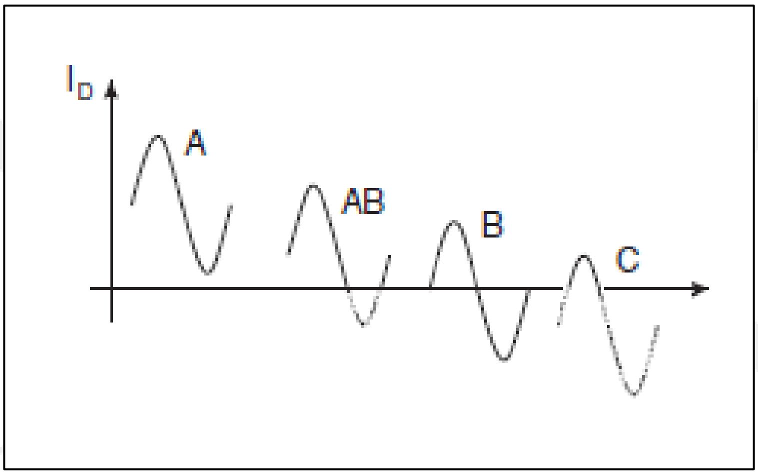

Figure 2. 1: Current waveforms comparison of power amplifier classes.

2.1 Class A Power Amplifiers

Gate bias of Class A amplifiers are selected as the mid-point of transistor saturation voltage and cut-off voltage. By doing so, linear output current is provided between its minimum and maximum values.

A typical Class A power amplifier is given in Figure 2.2 [12].

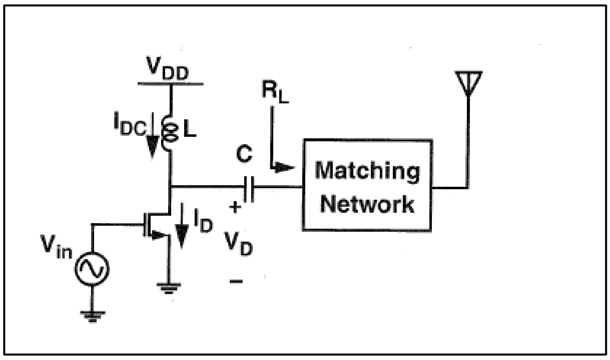

Figure 2. 2: Typical class a power amplifier.

As it can be seen from Figure 2. 1, quiescent current of Class A power amplifiers are high regardless of input and they consume DC power continuously which makes them to have low efficiency.

Maximum output power of a Class A amplifier is given in equation 2.1 and corresponding maximum drain efficiency is 50% as given in equation 2.2.

$$P_{OUT} = \frac{{V_{DD}}^2}{2*R_{OPT}} \tag{2.1}$$

$$\eta = 100 * \frac{P_{OUT}}{P_{DC}} = 100 * \frac{\frac{{V_{DD}}^2}{2*R_{OPT}}}{V_{DD}*I_{DC}} = 100* \frac{V_{DD}*I_{DD}}{2*V_{DD}*I_{DC}} = 50\% \tag{2.2}$$

theoretical 50% drain efficiency is hard to achieve and in practice Class A power amplifiers have drain efficiency around 20%-30% and most of the power is dissipated as heat. Advantage of Class A amplifiers is to have highest linearity comparing with other power amplifier classes. As it will be investigated in other classes, there is always a trade of between efficiency and linearity, as efficiency increases, amplifier become less linear.

2.2 Class B Power Amplifiers

As it is stated, Class A amplifiers suffers from low efficiency as the current through and voltage across the drain overlaps for all cycle which means continuous power consumption. Class B power amplifiers are bias just at the pinch-off voltage, so there is no current flow in quiescent. Also, half cycle of a sinusoidal input signal puts the device into cut-off while drain is at the maximum value.

Class B amplifiers can be designed with two transistors such that one transistor is operational for the positive half cycle and the other is operational for the negative half cycle which is called push-pull configuration. Also, Class B power amplifiers can be designed with a single transistor and tuned with a narrow-band matching circuitry at their output and output voltage is the multiplication of load resistance and the fundamental component of drain current which has the maximum value of $\frac{2*V_{DD}}{R_L}$.

The current drawn from the source is the average of the current drawn in a half cycle and calculated in equation 2.3.

$$I_{DC} = i_{D,avg} = \int_0^T i_D(t)dt = \int_0^{\frac{T}{2}} \frac{2*V_{DD}}{R_L} * \sin(w_0 t)dt = \frac{2*V_{DD}}{\pi*R_L} \tag{2.3}$$

Since the maximum drain voltage is equal to VDD, maximum efficiency of Class B amplifiers is calculated as 78% as given in equation 2.4.

$$\eta = 100 * \frac{P_{OUT,max}}{P_{DC}} = 100 * \frac{\frac{{V_{DD}}^2}{2*R_L}}{V_{DD}*I_{DC}} = \frac{\pi}{4} = 78\% \qquad (2.4)$$

Changing bias point of the gate and making the transistor operational for only the half cycle decreases the DC power consumption in Class B power amplifiers and theoretical efficiency is increased from 50% to 78% comparing with the Class A amplifiers in exchange to decrease in amplifier linearity.

2.3 Class C Power Amplifiers

As it is seen in Class B amplifiers, efficiency of the amplifier can be improved with the decrease in the conduction angle which was 180°. Class C Power Amplifiers are the power amplifier class in which conduction angle is decreased below 180° to increase efficiency even further. In such configuration, the transistor conducts current only in a small portion of the whole cycle and power consumption is very low. Theoretical efficiency of Class C Power Amplifiers can go up to 100% as conduction angle approach to 0° and 78.5% as conduction angle approaches to 180°[10].
To shape the output waveform as a sinusoid from a non-sinusoidal current, narrowband tank at the operating frequency is formed at the output.

2.4 Class AB Power Amplifiers

Drain efficiency is increased with decreasing conduction angle and reached the maximum with Class C power amplifiers but Class C amplifiers suffer from the lack of linearity. Even if efficiency is very important linearity should also be maintained. At this point Class AB amplifier is the class of power amplifier where linearity and efficiency are achieved with reasonable compromise.
As the name implies, Class AB power amplifiers are biased at a point just above the pinch-off voltage and the conduction angle lies between 180° and 360°. Theoretical drain efficiency lies between Class A and Class B, 50% and %78.5 [10].
In the next section, design of a Class AB Power Design at frequency range of 3.3 GHz and 3.6 GHz will be evaluated. Simulation results will be shared and compared with measurement results.

3. CLASS AB POWER AMPLIFIER DESIGN

3.1 Design Goals

In this study, a GaN based Class AB power amplifier for the frequency range 3.3 GHz and 3.6 GHz will be designed. Design parameters are given in table 2.1. The power amplifier should deliver 40 dBm output power with a PAE greater than 50% at 3 dB compression point. The goal for the linear gain of the amplifier will be higher than 18 dB. Design goals are given in Table 3. 1.

Table 3. 1: Design goals of class ab power amplifier.

Operating Frequency Range	3.3 GHz – 3.6 GHz
Output Power	>40 dBm
PAE	>50%
Small Signal Gain	>18dB

Numbers of GaN transistors were evaluated for this design in terms of operating frequency, power handling, efficiency, availability, price, packaging. After transistor evaluation, QPD1009 GaN PHEMT transistor from Qorvo is selected for Class AB power amplifier design.

3.2 Transistor Properties

The Qorvo QPD1009 is a 15 W (P3dB) discrete GaN on SiC HEMT which operates from DC to 4 GHz. The device is constructed with Qorvo's proven QGaN25HV process, which features advanced field plate techniques to optimize power and efficiency at high drain bias operating conditions. This optimization can potentially lower system costs in terms of fewer amplifier line-ups and lower thermal management costs [13].

3.3 Bias Point Selection and Small Signal Analysis

Non-linear model of the device is provided by Modelithics Qorvo GaN Library. Library is imported into Cadence AWR Microwave Office. Ideal bias circuitry is created and given in Figure 3. 1. Drain bias is selected as 50V and gate voltage is swept as given in Figure 3. 2. Gate bias of -2.6 V is selected which provided 59.5 mA of quiescent drain current.

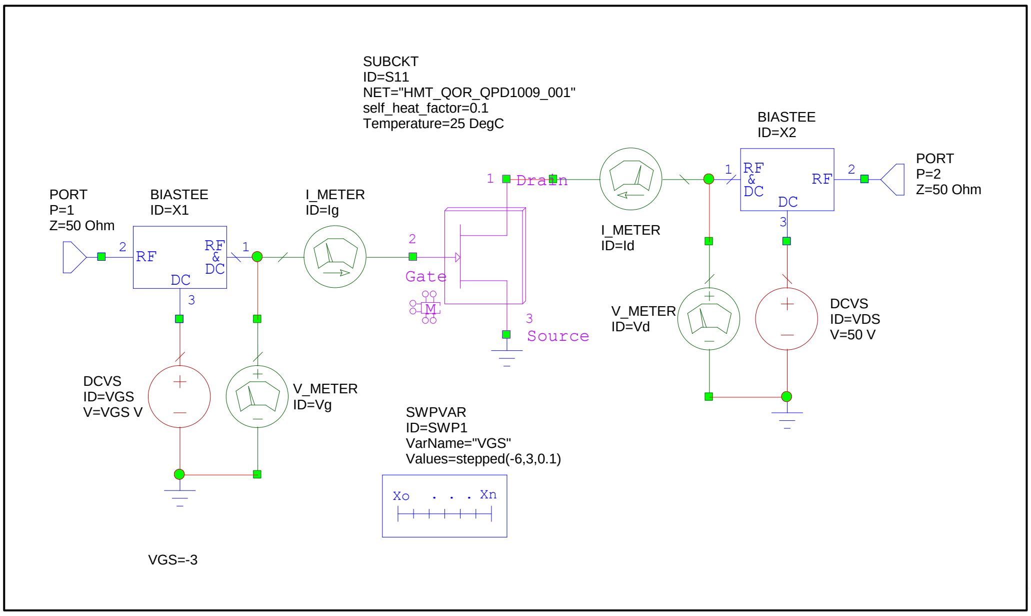

Figure 3. 1: Ideal bias circuit.

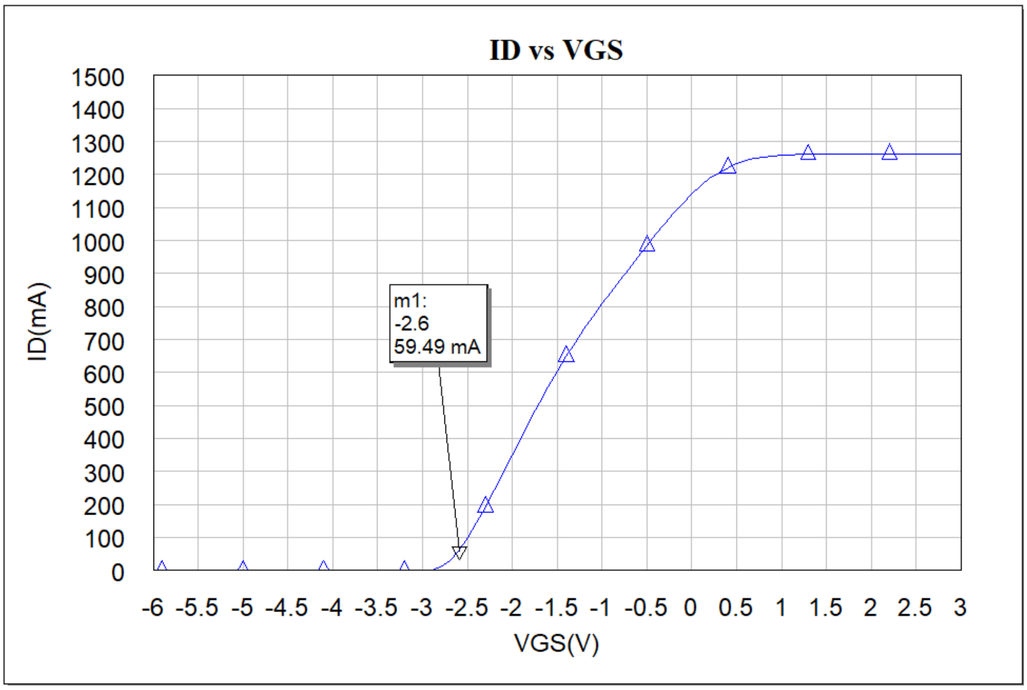

Figure 3. 2: ID vs VGS curve and selected bias point.

Small signal parameters of ideally biased, unmatched transistor is given in Figure 3. 3.

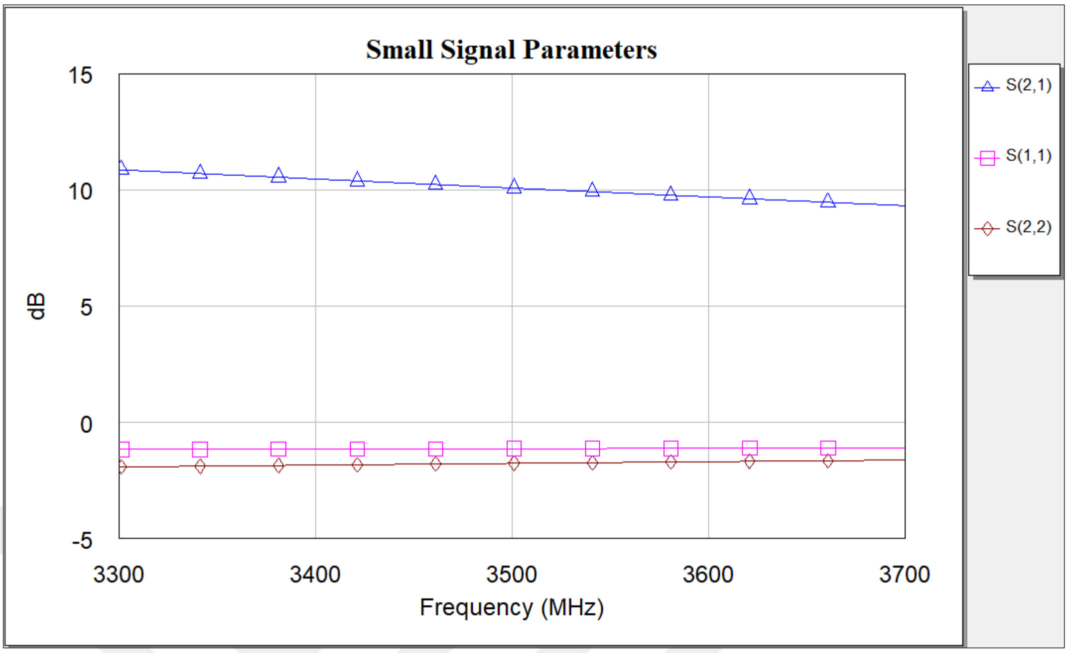

Figure 3. 3: Small signal parameters of unmatched, ideally biased transistor.

First step before starting the design is to stabilize the amplifier for a wide frequency range. Output and input stability circles of ideally biased transistor are given in Figure 3. 4 and Figure 3. 5, respectively.

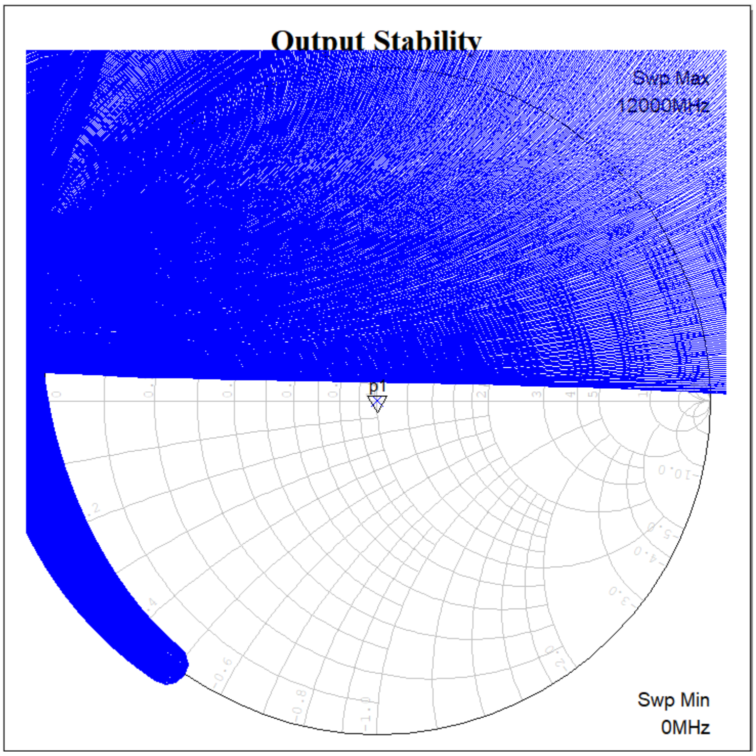

Figure 3. 4: Output stability circles.

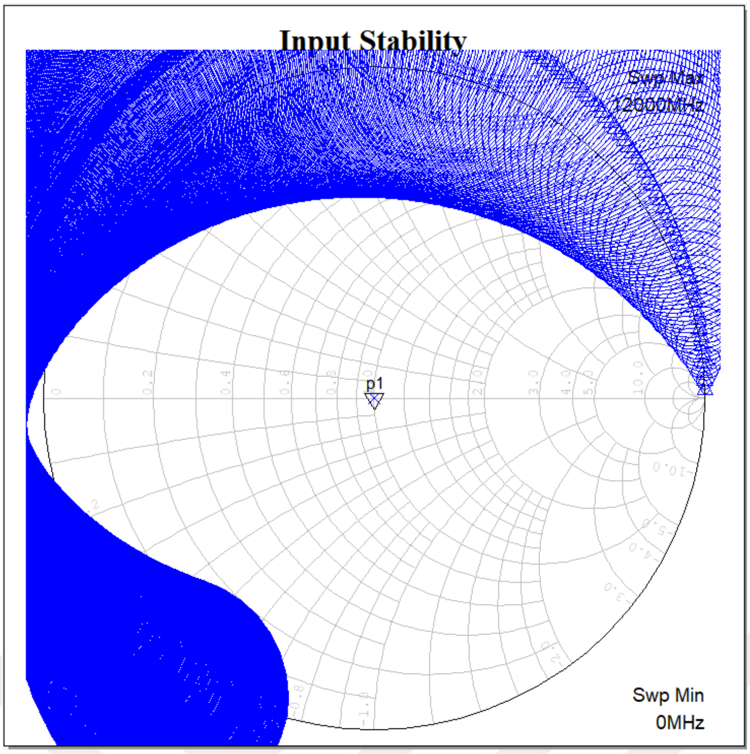

Figure 3. 5: Input stability circles.

3.4 Load Pull Setup

Device should be evaluated under different load and source impedances and output power, PAE and gain should be determined with each source and load impedance. Load-pull provides to sweep load and source impedance for a defined frequency and creates contours for the desired parameter, PAE, gain and output power. Selection of the load point is a compromise between power and efficiency such that if load point which gives the highest PAE is selected output power would be lower than the maximum. In same manner, if load point which gives the maximum output power is selected, PAE would be lower than its maximum value. The key point is to find a load impedance point which satisfies all the design goals determined beforehand.

To define the load and source impedance points, ideal load pull setup is created as given in Figure 3. 6. Load-pull analysis is an iterative analysis such that it should be carried out a few times to find the best impedance points.

Also, it should be kept in mind that the values taken with load-pull analysis are the ideal values which does not include any loss of any circuit element. Real circuit elements such as transmission lines and lumped elements are lossy and degrades the results taken from the load-pull analysis. Also, it is very unlikely to realize certain impedance values for different frequencies with designed input and output circuitry.

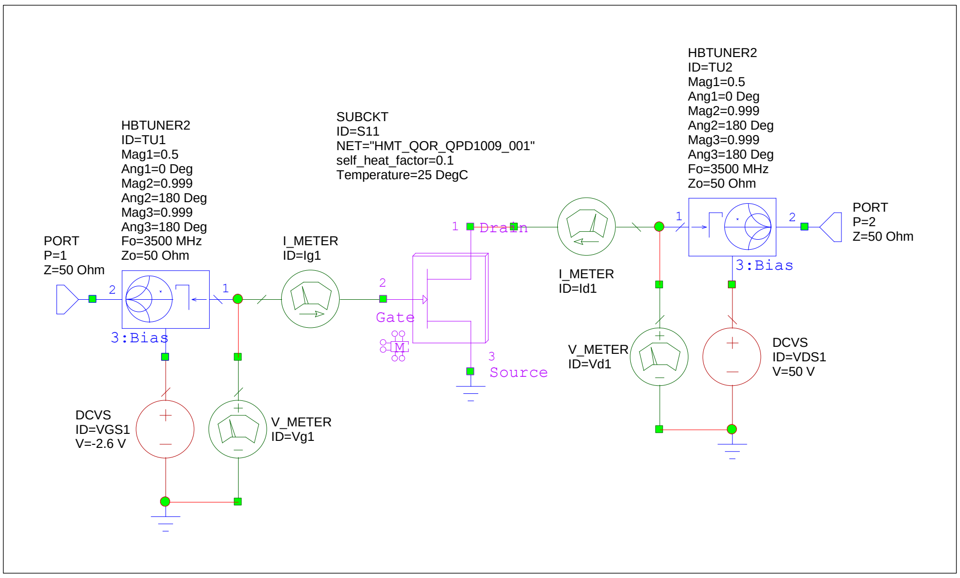

Figure 3. 6: Simulation setup for load-pull analysis.

The key point is to design optimum input and output circuitry which satisfies PAE, gain and output power for whole frequency range. Gain, PAE and output power contours for 3.3 GHz, 3.4 GHz, 3.5 GHz, and 3.6 GHz at 3 dB compression point are given in Figure 3. 7, Figure 3. 8, Figure 3. 9, and Figure 3. 10, respectively.

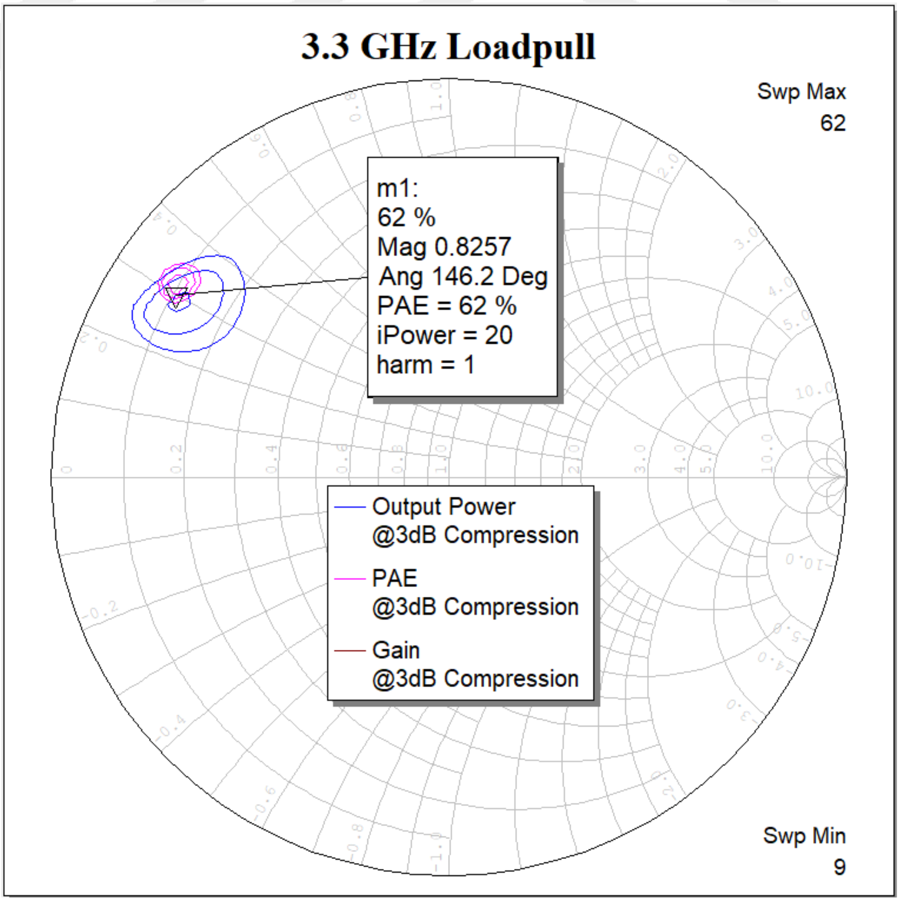

Figure 3. 7: Load-pull contours for 3.3 GHz.

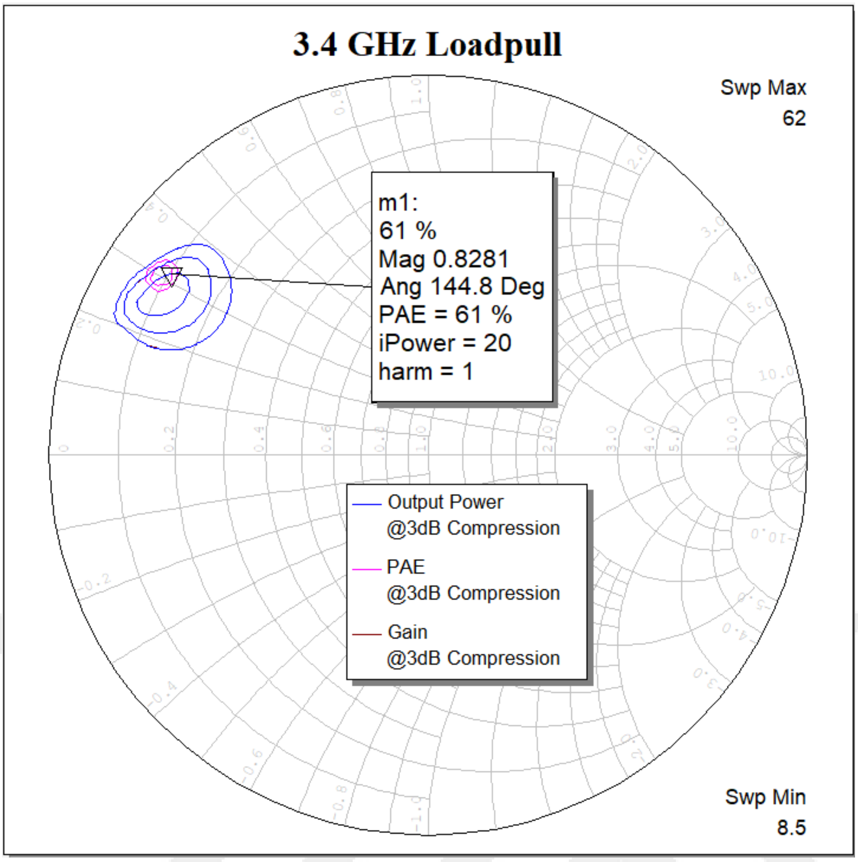

Figure 3. 8: Load-Pull contours for 3.4 GHz.

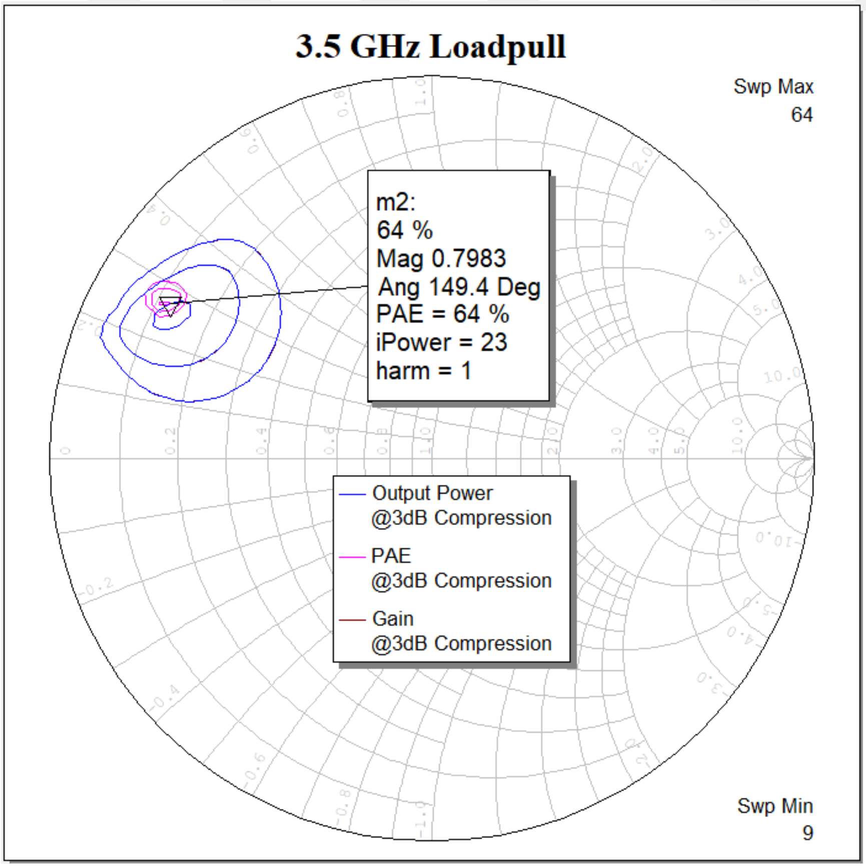

Figure 3. 9: Load-Pull contours for 3.5 GHz.

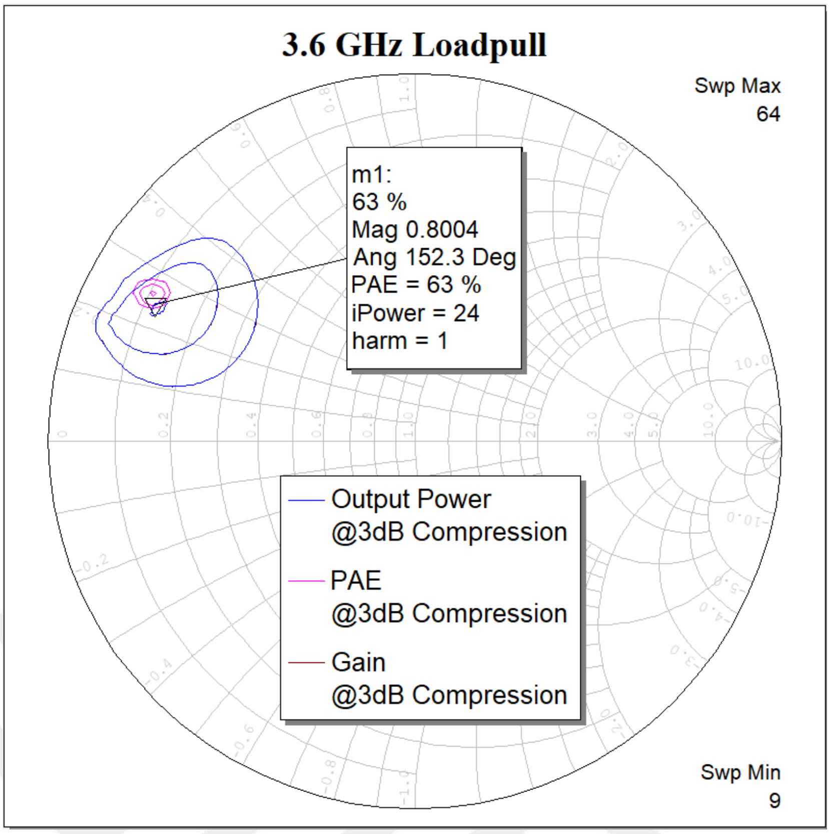

Figure 3. 10: Load-Pull contours for 3.6 GHz.

3.5 Output Circuit Design

Output load points for different frequencies satisfying the design specifications are determined with load-pull analysis in Section 2.4. Loadpull analysis is done with ideal HBTUNER element which only helps to find load impedance ideally. Now, determined output load points for 3.3 GHz to 3.6 GHz should be realized with real circuit elements. The purpose here is to design output circuitry that show determined load impedance to the transistor output. However, bias circuitry must also be designed. HBTUNER elements provides DC voltage to device ideally such that there is no RF leakage from device to supply, in other words it shows infinite impedance ideally, so there is no loss from the output power through supply line.

It is needed to design a bias line that shows high (ideally infinite) impedance in operating frequency comparing with output impedance. If bias line impedance is comparable with output impedance, there would be RF leakage through supply circuitry to ground, which decreases the output power that can be got from the amplifier.

Determined load reflection points are gathered with ideal HBTUNER element as given in Figure 3. 11 and corresponding impedance points are shown on Smith Chart as given in Figure 3. 12 .

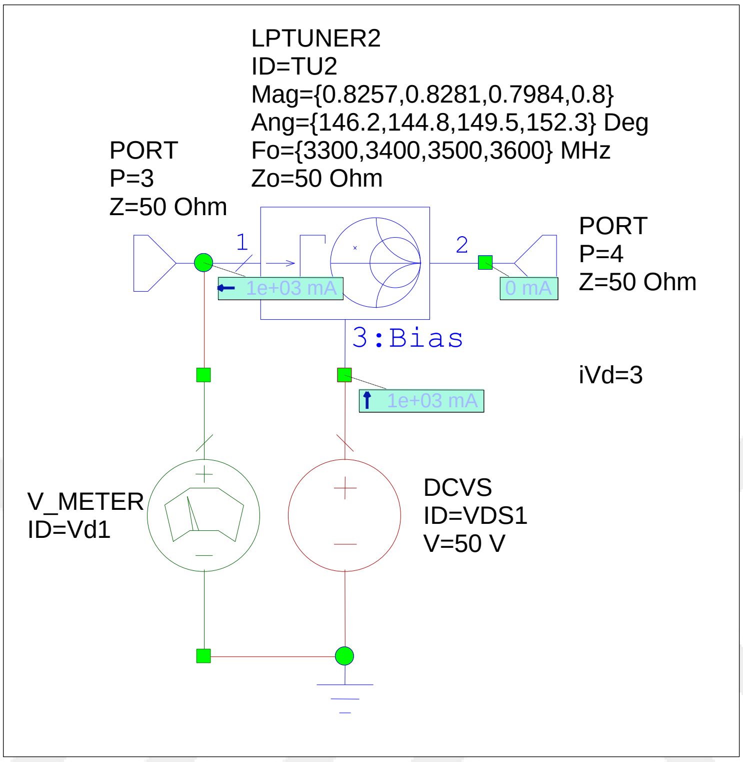

Figure 3. 11: HBTUNER element with ideal load reflection values.

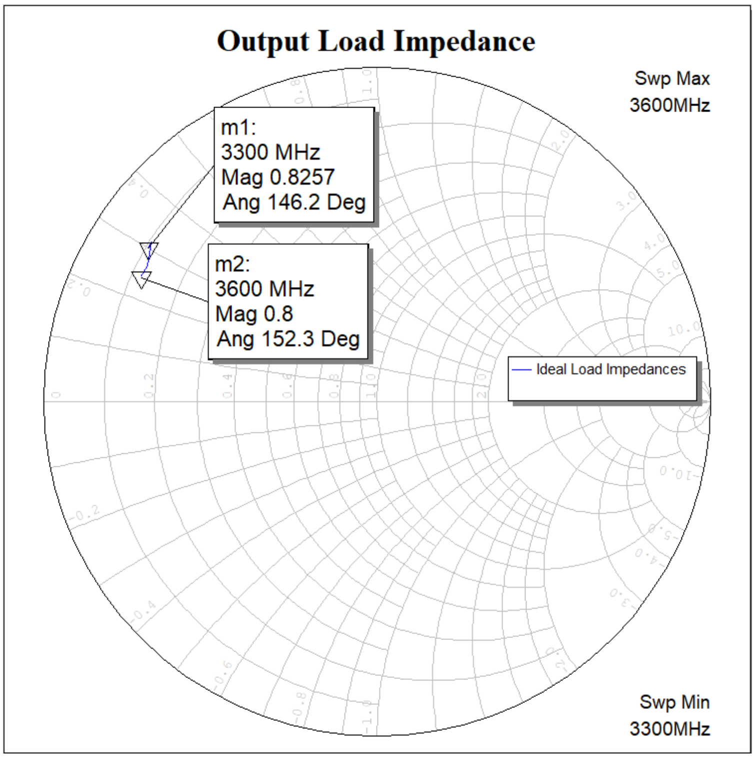

Figure 3. 12: Impedance points of designed output circuit.

Aim was to provide the desired load impedance points seen by transistor at the output. Output matching network and bias circuitry is designed together which provides the load impedance values for determined power added efficiency values. Designed wideband matching network is given in Figure 3. 13 .As given in Figure 3. 14, designed output circuitry provides close impedance points comparing with the ideal case.

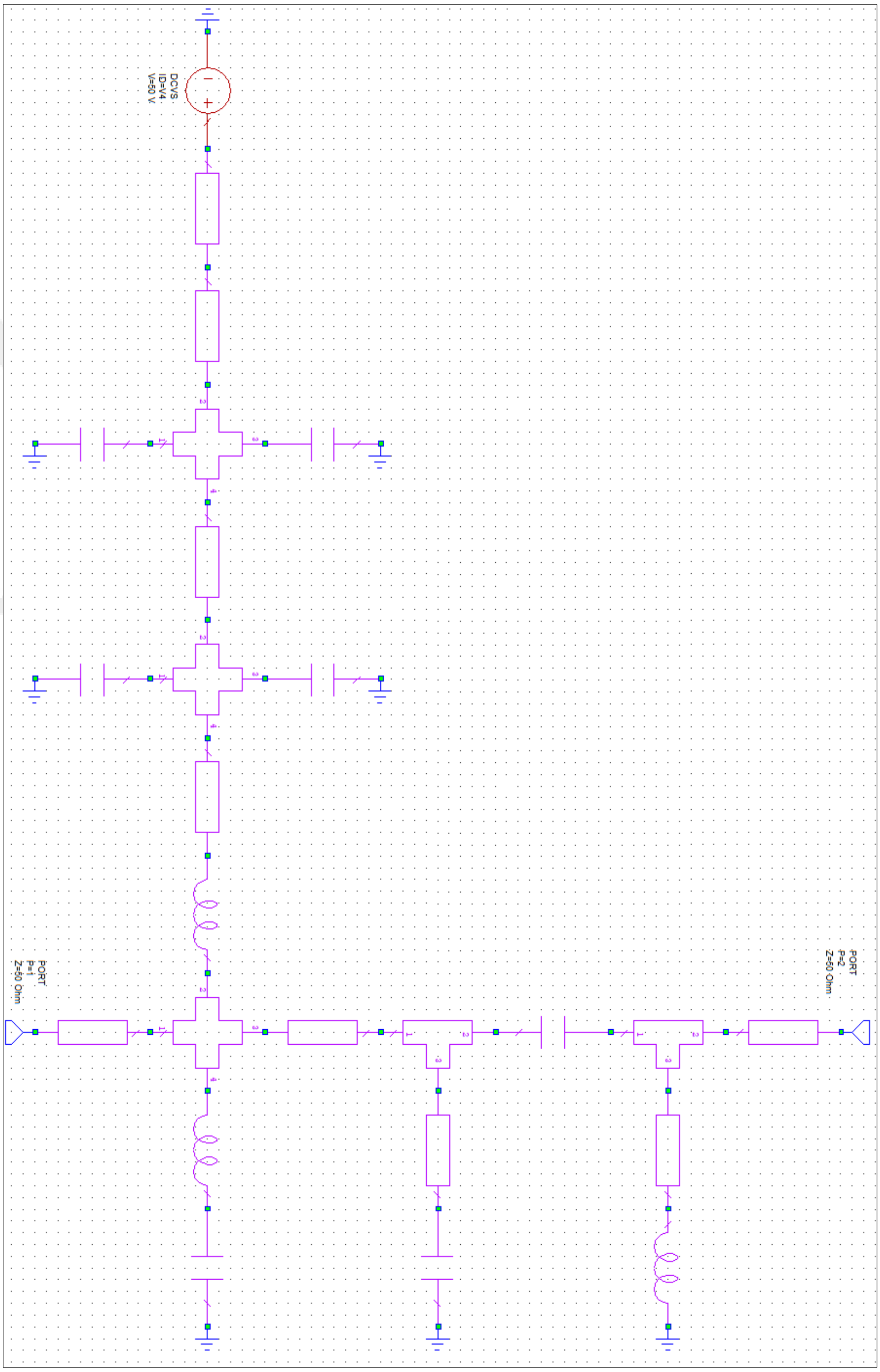

Figure 3. 13: Designed Output Circuit

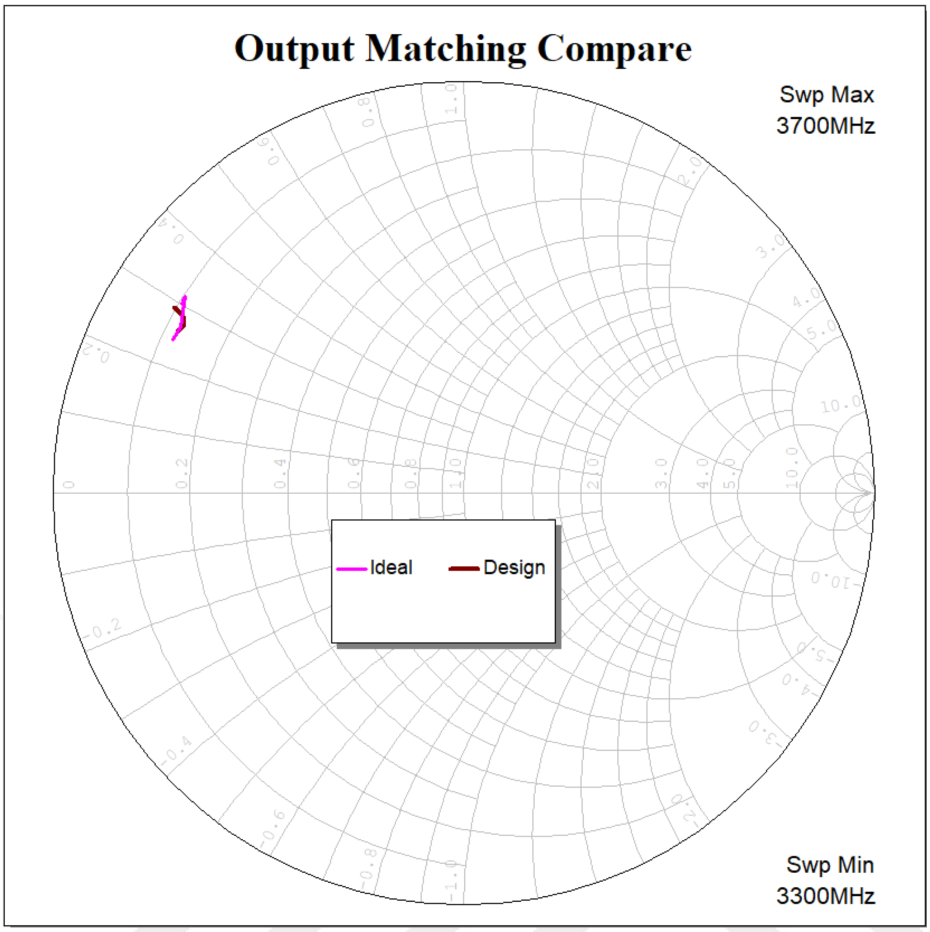

Figure 3. 14: Load impedance comparison of ideal and designed output.

3.6 Input Circuit Design

After completing output matching circuit design, next step is to design input gate bias circuit and matching circuit. Gate bias line is included into input matching network. The purpose here is to achieve high impedance on bias line and to provide wide-band input matching which provides <-10 dB reflection for entire operation frequency.

Other important point of input bias and matching network design is stability. As it is given in Figure 3. 4 and Figure 3. 5 , amplifier was not stable at the beginning of design for selected Class AB operation point. There are different ways to satisfy the stability of amplifier. Series resistor on gate bias line and main RF line is one way which is selected for this design as given in Figure 3. 15 .

Series resistor on main line helps to provide stability but it effectively decreases the gain which is not desired. To mitigate gain issue, a capacitor is added in parallel with the resistor which provides low impedance path for the signal on operating frequency while blocking low frequency signal and improve stability [14]

Designed input circuitry is given in Figure 3. 16 .

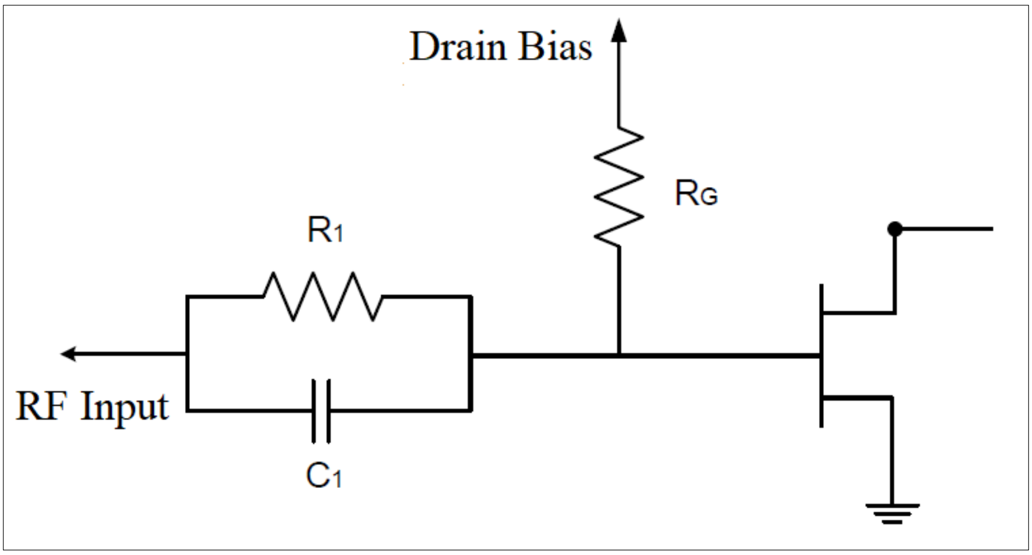

Figure 3. 15: Resistors on input matching for amplifier stabilization.

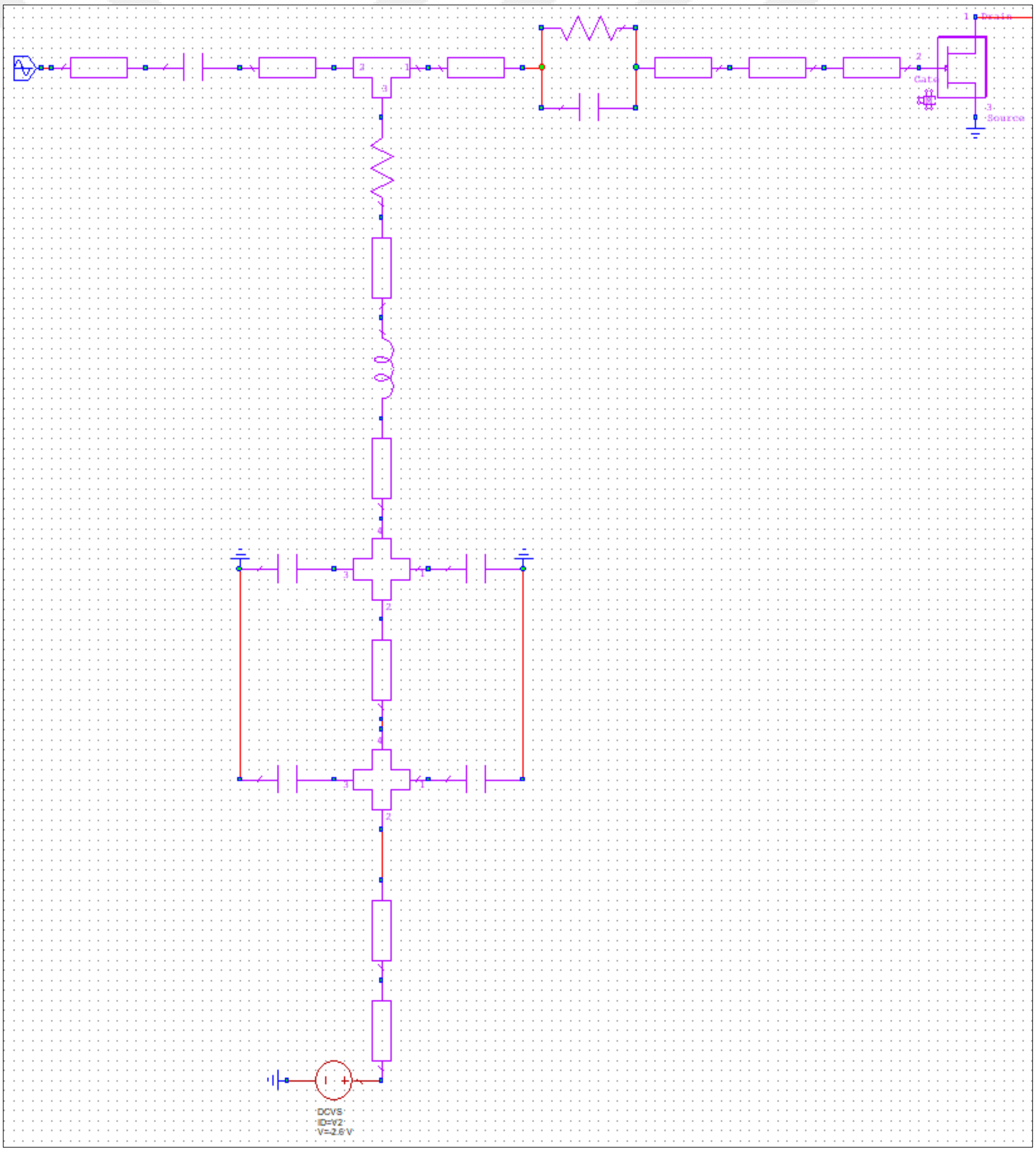

Figure 3. 16: Designed input circuit.

3.7 EM Simulation and Results

Output circuitry is designed for determined load points to provide high power efficiency and output power with high linear gain. Input circuitry is designed to provide wide band matching which provides low return loss.

Next step is to conduct electromagnetic simulation to get simulation results which reflects real behavior of used microstrip lines, discontinuities, trace loses. EM simulation results is expected to be more consistent with real measurement results.

EM EXCRAT element in AWR is used to extract electromagnetic layout of the designed circuitry. EXTRACT element determines electromagnetic ports between selected microstrip lines and creates the environment that is defined with substrate parameters. The layout that will be used in EM simulation is given in Figure 3. 17.

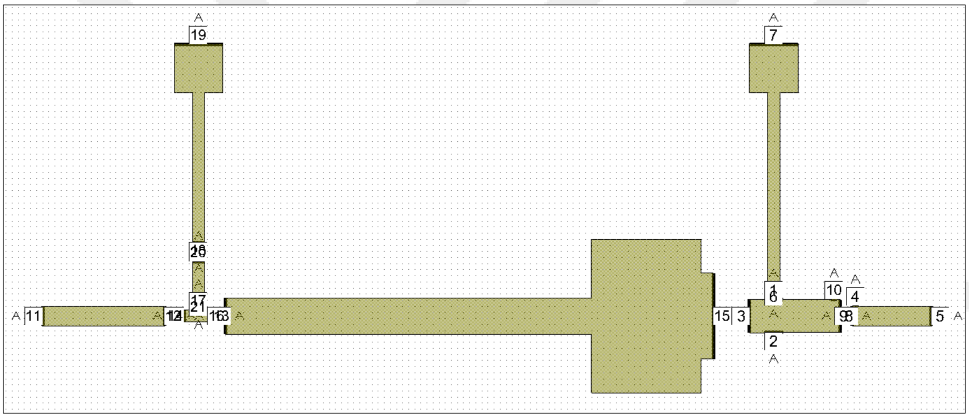

Figure 3. 17: Layout and port allocation of layout used for em simulation.

Small signal parameter simulation results ares given in Figure 3. 18 which satisfy design goals.

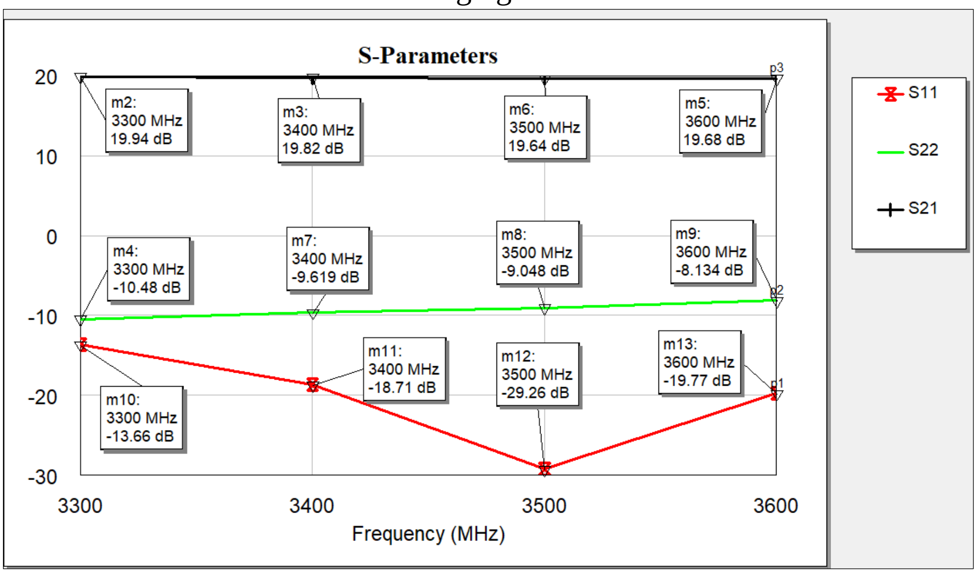

Figure 3. 18: S parameters of designed amplifier.

Complete circuit schematic of the dedigned Class AB power amplifier is provided in Figure 3. 19 .

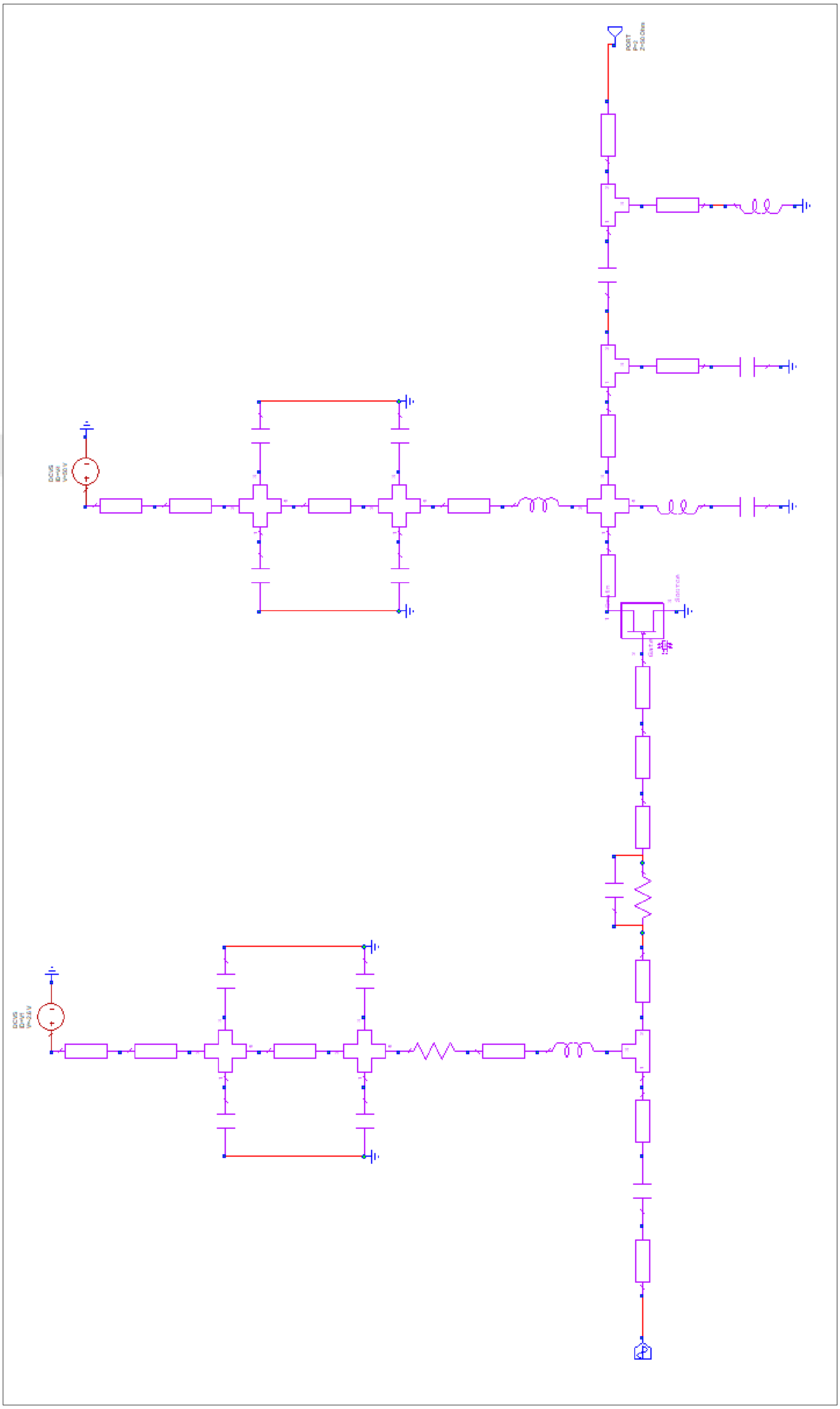

Figure 3. 19: Complete amplifier schematic.

Simulation results of electromagnetic simulation are evaluated and compared with the initial design goals and provided in Figure 20, Figure 21, Figure 22, 23, Figure 24 and Figure 25.

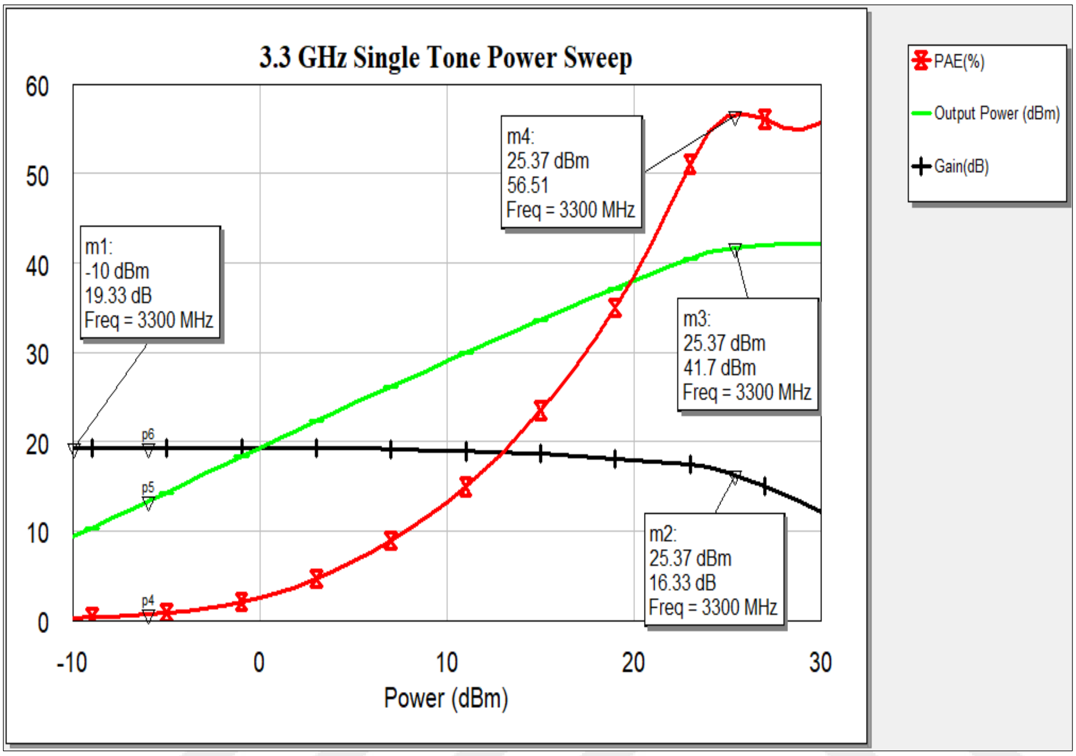

Figure 3. 20: Power sweep for 3.3 GHz, PAE, gain and output power values.

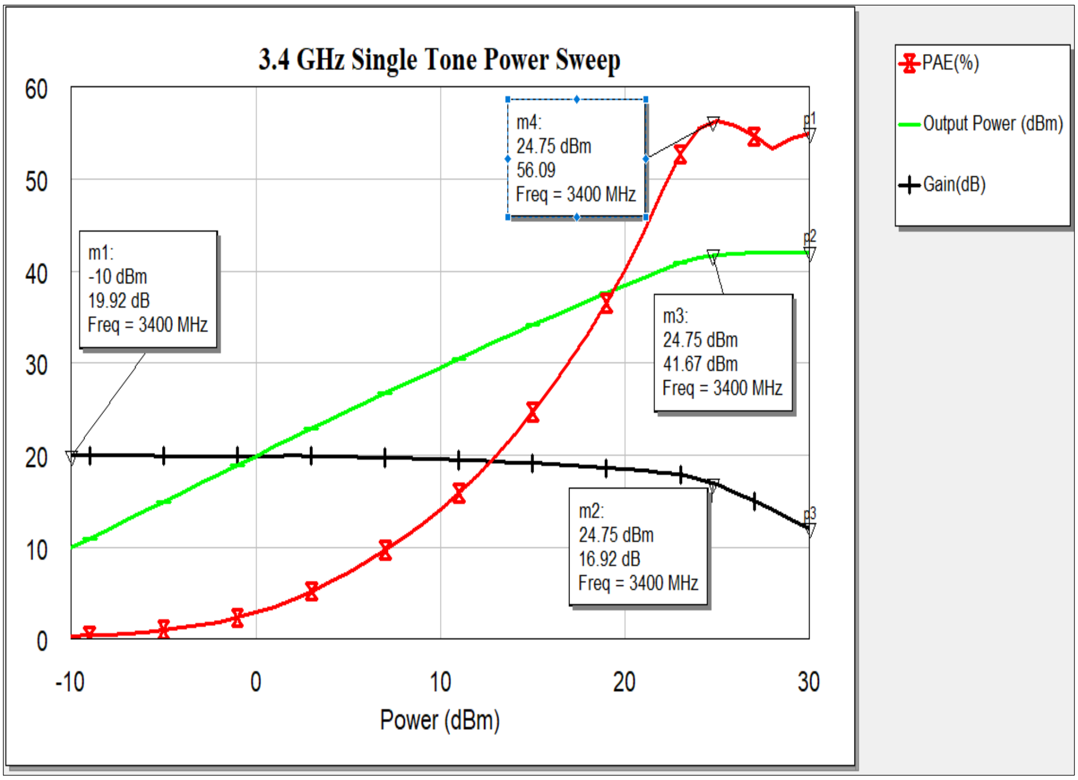

Figure 3. 21: Power sweep for 3.4 GHz, PAE, gain and output power values.

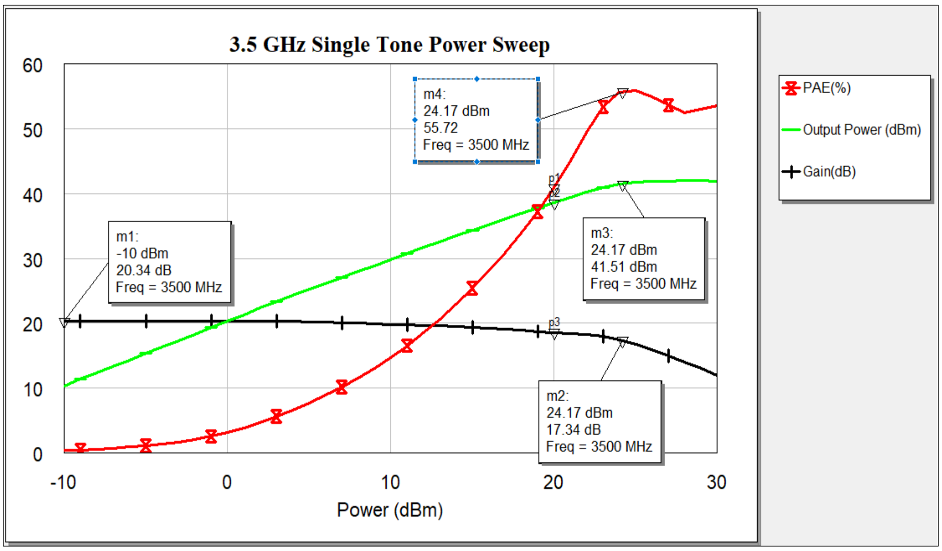

Figure 3. 22: Power sweep for 3.5 GHz, PAE, gain and output power values.

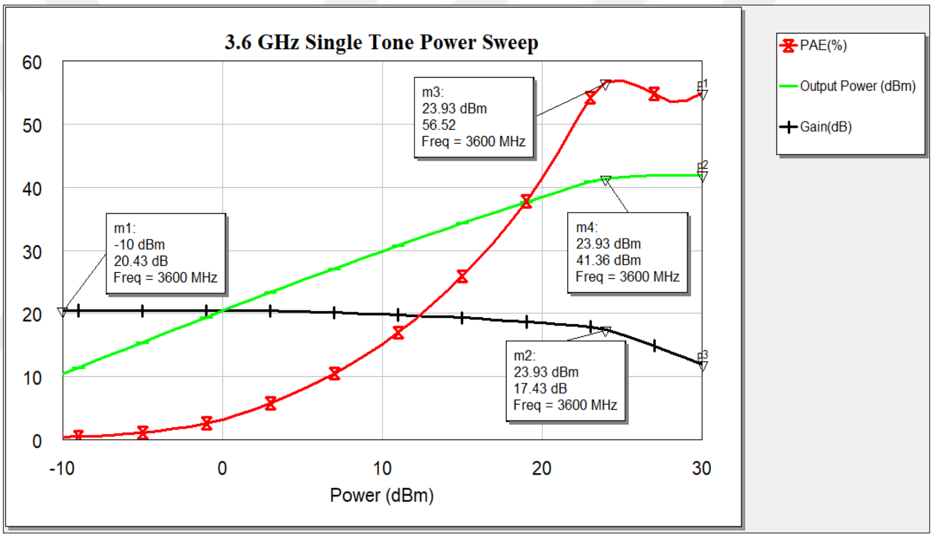

Figure 3. 23: Power sweep for 3.6 GHz, PAE, gain and output power values.

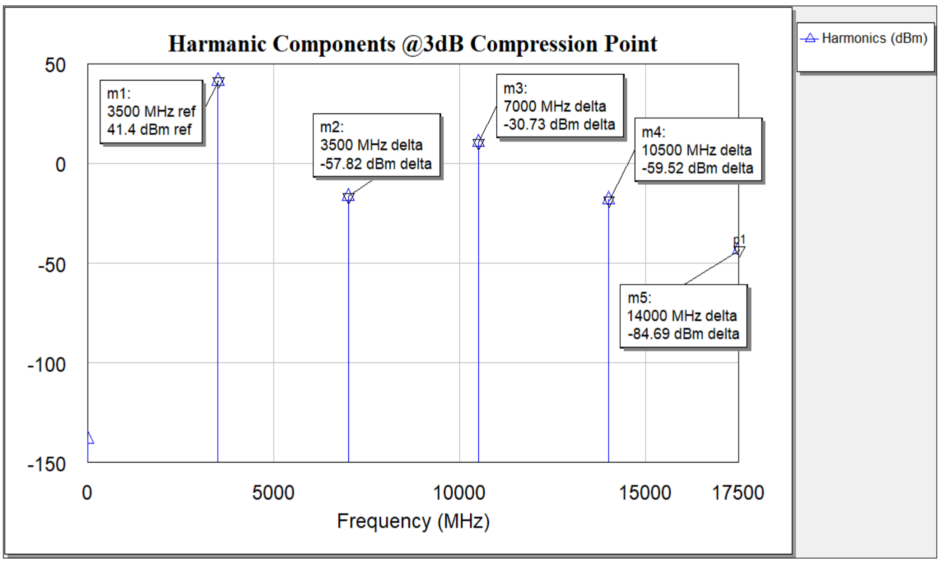

Figure 3. 24: Harmonic components at the output at 3 dB compression point.

It is also important to check the time domain drain current and output voltage waveform and verify that Class AB operation is valid. Drain current and output voltage waveforms are investigated for each frequency during design. Drain current and output voltage waveforms at 3.5 GHz for different input current levels are given in Figure 3. 25, Figure 3. 26, Figure 3. 27,and Figure 3. 28. As it can be seen transistor is on for small levels of input power and it is off for less than half period for higher input power levels as it is expected in Class AB operation. Output voltage graphs also show that non-sinusoidal drain current is converted to sinusoidal output voltage.

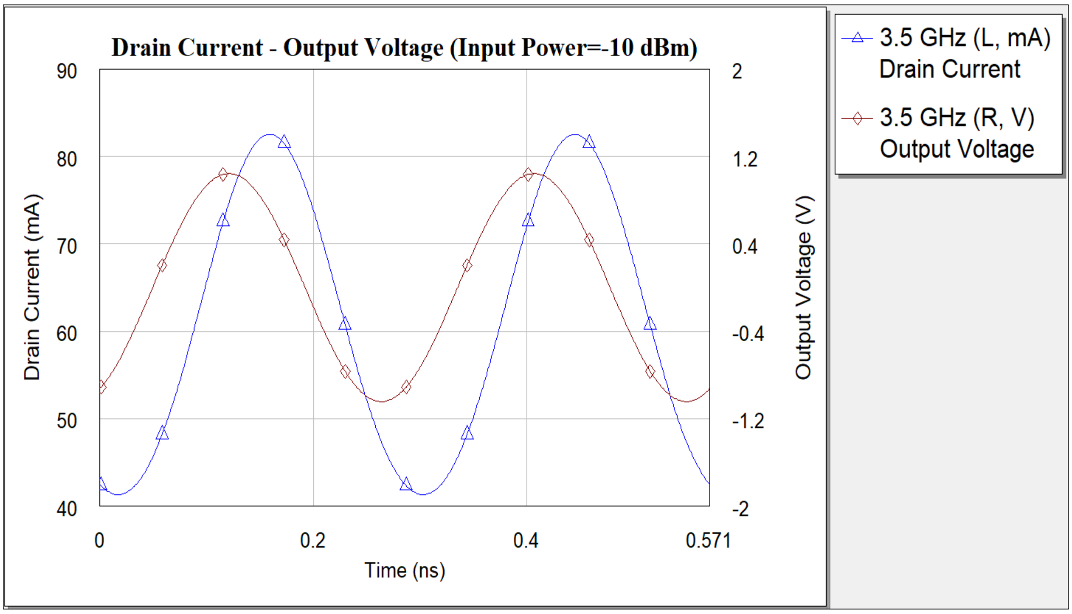

Figure 3. 25: Drain current and output voltage waveform for Pin=-10 dBm.

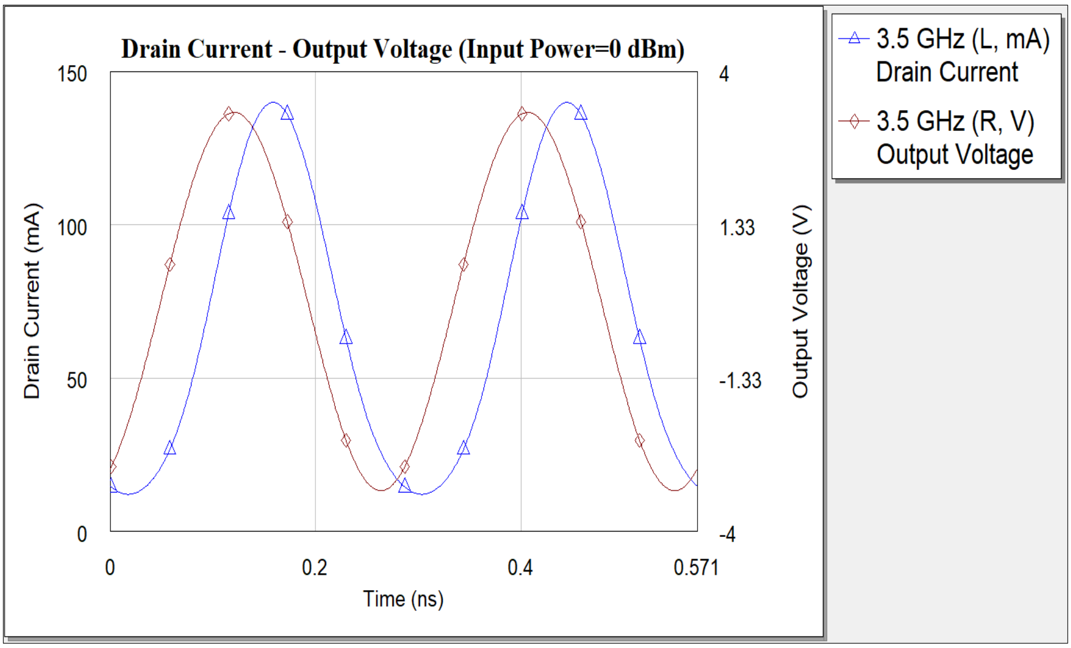

Figure 3. 26: Drain current and output voltage waveform for Pin=0 dBm.

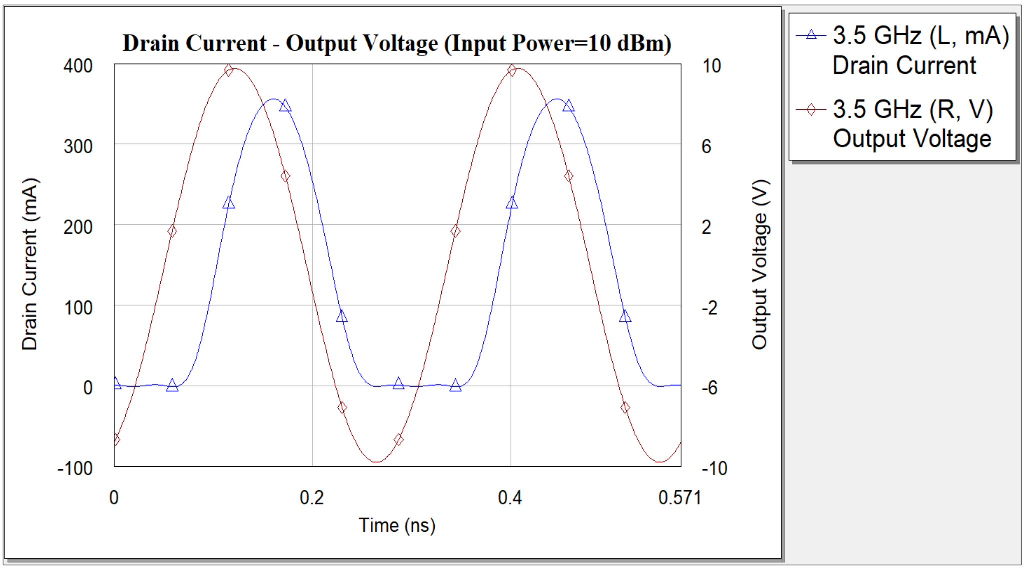

Figure 3. 27: Drain current and output voltage waveform for Pin=10 dBm.

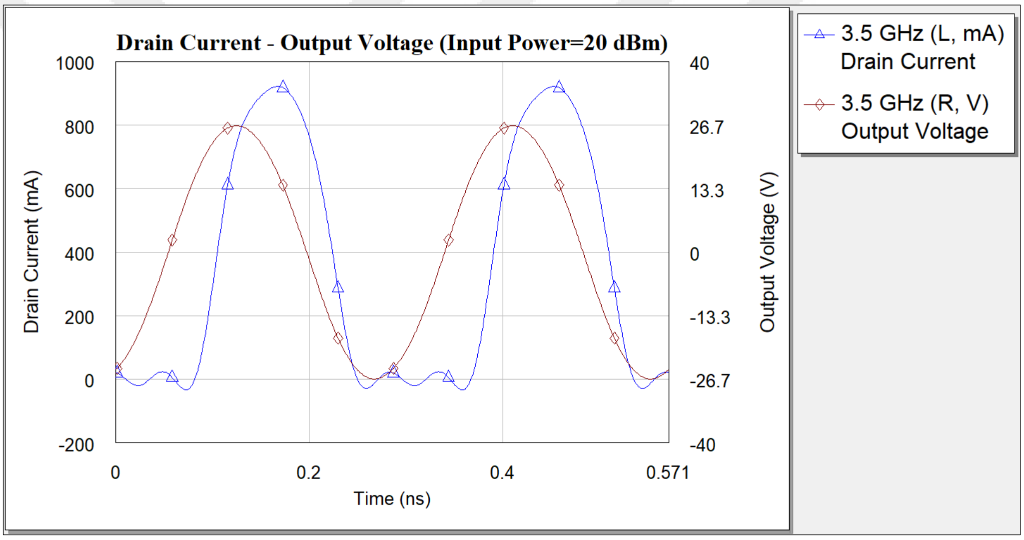

Figure 3. 28: Drain current and output voltage waveform for Pin=20 dBm.

4. IMPLEMENTATION AND MEASUREMENT

4.1 Layout

After completing electromagnetic simulation, layout of the designed circuit is completed to make it ready for manufacturing. Complete layout of the designed circuit is given in Figure 4. 1.

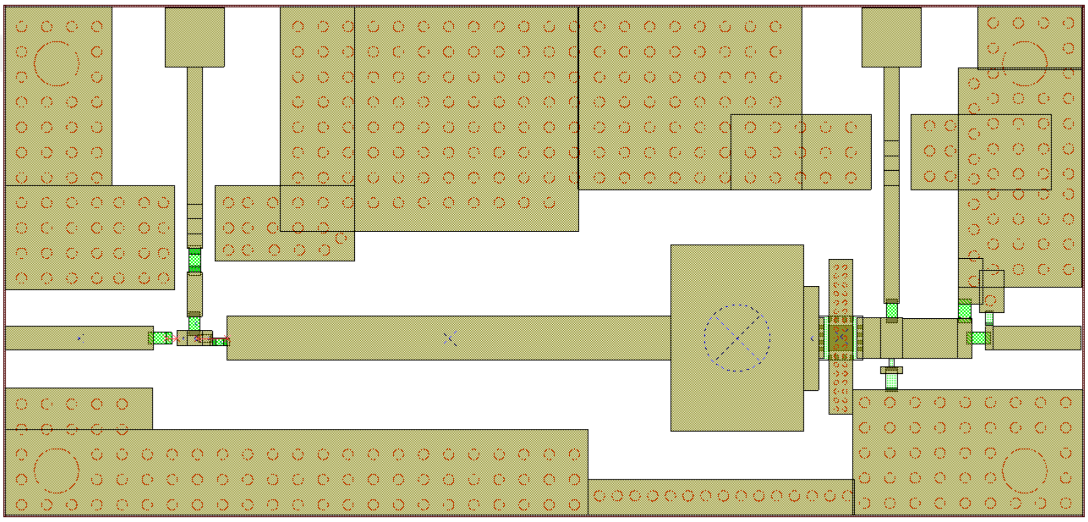

Figure 4. 1: Layout of the designed amplifier.

After completing layout, Gerber files which are required for the manufacturing are generated with AWR Gerber Tool and sent to manufacturing company.

4.2 Fabricated and Assembled Circuits

After getting manufactured circuits back from the company, the circuit elements, transistor, capacitors, inductors, and resistors are assembled on the bare board. Power supply cables for V_{GS}, V_{DS} and ground are soldered to bias points. SMA connectors are assembled at the RF input and output.

Board in mounted on an aluminum heatsink to remove the dissipated power away from the board. Thermal paste is applied between the bottom face of the board and heatsink to provide better thermal conductivity. Complete circuit is given in Figure 4. 2.

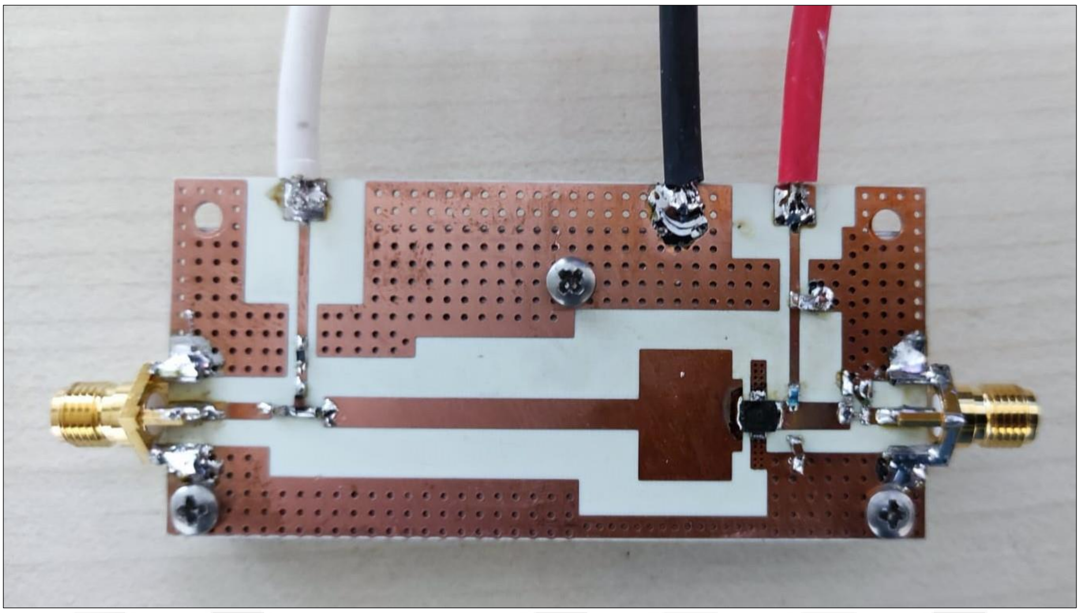

Figure 4. 2: Assembled circuit.

After completing manufacturing and the assembly of the designed power amplifier, next step is to complete both small signal and large signal measurements of the designed amplifier and compare them with the simulation results.

4.3 Measurement Setup

There is a certain power-up and power-down sequence which must be carefully performed for used GaN transistor. If there is a violation in the power-up, power-down sequence transistor may be damaged due to the charged capacitances on the devices. Correct power up sequence is as follow:

- VGS bias is set to -4 V and turned-on
- VDS bias is set to 50 V and turned-on
- VGS is increased slowly until desired drain current level is reached (59 mA)
- RF input signal is applied

Similarly, power-down sequence is as follow:

- RF input signal is removed
- VGS bias is decreased until there is no drain current
- VDS is turned-off
- After a few seconds, VGS is turned-off

It should be ensured that amplifier is stable and there is no oscillation before starting measurements. Input of the transistor is terminated with 50 ohm load and output is connected to a spectrum analyzer. Spectrum analyzer span is adjusted to observe very wide spectrum. Amplifier is powered-on and spectrum is observed for a time. It is ensured that there is no signal on the spectrum which means that there is no oscillation. After stability check, it is safe to start measurements. Two port Vector Network Analyzer (VNA) is used for the small signal measurements. VNA is calibrated for the desired frequency interval (3.3 – 3.6 GHz) using SOLT (short-open-load-thru) calibration. Calibration is performed for -15 dBm port power level to ensure small signal operation.

For large signal measurements, it is required to sweep input power starting from a low power level around -10 dBm to a level where amplifier reaches its 3 dB compression point. From the simulations, it is seen that 25 dBm and even more is required as the upper level of input power.

In general, 25 dBm output power is a high-power level for signal generators and around this power level signal generators starts to go into compression so the measurement results will be affected from the signal generator performance. To keep signal generator output linear and reach the required power level, a high gain, highly linear amplifier is used at the output of signal generator.

Another point about the power amplifier measurement is to protect the measurement equipment at the output, spectrum analyzer or power meter. Designed power amplifier is expected to produce around 10 W output power. Absolute maximum power rating of commercially available spectrum analyzers and power meters are well below this point and typically around 1W for spectrum analyzers and 100-200 mW for power meters. To protect the measurement equipment, attenuators which can handle the output power of the power amplifier should be used. By doing so, output power level is kept below the maximum rating of measurement equipment.

There is two problem about such measurement setup. First one is the frequency dependence of linear amplifier gain, attenuator loss and cable loss. Attenuators and cables show different loss at different frequencies and in general it is generally proportional to increasing frequency. The other is the difference in amplifier gain in different frequencies. All these unwanted factors should be calibrated out to get correct measurement results.

The measurement setup given in Figure 4. 3 is created to mitigate the frequency dependent factors.

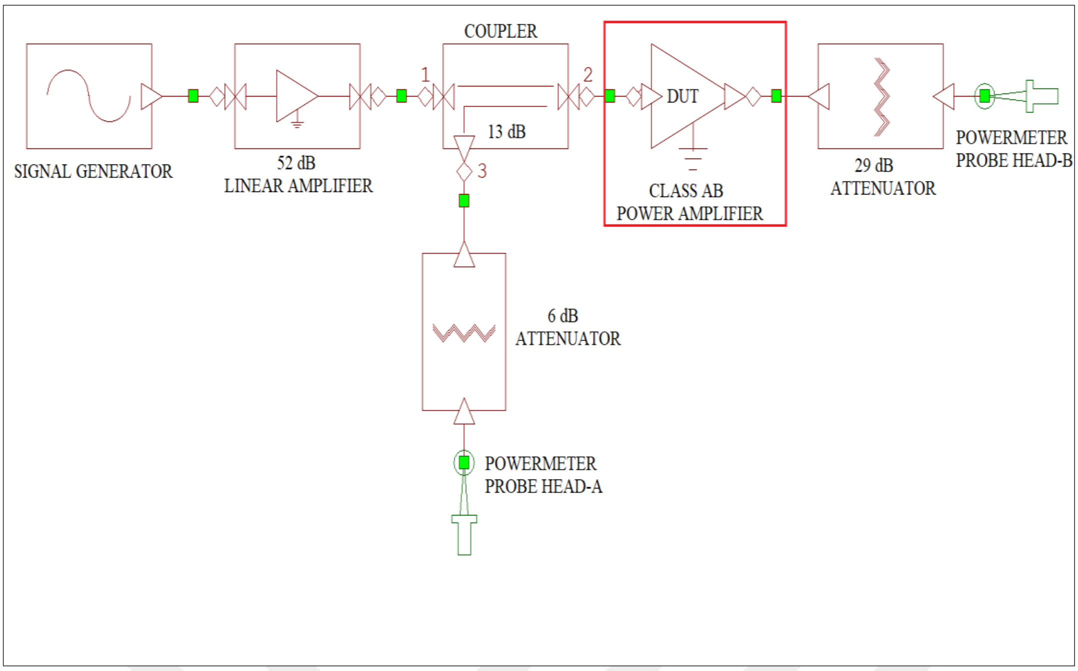

Figure 4. 3: Large signal measurement setup.

Measurement setup is firstly calibrated without putting the DUT in the measurement setup. The power meter probe head A and power meter probe head B is with an automatic sweep for all frequencies and all power values. By doing so, total system loss is determined for each frequency. System is adjusted such that power at the input of designed amplifier is swept between -10 dBm and +25 dBm. In the meantime, power supply values are continuously readback and noted for each input power value.

In each input power level sweep, input power, output power and drain current is automatically written into a CSV file which is evaluated to determine gain and corresponding efficiency after sweep.

4.4 Measurement Results

It is seen that input reflection (S11) is different than the simulation. Lumped elements in the input circuitry changed to see the effect but it is seen that there is a resonance at 3 GHz and it is not changing. This behavior could be changed by decreasing the line widths, but it was irreversible. Instead, it is decided to put copper tape on input line and move the resonance point to operating frequency. Modification made on the input circuitry is given in Figure 4. 4.

Simulation results is given in Figure 4. 5 and compared with the simulation results. As it can be seen forward gain and output reflection results are quite consistent.

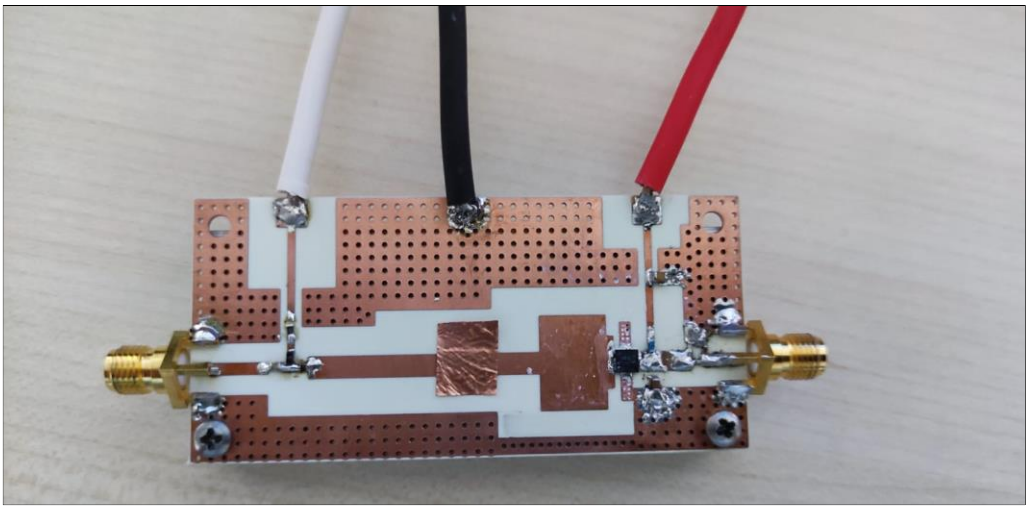

Figure 4. 4: Copper band added to input for matching.

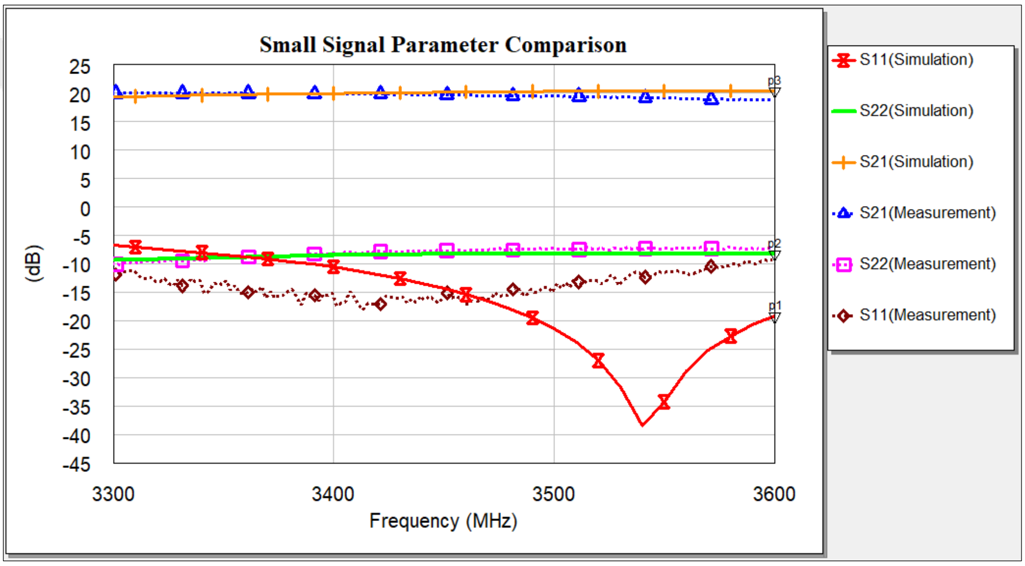

Figure 4. 5: Small signal measurement result and comparison with simulation.

For output power and PAE measurements, test setup given in Figure 4. 3 is created. Input power of the amplifier is swept from -10 dBm to +25 dBm. Test setup is configured to record DC current value and corresponding output power for each input power level.

Recorded DC current value, input power level and output power level are evaluated to determine gain, 3 dB compression point and corresponding PAE and output power levels for each frequency.

Power sweep measurement results for 3.3 GHz, 3.4 GHz, 3.5 GHz and 3.6 GHz and comparison with the simulation results are given in Figure 4. 6, Figure 4. 7, Figure 4. 8, and Figure 4. 9, respectively.

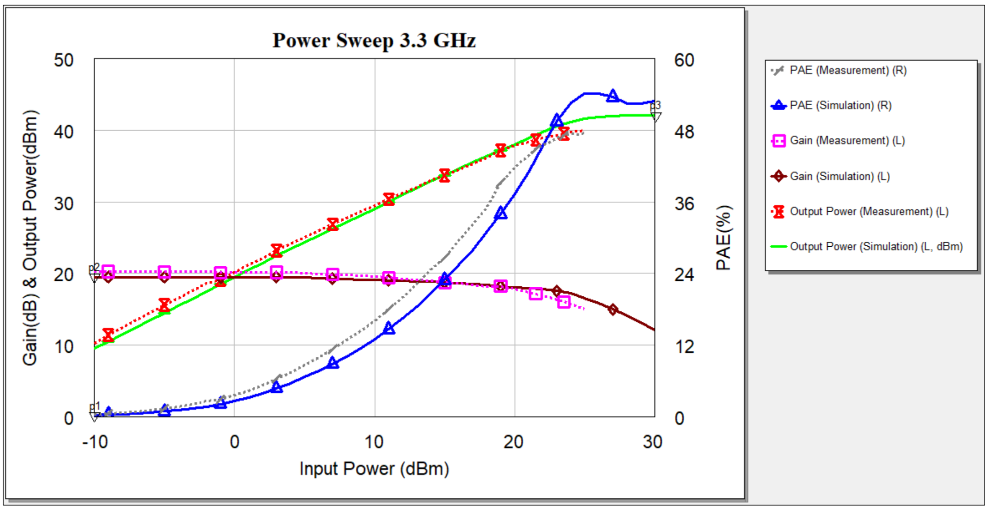

Figure 4. 6: 3.3 GHz gain, output power and PAE measurement results and comparison with simulation.

Figure 4. 7: 3.4 GHz gain, output power and PAE measurement results and comparison with simulation.

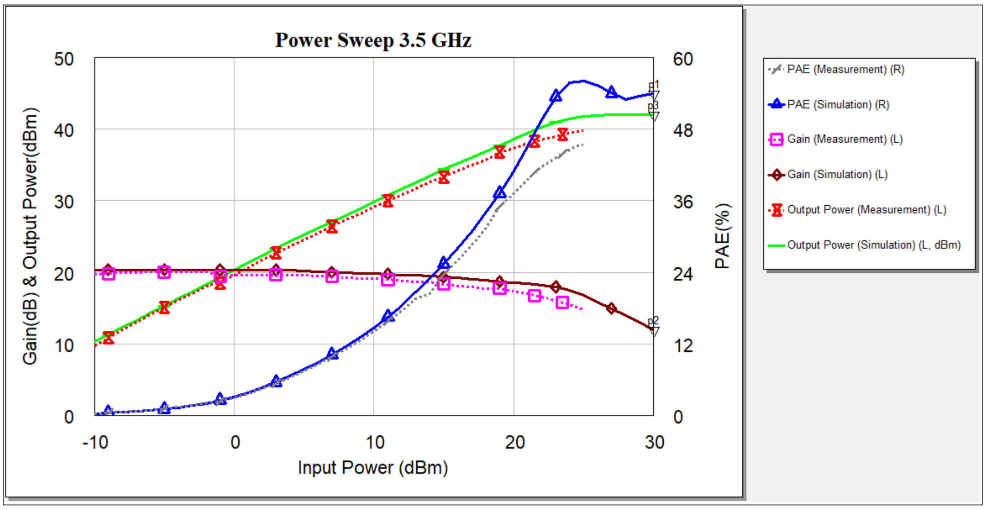

Figure 4. 8: 3.5 GHz gain, output power and PAE measurement results and comparison with simulation.

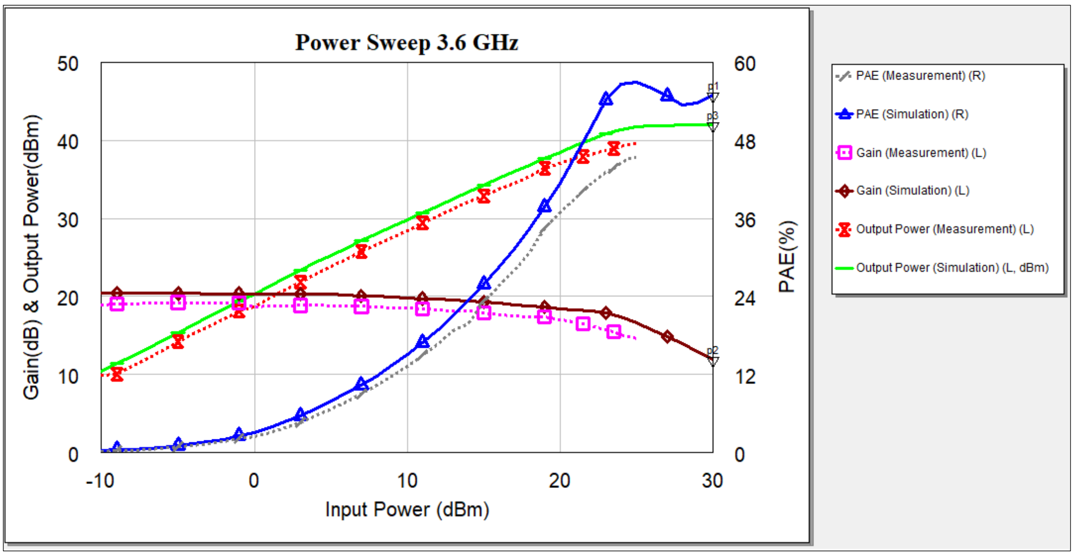

Figure 4. 9: 3.6 GHz gain, output power and PAE measurement results and comparison with simulation.

Comparison of gain, output power and PAE for each frequency at 3 dB compression point is given in Table 4. 1.

Table 4. 1: Comparison of measurement and simulation results.

	Gain (dB)		Output Power (dBm)		PAE (%)	
Frequency	Sim.	Meas.	Sim.	Meas.	Sim.	Meas.
3.3 GHz	16.33	17.2	41.7	38.7	56.5	44.8
3.4 GHz	16.92	16.97	41.6	38.15	56	39.8
3.5 GHz	17.34	16.68	41.5	38.4	55.7	41
3.6 GHz	17.4	16.94	41.3	38.55	56.5	42.4

As it is seen, lineer gain of the amplifier mostly consistent with the simulation. Output power levels in the simulation is not achieved during simulations. Lower output power is also the reason of getting lower power added efficiency than desired.

Along with the resonance issue seen at input matching, output circuitry is also showed different behaviour than the simulation. The reason of not getting the simulated output power and power added efficiency values can be related with the model issue.

The reason of the difference seen in input reflection is tried to be seen in the simulation and after that added copper band is included in the simulation to see its effect. Slight change in the length of the microstrip line at the transistor input shifted the input reflection point around 3GHz as it is seen in the measurements and it is given in Figure 4. 10.

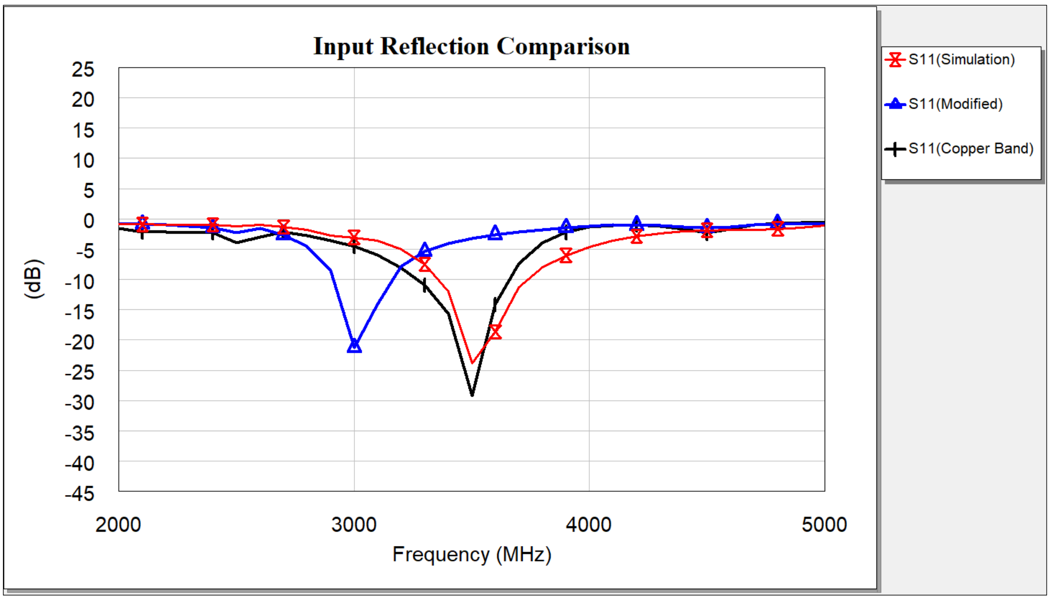

Figure 4. 10: Input reflection comparison.

5. CONCLUSION

In this study, power amplifier fundamentals and different power amplifier classes are investigated. Gallium Nitride based transistor is selected for Class AB amplifier design for outstanding power and thermal performance of gallium nitride in the high power applications.

Operating frequency of the Class AB power amplifier is selected for sub-6 5G transmitter systems centered around 3.5 GHz. 5G is selected as the target application because of the improvements that it will bring to mobile communication system and the change that will occur on the daily life.

The power amplifier design was aiming to have a lineer gain of 18 dB, PAE of 50% and output power of 10 Watt. Simulation results were satisfactory and had enough margin to fullfill the design goals. Measurement results showed satisfactory lineer gain and compatible with simulation results while output power is around 6.75 Watt at 3 dB compression point. Power added efficiency level of %55 is not reached in the measurements because of the low output power level.

The difference between the simulation results and the measurement results is interpreted as the difference between the non-linear model and real life behaviour of the selected transistor. The difference may be associated with the other circuit component models.

Although the output power and PAE are below the expectation, lineer gain of the designed Class AB amplifier is satisfying and meets the design specifications. Next step of this study is to investigate the root cause of these differences and mitigate them.

REFERENCES

[1] **History of Wireless Communications. (2021).** *Retrieved 21 January 2021, from https://www.microwavejournal.com/articles/24759-history-of-wireless-communications#comments-container*

[2] **Pui-In Mak, Weng-Ieng Mok, Seng-Pan U and R. P. Martins**, "I/Q imbalance modeling of quadrature wireless transceiver analog front-ends in SIMULINK," *2003 IEEE 58th Vehicular Technology Conference. VTC 2003-Fall (IEEE Cat. No.03CH37484)*, Orlando, FL, 2003, pp. 2371-2374 Vol.4, doi: 10.1109/VETECF.2003.1285954.

[3] **Colantonio, Paolo, et al.** *High Efficiency RF and Microwave Solid State Power Amplifiers.* Wiley, 2009.

[4] **Kizilbey, O. and Palamutcuogullari, O.,** 2014. A comparison of GaN, Si and GaAs power amplifiers. *2014 22nd Signal Processing and Communications Applications Conference (SIU),*.

[5] **Moore, A.& Jimenez, J.** (2014). *GaN RF Technology for Dummies.* Hoboken, NJ: Wiley.

[6] GaN/SiC based High Electron Mobility Transistors for integrated microwave and power circuits. (2021). Retrieved 10 February 2021, from http://uef.fei.stuba.sk/moodle/mod/book/view.php?id=7920&chapterid=57

[7] **Q. K. Ud Din Arshad, A. U. Kashif and I. M. Quershi**, "A Review on the Evolution of Cellular Technologies," 2019 16th International Bhurban Conference on Applied Sciences and Technology (IBCAST), Islamabad, Pakistan, 2019, pp. 989-993, doi: 10.1109/IBCAST.2019.8667173.

[8] **G. Barb and M. Otesteanu,** "4G/5G: A Comparative Study and Overview on What to Expect from 5G," *2020 43rd International Conference on Telecommunications and Signal Processing (TSP)*, Milan, Italy, 2020, pp. 37-40, doi: 10.1109/TSP49548.2020.9163402.

[9] **Mukhopadhyay, Shameek & Agarwal, Vatsal & Sharma, Sourav & Gupta, Vineet.** (2016). A Study On Wireless Communication Networks Based On Different Generations. International Journal of Current Trends in Engineering & Research (IJCTER). 2. 300-304.

[10] **Ruiz, Hector Solar, and Pérez Roc Berenguer.** *Linear CMOS RF Power Amplifiers: a Complete Design Workflow.* Springer, 2014.

[11] **Albulet, Mihai.** *RF Power Amplifiers*. Noble, 2001.

[12] **Shirvani, A., & Wooley, B.** (2011). *Design and control of RF power amplifiers.* New York: Springer.

[13] ***Qorvo***, www.qorvo.com/products/p/QPD1009.

[14] **Ceylan, O (2015).** *küçük uydular için x bant gan sic-hemt f sinifi yüksek verimli güç kuvvetlendiricisi tasarimi ve rf güç fetleri için faz ile genlik duyarliği analizi* (PhD Thesis), İstanbul Teknik Üniversitesi, Fen Bilimleri Enstitüsü, ISTANBUL.

CURRICULUM VITAE

Name Surname : KUDRET ÜNAL

EDUCATION

- **B.Sc.** :2017, Istanbul Technical University, Faculy of Electrical and Electronics Engineering, Electronics and Communication Engineering

PROFESSIONAL EXPERIENCE AND REWARDS:

- 2019-Continue, Analog Devices, Application Engineer, Supporting PLL with Integrated VCOs and Clocking Parts
- 2016-2019, ABE Technology, Repeater System Design
- 2016-2017, ITU RF Electronics Laboratory, Low Noise Amplifier Design