ADVANCED CIRCUIT ARCHITECTURES FOR READOUT ELECTRONICS OF
LOW-COST MICROBOLOMETER FOCAL PLANE ARRAYS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

MUSTAFA HALUK ÇÖLOĞLU

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2017

Approval of the thesis:

**ADVANCED CIRCUIT ARCHITECTURES FOR READOUT
ELECTRONICS OF LOW-COST MICROBOLOMETER
FOCAL PLANE ARRAYS**

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ABSTRACT

ADVANCED CIRCUIT ARCHITECTURES FOR READOUT ELECTRONICS OF LOW-COST MICROBOLOMETER FOCAL PLANE ARRAYS

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September 2017, 112 pages

This thesis presents a study on the design and characterization of advanced circuit architectures for readout electronics of low-cost microbolometer focal plane arrays (FPAs). In this respect, two advanced circuit architectures are developed in order to improve the performance, flexibility, and simplicity of use of the microbolometer based low-cost thermal imaging sensors.

The first circuit architecture is developed for the readout electronics of 40x40 focal plane array (FPA) with 60 µm pixel pitch using 0.35 µm CMOS technology and contains several digital circuit blocks such as a digital controller, row scanner, column multiplexer, serial peripheral interface (SPI), sensor configuration memory, and pixel level biasing (PLB) memory assigned to the selected FPA row. The digital controller block allows the sensor to generate its own timing signals using only an external clock signal. The row scanner performs a selection of single FPA row at a time and the column multiplexer serializes the analog outputs of the column readout channels. A standard 4-wire SPI is designed to provide a simple communication means between the sensor memory and external controller. This programmability provides flexible operation under different conditions. The designed circuit blocks in the first sensor were tested and verified, then, first infrared images were obtained from the sensor. In order to improve the sensor performance, a simple but very

efficient detector bias calibration algorithm is developed on Field-Programmable-Gate-Array (FPGA). The test results of the developed algorithm show that the effects of all non-uniformity sources can be compensated in just 7 frames with simple camera electronics.

The second circuit architecture is developed for the readout electronics of 80x80 FPA with 35 μm pixel pitch using 0.18 μm CMOS technology. Besides the circuit blocks developed for the first sensor, the second circuit architecture has several important improvements. Firstly, the PLB memory of the second sensor is designed to store the calibration data of all pixels. This improvement simplifies the physical interface between the sensor and camera electronics, since no real time data transmission is required to fill PLB memory. Secondly, the detector bias calibration algorithm developed for the first sensor is integrated into the second sensor. Thanks to this improvement, the second sensor is able to self-calibrate itself by using only on-chip components. Lastly, the image windowing feature, which may be required in some applications to decrease total power consumption of the sensor by reducing the resolution of the output image, is added to the second sensor.

The circuit architectures developed in the scope of this thesis can be used for all types of microbolometer FPAs to improve their performance. The developed circuit architecture for the second sensor makes it the first thermal imaging sensor having fully on-chip non-uniformity correction feature in Turkey.

Keywords: Low-cost uncooled infrared detectors, focal plane array, microbolometer FPAs, on-chip detector bias calibration, non-uniformity correction, offset sources in microbolometer FPAs, CMOS IR, MEMS.

ÖZ

DÜŞÜK MALİYETLİ MİKROBOLOMETRE ODAK DÜZLEM MATRİSLERİNİN OKUMA ELEKTRONİĞİ İÇİN İLERİ SEVİYE DEVRE MİMARİLERİ

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Bu tez, düşük maliyetli mikrobolometre odak düzlem matrisleri okuma elektroniği için gelişmiş devre mimarilerinin tasarım ve karakterizasyon çalışmalarını sunmaktadır. Bu bağlamda, mikrobolometre tabanlı düşük maliyetli termal görüntüleme sensörlerinin performansını, esnekliğini ve kullanım kolaylığını artırmak için iki ileri seviye devre mimarisi geliştirildi.

0.35 µm CMOS teknolojisi kullanılarak tasarlanan birinci devre mimarisi, 60 µm piksel aralığına sahip olan 40x40 odak düzlem matrisinin (FPA) okuma elektroniği için geliştirildi ve dijital denetleyici, satır tarayıcı, sütun çoklayıcı, seri periferik arabirimi (SPI), sensör konfigürasyon belleği ve seçili FPA satırına tahsis edilmiş olan pixel seviyesinde kutuplama (PLB) belleği gibi dijital devre bloklarından oluşur. Sayısal denetleyici bloğu, sensörün kendi zamanlama sinyallerini yalnızca harici bir saat sinyali kullanarak üretmesine izin verir. Satır tarayıcı bir seferde tek FPA sırasını seçer ve sütün çoklayıcı sütun okuma devresi analog çıkışlarının seri hale getirilmesini sağlar. Standard 4-telli SPI, sensör belleği ve harici kontrolör arasında basit bir iletişim yolu sağlamak için tasarlanmıştır. Bu programlanabilirlik, farklı koşullar altında esnek bir çalışma sağlar. Birinci sensörde tasarlanan devre blokları test edilip doğrulandıktan sonra sensörden ilk infrared görüntüler elde edilmiştir.

Sensör performansını artırmak için basit fakat çok etkili bir dedektör kutuplama kalibrasyon algoritması Alan-Programlanabilir-Kapı-Dizisi (FPGA) üzerinde geliştirilmiştir. Geliştirilen algoritmanın test sonuçları, tüm düzensizlik kaynaklarının etkilerinin basit bir kamera elektroniği ile sadece 7 karede giderilebileceğini göstermektedir.

0.18 μm CMOS teknolojisi kullanılarak tasarlanan ikinci devre mimarisi, 35 μm piksel aralığına sahip olan 80x80 FPA okuma elektroniği için geliştirildi. Birinci sensör için geliştirilen devre bloklarına ilaveten, ikinci devre mimarisi birkaç önemli iyileştirmeye sahiptir. İlk olarak, ikinci sensörün PLB belleği tüm piksellerin kalibrasyon verilerini saklamak üzere tasarlanmıştır. Bu iyileştirme, sensör ve kamera elektroniği arasındaki fiziksel arayüzü basitleştirmektedir, çünkü PLB belleğini doldurmak için gerçek zamanlı veri iletimi gerekmez. İkinci olarak, birinci sensör için geliştirilen dedektör kutuplama kalibrasyonu algoritması, ikinci sensöre entegre edildi. Bu iyileştirme sayesinde, ikinci sensör, yalnızca yonga-üstü bileşenleri kullanarak kendi kendini kalibre edebilmektedir. Son olarak, ikinci sensöre, bazı uygulamalarda çıktı görüntüsünün çözünürlüğünü azaltarak sensörün toplam güç tüketimini azaltmak için gerekli olabilecek görüntü maskeleme özelliği eklenmiştir.

Bu tez kapsamında geliştirilen devre mimarileri, her tür mikrobolometre FPA'sının performansını iyileştirmek için kullanılabilir. İkinci sensör için geliştirilen devre mimarisi, bu sensörü tümüyle yonga-üstü düzensizlik giderme özelliği olan Türkiye'deki ilk termal görüntüleme sensörü yapmaktadır.

Anahtar Kelimeler: Düşük maliyetli soğutmasız kızılötesi dedektörler, odak düzlem matrisi, mikrobolometre FPA'ları, yonga-üstü dedektör kutuplama kalibrasyonu, düzensizlik giderme, mikrobolometre FPA'larındaki ofset kaynakları, CMOS IR, MEMS.

To my beloved family

ACKNOWLEDGEMENTS

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IR   :   Infrared

ROIC   :   Read-Out Integrated Circuit

MWIR   :   Mid-Wavelength Infrared

LWIR   :   Long-Wavelength Infrared

NETD   :   Noise Equivalent Temperature Difference

MEMS   :   Micro-Electro-Mechanical Systems

FPA   :   Focal Plane Array

TCR   :   Temperature Coefficient of Resistance

NEP   :   Noise Equivalent Power

SNR   :   Signal to Noise Ratio

SPI   :   Serial Peripheral Interface

ADC   :   Analog to Digital Converter

PLB   :   Pixel Level Biasing

CHAPTER 1

INTRODUCTION

Humans have a multitude of senses; sight, hearing, taste, smell and touch. Clearly, sight is the most important one among those senses. Without sight, we would be lack of plenty of information around us. This information which comes from the sight allows us to interact with our surroundings, keep us safe and avoid danger. Can we say that we have all the necessary information to interact with our surroundings and avoid danger with the sight? The answer is no because our sight capability is limited to visible light which constitutes very small portion of the electromagnetic spectrum. Therefore, we still have a lot of missing information around us. Some of this missing information exists in the infrared spectrum, which lies between the red end of the visible spectrum and microwave spectrum. Humankind first discovered infrared light and then its detectors to reveal a lot of information around us which was previously hidden. Today, infrared detectors are used in plenty of applications. Those applications include military, security, astronomy, scientific, medical, industrial, automotive, etc. Considering the fact that infrared blackbody radiation reaches its maximum power output in the 8 to 12 μm region at skin temperature (30 to 34℃) [1], thermal-infrared imaging becomes essential in both military and civilian applications. Also, infrared imaging is extensively used in astronomy, since some part of the infrared spectrum can easily penetrate through dust [2]. Consequently, by the advent of infrared detectors, plenty of invisible information in the universe has become visible and infrared imaging is being used in countless applications today. These applications have changed the world and human life extensively.

The main goal of this thesis is to develop advanced circuit architectures for readout electronics of low-cost microbolometer FPAs. These circuit architectures mainly focus on the non-uniformity correction, which must be performed due to the inevitable mismatches existing in the sensor such as pixel resistance non-uniformity

across FPA, non-uniformity between column readout channels and so on. This calibration reduces the offsets between pixel output voltages; therefore, significant improvements are observed in several performance parameters of the sensor. This chapter gives brief information about the infrared detectors and focuses mainly on the microbolometers. The working principles of the infrared detectors are summarized in Section 1.1. Then, the more detailed information about the microbolometers is given in Section 1.2. Some readout architectures in the literature are summarized in Section 1.3. Lastly, Section 1.4 finalizes the chapter by giving research objectives and thesis organization.

1.1 Infrared Detectors

An IR detector is a device that senses IR radiation and convert it into electrical signals which are then processed to form an image. Different types of detection systems can be used to detect IR radiation. According to the principle behind them, IR detectors can be classified as photon detectors and thermal detectors.

IR photon detectors are made up of semiconductor materials which absorb IR radiation and create electron-hole pairs as a result of the absorption of the IR light. By the help of built-in or externally applied electric field, these photo-excited electrons are then accumulated in capacitors located in the ROIC of the detector. The electrical potential created on these capacitors are converted into digital signals using analog to digital converters (ADCs) and IR imaging of an object can be realized using these signal data. Detection of IR radiation in photon detectors has some difficulties. Since the energy of the IR radiation in MWIR and LWIR bands is comparable to the phonon energy of materials at room temperature, IR photo-detectors should be cooled at cryogenic temperatures to reduce the effect of thermally generated electrons that contribute to the total current as noise. However, cryogenic cooling increases the cost and the total power dissipation of the system in addition to making the system bulky and more complex. The examples of photon detectors are Mercury Cadmium Telluride (MCT), Indium Antimonide (InSb), Quantum Well Infrared Photodetector (QWIP), and Supper Lattice Detectors [3].

Thermal detectors make use of the heat power of the IR radiation. When absorbed by a material, IR radiation warms up the material and increases its temperature. This temperature change may affect the material's some physical properties which can be converted into electrical signals. For example, conductivity change due to absorption of IR radiation is the basic working principle of a bolometer which is the most popular thermal detector type used in thermal imaging systems widely [4]. In bolometers, it is crucial to choose a material whose conductivity change when radiated by IR light is high enough to measure it with a suitable electronic circuitry. Bolometers do not need cryogenic cooling since rather than photon-induced electron excitation, thermally-induced conductivity change is important; therefore, thermally excited electrons do not affect the performance of the thermal detectors. Absence of cryogenic cooling makes this kind of thermal imaging systems light, compact and low cost. Being low cost is not only due to the absence of cryogenic cooling, but also these thermal sensors are easy to implement and manufacture in comparison to photon detectors where the crystal quality of the detector is very important and materials used to grow photon detectors are expensive. A disadvantage of these detectors is that vacuum packaging is needed to block other external heat sources apart from the IR radiation. Also, low detection capability and slow response time are other disadvantages of these detectors. Slow response time is due to the multi-step process where detector should first absorb IR radiation and as a second step its temperature should increase where conductivity change occurs and sensed by an electronic circuitry. Therefore, fast frame rates cannot be achieved using these detectors. Thermocouples are another group of thermal detectors. In thermocouples, rather than conductivity change, potential difference between two different jointly connected materials is measured when they are heated. The next group of thermal detectors is the pneumatic detectors which are not commonly used. Working principle of these detectors is based on the heating of the gaseous inside a cavity. Finally, pyroelectric detectors can be regarded as another group of thermal detectors. On pyroelectric detectors, in order to detect IR radiation, electrical potential created by the heat change of a polar material is used. Among all of these thermal detectors, the best performance is achieved by bolometers in thermal imaging systems [4].

To sum up, photon detectors have superior performance over thermal ones in terms of detector response time, NETD and multispectral operation. On the other hand, photon based imaging systems are bulky and expensive when compared to thermal based imaging systems. Therefore, photon detectors are preferred over thermal detectors if the system requires high performance and there is no constraint on the size and cost of the system. If the size and cost are important, thermal detectors become more advantageous [5].

Since this thesis focuses on read-out architectures for resistive-type, cost-effective microbolometers, the next section of the thesis is left to microbolometers which are the most widely used uncooled infrared detectors.

1.2 Microbolometers

A microbolometer is a thermal sensor whose dimensions are in the micrometer range. Figure 1-1 shows a representative view of the physical structure of a microbolometer detector pixel [5]. As shown in Figure 1-1, its physical structure seems like a suspended bridge. This bridge-like suspended structure with support arms provides great thermal isolation between the sensor and environment when the sensor is under vacuum. Thermal isolation allows measurable heat change when infrared radiation falls on a microbolometer detector since the temperature rise due to the absorbed radiation does not spread to the substrate easily. Therefore, thermal isolation between the sensor and environment becomes an important issue for thermal detectors.

In order to detect the temperature change on the microbolometer, a temperature sensitive material is buried in the sensor structure. Some electrical properties of this material change when it heats up. This slight change is measured and amplified with the suitable read-out circuitry inside the chip and converted into an image by external electronics.

Thanks to advanced MEMS technology, microbolometers can be manufactured in an array format called FPAs. Along with the improvements in fabrication processes for the microbolometric FPAs and advance of integrated circuit technology for CMOS

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ROIC, the performance of microbolometric FPA has made great progress [6]-[9]. Today, small pixel pitch and high resolution microbolometers are widely used in the market.
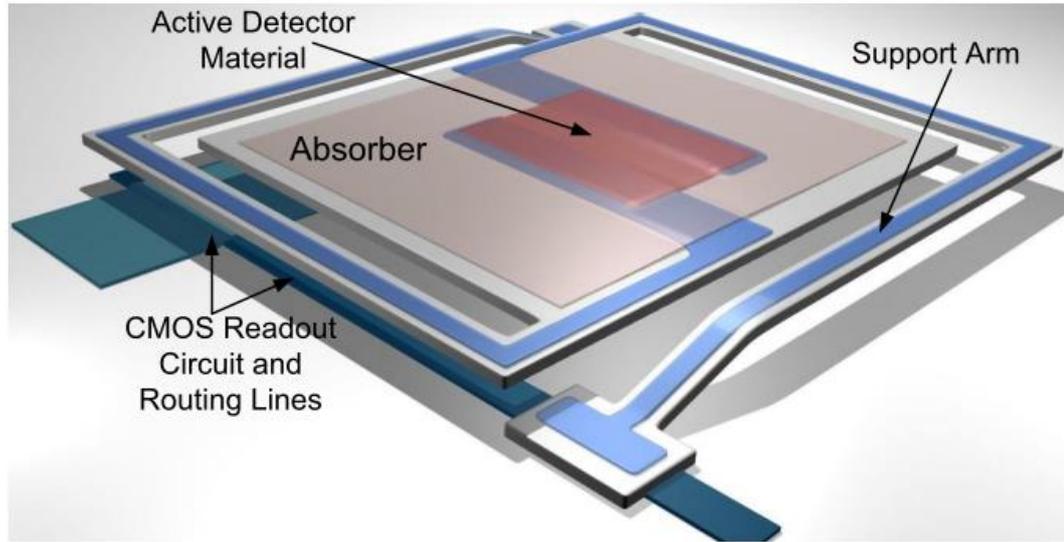
Figure 1-1: Representative view of the physical structure of microbolometer detector pixel [5].

The surface micromachining process is implemented in the fabrication of microbolometers conventionally. This process is done after CMOS fabrication and it increases complexity and cost, since it requires many post-processing steps to embed high TCR active material into the microbolometer and also to suspend the microbolometer array structure [10]. Therefore, multi-step surface micromachining process is not suitable for developing microbolometer FPAs for applications in which performance is not critical but the cost is important. Today, cost-effective CMOS-based microbolometer FPAs are developed by our team at MikroSens which is located at METU Technopolis in Turkey. These cost-effective microbolometer FPAs are realized using a bulk micromachining process after CMOS fabrication. Active materials of these cost-effective sensors are buried into the microbolometer structure during CMOS fabrication and these materials can be either thin-film resistor or a diode. Since this thesis focuses on circuit architectures for non-uniformity correction

in resistive-type microbolometer FPAs, the rest of this thesis will center on resistive-type microbolometers.

1.2.1 Parameters of Resistive Type Microbolometers

As stated earlier, resistive type microbolometers make use of the resistance change of the temperature sensitive material due to heating up when IR radiation falls on it. Since the absorbed IR radiation per pixel can be as low as a fraction of nano-watts, this heating up event results in too little increase in the temperature of the active material [11]. Therefore, the temperature sensitivity of the resistance buried into microbolometer is one of the most important parameter that is described by the temperature coefficient of resistance (TCR). TCR is defined as

$$\alpha = \frac{1}{R}\frac{dR}{dT} \tag{1.1}$$

where α is the TCR of the detector resistance in %/K, R and T are the resistance and temperature of the detector, respectively. TCR can be negative or positive depending on the type of the material used in the detector. For example, metals have positive while semiconductors have negative TCR values [12]. Since the temperature increase, ΔT, due to the absorption of IR radiation is very small, the change in the microbolometer resistance, ΔR, can be written using the TCR equation as follows:

$$\Delta R = R \cdot \Delta T \cdot \alpha \tag{1.2}$$

The second important parameter of the microbolometers is the thermal conductance which indicates the thermal isolation between suspended microbolometer bridge and environment. There is an inverse relationship between the isolation and thermal conductance, as isolation gets better, the thermal conductance decreases. The heat transfer between microbolometer and its surroundings occurs via 3 ways: conduction, convection and radiation. Therefore, there are three components of the thermal conductance which are listed as follows: (1) thermal conductance due to support arms, (2) thermal conductance due to gas environment, and (3) radiative thermal

conductance. The total thermal conductance is calculated by the addition of these three components [12].

The third parameter of the microbolometer is the thermal capacitance. It is related to the total volume and the mass of the microbolometer membrane directly. It affects the speed of the microbolometer by changing its heat up curve. Higher thermal capacitance means slower detector response since it takes more time to heat up by the absorbed IR radiation [5].

The fourth parameter of the microbolometer is the fill factor which is defined by the ratio of the IR light absorbing area to the total detector area. The fill factor is limited by three factors: the support arms, the gap between the arms and the bridge, and the anchor dimensions as shown in Figure 1-1. As these dimensions get bigger, the fill factor decreases [5].

The final parameter when considering about the microbolometer is the absorption coefficient. The incoming radiation that falls onto a detector is not completely absorbed. The ratio of absorbed radiation by the active area to the total radiation that falls onto it defines the absorption coefficient [5].

1.2.2 Microbolometer Model

A resistive type microbolometer is basically a temperature dependent resistance. Therefore, the electrical model of a microbolometer is based on its resistance-temperature characteristics. The resistance of a microbolometer as a function of temperature for slight temperature changes can be expressed as [5]

$$R(T) = R(T_0) + R(T_0) \cdot (T - T_0) \cdot \alpha \qquad (1.3)$$

where T_0 is the substrate temperature, T is the detector temperature and α is the detector TCR. In order to find the change in detector resistance using eqn. (1.3), first, it is necessary to find change in detector temperature. Change in detector temperature can be found by analyzing the microbolometer thermal equivalent circuit which is given in Figure 1-2 [12].
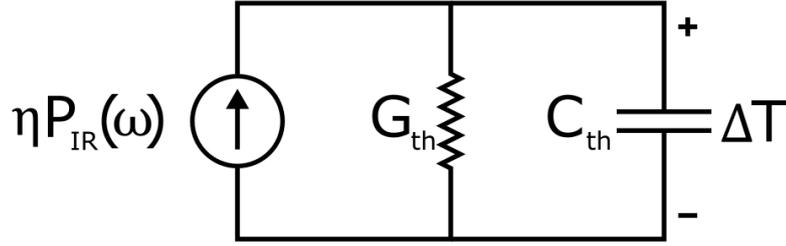
Figure 1-2: Microbolometer thermal equivalent circuit [12].

Considering the microbolometer thermal equivalent circuit in Figure 1-2, the heat flow equation of the circuit can be written as [13]

$$C_{th}\frac{d\Delta T}{dt} + G_{th}\Delta T = \eta P_{IR}e^{j\omega t} \qquad (1.4)$$

where C_{th} is the thermal capacitance, G_{th} is the thermal conductance, ΔT is the temperature change, η is the absorption coefficient, P_{IR} is the radiation power incident on the detector active area, w is the angular frequency of modulation of the radiation, t is the time, and $j = \sqrt{-1}$. Since we try to find the temperature change in the IR sensitive area due to the IR radiation falling on the detector, this equation neglects the power dissipation in the IR sensitive area due to applied electrical bias. The solution of eqn. (1.4) is

$$\Delta T = \frac{\eta P_{IR}e^{j\omega t}}{G_{th} + j\omega C_{th}} = \frac{\eta P_{IR}}{G_{th}(1 + \omega^2\tau^2)^{1/2}} \qquad (1.5)$$

where τ is the thermal time constant, defined as

$$\tau = \frac{C_{th}}{G_{th}} \qquad (1.6)$$

Eqn. (1.5) defines the amount of temperature increase of the IR sensitive area when sinusoidally modulated IR power with amplitude P_{IR} and frequency ω falls on the sensitive area of the detector. In order to calculate the change in the microbolometer resistance, ΔR, due to absorbed infrared power, we can substitute eqn. (1.5) into eqn. (1.3) and get the following expression:

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$$\Delta R = R(T) - R(T_0) = \frac{R(T_0) \cdot \eta \cdot P_{IR} \cdot \alpha}{G_{th} \cdot (1 + \omega^2 \tau^2)^{1/2}} \qquad (1.7)$$

At low frequencies for which $\omega\tau \ll 1$, the resistance change can be approximated as

$$\Delta R = \frac{R(T_0) \cdot \eta \cdot P_{IR} \cdot \alpha}{G_{th}} \qquad \omega\tau \ll 1 \qquad (1.8)$$

where the parameter C_{th} disappears since as the frequency approaches to 0, effect of C_{th} on the resistance change becomes insignificant. At high frequencies for which $\omega\tau \gg 1$, eqn. (1.7) can be rewritten as

$$\Delta R = \frac{R(T_0) \cdot \eta \cdot P_{IR} \cdot \alpha}{\omega \cdot C_{th}} \qquad \omega\tau \gg 1 \qquad (1.9)$$

where ΔR becomes G_{th} independent. Therefore, thermal time constant, τ, must be considered while characterizing the microbolometer resistance change between the low and high frequency regions [13].

1.2.3 Figure of Merits

1. Responsivity

Responsivity is a parameter that shows the amount of electrical signal generated at the output of the detector by the radiation power received by the detector. The electrical signal generated at the output of the detector can be voltage or current depending on the readout architecture. Therefore, responsivity can be either expressed as volts per watt (V/W) or amperes per watt (A/W). For a resistive microbolometer biased by a fixed current, the change in the output voltage, ΔV, is expressed as

$$\Delta V = I_d \Delta R = I_d \alpha R(T_0) \Delta T \qquad (1.10)$$

where I_d is the detector biasing current, α is the TCR of the detector, T_0 is the substrate temperature, $R(T_0)$ is the detector resistance at T_0, and ΔT is the

temperature change of the IR sensitive area. If the detector is biased by a fixed voltage, then the change in the detector current, ΔI, is expressed as

$$\Delta I = \frac{V_d}{R(T_0) - \Delta R} - \frac{V_d}{R(T_0)} \approx \alpha \Delta T \frac{V_d}{R(T_0)} \tag{1.11}$$

where V_d is the detector biasing voltage. If eqn. (1.5) is substituted in eqn. (1.10) and eqn. (1.11), then the voltage responsivity, $\Re_V$, and the current responsivity, $\Re_I$, are expressed as

$$\Re_V = \frac{\Delta V}{P_{IR}} = \frac{I_d \alpha R(T_0)\eta}{G_{th}(1 + \omega^2 \tau^2)^{1/2}} \tag{1.12}$$

$$\Re_I = \frac{\Delta I}{P_{IR}} = \frac{V_d \alpha \eta}{R(T_0)G_{th}(1 + \omega^2 \tau^2)^{1/2}} \tag{1.13}$$

As eqn. (1.12) and (1.13) state, in order to have high responsivity, bias parameter, absorption coefficient, and TCR should be increased as much as possible while the thermal conductance of the detector should be kept minimal.

2. Noise Equivalent Power (NEP)

Noise equivalent power (NEP) is defined as the total power incident on the detector that produces an output signal equal to the root-mean-square (RMS) noise of the detector and it is expressed as

$$NEP = \frac{v_n}{\Re_V} \tag{1.14}$$

where v_n is the total RMS noise voltage, and $\Re_V$ is the voltage responsivity of the detector. In order to calculate total RMS noise voltage, v_n, all noise sources should be considered. There are two main sources of a microbolometer itself: thermal noise and flicker noise. Thermal noise is the electronic noise created by the thermal agitation of the charge carriers. Thermal noise of a microbolometer is independent of any applied bias and can be expressed as

$$v_{n,th} = \sqrt{4kTR_d\Delta f} \tag{1.15}$$

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where $v_{n,th}$ is the RMS value of thermal noise voltage, k is the Boltzmann constant, T is the temperature in K, R_d is the detector resistance, and Δf is the electrical bandwidth of the system. As eqn. (1.15) states, thermal noise is frequency independent and has a flat characteristic over the entire band. On the other hand, flicker noise is frequency dependent and it is expressed as

$$v_{n,1/_f} = \sqrt{\frac{K_f}{f} \Delta f} \tag{1.16}$$

where $v_{n,1/_f}$ is the RMS value of flicker noise, f is the frequency, and Δf is the electrical bandwidth of the system, and K_f is the flicker noise coefficient, which depends on various parameters such as bias current, resistivity, and thin-film fabrication conditions [5], [12]. Using eqn. (1.15) and eqn. (1.16), the noise of a microbolometer itself is expressed as [5]

$$v_{n,det} = \sqrt{\int_{f_1}^{f_2} \left(4kTR + \frac{K_f}{f} \right) df} \tag{1.17}$$

where f_1 and f_2 are the lower and higher limits electrical bandwidths, respectively. Frame rate is the determining factor for f_1 while f_2 depends on the read-out circuit architecture. In order to calculate the NEP value of the system properly, other noise sources, which are read-out circuit noise, temperature fluctuation noise, background fluctuation noise etc., should also be added to the total noise voltage.

3. Noise Equivalent Temperature Difference (NETD)

Noise equivalent temperature difference (NETD) is defined as the change in target temperature which results in the generation of signal at the detector output that is equal to the total RMS noise voltage. As the definition states, NETD can be interpreted as the minimum resolvable temperature difference by the camera system. NETD is not only dependent to the sensor parameters, but also affected by the optics of the camera system and it is expressed as

$$NETD = \frac{4F^2 v_n}{\tau_o A_D \mathfrak{R}_V (\Delta P / \Delta T)_{\lambda_1 - \lambda_2}} \tag{1.18}$$

where v_n is the total RMS noise voltage, τ_o is the transmission of the optics, A_D is the sensitive area of the detector, $\mathfrak{R}_V$ is the voltage responsivity of the detector, $(\Delta P / \Delta T)_{\lambda_1 - \lambda_2}$ is the power per unit area radiated by a blackbody at temperature T measured within the spectral band of $\lambda_1 - \lambda_2$, and F is the F-number of the optics. Assuming the target is at infinity, F is expressed as

$$4F^2 = 4\left(\frac{f}{D}\right)^2 + 1 \tag{1.19}$$

where f and D are the focal length and the diameter of the optics, respectively. NETD is an important parameter to characterize performance of FPAs. NETD is desired to be as small as possible since small NETD value means that the detector can sense very small changes in the target temperature. As eqn. (1.18) states, in order to obtain small NETD values, noise of the overall system and the F-number of the optics should be decreased, while transmission of the optics, detector sensitive area, and detector responsivity should be increased.

1.3   Readout Architectures

There exist different read-out architectures to read pixels of an uncooled microbolometer FPA. These are classified as pixel-wise, column-wise, and serial readout architectures [14]. Pixel-wise readout architecture for an N by M microbolometer array, where N is the number of columns and M is the number of rows, is illustrated in Figure 1-3 [14]. In Figure 1-3, D, A, and I represent the detector, amplifier, and integrator, respectively. As shown in Figure 1-3, each detector requires its own amplifier and integrator in pixel-wise readout configuration. The detector resistance changes in all pixels can be amplified and integrated simultaneously with this configuration which results in low read-out bandwidth, therefore, the total noise voltage decreases. Also, the close placement of amplifiers to the detectors reduces the effect of interference in wire connections. Although pixel-

wise readout architecture has these aforementioned advantages, this architecture is not preferred due to several reasons. Firstly, the total area for an amplifier and integrator pair is limited by the pixel area which is relatively small. Secondly, this architecture suffers from high power consumption due to the large number of amplifiers and integrators that work in parallel.
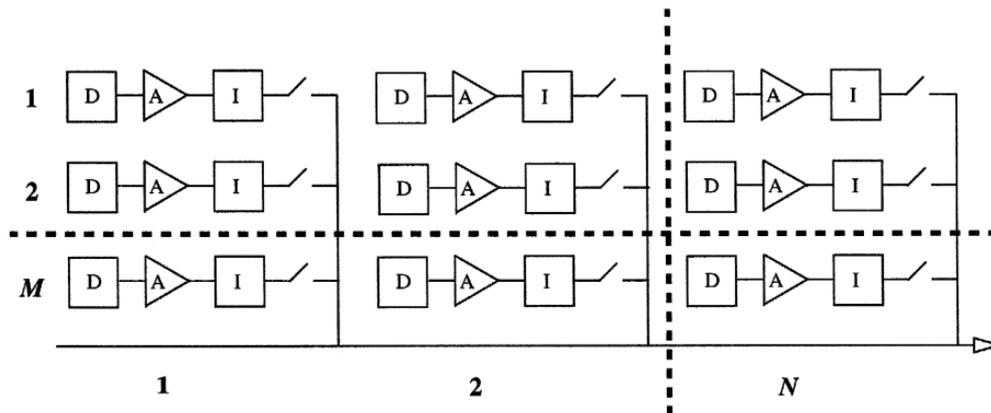
Figure 1-3: Pixel-wise readout.

The other type of architecture is the serial readout that is illustrated in Figure 1-4 [14]. In this architecture, all the pixels are read out one by one, therefore, there is only one amplifier-integrator pair. Although it is compact in layout and it is power efficient, the main disadvantage of this architecture is that the bandwidth of the circuit is very high resulting in higher total noise voltage. Also, this architecture suffers from low frame rates since each pixel is integrated and then read individually.
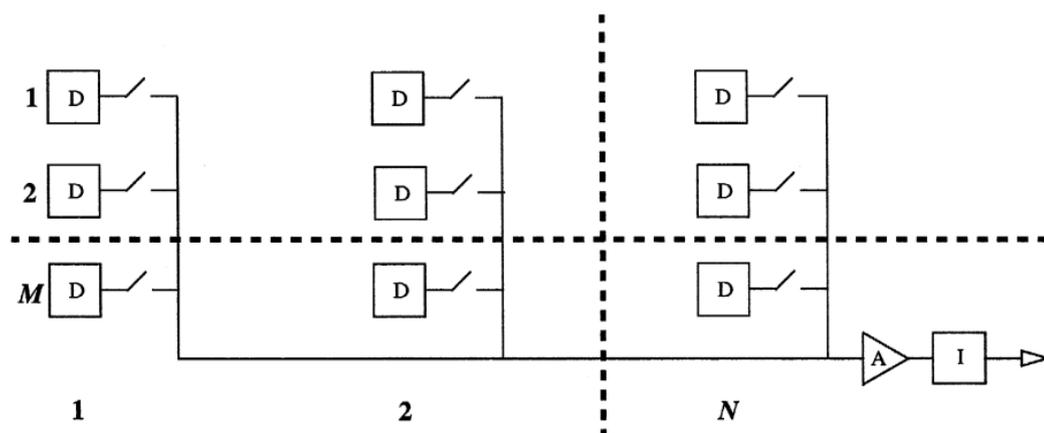
Figure 1-4: Serial readout.

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The last and the most widely used architecture is column-wise readout as illustrated in Figure 1-5 [14]. This architecture is much more practical than pixel-wise architecture since the read-out circuit area is not limited by the pixel area. Also, less number of amplifiers and integrators are implemented in this architecture; therefore, the total layout area and power consumption may not exceed the limits. In column-wise architecture, detector signals are read via row by row fashion. In some cases, single readout channel may be shared by multiple FPA columns. This may be needed to decrease the average power consumption and total noise contribution of the readout channel since larger transistors can be implemented. A typical block diagram of an uncooled infrared sensor which uses column-wise readout architecture is illustrated in Figure 1-6 [15]. As shown in Figure 1-6, typical uncooled infrared sensor is composed of a detector array, an analog biasing block, an analog readout circuit, a digital controller, a row decoder, and a column multiplexer. The digital controller block is used to generate necessary timing signals for row decoder, column multiplexer, analog readout circuit, and external electrical interface. Necessary biasing of analog readout circuit is supplied by analog biasing block. Each pixel in the detector array has its own row select switch. The row decoder selects a single row at a time by enabling switches of the pixels that share the same row. After the selection of a row, the parameter change of the detector due to the absorbed IR radiation is sensed and amplified by the analog readout circuits. This amplified signal is band limited by the integrator inside the analog readout circuit. After the end of the
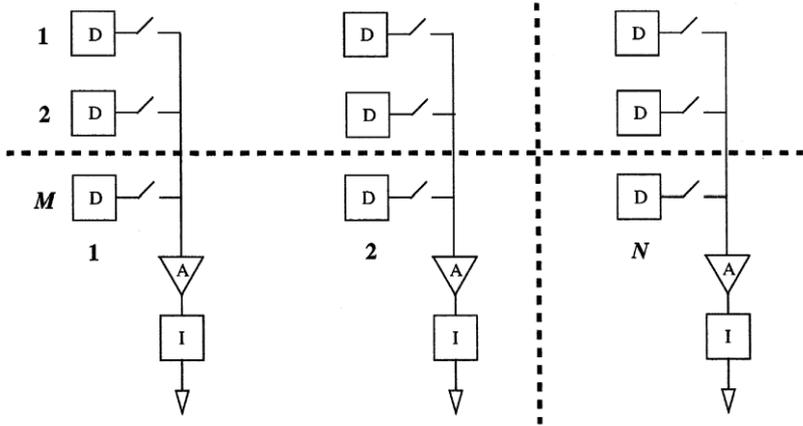
Figure 1-5: Column-wise readout.

integration, the amplified analog voltages are stored in the capacitors inside the readout circuit and then these voltages are read one by one with the help of column multiplexer.
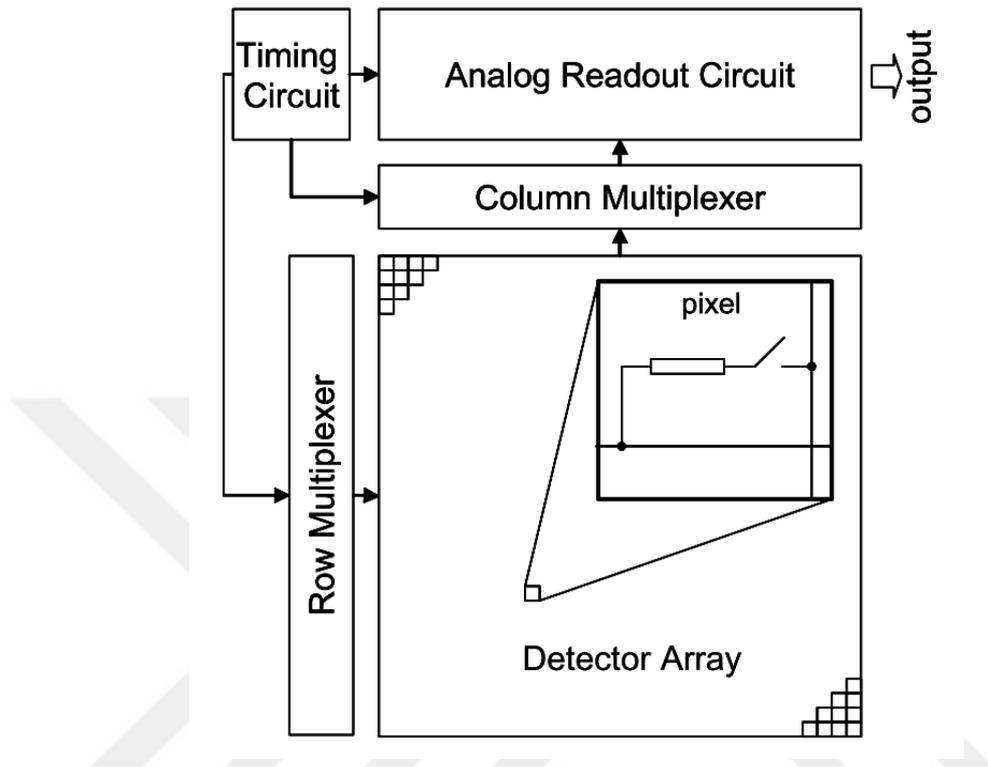
Figure 1-6: A typical block diagram of an uncooled infrared sensor with column-wise readout architecture [15].

1.4 Research Objectives and Thesis Organization

The ultimate goal of this thesis is to develop an advanced circuit architecture which aims at fully on-chip detector bias calibration to correct offsets in pixel output voltages. The specific objectives can be listed as follows:

1. Investigation of non-uniformity sources, which result in detector output offset voltages, in a microbolometer FPA. Understanding the non-uniformity sources is important to develop a non-uniformity calibration technique.

2. Investigation of the effects of offset voltage on the detector performance. These negative effects are actually the push factors for correcting offset. Advantages of eliminating offset are also investigated.

3. Design of the first circuit architecture, which allows specific biasing of each pixel to correct output offset voltage, for 40x40 low cost resistive type microbolometer FPA. The developed circuit architecture should allow communication with the external processor for programming of both sensor configuration and pixel level biasing memory blocks inside the sensor. Also, it should be able to generate its own timing and output synchronization signals using only an externally supplied 1 MHz clock signal to simplify the usage of the sensor.

4. Development of a fast and precise calibration algorithm which is necessary to find the correct biasing value for each pixel in a very short time.

5. Implementation of the developed algorithm using Field Programmable Gate Array (FPGA) which is connected to the sensor for communication and image construction.

6. Design of the second circuit architecture, which allows specific biasing of each pixel to correct output offset voltage, for 80x80 low cost resistive type microbolometer FPA. The developed architecture should allow both manual and on-chip detector bias calibration using the algorithm developed for the first sensor and have enough memory space to store the calibration data of each pixel. In addition to all digital capabilities of the first sensor, it should allow frame windowing, pixel synchronization signal delaying and polarity changing functions.

The rest of this dissertation is organized as follows:

CHAPTER 2 gives information about the sources of offset voltages and its effects on the detector performance briefly. These investigations are based on read-out circuit architectures in which charge trans-impedance amplifier (CTIA) structure is used since both the first and second sensors make use of CTIA structure in their preamplifier stage.

CHAPTER 3 introduces offset correction methods for microbolometer FPAs. Some works on offset correction in the literature are investigated and then the circuit architecture developed for the first sensor is explained along with the designed offset calibration circuit and calibration algorithm.

CHAPTER 4 summarizes the test and characterization results of the first circuit architecture. The overall functional operation of the sensor and the results of the offset calibration algorithm are verified by the tests given in this chapter.

CHAPTER 5 gives information about the design and development of the circuit architecture, which enables on-chip offset calibration, implemented in the second sensor using the experience gained from the first sensor.

CHAPTER 6 summarizes the test and characterization results of the second circuit architecture. The overall functional operation of the sensor and the results of the on-chip offset calibration circuit are verified by the tests given in this chapter.

CHAPTER 7 finalizes the thesis by giving the concluding observations and future works.

CHAPTER 2

ANALYSIS OF DETECTOR OUTPUT OFFSETS IN MICROBOLOMETER FPAs

This chapter focuses on the sources of detector output offsets in microbolometer FPAs in which CTIA circuit architecture is used. The first section of this chapter gives an overview about the CTIA architecture used in both the first and second sensors. Section 2.2 describes the non-uniformity sources that result in offset voltages in microbolometer FPAs. Lastly, the advantages of eliminating FPN are discussed in Section 2.3.

2.1   Introduction

Readout circuit designing is a challenging procedure for the microbolometer based thermal imaging systems. The reason is that IR light power that sheds on the detector active region is very low, therefore, resulting signal current or voltage from the detector is also very low. In fact, it is more challenging to design a readout circuit for cost-effective type microbolometers in which the sensitivity of the active material is much lower than the ones used in high performance microbolometers. Hence, special attention must be paid while designing readout circuits for cost-effective type microbolometer FPAs.

A typical block diagram of a ROIC for microbolometer FPAs is illustrated in Figure 2-1. In Figure 2-1, the detector array is indicated as M x N FPA where M and N can be any number. Digital controller block generates necessary timings for the corresponding blocks. Row decoder performs a dynamic row selection. Column readout channels are used to amplify the signal generated due to the resistance change of pixels when infrared power falls on them. Column multiplexer block selects the outputs of the column readout channels dynamically so that single pixel in

the selected row is read out at a time. Output buffer outputs analog pixel data which is multiplexed by column multiplexer. Bias generator block generates necessary biasing voltages and currents for the analog blocks.
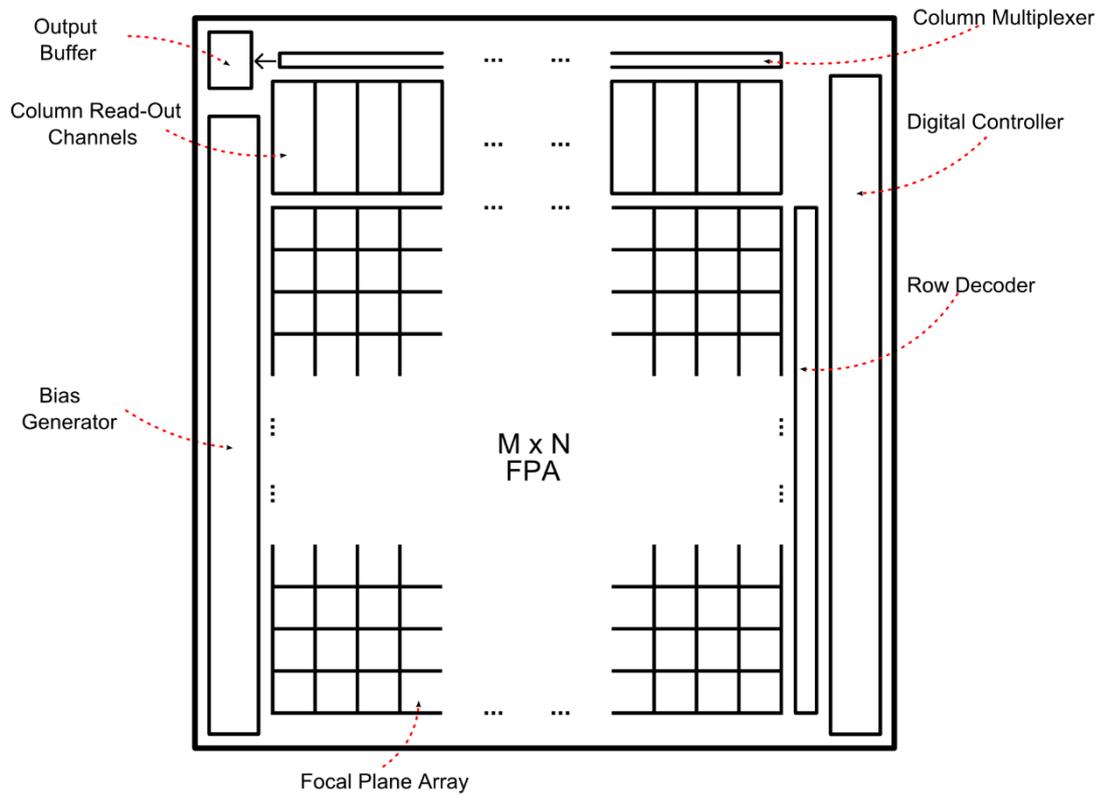
Figure 2-1: A typical block diagram of a ROIC for microbolometer FPAs.

A conventional microbolometer biasing circuit (CTIA) constituting the first stage of column readout channel is illustrated in Figure 2-2. In Figure 2-2, R_{ref} is the reference resistance and R_{det} is the detector resistance of the microbolometer. Selection of R_{det} is done by the row decoder as mentioned before. Note that multiplexing switches in the FPA are not shown in the figure for the sake of simplicity. Two injection transistors M_n and M_p are used to bias reference and detector bolometers. I_{ref} and I_{det} are the reference and detector bolometer currents, respectively. These currents are directly dependent on the gate biases of the injection transistors. Ideally, V_p and V_n biases are adjusted such that the detector current and reference bolometer current cancel each other under the reference infrared illumination which results in zero integration current. When the detector resistance

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changes with the absorption of IR radiation, integration current becomes non-zero. This current is converted into a voltage by the switched-capacitor integrator shown in Figure 2-2. The gain of the switched-capacitor integrator circuit is expressed as

$$\frac{\Delta V_{out}}{I_{int}} = \frac{T_{int}}{C_{int}} (V/A) \tag{2.1}$$

where T_{int} is the integration time, I_{int} is the integration current, ΔV_{out} is the change in output voltage, and C_{int} is the integration capacitance.
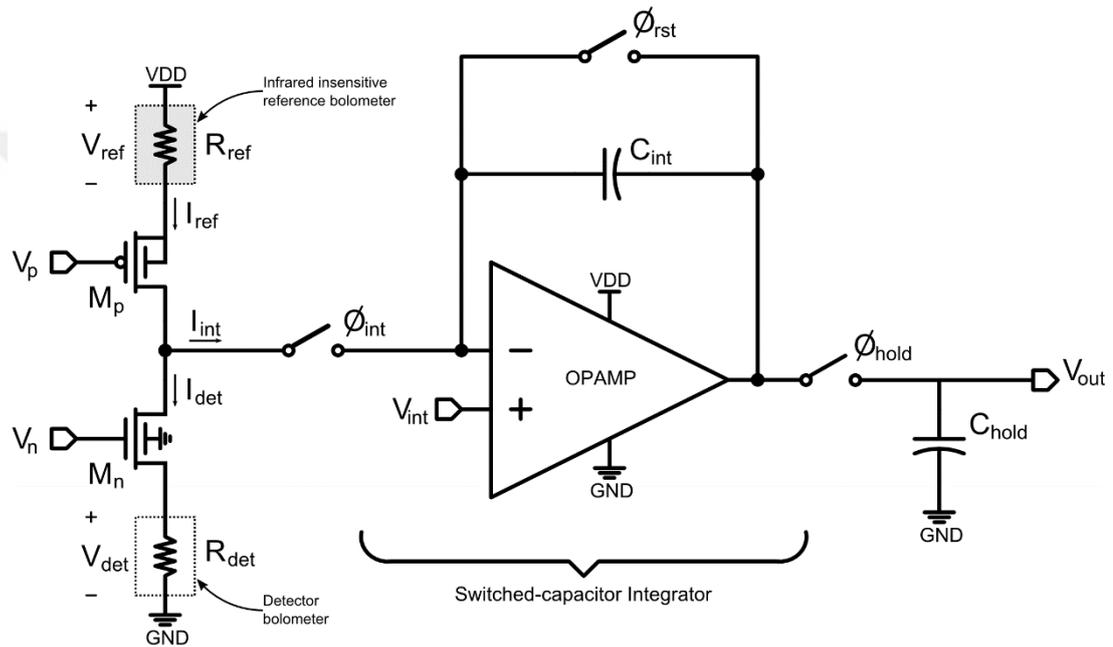
Figure 2-2: A typical microbolometer biasing circuit.

In Figure 2-2, an infrared insensitive reference bolometer is used to cancel infrared irrelevant current. The purpose of the reference bolometer is to generate I_{ref} current that has similar characteristics with the I_{det} current. Therefore, I_{det} is cancelled by I_{ref} and integration current, I_{int}, becomes zero under the reference IR illumination ideally. Also, since substrate temperature change affects both detectors similarly, the reference detector provides less dependency on the temperature of the environment. On the other hand, the reference bolometers are generally designed similar to the detector bolometers except that they are thermally shorted to the substrate. This leads

to an important difference between the detector and reference bolometers called bias heating. Since the detector bolometers are isolated from the substrate, they are heated up when biased; and therefore, the temperature of the detector bolometer becomes higher than the reference bolometer when they are biased. This temperature increase changes the resistance of the detector bolometer resulting in an unwanted integration current. In order to get rid of the effects of bias heating, the reference and detector bias voltages are adjusted so that the integral of the integration current during integration time becomes close to zero.
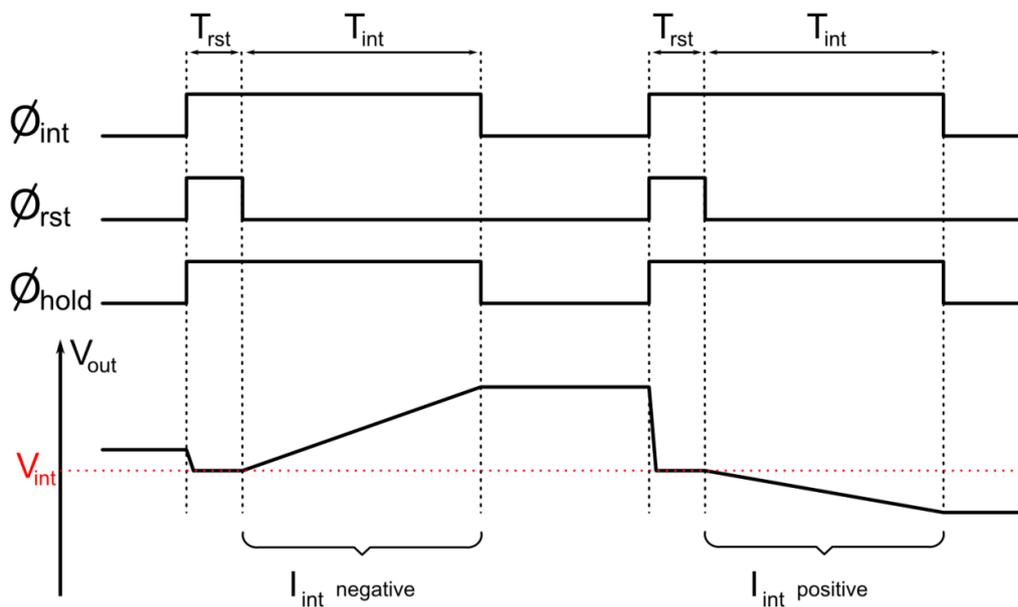
Figure 2-3: Sample timings for reset, integrate and hold switches along with output voltage.

Sample timings for reset ($\emptyset_{rst}$), integrate ($\emptyset_{int}$) and hold ($\emptyset_{hold}$) switches along with output voltage (V_{out}) are given in Figure 2-3. The integration phase starts with resetting the integration capacitance with duration of T_{rst}. At the end of reset operation, V_{out} of switched-capacitor integrator becomes V_{int} due to high open-loop gain of the operational amplifier which also fixes the common node of the injection transistors to V_{int} potential. As a result, the reference and detector bolometer voltages are independent from the integration voltage. Just after the reset signal goes to low

state, integration of I_{int} current onto C_{int} starts. At the end of integration, V_{out} is expressed as follows:

$$V_{out} = V_{int} - \frac{(I_{ref} - I_{det})T_{int}}{C_{int}} = V_{int} - \frac{I_{int}T_{int}}{C_{int}} \qquad (2.2)$$

In general, V_{int} voltage is set as the mid of the supply rails to keep the dynamic range maximum. Depending on the direction of I_{int}, V_{out} may rise or fall as illustrated in Figure 2-3. As stated before, under reference IR illumination, I_{int} must be 0, however, this does not happen due to some non-idealities. Therefore, the offset voltage under reference IR illumination is expressed by the second term of the right hand side of the eqn. (2.2) which is given as

$$V_{offset} = -\frac{I_{int}T_{int}}{C_{int}} \qquad (2.3)$$

where I_{int} is the difference between I_{ref} and I_{det} currents. These currents can be calculated using the saturation equation of the injection transistors. Therefore, I_{det} is expressed as

$$I_{det} = \frac{V_{det}}{R_{det}} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W_n}{L_n}(V_n - V_{tn} - V_{det})^2 \cdot [1 + \lambda(V_{int} - V_{det})] \qquad (2.4)$$

and I_{ref} as

$$I_{ref} = \frac{V_{ref}}{R_{ref}} = \frac{\mu_p C_{ox}}{2} \cdot \frac{W_p}{L_p}(VDD - V_{ref} - V_p - |V_{tp}|)^2 \cdot [1 \\ + \lambda(V_{ref} - V_{int})] \qquad (2.5)$$

where μ_n and μ_p are the mobility of N-channel and P-channel transistors, C_{ox} is the unit gate oxide capacitance, W_n/L_n and W_p/L_p are the aspect ratio of N-channel and P-channel transistors, V_n and V_p are the gate potential of N-channel and P-channel transistors, V_{tn} and V_{tp} are the threshold voltage of N-channel and P-channel transistors, and λ is the channel length modulation coefficient. Eqn. (2.4) and (2.5) result in a lengthy solution that is impractical to be used in many cases. Assuming

that the overdrive voltages of both transistors M_n and M_p are very small for small detector and reference currents, V_{det} can be simplified as

$$V_{det} = V_n - V_{gs,n} \approx V_n - V_{tn} \tag{2.6}$$

and V_{ref} as

$$V_{ref} = VDD - V_p - V_{sg,p} \approx VDD - V_p - |V_{tp}| \tag{2.7}$$

Using eqn. (2.6) and (2.7), we can express I_{int} as follows:

$$I_{int} = \frac{VDD - V_p - |V_{tp}|}{R_{ref}} - \frac{V_n - V_{tn}}{R_{det}} \tag{2.8}$$

One of the purposes of the study in this thesis is to develop a circuit architecture that allows bias calibration of each pixel (V_n) so that integration currents I_{int} for all pixels are almost equal.

There are several non-uniformity sources that affect the offset voltage in microbolometer FPAs. These sources are investigated in Section 2.2. Then, the advantages of eliminating offset in microbolometer FPAs are discussed in Section 2.3.

2.2   Offset Sources in Microbolometer FPAs

The first and the most important source of the offset is the mismatch between the reference and detector bolometers. These mismatches are mainly due to the fabrication non-idealities. The resistance of the each pixel may change across FPA depending on the position of the pixel in the FPA, the die position on the wafer, and random variations of the process parameters. The expected resistance non-uniformity in the high-performance large format FPAs is smaller than $\pm 5\%$ [5]. This amount of non-uniformity may result in saturation of the pixel output voltages and performance degradation of the sensor whose read-out circuit is optimized for sensing very small resistance changes. Even in cost-effective microbolometer FPAs in which detector resistances are fully CMOS based, the non-uniformity is about $\pm 1\%$. Although it is

almost five times smaller than its high-performance counterpart, it still becomes an important issue in the cost-effective microbolometer FPAs also. The reason is that high readout gains are required for this kind of microbolometer FPAs since the resulting signal due to resistance change of the detector with the absorption of IR light is very low when compared to high-performance microbolometers. Also, long integration times are required to decrease the total noise of the system further, and small integration capacitances are used to keep the total die area minimum so that further reduction in sensor cost can be achieved. Moreover, parasitic resistances due to the routing of pixels across FPA are also added to the amount of resistance mismatch between pixels.

Assume that total resistance mismatch on the reference side is ΔR_{ref} and the detector side is ΔR_{det} as shown in Figure 2-4. Moreover, assume that integration current is zero ($I_{ref} = I_{det}$) before adding resistance mismatches and no bias heating occurs. Assume also that ΔR_{ref} is 1% of R_{ref} and ΔR_{det} is -1% of R_{det} which is the worst case scenario in cost-effective type microbolometer FPAs. Then, we can rewrite eqn. (2.8) as

$$I_{int} = \frac{V_{ref}}{R_{ref} + 0.01 R_{ref}} - \frac{V_{det}}{R_{det} - 0.01 R_{det}} \tag{2.9}$$
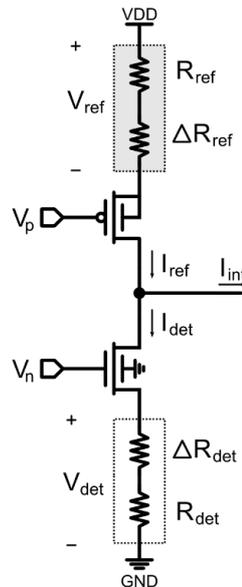
Figure 2-4: Charge injection circuit with added resistance mismatches.

where R_{ref} is generally selected as the same as R_{det}. For a 60 kΩ of detector and reference bolometer resistance with 1.2 V V_{ref} and V_{det} voltages in 3.3 V (VDD) system, the resulting integration current becomes -400 nA. For 100 μs of integration time, 16 pF of integration capacitance and 1.65 V of common node voltage V_{int}, offset voltage V_{offset} is calculated to be 2.5 V which is greater than available voltage headroom (VDD-V_{int}) therefore resulting in saturation of the corresponding pixel output voltage. This problem can be fixed by adjusting the bias of each detector or reference bolometer specifically so that integration current under reference IR illumination gets close to 0. Figure 2-5 shows a sample detector-reference bolometer current and the corresponding output voltage graphs for the cases before and after the calibration of the detector biases. The area A in Figure 2-5 represents the total charge integrated onto integration capacitance C_{int} during integration time, T_{int}. Therefore, the total offset voltage V_{offset} due to the resistance mismatches (ignoring the bias heating effect) can be calculated by dividing A by C_{int}. As shown in Figure 2-5, the calibration of detector biases decreases the difference between I_{ref} and I_{det}; therefore, offset voltage is greatly reduced.
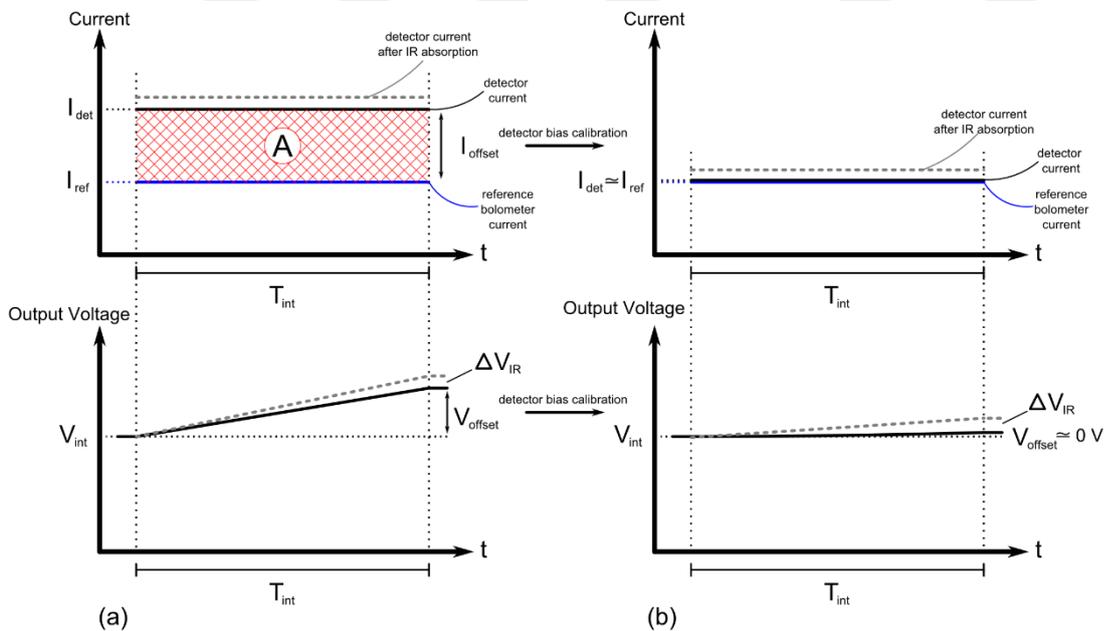
Figure 2-5: The detector-reference bolometer current and integration voltage scheme (a) before the bias calibration (b) after the bias calibration.

The second important source of offset is the bias heating of the detector. As mentioned before, detectors on the FPA are thermally isolated from the substrate so that the IR power absorbed by the detector can create enough temperature change. On the other hand, reference bolometers are generally thermally-shorted to substrate to make them IR insensitive. The power dissipated in the detector resistance heats it up and the resistance of the detector changes significantly. This change is observed as offset on the output, and the amount of offset may differ from pixel to pixel due to C_{th} and G_{th} mismatches of the pixels. The integration current during integration time under bias heating is expressed as

$$I_{int} = \frac{V_{ref}}{R_{ref}} - \frac{V_{det}}{R_{det}(t)} \qquad (2.10)$$

where V_{det} and V_{ref} are the detector and reference bolometer voltages, R_{ref} is the reference bolometer resistance, R_{det} is the detector resistance which changes in time
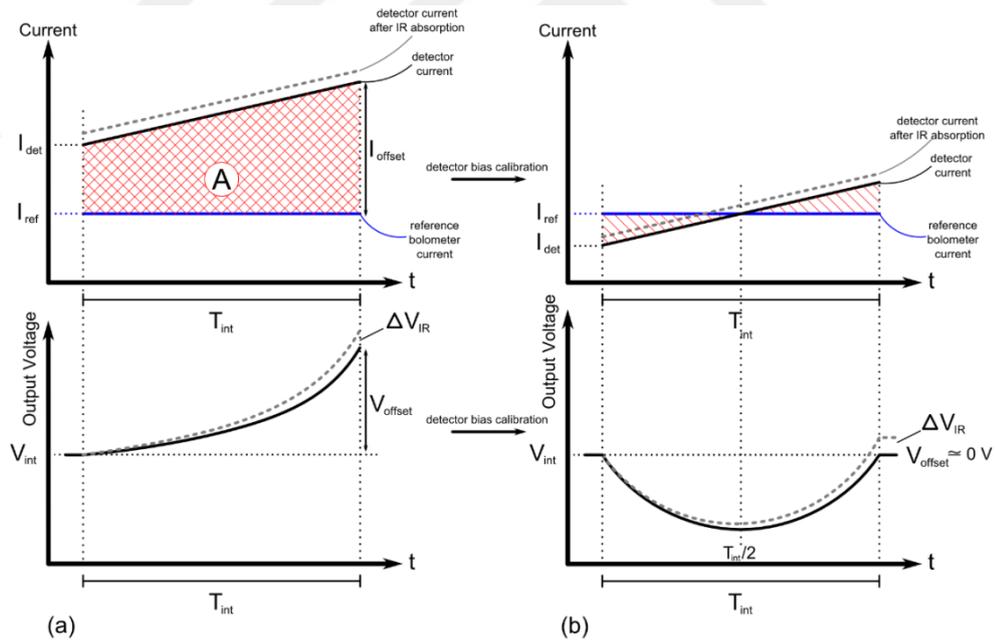
Figure 2-6: The detector-reference bolometer current and integration voltage schemes when bias-heating effect is included (a) before bias calibration (b) after bias calibration.

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during integration due to the bias heating, and t is the time. Assuming that t is much smaller than the thermal time constant, the time dependent detector resistance can be approximated as

$$R_{det}(t) = R_{det0}(1 + \frac{V_{det}^2 \cdot \alpha \cdot t}{R_{det0} \cdot C_{th}})$$ (2.11)

where R_{det0} is the initial detector resistance, α is the detector TCR, and C_{th} is the detector thermal capacitance. As eqn. (2.11) states, the detector resistance shows a linear dependency on time, assuming that the heating duration is much smaller than the detector thermal time constant. Also, Figure 2-6 shows the detector-reference bolometer current and integration voltage schemes when bias-heating effect is included. As shown in Figure 2-6, the change in resistance of the detector due to the bias heating during integration time creates a detector current that is dependent on time linearly. As a result, output offset voltage for the worst case scenario becomes higher. In order to cancel the offset voltage due to both bias heating and resistance mismatch effects, detector bias can be calibrated such that the total integrated charge on the C_{int} during the integration time gets close to 0 as illustrated in Figure 2-6.

The third important source of offset is the mismatch between the integration capacitances of integrators in column readout channels. This mismatch directly affects the gain of integrator stage, which result in column based FPN. The integration capacitance mismatch may become an important issue in cost-effective type microbolometers in which TCR of the IR sensitive material is very low compared to high performance counterparts. Therefore, high readout gains may be needed to amplify the microbolometer signal so that measurable output signal can be obtained. This can be achieved by increasing the integration time and decreasing the size of integration capacitance as eqn. (2.1) states. Decreasing the size of the integration capacitances results in higher mismatches between integration capacitances of readout channels since the percentage of standard deviation increases as capacitor size decreases. The amount of standard deviation due to the mismatch between integration capacitances can be calculated from the pelgrom coefficient for the capacitance mismatch parameter (AC) which is given in the "Process and Device

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Table 2-1: Integration capacitance parameters used in the first and the second sensors. These parameters are obtained from the process design specification files of 0.18 and 0.35 µm CMOS processes.

Sensor	AC (%µm)	C_{int} (pF)	W (µm)	L (µm)	σ (%)	σ (fF)
1st Gen.	0.3	16	80	80	3.875e-3	~62
1st Gen.	0.31	4	40	40	7.750e-3	~31
2nd Gen.	0.23	16	73	73	3.150e-3	~50
2nd Gen.	0.23	4	36.5	36.5	6.300e-3	~25

Specification" document of the corresponding CMOS technology. The relation between the standard deviation σ and pelgrom coefficient AC is expressed as

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{AC}{\sqrt{WL}} \tag{2.12}$$

where σ is the standard deviation in percent, AC is the pelgrom coefficient of capacitance mismatch in %µm, W is the width of the capacitor in µm, and L is the length of the capacitor in µm. The integration capacitance parameters used in the first and the second sensors are given in Table 2-1.

Due to the Gaussian nature of mismatches in a sensor, these integration capacitances are normally distributed with a standard deviation σ. From the three sigma rule, it can be assumed that practical values of integration capacitance lie in the range $C_{int} \mp 3\sigma$. Assume that two readout channels in the second sensor have the same integration currents of 25 nA due to pixel resistance mismatch under reference IR illumination (ignore bias-heating). Assume also that the integration capacitance value is targeted to be 4 pF. Considering the data in Table 2-1, the first readout channel may have ~3.925 pF and the second readout channel may have approximately ~4.075 pF for the worst case scenario. For a typical integration time of 250 μs in cost-effective microbolometers, the output offset voltages for the first ($V_{offset,1}$) and second ($V_{offset,2}$) readout channels are calculated as follows:

$$V_{offset,1} = -\frac{25\ nA\ \times 250\ \mu s}{3.925\ pF} \cong 1592.36\ \text{mV} \qquad (2.13)$$

$$V_{offset,2} = -\frac{25\ nA\ \times 250\ \mu s}{4.075\ pF} \cong 1533.74\ \text{mV} \qquad (2.14)$$

Therefore, under the same integration current condition, the output of the first readout channel differs ~60 mV from the output of the second readout channel due to the integration capacitance mismatch. This difference increases as the integrated current increases. Pixel level bias calibration eliminates unwanted component of the integration current and then the effect of integration capacitance mismatch becomes negligible. The readout circuit dependent other offset sources can be listed as below:

- Injection transistor parameter mismatches between readout channels
    - W/L mismatch
    - V_t mismatch
    - μ and C_{ox} mismatch
- Integration OPAMP input offset voltage and feedback error
- CTIA block switch charge injections
- Line Driver OPAMP input offset voltage and feedback error
- Video output buffer OPAMP input offset voltage and feedback error

Under the same reference or detector bias voltages applied from the gate of injection transistors, the reference or detector currents may differ from one readout channel to another due to injection transistor parameter mismatches. The resulting offset voltage may be obtrusive when the gain is high. The input offset voltages and feedback errors of the OPAMPs, and switch charge injections may contribute few millivolts to the total output offset voltage.

Another offset source is the temperature gradient on the microbolometer FPA. This gradient may come from the placement of the power dissipating blocks on the sensor. Also, the off-chip effects such as some heat generating components on the printed circuit board (PCB) may lead to non-uniform heating of the sensor. This results in offset voltages due to non-uniform heating of pixels that are optimized to be highly

temperature sensitive. The total output offset voltage due to the all sources mentioned above can be minimized by a proper pixel bias calibration circuitry.

2.3   Advantages of Eliminating Offset Using Bias Calibration Method

One of the main works done for this thesis is the development of the on-chip offset calibration circuitry. The typical offset cancellation technique requires an external electronic circuitry to write calibration data in the sensor memory dynamically. On the other hand, a sensor having on-chip calibration circuitry extracts its bias calibration data itself and stores this data in its own memory to read it during pixel biasing. The advantages of eliminating offset voltage and eliminating offset voltage with on-chip circuitry are investigated in this chapter separately. There are many advantages of eliminating offset in a microbolometer sensor using bias calibration method.

Firstly, it minimizes the effects of all aforementioned mismatches that contribute to the offset voltage. Hence, the effect of inevitable mismatches that come from any part of the sensor (microbolometers, injection transistors, switched-capacitor integrator etc.) becomes minimal.

Secondly, the range of substrate temperature for which the sensor can operate without saturation of the pixels is extended. Normally, sensor output voltage histogram shifts to the lower or upper supply rails as substrate temperature changes depending on the readout architecture used. The standard deviation of this histogram is relatively high before bias calibration. When the substrate temperature changes, the pixels corresponding to the tails of the output histogram may start being saturated due to shift in the pixel output voltages. After the bias calibration, the output offset voltage is minimized for the same gain settings and then the standard deviation becomes much smaller. Therefore, the microbolometer sensor may operate without sacrificing any pixel under the extreme environmental temperature conditions.

Thirdly, the detectable object temperature range (dynamic range) increases highly due to the similar reasons mentioned in the second advantage. The narrow output

voltage histogram around the mid of the supply rail creates a huge headroom for the pixels. Thus, objects having extreme temperatures are detected without saturation of the pixel voltages. This may be useful for some applications in which temperature measurement is needed for extremely high or low temperature objects.

Fourthly, the integration capacitances in the readout circuit can have smaller value because higher gain values can be reached without saturation of the pixels. The smaller integration capacitance means a smaller layout area filled by integration capacitors and as a result a smaller die area is obtained which reduces the cost further. This is especially important in cost-effective type sensors in which number of dies on a wafer is tried to be maximized. However, it should be noted that as gain increases, the detectable object temperature range and operable substrate temperature range decreases.

Fifthly, very high readout gains can be achieved. High readout gains may be needed to relax the requirements of analog-to-digital converter (ADC) to be used with/within the sensor. High readout gain means higher amplification of the signal generated by the resistance change of the microbolometer; and therefore, the minimum detectable infrared power generates higher output voltage change. This change can be measured by an ADC with lower resolution, which has a lower cost when compared to a high resolution one. Also, since the smaller layout area is used by the lower resolution ADC, the effect of ADC on the sensor cost is reduced when the on-chip ADC is implemented.

Lastly, the bias calibration makes high integration times possible, which reduces the bandwidth of the system, and therefore, lower noise voltages are achieved. Normally, high integration times are hard to achieve without bias calibration since the integration time increases the readout gain resulting in an increase in the standard deviation of the output voltage histogram. If this standard deviation increases too much, pixels corresponding to the tails of the histogram start being saturated as mentioned before. In cost-effective thermal sensors the sensitivity of the active material is much less than their high performance counterparts. Hence, higher integration times are necessary to decrease the total noise further so that acceptable

signal-to-noise ratio can be achieved in cost-effective IR sensors. The drawback of increasing the integration time is that the frame rate decreases as integration time increases. However, this is not a problem for low cost imaging systems since they operate at low frame rates like 9 Hz.

In addition to these advantages, the offset cancellation through fully on-chip bias calibration circuitry has many other advantages that are listed as follows:

o It provides simplification of the camera electronics. No external digital signal processors (DSPs) or high-performance processors are needed for extracting calibration data.

o The total cost of the camera system is reduced with the elimination of high-cost processors. This is especially important when cost-effective IR sensor is used in the camera system.

o The electrical interface between the sensor and external electronics becomes simpler.

o It provides less power consumption on system level due to the elimination of high performance processors. This is also important for cost-effective type IR sensors because the main market of these sensors includes consumer electronics, internet of things (IoT), machine vision etc. in which battery operated IR cameras may be needed. By the help of on-chip bias calibration, the battery life of these systems can be extended.

CHAPTER 3

OFFSET CALIBRATION METHODS FOR MICROBOLOMETER FPAs

The first circuit architecture designed in the scope of this thesis is composed of bias calibration, digital controller, serial peripheral interface, row decoder, and column multiplexer circuits, which are optimized for 40x40 resistive microbolometer FPAs that use CMOS based polysilicon as the temperature sensitive material. The designed circuit is embedded into the first sensor which is fabricated with 0.35 μm CMOS technology. The sensor includes 22 readout channels, each of which reads two columns of the microbolometer FPA.

This chapter is organized as follows: Section 3.1 provides brief information about the works made for the first part of this thesis work. Section 3.2 gives some bias calibration architectures in the literature. Then, the development of the detector bias calibration circuit along with the simulation results are given in Section 3.3.

3.1 Introduction

As mentioned in Section 1.4, one of the goals of this thesis is to develop circuit architecture optimized for the readout electronics of resistive type cost-effective 40x40 microbolometer FPA including all digital blocks such as the bias calibration circuit, digital controller, row scanner, column multiplexer, sensor memory, and serial peripheral interface. This circuit architecture has been designed and implemented in the first sensor. The designed circuit allows programming of both sensor configuration memory and calibration data memory separately from any external microcontroller or FPGA through standard SPI communication interface. This programmability allows sensor operation over a wide range of conditions and provides a large degree of flexibility. Figure 3-1 shows the layout view of the first

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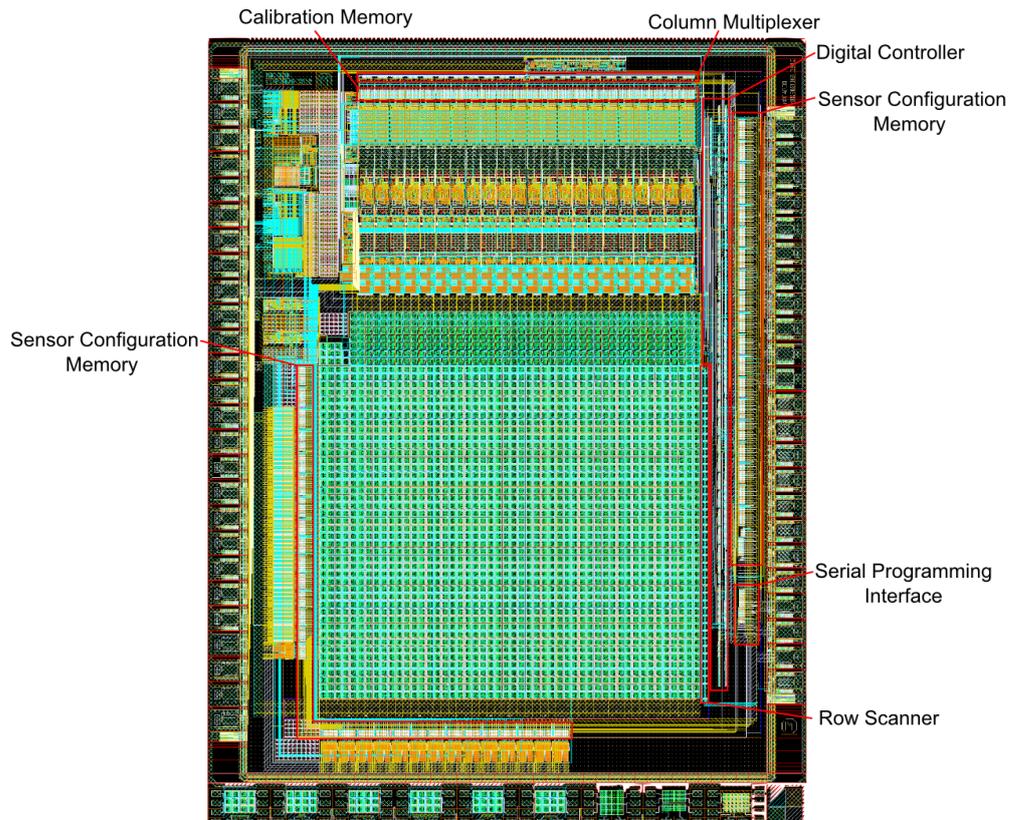
Figure 3-1: The layout view of the first sensor. The designed digital blocks for the first part of this thesis are shown inside the red boxes.

sensor which occupies 4.7 x 5.9 mm^2 silicon area. The layouts of the circuits developed for the first part of this thesis are shown inside the red boxes in Figure 3-1. The digital I/O level of the sensor was designed to be 3.3 V which is compatible for most of the microcontroller and FPGA based systems. The first sensor provides different synchronization signals to ease the interface between the sensor and external electronics. Some of the programmable features implemented in the first sensor are given as below:

- Repeated read operation of the selected row before passing to the next row
- Fixed or externally programmable pixel biasing
- Bi-directional column multiplexing (left-to-right or right-to-left)
- Bi-directional row scanning (top-to-bottom or bottom-to-top)

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- On-chip temperature sensor voltage output from video-output pad
- Selectable fast or slow image data output modes
- Programmable integration and reset times
- Programmable frame rate without changing the system clock speed
- Selectable reference detector
- First reset, then read operation to cancel the contribution of the readout noise

3.2   Calibration Methods

There are different methods proposed for resistance non-uniformity compensation of microbolometer FPAs in the literature. Belenky et al. [16] propose that the dynamic range of the readout integrated circuits designed for microbolometer sensors can be expanded by subdividing the total integration time into several integration times which are progressively shorter. The method suggests that the dynamic range of the microbolometer sensor can be increased by resetting the integrator at certain time points at which output of the selected row exceeds the predefined threshold voltage and storing the number of reset operation, which is used to calculate actual voltage representation of the detector integrated current value, in a memory during integration. The proposed readout architecture by Belenky et al. is given in Figure 3-2 [16]. Although this method does not compensate the effect of non-uniformity on the pixel output voltage, it just prevents output voltage from being saturated by multiple integrations. There are several drawbacks of this architecture. Firstly, it requires utilization of a comparator in each column readout channel which increases the total power consumption and occupies an extra layout area. Secondly, this architecture does not cancel unwanted integration current; and therefore, readout circuit gain is limited by the number of bits available in the memory unit. Lastly, it complicates the interpretation of the pixel output voltages by the external electronics.

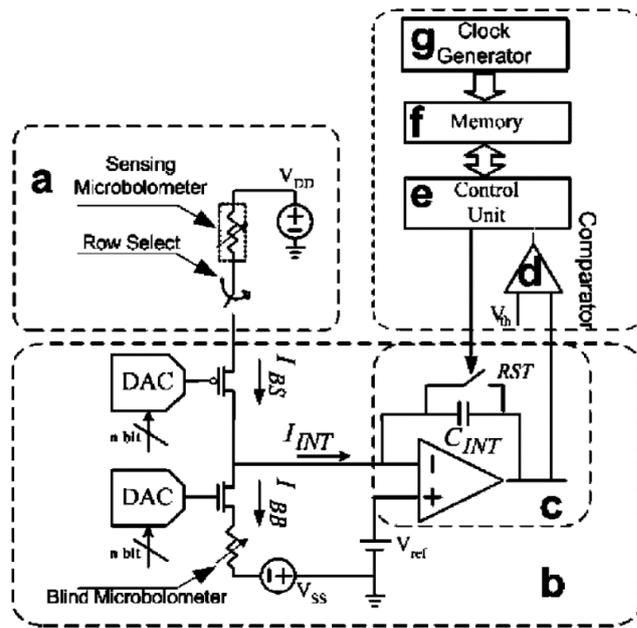Figure 3-2: Proposed readout architecture by Belenky et al. for improving dynamic range of the microbolometer sensors. (a) sensing microbolometer, (b) Sofradir and Indigo companies' ROIC, (c) CTIA circuit, (d) analog comparator, (e) control unit (f) digital memory, and (g) clock generator [16].
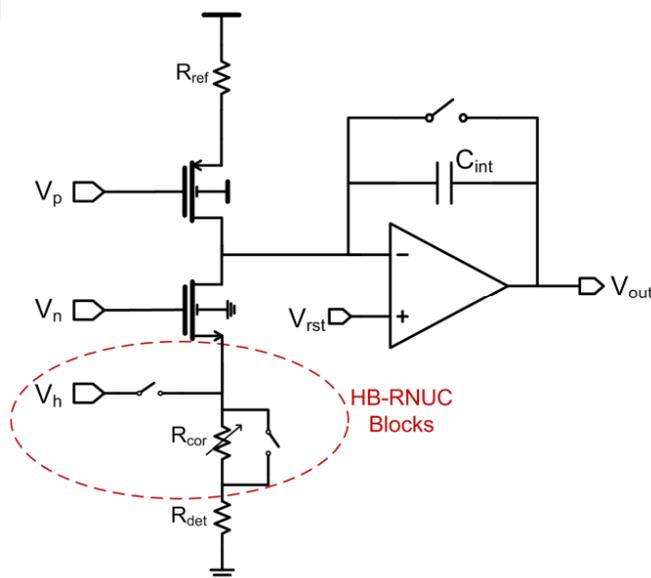

Figure 3-3: The schematic of the CTIA type preamplifier in the readout channels, with the HB-RNUC related components added [18].

Another method for resistance non-uniformity compensation is proposed by Tepegoz et al. [17], [18]. This method suggests that pixel resistance non-uniformity can be compensated through heating based resistance non-uniformity compensation (HB-RNUC) that utilizes a configurable bias heating duration for each pixel in order to minimize the ROIC output voltage distribution range. HB-RNUC method proposes modifying the resistances of the pixels instead of the bias voltages through heating of pixels for a specific amount of time before the readout operation. The proposed schematic of the CTIA type circuit implementing HB-RNUC is given in Figure 3-3. The idea behind HB-RNUC is that the mismatch between detector and reference pixels can be corrected by adding or subtracting resistance from the detector pixel resistance. The addition of resistance is done by the programmable correction resistance R_{cor} connected to the detector resistance serially as seen in Figure 3-3. On the other hand, subtraction of resistance is simply realized by heating the detector pixel up prior to the readout operation. The calibration data for the amount of correction resistance to be added and the heating time for each pixel is found and then stored in the memory so that it can be read from the memory during row scanning. There are several drawbacks of this method. Firstly, the programmable correction resistance requires an extra layout area due to the addition of different values of correction resistances and their selection switches. Secondly, since it utilizes electrical heating source to reduce detector resistances, this method increases the total power consumption of the sensor significantly. Lastly, the duration of the detector heating phase is defined by the detector with highest resistance which may take relatively long heating time to lower the detector resistance. This long heating time may lead to decrease in frame rate, which is not desirable.

The next and the most widely employed method in commercially available microbolometers is using a digitally programmable on-chip detector bias regulation to adjust the bias of each pixel [19]. Adjusting the pixel and reference bolometer biases allows cancellation of unwanted current that leads to offset voltage. This can be done simply by placing digital-to-analog converter (DAC) into each readout channel. However, for large format arrays, placing DAC into each readout channel may be problematic due to the power consumption and area limitations. To overcome

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this issue Toprak et al. [19] proposes a two-stage DAC architecture for bias correction in uncooled microbolometer arrays. In this architecture, the first DAC stage generates the voltage interval that covers the bias voltage range of the overall FPA, while the second DAC stage is used to generate finely tuned voltage biases for pixel specific biasing. Simplified block diagram of the 2-stage bias correction DAC architecture proposed by Toprak et al. is given in Figure 3-4. In Figure 3-4, the first stage DAC generates the maximum and minimum voltage levels for all second stage DACs in column readout channels. These voltage levels are buffered and supplied to the second stage DACs which create finer voltage levels for the biasing of each pixel specifically. Hence, the first stage DAC is used for coarse tuning, while the second stage DACs are used for fine tuning of the pixel biases. This simple method allows a wide range of resistance non-uniformity correction without sacrificing the frame rate and increasing power consumption of the sensor.
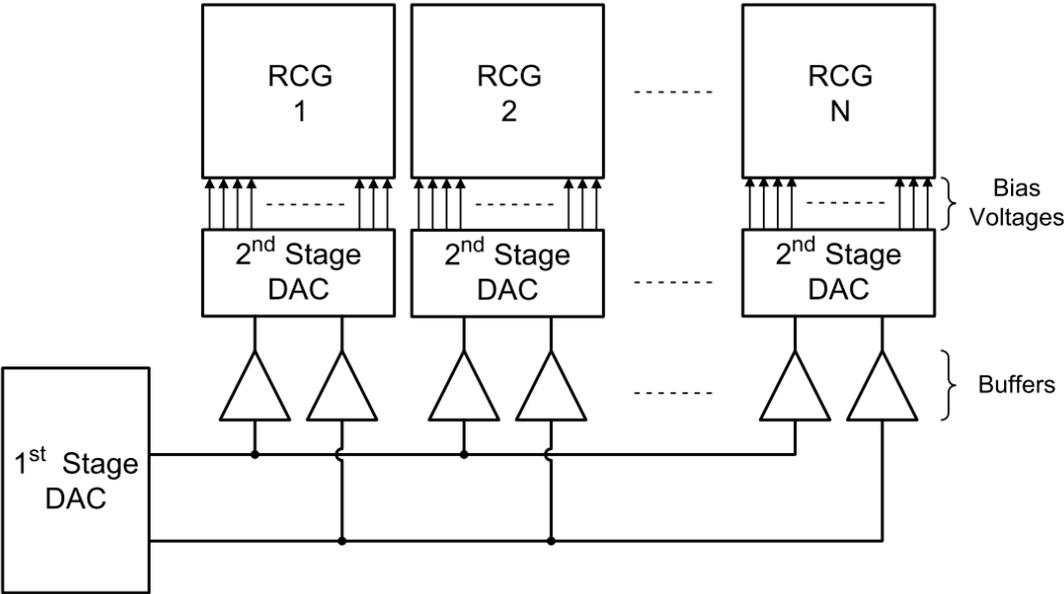

Figure 3-4: Simplified block diagram of the 2-stage bias correction DAC architecture proposed by Toprak et al. [19].

3.3   Detector Bias Calibration Development for the First Sensor

Each pixel of the first sensor contains CMOS based polysilicon resistor as temperature sensitive material. The advantage of using CMOS based polysilicon as temperature sensitive material is that the resistance mismatch between pixels are relatively low when compared to their high-performance counterparts such as a-Si or VO_x. The main disadvantage is that their sensitivity is almost 10 times lower than their high performance counterparts. Therefore, in order to increase signal-to-noise ratio of polysilicon based detector, high integration time becomes necessary since as integration time gets higher, the electrical bandwidth is reduced and then the total RMS noise at the output is reduced leading to higher signal-to-noise ratio. However, high integration time increases readout gain linearly; and therefore, the effects of resistance mismatch on the output image leaps to the eye due to the increase in standard deviation of the sensor output histogram. The bias calibration method implemented in the first sensor uses two-stage DAC architecture to apply pixel specific biasing through the gate of the injection transistors in readout channels. The implemented circuit is similar to the work in [19] but it uses only one first stage and one second stage DACs. The details of detector bias calibration circuit in the first sensor are given in Section 3.3.2 after the analysis of overall sensor architecture in Section 3.3.1.

3.3.1   Sensor Architecture

Overall block diagram of the first sensor is given in Figure 3-5. As shown in Figure 3-5, readout block is located on top of the FPA. Each column readout channel is assigned to two FPA columns for read operation. When the sensor is in the frame capture mode, first odd FPA columns and then even FPA columns are read out during row time by the corresponding column readout channel. The selection of odd or even FPA columns is achieved by FPA column select switches. Therefore, 22 column readout channels are used for reading of 44x42 FPA and image data is acquired in interlaced fashion by the external electronics. Analog block generates
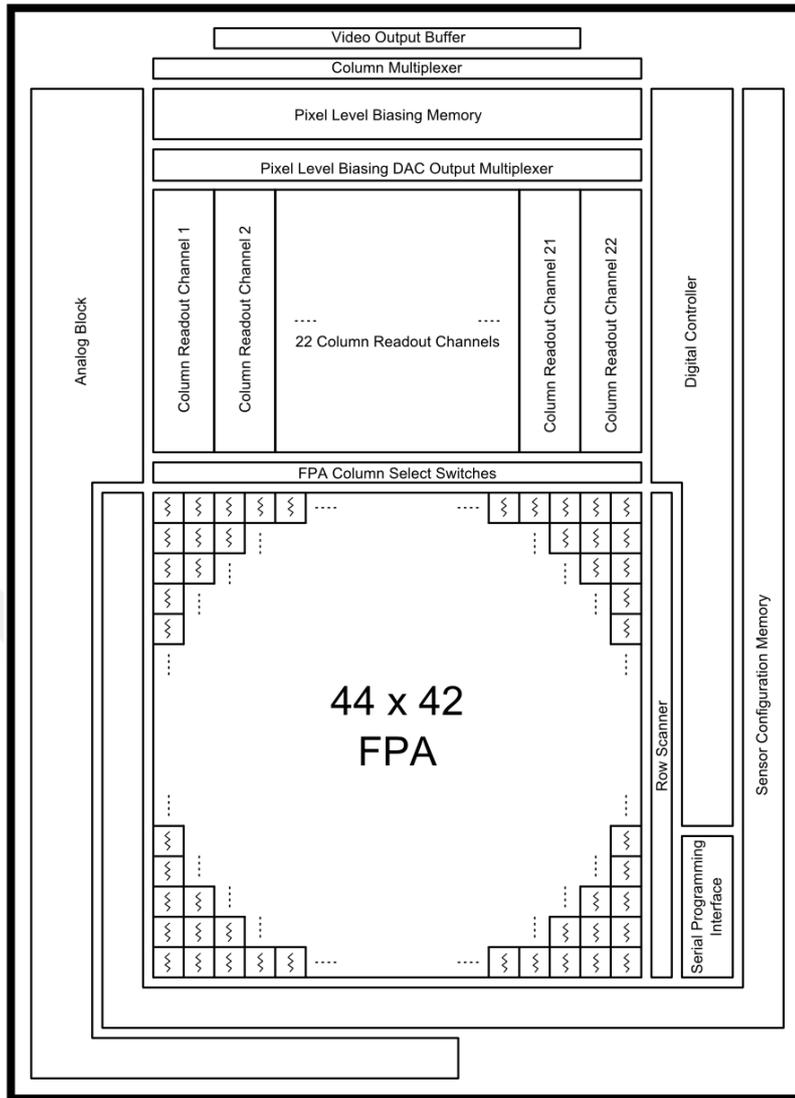
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Figure 3-5: Overall block diagram of the first sensor.

necessary biasing for column readout channels, pixel level biasing (PLB) and video output buffer. It includes 2-Stage DAC for detector bias calibration. PLB DAC output multiplexer block selects a biasing voltage from the second stage of calibration DAC and passes it to corresponding column readout channel. The select bits of the PLB DAC output multiplexer are provided from the PLB memory which is programmed dynamically by the external electronics before detector signal integration. The column multiplexer block is used to connect the output of each readout channel to the input of video output buffer. Row scanner is used to select

one FPA row at a time. Digital controller block generates necessary timings for row scanner, FPA column select switches, column readout channels, pixel level biasing memory and column multiplexer. The first sensor has a high degree of operational flexibility thanks to the programmability of many sensor configurations through serial peripheral interface block. Configuration data is stored in the sensor configuration memory which is distributed from digital to analog block along the bottom of the sensor. All the current and voltage biases are finely tuned with the help of sensor configuration memory and DACs in the analog block.

3.3.1.1   Pixel Array

The first sensor FPA consists of 42x44 resistive microbolometer pixels. The first row, the last row, the first two columns and the last two columns of the FPA are composed of IR blind pixels, while the remaining pixels are IR sensitive as illustrated in Figure 3-6. IR blind pixels are unsuspended microbolometer structures simply. Each pixel in the FPA contains a row select switch and a microbolometer
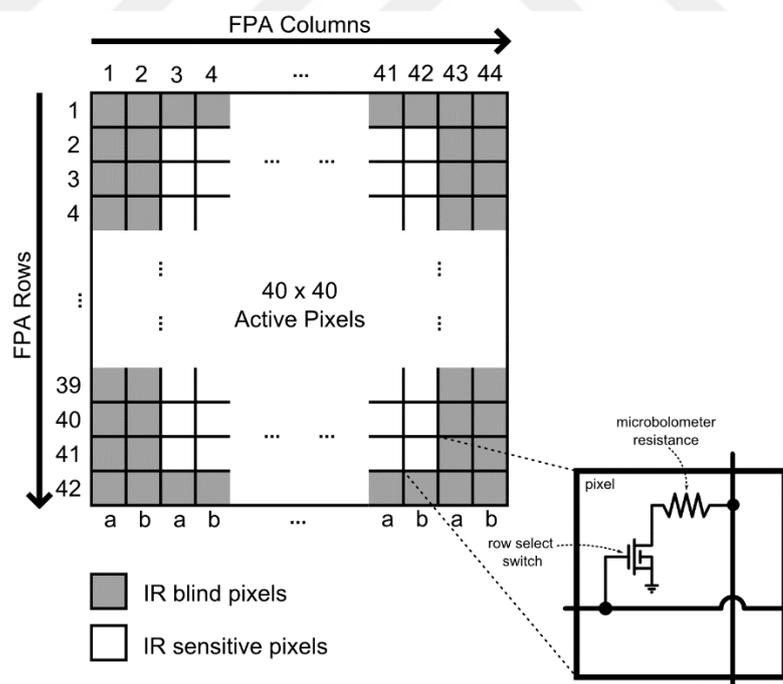
Figure 3-6: Illustration of FPA structure in the first sensor.

resistance. The selection of a row during read operation is accomplished by the row select switch. This switch connects one port of the microbolometer resistance to ground, and the other port is connected to the common column bus constantly. The microbolometer signal is carried by this bus to column readout channel.

3.3.1.2 Column Readout

The first sensor accommodates 22 readout channels, each of which is responsible for reading of two FPA columns. The selection of FPA columns is accomplished by FPA column select switches. The block diagram of the column readout channel is illustrated in Figure 3-7. As shown in Figure 3-7, biasing of the detector and reference bolometers is applied to the gate of injection transistors via 6-bit DACs, whose maximum and minimum voltage levels are adjusted by first-stage 10-bit DACs. By this way, the precise bias adjustment can be made. The timings of the column readout switches along with row and column select switches are shown in Figure 3-8. The selection of odd columns, even columns and rows of the pixel array is accomplished by $\emptyset_a$, $\emptyset_b$ and $\emptyset_{row}$ switches. After the selection of a row, $\emptyset_{sta}$ switch is closed until the start of integration. This keeps injection node away from being floating and allows stabilization of this node before integration starts. Just after the opening of $\emptyset_{sta}$ switch, $\emptyset_{int}$ and $\emptyset_{rst}$ switches are closed simultaneously and
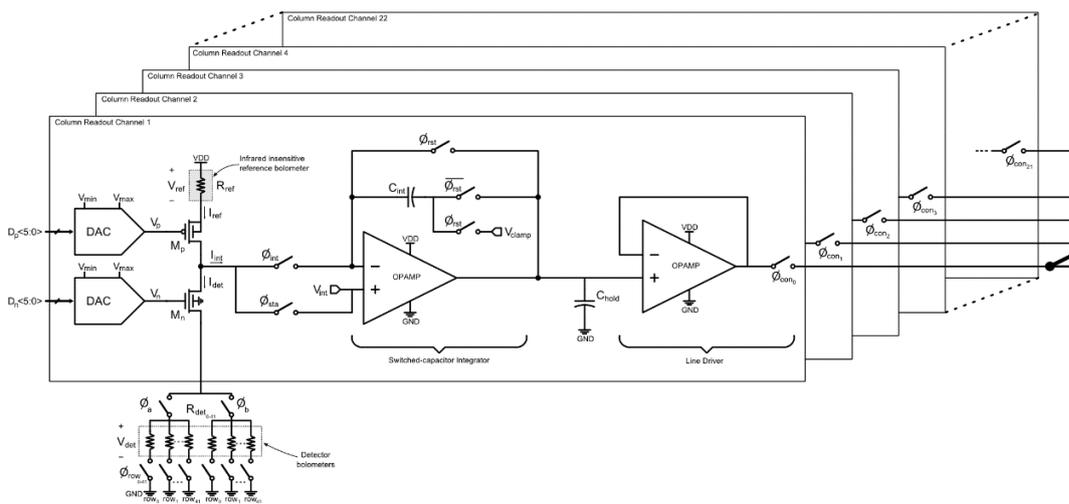

Figure 3-7: Column readout channel.

reset operation starts. Then, $\emptyset_{rst}$ switch goes back to open state and integration starts. At the end of integration, the resulting voltage due to the integrated current on the integration capacitor is stored on the hold capacitor C_{hold}. This voltage is buffered by the line driver and transferred to the input of video output buffer through output multiplexing switches.
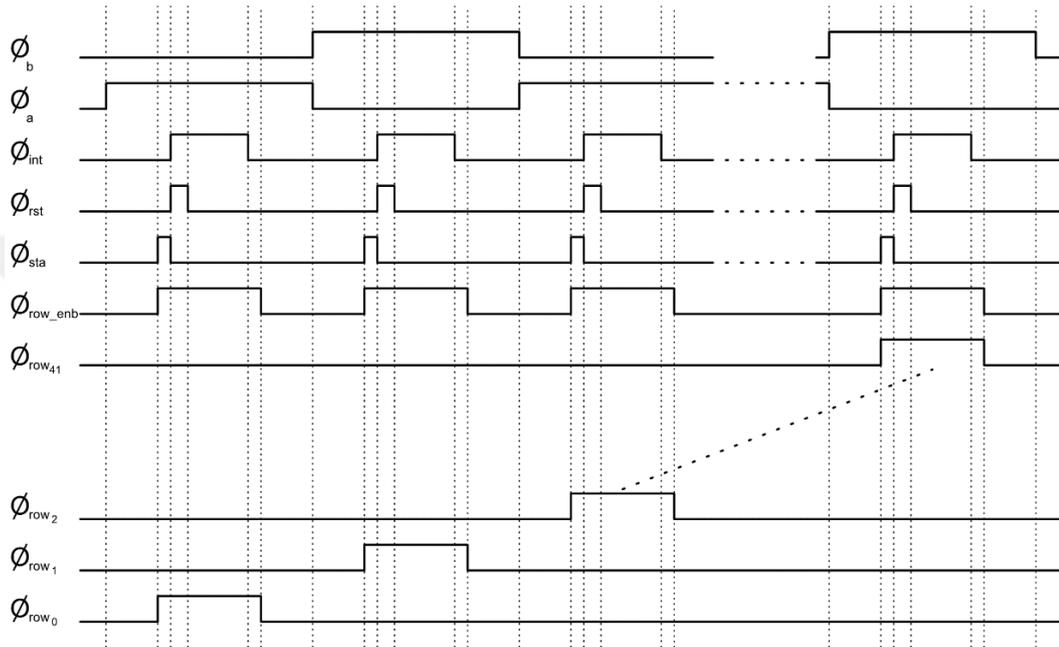

Figure 3-8: Timings of the column readout switches along with row and column select switches.

3.3.1.3 Digital Controller

The main purpose of the digital controller designed for the first sensor is to generate necessary timing signals for the ROIC, using the information stored in sensor configuration memory. Many of these timings are designed to be adjustable through SPI of the sensor to increase the operational flexibility. The block diagram of the digital controller is given in Figure 3-9. There are three main units in digital controller; state machine, counters & comparators and timing generator. The state machine is the core section of the digital controller block and controls operational states of the sensor. The state diagram of the state machine is shown in Figure 3-10.

Each state of the state machine (except Initiation state) is associated with a counter & comparator pair, which defines the duration of corresponding state according to the information stored in the sensor configuration memory. In Figure 3-10, arrows indicate the triggering of the next state pointed by that arrow. At each triggering, the counter corresponding to the pointed state is incremented once. If the counter value of the pointed state becomes equal to the limit defined by the sensor configuration memory, then the counter of that state is reset and the next state is triggered by the red arrow. The state machine is initiated by the Start signal which comes either from the sensor configuration memory or start pad of the sensor. Initiation state only checks the level of Start signal. If it is high, it triggers the next state once, otherwise, it waits until a Start signal is applied. Once the next state is triggered, it cannot be stopped until the end of the frame even if the Start signal becomes low during the frame capturing mode. All the delay states shown in Figure 3-10 were added to put some programmable delay times between critical events so that they can be adjusted according to application requirements. Frame Delay Repeat and Frame Delay states are used to adjust the delay time between two consecutive frames. Since 10-bit counters are assigned to both of these states and the clock frequency of the sensor is 1 MHz, maximum 1.048576 (1024x1024 µs) seconds of delay can be added between successive frames. Row state is used to keep track of the row number. Since both integration and read operations are done twice for a selected row during a row time, the Row Repeat state is used to accomplish this task. PLB Pre-loading Delay state defines the time duration between the latest Read operation and the incoming PLB Loading event. The PLB Loading state defines the duration assigned for the loading of the detector biasing data. After the loading of the detector biasing data, Pre-integration Delay state comes which is also used to add some delay between the end of the detector biasing data loading event and the beginning of the integration event. Pre-integration delay provides to spare some time to settling of detector biasing DAC outputs. The Integration Repeat state defines the number of repetitions of integration event. By the help of this state, the same row can be integrated more than once; therefore, some advanced noise cancelling methods can be implemented such as Correlated Double Sampling (CDS). The total integration event duration is defined by the Integration state in which column readout switching signals are generated. At

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the end of Integration State, the outputs of all pixels in the selected row are stored in the hold capacitors as analog voltages. The end of Integration state is followed by Pre-read Delay state that is similar to other delay states defining the time between the former and next states. Finally, after Pre-read Delay state, Read state comes in which transferring of pixel output voltages to off-chip electronics is done through column multiplexer and video output buffer.
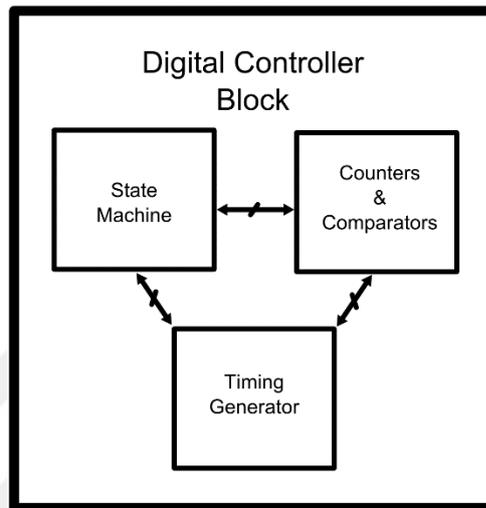

Figure 3-9: Block diagram of the digital controller.

The Timing Generator unit checks the current state of the sensor and generates necessary timings using the information that comes from Counters & Comparators unit. It generates driving signals for column multiplexer, row scanner, column readout channels etc. In addition to them, output synchronization signals called *vsync*, *hsync*, and *pixsync* are also generated by this unit. These output synchronization signals eases the sampling of pixel output voltage and image construction by the external electronics. These signals are illustrated in Figure 3-11 along with analog video output signal, *avout*. Among these signals, *vsync* and *hsync* are used for vertical and horizontal synchronizations, respectively. The signal *vsync* goes to high and returns back to low at the beginning and end of each frame, respectively. On the other hand, *hsync* is high whenever analog video output is ready to be multiplexed. In addition to these signals, *pixsync* is used to signify the time for which the analog video output data on *avout* pad should be sampled by external

camera electronics. Therefore, using all of these synchronization signals, the position of the pixel whose output is sampled can be found easily. As illustrated in Figure 3-11, two consecutive *hsync* pulses correspond to reading of single row due to the interlaced fashion. For each pair of the *hsync* pulse, first pulse corresponds to reading of odd FPA columns while the second one corresponds to reading of even FPA columns. Also, in each *hsync* pulse, 22 *pixsync* pulses are generated each of which corresponds to single readout channel output.
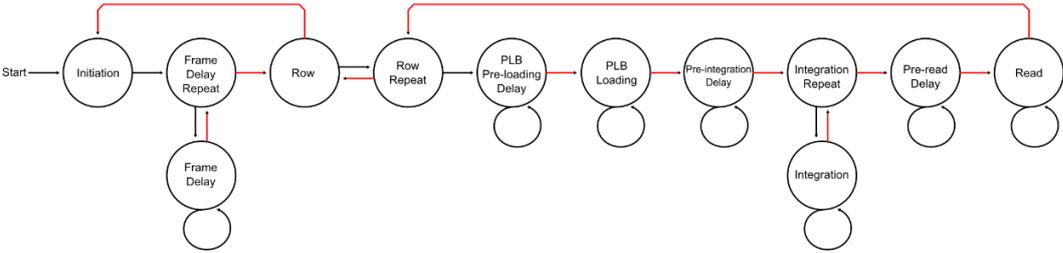

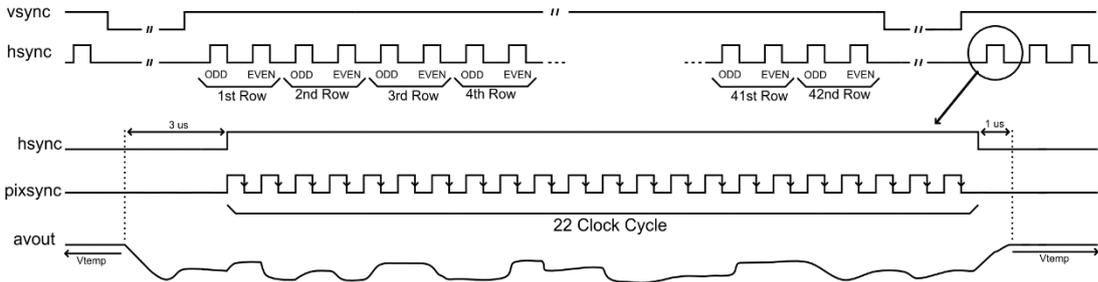Figure 3-10: State diagram of the state machine.

Figure 3-11: Illustration of output synchronization signals.

Since the frame rate constraint of these cost effective IR sensors is not strict, slow read operation can be activated which provides longer available time for settling of the video output buffer and lower sampling rate requirement for analog-to-digital converter (ADC) to be used with the sensor. The lower sampling rate requirement for ADC decreases the cost of the camera system further since they are cheaper than high sample rate counterparts generally. Therefore, slow read mode is implemented in the first sensor. The frequency of *pixsync* pulses is equal to the sensor clock frequency which is 1 MHz normally. With the activation of slow read mode, *pixsync*

frequency is slowed down to 500 KHz by the digital controller unit and all the other timings are kept the same.

3.3.1.4 Row Scanner and Column Multiplexer

Row scanner is used to scan FPA rows in rolling line fashion. The designed row scanner allows bidirectional scanning of the FPA from top to bottom or bottom to top. It is actually a 42-bit shift register with bidirectional shifting property and its schematic is illustrated in Figure 3-12. As shown in Figure 3-12, multiplexer is used to change the scanning direction according to the value of select bit *dir_rs* from the sensor configuration memory. At the beginning of each row time, the pulse *clk_rs* is generated and data in the row scanner circuit is shifted once. The pulse *coin_rs* is generated by the digital controller at the beginning of each frame as the input data of the shift register. The output of the each shift register bit is anded by *row_enb* signal so that excessive biasing of pixels can be prevented. The timings for *row_enb* along with the outputs of row scanner are illustrated in Figure 3-8.

The column multiplexer block is used to connect the outputs of line drivers to two column readout analog video output busses sequentially. It has also bidirectional shift register structure as shown in Figure 3-13. While one of these video output buses is connected to odd numbered readout channels, the other one is connected to evenly numbered readout channels through column multiplexer switches sequentially during Read state. These two busses further multiplexed and connected to the input of the analog video output buffer through bus select switches $\emptyset_{bus_a}$ and $\emptyset_{bus_b}$ as illustrated in Figure 3-14. As shown in Figure 3-14, there is also $\emptyset_{temp}$ switch which connects the analog output of internal temperature sensor to input of the analog video output buffer when the sensor is not in Read state. Timings of column multiplexer and video buffer input select switches along with *pixsync* are given in Figure 3-15.
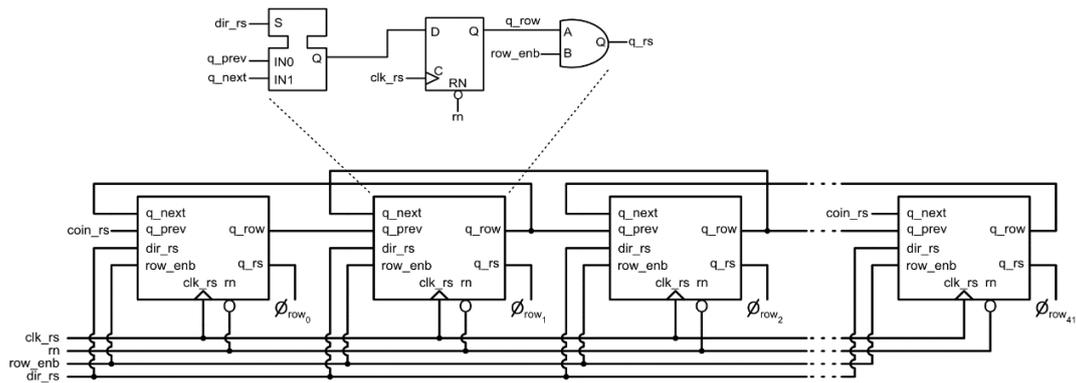
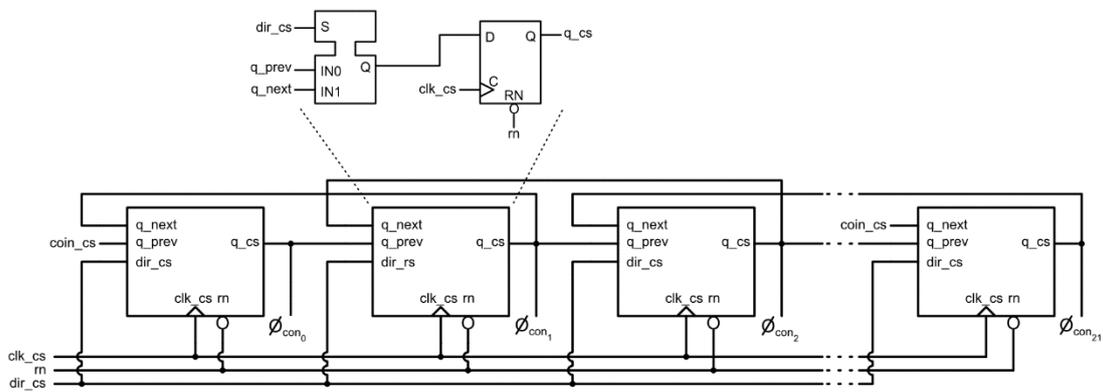Figure 3-12: Schematic of the row scanner.

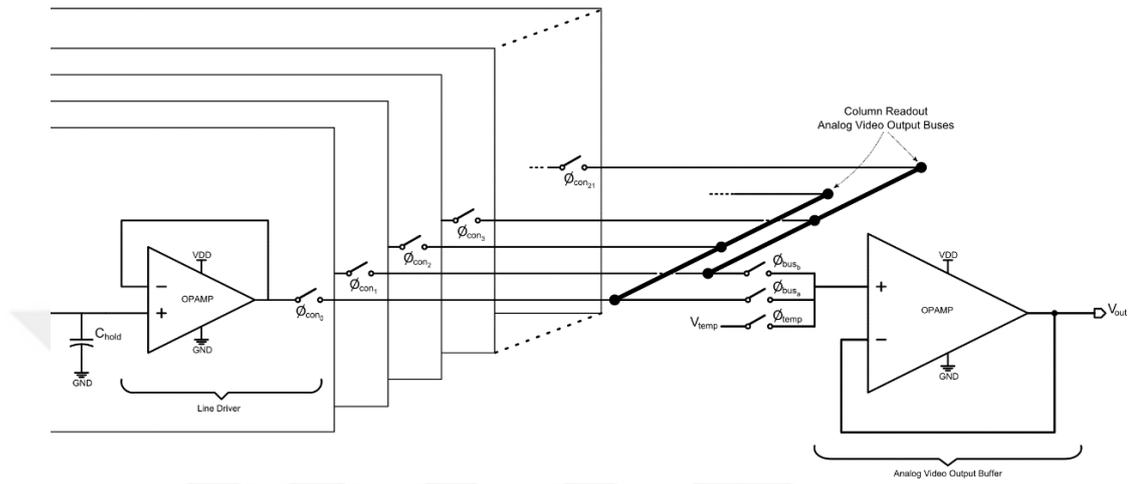Figure 3-13: Schematic of the column multiplexer.
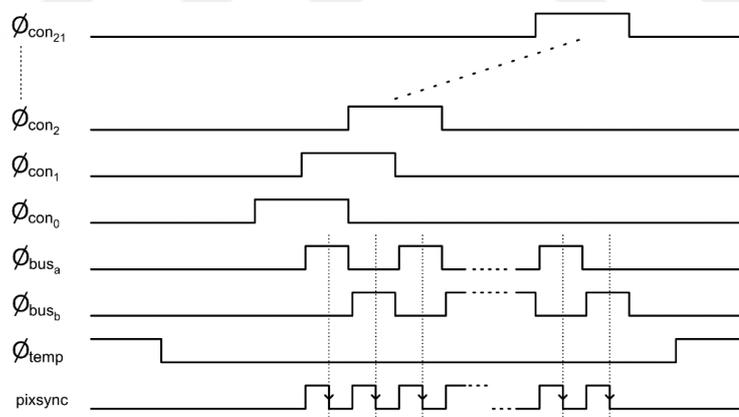
Figure 3-14: Illustration of column multiplexing.

Figure 3-15: Timings of column multiplexer and video buffer input select switches along with *pixsync*.

3.3.1.5 Sensor Configuration Memory and Serial Peripheral Interface

To increase the operational flexibility of the ROIC, sensor configuration memory block is implemented in the first sensor. This memory block is composed of 49 memory units with unique memory address assigned to each. All of the standard memory units can store 10-bits of data except the reserved memory unit which can only store 4-bits of data. Each standard memory unit includes address decoder & read/write controller block, hold registers, and shadow registers while the reserved memory unit includes only address decoder and 4-bit register as illustrated in Figure 3-16. Since the total of 49 memory units exist in the first sensor, 6-bit addressing scheme is used. The purpose of using hold and shadow registers is to allow controlled write operation. For example, if the sensor is in frame capturing mode,
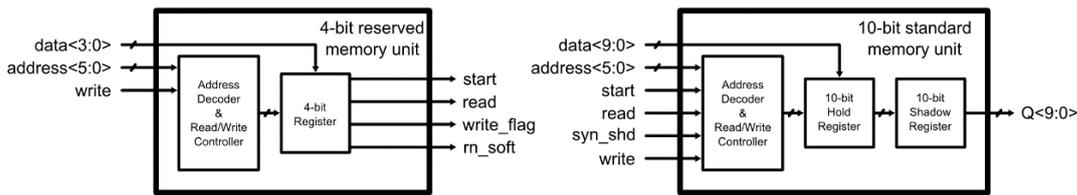

Figure 3-16: Block diagram of 10-bit memory unit.

Table 3-1: Explanation of reserved memory bits.

Bit Name	Type	Explanation
start	Write-only	Puts sensor in 0: idle mode 1: frame capturing mode
read	Write-only	0: SPI write mode is active 1: SPI read mode is active
write_flag	Write-only	It is set to tell sensor that new data is loaded into hold registers during frame capturing event. This bit is reset by the sensor itself at the beginning of the next frame.
rn_soft	Write-only	Active low soft reset

then the data written during the frame capturing event are first stored in the hold registers until the end of the frame so that the current configuration of the frame is not affected by the new configuration. Then, it is passed to shadow registers from which new data is read by the corresponding blocks. On the other hand, data written into reserved memory have higher priority and it has immediate effect on the sensor operation. Explanation of reserved memory bits is given in Table 3-1.

In order to communicate with external electronics, a simple standard SPI controller module is designed. It supports 4-wire communication with 16-bit data packet transfer per transaction. It allows both write into sensor configuration memory and read from it. SPI unit operates with 3 digital inputs (*spi_clk, spi_enb, spi_data*) and 1 digital output (*spi_out*). The description of these ports is given in Table 3-2. The mode of the SPI (read or write) is selected by the *read* bit of the reserved memory unit. Sample timing diagrams for both SPI read and write operations are shown in Figure 3-17. As shown in Figure 3-17, both *spi_clk* and *spi_enb* signals are kept high by the master in it is idle state. The start of transmission is signified by the *spi_enb* signal being driven low by the master. Then, the master sends data bits serially from the *spi_data* port at each negative edge of the *spi_clk* signal. During data transmission, the sensor shifts the data into a shift register at each positive edge of the *spi_clk* signal. After all bits are transferred, master drives both clock and data busses to high again.

Table 3-2: Description of SPI communication wires

Port Name	Direction	Description
spi_enb	IN	Active low chip select signal
spi_clk	IN	Clock signal for serial communication
spi_data	IN	Serial data input
spi_out	OUT	Serial data output
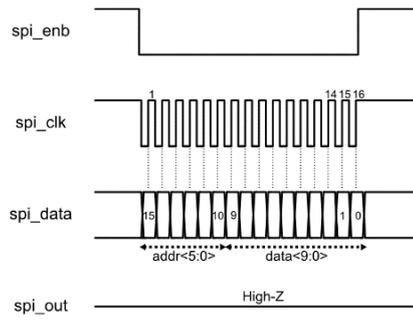
(a)
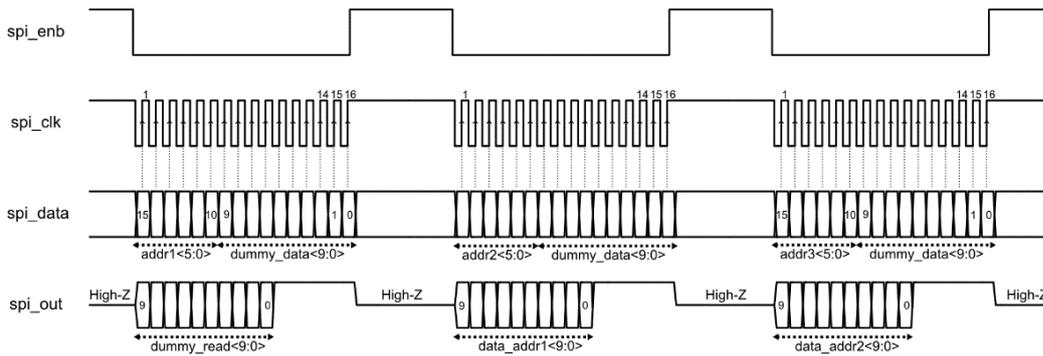
(b)

Figure 3-17: Sample timing diagrams for (a) SPI write operation (b) SPI read operation.

3.3.1.6 Pixel Level Biasing Memory

As stated previously, the first sensor includes resistive type microbolometer array. The resistance mismatches between pixels greatly increase the amount of FPN observed on the output image. In order to reduce this noise, each pixel should be biased with a unique biasing voltage. This is called "pixel level biasing (PLB)" and those biasing voltages are supplied to the gate of the n-channel injection transistors through 2-stage DAC. The first stage of this DAC generates the maximum and minimum voltage levels for the second stage DAC. These maximum and minimum voltage levels are adjusted by 10-bit R-2R DACs whose outputs are directly programmed by sensor configuration memory and kept unchanged during frame capture. The 2nd stage is composed of simple 6-bit resistor string DAC. The purpose
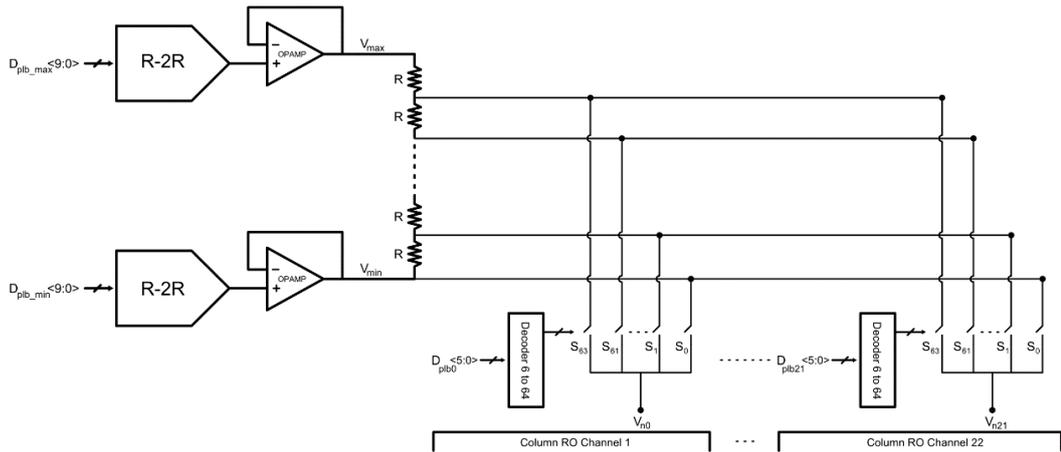
Figure 3-18: Illustration of 2-stage DAC architecture along with PLB decoder.

of it is to fine tune of pixel biasing voltages. 2-statge DAC architecture along with PLB decoder is illustrated in Figure 3-18.

The basing data is fed from the pixel level biasing memory which is composed of 176-bit shift and shadow registers as shown in Figure 3-19. The outputs of shadow register are sent to column readout circuit channels as 8-bit data packages. Least significant 6 bits of each 8-bit data package selects the pixel specific biasing voltage
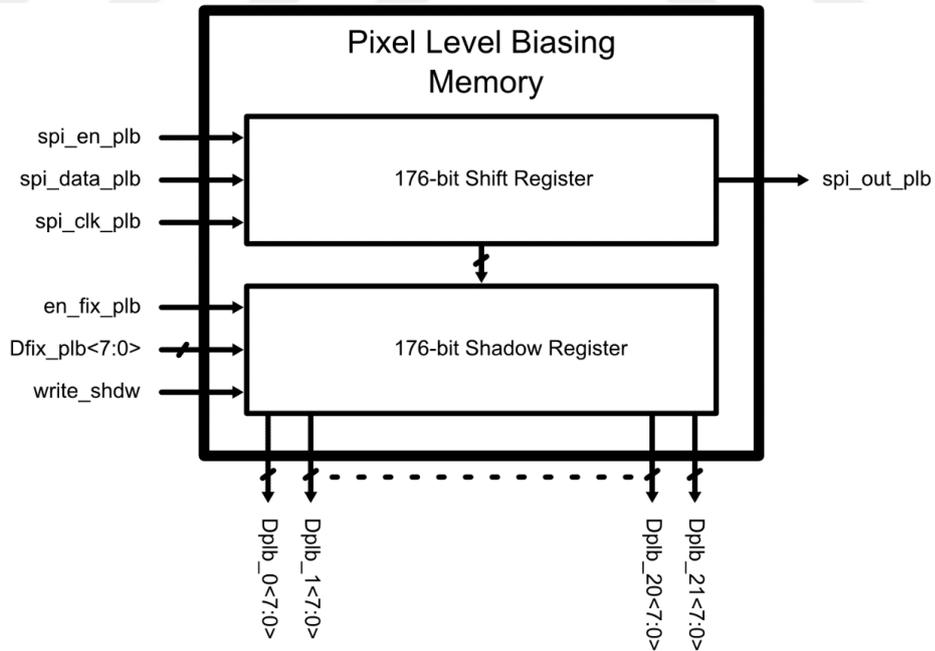

Figure 3-19: Block diagram of pixel level biasing memory.

by multiplexing the output of 2nd stage. 7th bit is set to 1 if the corresponding pixel is shorted to ground during post-processing of the sensor. This prevents excessive current sink from n-channel injection transistor. 8th bit is reserved for resistance measurement tests during sensor characterization. This memory block has its own SPI communication ports so that it can be programmed separately from the sensor configuration memory. However, it is possible to short SPI communication ports except *spi_en_plb* and *spi_en* so that only one clock and data port is allocated for SPI communication by the external microcontroller. PLB Memory is loaded at the beginning of each row time. Synchronization between external electronics is accomplished by *st_plb* signal which is output from the sensor. The rise of *st_plb* signal indicates that sensor waits for PLB data to be loaded. When it goes back to low again, *write_shdw* pulse is generated and the data in the shift register is loaded into the shadow register and then PLB voltages are set. The duration of the *st_plb* signal is designed to be fully programmable so that 176 bits of data can be loaded at any desired speed. The timings of the *st_plb* signal along with the *vsync* and *hsync* signals are illustrated in Figure 3-20. There is also fixed PLB mode of the PLB memory unit. This can be activated by setting *en_fix_plb* bit as high. When it is set, *Dfix_plb<7:0>* is used as the common biasing data for all pixels.
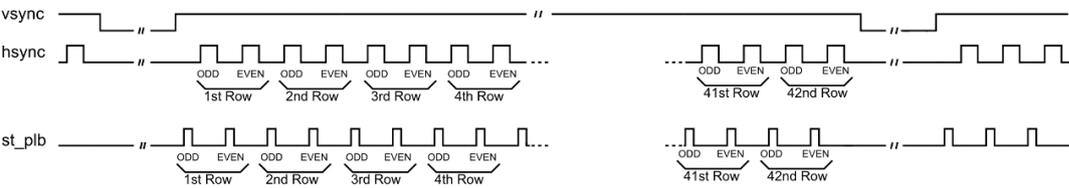

Figure 3-20: Synchronization signals for PLB loading.

3.3.2 Detector Bias Calibration

A typical block diagram for image acquisition and detector bias calibration of the first sensor is given in Figure 3-21. In Figure 3-21, power block provides biasing voltages to other blocks. Since the sensor does not include on-chip ADC, off-chip ADC is used to digitize the analog video output of the sensor. The digitized data are acquired by the image capturing unit which may be FPGA or MCU. The captured

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image may be transferred to a PC for visualization and advanced image processing purposes. Configuration and PLB memories are programmed by FPGA/MCU through the SPI communication interface.
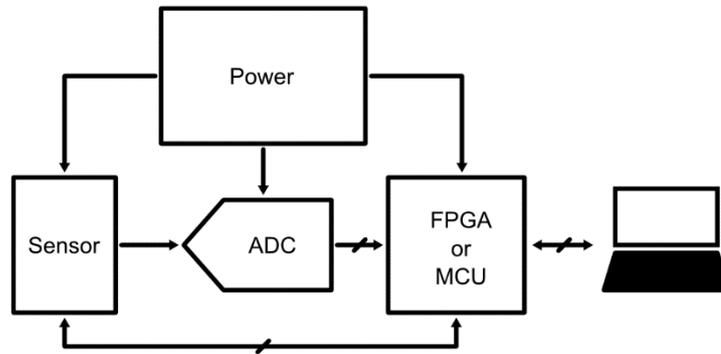

Figure 3-21: A typical block diagram for image acquisition and detector bias calibration of the first sensor.

At power up, the sensor starts operating in idle state in which all of its analog blocks are powered off and frame capturing is disabled. Before starting the detector bias calibration, first, bias adjustment for the analog blocks inside the sensor is done by writing proper biasing values to the sensor configuration memory. Then, the state machine is triggered for frame capturing by setting *start* bit as high in the reserved memory. Next, the sensor is put into the fixed PLB mode for the lowest biasing value of the 2nd stage DAC by setting *en_fix_plb* bit as high and *Dfix_plb<7:0>* as 0. In this configuration, the minimum biasing level of the 2nd stage resistor string DAC, which is defined by *Dplb_min<9:0>*, is used to bias all the pixels in the FPA. Now, the maximum possible value for *Dplb_min<9:0>* is adjusted manually for which outputs of all active pixels are less than mid-supply value. Afterwards, *Dfix_plb<7:0>* is set as 63 which corresponds to the biasing of pixels with the highest possible value of the 2nd stage DAC. This time the minimum possible value for *Dplb_max<9:0>* is adjusted manually for which outputs of all active pixels are higher than mid-supply value. After the adjustments of 1st stage DAC outputs, fixed PLB mode is disabled by setting *en_fix_plb* bit as low and detector bias calibration is initiated by FPGA/MCU. For the purpose of bias calibration of the first sensor,

binary search, also known as half-interval search, algorithm is implemented since it is very efficient for finding an optimal biasing point in just a few frames [20]. If 6-bit PLB data is used, for example, it only takes 6 frame time at least to find the correct biasing value for all pixels. In the binary search algorithm, the target value is compared with the middle element of the array; if the target value is greater or less than the middle element, the half in which target cannot lie is eliminated and the search continues on the remaining half until the remaining half is empty. In order to maximize the dynamic range of the sensor, the target value can be selected as the middle of the supply range. The calibration starts with setting the bias values of all pixels as the middle of the 2nd stage DAC voltage range. This corresponds to setting the most significant bit of the 6-bit pixel biasing value to 1 and the remaining bits to 0. This is done by programming the PLB memory of the sensor during frame capture by the external FPGA/MCU. Then, the digitized output of each pixel is sent to the FPGA/MCU which compares it to the target value which is the middle of the supply range in the digital domain. If the digitized output data of the pixel is greater (or less) than the target value, new calibration data is generated by setting the most significant bit as 0 (or 1) and the next bit as 1 for the corresponding pixel. This procedure continues until all bits are found for each pixel which may take at least 6 frame time. However, it is preferred to continue biasing of the pixels more than one frame time for each bit found so that pixel temperatures can reach their final value which is affected by the biasing point of the pixel. This provides better calibration of pixel biases since pixel output is affected by its temperature greatly. Sample graph which illustrates the binary search operation during bias calibration of a pixel is given in Figure 3-22.
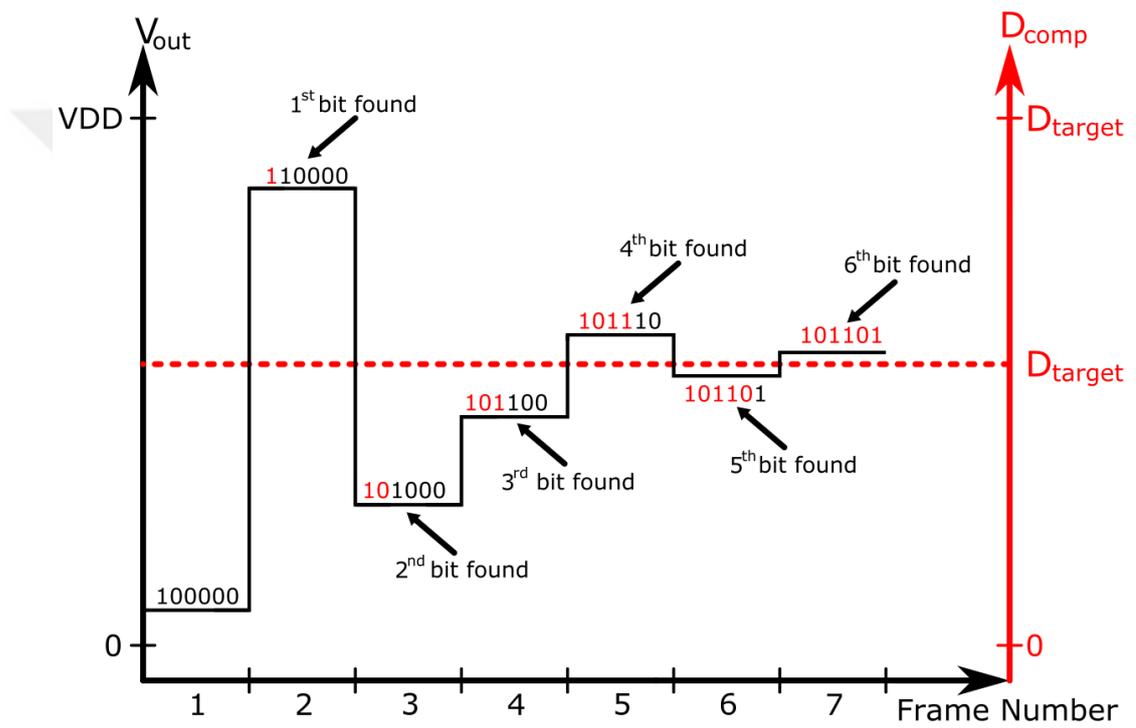
Figure 3-22: Sample graph illustrating the binary search operation during bias calibration of a pixel.

CHAPTER 4

TEST RESULTS OF THE FIRST SENSOR

The complementary circuit blocks of the first sensor that lie outside the scope of this thesis work have been designed by other IC design group members of Mikrosens. The designed digital blocks developed within the framework of this thesis were interfaced with these circuit blocks, e.g. FPA, column readout channels, bias generator, and video output buffer. The sensor was fabricated in a standard 0.35 µm CMOS process. The post-CMOS MEMS processing was done by MEMS processing group of Mikrosens in METU-MEMS Research and Applications Center facilities. The purpose of the post-CMOS MEMS processing is to suspend pixels in the FPA and to vacuum package the sensor dies. In order to test and characterize the sensor, the dewar motherboard, the proximity card and the PC test software were developed by the System Group of Mikrosens.

This chapter is organized as follows: Chapter 4.1 gives an introduction about the test system, Chapter 4.2 summarizes the test results of the digital blocks, Chapter 4.3 covers the tests of the detector bias calibration and finally Chapter 4.4 concludes the chapter.

4.1   Introduction

This section gives the test results of the designed circuit blocks in the fabricated first sensor. In order to measure the intrinsic sensor performance, the tests were done in a dewar environment with the plain sensor sample that has only undergone pixel suspension process but not vacuum packaging. The sensor was wire-bonded to a proximity test card that makes interface between the dewar mother board and the sensor as shown in Figure 4-1. The proximity card includes the sensor, voltage

regulators and some connectors mainly. These connectors carry digital I/Os, sensor analog video output, and power supply signals. The sensor analog video output is digitized by the ADC located on the dewar motherboard. All of these digital signals that are output from the dewar electronics are buffered by bus driver ICs and transferred to the FPGA test card through dewar cabling. The digitized image data is formatted by FPGA and sent to the PC through USB link. The test software is used to configure the sensor, process the image and display it on the computer screen. In order to vacuum the dewar environment, vacuum pump is used. This pump provides 3-4 mTorr of vacuum levels measured by the vacuum sensor which is well enough to characterize sensor performance. Black body radiation source and its controller were added to test setup so that NETD value of the sensor can be extracted. The picture of the test setup that contains aforementioned test equipment is shown in Figure 4-2.

The next sections in this chapter will give the summarized information about the tests of the circuits designed in the scope of this thesis work.

Figure 4-1: Dewar motherboard and proximity card with wire-bonded sensor.

Figure 4-2: Overall picture of test setup.

4.2   Digital Circuits

The digital circuits of the first sensor can be grouped as two main parts; the serial peripheral interface and the digital controller. The rest of this section will summarize the tests of these parts in order.

4.2.1   Serial Peripheral Interface

The serial peripheral interface provides the programming of sensor configuration memory by the external camera electronics, according to the required operation condition. The serial interface is implemented with 4 digital signals that are SCLK, SDATA, SENB, and SOUT. The external camera electronics provide 16-bit word for each data transaction where the first 6-bit defines the memory address and the last 10-bit is the data to be written into that address. The first sensor provides 48 memory addresses each of which can store 10-bit configuration data and single reserved memory unit that can hold 4-bit data resulting in 484 programmable bits in total. Figure 4-3 (a) shows the test results of a sample programming of address 48 with

data "0001111001" and (b) shows a sample SPI read operation from the same address.

(a)

(b)

Figure 4-3: (a) Shows the test result of a sample programming of address 48 with data "0001111001" and (b) shows a sample SPI read operation from the same address.

Figure 4-4: The test results of some of the important digital signals generated by the digital controller.

4.2.2 Digital Controller

Digital controller block of the sensor requires only the CLK signal from the external electronics to generate ROIC timings, frame synchronization signals etc. With the setting of the START bit as high in the reserved memory, digital controller block starts operating. Some of the important signals it generates are VSYNC, HSYNC, PIXSYNC, STPLB, INTENB, and RST where VSYNC, HSYNC and PIXSYNC are used by the external camera electronics for frame synchronization, and STPLB is also used by the external camera electronics to synchronize loading of detector bias calibration data into the sensor PLB memory. INTENB and RST signals are used by column readout channels for operating analog switches of the switched-capacitor integrator. High level of STPLB signal indicates the time that serial calibration data,

PLBDATA, can be shifted into PLB memory through the sensor's second SPI interface reserved for this operation. The duration of RST signal, T_{rst}, determines the total reset time for the integration capacitors, while the total integration time, T_{int}, is defined by the duration for which INTENB is high, but RST is low. STPLB, INTENB, and RST pulse durations are all designed to be programmable which makes the operation of the readout circuit very flexible. Frame synchronization is provided by VSYNC that makes low-to-high and high-to-low transitions at the beginning and the end of the each frame respectively. Therefore, frame rate is calculated by the frequency of VSYNC. In order to synchronize rows in the frame, HSYNC pulse is generated twice, i.e., one for odd and one for even pixel columns during single row time, T_{row}. Lastly, PIXSYNC is used for pixel synchronization and sampling of analog video output signal. Test results of these signals are presented in Figure 4-4.

4.3 Image Acquisition and Detector Bias Calibration

In order to verify the functional operation, the readout circuit was tested by the IC Design Group Members of Mikrosens. Operating points of the sub-blocks of the readout circuit were adjusted so that optimum performance can be obtained. Figure 4-5 (a) shows a sample raw image obtained from the first sensor and (b) shows the same image after interlacing process. This image was taken under 100 μs of integration time with 31 pF of integration capacitance configurations and no detector bias calibration implemented, i.e., fixed detector biasing was applied to all pixels. As shown in the Figure 4-5, a color gradient in the columns of the FPA is observed such that the pixels get darker from left to right meaning that there is a column based non-uniformity in the pixel output signals which may be due to the gradient in some biasing powers along column readout circuits. This non-uniformity is eliminated by performing detector bias calibration. The histogram of the obtained image is illustrated in Figure 4-6. It can be said that although CMOS based IR sensitive active materials are embedded in the pixels, there is still high non-uniformity in the pixel output voltages according to the Figure 4-6.

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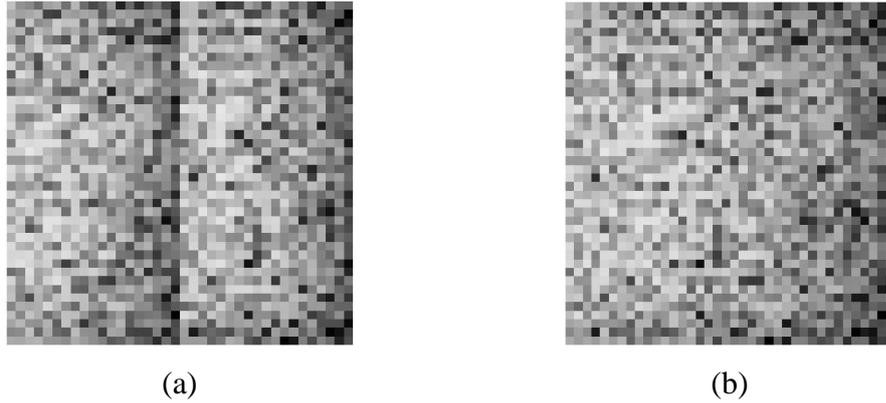(a)   (b)

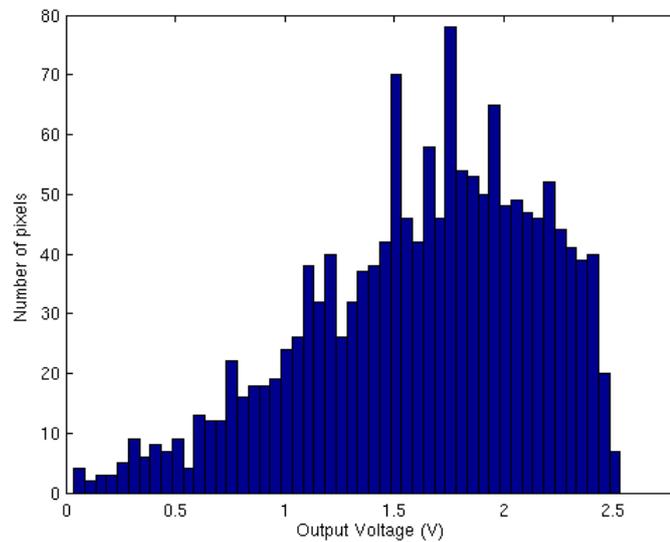Figure 4-5: (a) shows a sample raw image obtained from the first sensor (b) shows the same image after deinterlacing process.


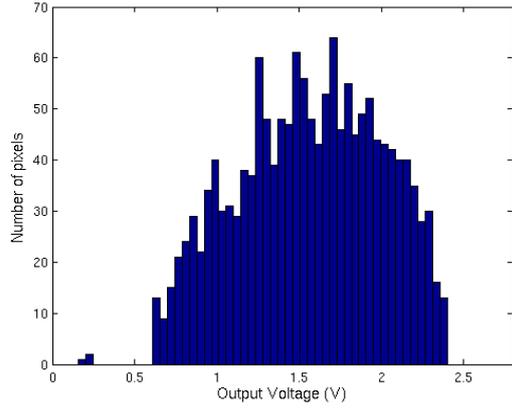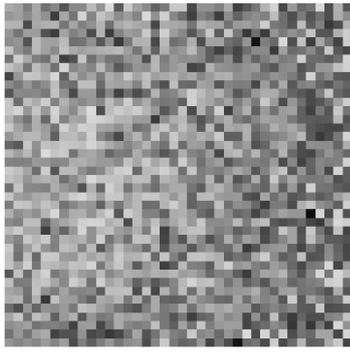Figure 4-6: Histogram of the obtained image.

In order to eliminate high non-uniformity in the pixel output voltages, and test pixel level biasing circuitry in the first sensor the FPGA firmware has been developed in the scope of this thesis work. The firmware basically performs binary search operation by checking the digitized pixel outputs, comparing them with a reference value, generating a new calibration data, and writing it into the PLB memory unit of the first sensor when STPLB is high. Before triggering the calibration block of the FPGA firmware, first, coarse tuning of the first stage PLB DACs that define the maximum and the minimum voltages for the second stage DAC is done. Adjustment of the first stage DAC that defines the minima/maxima of the second stage DAC is

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done by finding the maximum/minimum biasing voltage for which pixel output voltages are lower/higher than the reference voltage used during binary search. After coarse tuning is accomplished, detector bias calibration is triggered from the test software. The raw images obtained at each step of the detector bias calibration and the corresponding output voltage histograms are illustrated in Figure 4-7. These images are also obtained for 100 µs of integration time and 31 pF of integration capacitance. If Figure 4-5 (b) is compared with the Figure 4-7 (g), it is observed that detector bias calibration algorithm developed for the first sensor suppresses the high degree of deviations in the pixel output voltages very effectively. In other words, non-uniformity sources that lead to relatively high variations in the pixel output voltages are compensated in just a few frame cycles with the algorithm developed in the scope of this thesis. The standard deviation of the FPA output voltage is reduced from ~527 mV to ~19.5 mV after the detector bias calibration. In order to observe the effectiveness of the algorithm, few more tests have been performed for much higher readout gain configurations.
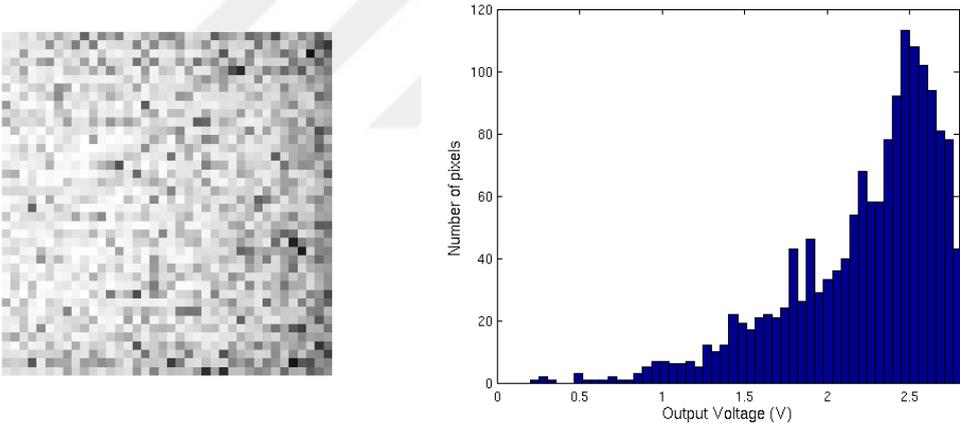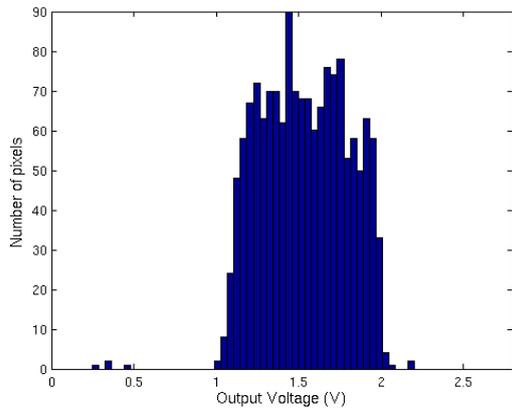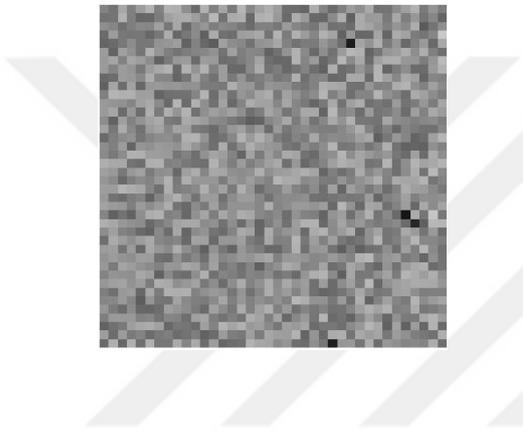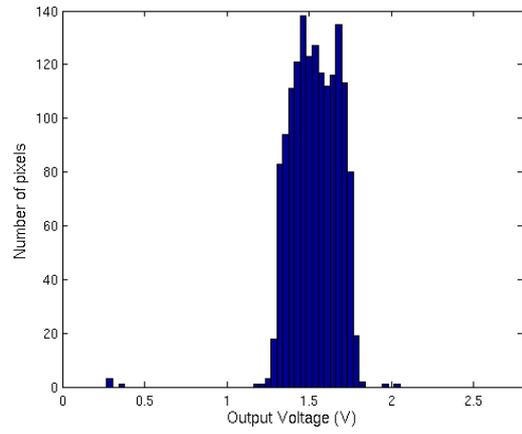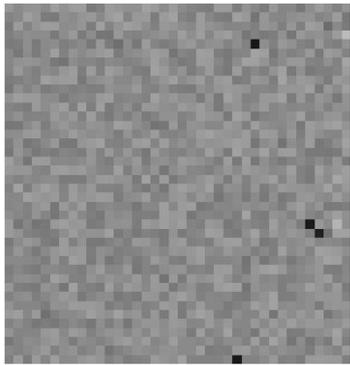

(a)

Figure 4-7: The raw images and the corresponding output voltage histograms obtained at each step of the detector bias calibration. Figures (a) to (g) correspond to calibration steps 1 to 7.
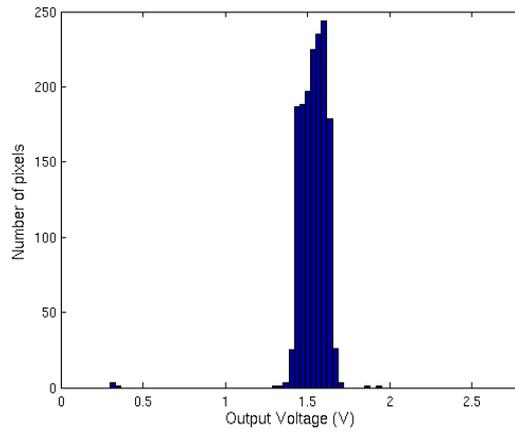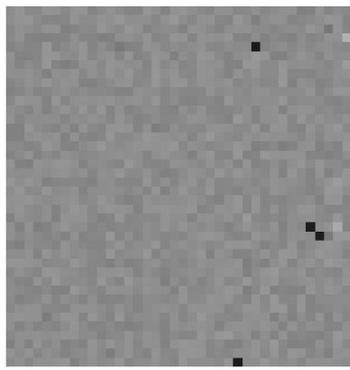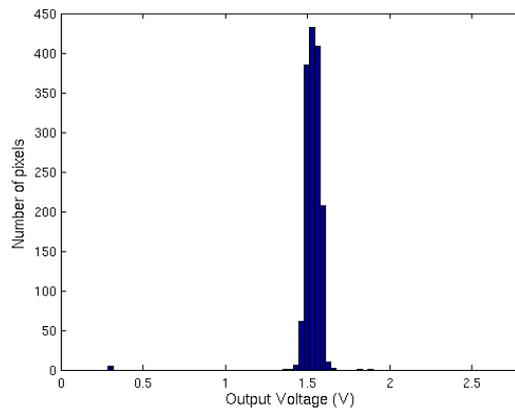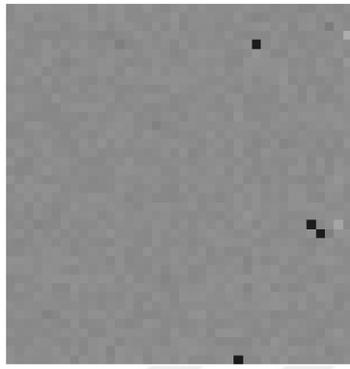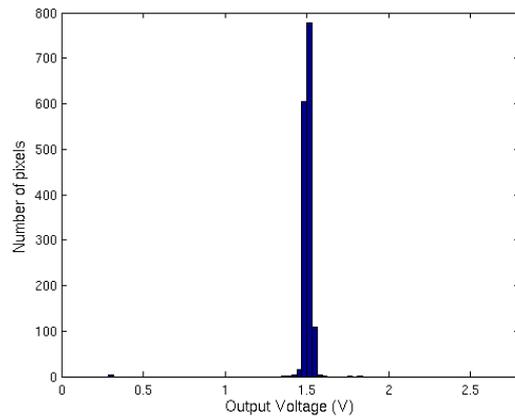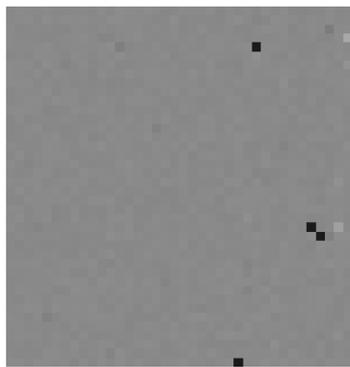
(b)

(c)

(d)

Figure 4-7 (cont'd)

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(e)

(f)

(g)

Figure 4-7 (cont'd)

Figure 4-8 shows the obtained images and the corresponding histograms before and after the detector bias calibration when readout gain is increased almost 8 times, i.e., integration time is kept as 100 µs and the integration capacitor is configured to be 4 pF. As shown in Figure 4-8, even for very high readout gain configurations, detector bias calibration algorithm together with the designed circuit blocks works very well such that no saturated pixel is observed after the calibration, but there are still 4 dead pixels whose outputs are not affected by the change in detector bias. The readout gain of the sensor can be increased not only by decreasing the integration capacitance but also increasing the integration time. Increasing the integration time also reduces the noise in the output voltage due to decrease in the readout circuit bandwidth, but the frame rate gets lower as integration time increases. Sample images obtained from the first sensor after some image processing steps such as one-point and two-point corrections, dead pixel correction, color mapping, and contrast-brightness adjustments [21] are illustrated in Figure 4-9. These images were taken using the dewar camera system with F1.0 Germanium lens, 100 µs of integration time, 4 pF of integration capacitance, and 8 times frame averaging. Under such condition, the resulting frame rate is about 8 fps and the obtained NETD histogram of the first camera system is given in Figure 4-10. As shown in the NETD histogram, the peak NETD value is about 135 mK which is low enough for most of the low-cost thermal imaging applications.
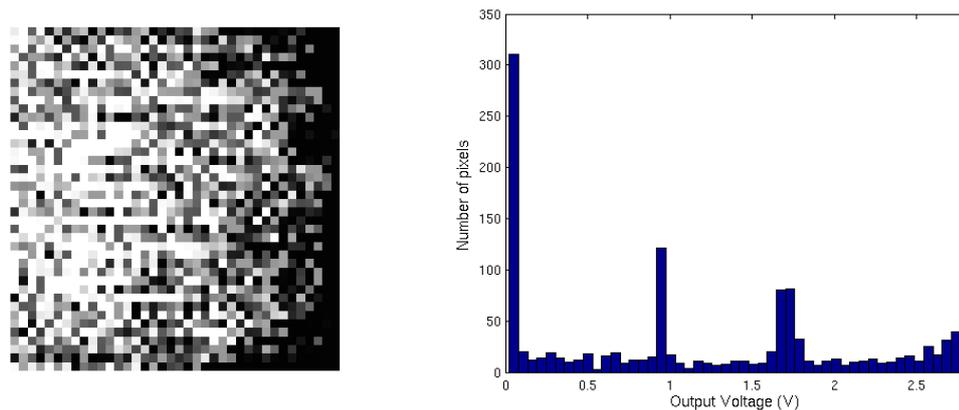
(a)

Figure 4-8: The obtained images and their output voltage histograms (a) before the detector bias calibration (b) after the detector bias calibration.

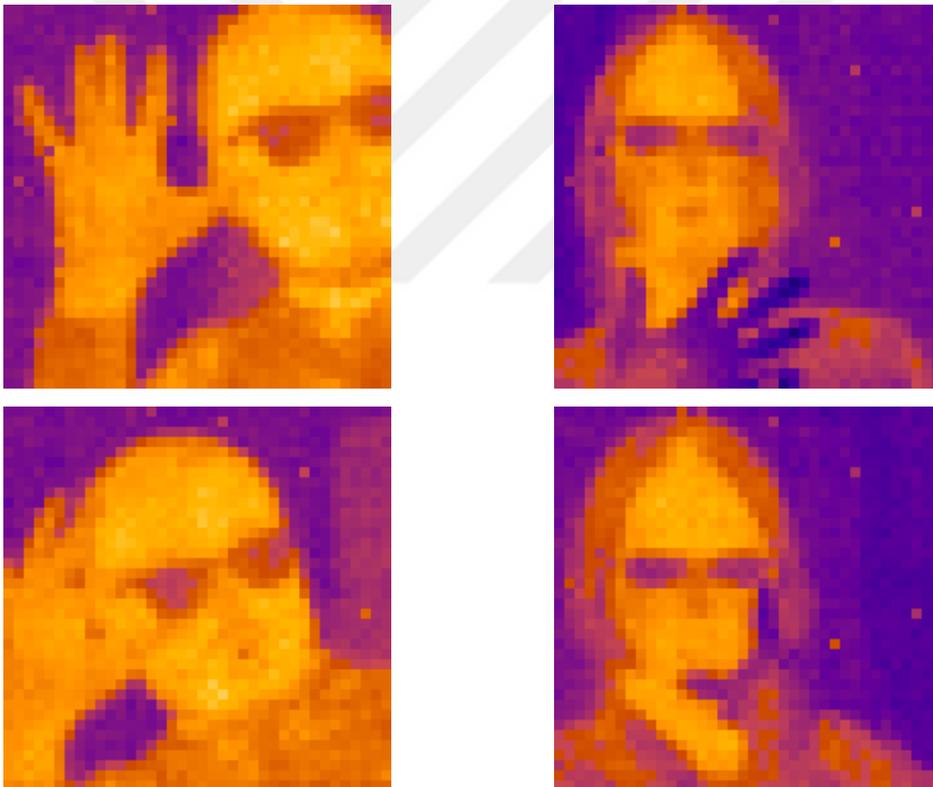71
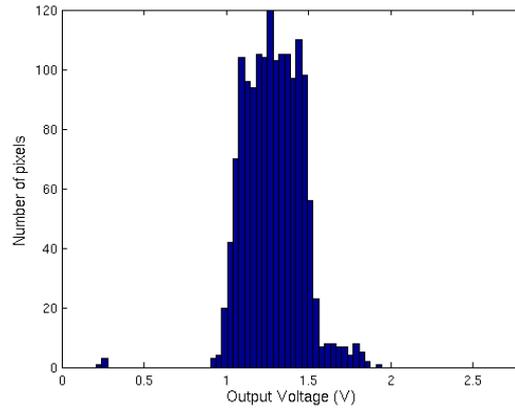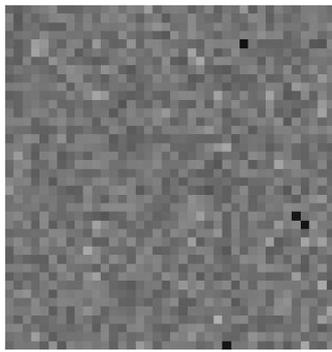
(b)

Figure 4-8 (cont'd)

Figure 4-9: Sample images obtained from the first sensor after one-point correction, and contrast and brightness adjustments.
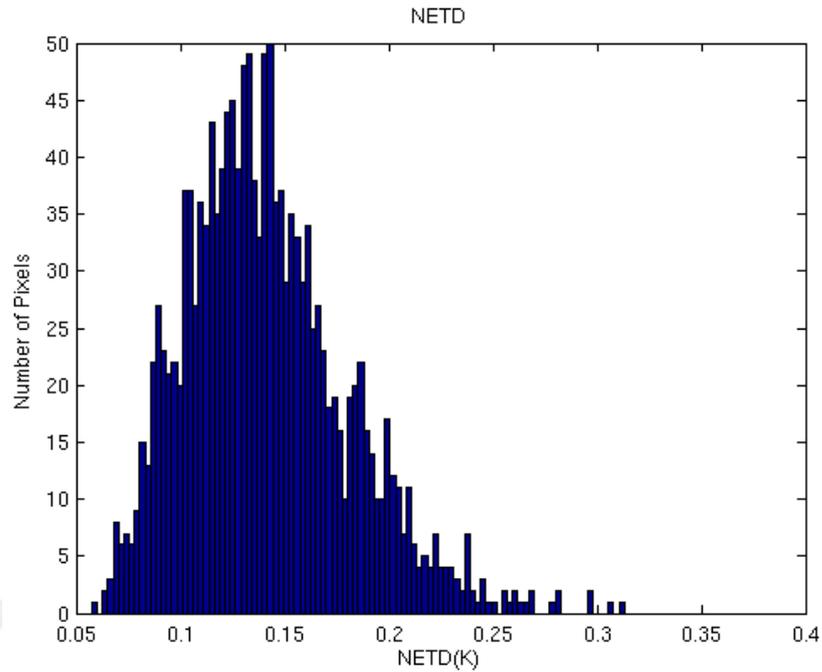
Figure 4-10: The obtained NETD histogram of the first camera system.

4.4 Conclusion

This chapter summarized the test results of the circuit blocks in the first sensor, designed in the scope of this thesis work. In order to conduct the required tests, a simple test system is developed. First, serial peripheral interface has been tested to verify that the sensor is programmed correctly. Then, digital controller block has been tested to verify that digital timings are all as expected. Next, the overall readout circuit was operated and some sample images were generated. Finally, the detector bias calibration algorithm has been developed and implemented using FPGA. The test results of the detector bias calibration algorithm have been presented.

The test results in this chapter verify that all the circuit blocks designed for the first sensor in the scope of this thesis operates as expected. Thanks to the efficient detector bias calibration algorithm developed, the first sensor can be used under extreme operating conditions such as very low or high temperature environment, very high readout gains etc. It can be concluded that the first sensor is ready to be used in a commercial camera systems.

CHAPTER 5

ON-CHIP BIAS CALIBRATION ARCHITECTURE DEVELOPMENT

5.1   Introduction

As mentioned in Section 1.4, the main goal of this thesis is to develop ROIC architecture that allows on-chip bias calibration of pixels to correct output offset voltage. In order to achieve this goal, an advanced ROIC architecture is designed and implemented in the second sensor using the experience gained in the first sensor. As in the first sensor, digital blocks such as PLB circuit, digital controller, row scanner, column multiplexer, sensor memory and programming interface are also designed in the second sensor. However, the second sensor has additional features, for example, its bias calibration circuit allows on-chip pixel bias correction and storage of calibration data inside on-chip memory. Figure 5-1 shows the layout of the first sensor which occupies 4.9 x 6.2 mm^2 silicon area. The layouts of the circuits developed for this part of this thesis are shown inside red boxes in Figure 5-1. The digital I/O level of the sensor was designed to be 3.3 and 5 V compatible for most of the microcontroller and FPGA based systems. The second sensor also provides different synchronization signals to ease the interface between the sensor and the external electronics. Some of the important features implemented in the second sensor are given as below:

- On-chip pixel level biasing memory that can be accessed by on-chip bias calibration circuit or external FPGA/MCU
- On-chip detector bias calibration circuit
- Standard SPI communication interface
- Repeated read operation of the selected row before passing to the next row
- Bi-directional column multiplexing (left-to-right or right-to-left)
- Bi-directional row scanning (top-to-bottom or bottom-to-top)

- Frame windowing (8x1 to 80x80)
- On-chip temperature sensor voltage output from video-output pad
- Programmable integration and reset times
- Programmable frame rate without changing system clock or integration time
- First reset, then read operation for cancelling contribution of the readout noise
- Selectable polarity and adjustable delay time for pixel synchronization signal
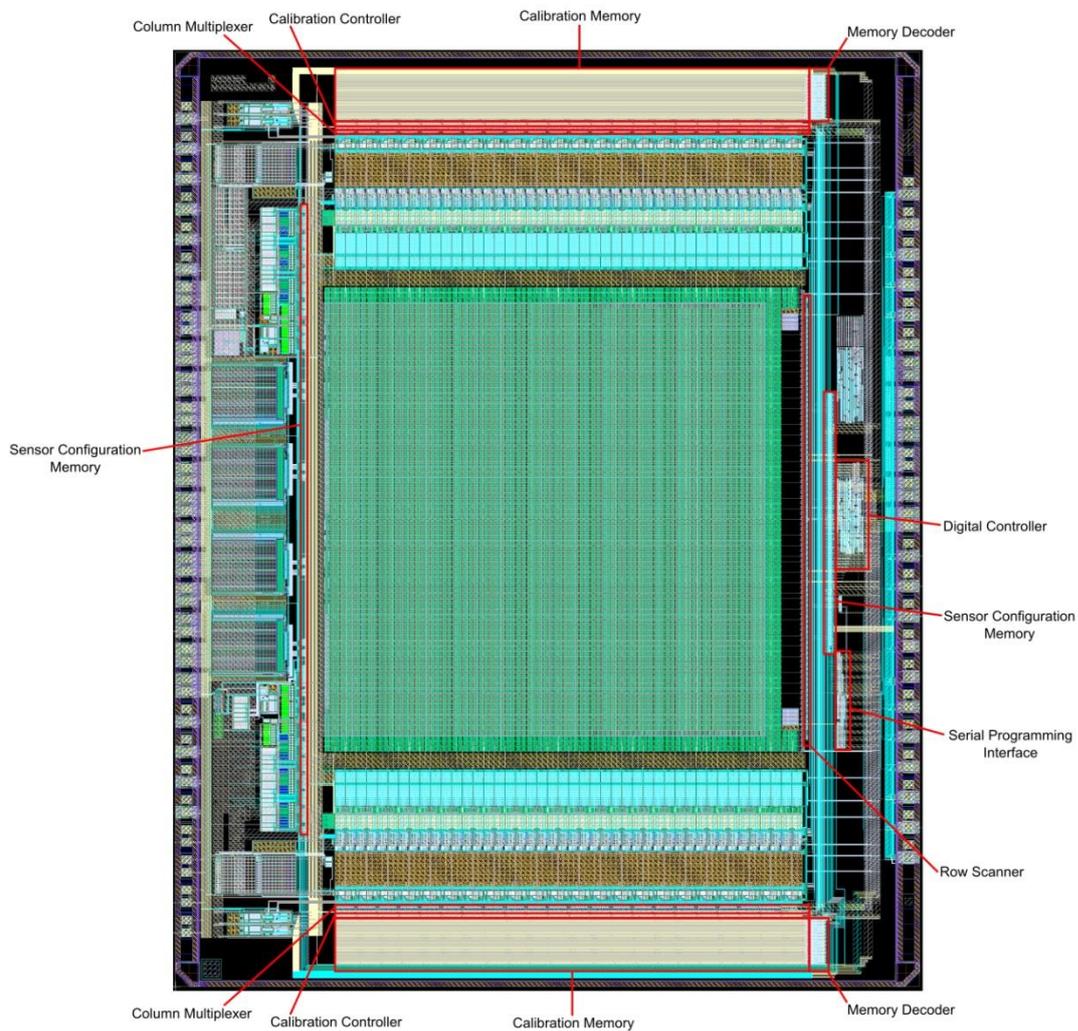

Figure 5-1: Layout view of the second sensor. The layouts of the designed digital blocks for the second part of this thesis are shown inside the red boxes.

5.2   On-Chip Detector Bias Calibration Development for the Second Sensor

The advantages of detector bias calibration using both on-chip and off-chip methods are investigated in Section 2.3. As mentioned in Section 2.3, on-chip bias calibration simplifies the communication interface between the sensor and the external electronics and eliminates the need for high performance micro processing unit which is required to implement calibration algorithm and loading of the calibration data into the sensor memory. This is especially important for low cost thermal imaging systems for which it is necessary to make the overall system relatively small and cost efficient. For this reason, using the experience gained from the first sensor, on-chip detector bias calibration circuit is developed in the second sensor. This circuit is designed on the basis of the calibration algorithm developed for the first sensor. The details of the on-chip detector bias calibration circuit are given in Section 5.2.2 after the analysis of the overall sensor architecture of the second sensor in Section 5.2.1.

5.2.1   Sensor Architecture

Overall block diagram of the second sensor is illustrated in Figure 5-2. As shown in the figure, readout blocks are located on both top and bottom of the FPA. By the help of this positioning, optical center is set as the center of the sensor. There are 21 column readout channels on both top and bottom of the FPA. The first 20 of them are used to read active pixels and the last channels (21st column readout channels from the top and the bottom) are used to read IR insensitive pixel columns in the FPA. As in the first sensor, each of the first 20 column readout channels is assigned to two FPA columns for read operation. On the other hand, each of the last column readouts is assigned to the single FPA column that is reserved for IR insensitive pixels. During frame capturing, first odd FPA columns and then even FPA columns are read out in a row time by the corresponding column readout channels. The selection of odd or even FPA columns is achieved by FPA column select switches. Therefore,
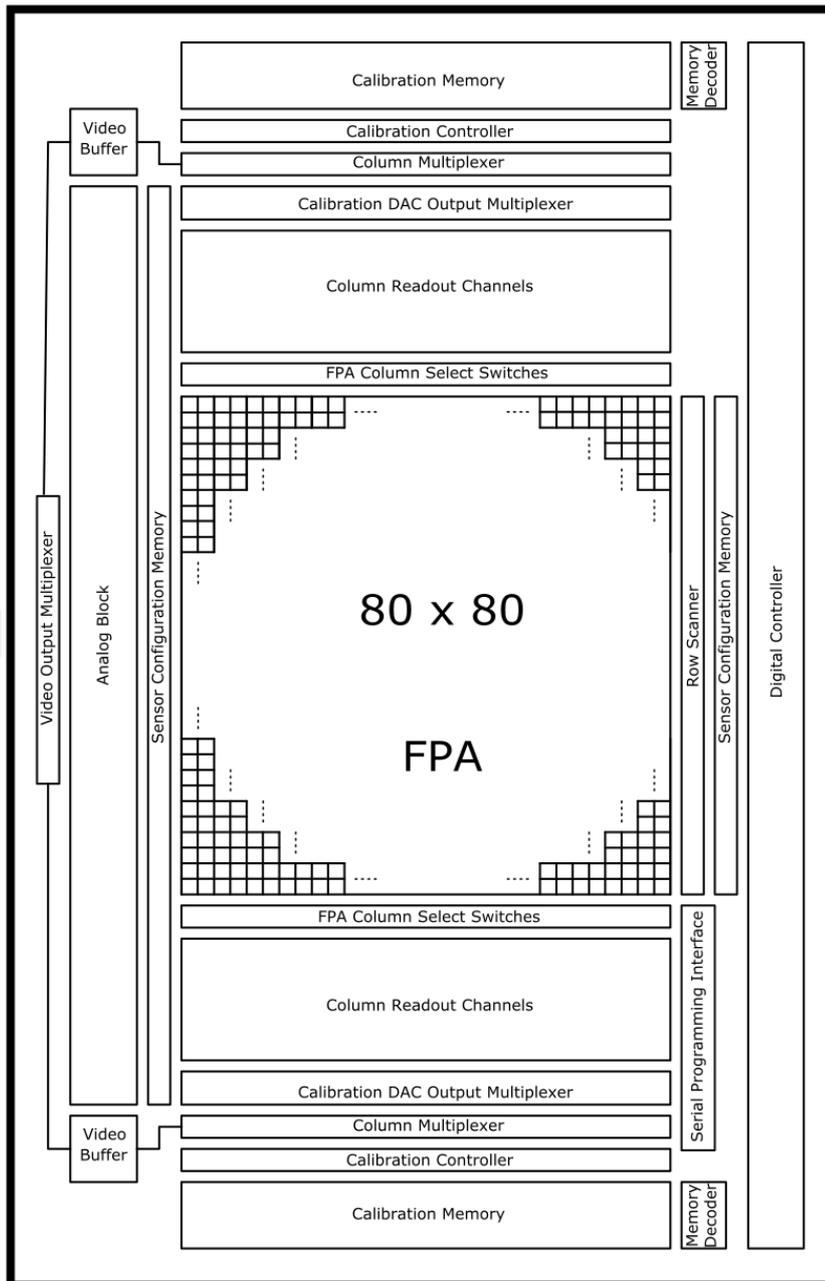
Figure 5-2: Overall block diagram of the second sensor.

a total of 42 column readout channels are used for reading of 82x82 FPA and image data is acquired in interlaced fashion by external electronics as in the first sensor. Similar to the first sensor, analog block generates biasing currents and voltages for column readout channels and video output buffer. The analog front-end circuit architecture of the PLB unit is the same as in the first sensor in which 2-stage PLB DAC is used for detector bias generation. PLB DAC output multiplexer block selects

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a biasing voltage from the 2nd stage of calibration DAC and passes it to corresponding column readout channels. The select bits of PLB DAC output multiplexing block are provided from PLB memory which stores biasing values of all pixels and does not require dynamic write operation during frame capturing in contrast to the first sensor. It is either programmed by on-chip calibration controller block with an external trigger or it can be programmed manually by the external electronics when the sensor is in idle state. Column multiplexer blocks are used to connect the output of each readout channel to the input of video output buffers. The outputs of these video output buffers assigned for top and bottom column readout channels are further multiplexed by the video output multiplexer block to provide a single video output signal to the external electronics. Row scanner is used to select one FPA row at a time during frame capturing event. Digital controller block generates necessary timings for row scanner, FPA column select switches, column readout channels, PLB memory and memory decoder, column multiplexer, and calibration controller blocks. As in the first sensor, the second sensor also includes sensor configuration memory and SPI that are required to operate the sensor in different modes, and tune voltage and current biases precisely.

5.2.1.1   Pixel Array

FPA of the second sensor consists of 82x82 resistive type microbolometer pixels. First row, last row and the last two columns of the FPA are composed of IR blind pixels, while the remaining pixels are IR sensitive as illustrated in Figure 5-3. The pixel selection circuitry and FPA structure are the same as in the first sensor.

5.2.1.2   Column Readout

The second sensor accommodates a total of 42 column readout channels. Half of them are located on top of the FPA, while the remaining half is located on the bottom of the FPA as shown in Figure 5-2. There is no major difference between the column

readout circuits of the first and the second sensors. Pixel biasing and pixel signal reading operations are performed by the similar manner.
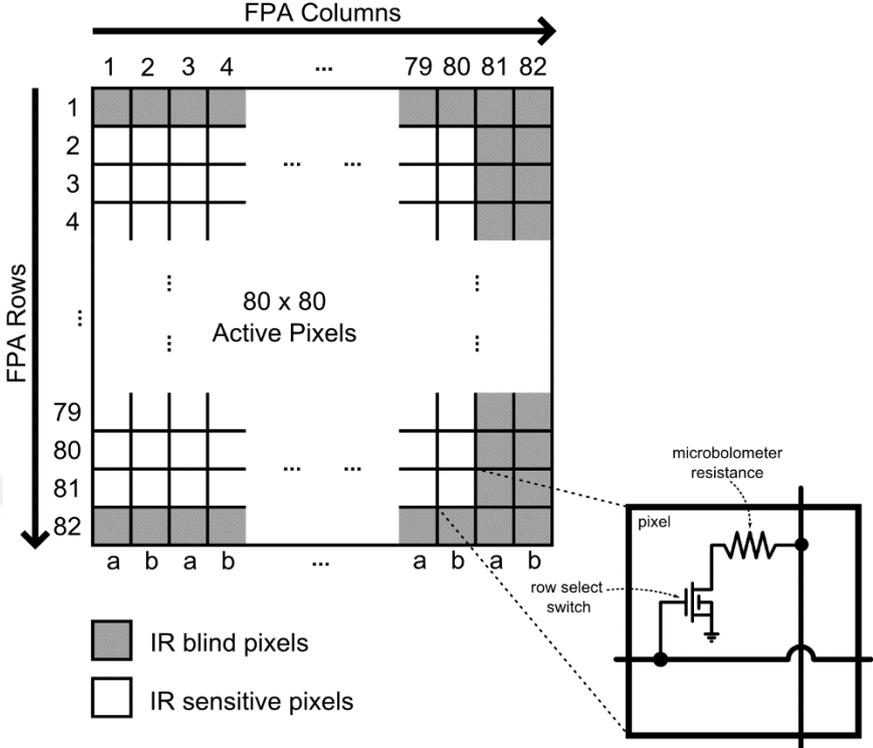

Figure 5-3: Illustration of FPA structure in the second sensor.

5.2.1.3   Digital Controller

Digital controller of the second sensor is similar to the one in the first sensor, however, it provides some additional features and it is optimized for 80x80 FPA. It is also composed of 3 main units as in the first sensor; state machine, counters & comparators, and timing generator as illustrated Figure 3-9. In order to provide bi-directional row and column scanning, and allow frame windowing, row scanner and column multiplexer circuits are designed to be decoder based. Hence, a different kind of counter circuit having up/down counting and preset features is designed in the second sensor so that bi-directional scanning and frame windowing functions can be performed easily. Due to the addition of on-chip pixel bias calibration circuit and on-

chip pixel level biasing memory, state machine of the second sensor is designed to be a little bit different than the one in the first sensor. The state diagram of the state machine designed in the second sensor is given in Figure 5-4. As shown in Figure 5-4, PLB Pre-loading Delay and PLB Loading states are removed since they are not needed anymore, thanks to the on-chip PLB memory that can store biasing data of each pixel in the FPA. On the other hand, Frame Count, Bit Count and Post-read Delay states are added to generate necessary timings for calibration controller blocks. The second sensor supports 6-bit detector biasing data also. On-chip detector calibration circuitry in this sensor implements a binary search algorithm to find the correct pixel biasing data. Therefore, starting from the MSB, it takes 6 steps to find the correct biasing value. These steps are counted by Bit Count and the completion of on-chip calibration is signaled by this state. In order to add a certain delay between consecutive calibration steps, Frame Count is added. This state adds predefined number of frame cycles between consecutive calibration steps so that the bias heating curve of the each pixel can take its final shape for the corresponding biasing data before the generation of new biasing data.
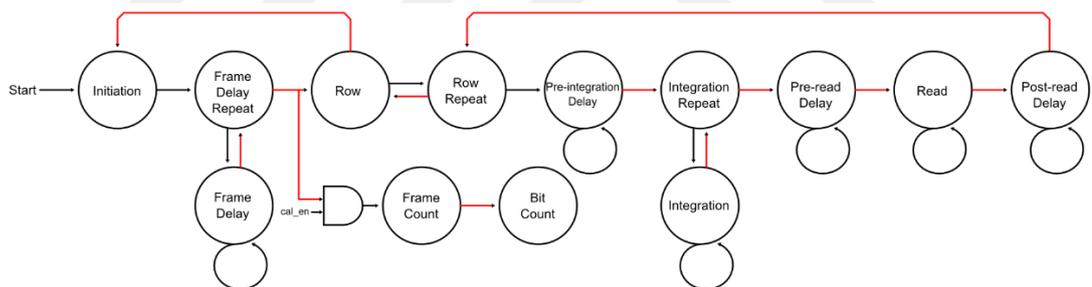

Figure 5-4: State diagram of the state machine in the second sensor.

Using the state information and counter & comparator output values, timing generator unit generates necessary driving signals for column multiplexer, row scanner, column readout channels, calibration controller, PLB memory decoder etc. The same frame synchronization signals are also provided in the second sensor. The only difference is that the number of *pixsync* and *hsync* pulses in each *vsync* pulse is different due to the FPA size. Also, sampling edge polarity of the *pixsync* is programmable in the second sensor; therefore, analog video output data can be either

sampled at the positive edge or the negative edge of the *pixsync* signal depending on the selected polarity. Moreover, the programmable *pixsync* delay feature is also added to the second sensor. By using this feature, *pixsync* signal can be delayed up to ~480 ns so that analog video output signal is settled sufficiently before being sampled. Output synchronization signals along with different *pixsync* modes are illustrated in Figure 5-5.
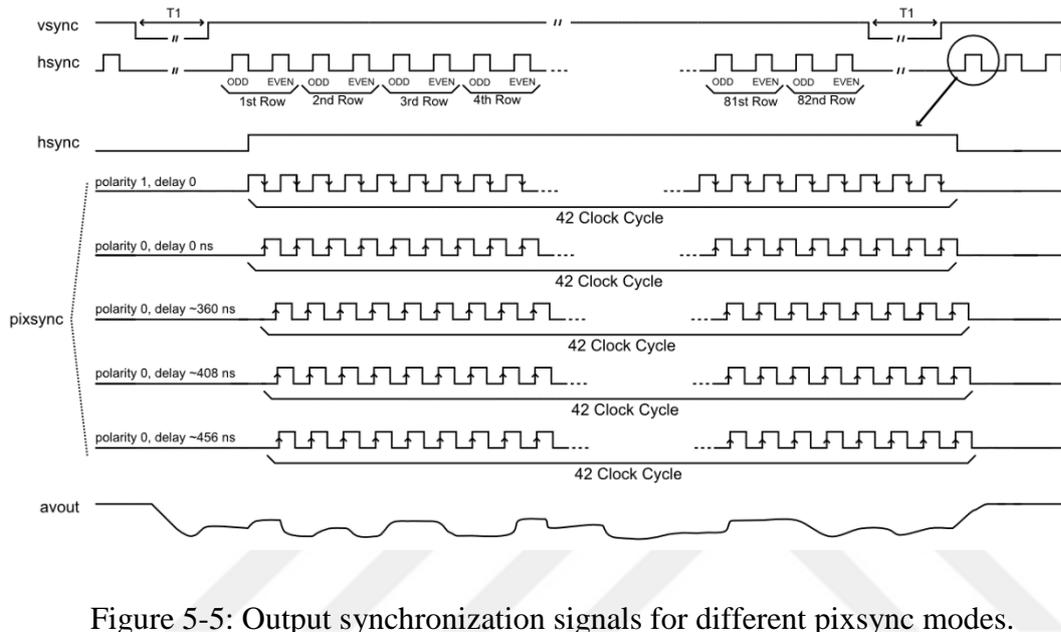

Figure 5-5: Output synchronization signals for different pixsync modes.

5.2.1.4   Row Scanner and Column Multiplexer

In contrast to the shift register based circuit in the first sensor, decoder based circuit is chosen for both row scanner and column multiplexer circuits in the second sensor. Using decoder based circuit eases the frame windo and bi-directional scanning operations. Since there exist 82 FPA rows and 42 column readout channels in the second sensor, 7-bit row counter and 6-bit column counter are implemented and associated with Row state and Read state, respectively. Row scanner and column multiplexer circuits use the output values of these counters as their decoder input values. Up/down counting and pre-loading features are added to these counters to enable bi-directional scanning and frame windowing functions. Frame windowing allows local reading of FPA pixels which may be required in some applications. In order to configure frame windowing, 4 registers are allocated in the sensor

82

configuration memory. These registers are named as ROWBEGIN, ROWEND, COLBEGIN and COLEND. ROWBEGIN and ROWEND registers can take values in between 0 to 79. Only the FPA rows between these values are read during frame capturing. On the other hand, COLBEGIN and COLEND registers can take values in between 0 to 9. When COLBEGIN is set as 0 and COLEND as 9, all the column readout channels are active and all the FPA columns are read during frame capturing. If COLBEGIN is set as 1 and the COLEND as 8, for example, the first two and last two column readout channels from the top and the bottom of the FPA are powered down; therefore, the first 8 and the last 8 FPA columns are not read during frame capturing. However, IR blind rows and columns are always read during frame capturing even if frame windowing is active. Illustration of frame windowing for 2 different sets of frame windowing register values is given in Figure 5-6.

5.2.1.5 Sensor Configuration Memory and Serial Peripheral Interface

The structure of the sensor configuration memory in the second sensor is very similar to the one designed for the first sensor. The only difference is that 8-bit data and 7-bit addressing schemes are implemented in the second sensor instead of 10-bit data and 6-bit addressing scheme. Because of the decrease in the number of data bits and addition of new features, the total number of memory addresses is increased to 87 in the second sensor.

In order to communicate with external electronics, standard SPI peripheral is designed for the second sensor. This peripheral works exactly the same way as in the first sensor. It supports 4-wire communication with 16-bit data packet transfer per transaction. Only difference is the 16-bit packet format where the MSB bit, selects the type of the memory that the data will be written into the second sensor. When the MSB bit is set to 0, the transmitted data are written into sensor configuration memory, when it is set to 1 the transmitted data are written into pixel level biasing memory for manual detector bias calibration.

COLBEGIN=1, COLEND=8, ROWBEGIN=18, ROWEND=58
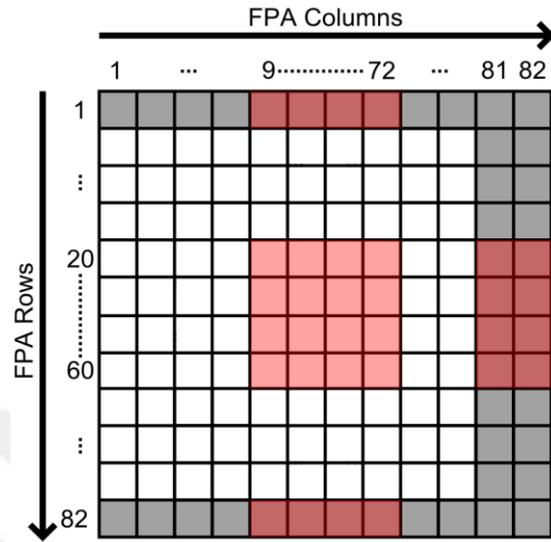
(a)

COLBEGIN=3, COLEND=6, ROWBEGIN=13, ROWEND=44
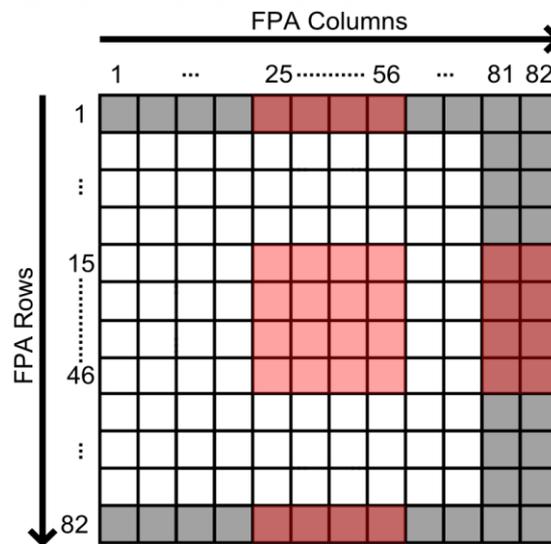
(b)

Figure 5-6: Illustration of frame windowing for 2 different sets of frame windowing register values.

5.2.1.6 Pixel Level Biasing Memory

Pixel level biasing (PLB) memory of the second sensor is designed to store the calibration data of all pixels in the FPA. In order to store this amount of data, special attention is paid to the design of unit memory cell. For this purpose, the smallest D-latch memory that is provided by XT0.18 design kit is further modified to reduce its layout area. The resulting circuit schematic and layout view of the unit memory cell which can store 1-bit information is given in Figure 5-7. As shown in Figure 5-7, unit memory cell is designed to have tri-state output with enable input. In order to calibrate detector biases, 6-bit calibration data is assigned to each pixel in the FPA. This data is used for multiplexing the PLB DAC output to select an optimum biasing point that provides the highest dynamic range for the corresponding pixel. The PLB memory block is associated with a memory address decoder to enable single memory address at a time. For this reason, the outputs of the calibration bits corresponding to pixels in the same FPA column are designed to share common data bus. In frame capturing mode, memory address decoder shares the same input with the row address decoder which means that number of FPA rows equals to the number of memory address. PLB memory designed for the second sensor can be written either manually via external electronics or automatically via on-chip detector bias calibration circuit. If the sensor is in the idle mode, then memory enters into manual write configuration and allows external access. A memory buffer unit is designed to provide manual write operation. In order to write desired data to an address of PLB memory, this buffer is first filled with that data through the SPI communication interface. After the buffer is filled with desired data, a special SPI packet is sent which writes the data in this buffer into the selected PLB memory address. Thus, whole memory can be filled with desired data by performing this operation for each memory address.

(a)

(b)

Figure 5-7: Schematic (a) and layout (b) view of the unit memory cell that can store 1-bit data.

5.2.1.7 Analog Comparator

The analog comparator is designed as a part of the on-chip detector bias calibration circuitry. It is used to generate binary feedback for the calibration controller block which will be discussed in the next section. The block diagram of the analog comparator section is illustrated in Figure 5-8. The negative input of the comparator is connected to the analog video output pad constantly while the positive input can be connected to either V_{clamp} voltage or internal DAC output that is programmable through the SPI interface. The voltage on the positive input of the comparator defines the mean value of the pixel output voltages after detector bias calibration. If it is selected as V_{clamp}, then the total unwanted integration gets close to zero at the end of calibration for $V_{clamp} = V_{rst}$. If it is selected as the output of the 8-bit DAC, then the center of the output voltage histogram is moved to the negative or positive supply rails according to the DAC output voltage after the calibration.
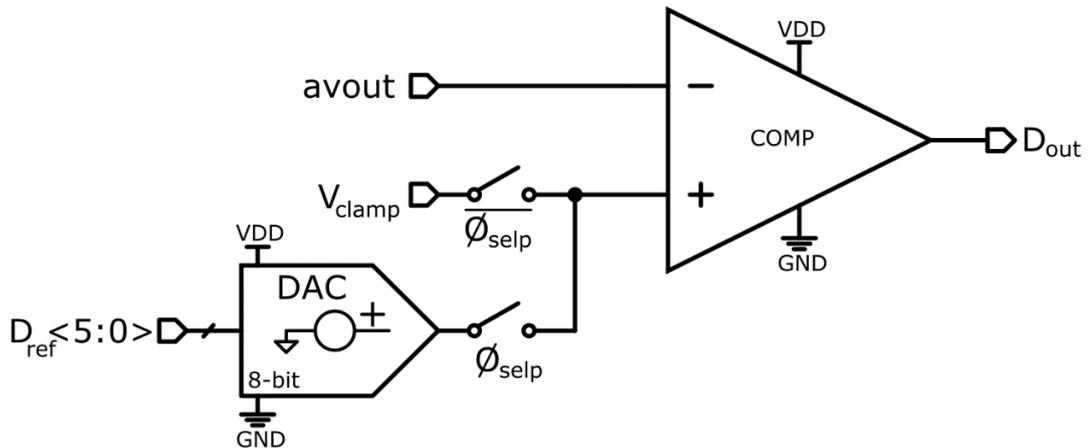

Figure 5-8: The block diagram of the analog comparator.

5.2.1.8 Calibration Controller

Calibration controller is a digital circuit that is able to read/write data from/into PLB memory during frame capturing mode. It includes Successive Approximation Register (SAR) circuit to perform binary search operation which allows finding optimal detector biasing value in a just few iterations. It is active during the calibration phase only and becomes inactive after bias calibration is done. Calibration controller is composed of column unit cells each of which corresponds to single column readout channel. As shown in Figure 5-9, each calibration controller unit cell consists of 3 main sub-blocks; shift register, data generator, and data loader. The shift register is used to point calibration data bit that will be set as high. The number of calibration steps is equal to the calibration data bit size which is 6 for both the first and the second sensors. With the start of calibration mode, *coin* is set as high and shifted into the shift register from the MSB side in the first calibration step after which it goes back to low again. Then, this bit is shifted from MSB to LSB side at each calibration step. At the first calibration cycle, *init_cond* is also set to high by digital controller block and data loader block writes the mid of the detector biasing range (6b'100000) into the corresponding pixel memory without considering the data coming from the data generator block. In the next calibration steps, *init_cond* signal goes back to low again and data loader block writes the data coming from the data generator block into the corresponding pixel memory. Data generator block decides which data to be written into the PLB memory by reading the latest data in the PLB
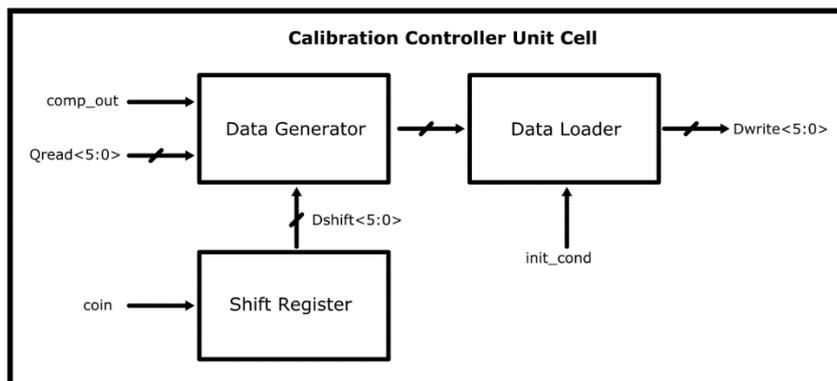

Figure 5-9: Block diagram of calibration controller unit cell.

memory and checking the binary feedback from the comparator which compares analog video output voltage with a programmable reference voltage. After bias calibration, the outputs of all pixels lie in the vicinity of this reference voltage making a Gaussian like curve. The details of detector bias calibration are given in Section 5.2.2

5.2.2   On-Chip Detector Bias Calibration

Simplified block diagram of the ROIC architecture used in the second sensor is illustrated in Figure 5-10. Each detector is connected to the corresponding column readout channel via row multiplexing switch during frame capturing mode. The connected detector is biased by the detector biasing circuit which reads biasing data from the calibration memory and generates detector biasing voltage accordingly. As a result of the detector biasing, integration current is generated. This current is sampled and then converted to an analog voltage by sample & hold circuit. This analog voltage buffered by line driver which is actually a unity gain buffer. The buffered signals at the output of column readout circuits are multiplexed by column multiplexing switches and transferred to the input of video buffer one by one. Then, video buffer transfers the multiplexed and buffered pixel output voltages to the analog video output pad of the sensor. The blocks described so far are common to the first sensor. In addition to these blocks, the second sensor contains on-chip detector bias calibration circuit as shown in Figure 5-10. This circuit is only active during detector bias calibration and composed of 3 main components; calibration memory (PLB memory), calibration controller and analog comparator. Both calibration controller and calibration memory blocks are distributed along the column readout channels such that each column readout channel is associated with a unit calibration controller cell and a calibration memory segment that stores the biasing data of the pixels corresponding to that column readout channel. On the other hand, there is only one analog comparator shared by the both top and bottom calibration controller blocks. This comparator compares a programmable reference voltage, V_{ref}, with the analog video output voltage of the sensor and generates a binary feedback for the

calibration controller unit cells, which produce new detector biasing data to be written into calibration memory, according to the calibration step and the value of binary feedback from the comparator. In order to trigger on-chip detector calibration circuit, the CAL bit in the sensor configuration memory is set. Then, digital controller enters on-chip detector bias calibration mode in the next frame and generates necessary timing signals for the calibration controller. At the end of detector bias calibration, CAL bit is reset by the sensor itself sensor operates in normal mode.
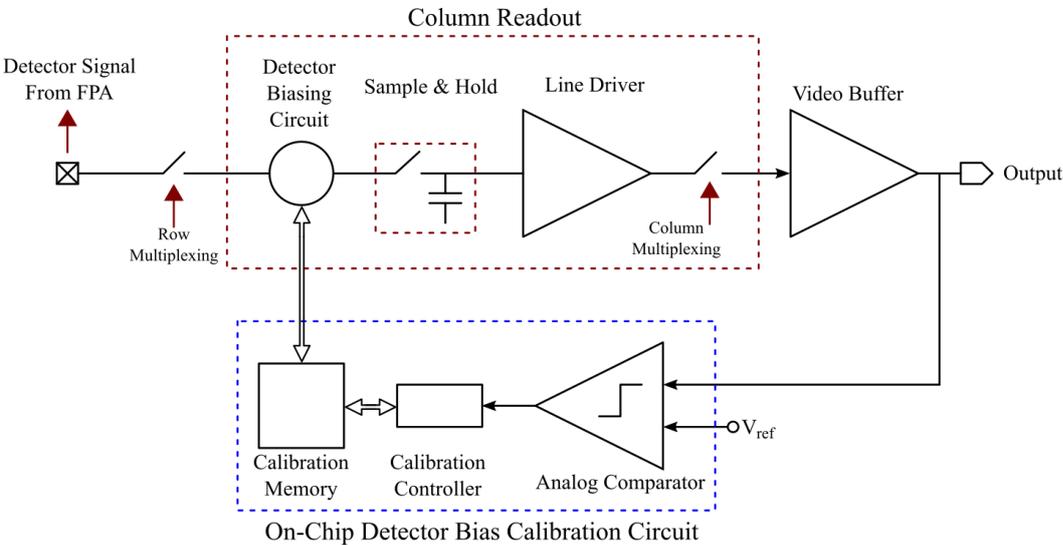
Figure 5-10: Simplified block diagram of the ROIC architecture in the second sensor.

CHAPTER 6

TEST RESULTS OF THE SECOND SENSOR

As in the first sensor, the complementary circuit blocks of the second sensor that lie outside the scope of this thesis work have been designed by other IC design group members of Mikrosens. The designed digital blocks developed within the framework of this thesis were interfaced with these circuit blocks, e.g. FPA, column readout channels, bias generator, voltage regulator, and video output buffer. The sensor was fabricated in an SOI 0.18 µm CMOS process. The post-CMOS MEMS processing was done by MEMS processing group of Mikrosens in METU-MEMS Research and Applications Center facilities. The purpose of the post-CMOS MEMS processing is to suspend pixels in the FPA and to vacuum package the sensors. The test and characterization of the sensor were done with the LWIR Camera Core and the PC companion software developed by the System Group of Mikrosens.

This chapter is organized as follows: Chapter 6.1 gives an introduction about the test system, Chapter 6.2 and Chapter 6.3 summarizes the test results of the digital blocks and analog comparator respectively, Chapter 6.4 covers the tests of the detector bias calibration and finally Chapter 6.5 concludes the chapter.

6.1   Introduction

This section gives the test results of the circuit blocks, which are related to this thesis work, in the fabricated second sensor. After the pixel suspension process, the sensors are vacuum packaged with wafer-level vacuum packaging process. In order to increase the IR transparency of the cap wafer that is used for vacuum packaging, anti-reflection (AR) coating on the cap wafer is done with external service procurement. Then, the final wafer is diced to singularize vacuum packaged sensor dies. Figure 6-1 shows a sample picture of the vacuum packaged sensor die. The

LWIR Camera Core that includes camera housing with optical shutter and a replaceable lens, the second sensor, and an analog-to-digital converter that converts analog sensor output to digital domain was designed as an end product by the system group of Mikrosens. In order to provide bias voltages to camera core, handle digital data, and set up a communication network between the sensor and the computer, the evaluation board and the companion PC software that processes the microbolometer output were also designed by the same group. The pictures of the LWIR Camera Core and its evaluation board are shown in Figure 6-2. In contrast to the dewar environment used to characterize the first sensor, the tests of the second sensor have been done using this LWIR Camera Core – evaluation board – PC software system that is well enough to characterize the sensor performance thanks to the high quality vacuum packaging and AR coating.

The next sections in this chapter will give the summarized information about the tests of the circuits designed in the scope of this thesis work.
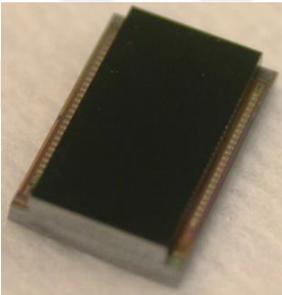

Figure 6-1: A sample picture of the vacuum packaged sensor die.

(a)   (b)

Figure 6-2: The pictures of LWIR Camera Core (a) and evaluation board with LWIR Camera Core connected (b).

6.2   Digital Circuits

The digital circuits of the second sensor can be grouped as two main parts; the serial peripheral interface and the digital controller. The rest of this section will summarize the tests of these parts in order.

6.2.1   Serial Peripheral Interface

The second sensor implements a similar programming interface with the one in the first sensor. The only difference is the representation of the address and data bits in a 16-bit word where the MSB defines the type of the sensor memory to be used for write operation, the next 7-bit defines the memory address and the last 8-bit defines the data to be written into that address. The second sensor provides 86 memory addresses allocated for sensor configuration, each of which can store 8-bit configuration data and a reserved memory unit that can hold 4-bit data resulting in total of 692 programmable bits for sensor configuration. Also, it has about 5 kB (82x82x6-bit) of memory to store the calibration data of each pixel. Figure 6-3 (a) shows the test results of a sample programming of address 4 with data "01001111" and (b) shows a sample SPI read operation from the same address.
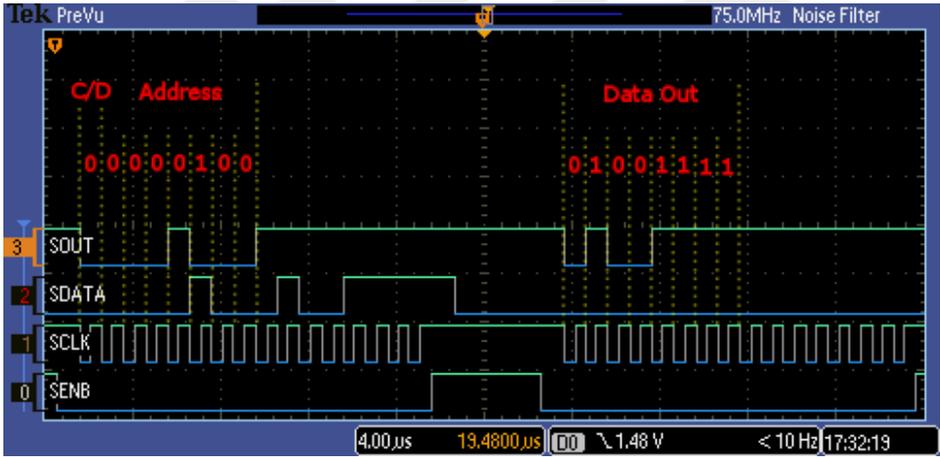
6.2.2   Digital Controller

Digital controller block of the second sensor is very similar to the one in the first sensor. It requires only the CLK signal from the external electronics to generate ROIC timings, frame synchronization signals etc. The same frame synchronization signals are also valid for the second sensor, but there is no STPLB signal anymore since detector bias calibration does not require synchronization with the external electronics in the second sensor. The setting of the START bit as high in the reserved memory triggers digital controller block and the aforementioned ROIC timings and synchronization signals become active. Test results of these signals are presented in Figure 6-4. Compared to the first sensor, PIXSYNC of the second sensor is more

flexible such that its polarity can be reversed and it can be delayed for a specific amount of time. Figure 6-5 shows the test result of PIXSYNC polarity reversing and delay adjustment.

(a)

(b)

Figure 6-3: The test result of (a) a sample programming of address 4 with data "01001111" and (b) a sample SPI read operation from the same address.
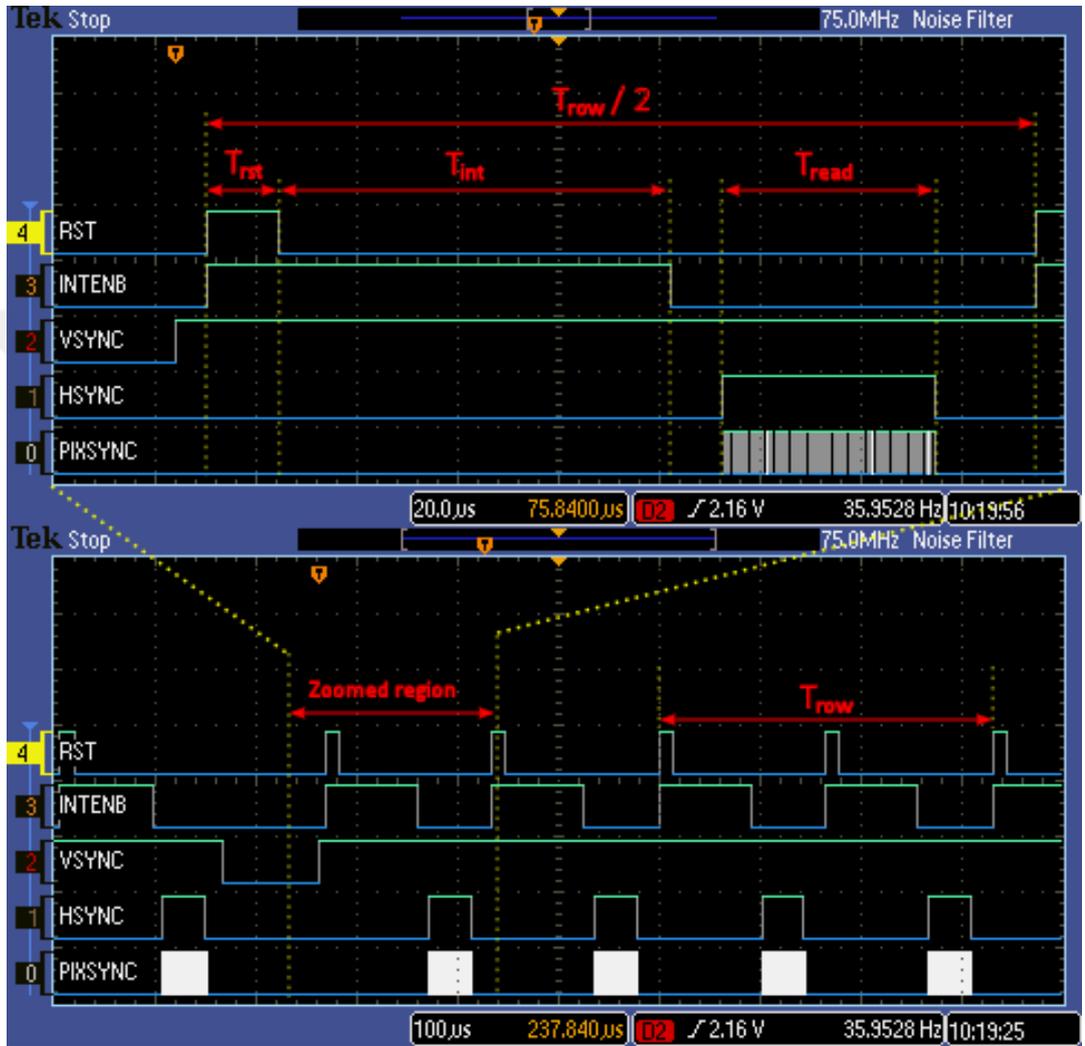
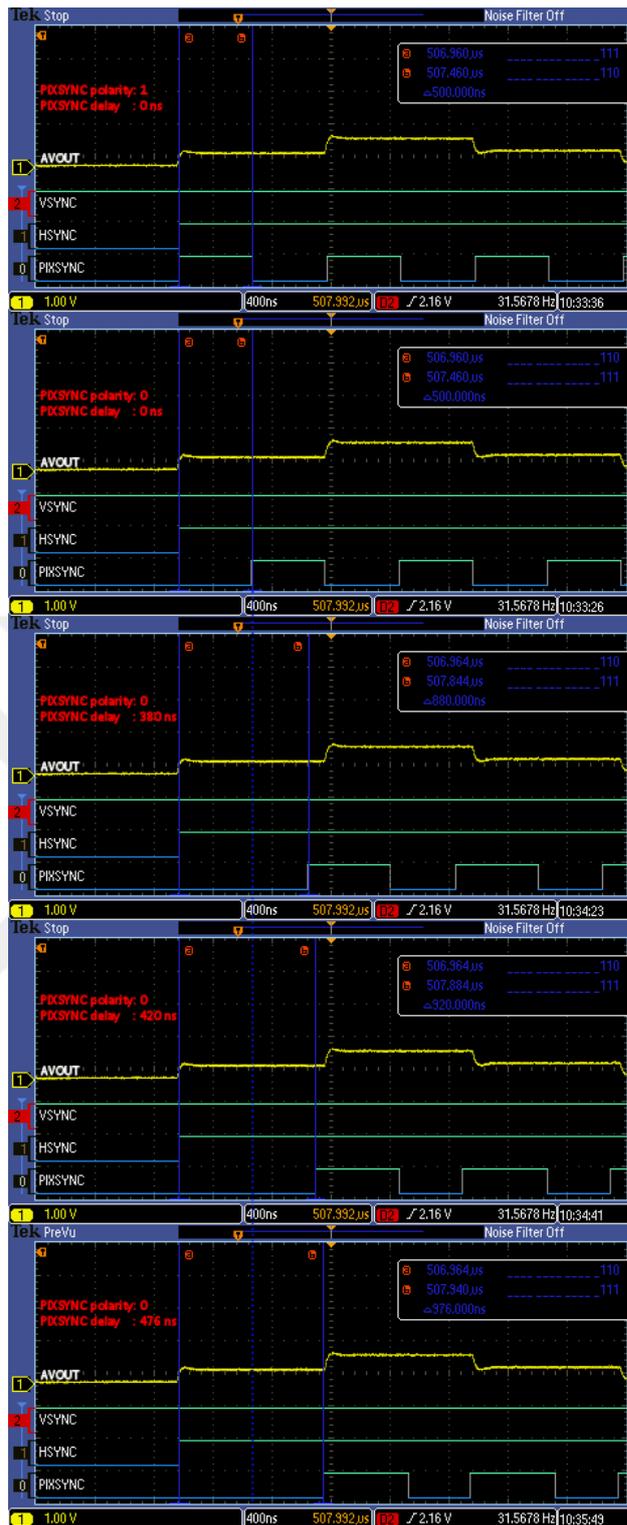Figure 6-4: The test results of some of the important digital signals generated by the digital controller of the second sensor.

Figure 6-5: The test result of the PIXSYNC polarity reversing and delay adjustment.

6.3   Analog Comparator

The analog comparator is used to generate binary feedback for the calibration controller block. Its negative input is connected to the analog video output pad constantly. In order to test analog comparator, first, its positive input configured to be connected to V_{clamp} voltage which is adjusted by the 8-bit DAC inside the sensor and can be measured from one of the sensor pads. Next, sensor video output is put into test mode in which output voltage of an internal 6-bit test DAC is given to the analog video output pad of the sensor by configuring the input multiplexing switches of the video buffer accordingly. Lastly, the sensor is configured such that binary output of the comparator can be observed from one of the digital output test pads of the sensor. With this configuration, all 3 ports of the comparator are observed via testing instrument from the 3 different pads of the sensor which are analog video output pad, V_{clamp} monitoring pad, and one of the digital output test pads. By keeping the output voltage of 6-bit test DAC unchanged and sweeping the value of V_{clamp} voltage through its 8-bit DAC from 0 to 3.3 V, the voltage transfer curve of the comparator is obtained roughly. Since the resolution of V_{clamp} voltage is 8 bits, a precise characterization of the analog comparator is not possible; therefore, the test results prove only that the input offset voltage of the comparator is less than approximately 8 mV. The obtained voltage transfer characteristic of the analog

Table 6-1: The obtained voltage transfer characteristics of the analog comparator around transition region. The designed comparator has less than 8 mV of input offset voltage.

V_{clamp}	avout	V_{clamp} – avout	D_{out}
1.559	1.579	-20 mV	0
1.571	1.579	-8 mV	0
1.579	1.579	0 mV	1
1.591	1.579	12 mV	1

comparator around transition region is presented in Table 6-1 which states that the designed comparator has less than 8 mV of input offset voltage.

6.4 Image Acquisition and On-Chip Detector Bias Calibration

In order to verify the functional operation, the whole readout circuit of the second sensor was tested by the IC Design Group Members of Mikrosens. Operating points of the sub-blocks of the readout circuit were adjusted so that optimum performance can be obtained. Figure 6-6 (a) shows a sample raw image obtained from the second sensor and (b) shows the same image after deinterlacing process. This image was taken prior to the detector bias calibration under 100 μs of integration time with 31 pF of integration capacitance configurations. As shown in the Figure 6-6, the columns that correspond to the top column readout channels look brighter than the ones that correspond to the bottom column readout channels. The reason for this non-uniformity may be due to the asymmetric power line routings in the physical layout of the sensor and it can be eliminated by detector bias calibration. The FPA output

(a)   (b)
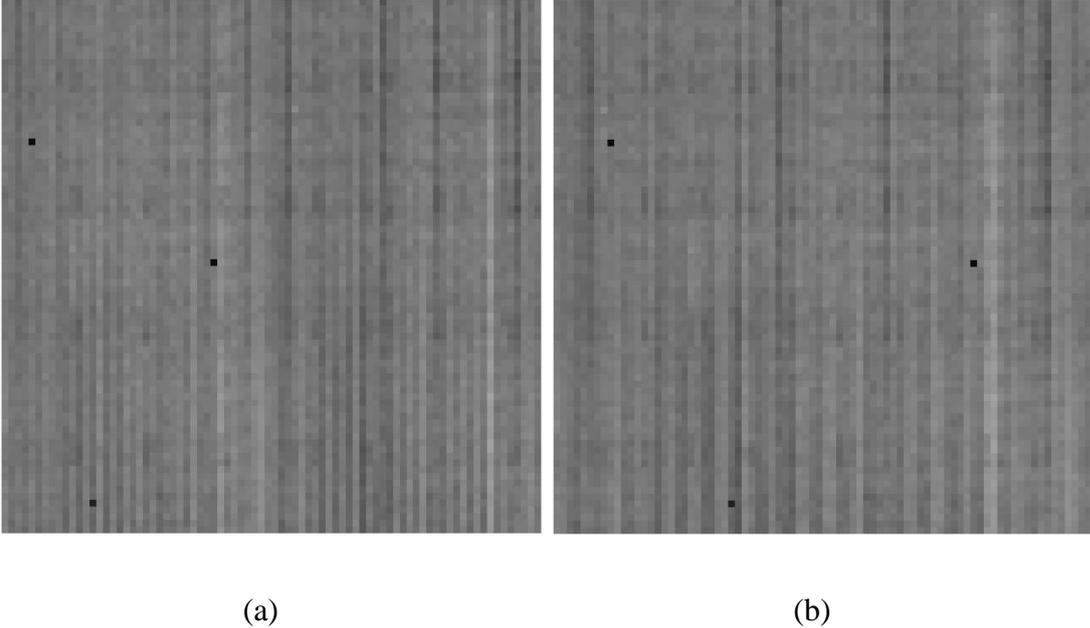
Figure 6-6: (a) shows a sample raw image obtained from the second sensor (b) shows the same image after deinterlacing process.

voltage histogram of the obtained image is illustrated in Figure 6-7. If Figure 4-6 is compared with the Figure 6-7, it can be concluded that the output response of the second sensor is much more uniform than the one in the first sensor under the same readout circuit gain configurations. The main reason for better uniformity in the second sensor is the usage of the more advanced CMOS process during production of the sensor. Also, a different MEMS technique is used for suspending the pixels in the second sensor. This new technique results in much better uniformity compared to the pixel suspension method used in the first sensor.
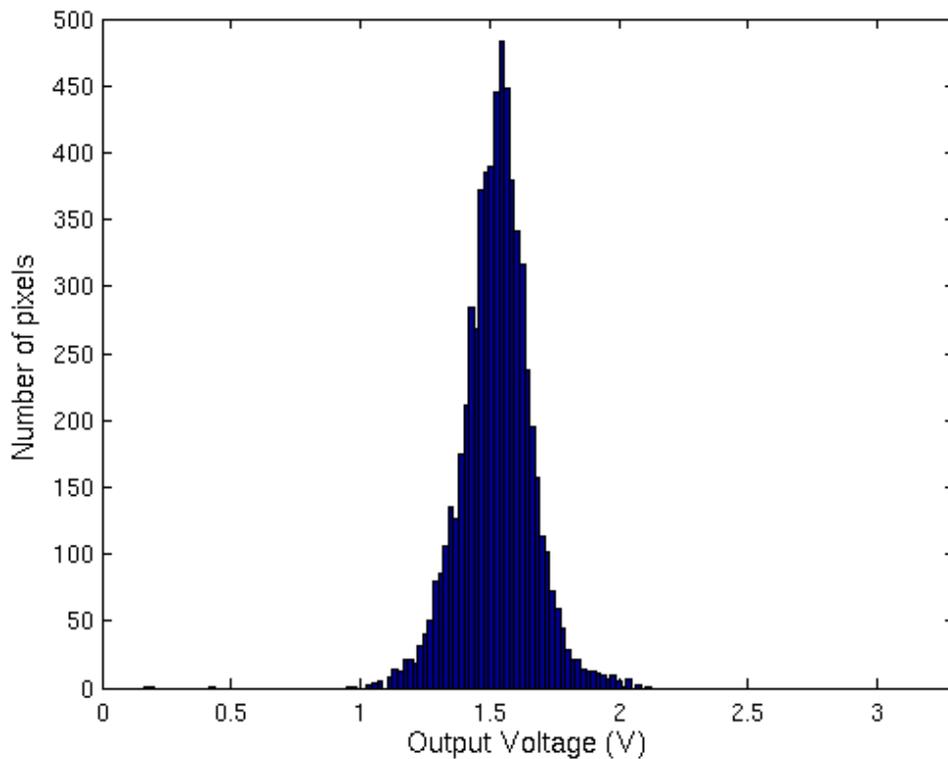
Figure 6-7: The FPA output voltage histogram of the obtained image.

In order to test on-chip detector bias calibration circuitry, first, the maximum and the minimum voltage levels of the second stage PLB DAC are tuned as described for the first sensor. After this tuning is accomplished, detector bias calibration is triggered by setting CAL bit in the sensor configuration memory while the sensor is in the frame capturing mode. The raw images obtained at each step of the on-chip detector bias calibration and the corresponding output voltage histograms are illustrated in Figure 6-8. These images were also obtained for 100 µs of integration time and 31 pF of integration capacitance so that the effectiveness of the on-chip detector bias calibration circuit can be observed by comparing Figure 6-6 (b) with Figure 6-8 (g). The standard deviation of the FPA output voltage is reduced from ~132 mV to ~8 mV after the on-chip detector bias calibration. Each calibration step takes at least 2 frame cycles only; however, it can be programmed up to 32 frame cycles so that the detector output voltage can stabilize better before passing to the next calibration step.
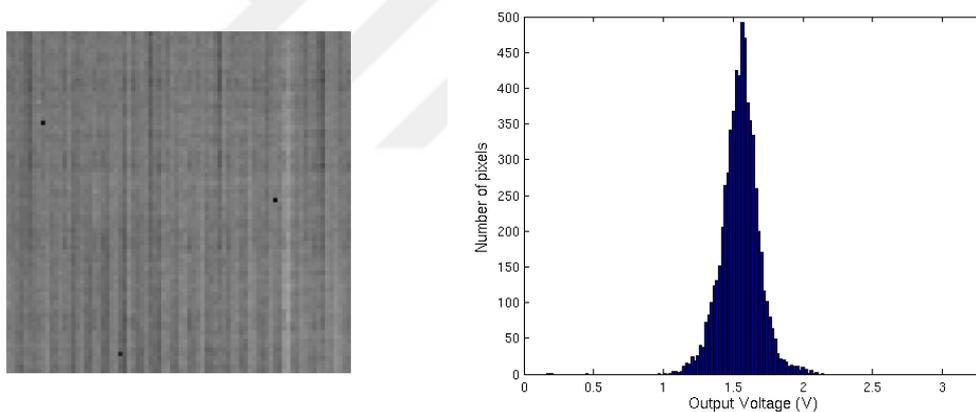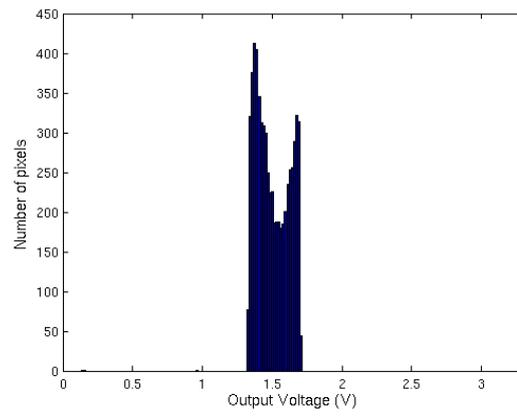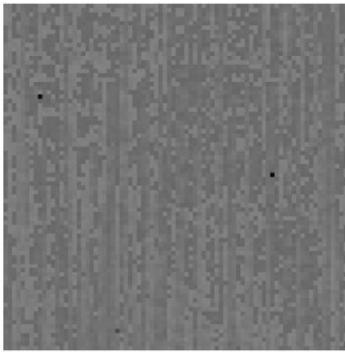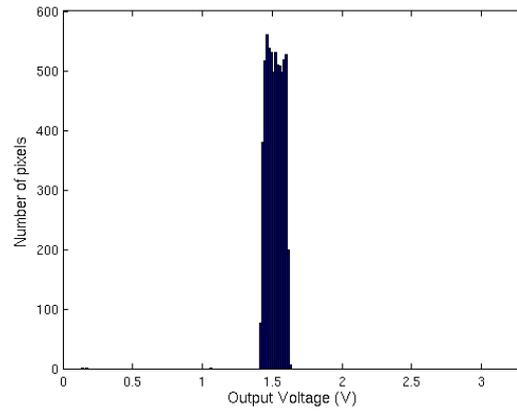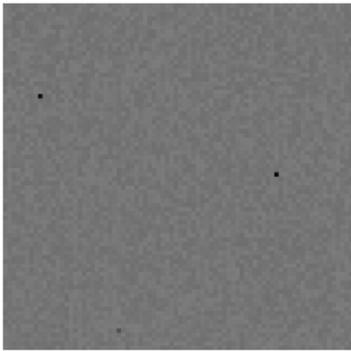

(a)

Figure 6-8: The raw images and the corresponding output voltage histograms obtained at each step of the on-chip detector bias calibration. Figures (a) to (g) correspond to calibration steps 1 to 7.
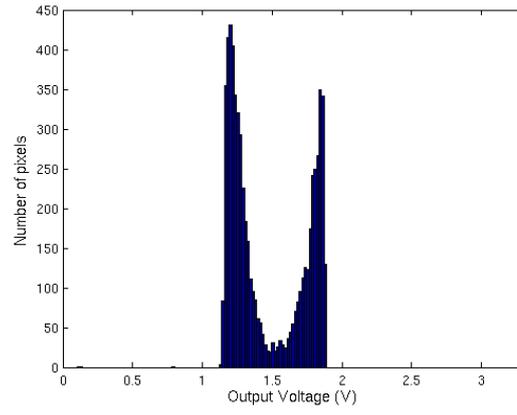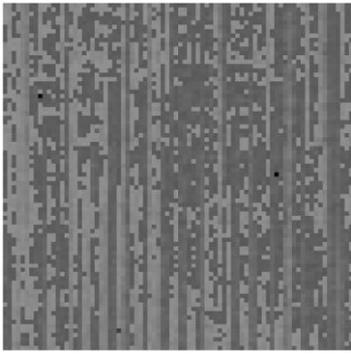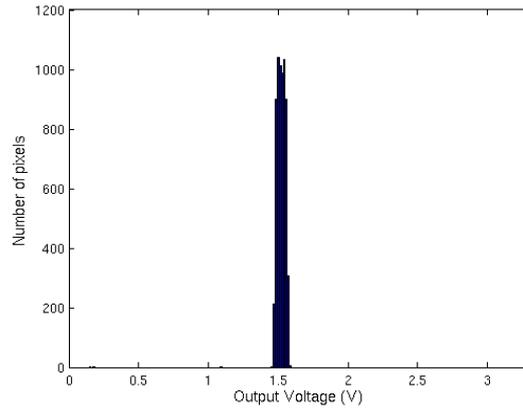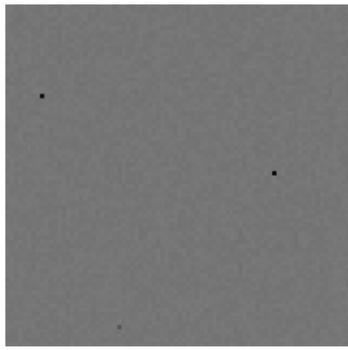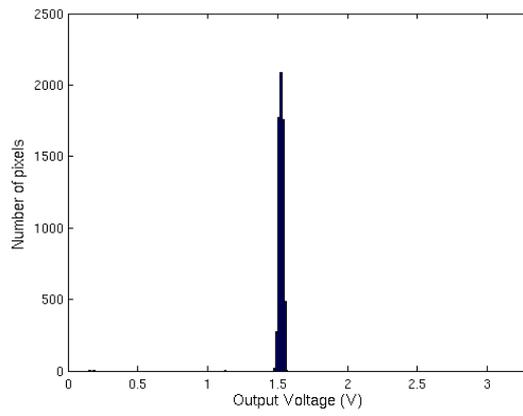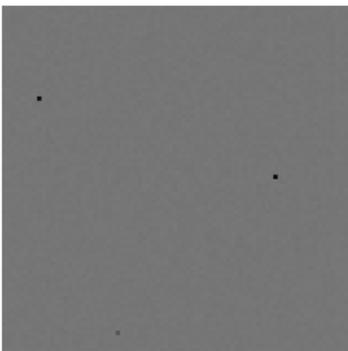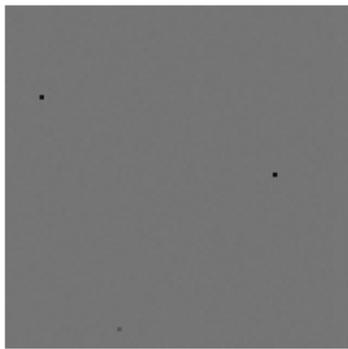
(b)

(c)


(d)

Figure 6-8 (cont'd)

(e)

(f)
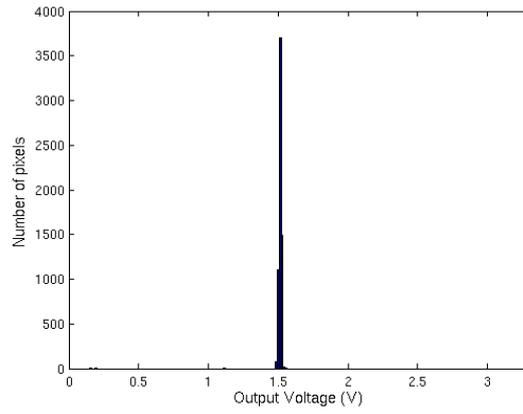
(g)

Figure 6-8 (cont'd)

The integration capacitor is designed to be configurable from 1 pF up to 31 pF so that a wide range of readout circuit gain can be used. However, as readout gain increases, the effect of non-uniformities on the output voltage becomes more visible. In order to observe the performance of on-chip detector bias calibration circuit under extreme readout gains, one more test has been performed by keeping the integration time unchanged, but configuring the integration capacitor as 1 pF which corresponds to 31 times more readout circuit gain. Figure 6-9 (a) and (b) show the obtained images and corresponding output voltage histograms before and after the calibration when the readout circuit gain is increased 31 times, respectively. As shown in Figure 6-9, thanks to the highly uniform FPA and designed on-chip detector bias calibration circuit, no saturated pixels are observed apart from dead pixels even for extremely high readout gain configurations.

After some image processing such as one-point and two-point corrections, dead pixel correction, resolution enhancement, color mapping, and contrast-brightness adjustments [21], sample images were obtained from the second sensor using the LWIR Camera Core as illustrated in Figure 6-10. These images were taken with the following camera and sensor related parameters; F1.1 Germanium lens, 1 pF integration capacitance, 100 µs integration time and 4 times frame averaging. The resulting frame rate under such condition is about 8 fps, which is a typical frame rate value for low cost thermal imaging cameras. The NETD histogram of the LWIR Camera Core is shown in Figure 6-11. As shown in the figure, the peak NETD is about 94 mK which is low enough for most of the low-cost thermal imaging applications.
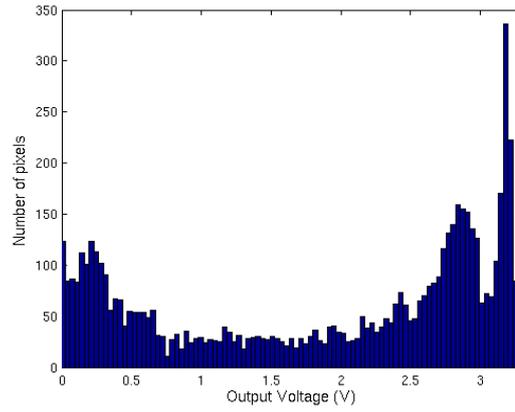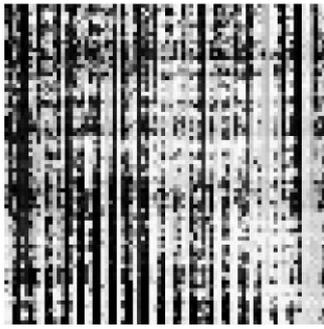
(a)
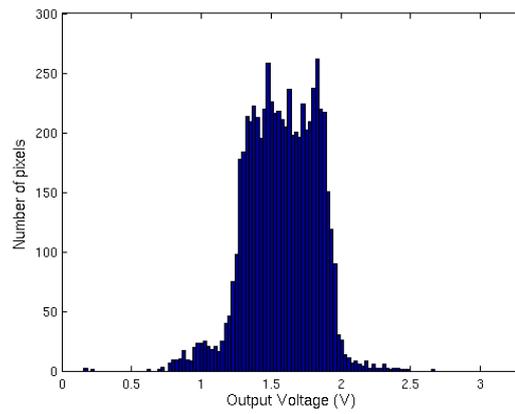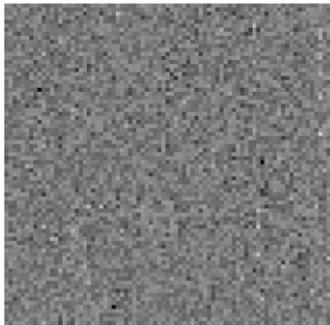
(b)

Figure 6-9: The obtained images and their output voltage histograms when the readout circuit gain is increased 31 times (a) before the detector bias calibration (b) after the detector bias calibration.
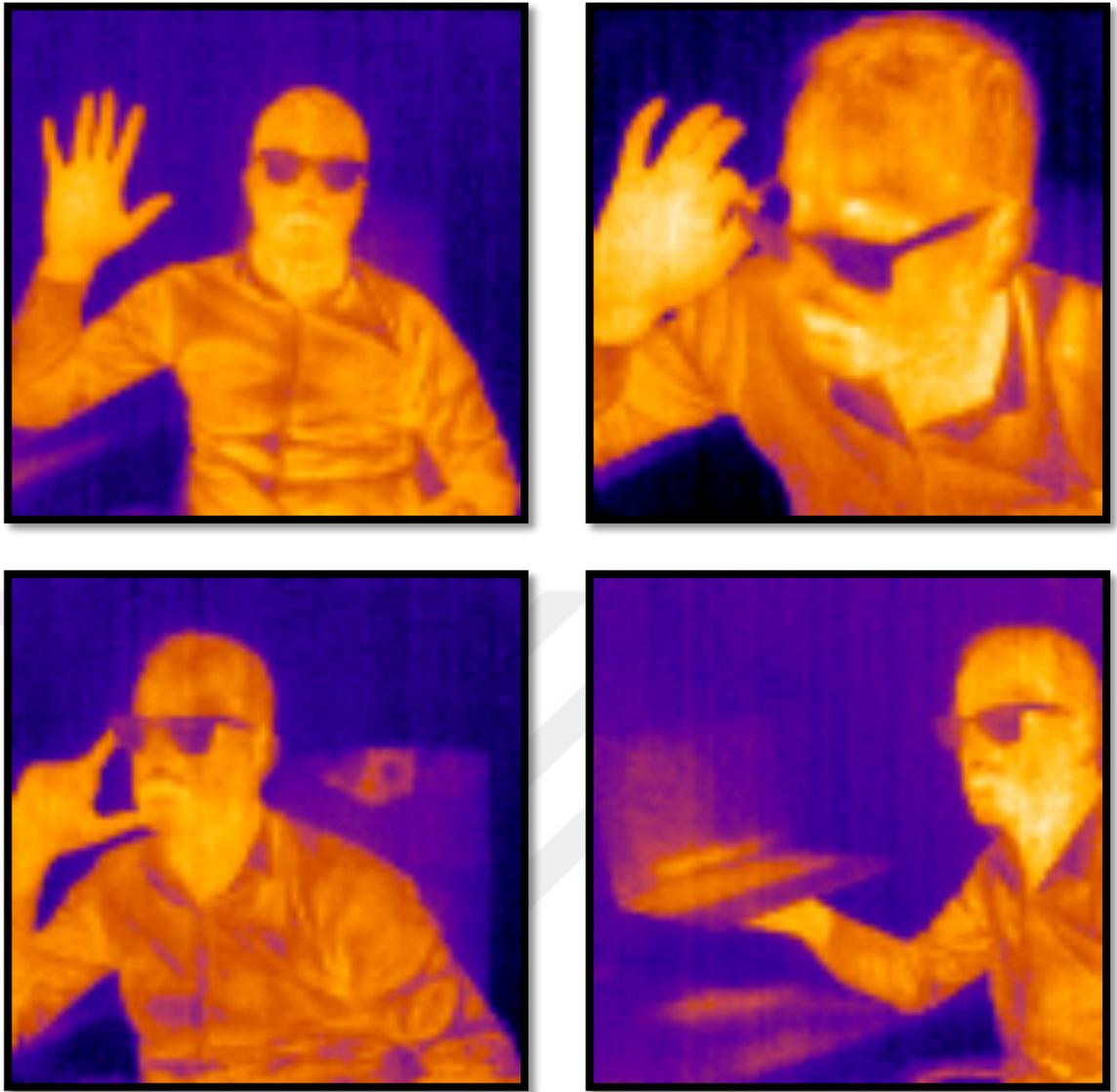
Figure 6-10: Sample images obtained from the second sensor after one-point correction, and contrast and brightness adjustments.
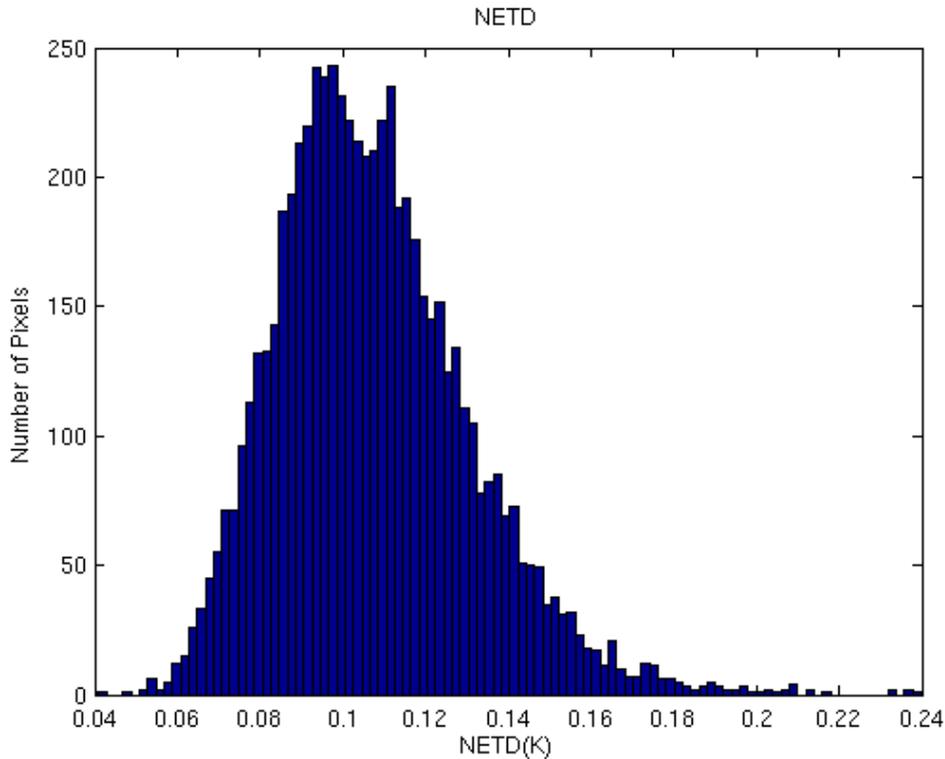
Figure 6-11: NETD histogram of the LWIR Camera Core developed using the second sensor.

6.5   Conclusion

This chapter summarized the test results of the circuit blocks, which are related to this thesis work, in the second sensor. Tests were conducted on the Mikrosens's LWIR Camera Core product. First, serial peripheral interface has been tested to verify that the sensor is programmed correctly. Then, digital controller block has been tested to verify that digital timings are all as expected. Next, the overall readout circuit was operated and some sample images were generated. Finally, the operation of on-chip detector bias calibration circuit has been tested.

The test results in this chapter verify that all the circuit blocks in the second sensor developed in the scope of this thesis operate as expected. Thanks to the efficient on-chip detector bias calibration circuit developed, the second sensor can be used under extreme operating conditions such as very low or high temperature environment, very high readout gains etc. The second sensor is now being used in the commercial camera systems.

CHAPTER 7

CONCLUSION

The research conducted in the scope of this thesis involves the design and development of advanced circuit architectures for readout electronics of low-cost resistive type microbolometer FPAs. Two circuit architectures are designed in this framework that focus on improving sensor performance and operational flexibility. The first circuit architecture is developed for 40x40 CMOS IR FPA with 60 μm pixel pitch and the second is developed for 80x80 CMOS IR FPA with 35 μm pixel pitch. After the Post-CMOS processing of the first sensor FPA, the operation of the developed circuit architecture is verified with the camera system developed by System Group of Mikrosens. A precise and efficient detector bias calibration algorithm developed and implemented as a firmware block in the camera system. The algorithm along with the developed detector bias calibration circuit proved that main performance limiting factors, which are detector bias heating effect and resistance non-uniformity, can be compensated in just 7 frame cycles. This improvement makes long integration times possible, reduces number of bit requirements of the ADC, increases detectable target temperature range and operating temperature range of the sensor, enables usage of small integration capacitances, relaxes maximum swing requirements of the OPAMPs used in the analog front-end circuitry etc.

The second circuit architecture has several improvements compared to the first one. First of all, on-chip calibration memory is designed to store bias calibration data of all pixels thanks to the use of the more advanced CMOS process. Moreover, the detector bias calibration algorithm developed for the first sensor is redesigned as a circuit block and integrated into the second sensor. This improvement allows fully on-chip non-uniformity correction, which reduces the overall camera system complexity and costs, enables simpler electrical interface between sensor and camera

electronics, and decreases the total power dissipation of the camera system thanks to the elimination of continuous calibration data transfer between the sensor and master device. Lastly, some extra features are added to the digital controller unit such as programmable frame windowing and pixsync delaying. Frame windowing allows user configurable output image resolution which may be required for some applications to increase frame rate, and decrease total power dissipation of the sensor etc. The programmable pixsync delay provides additional settling time for the analog video output signal before it is sampled by the ADC.

A summary of the work performed in this thesis is listed below:

1. Offset sources in resistive type microbolometer sensors are analyzed carefully prior to the development of a solution for offset compensation.

2. Offset calibration methods in the literature are investigated. Advantages and disadvantages of the calibration methods in the literature are evaluated and detector specific biasing is selected as the offset calibration method in this thesis work.

    a. One of the most important offset sources of the uncooled infrared imaging systems is the large temperature rise due to applied electrical bias on the detector which results in unwanted detector current which can be minimized by applying a pixel specific biasing.

    b. Another important offset source in the microbolometer sensor is the resistance non-uniformity across FPA. This non-uniformity can also be compensated by detector bias calibration successfully.

3. The first circuit architecture is designed for readout electronics of 40x40 FPA with 60 µm detector pitch using 0.35 µm CMOS technology. A digital controller is implemented to manage the general operation of the sensor, provide the necessary signals for column readout circuits, and control electrical interface between sensor and the master device. A 6-bit detector bias calibration block is designed to allow pixel-level uniformity correction. These circuits are designed to be very flexible in order to allow various types of operating modes.

4. The designed circuit blocks in the first sensor are tested and verified. Then, in order to improve sensor performance, a simple but very efficient detector bias calibration algorithm is developed on FPGA. The test results show that the effects of all non-uniformity sources on the pixel output voltage can be compensated in just 7 frames with a simple camera electronics.

5. The second circuit architecture is designed for readout electronics of 80x80 FPA with 35 µm detector pitch using 0.18 µm CMOS technology. This circuit architecture has several improvements as summarized at the beginning of this chapter.

6. The designed circuit blocks in the second sensor are tested and verified. The test results show that the second sensor can self-calibrate itself with only on-chip components in just 13 frames. The developed circuit architecture makes the second sensor as the first uncooled thermal imaging sensor with on-chip non-uniformity correction feature in Turkey.

There are two important works that need to be done in order to increase the sensor performance, and reduce the camera system cost and size further. These future works are summarized as follows:

1. Both the first and second sensors have analog outputs. This necessitates the use of external ADCs. However, this increases the total cost and size of the camera system. Also, the low noise analog video bus between sensor and ADC is vulnerable to any signal coupling which is an important noise source and could be solved by developing on-chip low power ADCs.

2. The camera systems developed using the first and the second sensors require shutter for one point non-uniformity correction. Embedding a shutter in the camera system requires an extra effort; moreover, it increases the cost and the size of the camera system. However, it is possible to obtain substrate temperature independent video signal for a wide temperature range by implementing certain calibration procedures. Although some works have already been performed and good results have been obtained in a dewar environment, more effort is required when developing the shutterless camera system.

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