T.C.
SÜLEYMAN DEMİREL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

DESIGN AND SIMULATION OF SIGMA DELTA FRACTIONAL N-PLL MODULATOR USING ADVANCED DESIGN SYSTEM (ADS)

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"Design and Simulation of Sigma Delta Fractional N-PLL Modulator Using Advanced Design System (ADS)" submitted by **Harith Nazar Mustafa AL-NUAIMI** in partial fulfillment of the requirements for the degree of **Master of Science** in **Department of Electronics and Communication**, Graduate School of Natural and Applied Sciences, Süleyman Demirel University by,

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COMMITMENT

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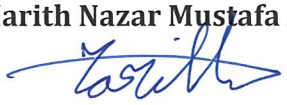
Harith Nazar Mustafa Al-NUAIMI



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ABSTRACT

Master of Science

DESIGN AND SIMULATION OF SIGMA DELTA FRACTIONAL N-PLL MODULATOR USING ADVANCED DESIGN SYSTEM (ADS)

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Phase locked Loop (PLL) frequency synthesizers are widely used in modern communication systems due to its excellent performance, relative simplicity, and low cost. The switching time and frequency resolution are the two keys trade-off of the frequency synthesizers, where the switching time is related to the loop bandwidth of the pll. Fractional-N pll frequency synthesizer is the most used technique to obtain high frequency resolution and good switching time. The fractional division ratio is obtained by changing the division ratio between two integer numbers; the continuous changing in the division ratio will generate a Spurs noise in the spectrum output of the frequency synthesizer. Sigma-Delta modulation technique is used to obtain a spectrum without any Spurs noise.

In this thesis, the analysis, and design of 1st, 2nd, and 3rd order sigma-delta modulators, and 2nd, 3rd, 4th order loop filters are discussed to show their impact on the performance of fractional-N pll frequency synthesizer for Bluetooth system. Advance Design System (ADS) and Matlab programs are used for the design and simulation of sigma-delta fractional-N pll frequency synthesizer. All simulation results showed that the system is stable, and most of the results matched the requirements for Bluetooth system. Simulation results also showed that the frequency synthesizer with 3rd order loop filter and 2nd order sigma-delta modulator is one of the best proposed designsince it provideslow phase noise, spectrum free from any spurious noise, and perfect switching time, where the phase noise was -125 dBc/Hz at 2 MHz offset frequency, -131.5 dBc/Hz at 3 MHz, andthe switching time was 13.69 µsec at 2401.933 MHz output frequency.

Keywords: PLL, frequency synthesizers, ADS, VCO, sigma-delta modulators, Phase Frequency Detector , Chaege Pump.

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ÖZET

Yüksek Lisans Tezi

GELİŞMIŞ DIZAYN SISTEMINDE KULLANILAN SIGMA-DELTA KIŞMI N-PLL MODÜLATÖRÜNÜN SIMÜLASYON VE DIZAYNI

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PLL frekans birleştiricileri düşük maliyet, basit yapısı ve harika performansları nedeniyle modern iletişim sistemlerinde yaygın bir şekilde kullanılır. Açma kapama zamanı ve frekans çözünürlüğü ile değiş tokuşun iki anahtarıdır. Kademeli-N frekans birleştiricisi yüksek frekans çözünürlüğü, ve açma kapama zamanını sağlamak için en fazla kullanılan tekniktir. Kısmi ayrım oranı iki tam sayı arasındaki ayrım oranını değiştirmek için elde edilir. Ayrım oranındaki sürekli değişim frekans birleştiricisinin spektrum çıkışında ses üretir. Sigma-delta modülasyon tekniği ise ses üretimi olmadan spektrum sağlamak için kullanılır.

Bu çalışmada birinci, ikinci ve üçüncü dizayn ve analiz sigma-delta modülatörlerini düzenler. İkinci, üçüncü, dördüncü de bluetooth sisteminde kademeli-N frekans birleştiricisinin performansındaki etkisini göstermek için tartışılan döngü süzgeçlerini düzenler. Gelişmiş dizayn sistemleri ve Matlab programları kademeli-N frekans birleştiricisinin performansındaki sigma deltanın simülasyon ve dizaynı için kullanılırlar. Tüm simülasyon sonuçları sistemin sabit olduğunu ve sonuçların çoğunun bluetooth sistemi için gereksinimlerle eşleştiğini gösterir. Simülasyon sonuçları aynı zamanda üçüncü frekans birleştiricisinin döngü süzgecini düzenlediğini ve ikincisinin de teklif edilen en iyi dizayn olan sigma delta modülatörünü sağladığını da gösterir. Delta modülatörü yavaş faz sesi, herhangi bir yapay sesten spektrum, 2MHz ofset frekansında faz sesi -125dBc/Hz, -131.5dBc/Hz 3MHZ olduğu zaman harika bir açma kapama zamanlaması, çıkış frekansı 2401.933MHz olduğunda açma kapama zamanlaması 13.69 değerlerini sağlar.

Anahtar Kelimeler:PLL, frequency synthesizers, ADS, VCO, sigma-delta modulators, Phase Frequency Detector , Chaege Pump.

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LIST OF SYMBOLS AND ABBREVIATION

N	Division ratio
ω_c	Carrier frequency
Δf	Frequency offset
dBc/Hz	Phase noise unit
dBc	Spurs noise unit
F_{Ref}	Input signal frequency
ω_S	Spurs noise frequency
ω_{int}	interference frequency
ω_{IF}	Information signal frequency
V_{out}	Loop filter output voltage
I_1	Charge current of charge pump
C	Capacitor
$\Delta\phi$	The phase of phase detector output signal
I_2	discharge current of charge pump
I_{net}	Charge pump total current
F_{FR}	Free Running Frequency
K_{VCO}	VCO Gain
V_{tune}	VCO input voltage
Hz/v	VCO Gain unit
F_{vco}	VCO output frequency
ϕ_{vco}	VCO output Phase
F_{out}	Output Frequency
$F_{B.W}$	Bandwidth frequency
$\propto$	Fractional part for the division ratio
OSR	Over sampling
MASH	Multi Stage Noise Shaping
ISM	Industrial Scientific-Medical
R	Resistance
Ø	Phase Margin
Z	Damping Factor

1. INTRODUCTION

Wireless communications have grown significantly in recent timesdue tothe lower cost and many new application which include wireless and cellular phones, Global Positioning Systems (GPS), Radio frequency identification devices and Bluetooth devices etc [Richard Gu,2007]. the Transceivers are The most important components for radio and telecommunications systems. Figure 1-1 shows Flipchartfor transceivers, where the Amplifier amplify the signal to be sent at transmission point then this signal mixed with the Oscillator's output signal by the Mixer, then the Filter make filtration to that signal, after that the filter's output signal amplify again to sent by the Antenna[Zhiming, 2007].

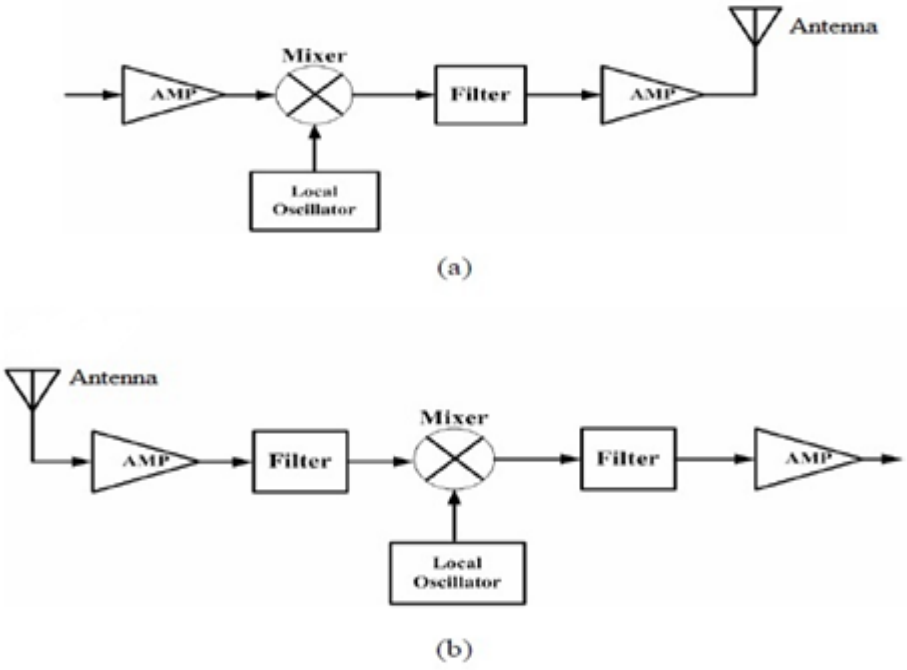


Figure 1-1Flipchart(a)Transmitter (b)Receiver

Modern communication systems protocols working on the allocation of frequency channels close to each other at very high frequencies. As an example, Bluetooth system allocates 79 frequency channels separated by a distance 1MHz at frequency range (2402 MHz – 2480MHz), where the noise that generated by the local oscillator was small enough in order not to affect to nearby frequency channels[Ranganathan, 2003], Local Oscillators usually used as frequency Synthesizer, frequency synthesizer exist in most transceiver devices to generate

one signal or several signals separated by a distance of a specific frequency depends on the user's application[H. T., 2008].

Usually the Receivers have high sensitivity to the signals and have high ability to capture the weak received signal among several undesirable noisy signals, As well as the Transmitters must be able to generate signals with sufficient capacity, very accurate and without any noise in the output spectrum[H. T., 2008].

There are several different techniques for Frequency Syntheser and most commonly used are [Marques, 1998]:

1) The direct analog synthesis : the most important features of this technology is a high frequency resolution and fast switching time but the disadvantages of this technique is not suitable for high frequency, low phase noise synthesis in conventional CMOS or (BiCMOS) technology and it is expensive .
2) The direct digital synthesis: the most important features of this technology is a high frequency resolution and fast switching time. It is also possible to fully appliance this technique in a standard CMOS technology. Furthermore, By simple modification of the phase accumulator structure, it even provides a simple way of achieving directly phase and frequency modulation at the cost of a slightly higher chip area. However, for typical wireless applications requiring high frequency and low phase noise, the hard demands on DAC clock frequency, resolution, non linearity and glitch energy make the usage of this technique impossible.
3) The indirect synthesis : by using Phase Lock Loop (PLL), By comparing with the two previous techniques, this technique is most commonly used to generate high-frequency signals, Also, the main building blocks of the synthesizer can be integrated in a BiCMOS or even in a CMOS technology. The most important of these technical features is low-cost, high accuracy, excellent performance, and contain very low phase noise, and with a range of high bandwidth up to l Giga Hertz and fast time stability.

Phase Locked Loop (PLL) was used for the first time in 1932 when deBellescizi used a tube-based Phase Locked Loop to synchronously demodulated radio signal. In 1960, the NASA satellite program using phase locked technique in satellite systems to determine the frequency of the transmitted signal . Today Phase Locked Loop (PLL) are used not only as frequency synthesizer also used in many application like filtering, control the speed of motors, frequency modulation and demodulation, and signal detector and other applications. PLL circuit be either analog or digital, but most common circuit use hybrid components both analog and digital[Jack R, 1985].

In general PLL consist of Voltage Controlled Oscillator (VCO), Loop Filter ,Phase detector and the source input signal[Kaveh, 2011] , as shown in figure 1-2

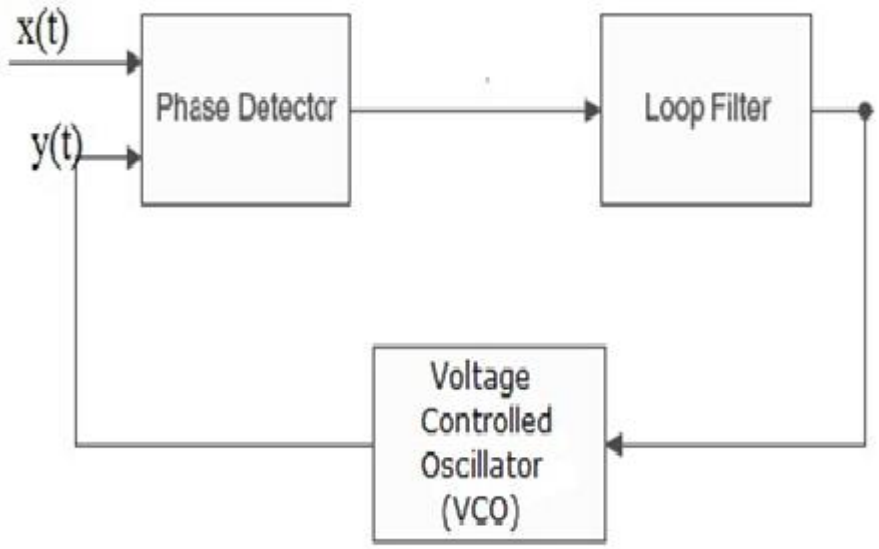


figure 1-2 Block diagram of PLL

Figure 1-2 illustrates the basic architecture of the phase locked loop. The generated signal from phase detector is a function of the difference between the phases of two input signal then it filtered and the dc component of the error signal is applied to the voltage controlled oscillator (VCO). The voltage controlled oscillator (VCO) output signal fed back to the phase detector. The VCO input signal force the VCO to change frequency in direction that reduce the difference between the input frequency and VCO output frequency. If the two frequencies are approximately close, The PLL feedback mechanism forces the

two inputs frequencies of phase detector are equal, and the VCO is “Locked” with incoming frequency[Kaveh, 2011&Rezavi, 2001]. Usually the filter that used in PLL is first order or second order and the RC Low Pass Filter is simplest type of filter.

while there are several type of the phase detector and the most common used is[David, 1997]:

1- Exclusive OR gate
2- Analog Multiplier
3- Combinational digital circuits such as D Flip Flop.

1.1. Previous researches

There are many researchers who research in field of frequency generation by using Sigma-Delta Phase Locked Loop Modulator circuit, They designed, analyzed, simulated and developed this circuit furthermore some of them implemented it practically by using different techniques, A brief explanation of some of these efforts .

In 2002, Soo Hwan Kim with a group of researchers designed fractional Phase Locked Loop frequency synthiser and implemented it by using CMOS techniqe by adopting a frequency divider and a simplified 3-stage MASH Sigma-Delta modulator. He use the simple type of frequency divider to reduce the complexity of the circuit and to reduce the power consumption. The result of this design shows a rapid switching time, The measured VCO phase noise is good as (122.99 dBc/Hz at a 7.5-MHz offset) while The measured fractional spur level is -101.6 dBc [Soo,2002].

In 2002, TaoufikBourdi ,AssaadBorjak and Izzet Kale designed fractional Phase Locked Loop frequency synthiser to get high Frequency Resolution, fast Switching Time and low level Phase Noise in the frequency synthiser output spectrum. They use Segma-Delta modulater to eleminatSpurs Noise that cuased by fractional division.they use RFCMOS techniq to implement this design at 1800 MHz . The result show an improvement in the noise level by 10 dB, while the Switching Time was (25μsec)[Bourdi, 2002].

In 2004, Mucahitkozak and EbyG.friedman designed fractional Phase Locked Loop frequency synthesizer at 905 MHz and analyzed it by using 3-stage MASH Sigma-Delta modulator by adoption a quick way for the design and analysis using MATLAB and CMEX^TM. They use 3rd order filter at bandwidth of (199.18 KHz). The theoretical result show that the switching time was very small and there is no fractional Spurs Noise while, the refranceSpurs Noise still exsist[Mücahit, 2004].

In 2005, Kenichi Tajima ,Ryoji Hayashi and Tadashi Takagi suggest new method to reduce or remove Spurs noise that caused from 2-stage MASH Sigma-Delta modulator techniq of Phase Locked Loop frequency synthesizer by using analog phase detector . This proposed design presented an improvement to the amount of voltage difference or the difference between the two inputs of phase detector. The voltage difference was controlled by using Presetscheme circuit by adding a voltage called (Preset voltage) to the voltage controlled oscillator (VCO). When programming Preset voltage we can get the specific frequency . The result show an improvement in the noise level by 15 dB[Kenichi, 2005].

In 2005, VolodymyrKratyak and Pavan Kuma Hanumoln present a new method to reduce Spurs in the output spectrum of Phase Locked Loop frequency synthesizer by using new technique in loop filter design called (discrete time comb filter) where this filter make Spurs reduction in the output spectrum of Phase Locked Loop frequency synthesizer. This filter make notches at the frequency of fractionalSpurs. Through the selection of notches frequency depend on the position of Spurs frequency in the output spectrum. The most important features of this new technique are the low power and low level Spurs noise. This research pointed out that the most important determinants of this filter that it is not possible to use this filter if the Spurs occur within the frequency bandwidth[Volodymyr, 2005].

In 2006, ErkanBilhan and Feng Ying suggest new method to reduce fractional Spurs noise of fractional Phase Locked Loop frequency synthesizer, This proposed technique does not use the traditional method of changing the value of the division between (N and N+1) But it use multiple phases of the oscillating frequency separated by a specific distance then processed using resonant oscillator. It is insert these multiple phases to the control circuitry to determine

the appropriate phase to generate the desired frequency. The implementation of this proposed design at a practical frequency 250 MHz by designing Oscillator (VCO) in order to generate the eight phases. Theoretical results show that the proposed design does not contain any fractional Spurs in the spectrum of the output signal[Erkan, 2006].

In 2006, Hongyu Wang and Paul Bernnan design Phase Locked Loop frequency synthesizer by using different type of Sigma-Delta modulator. MATLAB software was used to simulate the proposed design. And FPGA was used to implement the proposed design at GSM and DCS frequencies. The results were identical to what is required in wireless systems applications (GSM and DCS) in term of noise level and Spurs noise and switching time[Hongyu, 2006].

In 2008, H. Ziboon and H. M. Azawi design and simulation of proposed fractional Phase Locked Loop frequency synthesizer which can be used for WiMAX system by using Sigma-Delta modulator to reduce settling time, Spurs level and phase noise. They use Sample and Hold circuit to reduce Reference Spurs. and they use MATLAB and C++ simulator language to simulate the proposed design . The results were identical to that required for WIMAX systems due to settling time, Spurs level and phase noise[H. T., 2008].

In 2010, N. Fatahi and H. Nabovati design Phase Locked Loop frequency synthesizer by using 3rd stage Sigma-Delta modulator, The goal of this research is to get lower Spurs level and phase noise. The result shows the in-band phase noise of -95 dBc/Hz at 10-kHz offset with a spur of less than -96 dBc is achieved with a reference frequency of 8 MHz and a loop bandwidth of 40 kHz [Chun-Pang, 2011].

Finally in 2011, Chan-Pang and Sheng-Sian design Phase Locked Loop frequency synthesizer at output frequency of 3.9 GHz and loop bandwidth of 300 kHz .and simulate it by using new technique to reduce fractional Spurs and quantization noise. They use several stages of the delay units between reference input signal and the Phase Detector to get several phases of the input signal. Where the compensation control unit have been used to get the desired phase signal. They use 2nd and 3rd stage Sigma-Delta modulator. They implement this design by using CMOS technology . The theoretical results show that there is an

improvement in noise level for the quantization process and the level of fractional Spurs noise by 13db [Hadi, 2011].

1.2 Purpose of the research

1- Study the work of the Fractional-N Phase Locked Loop frequency synthesizer circuit in modern wireless communications devices, TVs and other devices.
2- Design Fractional-N Phase Locked Loop frequency synthesizer circuit and simulate it by using (ADS) design program and MATLAB.
3- Using Sigma-Delta modulator to reduce the fractional Spurs from the frequency synthesizer.
4- Improve the performance of the frequency synthesizer work (Phase noise, Spurs noise and Switching time) by design loop filter able to remove Spurs noise, and reduce the Switching time and phase noise level.

1.3 The research Contents

This research will included five chapters distributed as follows:
The first chapter included an introduction and types of frequency synthesizer and review of previous researches and research and the Purpose of the Study. Chapter II will address a detailed study of the Fractional-N Phase Locked Loop frequency synthesizer, frequency synthesizer characteristics, the main components of the Phase Locked Loop circuit and the main problems in the work of the frequency synthesizer and the techniques used to solve it. Chapter III will address the design of loop filter and its main equation as well as design different stages of Sigma-Delta modulator . This chapter also address the circuits used in the process of Fractional-N frequency synthesizer design. Chapter IV deals with the results of simulations and discussed various designs of Fractional-N frequency synthesizer using Sigma-Delta modulator as well as make comparisons between these results. Finally Chapter V will include conclusions that have been reached through this study as well as a number of proposed future researches in this area.

2. Phase Locked Loop Frequency Synthesizer Using Sigma-Delta Modulator

Phase Locked Loop Frequency Synthesizer is widely used in wireless and radio communication systems for its ability to generate high frequency signals and low power. Phase Locked Loop is a close feedback system. Where the feedback signal used to lock signal output frequency and phase at a frequency and phase input signal. Phase Locked Loop circuit consist of three major components is 1: Voltage control oscillator (VCO) , 2: Loop filter, 3: Phase detector. When Phase Locked Loop circuit contain frequency divider then it called Phase Locked Loop Frequency Synthesizer as shown in figure 2-1. When the frequency of source signal is fixed then the frequency of the output signal of the oscillator will change as the frequency divider (N) is change[Ranganathan, 2003&Kaveh, 2011].

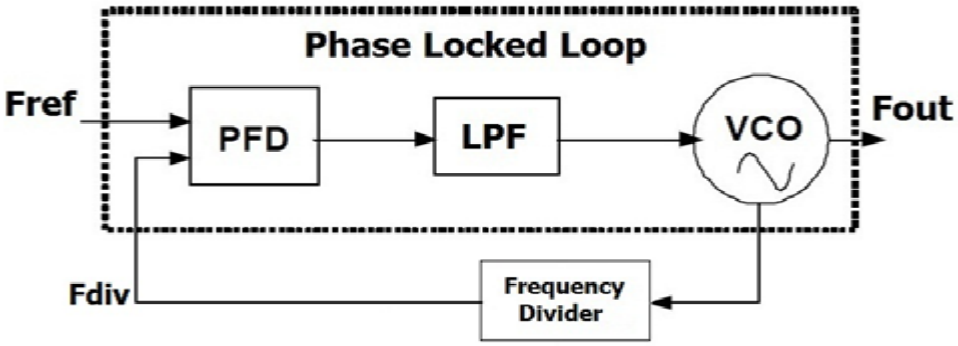


figure 2-1 Phase Locked Loop Frequency Synthesizer

2.1 Frequency Synthesizer Properties

The modern wireless communication systems standards set several conditions in the Frequency Synthesizer design. Here is the most important factors that characterize the performance of the frequency Synthesizer of each others

2.1.1 Channel spacing

This factor determine the separation distance between the channels, for example if the Channel Spacing is 500 KHz that mean the frequency of the first

channel is (fc) and the frequency of the second channel is (fc+500 KHz). The channel spacing varies depending on the application used the Frequency Synthesizer, that it is the separation distance between the channels 200 KHz for GSM system , while it is 1 MHz for Bluetooth system.

2.1.2 Settling Time

Is the time that taken by the oscillator output signal to reach a steady state during the transition from the channel to the other and it is depend on the bandwidth of the filter where the increasing in the bandwidth of the filter will improve the Settling time [Hadi, 2011].

2.1.3Phase Noise

Ideal Voltage Control Oscillator (VCO) generate frequent signal without any noise at frequency (ω_c) according to the following equation[Rezavi, 2011]:

$X(t) = A \cos(\omega_c t)$ (1-2)

In fact, the signal generated from all type of oscillators contain noise called (Phase noise) to represent this noise the equation (1-2) will be :

$X(t) = A \cos[\omega_c t + \emptyset_n(t)]$ (2-2)

Where $\emptyset_n(t)$ represent random phase noise. The existence of the Phase noise in the (VCO) will change the zero-crossing points of the generated signal as it shown in figure (2-2)

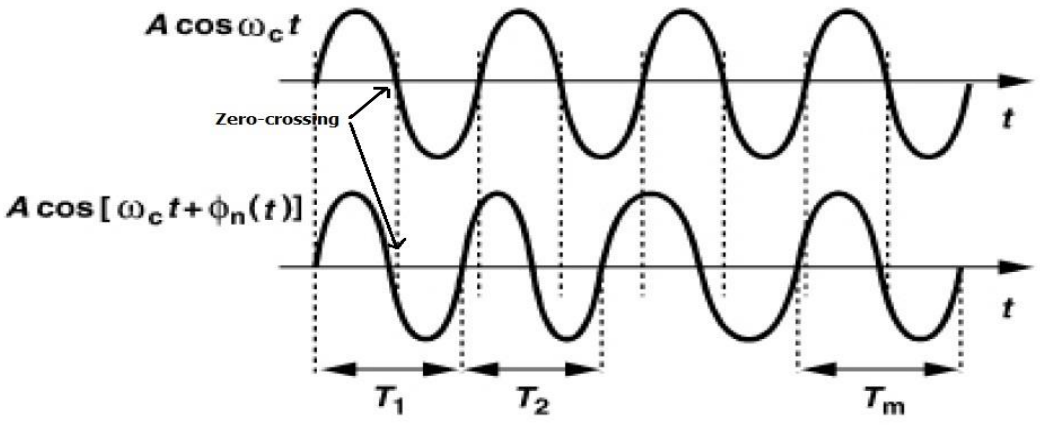


Fig (2-2) : The effect of phase noise in VCO signal

The signal spectrum of ideal VCO in the form of a single pulse at frequency (ω_c) as shown in figure (2-3 a). While the signal spectrum of non ideal VCO contain random changes surrounding the generated signal at frequency (ω_c) as shown in figure (2-3 b).

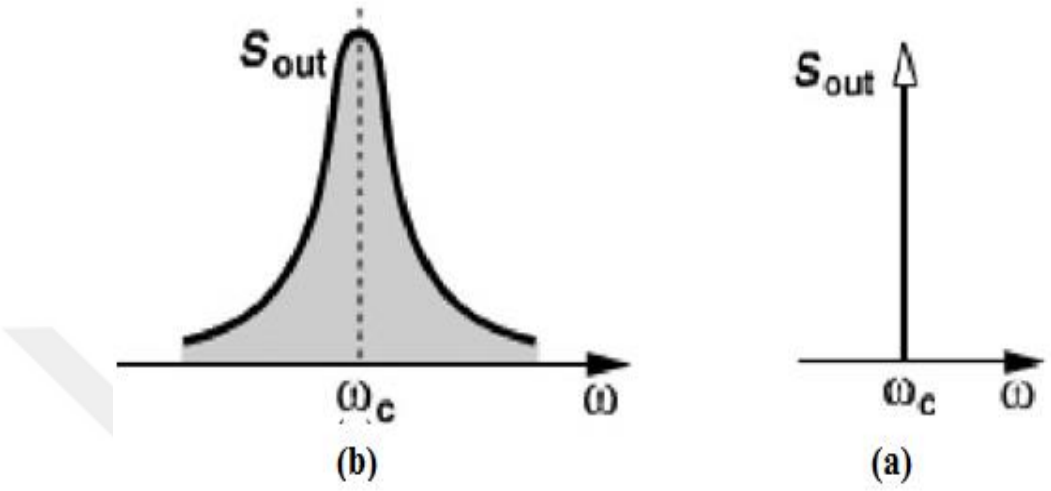
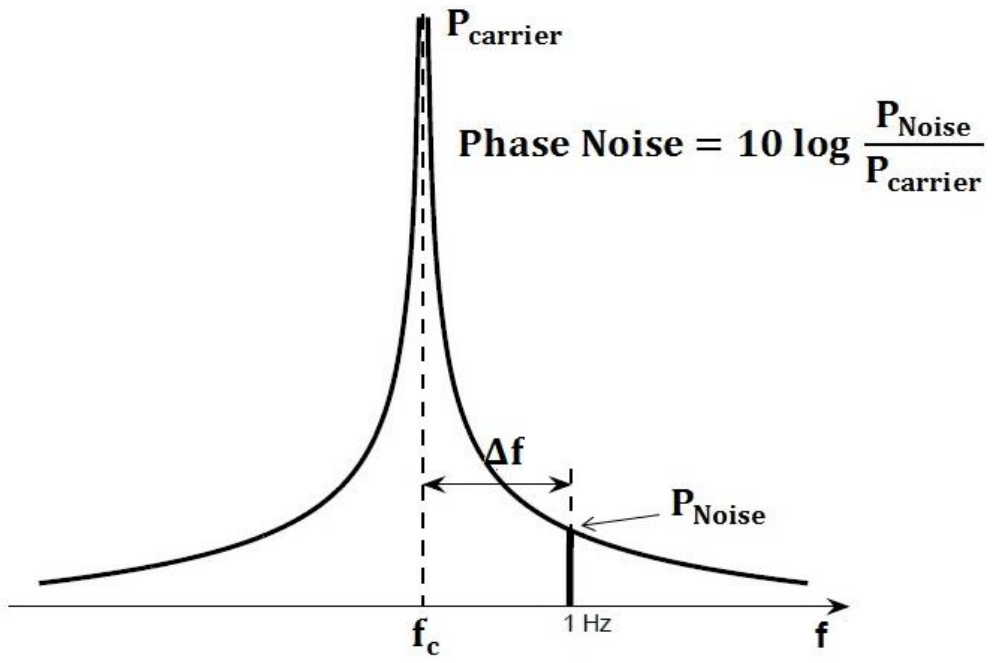


Fig (2-3) :(a)Ideal VCO spectrum (b)Non ideal VCO spectrum

Phase Noise define as the ratio between the power of the noise signal (in the domain of bandwidth (1Hz) at frequency offset equal (Δf) from the frequency of the generated signal) to the power of the signal at frequency (fc) and it measured by (dBc/Hz) as in the following equation [Rezavi, 2011&Hongyu, 2009]:

$$\text{Phase Noise} = 10 \log \frac{P_{Noise}(\text{at } f_c+\Delta f \text{ in 1 Hz bandwidth})}{P_{carrier}(\text{at } f_c)} \text{dBc/Hz} \qquad (2\text{-}3)$$

Figure (2-4) show the Phase noise in the output spectrum of VCO and how to measure this noise.



Fig(2-4): the Phase noise in VCO output spectrum

2.1.4 Spurs Noise

It is unwanted and non-harmonically related signals appear at the output spectrum of VCO . it defined as the ratio of the spur noise power (at offset equal (Δf) from the frequency of the oscillator (fc)) to the power (at frequency equal (fc)) and it is usually expressed in terms of dBc as in the following equation [Ranganathan, 2003: Keliu, 2001 & Cicero, 2002]:

$$\text{Spurs Noise} = 10 \log \frac{P_{spur}}{P_{carrier}} \quad \text{dBc} \qquad (2\text{-}4)$$

Figure (2-5) show the Spurs noise on the both side of the output signal of VCO. It should be noted that the Spurs noise inversely proportional to the input signal frequency [Wong, 2002].

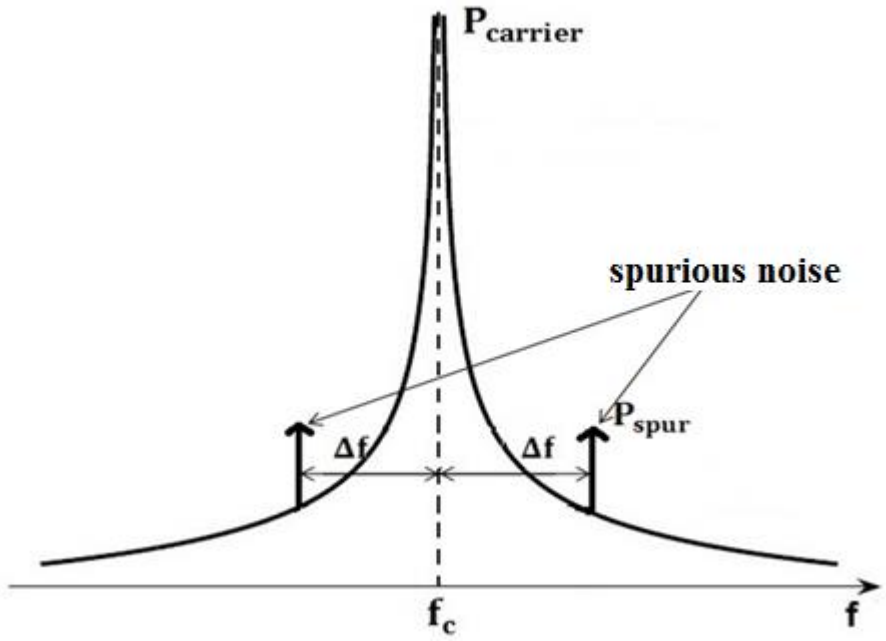


Fig (2-5) Spurs noise in VCO output signal

Spurs noise divided into Fractional Spurs Noise and Reference Spurs Noise. Fractional Spurs Noise appear in fractional phase lock loop which use fractional divider with fractional value as will be explained later , While Reference Spurs Noise appear when offsets frequency equal to the frequency of the input signal (Fref)[Kevin, 2008].

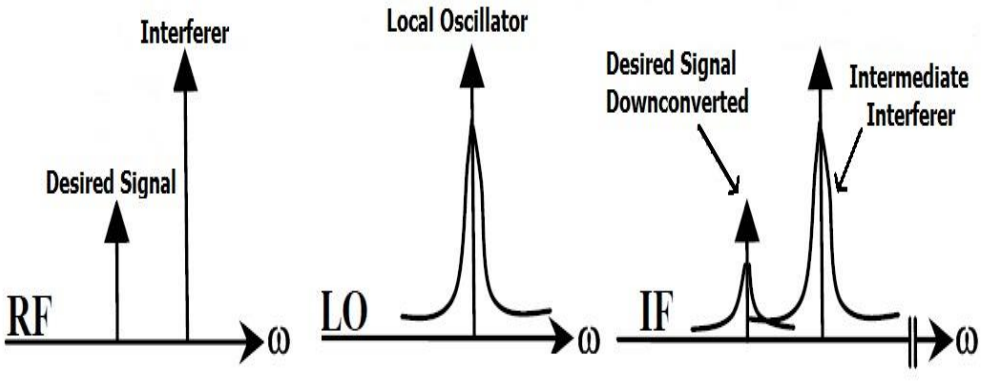
2.2. The Effect of the Phase Noise and Spurs Noise on the Transmitters and Receivers

The Phase Noise and Spurs Noise in the output signal spectrum distort signal transmitted or received in the transmitter and receiver devices. In the following a detailed explanation of these effects:

2.2.1. Effect of the phase noise

Figure (2-6) shows the effect of the phase noise in the output spectrum of VCO in the received signal. The received signal contain the transmitted signal in addition to interfere signal which have power may be significant compared with information transmitted signal. When the received signal converted to

intermediate signal by using local oscillator (LO) contained phase noise the intermediate interferer distort desired signal downconverted [Saurabh, 2002].



Fig(2-6) effect of the phase noise in the received signal

2.2.2. Effect of the Spurs noise

When the output spectrum of frequencysynthezer contained sideband Spurs noise. This Spurs noise distort the received signal at receiver side. Figure (2-7) shows the effect of Spurs noise on information received signal at the receiver side [Rezavi, 1996]. The spectrum of frequency synthezer contained carrier signal at (ωc) frequency and sideband Spurs noise at (ωs) frequency .while the received signal contain from transmitted information signal in addition to interfere signal. Figure (2-7) shows that after the received signal converted to intermediate signal a noise signal will appear called (intermediate interferer) at frequency equal ($\omega_{\mathrm{int}} - \omega_{\mathrm{S}}$) . if the frequency of the intermediate interferer equal to the frequency of intermediate information carrier signal that mean ($\omega_{\mathrm{IF}} = \omega_{\mathrm{int}} - \omega_{\mathrm{S}}$) this will lead to the intermediate interferer be inside the intermediate information carrier therefore the information carrier signal will distort [Rezavi, 1996].

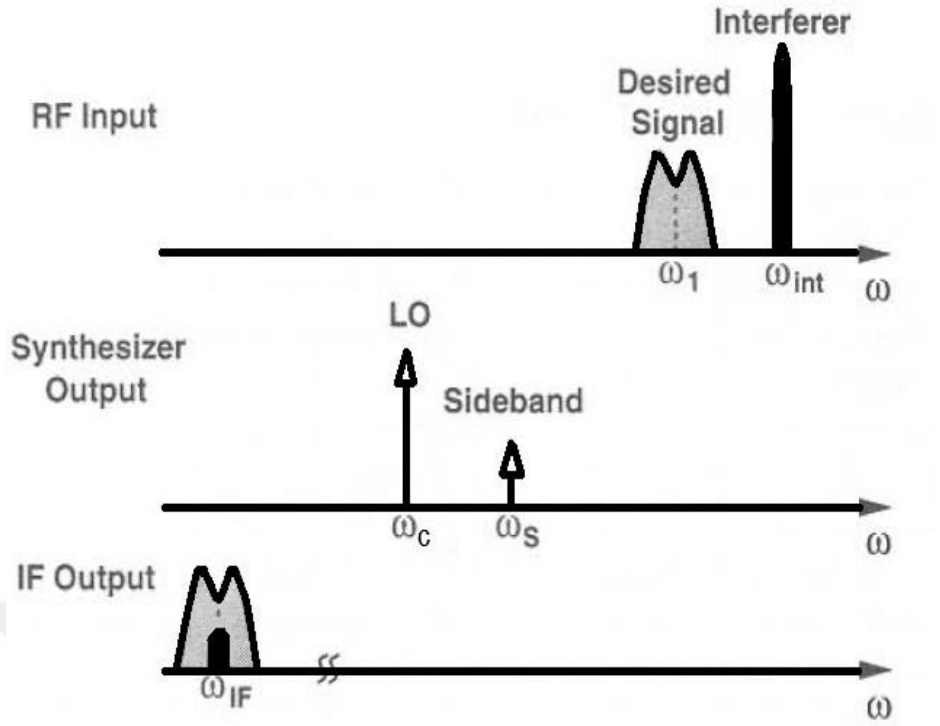


Fig (2-7) the effect of Spurs noise on the received signal [Rezavi, 1996]

2.3The main component of Phase Locked Loop Frequency SynthesizerReceivers

Nowadays the Phase Locked Loop Frequency Synthesizer contain from five component :

2.3.1. Phase-Frequency Detector

It use to compare between the phase and the frequency for reference signal with the phase and frequency for the divider signal [Curtis, 1999] figure(2-8) show the operation of the Phase-Frequency Detector . the working principle of the Phase-Frequency Detector as follow:

1) When (Fref) > (Fdiv) : The rising edge of (Fref) cause rising edge at the output UP and still like that until the rising edge of (Fdiv) became then the output UP turn to falling edge. In this case the output Down not change .

2) When (Fref) > (Fdiv) : The rising edge of (Fdiv) cause rising edge at the output Down and still like that until the rising edge of (Fref) became then the output Down turn to falling edge. In this case the output UP not change .
3) When (Fref) = (Fdiv) and divider signal lagging reference signal: it will be the same of point one where The rising edge of (Fref) cause rising edge at the output UP and still like that until the rising edge of (Fdiv) became then the output UP turn to falling edge. In this case the output Down not change .
4) When (Fref) = (Fdiv) and reference signal lagging divider signal: it will be the same of point two where : The rising edge of (Fdiv) cause rising edge at the output Down and still like that until the rising edge of (Fref) became then the output Down turn to falling edge. In this case the output UP not change .

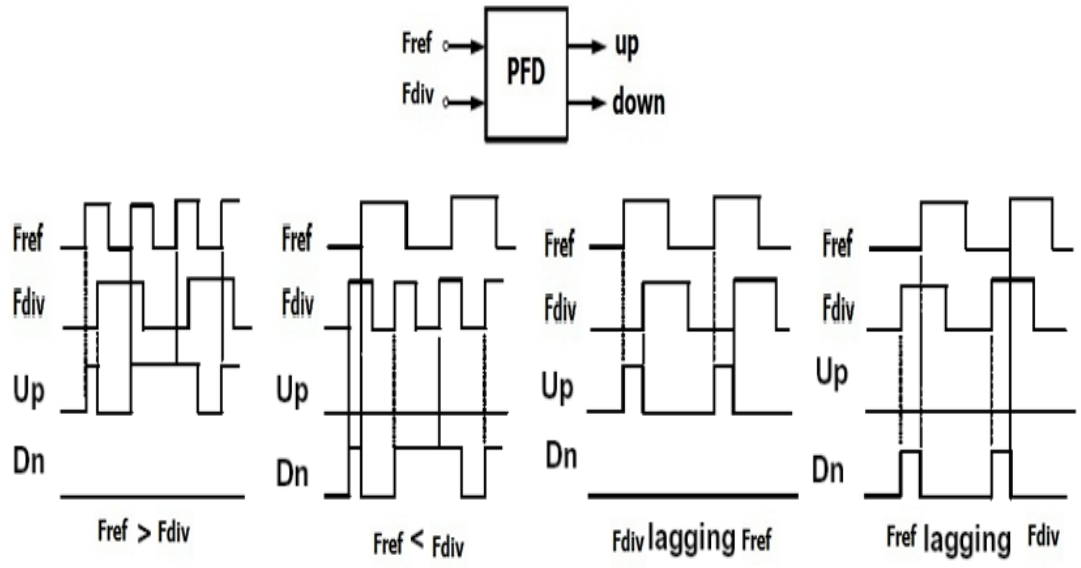


Fig (2-8) The operation of the Phase-Frequency Detector

figure (2-9) show the architectures of the Phase-Frequency Detector show that it consist of two D flip-flop with one AND gate .the D input of the two flip flop connected to VDD and the clock of one of them connected to (Fref) and the other clock connected to (Fdiv) that mean the output of one of the D flip-flop depend on (Fref) and the other depend on (Fdiv). when (Fref) or (Fdiv) change

to high, this flip-flop will charged and change its output to high. The used of AND gate is to prevent both flip-flop to be high at the same time. One of the input of AND gate connected to the output UP of one flip-flop and the other connected to the output Down of the other flip-flop and the output of the AND gate connected to reset of the both flip-flop thus when the (UP and Down) high the output of AND gate will be high and reset both flip-flop and avoid this condition. When The rising edge of (Fref) cause the output UP will be high and still high till The rising edge of (Fdiv) became that made the AND gate reset the flip-flop. The output (UP and Down) control the output current from Charge Pump .where the output UP used to increase the frequency of VCO while the output Down used to decrease the frequency of the VCO.

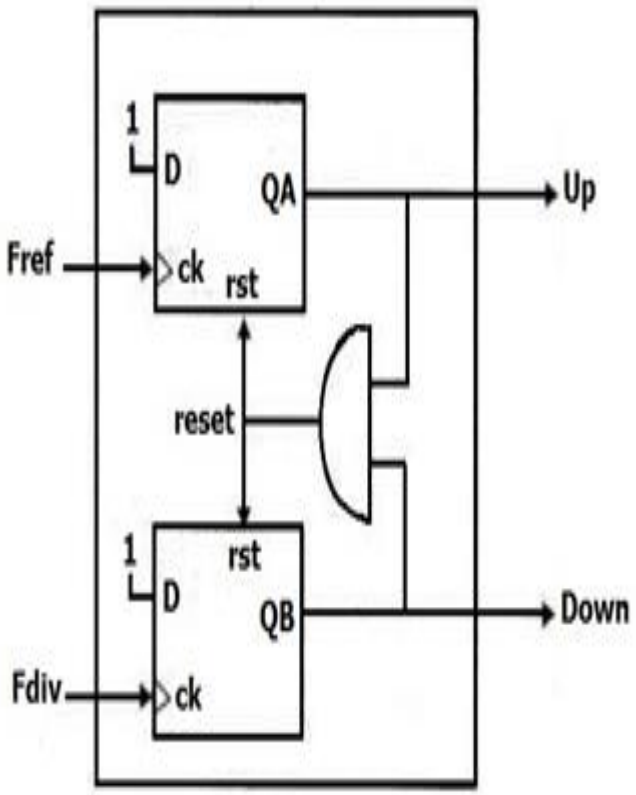


Fig (2-9) architectures of the Phase-Frequency Detector

2.3.2. Charge Pump (CP)

Charge pump is a three position electronic switch which is controlled by the three states of PFD. Where when the output UP of the PFD is logic "1" it

delivers a pump voltage ±VP to the loop filter, and when the output Down of the PFD is logic “1” it delivers a pump current ±IP to the loop filter.When both UP and Down of PFD are logic “0”, the switch is open, thus isolating the loop filter from the charge pump and PFD. figure (2-10) show the architectures charge pump.

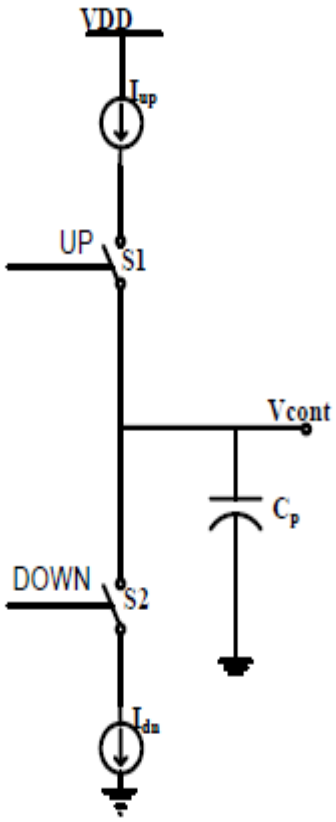


fig (2-10) the architectures charge pump

where the two current source (Iup and Idn) are equal . the outputs of PFD UP and Down are given to the UP and DOWN inputs of charge pump (CP) respectively.

Figure (2-11) shows the charge pump accompanied with Phase Frequency detector and loop filter.

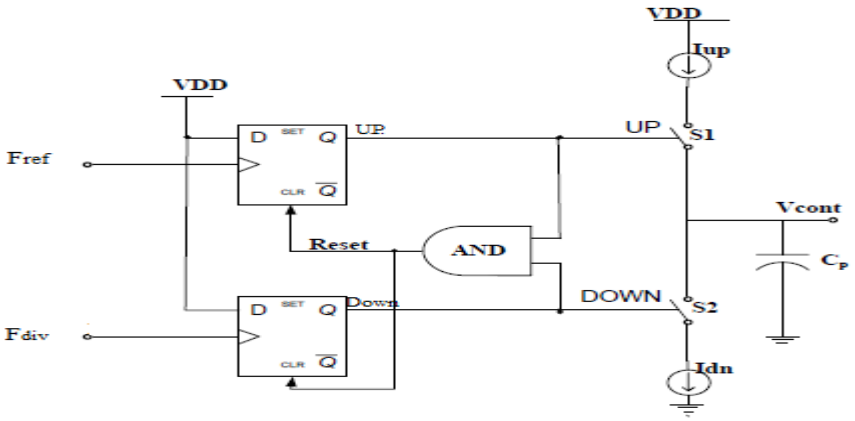


Fig (2-11) PFD-CP-Loop Filter Combination

If the PFD outputs UP=Down=0, then S1 and S2 are off and Vout (or Vcont) remains constant. If the PFD outputs UP is high and the PFD outputs Down is low, then Iup (UP current) charges Cp. Conversely if the PFD outputs UP is low and Down is high, then Idn (DOWN current) discharges Cp. Hence, if suppose, Fref leads Fdiv, then UP continues to produce pulses and Vcont rises steadily. Figure (2-12) shows the response of PFD-CP combination.

Fig (2-12) the response of PFD-CP combination.

2.3.3. Loop Filter

Loop filter it's low pass filter ,It's one of the necessary requirements in most applications to reduce noise at high frequency[Brian, 2008].It is noteworthy that we cannot connect directly the Charge Pump output signal to the Voltage Control Oscillator (VCO) for two reasons:

1. The output of the Charge Pump in current form and cannot be used to control the Voltage Control Oscillator (VCO).
2. The output of the Charge Pump contain harmonics that affect to the output spectrum of the Voltage Control Oscillator (VCO).

Therefore, the Loop filter is used to convert the Charge Pump output current to the voltage to control the Voltage Control Oscillator (VCO), As well as removing the harmonics in the output of the Charge Pump[Zhiming, 2007].There are two types of Loop filter: Active filters and Passive filter ,An active filter is a type of analog electronic filter that uses active components such as an amplifier As in Figure (2-13b) .while passive filter consist of resistors and capacitors As in Figure (2-13a) Some passive filter contain inductors in addition to the resistors and capacitors . Nowadays inductors not used in the design of filters; because they generate high noise compared resistors and capacitors, as well as they occupy a large volume at practically implemented[Michael, 2005]

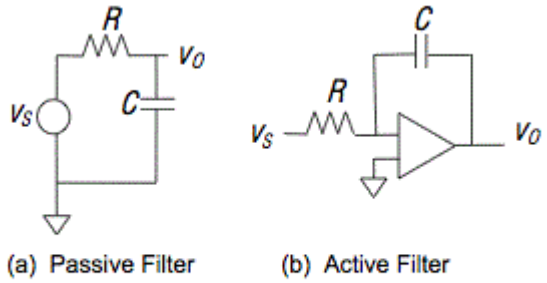


Fig. (2-13) Active and Passive Loop-Filters

The avoidance of use active filter due to the high noise resulting from the use of the Amplifiers circuit, Increase the complexity of the filter, higher cost , reduce the stability of the system , for that we used Passive Filters[Curtis, 1999 & Brian, 2008].

The frequency synthizer that use first order loop filter contain burrs in the output spectrum due to the ripple in the output voltage of the loop filter. For that second order or higher loop filter are used to get output spectrum without burrs , but increase the complexity of the filter[Brian, 2008 &Alaa, 2002]. The bandwidth of the loop filter determined the bandwidth of the frequency synthizer.

2.3.4. Voltage Controlled Oscillator

Voltage controlled oscillator (VCO) is a type of oscillator where the frequency of the output oscillations can be varied by varying the amplitude of an input voltage signal (output of the loop filter). The relation between output frequency and input voltage can be represent in following equation [Jack, 1985]:

$F_{out} = F_{FR} + dF = F_{FR} + K_{VCO}.V_{tune}$ (2-5)

Where K_{VCO} represent VCO gain and is given by

$K_{VCO} = 2\pi \frac{fmax - fmin}{Vmax - Vmin}$ (2-6)

V_{tune} represent the input voltage signal

while F_{FR} represent Free Running Frequency.

Figure (2-14) show the Transfer function of the VCO it is linear.

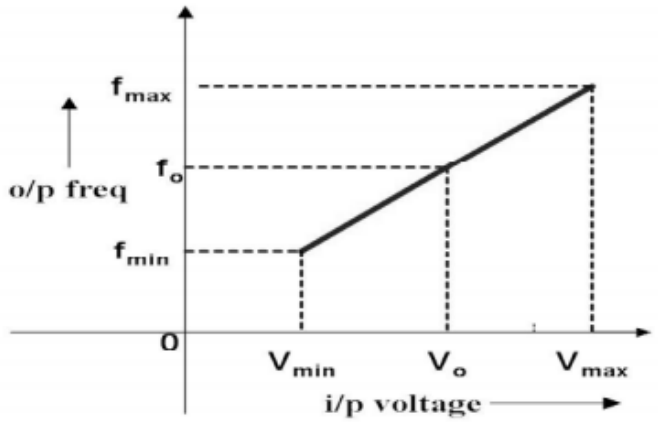


Fig (2-14) Transfer function of the VCO

Equation (2-6) explain the relation between the output phase and frequency of the VCO

$\phi_{vco}(t) = \int_0^t dF(t)dt = \int_0^t K_{VCO}.dV(t)dt = \int_0^t K_{VCO}.V_{tune}(t)dt$

$= K_{VCO} \int_0^t .V_{tune}(t)dt$ (2-7)

$\phi_{vco}(t)$ represent the output phase while $dF(t)$ represent the frequency change when $V_{tune}(t)$ is changed.

By applying Laplace transformer to equation (2-6) we can get

$\frac{\phi_{vco(s)}}{V_{tune}(s)} = \frac{K_{VCO}}{S}$ (2-8)

That mean that the VCO add pole at the origin. And this additional pole is necessary to convert the oscillator output signal from frequency to phase to compared with the input signal phase.

2.3.5.Frequency Divider

The frequency divider of the most important components of Phase locked Loop frequency syntheser .It is used to convert the VCO output signal of high-frequency to low frequency signal to be compared with the input signal using the phase frequency detector.

The relation between the VCO output frequency and the Divider output frequency can expressed by following equation

$$F_{div} = \frac{F_{out}}{N} \quad (2\text{-}9)$$

Where N represent division ratio.

Frequency divider divided into:

- Integer frequency divider :In the form of a digital counter
- Fractional frequency divider : It divided into
    - Dual-Modulus: This type of dividers used to change the division ratio between the two integer numbers from N_{int} to N_{int}+1. This type of dividers controlled by Accumulator as will be explained later. Figure (2-15 a) show the internal structure of the frequency divider (÷2) of D flip-flop. While Figure (2-15 b) show the internal structure of the frequency divider (÷3) of D flip-flop. Figure (2-15 c) show the internal structure of the frequency divider ($\div\frac{2}{3}$) of D flip-flop it consist of (÷2) frequency divider and (÷3) frequency divider, if the mod value equal zero then the division ratio equal 3, while if the mod value equal one then the division ratio equal 2[Ranganathan, 2003]

Multi Modulus: This type of dividers used to change the division ratio (N) among more than two values, This type of dividers controlled by Sigma Delta Modulator (∑Δ Modulator). This type of dividers consist of a series from Dual-Modulus dividers as in Figure (2-16)

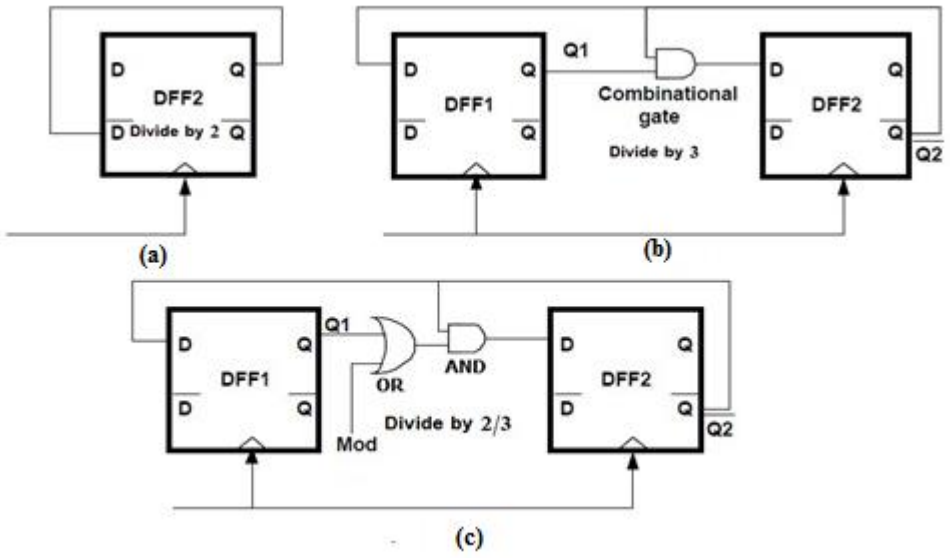


Fig (2-15)(a) frequency divider (÷2) (b) frequency divider (÷3)

(c) frequency divider ($\div\frac{2}{3}$)

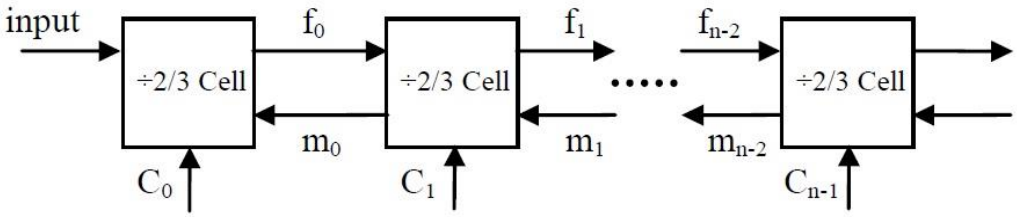


Fig (2-16) Multi-Modulus frequency divider

2.4. The working principle of Phase Locked Loop Frequency Synthesizer

Phase Locked Loop Frequency Synthesizer consist of five component : Phase-Frequency Detector (PFD),Charge Pump (CP),Loop Filter,Voltage Controlled Oscillator (VCO) and Frequency Divider as in Figure(2-17).

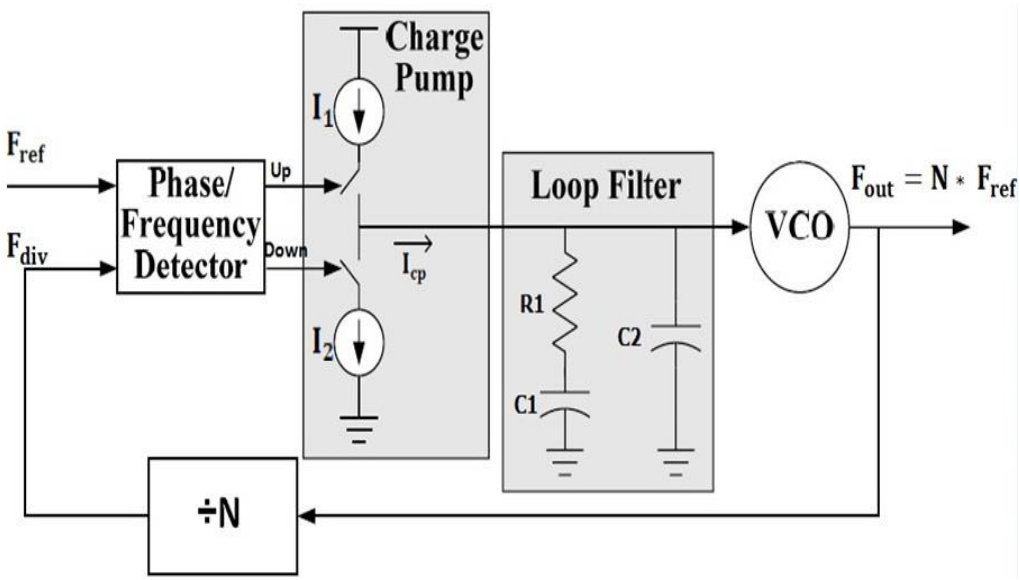


Fig (2-17)Phase Locked Loop Frequency Synthesizer

The frequency and the phase of the reference signal compared with the frequency and the phase of Frequency Divider output signal by using Phase-Frequency Detector (PFD) which generate pulses signal it's bandwidth depend on the phase difference between the reference signal and the Frequency Divider output signal, this pulses signal control to increase or decrease Charge Pump (CP) output signal. The Charge Pump (CP) output current converted to voltage by using Loop Filter, the Loop Filter output voltage directly proportional to the phase difference between the reference signal and the Frequency Divider output signal. Loop Filter remove high-frequency component form Charge Pump (CP) output signal and its output voltage control the Voltage Controlled Oscillator (VCO) to obtain the desired frequency[Erkan, 2006: Kevin, 2010 & Prakash, 2009]. If the phase difference is variable with time, this means that the frequency lock process has not occur yet However, if the phase difference constant with time, it means that the frequency lock process occurs[Kaveh, 2011].

2.5Type of Phase Locked Loop Frequency Synthesizer

Phase Locked Loop Frequency Synthesizer divided into two types: Integer-N Phase Locked Loop Frequency Synthesizer and Fractional-N Phase Locked Loop Frequency Synthesizer.

2.5.1 Integer-N Phase Locked Loop Frequency Synthesizer

The division ratio of the Frequency Divider that used in Integer-N Phase Locked Loop Frequency Synthesizer is integer (N) as in Figure(2-17) the output frequency for such Frequency Synthesizer can be describe by the following equation: xd2q

$$F_{out} = N.F_{ref} \quad (2\text{-}10)$$

The channel spacing in Integer-N Phase Locked Loop Frequency Synthesizer equal to the reference frequency (F_{ref}) . Reducing the reference frequency (F_{ref}) is the only solution to get frequency channel separated by narrow channel spacing but this reduction cause many problem [Richard, 2007; Hongyu,2009; Golsa,2009; Fatahi, 2010].

1- For the stability the bandwidth must be much less than the reference frequency ($0.1*F_{ref} >> F_{B.W}$) but reducing the reference frequency (F_{ref}) mean reducing the bandwidth and that cause increasing the time to reach the stady state value and This undesirable in Phase Locked Loop Frequency Synthesizer
2- It will lead to increase the division ratio (N) and this cause increasing the Phase noise by 20log(N).
3- Since the Spurs Noise depend on the reference frequency (F_{ref}) for that the reducing the reference frequency (F_{ref}) mean that the Spurs Noise will be inside or near the bandwidth.

These problems in Integer-N Phase Locked Loop Frequency Synthesizer determined it use in These problems existing in the stained-phase circuits that use the correct frequency dividers determine who uses the radio frequency that you need a narrow frequency channels reciprocating distance between

applications and a few transition time between the frequency channels that need frequency channel separated by narrow channel spacing

2.5.2 Fractional-N Phase Locked Loop Frequency Synthesizer

The most important advantages of this technique is the possibility to get frequency channel separated by narrow channel spacing without going to reduce the reference frequency (F_{ref}). This technique provides low Phase noise and the Spurs Noise will not be inside or near the bandwidth and also provides wide bandwidth.

Fractional division ratio generated by using Dual-Modulus Frequency divider .where the frequency divider controlled by the Accumulator. The Carry-out signal used to change the division ratio from N_{int} to N_{int}+1 to get Fractional division ratio ($N_{int} + \propto$).where N_{int} represent the integer part of the division ratio and ∝represent the fractional part of the division ratio (1>∝>0) as in Figure(2-18).

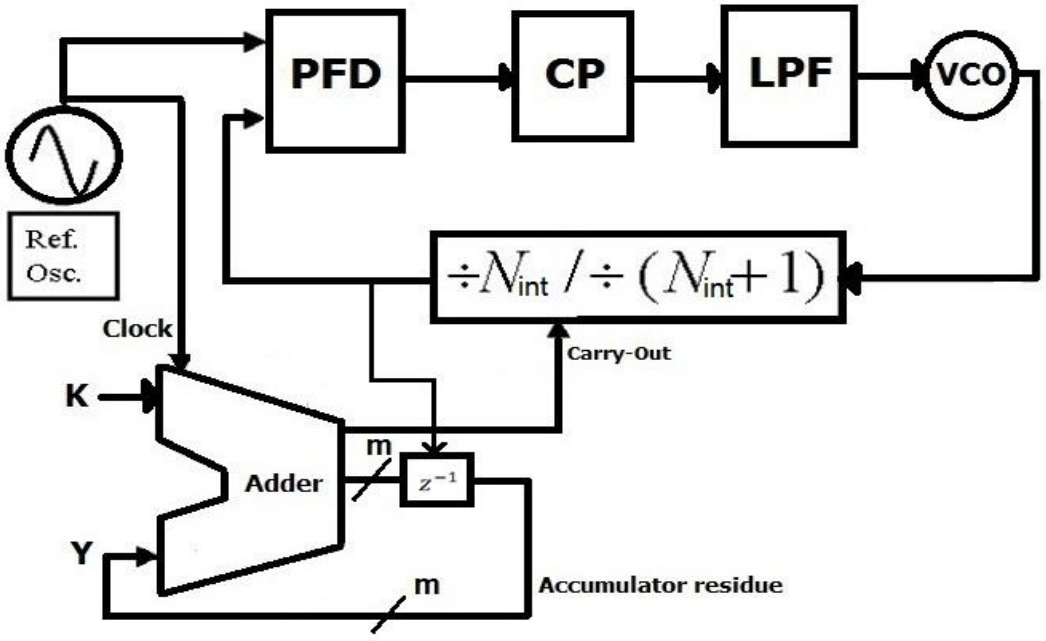


Fig (2-18)Fractional-N Phase Locked Loop Frequency Synthesizer

The digital input (K) is applied to the Accumulator. The Accumulator collects (K) value at each reference frequency (F_{ref}) period until the Overflow occurs then the carry-out changed from (0) to (1) and that will changed the division

ratio from N_{int} to N_{int}+1. Where the division ratio equal N_{int}at 2^m-K times. While it equal N_{int}+1 at K times . as the following equation

$$N_{frac} = \frac{(2^m - K).N_{int} + K.(N_{int}+1)}{2^m} = N_{int} + \frac{K}{2^m} == N_{int} + \propto \qquad (2\text{-}11)$$

Where 2^mrepresent Accumulator output samples. Figure (2-19) show the timeline function for Fractional-N Phase Locked Loop Frequency Synthesizer function

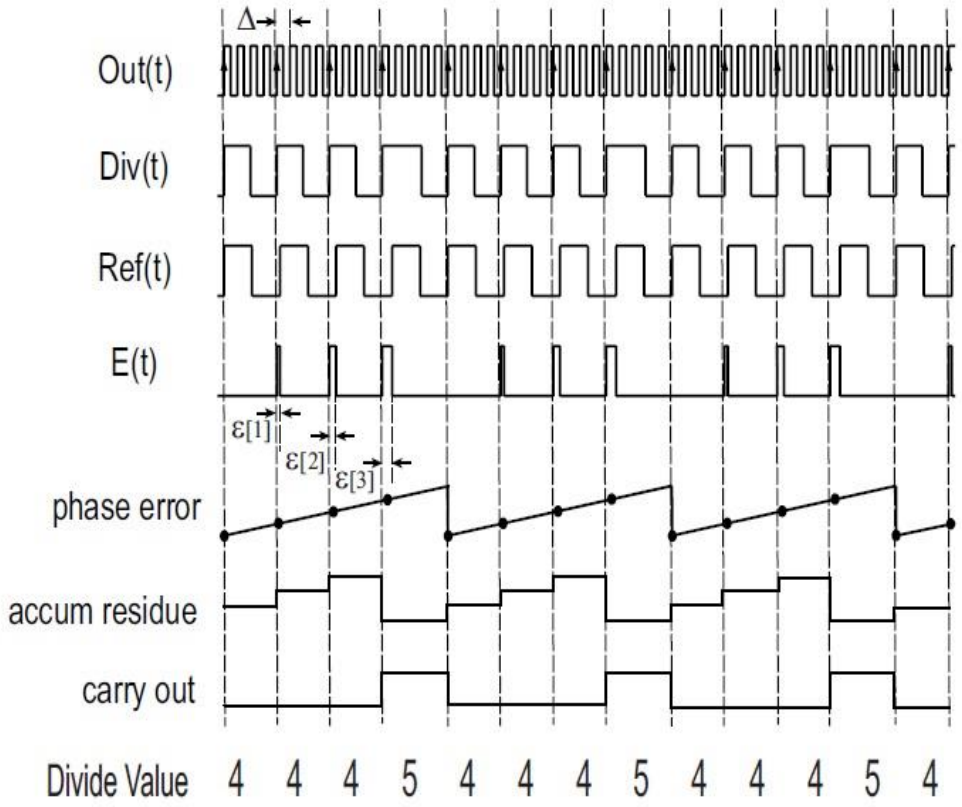


Fig (2-19) the timeline function for Fractional-N Phase Locked Loop Frequency Synthesizer function

It is clear from the figure above that the integer value N equal 4 while the fractional value ∝ equal 0.25 and that is mean that the carry-out signal will be enable when the reference frequency (F_{ref}) complete the fourth period and that will change the division ratio Repeatedly in the sequence [4,4,4,5]. The phase difference increase gradually during the adding process in the accumulator .when the overflow happen the phase difference become zero[Hongyu, 2009 & Bram, 2003]. As a result of continuous change made in the division ratio from N_{int} to N_{int}+1 the phase difference oscillatory variable by frequency ($\propto F_{ref}$) and that produce Spurs Noise in the output spectrum of the frequency synthesizer called Fractional Spurs Noise.

2.6The techniques used to remove Fractional Spurs Noise

There are several techniques used to remove Fractional Spurs Noise in the output spectrum of the frequency synthesizer resulting from the use of Accumulator.

2.6.1The Phase Interpolation

The traditional method used to remove Fractional SpursNoise fromPhase Locked Loop Frequency Synthesizer using a technique Phase Interpolation as in Figure(2-20)[Daniel, 2009]

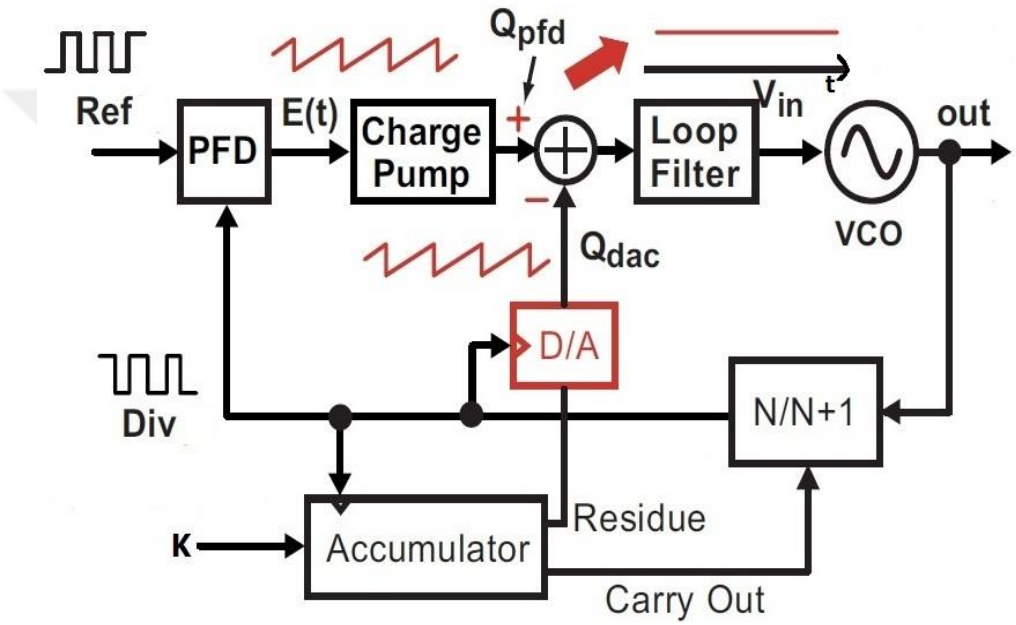


Fig (2-20) Phase Interpolation technique

The Carry- out signal controlled (Dual- Modulus Frequency Divider) to change division ratio from N_{int} to N_{int}+1 to obtained required division ratio. When the Accumulator in addition process the remaining stored value of that process directly proportional to the phase difference . Digital to analog convertor (DAC) used to convert the remaining value in the Accumulator to quantity equivalent the Charge Pump output current to reduce the oscillation in the phase difference signal that produced by the iterative process to change the division ratio (N). The disadvantage of this technique is the difficulty of matching between the phase different signal and the output of the DAC signal .where the mismatch produce noise in the output spectrum [H. T., 2008; Scott, 2005 & Scott, 2003].

2.6.2. Sigma-Delta Modulator

The main reason for the appearance of spur in Fractional N Phase Locked Loop Frequency Synthesizer is the iterative process to change the division ratio from N_{int} to $N_{int}+1$. Fractional Spurs Noise removed by cancelling the iterative process in the Frequency divider and that achieved by using Sigma-Delta Modulator technology as in figure (2-21)[11,15,42]. Where it generate a random integer numbers the average of these numbers equivalent the required fractional value (∝). Also it restructuring the noise by pushing the noise that resulting from the quantization process to the high frequencies to be removed using the loop filter [Xiao, 2008].

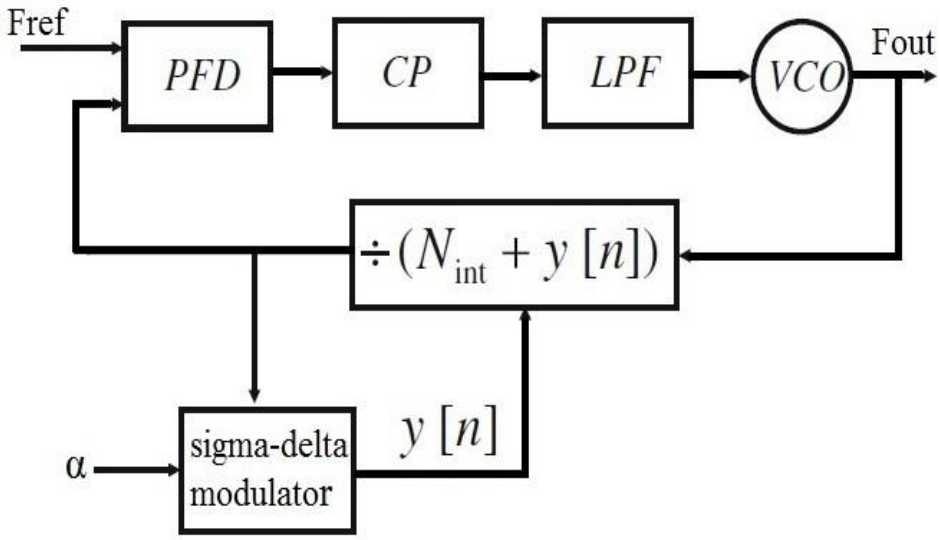


Fig (2-21) PLL Frequency Synthesizer Using Sigma-Delta Modulator

Where the required fractional value (∝) is the input of the Sigma-Delta Modulator while its output is fixed value y[n] represent the integer numbers the average of these numbers equivalent the required fractional value (∝) in addition to (the noise that resulting from the quantization process) that resulting from using integer frequency divider instead of using ideal fractional frequency divider.VCO output frequency divided by N_{int} + y[n].where y[n] is the output of the Sigma-Delta Modulator[Kaveh, 2011].

2.7. The working principle of the Sigma-Delta Modulator

First order Sigma-Delta Modulator consist of (One difference Operator) , one integrator and 1-bit quantizeras in figure (2-22) [Zhiming, 2007 & Steven,1997]

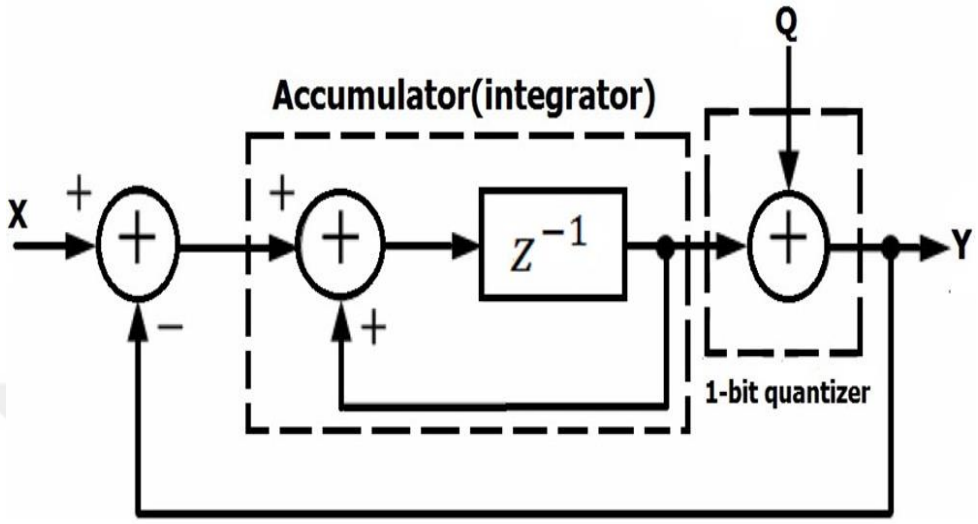


Fig (2-22) First order Sigma-Delta Modulator [Zhiming, 2007 & Steven, 1997]

The working principle of the Sigma-Delta Modulator depends on the Noise Shaping property and the Oversampling property. Where the OSR (Over sampling ratio) reduce the noise that resulting from the quantization process at the required bandwidth so increase the (SNR). The input signal (X) modelling by using signal at (Fs) frequency. The frequency of the modelling signal larger than double the frequency of the input signal .

The Oversampling is the ratio between modelling signal to the double of input signal frequency as the following equation

$$OSR=\frac{F_S}{2.F_B} \qquad (2\text{-}12)$$

The Noise Shaping push the noise that resulting from the quantization process to the high frequencies to be removed by using the loop filter. The equation of the output of the first order Sigma-Delta Modulator is

$$Y(z)= X(z).z^{-1}+ (1-z^{-1}) Q(z) \qquad (2\text{-}13)$$

Where Q(z) represent the noise that resulting from the quantization process.

From eq(2-13) we conclude that the input signal (X) remain unchanged while the noise that resulting from the quantization process pushed to the high

frequencies as a result of the presence the term $(1-z^{-1})$ .The Noise Shaping function can give by the following equation

$$\frac{Y(z)}{Q(z)} = 1-z^{-1} \qquad (2\text{-}14)$$

By Derive the equation (2-14) we can get the noise power for First order Sigma-Delta Modulator [19]

$$S_y(f) = 2\frac{X(1-X)}{T_{ck}}\left(\frac{\sin \pi T_{ck} f}{\pi f}\right)^2 |1-\cos(2\pi f T_{ck})| \qquad (2\text{-}15)$$

$$S_y(f) = 2 S_q(f) |1-\cos(\frac{2\pi f}{F_s})| \qquad (2\text{-}16)$$

Where $S_q(f)$represent noise spectrum for the quantization signal

$S_y(f)$ representnoise power for First order Sigma-Delta Modulator

(X) represent the input of the Modulator

$|1-\cos(\frac{2\pi f}{F_s})|$= Noise Shaping function

$F_s = \frac{1}{T_{ck}}$ modelling frequency

Figure (2-23) show the spectrum of the Noise Shaping function , where it start from zero initial value at f=0 and it become 4 at frequency equal the half of the modelling frequency ($f = \frac{F_s}{2}$). whenthe modelling frequency increase then the Noise Shaping function will expand horizontally thus the noise concentration will be decreased at low frequencies [Rezavi, 2011]

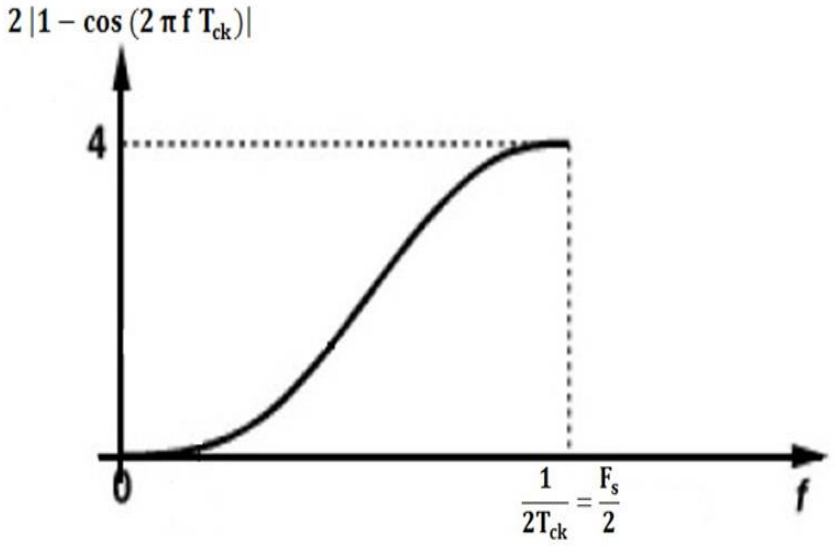


Fig (2-23) spectrum of the Noise Shaping function

In fact the modelling frequency equal to the frequency of the reference frequency (F_{ref}) .since the reference frequency (F_{ref}) much greater than the

bandwidth of the frequency synthesizer so we can consider that $S_q(f)$ be of planar form (constant) at required frequencies as shown in figure (2-24)

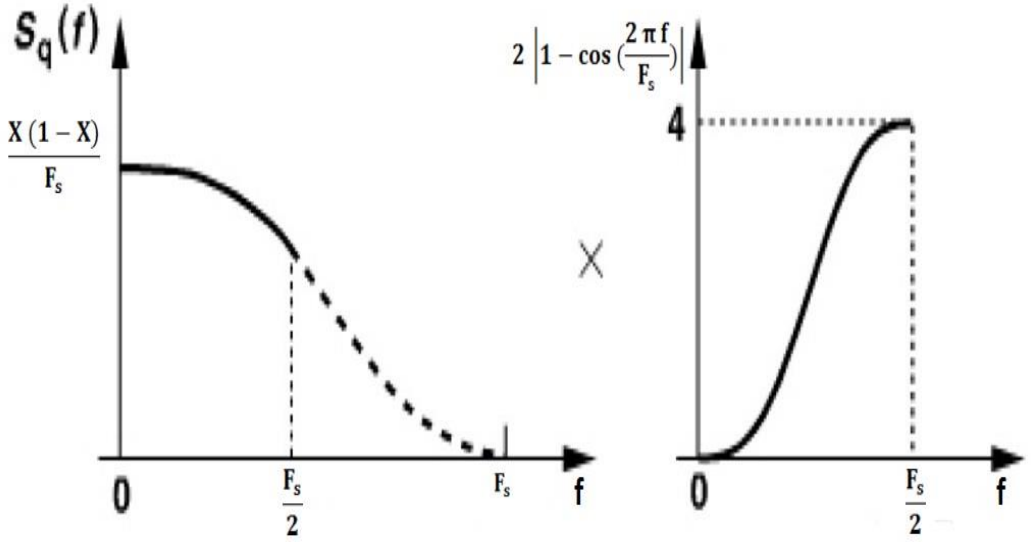


Fig (2-24) the multiplication of noise spectrum for the quantization signal with Noise Shaping function for First order Sigma-Delta Modulator

For this we can assume that the Noise Shaping process for First order Sigma-Delta Modulator will be almost as in figure (2-23) [Rezavi, 2011]. The (SNR) depend on the (OSFR) as the following equation

SNR= 6.02R + 1.76-5.17+30 log(OSR) (2-17)

Where R represent number of the bits for the used modulator.
From the equation above, we conclude that a doubling the OSR will improve the SNR by 9dB.

2.8Second order Sigma-Delta Modulator

The Second order Sigma-Delta Modulator consist of Two differences ,Two integrator and 1-bit quantizer as shown in figure (2-25)

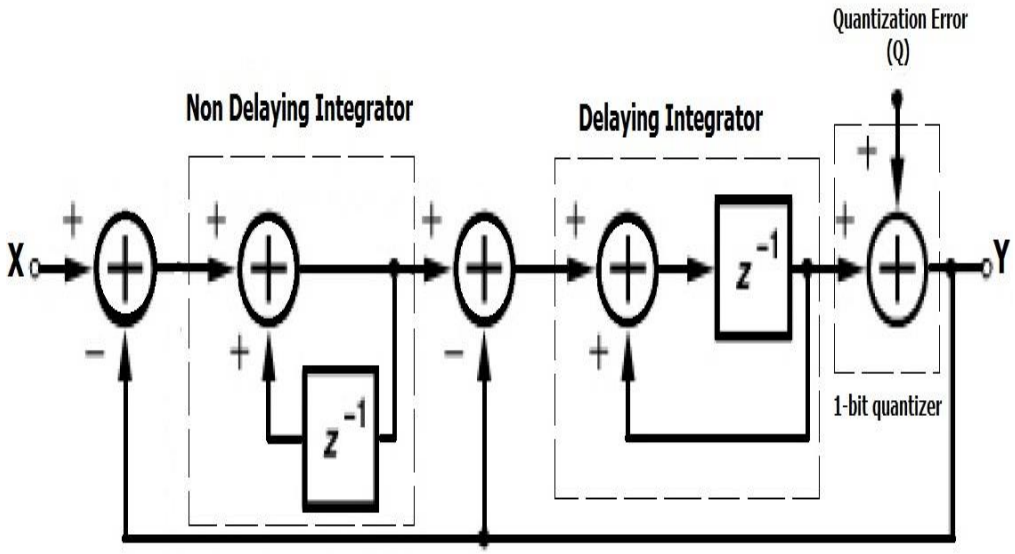


Fig (2-25) Second order Sigma-Delta Modulator

Second order Sigma-Delta Modulator reduce the noise that resulting from the quantization process at low frequency Better than first order Sigma-Delta Modulator [Rezavi, 2011&Alaa, 2002]. The Noise Shaping function can give by the following equation

$$\frac{Y(z)}{X(z)} = (1-z^{-1})^2 \qquad (2\text{-}18)$$

By Derive the equation (2-18) we can get the noise power for Second order Sigma-Delta Modulator

$$S_y(f) = S_q(f)|2\sin(\pi f T_{ck})|^4 \qquad (2\text{-}19)$$

Figure (2-26) show Noise Shaping function for First and Second orders Sigma-Delta Modulator

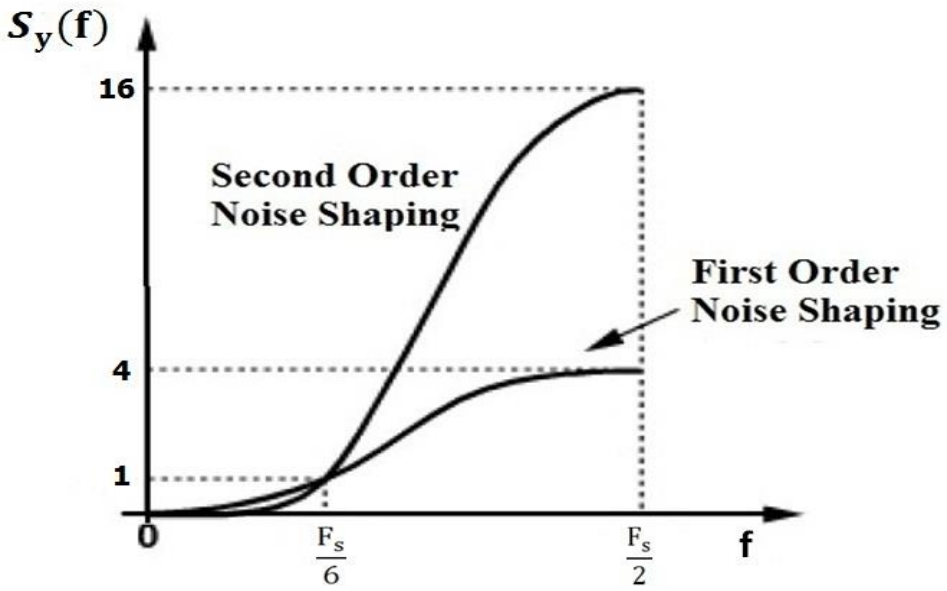


Fig (2-26) the Noise Shaping function for First and Second orders Sigma-Delta Modulator

The (SNR) for Second order Sigma-Delta Modulator is given by

SNR= 6.02R + 1.76- 12.9+50 log(OSR) (2-20)

From the equation above, we conclude that a doubling the OSR will improve the SNR by 15dB

2.9Higher orders Sigma-Delta Modulator

Higher order Sigma-Delta Modulator reduce the noise that resulting from the quantization process at low frequency Better than first and second orders Sigma-Delta Modulator. Figure (2-27) show the instruction of Lth orders Sigma-Delta Modulator where it consist of (Lth integrate) (the number of integrate identify the order of the Modulator [Yongjie, 2006]).

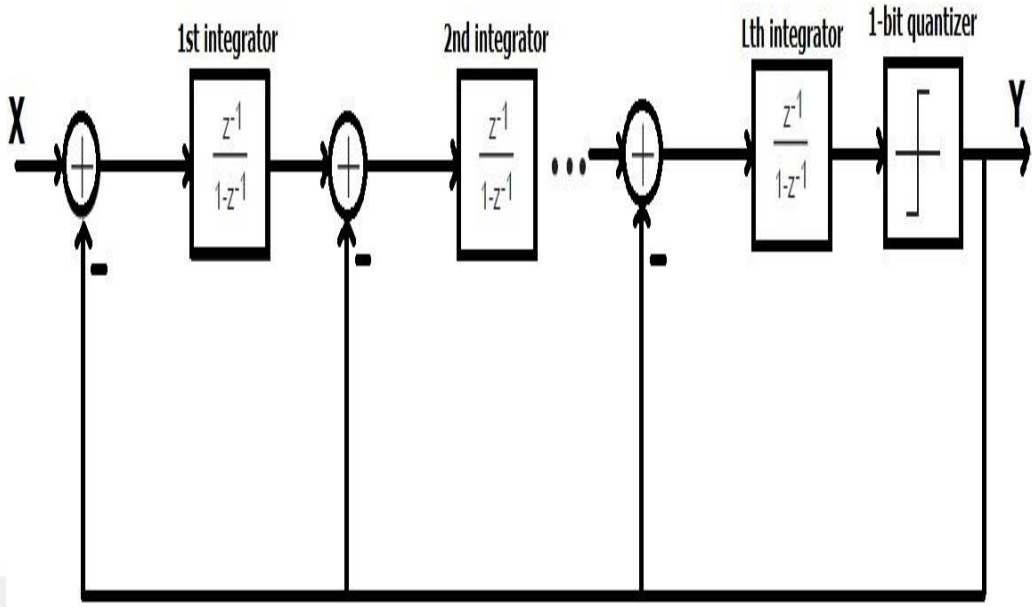


Fig (2-27) Lth orders Sigma-Delta Modulator

The Noise Shaping function can give by the following equation

$$NTF= (1-z^{-1})^{L} \quad (2\text{-}21)$$

By Derive the equation (2-21) we can get the noise power for Second order Sigma-Delta Modulator

$$S_y(f) = S_q(f)|2\sin(\pi f T_{ck})|^{L} \quad (2\text{-}22)$$

Figure (2-28) show comparing The Noise Shaping function for different orders of Sigma-Delta Modulator

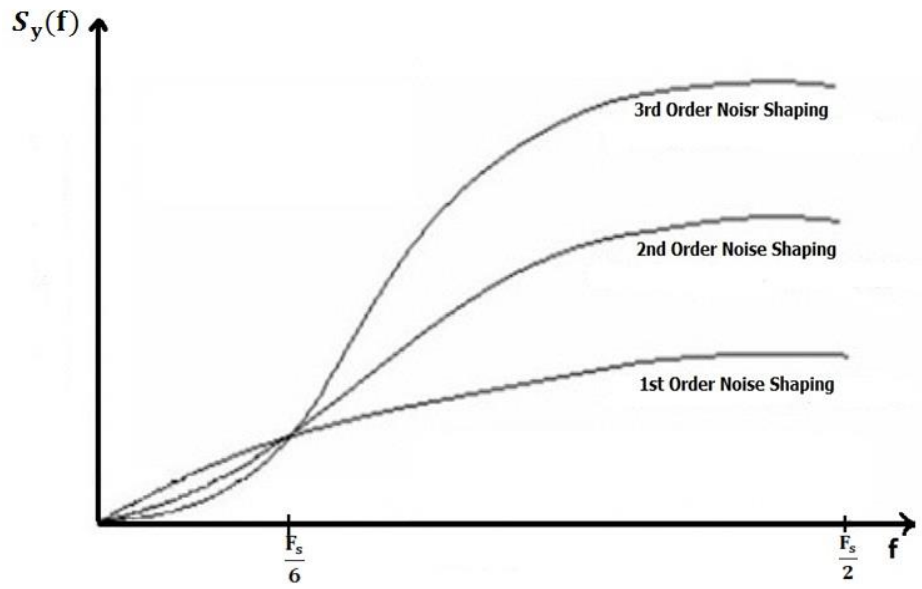


Fig (2-28) The Noise Shaping function for different orders of Sigma-Delta Modulator

Although Higher order Sigma-Delta Modulator reduce the noise that resulting from the quantization process at low frequency but it increase the noise that resulting from the quantization process at high frequency between ($\frac{Fs}{6}$<f<$\frac{Fs}{2}$).to solve this problem the loop filter must be in the same or higher order of Sigma-Delta Modulator to make sure that noise does not effect on VCO output signal spectrum [Mücahit, 2004 &Fatahi, 2010].

The (SNR) for Higher order Sigma-Delta Modulator is given by

$$SNR = 10\log\left(\frac{3}{2}2^{2R}\right) + 10\log\left[\frac{(2L+1)}{\pi^{2L}}(OSR)^{2L+1}\right] \quad (2\text{-}23)$$

2.10Sigma-Delta Modulator types

Sigma-Delta Modulator divided into :

1- Multi Stage Noise Shaping (MASH)
2- Single loop

Where MASH Modulators provides multi bits output, while Single loop provides single or multi bits output depending on the type of the quantizer that used[1].figure (2-29) show third order MASH Modulators

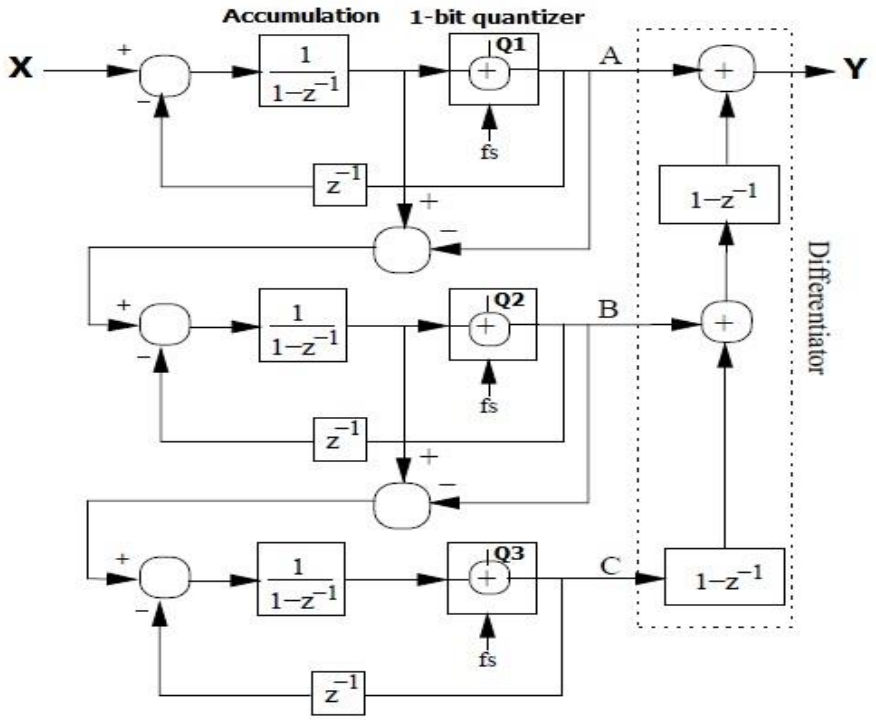


fig (2-29) Third order MASH Modulators

the figure above show that the MASH MODULATOR consist of three first order Sigma-Delta Modulator. The input signal (X) applied on the first modulator , while the input of the second modulator is the sum of the noise signal resulting from the quantization process for first modulator with the quantizer output of the second modulator Thus, for the third modulator.The relationship between the input and the output for the Third order MASH Modulators can given by [Hongyu, 2009; Alaa, 2002 &Yongjie, 2006]

$Y(Z)= A + B(1-z^{-1})+c(1 - z^{-1})^2$ (2-24)

Where

$A= X(z) +Q_1(z)(1-z^{-1})$ (2-25)

$B= [-Q_1+ Q_2(z)(1-z^{-1})](1-z^{-1})$ (2-26)

$C= [-Q_2+ Q_3(z) (1-z^{-1})](1-z^{-1})$ (2-27)

By Substitution for A,B and C in equation (2-24) we can get

$Y(z)= X(z) + (1-z^{-1})^3 Q_3(z)$ (2-28)

The advantage of the MASH Modulators is easily design compared with Single loop Modulators. figure (2-30) show third order Single loop Modulators where

it consist of Three integrate , Two gain blocks, Three feedback line, one bit quantizer[Hongyu, 2006].

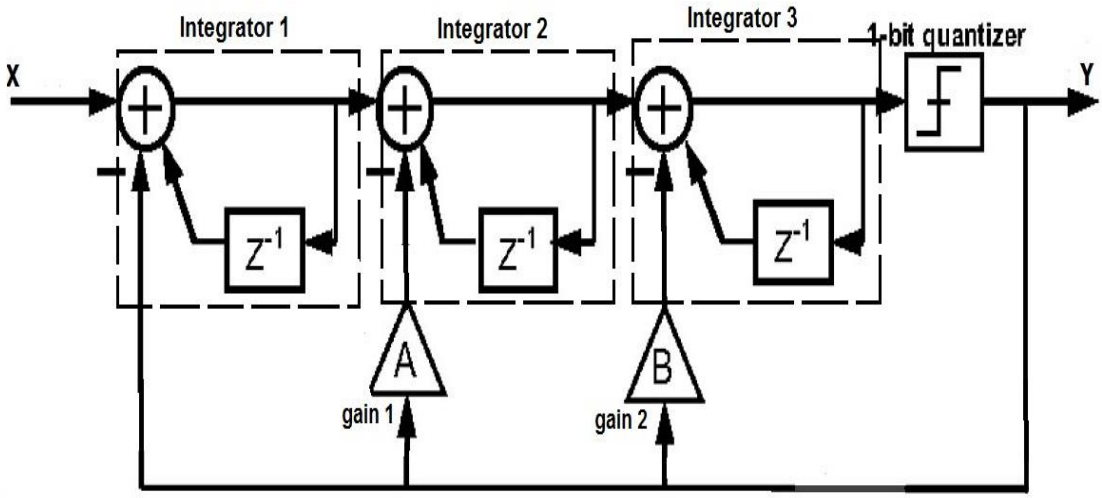


fig (2-30) Third order Single loop

Single loop modulator provides the freedom to choose the values of the constants (A,B) to get best Noise Shaping function [1].the disadvantage of higher order Single loop modulator which use one bit quantizer is not good stability as a result of one bit quantizer overload , to solve this problem the multi bit quantizer must be used . One of the main advantages of using multi bit quantizer is increasing (SNR) where the (SNR) increase by (6dB) for each additional bit[Yongjie, 2006]. Table (2-1) shows a simple comparison between MASH Modulators and Single loop Modulator.

MASH	Single Loop
NTF = $(1 - z^{-1})^L$	NTF = $\frac{(1-z^{-1})^L}{D(z)}$
Noise spectrum cannot be controlled	Controlled Noise spectrum
Easily design and construction	The difficulty of design and construction.
Always Stable.	The Stability depends on the used quantizer
Multi bit output	Multi or one bit output

3. Design and Simulation of Sigma-Delta Fractional-N PLL for Bluetooth System

Bluetooth system can provide a short-range remote connection between mobile phones, personal computers and many other electronic systems. Bluetooth system works at high frequencies of 2.4GHz, using the technique of (Frequency Hopped Spread Spectrum) to decrease the interference and attenuation in the transmitted and received signals. In addition, Bluetooth enables users to communicate with no cables. Bluetooth uses a frequency band called Industrial Scientific-Medical (ISM) [Bluetooth corporation, 2003 &Hooman, 2001]. ISM band is used to provide communications in many applications like communications between mobile phones, cars security systems, noisy signals generators like microwaves and other applications. In America and most European countries, a frequency range from 2.404 to 2.480GHz is used. Table 1-3 gives 79 frequency channels, with a space of 1MHz between each two adjacent channels to prevent interference between channels signals. In Spain and France, 23 frequency band are used. The Bluetooth integrated circuit contains a single phase interleaved circuit. Bluetooth is a cheap and low power consuming device for efficient usage [Stephen, 2001].

Table 3-1 Bluetooth Frequency Bands in Different Countries.

Country	Frequency Band	RF Channel Centers	
USA and most of Europe	2400.0 MHz to 2483.5 MHz	f = 2402 MHz + k MHz	k = 0, ..., 78
Japan	2471.0 MHz to 2497.0 MHz	f = 2473 MHz + k MHz	k = 0, ..., 22
Spain	2445.0 MHz to 2475.0 MHz	f = 2449 MHz + k MHz	k = 0, ..., 22
France	2446.5 MHz to 2483.5 MHz	f = 2454 MHz + k MHz	k = 0, ..., 22

Figure 3-1 The Distribution of the Frequency Bands in Bluetooth Systems.

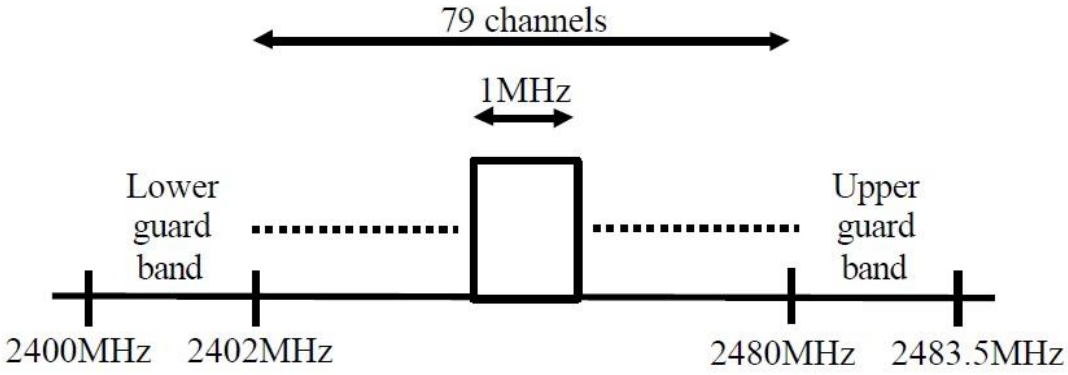


Fig (3-1) the Frequency Bands in Bluetooth Systems

Figure 3-1 shows that a space of 2MHz is left between the frequency bands in the range between 2400 to 2402MHz, while 3.5MHz is left when using the range between 2480 to 2483.5MHz. Equation 3-1 gives the central frequencies of frequency channels [23]:

f channel= 2402 + (A-1) MHz ... (3-1)

where:

A= 1,2,……..,79.

3.1.The Basic Specifications and Requirements of Designing the Frequency Synthesizer of Bluetooth Systems.

Each system has its own specifications, in order to ensure efficient and stable performance for this system. The frequency Synthesizer differ in the phase noise, Spurs Noise and the stability time for the signal generated depending on the application in which this frequency Synthesizer is being used. Table 3-2 shows the requirements and basic specifications that should be provided when designing the frequency Synthesizer of Bluetooth systems [Nilakantan, 2002; William, 2000; National Semiconductor Corporation, 2000; Prakash, 2009 & Wong, 2002].

Table 3-2 The Requirements and Basic Specification of Bluetooth Systems.

Specification	Bluetooth
(MHz)F_{ref}	13,19.2,20,26,39.2,40
Frequency Range	2402 to 2480 MHz
Channel Spacing	1 MHz
Accuracy	±75 kHz
Phase Noise	-110 dBc/Hz @ 2 MHz, -119 dBc/Hz @ 3 MHz
Settling Time	≤ 220 μsec
Reference Spurs	≤ -49 dBc
Fractional Spurs	Free

3.2 The Proposed Design Structure

The frequency Synthesizer is considered the most important factor in signal generation in wireless communications systems. Due to the importance of having very high speed in transmitting data, high frequencies are usually used. This means that frequency Synthesizer should generate high frequencies with high resolution, like the frequency used in Bluetooth systems. In this thesis, the fractional Phase Locked Loop Frequency Synthesizer and its design are studied. Figure 3.2 shows the proposed design using Advanced Design System (ADS).

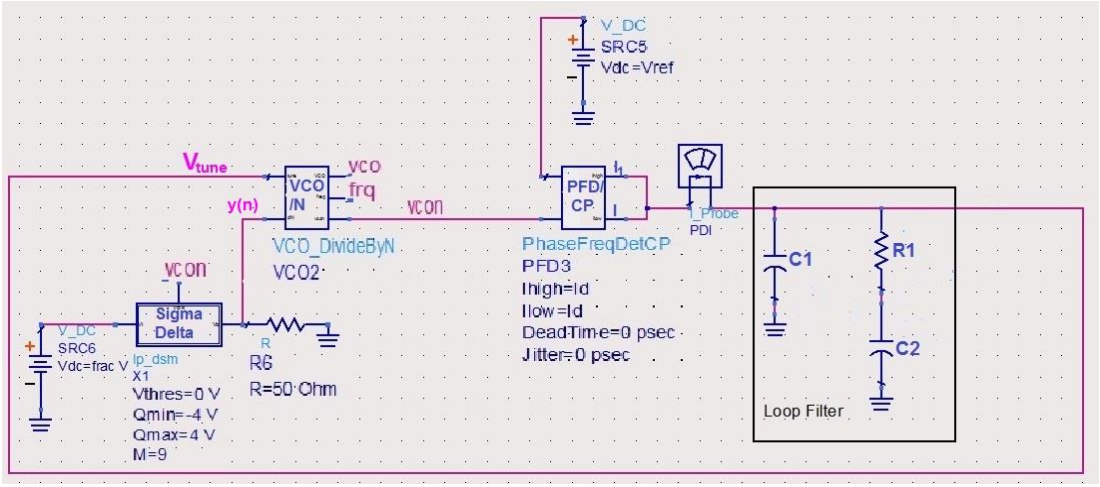


Figure 3-2 The Proposed Design using (ADS)

The proposed design consists of frequency and phase detector, filter, frequency-controlled oscillator, current or charges generator, frequency divider and Sigma-Delta modulator. The main purpose of this thesis is to design a frequency Synthesizer using the Phase Locked Loop technique for Bluetooth system, in addition to improving the performance of this frequency Synthesizer.

Different levels of filters were designed to note the effect of changing the filter order on the level of Spurs Noise and phase noise. A single circuit Sigma-Delta modulator was used in the proposed frequency Synthesizer, where different orders of this modulator were used in order to specify the best performance that can be achieved in removing the Spurs Noise. The proposed circuit was simulated using ADS and Matlab programs. ADS is a programming system used for electronic design, produced by Agilent EEs of EDA Company, where it is able to provide a complete design environment for designing electronic systems that work at radio frequencies like mobile phones, satellites and radar systems. The simulations of this program are very near to the experimental lab results.

3.2.1Filter Design

This section focuses on the filter design and the accompanied complications. Designing a filter requires high accuracy in selecting the basic filter characteristics like filter order, phase margin and the width of the filter pass band. When these parameters are specified, both the filter parameters (R, C) can be found.

3.2.1.1 Filter Order

Filter order is specified by the number of Poles used in the filter. Second order filters are usually used for its simplicity. However, second-order filters can be useless in removing the reference Spurs Noise that result from the current generator. Thus, third or fourth-order filters are used instead.

3.2.1.2 The Bandwidth and Phase Margin of the loop filter

The filter bandwidth is the most important factor to be specified in the filter design. The bandwidth specifies the level of the noise Spurs Noise and stability time, where narrower bandwidth decreases the level of these noise Spurs Noise, while increases the stability time. During filter design, The values of thecapacitor should be considered. Narrow bandwidth mean that the capacitor have very high and unreal values, while wide pass bands means that the values of capacitor are very low and thus will have no effect because of the capacitorof the input of voltage-controlled oscillator. The selected phase margin specifies the stability of the system, where increasing the phase margin leads to decreasing the peak response of the output signal [Dean, 2006].

3.2.2 Second-order Filter Design

Second-order filters have simple design. Figure 3-3 shows the design of the filter used in this work. This filter consists of two capacitor and one impedance [Dean, 2006].

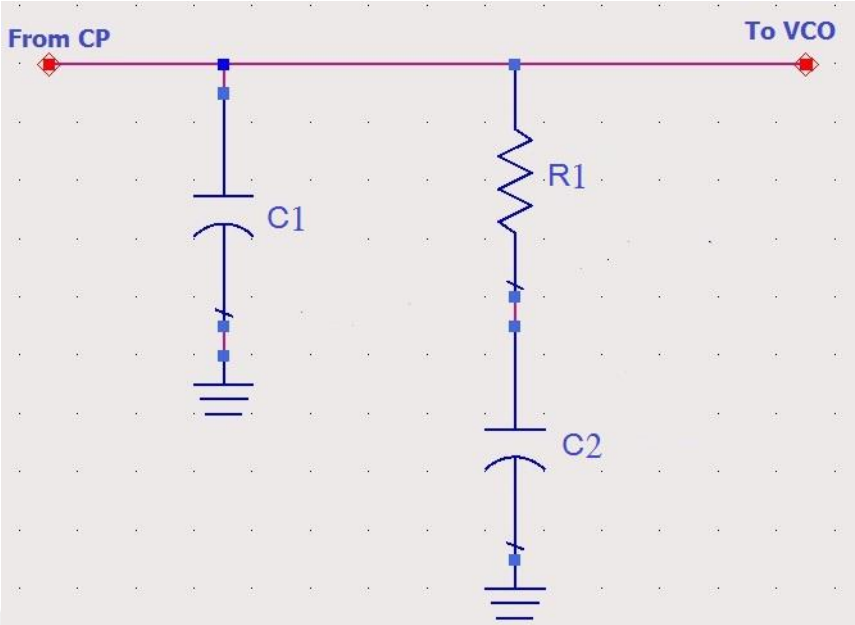


Figure 3-3 The proposed second-order filter using (ADS)

The transfer function or impedance of the used filter is given in the following equation [Dean, 2006]:

$$Z(s)== \frac{1 + s.C2.R1}{s\,(C1 + C2).(1+\frac{s.C1.C2.R1}{C1+C2})} = \frac{1+s.T2}{s.A0.(1+s.T1)} \qquad (3\text{-}2)$$

Where T1 is the zero in the loop filter transfer function, T2 is the first pole in the loop filter transfer function and A0 is the loop filter coefficient. The filter parameters (R1, C1 and C3) can be found using the following equations [Dean, 2006]:

$$C1= A0.\frac{T1}{T2} \qquad (3\text{-}3)$$

$$C2= A0\text{-}C1 \qquad (3\text{-}4)$$

$$R1= \frac{T2}{C2} \qquad (3\text{-}5)$$

where:

$$T1= \frac{\sqrt{(1+\gamma)^2.\tan^2\emptyset+4\,\gamma}-(1+\gamma).\tan\emptyset}{2.\omega c} \qquad (3\text{-}6)$$

$$T2= \frac{\gamma}{wc^2.T1} \qquad (3\text{-}7)$$

$$A0= \frac{K_\emptyset.K_{vco}}{N.wc^2} * \sqrt{\frac{(1 + wc^2.T2^2)}{(1 + wc^2.T1^2)}} \qquad (3\text{-}8)$$

Where γ is the improvement factor, K_Φ is the charges emitting current, Kvco is the gain of the voltage-controlled oscillator and $\Phi$is the amount of phase margin.

3.2.3 Third-Order Filter Design

The third order filter provides an efficient filtering operation for the Spurs Noise that occur at the frequency shift of $10*F_{B.W}$[Dean, 2006]. This type of filter is used with the Synthesizer that uses second-order Sigma-Delta modulator to remove the noise that occur at high frequencies.

Figure 3-4 shows the third-order filter that is used in the proposed design. The design operation requires finding the values of the time constants (T1, T2 and T3). From these time constants, the values of the resistors and capacitorof the filter can be found. The designer choses the required width of the pass band, the phase margin and the ratio between the second pole to the first pole (T31), where the value of T31 is between zero and 1 [Dean, 2006].

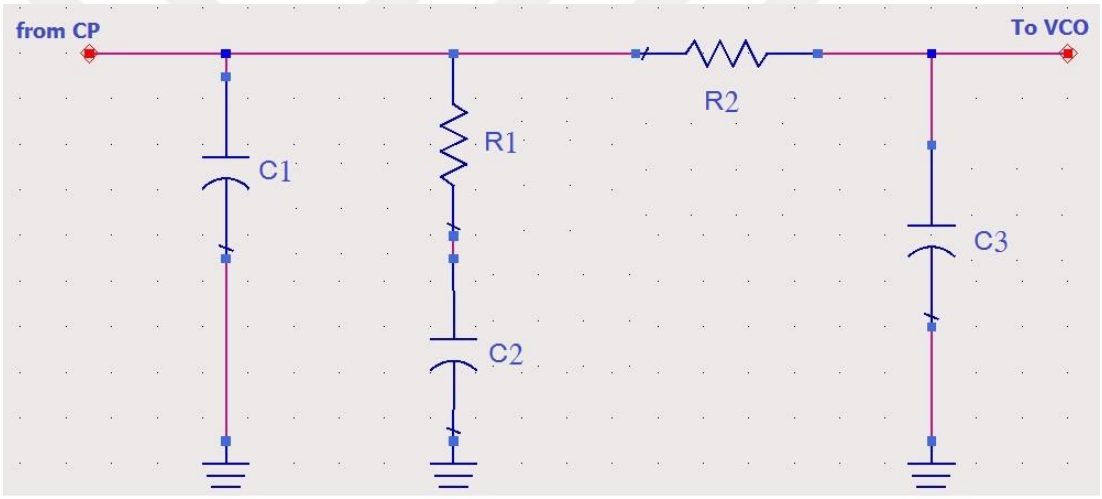


Figure 3-4 The designed third-order filter using (ADS)

The impedance of the third-order filter is given by the following equation :

$$Z(s)=\frac{1+s.T2}{s.A0.(1+s.T1).(1+s.T3)}=\frac{1+s.T2}{s.(A2.S^2+A1.s+A0)} \quad (3\text{-}9)$$

Where T3 is the second pole in the loop filter transfer function and A1 and A2 represent the loop filter coefficients. The value of impedance R1 can be found using equation (3-5), while the values of the filter parameters (R2, C1, C2 anC3) can be found from the equations given in Appendix A [Dean, 2006].

3.2.4 Fourth-Order Filter Design

The fourth-order filter is very effective in removing the Spurs Noise or noise that occur at the frequency shift that equals to ($20*F_{B.W}$) [Dean, 2006]. This filter is used with Synthesizer that uses third-order Sigma-Delta modulator to remove the noise that occur at high frequencies, where the noise that result from the modulator increases with the modulator's order. These filters have a very complicated design. The main challenge in the design operation is in designing a stable filter with parameters of real values. Figure 3-5 shows the proposed fourth-order filter used in the design [Dean, 2006].

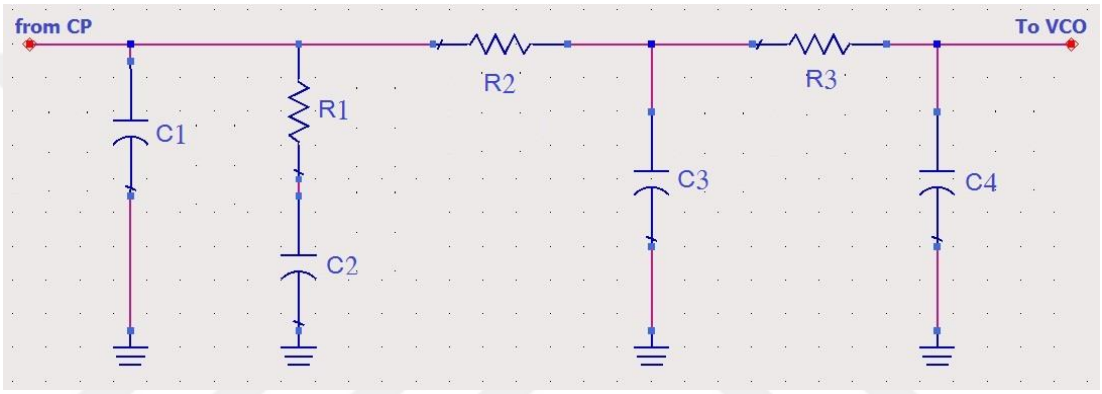


Figure 3-5 The proposed fourth-order filter using (ADS)

The impedance of this filter is given in the following equation [Dean, 2006]:

$$Z(s)=\frac{1+s.T2}{s.(A3.s^3+A2.s^2+A1.s+A0)} \qquad (3\text{-}10)$$

where A3 is the loop filter coefficient. The value of resistance R1 can be found using equation (3-5), while the values of the filter parameters (C1, C2, C3, C4, R2 and R3) can be found using the equations given in Appendix B [Dean, 2006].

3.2.5 Sigma-Delta Modulator used in the Proposed Design

Sigma-Delta modulator of Single loop type was used in the proposed frequency Synthesizer, where three different orders of Sigma-Delta modulator were used. These orders are the first, second and third order.

3.2.5 .1 First-Order Sigma-Delta Modulator

Figure 3-6 gives the proposed design of the first-order modulator. This modulator consists of a single accumulator circuit and a single-bit quantizer. The output of the quantizer is either zero or one. The first order modulator output is the same as the output of the accumulator explained in chapter2. This is why the accumulator technique is called first-order Sigma-Delta modulator.

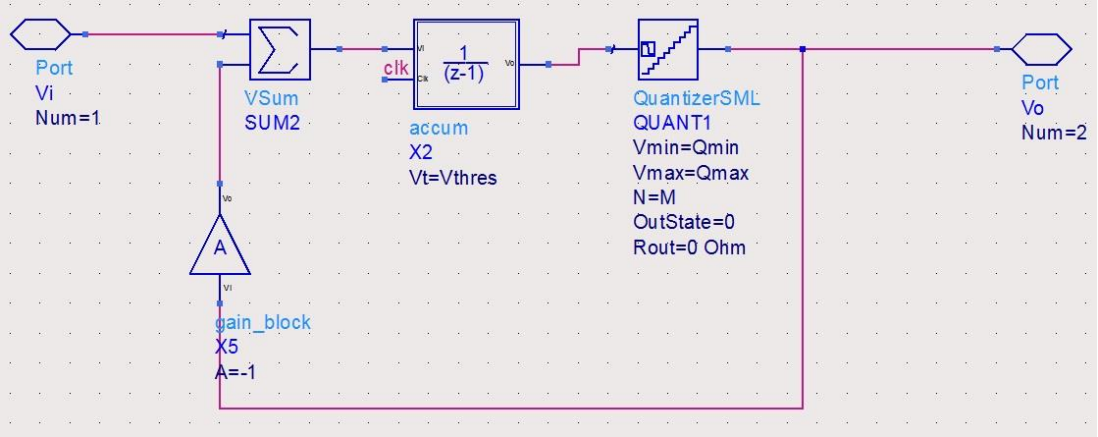


Figure 3-6 The design of the first-order Sigma-Delta modulator using (ADS)

Depending on the figure above, the relation between the input and output of the modulator and the function of the noise configuration is derived in the following equations:

$$Vo = Vi.z^{-1} + Q(z)\,(1-z^{-1}) \qquad (3\text{-}11)$$

$$NTF = \frac{Vo}{Q(z)} = (1-z^{-1}) \qquad (3\text{-}12)$$

Where Q(z) represents the noise results from the accumulation operation, Vi is the input voltage and Vo is the modulator output voltage.

3.2.5.2 Second-Order Sigma-Delta Modulator

Figure 3-7 shows the proposed modulator of second-order Single loop type, where it consists of two accumulator circuits, a multi-bits accumulator and two gains. The value of the accumulator output is between -1 and 2. This is because there are two accumulator circuits (two integrated circuits). The two accumulator circuits push the fractional Spurious Noise to higher frequencies in

addition to decreasing the noise that results from the accumulation operation or the phase noise at the low frequencies.

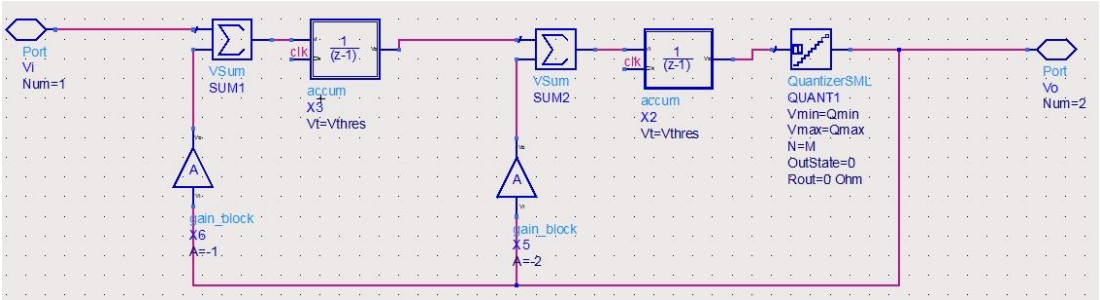


Figure 3-7 The proposed design of second order Sigma-Delta Modulator using (ADS)

Depending on figure 3-7, the equations that represent the relation between the input and output of the modulator and the noise configuration function of the proposed modulator are as follows:

$$[(((Vi - Vo)\frac{1}{z-1}) - 2\,Vo).\frac{1}{z-1}] + Q(z) = Vo \qquad (3\text{-}13)$$

$$Vi.\frac{z^{-2}}{(1-z^{-1})^2} - V0.\frac{z^{-2}}{(1-z^{-1})^2} - 2\,Vo.\frac{z^{-1}}{1-z^{-1}} + Q(z) = Vo \qquad (3\text{-}14)$$

$$Vo.[1 + \frac{2.z^{-1}}{1-z^{-1}} + \frac{z^{-2}}{(1-z^{-1})^2}] = Vi\,\frac{z^{-2}}{(1-z^{-1})^2} + Q(z) \qquad (3\text{-}15)$$

$$Vo = Vi.z^{-2} + Q(z).(1 - z^{-1})^2 \qquad (3\text{-}16)$$

$$NTF = \frac{Vo}{Q(z)} = (1 - z^{-1})^2 \qquad (3\text{-}17)$$

3.2.5.3 Third-Order Sigma-Delta of Single loop type Modulator

Figure 3-8 gives the main parts of the proposed third-order of Single loop type modulator. This modulator consists of three accumulators, a single multi-bit quantizer and three gains. The purpose of this type of modulator is to decrease the phase noise at low frequencies. However, the use of this accumulator may require designing a fourth-order filter to decrease the phase noise at high frequencies.

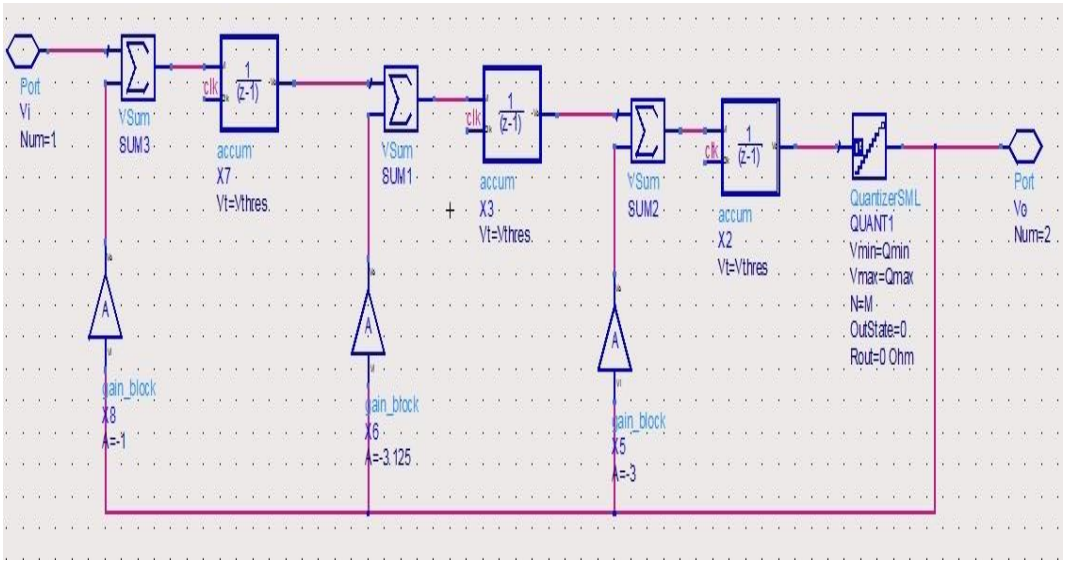


Figure 3-8 The Proposed Third-order Sigma-Delta Modulator using (ADS)

Depending on figure 3-8, the equations that explain the relation between the input and output of the modulator and the noise configuration function of the modulator proposed in this work are derived as follows:

$$[((Vi - Vo)\frac{1}{z-1} - 3.125\ Vo).\frac{1}{z-1} - 3\ Vo]\frac{1}{z-1} + Q(z) = Vo \quad (3\text{-}18)$$

$$[((Vi - Vo)\frac{z^{-1}}{1-z^{-1}} - 3.125Vo)\frac{z^{-1}}{1-z^{-1}} - 3\ Vo]\ \frac{z^{-1}}{1-z^{-1}} + Q(z) = Vo \quad (3\text{-}19)$$

$$Vi\frac{z^{-3}}{(1-z^{-1})^{-3}} - Vo\frac{z^{-3}}{(1-z^{-1})^{-3}} - 3.125Vo\frac{z^{-2}}{(1-z^{-1})^{-2}} - 3Vo\frac{z^{-1}}{1-z^{-1}} + Q(z) = Vo \quad (3\text{-}20)$$

$$Vo[1+\frac{z^{-3}}{(1-z^{-1})^{-3}}+3.125\frac{z^{-2}}{(1-z^{-1})^{-2}}+3\frac{z^{-1}}{1-z^{-1}}] = Q(z)+Vi\frac{z^{-3}}{(1-z^{-1})^{-3}} \quad (3\text{-}21)$$

$$NTF = \frac{(1-z^{-1})^3}{1+0.125\ z^{-2} - 0.125\ z^{-3}} \quad (3\text{-}22)$$

3.2.6 The Multi-bit Quantizer Used in Sigma-Delta Modulator

Figure 3-9 shows the multi-bit quantizer used in the Sigma-Delta modulator design which consists of nine levels.

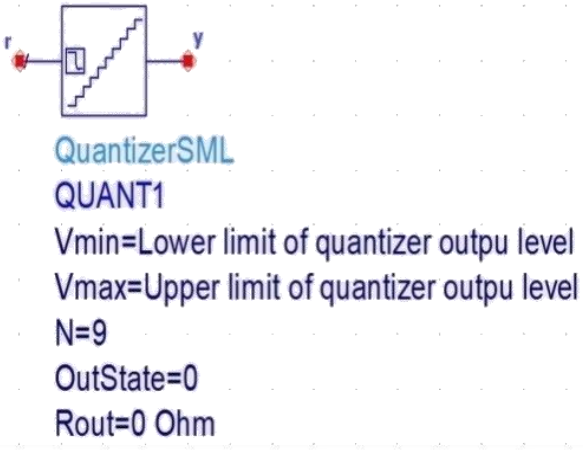


Figure 3-9 The Multi-Bit Quantizer using (ADS)

where N represents the number of levels, Vmin is the lowest limit of the quantizer output, Vmax is the maximum limit of this output, r is the quantizer input and y is the quantizer output.
Figure 3-10 shows the quantizer input and output characteristics for Δ equals to 1, where Δ is the quantizer step.

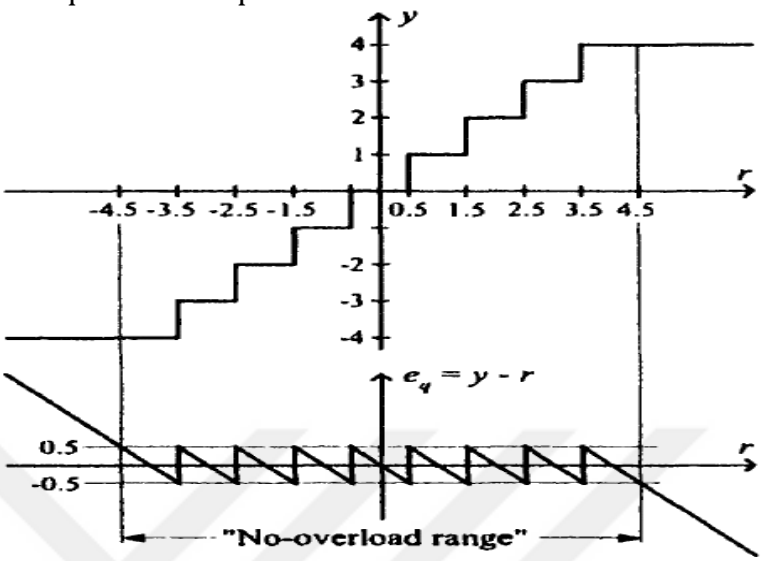


Figure 3-10 Input/output properties of the 9-level Quantizer [Rezavi, 2003]

whereeq is the noise resulted from the Quantizer.
The used quantizer works as follows [Rezavi, 2003]:

1- When the input r is greater than 9Δ/2, the quantizer is in the overload stage and its output is 4Δ.
2- When the input r is less than -9Δ/2, the quantizer is in the overload stage and its output is -4Δ.
3- When the input r is between 9Δ/2 and -9Δ/2, the quantizer gives an output value that represents nearest integer of the input.

4. Simulation Results and Discussion

This chapter includes display ,clarify and make comparisons to the simulations results that have been practically obtained using the two programs (ADS and MATLAB) for The proposed frequency Synthesizer. This chapter show the simulations results of the frequency response for the proposed system and the simulations results for the proposed modulator that used in the design and the simulations results of noisy response for (output spectrum, Phase noise ,Spurs noise and the settling time) for The proposed frequency Synthesizer.

Phase Margin value that chosen by the designer is very important in determining the stability and response of the system , usually the range of the Phase Margin value is between 30 ˚ to 70 ˚.and usually the Phase Margin value chosen between 45˚ and 55˚ [Dean, 2006].

The bandwidth determine settling time, Spurs noise level and Phase noise level.

4.1 The simulations results for the noise and frequency response for The proposed Frequency Synthesizer and the proposed

This section include the simulations results forthe magnitude and phase response for The proposed Frequency Synthesizer at 150 kHz bandwidth ,and the simulations results for first order Sigma-Delta modulator, and also include the simulations results for the proposed frequency Synthesizer.

4.1.1The simulations results forthe proposed Frequency Synthesizer at 150 kHz bandwidth

Second order loop filter has been used in the proposed Frequency Synthesizer that designed at 150 kHz bandwidth , 50˚ phase margin , $K_{\emptyset} = 50$ µA,$K_{vco} =$ 210 MHz and reference frequency (F_{ref}) =19.2MHz. by using the equation for the second order loop filter the value of the loop filter components will be C1=34.39 PF, C2=225.21 PF, R1=12.944 KΩ . equation (4-1) show open loop gain function for the proposed design[Michael, 2005].

$$A(s) = \frac{Z(s).K_{\emptyset}.K_{vco}}{N.s} \qquad (4\text{-}1)$$

While equation (4-2) show close loop gain function for the proposed design

$$G(s) = \frac{A(s)}{1+A(s)} \qquad (4\text{-}2)$$

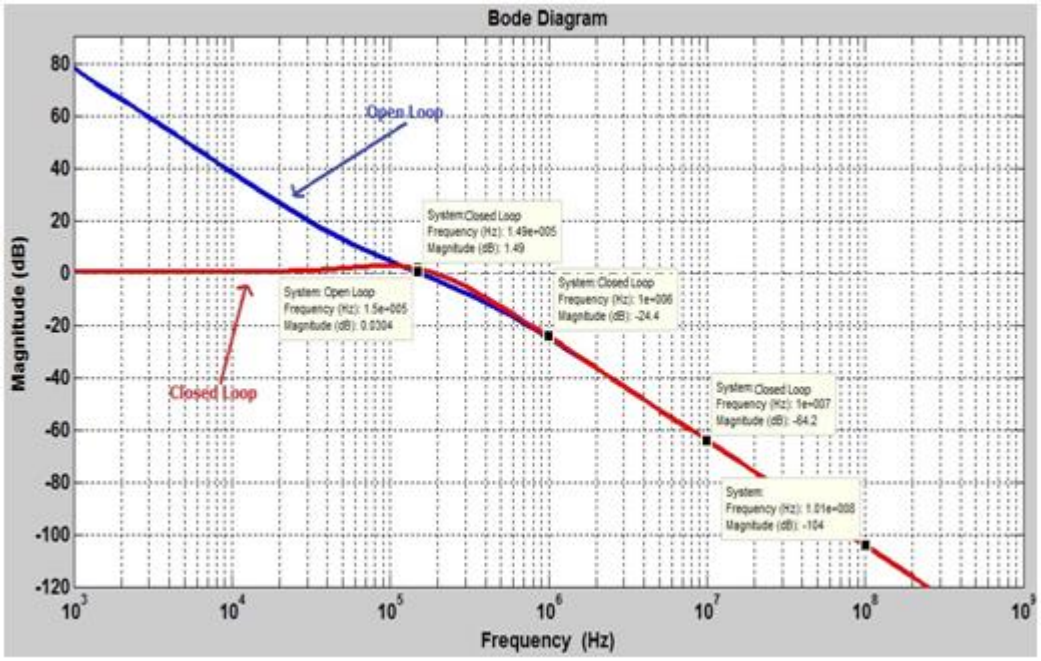
The impedance of the loop filter have been calculated by using the value of the loop filter component.

By substitute the value of the loop filter impedance the equations (4-1) and (4-2) will be

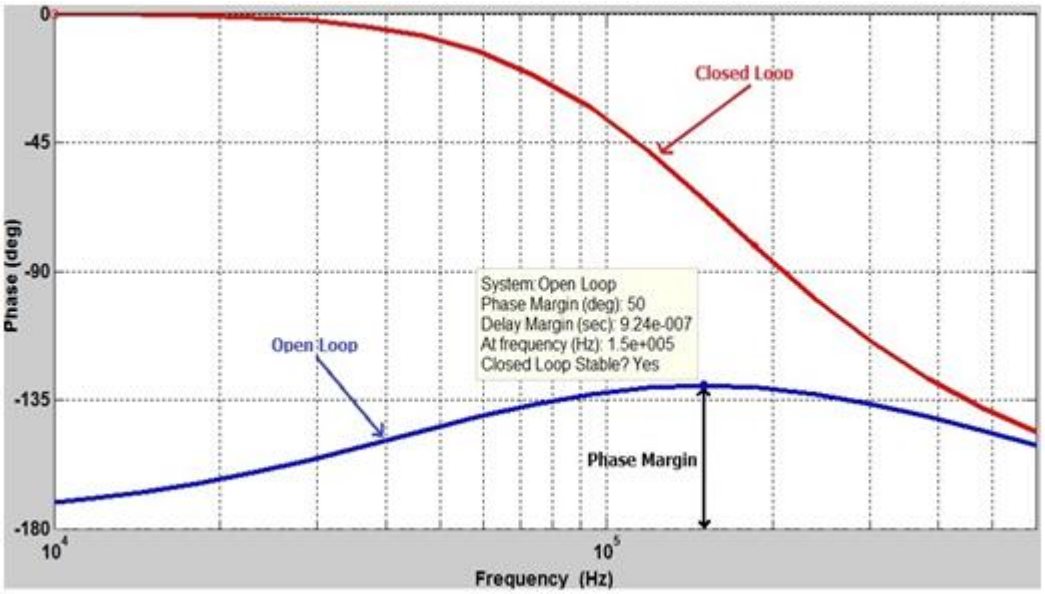
$$A(s)=\frac{32.4*10^{10}.\ (1+\ 2.9*10^{-6}\ s\ )}{s^2.(1+3.86*10^{-7}s)} \qquad (4\text{-}3)$$

$$G(s) = \frac{(94.46*10^{4}s\ +32.4*10^{10})}{(3.86*10^{-7}s^3+\ s^2+94.46*10^{4}s\ +32.4*10^{10})} \qquad (4\text{-}4)$$

Figure (4-1) show the frequency response of the proposed Frequency Synthesizer for (open loop gain and close loop gain) by using MATLAB.



(a)



(b)

Fig (4-1):(a) frequency response Magnitude for the proposed Frequency Synthesizer (b) frequency response Phase for the proposed frequency Synthesizer

Figure (4-1)(a) show that the operation of the proposed Frequency Synthesizer is at 150 kHz bandwidth and it is the same value that was selected in the design process, and show that the magnitude frequency response of the closed-loop gain was equal to 1.49 dB at a frequency of 150 KHz where the performance of the loop filter is improving when it will be small value, also the magnitude frequency response decreased with increasing frequency and this is one of the characteristics of low pass filter. It should be noted that whenever the slope of the magnitude frequency response faster to go down the loop filter remove the phase noise at higher frequencies better. The Phase margin of the proposed Frequency Synthesizer given by the following equation:

Phase Margin = 180˚ –|phase of open Loop T. f (in deg)| (4-5)

While figure (4-1)(b) show that the phase of open loop equal 130˚,by using equation (4-5) the phase margin of the proposed Frequency Synthesizer equal 50˚ and it is the same value that was selected in the design process. this figure also show that at the closed loop the system is stable.

Figure (4-2) show simulation of the proposed Frequency Synthesizer the open loop gain and the close loop gain by using ADS.

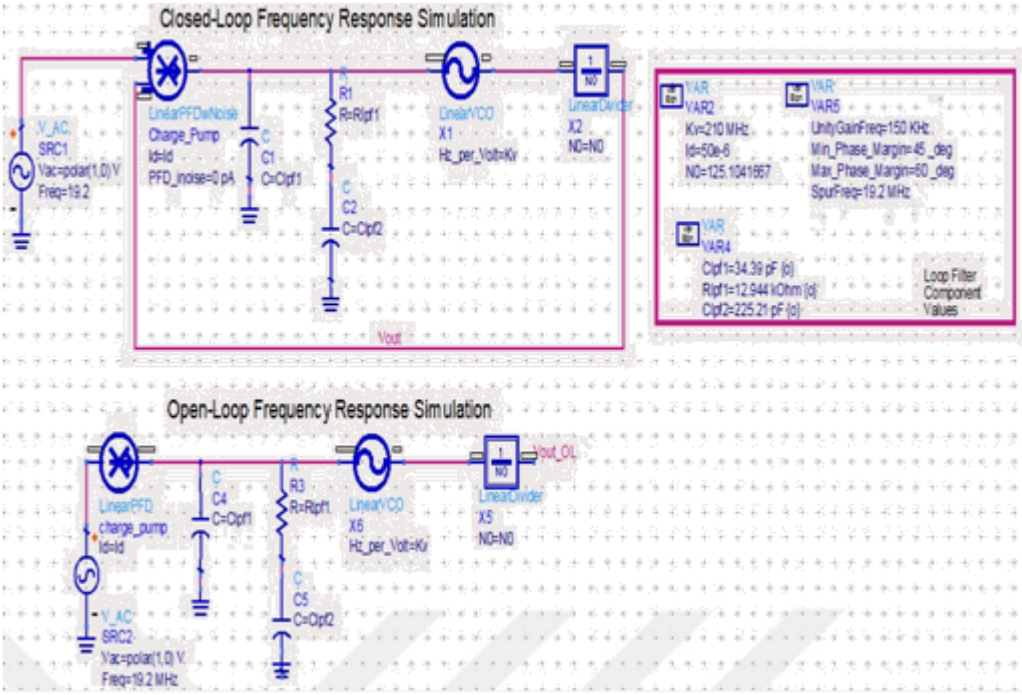


Fig (4-2) the simulation of the proposed Frequency Synthesizer that have second order loop filter by using ADS

Figure (4-3) show the frequency response of the proposed Frequency Synthesizer for (open loop gain and close loop gain) by using ADS.

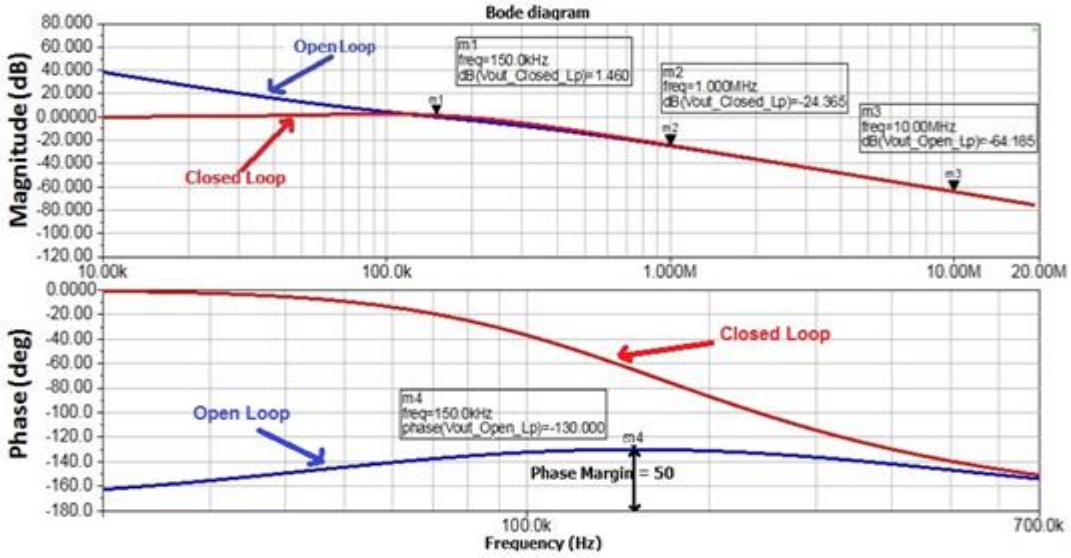


Fig (4-3) the frequency response of the proposed Frequency Synthesizer for (open loop gain and close loop gain) by using ADS

Figure (4-3) show that the operation of the proposed Frequency Synthesizer is at 150 kHz bandwidth and it is the same value that was selected in the design process. Also show that The results that obtained by using ADS were largely approach to the results that have been obtained using MATLAB. Where the

magnitude frequency response of the closed-loop gain was equal to 1.46 dB at a frequency of 150 KHz by using ADS while it is 1.49 dB at a frequency of 150 KHz by using MATLAB. While the phase of open loop equal 130˚,by using equation (4-5) the phase margin of the proposed Frequency Synthesizer equal 50˚ and it is the same value that obtained by using MATLAB. this figure also show that at the closed loop the system is stable.

4.1.2 Simulation result of first order Sigma Delta Modulator

First order Sigma Delta Modulator have been used in the design of the proposed frequency Synthesizer. Figure (4-4) show the output of First order Sigma Delta Modulator at value equal 5/48 (where 5/48 represent the fractional part of the division ratio resulting from dividing the output signal frequency of 2402 MHz to the input signal frequency 19.2 MHz). As shown in Figure (4-4) the Modulator output will be change between zero and one and this will be the generate the required fractional part. The modulator output equal one every 479.1 nsec for one clk. The changing in the fractional part will generate fractional spurs in the modulator output spectrum And thus distort the Frequency Synthesizer output spectrum.

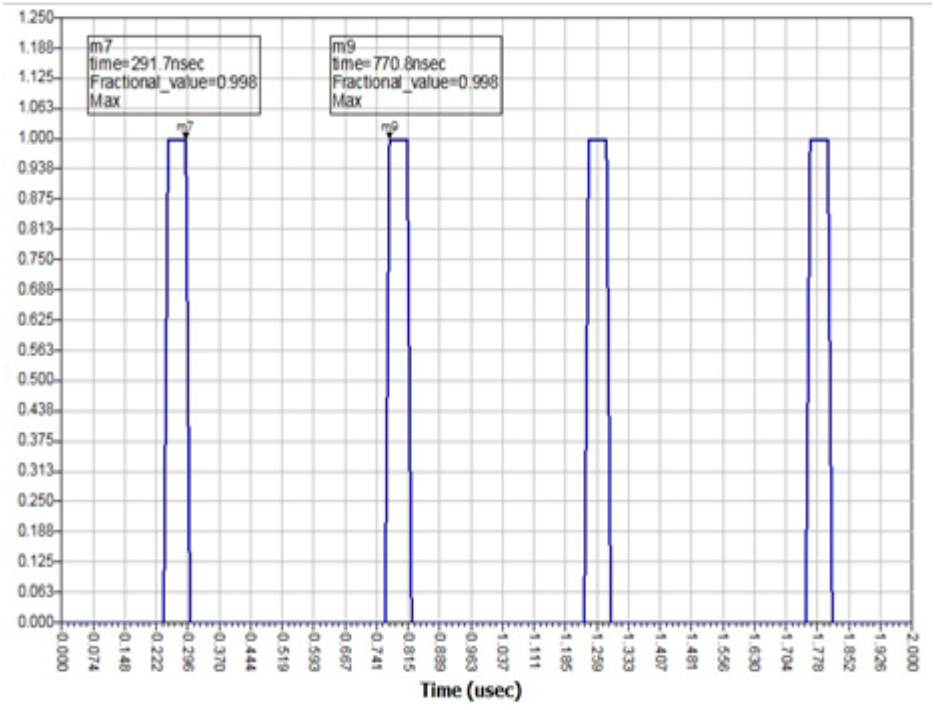


Fig (4-4) First order Sigma Delta Modulator output

Figure (4-5) show the output spectrum of First order Sigma Delta Modulator

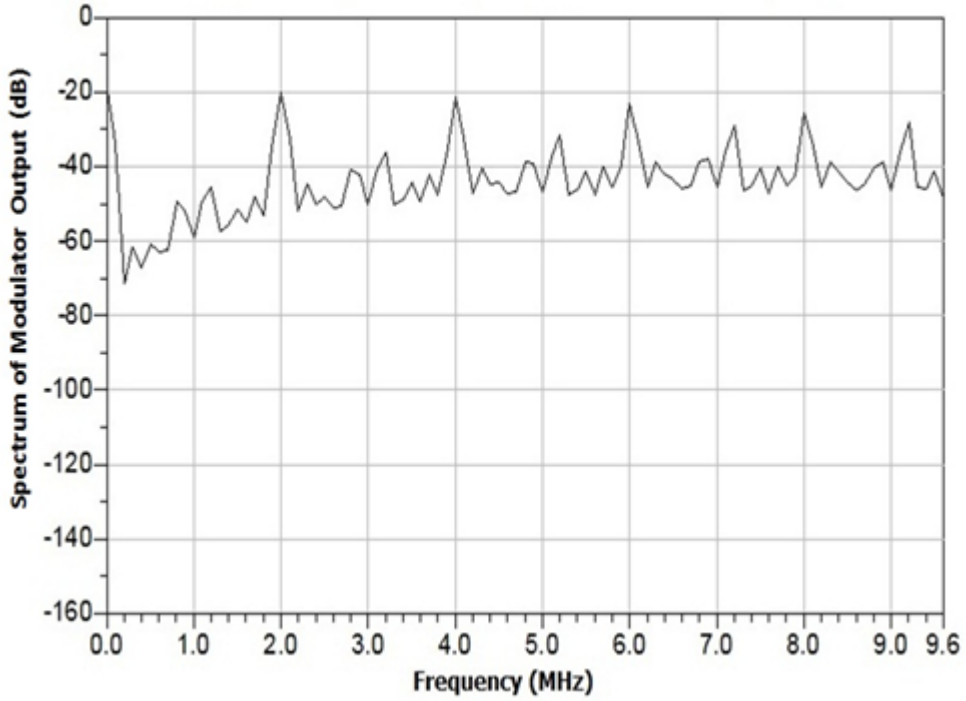


Fig (4-5) First order Sigma Delta Modulator output spectrum

Figure (4-5) show the output spectrum of First order Sigma Delta Modulator have fractional spurs at 2 MHz ,4 MHz and its multiplier because of the modulator output changed between zero and one every 479.1 nsec. This fractional spurs will distort the proposed Frequency Synthesizer and reduce performance of it.

4.1.3 The simulation result of the proposed Frequency Synthesizer (Output spectrum, Phase noise, Settling time) at 150 kHz bandwidth

This section contain the simulation result the proposed Frequency Synthesizer that consist of second order loop filter and first order Sigma Delta modulator. Figure (4-6) show the output spectrum of the proposed Frequency Synthesizer that consist of second order loop filter and first order Sigma Delta modulator at 150 kHz bandwidth.

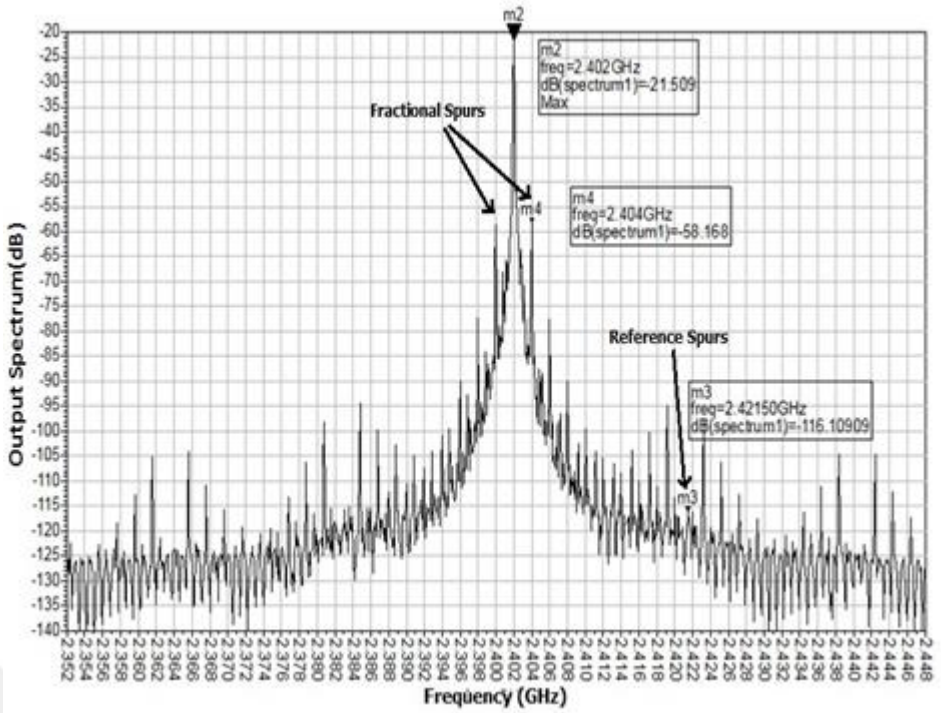


Fig (4-6) The output spectrum of the proposed frequency Synthesizer

Figure (4-6) The output spectrum of the proposed Frequency Synthesizer have fractional and reference Spurs noise . as mentioned before the fractional Spurs noise resulted because of the function of the modulator is similar to the function of accumulator. While reference Spurs noise resulted from the mismatch between Charge pump currents (UP & Down) .theSpurs noise level function is given by

$$\text{Spurs level} = P_{Noise}(\text{at offset freq}) - P_{Carrier} \quad (4\text{-}6)$$

Where P_{Noise}(at offset freq) represent the power of the noise signal at a specific frequency offsets.

While $P_{Carrier}$ represent the power of the carrier signal.

The level of first fractional spur noise equal -36.651 dBc at 2 MHz frequency offsets while the level of first reference spur noise equal -94.6 dBc at 19.2 MHz frequency offsets. The Phase noise function is given by

$$\text{Phase Noise} = P_{Noise}(\text{at offset freq}) - P_{Carrier} - 10 \log (1.2 * RBW) + 1.05\ dB + 1.45\ dB \quad (4\text{-}7)$$

Where RBW represent bandwidth resolution for the spectrum analyzer and 1.05 represent the detector response in the spectrum analyzer. Figure (4-7) show the Phase noise of the proposed Frequency Synthesizer that consist of

second order loop filter and first order Sigma Delta modulator at 150 kHz bandwidth and frequency offsets between 0 MHz to 20 MHz.

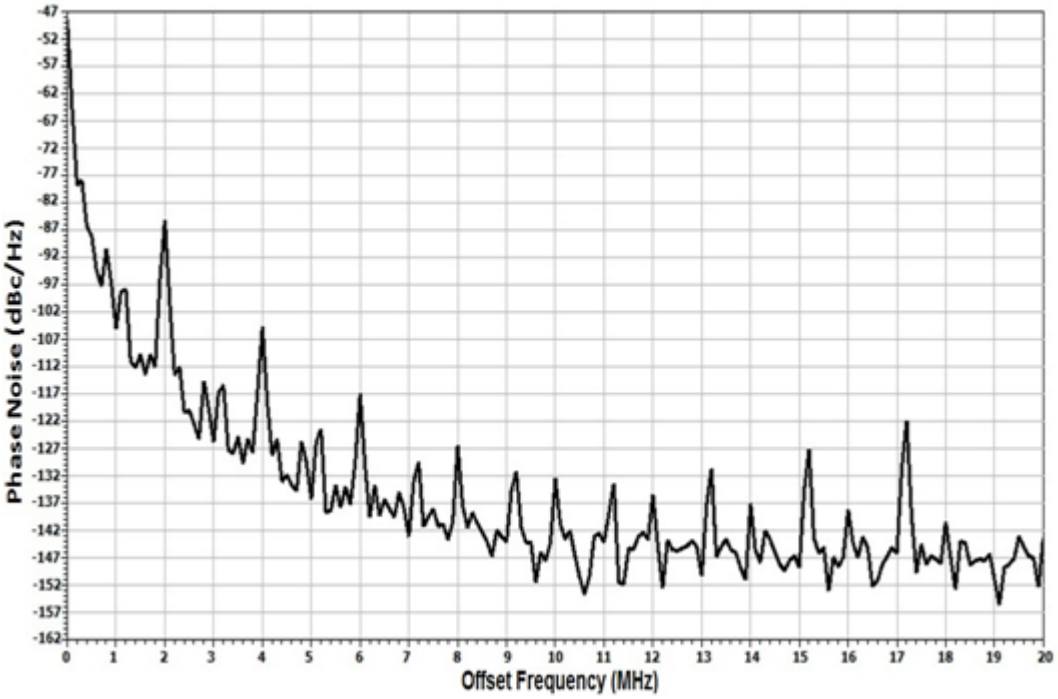


Fig (4-7) The Phase noise of the proposed frequency Synthesizer

Figure (4-7) show that the phase noise equal -85 dBc/Hz at 2 MHz frequency offsets. While it equal -126 dBc/Hz at 3 MHz frequency offsets and it's not acceptable values in Bluetooth application. Also it have high fractional Spurs noise level and this will distort the Received or Transmitted signal and that will decrease the performance frequency Synthesizer. One of the important factors that must be computed in the Frequency Synthesizer is settling time and it was calculated for the Frequency Synthesizer using the equation (4-8)

$$\text{Settling Time} = \frac{-\ln\left(\frac{tol}{f2-f1}\sqrt{1-\zeta^2}\right)}{\zeta.\omega n} \qquad (4\text{-}8)$$

Where

$$\omega n \text{ (Ringing Frequency)} = \sqrt{\frac{K_{\emptyset}.K_{vco}}{N.A0}} \qquad (4\text{-}9)$$

$$\zeta(\text{ Damping Factor}) = \frac{T2}{2}\omega n \qquad (4\text{-}10)$$

$f_2$represent the final frequency , f_1 represent the initial frequency, and tol represent frequency tolerance. The Damping Factor determines the shape of the frequency of output signal for the Frequency Synthesizer. when the

Damping Factor increase the settling time improved. While resonance frequency (ωn) represent the fluctuation in the output signal to stabilize , increase resonance frequency cause increasing frequency resolution of the output signal [Dean, 2006]. The settling time that calculated by equation (4-8) at 150 kHz equal 9.06 μsec. figure (4-8) show the time and frequency of the Frequency Synthesizer.

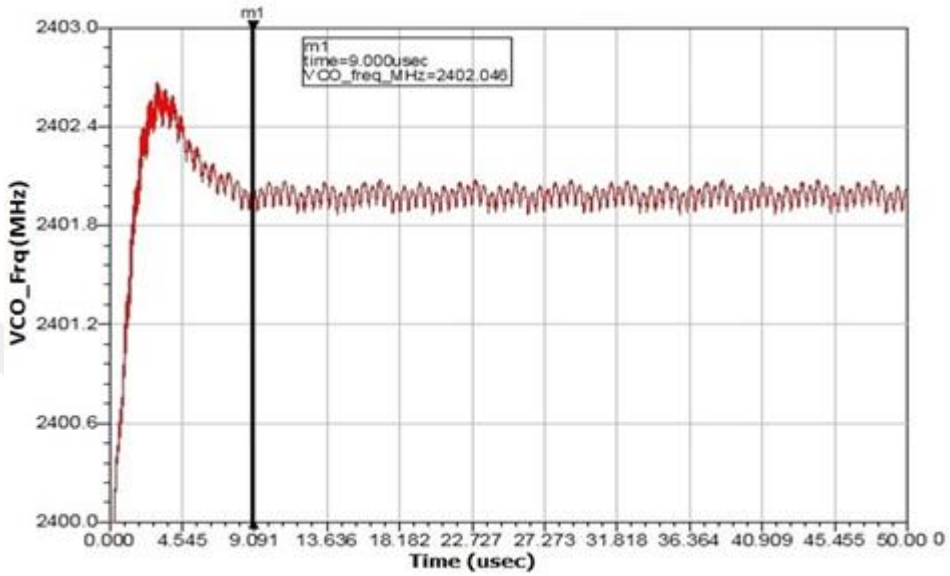


fig (4-8) The time and frequency of the Frequency Synthesizer

figure (4-8) show that the settling time equal 9 μsec and it is the same value obtained by using a theoretical equation (4-8) and it is a good value for Bluetooth system. While the error in the output signal equal 46 KHz. We can say that this proposed Frequency Synthesizer ineffective because it contains a high level of Spurs noise and Phase noise that distort the output spectrum of it. There are several solution to reduce the level of Spurs noise and Phase noise that will be mentioned in the next section.

4.2 Solutions used to reduce the level of Spurs noise and Phase noise

There are several solution to reduce the level of Spurs noise and Phase noise for the proposed Frequency Synthesizer as follow :

4.2.1 Reduce the bandwidth toreduce the level of Spurs noise and Phase noise

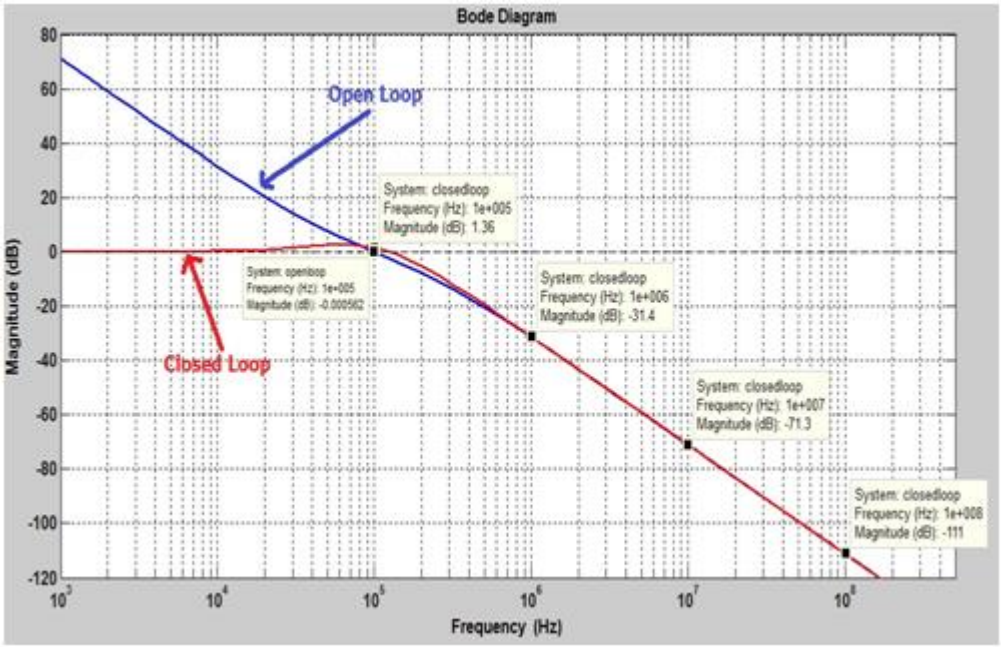
This section include the simulations results forthe magnitude and phase response for The proposed Frequency Synthesizer at 100 kHz bandwidth and the simulations results (Output spectrum, Phase noise , Settling time) for The proposed Frequency Synthesizer.

4.2.1.1 The simulations results for the proposed Frequency Synthesizer at 100 kHz bandwidth

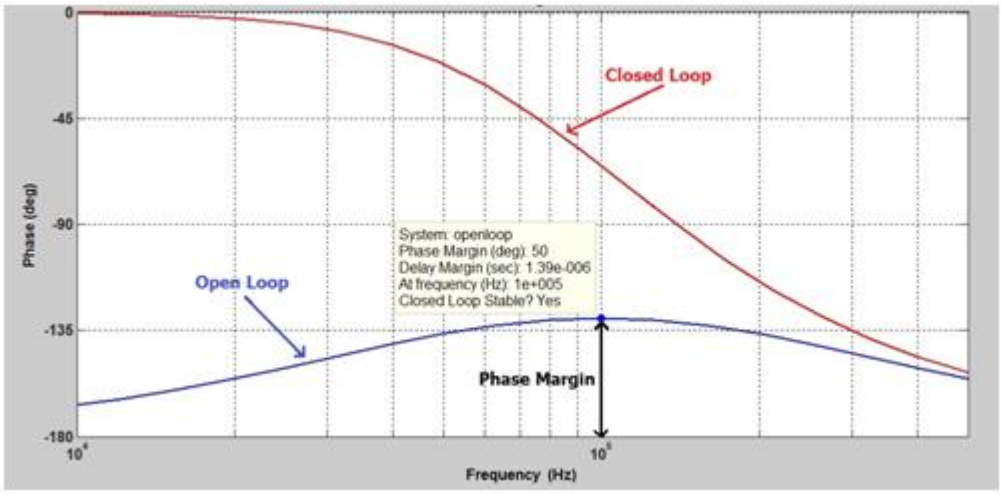
By using equation (4-1) the open-loop function for the proposed Frequency Synthesizer at 100 kHz bandwidth is:

$$A(s)=\frac{14.368*10^{10}.(1+4.37*10^{-6}\,s)}{s^2(1+5.793*10^{-7}\,s)} \qquad (4\text{-}11)$$

Figure (4-9) show the frequency response of the proposed Frequency Synthesizer for (open loop gain and close loop gain) by using MATLAB



(a)



(b)

Fig (4-9)(a) frequency response Magnitude for the proposed Frequency Synthesizer (b) frequency response Phase for the proposed frequency Synthesizer

Figure (4-9)(a) show that the operation of the proposed Frequency Synthesizer is at 100 kHz bandwidth and it is the same value that was selected in the design process. And show that the magnitude frequency response of the closed-loop gain is improved by reducing the bandwidth to 100 kHz because the pole (T1) moved toward the few frequencies thus increasing the slope of the magnitude frequency response. Where the magnitude frequency response equal 1.36 dB at 100 KHz bandwidth while it was 1.49 dB at 150 kHz bandwidth. Table 4-1 shows a close-loop comparison between the magnitude frequency response for proposed Frequency Synthesizer is at 100 kHz bandwidth and the magnitude frequency response for proposed Frequency Synthesizer is at 150 kHz bandwidth.

Frequency (MHz)	Closed Loop T.F Magnitude (dB)	
	B.W= 100 KHz	B.W= 150 KHz
1	-31.4	-24.4
10	-71.3	-64.2
100	-111	-104

Table 4-1

Table 4-1 show that the frequency response for proposed Frequency Synthesizer is at 100 kHz bandwidth is better than the frequency response for proposed Frequency Synthesizer is at 150 kHz bandwidth. Where the magnitude frequency response for proposed Frequency Synthesizer is at 100 kHz bandwidth equal -31.4 dB at 1 MHz while it equal -24.4 dB for proposed Frequency Synthesizer is at 150 kHz.

Figure (4-9)(b) show that the phase of open loop equal 130˚,by using equation (4-5) the phase margin of the proposed Frequency Synthesizer equal 50˚ and it is the same value that was selected in the design process. Figure (4-10) show simulation of the proposed Frequency Synthesizer the open loop gain and the close loop gain by using ADS.

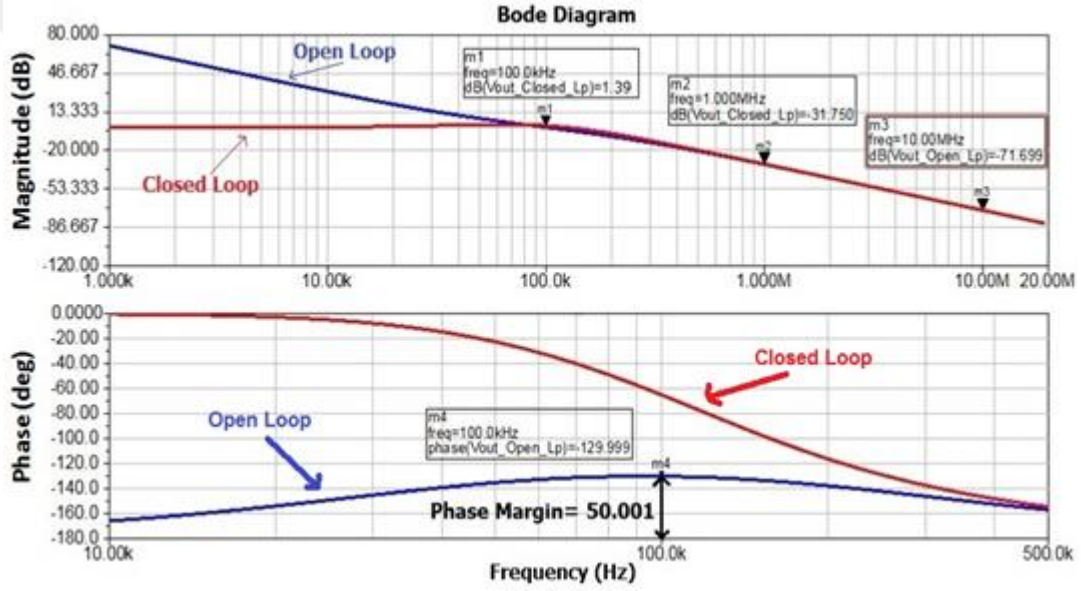


Fig (4-10) the frequency response of the proposed Frequency Synthesizer for (open loop gain and close loop gain) by using ADS

Figure (4-10) show that the operation of the Frequency Synthesizer at 100 kHz bandwidth and it is the same value that was obtained by using MATLAB. Also show that The results that obtained by using ADS were largely approach to the results that have been obtained using MATLAB. Where the magnitude frequency response of the closed-loop gain was equal to 1.39 dB at a frequency of 100 KHz by using ADS while it is 1.36 dB by using MATLAB. While the phase of open loop equal 129.999˚,by using equation (4-5) the phase margin of the proposed Frequency Synthesizer equal 50.001˚ and it is approach to the value obtained by

using MATLAB. The little difference between the results of the two programs resulting from the ADS program give practical and realistic results unlike MATLAB program, which give theory results.

4.2.1.2 The simulation result of the proposed Frequency Synthesizer (Output spectrum, Phase noise , Settling time) at 100 kHz bandwidth

Figure (4-11) show the output spectrum of the proposed Frequency Synthesizer that consist of second order loop filter and first order Sigma Delta modulator at 100 kHz bandwidth

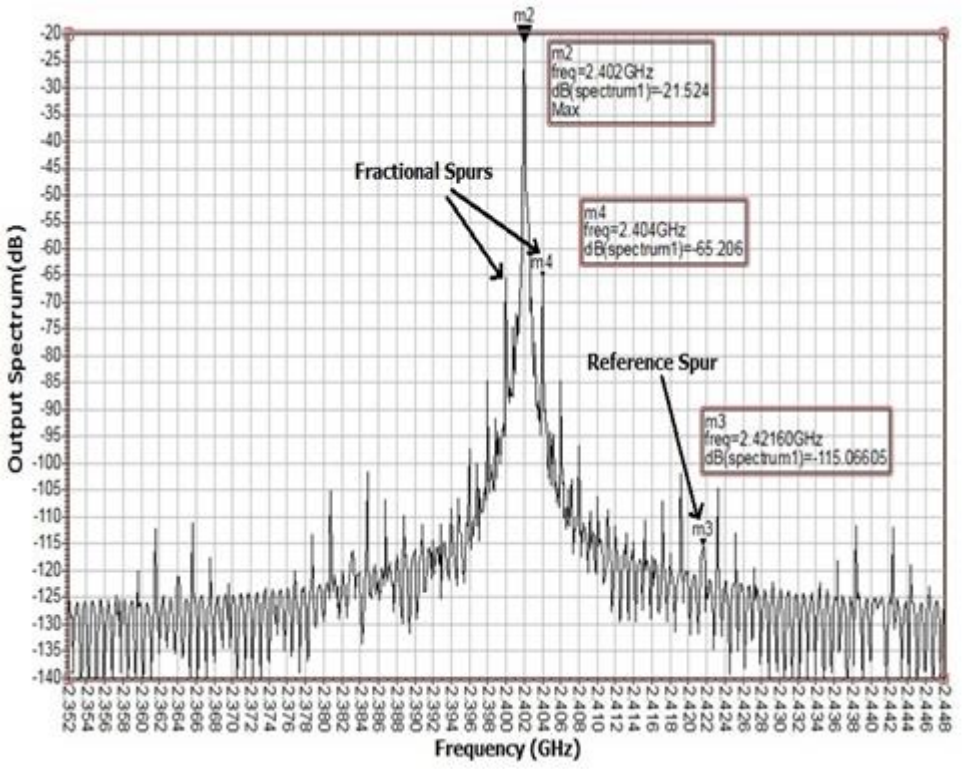


Fig (4-11) The output spectrum of the proposed frequency Synthesizer

Figure (4-11) show that the fractional Spurs noise level decreased, where the level of first fractional spur noise equal -43.7 dBc at 100kHz bandwidth while the level of first fractional spur noise equal -36.651 dBc at 150kHz bandwidth . Figure (4-12) show the Phase noise of the proposed Frequency Synthesizer that consist of second order loop filter and first order Sigma Delta modulator at 100 kHz bandwidth

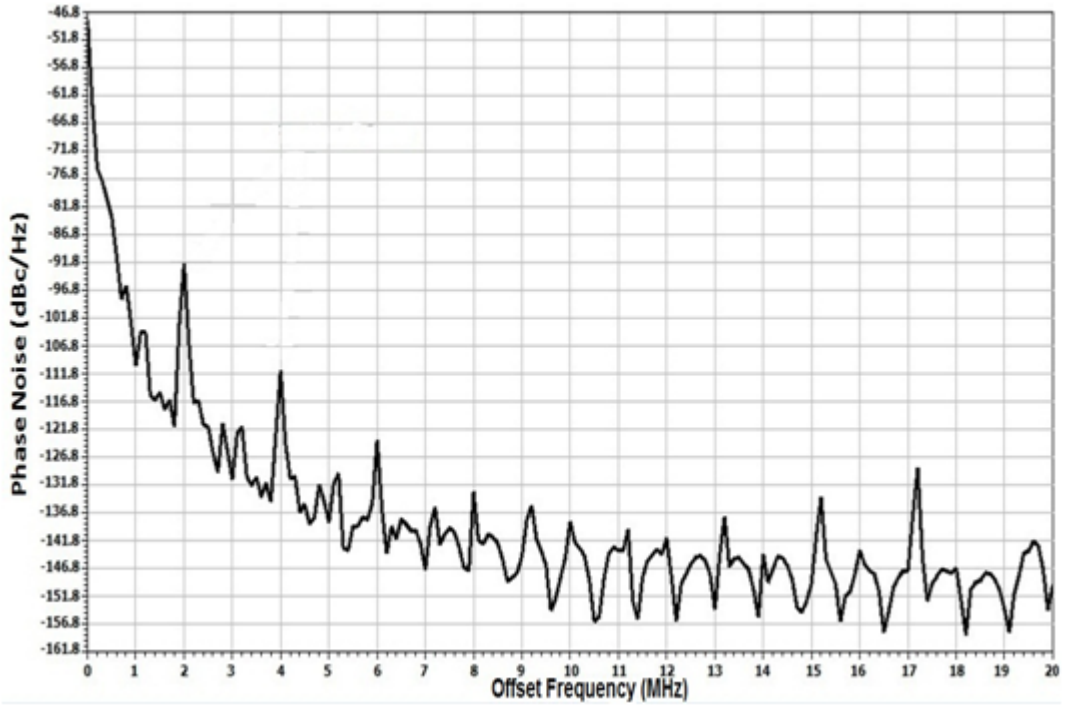


Fig (4-12) The Phase noise of the proposed frequency Synthesizer

Figure (4-12) show that the Phase noise level is improved by decrease the bandwidth to 100 kHz because decreasing the bandwidth cause improving in the frequency response for the proposed frequency Synthesizer. Table 4-2 show Phase noise comparison between the proposed Frequency Synthesizer is at 100 kHz bandwidth and the proposed Frequency Synthesizer is at 150 kHz bandwidth

Offset Frequency (MHz)	Phase Noise (dBc/Hz)	
	B.W= 100 KHz	B.W= 150 KHz
1	-109	-105
2	-92	-85
3	-130.8	-126
5	-138	-136
7	-146.8	-143

Table 4-2

Table 4-2 show that the Phase noise for proposed Frequency Synthesizer at 100 kHz bandwidth equal -92 dBc/Hzat 2 MHz frequency offset while it equal -85

dBc/Hzfor proposed Frequency Synthesizer is at 150 kHz. And it's not good value for Bluetooth application. By using equation (4-7) the settling time equal 13.6 µsec figure (4-13) show the time and frequency of the Frequency Synthesizer

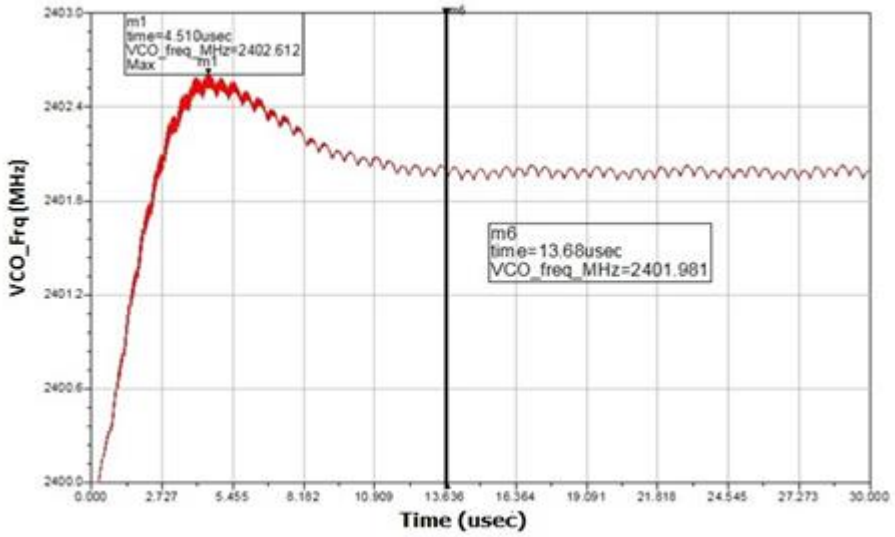


fig (4-13) The time and frequency of the Frequency Synthesizer

Figure (4-13) show that the settling time equal 13.68 µsec and it is approach to the value obtained by using theoretical equations. In comparison with proposed Frequency Synthesizer is at 150 kHz bandwidth we find that the frequency resolution of the output signal improved by reducing the bandwidth to 100 kHz. Where the output frequency equal 2401.981 MHz at 100 kHz bandwidth while it equal 2402.46 MHz at 150 kHz bandwidth. But decreasing the bandwidth cause increasing the settling time. The obtained result show that when decrease the bandwidth to 100 kHz the Spurs noise level and the Phase noise decreased and the frequency resolution improved but increasing the settling time. And this proposed Frequency Synthesizer is not effective for Bluetooth application because the output spectrum have Spurs noise distort the receiver and transmitter signals.

4.2.2 Increasing loop filter order toreduce the level of Spurs noise and Phase noise

This section include frequency response simulation (open-loop and close-loop) for proposed Frequency Synthesizer that contain third order loop filter at 100

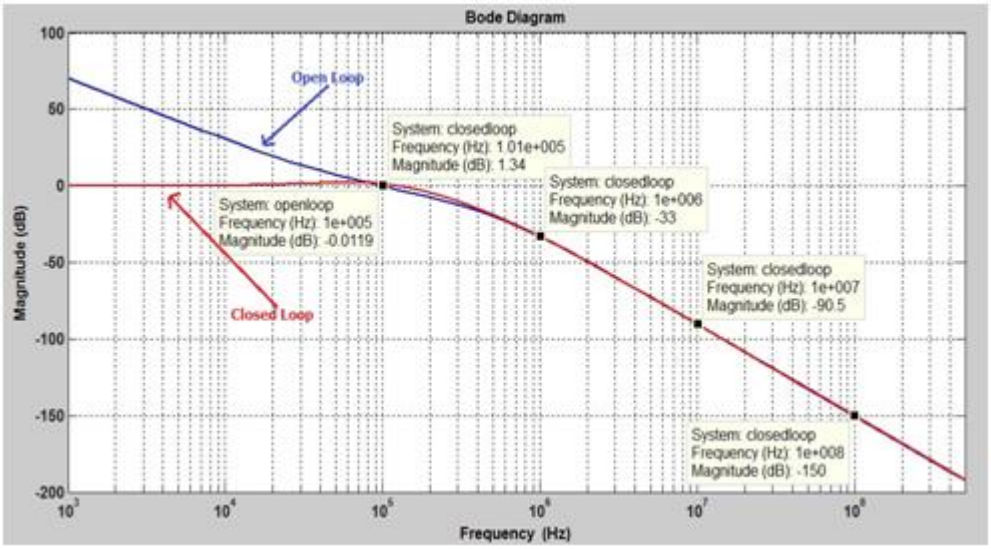
kHz bandwidth and the simulation result of the proposed Frequency Synthesizer (Output spectrum, Phase noise , Settling time)

4.2.2.1 Frequency response simulation for proposed Frequency Synthesizer that contain third order loop filter at 100 kHz bandwidth

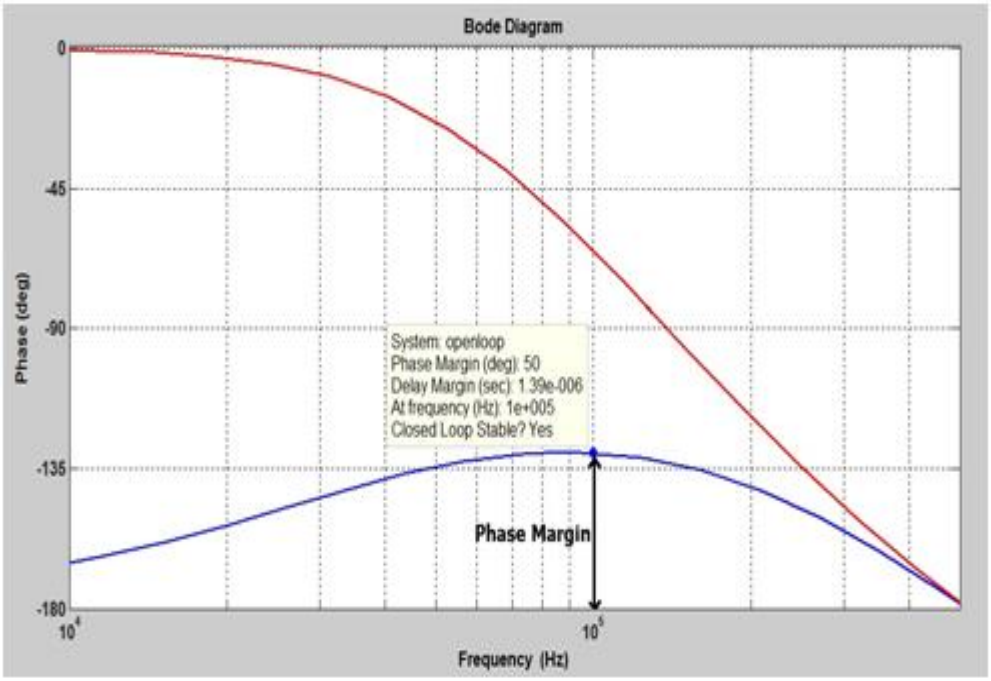
By using equation (4-1) the open-loop function for the proposed Frequency Synthesizer at 100 kHz bandwidth is:

$$A(s)=\frac{12.9*10^{10}(1+4.8*10^{-6}s)}{s^2.(1+4.07*10^{-7}s).(1+2.03*10^{-7}s)} \quad (4\text{-}12)$$

Figure (4-14) show the frequency response for proposed Frequency Synthesizer that contain third order loop filter at 100 kHz bandwidth and Phase margin =50˚ by using MATLAB.



(a)



(b)

Fig (4-14)(a) frequency response Magnitude for the proposed Frequency Synthesizer (b) frequency response Phase for the proposed frequency Synthesizer

Figure (4-14)(a) show that the operation of the proposed Frequency Synthesizer is at 100 kHz bandwidth and it is the same value that was selected in the design process. Also show that the frequency response Magnitude for the proposed Frequency Synthesizer that contain third order loop filter better than the frequency response Magnitude for the proposed Frequency Synthesizer that contain second order loop filter. This improving because of the additional pole (T3) for third order loop filter. This additional pole will reduce the level of Spurs noise and Phase noise.

Table 4-3 shows a close-loop comparison between the magnitude frequency response for proposed Frequency Synthesizer that contain third order loop filter and the magnitude frequency response for proposed Frequency Synthesizer that contain second order loop filter.

Frequency (MHz)	Closed Loop T.F Magnitude (dB)	
	Third Order Filter	Second Order Filter
1	-33	-31.4
5	-75	-60
10	-90.5	-71.3
100	-150	-111

Table 4-3

Table 4-3 show that the frequency response Magnitude for the proposed Frequency Synthesizer that contain third order loop filter better than the frequency response Magnitude for the proposed Frequency Synthesizer that contain second order loop filter where the improvement in the magnitude clearly appear at high frequencies better than at the low frequencies because of the additional pole (T3).

Figure (14-4) (b) show that the phase of open loop equal 130˚, the phase margin of the proposed Frequency Synthesizer equal 50˚ and it is the same value that was selected in the design process.

Figure (4-15) show simulation of the proposed Frequency Synthesizer the open loop gain and the close loop gain by using ADS

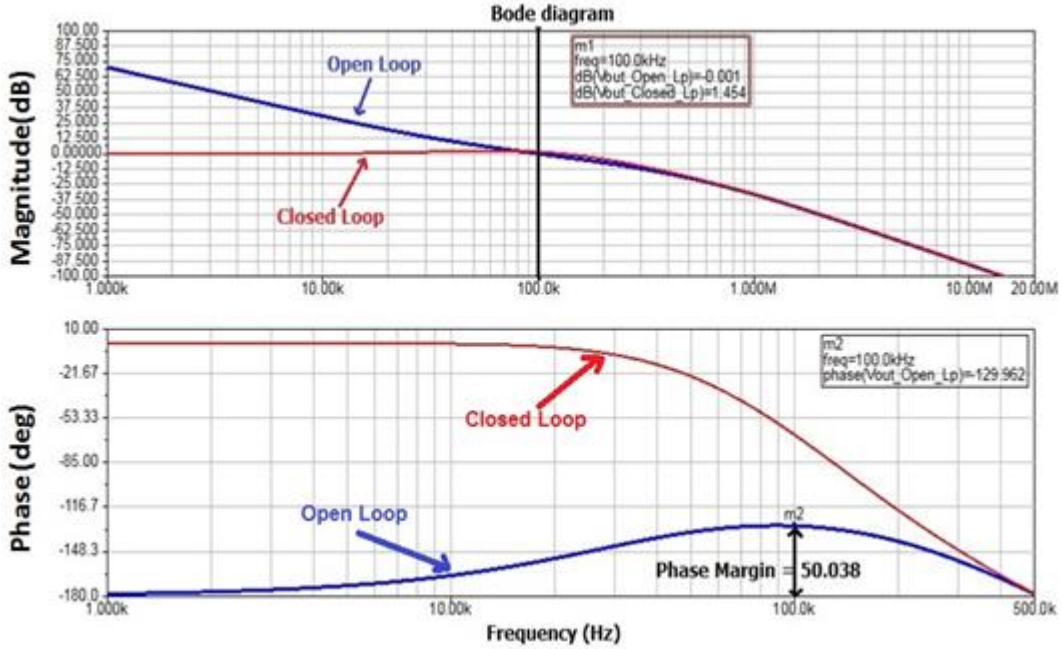


Fig (4-15) The simulation of the proposed Frequency Synthesizer the open loop gain and the close loop gain by using ADS

Figure (4-15) show that the operation of the Frequency Synthesizer at 100 kHz bandwidth and it is the same value that was obtained by using MATLAB. Also show that The results that obtained by using ADS were a little different to the results that have been obtained using MATLAB. Where the magnitude frequency response of the closed-loop gain was equal to 1.45 dB at a frequency of 100 KHz by using ADS while it is 1.34 dB by using MATLAB. While the phase of open loop equal 129.962˚,by using equation (4-5) the phase margin of the proposed Frequency Synthesizer equal 50.038˚ and it is approach to the value obtained by using MATLAB.

4.2.2.2 The simulation result of the proposed Frequency Synthesizer (Output spectrum, Phase noise , Settling time) at 100 kHz bandwidth

Figure (4-16) show the output spectrum of the proposed Frequency Synthesizer that consist of third order loop filter and first order Sigma Delta modulator at 100 kHz bandwidth

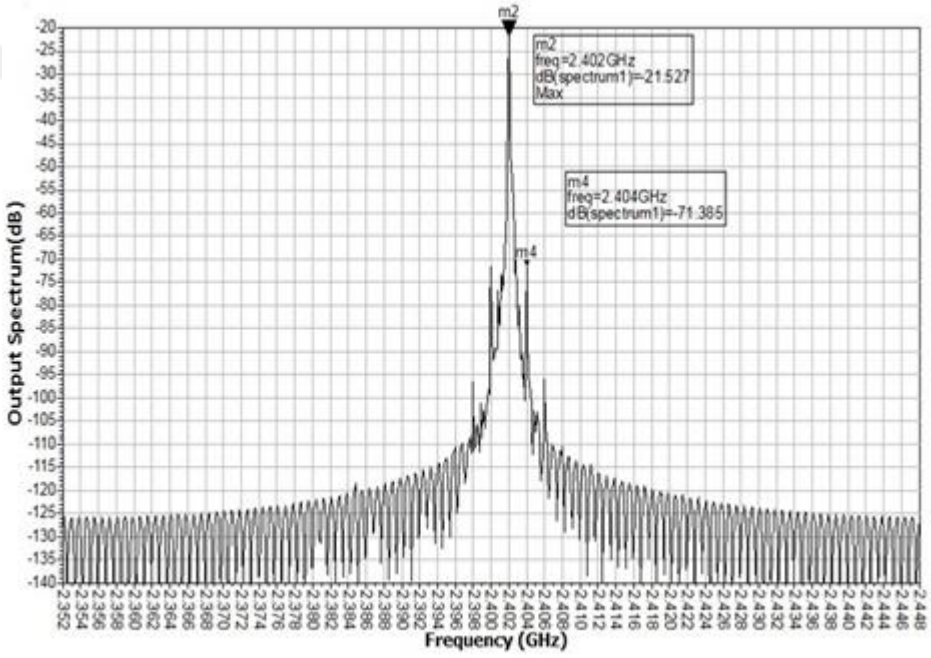


Fig (4-16) The output spectrum of the proposed frequency Synthesizer

Figure (4-16) show that the fractional Spurs noise level dramatically improved by using third order loop filter. where the level of first fractional spur noise equal -49.85 dBc while the level of first fractional spur noise equal -43.7 dBc for second order loop filter. As well as removing all fractional spur noise above 4

MHz. but the existing Spurs in the output spectrum is not acceptable in a Bluetooth applications. Figure (4-17) show the Phase noise of the proposed Frequency Synthesizer that consist of third order loop filter at 100 kHz bandwidth .

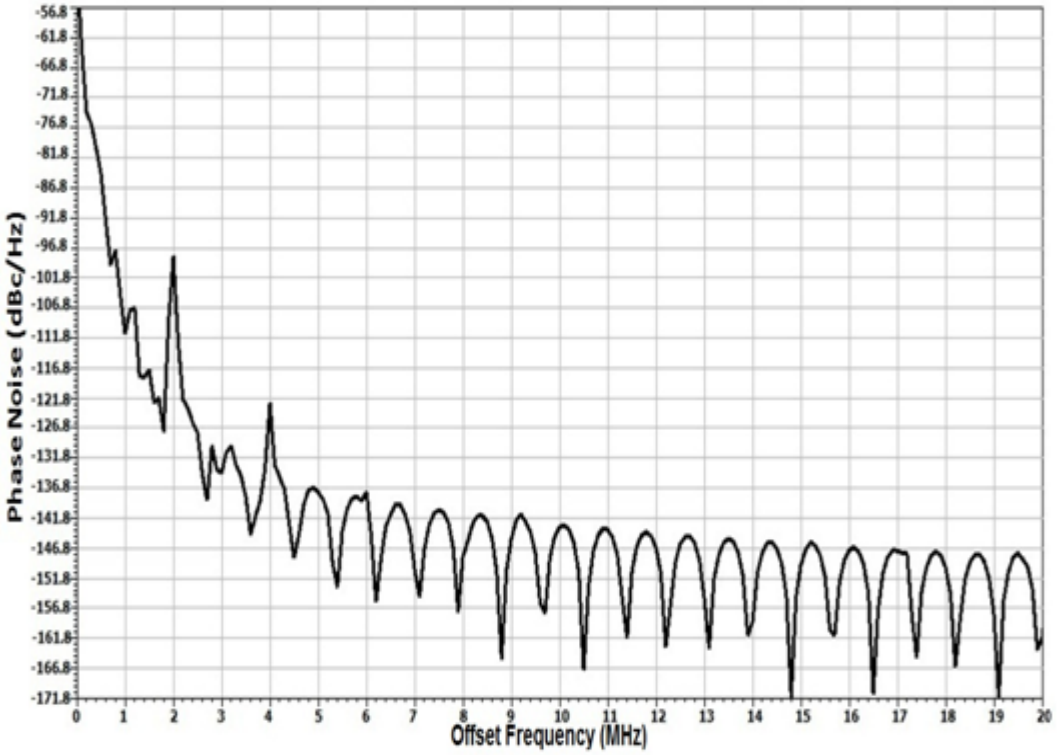


Fig (4-17) The Phase noise of the proposed frequency Synthesizer

Figure (4-17) show the phase noise level is improved by increasing the filter loop order for the proposed frequency Synthesizer. where the third order loop filter that use in design the proposed frequency Synthesizer provides better removal of Phase noise because of the additional pole (T3) ,but the proposed frequency Synthesizer not acceptable in a Bluetooth applications because of the high level Phase noise at 2MHz . figure (4-18) show the time and frequency of the Frequency Synthesizer

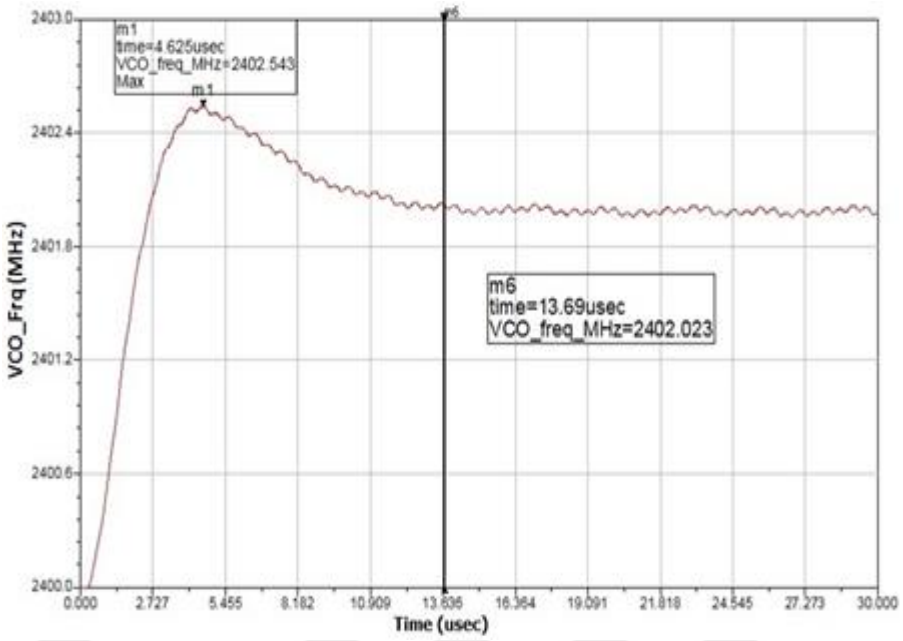


fig (4-18) The time and frequency of the Frequency Synthesizer

figure (4-18) show the settling time equal 13.69µsec and it is the same value that obtained by using second order loop filter, while the error in the output signal frequency equal 23 kHz. Where output signal frequency equal 2402.023 MHz. the obtained result show that when increase the loop filter order the fractional Spurs noise still exist in the output spectrum of the proposed Frequency Synthesizer and it is not acceptable in a Bluetooth applications. To get output spectrum free of any fractional Spurs noise the solution by Increasing Sigma Delta modulator order as follow.

4.2.3 Increasing Sigma Delta modulator order to get output spectrum free of any fractional Spurs noise

Figure (4-19) show the output of proposed second order single loop Sigma Delta modulator at input (5/48) where it consist from four level changed between -1 and 2 because there is two integrator. This change will be enough to not generate any Spurs noise in the output spectrum for the proposed Frequency Synthesizer. the output of Sigma Delta modulator represent the fractional part to be added to the correct part of the division ratio (125) to generate the required division ratio. Figure (4-20) show the required division ratio (125.104)

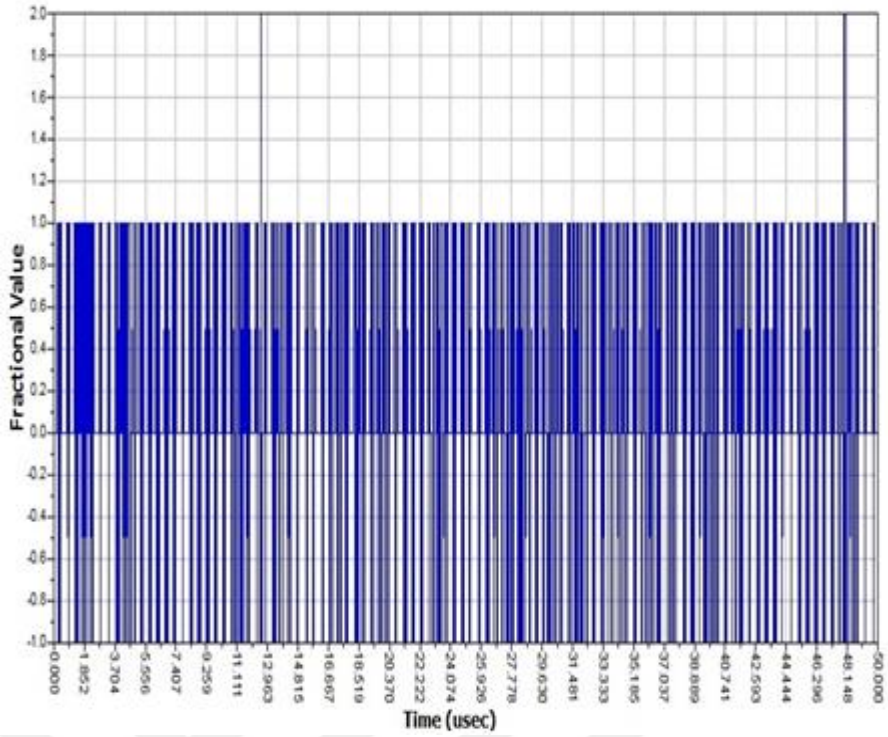


Fig (4-19) Sigma Delta modulator output

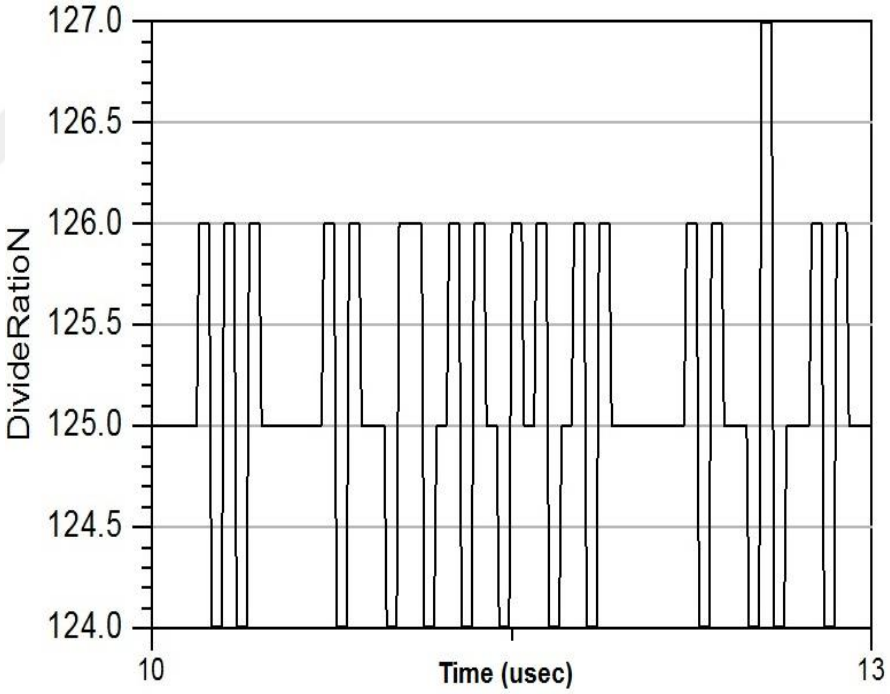


Fig (4-20) Total division ratio of the proposed Frequency Synthesizer

Figure (4-20) show that the division ratio randomly changed among 124, 125, 126 ,127 to generate the required division ratio (125.104). figure (4-21) show the output spectrum of Sigma Delta modulator

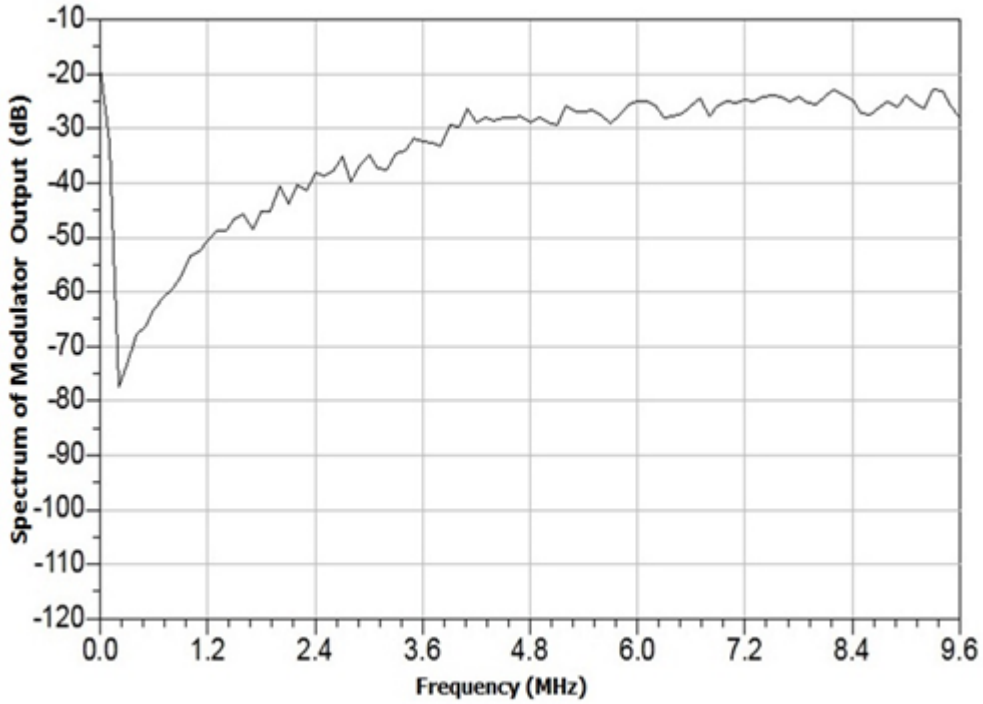


Fig (4-21) The output spectrum of Sigma Delta modulator

Figure (4-21) show that second order Sigma Delta modulator don't have any fractional Spursnoise .figure (4-22) show the output spectrum of the proposed Frequency Synthesizer that contain second order Sigma Delta modulator and second order loop filter at 100 kHz bandwidth , 50° Phase margin

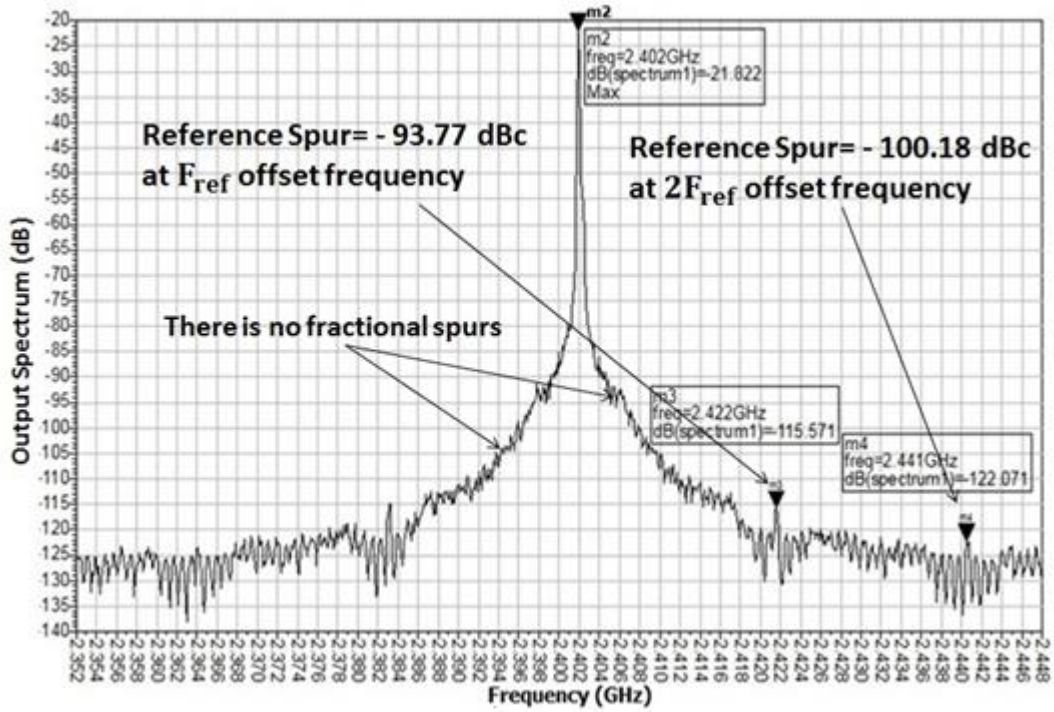


Fig (4-22) the output spectrum for the proposed Frequency Synthesizer

Figure (4-22) show that there is a significant improvement by using second order Sigma Delta modulator where the output spectrum for the proposed Frequency Synthesizer don't have any fractional Spurs noise also there isn't any Spurs noise caused by the second order Sigma Delta modulator but there is Reference Spurs noise because of the mismatch between the Charge Pump currents . where the level of Reference Spurs noise equal -93.77dBc at 19.2 MHz while it was equal -100.18 dBc at 38.4 MHz and it is acceptable value for Bluetooth application where the level of Reference Spurs noise must not exceed -49 dBc as shown in Table 3-2 . figure (4-23) show the Phase noise of the proposed Frequency Synthesizer that contain second order Sigma Delta modulator and second order loop filter at 100 kHz bandwidth.

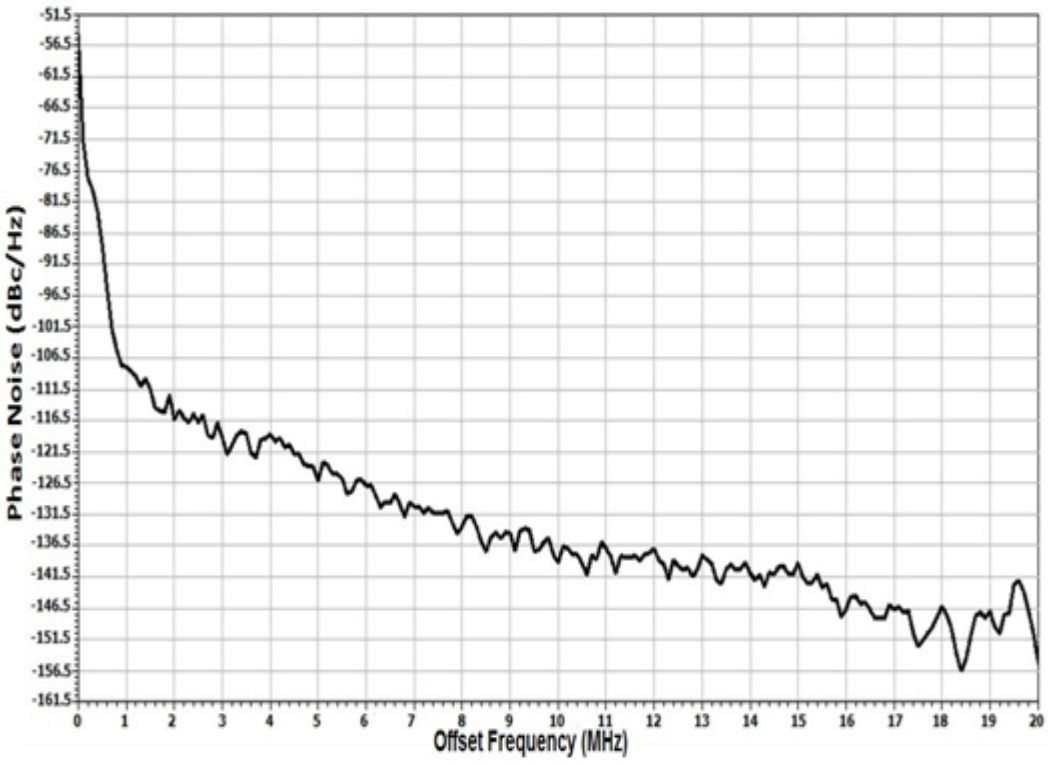


Fig (4-23) The Phase noise of the proposed Frequency Synthesizer

Figure (4-23) show that The Phase noise of the proposed Frequency Synthesizer dramatically improved where it do not contain any fractional Spurs noise at low frequencies. Table 4-4 Phase noise comparison between the proposed Frequency Synthesizer that contain second order Sigma Delta modulator and the proposed Frequency Synthesizer that contain first order Sigma Delta modulator.

Offset Frequency	Phase Noise (dBc/Hz) for Frequency Synthesizer with	
	2nd order Sigma-Delta Modulator	**1st order Sigma-Delta Modulator**
200 KHz	-78.5	-74.5
400 KHz	-84.5	-80.8
600KHz	-95	-91.5
800KHz	-105.5	-97
2 MHz	-116.5	-91.8
3 MHz	-119.5	-130.8
5 MHz	-126.5	-138.8
7 MHz	-130.5	-147

Table 4-4

Table 4-4 show that the Phase noise the proposed Frequency Synthesizer that contain second order Sigma Delta modulator is better than the Phase noise the proposed Frequency Synthesizer that contain first order Sigma Delta modulator at low frequencies and acceptable in Bluetooth application where the Phase noise must not exceed -110 dBc/Hz at 2 MHz Frequency Offset and -119 dBc/Hz at 3 MHz Frequency Offset as shown in Table 3-2. While the Phase noise the proposed Frequency Synthesizer equal -116.5dBc/Hz at 2 MHz Frequency Offset and -119.5 dBc/Hz at 3 MHz Frequency Offset. But increasing the Sigma Delta modulator order mean increasing in the Phase noise at high frequency because of that the order of the loop filter must be higher than the order of Sigma Delta modulator so the loop filter reduce the Phase noise at high frequency.

Figure (4-24) show the time and frequency of the Frequency Synthesizer

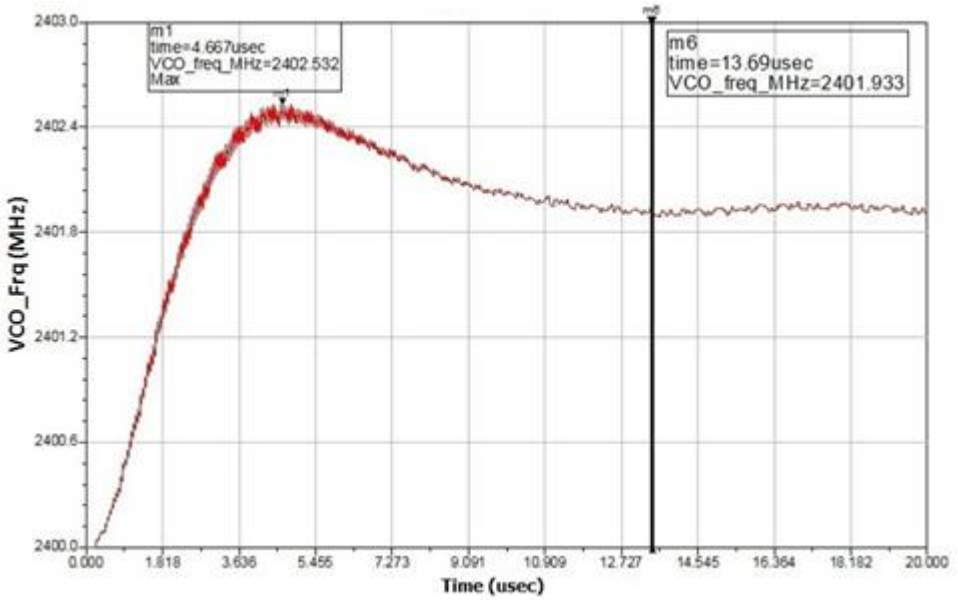


Fig (4-24) The time and frequency of the Frequency Synthesizer

Figure (4-24) show that the output signal frequency equal 2401.933 MHz at 13.69 µsec and it is acceptable value for Bluetooth applicationthis figure also show that the frequency resolution a little bit decrease where the error in the output signal frequency equal 67 kHz while it was 19 KHz the proposed Frequency Synthesizer that contain first order Sigma Delta modulator. The deceasing in the frequency resolution is because of the level change of the output of second order modulator larger than the level change of the output of first order modulator because there is tow integrators in second order modulator. The obtained result show that when increase the modulator order there is a significant improvement in the level of Spurs noise and Phase noise but increasing the phase noise at high frequencies , reduce the frequency resolution of the output signal and there is Reference Spurs noise in the output spectrum of the proposed Frequency Synthesizer.

4.2.3.1 Increase the Phase Margin to improve frequency resolution of the output signal and to reduce the settling time for proposed Frequency Synthesizer that contain second order Sigma- Delta and second order loop filter

Figure 25-4 shows the output signal frequency and the time of proposed frequency synthesizer with second order sigma- delta modulator and second order loop filter at 60° phase margin.

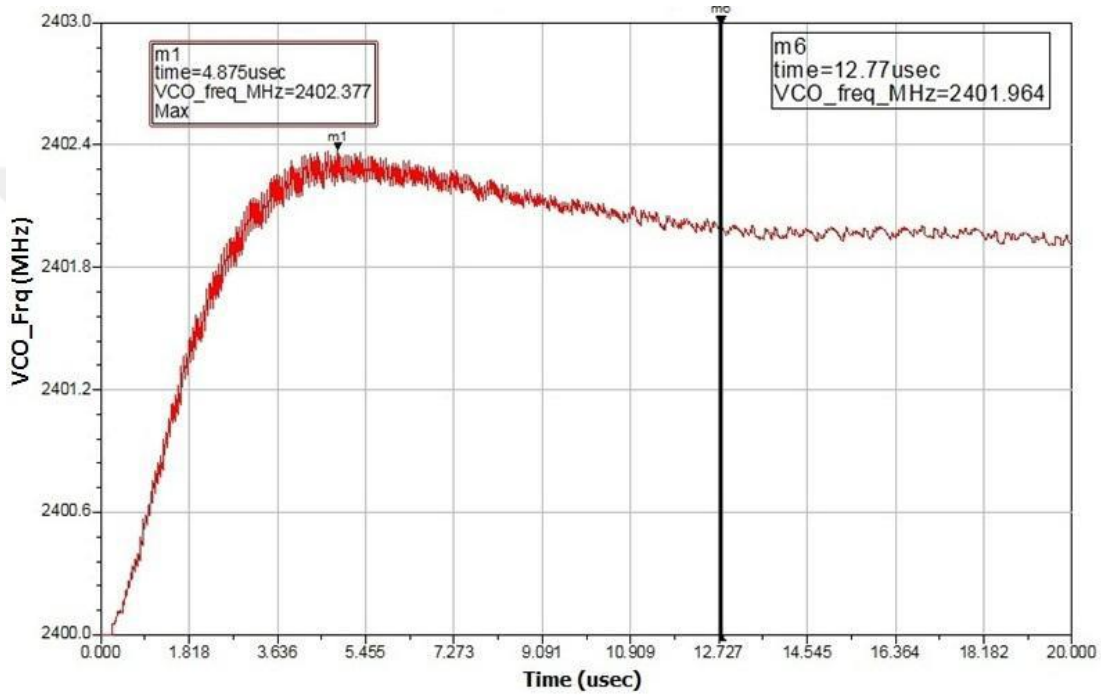


Fig (4-25) The time and frequency of the Frequency Synthesizer

Figure (4-25) show that increasing the Phase margin to 60˚ lead to improve the settling time and the frequency resolution of the output signal where the output signal frequency equal 2401.964 MHz at 12.77 µsec. where the error of output signal equal 36 KHz while it was equal 67 KHz at 50˚ phase margin. Figure (4-26) show the ouput spectrum of the Frequency Synthesizer that contain second order Sigma Delta modulator and second order loop filter at 60˚ phase margin.

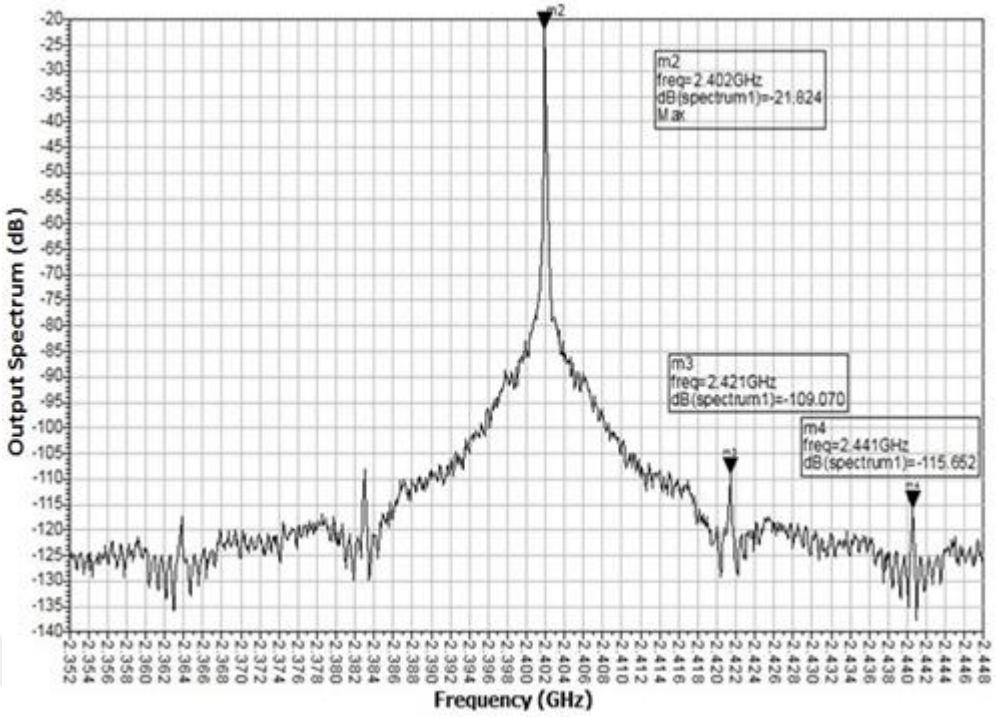


Fig (4-26) the output spectrum for the proposed Frequency Synthesizer

Figure (4-26) show the increasing the phase margin lead to increase the Reference Spurs noise level where first Reference Spurs noise level equal -87.2 dBc while second Reference Spurs noise level equal -93.83 dBc this values is acceptable in Bluetooth application . the increasing in Spurs noise level caused by the pole (T1) that moved toward the high frequencies where the pole (T1) equal $4.26*10^{-7}$s at 60° Phase margin while it equal $5.79*10^{-7}$s at 60° Phase margin. The movement of the pole (T1) lead to increase the frequency response magnitude at high frequencies therefore the Spurs noise level will increase.

The obtained result show that the increasing in the phase margin the proposed Frequency Synthesizer lead to improve the settling time and the frequency resolution of the output signal but the Spurs noise level in the output spectrum will increased.

4.2.4 Increasing the loop filter order to remove the Reference Spurs noise level, improve the frequency resolution of the output signal and reduce the Phase noise that is caused by second order Sigma Delta Modulator

Figure (4-27) show the output spectrum for the proposed Frequency Synthesizer that contain third order loop filter and second order Sigma Delta modulator

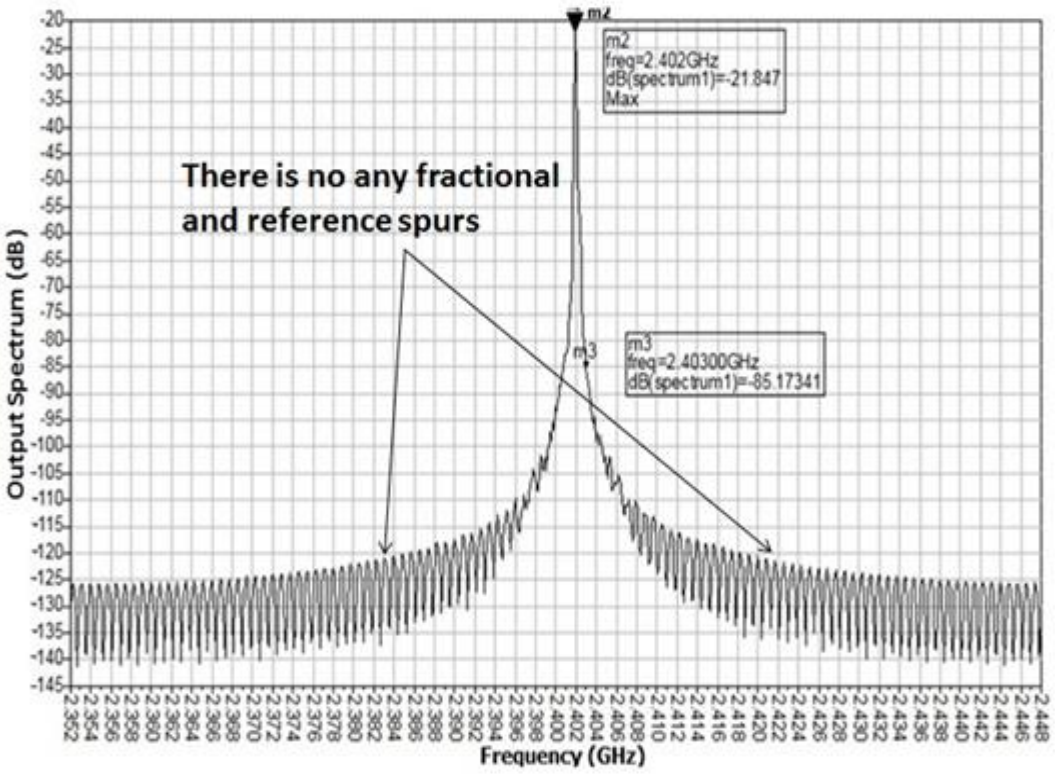


Fig (4-27) The output spectrum the proposed Frequency Synthesizer

Figure (4-27) show that there is no any fractional and reference spurs in the output spectrum of the proposed Frequency Synthesizer because of the third order loop filter remove it.

Figure (4-28) show the Phase noise for the proposed Frequency Synthesizer that contain third order loop filter and second order Sigma Delta modulator.

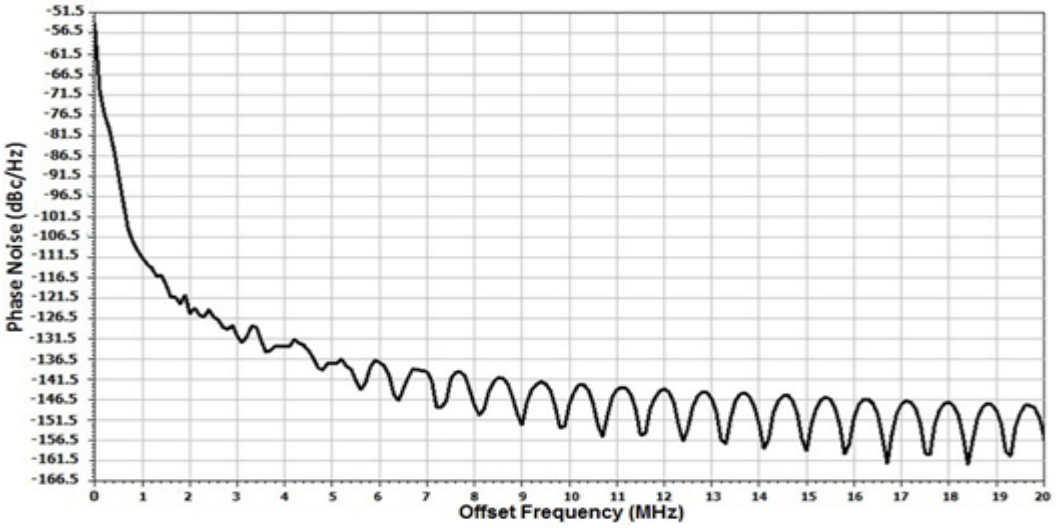


Fig (4-28) The Phase noise for the proposed Frequency Synthesizer

Figure (4-28) show that the Phase noise level decreased at high frequencies because of the additional pole for third order loop filter. Table 4-5 show the Phase noise comparison between the proposed Frequency Synthesizer that contain third order loop filter and the proposed Frequency Synthesizer that contain second order loop filter.

Offset Frequency	**Phase Noise (dBc/Hz) for Frequency Synthesizer with**	
	3rd Order Filter	**2nd Order Filter**
600 KHz	-101.5	-96.5
800 KHz	-108.5	-105.5
1 MHz	-111.5	-108.5
2 MHz	-125.5	-116.5
3 MHz	-131.5	-119.5
4 MHz	-133.5	-118.5
5 MHz	-137.5	-126.5

Table 4-5

Table 4-5 show that the Phase noise level for the proposed Frequency Synthesizer that contain third order loop filter dramatically improved at high frequencies but the improvement is less at low frequencies because of the position of the additional pole. Also show that the Phase noise level is good and

acceptable for Bluetooth applications where the Phase noise must not exceed -110 dBc/Hz at 2 MHz Frequency Offset and -119 dBc/Hz at 3 MHz Frequency Offset as shown in Table 3-2. While the Phase noise the proposed Frequency Synthesizer equal -125.5dBc/Hz at 2 MHz Frequency Offset and -131.5 dBc/Hz at 3 MHz Frequency Offset. Figure (4-29) shows the output signal frequency and the time of proposed frequency synthesizer with second order sigma- delta modulator and third order loop filter

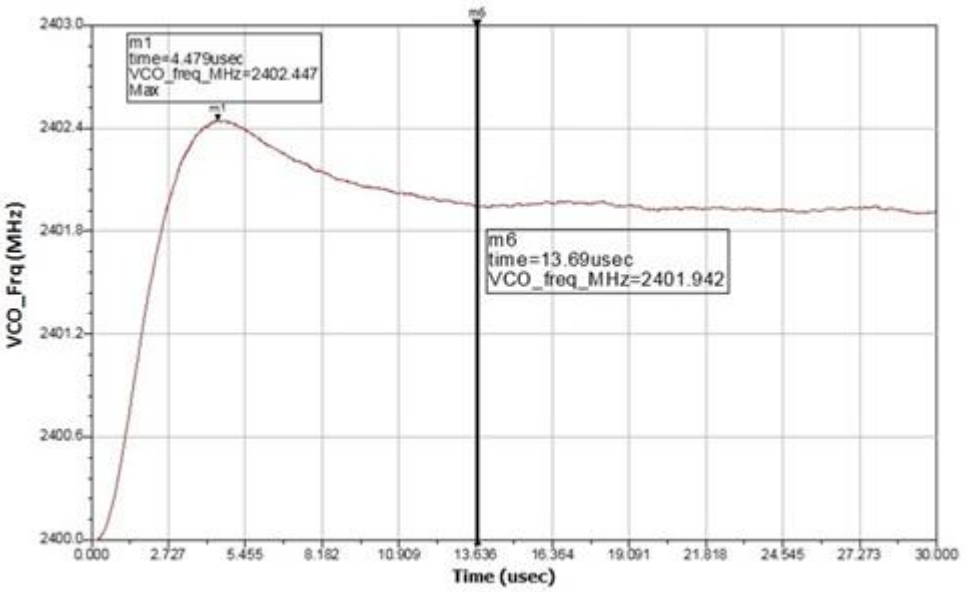


Fig (4-29) The time and frequency of the Frequency Synthesizer

Figure (4-29) show that the frequency resolution of the output signal is improved by increasing the order of the loop filter, where the output signal frequency equal 2401.942 MHz at 13.69 µsec. where the error of output signal equal 58 KHz while it was equal 67 KHz for the second order of the loop filter. It should be noted that the current design is one of the best proposed designs because it provide lower Phase noise level and spurs noise level lower settling time and good frequency resolution.

4.2.5 Using third order single loop Sigma Delta modulator to reduce the Phase noise of the proposed Frequency Synthesizer at low frequencies

Figure (4-30) show the output of third order Sigma Delta modulator when the input value equal (5/48).

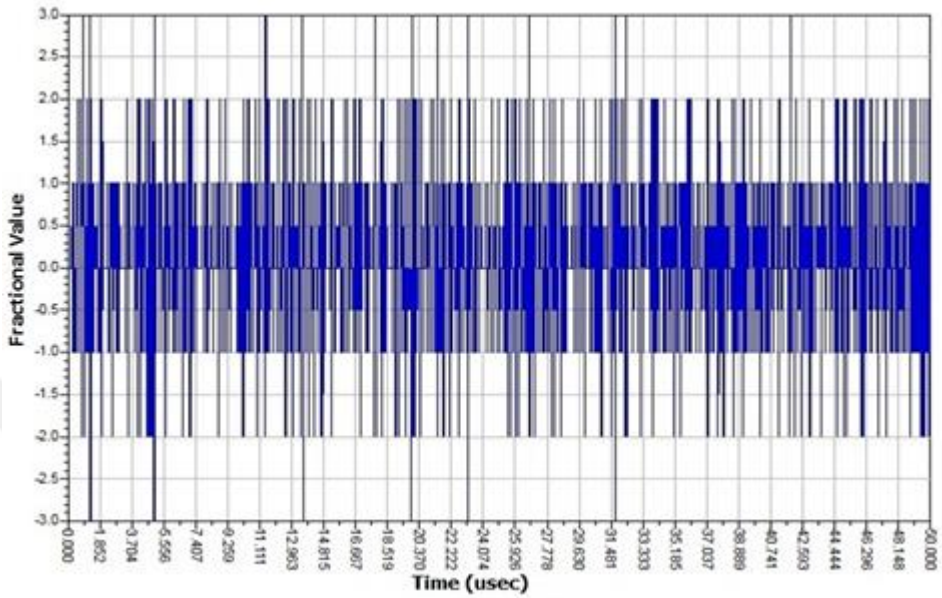


Fig (4-30) The output of third order Sigma Delta modulator

Figure (4-30) show that the output of third order Sigma Delta modulator consist of seven levels that changed among 3 and -3 while second order Sigma Delta modulator consist of four levels. Increasing the level of the output Sigma Delta modulator leads to reduce the Phase noise at low frequencies but increase it at high frequencies. the output of Sigma Delta modulator represent the fractional part to be added to the correct part of the division ratio (125) to generate the required division ratio.

Figure (4-31) show the required division ratio (125.104).

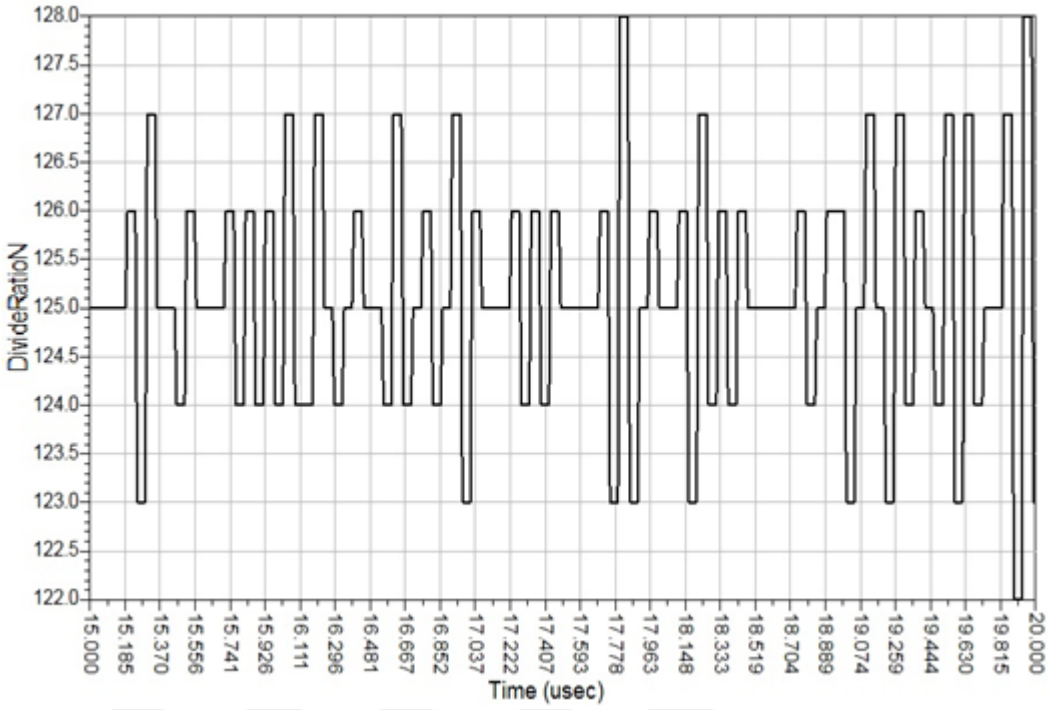


Fig (4-31) Total division ratio (125.104).

Figure (4-31) show that the division ratio level randomly changed among 122, 123,124,125,126,127,128 to generate the required division ratio (125.104). figure (4-32) the output spectrum of third order Sigma Delta modulator

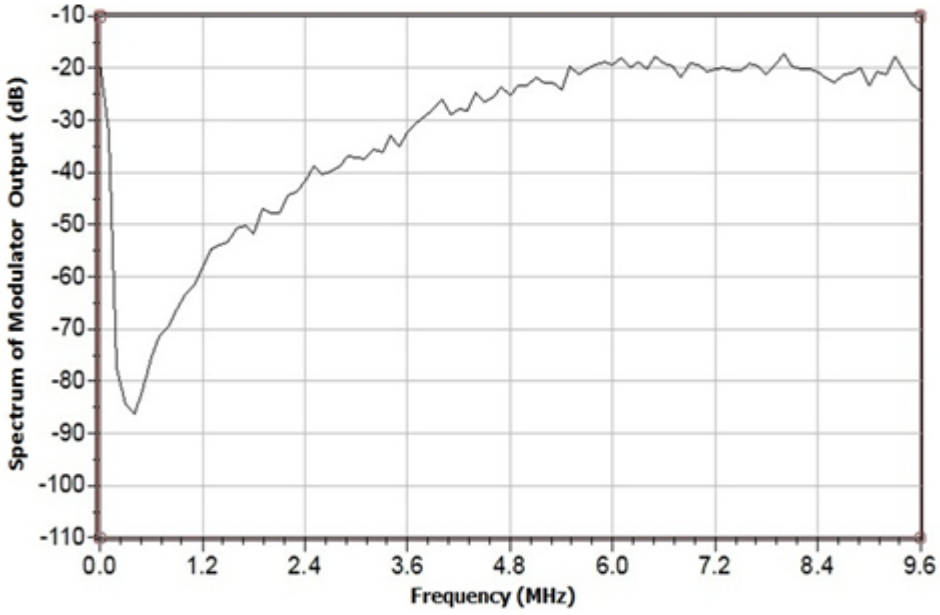


Fig (4-32) The output spectrum of third order Sigma Delta modulator

Figure (4-32) show that increasing Sigma Delta modulator order leads to reduce the noise at low frequencies that mean reduce the Phase noise for the proposed Frequency Synthesizer at low frequencies but also lead to increase the noise at high frequencies therefore the Phase noise for the proposed Frequency Synthesizer at high frequencies will increases because of that fourth order loop filter will used to reduce the Phase noise at high frequencies. Figure (4-33) show the Phase noise for the proposed Frequency Synthesizer that contain third order Sigma Delta modulator and fourth order loop filter at 100 kHz bandwidth and 50˚ Phase margin.

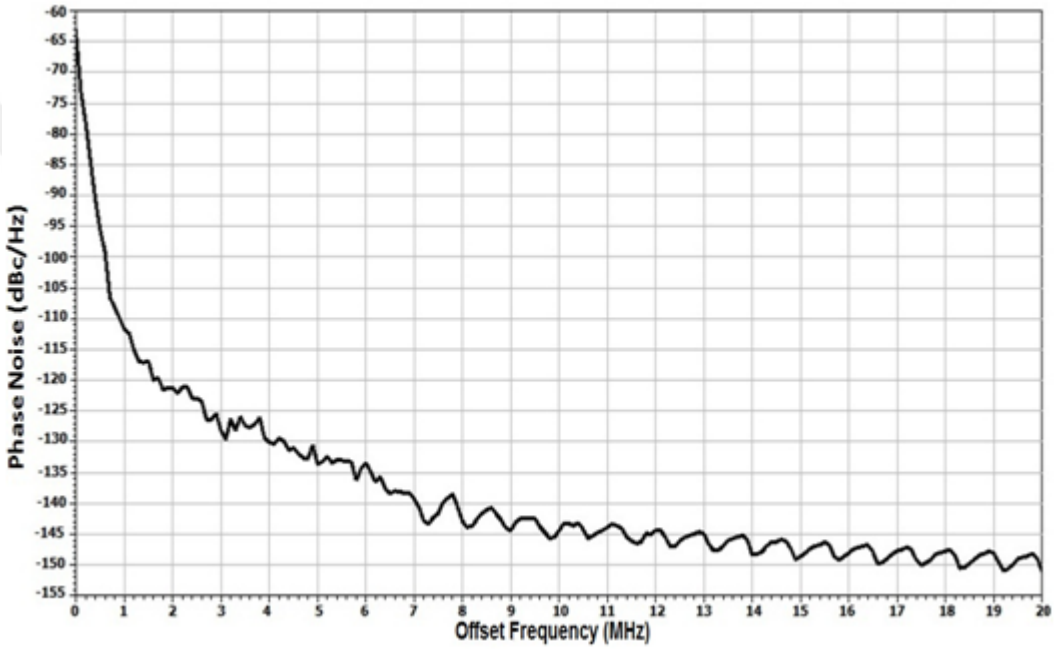


Fig (4-33) The Phase noise for the proposed Frequency Synthesizer

Figure (4-33) show that the Phase noise improved at low frequencies because of using third order Sigma Delta modulator instead of using second order Sigma Delta modulator. While the Phase noise at high frequencies is removed by using fourth order loop filter. Table 4-6 show the Phase noise comparison between for the proposed Frequency Synthesizer that contain (third order Sigma Delta modulator and fourth order loop filter) with the proposed Frequency Synthesizer that contain (second order Sigma Delta modulator and third order loop filter) at 100 kHz bandwidth and 50˚ Phase margin.

Offset Frequency	Phase Noise (dBc/Hz) for Frequency Synthesizer with	
	4th Order Filter and 3rd order Sigma-Delta Modulator	**3rd Order Filter and 2nd order Sigma-Delta Modulator**
100 KHz	-75	-72.5
200 KHz	-82	-78.5
300KHz	-87	-81.5
400KHz	-93	-85.5
500KHz	-95	-93.5
600KHz	-101	-98.5
700KHz	-107	-106
800 KHz	-109	-108.5
900 KHz	-111	-110.5
1 MHz	-112	-111.5

Table 4-6

Table 4-6 show that the phase noise for the proposed Frequency Synthesizer that contain (third order Sigma Delta modulator and fourth order loop filter) is better than the Phase noise the proposed Frequency Synthesizer that contain (second order Sigma Delta modulator and third order loop filter) at low frequencies specially at 300 kHz and 400 kHz.

Figure (4-34) shows the output signal frequency and the time of proposed frequency synthesizer with third order sigma- delta modulator and fourth order loop filter.

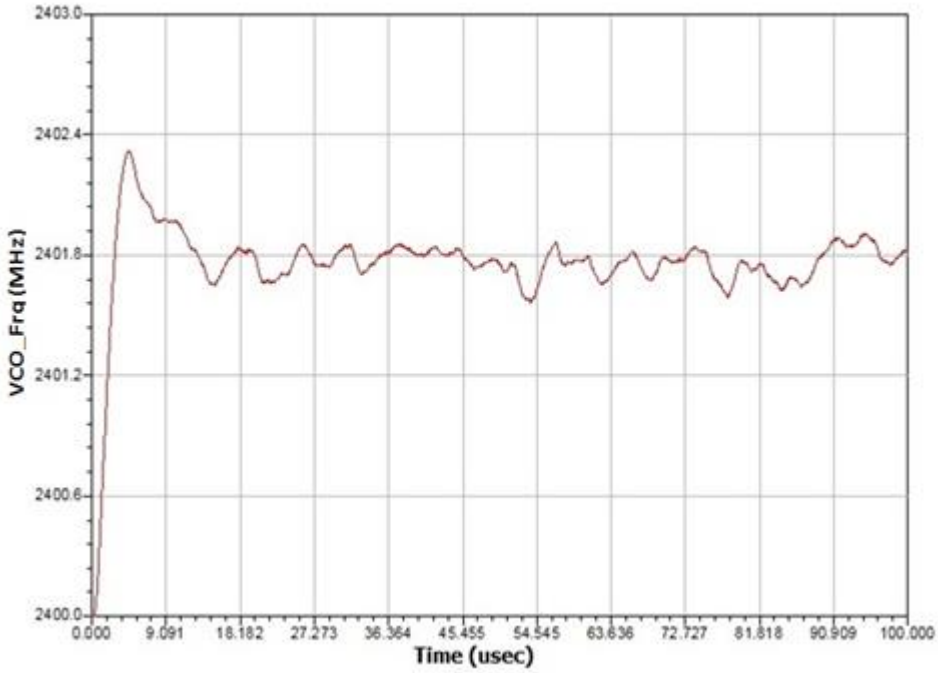


Fig (4-34) The time and frequency of the Frequency Synthesizer

Figure (4-34) show the frequency resolution of the output signal for the Frequency Synthesizer not good and it is not acceptable for Bluetooth application. Where the error in output signal frequency equal 240 kHz .the increasing the order of Sigma Delta modulator Also require increasing the order of the loop filter therefore increasing the complexity of the design.

Table 4-7 the error comparison in the output signal for all proposed Frequency Synthesizers.

Frequency Synthesizer with	**Output Frequency (MHz)**	**Accuracy (Frequency error)**
1st order sigma-delta modulator and 2nd order filter with B.W= 150 KHz and phase margin= 50°	2402.046	46 KHz
1st order sigma-delta modulator and 2nd order filter with B.W= 100 KHz and phase margin= 50°	2401.981	19 KHz
1st order sigma-delta modulator and 3rd order filter with B.W= 100 KHz and phase margin= 50°	2402.023	23 KHz
2nd order sigma-delta modulator and 2nd order filter with B.W= 100 KHz and phase margin= 50°	2401.933	67 KHz
2nd order sigma-delta modulator and 2nd order filter with B.W= 100 KHz and phase margin= 60°	2401.964	36 KHz
2nd order sigma-delta modulator and 3rd order filter with B.W= 100 KHz and phase margin= 50°	2401.942	58 KHz
3rd order sigma-delta modulator and 4thorder filter with B.W= 100 KHz and phase margin= 50°	2401.760	240 KHz

Table 4-7

Table 4-7 show that the error in the output signal frequency increase by increasing the order of Sigma Delta modulator while it decrease by increasing the order of the loop filter. This Table also show that the error in the output signal frequency for all proposed Frequency Synthesizers are good and acceptable for Bluetooth applications except the last proposed Frequency

Synthesizer where the error in the output signal frequency dramatically increase by increasing the modulator to the third order.

Table 4-8 show comparison between the result that is obtained in this chapter and the result of Previous research. Where Table 4-8 show that the all result dramatically identical to specifications and requirements of designing the Frequency Synthesizer of Bluetooth Systems .in addition this proposed Frequency Synthesizer is free from any spurs noise (fractional or reference) in the output spectrum while the output spectrum in the Previous research contain spurs noise. Where the Phase noise equal -131.5 dBc/Hz at 3 MHz frequency offset and it is good result compared to previous research . The settling time which was obtained is better than the settling time that obtained by [Wrong, 2002] at same bandwidth.

Parameter/ References	**Bluetooth requirements**	**[**Wong, 2002**]**	**[** Kevin J. 2008**]**	**[** N. Fatahi, 2010**]**	**This work**
Output frequency	2.402 to 2.480 GHz	2.4 GHz	2.4 GHz	900 MHz	2.4 GHz
Input frequency (MHz)	13,19.2,20,26, 39.2,40	18	12	8	19.2
Bandwidth (KHz)	N/A	100	975	40	100
Phase noise (dBc/Hz)	-110 dBc/Hz @ 2 MHz, -119 dBc/Hz @ 3 MHz	-92.5 @ 500 KHz	-121 @ 3 MHz	-135 @ 3 MHz	-101.5@ 600 KHz, -125.5 dBc/Hz @ 2 MHz, -131.5 @ 3 MHz
Spurs noise (dBc)	≤ -49	-51	-70	-96	Free
Switching time (µsec)	≤ 220	55	N/A	N/A	13.69

Table 4-8

5. CONCLUSION

This thesis includes the study and design fractional frequency synthesizer by using Sigma Delta modulator at Bluetooth frequency . the proposed frequency synthesizer operate at 100 kHz bandwidth and 50˚ phase margin .Sigma Delta modulator provide a good performance to reduce the noise generated by the fractional frequency synthesizer where first ,second and third order single loop sigma Delta modulator and second , third and fourth loop also used in the proposed design To reduce the high noise generated from Sigma Delta modulator at high frequencies Depending on the results obtained there are several conclusions reached by the research is:

1- The Phase locked loop technique was very effective for frequency synthesizer. because of facility and simplicity in generating good accuracy at bluetooth system frequency .
2- Reducing the bandwidth lead to improve fractional spurs noise level and Phase noise level . where the improvement in spurs noise equal 7 dBc while the improvement in the Phase noise equal 4 dBc/Hz but increasing the settling time by 4.69 μsec.
3- Increasing loop filter order from second order to third order lead to improve fractional spurs noise level by 6 dBc and remove reference spurs noise in the output spectrum of frequency synthesizer.
4- Increasing loop filter order to third order lead to improve Phase noise level for the proposed frequency synthesizer specially at high frequencies .where the Phase noise reduced by 11 dBc/Hz at high frequencies.
5- Increasing loop filter order lead to improve the error of the output signal frequency by 10 KHz.
6- Increasing the Sigma Delta modulator order from first order to second order lead to remove fractional spurs noise of output spectrum of the proposed frequency synthesizer also improve the Phase noise at low frequencies by 3 dBc/Hz.
7- Increasing the Sigma Delta modulator order from second order to third order lead to improve Phase noise level at low frequencies by 7 dBc/Hz.

8- Increasing the Sigma Delta modulator order lead to reduce frequency resolution of the output signal for the frequency synthesizer. where the error in the output signal frequency increase by 48 kHz while the frequency resolution dramatically decreased when using third order Sigma Delta modulator for this reason the frequency synthesizer that contain third order Sigma Delta modulator Can not be used in Bluetooth application .

9- Increasing the Phase Margin for the proposed frequency resolution lead to improve the settling time and the frequency resolution of the output signal .where the error in the output signal frequency decreased by 30 kHz while the settling time improved by 1 μsec.

10- The position and level of spurs noise (fractional and reference) could be controlled by the frequency of the input signal F_{ref} .as shown from the result in chapter four the position of spurs noise depend on input signal frequency . if the input signal frequency increase then the spurs noise will moved toward the high frequencies to be removed by the loop filter. but increasing input signal frequency lead to reduce the frequency resolution of the output signal for the proposed frequency synthesizer.

Appendix(A)

Third order loop filter design equations:

$$C1=\frac{A2}{T2^2}.\{1+\sqrt{1+(T2.A0-A1).\frac{T2}{A2}}\} \quad \text{(A-1)}$$

$$C3=\frac{-T2^2.C1^2+T2.A1.C1-A2.A0}{T2^2.C1-A2} \quad \text{(A-2)}$$

$$C2= A0-C1-C3 \quad \text{(A-3)}$$

$$R2= \frac{A2}{C1.C3.T2} \quad \text{(A-4)}$$

Where

$$T1\approx\frac{\sec(\emptyset)-\tan(\emptyset)}{\omega c(1+T31)} \quad \text{(A-5)}$$

$$T2=\frac{\gamma}{\omega c^2.(T1+T3)} \quad \text{(A-6)}$$

$$T3= T1.T3 \quad \text{(A-7)}$$

$$A0=\frac{K_{\emptyset}.K_{vco}}{N.\omega c^2}*\sqrt{\frac{(1+\omega c^2.T2^2)}{(1+wc^2.T1^2).(1+\omega c^2.T3^2)}} \quad \text{(A-8)}$$

$$A1= A0(T1+T3) = T2.C1-\frac{A2.A0}{T2.C1}-\frac{A2.C3}{T2.C1} \quad \text{(A-9)}$$

$$A2= A0.T1.T3= C1.C2.R1.C3.R2 \quad \text{(A-10)}$$

Appendix (B)

Fourth order loop filter design equations

$$C1 = \frac{a2}{T2^2}\left(1+\sqrt{\left(1+\frac{T2}{a2}\right).(T2.A0 - a1)}\right) \quad \text{(B-1)}$$

$$C2 = \frac{-b+\sqrt{b^2-4.a.c}}{2.a} \quad \text{(B-2)}$$

$$C3 = \frac{T2.A3.C1}{R2.[k0.T2.A3.C1 - C2.(A3.R2(T2.C1)^2]} \quad \text{(B-3)}$$

$$C4 = A0\text{-}C1\text{-}C2\text{-}C3 \quad \text{(B-4)}$$

$$R2 = \frac{a2}{(C1.c3.T2)} \quad \text{(B-5)}$$

$$R3 = \frac{A3}{T2.R2.C1.C3.C4} \quad \text{(B-6)}$$

Where

$$a2 = A0.T1.T3 \quad \text{(B-7)}$$

$$a1 = A0(T1+T3) \quad \text{(B-8)}$$

$$b = T2 + R2.(C1\text{-}A0) + \left(\frac{A3}{T2.C1}\right).\left(\frac{1}{T2} - k0\right) \quad \text{(B-9)}$$

$$a = \frac{A3}{(T2.C1)^2} \quad \text{(B-10)}$$

$$c = k1\text{-}\frac{ko.A3}{T2} \quad \text{(B-11)}$$

$$k0 = \left(\frac{A2}{C1}\right) - \left(\frac{1}{T2}\right) - \left(\frac{(A0-C1).T2.R2.C1)}{A3}\right. \quad \text{(B-12)}$$

$$c3 = \frac{T2.a1.C1 - a2.A0.(T2.C1)^2}{T2^2.C1 - a2} \quad \text{(B-13)}$$

$$k1 = \frac{A1-(T2.A0)-A3}{(T2.R2.C1) - ((A0-C1).R2.C1)} \quad \text{(B-14)}$$

$$T2 = \frac{\gamma}{\omega c^2.(T1 + T3+T4)} \quad \text{(B-15)}$$

$$T3 = T1.T31 \quad \text{(B-16)}$$

$$T4 = T1.T31.T43 \quad \text{(B-17)}$$

$$A3 = C1.C2.C3.C4.R1.R2.R3(\text{loop filter coefficient}) \quad \text{(B-18)}$$

$$A2 = C1.C2.R1.R2(\ C3 + C4\ ) + C4.R3(C2.C3.R2 + C1.C3.R2 + C1.C2.R1 + C2.C3.R1) \quad \text{(B-19)}$$

$$A1 = C2.R1.(C1+C2+C3)+R2.(C1+C2).(C3+C4) + C4.R3(C1+C2+C3) \quad \text{(B-20)}$$

$$A0 = C1+C2+C3+C4 \quad \text{(B-21)}$$

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