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Design und Implementierung eines Time-to-Digital Wandlers für digitale Silicon Photomultipliers

Design and Implementation of a Time-to-Digital Converter for digital Silicon Photomultipliers

Master Thesis

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M139

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Acronyms

A-SiPM	Analog Silicon Photomultiplier
ADC	analog-to-digital converter
CTR	coincidence time resolution
D-SiPM	Digital Silicon Photomultiplier
DAC	Digital-to-analog converter
DFF	D flip-flop
DNL	Differential Nonlinearity
FWHM	full width at half maximum
GRO	Gated Ring Oscillator
HDL	Hardware Description Language
HEP	High Energy Physics
I/O	input-output
INL	Integral Nonlinearity
LCU	Logic Control Unit
LSB	least significant bit
MD-SiPM	Multi-Channel Digital Silicon Photomultiplier
PET	Positron Emission Tomography
PSS	Periodic steady state
PVT	Process, voltage, and temperature
RO	Ring Oscillator
RSD	Relative standard deviation
SiPM	Silicon Photomultiplier
SNR	signal-to-noise ratio

SPAD Single Photon Avalanche Diode
TDC Time-to-Digital Converter
ToF Time-of-Flight



1 Introduction

Time-of-Flight (ToF) measurements are used in applications such as High Energy Physics (HEP) and Positron Emission Tomography (PET). Performance of a ToF measurement, such as its resolution and precision, is a determining factor in the overall performance of these applications. There is an increasing demand especially for a new generation of PET scanners with higher sensitivity. If the 500 ps coincidence time resolution (CTR) performance of contemporary PET scanners can be reduced to levels below 100 ps, this will be a game changer for the future of medical molecular imaging [2]. This technological improvement will result in much higher signal-to-noise ratio (SNR) values for the captured images and, therefore, the radiation dose injected to a patient can be drastically reduced, opening the way for PET scans to be used on new group of patients such as children and pregnant women [2]. In order to reach this goal, the performance of each component in the detector chain of a PET scanner needs to be improved, namely, scintillators, photodetectors and electronics.

Silicon Photomultiplier (SiPM) is a leading photodetector device that can be used in the above-mentioned detection chain, whereas a Time-to-Digital Converter (TDC) is an essential electronics component that lies in the end of the ToF measurement process. Integration of a TDC in each cell of a SiPM has recently emerged as a promising configuration which offers performance improvements. The suitable TDC is required to have high resolution, high precision, compact size and low power consumption in order to achieve the intended improvements. This thesis deals with the design and implementation of such a TDC which will be used for a SiPM. The design is implemented in a 28 nm technology.

In the first chapter, fundamental information is provided about the terms and concepts discussed throughout the thesis. In the next chapter, the specifications of the TDC is

presented, and the design and implementation process is explained in detail. In the third chapter, the results of the simulations performed on the TDC are presented and the performance is summarized. The thesis is concluded with final remarks and the outlook.



2 Fundamentals

This chapter begins with sections related to ToF, PET and SiPM. These are helpful in regards to understanding the motivation of the work. Then, fundamental information about the TDC is provided, including its performance parameters. Finally, available TDC architectures for SiPM applications are presented with possible advantages and drawbacks for each.

2.1 Time of Flight Measurements

ToF specifies the measurement of the time taken by an object, particle or a wave to travel through a medium. Improving the performance of existing ToF measurement techniques by achieving low timing uncertainty (timing resolution) has emerged as a promising research area for advancement in applications such as HEP and PET [1].

2.1.1 Positron Emission Tomography

PET is a medical imaging technique which can display metabolic functions in a patient's body. The operation mechanism of PET is illustrated in Figure 2.1 and can be briefly summarized as follows:

1. A radioactive compound of positron-emitter type, called tracer, is injected in the patient and binds to the targeted tissue.
2. Positron emitted by the tracer annihilates with an electron, resulting in further emission of two back-to-back γ photons of 511 keV.

3. γ photons are converted to large number of optical and ultraviolet ones by scintillation and these secondary photons are subsequently detected by photodetectors, such as a SiPM.

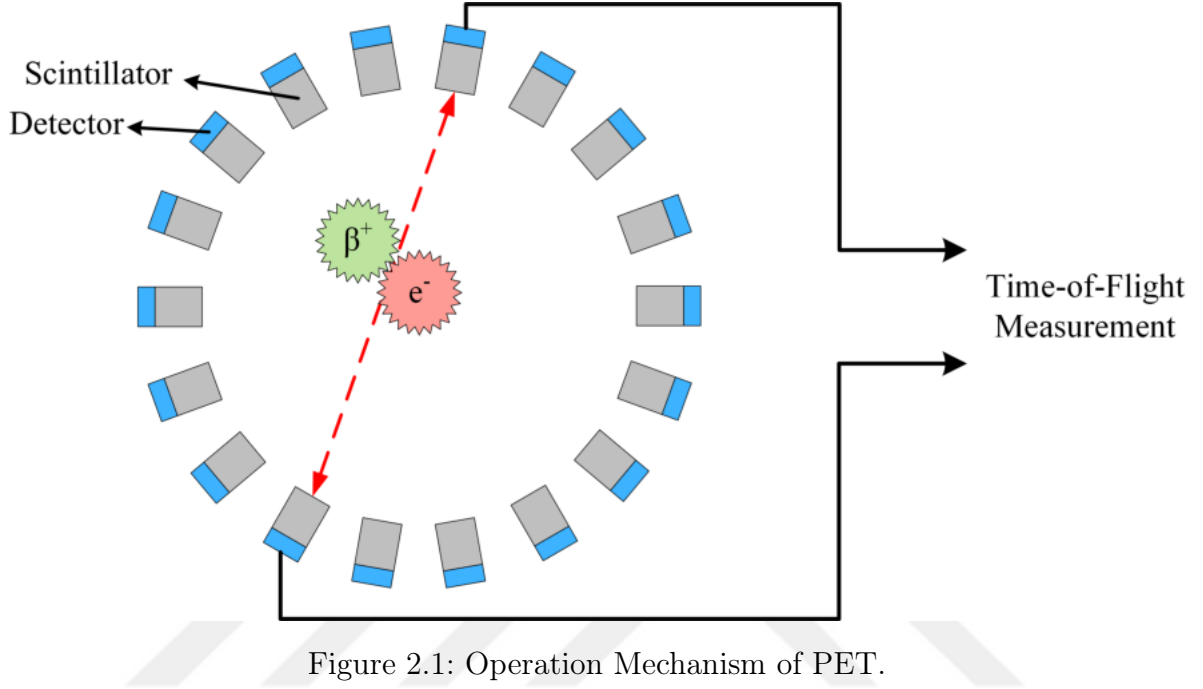


Figure 2.1: Operation Mechanism of PET.

Measuring the time difference between the detection of two γ photons enables to identify the specific section of the line on which the detection occurred. Due to timing uncertainty of scintillators and detectors, ToF measurement result is a distribution with its full width at half maximum (FWHM) named coincidence time resolution (CTR). Achieving lower CTR values in PET is highly desired because it will improve the signal-to-noise ratio (SNR) of constructed images and reduce the radiation dose injected to patients. Performance improvements in scintillators, photodetectors and electronics are needed in order to reach these goals [2].

2.2 Single Photon Avalanche Diode

Single Photon Avalanche Diode (SPAD) is a special type of photodiode that can generate macroscopic current flow by absorption of as few as a single photon. To achieve this

property, a sufficiently high electric field must be created along the depletion region of the photodiode, with the help of some modifications in design and the application of recommended reverse bias which is beyond the nominal breakdown voltage of the p-n junction. Under the effect of this strong electric field, a photo-generated charge carrier attains a kinetic energy that is high enough to overcome the ionization energy of the bulk material, resulting in creation of secondary charge pairs. Eventually, an avalanche current is generated as a result of these self-amplifying cascade of ionizations. This phenomenon is known as impact ionization and explains the distinct feature of SPAD from a standard photodiode. An SPAD utilized in this mechanism of breakdown to achieve high gain is said to be in Geiger mode due to similarities with the operation of a Geiger-Mueller tube.

Induced macroscopic current through an SPAD is suppressed (quenched) by integrating a quenching circuit to it. The easiest way of doing this is passive quenching, in which a series resistor is used to limit the current drawn by an SPAD during breakdown, reducing the voltage seen by the diode to a value below breakdown voltage and stopping the avalanche process. Eventually, SPAD recharges back to its recommended voltage bias and stands by for the new photon detection. The trigger of avalanche current and subsequent quenching period is illustrated in Figure 2.2, with approximate values taken from [3].

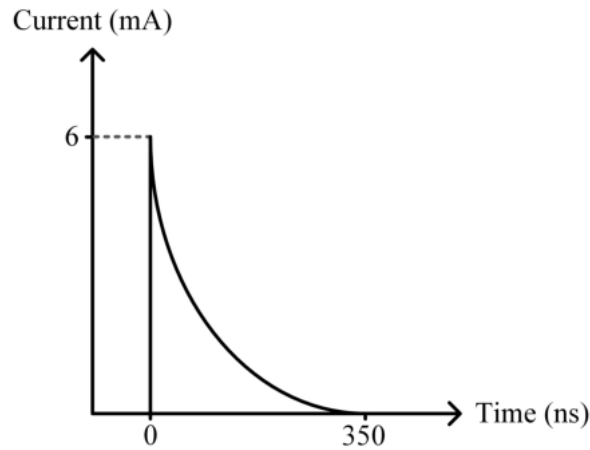


Figure 2.2: Trigger of avalanche current in an SPAD.

High gain and the resulting fast build-up of avalanche current together with low timing jitter makes SPADs a suitable device for applications that require high timing resolution and single photon sensitivity such as 3D imaging, time-resolved imaging and PET [4].

Due to the exponential increase of photocurrent in an SPAD in Geiger mode, no linear relation exists between the number of photons absorbed at the same time, and the signal output of the device. In other words, the amplitude of current induced by absorbing multiple photons is no different to the case of a single photon. Therefore, an SPAD operated in Geiger mode can only provide binary output.

2.3 Silicon Photomultiplier

In order to obtain proportionality between the number of absorbed photons and the signal output, a new configuration named Silicon Photomultiplier (SiPM) is created. It consists of a dense array of SPAD sensors, which can operate independently from each other with their own quenching circuitry, implemented on a common silicon substrate. Each of these independent SPAD sensors is called a pixel.

SiPMs have recently emerged as suitable devices that can surpass the performance of existing Photomultiplier Tubes in many applications. They offer increased ruggedness, compactness and less sensitivity to magnetic fields. Furthermore, being solid-state devices, they have relatively low operating voltage, low power consumption and are easier to fabricate in large quantities [5].

There are two configurations for the implementation of a SiPM: Analog Silicon Photomultiplier (A-SiPM) and Digital Silicon Photomultiplier (D-SiPM). In A-SiPM, output photocurrent of each SPAD sensor is summed in a common node, providing information about the magnitude of photon flux, as shown in Figure 2.3 with each pixel consisting of an SPAD and a quenching resistor. In a D-SiPM, SPAD sensor architecture is augmented with specific circuitry to generate digital signals for each photon detection. In a conventional D-SiPM which is designed for photon time of arrival applications, all sensor output signals are routed to an OR gate and the resulting signal is fed into an on-chip TDC. D-SiPMs have advantages over A-SiPMs in these applications because sources of time uncertainty such as SPAD sensor jitter and TDC nonlinearities can be removed or compensated [6].

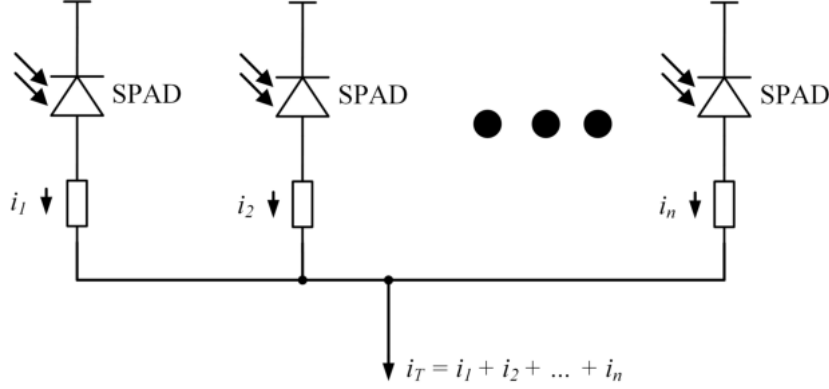


Figure 2.3: Analog Silicon Photomultiplier.

Another significant contributor to timing resolution in SPAD arrays is pixel-to-pixel timing skew. In the above-mentioned two cases of A-SiPM and conventional D-SiPM, timing skew becomes significant due to different distances of pixels to output and the corresponding uneven propagation delay values [4].

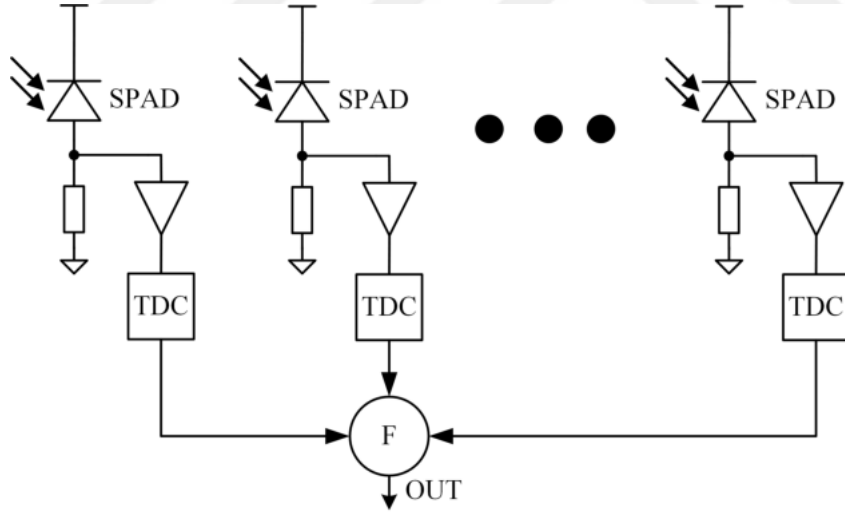


Figure 2.4: Multi-Channel Digital Silicon Photomultiplier.

An alternative configuration to decrease pixel-to-pixel timing skew is integrating a TDC in each pixel. This structure is called a Multi-Channel Digital Silicon Photomultiplier (MD-SiPM) and can be seen in Figure 2.4. This approach also enables independent

detection and subsequent signal processing of multiple photons at the same time, and thus providing robust and more detailed statistical information about the event that is the source of the photon flux [7].

2.4 Time-to-Digital Converter

A Time-to-Digital Converter (TDC) is a device which converts a time variable to a digital code. It essentially performs an analog-to-digital conversion. While an analog-to-digital converter (ADC) uses an electrical voltage as the input, a TDC uses a time difference. TDCs are the essential building blocks of time-mode circuits and have been used in a wide range of applications such as ToF measurements in HEP and PET, all digital frequency synthesizers, serial links and software defined radios [8].

2.4.1 Performance Parameters of TDCs

A summary of the most important performance parameters of TDCs, other than the obvious ones such as power and area consumption, is provided below.

2.4.1.1 Resolution

Resolution is the minimum time variable that a TDC can quantize. It is also the least significant bit (LSB) of the output digital code. It can be expressed in terms of the full-scale input time difference range of the TDC, FSR , and the number of bits in the output code, N , as given in (2.1). Resolution of a TDC is highly dependent on its architecture.

$$LSB = \frac{FSR}{2^N - 1} \quad (2.1)$$

2.4.1.2 Timing Accuracy

Timing accuracy (precision) depicts the difference between the digital output value and the actual input time difference of a TDC. Quantization noise being the theoretical minimum level, there are many sources of noise in a TDC such as reference clock jitter and additional noise coming from electronic components that can degrade the timing accuracy. A simplified equation for precision can be seen in (2.2) where σ_{add} denotes the noise sources other than the quantization noise. The equation for quantization noise is given in (2.3), which is directly related to the resolution (LSB) of the TDC [1].

$$\sigma_{TDC,rms} = \sqrt{\sigma_q^2 + \sigma_{add}^2} \quad (2.2)$$

$$\sigma_q = \frac{T_{LSB}}{\sqrt{12}} \quad (2.3)$$

2.4.1.3 Linearity

Linearity characterizes the measure of conformity of a time-to-digital transfer curve of a TDC with the ideal, linear transfer curve. It is quantified by two measures of performance Differential Nonlinearity (DNL) and Integral Nonlinearity (INL), which can be defined for all quantization processes. DNL depicts the difference between an actual step width in the input-output (I/O) transfer curve and the ideal step width, whereas INL depicts the cumulative effect of DNL up to a desired point in the curve. Both DNL and INL are quantified in terms of LSB and the equations to calculate these parameters are given in (2.4) and (2.5). Process, voltage, and temperature (PVT) variations are the major sources of nonlinearity in a TDC.

$$DNL(n) = \frac{T_{in}(n+1) - T_{in}(n)}{T_{LSB}} - 1 \quad (2.4)$$

$$INL(n) = \sum_{k=1}^n DNL(k) \quad (2.5)$$

2.4.1.4 Conversion Time

Conversion time is the amount of time it takes for a TDC to complete the conversion of the input time difference to its digital representation. It is a particularly important parameter for TDCs used in high speed applications.

2.4.1.5 Dynamic Range

Dynamic range is the maximum input time difference a TDC can digitize. In ToF measurements, this corresponds to the maximum range in which the system should be able to detect the source events.

2.4.1.6 Voltage Sensitivity

Voltage sensitivity is the measure of the effects of fluctuations in supply voltage level on the performance of the TDC, such as its timing accuracy, linearity etc.

2.4.1.7 Temperature Sensitivity

Temperature sensitivity is the measure of the effects of temperature variations on the performance of the TDC, such as its timing accuracy, linearity etc.

2.5 TDC Architectures

There are many different types of TDC architectures which can be encountered in the literature such as Counter TDCs, TDCs with Interpolation, Pulse-Stretching TDCs, Pulse-Shrinking TDCs, Successive Approximation TDCs and Flash TDCs, to name a few. In the following, only the architectures which are frequently selected for SiPM applications will be presented in more detail.

2.5.1 Delay Line TDC

Delay line TDC is one of the simplest architectures available and it is illustrated in Figure 2.5. It consists of N delay blocks and D flip-flop (DFF)s and its operation is as follows: Start signal, which denotes the beginning of the input time difference, propagates through the cascade of delay blocks with each of them having a delay of τ , while Stop signal is connected to the clock input port of DFFs. With the arrival of the Stop signal, all DFFs sample the corresponding stage of the delay line, and a thermometer code output is obtained, which is a digital representation of the input time difference.

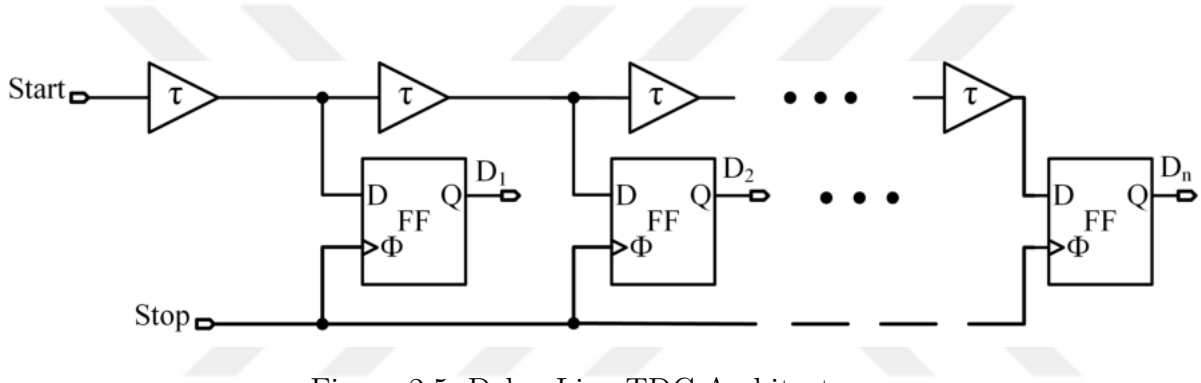


Figure 2.5: Delay Line TDC Architecture.

Resolution of the delay line TDC is limited by the per stage delay τ , as shown in (2.6), as long as the delay of DFFs is negligible in comparison. Therefore, this architecture is not suitable to achieve very fine resolution values. One significant concern in the operation of delay line TDCs is the possible metastability problems of DFFs, which is a consequence of the asynchronization of Start and Stop signals. These result in uncertain or incorrect output signals and, therefore, mistakes in the output code.

In the ideal case, the dynamic range of a delay line TDC is limited by the number of stages N as shown in (2.7). However, when we consider the jitter and mismatch of delay stages, which arise as a consequence of switching noise, cross talk, thermal noise and process variations between individual stages, and accumulative characteristic of these unwanted effects along the line, deteriorating nonlinearity becomes a significant problem. Therefore,

long delay line TDCs cannot offer the desired dynamic range in practice.

$$T_{LSB} = \tau \quad (2.6)$$

$$DR = N \cdot \tau \quad (2.7)$$

2.5.2 Vernier Delay Line TDC

The fact that the minimum resolution of a delay line TDC is limited by the individual stage delay, calls for additional techniques to be used for applications which require sub-stage delay resolution. Vernier technique is one that is widely used and encountered in literature.

Vernier delay line TDC architecture contains an extra delay line with the same number of stages N , but slightly different per-stage delay, and is illustrated in Figure 2.6.

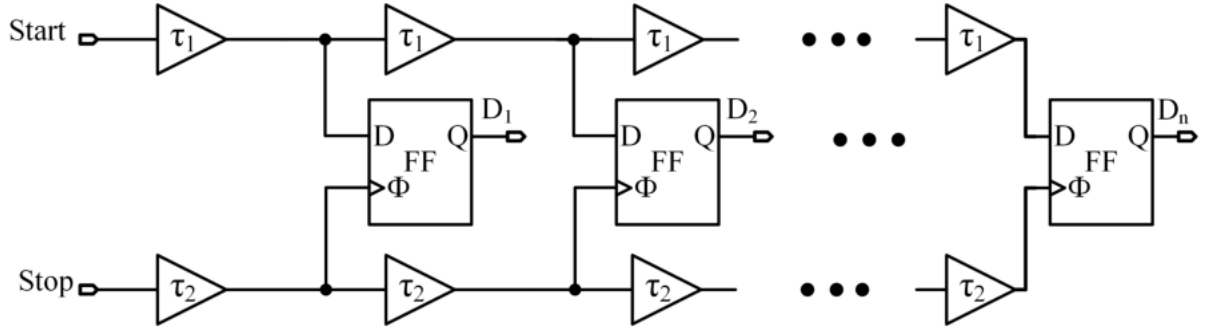


Figure 2.6: Vernier Delay Line TDC Architecture.

It operates as follows: Start signal propagates through the delay line with slightly larger stage delay τ_1 , whereas Stop signal propagates through other delay line with stage delay τ_2 . Eventually, Stop signal catches up with Start signal along the line and this instance is detected by the corresponding DFF.

The resolution is equal to $\Delta\tau = \tau_1 - \tau_2$, as shown in (2.8) and the upper-limit of the dynamic range is given in (2.9). The cost of achieving sub-stage resolution is the significant drop in the dynamic range, and the increase in power and area consumption.

$$T_{LSB} = \tau_1 - \tau_2 \quad (2.8)$$

$$DR = N \cdot (\tau_1 - \tau_2) \quad (2.9)$$

One important advantage of vernier operation is being able to minimize common-mode disturbances in the system to the first order, because of its fully differential nature. The effect of supply and temperature variation on the propagation delay of the stages can be given as examples of these disturbances.

2.5.3 Gated Ring Oscillator TDC

Ring oscillators are utilized in a wide range of applications due to their attractive properties such as compact layout, scalable digital implementation and wide tuning range. Gated Ring Oscillator (GRO) is a special class of ring oscillators which can be turned on/off by a gating signal and the TDC architecture based on GRO can be seen in Figure 2.7.

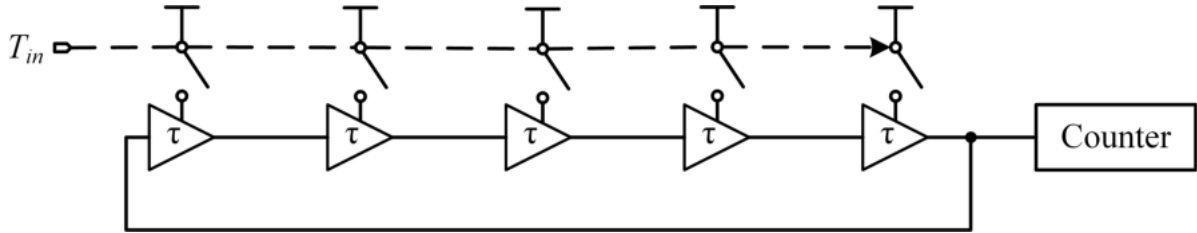


Figure 2.7: Gated Ring Oscillator TDC.

When the gating signal T_{in} goes high, GRO is turned on, and similarly when it goes low, GRO is turned off. While the oscillator is running, the number of oscillation cycles is counted by a counter block connected to the output node. Counter result gives a digital representation of T_{in} with the resolution of one oscillation period length, which is given

in (2.10) where N is the number of stages in the ring and τ is the delay of a single stage. Achieving lower resolution values requires increasing the oscillation frequency of GRO.

$$T_{LSB} = 2N\tau = \frac{1}{f_{osc}} \quad (2.10)$$

The main advantage of GRO TDCs over delay line TDCs is their theoretically unlimited dynamic range, since the signals do not propagate once but multiple times through the system, due to delay stages being connected in a ring format.

2.5.4 Vernier Gated Ring Oscillator TDC

Vernier GRO TDC combines the advantages of GRO and vernier technique together in a single architecture and is shown in Figure 2.8. It contains two GROs with slightly different oscillation frequencies, two counters and a coincidence circuit.

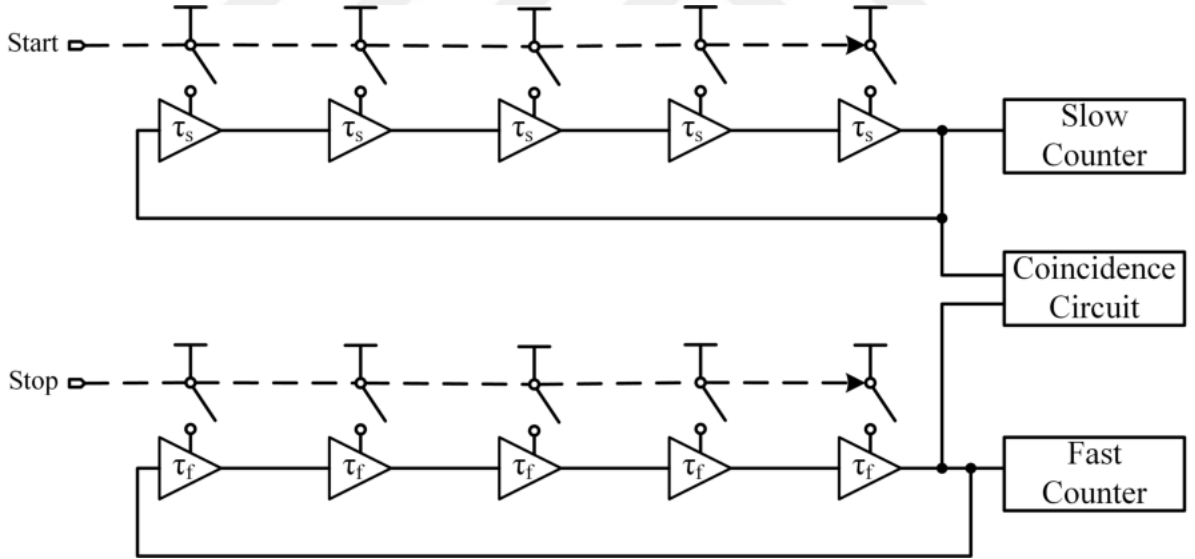


Figure 2.8: Vernier Gated Ring Oscillator TDC.

The operation is illustrated in Figure 2.9. Start signal turns on the slow oscillator and Stop signal similarly turns on the fast oscillator. Eventually, the fast oscillator signal's edge catches up with that of the slow oscillator and this instance is flagged by the coincidence circuit, which brings the conversion to an end. The time interval in which slow oscillator is already running but the fast oscillator is not, is called the coarse mode, and the remaining part until coincidence is called the vernier mode. The conversion result is obtained by slow and fast counters as given in (2.12), where n_s and n_f denote slow and fast oscillation counts, and T_s is the period of the slow oscillator.

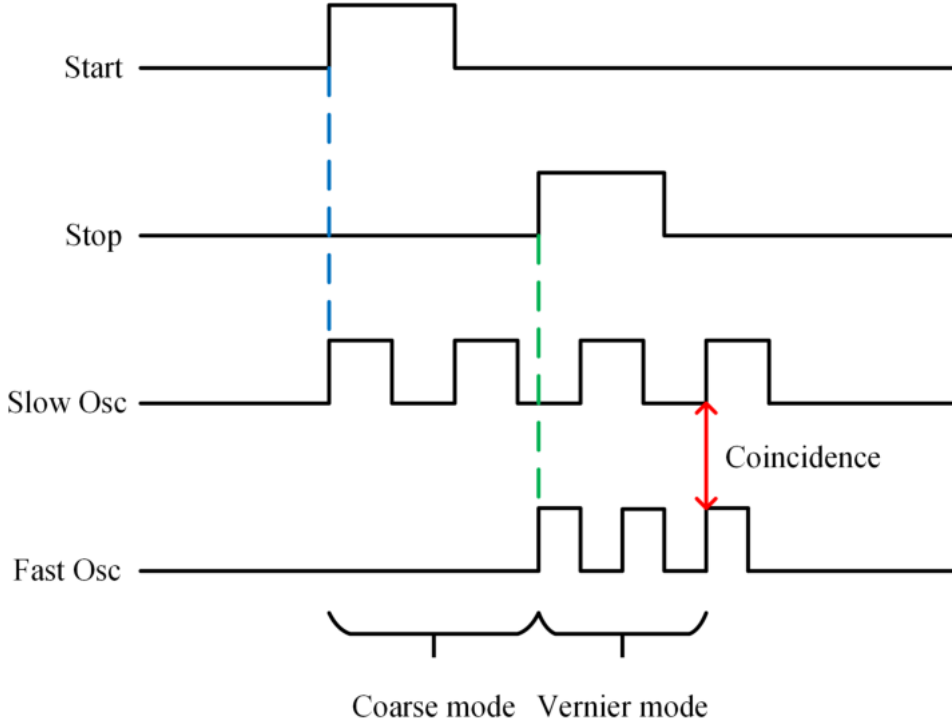


Figure 2.9: Vernier GRO TDC Operation.

The resolution of vernier GRO TDC is given in (2.11), where τ_s and τ_f denote the slow and fast oscillator stage delays, respectively.

$$T_{LSB} = 2N(\tau_s - \tau_f) = \frac{1}{f_{osc,s}} - \frac{1}{f_{osc,f}} \quad (2.11)$$

$$\text{Conv.Result} = T_s \cdot (n_s - n_f) + T_{LSB} \cdot n_f \quad (2.12)$$

The timing accuracy of a TDC was given in (2.2). In the case of vernier GRO TDC, the dominant part of the additional noise comes from the jitter of oscillators, σ_{osc} , which can be expressed in terms of individual oscillator jitters, σ_s and σ_f as in (2.13). In most of the cases, coarse mode slow oscillator counts can be neglected in comparison to n_f , so the overall jitter of TDC can be approximated as in (2.14) [1].

$$\sigma_{TDC}^2 \approx \sigma_{osc}^2 = \sigma_s^2 \cdot (n_s) + \sigma_f^2 \cdot (n_f) \quad (2.13)$$

$$\sigma_{TDC}^2 \approx (\sigma_s^2 + \sigma_f^2) \cdot (n_f) \quad (2.14)$$

Usually a periodic reference clock is used as the Stop signal. The period of this signal also determines the dynamic range of the TDC. The maximum values of slow and fast oscillator cycles can be found as in (2.15) and (2.16), where T_{stop} denotes the period of the Stop signal.

$$n_{f,max} = \frac{T_s}{T_{LSB}} \quad (2.15)$$

$$n_{s,max} = \frac{T_{stop}}{T_s} + n_{f,max} \quad (2.16)$$

Conversion time of the TDC can easily be found as in (2.17). When the maximum values of n_s and n_f are inserted into (2.17), maximum conversion time of the TDC is obtained in (2.18).

$$t_c = T_s \cdot n_s \quad (2.17)$$

$$t_{c,max} = T_s \cdot n_{s,max} = T_{stop} + \frac{T_s^2}{T_{LSB}} \quad (2.18)$$

When equations (2.14) and (2.18) are examined, it is seen that in order to lower the jitter and conversion time of a vernier GRO TDC, the oscillation frequencies of the GROs have

to be increased, i.e. oscillation periods have to be decreased. However, the well-known equation of dynamic power consumption in digital circuits, $P_D = fCV_{DD}^2$, constitutes a direct relationship between the frequency of a circuit and its dynamic power consumption. Therefore, a trade-off between better jitter/conversion time, and lower power consumption exists in the design process of a vernier GRO TDC.



3 TDC Design and Implementation

In this chapter, the design and implementation process of the TDC is explained in detail. After presenting the requirements of the present TDC application, the reasoning behind the selection of the TDC architecture and the delay cell architecture is explained. Then, a detailed explanation of the GRO, the coincidence circuit and the logic control unit design are given. The chapter is concluded with the implementation of the counters.

3.1 TDC Requirements

The target application of ToF PET imaging sets some demanding performance requirements for the TDC. In order to achieve direct image reconstruction with millimetric precision, a CTR of 4 ps rms has to be achieved, which imposes the maximum limits for the timing accuracy (jitter) and also the resolution specifications, due to quantization noise being a significant part of the overall jitter as given in (2.3) [9]. DNL and INL are also required to be kept small so that the intended timing accuracy performance can be achieved.

Dynamic range specification is determined by considering the range of source events in PET application. Conversion time is desired to be smaller than 100 ns so that the TDC can operate with the expected events per second in PET.

The TDC has to be integrated with an SPAD in a single pixel of the D-SiPM. This requires it to have a very compact size so that the fill factor of a pixel, which is equal to the percentage of the surface area that is sensitive to light, can be kept high enough and the photon detection efficiency is not compromised [10]. Furthermore, the array structure and the corresponding high number of TDCs used in the D-SiPM compels the power

consumption to be another important consideration in the design, which needs to be kept as low as possible. The overall TDC specifications are given in Table 3.1.

Table 3.1: TDC Specifications.

Parameter	Specification
Technology	TSMC 28 nm
Supply Voltage	0.9 V
Resolution (LSB)	5 ps
Jitter (Timing Accuracy)	< 4 ps rms
Conversion Time	< 100 ns
Dynamic Range	4 ns
DNL/INL	< 1 LSB

3.2 Selection of TDC Architecture

The specifications require the TDC to have both very fine resolution and a considerable dynamic range at the same time. Considering the stringent requirement on the design to have a very compact size, i.e. small footprint, delay line TDC architectures have to be eliminated. Implementation of these architectures would require a prohibitively long delay line and correspondingly cover a large area on the chip.

Although GRO TDC offers a straightforward and easy implementation, in order to reach 5 ps resolution in this architecture, an oscillation frequency of 200 GHz would be required. This is a prohibitively high frequency value which is not feasible due to two main reasons: It would result in very high dynamic power consumption and also difficulties in compensating for the nonideal effects.

Vernier GRO TDC, on the other hand, stands out as the most suitable architecture. Here 5 ps resolution can be achieved without having to use extremely high oscillation frequencies. Furthermore, 4 ns dynamic range can be reached by using much less silicon area than in delay line architectures.

3.2.1 Architectural Specifications

Having selected vernier GRO as the architecture of the TDC, oscillation frequencies of slow and fast Ring Oscillator (RO)s have to be determined. Dynamic range specification automatically sets the value of f_{stop} , frequency of the stop signal, as in (3.1). When this value is inserted into (2.18), together with the maximum conversion time specification of 100 ns, it sets a theoretical upper-limit of around 690 ps for the slow oscillator period, T_s .

$$f_{stop} = \frac{1}{T_{stop}} = \frac{1}{DR} \quad (3.1)$$

Considering the previously discussed trade-off between jitter/conversion time and power consumption, T_s is determined as 500 ps, which gives an adequate overhead for conversion time without increasing the oscillation frequency, and correspondingly the power consumption, unnecessarily high. The final specifications of the architecture are given in Table 3.2.

Table 3.2: Architectural Specifications.

Specification	Symbol	Value
Architecture		Vernier GRO TDC
Stop Signal Frequency	f_{stop}	250 MHz
Slow Oscillator Period/Frequency	T_s/f_s	500 ps/2 GHz
Fast Oscillator Period/Frequency	T_f/f_f	495 ps/2.02 GHz
Resolution (LSB)	T_{LSB}	5 ps

3.3 Delay Cell Architectures

The next step in the design of the vernier GRO TDC is selecting the delay cell (delay stage) which is going to be used in forming the GRO. The delay cell should digitally invert the input signal and cause an externally controllable propagation delay to occur. Deciding on the most suitable delay cell architecture is an important step of the design process,

which requires detailed simulations to be carried out. To this end, four different delay cell architectures are considered.

3.3.1 Current Starved Inverter

One of the simplest designs for a delay cell is the current starved inverter shown in Figure 3.1. It contains an inverter formed by M2 and M3 transistors, and two current controlling (starving) M1 and M4 transistors. The desired propagation delay can be adjusted with the help of two control voltages V_{ctrlp} and V_{ctrln} [1].

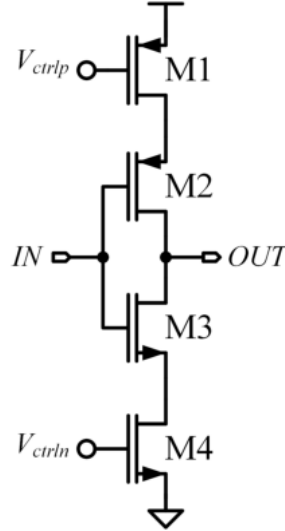
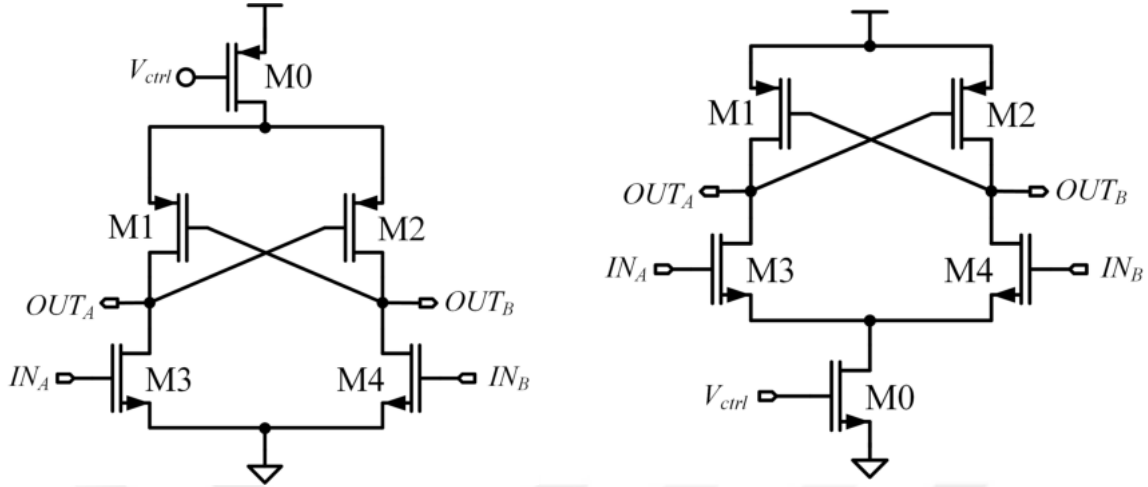


Figure 3.1: Current Starved Inverter.

3.3.2 Differential Inverter with PMOS Control

The alternative to the single-ended topology of current starved inverter is differential inverters. Differential inverter with PMOS control is shown in Figure 3.2(a). It contains a differential pair M3-M4 with cross-coupled PMOS transistors M1-M2 connected to the load, and a current starving transistor M0 [11].



(a) Differential Inverter with PMOS Control. (b) Differential Inverter with NMOS Control.

Figure 3.2: Differential Inverters.

3.3.3 Differential Inverter with NMOS Control

Differential inverter with NMOS control is shown in Figure 3.2(b). It is a very similar architecture to the one with PMOS control except here the dual approach of NMOS control is preferred to control the current flow through the cell.

3.3.4 Pseudo-Differential Inverter

The schematic of the pseudo-differential inverter is given in Figure 3.3. It is essentially formed by two inverters whose output nodes are connected with a pair of additional cross-coupled inverters, which prevent latch-up. A ring oscillator formed by two pseudo-differential inverters is drawn in Figure 3.4 for convenience, which is a very useful architecture in providing quadrature phases from its four output nodes [12].

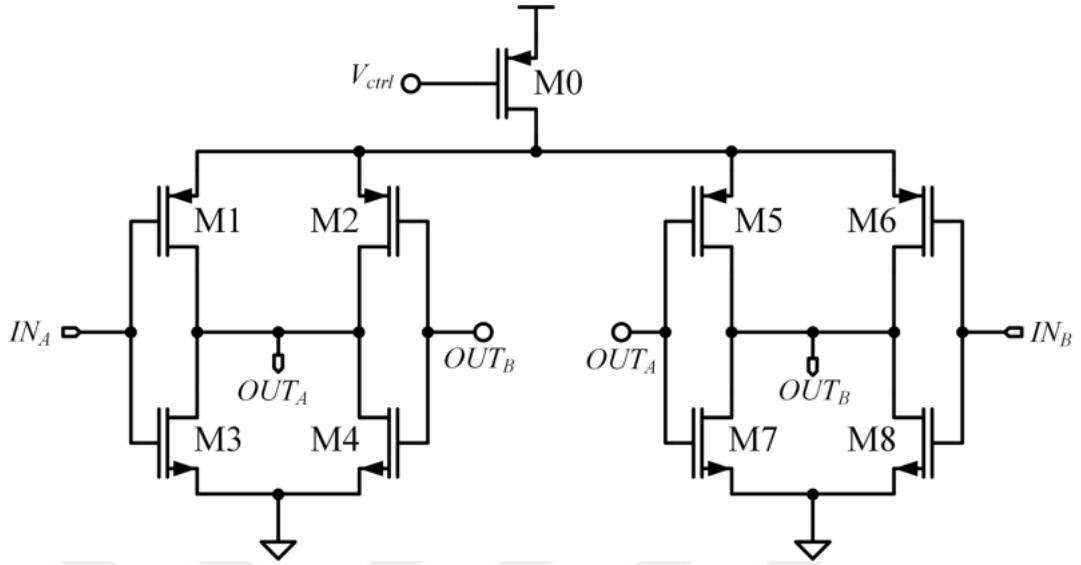


Figure 3.3: Pseudo-Differential Inverter.

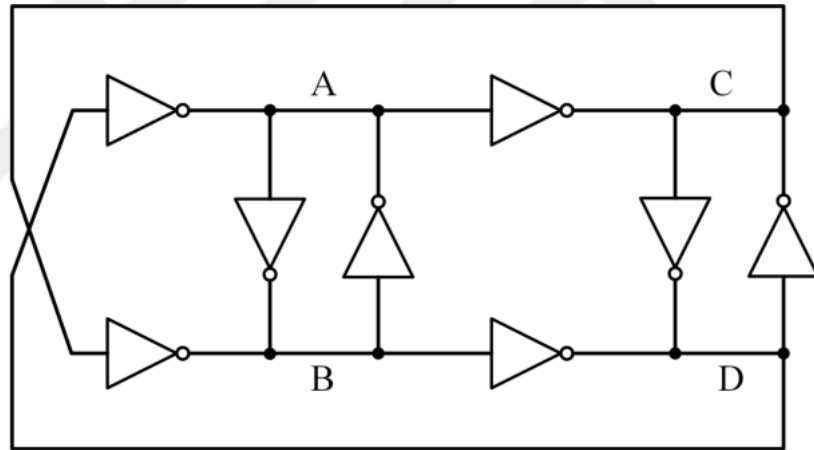


Figure 3.4: A Ring formed by 2 Pseudo-Differential Inverters.

3.4 Design of the GRO

Design of the GRO involves selecting the most suitable delay cell architecture and the number of stages, and the implementation of the gating function.

3.4.1 Initial Assessment of Delay Cell Architectures

The performance of different delay cells are simulated by forming ring oscillators. Simulations are carried out in Cadence Virtuoso software environment. The most important performance parameters to be checked in the first phase of simulations are average power consumption, cycle jitter and the stability of the oscillation frequency under PVT variations. The results are given in Table 3.3. Cycle jitter is equal to the standard deviation of the length of a single period, and gives a measure for the oscillation stability under nominal conditions. Periodic steady state (PSS) analysis is used to conduct this simulation.

Monte Carlo (MC) simulations are carried out to investigate the stability of the oscillation frequency under PVT variations. Histogram plots of the results are created for each configuration in Table 3.3, and can be seen in Figure 3.5 to Figure 3.7. Relative standard deviation (RSD) value, which is equal to σ/μ for each configuration, is also included in Table 3.3 to easily compare the relative variation of the oscillation frequencies.

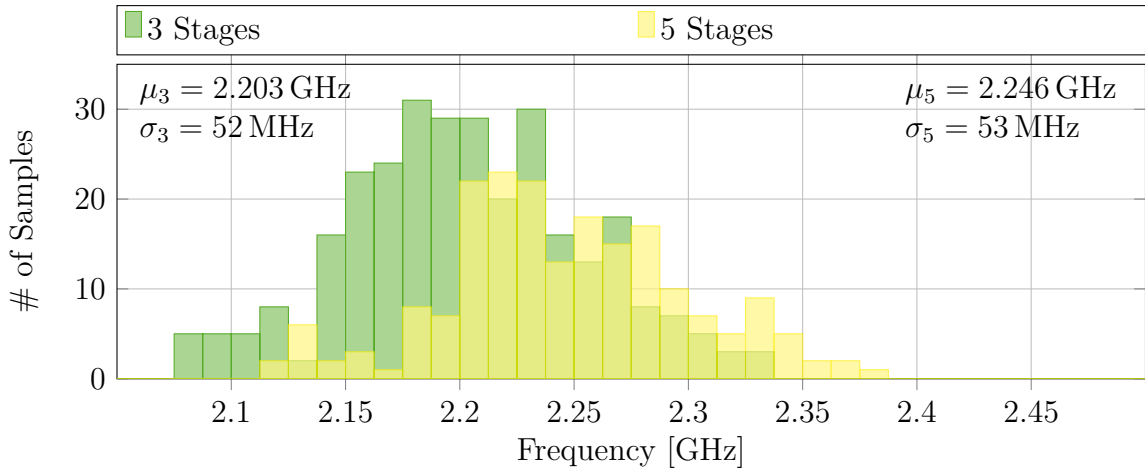


Figure 3.5: Histogram Plot for RO based on Current Starved Inverter.

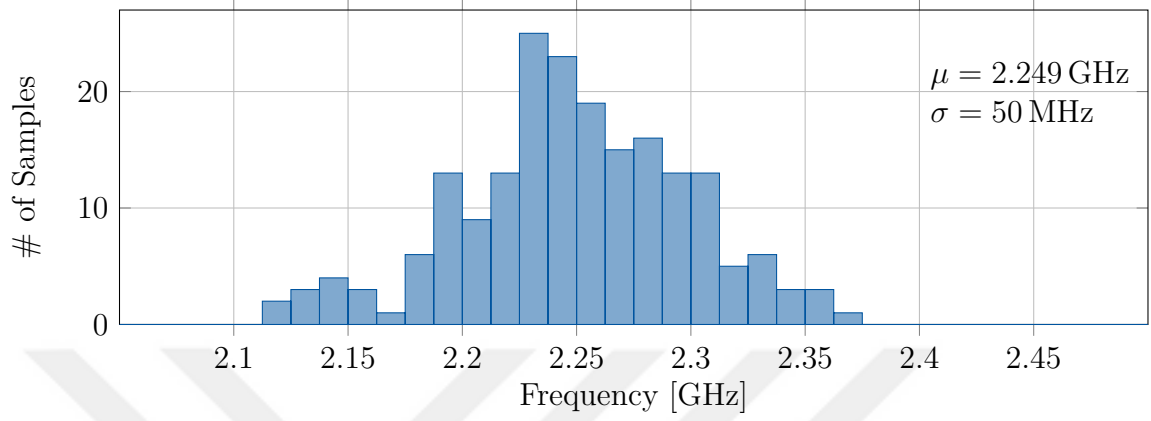


Figure 3.6: Histogram Plot for RO based on Pseudo-Differential Inverter.

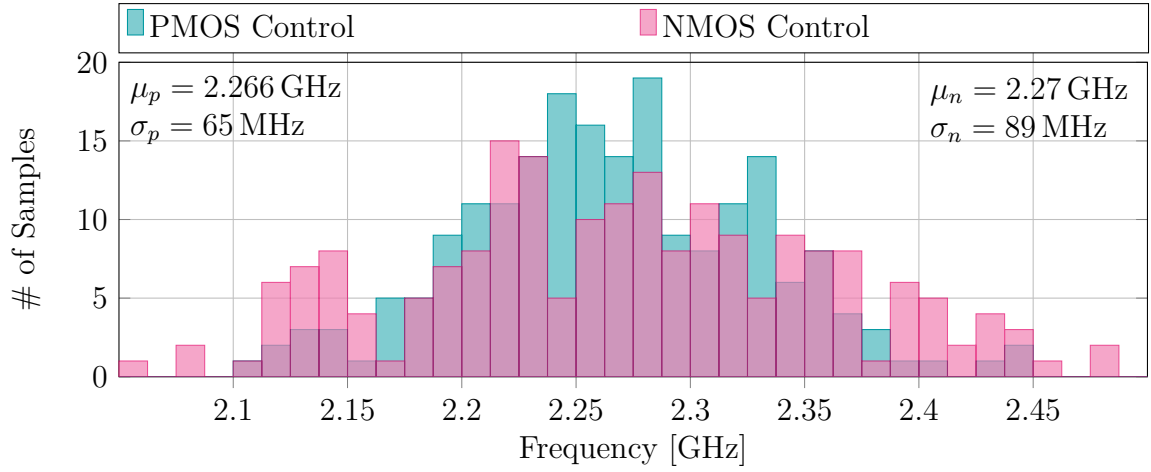


Figure 3.7: Histogram Plot for RO based on Differential Inverters.

Table 3.3: RO Simulation Results.

Delay Cell	Number of Stages	Av. Power Consumption [μ W]	Cycle Jitter [ps-rms]	RSD [%]
Current Starved Inverter	3	22	0.72	2.4
Current Starved Inverter	5	33	0.58	2.4
Pseudo-Differential Inverter	2	81	0.43	2.2
Differential Inverter with NMOS Control	3	98	1.22	3.9
Differential Inverter with PMOS Control	3	89	0.89	2.9

The results in Table 3.3 show that the pseudo-differential inverter has a clear advantage over the other two differential architectures because it produces oscillations with much lower cycle jitter and its RSD under PVT variations is lower. However, current starved inverter also stands out with the low power consumption of the RO. Therefore, in the end of the first phase of the simulations, these two alternatives remain for the delay cell architecture.

3.4.2 Implementation of the Gating Function

There are two different methods in the literature to incorporate a gating function to the RO. First method is to add gating (or enabling) transistors directly to delay cells. These transistors are usually located in the top and/or bottom of the delay cell and cut off the current flow through the cell when desired. After the current flow is stopped, the output node voltage of the oscillator is maintained by the output capacitance [13].

The second method is to use an additional enabler (or multiplexer) block in the RO. This block can be used to stop the oscillations and fix the output node voltage at high level when the RO is turned off, and start and keep the oscillations going by alternating its output voltage, essentially functioning as another inverter cell. This method is preferred

over the first one because it has a simple implementation, does not rely on capacitance to maintain nodal voltages, and also consumes less area.

In order to implement an enabler block for single-ended topology, a truth table of the desired functionality is created as in Table 3.4, where EN stands for enable(gating) signal to control the GRO. The table reveals the NAND gate as the block which can fully serve to our purposes as shown in (3.2).

Table 3.4: Truth Table of the Enabler Block.

IN	EN	OUT
0	0	1
1	0	1
0	1	1
1	1	0

$$OUT = (IN \wedge EN)' \quad (3.2)$$

If the same functionality is desired for a differential topology such as pseudo-differential inverter, because two output signals are available, another block which keeps its output node at low level in the off state of the GRO is required, on the contrary to the first one. Using the same methodology, it can easily be seen that a NOR gate is the suitable block for this purpose, with the inverted gating signal applied to its control input.

3.4.3 Final Assessment of Delay Cell Architectures

3.4.3.1 Initial Stability of the GRO

Obtaining stable oscillations, i.e. with negligible deviation from the target frequency/period, starting from the very first cycle is an important consideration so that the accuracy of the conversion and the linearity of the transfer curve can be kept in the intended range. To this end, simulations are performed with current starved inverter and pseudo differential inverter based GROs and the following results given in Figure 3.9 and Figure 3.8 are obtained. The given number of stage values in the figures do not include the enabler

block(s).

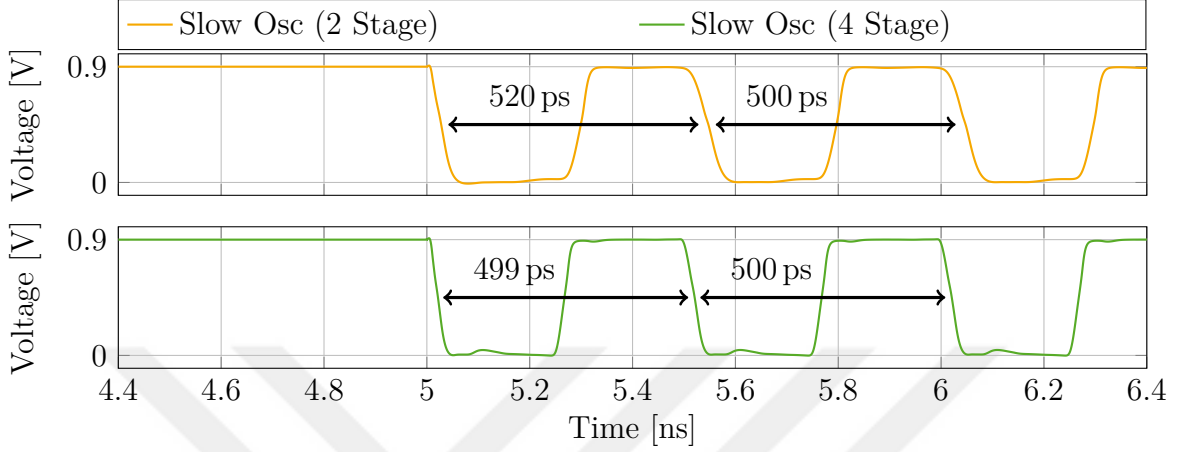


Figure 3.8: Initial Stability of Pseudo-Differential Inverter based GRO.

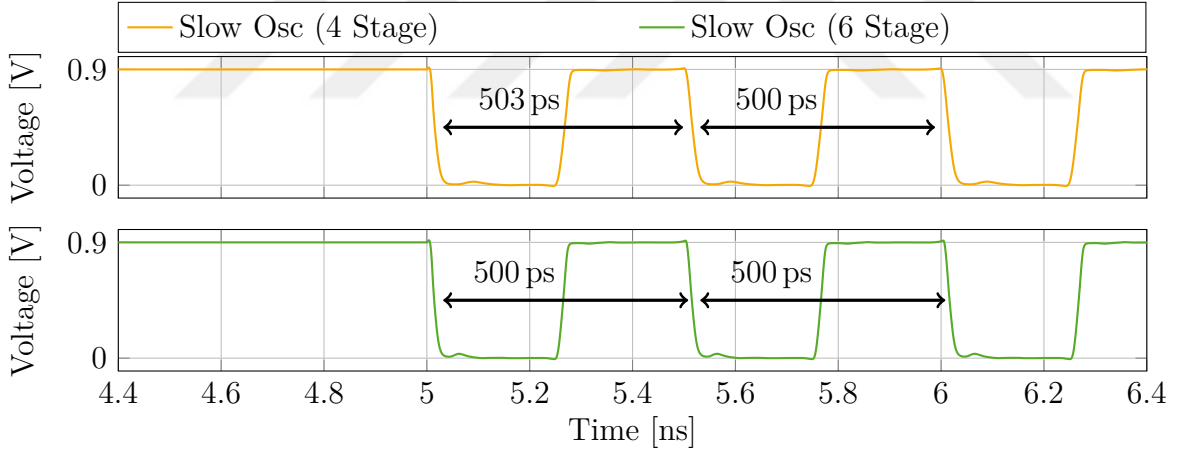


Figure 3.9: Initial Stability of Current Starved Inverter based GRO.

The results reveal a strong relation between the number of stages in the ring and the initial stability of the oscillator. The deviation from the target oscillation period is desired to be less than 1ps. Therefore, at least four stages are needed in a GRO based on pseudo-differential inverter, and six stages are needed for the one based on current starved inverter.

3.4.3.2 Investigation of Power Supply Noise Effects

In addition to oscillation stability, phase noise/jitter and power consumption, the effect of power supply noise on the GRO is another important consideration in the selection process of the delay cell architecture. In order to simulate this effect, a white noise signal with approximately 20 mV peak-to-peak amplitude is added on top of the standard 0.9 V to create a noisy power supply signal as shown in Figure 3.10. This noisy power supply is used in a new set of simulations in which its effect on the jitter of oscillations are observed.

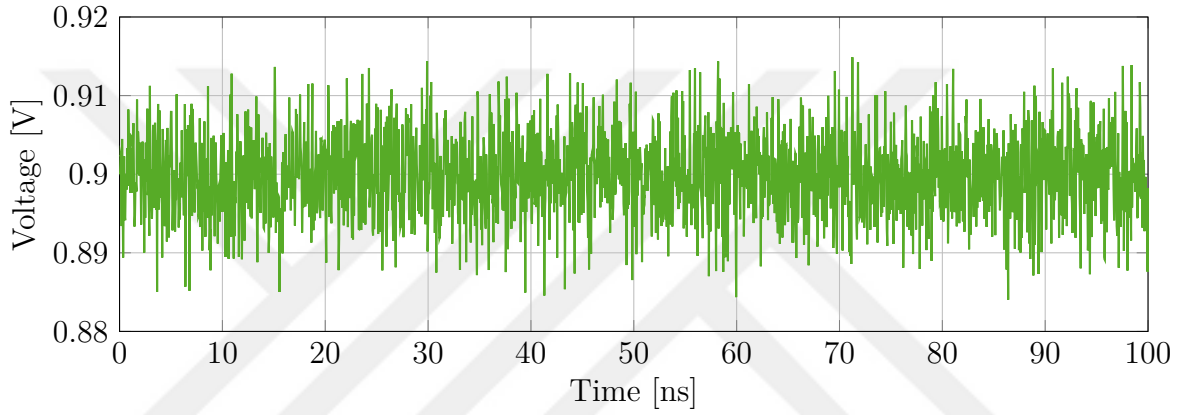


Figure 3.10: Noisy Power Supply with approx. 20 mV White Noise added.

3.4.3.3 Finalization of the GRO

After the implementation of the gating function and the findings about the initial stability of the GROs, a final set of simulations are performed on current starved inverter based GRO with six stages and pseudo-differential inverter based GRO with four stages. The results are given in Table 3.5, where N denotes the number of stages, J_C the cycle jitter, and $J_{C,noisy}$ the cycle jitter with the noisy supply. Specified number of stages do not include the enabler block(s). Average power consumption values include both slow and fast oscillators.

The results show that the two architectures achieve similar performance in terms of the jitter of oscillations, both with ideal power supply and noisy power supply. However, there is a very significant difference between the average power consumption values of them.

Table 3.5: Final GRO Simulation Results.

Delay Cell	N	P_{tot} [μ W]	J_C [ps-rms]	$J_{C,noisy}$ [ps-rms]
Current Starved Inverter	6	73	0.59	2.18
Pseudo-Differential Inverter	4	305	0.43	2.14

Current starved inverter based GRO stands out as the much more efficient architecture, and hence, it is selected to implement the vernier GRO TDC. The final configuration of the GRO is shown in Figure 3.11. It consists of six current starved inverter stages and a NAND gate.

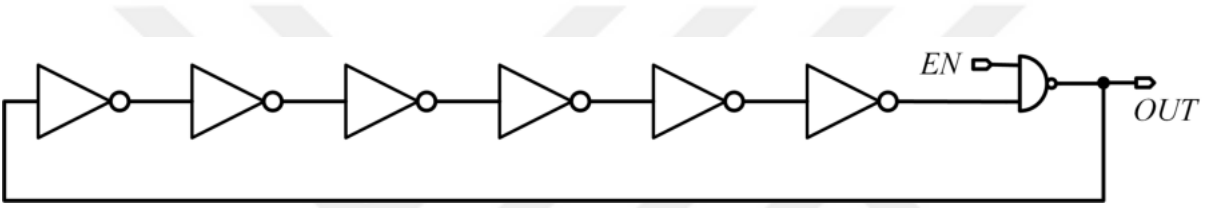


Figure 3.11: Final Configuration of the GRO.

3.5 Coincidence Detection Circuit

The TDC has to include a time comparator circuit which should output a digital signal providing information about the precedence of the slow and fast oscillation edges. This circuit will serve as the main block to detect the coincidence of the slow and fast oscillator signal edges and flag the end of the time-to-digital conversion.

There are two methods to implement the coincidence detection in the TDC. One is to use a single coincidence detection circuit and the other is to use multiple ones. Multiple coincidence circuit schemes can further increase the resolution of the TDC by enabling detection in delay cell level. However, unmatched delay cells will cause problems with the linearity, while matching the cells is an area hungry approach. Considering the importance of a small footprint for our TDC, as well as the prospect of a simpler implementation, using a single coincidence detection circuit is preferred [1].

There are several alternative circuits that can perform the time comparison function. DFFs are one of these alternatives. However, in analogy to the voltage offset in voltage comparators, there exists a time offset in time comparators that needs consideration. In this regard, DFFs are poor performers with unbalanced loads in their clock and data paths, and set and hold time requirements and the related metastability issues [10].

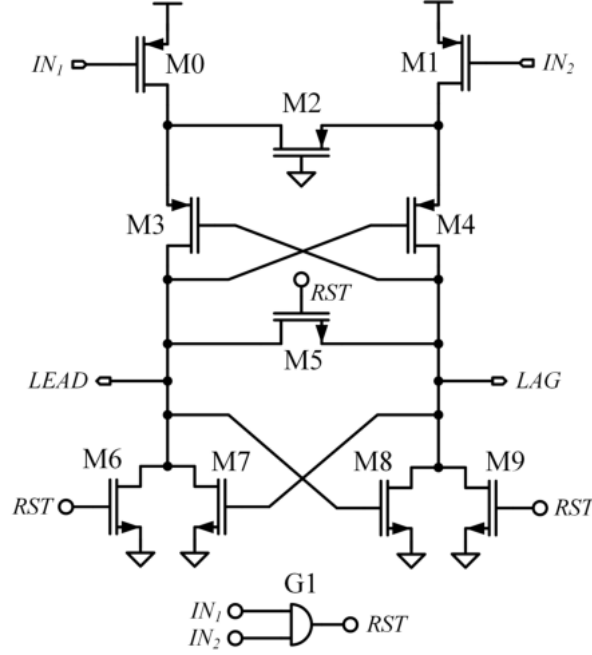


Figure 3.12: Schematic of the Arbiter.

One of the other alternatives is an arbiter. An arbiter offers much better performance regarding metastability issues because it utilizes regeneration for speed enhancement, which allows it to detect very small time differences between its two inputs [8]. Furthermore, the two input paths of an arbiter are well matched, and its area consumption is less than that of a DFF. Because of these advantages, it is selected to implement the coincidence detection circuit.

The schematic of the arbiter circuit is given in Figure 3.12. It is essentially a specifically modified SR latch. In addition to two cross-coupled NOR gates of a standard SR latch, it contains two weak transistors M2 and M5, whose purpose is to balance the nodal voltages

in the two branches. The RST signal, which is created by the AND operation of the two input signals, limits the reset functionality of the circuit only to the case when both of the inputs are high. In this way, unnecessary charge/discharge cycles are prevented and the power consumption of the circuit is reduced. The design in Figure 3.12 is adapted based on the needs of our application. The original circuit, reported in [14], is designed to detect the rising edges of the input signals, so it is based on two cross-coupled NAND gates.

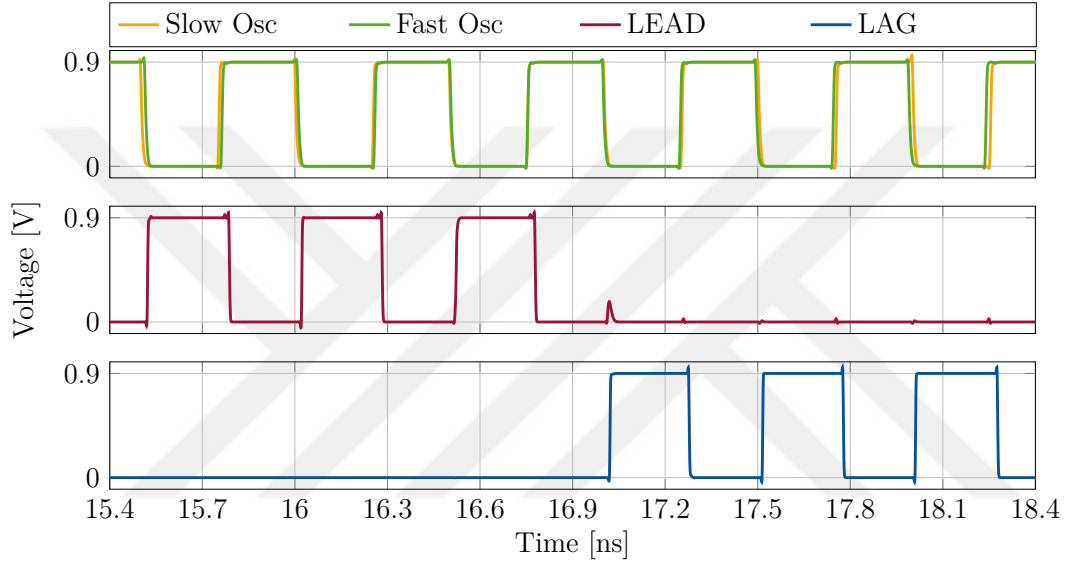


Figure 3.13: Operation of the Arbiter.

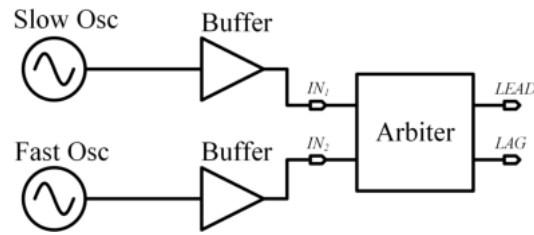


Figure 3.14: GROs and the Arbiter.

The operation is illustrated in Figure 3.13, which is obtained from the setup given in Figure 3.14, where buffers are placed between the oscillators and the arbiter to minimize the disruptive effects of charge/discharge activities in arbiter on the oscillation frequencies.

After the output nodes are reset, the preceding falling edge of either of the input signals triggers the corresponding output to go high, which are named *LEAD* and *LAG* to indicate the temporal position of IN_1 in comparison to IN_2 . When slow and fast oscillators are connected to the input ports of the arbiter, the instance of fast oscillations catching up with the slow oscillations can be detected.

3.6 Logic Control Unit

Logic Control Unit (LCU) is the unit of the TDC which is responsible of controlling the whole operation. It generates the gating signals of slow and fast GROs, and in this way turns them on or off, as required. Coincidence detection is also finalized in this unit by utilizing the output signals of the arbiter. The duties of the LCU can be summarized under four main headings:

1. Controlling the activity of the slow and fast GROs: As soon as *START* and *STOP* signals are received, the LCU has to turn on the slow and fast GROs respectively.
2. Validating the rising edge of the *STOP* signal: Input time difference is bounded by the rising edges of *START* and *STOP* signals, respectively. As discussed previously, a periodic reference clock is used as the *STOP* signal. Therefore, *STOP* signal rising edges arriving before the *START* signal is received, must be disregarded.
3. Coincidence detection: The output signals of the arbiter need to be utilized and evaluated in the LCU so that the conclusion of a coincidence detection can be reached. After coincidence, the slow and fast oscillators are required to be turned off as soon as possible to keep the power consumption to a minimum.
4. Resetting the TDC after each conversion: After a time-to-digital conversion is completed, the LCU has to reset the system to its initial status so that a new conversion cycle can begin.

The schematic diagram of the LCU design is shown in Figure 3.15. It consists of four subunits: System Reset, Coincidence Detection, Slow Oscillator Controller and Fast Oscillator Controller.

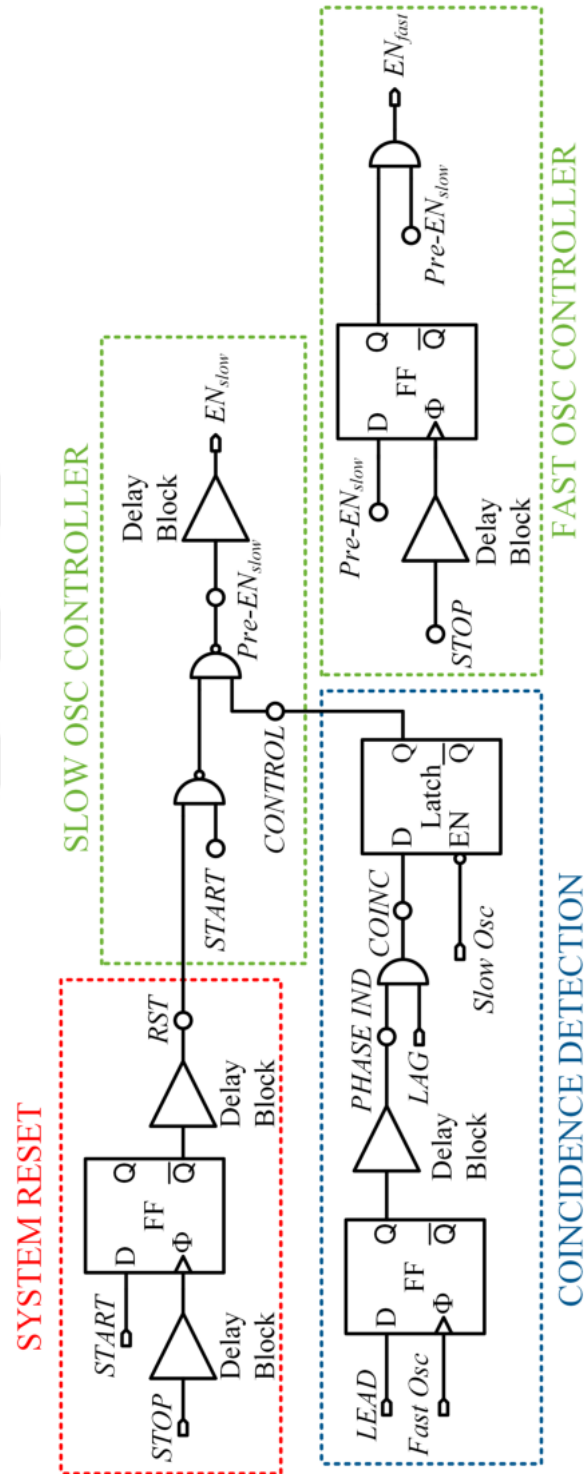


Figure 3.15: Schematic Diagram of the LCU.

3.6.1 System Reset

The duty of the system reset subunit, which is shown in Figure 3.16, is to generate the binary *RST* signal which conveys the information that either the system is in idle state and ready for the start of a new conversion cycle, or the system is in the operational state and disables the control of the *START* signal over the slow oscillator activity, as shown in Table 3.6.

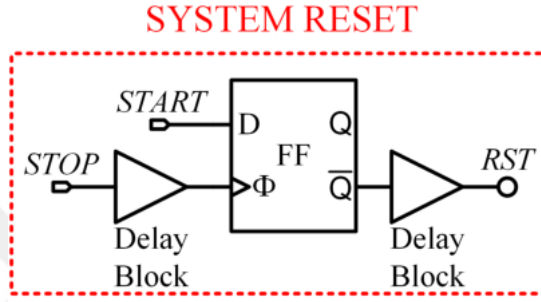


Figure 3.16: Schematic Diagram of the System Reset Subunit.

Table 3.6: *RST* Signal States.

<i>RST</i> Level	System Description
Low	Operational State
High	Idle State

In the idle state, the reception of the *START* signal turns on the slow oscillator by prompting its gating signal EN_{slow} to go high. Since *START* signal received from a sensor of the D-SiPM is expected to remain high longer than 100 ns, as illustrated in Figure 2.2, the control of *START* signal on EN_{slow} needs to be ceased after some time, so that the slow oscillator can be turned off after the time-to-digital conversion is finished. *STOP* signal is utilized for this purpose and connected to the *clock* input port of a DFF which samples the level of the *START* signal as shown in Figure 3.15. When the *START* signal is sampled in its high level, *RST* signal goes low to its operational state and the slow oscillator is liberated to be turned off after coincidence, as shown in Figure 3.17. A delay block (buffer chain) is placed between *STOP* signal and the DFF so that the system can also work for very small input time differences between *START* and *STOP*, due to the setup time limitation of the DFF.

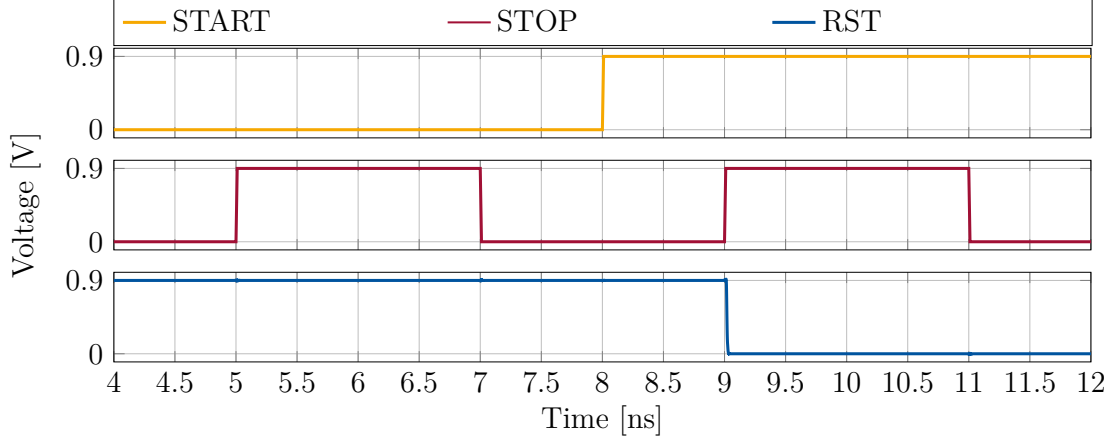


Figure 3.17: Operation of the System Reset Subunit-1.

Utilization of *STOP* signal to remove the control of *START* signal on the slow oscillator activity creates a challenge for the design in the case of small input time difference values less than approximately 50 ps: *RST* signal goes to its operational state before *CONTROL* signal can take over the duty of controlling EN_{slow} . This necessitates the usage of a delay block (buffer chain) in the path of the *RST* signal so that even for small time differences between *START* and *STOP*, a smooth transition of control can be realized and the disruptions in EN_{slow} can be prevented. After the time-to-digital conversion is completed and *START* signal goes to low level, this instance is sampled by the DFF and the *RST* signal returns to its idle state as shown in Figure 3.18

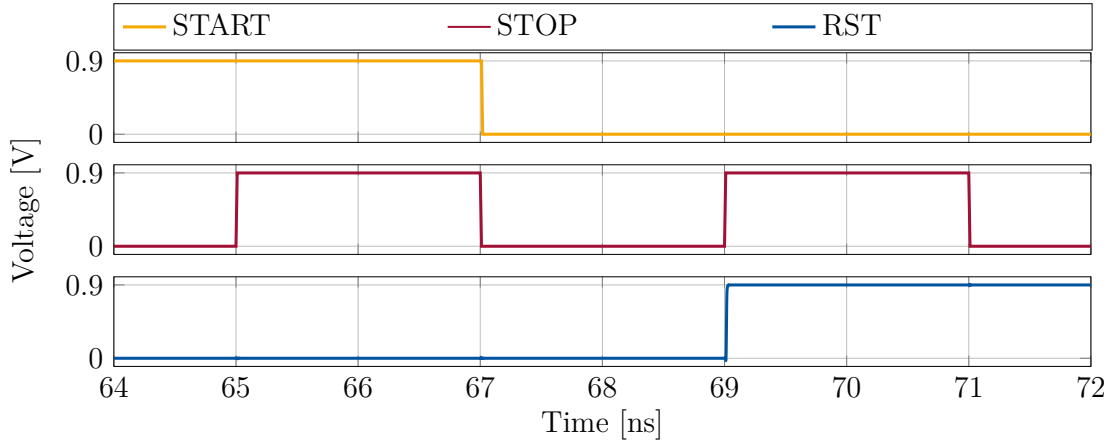


Figure 3.18: Operation of the System Reset Subunit-2.

3.6.2 Coincidence Detection

The first duty of coincidence detection subunit, which is shown in Figure 3.19, is to assume the control of the slow oscillator after *RST* signal goes into operational state. Its second duty is to make the decision that the coincidence of the slow and fast oscillator signals has occurred. Its operation is best understood by examining the input, output and internal signal waveforms of the LCU during a complete time-to-digital conversion cycle. Two example set of waveforms are presented in Figure 3.20 and Figure 3.21.

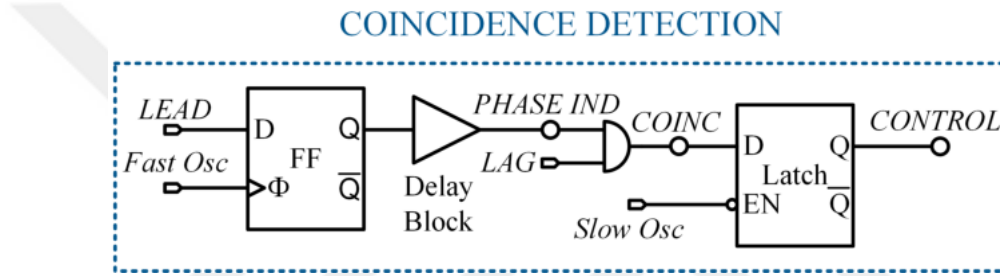


Figure 3.19: Schematic Diagram of the Coincidence Detection Subunit.

LAG signal marks the instance of fast oscillator signal catching up with the slow one, but it is not sufficient by itself to reach the conclusion of a coincidence. There are two different scenarios of how the fast oscillator signal falling edge can be located in relation to slow oscillator signal: either when the slow oscillator signal is at low level or at high level, depending on the vernier mode input time difference being smaller or larger than 250 ps, respectively. These two scenarios are illustrated in Figure 3.20 and Figure 3.21.

In the first scenario, there is no need for any additional signals and the coincidence can be detected by following only the *LAG* signal level. However, in the second scenario, during the time frame when both oscillator signals are at high level, the arbiter output signals *LEAD* and *LAG* are both reset, and since the fast oscillator falls to low level prior to slow one, *LAG* signal is activated as shown in Figure 3.21. The second scenario necessitates to distinguish between these two cases, and this is achieved by creating the *PHASE IND* (*PI*) signal.

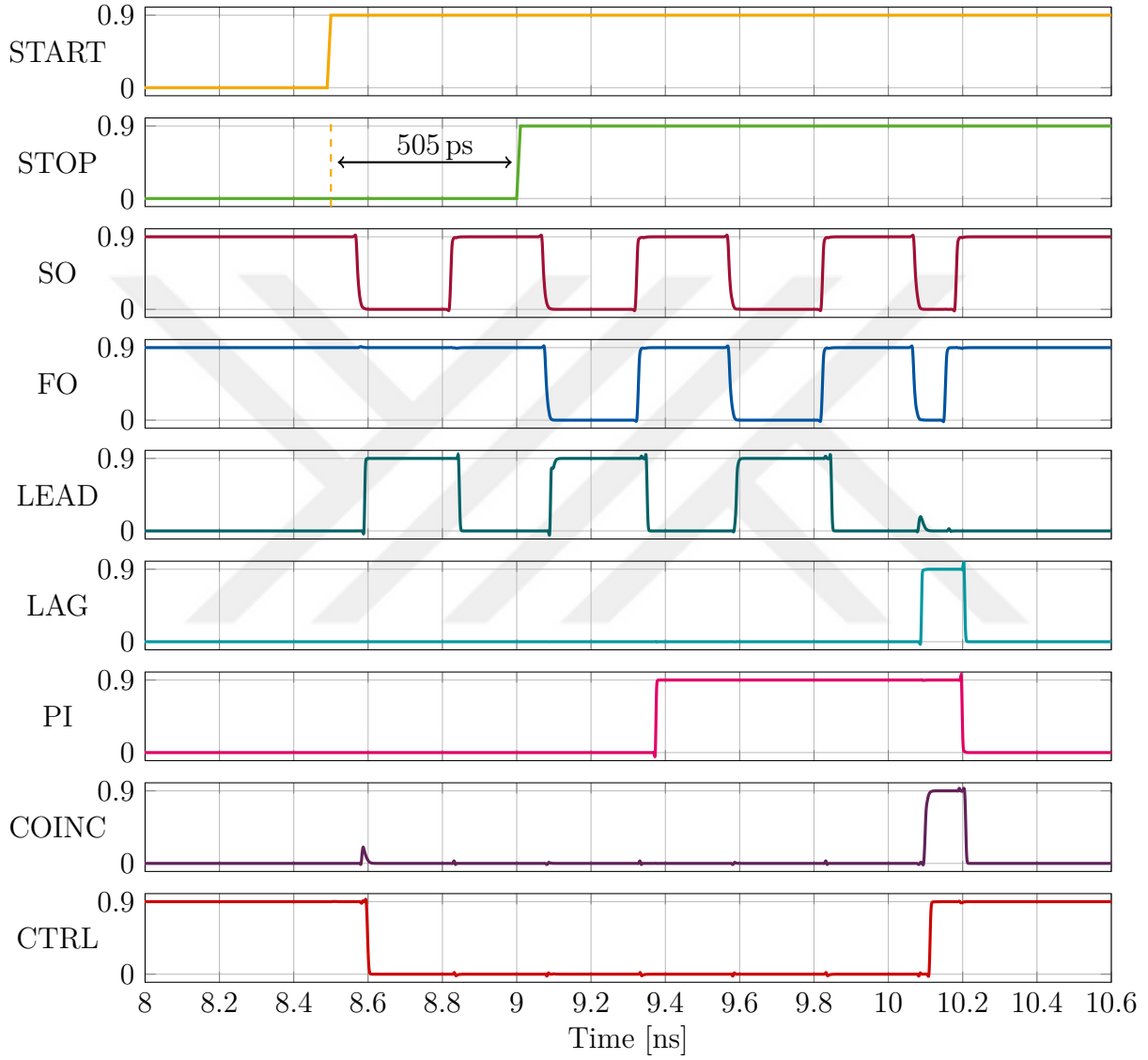


Figure 3.20: LCU Signal Waveforms during a Conversion Operation-1.

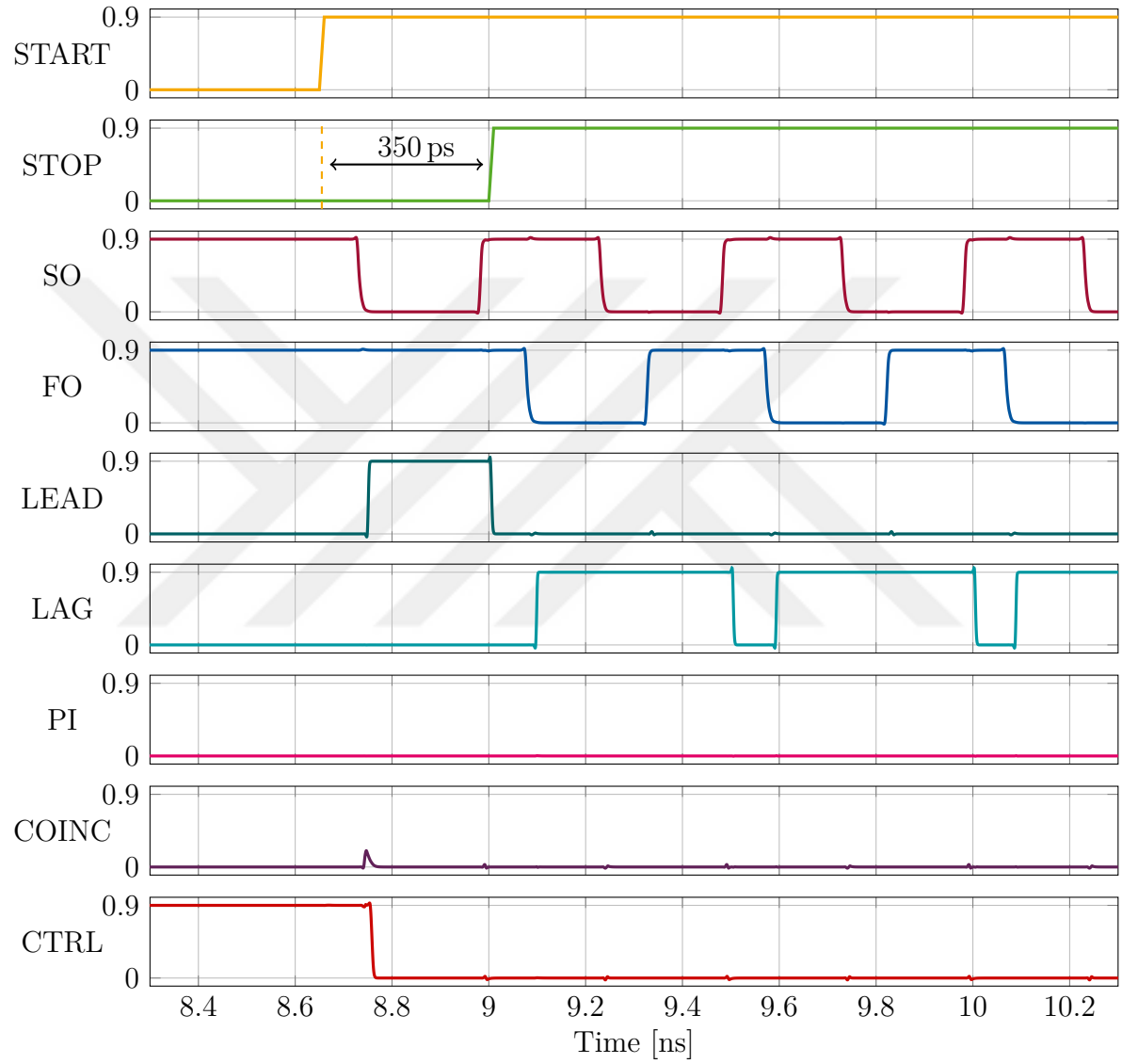


Figure 3.21: LCU Signal Waveforms during a Conversion Operation-2.

PI signal is generated by sampling the *LEAD* output signal of the arbiter with a DFF in which the fast oscillator (*FO*) signal is used as the clock. When the falling edge of the *FO* signal coincides with the low level of the slow oscillator (*SO*), this is indicated by the *PI* signal going high, as shown in Figure 3.20. In the case of larger than 250 ps vernier mode input time difference, however, *PI* signal remains low until the above-mentioned condition is satisfied in the later stages of the operation, as shown in Figure 3.21. A delay block (buffer chain) is used in the path of the *PI* signal to ensure a smooth latching action in the following D latch.

Coincidence detection process can be finalized by combining the *PI* and *LAG* signals in an AND operation and generating the *COINC* signal, which conveys the sole information of coincidence detection whenever it goes to high level.

3.6.3 Control of the Oscillators

The subunits of slow and fast oscillator controllers are shown in Figure 3.22. Shortly after the reception of *START* signal, the slow oscillator is turned on, and this consequently activates the D latch whose data input is connected to *COINC* signal and the clock input is connected to *SO* signal. Until the coincidence detection is indicated by the *COINC* signal, the *CONTROL* signal generated by the D latch keeps the slow oscillator on, which in turn provides the clock signal of the latch, forming a feedback loop. *CONTROL* signal is connected to a NAND gate which actually functions as an 'OR gate for 0 (low) level'. After the coincidence, the *CONTROL* signal goes high and turns off the slow oscillator as EN_{slow} drops to low level. A D latch instead of a DFF is used in this part of the LCU because it is desired that *CONTROL* signal is generated as soon as possible to take over the control of the slow oscillator before the *RST* signal attains its operational state and ceases the control.

The control of the fast oscillator is closely integrated with the slow one due to the nature of the vernier technique. *STOP* signal is desired to turn on the fast oscillator only if *START* signal has already been received and the slow oscillator is ON. However, the information that the slow oscillator is ON cannot become available immediately, since the signal propagation through logic gates and the charging of the nodes must take some time.

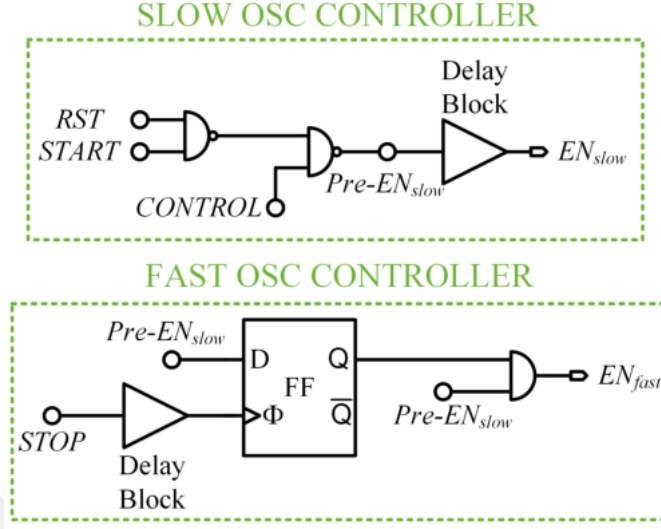


Figure 3.22: Schematic Diagram of the Oscillator Controller Subunits.

This causes problems in the operation for very small input time differences. In order to overcome this issue, a delay block (buffer chain) is placed before the EN_{slow} output and the $Pre - EN_{slow}$ signal is generated. $Pre - EN_{slow}$ signal is sampled by a DFF in which $STOP$ signal is used as the clock. Whenever the $STOP$ signal rising edge is received after $Pre - EN_{slow}$ is high, the gating signal of the fast oscillator, EN_{fast} , also goes high and the fast oscillator is turned on. A delay block of approx. one T_{LSB} larger value than the above-mentioned block is also placed between $STOP$ signal and the clock input port of the DFF in order to preserve the input time difference value. The delay is increased by approx. one T_{LSB} so that the starting point of the TDC range can be shifted to 0 ps from 5 ps. This extra delay is taken into account when obtaining the conversion result, as explained in section 3.7.

Since the fast oscillator is not required to run independently from the slow one, the gating signal of the slow oscillator can also be utilized to turn it off. This is realized by combining the output of the above-mentioned DFF with the $Pre - EN_{slow}$ signal in an AND operation to create the EN_{fast} signal. In this way, whenever the slow oscillator is turned off after the coincidence detection, the fast oscillator is automatically turned off as well.

3.7 Counters

Counters constitute the final main unit of the TDC. Their duty is to count the number of oscillation cycles in the GROs and output the result in the binary format. For this purpose, one slow oscillation counter and one fast oscillation counter are needed. Maximum numbers that each counter should be able to reach are given in (3.3) and (3.4) where $C_{s,max}$ and $C_{f,max}$ denote the slow and fast ones, respectively. The values of $C_{s,max}$ and $C_{f,max}$ reveal that both counters need to have seven bits in order to cover the whole range.

$$C_{s,max} = \left(\frac{T_{stop}}{T_s} - 1 \right) + \frac{T_s}{T_{LSB}} = 107 \quad (3.3)$$

$$C_{f,max} = \frac{T_s}{T_{LSB}} = 100 \quad (3.4)$$

A pair of 7-bit synchronous binary counters are designed by using Verilog Hardware Description Language (HDL). The source code is provided in Appendix. The two counter blocks are illustrated in Figure 3.23. The number of falling edges in the oscillation signals are counted and the output bits are reset when the *START* signal goes to low level after the end of a conversion cycle.

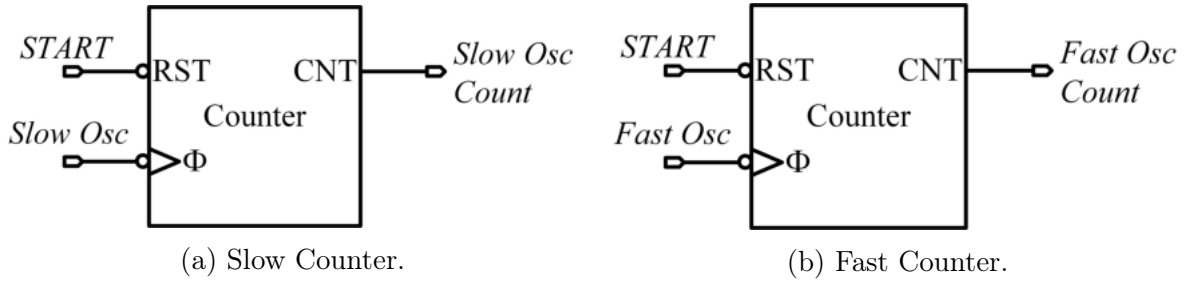


Figure 3.23: Counters.

The time-to-digital conversion result is obtained by the slow oscillation count (*SOC*) and the fast oscillation count (*FOC*) as given in (3.5). An additional T_{LSB} is subtracted in order to compensate for the additional one T_{LSB} delay created by the delay block in fast

oscillator controller subunit, as explained in subsection 3.6.3.

$$Conv.Result = (SOC - FOC) \cdot T_s + (FOC - 1) \cdot T_{LSB} - T_{LSB} \quad (3.5)$$

For example, in the conversion operation illustrated in Figure 3.20, $SOC=4$ and $FOC=3$, so the conversion result is equal to 505 ps.

4 Results

In this chapter, the results of the simulations that have been performed on the TDC are presented. These simulations are designed to assess the overall performance of the TDC unit as a whole, which is illustrated in Figure 4.1 with its input, output signals and five constituent subunits: slow oscillator, fast oscillator, arbiter, LCU and counters.

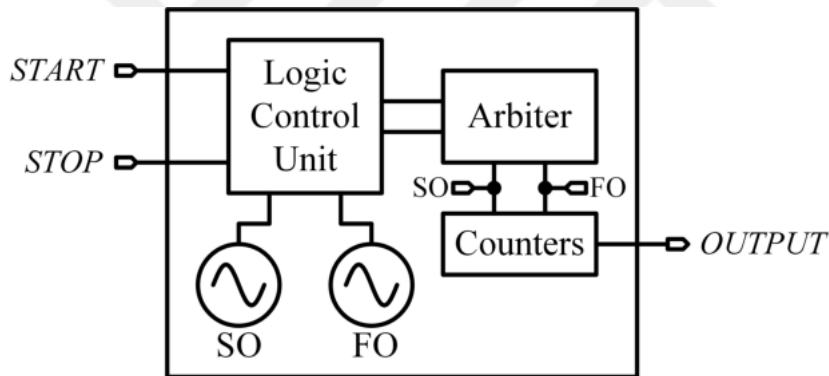


Figure 4.1: Overall Structure of the TDC.

4.1 Transfer Function

The first simulation to carry out on the TDC is to create its transfer function by sweeping the input time difference values for the whole range and obtaining the corresponding output digital codes. Each digital code represents a conversion result, e.g. code 1 - 5 ps, code 2 - 10 ps etc.

The simulation is performed for the nominal case as well as the four front end of line (FEOL) process corners to study the effects of PVT variations on the transfer function. These four corners are named FF (fast-fast), SS (slow-slow), FS (fast-slow) and SF (slow-fast), where the first letter denotes the NMOS corner and the second one the PMOS corner. They represent the most extreme cases of PVT variation and result in either higher or lower carrier mobilities.

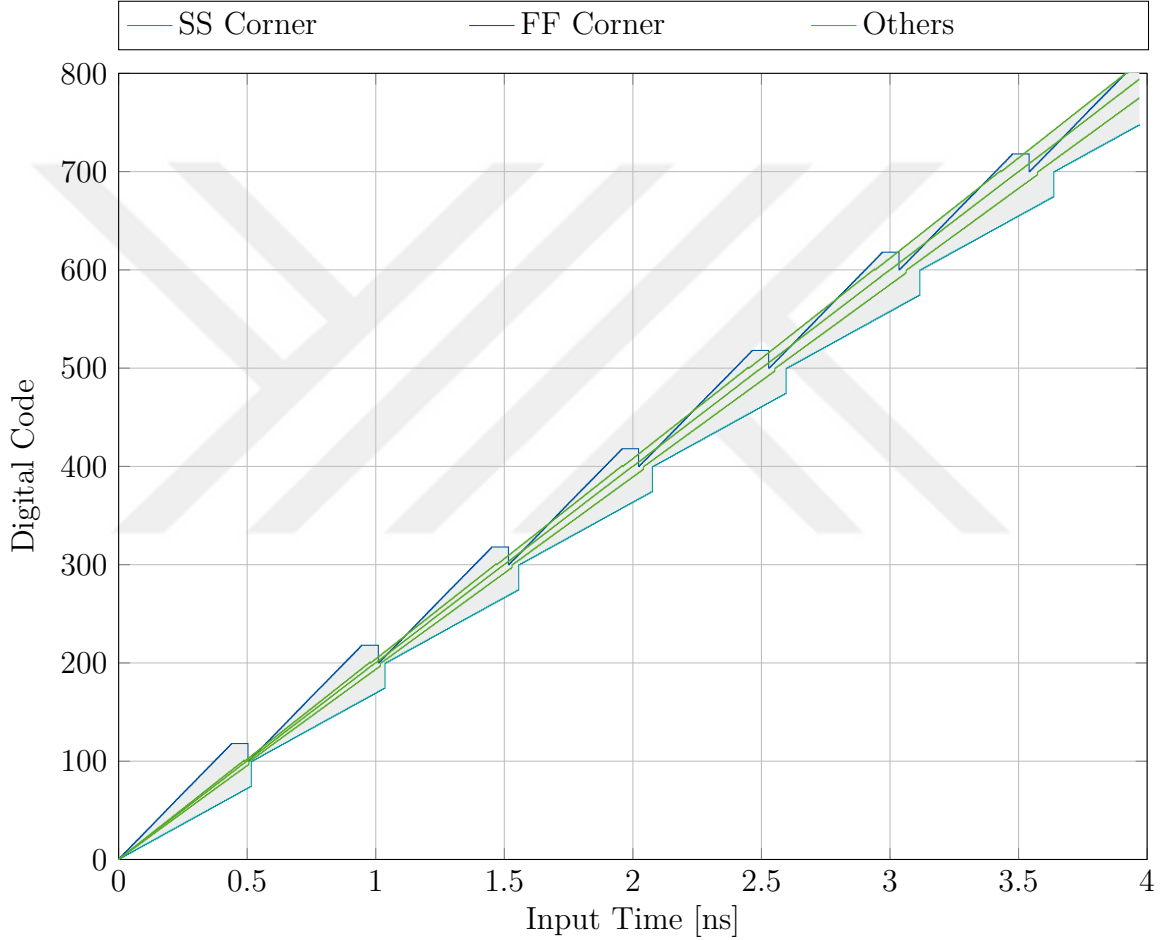


Figure 4.2: Transfer Function of the TDC.

Transfer function of the TDC for the nominal corner and the other four corners is given in Figure 4.2. It is seen that the transfer function for the SS corner regularly gives smaller output codes than the nominal case through the vernier mode of the TDC, and closes this gap with each new coarse mode cycle, as indicated by the missing codes in the curve.

Transfer function for the FF corner shows a similar behavior in the opposite direction to the SS one, and therefore, forms a non-monotonic transfer characteristic. It can also be seen that the FF corner transfer function gets limited regularly through the end of each vernier mode due to limitations placed by the maximum range of counters.

There are two reasons behind the deviations observed in the transfer functions for the corners. The first one is the variation in the difference between the slow and fast oscillator frequencies/periods. The second one is the individual variation in the slow oscillator frequency/period. A period difference greater than 5 ps results in the fast oscillator edge catching up with the slow one in less oscillation cycles, which consequently produces smaller output codes than normal, as in the case of SS corner. A period difference less than 5 ps similarly causes a deviation of the transfer curve in the opposite direction, as in the case of FF corner. Transfer functions for SF and FS corners mostly lie in the range between these two extreme cases. The individual variation in the slow oscillator frequency also increases the deviation by causing inaccuracy in the coarse mode element of the conversion result equation (3.5). These two effects exhibit an accumulative behavior as the number of cycles involved in the calculation increases.

4.2 Linearity

The linearity of the TDC is quantified by Differential Nonlinearity (DNL) and Integral Nonlinearity (INL). These parameters are calculated by sweeping the input time difference for the whole dynamic range from 0 ps to the end by 1 ps increments and using equations (2.4) and (2.5) for each digital code. The resulting graphs for the nominal and the SS corner are given in Figure 4.3. The SS corner is selected in addition to the nominal one for its monotonic transfer function and representing the maximum distortive effects of PVT variations.

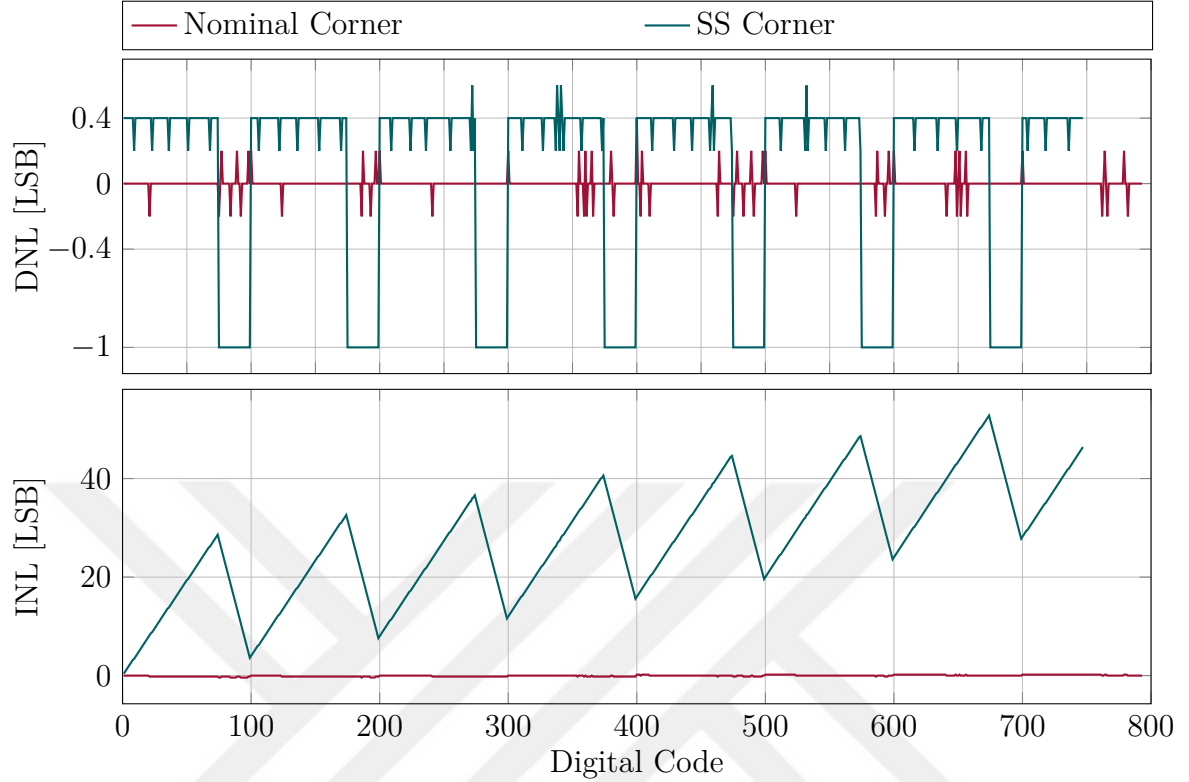


Figure 4.3: DNL and INL.

Figure 4.3 shows a rather discrete characteristic because the time increment of the simulation (1 ps) is relatively large in proportion to the LSB (5 ps). This yields a resolution of 0.2 LSB for the DNL calculation. Achieving a smaller value is not feasible due to huge computational loads of a simulation with smaller increments. The accumulative effect of the deviations in SS corner transfer function brings about the regular increase observed in INL as the output code increases. Another observation about the graph is the correspondence between the missing codes in the transfer function and the codes with a DNL of -1 LSB.

4.3 Timing Accuracy

The timing accuracy (precision) of the TDC is quantified by sweeping the entire range of the input time difference values and obtaining the jitter value for each code by examining the

distribution of the corresponding input values [4]. Standard deviation of the distribution is computed for each code by assuming equal probability for each input time difference value (uniform distribution). The resulting graph of jitter for the nominal and the SS corners are given in Figure 4.4. A strong correlation is observed between the INL and jitter graphs since the timing accuracy degrades with increasing INL. The average jitter for the nominal case is found as 2 ps rms.

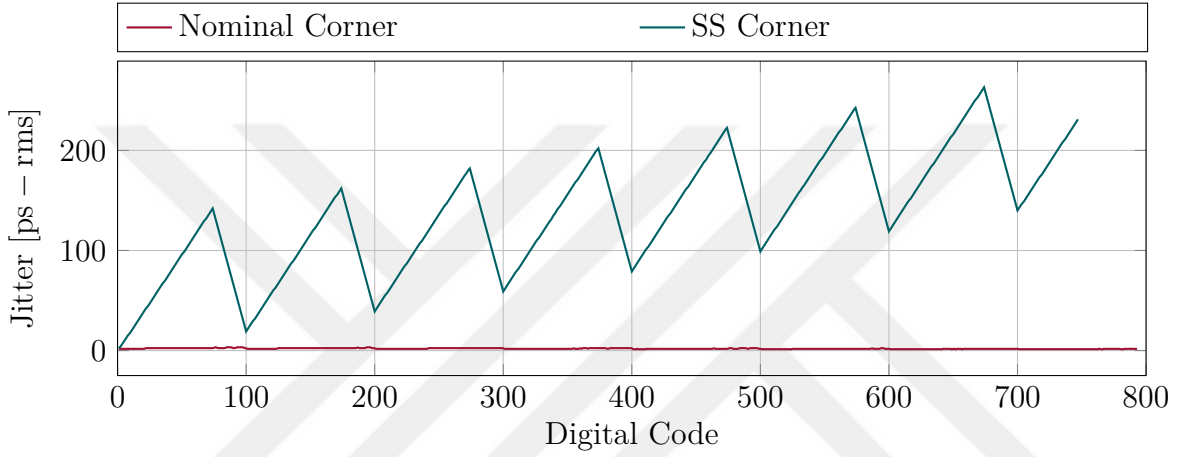


Figure 4.4: Timing Accuracy of the TDC.

4.4 Power Consumption

Power consumption of the TDC is divided into power consumption during conversion and power consumption in the idle state. Power consumption during conversion depends on the value of the input time difference since it changes the number of cycles in the oscillators. The average power consumption for each code is computed by sweeping the input time difference with 1 ps increments and taking the time frame from the reception of *START* signal until the coincidence detection and the end of conversion, to calculate the power consumption during conversion. The resulting graph is given in Figure 4.5. Overall average power consumption during conversion is found as 130 μ W. The distribution of this value among the units of slow oscillator, fast oscillator, arbiter and LCU is illustrated in

Figure 4.6. Fast oscillator value is found to be lower than slow one. This is a result of the cases in which the fast oscillator is not operational for the whole time frame of conversion. Power consumption in the idle state is found as $5.6\mu\text{W}$.

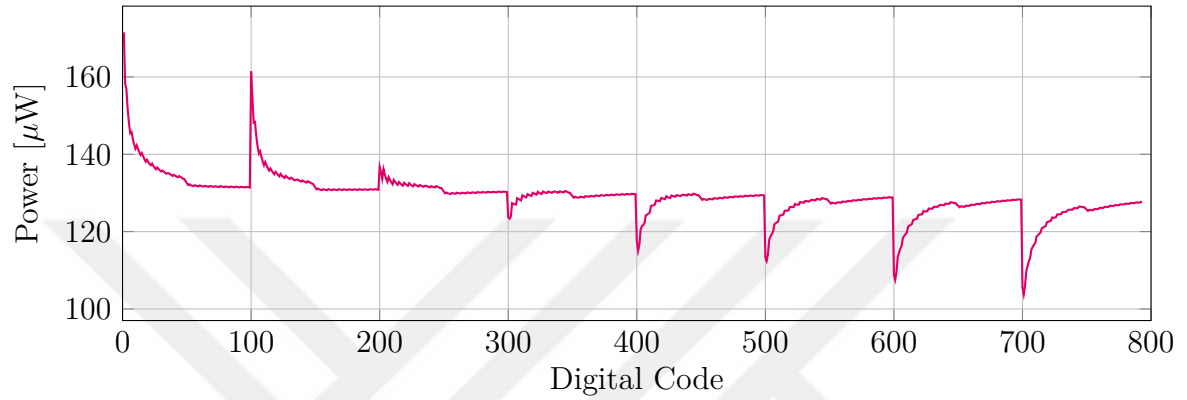


Figure 4.5: Average Power Consumption of the TDC during Conversion.

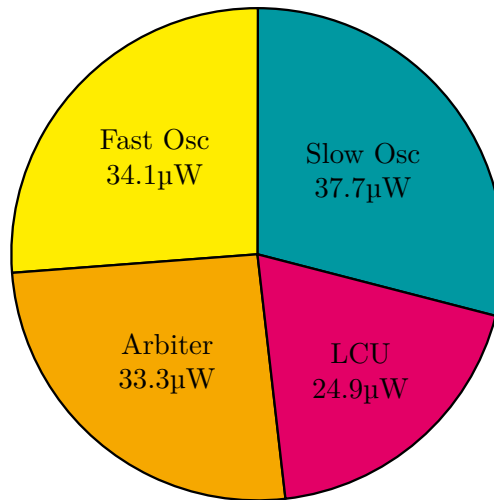


Figure 4.6: Average Power Consumption of each Unit.

4.5 Summary and Comparison

The results of the simulations performed on the TDC to determine its performance parameters are summarized in Table 4.1 for the nominal conditions. Comparison with the TDC specifications, and three similar and recent works in the literature are also provided in Table 4.1.

Table 4.1: Summary of the TDC Performance.

Parameter	Nominal Result	Specification	[1]	[15]	[9]
Technology	28 nm	28 nm	65 nm	40 nm	65 nm
Resolution (LSB)	5 ps	5 ps	15 ps	40 ps	5.1 ps
Jitter	2 ps rms	< 4 ps rms	6.9 ps rms	-	5.5 ps
Conversion Time	58 ns	< 100 ns	15.5 ns	15.6 ns	-
Dynamic Range	3.97 ns	4 ns	3 ns	1 μ s	4 ns
DNL	0.4 LSB	< 1 LSB	0.5 LSB	0.1 LSB	-
INL	0.4 LSB	< 1 LSB	0.8 LSB	1 LSB	-
Av. Power Cons.	130 μ W	Minimum	160 μ W*	171 μ W	22 μ W*

Conversion time is obtained by adding the system reset period of 4 ns to the theoretical value given in (2.18).

Dynamic range is less than the target value of 4 ns because the TDC is unable to correctly convert the input time difference values in the last approx. 30 ps of the targeted dynamic range. The delay blocks which are used in the LCU make it possible to detect very small input time difference values. However, when *STOP* signal arrives right before *START* signal, i.e. in the end of the dynamic range, these delay blocks distort the formation of accurate logic states and result in incorrect 0 ps conversion result. If required, a slight increase in the period of *STOP* signal could be a simple method to reach the intended value.

The results show that, under nominal conditions, the TDC meets all specifications except a very slight reduction in dynamic range. However, when the effects of PVT variations are taken into account, significant deviations from the nominal results are observed. Therefore, a calibration mechanism, which is able to adjust the oscillator frequencies by tuning the control voltages of the delay cells in the GRO, is required in order to keep the performance

of the TDC within specifications for the nonnominal conditions as well. Such a calibration can be realized by using the *STOP* signal as a reference to first adjust the slow oscillator period by counting the number of oscillation cycles in a certain time frame, and then adjusting the fast oscillator period similarly by counting the number of oscillations it takes for the two signal edges to catch up with a certain initial time difference. A HDL based circuit can be synthesized to implement the necessary algorithm, while a DAC is needed to obtain the analog control voltages in the end.

In Table 4.1, average power consumption values with an '*' sign are calculated by using a different approach to this work. These are calculated by assuming a certain value of events per second. For example, 22 μ W value provided in [9] is obtained by assuming a single event in every 100 μ s. Running our TDC in the same setting would yield an average power consumption of 5.7 μ W, which is almost equal to the idle state consumption.

Comparing the obtained results with similar work in the literature given in Table 4.1, this work stands out with its high resolution and low average power consumption during conversion and idle state. In addition to advantages provided by the more advanced technology, this is achieved through the LCU, which is a custom design for the specific requirements of the application. The operation is optimized to run as efficient as possible by preventing unnecessary power consumption, for instance, by running the power hungry oscillators only when it is required and turning them off as soon as the conversion is finished.

Finally, it should be noted that the three works ([1], [15], [9]) provided in the table are in the advanced stages of the implementation and the given results are obtained by performing tests on the fabricated TDC.

5 Conclusion and Outlook

The design and implementation of a TDC for SiPM applications has been presented in this thesis. In this chapter, the work is summarized and an assessment of the obtained results is presented, as well as an outlook for future work.

5.1 Conclusion

The work that has been carried out can be summarized as follows. Firstly, literature research has been conducted to determine the available TDC architectures which are frequently used in leading SiPM applications. After deciding on vernier GRO architecture with the slow oscillator period of 500 ps and the fast oscillator period of 495 ps, four different options for the delay cell architecture have been determined. Extensive simulations have been performed on these four architectures to select the most suitable one for the application because the delay cell is the core building block of the RO and, therefore, has a big impact on the overall performance. Having finalized the GROs, an arbiter circuit is implemented which detects the coincidence of two oscillator signals. An application specific LCU is designed to control the whole operation of the TDC with a specific emphasis on keeping the power consumption to a minimum. TDC design is finalized with the implementation of the counters through Verilog HDL.

The results of the simulations performed on the TDC show that, under nominal conditions, it meets all specifications except a very slight reduction in dynamic range. When compared with similar and recent works in the literature, this work stands out with its high resolution and low power consumption. The resolution is 5 ps, and the power consumption in idle state is a mere 5.6 μ W, while the consumption during conversion is 130 μ W. This is

achieved with the custom-made LCU that strives to run the operation as efficient as possible.

5.2 Outlook

The study of the PVT variation effects reveal significant deterioration in linearity and consequently timing accuracy of the TDC. Future work is needed to ensure the performance meets the specifications under nonnominal conditions as well, by compensating for these effects through a calibration mechanism which can tune the slow and fast oscillation frequencies to their nominal values. This mechanism could be realized by using a certain algorithm, e.g. Successive Approximation Register (SAR), to adjust the control voltages of GRO delay cells with the help of a DAC.

SiPM application requires many TDCs to be placed in close proximity to each other. This configuration could lead to some mutual disturbance effects between individual TDC units. Noisy power supply simulation is performed in the selection process of the delay cell architecture to emulate the possible undesired effects of this end configuration on the GROs. This investigation can be expanded before moving on to layout and fabrication stages.

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6 Appendix

6.1 Counter Verilog HDL Listing:

Verilog HDL code to realize the counters is provided below.

```
module counter(clk , reset_N , count);  
  
    // Port Declaration  
    output [6:0] count;  
    input clk , reset_N;  
    reg [6:0] cnt;  
  
    //Initial counter reset  
    initial  
    begin  
        cnt = 7'b0000000;  
    end  
  
    always @ (negedge clk , negedge reset_N)  
    if(~reset_N) cnt <= 7'b0000000;  
    else cnt <= cnt + 1'b1;  
  
    assign count=cnt;  
  
endmodule
```

Figure 6.1: Counter Verilog HDL Listing.

6.2 MATLAB Evaluation Script

MATLAB script to obtain the linearity, the timing accuracy and the average power consumption data of the TDC is provided below.

```
%Read the TDC results
data=readmatrix('tdc_results.csv');
digital=round(data(:,2)./1e-12);
time=round(data(:,1)./1e-12);
power=data(:,3);

pow_con=mean(power);
n=3965; %Maximum conversion result
m=3971; %Length of the data array
%DNL of each code
dnl=((sum(digital(:) == (5:5:n)))./5) - ones(1,n/5);
inl=cumsum(dnl); %INL of each code
var=((time-digital).^2);
for s=5:5:n
    prob=zeros(m,1);
    pow_run_avg=zeros(m,1);
    for j=1:m
        if digital(j,1)==s
            %Uniform distribution for each code
            prob(j,1)=1./sum(digital(:) == s);
            pow_run_avg(j,1)=power(j,1);
        else
            end
        end
    end
    %Timing accuracy for each code
    jitter(s/5)=sqrt(sum(prob.*var)).*1e-12;
    %Average power con. for each code
    pow_per_code(s/5)=sum(pow_run_avg)./sum(pow_run_avg~=0);
end
```

Figure 6.2: MATLAB Evaluation Script.

7 Presentation Slides

7.1 First Master Thesis Presentation

Design and Implementation of a Time-to-Digital Converter for digital Silicon Photomultipliers

Ismail Oguz Erdal
First Master Thesis Presentation

Supervisors: Alexander Meyer, M.Sc.
Tim Lauber, M.Sc.

Univ.-Prof. Dr.-Ing. Stefan Heinen
Integrated Analog Circuits and RF Systems Laboratory

IAS RWTH AACHEN UNIVERSITY

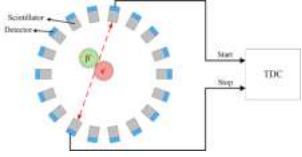
Outline

- Motivation
- TDC Requirements
- TDC Architectures
- Vernier GRO Architecture
- RO Delay Cell Architectures
- Simulation Results
- Architectural Specifications
- Outlook

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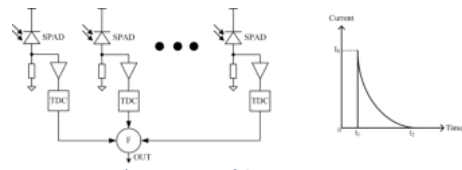
Motivation

- Highly accurate photon time-of-flight measurements are critical for advancements in
 - Positron Emission Tomography (PET)
 - High Energy Physics (HEP) applications



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Silicon Photomultiplier (SiPM)



- Integrates a dense array of SPAD sensors
 - A single absorbed photon can trigger macroscopic current flow
- Radiation detector with extremely high sensitivity
- Focus on integrating dSiPM and TDC in a single cell
- Successful implementation requires TDCs with:
 - Low resolution / high precision
 - Low power consumption / small footprint

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TDC Requirements

Parameter	Requirement
Technology	TSMC 28 nm
Supply voltage	0.9 V
Resolution (LSB)	< 5 ps
Conversion Time	< 100 ns
DNL / INL	< 1 LSB
Reference CLK	250 MHz
Dynamic Range	4 ns
Jitter	< 4 ps rms

- Mutual disturbances caused by array of TDCs to be studied
- PVT variations should be compensated
- P_T and A_T should be as low as possible

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TDC Architectures

- Delay Line TDC
 - Thermometer code output
 - Resolution limited by per-stage delay

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TDC Architectures

- Vernier Delay Line TDC
 - Sub-stage delay resolution possible
 - $T_{LSB} = \tau_1 - \tau_2$
 - Differential operation
 - Capable of minimizing first order common-mode disturbances
 - Increased P_T and A_T / reduced range

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TDC Architectures

- Gated Ring Oscillator Based TDC
 - Oscillator turned on/off by gating signal
 - Large dynamic range possible
 - Oscillation frequency not feasible for ps range resolution
 - $T_{LSB} = T_{OSC} = 2n\tau$, n = number of stages

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TDC Architectures

- Vernier GRO Based TDC
 - Combines the advantages of GRO with Vernier operation
 - Fine resolution
 - $T_{LSB} = T_s - \tau_r = 2n(\tau_s - \tau_r)$
 - Relatively long conversion time

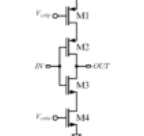
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Vernier GRO Architecture

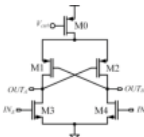
- $T_{meas} = n_c \times T_{slow} + n_v \times T_{LSB}$
- Trade-off between conversion time / jitter and P_T

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RO Delay Cell Architectures



Current Starved Inverter

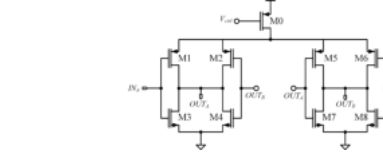


Differential Inverter with PMOS Regulation

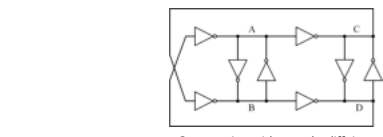
- Single-ended topology
 - Direct modulation of f_o by V_{DD}
 - $\tau \sim \frac{1}{V_{DD}}$
 - Very large supply sensitivity
 - Problem of supply noise
- Differential topology
 - Much lower supply sensitivity
 - Greatly alleviates supply noise problem
 - Higher P_T

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RO Delay Cell Architectures



Pseudo-differential Inverter



2-stage ring with pseudo-diff. inv.

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Simulation Results

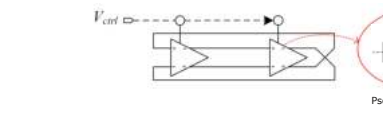
Architecture	Power Cons. (μ W)	Std. Dev. of f_{OSC} (@ 2 GHz) (MC)	Cycle Jitter (ps-rms)	PSRR @ f_{OSC} (dB) (MC)
St. Inv. (3-stage)	22	2.4%	0.72	5
St. Inv. (5-stage)	33	2.4%	0.58	5
Pseudo-differential (2-stage)	81	2.2%	0.43	38 ($\sigma=9$)
NMOS Differential (3-stage)	98	3.9%	1.22	N/A
PMOS Differential (3-stage)	89	2.9%	0.89	N/A

□ Footprints are in the same order of magnitude

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Architectural Specifications

Specification	Value
TDC architecture	Vernier GRO
Delay cell	Pseudo-differential
Number of stages	2
Power consumption per stage	$\sim 40 \mu$ W
T_{slow} / f_{slow}	500 ps / 2 GHz
T_{fast} / f_{fast}	495 ps / 2.02 GHz



Pseudo-differential Inverter

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Outlook

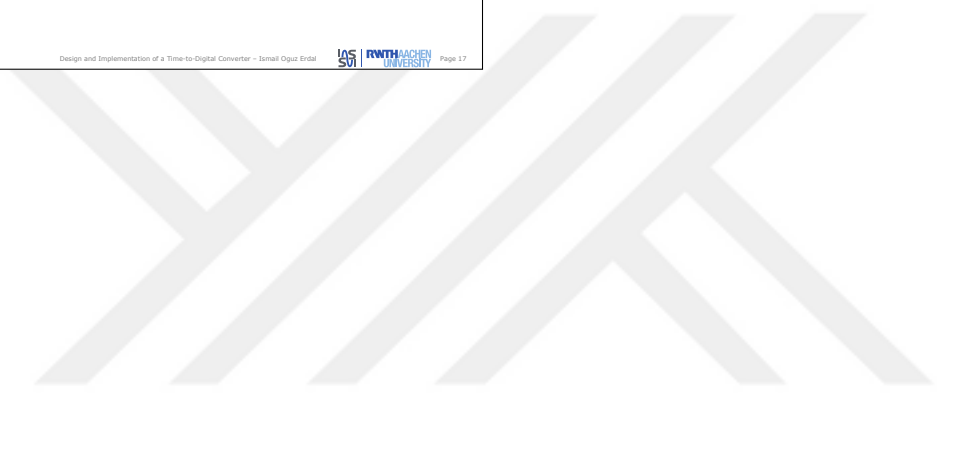
- Control logic design
- Coincidence circuit
- Study and minimize PVT effects
- Calibration mechanism

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Thank you for your attention!

Appendix

- Jitter
 $\sigma_{osc} \approx \sqrt{n_v \times \sigma_v^2}$
- Max. counter values
 $n_{v, \max} = \frac{T_{slow}}{T_{LSB}}, \quad n_{c, \max} = \frac{T_{slow}}{T_{stop}}$
- Max. conversion time
 $t_{c, \max} = T_{stop} + \frac{T_{slow}^2}{T_{LSB}}$
- Av. Power Cons.
 $P_{av} = f_{osc} \times C \times V_{DD}^2$



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7.2 Second Master Thesis Presentation

Design and Implementation of a Time-to-Digital Converter for digital Silicon Photomultipliers

Ismail Oguz Erdal
Second Master Thesis Presentation

Supervisors: Alexander Meyer, M.Sc.
Tim Lauber, M.Sc.

Univ.-Prof. Dr.-Ing. Stefan Heinen
Integrated Analog Circuits and RF Systems Laboratory



Outline

- Revision of GRO
- Coincidence Circuit
- Logic Control
- Counters
- Measurement Results
- Outlook

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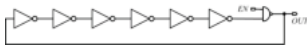


Page 2

Revision of GRO

- New approach to simulating supply noise effects
 - White noise with amplitude of 20 mV p-p added to VDD
 - Effect on jitter simulation result observed
- Enabler block added to the ring
 - Keeps output node voltage fixed when enable signal is low
 - Alternates the input when enable signal is high

IN	EN	OUT
0	0	1
0	1	1
1	0	1
1	1	0



May 2021

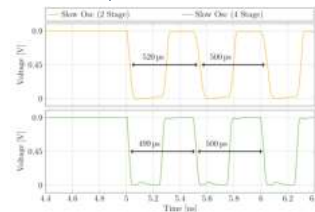
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Page 3

Revision of GRO / Diff. Inv. Simulation

- Stability problems in oscillation frequency discovered
 - Inaccurate frequency of oscillation in the initial phase
 - Number of stages related to the problem
 - Increased from two to four
 - Shift reduced to acceptable values (< 1 ps)
 - 50% increase in P_T



May 2021

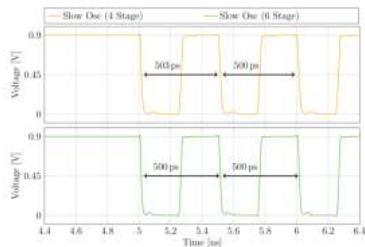
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Revision of GRO / Stv. Inv. Simulation

- Delay cell architecture reconsidered
 - Renewed simulations for GRO based on current starved inv.



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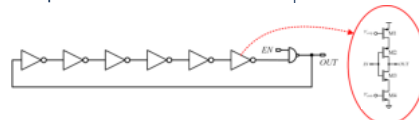


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Revision of GRO

Architecture	Cycle Jitter (ps-rms)	Cycle Jitter (ps-rms) [Noisy Supply]	P_T (μ W) [Fast and slow rings total]
Starved Inverter (6-stage + NAND)	0.59	2.18	73
Pseudo-differential Inverter (4-stage + NAND)	0.43	2.14	305

- Delay cell architecture revised to starved inverter
 - Similar performance with much less P_T



May 2021

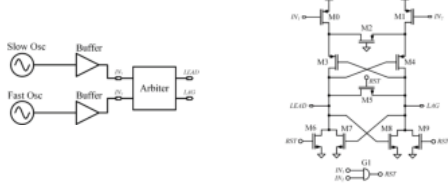
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7 Presentation Slides

Coincidence Circuit



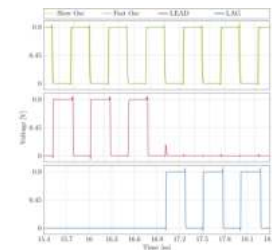
- Arbiter circuit based on an SR latch
 - 2 cross-coupled NOR gates in the core
 - M2 and M5 are balancing transistors
 - RST signal disables latching action i.e., continuous set/reset
 - Output signals reset only when both inputs are high
 - Detects the input signal falling edge which precedes the other

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Coincidence Circuit

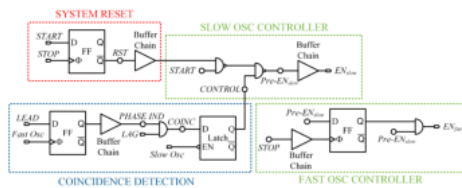


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Logic Control



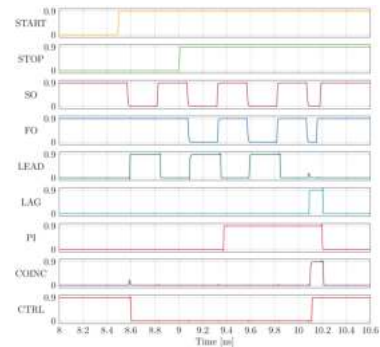
1. Turns on slow and fast oscillators
2. Disregards STOP signal edge that arrives before START
3. Turns off the oscillators after coincidence
4. Resets the system after each measurement

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Logic Control



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Counters

- Pair of 7-bit synchronous binary counters needed
- Implementation through Verilog HDL
- START signal resets the counters after measurement



$$\text{Measurement Result} = [(SOC - FOC) \times 500 \text{ ps}] + [(FOC - 1) \times 5 \text{ ps}]$$

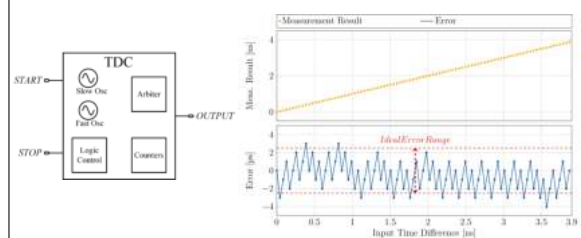
SOC: Slow Osc Count, FOC: Fast Osc Count

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TDC Simulation Results

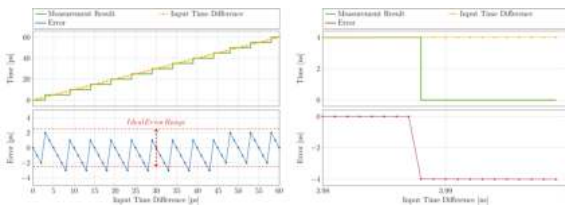


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TDC Simulation Results



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Outlook

- Further study of PVT effects
- Minimization of PVT effects
 - Devising a calibration method
- Working on some minor issues in measurement

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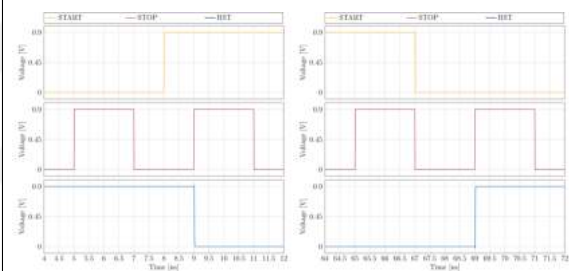
Thank you for your attention!

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Appendix A – System Reset Block

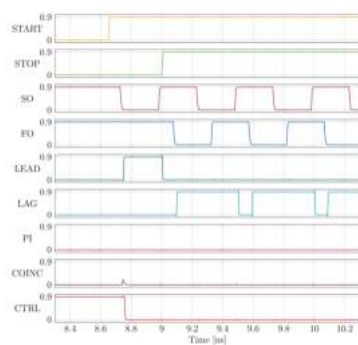


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Appendix B – Purpose of PI Signal



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