DESIGN AND IMPLEMENTATION OF A LOW-NOISE, LOW-POWER AMPLIFIER FOR A 3 TESLA MAGNETIC RESONANCE IMAGING SYSTEM

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Design and Implementation of a Low-Noise, Low-Power Amplifier for a 3 Tesla Magnetic Resonance Imaging System
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We certify that we have read this thesis and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

DESIGN AND IMPLEMENTATION OF A LOW-NOISE, LOW-POWER AMPLIFIER FOR A 3 TESLA MAGNETIC RESONANCE IMAGING SYSTEM

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Magnetic Resonance Imaging (MRI) is a vital diagnostic tool in modern medicine due to its high spatial resolution, excellent soft tissue contrast, and non-invasive nature. The signal quality in MRI systems is primarily determined by the signal-to-noise ratio (SNR), which is crucial in high-field MRI systems like 3 T scanners. This thesis presents the design and implementation of a low-noise amplifier (LNA) operating at 123 MHz, corresponding to the Larmor frequency of hydrogen nuclei at 3 T. The LNA, based on a single-stage common-source topology using a GaAs pHEMT transistor, achieves a measured gain of 14.5 dB, a noise figure (NF) of 0.64 dB, an input reflection coefficient (S_{11}) of -0.28 dB, and a 1 dB compression input power (P_{in1dB}) of -10.75 dBm. These results were validated against simulations, where the design showed high performance, with a power consumption of only 12.6 mW. The amplifier meets the requirements for MRI receiver systems, ensuring low noise and power consumption. Additionally, another version was implemented with input protection diodes for safe operation. This version achieves a measured gain of 14.9 dB, a noise figure (NF) of 0.79 dB, an input reflection coefficient (S_{11}) of -0.32 dB, and a 1 dB compression input power (P_{in1dB}) of -9.65 dBm. This version also achieved 3.5 μs recovery time after 14 dBm of input power was applied for 1 ms. Key challenges such as impedance matching to short circuit, bias network, and input protection circuit are addressed in the design.

Keywords: Low Noise Amplifier, MRI, Signal-to-Noise Ratio, Larmor Frequency, GaAs pHEMT, RF Design.

ÖZET

3 T MANYETİK REZONANS GÖRÜNTÜLEME SİSTEMLERİ İÇİN DÜŞÜK GÜRÜLTÜ VE DÜŞÜK GÜÇ TÜKETİMLİ AMPLİFİKATÖRÜN TASARIMI VE UYGULAMASI

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Manyetik Rezonans Görüntüleme (MRI), yüksek çözünürlüklü görseller, mükemmel yumuşak doku kontrastı ve zarar vermeyen doğasıyla modern tıpta önemli bir tanı aracıdır. MRI sistemlerinde sinyal kalitesi, özellikle 3 T gibi yüksek manyetik alanlı sistemlerde kritik olan sinyal-gürültü oranı (SNR) ile belirlenir. Bu tez, hidrojen çekirdeklerinin 3T alan gücü ile ilişkili 123 MHz'de çalışan, düşük güç tüketimli ve düşük gürültü figürlü bir yükselteçin tasarımını ve uygulanmasını sunmaktadır. Tek kademeli ortak kaynak (common-source) topolojisi kullanan bu LNA, GaAs pHEMT transistörüyle tasarlanmıştır ve ölçülen kazancı 14,5 dB, gürültü figürü (NF) 0,64 dB, giriş 1 dB kısılım gücü (P_{in1dB}) $-10{,}75$ dB ve giriş yansıma katsayısı (S_{11}) $-0{,}28$ dB olarak bulunmuştur. Bu sonuçlar, simülasyonlarla doğrulanmış ve tasarım, 12,6 mW güç tüketimi ile yüksek performans sergilemiştir. Yükselteç, MRI alıcı sistemleri için düşük gürültü ve düşük güç tüketimi sağlayarak, sistemin gereksinimlerini karşılamaktadır. Ayrıca, güvenilir çalışma için giriş tarafında koruyucu diyotları olan diğer bir versiyon daha yapılmıştır. Bu versiyonun ölçülen kazancı 14,9 dB, gürültü figürü (NF) 0,79 dB, giriş yansıma katsayısı (S_{11}) $-0{,}32$ dB, giriş 1 dB kısılım gücü (P_{in1dB}) $-9{,}65$ dBm olarak bulunmuştur. Ayrıca, bu versiyon 1 ms süreli 14 dBm güce sahip sinyal uygulandıktan sonra 3,5 μs iyileşme süresi göstermiştir. Tasarımda, kısa devre empedansına uyumlama, kutuplama devresi ve giriş koruma devresi gibi önemli kriterler ele alınmıştır.

Anahtar sözcükler: Düşük Gürültü Amplifikatörü, MRI, Sinyal-Gürültü Oranı, Larmor Frekansı, GaAs pHEMT, RF Tasarımı.

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Contents

List of Figures

List of Tables

Chapter 1

Introduction

Magnetic Resonance Imaging (MRI) has become an essential diagnostic tool in modern medicine due to its high spatial resolution, excellent soft tissue contrast, and non-invasive nature. The signal quality in MRI is primarily determined by the signal-to-noise ratio (SNR), which is especially important in high-field systems like 3 T scanners, used in this thesis. As the first active component in the MRI receive chain, the Low Noise Amplifier (LNA) is key in preserving and amplifying the weak signals detected by the receive coil for further use. According to Friis' formula, the first item in the receiver chain, LNA's, noise figure heavily influences the system's total noise performance, making LNA optimization a critical design step for system design [1, 2].

LNA design for MRI systems introduces unique challenges compared to general RF applications. Although the input of the LNA is ideally connected to the receive coil through a $\lambda/4$ transmission line to transform its low impedance into an open circuit, practical implementations often include matching capacitors at the coil terminals. These components effectively shorten the required transmission line length, deviating from the exact $\lambda/4$ condition. As a result, standard 50 Ω matching strategies are not optimal in this context. Instead, designers must prioritize maximizing power transfer from a source with near-short impedance while minimizing resistive losses and ensuring low input current to preserve array decoupling [3]. Additionally, in the MRI environment, every component must be carefully selected to avoid any distortion of the static magnetic field (B_0) or the transmitted RF field (B_1). This rules out the use of magnetic materials, such as ferrite-based inductors or bias chokes, and limits the types of components that can be placed near the imaging volume [4].

Another important consideration in MRI-oriented amplifier design is power consumption. In modern multi-channel MRI systems, dozens of LNAs may be placed near the patient. This increases the importance of minimizing heat dissipation to avoid temperature-dependent drifts in RF performance. Therefore, low noise and reasonable gain must be balanced with stringent power constraints. In the context of this thesis, power consumption is not only a thermal concern but also an operational limitation: the amplifier is powered through a fiber-optic link, which imposes strict limits on available current. As such, all design choices—from transistor selection to biasing topology—must adhere to tight power budgets while still achieving high RF performance.

This thesis presents the design, simulation, implementation, and characterization of a low-power, low-noise amplifier operating at 123 MHz, corresponding to the Larmor frequency of hydrogen nuclei at 3 T field strength. The proposed amplifier is based on a single-stage common-source topology using a GaAs pHEMT transistor. The chosen configuration avoids source degeneration to maintain compatibility with low-impedance sources and simplify the matching network. Emphasis is placed on minimizing component losses, ensuring magnetic compatibility, maintaining design simplicity, bias network justification, and input protection circuit insertion to ensure safe operation.

The thesis is organized as follows: Chapter 2 introduces the theoretical background necessary for understanding LNA design in the context of MRI, MRI signal characteristics, and requirements for preamplifier design in MRI receiver chains. Chapter 3 presents RF fundamentals including S-parameters, noise, linearity, and stability. A literature review of existing LNA topologies and MRI-related amplifier implementations, followed by a summary of design requirements, is also given in this section. Chapter 4 focuses on selecting the amplifier topology and components, including transistors, inductors, bias network, and protection circuit. Chapter 5 covers the schematic design and simulation results, while Chapter 6 details the PCB assembly, measurement setup, and experimental results. Finally, Chapter 7 summarizes the findings, a comparison with existing solutions, and suggestions for future work.

Chapter 2

MRI Background and Signal Characteristics

Magnetic Resonance Imaging (MRI) is a non-invasive diagnostic technique that utilizes the magnetic properties of atomic nuclei to generate high-resolution images of biological tissues. The most commonly imaged nucleus is hydrogen (^{1}H), due to its high natural abundance in the human body, especially in water and fat. When placed in a strong static magnetic field B_0, typically 1.5 T or 3 T in clinical systems, hydrogen protons align with the field and precess at a frequency known as the Larmor frequency. This frequency is given by

$$f = \frac{\gamma}{2\pi} B_0, \tag{2.1}$$

where $\gamma/2\pi$ is the gyromagnetic ratio. For ^{1}H, $\gamma/2\pi \approx 42.58$ MHz/T, resulting in a Larmor frequency of approximately 123 MHz at 3 T [5]. The Larmor frequency sets the center frequency for both transmission and reception in the MRI system.

MRI signal generation begins with an RF excitation pulse at the Larmor frequency, which perturbs the equilibrium alignment of the nuclear magnetization. As the spins relax back to equilibrium, they emit a decaying RF signal — the free induction decay (FID) — which is detected by the receive coil. This signal can exhibit a wide dynamic range: immediately after RF excitation, peak voltages at the coil output can reach up to 1–5 V in some configurations [1]. During typical acquisition periods, the signal amplitude often settles into the range of 100 μV to a few millivolts. The preservation and amplification of this signal are critical for maintaining a high signal-to-noise ratio (SNR) in the final image.

The receive coil acts as both a detector and a front-line filter against external noise. Typically implemented as a single loop or an array of loops, the coil is tuned to the Larmor frequency and matched to an optimal load impedance [1].

Coils are also designed with built-in protection elements to handle high-voltage transmit pulses and prevent damage to downstream electronics. Detuning circuits, typically using PIN diodes, deactivate the coil during transmission to avoid coupling with the transmit field. Additionally, clamping diodes or limiter circuits are used to protect the sensitive receive chain from transient voltages that may occur during switching events or in the presence of strong eddy currents [6]. These protection mechanisms are especially important during echo-planar imaging (EPI) and fast imaging sequences where frequent switching occurs.

It is important to note that the MRI signal is most susceptible to distortion immediately following RF excitation. At this stage, the signal reaches its peak amplitude and must be transferred to the LNA with minimal distortion. Any loss or distortion at this stage can significantly degrade image quality. Thus, the coil's electromagnetic behavior and impedance characteristics directly influence the requirements placed on the first-stage amplifier and signal chain design.

In scenarios where the MRI signal peaks at high amplitudes — sometimes reaching several volts immediately after excitation — it is critical to protect the input stage of the receiver circuitry. Excessive voltage can damage the gate of sensitive transistors or drive them into nonlinear regions, resulting in distortion or long recovery times. To mitigate this, MRI front-ends often employ passive protection circuits such as RF limiters or clamping diodes at the coil output. Additionally, the active device itself should exhibit fast recovery characteristics, allowing it to return to its linear operating region promptly after exposure to a strong signal. This is important to detect subsequent low-level signals without entering a "dead zone" caused by saturation. Device selection and circuit layout must therefore consider both transient protection and dynamic recovery behavior.

The target gain for the LNA is also important to balance the need for effective noise suppression with the constraints of system linearity and dynamic range. On the lower end, a decent gain is essential to elevate the weak MRI signals, often in the microvolt range, above the quantization noise floor of the analog-to-digital converter (ADC) following the LNA. This ensures that the noise figure of the overall receiver chain is dominated by the LNA, thereby preserving the signal-to-noise ratio (SNR) established at the coil interface. Conversely, excessive gain can lead to challenges in the dynamic range of the following ADC. High gain may cause signal clipping at the ADC input or reduce headroom for unexpected input variations. Moreover, overly high gain compresses the ADC's effective number of bits (ENOB), limiting its ability to digitize weaker components of the signal without distortion. Thus, the amplifier gain must be sufficient to lift the signal above the quantization noise floor without exceeding the dynamic range ceiling imposed by the ADC, ensuring optimal utilization of the available digital resolution [7].

In MRI, receive coils are tuned to the Larmor frequency to detect the weak RF signals emitted by the relaxing nuclei. These highly sensitive coils should see a very high impedance during operation to limit the flowing current. Reduced current is crucial for minimizing electromagnetic coupling between coils in an array. Ideally, a $\lambda/4$ transmission line transforms the low input impedance of the LNA into a high impedance at the coil side. However, in practical designs, tuning and matching capacitors placed at the coil terminals alter the electrical length of the connection, effectively shortening the transmission line. As a result, the transformation no longer corresponds exactly to a $\lambda/4$ condition. Nevertheless, the LNA must still present a near short-circuit input impedance to maintain high impedance at the coil and enable effective decoupling. This creates a unique matching challenge, as the LNA must efficiently amplify power from a near short source while introducing minimal noise [8].

Additionally, MRI systems are extremely sensitive to electromagnetic interference. All electronics positioned near the imaging volume must be free of magnetic materials to avoid distortion of static and RF magnetic fields [9]. This constraint significantly limits the selection of components such as inductors, capacitors, connectors, and PCB substrates. Beyond electromagnetic compatibility, power consumption emerges as a critical design factor, especially in modern systems that employ dozens or even hundreds of receive channels. Each additional channel adds cumulative power dissipation, which can lead to local heating of sensitive components and potential image artifacts caused by temperature-induced frequency drift or coil detuning. Moreover, increased thermal output may degrade the performance of nearby amplifiers or shift the bias point of active devices. For these reasons, low-power circuit design is essential not only for overall system efficiency but also for ensuring thermal and magnetic stability within the tightly constrained MRI environment [10]. Furthermore, for the receiver chains that are powered by fiber optics, like in this thesis, there is a current limit that fiber optic cable can carry. To satisfy the current rating, each component should work at its minimum possible current level.

2.1 Preamplifier Requirements in MRI Receiver Chains

The design of the MRI preamplifier requires careful attention to the electromagnetic and physical constraints imposed by the imaging environment. A key challenge is that the LNA input is not matched to the standard 50 Ω termination. In coil arrays, LNAs are typically connected to the receive coils through a transmission line with an electrical length close to $\lambda/4$ at the Larmor frequency. This setup is intended to transform the low input impedance of the LNA into a high impedance at the coil side, thereby reducing mutual coupling and suppressing induced currents in neighboring elements to enhance array decoupling [11]. However, in practice, tuning and matching capacitors placed at the coil terminals shift the resonance and effectively reduce the required physical length of the transmission line. Despite this deviation from the ideal $\lambda/4$ configuration, the LNA is still designed to present a near short-circuit input impedance so that the coil sees a high impedance overall, maintaining low current and ensuring minimal coupling between elements. Figure 2.1 shows an example of a 4-channel receiver system. Additionally, the amplifier must remain electrically and magnetically quiet to avoid distortion of the imaging fields [3].

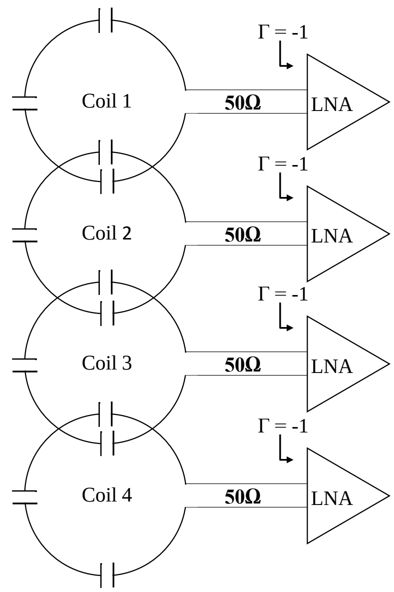


Figure 2.1: Schematic description of the 4-channel receiver system.

Biasing and layout are also critical in MRI-specific LNA design. Bypass capacitors, chokes, and inductors must be chosen not only for their RF performance but also for their magnetic transparency. Additionally, input protection circuitry can be implemented for safe operation.

In addition to standard RF considerations, LNAs working in non-controllable receiver chains, like MRI, must be able to tolerate and recover from incoming large input signals. During imaging sequences, high-power RF pulses can couple into the receive path due to imperfect isolation or switching transients. If the LNA is not designed to handle these conditions, it may become saturated or even permanently damaged. Therefore, the maximum input power level must be specified for robust operation. Moreover, once such a large signal disappears, the amplifier must recover rapidly to continue normal, low-noise amplification without introducing dead time. This recovery behavior is influenced by transistor and bypass capacitor selection and is especially critical in fast imaging protocols.

To summarize:

- **Impedance matching**: The design of MRI preamplifiers requires precise impedance matching. LNAs are typically configured with low input reflection coefficients in multi-channel arrays to improve overall array decoupling.
- **Noise performance**: The MRI preamplifier should add a minimal amount of additional noise to be able to detect small signals.
- **Magnetic compatibility**: If the LNA is placed near the coil, components must be non-magnetic to avoid distortion of the MRI's magnetic fields.
- **Power consumption**: Low power consumption is critical in multi-channel systems to minimize heating and ensure patient safety. Also, due to fiber optic cable limitations, current consumption should be minimized in optically powered systems.
- **Physical size**: Compact designs are preferred to fit within the spatial constraints of MRI systems.
- **Maximum input power level**: The LNA must be able to withstand occasional large signal inputs without entering breakdown or permanent degradation.
- **Recovery time**: After exposure to a high-power pulse, the LNA must quickly return to its linear, low-noise operating state to avoid signal loss.

Chapter 3

Literature Review and LNA Design Considerations

This chapter reviews RF fundamentals and commonly used low-noise amplifier (LNA) topologies, both in general RF systems and MRI-specific applications. A summary of design considerations unique to MRI environments is also provided. Finally, the design goals for the LNA developed in this work are listed based on application requirements and prior research.

3.1 RF Fundamentals for LNA Design

The design and evaluation of low-noise amplifiers in MRI systems rely on core RF engineering concepts that quantify impedance behavior, noise contribution, linearity, and stability. These RF fundamentals not only govern transistor-level performance but also provide a framework to interpret how the amplifier interacts with the MRI coil and signal environment. This section introduces the key parameters and tools used throughout this work to analyze and validate the proposed LNA design.

3.1.1 S-Parameters and Impedance Matching

Scattering parameters (S-parameters) are widely used in RF design to characterize how signals are transmitted and reflected within a network. For a two-port LNA, the most relevant parameters are:

- S_{11}: input reflection coefficient (impedance at input)
- S_{21}: forward gain
- S_{22}: output reflection coefficient (impedance at output)
- S_{12}: reverse isolation

In conventional RF systems, the input and output ports are matched to 50 Ω. However, in MRI applications, the LNA is typically connected to the receive coil via a $\lambda/4$ transmission line, and the system is deliberately mismatched in the conventional sense. The impedance seen from the coil is often engineered to approach an open-circuit condition to suppress mutual coupling in array configurations [11]. To enable this, the LNA is usually designed with a low input impedance (i.e., Z_{in} nearly equal to 2 Ω), effectively presenting a short-circuit when viewed from its input. This MRI-specific impedance strategy requires that matching networks be optimized accordingly.

3.1.2 Noise Figure

The noise figure (NF) quantifies the noise contribution of the amplifier relative to an ideal noiseless device. It is defined as the ratio of the signal-to-noise ratio (SNR) at the input to that at the output while the input noise is at a specific level defined by $T_0 = 290^\circ$ K:

$$NF \triangleq \left.\frac{\mathrm{SNR_{in}}}{\mathrm{SNR_{out}}}\right|_{T=T_0\,(290^\circ\ \mathrm{K})} \tag{3.1}$$

Lower NF values indicate better noise performance and are typically expressed in decibels. In MRI systems where received signals are extremely weak and SNR is critical to image quality, minimizing the LNA's noise figure is a primary design objective.

3.1.3 Linearity

Although MRI signals are typically low in amplitude, non-ideal operating conditions can lead to unexpectedly strong voltages at the LNA input. Sources of interference include transmit leakage and coupling between array elements. The large transmit signal leakage can drive the LNA into saturation and may even cause destruction of the LNA transistor. The destruction of the LNA transistor may be prevented by protection circuits at the input of the LNA. Additionally, the LNA may not recover from the saturation condition for a while, even after the transmit leakage signal has disappeared.

Two key figures of merit for characterizing linearity are the 1 dB compression point ($\mathrm{P_{1dB}}$) and the third-order intercept point (IP3). $\mathrm{P_{1dB}}$ indicates the output (or input) power level at which the gain drops by 1 dB from its small-signal value, marking the transition into compression. This work uses P_{in1dB} to reflect the LNA's input-handling capability. The IP3 measures the extrapolated intersection point of the fundamental and third-order intermodulation tones, providing insight into distortion behavior. If this metric is defined for input power level, it is called IIP3, and if for output, it is denoted as OIP3. High values of both $\mathrm{P_{in1dB}}$ and IP3 are essential to maintain signal fidelity, particularly in broadband or multi-coil systems [12, 13]. Better linearity results can be achieved by increasing the supplied voltage and optimizing the S_{22} value.

3.1.4 Stability

An essential requirement for any LNA is unconditional stability across its entire operating frequency range. The most widely used stability metric is the Rollett stability factor K, defined as:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{3.2}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. For unconditional stability, the condition $K > 1$ and $|\Delta| < 1$ must be met over all of the frequency range. In practice, matching networks, layout parasitic, and feedback elements must be carefully designed to maintain stability without degrading noise performance [12]. The transistor used in the LNA should be characterized in the wide frequency range, especially at low frequencies, to be able to check the stability at all frequencies.

3.2 Review of Common LNA Topologies

From the past, several LNA topologies have been studied and implemented extensively. Each topology offers unique trade-offs between performance metrics such as gain, noise figure, bandwidth, and input matching.

The Common-Gate (CG) topology has been widely used in wide-band applications due to its inherently low input impedance, which naturally matches 50 Ω sources without needing external matching networks [12]. Despite this advantage, since signal flows through the channel, which is noisy, CG amplifiers typically suffer from higher noise figures and lower gain than other topologies, limiting their applicability in low-frequency or low-noise designs like those used in MRI.

The Cascode topology combines a common-source and a common-gate stage, offering superior reverse isolation and gain by minimizing the Miller effect [13]. It is often used in high-frequency applications but comes with increased voltage headroom and power consumption requirements, making it less ideal for compact or battery-sensitive MRI receiver coils.

Differential LNAs are advantageous in environments with significant common-mode noise, providing improved linearity, even-order harmonic cancellation, and immunity to power supply fluctuations. However, their implementation increases circuit complexity, noise figure, die area, and power consumption [14]. These trade-offs are not always justifiable in tightly controlled MRI environments, where single-ended low-noise designs can often efficiently meet performance targets.

The Common-Source (CS) topology effectively balances gain, noise, and simplicity. Moreover, the CS topology offers design flexibility through inductive source degeneration and tunable matching networks, enabling impedance optimization for maximum power transfer and minimal noise contribution. Its relatively simple architecture also supports straightforward integration in multi-channel or phased-array MRI receiver systems, where layout density, power efficiency, and thermal stability are important considerations.

In addition to field-effect transistor (FET) topologies, bipolar junction transistor (BJT)-based designs have long played a significant role in low-noise amplifier development. BJTs offer inherently high transconductance (g_m) even at relatively low collector currents. This directly contributes to lower noise figures—especially important in low-frequency or narrow-band applications such as MRI [15]. This makes BJT-based topologies competitive alternatives to their FET counterparts, particularly in silicon-based technologies where GaAs or CMOS options may not be available or practical.

Among BJT topologies, the Common-Emitter (CE) configuration is directly analogous to the Common-Source (CS) topology in FETs. It offers high gain and excellent noise performance and is widely used in discrete or hybrid MRI LNA designs [16]. Proper biasing and thermal stabilization are critical, as BJTs are more sensitive to temperature-induced performance variation.

Cascode configurations can also be implemented using BJTs, providing high gain and wide bandwidth while reducing the Miller effect. Similarly, differential

BJT LNAs are often found in more advanced or integrated systems where linearity and noise immunity are essential.

While BJTs offer competitive noise and gain performance, especially in low-frequency bands, they generally exhibit higher power consumption and require more complex biasing schemes than FETs. Moreover, GaAs-based FETs (like pHEMTs) maintain an advantage in ultra-low noise and high-frequency operation due to superior electron mobility and lower parasitic capacitance [17]. The trade-offs in MRI receiver design—especially for narrow-band systems—often favor FET-based Common-Source designs, particularly when low noise, simplicity, and integration potential are prioritized. Nonetheless, BJT-based Common-Emitter designs remain viable alternatives in silicon-based or hybrid MRI systems where performance, availability, and cost must be balanced.

Table 3.1: Comparison of Common LNA Topologies

Topology	**Gain**	**Noise Figure**	**Bandwidth**	**Input Matching**
Common-Gate (CG)	Medium	High	Wide	Natural 50 Ω
Common-Source (CS)	High	Low	Medium	Needs match
Cascode	Very High	Low	Wide	Needs match
Differential	High	Higher	Med.–Wide	Differential

3.3 Recent MRI-Specific LNA Designs

Various LNA topologies and implementations have been explored in the literature to meet the stringent requirements of MRI systems. While the common-source (CS) topology remains popular due to its simplicity and low noise potential, other configurations such as common-gate (CG), cascode, and differential architectures have also been considered, depending on the application constraints such as power, layout area, and matching needs.

Kabel et al. (2017) presented an ultra-low-noise LNA for MRI applications operating at 32 MHz. The design utilized a cascode topology to improve gain and stability while achieving a measured noise figure as low as 0.45 dB and a gain of 11.6 dB. The cascode arrangement helped mitigate Miller capacitance and provided isolation between stages, contributing to unconditional stability up to 6 GHz [18].

Another recent contribution tackled the challenge of improving decoupling in low-frequency MRI receive arrays by modifying the impedance of the preamplifier rather than relying solely on geometrical coil decoupling. This approach, presented in a 2018 study, highlights how careful impedance engineering at the LNA input can improve isolation between channels in high-density receiver arrays, ultimately enhancing image quality [19].

Cao et al. (2016) proposed a preamplifier design for 3 T MRI systems that focuses on achieving stability performance insensitive to coil loading variations. This is particularly important in multi-channel arrays where changing loading conditions can alter the input impedance seen by the amplifier, potentially leading to instability or degraded performance. The authors used a robust input matching strategy and carefully engineered the amplifier's feedback path to suppress instability without sacrificing low-noise operation. The design achieved stable behavior across various loading conditions, making it suitable for scalable MRI receiver arrays. Their results also demonstrated that the noise performance remained consistent, with NF values below 1 dB, validating the approach for high-field clinical systems. Also, their power consumption is 215 mW with an input impedance of 3.6 Ω [20].

Johansen et al. (2017) presented two preamplifier designs tailored for ^{13}C imaging at 3 T, operating at 32.1 MHz. The first design prioritized achieving an ultra-low noise figure, attaining 0.25 dB with a gain of 23 dB and input return loss of 0.28 dB, making it suitable for single-coil applications where minimizing noise is paramount. The second design focused on optimizing the input impedance to enhance decoupling in array configurations, achieving an input impedance of 0.4 Ω with an inductive component, a gain of 20 dB, and a noise figure of 0.75 dB. Both designs have the power consumption of 99 mW and utilize the Avago ATF-54143 enhancement-mode pHEMT transistor, chosen for its low noise characteristics and positive biasing requirements. The common-source topology was selected for its stability, as alternative topologies like common-gate proved challenging to stabilize. These designs underscore the trade-offs between noise performance and impedance matching in preamplifier design for ^{13}C MRI applications [21].

Horneff et al. (2019) introduced a broadband, high-impedance CMOS low-noise amplifier (LNA) tailored for magnetic resonance imaging (MRI) applications. The design achieved a noise figure of 0.45 dB and a gain of 44 dB with 55 mW power consumption, which is notably low for CMOS-based implementations. This performance was accomplished through an innovative impedance transformation network that effectively matched the high impedance of MRI coils to the LNA's input, thereby minimizing noise contributions. The amplifier's broadband capability ensures compatibility with various MRI frequencies, enhancing its versatility in different imaging scenarios. The integration of the LNA in CMOS technology also offers advantages in terms of scalability and potential for on-chip integration with other MRI system components [22].

Commercially, several MRI-specific preamplifiers are available that are shaped to various system requirements. For instance, Siemens offers the 128 MHz Preamplifier (Part No. 7576312), designed for high-field MRI applications with optimized noise performance and stability. This preamplifier consumes 196 mW power with a gain of 27 dB and a noise figure of 0.71 dB [20]. Texas Instruments provides the TL5500, a low-noise preamplifier tailored for MRI systems. This preamplifier consumes 110 mW power with a gain of 28 dB and a noise figure of 0.5 dB [23]. Agile Microwave Technology Inc. offers the AMT-AN0064, a 40 MHz to 50 MHz non-magnetic low noise amplifier suitable for MRI applications requiring minimal magnetic interference. This preamplifier consumes 152 mW power with a gain of 30 dB and a noise figure of 0.4 dB [24]. WanTcom Inc.'s WMA32C is a 32.19 MHz low-noise, low-impedance preamplifier designed to interface effectively with MRI coils. This preamplifier consumes 180 mW power with a gain of 28 dB and a noise figure of 0.7 dB [25]. These commercial solutions provide ready-to-use options for MRI system designers, balancing performance with ease of integration.

These designs collectively demonstrate that the choice of topology—whether CS, CG, cascode, or differential—must be guided by application-specific constraints such as operating frequency, magnetic compatibility, and power efficiency. Among them, common-source amplifiers are frequently favored in MRI due to their simplicity, low noise performance, and compatibility with low-impedance coil sources, provided that stability is carefully managed. While cascode designs offer improved gain and isolation, they often come with higher power consumption and increased circuit complexity, making them less ideal for densely packed, thermally constrained receive arrays. In contrast, differential and common-gate configurations, though beneficial in certain scenarios, generally fail to meet the power and noise performance trade-offs required in low-field, multi-channel MRI systems. Given the increasing channel counts in modern MRI scanners and the strict limitations on heat dissipation and electromagnetic interference, reducing preamplifier power consumption has become a primary design objective. This thesis specifically targets the development of a low-power MRI-compatible LNA that maintains acceptable noise and linearity performance.

3.4 Design Objectives for This Work

Based on the discussions in Chapter 2 and 3, the design goals for the LNA in this work are defined to meet both RF and MRI-specific constraints. Table 3.2 summarizes the target specifications used as reference in the design and evaluation process.

Table 3.2: Design goals for the proposed LNA

Parameter	**Target Value**	**Reason**
Operating Frequency	123 MHz	Larmor frequency of ^{1}H for 3 T MRI
Input Reflection Coefficient (S_{11})	≥ -0.7 dB	Almost full reflection is required for low current in the coils
Phase of Input Impedance	180°	To present an open-circuit impedance at the coil terminals (after a shortened $\lambda/4$ line), minimizing current and inter-coil coupling in arrays
Gain	≈ 14 dB	To amplify the signal above the quantization noise floor of A/D converter
Noise Figure	≤ 1 dB	Not to degrade the noise floor
Power Consumption	≤ 15 mW	To be compatible with fiber optic power.
Output Reflection Coefficient (S_{22})	No target	Output should be matched for higher P_{1dB} values.
Magnetic Compatibility	No ferrite or magnetic materials	To be compatible with high magnetic field when placed near the coil
Maximum Input Power	≥ 13 dBm	To withstand transmit leakage and protect the front-end during large input signal events
Recovery Time	≤ 10 μs	To return quickly to linear operation after high-power transients and avoid signal dead time
Bias Supply	Single-supply, MRI-safe, low ripple	To reduce complexity and ensure steady operation

Chapter 4

Topology and Component Selection

This chapter outlines the reasoning behind selecting the amplifier topology, active device, and passive components used in the proposed LNA design. Given the MRI-specific design constraints, including low impedance matching, magnetic compatibility, and power efficiency, the final configuration aims to balance low noise, stability, and simplicity.

4.1 Topology Selection

Among the available LNA topologies discussed in Chapter 3, the common-source (CS) amplifier was selected for this work. The CS topology offers several advantages in the context of MRI applications:

- It provides high gain and low noise when properly matched to the source.
- Unlike cascode or differential topologies, the CS design minimizes power consumption and component count, critical for multi-channel MRI arrays.

In typical RF systems, source degeneration is often added to improve input matching and linearity. However, for MRI applications, this is generally avoided. Preamplifier input impedance should be as close as possible to the short circuit, and source degeneration moves the impedance locus inward on the Smith Chart, making it more difficult to match efficiently to such low-impedance [26]. For this reason, a non-degenerated common-source topology was selected, allowing direct matching to the coil and reducing ESR-induced losses.

Alternative topologies, such as common-gate or cascode, were considered but dismissed. Common-gate amplifiers, while offering wide-band matching, exhibit higher noise figures. Cascode amplifiers, as shown in previous studies [18, 20], perform well in gain and stability but increase power and complexity, which is undesirable in compact MRI front-ends.

4.2 Transistor Selection and Comparative Analysis

The transistor choice is critical to achieving low noise, gain, and power performance in MRI applications. After evaluating several available devices and technologies, the Mini-Circuits SAV-541+ GaAs pHEMT was selected as the active device in this design. This decision is justified from the semiconductor physics perspective and practical considerations in discrete RF circuit design.

From a physical perspective, high-electron mobility transistors (HEMTs) are widely used in low-noise RF applications due to their superior carrier transport properties. Among common HEMT channel materials, GaN, GaAs, InP, and SiGe each offer different trade-offs:

- **GaN** exhibits very high breakdown voltage and power density, making it ideal for high-power and high-frequency applications. However, it has relatively high noise figures in low-voltage operation due to its lower electron mobility and higher thermal noise, which are undesirable in low-power MRI front ends [27].

- **InP** offers the highest electron mobility among III–V semiconductor materials, with values around 5400 $cm^2/V{\cdot}s$ at room temperature. This exceptional electron mobility enables faster electron transport, making InP highly suitable for ultra-high-speed and sub-millimeter wave applications, such as terahertz frequency devices and high-speed optoelectronics [28]. However, InP is known to be fragile and expensive, and discrete packaged transistors made from InP are not commonly available for low-frequency operations in the 100– 200 MHz range, limiting their practicality for such applications.

- **Si and SiGe**: Silicon-Germanium (SiGe) Heterojunction Bipolar Transistors (HBTs) are prevalent in CMOS and BiCMOS integrated designs due to their compatibility with silicon processing and favorable high-frequency characteristics. However, their electron mobility is lower compared to III–V semiconductors. Specifically, electron mobility in silicon is approximately 1,400 $cm^2/V{\cdot}s$, while in SiGe alloys, it ranges from 1,500 to 3,000 $cm^2/V{\cdot}s$, depending on the germanium content and strain conditions [29]. This is significantly less than the electron mobility in materials like GaAs or InP, which can exceed 8,500 $cm^2/V{\cdot}s$. Additionally, SiGe HBTs typically exhibit higher 1/f noise and reduced transconductance at low drain currents, which can be detrimental in discrete low-noise amplifier (LNA) implementations operating in the 100– 200 MHz range [30].

- **GaAs**, specifically in enhancement-mode pHEMT structures, offers a strong balance. It provides high electron mobility (8500 cm^2/Vs), low effective mass, and excellent low-voltage operation with minimal gate leakage. These attributes translate into superior noise performance and high gain, even at modest supply voltages. Their minimal parasitics and simple biasing contribute to rapid recovery following overload, making them ideal for preserving signal fidelity between transmit-receive cycles in fast imaging sequences. These properties make it well-suited for low-power and magnetically sensitive environments like MRI systems [31].

The SAV-541+ is a GaAs enhancement-mode pseudomorphic high electron mobility transistor (E-pHEMT) specifically optimized for low-noise amplification across the 45 MHz to 6 GHz frequency range. E-pHEMTs combine the high electron mobility of GaAs with a normally-off (enhancement-mode) operation, eliminating the need for negative gate bias. E-pHEMTs leverage a heterostructure interface (typically AlGaAs/GaAs) that forms a two-dimensional electron gas (2DEG) channel with high carrier mobility and low noise characteristics. This makes them ideal for front-end amplifiers in RF and microwave systems where gain and noise figure must be optimized simultaneously.

The SAV-541+ exemplifies these characteristics. Operating at 3 V drain voltage and 60 mA bias current, it delivers a typical noise figure of 0.5 dB and gain of 17.4 dB at 2 GHz, while maintaining unconditional stability over a wide frequency range [32]. Its compact SC-70 packaging is advantageous for minimizing layout parasitics near the receive coil.

Market Comparison and Selection Justification

Alternative devices considered include:

- **ATF-54143 (Broadcom)**: Also a GaAs pHEMT, this device offers similar performance, but its recommended frequency interval is 450 MHz to 6 GHz. It can be used as a replacement for higher frequency applications [33].
- **SAV-551+ (Mini-Circuits)**: A higher-frequency-optimized sibling of the SAV-541+, its performance below 200 MHz is slightly less predictable. SAV-541+ showed better gain flatness and match around 123 MHz in simulation [34].
- **SiGe HBTs (e.g., BFP640, BFR520)**: Readily available and inexpensive, alternatives in HBT [35, 36].

In the context of MRI, where magnetic compatibility, low power consumption, compact layout, and RF stability are paramount, the SAV-541+ stands out. It offers superior material-level advantages (due to GaAs), excellent application documentation, and consistent performance at the 123 MHz target frequency. Furthermore, Mini-Circuits provides extensive simulation models (both S-parameters and harmonic balance) and recommended bias networks, significantly reducing development time and layout risk.

4.3 Inductor and Passive Component Selection

High-quality passive components were selected for impedance matching and DC biasing networks to minimize losses and preserve SNR. In MRI systems, magnetic compatibility is a key constraint; hence, air-core inductors were chosen to avoid any interaction with the static B_0 field.

The Coilcraft Square-Air-Core inductor series was selected as a part of the matching network. This inductor family provides a high Q factor (typically above 140 at 50 MHz) and low series resistance. From the manufacturer's website, selecting at most 90 nH inductors is safe regarding their almost constant values in the inductance versus frequency graphs up to 120 MHz. Moreover, the Q factor of 90 nH is slightly better than smaller valued inductors. Therefore, a 90 nH air-core inductor is selected, providing a high Q factor (typically above 250 at 123 MHz) and low series resistance [37]. Simulation results showed that replacing it with a lower-Q alternative leads to over 0.4 dB degradation in input return loss due to increased resistive losses.

The Q factor is given by:

$$Q = \frac{\omega L}{R_s} \tag{4.1}$$

where R_s is the series resistance and $\omega = 2\pi f$.

Capacitors were chosen among ultra-low ESR valued ones. All passives are surface-mount and certified non-magnetic per MRI compatibility standards.

4.4 Biasing Network

The biasing network in a low-noise amplifier defines the transistor's operating point and influences overall stability, noise, and integration constraints. For this design, the SAV-541+ GaAs pHEMT transistor was selected, which operates in enhancement mode—meaning it is normally off when $V_{GS} = 0$ [32].

Several biasing strategies were evaluated before finalizing the implementation. A conventional approach uses separate supplies for the gate and drain terminals, allowing full control over V_{GS}. However, this method requires more complex cabling, which is undesirable in MRI environments, particularly when dealing with multiple parallel channels in a confined space.

A more compact and power-efficient alternative is using a passive resistive voltage divider to derive the gate voltage from the drain supply. While this enables single-supply operation, the extremely high input impedance of the pHEMT gate causes the gate voltage to be sensitive to component tolerances and layout-induced leakage, especially over temperature. The lack of inherent feedback also means that any variation in supply or device characteristics directly affects the drain current, making this configuration less robust for stable analog front-end performance. Also, even though it seems stable in simulations, the circuit oscillated during measurements and prevented healthy operation.

The biasing network recommended for the SAV-541+ employs an active current source configuration based on two matched PNP bipolar transistors (MMBT3906). This circuit is designed to provide a stable drain current that is robust against temperature variations and supply fluctuations. As illustrated in Figure 4.1, transistors Q1 and Q2 form a current mirror: Q1 is diode-connected and sets the reference current through resistor R4, which is mirrored by Q2 to supply the drain of the E-pHEMT through inductor L2. This ensures a predictable bias current. The drain current can be approximated by the expressions in Equation (4.2) and Equation (4.3), where V_{BE} is the base-emitter voltage of the matched BJT pair:

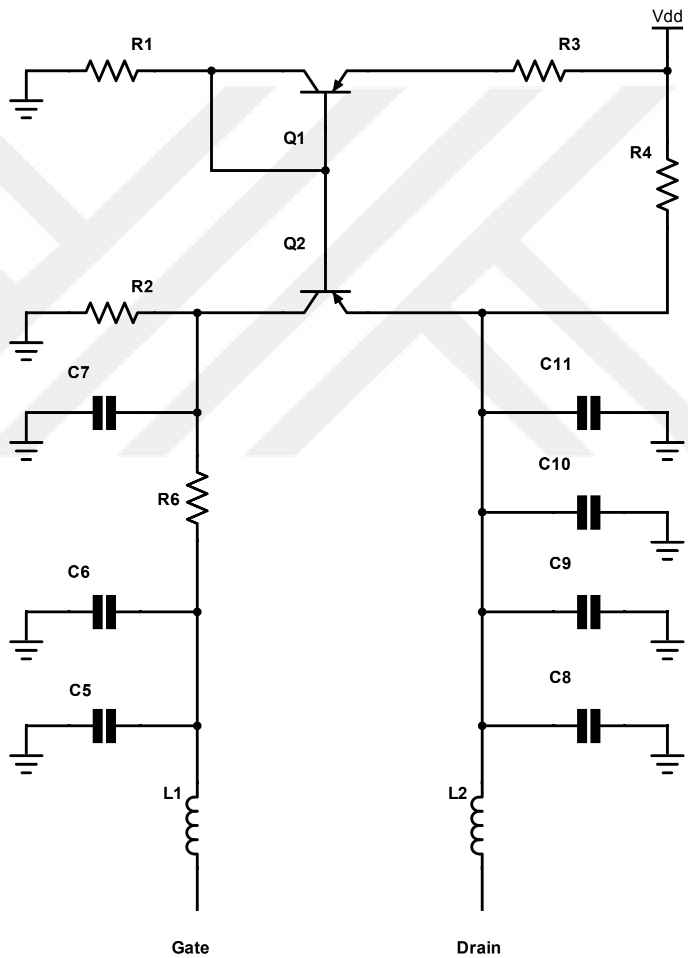


Figure 4.1: Recommended biasing network for the SAV-541+ E-pHEMT transistor.

$$I_{R_4} = \left(\frac{V_{\mathrm{dd}} - V_{BE}}{R_1 + R_3}\right) \cdot \frac{R_3}{R_4} \tag{4.2}$$

$$I_d = I_{R_4} - \frac{V_g}{R_2} \tag{4.3}$$

In addition to accurate current regulation, this biasing topology introduces a built-in negative feedback mechanism that plays a critical role in stabilizing the operation of the high-gain transistor. Due to the large gain of the E-pHEMT, the circuit is prone to unintended positive feedback at very low frequencies, potentially leading to bistable behavior similar to a flip-flop. To suppress this, the gate bias voltage should be made responsive to changes in the drain current.

The feedback mechanism functions as follows: R3, Q1, and R1 form part of the gate bias path. The drain current and Q2's collector current both flow through R4. If the drain current increases, the base-emitter voltage (V_{BE}) of Q2 decreases, reducing its collector current. As a result, the voltage drop across R2 decreases, which lowers the gate voltage of the E-pHEMT. This negative feedback reduces V_{GS}, counteracting the initial rise in current and thereby stabilizing the bias point.

Such feedback is particularly beneficial in low-frequency or quasi-static operating regimes, where parasitic capacitances and layout imperfections can reinforce feedback paths. In contrast, biasing networks without feedback regulation can lead to unstable or bistable operating points, especially when used with high-gain transistors in narrowband, low-frequency applications such as MRI.

In the design of bias networks for RF amplifiers, two critical considerations beyond DC biasing are the frequency-dependent gain of the network and its recovery time following large input transients. The biasing circuit should not introduce significant gain at the operating frequency, as this may interfere with the intended gain and frequency response of the RF amplifier. Additionally, short recovery time is essential in applications such as MRI, where high-power transmit pulses may precede weak receive signals. A bias network that recovers slowly can introduce dead time, during which the amplifier is unable to respond linearly to incoming signals.

To implement this network, standard surface-mount resistors and air-core inductors were used. This configuration enables a clean and layout-efficient solution that fully supports the low-power, low-noise, and magnetically safe operation demanded by MRI receiver systems.

4.5 Input Limiter Network

High-power RF transients at the MRI coil output can generate voltage spikes that exceed the safe gate voltage of the LNA, risking device breakdown or degraded noise performance. To protect the amplifier, a passive limiter circuit is implemented immediately before the gate.

Figure 4.2 shows the limiter configuration: a DC-block capacitor (C12), AC-couples RF into two antiparallel diodes—a Schottky diode (D2) and a PIN diode (D1) [14]. The Schottky diode, with its metal–semiconductor junction, has a low forward voltage drop (0.2–0.3 V) and fast switching speed, making it ideal for rapidly clamping negative-going peaks with minimal off-state capacitance [38]. The PIN diode, featuring an intrinsic layer between its p- and n-regions, behaves as a current-controlled resistor whose RF resistance decreases with forward bias, allowing it to absorb high-energy positive peaks and handle large pulse power while still exhibiting low off-state capacitance [39].

Under small-signal conditions, the RF voltage swing at the gate is well below either diode's forward threshold ($|V| \ll 0.3\text{–}0.7\,\mathrm{V}$), so neither the Schottky nor the PIN conducts. As a result, the limiter branch is effectively "off" and contributes negligible loading or insertion loss. Once the RF amplitude exceeds the Schottky turn-on threshold, D2 conducts first, generating a forward current I_F that lowers the PIN's equivalent series resistance R_d. The resulting low R_d shunts excess RF energy back to the source, clipping waveform peaks at the designed knee voltage without degrading the LNA's noise figure or detuning the coil [40].

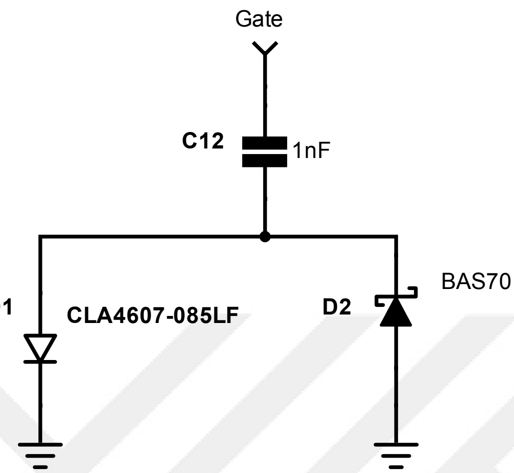


Figure 4.2: Schematic of the protection network.

When the RF amplitude exceeds the combined diode forward thresholds, the diodes begin to conduct and clip the waveform peaks. The PIN diode (D1, CLA4607-085LF) is chosen for its high power handling and relatively slow recovery, so it can absorb large RF pulses without damage [39]. The Schottky diode (D2, BAS70) has a low forward voltage and extremely fast response, which provides rapid clamping of negative-going peaks. Together, they ensure that both positive and negative excursions of the input voltage are limited to safe levels, thereby protecting the GaAs pHEMT gate from overdrive or breakdown [38]. Under small-signal conditions, the Schottky remains off, and the PIN's equivalent series resistance

$$R_d = \frac{W^2}{2\,\mu\,I_F\,\tau} \tag{4.4}$$

where W is the PIN diode's intrinsic-layer thickness, μ is the ambipolar mobility of electrons and holes, and τ is the minority-carrier lifetime, is very large, so the limiter branch is essentially invisible. As the RF input exceeds the Schottky turn-on threshold, the diode conducts and generates a forward current I_F. This reduces R_d dramatically, reflecting energy back toward the source and clipping the waveform. The attenuation becomes:

$$A_{\mathrm{dB}} \; = \; 20 \log_{10}\!\Big(1 + \frac{Z_0}{2\,R_d}\Big), \tag{4.5}$$

In a typical MRI receive chain, the coil at resonance behaves like a very low source impedance, reflecting most of the RF energy back toward the antenna terminals. Because limiter diodes conduct based on the voltage across them, this high reflection coefficient means the limiter "sees" only a small voltage swing, even when the coil current is large, and therefore never reaches its knee voltage to ensure protection.

By relocating the limiter from the coil output to the gate of the LNA transistor, immediately after the narrowband LC matching network, we exploit the matching circuit's impedance transformation. Resonant inductor and capacitor boost the coil's low impedance to a higher voltage at the gate, so that for a given coil current, the limiter diodes now experience a significantly larger RF voltage. This ensures the shunt PIN+Schottky pair can reliably enter conduction at the designed knee voltage, providing robust transient protection without degrading the coil tuning or the amplifier's noise figure drastically.

Thus, the Schottky-enhanced topology combines the high power handling of the PIN device with the low knee voltage of the Schottky, yielding a compact, low-threshold, wideband RF protection element. This simple, bias-free arrangement provides robust front-end protection with minimal impact on the low-noise performance of the amplifier [40].

4.5.1 Comparison of Alternative PIN Diodes for Input Limiter

Table 4.1 summarizes key parameters of candidate PIN diodes from the market, being suitable for the shunt-limiter for 123 MHz LNA. All devices are in similar SOD-123 packages and have intrinsic layers optimized for RF limiter applications.

To get a better noise performance, C_{j0} should be smaller. Also, power capability is another crucial aspect in limiters, and it should be high. From this table, CLA4607-085LF gives a good balance between NF and power capability. Moreover, CLA4607-085LF works in the range of 10 MHz - 6 GHz, being enough for 3 T MRI applications. Since this diode has no model for large signals, an ideal PIN diode is used with a BAS70 Schottky diode in the simulations. Figure 4.3 shows the current through the PIN diode with respect to the input power level.

To simplify the analysis, (4.4) can be written as:

$$R_d = \frac{K}{I_F} \tag{4.6}$$

where $K = \frac{W^2}{2\mu\tau}$. Further simplification can be done by assuming K is independent of the I_F. From the datasheet of CLA4607-085LF, K can be found numerically as 1.3 $\Omega\times$ 10 mA = 13 mV when I_F is 10 mA [39]. Using (4.5) and (4.6), attenuation level can be plotted as in Figure 4.4. At 25 dBm input power, this limiter has 21.2 dBm attenuation, which makes it safe to use this structure as protection.

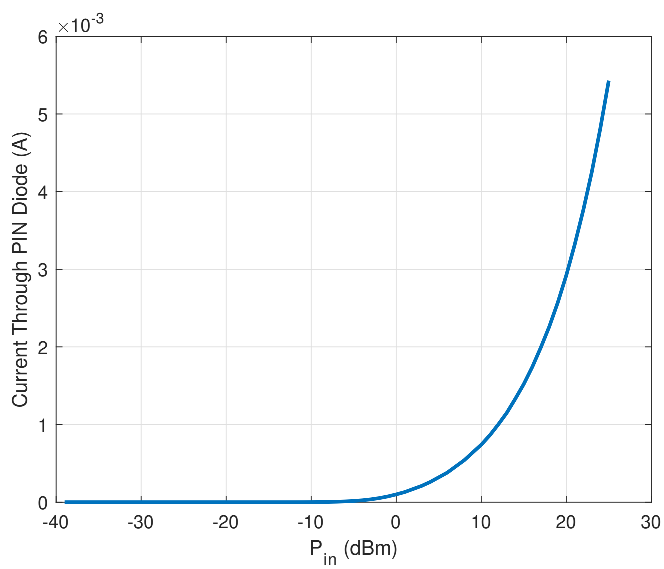


Figure 4.3: PIN diode current vs input power graph for proposed limiter.

Table 4.1: Comparison of Candidate PIN Diodes for the Input Limiter

Part #	**Manufacturer**	$\mathbf{C_{j0}}$ (pF)	$\mathbf{P}_{\mathrm{CW,max}}$ (W)	$\mathbf{R_d}$ (Ω)
CLA4607-085LF	Skyworks Solutions	0.30	5	1.3 (@ 500 MHz and I_F = 10 mA) [39].
CLA4611-085LF	Skyworks Solutions	0.30–0.35	10	0.75 (@ 500 MHz and I_F = 10 mA) [41].
CLA4608-085LF	Skyworks Solutions	0.60–0.65	5	1 (@ 500 MHz and I_F = 10 mA) [42].
MA4AGBLP912	MACOM	0.03	0.2	4 (@ 1 GHz and I_F = 20 mA) [43].
BAP50-04	Nexperia	0.45	0.25	3 (@ 100 MHz and I_F = 10 mA) [44].

Notes: C_{j0} is the zero-bias junction capacitance; $P_{\mathrm{CW,max}}$ is the maximum continuous-wave power rating; R_d is the series resistance. Specifications from manufacturer datasheets.

4.6 Drain Voltage Swing and Linearity Estimation

Since the amplifier operates in Class-A mode, its linearity is primarily determined by the available drain voltage swing around the quiescent operating point. The quiescent drain voltage V_Q is given by:

$$V_Q = V_{\mathrm{DD}} - I_D \cdot R_4 \tag{4.7}$$

Substituting the known values:

$$V_Q = 4.2\,\mathrm{V} - 3.3\,\mathrm{mA} \times 390\,\Omega = 2.91\,\mathrm{V} \tag{4.8}$$

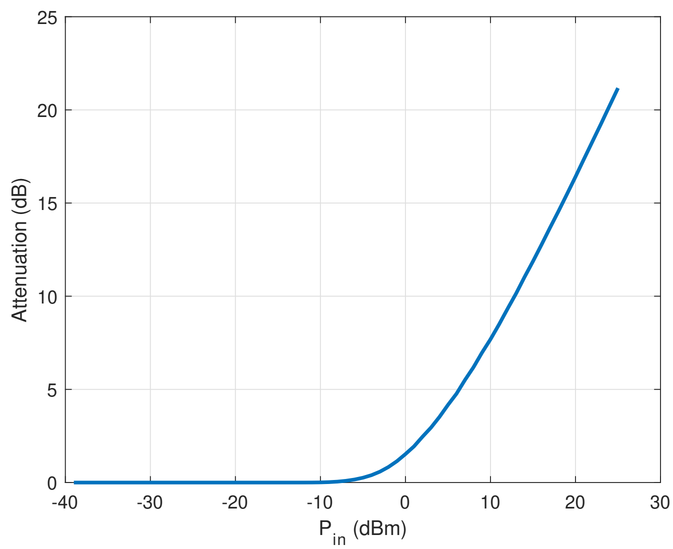


Figure 4.4: Attenuation vs input power graph for proposed limiter.

For Class-A operation, the output signal should ideally swing symmetrically around V_Q. To maintain linearity, the minimum drain voltage should remain above approximately 0.2 V. Thus, the peak swing is approximately:

$$V_{\text{peak}} \approx V_Q - 0.2\,\text{V} = 2.7\,\text{V} \tag{4.9}$$

This corresponds to a total peak-to-peak voltage swing of:

$$V_{\text{pp,drain}} = 2 \times V_{\text{peak}} = 5.4\,\text{V} \tag{4.10}$$

At the quiescent point, the drain current is $I_D = 3.3$ mA, and the drain voltage is $V_D = 2.91$ V, implying that the load impedance seen by the drain is:

$$R_{\text{load}} = \frac{V_D}{I_D} = \frac{2.91\ \text{V}}{3.3\ \text{mA}} \approx 880\ \Omega \tag{4.11}$$

Assuming this 880 Ω impedance is matched to 50 Ω via an ideal transformer or matching network, the voltage transformation factor is:

$$\frac{V_{\text{pp},50}}{V_{\text{pp,drain}}} = \sqrt{\frac{50}{880}} \Rightarrow V_{\text{pp},50} = \frac{5.4\,\text{V}}{\sqrt{880/50}} \approx 1.28\,\text{V} \tag{4.12}$$

This results in an output power of:

$$P_{\text{out}} = \left(\frac{V_{\text{pp},50}}{2\sqrt{2}}\right)^2 \Big/ 50 \approx \left(\frac{1.28}{2\sqrt{2}}\right)^2 \Big/ 50 \approx 6\,\text{dBm} \tag{4.13}$$

Given an amplifier gain of approximately 14 dB, the estimated input 1 dB compression point is:

$$P_{\text{in1dB}} = P_{\text{out1dB}} - \text{Gain} = 6\,\text{dBm} - 14\,\text{dB} = -8\,\text{dBm} \tag{4.14}$$

This calculation serves as an estimate of the LNA's linearity limit and validates that the selected bias point and matching strategy are consistent with the required signal handling capabilities.

Since there is a stabilization resistance in the drain, the actual value of the input compression point will be lower than the calculated value above. That resistance will absorb a significant portion of the output power.

Chapter 5

Circuit Design and Simulation

This chapter presents the proposed low-noise amplifier's schematic design and simulation results. The design was first implemented using ideal passive components to validate the basic matching and gain structure. Next, realistic vendor-based models were used to account for non-ideal parasitics and verify performance under practical conditions. Simulations were conducted to evaluate S-parameters, noise figure, stability, and input/output matching, all centered around the 123 MHz target frequency corresponding to 3 T MRI systems. Keysight Advanced Design Studio (ADS) was used as a simulation tool.

The amplifier is based on the common-source topology using the SAV-541+ GaAs E-pHEMT transistor. The input is matched to the low-impedance output of an MRI receive coil, while the output is matched to 50 Ω for compatibility with downstream signal processing or measurement equipment. A feedback biasing network provides single-supply operation as discussed in Chapter 4. Using Equation (4.2) and Equation (4.3) to get 3 mA gives the $R_1 = R_2 = 3.9$ kΩ, $R_3 = 2.2$ kΩ, and $R_4 = 390\ \Omega$ with $V_{dd} = 4.2$ V, $V_g = 0.12$ V, and $V_{BE} = 0.6$ V.

$$3.3\ mA \approx \left(\frac{4.2 - 0.6}{3900 + 2200}\right) \cdot \frac{2200}{390} - \frac{0.12}{3900} \tag{5.1}$$

Figure 5.1 shows the complete schematic of the design.

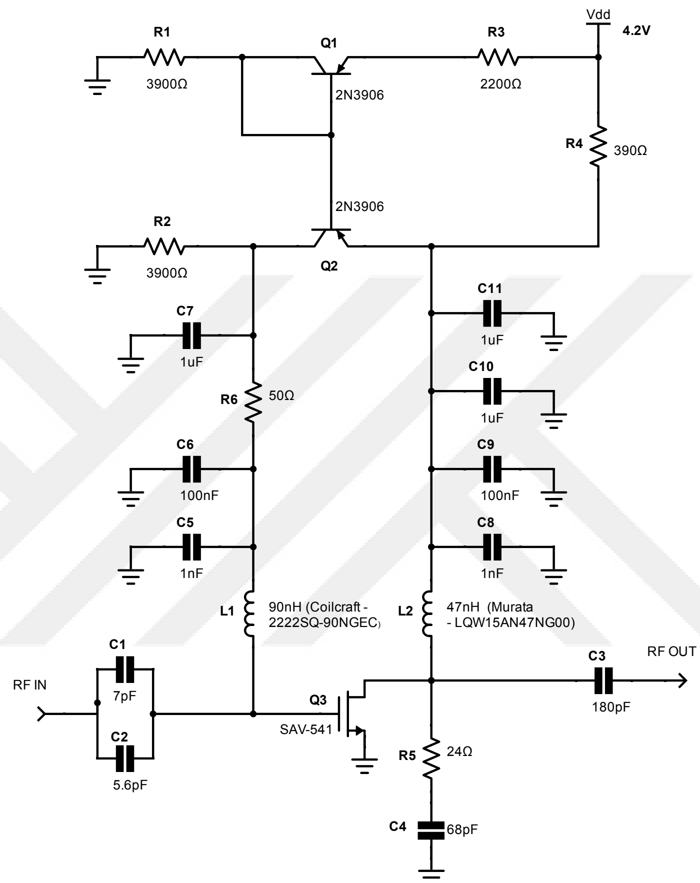


Figure 5.1: Schematic of the LNA circuit using SAV-541+ with feedback biasing and matching networks.

Input impedance matching was achieved using a high-Q 90 nH air-core inductor (Coilcraft 2222SQ-90N) as a DC feed with DC block capacitors placed parallel to increase flexibility in hardware tuning. This inductor was chosen for its low series resistance and magnetic compatibility. Input matching was not aimed at 50 Ω, but rather optimized for power transfer from a short circuit impedance at 123 MHz. C1 + C2 and L1 resonate at 123 MHz as a series resonant circuit to generate the short-circuit input impedance. The inductance value is slightly smaller than the resonant value because of the addition of the input capacitance of the pHEMT transistor. Smith chart analysis was used to visualize the impedance transformation.

Initial simulations used ideal inductors and capacitors to validate the matching network, transistor gain, and noise figure. Later, S-parameter models of the SAV-541+ and the Coilcraft 2222SQ-90N inductor were incorporated to reflect real-world behavior better. The component vendors supplied these models, including parasitic elements such as series resistance, packaging inductance, and dielectric losses. The simulation was repeated with ideal models to investigate these realistic effects, and the comparative results for S_{11} are shown in Figure 5.2.

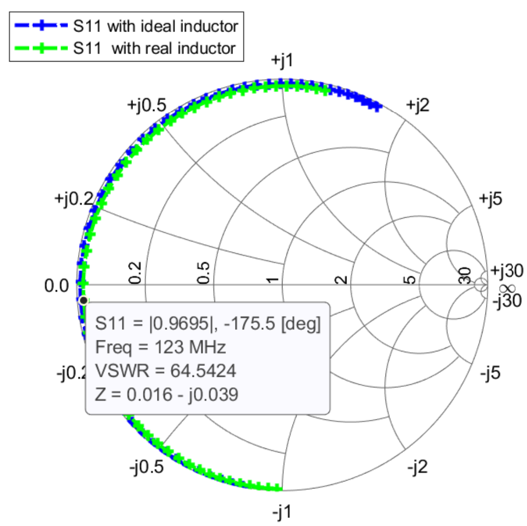


Figure 5.2: Simulated S_{11} with ideal input DC feed inductor (blue) and with real input DC feed inductor (green). Note a slight shift in phase and magnitude due to parasitics and conduction loss.

Simulation of the realistic design achieved a forward gain (S_{21}) exceeding 10 dB and a noise figure below 0.7 dB at 123 MHz. The input reflection coefficient (S_{11}) remained bigger than -0.3 dB. Figure 5.3 gives S-parameters simulation results in dB.

The amplifier's stability was analyzed using the Rollett stability factor (K). Across a wide frequency range (10 MHz to 1 GHz), the amplifier maintained $K > 0.95$, indicating conditional stability. However, due to additional losses mainly caused by the conduction loss in PCB and ESR of the capacitors, the

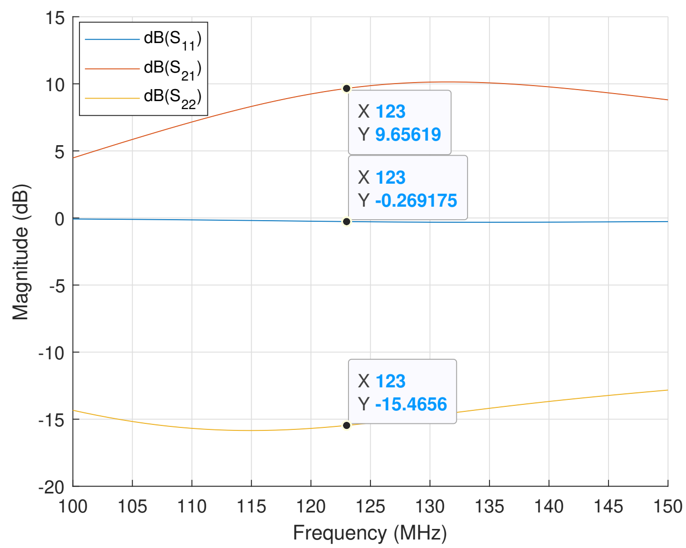


Figure 5.3: Simulated S-parameters using realistic models.

K factor was left at 0.95 in the simulation. This result was achieved without requiring source degeneration or additional shunt feedback, thanks to careful output load selection and a high-impedance RF choke on the drain. Figure 5.4 shows the simulated K factor across frequency.

Noise figure simulations were performed using the transistor's noise model, assuming a 50 Ω noise source at the input. At 123 MHz, the simulated noise figure was approximately 0.85 dB, consistent with the datasheet performance and vendor-provided models. This validates the suitability of the selected bias point and component values for ultra-low-noise operation. The NF simulation results are shown in Figure 5.5 in the frequency range of 105- 150 MHz.

5.1 Input Protection Diodes

Since LNA is the first component in the receiver system, it is prone to high-power input signals. To operate successfully after such signals, protection should be made. In this thesis, a back-to-back connected PIN diode and Schottky diode pair is used for this purpose. Figure 5.6 shows the updated schematic for this

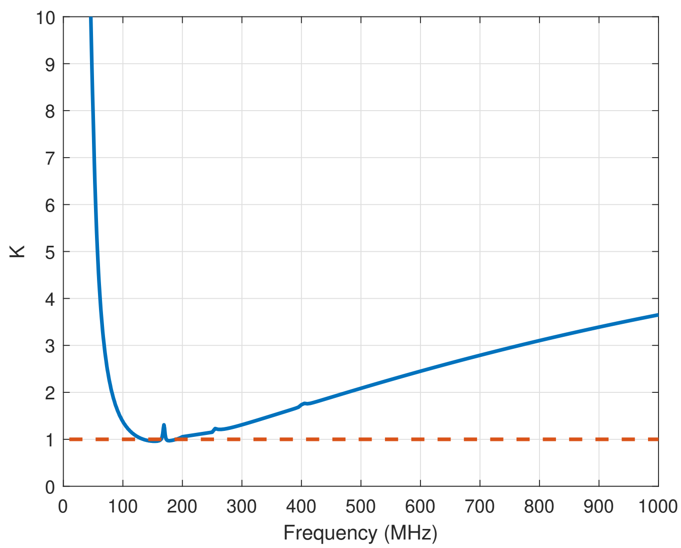


Figure 5.4: Stability factor K versus frequency across the wide bandwidth.

purpose as discussed in Section 4.5. Since diodes introduce additional capacitance at the gate node, RF matching capacitors C1+C2 are also changed for a better input short-circuit performance. Moreover, to get better P_{1dB}, output matching also changed from optimum gain to optimum power with some degradation in S_{22}.

Due to the lack of a PIN diode model or S-parameters file for low power levels, tuning was accomplished in the hardware, and results are provided in Chapter 6. The output matching network was also tuned for better P_{1dB} using a triple stub tuner, and then relevant updates were made in the circuit.

Both gain suppression and recovery behavior are influenced by the selection of bypass capacitors. Larger capacitor values are generally preferred for attenuating high-frequency gain, while smaller values facilitate faster recovery by allowing quicker discharge paths. These trade-offs can be analyzed through simulation. Using LTSpice, a transient analysis was performed to determine the effect of varying capacitor C5 and C8 on the recovery characteristics of the gate voltage. During this test, the bias circuitry and transistor are used. Transistor is selected among the examples, and its threshold is adjusted to 50 mV. Saturation behavior is modeled by putting a parallel pulsed current source to the drain, and its

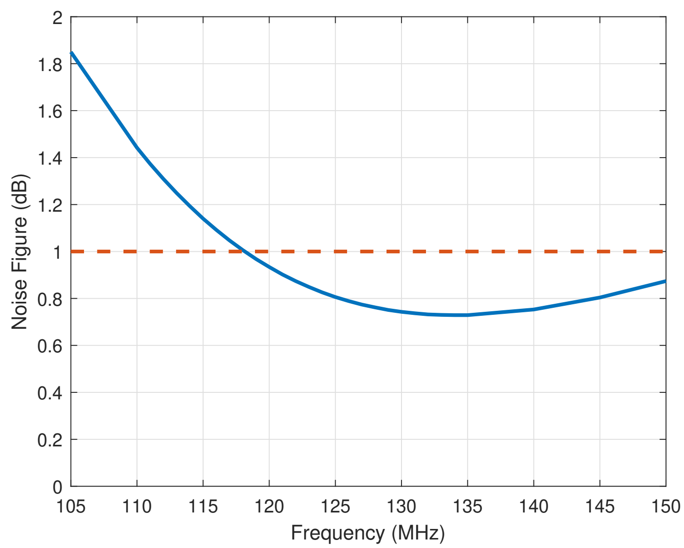


Figure 5.5: Simulated noise figure of the amplifier between 105-150 MHz.

magnitude is increased to 6 mA for 1 ms. Recovery is monitored by checking the time that the drain current goes to its small signal value.

As shown in Figure 5.7, reducing total capacitance from 1 μF to 4.7 nF significantly improves the recovery time, but further reduction increases the AC gain of this bias circuit, and it may deteriorate RF performance. Based on this analysis, the bypass capacitors were selected as C5 = C8 = 4.7 nF, and others were removed.

The corresponding AC response of the bias network, depicted in Figure 5.8, confirms that the gain remains sufficiently low across the frequency band of interest, thereby ensuring that the biasing circuitry does not interfere with the performance of the RF signal path.

Simulation results confirm that the amplifier design achieves high gain, low noise, and stable performance at the 123 MHz MRI operating frequency. Figure 5.9 shows the layout of the designed PCB to be used in the measurements. The next chapter will describe the physical layout implementation and measured performance, followed by a comparison with the simulated data.

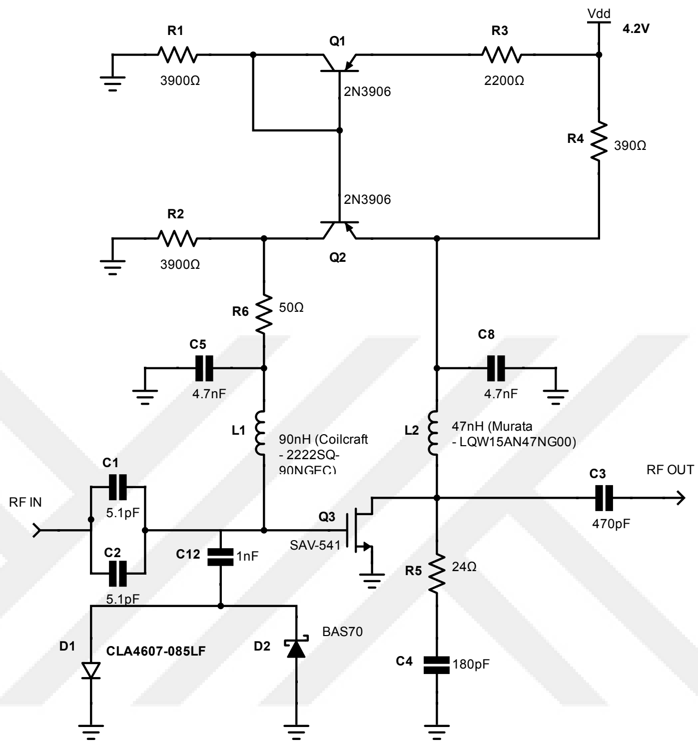


Figure 5.6: Schematic of the LNA with diode protection.

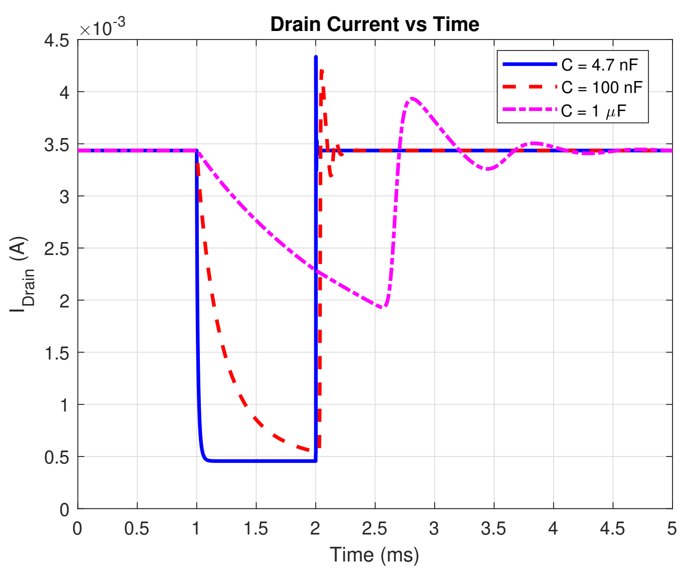


Figure 5.7: Drain current vs time when circuit has high current at drain between 1- 2 ms for bypass capacitors of C5 = C8 = 4.7 nF, 100 nF, and 1 μF. C6, C7, C9, C10, and C11 are removed for this test.

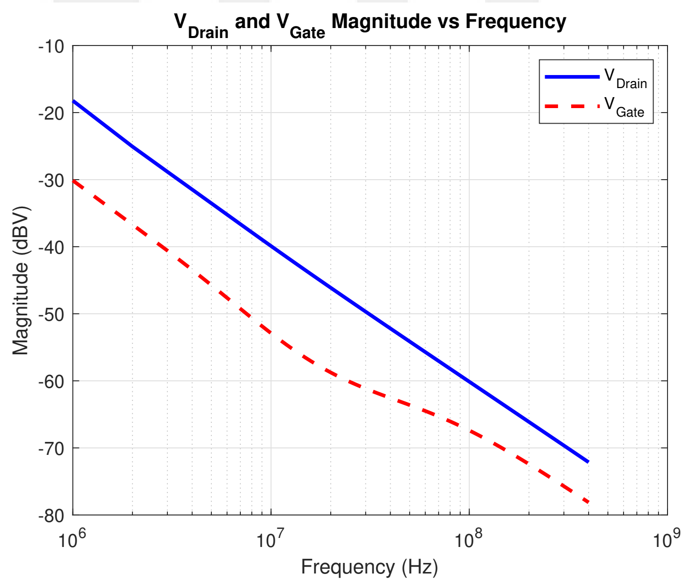


Figure 5.8: Voltage gain vs frequency with selected bypass capacitors.

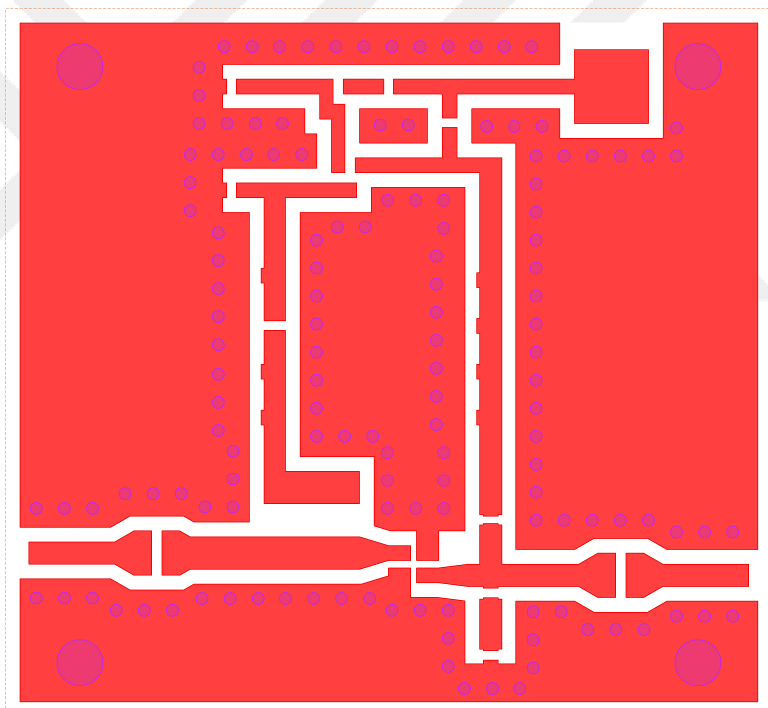


Figure 5.9: Top view of the designed PCB layout.

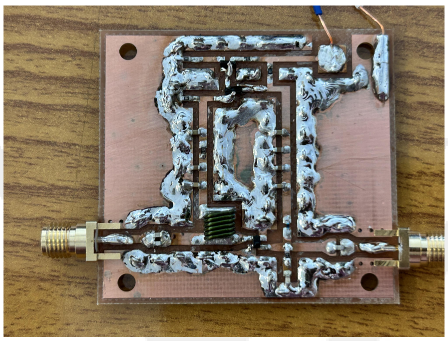
Chapter 6

Implementation and Measurement

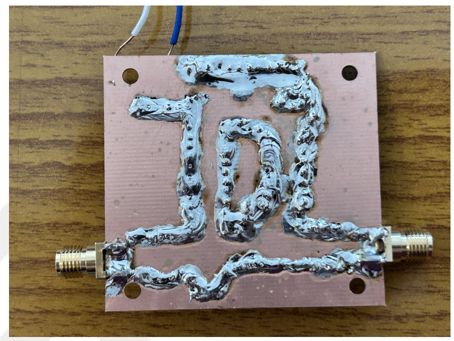
This chapter describes the practical implementation of the designed LNA circuit, including PCB layout, assembly, and performance measurements. Measurement results are compared with the simulated data discussed in Chapter 5, highlighting the effects of layout parasitics, connector interfaces, and component tolerances. The impact of MRI-specific constraints, such as magnetic compatibility and power handling, is also addressed. Also, to be safe in real imaging scenarios where high input power may be present, some sort of protection should be done. Another version with protection diodes and slight updates in the matching circuit is discussed.

The circuit was implemented on a two-layer FR-4 PCB using standard surface-mount components. Special attention was paid to minimizing parasitic inductance and ensuring a continuous ground return path to reduce potential stability issues. A solid ground plane was used on the bottom layer, and the top layer included short, wide traces for RF paths, with careful via placement for referencing ground equally at every node.

To maintain MRI compatibility, all components were selected for non-magnetic construction. This included air-core inductors, ceramic capacitors, and plastic-packaged transistors. No ferrite beads or magnetically reactive shielding elements were used, preventing distortion of the MRI's static and RF magnetic fields. The final assembly is shown in Figure 6.1.



(a) Top view of the assembled PCB. The left side is the RF input, and the right side is the RF output.



(b) Bottom view of the assembled PCB.

Figure 6.1: Top and Bottom views of the assembled PCB.

Measurements were performed using a vector network analyzer (Agilent E5071C Network Analyzer) for S-parameters and a calibrated noise figure analyzer (HP 8970B Noise Figure Meter) for NF verification. The circuit was powered with a regulated 4.2 V DC supply, and the bias current was monitored to ensure correct device operation. The amplifier was tested at 123 MHz, corresponding to the Larmor frequency for hydrogen nuclei in a 3 T MRI system.

The S-parameters were measured to verify the amplifier's input, output matching, and gain. The measured results are shown in Figure 6.3, where the gain (S_{21}), input reflection (S_{11}), and output reflection (S_{22}) were evaluated. The amplifier achieved a measured gain of approximately 14.5 dB at 123 MHz, higher than the simulated value of 9.65 dB. The input return loss was 0.28 dB, and the output return loss was better than 10 dB, indicating good impedance matching at both the input and output. The S-parameters measurement results are shown in Figure 6.3 in the frequency range of 100- 150 MHz. Also, Figure 6.3 gives the measured S_{11} on the Smith Chart, showing the impedance is quite close to the short.

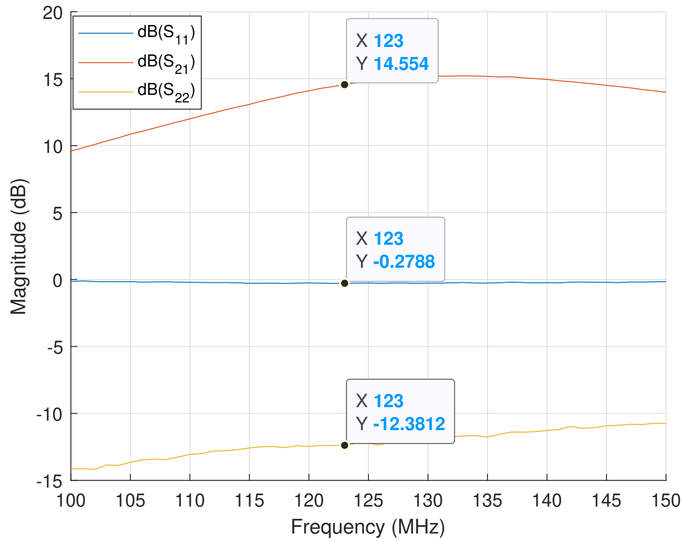


Figure 6.2: Measured S-parameters of the amplifier. Input match S_{11}, gain S_{21}, and output match S_{22} are shown.

Noise figure (NF) measurements were conducted using a calibrated noise figure analyzer. The measured noise figure of the amplifier was approximately 0.64 dB, slightly better than the simulated value of 0.86 dB. This confirms that the amplifier operates with very low noise, crucial for maintaining signal integrity in MRI systems. The NF measurement results are shown in Figure 6.4 in the frequency range of 110- 150 MHz.

Figure 6.5 demonstrates the forward gain (S_{21}) vs input power (P_{in}). From this graph, P_{1dB} can be calculated as:

$$P_{\mathrm{1dB}} = P_{\mathrm{in1dB}} + \mathrm{Gain} = -10.75\,\mathrm{dBm} + 13.6\,\mathrm{dB} = 2.85\,\mathrm{dBm} \qquad (6.1)$$

This result is less than the calculated value of 6 dBm in Section 4.6 because this version is matched for better output return loss.

The amplifier's power consumption was measured to ensure it met the design requirements for low-power operation. The amplifier was powered at 4.2 V and consumed approximately 12.6 mW, which aligns with the predicted value of

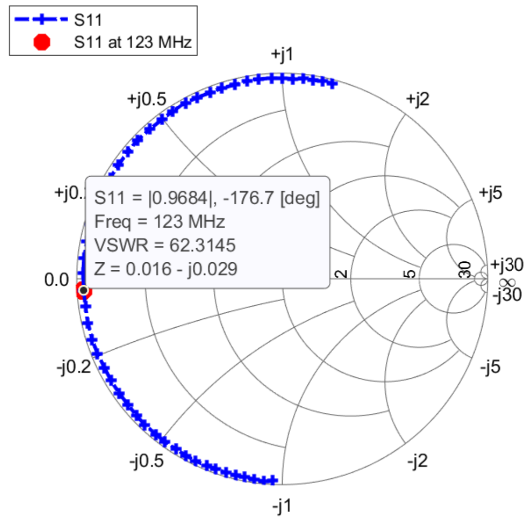


Figure 6.3: Measured S_{11} of the amplifier.

12.6 mW. This low power consumption ensures that the amplifier can be used in multi-channel MRI systems without generating excessive heat, which could cause performance degradation over time.

6.1 Protection Diode Insertion

Since LNA is the first component in the receiver system, it is prone to high-power input signals. To operate successfully after such signals, protection should be made. In this thesis, a back-to-back connected PIN diode and Schottky diode pair is used for this purpose. Figure 5.6 shows the updated schematic for this purpose as discussed in Section 4.5. Since diodes introduce off-capacitance in the small signal regime, RF matching is also changed for better performance. Moreover, to get better P_{1dB}, output matching also changed from optimum gain to optimum power with degradation in S_{22}. Figure 6.6 shows the S-parameter measurement results for this version. From the measurements, a gain of 14.9 dB, input return loss of 0.32 dB, and output return loss of 8.5 dB were reached. Figure 6.7 illustrates the phase of input impedance, which is close to a short circuit. From Figure 6.8, the noise figure of this design is 0.79 dB.

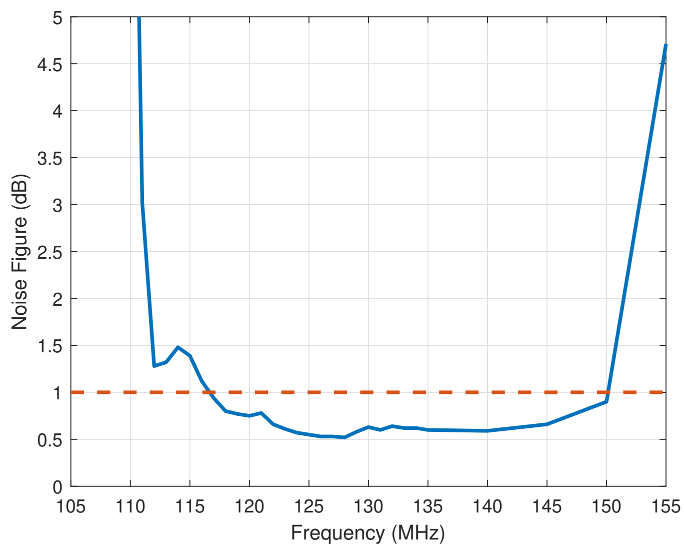


Figure 6.4: Measured noise figure of the amplifier between 110- 150 MHz using a calibrated NF analyzer.

From Figure 6.9, P_{1dB} can be calculated as:

$$P_{\mathrm{1dB}} = P_{\mathrm{in1dB}} + \mathrm{Gain} = -9.65\,\mathrm{dBm} + 14.1\,\mathrm{dB} = 4.45\,\mathrm{dBm} \tag{6.2}$$

Since this version is updated for better output power, its P_{1dB} is higher than optimum gain matching, being 2.85 dBm. This result also confirms the calculated value of 6 dBm in Section 4.6.

6.1.1 Recovery-Time Measurement

Figure 6.10 shows the test configuration used to measure the limiter's recovery time. A continuous low-level tone (123 MHz, –30 dBm CW) from Signal Generator 1 provides the baseline small-signal input to the LNA, while Signal Generator 2 injects high-power pulses (123 MHz, 17 dBm peak; 15 ms period, 1 ms pulse width) that drive the limiter into its saturation region. Because of the power combiner's 3 dB loss, each generator's output is attenuated by 3 dB before reaching the LNA input. The LNA output is monitored on an oscilloscope to determine

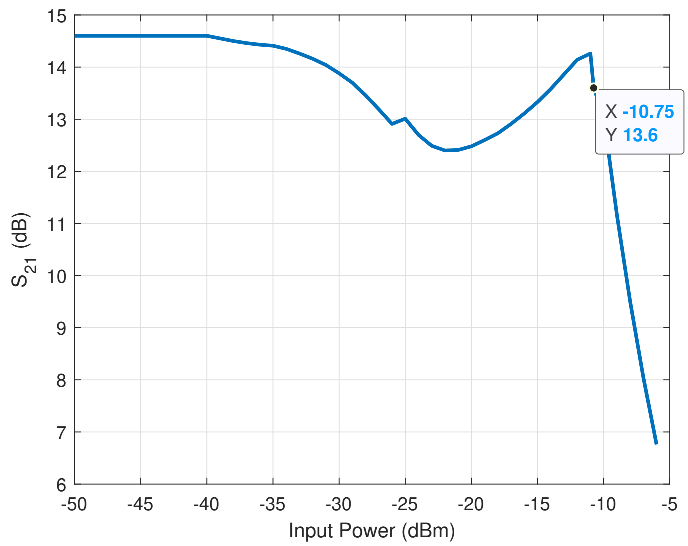


Figure 6.5: Linearity measurement at 123 MHz.

the time required for the circuit to return to its small-signal operating point.

Figure 6.11 and Figure 6.12 compares the two bias-network configurations: $C_{total} = 1.1\ \mu$F versus $C_{total} = 4.7\ n$F at the drain and gate lines separately. In these figures, yellow (top) traces are the input signal, and red (bottom) traces are the output signal. The measurements confirm the trends predicted in Section 4.4: using 4.7 nF bypass capacitors yields a significantly faster recovery (3.5 μs) than 1.1 μF capacitor recovery time (0.65 ms). Decreasing capacitor values beyond these values deteriorates the RF performance of the circuit.

6.1.2 MRI Measurement

The LNA was tested using a real MRI signal to evaluate its performance under practical operating conditions. In this experiment, the authentic MRI output was applied directly to the LNA input. The primary goal was to assess the signal-to-noise ratio (SNR) and examine the LNA's behavior during high-power RF pulse events. To achieve this, the digital output from the ADC was processed using MATLAB code, which enabled the separation of signal and noise components.

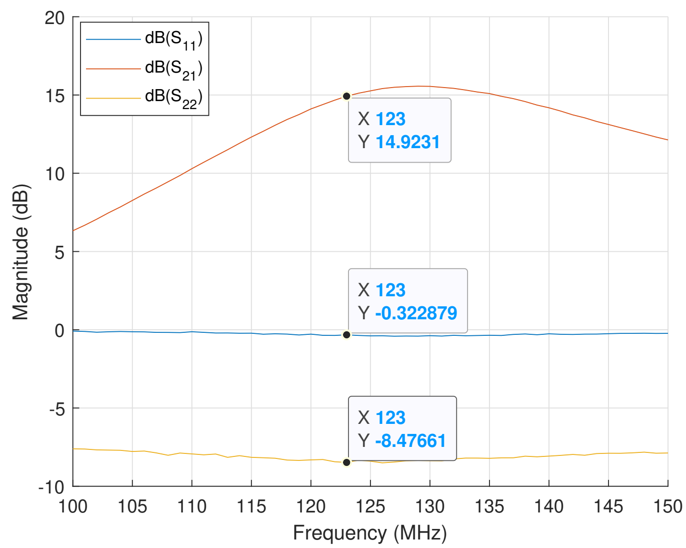


Figure 6.6: Measured S-parameters (S_{11}, S_{21}, S_{22}) of the circuit with protection.

The output was measured separately during both signal and noise-only periods, allowing for a calibrated comparison of amplitude levels over time. This setup enabled a clear evaluation of the LNA's stability, SNR performance, and recovery behavior under MRI-related interference. As shown in Figure 6.13, although the input signal reaches a high level initially, the amplifier handles the transition without entering saturation. No dead time or signal loss is observed, confirming that the protection circuitry and biasing are sufficient to maintain continuous linear operation, even immediately following strong transmit leakage pulses.

A phantom measurement was carried out using a standard MRI test object to check the performance of the low-noise amplifier. The axial and sagittal images shown in Figure 6.14 display good signal uniformity across the phantom. These results confirm that the amplifier operates with sufficient gain and low noise to preserve image quality.

Compared to Figure 6.14, the images in Figure 6.15 were acquired using a commercial TL5500 preamplifier, which provides approximately 10 dB higher gain. Both sets of images exhibit similar spatial uniformity. However, the additional gain can contribute to improved signal-to-noise ratio and robustness, especially under lower signal conditions.

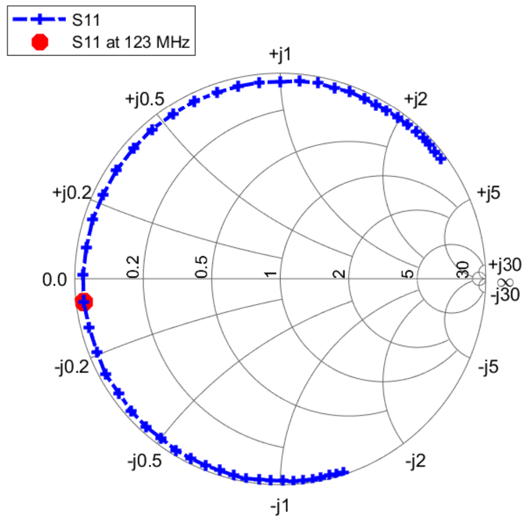


Figure 6.7: Measured S_{11} of the circuit with protection on a Smith chart.

Table 6.1 summarizes the key performance metrics of the amplifier, comparing the simulated and measured values.

The LNA design presented in this chapter has been successfully implemented and characterized. The amplifier demonstrates high gain, low noise, and stability, making it suitable for integration into MRI receiver systems. The measured results closely match the simulated performance, confirming that the design meets the stringent requirements for MRI applications.

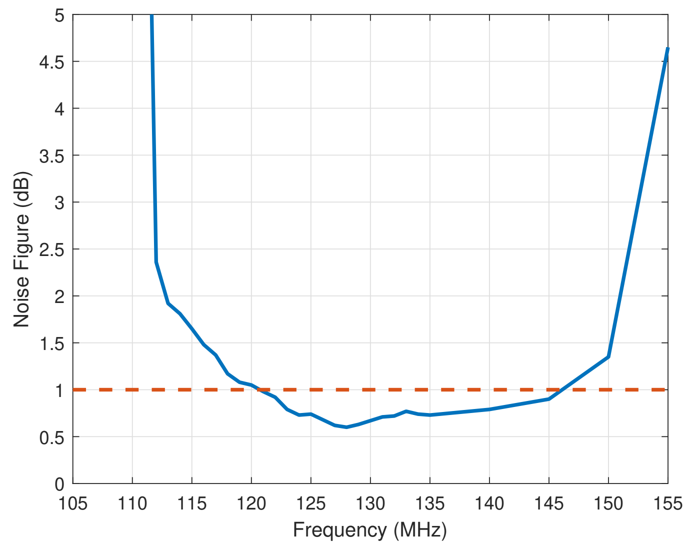


Figure 6.8: Noise figure measurement of the circuit with protection from 110–150 MHz.

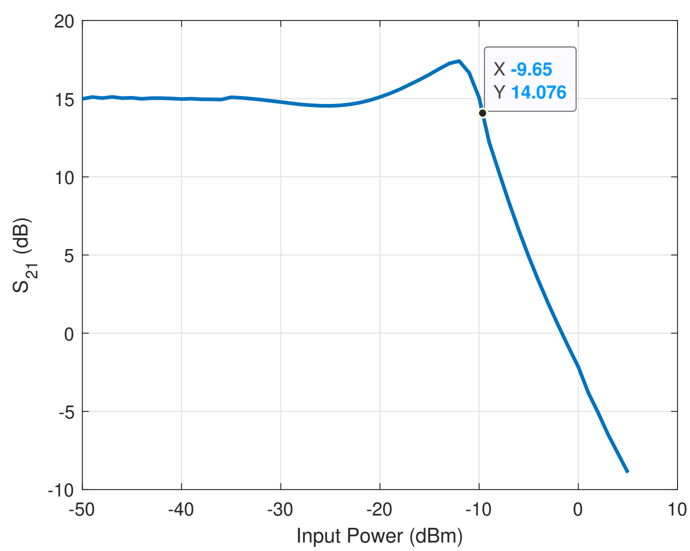


Figure 6.9: Linearity measurement of the circuit with protection at 123 MHz.

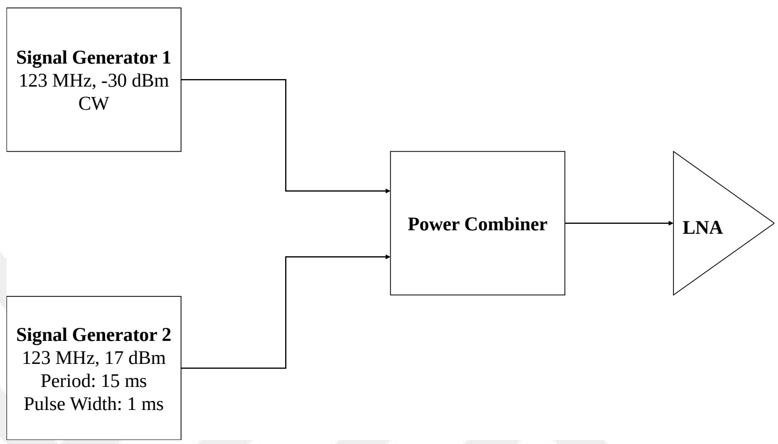


Figure 6.10: Recovery time measurement setup.

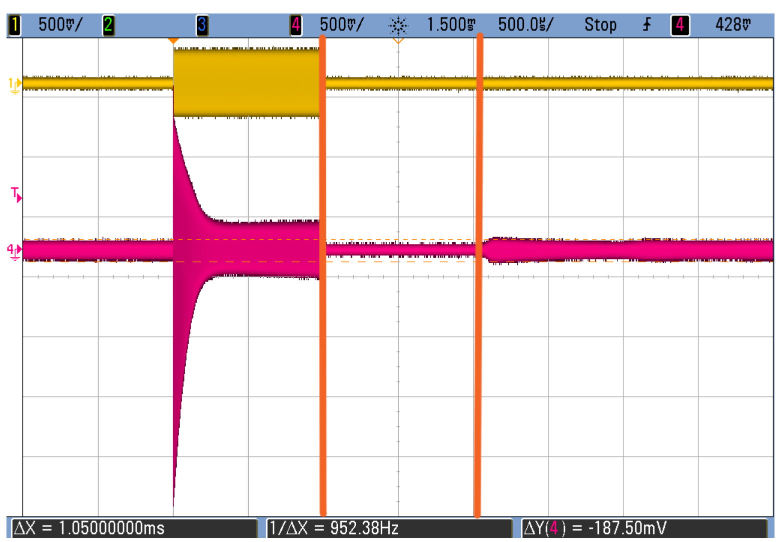


Figure 6.11: Recovery time of the circuit is 1.05 ms when C5 = C8 = 1 nF, C6 = C9 = 100 nF, and C7 = C10 = C11 = 1 μF.

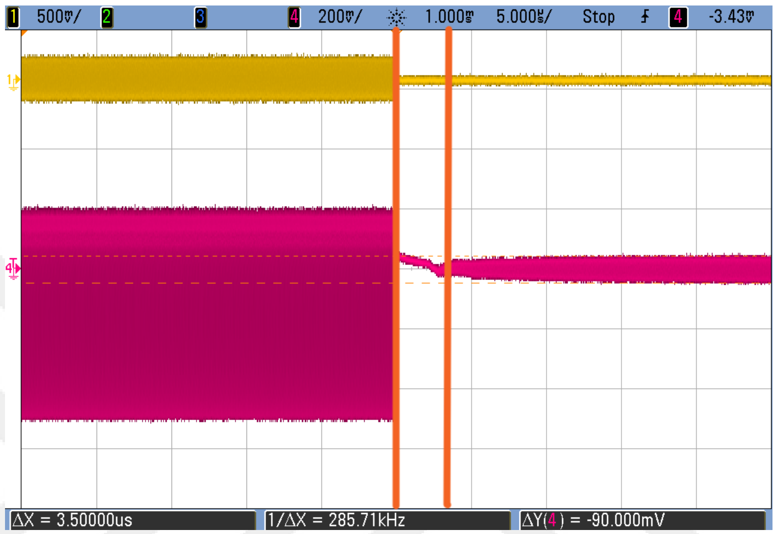


Figure 6.12: Recovery time of the circuit is 3.5 μs when C5 = C8 = 4.7 nF and other bypass capacitors removed.

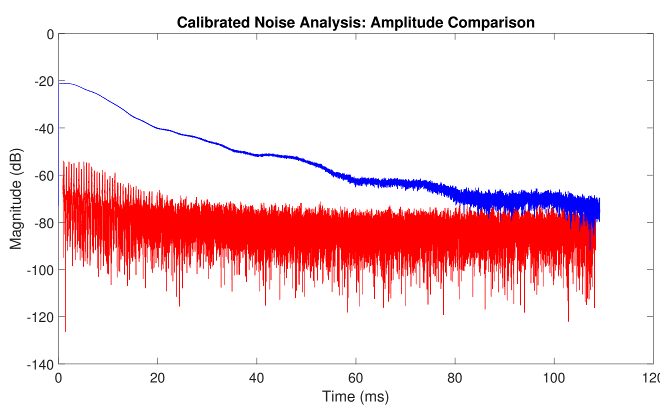
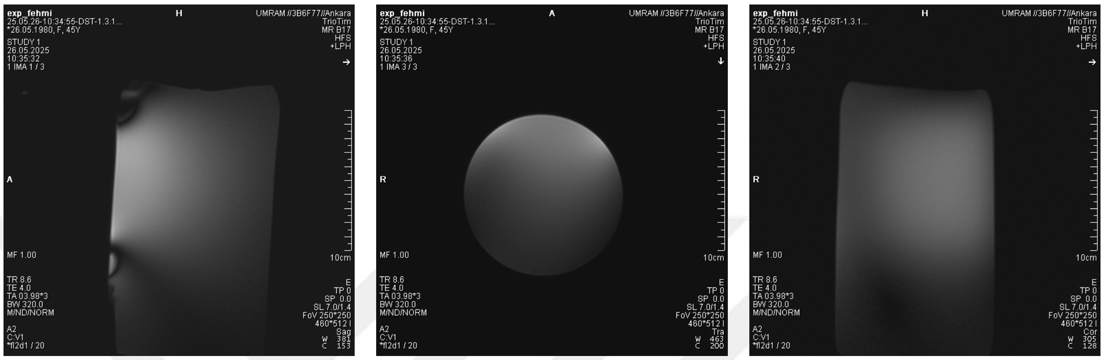
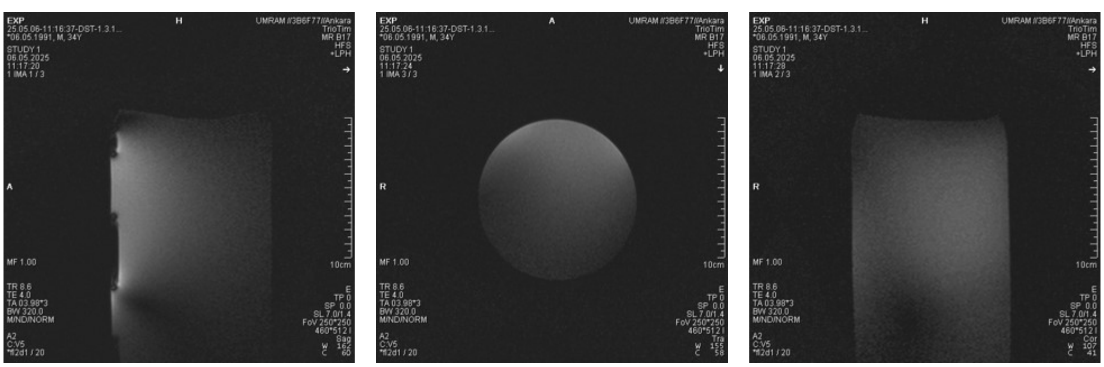


Figure 6.13: Signal amplitude (blue) and noise level (red) with respect to time when C5 = C8 = 4.7 nF and other bypass capacitors removed.



(a) Sagittal view 1 (b) Axial view (c) Sagittal view 2

Figure 6.14: Axial and sagittal MRI slices of the phantom showing uniform signal distribution.



(a) Sagittal view 1 (b) Axial view (c) Sagittal view 2

Figure 6.15: Axial and sagittal MRI slices of the phantom using Texas Instruments' TL5500 preamplifier.

Table 6.1: Comparison of Measured and Simulated LNA Performance at 123 MHz

Parameter	**Simulation**	**Measurement**	**Measurement (With Protection)**
Gain (S_{21})	9.65 dB	14.55 dB	14.92 dB
Input Reflection Coefficient (S_{11})	-0.27 dB	-0.28 dB	-0.32 dB
Output Reflection Coefficient (S_{22})	-15.5 dB	-12.4 dB	-8.5 dB
Noise Figure	0.85 dB	0.64 dB	0.79 dB
Power Consumption	12.6 mW	12.6 mW	12.6 mW

Chapter 7

Conclusion

This chapter summarizes the key findings of the thesis, compares them with recent advancements in MRI-specific Low Noise Amplifier (LNA) designs, and discusses potential areas for future work in the field. The amplifier design presented in this work has been evaluated for its performance, including noise figure, gain, power consumption, and linearity. The design successfully meets the stringent requirements for MRI systems, and its performance is comparable to or exceeds that of several recent designs, as outlined in the literature review.

7.1 Summary of Key Findings

The design of a low-noise amplifier for 3 T MRI systems operating at 123 MHz has been carried out with a focus on minimizing noise figure, optimizing gain, and ensuring stability, while maintaining magnetic compatibility with MRI systems. The amplifier with protection diodes, based on a common-source topology using the Mini-Circuits SAV-541+ GaAs pHEMT transistor, was found to achieve:

- **Gain**: Approximately 14.9 dB at 123 MHz, almost equal to the target.
- **Noise Figure**: Measured at 0.79 dB, which is lower than the target of

1 dB.

- **Input Matching**: Achieved a input reflection coefficient (S_{11}) of -0.32 dB, indicating good impedance matching for the MRI coil requirements.
- **Power Consumption**: The amplifier consumed 12.6 mW, aligning with the predicted value.
- **Linearity**: Measured as -9.65 dBm at the input, being enough for MRI requirements.
- **Output Matching**: Achieved an input reflection coefficient (S_{22}) of -8.5 dB, indicating both good impedance matching for the subsequent components and high linearity.
- **Recovery Time**: The version with protection diodes achieved 3.5 μs recovery time when 14 dBm of input power was applied for 1 ms.
- **Bandwidth**: The 3 dB bandwidth of the amplifier, defined as the frequency range over which the gain remains within 3 dB of its peak value, extends from 115 MHz to 148 MHz, resulting in a total bandwidth of 33 MHz.

The design was successfully implemented on a two-layer FR-4 PCB, and the measured performance was consistent with the simulated results. This demonstrates the effectiveness of the chosen topology and component selection in meeting MRI-specific design constraints, such as low noise, stability, linearity, and recovery time.

7.2 Comparison with Recent MRI-Specific LNA Designs

Table 6.1 compares the designed LNA with similar alternatives. This work outperforms others in terms of its power consumption and performs comparably in other aspects.

Table 7.1: Comparison of Key Performance Metrics for Recent MRI-Specific LNA Designs

Design	**Frequency**	**Gain (S_{21}) (dB)**	**Noise Figure (dB)**	**Input Reflection Coefficient (S_{11}) (dB)**	$\boldsymbol{P_{\mathrm{in1dB}}}$ **(dBm)**	**Power Consumption (mW)**
This work	123 MHz	14.5	0.64	-0.28	-10.75	12.6
This work (with protection)	123 MHz	14.9	0.73	-0.32	-9.65	12.6
Kabel et al. (2017)	32 MHz	11.6	0.45	-0.12	-18	75
Cao et al. (2016)	123 MHz	32	1.02	-1.25	-28.5	215
Johansen et al. (2017)	32.1 MHz	20	0.75	-0.05	-13.8	99
Horneff et al. (2019)	1.5 MHz-90 MHz	44	0.45	-	-	55
Commercial (Siemens-7576312)	123 MHz	27	0.71	-0.65	-14.5	196
Commercial (Texas Instruments-TL5500)	123 MHz	28	0.5	-0.52	-15	110
Commercial (WanTcom Inc.-WMA32C)	32 MHz	28	0.7	-0.89	-18	180

7.3 Areas for Future Work

While the proposed design meets the key performance criteria for 3T MRI systems, there are several areas where future improvements can be explored:

- **Bandwidth Expansion**: The current design is optimized for a narrow frequency band around 123 MHz. It could improve its versatility by extending the bandwidth to support multi-frequency MRI systems or higher-field strength (e.g., 7 T).

- **Multi-Channel System Integration**: As MRI systems increasingly adopt multi-channel receiver arrays, further work could focus on integrating multiple LNAs into a single, compact system while maintaining low noise and power consumption.

- **Advanced Materials**: The use of newer semiconductor materials such as Gallium Nitride (GaN) or Indium Phosphide (InP) could be explored to improve noise figure and gain, especially for higher-frequency or high-power applications.

- **Linearity**: While the current design has decent P_{1dB}, increasing the current and changing the output matching network would give higher P_{1dB}.

- **Input protection**: Choosing a more suitable PIN diode for the operation frequency may improve the recovery time further. Use of a second and inverted PIN diode/Schottky diode circuit at the input may also reduce the signal level at the input of LNA during the MRI transmit pulse.

7.4 Final Remarks

This thesis presented a low-power, low-noise amplifier design optimized for 3 T MRI systems. The proposed design meets or exceeds the performance of existing MRI-specific LNAs in terms of gain, noise figure, linearity, and power consumption. This design outperforms others in terms of its low power consumption without sacrificing noise figure, input return loss, and linearity. Additionally, the recovery time is fast enough for MRI signals not to miss any information. The design could be adapted with further refinement for broader MRI applications, including multi-frequency systems and higher-field MRI environments. The findings highlight the importance of balancing noise, power, and stability in the design of MRI LNAs and provide a strong foundation for future research and development in this area.

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Appendix A

LTSpice Simulation Bench

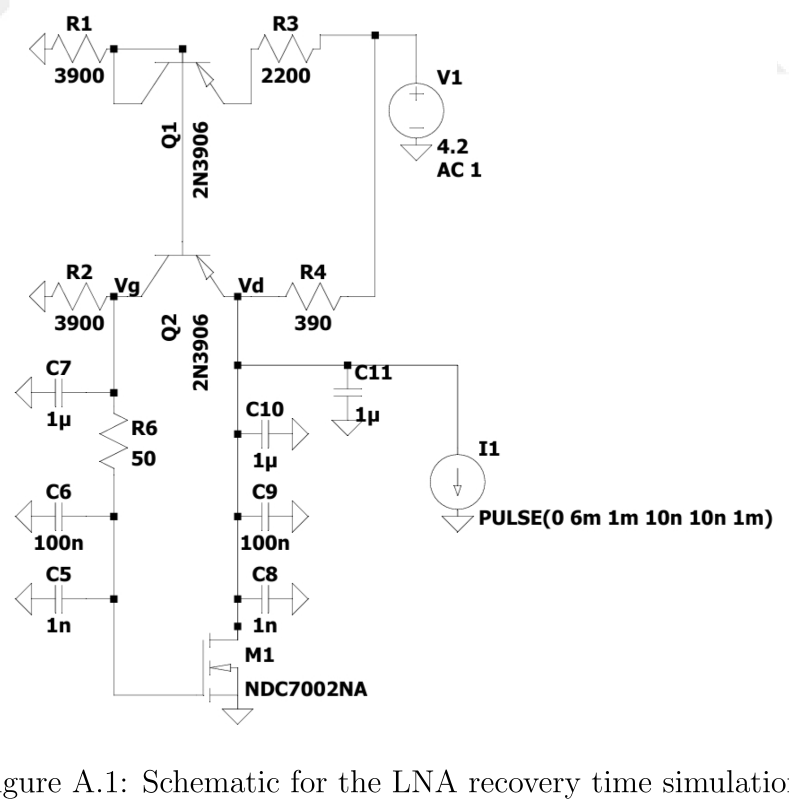

Figure A.1: Schematic for the LNA recovery time simulation.

LTSpice Simulation Note

Since a pHEMT model was not available for LTSpice simulation, a modified Spice model of an NMOS transistor was used instead. The following SPICE model was applied to approximate the desired behavior with the threshold voltage changed to 0.05V:

```
.model NDC7002NA VDMOS(Rg=3 Vto=0.050 Rd=.8 Rs=.2 Rb=1
Kp=.4 lambda=.01 Cgdmax=.05n Cgdmin=.02n Cgs=.02n
Cjo=.02n Is=2p ksubthres=.1 mfg=Fairchild Vds=50
Ron=2000m Qg=1n)
```