A Performance-Enhanced Planar Schottky Diode for Terahertz Applications: An Electromagnetic Modeling Approach

A THESIS

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By

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September 2014

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ABSTRACT

A Performance-Enhanced Planar Schottky Diode for Terahertz Applications: An Electromagnetic Modeling Approach

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Terahertz (THz) spectrum, also called submillimeter spectrum, is a portion of electromagnetic (EM) band within the ITU-designated band of frequencies from 0.3 THz to 3 THz sandwiched between microwave and infrared/optical in EM spectrum. However compared to its microwave and infrared/optical neighbors, 'THz gap' is not heavily explored and it became a hot topic for researchers in recent years. As a result, progress in THz electromagnetics is currently undergoing a renaissance, with burgeoning wide range of applications such as biomedical imaging, sensing and communication applications.

Schottky diode, the fastest conventional detection technology, is a promising component for future THz communication receiver systems. However, the overall performance of planar Schottky diode is limited by parasitic elements at THz frequencies. Recently, a lot of efforts are devoted to decreasing the impact of parasitic components.

In this work, we introduce a systematic approach for analyzing the Schottky diode structure based on electromagnetic modeling using high frequency structural simulator (HFSS). S-parameters obtained from this 3-dimensional EM simulation were imported to Microwave Office environment to extract all parasitic elements (resistances and capacitances) from lumped-equivalent circuit model. Using this methodology, the effect of geometrical design parameters on the performance of the diode is investigated by which an optimized diode can be obtained. Using this methodology, we propose two

concepts to minimize the amount of shunt capacitance and series resistance. The proposed design shows a cut-off frequency that is about 4 times greater than that of reference conventional diode. This methodology is not just limited to the diode but also it can be extended to all integrated planar devices where high frequency cross talk noise is detrimental.

Keywords: *Schottky diode, Terahertz, Electromagnetic Modeling, GaAs*

ÖZET

Terahertz Uygulamaları İçin Optimize Edilmiş Bir Yüzeysel Schottky Diyot: Elektromanyetik Modelleme Tabanlı Bir Yaklaşım

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Milimetre altı tayfı olarak da bilinen terahertz (THz) tayfı, elektromanyetik bantın mikrodalga ile kızılötesi/görünür bölgeleri arasında bulunan ve ITU tarafından 0.3 THz ve 3 THz arasındaki frekansları kapsayacak şekilde tanımlanmış bir frekans bölgesidir. Fakat mikrodalga ve kızılötesi/görünür bölgelere nazaran "THz bölgesi" detaylı olarak incelenmiş bir bölge değildir ve ancak son yıllarda yoğun olarak bilimsel ilgi görmeye başlamıştır. Dolayısıyla, THz tabanlı elektromanyetik araştırmalar günümüzde bir bilimsel devrim altında bulunmakta ve biyotıp, sensörler ve iletişim gibi birçok sektörde kullanım için geliştirilmektedir.

Hali hazırda kullanılan algı sistemlerinin en hızlısı olan Schottky diyodu, THz-bazlı iletişim alıcıları için umut verici bir parçadır. Ancak Schottky diyotlarının verimi, THz frekanslarında bulunan parazitik elemanlar tarafından sınırlandırılmaktadır. Bu parazitik parçaların etkilerinin azaltılması konusunda son yıllarda yoğun ilgi gören bir araştırma konusudur.

Bu çalışmada yüksek frekanslı yapısal simülatör (high frequency structural simülatör, HFSS) yardımı ile elektromanyetik modelleme yapılarak Schottky diyot yapılarının analizi için sistematik bir yaklaşım geliştirilmiştir. 3-boyutlu EM modelleme sonucu alınan S-parametreleri Microwave Office ortamına alınarak tüm

parazitik elemanlar (dirençler ve kapasitanslar) toplu eşdeğer devre modelinden çıkarılmıştır. Bu yöntem kullanılarak bir diyot üzerindeki geometrik tasarım parametrelerinin diyot performansına yaptığı etki görülüp, optimal diyot tasarımları elde edilmektedir. Bahsedilen yöntem ile shunt kapasitansı ve seri direncini minimuma indirecek iki tasarım konsepti öne sürmekteyiz. Öne sürülen tasarım, referans olarak kullanılan standart bir diyoda nazaran dört kat daha yüksek bir kesim frekansı göstermektedir. Kullanılan yöntem, sadece diyot optimizasyonu ile sınırlı olmayıp, yüksek frekanslı çapraz konuşma gürültüsünün azaltılmasının önemli olduğu tüm entegre yüzeysel cihazlar için de kullanılabilmektedir.

Anahtar sözcükler: *Schottky Diyot, Terahertz, Elektromanyetik Modelleme, GaAs*

Dedicated to my dear parents and beloved brothers Mehdi and Akbar…..

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I have no words to express my feelings towards my parents and my brothers Mehdi and Akbar. I dedicate this thesis to you and I hope that this achievement will turn to reality the dream that you had for me all those many years ago when you chose to give me the best education you could. I hope that I will be worthy of your love.

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Chapter 1

Introduction

Terahertz (THz) spectrum, also called submillimeter spectrum, is a portion of electromagnetic (EM) band within the ITU-designated band of frequencies from 0.3 THz to 3 THz sandwiched between microwave and infrared/optical in EM spectrum. However compared to its microwave and infrared/optical neighbors, 'THz gap' is not heavily explored and it became a hot topic for researchers in recent years[1]. As a result, progress in THz electromagnetics is currently undergoing a renaissance, with burgeoning wide range of applications such as biomedical imaging, sensing and communication applications[2–5]. There are several reasons for the fast-growing interest in this spectral region. First, THz waves can penetrate into a wide variety of non-conducting materials such as clothing, paper, cardboard, wood, masonry, plastic and ceramics. But they cannot pass through metals and are strongly attenuated in water. When THz waves pass through any of these materials, their photon energy causes them to interact with material via a number of mechanisms. These mechanisms often involve phonons, weak material bond vibrations and deformations, and consequently are unique to the exact chemical and physical composition of the material.

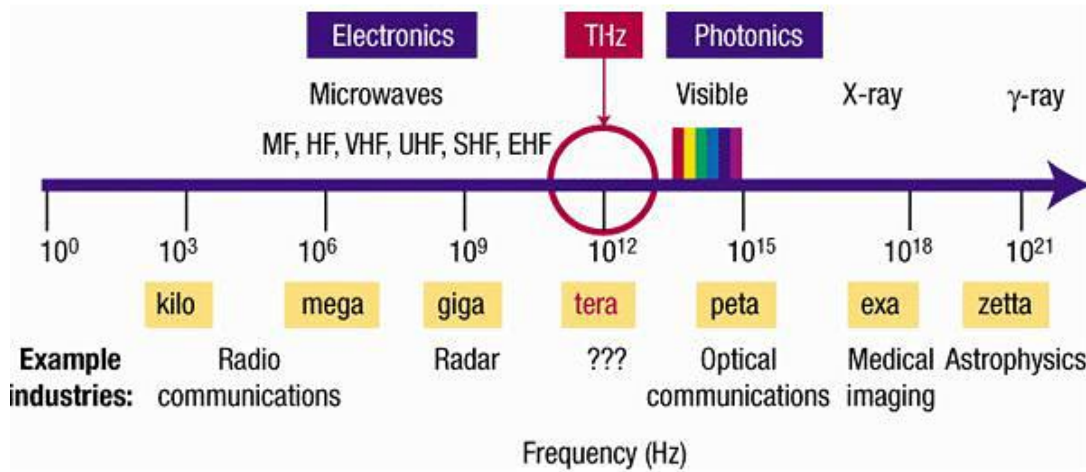

Figure 1.1: The position of THz band between the microwave and far-infrared electromagnetic spectrum [1].

Therefore, any internal variations in thickness, density and/or chemical composition impart information to the THz signal in the form of intensity (absorption) and phase (refractive index) variations[6,7]. The information, obtained from this analysis, can be used to reconstruct two and three dimensional images of objects that are opaque to visible or infrared light. Because a lot of biological objects like living tissue, tumors and DNA have special absorption spectrum in this range[8–12], these substances can be easily identified by using the absorption lines. In other words, considering distinct THz signature of these objects, THz imaging technology for biomedical application is expected to be a non-destructive and safe alternative[1] for conventional x-Ray imaging systems which work based on high energetic x-ray photon and can damage living tissues. It is interesting to note that many explosive and narcotic object has a specific signature in its THz spectra, making THz spectroscopy valuable for security applications[13]. In particular, it is possible to distinguish illegal drugs and explosives from benign compounds. For example, materials can be identified using THz multispectral images and component spatial-pattern analysis without having to open the mail[13]. In spite of all of these potential applications, with the monotonic increasing demand of the higher bandwidth for the next generation wireless communication system, the extension of the operating frequency of the communication system to the millimeter/Terahertz wave regime of the electromagnetic spectrum where several low-attenuation windows exist is inevitable. There are mainly two possible ways in which the data rate can be enhanced. First, by bandwidth

enhancement of the system but the system is inherited with the narrow bandwidth and in most of the cases the device bandwidth is only about 10% of its operating frequency. The next option is increasing the operating frequency in a way that even with the narrowband components; communication systems may fetch a high data rate to the target customers. Recently, to meet the high bandwidth requirement, 60 GHz and 90 GHz[14,15] wireless systems have been developed but they are still insufficient to meet the future requirement. The next best solution to this problem is to move the operating frequency to the terahertz band. However, with the increase in the operating frequency, the device characteristic also changes and there is the need of the analysis of the various THz wireless communication system components [16]. Interestingly, due to its unique position, as this band is situated between these two already well explored regimes of the spectrum, it is possible to use electronic as well as photonic route to pave the way in the terahertz spectrum. In this way, the electronic and photonic routes are capable of exploring these components in the in the near microwave and the far-infrared THz band, respectively[16]. Although, THz communication link in the near millimeter wavelength of the electromagnetic spectrum is convincing and promising, but before full commercialization, the associated limitations of the system needs to be addressed. The atmospheric path loss is the main obstacle for the realization of the commercial THz wireless communication system. This loss is affected by various atmospheric conditions and their effect on the propagation of electromagnetic wave over a wide band of the frequency is shown in Figure 1.2[17]. Fortunately, there are certain low atmospheric attenuation windows in the terahertz region where the successful wireless communication can be established. However, below 1 THz, these windows exist around 220 GHz, 340 GHz, 410 GHz, 650 GHz and 850 GHz[18], in which the atmospheric loss is below 100 dB/km and they may be used in the short-range wireless communication. Apart from this, above 16 km from Earth's surface where the effect of moisture is negligible, the attenuation is also insignificant and such elevation, hence the inter-satellite communication can be established.

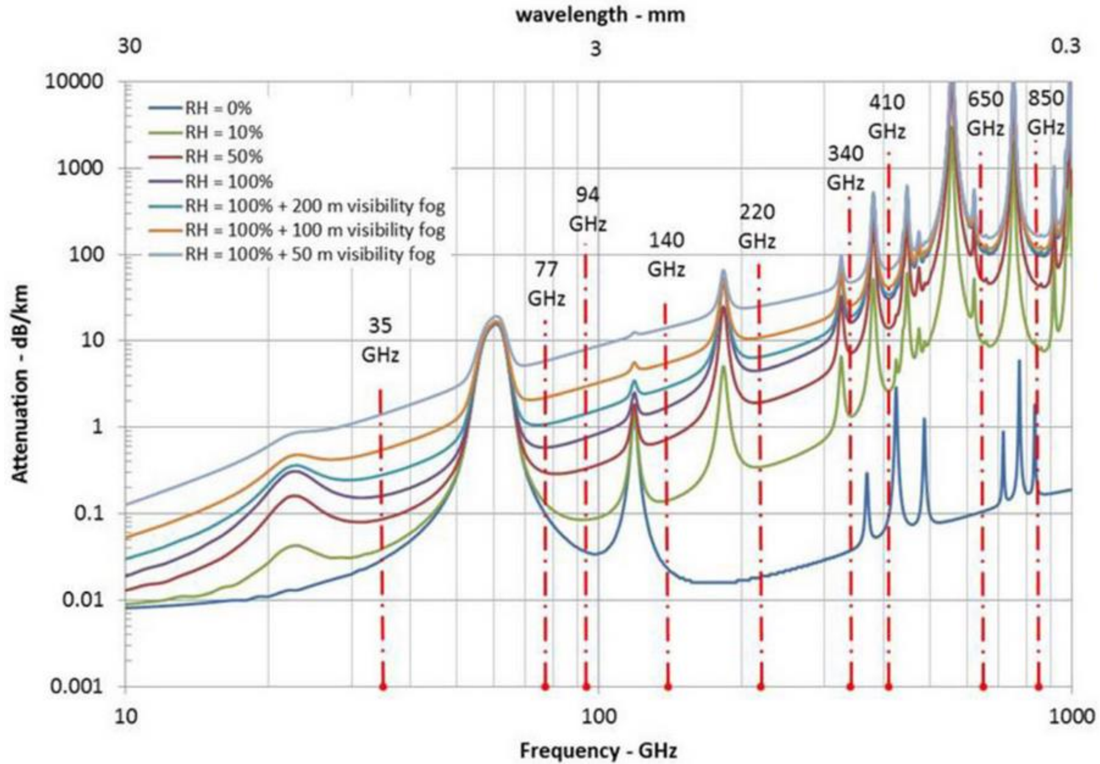

Figure 1. 2: Atmospheric attenuation in THz and infrared band [18].

As a result, design of a performance optimized THz communication transmitter/receiver has attracted much attention in recent years. Most of the initial efforts are devoted to optimize the performance of all of the sub-components of a THz receiver. Consequently, demand for compact, fast, and reliable THz components such as tunable oscillators, mixers and multipliers used in THz sources has increased significantly.

GaAs-based Schottky diodes, as a building block for all of these components, are the most popular devices for THz sources[19–24] and detectors [25–28], mainly due to the high electron mobility, simplicity of integration with planar THz device structures and fast operation. However, the performance of such planar GaAs Schottky diodes degrades at THz region as a result of high frequency parasitic effects. Therefore, this research work aims to provide a comprehensive study on the impact of different parameters in planar THz Schottky diode performance through developing a systematic modeling approach. This thesis contains results and features which can provide an optimized approach for designing future performance enhanced THz components.

1.1 Background

When a metal makes intimate contact with a semiconductor, a barrier is formed at the metal-semiconductor interface. This metal-semiconductor structure possesses rectifying properties, and is referred to as Schottky barrier diode. The earliest systematic investigation on metal-semiconductor rectifying systems is generally attributed to Braun [29], who in 1874 discovered the asymmetric nature of electrical conduction between metal contacts and semiconductors such as copper and iron sulphide. The point-contact rectifier in various forms found practical applications beginning in 1904[30]. In 1938, Schottky suggested that the potential barrier could arise from stable space charges in the semiconductor alone without the presence of a chemical layer[31]. The model arising from this consideration is known as the Schottky barrier diode. The Schottky diode has a long history of use for both heterodyne and direct detection of power at submilimeter wavelengths. Schottky diodes have the advantage that they can operate at ambient or cryogenic temperatures and allow for long integration times. But the feature which makes it special for THz communication receivers is its extremely short response time compared with other detection technologies.

A great deal of research has been necessary to bring GaAs Schottky technology to the point where it is suitable for use in THz receiver applications. Although it is beyond the scope of this thesis to outline this research in detail, it is helpful to acknowledge several of the major milestones. The first such milestone was the initial development of the "honeycomb" Schottky diode by Young and Irvin in 1965[32]. This work used modern photolithographic technology to define the metal-semiconductor junction in a reproducible and controlled manner. Their basic chip design, shown in Figure 1.3, is still in use today, mainly because the whisker contact adds minimal series resistance and shunt capacitance to the diode circuit. In addition, microwave engineers have used the whisker to couple the high-frequency radiation into the diode, and have even used the whisker inductance to tune out part of the shunt capacitance. Once the basic chip design of Young and Irvin was recognized as a suitable structure for high-frequency receivers,

many groups began investigations to determine the-optimum design for the GaAs epitaxial layers and to improve the fabrication technologies. Major contributions to this

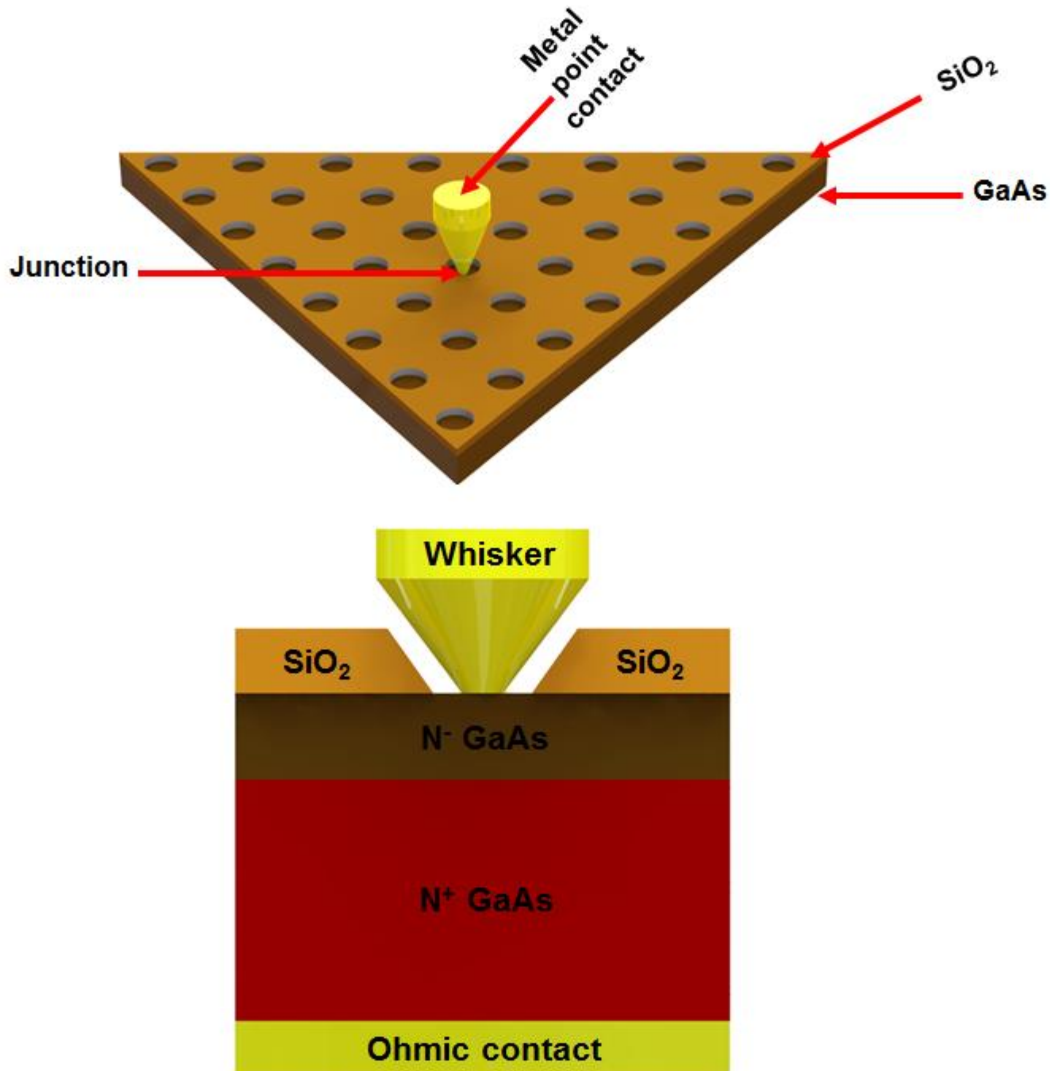

Figure 1. 3: Honeycomb structure of whisker-contacted Schottky diode.

work were made by over a dozen research teams including those at Bell Labs, MIT, University College in Ireland, Chalmers University in Sweden, and the University of Virginia. Theoretical research has resulted in great advance in the understanding of electronic conduction in the diode, including the effect of electron tunneling on the IV curve[33] and the increase in series resistance due to the skin effect[34] and plasma resonance [35]. The generation of noise in the diode was intensively studied by many groups, culminating in the Unified Noise Theory of Viola and Mattauch[36], which was later extended to include the so called hot-electron noise[37]. Modern fabrication technology

allowed the reduction of the anode size and vastly improved control of the thickness and doping concentration of the epitaxial layer, reducing junction capacitance and series resistance. The fabrication of highly reliable metal-semiconductor interfaces was seen as a major prerequisite to the fabrication of devices without excess noise, and many papers were written on this subject[37,38]. However, the fragile whisker-contact is difficult to space qualify and integration with surrounding circuitry is extremely challenging. The University of Virginia developed planar Schottky mixer diode with good RF performance

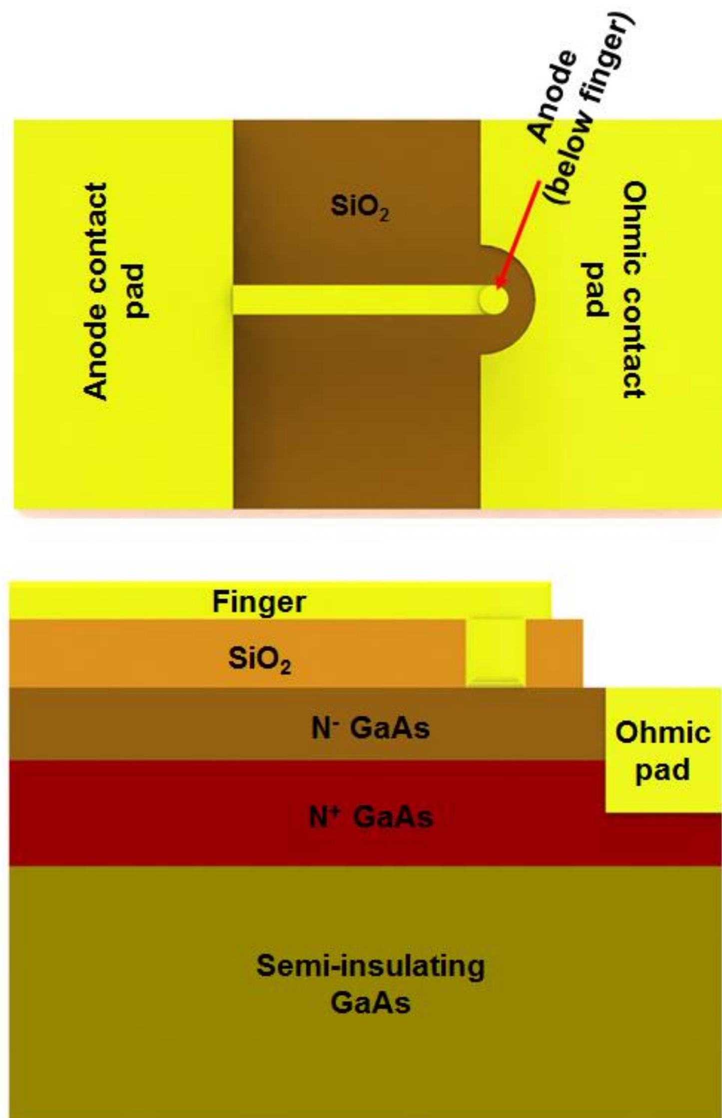

Figure 1.4: Planar Schottky diode structure

inherent mechanical ruggedness, and adaptability to higher levels of integration [39], as depicted in Figure 1.4. Afterwards, several groups have successfully used the planar diode structure in receivers[40,41]. GaAs planar Schottky devices have been under development for a number of years now, with the hope that they will replace the whisker-contacted honeycomb diodes currently being used for most high frequency space borne applications and they can open a new path for circuit integration towards building highly compact and low cost transmitters/receivers. However, the planar design of this structure with a high dielectric GaAs substrate exhibits higher parasitic shunt capacitance, which is a detrimental effect for such a high frequency operating region and it can degrade the planar diode performance. Planar Schottky diodes fabricated at the University of Virginia utilize the surface channel structure as illustrated in Figure 1.5. The cathode pad is an ohmic contact formed on the highly doped n-type GaAs (n^+ buffer layer). The anode pad may also be an ohmic contact or it may be a non-ohmic metallization on GaAs or on a silicon dioxide layer above the GaAs. A single circular Schottky barrier diode is formed near the ohmic contact pad. The forward electron current path is from the ohmic contact metallization through the n^+ buffer layer to the n-type GaAs below the anode. From here, the electrons are emitted into the anode metal, travel along the finger and into the anode contact pad. The semi-insulating substrate and the surface channel ensure that all conduction current passes through the Schottky contact. As it can be seen in this figure, there are a lot of parasitic elements which can induce detrimental effects on the diode performance through reducing the cut-off frequency of the device. That is why it is an important task to suppress the effect of these parasitic elements via optimization of diode design.

During the last couple of decades, intensive studies are focused on this area to enhance performance of Schottky diodes mainly via 2 routs 1) proposing an innovative design, and 2) utilizing complex fabrication methods to mitigate these parasitic elements' impact.

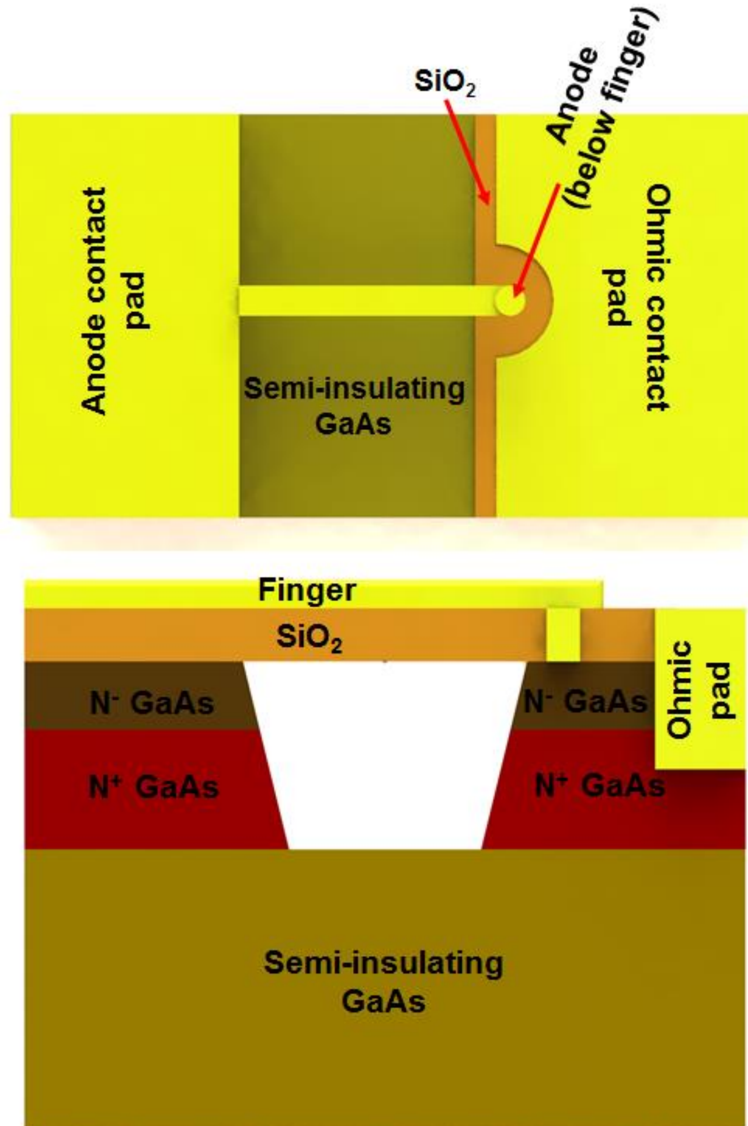

Figure 1. 5: Surface channel planar Schottky diode suitable for THz application

All of these new designs are based on this motivation to isolate finger from high-dielectric GaAs substrate. Quasi-vertical planar Schottky diode (QVD)[42] and parallel finger diode[43] are the examples of these designs. On the other hand, to reduce substrate losses, the diode substrate transfer technology[44–46] and the monolithic diode-circuit integration technology, using membrane monolithic diode[47] and substrateless techniques[48], are developed. But all of these methods impose several additional fabrication steps which make diode fabrication to be a complex and expensive process.

1.2 Motivation and results

Considering all of these facts, it is an imperative task to develop a systematic modeling approach being able to optimize device performance without adding any new complex fabrication steps. In this work, we introduce a systematic approach for analyzing the Schottky diode structure based on electromagnetic modeling using High Frequency Structural Simulator (HFSS)[49]. Afterwards, S-parameters results obtained from this 3-D EM simulation were imported to Microwave Office environment[50] to extract all parasitic resistances and capacitances from lumped-equivalent circuit model. Using this methodology, the effect of all geometries on the performance of the diode is obtained in which an optimized performance for the diode can be attained. At the end of this development, we introduce two ideas to minimize the amount of shunt capacitance and series resistance. The proposed design shows a cut-off frequency which is about 4 times greater compared to that of reference conventional diode. This methodology is not just limited to the diode device but also it can be extended to all integrated planar devices in which cross talk noise degrades device high frequency performance. As starting point for making a performance enhanced THz Schottky diode, the methodology presented here provides a good estimate of diode impedance which might be used to design monolithically integrated detectors where THz antenna impedance is conjugate-matched to the Schottky diode impedance to increase detector sensitivity.

1.3 Thesis outline

The outline of the thesis can be categorized as follows;

Chapter 1 provides a brief summary about planar THz Schottky diode including a background on today's technology and challenges for more development, a description of the main motivation of this thesis and an outline about all chapters of the thesis.

Chapter 2 provides a basic description of the physics beyond device performance and its operation principle including current-voltage (I-V) characteristics and series resistance.

Chapter 3 is conducted with a step by step explanation of the modeling approach. In this chapter, model methodology will be illustrated in detail.

Finally in Chapter 4, a parametric study for understanding the impact of all diode parts on parasitic elements will be carried out based on the developed approach. All of the corresponding results and analysis will be scrutinized on their physics. At the end of the thesis, according to the features obtained from this modeling approach two ideas will be proposed to improve device performance; 1) using a deep-trench in the substrate between electrical pads to minimize parasitic capacitance and 2) introducing a closed-loop junction around the Schottky contact to reduce the amount of series resistance losses. As a result, cut-off frequency of the diode will be shown to increase to significantly greater amount in which a reliable performance of the diode in our desired frequency will be achieved.

Chapter 5 will provide a step-by-step explanation of the diode fabrication and all parameters which are important.

Conclusions, appendix and bibliography will complete this thesis.

Chapter 2

THz planar Schottky diodes

2.1 Overview of Schottky diode operation

When a metal comes in contact with a specific type and doping level of a semiconductor, according to continuity of the Fermi level, the band alignment will be in a way that the Fermi levels in the two materials must be coincident at thermal equilibrium. Therefore, a charge dipole between negative charge on the surface of the metal and a positive charge at the semiconductor surface (let's assume n-type semiconductor) will be established which is a result of lining up of the Fermi levels. These positive charges, in n-type semiconductor, arise from conduction electrons receding from the surface, leaving a huge concentration of uncompensated donor space charges at the interface. Since the concentration of these donor ions is several orders of magnitude smaller than that of electrons in the metal surface, this balancing positive species will inhabit a thick layer of

semiconductor which is called depletion region and it consequently will bend semiconductor bands upwards. Thus a potential barrier will exist at the intimate metal-semiconductor (M-S) interface. This barrier is called as Schottky barrier. The potential barrier for the electrons in the semiconductor is also called the built-in voltage. The built-in voltage can be calculated by:

$$q\Phi_{bi} = q(\Phi_M - \Phi_S) \qquad (2.1)$$

In which Φ_M is Metal work function and Φ_S is semiconductor work function, respectively. It should be noted that the work function is the energy difference between the Fermi and vacuum level of a material.

On the other hand the barrier seen by electrons injecting from metal side can be calculated by:

$$q\Phi_B = q(\Phi_M - \chi) \qquad (2.2)$$

Where, χ shows the electron affinity which is the energy difference between the conduction band minimum and the vacuum level of the semiconductor, as shown in Figure 2.1 (a) [1]. Figure 2.1 (b) depicts the band energy diagram for an M-S contact for the case after coming to contact.

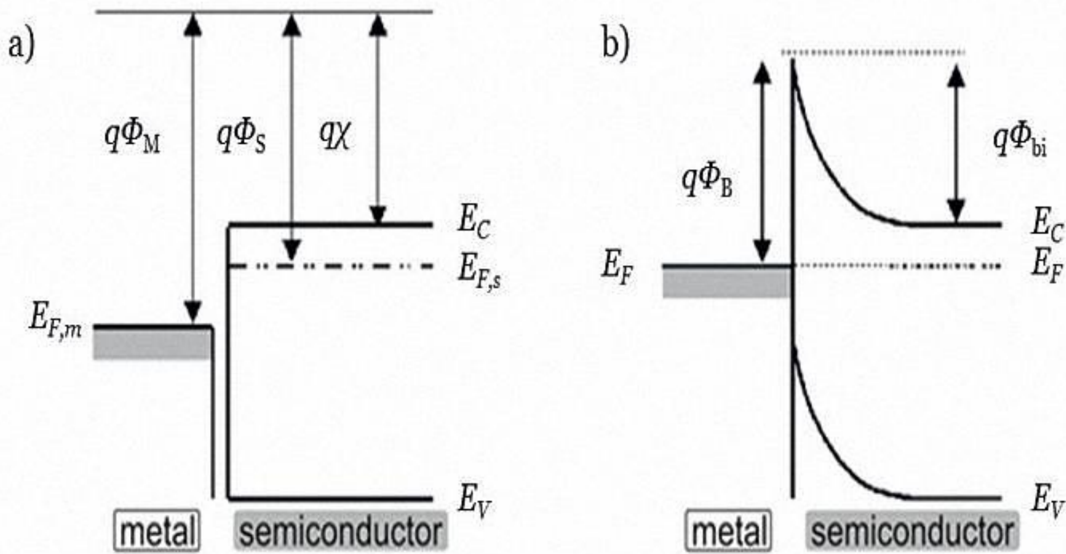

Figure 2.1: Energy band diagram of metal-semiconductor (n-type) contact. In a) metal and semiconductor are not in contact, in b) metal and semiconductor are connected and form a single system.

2.1.1 Current-voltage characteristics

When a bias voltage is applied across the Schottky contact, the current starts to flow. There are two main ways in which electrons can be transported across M-S junction under forward bias as it is shown schematically for n-type semiconductor in Figure 2.2. One is based on thermionic emission process. The thermionic emission theory of current transport in a Schottky diode was first introduced by Bethe. This theory stands up based on 3 assumptions; 1) In vicinity of room temperate, the barrier height $q\Phi_B$ is much larger than kT, 2) thermal equilibrium is established at the plane of the M-S interface and 3) the existence of a flowing net current does not disturb this equilibrium, so that one can superimpose two current fluxes - one from metal to semiconductor, and the other from semiconductor to metal, each with a different quasi-Fermi level. Taking these assumptions, the current-voltage (I-V) characteristic for a Schottky barrier diode can be expressed as:

$$I = I_S \left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{2.3}$$

Where

$$I_S = AA^*T^2 \exp\left(-\frac{q\Phi_B}{kT}\right) \tag{2.4}$$

In this equation, I_S is the saturation current density, q is the magnitude of electronic charge, k is the Boltzmann's constant, T is the temperature, A is the area of Schottky contact, A* is the effective Richardson's constant for thermionic process, and Φ_B is the Schottky barrier height. The effective Richardson's constant is given by:

$$A^* = \frac{4\pi q m^* k^2}{h^3} \tag{2.5}$$

Where m* is the effective mass of the electron in the semiconductor, and h is the Planck's constant. For free electrons the Richardson's constant is 120 $A/cm^2/K^2$.

The second main process for Schottky diode current flow is based on tunneling. Under certain circumstances it may be possible for electrons with energies below the top of the

barrier to penetrate the barrier by quantum-mechanical tunneling. This may modify the ordinary thermionic process in one of two ways which may be understood with reference to Figure 2.2. In the case of a very heavily doped (degenerate) semiconductor at low temperature, the current in the forward direction arises from the tunneling of electrons with energies close to the Fermi energy of semiconductor. This process is referred to as

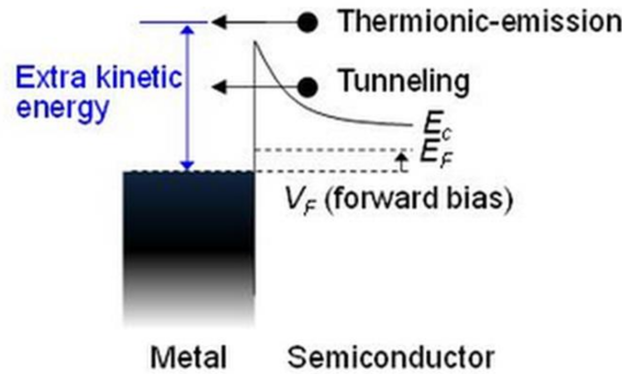

Figure 2.2: Current transport processes in a forward biased Schottky barrier diode.

field emission. If the temperature is raised, electrons are excited to higher energies, and the tunneling probability increases very rapidly because electrons have to cross a thinner and lower barrier. On the other hand, the number of electrons decreases very rapidly with increasing energy, and there will be a maximum contribution to the current from electrons which have an energy E_m above the bottom of the conduction band. This process is known as thermionic-field emission. If the temperature is raised still further, a point is eventually reached in which virtually all the electrons have enough energy to go over the top of the barrier; the effect of tunneling is negligible and pure thermionic emission is obtained.

The theory of field and thermionic-field emission has been developed by Padovani and Stratton, and by Crowell and Rideout. According to this theory, the current-voltage (I-V) relationship is of the form:

$$I = I_s \exp\left(\frac{qV}{kT}\right) \tag{2.6}$$

In which

$$E_0 = E_{00} coth\left(\frac{E_{00}}{kT}\right) \tag{2.7}$$

The parameter E_0 is referred to as tunneling parameter or characteristic energy. The parameter E_{00} is given by:

$$E_{00} = \frac{qh}{4\pi}\left(\frac{N_D}{m^* \varepsilon_S}\right)^{\frac{1}{2}} \tag{2.8}$$

Here N_D is the donor concentration, m^* is the effective mass of electrons in the semiconductor and ε_S is the permittivity of the semiconductor. The pre-exponential term I_S in Equation (2.6) is a complicated function of the temperature, barrier height and semiconductor parameters, and is given graphically as function of kT/E_{00} by Crowell and Rideout. The physical significance of the tunneling parameter E_{00} is that it is the diffusion potential of a Schottky barrier such that the transmission probability for an electron whose energy coincides with the bottom of the conduction band at the edge of the depletion region is equal to 1/e. Therefore the ratio kT/E_{00} is a measure of the relative importance of thermionic emission and tunneling.

2.1.2 Series resistance

As it is mentioned above, the main concern in diode design and operation is the impact of parasitic elements which degrade device performance by introducing new losses mechanism. Series resistance is one of these parasitic elements which limit the Schottky diode performance for applications in high frequencies. In this section we will try to provide an introduction on series resistance and their effect on device performance degradation. The diode series resistance is a non-trivial parasitic element which models power dissipation inside the diode.

As shown in Figure 2.3, for a typical vertical diode there are four main elements constituting the series resistance which can be expressed by:

$$R_S = R_{Spreading} + R_{Contact} + R_{epi} \tag{2.9}$$

In this equation, where R_{epi} is the junction epitaxial layer resistance, $R_{Spreading}$ is the buffer layer spreading resistance and $R_{Contact}$ is the ohmic contact resistance.

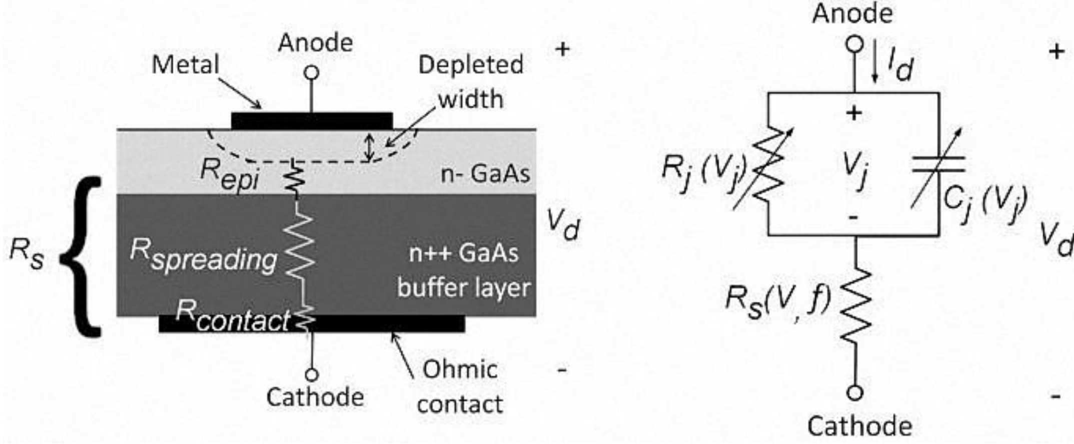

Figure 2.3: A typical Schottky diode. (a) cross-section view and (b) equivalent circuit model.

A. *Buffer layer spreading resistance ($R_{Spreading}$)*

The buffer layer is a highly doped semiconductor layer to provide current flow inside the substrate. Therefore, the finite conductance of the buffer layer results in current crowding and only a portion of total current can be collected at the ohmic contact. This loss is modeled by a resistor, $R_{spreading}$, in the equivalent circuit model. It should be noted that the spreading of the current can also happen in epi layer but considering the fact that the doping level of this layer is an order of magnitude lower we can neglect this resistance. Although the nature of this loss has a close relation with geometrical properties of the device, for a typical vertical Schottky diode, this resistance is calculated to be[51]:

$$R_{Spreading} = \frac{1}{qN_{ds}\mu\, min(d_n + R_b)} \tag{2.10}$$

Where μ and N_{ds} are the electron mobility and doping concentration of the buffer layer, respectively. Also R_b is the shortest distance between the center of the anode and the edge of the radial ohmic contact pad. In upcoming section, we will show that for a planar Schottky diode this current has more complex nature due to its lateral flow and only geometric parameter that affects spreading resistance is the buffer layer thickness.

B. *Ohmic-contact resistance ($R_{Contact}$)*

Ohmic contact resistance is a model for losses through current flow between the semiconductor buffer layer and the external circuit. Like spreading resistance, this resistance is also a geometry-dependent factor. But for a simple conventional Schottky, this can be estimated by[51]:

$$R_{Contact} = \frac{R_{Spreading} L_T}{-2\pi R_b} \left\{ \frac{I_0\left(\frac{R_b}{L_T}\right) - \frac{I'_0\left(\frac{R_C}{L_T}\right)}{K'_0\left(\frac{R_C}{L_T}\right)} K_0\left(\frac{R_b}{L_T}\right)}{I'_0\left(\frac{R_b}{L_T}\right) - \frac{I'_0\left(\frac{R_C}{L_T}\right)}{K'_0\left(\frac{R_C}{L_T}\right)} K'_0\left(\frac{R_b}{L_T}\right)} \right\} \tag{2.11}$$

With

$$L_T = \sqrt{\frac{\rho_c}{R_{Spreading}}} \tag{2.12}$$

I_0 and K_0 represent the modified Bessel functions of the first and second kind. R_b, as mentioned above, is the shortest distance between the center of the anode and the edge of the radial ohmic contact pad. L_T denotes the distance between the center of the anode and the far end of the ohmic contact pad and finally, $R_{Spreading}$ is buffer layer spreading resistance calculated above. Considering the different alloys used for ohmic contact formation in GaAs including, Au/Ge, Pd/Ge, Pd/Si, Ti/Pt/Au, Ni/Ge/Au, Ni/Ge/Ni/Au, the amount of this resistance is couple of order of magnitudes smaller than other components. Therefore, this contact resistance is usually very low and it is safely neglected in calculations.

C. *Junction epitaxial layer resistance (R_{epi})*

A junction epi-layer resistance, R_{epi}, is a resistance that arises due to the undepleted epi-layer. For a typical THz diode, the junction epi-layer thickness, t_{epi}, is within a range of tens to hundreds of nanometers. As it was mentioned before, the spreading of the current in the epi-layer is not as much as buffer layer (due to its low conductivity). Therefore current flow in this layer is concentrated in the vicinity of the anode contact and it can be approximated using equation:

$$R_{epi}(V_j) = \frac{t_{epi} - w_d(V_j)}{Aq\mu_{epi}N_{epi}} \tag{2.13}$$

In which μ_{epi} and N_{epi} are the electron mobility in the epi-layer and donor concentration in the epi-layer, respectively. t_{epi} is the thickness of the epi-layer and $w_d(V_j)$ is the depletion width.

When the diode is forward biased, the depletion width $w_d(V_j)$ of the layer decreases with the increase of applied voltage. On the other hand, when the diode is reversed biased the epi-layer can be fully depleted.

Among these components $R_{Spreading}$ and $R_{Contact}$ depend only on operation frequency but R_{epi} is a function of both operation frequency and applied voltage. Although these formulations provide some initial estimation about different loss components in a typical Schottky contact, they are not applicable to planar design. The reason is 1) these formulas are estimated for a device working under DC or low frequency region 2) all of the losses have strong relation with geometry and materials used for the fabrication of the diode. The main motivation of this work is to provide a systematic approach to achieve accurate estimations on all of these parasitic elements regardless of their geometrical design and working frequency. Next chapter will be devoted to introduce our modeling approach in detail.

2.1.3 Effect of series resistance on current-voltage characteristics

The current-voltage (I-V) relationship for an ideal Schottky barrier diode having thermionic emission as the most important current transport process is given by Equation (2.14). But in general, most of the Schottky barrier diodes exhibit non-ideal behavior, and this means that other transport processes like generation-recombination, tunneling etc. also contribute towards the current flow in the diode. The effects of these current components depend on parameters such as device temperature, device area, dopant concentration, value of the barrier height, density of interface states, structural properties of the interface etc. Some recent studies have shown that the non-idealities can be correlated with the existence of lateral inhomogeneities in Schottky barrier heights in

nanometer length scales. Now the current-voltage relationship for a non-ideal Schottky barrier diode can be expressed as:

$$I = I_S\, exp\left(\frac{q(V-IR_S)}{nkT} - 1\right) \qquad (2.14)$$

where two new parameters are added to the ideal equation to extend it to non-ideal case. These important parameters of the Schottky barrier are ideality factor, n and series resistance, R_s. The ideality factor signifies the relative importance of current transport mechanisms other than thermionic emission in Schottky diode and series resistance shows the losses seen by current through flowing between two contacts (as explained in previous section).

2.2 **Planar THz Schottky diode**

Although whisker-contacted diode benefits from a minimum parasitic capacitance and a simple and highly mature fabrication, they are costly to assemble, show reliability problems due to the whisker contact and are impractical for systems using more than one diode. With the need for low cost and reliable mixer elements, the development of planar Schottky diodes is an important topic of investigation. The essential drawback of these devices with respect to THz applications is the high parasitic capacitance and the increased series resistance compared to whisker contacted diodes. Therefore, in recent years, tremendous studies have been devoted to develop planar Schottky diode design as a promising alternative for whisker-contacted diode in THz applications. These investigations brought Schottky diode community to a conclusion that using the surface-channel type of planar diode can provide a good trade-off between fabrication complexity and detrimental effects of parasitic elements. Therefore, planar Schottky diode technology has been further developed and optimized based on the surface-channel planar configuration. However, even this structure can improve device performance partially and further reduction on parasitic components is desired. Taking all into consideration, it is an essential task to provide a modeling approach in which one can get a deep understanding on all of the geometry-dependent parasitic elements and minimize their detrimental effect on diode performance. The modeling methodology used in this

thesis is an efficient combination of 3D full-wave EM simulation and lumped equivalent circuit parameter extraction. The 3D EM fields inside the lossy material and the fields coupled among different parts of the diode are calculated using the finite-element method. As an outline for this chapter, first we provide a brief introduction on physical structure of planar Schottky diode. Afterward, the equivalent lumped circuit and its contributed parasitic elements will be discussed in detail. Finally, this chapter will be completed by describing the EM modeling approach used in diode performance analysis.

2.2.1 Physical structure and Contributed parasitic elements

A schematic of a typical surface-channel planar Schottky diode (developed for high frequencies) is shown in Figure 2.4 (both cross sectional and top views). As it can be seen from cross sectional view, device consists of layer by layer structure. The chip substrate (or supporting substrate) is a semi-insulating GaAs layer with a typical thickness of 100-500 µm. The epitaxial GaAs structure consists of a thin n-type layer (which has a typical thickness of 100-300 nm) on top of a thick (in the range of 2-5 µm), heavily doped n+ buffer layer. The concentration of n+ doping is in the order of 10^{18}-10^{19} cm^{-3} to provide a good conducting layer for electron flow in the buffer layer and for n^- layer, is approximately an order of magnitude smaller to make a good Schottky contact. The anode which is mainly gold (Au) or platinum (Pt) is formed on the n-type GaAs with a 300-500 nm thick SiO_2 layer providing passivation and insulation. An ohmic cathode pad is also deposited on one end of the chip in close a proximity to the anode. The anode is connected to a bonding pad by means of a narrow finger which is mainly realized by a low loss metal layer like gold and lies on SiO_2 passivation layer to avoid any bending or short circuit with the underlying layers. At the end, an air surface-channel will be formed beneath the finger and completely across the width of the chip to isolate the anode contact pad from the cathode (mitigating buffer-to-buffer coupling). This feature combined with the inherent low dielectric of the air is utilized to reduce the shunt capacitance between the contact pads and the shunt capacitance from the contact finger to the conductive GaAs of the cathode. This structure produces lower shunt capacitance than other designs which rely on mesa isolation. As it can be clearly seen, a lot of parasitic factors including resistances, capacitances and inductances are correlated with

this design. In order to reduce their detrimental impact on device performance, it is imperative to have a better insight about their origin.

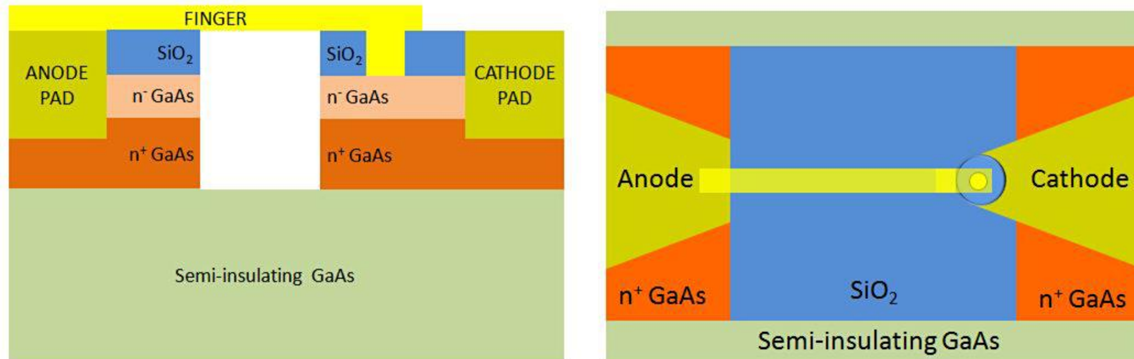

Figure 2.4: A schematic of cross sectional (a) and top view (b) of conventional surface-channel planar Schottky diode.

2.2.2 **Parasitic capacitances**

Figure 2.5 illustrates all parasitic elements contributing to device performance degradation. Total parasitic capacitance (C_p) is comprised of two main parts; finger capacitance (C_f) and pad capacitance (C_{pp}). For finger capacitance, the EM coupling between finger and buffer layer (C_{fb}) and between finger and pad (C_{fp}) model fringing fields, respectively. Also C_{pp1} and C_{pp2} model electrical coupling between contact pads through air and semi-insulating GaAs substrate, respectively.

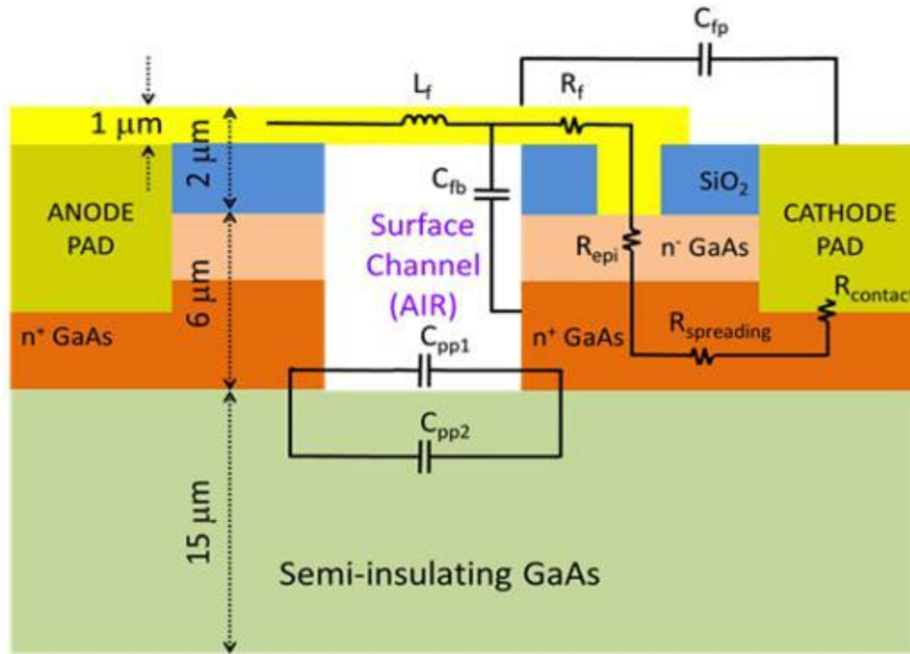

Figure 2.5: Contributing parasitic components in a planar Schottky diode.

As explained earlier, the EM coupling between two buffer layers (pad-to-pad capacitance) can be devided to two parts: 1) through the air with a dielectric constant of 1 and 2) through GaAs substrate with a dielectric constant of 12.9. Considering the simple capacitance formula, it would be anticipated that the GaAs-coupled portion of the wave will be more pronounced compared to the coupling in the air. Also it is expected that this amount is much more dominant than finger induced capacitances due to smaller area associated with the finger. Therefore, it is of great desire to minimize C_{pp} as dominant factor in parasitic capacitances. As a simple idea, this capacitance can be decreased by reducing pad area, increasing pad separation, decreasing substrate dielectric constant and substrate thickness. However, all of these modifications are somehow impractical and induce several detrimental side effects in device performance. Pad dimensions are limited by considerations of handling and bonding by ohmic contact resistivity in which such small dimensions can make fabrication process tough and unrepeatable[44]. Also, large pad spacing, in addition to increasing footprint, leads to excessive inductance that is not desirable and such a long finger makes fabrication process more difficult[52]. Finally, it should be noted that for such a high-speed application, a semiconductor with high

mobility and high saturation electron velocity is a must. These factors are available in only couple of materials such as GaAs, InP, GaInAs which all of them have a dielectric constants similar to that of GaAs substrate. The most effective solution for decreasing pad-to-pad capacitance is to reduce the substrate thickness. But to reduce this component, a significant reduction in substrate thickness is needed. Considering inherent brittleness of the GaAs wafers such thinning will make situation worse in which difficulty in handling during the fabrication will be a disadvantage for this modification.

On the other hand, finger dependent parasitic capacitances can be reduced by reducing finger area, increasing separation between finger and underlying conductive material and reducing passivation layer thickness that are depended to fabrication possibilities[52,53]. But, in general, the pad-to-pad capacitance plays dominant role in total parasitic capacitance of the diode. In the next chapter, we will introduce a new approach in which device performance can be enhanced significantly without suffering from any of these difficulties.

2.2.3 **Parasitic resistances**

In the previous chapter we have explained different components of the total resistance of the diode in a typical vertical design. For a planar structure, there are four main elements constituting the series resistance which can be expressed by (1):

$$R_S = R_{Spreading} + R_{Contact} + R_{epi} + R_f \quad (2.15)$$

As it can be clearly seen in Figure 2.5, these elements are the same as that of a vertical structure and in addition a new component is also added which is finger resistance (R_f). Although these parameters are also geometry dependent, the estimation of these elements is more complicated compared to vertical structure mainly due to high frequency-induced power losses.

Lateral current flow in the planar structure together with partially closed loop junction in which just a portion of current will be collected with the ohmic contact and the rest of the power will be lost as a result of high frequency power loss phenomena. Also moving toward to higher frequencies, dimensions of the diode are scaled down and this reduction in the area can increase the amount of some of these resistances such as R_f and $R_{Contact}$.

But the most important portion of these losses is due to high frequency induced power losses which were negligible at lower frequency. High frequency current crowding phenomena such as eddy current and current crowding due to skin and proximity effects will add a new loss for lateral current flow in the buffer and this loss is mainly dissipated as heat inducing a substantial increase in the amount of spreading resistance.

Recently, it was investigated that the magnetic field couplings induced by the time-varying current in the air-bridge finger leads to the findings which links the high-frequency losses to the eddy current, and a mixture of skin and proximity effects. According to the Faraday's law, AC voltage induced in a conductor is a result of time-varying magnetic field. The induced voltage then forces eddy current to circulate in a closed path within the conductor. According to Lenz's law, this induced modification in current flow which is called eddy current, generates its own magnetic field to oppose the original magnetic field. The circulation of eddy current results in a non-uniform current density distribution (current crowding) and consequently will increase power loss associated with current flow. The power loss due to eddy current is proportional to the square of frequency as explained in:

$$P_{loss}^{eddy} \ \alpha \ f^2 \tag{2.15}$$

On the other hand, this eddy current by itself results in two loss effects, the skin and proximity effects. Skin effect occurs when eddy current is induced in a conductor (like buffer mesa in our case), which is subjected to a time-varying magnetic field originating from the current flowing in the conductor itself. On the contrary, proximity effect occurs when the eddy current is induced in a conductor due to a time-varying magnetic field originating from an adjacent conductor, e.g., the generation of eddy current in the buffer mesa due to a time-varying magnetic field originated from the air-bridge finger. The frequency dependency of the power loss due to skin effect is:

$$P_{loss}^{skin} \ \alpha \ \sqrt{f} \tag{2.16}$$

Moreover, it is found that power coupling between these two mechanisms will make higher orders of power losses such as f^4 in which these components start to be important moving to higher frequencies[54].

2.2.4 **Effect of parasitic elements in diode performance**

The performance of all THz components made by Schottky diode such as mixers and multipliers strongly depends on the diode device properties. Therefore, it is crucial to identify the figures of merit and possible diode parameters to be optimized. Although several figures of merit can be defined for evaluation of diode performance such as temperature noise, conversion loss (in mixers), in this thesis we didn't focus on temperature dependent issues and we focused on switching speed of the diode. Therefore, the diode performance is evaluated by comparing the cut-off frequencies.

The diode cut-off frequency, f_c, is a figure of merit describing the upper limit of the diode frequency response which means how fast your diode can move between on and off states. This feature is inversely proportional to parasitic elements such series resistance and parasitic capacitance. The diode cut-off frequency is calculated as:

$$f_C = \frac{1}{2\pi R_S C_P} \tag{2.17}$$

This estimated amount should be about 10 times higher than working frequency of the mixer to guaranty the safe performance of the design. In upcoming sections we will show that by some modifications in the diode design, the cut-off frequency can be shifted up considerably.

Taking all into consideration, a 3D EM-based numerical modeling approach is required to provide an accurate estimation of these parasitic elements.

Chapter 3

Modeling and Analysis Methodology

In order to have a better understanding of the effect of different geometries on parasitic elements and losses, a systematic modeling and analysis approach is required. In this approach, the Schottky diode structure is simulated in Ansoft High Frequency Structure Simulator (HFSS) and results of this electromagnetic simulation is used for lumped equivalent circuit extraction in Microwave Office environment. So for the first step, a practical equivalent circuit should be defined. Although, the parasitic elements are actually more complex than a simple circuit and furthermore they are distributed, introduction of an equivalent circuit can be a starting point to estimate device performance. This section describes this modeling approach in detail.

3.1 Electromagnetic-based Diode Analysis

Figure 3.1 shows the schematic of the diode structure used for 3D full wave EM simulation. As it can be clearly seen, the discrete planar Schottky diode is attached on a finite ground coplanar waveguide (CPW). This 50 Ω CPW on a GaAs substrate (ε_r = 12.9) is designed with a 30-µm-wide signal line and a gap of 21 µm. The Schottky diode is monolithically integrated along the signal line of the CPW. In this setup, the simulation

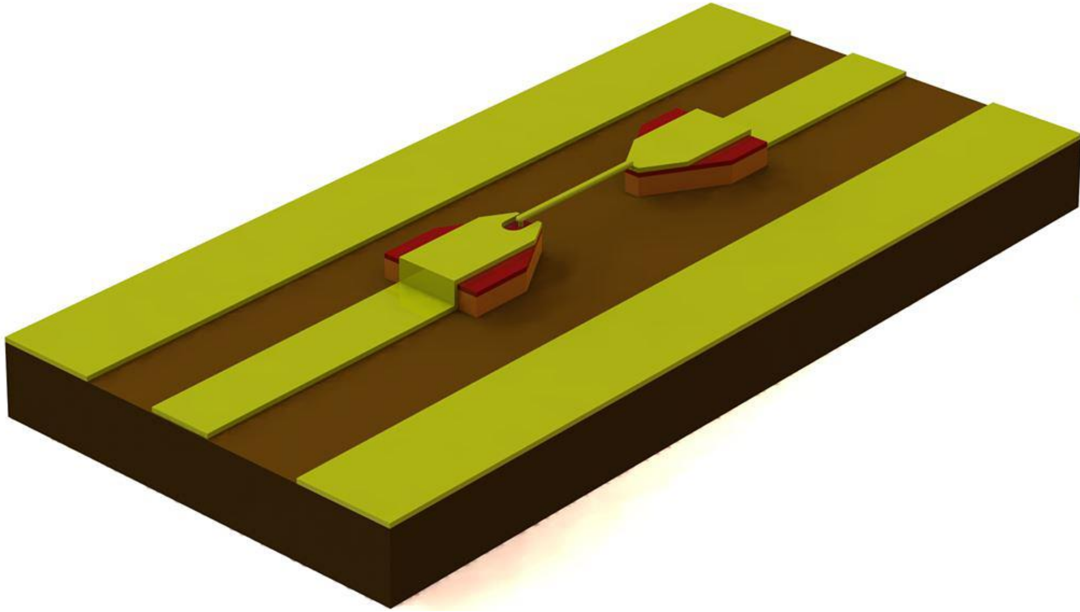

Figure 3.1: Configuration of proposed planar Schottky diode attached to CPW line.

is performed by feeding the CPW line from the both ends with two lump ports. The EM waves are alternately excited from both anode and cathode lumped ports. The length of the CPW feeding line is designated in a way that it ensures all evanescent waves created in the vicinity of the feeding point is decayed before reaching to the diode position (the length of the line is 500 μm which is longer than the half-wavelength of a wave propagating at frequencies higher than 300 GHz).

All structures are simulated with the HFSS through the proposed simulation setup. Afterward, the EM simulation results, scattering parameters (S-parameters), are de-embedded from both ends of the diode to reference planes of the surface channel. De-embedding is done by using COST (Cascaded Open-circuit, Short-circuit, Thru) method[55] as it shown in the Figure 3.2. At the end a MATLAB code is utilized to obtain de-embedded S-parameters (MATLAB code is provided in the appendix).

In our analysis, in total 3 different cases have been simulated;

1) lossless open-circuit
2) lossless short-circuit
3) lossy (cathode mesa) short-circuit.

For both lossless cases, all of the conductors including air-bridge finger, ohmic-contact mesas, and both anode and cathode buffer, are assumed to be perfect electric conductor

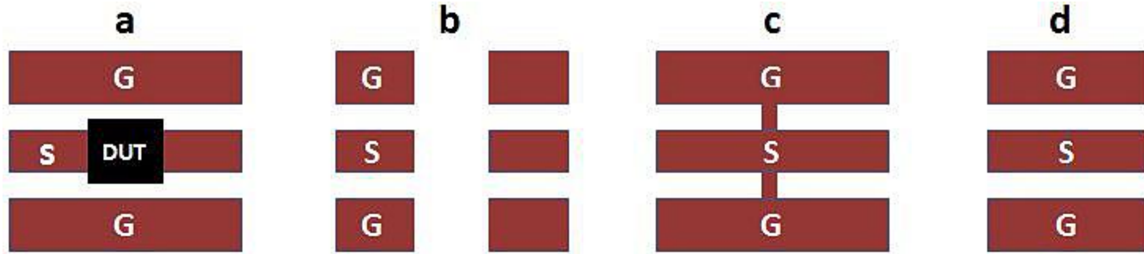

Figure 3.2: COST de-embedding method cases: a) device under test b) open, c) short and d) Thru cases for the fabricated structure.

(PEC) in the simulation setup analysis. In addition, for the lossy case, conductive losses inside the cathode buffer mesa is also added to our design and simulated through EM simulation software. Also, open case means there is no contact between finger and buffer layer and in short case finger and buffer layer are short-circuited. These cases will be shown in more details in next sections.

3.1 Equivalent Lumped Circuit Model

The equivalent lumped circuit model for the discrete planar Schottky diode device is shown in Figure 3.3. As it can be clearly seen, this circuit comprises over three main parts; ohmic cathode, diode structure and ohmic anode. Both cathode and anode are modeled with resistive, inductive and capacitive elements as it is shown in the figure. For the diode, there are two capacitors to model the coupling inside the device (the origin of these capacitors and their contribution in device performance is discussed in detail in previous chapter). L_f is also used to model the magnetic coupling within the air-bridge finger through current displacement inside the diode. The resistor R_s is also used to model the resistive losses through the current flow inside the diode. It should be noted that in this modeling approach the part of ohmic losses is neglected (because all of the contacts are selected to be PEC). But considering the fact that the amount of this resistor is much lower than other components like spreading resistance, the estimation of resistive losses is still valid and accurate. The diode is also modeled to be an ideal switch. In reality the diode junction is considered to be a RC circuit in which these elements are in

parallel arrangement. But taking it into account that our modeling is an EM-based model and also the amount of junction elements depend on geometries and how good is the diode fabrication, in our modeling approach there is no contribution for junction capacitance and resistance.

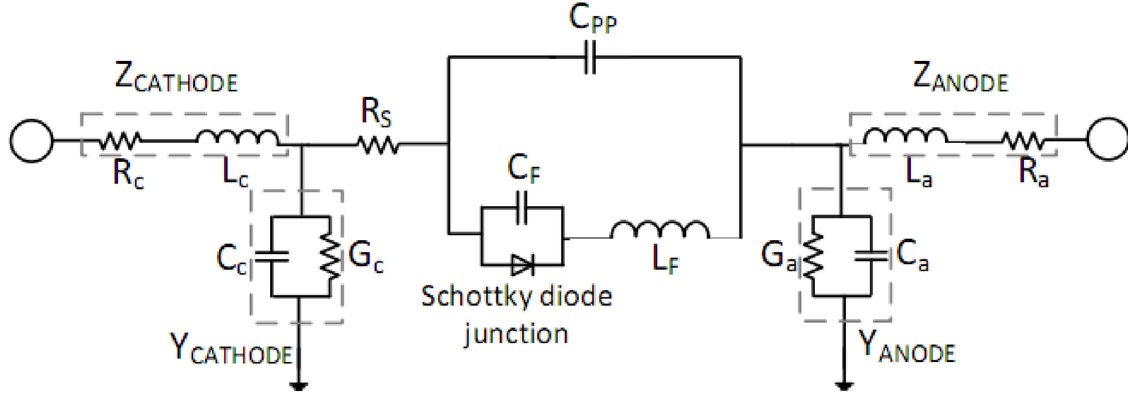

Figure 3. 3: Lumped equivalent circuit for our Schottky diode.

3.3 Geometry-dependent parasitic elements extraction

After providing an EM-based analysis approach and equivalent lumped circuit model for our structure, the all parasitic components are extracted through a fine-tuning method using Microwave Office software. This tuning is carried out for each single frequency utilizing least square error fitting.

To extract all parameters first, the EM simulations are done. These simulations are for 3 different cases as explained in previous sections. In the lossless case, as it is implied, there is no loss in current flow. Therefore, on the de-embedded S-parameter results, there are just C_{pp}, C_f and L_f contributions. Considering the range of inductances (pH) and capacitances (fF), the series combination of LC circuit can be simplified to a simple capacitor. Hence, the outcome of case study is the total amount of C_{pp} and C_f. In the second case, the diode is short-circuited and the buffer layer is lossless. So, C_f will be short and its contribution won't be considered. The overall circuit will have two components; L_f and C_{pp}. Using the results obtained from the first case, the amount of L_f can be estimated. Finally for the last case, the diode is short-circuited and lossy. The n^+ buffer layer is assumed to be doped with an electron concentration of 5×10^{18} cm^{-3} instead of using PEC which was the case in lossless setups. In this step, the amount of R_s can be

found through using previous amounts. Figure 3.4 indicate both open and short cases including their EM simulation setups.

Figure 3.4: EM simulation setup for open-circuit and short-circuit cases of diode.

Using "π" network model, we can estimate the amount of each of these parasitic elements by utilizing the equations (1-3);

$$C_P = C_{PP} + C_f = \left\{\frac{1}{\omega}\frac{[\text{image}(-Y_{12})]^2 + [\text{real}(-Y_{12})]^2}{\text{image}(-Y_{12})}\right\}_{\text{open-lossless}} \tag{1}$$

$$L_{tot} = L_f + L_a + L_c = \left\{\frac{1}{\omega}\frac{[\text{image}(Y_{12})]}{[\text{image}(Y_{12})]^2 + [\text{real }(Y_{12})]^2}\right\}_{\text{short-lossless}} \tag{2}$$

$$R_S = \left\{\frac{1}{\omega}\frac{[\text{real}(Y_{12})]}{[\text{image}(Y_{12})]^2 + [\text{real }(Y_{12})]^2}\right\}_{\text{short-lossy}} - \left\{\frac{[\text{real}(Y_{12})]}{[\text{image}(Y_{12})]^2 + [\text{real }(Y_{12})]^2}\right\}_{\text{short-lossless}} \tag{3}$$

These starting values for C_p, L_{tot} and R_s are used to fine-tune the equivalent circuit in Microwave Office for the whole frequency range (150 GHz – 600 GHz). This way, accurate values for each equivalent circuit parameter (C_{pp}, C_f, L_f, L_a, L_c and R_s) are extracted. The extraction is done by fine-tuning strategy in which all of these data is used to extract parasitic parameters at every frequency throughout the whole frequency range.

In the next chapter, we provide a comprehensive study about the effects of different geometry-dependent elements on each parasitic component.

Chapter 4

Results and Discussions

This chapter provides a comprehensive systematic study on the impact of geometry parameters on diode performance using the presented modeling methodology. Based on the simulation results, a performance-enhanced Schottky diode structure will be proposed at the end of this chapter. Initial dimensions for our simulations have been shown in Figure 3.1.

4.1 Geometrical optimization of the diode

To improve device performance, the impact of parasitic elements on the device degradation should be reduced. In this section, we will show that how different geometries can degrade device performance.

4.1.1 Parasitic Capacitances

According to Figure 2.5, total parasitic capacitance (C_p) can be divided into two parts; pad-to-pad capacitance C_{pp} (including C_{pp1} and C_{pp2}) and finger capacitance C_f (including finger-to-pad C_{fp} and finger-to-buffer C_{fb}). As it can be seen from Figure 4.1, contribution from the pad-to-pad capacitance is dominant (especially in higher frequencies).

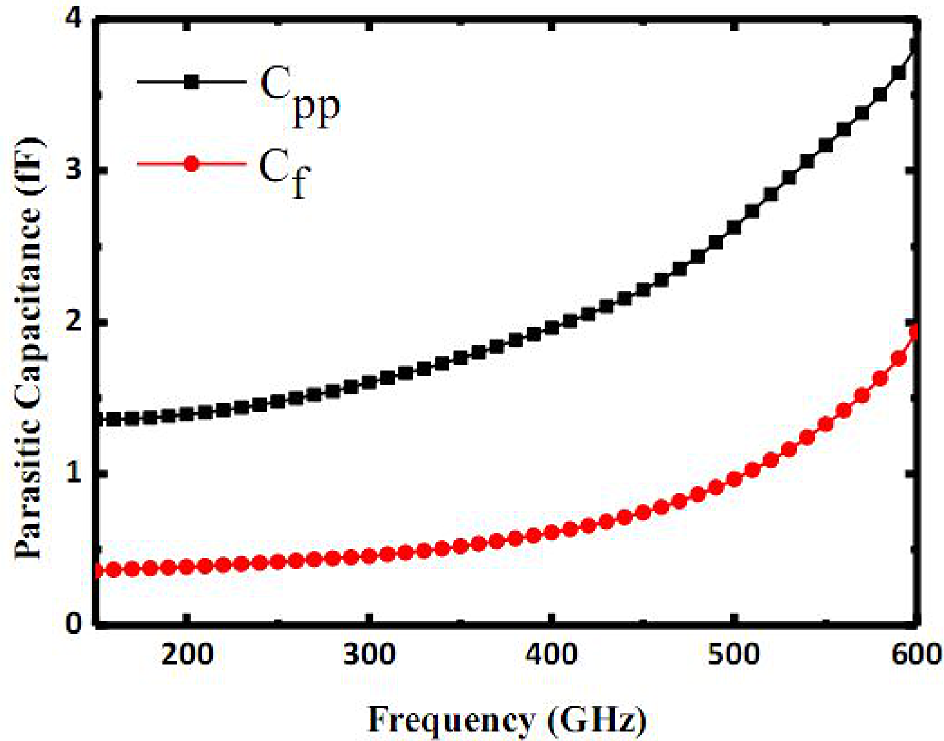

Figure 4.1: Pad-to-pad and finger capacitances as a function of frequency for substrate thickness of 15 µm.

Therefore, it is desirable to minimize C_{pp} which can be decreased by reducing pad area, increasing pad separation, decreasing substrate dielectric constant and substrate thickness. However, pad dimensions are limited by considerations of handling and bonding by ohmic contact resistivity[52]. Also, large pad spacing, in addition to increasing footprint, leads to excessive inductance that is not desirable[44]. Thus the most effective solution for decreasing pad-to-pad capacitance is to reduce the substrate thickness. Figure 4.2 plots C_p for different substrate thicknesses.

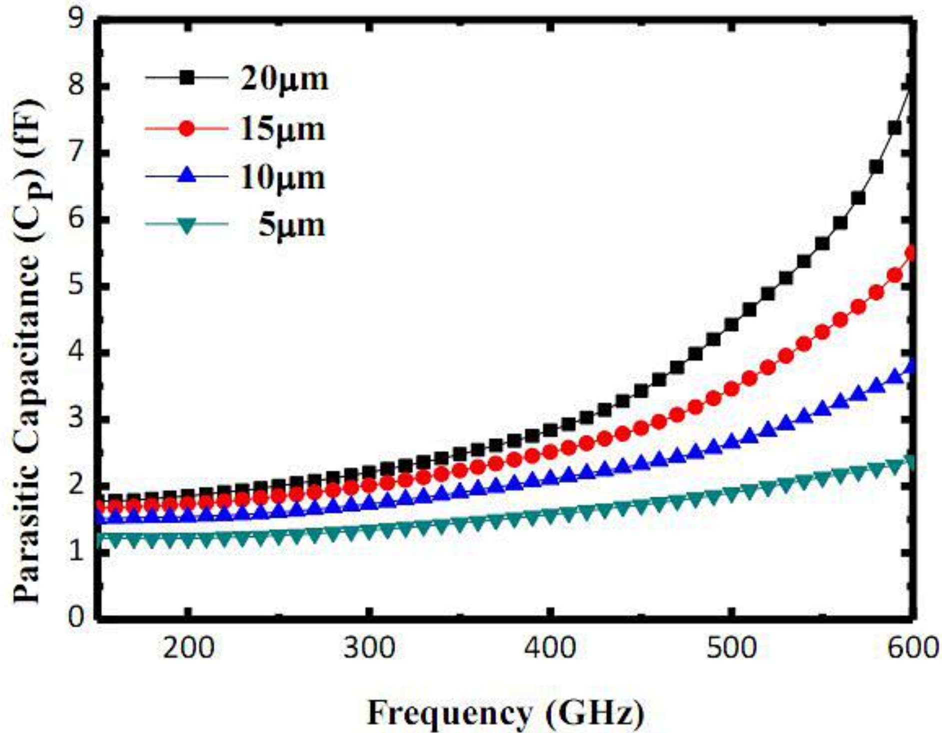

Figure 4.2: Effect of substrate thickness on parasitic capacitance. By increasing substrate thickness, capacitance increases significantly, especially at higher frequencies.

According to these results, by increasing substrate thickness, capacitance increases significantly, especially at higher frequencies. In all of the parametric studies, substrate thickness is fixed at 15 μm. Also it should be noted that finger capacitance also can be reduced by reducing finger area, increasing separation between finger and underlying conductive material and reducing passivation layer thickness that depended on fabrication possibilities.

4.1.2 **Parasitic Resistances**

As explained before, parasitic resistances are comprised of 4 main parts in which the spreading resistance is the dominant one. For finger and contact resistances, we can decrease their contribution in total losses with some simple methods. Reducing the finger length, increasing the contact and finger areas and utilizing low loss highly conductive metals are practical approaches to mitigate the resistive losses. But all of these modifications are subject to fabrication possibility and feasibility. Therefore, the only geometry dependent factor that can degrade Schottky diode performance is spreading

resistance ($R_{Spreading}$). The finite conductance of the buffer layer results in current crowding and only a portion of total current can be collected at the ohmic contact. This loss is modeled by a resistor, $R_{Spreading}$, in the equivalent circuit model. The only geometric parameter that affects spreading resistance is the buffer layer thickness.

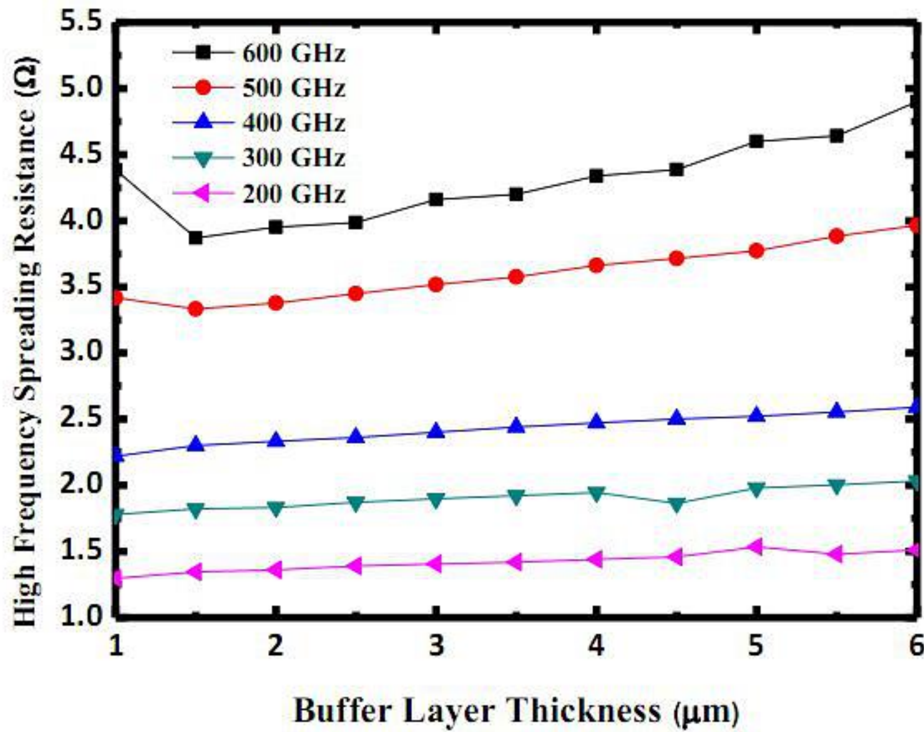

Figure 4.3: The high frequency spreading resistance as a function of buffer layer thickness.

Figure 4.3 plots spreading resistance values at different frequencies for different buffer layer thicknesses. As it is observed in[56], high frequency spreading resistance exhibits a weak minimum at buffer layer thicknesses close to skin depth (that in this case it is approximately 1.7 µm at 600 GHz).

Taking all of these results into consideration, it can be clearly seen that using this method we can provide a design in which all geometrical parameters are optimized. Therefore, this modeling approach is an efficient tool to optimize the overall device performance while considering fabrication limitations. Together with this, one can use this modeling to create some innovative designs in which the device structure can be adjusted in a way that parasitic elements will be minimized without using complicated and expensive fabrication processes.

4.2 *Performance Enhanced Schottky Diode*

In this part, a performance enhanced Schottky diode is proposed. C_{pp}, the dominant shunt capacitance contribution to total parasitic capacitance, is composed of two parts: the shunt capacitance between the pads distributed across a low permittivity region (air), C_{pp1} and a high permittivity (GaAs) substrate, C_{pp2}. In addition to introducing a higher capacitance due to higher permittivity of the substrate ($C_{pp2} > C_{pp1}$), C_{pp2} has greater frequency dependency and increases considerably with frequency. The parasitic capacitance can be reduced significantly by introducing a deep-trench in the substrate between the two electrical contact pads. Figure 4.4 shows the device structure for the proposed design. The deep-trench is etched through the semi-insulating substrate with different depths. For an etch depth equal to the substrate thickness, total parasitic capacitance (C_p) is minimized to less than 2 fF and relatively independent of the operation frequency, as depicted in Figure 4.5. This means that if the substrate between two pads is etched, the contribution of the pad-to-pad capacitance will be minimized and total capacitance will be mainly finger capacitance. Therefore, using such a simple etching technique, we can minimize the capacitive parasitic elements of our design.

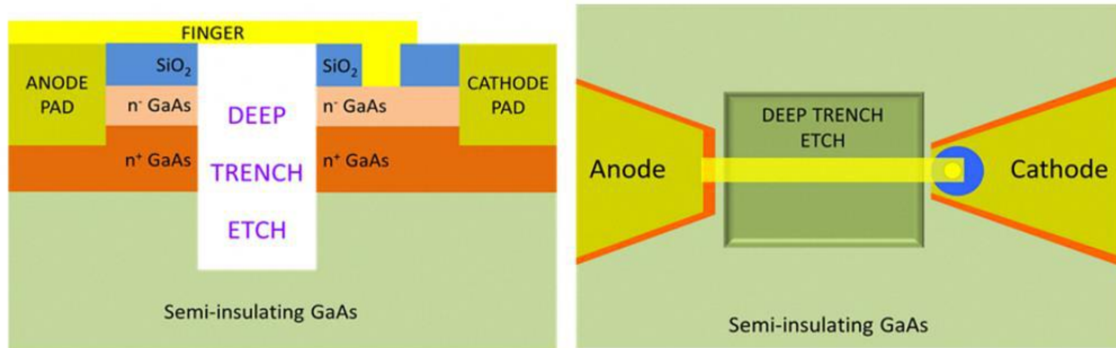

Figure 4.4: A schematic of cross sectional (a) and top view (b) of proposed surface-channel planar Schottky diode.

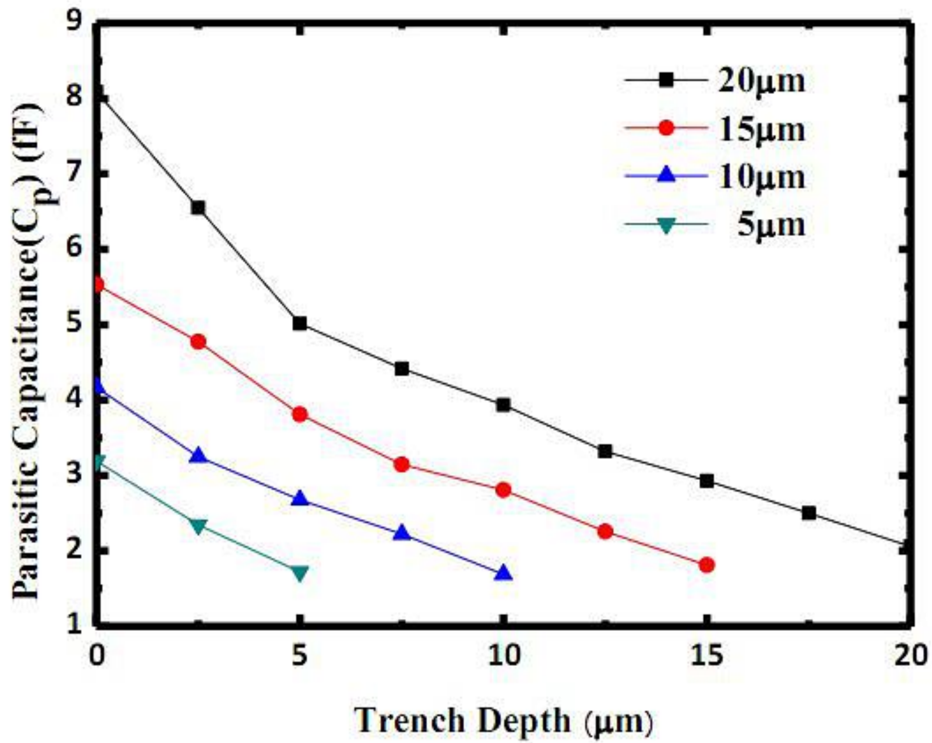

Figure 4.5: Effect of trench depth on reduction of parasitic capacitance for different substrate thicknesses

Another parameter that limits planar Schottky diode performance is the spreading resistance. In order to reduce $R_{Spreading}$, a closed-loop junction is proposed to collect radial current in all directions. Figure 4.6 compares the results for conventional and closed-loop junctions. As it can be clearly seen, in the whole frequency range the spreading resistance is reduced by a factor of ca 2.

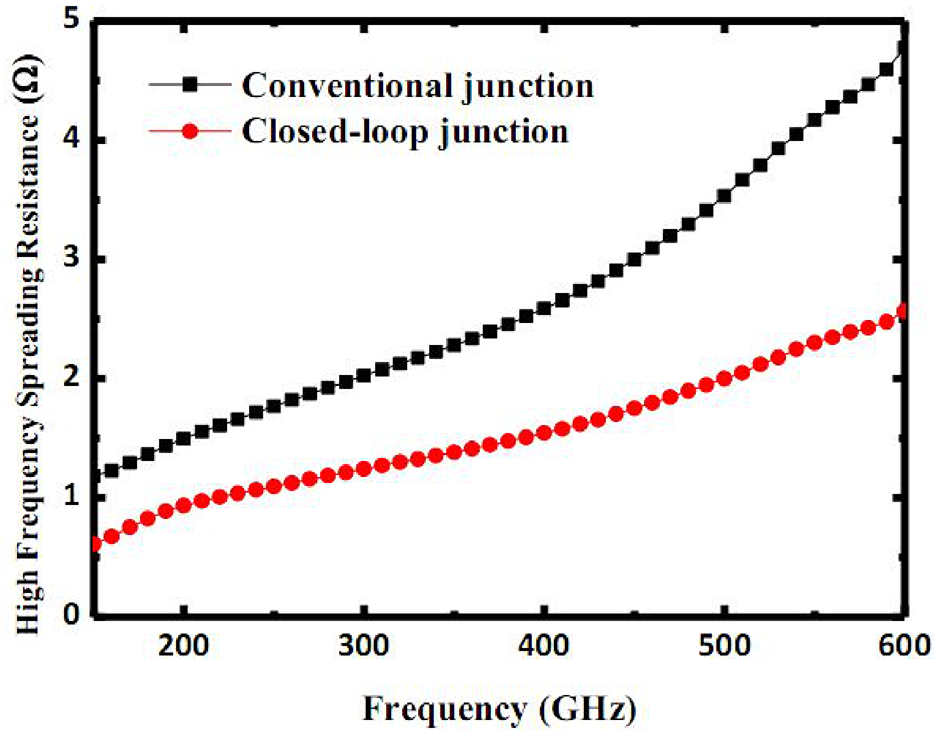

Figure 4.6: Effect of closed loop junction on reduction of high frequency spreading resistance. The spreading resistance is reduced by a factor of around two with the use of a closed loop junction.

Validity of such a modeling approach and obtained results is verified with reference[57]. By taking the value of the zero-bias junction capacitance (2.5 fF) from an earlier report of a fabricated planar Schottky diode structure[58], we can estimate the cut-off frequency of the conventional and performance enhanced Schottky diodes. Assuming a 15-μm-thick substrate and an operation frequency of 600 GHz, the cut-off frequency of the conventional structure is found to be 4.1 THz while that of the improved structure is 14.1 THz.

5 Device Fabrication

This chapter provides information on fabrication process of the diode structure. It will be shown that the fabrication of the diode is not a straightforward task and requires several optimizations on the etching process. Although our fabrication was not successful, the challenges and solutions for future runs have been provided in this chapter.

5.1 Fabrication process

This chapter describes the fabrication process of planar Schottky diode. All steps are conducted in UNAM Cleanroom Facilities (UCF) (class 100 and 1000) and Okyay Group Laboratories in UNAM at Bilkent University. The device fabrication consists of 6 main steps: i) deposition, patterning and etching of passivation layer, ii) patterning and etching of low-doped buffer layer, iii) formation of ohmic contacts, iv) patterning and etching of highly-doped buffer layer, v) formation of CPW lines and finger and vi) formation of deep-trench. Figure 5.1 explains all of these fabrication steps schematically. In this section, we will explain all steps in detail.

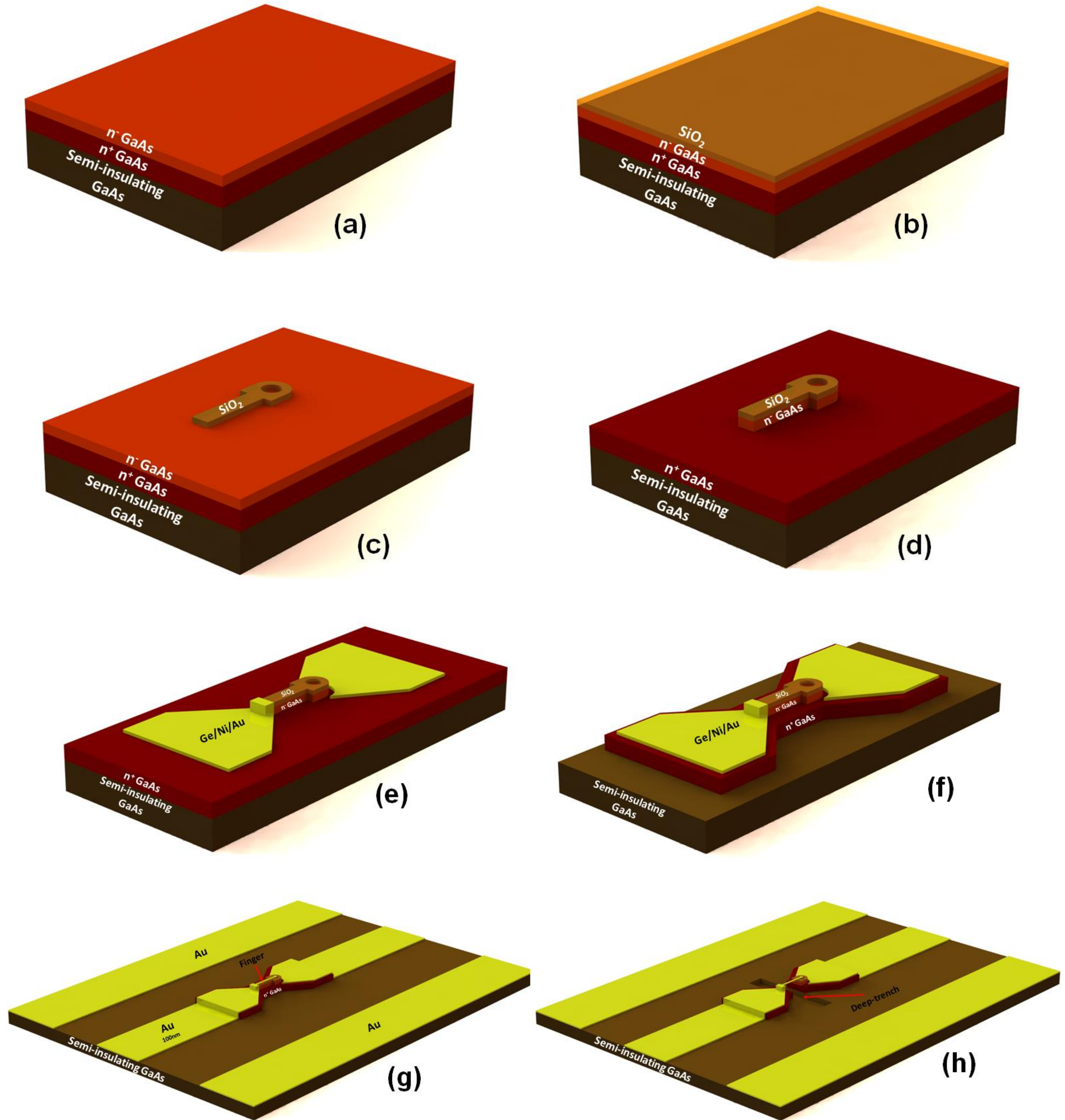

Figure 5.1: Fabrication steps of proposed planar Schottky diode. a) Initial epitaxial substrate, b) deposition of SiO2 layer, c) patterning and etching of the SiO2 layer, d) patterning and etching of n- layer, e) ohmic contact formation, f) patterning and etching of n+ layer, g) CPW and finger lines formation, h) deep-trench formation.

A. Deposition, patterning and etching of passivation layer

SiO_2 is used as passivation layer in our device. Before deposition of this passivation layer, dip HF step is carried out for the sample for duration of 30 sec. The initial substrate is a epitaxial GaAs layer which comprises over 3 layers: i) 500 μm-thick semi-insulating, ii) 4 μm-thick n^+, and iii) 250 nm-thick n^- layers. After dip HF, deposition of 200-nm-thick SiO_2 layer is deposited using VAKSIS CVD-Handy Plasma Enhanced Chemical Vapor Deposition (PECVD) system. The deposition is performed at 250 °C with a chamber pressure of 1 torr and RF power of 10 W. N_2O and SiH_4 are used as precursors with flow rates of 15 sccm and 6 sccm, respectively. As carrier gas, He is used with 700 sccm flow rate. See Figure 5.1 (b).

The active device area is patterned by photolithography and wet oxide etching. Initially, to improve adhesion of the photoresist, HMDS (hexamethyldisilazane) is spin coated at 4000 rpm for 40 seconds. AZ5214E is spin coated at 4000 rpm for 40 seconds; which resulted in 1.4-μm-thick photoresist layer. The samples are prebaked at 110 ºC for 60 seconds and exposed to UV light. Then, UV exposed regions are developed using AZ400K:H_2O (1:4) solution for 30 seconds. In order to improve the chemical stability of the photoresist layer, the samples are hard-baked at 120 ºC for 2 minutes. After defining active regions, the SiO_2 layer in these regions is etched using BOE for 10 minutes. Sample is rinsed with DI water and remaining photoresist is removed by sonicating in acetone (as shown in Figure 5.1 (c)).

B. Patterning and etching of low-doped buffer layer

Before the ohmic contact formation, the n^- layer is etched away through the wet etching process. For this aim, two different solutions are used: i) H_2SO_4:H_2O_2:H_2O (1:1:20) and ii) NH_4OH:H_2O_2:H_2O (8:3:30). After an optimization process we found that the later one has more anisotropic profile compared to the earlier. Considering our process in which we need to do etching process for a long period of time, we chose the second solution for our case. The etching rate was about 5nm/sec. Figure 5.1 (d) shows an illustrating image from the output of this step.

C. Formation of ohmic contacts

As ohmic contacts, an alloy of 3 different metals is used. Contact pads are formed using the following lift-off procedure. Initially, the contact regions are defined by photolithography. Then, Ge/Ni/Au (10nm/10nm/100nm) is evaporated using VAKSIS PVD Vapor 3S Thermal Evaporator without breaking the vacum level of 7×10^{-6} Torr through a deposition rate of 0.8 Å/sec. Afterward, the samples are sonicated in acetone to complete the lift-off process (See for the schematic of Figure 5.1 (e)). The samples are rinsed in isopropanol, DI water and dried with N_2 gun. Finally, anealing at 450 ˚C with rapid thermal anealing (RTA) was utilized for 45sec.

D. Patterning and etching of highly-doped buffer layer

Prior to CPW line formation, the highly doped layer should be etched away to avoid short-circuit problem in our device. Therefore, as shown in Figure 5.1 (f), the n^+ layer is etched from everwhere apart from beneath of the ohmic contact. Etching of this layer was performed by a wet etching process by NH_4OH:H_2O_2:H_2O (8:2.5:30). Because the thickness of the layer is 4 µm, the etching duration is too much (taking rate of deposition as 5nm/sec). Therefore, this step is a critical part of the fabrication in which the undercuts can destroy the contacts. In upcoming section we will see this problem.

E. Formation of CPW lines and finger

After etching the n^+ layer, the CPW line formation was carried out at the same time with finger deposition. For this step, the deposition was performed in the same condition with step B for a 100 nm-thick Au layer. After that the sample is sonicated in acetone to complete the lift-off process. Figure 5.1 (g) indicates the output of this step.

F. Formation of deep-trench

The most challenging part of the fabrication is formation of this trench. This step was done through wet etching. For this step, first, a window was opened between two pads through patterning of the structure. Afterwards, sample was immersed in BOE for 2 min

to remove the SiO_2 layer under the finger. Then sample was immersed at $NH_4OH:H_2O_2:H_2O$ (8:2.5:30) for a duration of 30 min to make the trench. The outcome of this step is supposed to be like Figure 5.1 (h). This step is the most challenging part of diode fabrication and requires a lot of optimizations on the etching process.

5.2 Critical steps in diode fabrication

The fabrication of planar surface channel Schottky diode is a challenging process in which several parameters should be optimized to provide a working device. We have fabricated our device on 3 different samples: i) Silicon, ii) thin epitaxial GaAs n^+/n^- (600nm / 400nm) and iii) thick epitaxial GaAs n^+/n^- (4µm / 250nm). Figure 5.2 shows all devices fabricated on these substrates.

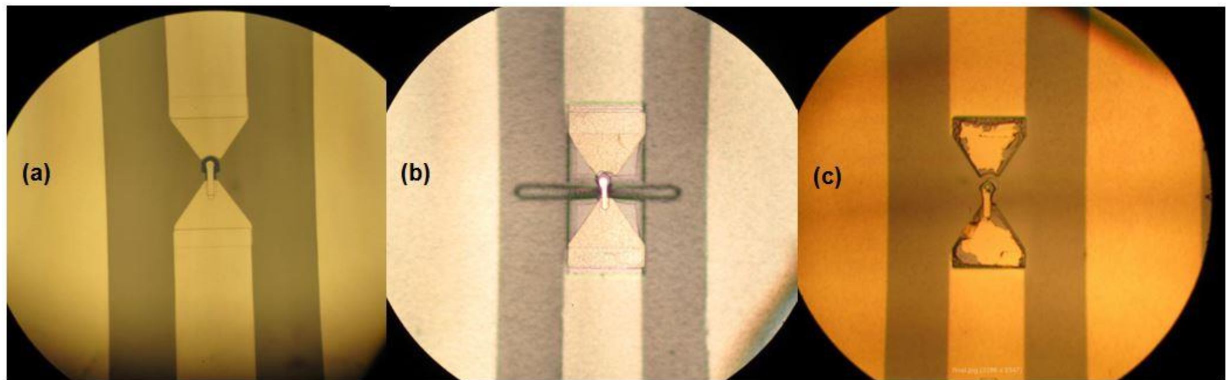

Figure 5.2: Fabricated prototype of the Schottky diode on different substrates: a) Silicon, b) thin epitaxial GaAs and c) thick epitaxial GaAs layer.

As we can see, the device fabrication on Si was totally successful. The same thing was also shown in thin GaAs case. But for thick layer of epitaxial GaAs substrate, we have several discontinuities on the final device, especially around the ohmic contacts. To scrutinize the reasons for this failure, we should go back to previous steps. Figure 5.3 shows one of these challenges. As we can see, for the thin epitaxial layer substrate, the mesa walls are distinguishable which means the undercut problem is not significant. But, for the thicker one, the undercuts have gone till under the contacts. This can be easily seen from wrinkles on the contact in which the supporting substrate beneath the ohmic

contacts has been etched away. Therefore, this can lead to discontinuity in the final device.

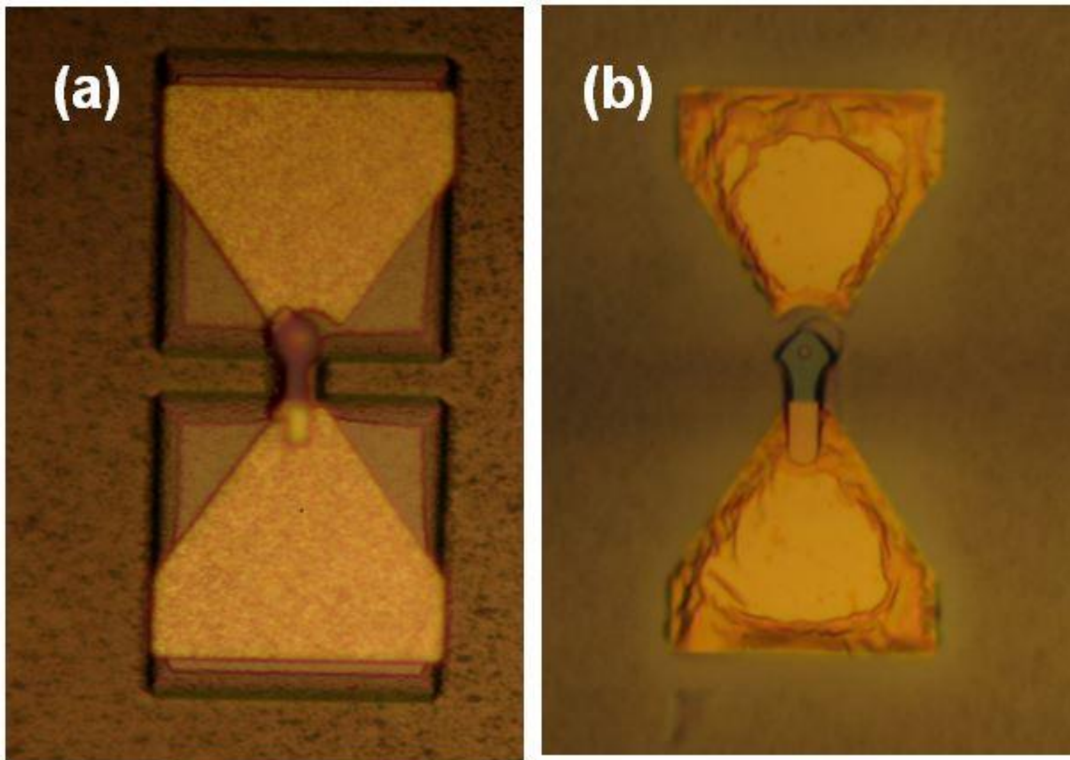

Figure 5.3: Formation of ohmic contacts on a) thin epitaxial GaAs and b) thick epitaxial GaAs layer.

To sum up, fabrication of the Schottky diode is a challenging process which requires several optimizations on each step. The duration of the etching and the etching profile for such a long-time etching process is an imperative task.

Chapter 6

Conclusions

In this thesis, the planar surface channel Schottky diodes have been studied and a systematic modeling approach was introduced to investigate the impact of different geometries on parasitic elements of the diode. The work has involved a step by step explanation of the modeling methodology together with scrutinizing the obtained results. The main scientific contribution of this work is development of a new and accurate modeling approach which is a hybrid of EM-based and circuit analysis. This approach can be extended to analysis of all integrated planar devices where high frequency cross talk noise is detrimental.

Getting insight on the effect of different geometrical parameters on parasitic capacitances and resistances, we demonstrate a performance-enhanced planar Schottky diode for THz applications using a hybrid electromagnetic and circuit modeling approach. For this aim, first, a parametric study is carried out to investigate the relationship between the physical parameters of the diode and parasitic elements which limit the device cut-off frequency. Afterwards, a performance-enhanced Schottky design was proposed. The improved design features a deep-trench in the substrate between electrical pads and a closed-loop junction which reduces the parasitic capacitance and series resistance, respectively. As a

result, cut-off frequency is estimated to increase from 4.1 THz to 14.1 THz for the improved Schottky diode design. The methodology presented here, provides a good estimate of diode impedance which might be used to design monolithically integrated detectors where THz antenna impedance is conjugately-matched to the Schottky diode impedance to increase detector sensitivity.

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