ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

HIGH SPEED DATA ACQUISITION TECHNIQUES for PIPELINED ANALOG to DIGITAL CONVERTERS in IHP SiGe BiCMOS 0.13 μm

Ph.D. THESIS

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Thesis Advisor: Assoc. Prof. Dr. Tufan Coşkun KARALAR

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ LİSANSÜSTÜ EĞİTİM ENSTİTÜSÜ

IHP SiGe BiCMOS 0.13 μm'de BORU HATTI ANALOGDAN DİJİTALE ÇEVİRİCİLER İÇİN YÜKSEK HIZLI VERİ ELDE ETME TEKNİKLERİ

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NİSAN 2024

Hakan ÇETİNKAYA, a Ph.D. student of ITU Graduate School ID of 504162210, successfully defended the thesis entitled "HIGH SPEED DATA ACQUISITION TECHNIQUES for PIPELINED ANALOG to DIGITAL CONVERTERS in IHP SiGe BiCMOS 0.13 μm", which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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Date of Submission : **5 February 2024**
Date of Defense : **29 April 2024**

To my dear and kind parents, brother and my lovely wife,

FOREWORD

Foremost, I would like to thank to my supervisor Assoc. Prof. Dr. Tufan Coşkun KARALAR for all of his support and guidance during my Ph.D. study and thesis.

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I would also like to express my gratitude to my family for their continuous support through all of my life.

This thesis is an extension of the Elsevier Microelectronics Journal in [1] which was published in September 2023. The conference paper in [2], of which I am the first author, was published in IEEE ELECO 2019. It became an academic reference for this Ph.D. dissertation.

Moreover, according to the decision of the Senate, publications produced from this thesis can only be used for one student's graduation. Turnitin check for the thesis results as 19% similarity rate.

APRIL 2024

Hakan ÇETİNKAYA
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ABBREVIATIONS

ADC : Analog-to-Digital Converter
BALUN : Balance Unbalance
BER : Bit Error Rate
BGR : Band-gap Reference
BiCMOS : Bipolar Complementary Metal Oxide Semiconductor
CMFB : Common-Mode Feedback
DAC : Digital-to-Analog Converter
DNL : Differential Non-Linearity
DNW : Deep N-well
DR : Dynamic Range
DSP : Digital Signal Processing
DWBF : Double-well body floating
EA : Error Amplifier
ENOB : Effective Number Of Bits
FR4 : Flame Retardant Level 4
FS : Full Scale
IC : Integrated Circuit
IF : Intermediate Frequency
INL : Integral Non-Linearity
ISI : Inter-symbol Interference
JTF : Jitter Transfer Function
LDO : Low Drop-out
LSB : Least Significant Bit
MDAC : Multiplying DAC
MSB : Most Significant Bit
PLL : Phase Locked Loop
PNOISE : Periodic Noise
PSRR : Power Supply Rejection Ratio
PSS : Periodic Steady State
PSUB : P-substrate
PVT : Process Voltage Temperature
PW : P-well
RF : Radio Frequency
RMS : Root Mean Square
RX : Receiver
SC : Switched Capacitor
SHA : Sample and Hold Amplifier
SHA-less : Sample and Hold Amplifier-less
S/H : Sample and Hold
SFDR : Spurious Free Dynamic Range
SiGe : Silicon Germanium
SINAD : Signal-to-noise and Distortion ratio

SNDR : Signal-to-Noise-and-Distortion Ratio
SNR : Signal-to-Noise-Ratio
THD : Total Harmonic Distortion
TW : Triple-well
TL : Transmission Line

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HIGH SPEED DATA ACQUISITION TECHNIQUES for PIPELINED ANALOG to DIGITAL CONVERTERS in IHP SiGe BiCMOS 0.13 μm

SUMMARY

The resolution of the analog-to-digital converter market may be categorized into 8-b, 10-b, 12-b, 14-b, 16-b, and other options. The incorporation of several resolutions arises from the demands of different applications. In 2018, the 12-b resolution lead the market for analog-to-digital converters. The 16-b type is expected to overtake and become the dominant force in the future. The use of 12-b for 5G connectivity presents a favorable opportunity for market expansion.

Texas Instruments unveiled a groundbreaking ADC in May 2019, boasting the industry's largest bandwidth, lowest power consumption, and fastest sampling rate. This converter is anticipated to assist engineers in attaining optimal measurement precision for 5G testing, oscilloscopes, and direct X-band sampling in radar applications.

In this work, a one way 11-b pipeline ADC, designed in a SiGe BiCMOS 0.13 μm, is presented. It has sampling frequencies up to 1.6 GS/s and can provide above 8-b ENOB for the low input signal frequency and 6.4-b ENOB for the highest input frequency of 799 MHz according to the simulation results obtained without calibration. For our ADC, sample-and-hold amplifier-less (SHA-less) architecture was preferred since the SHA was one of the most power-consuming sub-blocks, and brought inevitable noise and distortion. A composite ADC architecture, having 8x 1.5-b cascaded stages and a back-end 3-b flash ADC is designed to reach up to 11-b physical resolution. A novel MDAC is proposed to mitigate ISI. Moreover, a novel BiCMOS residue amplifier (RA), which performs 6.43 GHz UGB and 80 dB DC gain, is implemented. A non-overlapping clock generation architecture at 1.6 GHz is devised, incorporating a differential clock driver and clock level converters.The SNR_{jitter} of the clock generation system is 57 dBc at a clock signal frequency of 1.6 GHz. The results of the measurements carried out at ITU VLSI are included in the thesis. SiGe BiCMOS 0.13 μm process is utilized to fabricate the complete ADC, which has a 1.6 V supply and a silicon area of 2.2 mm × 3 mm.

IHP SiGe BiCMOS 0.13 μm'de
BORU HATTI ANALOGDAN DİJİTALE ÇEVİRİCİLER İÇİN
YÜKSEK HIZLI VERİ ELDE ETME TEKNİKLERİ

ÖZET

Günümüzün giderek dijitalleşen toplumunda, analog işaretleri dijital verilere dönüştürme yeteneği büyük önem taşımaktadır. Analogdan dijitale çeviriciler (ADÇ), fiziksel ve dijital alanlar arasında önemli bir köprü görevi görerek analog bilgileri analiz etmek ve işlemek için dijital hesaplamanın gücünden yararlanmamıza olanak tanır. Bu teknoloji, telekomünikasyon ve ses işlemeden bilimsel ölçüm ve tıbbi görüntülemeye kadar çok çeşitli uygulamaların temelini oluşturur.

Kablosuz iletişim alanındaki ileri teknolojiler, yüksek hızlı, veri yoğunluklu uygulamaların çoğalmasıyla karakterize edilen bir çağ başlattı. 5G ve ötesi, milimetre dalga görüntüleme, radar sistemleri ve yazılım tanımlı radyoyu da (software defined radio (SDR)) içeren bu uygulamalar, ultra yüksek hızlı ADÇ'ler ve RF alıcıların kullanımını gerektirir. RF ADÇ'ler, modern kablosuz iletişim sistemlerinde, analog RF alanı ile dijital işleme alanı arasında arayüz görevi gören önemli bileşenlerdir. Örnekleme hızları, alınan işaretin bant genişliğini doğrudan etkiler ve sonuç olarak performansları, genel sistemin yetenekleri üzerinde derin bir etkiye sahiptir.

Tamamlayıcı metal oksit yarı iletken (CMOS), silisyum-germanyum (SiGe) ve galyum-nitrit (GaN) gibi gelişmiş üretim teknolojilerinin ortaya çıkışı, benzeri görülmemiş derecede yüksek örnekleme hızlarında çalışan RF ADÇ'lerin ve RF alıcıların gerçekleştirilmesine olanak sağladı. RF ADÇ'ler, saniyede gigaörnek (GS/s) seviyelerinde işaretleri örnekleme yeteneğine sahip olup, geniş bant işaret edinimi sağlar ve hızla değişen RF işaretlerinin yakalanmasına olanak tanır.

Ultra yüksek hızlı RF ADÇ'ler ve RF alıcıları, kablosuz iletişim sistemleri için çok sayıda avantaj sunar. Bu avantajlar şunlardır:

- *Artırılmış işaret bant genişliği:*
  Yüksek örnekleme hızı, daha geniş bir frekans aralığının yakalanmasına olanak tanır, daha geniş modülasyon bant genişliklerini destekler ve daha fazla veri çıkışına olanak tanır.

- *Gecikmenin azalması:*
  İşaretleri yüksek hızlarda örnekleme yeteneği, gerçek zamanlı uygulamalar için kritik olan işaret işleme ve veri toplamayla ilişkili gecikmeyi azaltabilir.

- *Geliştirilmiş spektral saflık:*
  Yüksek örnekleme hızı, daha iyi bir frekans çözünürlüğü sağlar ve girişim ve harmonikler gibi istenmeyen spektral bileşenlerin algılanıp reddedilmesine olanak tanır.

Radar sistemlerde ultra yüksek hızlı RF ADÇ'ler, yüksek çözünürlüklü hedef tespit ve takibinin sağlanmasında önemli bir rol oynar. Yansıyan işareti, radar işaretinin

bant genişliğinden önemli ölçüde daha yüksek bir oranla örnekleyen bu ADÇ'ler, işaretteki ince ayrıntıları ve değişiklikleri doğru bir şekilde yakalayabilir, bu da hedef ayırabilmeyi ve durumsal farkındalığı artırır. Elektronik harp uygulamalarında RF işaretlerinin yüksek oranlarda örneklenebilmesi, işaret istihbaratı ve spektrum izlemede önemli bir avantaj sağlar. Bu işaretleri gerçek zamanlı olarak yakalayıp işleyerek, düşmanların operasyonel özellikleri ve niyetleri hakkında değerli bilgiler edinmek mümkündür.

Ultra yüksek hızlı RF ADÇ'ler ayrıca iletişim sistemlerinde, özellikle SDR'ler ve bilişsel radyolarda uygulama alanı bulur. Bu ADÇ'ler, geniş bantlı işaretlerin örneklenmesi ve işlenmesi için gerekli bant genişliğini sağlayarak gelişmiş modülasyon ve demodülasyon tekniklerinin uygulanmasına olanak tanır. Bu esneklik, SDR'lerin ve bilişsel radyoların değişen iletişim protokollerine ve spektrum koşullarına uyum sağlamasına olanak tanıyarak güvenilir ve verimli iletişim sağlar.

Ultra yüksek hızlı GS/s ADÇ'lerin geliştirilmesi, çeşitli RF sistemlerin yeteneklerini önemli ölçüde genişletti. Bu cihazlar, örnekleme performansının sınırlarını zorlayarak yeni uygulamalara olanak tanıyor ve mevcut uygulamaların performansını artırıyor. Yüksek bant genişliğine ve gerçek zamanlı şaret işlemeye olan talep artmaya devam ettikçe, ultra yüksek hızlı RF ADÇ'ler şüphesiz RF teknolojisinin geleceğini şekillendirmede giderek daha kritik bir rol oynayacaktır.

Çözünürlüğe göre analogdan dijitale dönüştürücü pazarı 8-b, 10-b, 12-b, 14-b, 16-b ve diğerleri olarak sınıflandırılabilir. Farklı çözünürlüklerin entegrasyonu, çeşitli uygulamaların gereksinimleri ile ortaya çıkmaktadır. 12-b çözünürlük türü, 2018 yılında analogdan dijitale dönüştürücü pazarına öncülük etti. 16-b çözünürlüğün, gelecekte liderliği alması bekleniyor. 5G iletişimi için 12-b'in benimsenmesi, ADÇ pazarının büyümesi için bir fırsattır.

Ortaya çıkan iletişim standartlarının katı gereksinimlerini karşılamak amacıyla, benzeri görülmemiş örnekleme oranları ve performansı elde etmek için gelişmiş ADÇ mimarileri araştırılmaktadır:

- *Boru hattı (pipeline) ADÇ:*
  Geleneksel boru hattı ADÇ'leri, her biri bir örnekle ve tut devresi, yükseltici ve niceleyiciden oluşan bir dizi kademeli aşama kullanır. Bu mimari yüksek örnekleme oranlarına izin verir, ancak birden fazla aşamadan dolayı gecikme ve güç tüketimi yüksek olabilir.

- *Zaman aralıklı (time-interleaved) mimari:*
  Boru hattı ADÇ'lerin sınırlamalarının üstesinden gelmek için zaman aralıklı mimariler ortaya çıkmıştır. Zaman aralıklı bir şekilde çalışıp birden fazla paralel kanal kullanarak örnekleme hızını etkili bir şekilde artırırken gecikmeyi ve güç tüketimini azaltabilir.

- *Flash ADÇ'ler:*
  Çözünürlük, güç tüketimi ve silikon üzerinde kapladığı alan pahasına çok yüksek örnekleme hızları elde etmek için paralel bir karşılaştırıcı dizisi kullanır.

- *Alt aralıklandırma (subranging) mimarisi:*
  Alt aralıklandırma ADÇ'leri, giriş işaretini birden fazla alt aralığa böler ve her bir alt aralığı niceler. Bu mimari yüksek hassasiyet ve düşük güç tüketimi sunar ancak örnekleme hızları sınırlı olabilir.

- *Katlanır enterpolasyon (folding interpolating) mimarisi*
  Bu gelişmiş veri dönüştürme sistemi, katlama enterpolasyon tekniklerini ADÇ teknolojisiyle birleştirir. Bu yaklaşım, giriş işaretini birden fazla alt işarete bölerek daha yüksek hassasiyete ve daha hızlı dönüşüm oranlarına olanak tanır; bunlar daha sonra ayrı ayrı enterpolasyona tabi tutulur ve dönüştürülür. Sonuçlar daha sonra analog giriş işaretinin doğru bir dijital temsilini oluşturmak için birleştirilir.

- *Hibrit mimariler:*
  Hibrit mimariler, performans özellikleri arasında bir denge sağlamak için farklı ADÇ mimarilerinin öğelerini birleştirir. Örneğin, hibrit ADÇ'ler, yüksek örnekleme oranları ve düşük gecikme süresi elde etmek için hem boru hattını hem de zaman aralıklı mimariyi birlikte içerebilir.

RF ADÇ'lerin performansı aşağıdaki gibi faktörlerle sınırlıdır:

- *Örnekleme hızı:*
  Daha yüksek örnekleme hızları, daha geniş işaret bant genişliklerine izin verir, ancak daha hızlı devre gerektirir ve güç tüketimini artırır.

- *Çözünürlük:*
  Daha yüksek çözünürlük, giriş işaretinin daha doğru temsil edilmesine olanak tanır, ancak ADÇ'de daha fazla bit gerektirir ve tasarım büyük ihtimalle kalibrasyona ihtiyaç duyar ve karmaşıklaşır.

- *Güç tüketimi:*
  Batarya ile çalışan cihazlar ve taşınabilir uygulamalar için düşük güç tüketimi şarttır.

- *Gelecekteki Araştırmar:*
  Ultra yüksek hızlı RF ADÇ mimarileri için gelecekteki araştırma önerileri şunlardır:

  - *Yeni ADÇ mimarilerinin araştırılması:*
    Daha da yüksek örnekleme oranlarına ulaşmak için geleneksel tasarımların sınırlamalarını aşan yeni ADÇ mimarilerine ihtiyaç vardır.
  - *Diğer cihazlarla entegrasyon:*
    RF ADÇ'lerin dijital işaret işlemcileri (DSP'ler) gibi diğer bileşenlerle entegrasyonu genel sistem performansını iyileştirebilir. Boyutu ve maliyeti azaltabilir.
  - *Düşük güçlü ADÇ tekniklerinin geliştirilmesi:*
    Güç açısından verimli ADÇ mimarileri, taşınabilir ve batarya ile çalışan uygulamalar için kritik öneme sahiptir.

Mayıs 2019'da Texas Instruments, sektördeki en geniş bant genişliğine, en düşük güç tüketimine ve en hızlı örnekleme hızına sahip yenilikçi, ultra yüksek hızlı bir ADÇ'yi piyasaya sürdü. Bu dönüştürücünün, mühendislerin 5G testi için verimli ölçüm doğruluğu elde etmelerine, osiloskoplar ve radar uygulamalarına (doğrudan X-bandı örnekleme) yardımcı olması bekleniyor.

Bu doktora tez çalışmasında, SiGe BiCMOS 0.13 μm'de 1.6 GS/s'ye kadar örnekleme frekanslarına sahip kalibrasyonsuz elde edilen simülasyon sonuçlarına göre düşük

giriş işareti frekansında 8-b ve en yüksek giriş frekansı olan 799 MHz'de 6.4-b üstünde ENOB sağlayabilen tek yönlü fiziksel 11-b bir boru hattı ADÇ sunulmaktadır. ADÇ'miz için, örnekle-tut kuvvetlendirici'nin (SHA) ADÇ'lerde en çok güç tüketen alt bloklardan biri olması ve kaçınılmaz gürültü ve bozulma getirmesi nedeniyle örnekle ve tut kuvvetlendiricisiz (SHA-less) mimari tercih edildi. 8x 1.5-b kaskad katlar ve arka uç 3-b flash ADÇ'ye sahip kompozit bir ADÇ mimarisi, 11-b'e kadar çözünürlüğe ulaşmak için tasarlanmıştır. ISI'yi azaltmak için yeni bir MDAC önerildi. Ayrıca, 6.43 GHz birim band genişliği ve 80 dB DC kazanç gerçekleştiren yeni bir BiCMOS RA uygulandı. Diferansiyel saat sürücüsü ve saat seviyesi kaydırıcıları ile 1.6 GHz örtüşmeyen farklı saat fazları oluşturma mimarisi tasarlanmıştır. Saat üretme sisteminin kendisi, simülasyonlarda 1.6 GHz saat sinyalinde , SNR_{jitter}, 57 dBc'ye ulaşır. İTÜ VLSI'da yapılan ölçümlerin sonuçlarına tezde yer verilir. 1.6 V beslemeli ve 2.2 mm x 3 mm silikon alanı kaplayan ADÇ'miz, SiGe BiCMOS 0.13 μm'de gerçeklenir.

1. INTRODUCTION

Analog signals and processing methods cannot be separated from our physical environment. The way we perceive the world in an analog manner, which means that the advantages of digital circuits are not immediately obvious. The coming section mentions about the motivation for the high speed ADCs (Analog Digital Conversion) by taking into account the philosophy behind it.

1.1 Motivation of High Speed ADC

The pervasive integration of digital computation and signal processing across numerous domains like as communications and instrumentation has resulted in a growing need for circuits that convert analog signals to digital format. ADC design is a continuously evolving field of study [3].

In the last 50 years, the electronics systems became increasingly digital [3, 4]. Digital circuits and digital signal processing are almost everywhere because of their noise immunity, strong anti-interference ability as well as high stability which make them more robust than analog counterparts. Very large scale integration (VLSI) fabrication technology improves semiconductor performance with each new generation. Therefore semiconductors attain improved performance over time while still maintaining lower costs due largely thanks VLSI technology's continuous improvements. The development of digital integrated circuits has been rapid over the past few decades, with progress being made in both synthesis tools and computer aided design (CAD) analysis as well [3, 4].

In order to establish a connection between digital and analog worlds, analog data should be sampled and quantized [3, 4]. Such circuits are known as analog digital converters. On the other hand, digital data can be converted to analog by zero order holding an analog value. This type of circuits is also known as digital analog converters.

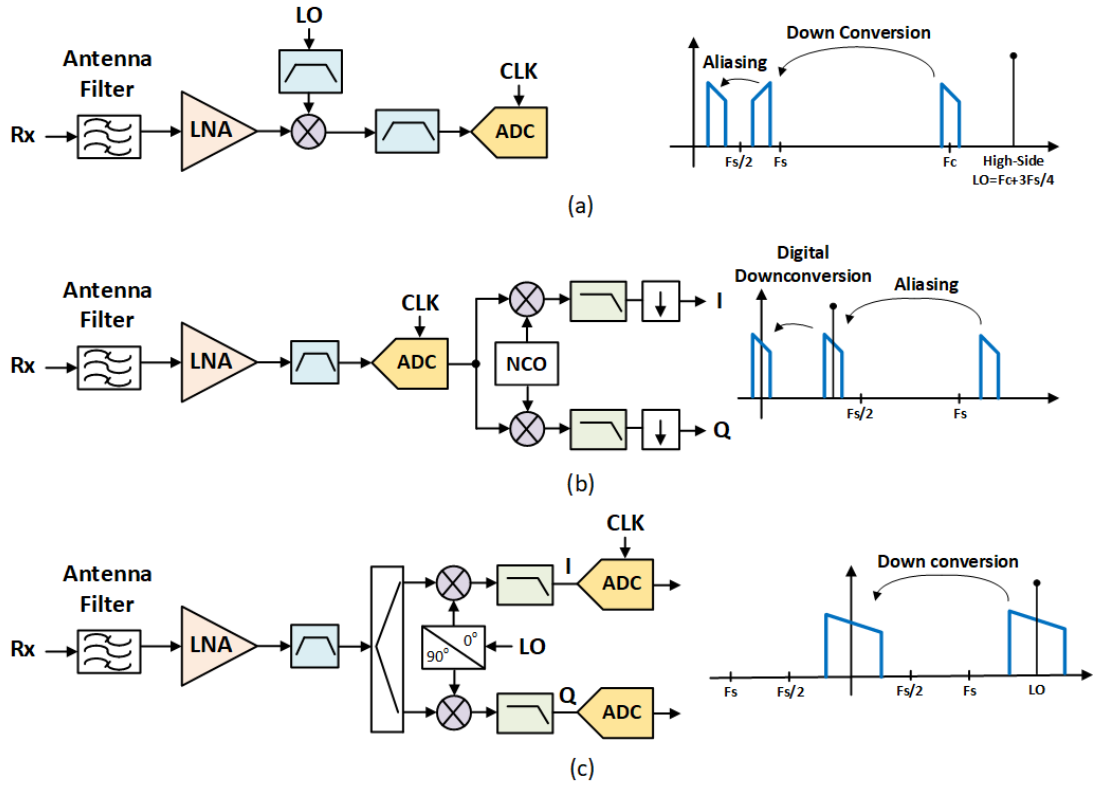


Figure 1.1 : (a) Heterodyne with 2nd Nyquist IF sampling, (b) Direct sampling with digital down conversion, (c)Direct-conversion/Zero-IF.

Audio communications often use sigma-delta, SAR, and algorithmic ADCs [3, 4]. A Flash ADC, which could utilize folding to achieve high speed but poor resolution (not exceeding 10 bits) [3, 4]. Since the 1990s, there has been a growing need for high-performance chips that have optimal parameters for both sampling rate and power consumption [3, 4]. This desire is particularly evident when dealing with intermediate frequencies (IF) that range from 50 MHz to 200 MHz, which require an output sample rate of over 400 MHz [3, 4].

ADC plays a crucial role in software defined radio and other wireless applications. As seen in Fig. 1.1, the proposal entails the conversion of the radio frequency (RF) signal into a digital format and its subsequent routing to the high-performance integrated circuit (IC) chip specialized in digital signal processing (DSP). This strategy seeks to surmount the obstacles posed by diverse wireless standards. The ADC must exhibit a notable degree of sensitivity, which is defined by a substantial signal-to-noise ratio (SNR) and a considerable spurious free dynamic range (SFDR). Furthermore, it is necessary to raise the sampling frequency to several Gigahertz while ensuring

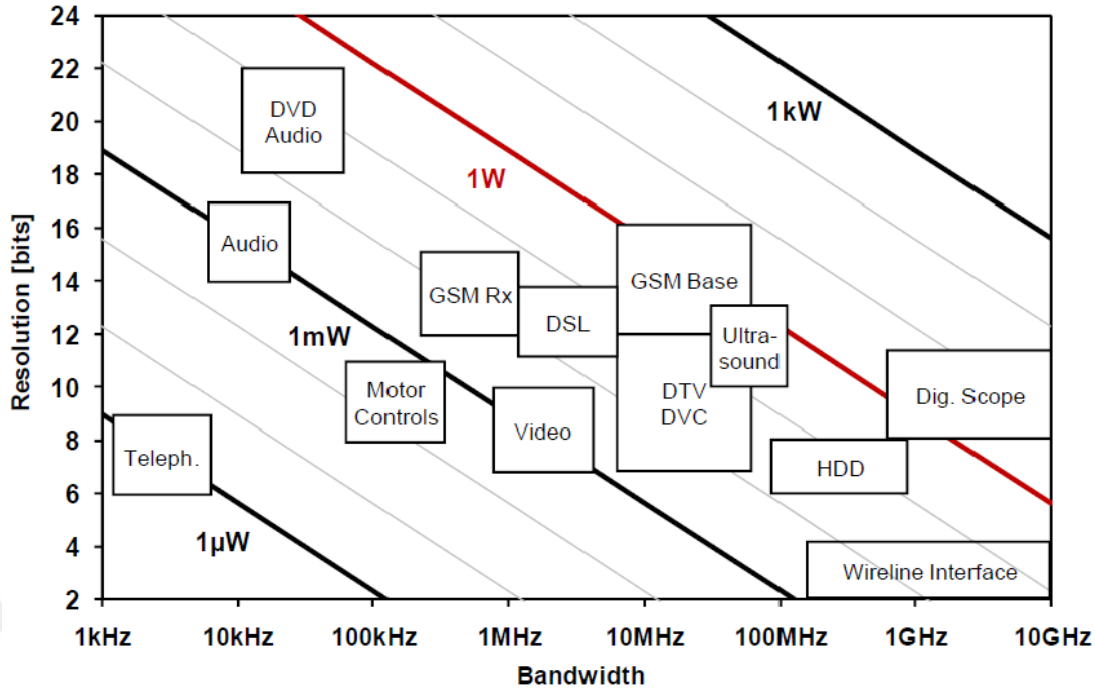


Figure 1.2 : ADC applications by Analog Devices, Inc.

a reasonably low power consumption. This is essential because the ADC must distribute power resources among different functional blocks within the transceiver system. Furthermore, ADC plays a pivotal role in wideband spectrum sensing, a basic capability essential to all cognitive radio systems. Hence, it is apparent that ADCs have a substantial influence on the architecture of software defined radio and other wireless systems.

Figure 1.2 displays the findings of a market analysis on the commercial products of ADC manufacturers. These devices have extensive applications in various fields, including communication and audio-visual equipment. They are available in a range of speeds, from 100 kHz to 10 GHz, with resolutions varying from 6-b (such as standard digital signal processing) to 22-b, which is commonly found in medical sensors or other high precision systems. In these systems, the focus is on larger quantities over extended periods of time rather than enhanced accuracy. The ADC market is projected to see a compound annual growth rate (CAGR) of 6.7 % and reach a value of 4 billion US dollars by 2027. In 2018, the market size was 2.30 billion US dollars.

1.2 Purpose of Thesis

This thesis emerges for the requirement of high speed sampling rate up to 1.6 GS/s and effective resolution above 8-b by taking advantage of IHP SiGe BiCMOS 0.13 μm, having promising performance with its 250 GHz transit frequency (f_T) of LV-NPN BJTs for high speed ADCs. A one-way 11-b pipeline ADC up to 1.6 GS/s sampling rate is targeted, which has not been reported in that technology process in the academic literature yet.

The scope of the thesis bases on high speed data acquisition techniques, implemented in the project TÜBİTAK-1003, 15E752:

- A composite one way pipelined ADC architecture, having 8x 1.5-b cascaded stages and a back-end 3-b flash ADC is proposed to reach up to 11-b resolution.
- A new multiplying digital to analog converter (MDAC) topology, which mitigates intersymbol interference (ISI) and increases signal-to-noise-ratio (SNR), is proposed [5].
- A novel highly linear BiCMOS residue amplifier (ResAmp) is proposed [6].
- Two patent applications for the proposed MDAC and ResAmp were accepted by the Turkish Patent and Trademark Office (TPTO) [5, 6].
- A 1.5-b BiCMOS current DAC with inverting buffers is proposed.
- A proposed architecture for non-overlapping clock generation incorporates a clock level shifter and a differential clock driver [7].
- In a 1.5-b front-end sub-ADC, cross-coupled adaptive power/ground switches and logics are integrated. [2]. Thus, power dissipation is reduced without the need for a dedicated SHA [2]. (Published at IEEE International ELECO 2019, Bursa, Turkey, and Granted as the Best Student Paper Award)

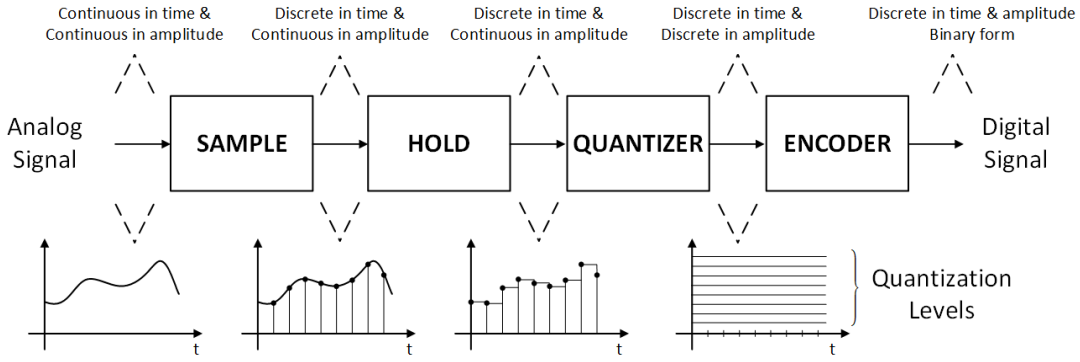


Figure 1.3 : A block diagram of an analog-to-digital converter.

1.3 ADC Overview

1.3.1 ADC definition

The ADC is responsible for converting an analog signal with time and amplitude into digital signals that can be processed by computers [3]. Sampling is a process of taking an analog signal and dividing it into more manageable pieces. The first step in this transformation involves converting the continuous level information from time domain, which becomes quantized when mapped to one sub-divided level within our digital codebook - called "code". This provides us assurance that signal can be reconstructed with arbitrary SNR.

1.3.2 Principal design considerations for ADC performance

First of all, with the increasing bandwidth of signal sources, like audio and video signals in modern times it is necessary to digitize signals at higher rates so they can be processed by ADC with higher speed sampling capabilities.

Secondly, the need for higher accuracy in data processing has led to an increase of the converters' dynamic range.

Third, the implementation of a complete electronic system in a single package is now easier than ever before as a result of the trend toward inexpensive and high-reliability monolithic integration on chip systems (SOC). Complete mixed signal circuits often combine digital processing along with analog calculated values.

1.3.3 ADC characterization

The purpose of this subsection is to provide an overview on how performance parameters are used in characterizing data converters [4]. Specifications can be divided into three groups: static, frequency-domain dynamic and time domain dynamics.

1.3.3.1 Static parameters

Accuracy of an ADC defines an error which it can convert a known voltage, including quantization and dynamic effects like distortion [3, 4].

Resolution, denoted by N bits, establishes the dimensions of the LSB within an ADC, thereby dictating the code lengths, dynamic range, and quantization error [3, 4].

Dynamic range is the ratio of the LSB to the FS. It can be expressed as [3]:

$$\mathrm{DR} = 20 \times \log\left(2^{\mathrm{N}}\right). \tag{1.1}$$

Offset error is the proportion by which the real transition voltage deviates from the ideal 1/2 LSB. Offset error is readily reducible through calibration [3, 4].

Gain error exhibits itself as the deviation in the slope of the line through ADC's end points at zero and full scale from the ideal slope of $2 \times \mathrm{N}/\mathrm{V_{FS}}$ codes-per-volt [3]. Gain error can be easily corrected by calibration.

Integral non-linearity (INL) is the distance of the code center in an ADC characteristic from the ideal line as illustrated in Fig. 1.4 [3, 4].

Differential non-linearity (DNL) refers to the discrepancy between the actual and expected step size in an ideal data converter, as illustrated in Figure 1.4 [3, 4].

Missing codes are an indication that the output digital code was not produced for any input voltage [3, 4]. Missing codes can be caused by either large DNL or non-monotonicity in the converter's internal design.

1.3.3.2 Frequency domain dynamic parameters

Signal to noise ratio (SNR) is the ratio between signal power and noise [3]. It can be expressed in decibels (dB) [3, 4]:

$$\mathrm{SNR} = \left(\frac{\text{Signal Power}}{\text{Total Noise Power}}\right) \text{ dB}. \tag{1.2}$$

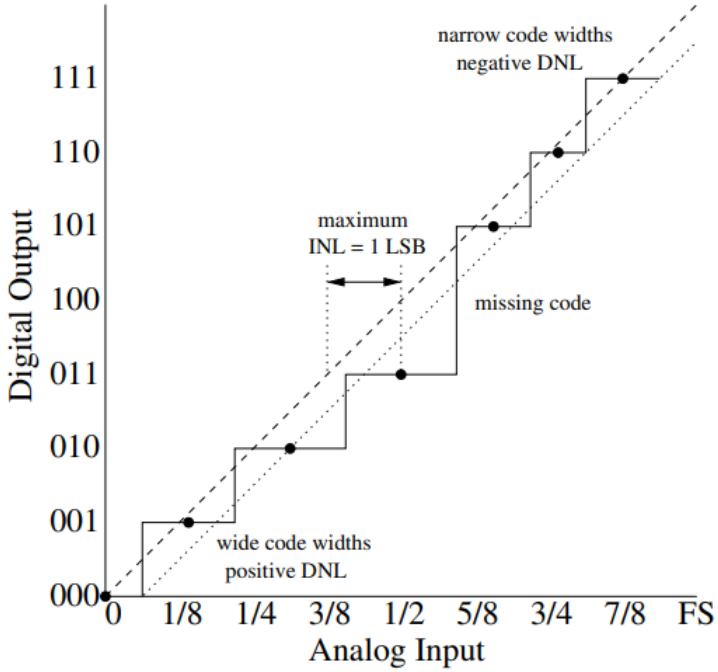


Figure 1.4 : ADC characteristic, showing non-linearity errors and a missing code. The dashed line is the ideal characteristic, and the dotted line is the best fit.

The SNR of a sinusoidal input in an ADC may be determined by considering the limitations imposed by quantization noise and thermal noise [3, 4]:

$$\mathrm{SNR} = 6.02 \times \mathrm{N} + 1.76\ \mathrm{dB}. \tag{1.3}$$

where N is the resolution of the ADC.

Spurious free dynamic range (SFDR) is the measure of the power ratio between the signal and the highest unwanted spurious component [3, 4]. Its primary reliance is on the input signal. Due to the fact that it represents the minimum signal magnitude that can be distinguished from a substantial interfering blocker [3, 4]. The specification of SFDR can be expressed in either full-scale (dBFS) or actual signal amplitude (dBc) units.

Total harmonic distortion (THD) is a measurement that quantifies the proportion of the combined root-mean-square (RMS) values of all harmonic components relative to the amplitude of the fundamental frequency within a certain frequency range [3, 4]:

$$\mathrm{THD} = 20 \times \log\left(\frac{\sqrt{\sum_{i=2}^{i} \mathrm{A}^2(\mathrm{kf_{in}})}}{\mathrm{A}(\mathrm{f_{in}})}\right) \tag{1.4}$$

where $\mathrm{A}(\mathrm{kf_{in}})$ is the amplitude of the harmonic tone presents at k-th multiple of input frequency $\mathrm{f_{in}}$.

Intermodulation distortion (IMD) occurs when a multi-tone input signal is mixed together nonlinearly with an ADC result that has integral Mathematics to generate tones at sum and difference frequencies [3, 4]. It can be calculated by taking the RMS value of these additional tones over one's fundamental tone.

Signal-to-noise and distortion ratio (SNDR) is a measure of the strength of the basic signal relative to the combined power of noise and distortion within a certain frequency range [3]. It can be represented as [3, 4]:

$$\text{SNDR} = \left(\frac{\text{Signal Power}}{\text{Total Noise and Distortion Power}} \right) \text{ dB}. \tag{1.5}$$

The limiting factor for SNDR at low levels is noise, while distortion becomes more prominent as the input signal strength increases [3, 4].

Effective number of bits (ENOB) is derived from the SNDR of an ADC and can be expressed as [3, 4]:

$$\text{ENOB} = \frac{\text{SNDR} - 1.76}{6.02}. \tag{1.6}$$

Effective resolution bandwidth (ERBW) is the frequency of the input signal at which the SNDR of the ADC decreases by 3 dB (0.5 bit) from its value for low-frequency input signals [3, 4]. It measures the bandwidth of the signal that an ADC is capable of processing. To prevent aliasing, it must typically not surpass the Nyquist frequency. On the other hand, the effective range of a sub-sample of ADCs may be expanded [3,4].

1.3.3.3 Time domain dynamic parameters

Jitter stems from random variations of the sampling instant around the ideal sampling time [3, 4]. It can be caused by the phase noise of the clock source, thermal noise and power supply noise. For a sinusoidal input, the SNR limitation, solely, because of jitter, can be expressed as [3, 4]:

$$\text{SNR}_{\text{Jitter}} = 20 \times \log \left(\frac{1}{2 \times \pi \times \text{f}_{\text{in}} \times \sigma_{\text{jitter}}} \right). \tag{1.7}$$

where σ_{jitter} is the root-mean-square jitter in seconds.

1.3.3.4 Figure of merit

Figure of merit Denoting the energy performance of an ADC, FoM is a straightforward metric [3, 4]. Power consumption, signal bandwidth, and effective

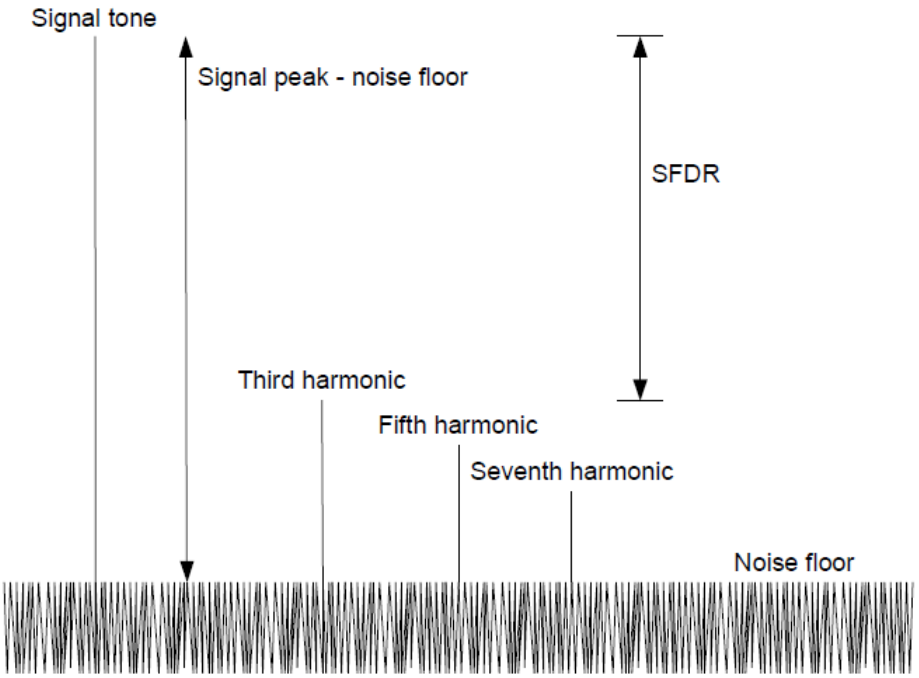


Figure 1.5 : ADC dynamic parameters.

resolution are considered in one of the most practical FoMs as follows [3, 4]:

$$\text{FoM} = \frac{\text{Power consumption}}{2^{\text{ENOB}} \times f_s}. \tag{1.8}$$

where f_s is the sampling frequency. It is a useful tool for quickly and easily comparing ADCs, but it should not be used as the sole criterion when judging ADC performance.

1.4 Organization of Thesis

Chapter 2 provides a concise overview of the pipeline ADC design. Chapter 3 introduces the SHA-less front-end 1.5-b sub-ADC and provides simulations of its performance. Chapters 4 discusses the process of designing a novel residue amplifier. Chapter 5 focuses on the design specifics and simulation outcomes of the proposed MDAC, which is a crucial component of the pipeline ADC. Chapter 6 provides an in-depth analysis of the 3-b back-end flash ADC and associated simulations for the proposed pipeline ADC. Chapter 7 mentions about a fully integrated multi-level non-overlapping clock phase generator. Chapter 8 provides an analysis of the simulation and measurement results for the other ADC components, as well as the overall implementation of the pipeline ADC. The dissertation is concluded in Chapter 9, which discusses the future prospects of the study.

2. SURVEY OF PIPELINED ADCs

This chapter provides a concise summary of the pipelined ADC design. We will provide brief description how it works and what its major subblocks do before getting into more technical complexity about non-idealities that affect resolution in ADCs with these types of architectures.

2.1 Architecture of Pipelined ADC

Pipeline ADCs are an excellent choice for applications that require high speeds. They achieve these qualities by breaking down quantization in multiple steps, with each stage being made up of similar components like those found within a fash ADC (though there is one sample-and-hold operation at the beginning). The block diagram of this architecture is shown on Fig. 2.1. It has advantages over other types such as increased latency but less noise figure due to its simplicity.

Prior to processing, the input signal is sampled by the sample-and-hold amplifier (SHA). Secondly, that sampled input signal gets quantized and converted into digital format by a sub-ADC which has M-b reduced resolution capabilities. The coarse digital output of that conversion is subsequently transformed into an analog signal by a sub-DAC and then subtracted from the sampled input signal. The residue obtained is an indicator of the quantization error that occurred during a single stage. The remaining data will then be transferred to the following stages for further digitization, but to uphold an identical dynamic range across all conversions at each step along the way (with M-b equal resolution), they're amplified by $2^{M_{eff}}$ which stands for amplifier with gain.

The ADC utilizes a dual-phase clock, where sampling and conversion operations are carried out in each of the phases. The stages collaborate, as seen in Fig. 2.2, to achieve optimal throughput, ensuring that fresh data is consistently accessible for output in each cycle (1/2 clocked). However this also means there's an introduced latency after

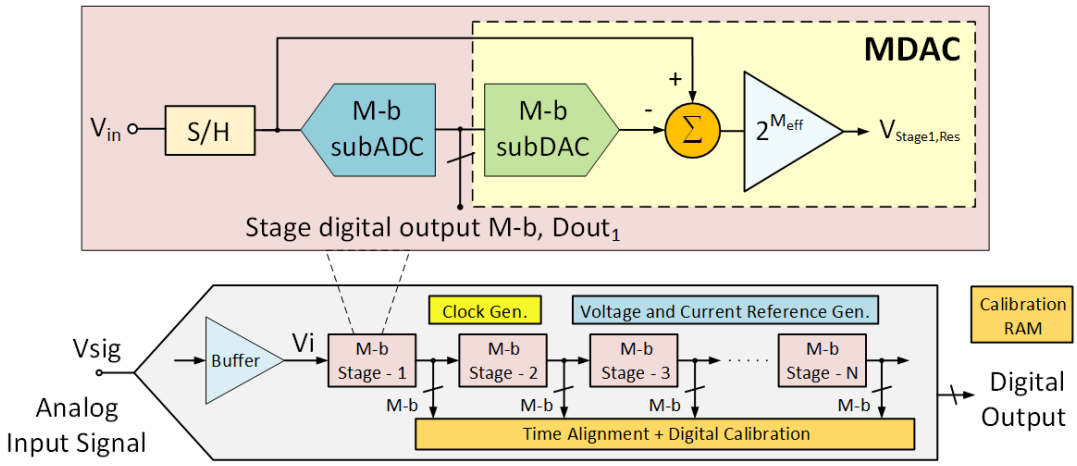


Figure 2.1 : Pipelined ADC architecture overview.

every operation; meaning we need some sort shift register or other device that can align the digital bits.

The total resolution of an ADC is defined by the combined effective resolutions of its individual stages. The number of unresolved bits lessens progressively as it passes through each stage. Because dynamic ranges remain constant at any given point in time for input signals being processed by these pipelines, there's no need extra precision with every passing stage [8].

2.1.1 Sub-blocks

The key components in a pipelined ADC system consist of the sub-ADC, sub-DAC, and residue amplifier. This section elucidates the collaboration between each block for digital output data to be generated from an analog input signal.

2.1.1.1 Sub-ADC

The sub-ADC samples the input signal and performs quantization on it. Generally, the sub-ADC is preferred to be a low-resolution quantizer due to the process of digitization being divided into several sequential stages. Typically, the flash architecture is used for the sub-ADCs [9]. Because, the design of flash ADCs is simple and they are suitable for low resolution and high speed application.

In Fig. 2.3, the trip points and comparators of a 1.5 bit sub-ADC are depicted. The trip voltages are at $\pm V_{REF}/4$. This is a simple 1.5-b flash ADC architecture. Regarding the trip points, the stage residual transfer function has 3 regions. The digital output

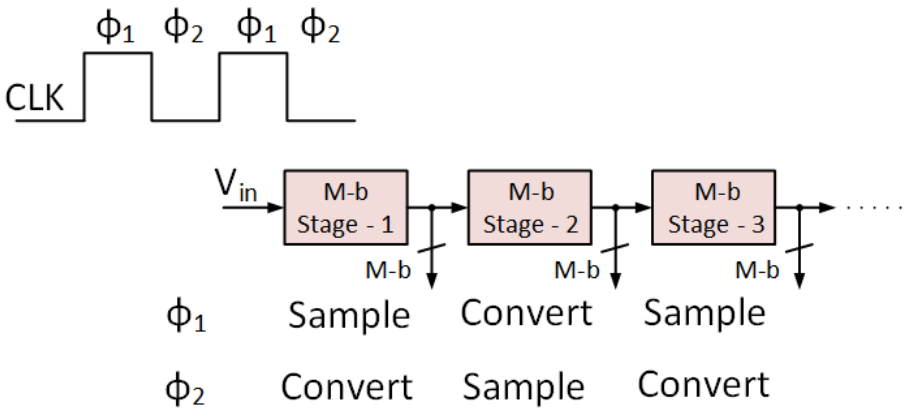


Figure 2.2 : Concurrent stage operation.

of the sub-ADC is represented as D_{out}, which becomes input for sub-DAC and digital calibration.

2.1.1.2 Sub-DAC

Douti, the output of the sub-ADC, must be deducted from the stage's input signal. This is accomplished through the utilization of a sub-DAC, which converts the digital output from the sub-ADC into its analog counterpart.

The most common sub-DAC topology is a capacitively operated device that can also sample and hold the input signal. This type of DAC has two phases. As shown in Fig. 2.4(a), during tracking, it uses its capacitors to track down any variations within an input signal. In hold phase, as depicted in Fig 2.4(b), these same capacitors are connected to reference voltages by which digital values are converted from the estimation of sub-ADC. The upper plates of the capacitors produce the residual voltage. This residual quantization error can essentially be expressed as

$$e_q = V_{in} - D_{out} \times \left(\frac{V_{REF}}{2^M} \right). \tag{2.1}$$

where $D_{out} \times (Vref/2^M)$ is the sub-ADC's output. The sub-DAC maps it onto the ADC reference voltage.

2.1.1.3 Residue amplifier

Pipelined ADCs commonly use inter-stage amplification of residue to ease the dynamic range requirements for subsequent stages. To ensure uniform swing across all their channels and minimize power usage, ideally a output stage's gain should be close or equal $2^{M_{eff}}$ which means it will have an amplifier with at least 20 dB more voltage gain.

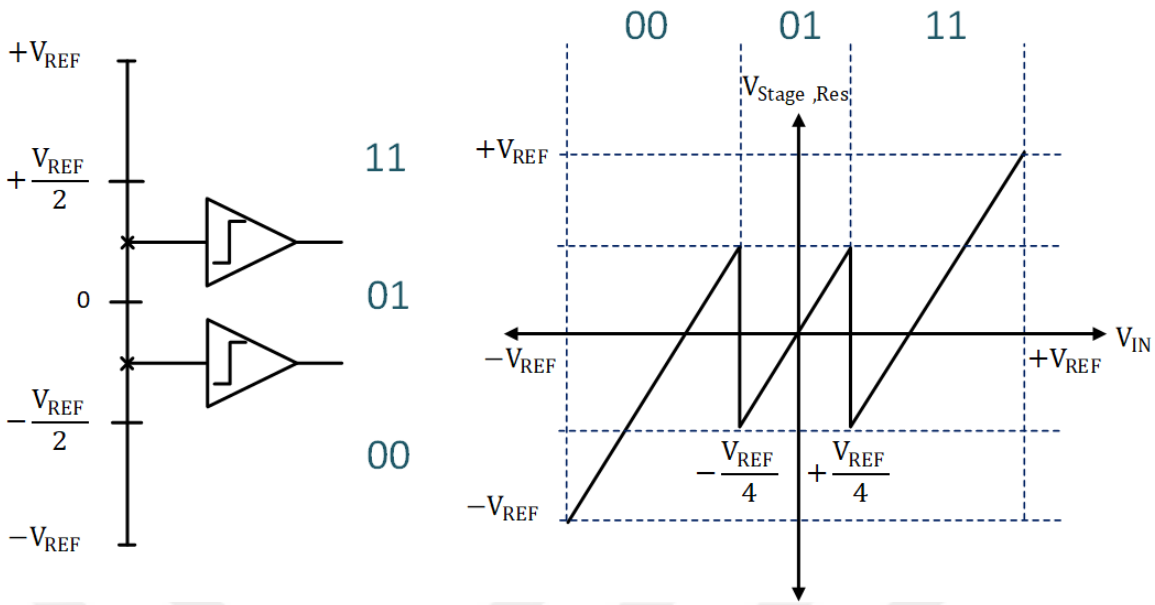


Figure 2.3 : Stage residue signal in 1.5-b stage.

The following expression describes the output of the amplifier which is the stage residue, or $V_{Stage,Res}$:

$$V_{Stage,Res} = G_a \times e_q = G_a \times \left(V_{in} - D_{out} \times \left(\frac{V_{REF}}{2^M} \right) \right). \tag{2.2}$$

where G_a is the amplification factor and equals to $2^{M_{eff}}$. If the digital output of the stage is incurred to reduction in the digital calibration, the stage gain is to be arranged by concerning the effective bit of the stage. For instance, a 1.5-b stage has a 1-b effective digital output; thus G_a of the stage is 2.

2.1.1.4 MDAC

As depicted in Fig. 2.1, the block formed by the ResAmp and the sub-DAC is called multiplying DAC or MDAC in short. A stage implementation by a flip around MDAC is illustrated in Fig. 2.4. Considering (2.2), the stage residue can be arranged as follows

$$V_{Stage,Res} = \begin{cases} \left(1 + \frac{C_S}{C_F}\right) \times V_{in} + \frac{C_S}{C_F} \times V_{REF}, & \text{if } -V_{REF}/4 > V_{in} \geq -V_{REF} \\ \left(1 + \frac{C_S}{C_F}\right) \times V_{in}, & \text{if } V_{REF}/4 > V_{in} \geq -V_{REF}/4 \\ \left(1 + \frac{C_S}{C_F}\right) \times V_{in} - \frac{C_S}{C_F} \times V_{REF}. & \text{if } V_{REF} \geq V_{in} \geq V_{REF}/4 \end{cases} \tag{2.3}$$

By operating the stages concurrently as shown in Fig. 2.5, we can have a sampling speed that is identical to each individual device while still resolving up until x bits per channel. This enables fast operation without significant constraints on resolution or

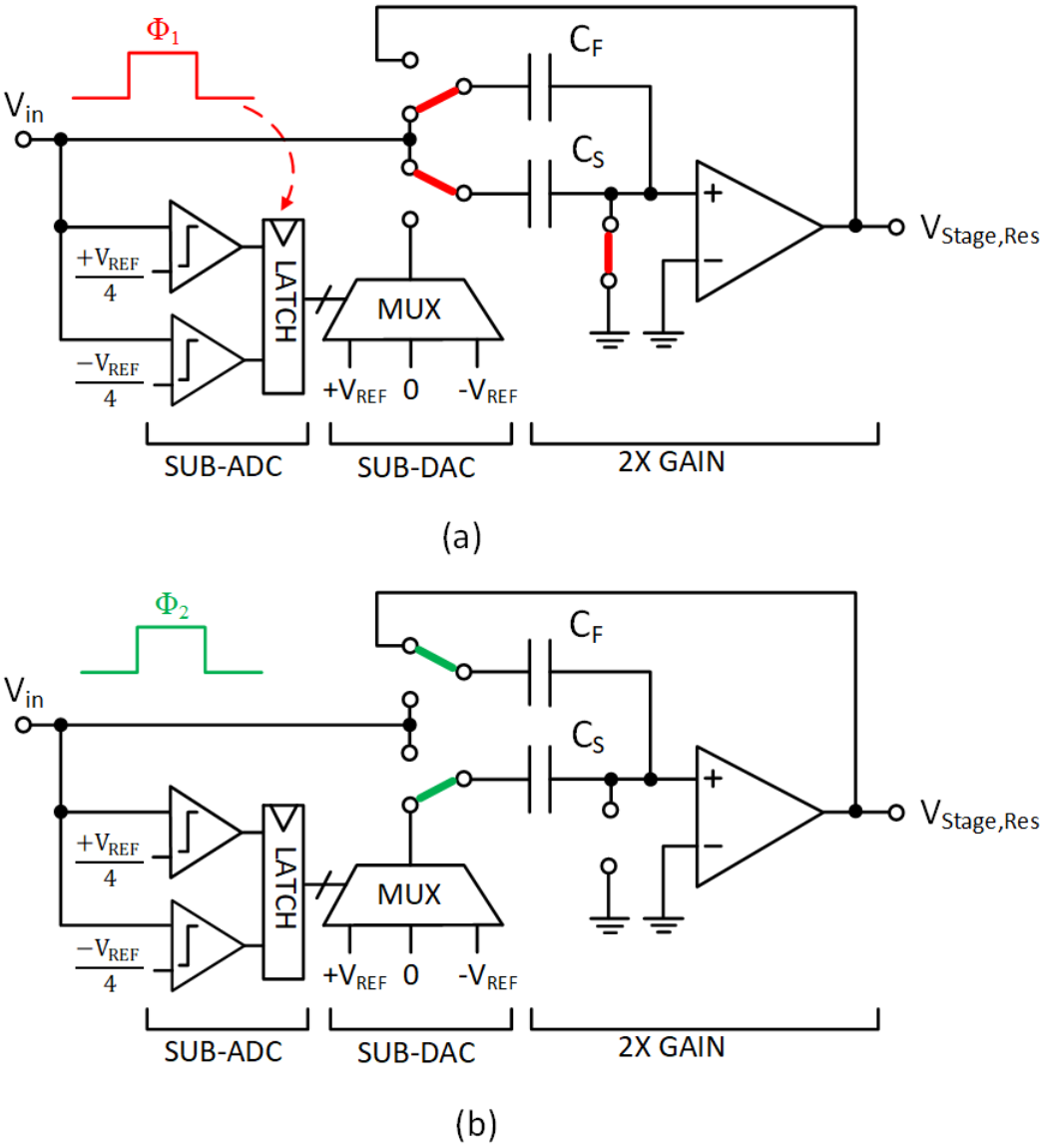


Figure 2.4 : 1.5-b stage implementation: a) Acquisition cycle, b) Conversion cycle

excessive expansion in area. However, it does incur an additional latency due to the utilization of numerous pathways during the conversion process..

2.2 Error Sources in Pipelined ADCs

Understanding and precisely quantifying the errors that have transpired are prerequisites for enhancing the precision of a data converter. Random errors typically arise from discrepancies among unit elements, whereas systematic errors can be attributed to conversion processes involving transformations. An example of such systematic errors is encountered during analog digital conversion.

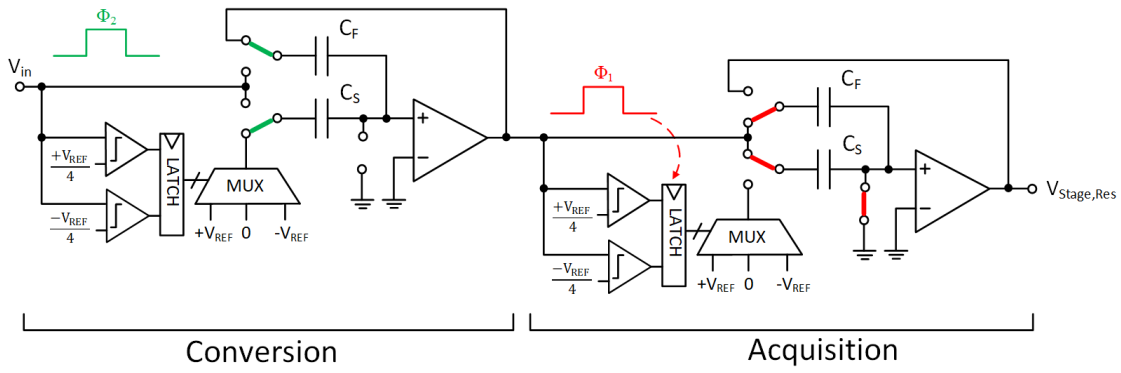


Figure 2.5 : Timing of 2 cascaded 1.5-b stages

It is simple to tolerate errors in a pipelined ADC by incorporating redundant conversion procedures [9]. As depicted in Fig. 2.6, the output code of the pipelined ADC, formed from 8x 1.5-b stages and a 3-b backend Falsh ADC, can be obtained by summing the shifted output bits of the stages.

The MDAC usually limits the performance of the pipelined ADCs. The sub-DAC, responsible for converting the sub-ADC's output to analog levels, must be accurate and precise in order to achieve the intended conversion accuracy. The step size for these calculations is determined by an array matched element but mismatched values can often lead errors across all stages. Observe the mismatch error in a DAC as segments of its transfer characteristic that are displaced by the product of capacitor discrepancies and inter-stage gain. Typically, capacitors are the most precise components utilized in the implementation of switched capacitor MDAC. The effect of a nonlinear 1.5-b sub-DAC on the ADC output transfer is depicted inin Fig. 2.7. Both non-monotonic behaviour and missing code can be observed in the digital output code.

Discrepancies in the comparator thresholds of the sub-ADC can affect the residual value despite providing an estimated value of the input signal. The main cause of error in this circuit's operation usually results in an offset that causes a shift in the sub-ranges of their ADC, as illustrated in Fig. 2.8. Without taking into account these changes at each step up through conversion could lead to missing codes. The 1.5-b stage pipelined ADC is a widely used design that incorporates the generation of overrange by including additional comparators in the sub-ADC. This architecture is designed to handle input signals within the nominal range of $-V_{REF}$ to $+V_{REF}$. One $\pm$Vref/4 input-referred offset is permissible for the comparators. Insufficient amplifier gain results in the

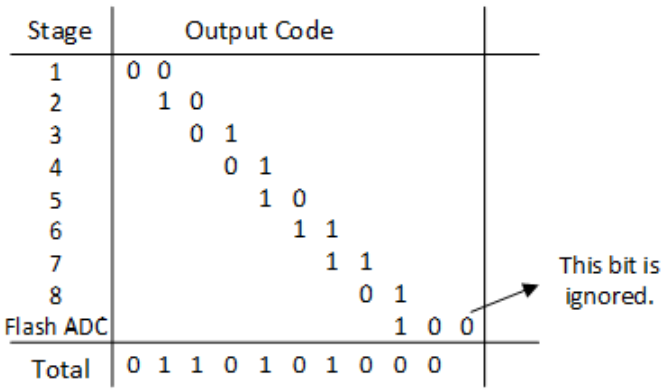


Figure 2.6 : Computing the output code for 8x 1.5b stages and 3-b backend Flash ADC.

presence of absent codes, as visually represented in Fig. 2.9. This signal-dependent gain may also distort the transfer function, as illustrated in Fig. 2.10, if the inter-stage gain is not uniformly linear. The settling of the residue amplifier is distorted due to the finite bandwidth of the operational amplifier.

In Fig. 2.11, the mathematical model of the stage error sources is illustrated. The summation nodes for the specific error sources are detailed, and the correction method for those errors are summarized in Table 2.1.

2.3 Calibration Techniques for Pipelined ADCs

The accuracy and precision of an ADC can be greatly impacted by its bandwidth. As seen in Fig. 2.12, increasing the analog bandwidth increases both noise and distortion levels which increases the importance of calibration when working at higher sampling rates [10].

The sampling rate of the pipeline ADC is commendable in conjunction with its high reliability. For pipelined ADCs with resolutions greater than 10-bits, it is crucial to carefully address the mismatch among capacitors [10]. Hence, SNDR is one figure that defines converter performance; calibration usually focuses on improving this value for every conversion done by an individual stage within the system.

Two principal methods are available for ADC calibration [10]:

- Internal hardware adjustment or refining is necessary for in-chip calibration [10].

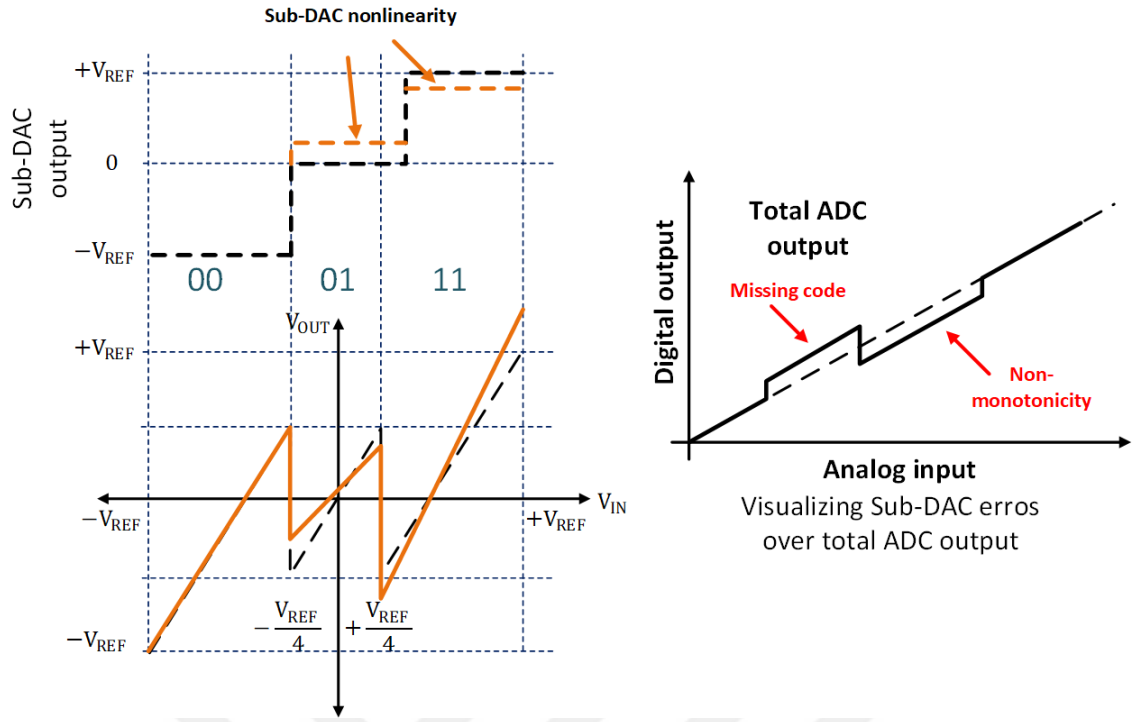


Figure 2.7 : ADC output transfer with a nonlinear 1.5-b sub-DAC

- DSP performs the compensation during off-chip calibration, wherein the ADC circuitry remains intact. Post-correction is a general term used to refer to this process [10].

DSP-based post-correction methodologies are the focus of this thesis because they are simpler to implement than circuit modifications [10]. Overall, post-correction methodologies exhibit greater adaptability and permit potential modifications or enhancements that necessitate solely the device's reprogramming [10]. This makes implementation much less complicated than trying to modify an entire complex ADC architecture from scratch with all its associated hardware requirements. By adding a block to the ADC output via a feedforward loop, the post-correction procedure is carried out, as shown in Fig. 2.13 [10].

The differences between static compensation versus dynamic calibration are depicted in Fig. 2.13a and Fig. 2.13b, respectively [10]. With a single correction term, ε_k, for every output code, static calibration provides an effective correction for early ADCs which had very narrow frequency bands. However, contemporary ADCs operate at high carrier frequencies where there is potential change in performance due to varying conditions such as PVT, distortions and interferences (ISI) so these types of

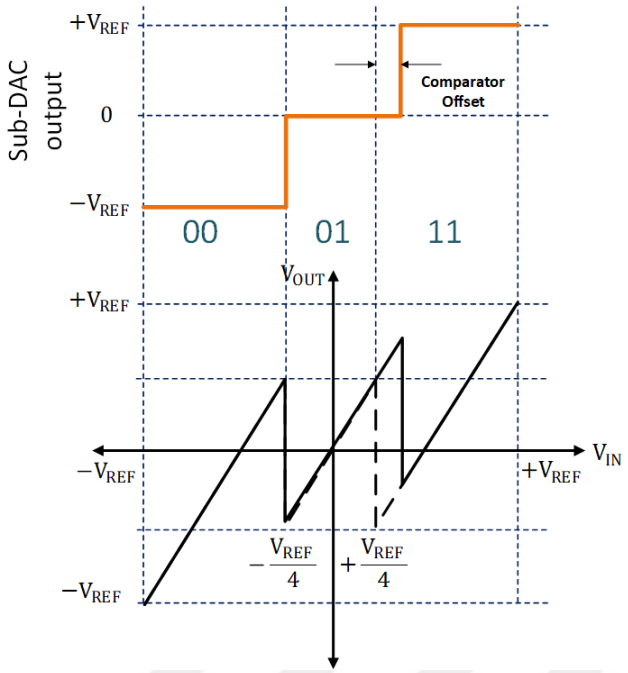


Figure 2.8 : The impact of comparator offset on a 1.5-b sub-ADC within a pipelined ADC stage.

measurements require more sophisticated methods than just adding one value into an equation. Additional characteristics such as frequency, slope, or previous sample are being incorporated into the development of a multidimensional table for dynamic error correction. These are denoted by m as illustrated in Fig. 2.13b [10].

2.4 Contribution to Calibrating ADC

This thesis presents three ideas on high-speed data acquisition approaches for pipelined ADCs, which are mutually complimentary.

Chapter-4

- A high-speed BiCMOS residue amplifier is proposed for MDAC.

Chapter-5

- Even though the SHA-less architecture has several advantages such as power reduction and not limiting the overall performance of the pipeline ADC, it also has a major drawback such as inter-symbol-interference [11]. The visibility of a quantized charge, coming from subDAC, at the sampling capacitor, which is visible at the input during the next sampling period, will cause ISI, which brings distortion tones into the Nyquist band. The new sample charge is correlated with the previous

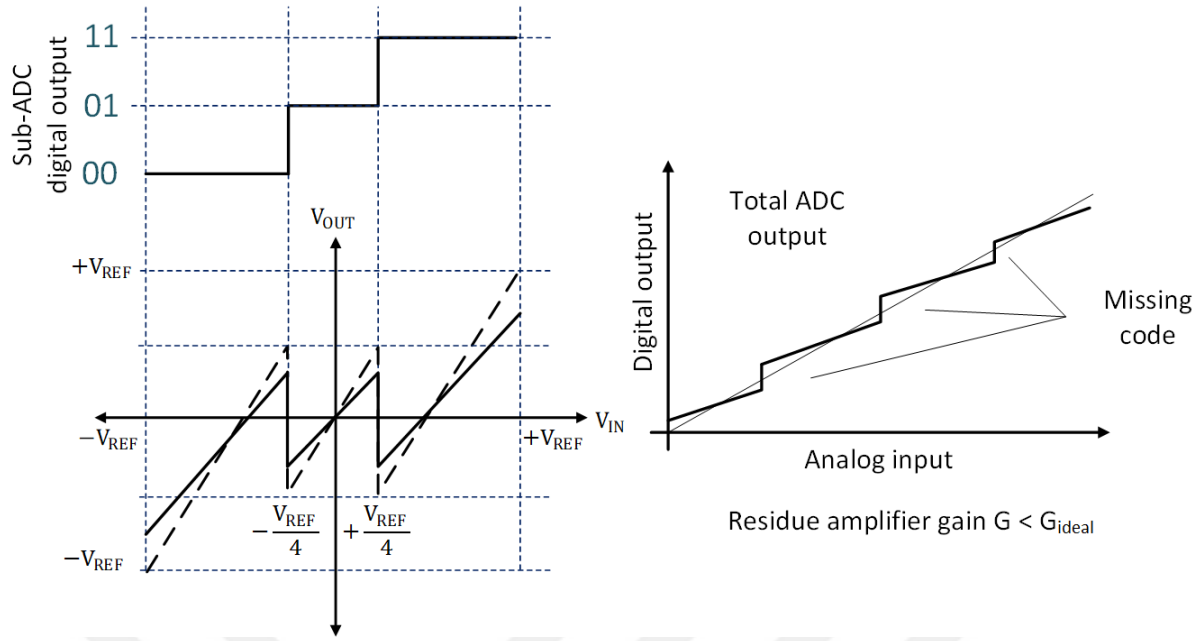


Figure 2.9 : The impact of amplifier gain error on the output code of an ADC.

sample. Thus, reset switches are proposed in order to alleviate the intersample interference effect (ISI) for the multiplying digital to analog converter (MDAC).

Chapter-7

- A groundbreaking fully integrated architecture for a multi-level non-overlapping clock phase generator is proposed [1,7]. SiGe BiCMOS process has BJT transistors having threshold voltage (V_{th}) around 850 mV. This naturally requires level shifted switches for switched capacitor operation. Design of high speed BiCMOS residue amplifiers for Pipelined ADCs requires very fast switching operation. In order to do that, the switches should charge and discharge the connected nodes very fast. In order to achieve fast switching, the gate voltage of the switch transistors can be level shifted. The proposed architecture provides 3 different voltage levels: [0-1.2V], [0.4V-1.6V], [1.6V-2.8V]. The proposed architecture provides fast switching operation, improves SNR of the ADC and lowers the switching noise [1,7].

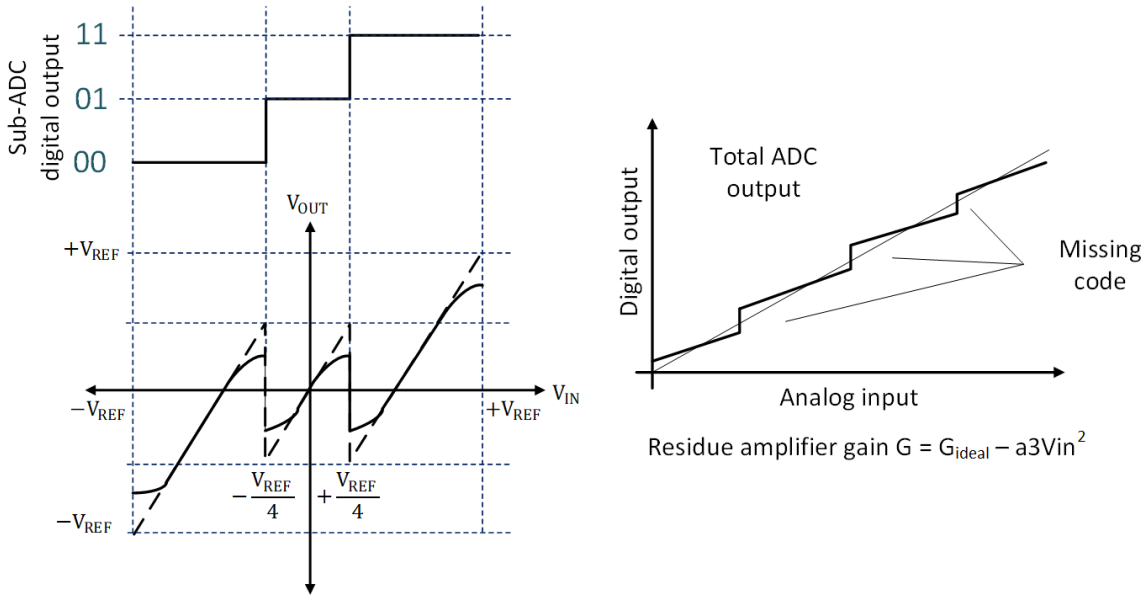


Figure 2.10 : Effect of amplifier nonlinearity on ADC output code.

2.5 Proposed Pipelined ADC

In a sample and hold operation we can simply obtain the SNR of a given input signal by regarding the total sampling capacitor as [3]:

$$\mathrm{SNR} = \frac{\mathrm{V}_{\mathrm{in,rms}}^2}{\mathrm{k} \times \mathrm{T}/\mathrm{C}_{\mathrm{S,total}}} \tag{2.4}$$

where $\mathrm{V}_{\mathrm{in,rms}}$ is the rms value of the peak-to-peak input voltage. In our design, we try to keep $\mathrm{V}_{\mathrm{in,rms}}$ as high as possible. The $\mathrm{V}_{\mathrm{in,p-p}}$ is 1V in our ADC. For an ADC of 12-b resolution and 1.6 GS/s, we need SNR of 74 dB and can use (2.4) as follows:

$$\mathrm{SNR} = \frac{\mathrm{V}_{\mathrm{in,rms}}^2}{\mathrm{k} \times \mathrm{T}/\mathrm{C}_{\mathrm{S,total}}} = \frac{(1/2\sqrt{2})^2}{4 \times 10^{-21}/\mathrm{C}_{\mathrm{S,total}}}, \quad \mathrm{C}_{\mathrm{S,total}} = 803\,\mathrm{fF} \tag{2.5}$$

As calculated in (2.5), the sampling capacitor should be at least 803 fF. However, this calculation omits the noise, emerging from the amplifier and ground noise in the amplifying mode for a 1.5-b MDAC.

Within an MDAC, the input noise is sampled and then sent towards the output of the Residual Amplifier (ResAmp). Additional noise is sampled when the entire capacitance $\mathrm{C}_{\mathrm{S,total}}$ is connected to the output of the DAC. Furthermore, the noise generated by the amplifier must be considered. The cumulative noise generated by

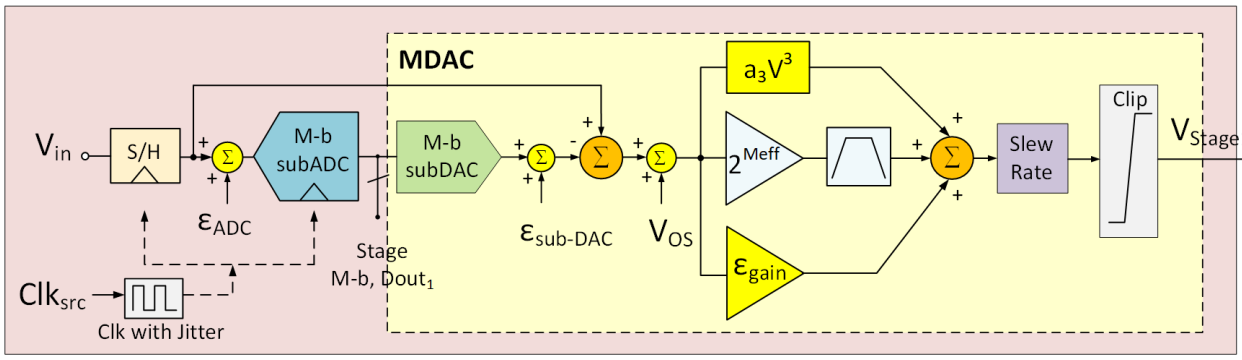


Figure 2.11 : Pipelined ADC stage error modelling.

the 1.5-b MDAC may be represented as:

$$v^2_{out,MDAC,noise} = \frac{3 \times k \times T}{C_{S,total}} < \frac{V^2_{LSB}}{12} = \frac{V^2_{p-p} \times 2^{-2\times N}}{12} \tag{2.6}$$

Consequently, we can calculate $C_{S,total}$ as follows

$$C_{S,total} = 2.48pF = \frac{12 \times 3 \times 1.38e^{-23} \times 298.15}{1 \times 2^{-2\times 12}} \tag{2.7}$$

We chose the total sampling capacitor almost the half of the value, calculated in (2.7). In the design, it is as 1.25 pF, which costs approximately 3 dB SNR reduction. In a 1.5-b flip-around MDAC, each of the capacitors, C_S and C_F, will be around 625 fF.

Now, we can estimate the noise, emerging from the cascaded stages. The overall noise for the cascaded stages of a pipelined ADC can be given as

$$v_{noise,ADC} = \sqrt{v^2_{noise,stg1} + v^2_{noise,stg2} \times G_1^{-2} + v^2_{noise,stg3} \times G_1^{-2} \times G_2^{-2} \ldots} \tag{2.8}$$

We can apply to (2.8) to take into account the noise contribution of each stage as follows

$$v_{noise,ADC} = \sqrt{\frac{3 \times k \times T}{C_{S,total,stg1}} + \frac{3 \times k \times T}{C_{S,total,stg2}} \times 2^{-2} + \frac{3 \times k \times T}{C_{S,total,stg3}} \times 2^{-4} \ldots} \tag{2.9}$$

Scenario-1

As mentioned above, $C_{S,total}$ is chosen as 1.25 pF for the 1st stage. Let's assume that the sampling capacitors of the following stages are also 1.25 pF. In that case, for the 1st, 2nd and 3rd stages, the total noise power can be calculated as:

$$v^2_{noise,ADC} = \frac{3 \times k \times T}{C_{S,total,stg1}} + \frac{3 \times k \times T}{C_{S,total,stg2}} \times 2^{-2} + \frac{3 \times k \times T}{C_{S,total,stg3}} \times 2^{-4} \tag{2.10}$$

Table 2.1 : Summary for the stage error parameters

Error	Description	Correction/Calibration
ε_{ADC}	Input offset voltage of the comparator	Redundancy either same stage or next stage
V_{OS}	Input offset voltage of the ResAmp	Redundancy either same stage or next stage
ε_{gain}	Gain error of the ResAmp	Digital adjustment
f_{UGBW}	Unity gain bandwidth of the ResAmp	Digital calibration
ε_{DAC}	Output offset voltage of the sub-DAC	Either sufficient component matching or digital calibration
a_3V^3	Third order distortion of the ResAmp	Digital calibration
σ_{jitter}	Phase jitter of the clock source	Filtering at clock source
SR	Slew rate	Digital calibration
Clipping	Power/ground limitation	Gain reduction

We can use (2.10) to derive the noise power:

$$v^2_{noise,ADC} = \frac{3\times 1.38e^{-23}\times 298.15}{1.25\text{ pF}} + \frac{3\times 1.38e^{-23}\times 298.15}{1.25\text{ pF}}\times 2^{-2} + \frac{3\times 1.38e^{-23}\times 298.15}{1.25\text{ pF}}\times 2^{-4} \tag{2.11}$$

where $v^2_{noise,ADC}$ is obtained as 1.3×10^{-8}. Now, we can apply to (2.4) in order to obtain SNR of the ADC:

$$\text{SNR} = \frac{V^2_{\text{in,rms}}}{v^2_{\text{noise,ADC}}} = \frac{(1/2\sqrt{2})^2}{1.3\times 10^{-8}} = 9644317.6 \tag{2.12}$$

which corresponds to 68.94 dB. Hereby, we do not apply the capacitor scaling for the 2nd and 3rd stages. There is 4.16 dB SNR loss according to the 12-b ADC.

Scenario-2

$C_{S,total}$ could be again chosen as 1.25 pF for the 1st stage. Let's assume that the sampling capacitors of the following stages are also 625 fF. In that case, for the 1st, 2nd and 3rd stages, the total noise power can be calculated as:

$$v^2_{noise,ADC} = \frac{3\times 1.38e^{-23}\times 298.15}{1.25\text{ pF}} + \frac{3\times 1.38e^{-23}\times 298.15}{625\text{ fF}}\times 2^{-2} + \frac{3\times 1.38e^{-23}\times 298.15}{625\text{ fF}}\times 2^{-4} \tag{2.13}$$

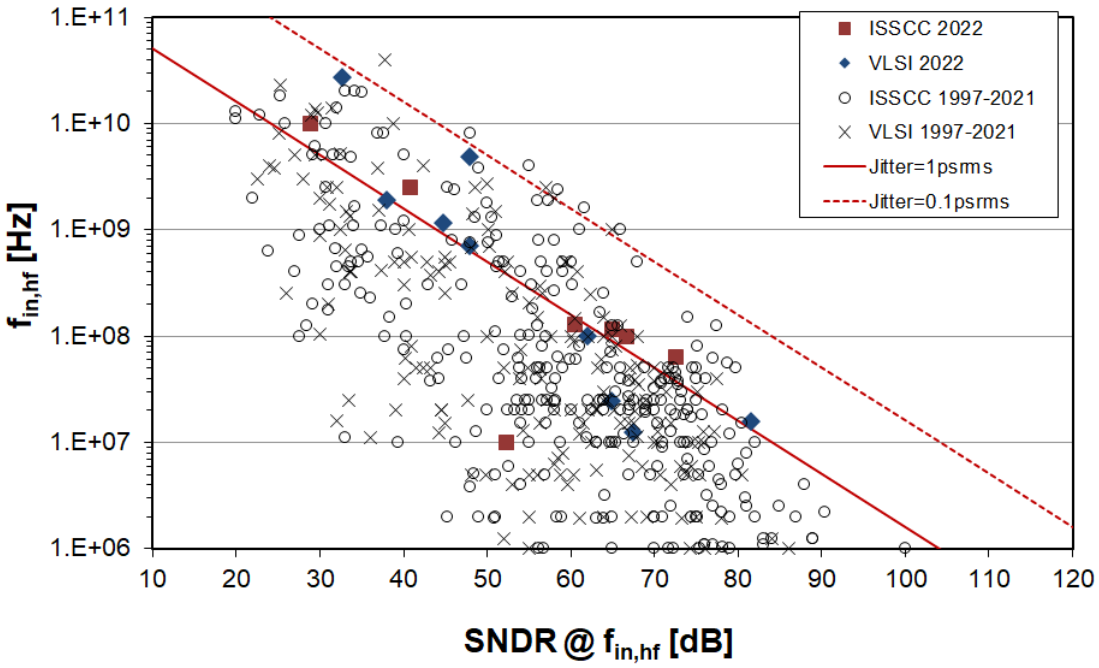


Figure 2.12 : The SNDR plotted versus the maximum input frequency for different ADC architectures taken from [12].

where $v^2_{noise,ADC}$ is obtained as 4.94×10^{-8}. Now, we can apply to (2.4) in order to obtain SNR of the ADC:

$$\mathrm{SNR} = \frac{\mathrm{V}^2_{\mathrm{in,rms}}}{\mathrm{v}^2_{\mathrm{noise,ADC}}} = \frac{(1/2\sqrt{2})^2}{4.94 \times 10^{-8}} = 2531715.3 \tag{2.14}$$

which corresponds to 64 dB. The capacitor scaling is applied for the 2nd and 3rd stages. There is 10 dB SNR loss according to the 12-b ADC. As depicted in Fig. 2.14, capacitor scaling is applied. From the stage-2 to stage-4, the sampling capacitor for each stage is 625 fF. From stage-5 to the final stage, the sampling capacitor is chosen as 325 fF for each stage.

SNR by individual noise contributors

Up to now, we only considered the thermal noise as the noise floor of the ADC. However, there are basically 3 different contributors which set the noise floor:

- Quantization noise of the ADC ($\mathrm{SNR_{Quantization}}$).
- Jitter of the clock source ($\mathrm{SNR_{Jitter}}$).
- Thermal noise of the ADC ($\mathrm{SNR_{Thermal}}$).

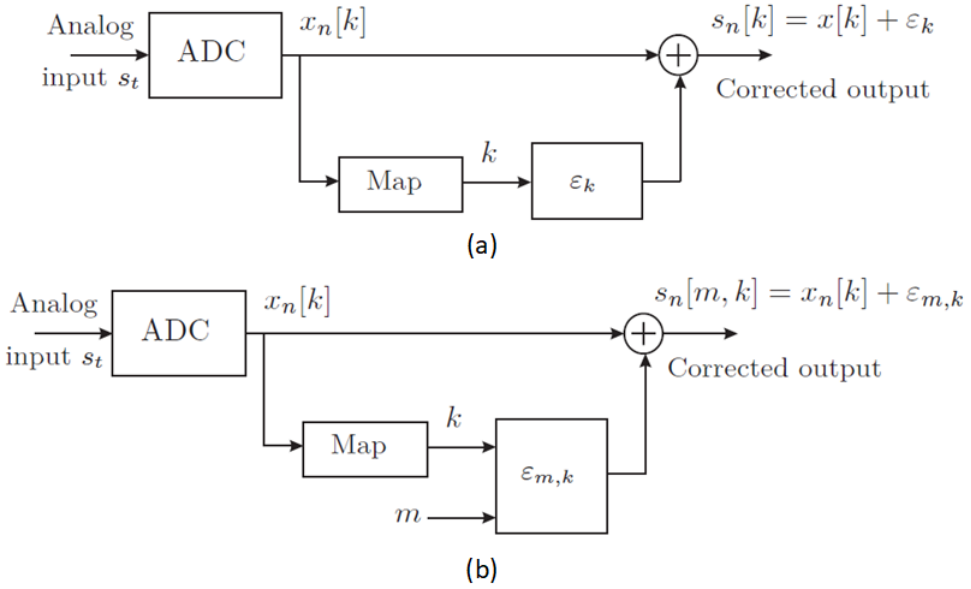


Figure 2.13 : Post-processing calibration: (a) Static ADC post-correction employing a look-up-table approach, n represents the running time index, (b)Dynamic ADC post-correction, where m is an additional parameter addressing the look-up-table.

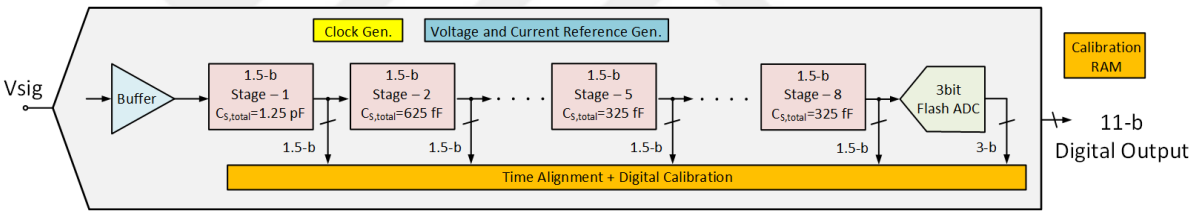


Figure 2.14 : The proposed 11-b SHA-less pipelined ADC.

$$\mathrm{SNR_{ADC}(dB)} = -20 \times \log\left(\sqrt{\left(10^{-\frac{\mathrm{SNR_{Quantization}}}{20}}\right)^2 + \left(10^{-\frac{\mathrm{SNR_{Jitter}}}{20}}\right)^2 + \left(10^{-\frac{\mathrm{SNR_{Thermal}}}{20}}\right)^2}\right) \tag{2.15}$$

According to the scenario-2, $\mathrm{SNR_{Thermal}}$ is obtained as 64 dB. The 11-b ADC has an $\mathrm{SNR_{Quantization}}$ of 68 dB. Considering (1.7), σ_{jitter} can be valued from 100 fs to 400 fs as illustrated in Fig. 2.15. An applicable σ_{jitter} can be 200 fs for our applications. The overall $\mathrm{SNR_{ADC}}$ is shown in Fig. 2.16. Still, the ADC could exhibit 10-b ENOB up to 500 MHz input signal frequency while the sampling frequency is at 1.6 GS/s.

2.6 Conclusion

This chapter provides a comprehensive analysis of the fundamental components of pipelined ADCs, including sub-ADC, sub-DAC, residue amplifier, and MDAC. The

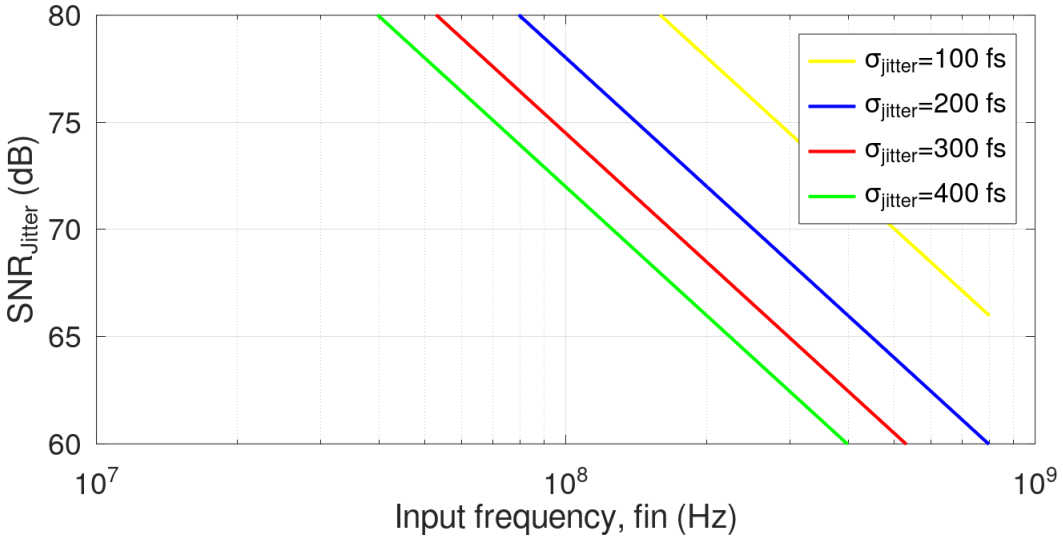


Figure 2.15 : SNR by individual noise contributors.

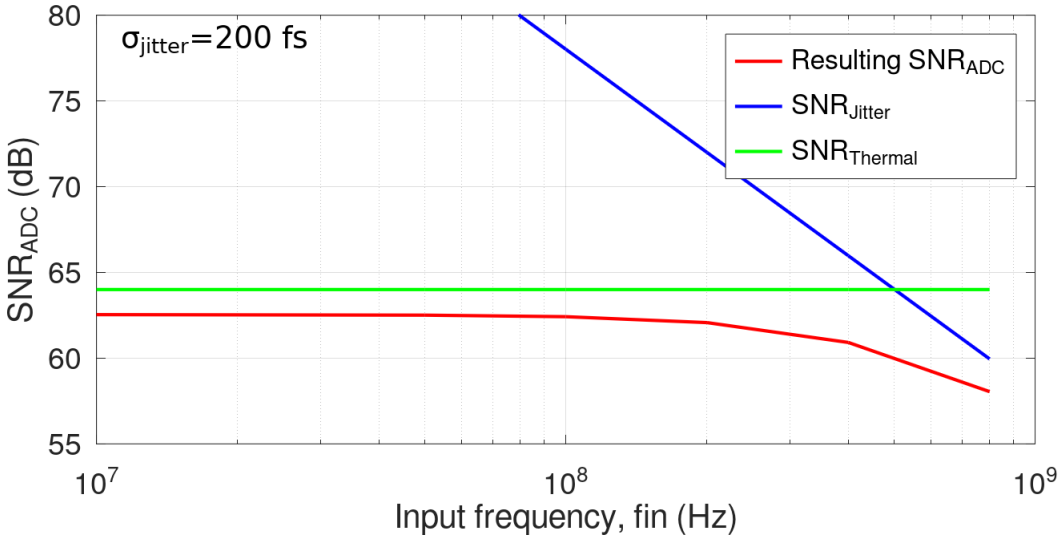


Figure 2.16 : SNR by individual noise contributors.

effects of their nonidealities on performance were also reviewed with special emphasis onto digital calibration techniques. They minimize those nonideal impacts as much as possible while still enable acceptable results from the measurements.

3. FRONT-END STAGE FOR SHA-LESS PIPELINED ADCs

SHA-less architectures are generally more desirable for high-speed pipeline ADCs due to the fact that the SHA circuitry is among the most energy-intensive sub-blocks [2]. Furthermore, no stage suppresses the noise and distortion of this block; therefore, the performance of the SHA imposes an irrevocable constraint on the overall performance of the ADC.

3.1 Purpose

While the S/H block does not include AD conversions, it does provide a consistent input voltage for the first stage of the pipeline ADC [11]. As depicted in Fig. 3.1a, the signal, denoted as V_1, which is sampled by the MDAC, should be identical to the signal, denoted as V_2, which is sampled by the sub-ADC. A mismatch between these signals is considered a discrepancy, which will manifest as a comparator offset. The magnitude of the erroneous signal, denoted as V_e, is contingent upon both the magnitude and frequency of the input signal. If the input signal is a sinusoidal waveform represented by $V_{in} = A \times \cos(2\pi \times f_{in} \times t)$, the most significant mistake happens at the highest rate of change of this waveform and also at the point when it crosses zero. The maximum skew of each MDAC is determined according to Chang's study in 2004 [2, 11]:

$$\Delta\tau \approx \frac{1}{8 \times \pi \times f_{in}} \approx \frac{1}{8 \times \pi \times 800\text{MHz}} \approx 49.74\text{ps}. \tag{3.1}$$

where $\Delta\tau$ is a tolerable skew. The value of $\Delta\tau$ may be determined as 49.74ps for a maximum input frequency of 800 MHz. Practically, it is advisable to maintain a minimal skew, taking into account additional imperfections [2]. For instance, when the comparator offset is taken into account, it is necessary to decrease the aperture error [2].

The decision time of the 1.5-b subADC (T_{subADC}) is a crucial specification that determines the conversion time of a pipeline stage, as seen in Fig. 3.1 [13]. If the duty cycle of ϕ_{1b} is 50%, and the sampling rate is 1.6 GS/s, then T_{subADC} may be

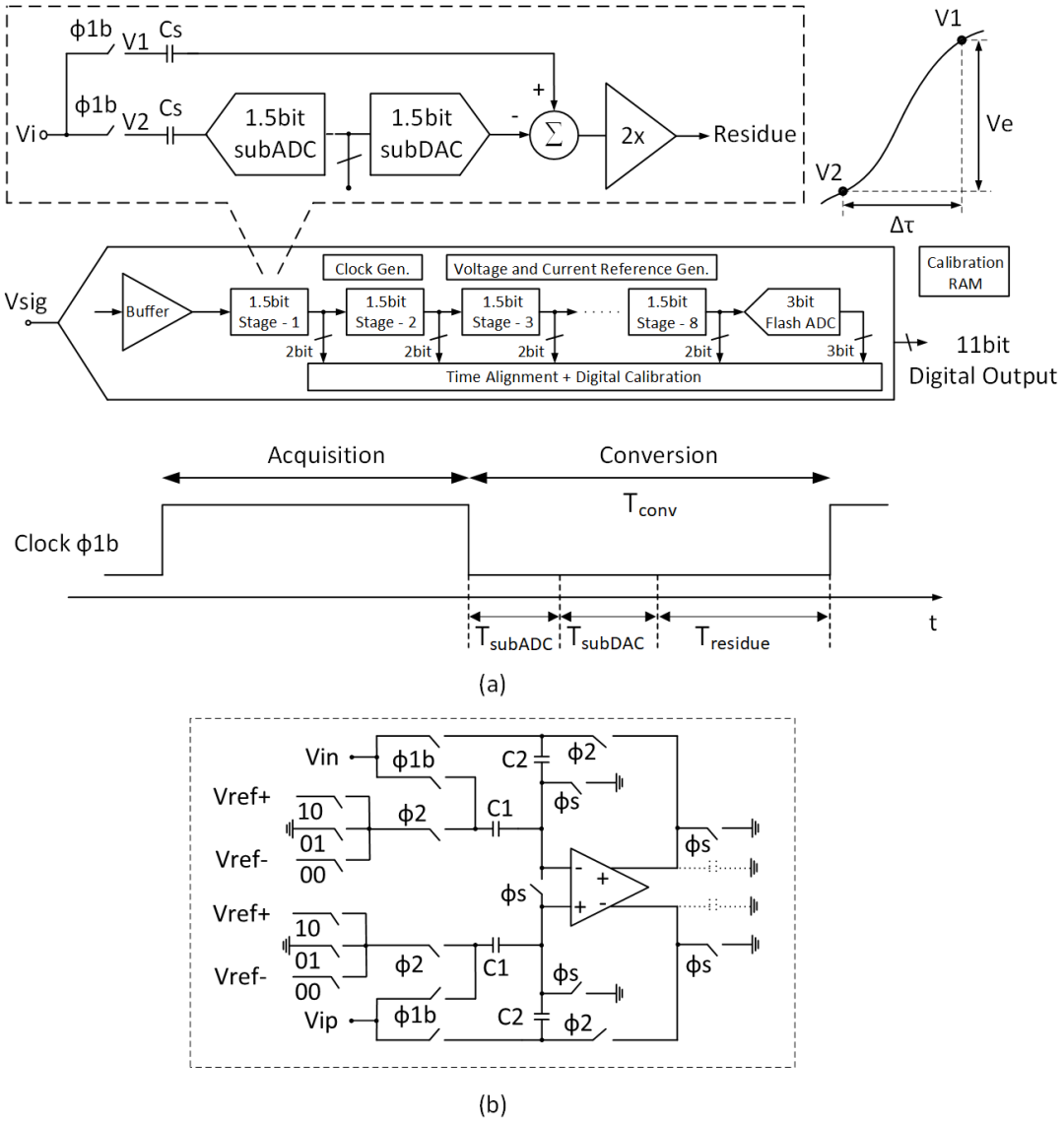


Figure 3.1 : (a) The proposed 11-b 1.6 GS/s SHA-less pipeline ADC in the project TÜBİTAK-15E752, and acquisition and conversion time for clock signal, ϕ_b [2], (b) a classical 1.5 bit flip-around MDAC [2].

calculated using the expression provided in [2, 13]:

$$T_{subADC} + T_{subDAC} + T_{residue} \leq T_{conv} \approx 312.5ps. \tag{3.2}$$

3.2 1.5-b Front-end SubADC

This section provides a concise overview of our design technique for the proposed 1.5-b front-end sub-ADC, as shown in Fig. 3.2.

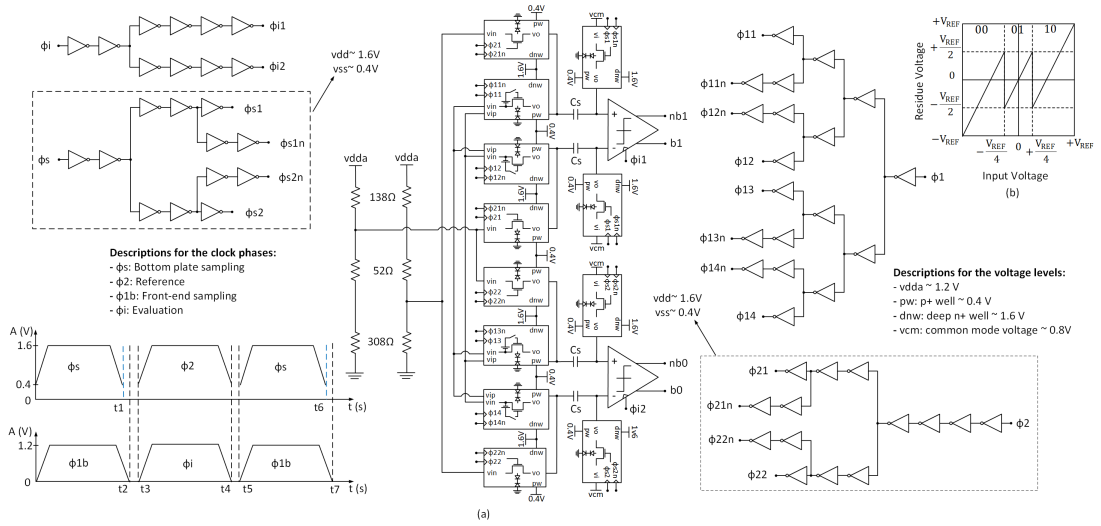


Figure 3.2 : (a) The proposed 1.5-b front-end subADC with modified charge distribution comparators, symmetrical cross coupled bootstrap and adaptive power/ground switches and logics [2], (b) A flip around pipeline stage residue characteristic with its digital output code [13].

3.2.1 Sizing the sampling capacitor

The input voltage range, denoted as $V_{in,p-p}$, is 1V in our pipeline Analog-to-Digital Converter (ADC) system, as shown in Fig. 3.1 [2]. This ADC has a physical resolution of 11 bits and a sampling rate of 1.6 GS/s. In a flip-around MDAC, the input noise is sampled and sent to the amplifier's output [3]. Additional noise is sampled when C_1 is linked to the output of the DAC. Furthermore, the noise generated by the amplifier must be considered. The whole noise, with an excess factor of 3, may be represented as stated in the reference [2, 3]:

$$v^2_{outMDAC,noise} \approx \frac{3 \times k \times T}{C_1 + C_2} < \frac{V^2_{LSB}}{12} = \frac{V^2_{p-p} \times 2^{2N}}{12}. \tag{3.3}$$

where C_1 and C_2 are the sampling capacitors, k is Boltzmann constant, 1.38×10^{-23} J/K and T is a room temperature in Kelvin, 298.15, N is resolution 11-b, V_{p-p} is the differential peak to peak input voltage, 1V. Regarding (3.3), C_1 + C_2 is calculated as 1.25 pF. Cs correspond to the half of C_1 + C_2.

3.2.2 Modified charge distribution strong ARM clocked comparator

In our design, we modified the charge distribution clocked comparator [2, 14] as depicted in Fig. 3.2a; thus, C_S is, solely, used as a sampling capacitor. Moreover we

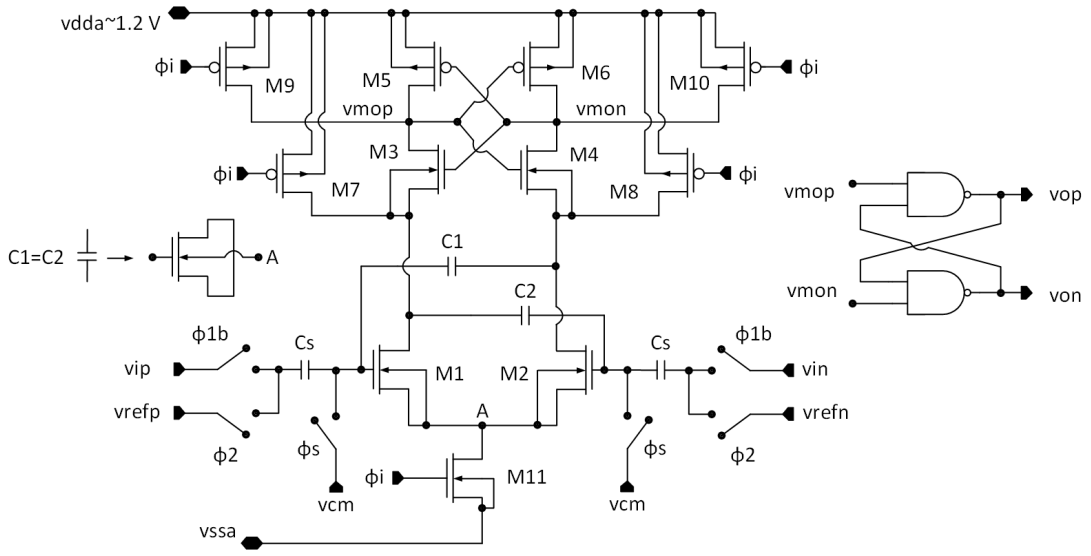


Figure 3.3 : A modified charge distribution strongARM clocked comparator with neutralization capacitor and NAND based SR latch [2, 14, 15].

use the strongARM clocked comparator circuit, which allows a significant reduction for the decision time and also neutralization capacitors [15] to mitigate the kick back effect, substantially.

3.2.3 Symmetrical cross coupled bootstrap switch

The linearity of a standard bootstrap switch is enhanced by including a symmetrical counterpart, as seen in Fig. 3.4 [2]. The switch transistor M4 is accompanied by a dummy transistor, M2, which mitigates clock feedthrough [2]. In addition, a coupling capacitor C_{dm} with a capacitance of 15 fF is used to eliminate the feedforward parasitic capacitance of the switch transistor, M1 [16].

In order to achieve a resolution of 10 to 14-b in an ADC, a time period (Ts) of around 7 to 10 time constants is required, as stated by [3]. When the sampling frequency (fs) is greater than 1.6 GS/s, the tracking time for half of the period (Ts/2) is precisely 312.5 ps. If our goal is to achieve a settling time of 7τ with an approximate inaccuracy of 0.1% [2, 3]:

$$R_{switch} \times C_S \approx \frac{T_S}{2 \times 7} = \frac{0.3125 \times 10^{-9}}{7 \times 625 \times 10^{-15}} = 71.42\Omega. \tag{3.4}$$

In order to get the desired channel resistance, the (W/L) of the switch transistor is selected as (70 μm)/(0.13 μm), resulting in a channel resistance of 50 Ω [2]. The driver's output impedance has a 20 Ω allowance, as shown in Fig. 3.1 [2].

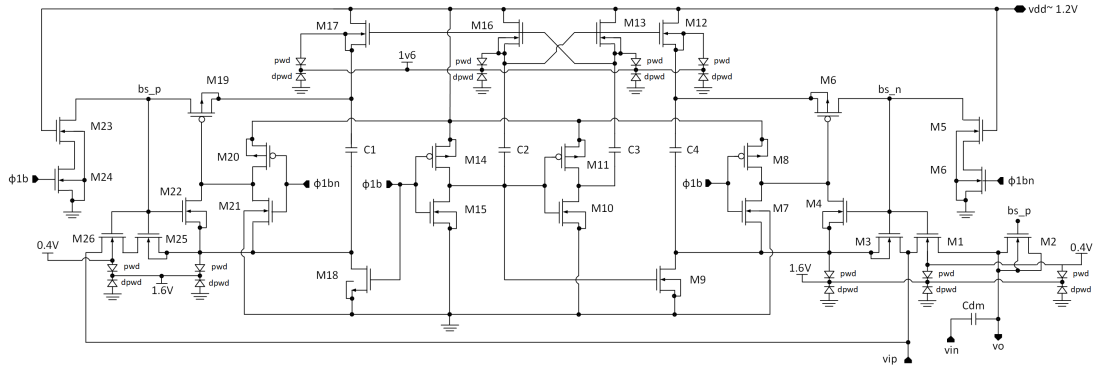


Figure 3.4 : The proposed symmetrical bootstrap switch with a forward neutralization capacitor, C_{dm}, and clocked feed-trough cancellation [2].

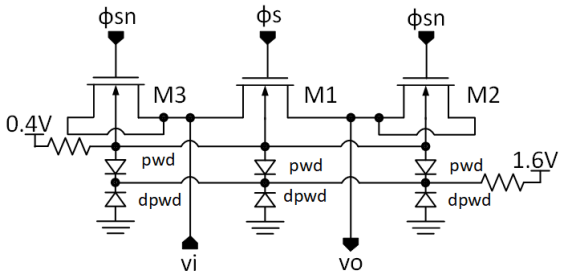


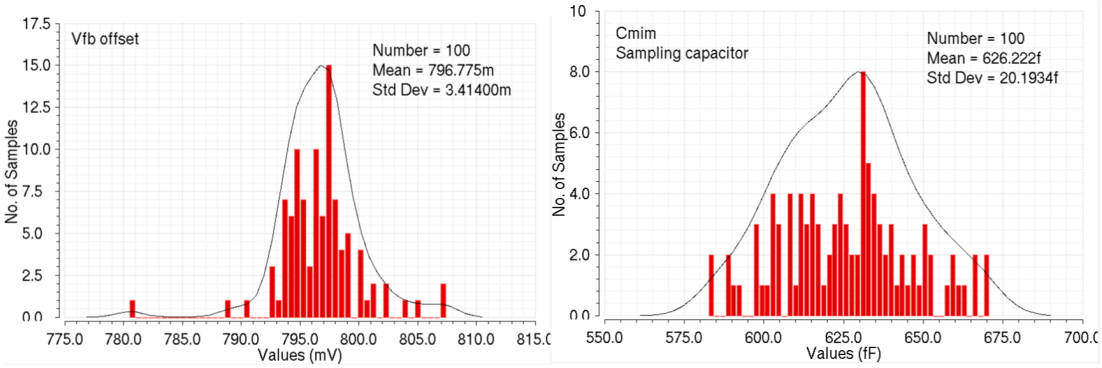
Figure 3.5 : The proposed adaptive power/ground NMOS switch [2].

3.2.4 Adaptive power/ground NMOS switches and logics

In this design, the voltage reference for the clocked comparator is set to 800 mV in order to increase the bandwidth [2]. In order to expedite the reset time at the input terminals of the clocked comparators, the adaptive power/ground switches are used, as shown in Fig. 3.5 [2]. To prevent clock feedthrough, the switch M1 is accompanied by two dummy transistors, M2 and M3, which support its two I/O terminals. The reset and reference switches are activated by clock signals that have been adjusted to a voltage range of 400 mV to 1.6 V [2].

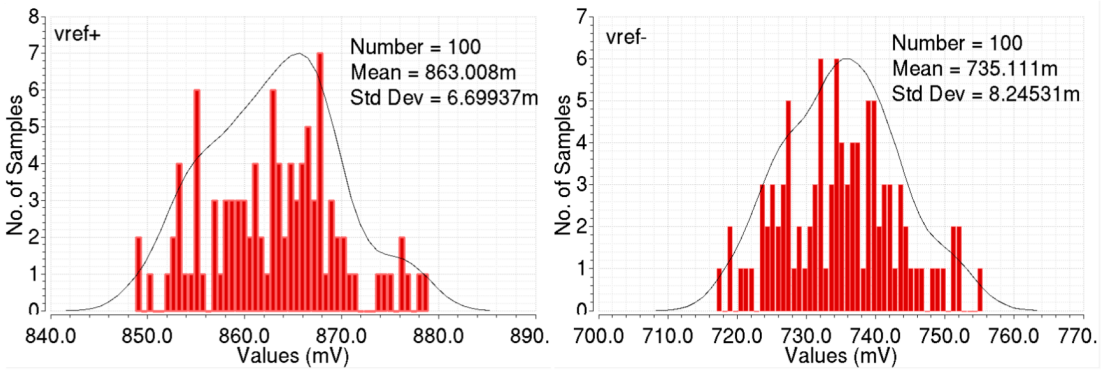
3.2.5 1.5-b reference resistive ladder

The 1.5-b subADC utilizes two distinct resistive ladders, as shown in Fig. 3.2, to generate the reference voltages [2]. This design effectively reduces the coupling effects caused by kick back [2].



(a) (b)

Figure 3.6 : (a) Offset voltage variation of the clocked comparator [2], (b) Process and mismatch variation of the Cmim capacitor, 625 fF [2].



(a) (b)

Figure 3.7 : (a) Process and mismatch variation of Vref+ [2], (b) Process and mismatch variation of Vref- [2].

3.3 Simulation Results

Cadence Spectre transient noise in this study [2]. Furthermore, the simulations are conducted to perform RC extraction using Quantus Extraction in Cadence. The test bench in [17] simulates the offset of the clocked comparator. Figure 3.6 illustrates the dynamic offset variations of the clocked comparator and the process and mismatch variation of Cmim. Figure 3.7 provides information on the process and mismatch variation of the resistive ladders. The boosted inverse clock signals reach a voltage of 1.92V, while the differential input signals are seen in Fig. 3.8 [2].

The digital outputs of the 1.5-b subADC are shown in Fig. 3.9 [2]. The performance of the bootstrap switch in terms of linearity is shown in Fig. 3.10. The use of symmetrical clock drive enhances the SFDR by 6 dB at an input frequency of 52 MHz.

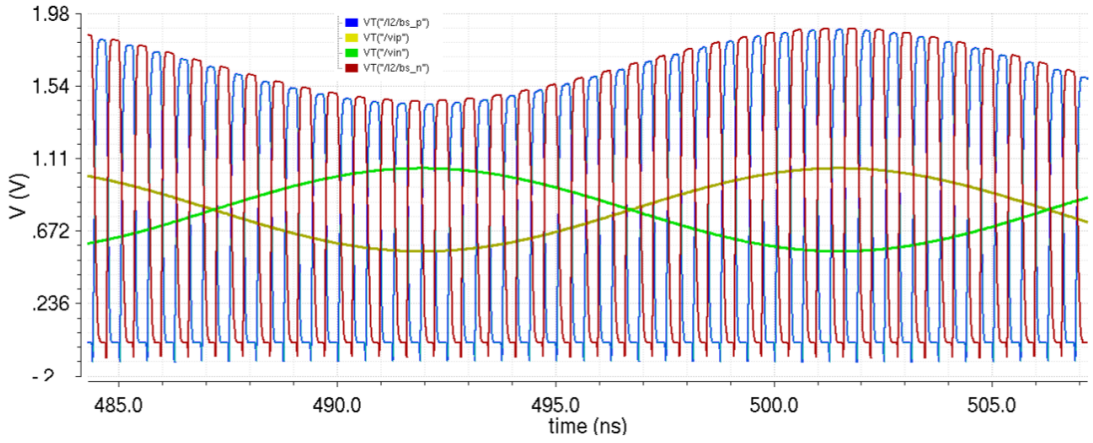


Figure 3.8 : Negative and positive input signals at 50 MHz, bootstrap voltages bs_p and bs_n [2].

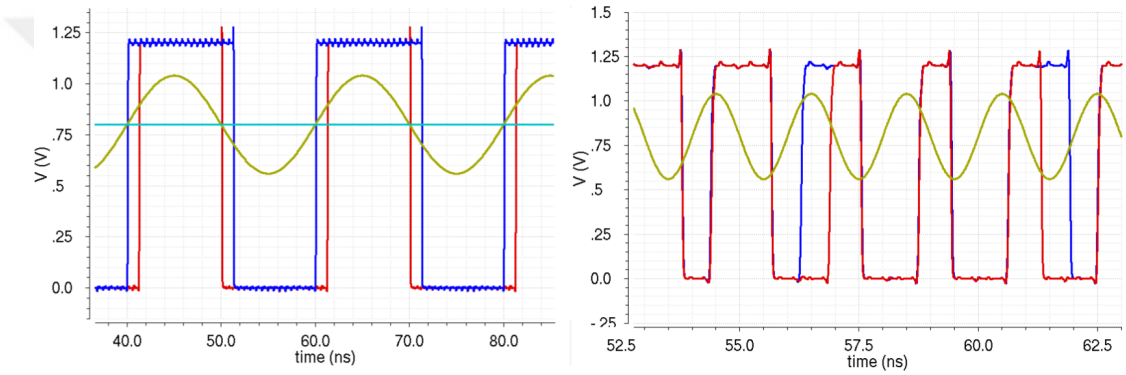


Figure 3.9 : (a) b0 (blue), b1 (red), vip (yellow) at 52 MHz [2], (b) b0 (blue), b1 (red), vip (yellow) at 480 MHz [2].

Additionally, the use of coupling capacitor C_{dm} improves the SFDR by 1 dB when the input frequency is 780 MHz. The performance of the 1.5-b front-end sub-ADC is presented in Table 3.1 [2].

The sub-ADC being suggested operates at a supply of 1.2 V and consumes a total of 19.2 mA. At a supply of 1.6 V, it consumes 7.2 mA. It occupies a silicon area of 156 μm$\times$ 205 μm and is implemented using a SiGe BiCMOS 0.13 μm process. The sub-ADC is incorporated into the pipeline ADC.

Table 3.1 : Performance of the 1.5-b front-end subADC [2]

Clocked comparator	Dynamic input offset voltage (σ)	3.414 mV
	Delay	92 ps
	Silicon area	28 μm $\times$ 30 μm
	Current consumption @ 1.2 V	1.6 mA
Bootstrap switch	SNDR/SFDR 52 MHz	88 dB/70 dB
	@1.6 GS/s 780 MHz	66 dB/49 dB
	Silicon area	48 μm $\times$ 78 μm
	Current consumption @ 1.2 V	1.8 mA
Clock tree logics	Current consumption @ 1.6 V/1.2 V	7.2 mA/4 mA
Resistive ladders	Current consumption @ 1.2 V	2 2.4 mA
1.5-b front-end subADC	Silicon area	156 μm $\times$ 205 μm
	Current consumption @ 1.6 V/1.2 V	7.2 mA/4 mA

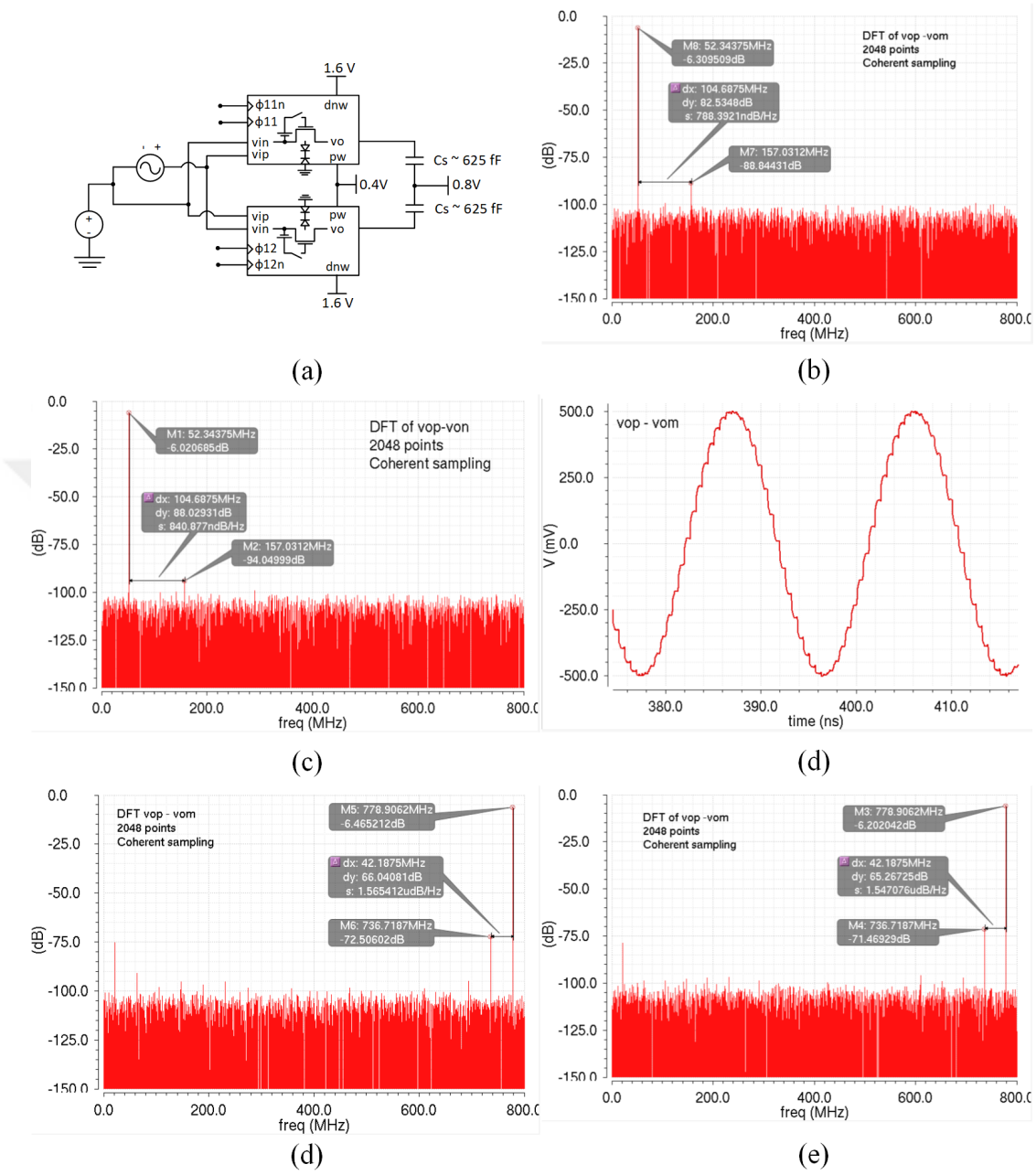


Figure 3.10 : (a) Test bench for bootstrap switches [2], (b) Without symmetrical clock drive Vodiff freq. spectrum for 52.34375 MHz input sinusoidal 1 $Vin_{diff,p-p}$ [2], (c) With symmetrical clock drive Vodiff freq. spectrum for 52.34375 MHz input sinusoidal 1 $Vin_{diff,p-p}$ [2], (d) Vodiff transient output signal for 52.34375 MHz input sinusoidal [2], (e) With Cdm Vodiff freq. spectrum for 778.9062 MHz input sinusoidal 1 $Vin_{diff,p-p}$ [2], (e) Without Cdm Vodiff freq. spectrum for 778.9062 MHz input sinusoidal 1 $Vin_{diff,p-p}$ [2].

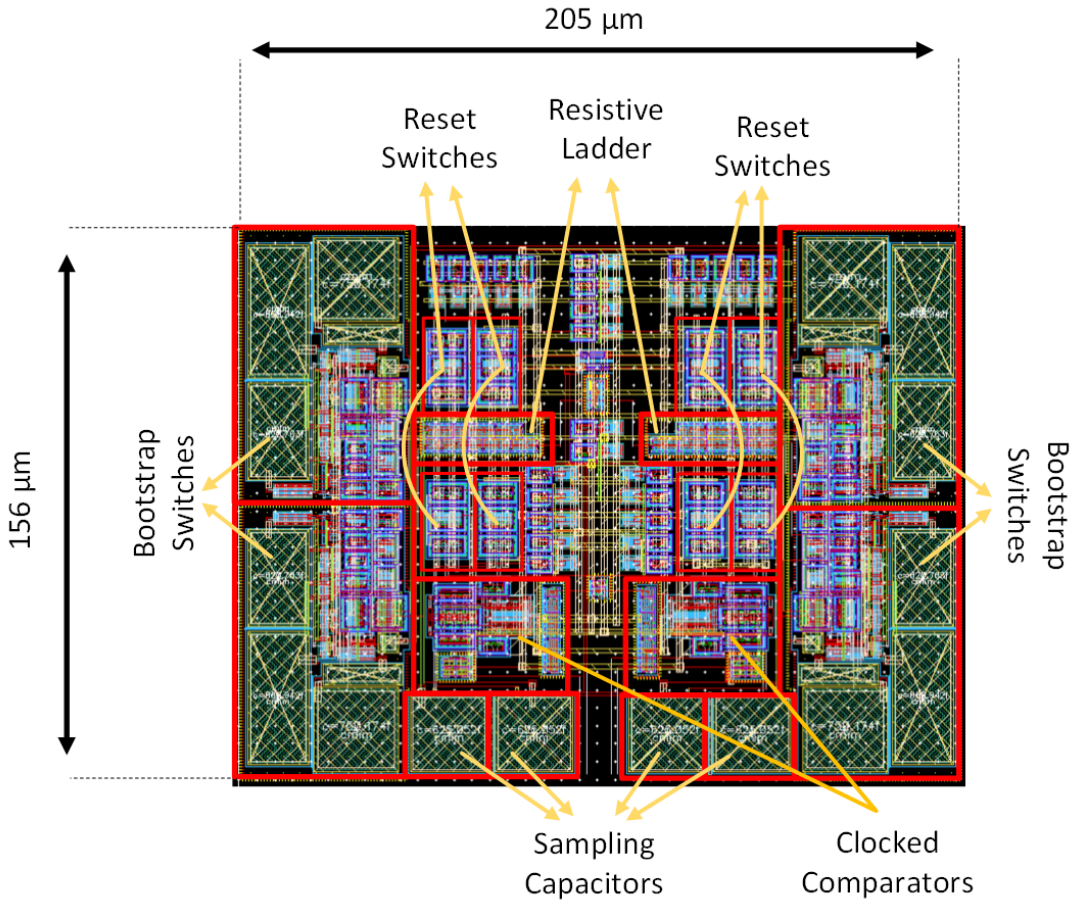


Figure 3.11 : Layout view of the 1.5-b subADC with 156 μm$\times$ 205 μm [2].

4. A NOVEL BiCMOS RESIDUE AMPLIFIER

In chapter 4, a novel BiCMOS residue amplifier is presented [6]. The novelty upon the proposed amplifier topology is protected at TPTO.

4.1 Purpose

A residue amplifier, also known as ResAmp, is an essential element in pipelined ADC [18–21]. The primary purpose of this system is to transmit discrete-time signals within a specific range from one stage of the pipeline to the next. In order to effectively fulfill its intended function, the ResAmp must adhere to specified requirements regarding noise, linearity, and gain accuracy. Designers have primarily tackled these difficulties by utilizing analog methods that involve a precise operational amplifier (op-amp) in a closed-loop (CL) design [18–20]. The high loop gain in this setup suppresses static gain errors and nonlinearities. However, the circuit complexity associated with such an approach degrades noise performance. Furthermore, the need for a wide bandwidth is necessary in order to minimize dynamic errors and get the requisite level of gain accuracy, rendering conventional ResAmp designs unfeasible for several applications. One way around this problem is to use digital correction techniques that can be applied in addition to or instead of the analog feedback loop. These require extra circuitry, but may payoff in terms of simplicity and improved performance. Another possibility is to use a hybrid approach that employs both analog and digital feedback loops. In any case, it is important to carefully consider the trade-offs involved in order to arrive at an optimal design.

The ResAmp should compromised with the following criteria [22–32]: The amplifier linearity is a key performance parameter in a BiCMOS pipelined ADC. In order to achieve high amplifier linearity, it is essential to design the amplifier such that it has high input impedance and low noise. One of the main challenges in designing a residue amplifier is that the input impedance of BJT decreases with the increase of collector current. This can eventually cause charge loss in switched capacitor

operation. Therefore, it is important to design the amplifier such that the input impedance is purely capacitive. Another criterion for designing the amplifier is to ensure that the amplifier should have a high unity-gain bandwidth (UGBW). NMOS and PMOS transistors exhibit 80 GHz of f_T and 30 GHz of f_T, respectively. If one of those types of transistors are deployed as input transistors for common source structure, achieving a UGBW greater than 6 GHz is difficult in considering C_L. This is necessary in order to avoid signal distortion. Finally, the noise performance of the amplifier is also an important consideration. In general, it is desirable to have an amplifier with low noise in order to achieve high overall ADC performance [22–32].

4.2 Previous Topologies for Residue Amplifier

Open-loop (OL) or integrating amplifiers have demonstrated superior power dissipation efficiency in relation to other amplifier topologies, while maintaining comparable noise performance [22], [23], [24–27]. Some examples include ring amplifiers [28], OL or integrating amplifiers [22], class-AB amplifiers [29], zero-crossing detectors [30], capacitive charge pumps [31], pulsed bucket brigades [33], and time-based amplification [32]. Despite nonlinearity of OL amplifiers, which can be mitigated through digital calibration, they remain a popular choice in pipelined ADCs due to their low power consumption.

As depicted in Fig. 4.1a, the negative feedback amplifier is a type of amplifier that uses negative feedback to stabilize the gain of the amplifier. Negative feedback is a process in which a portion of the output signal is fed back to the input, in order to cancel out any distortion. The use of negative feedback reduces the dependence of amplifier gain on transistor parameters or variation in the supply voltage. It also helps to reduce non-linear distortion levels in large signal amplifiers. In addition, negative feedback increases the input impedance or resistance of an amplifier, while decreasing the output impedance or resistance. As a result, negative feedback amplifiers are able to maintain a more linear output signal, even when there is a small input signal. This makes negative feedback amplifiers an essential tool in many scientific and academic applications.

In Fig. 4.2, a two stage amplifier is illustrated [34]. The source followers were used at the input to reduce the input capacitance and increase the feedback factor in a CL

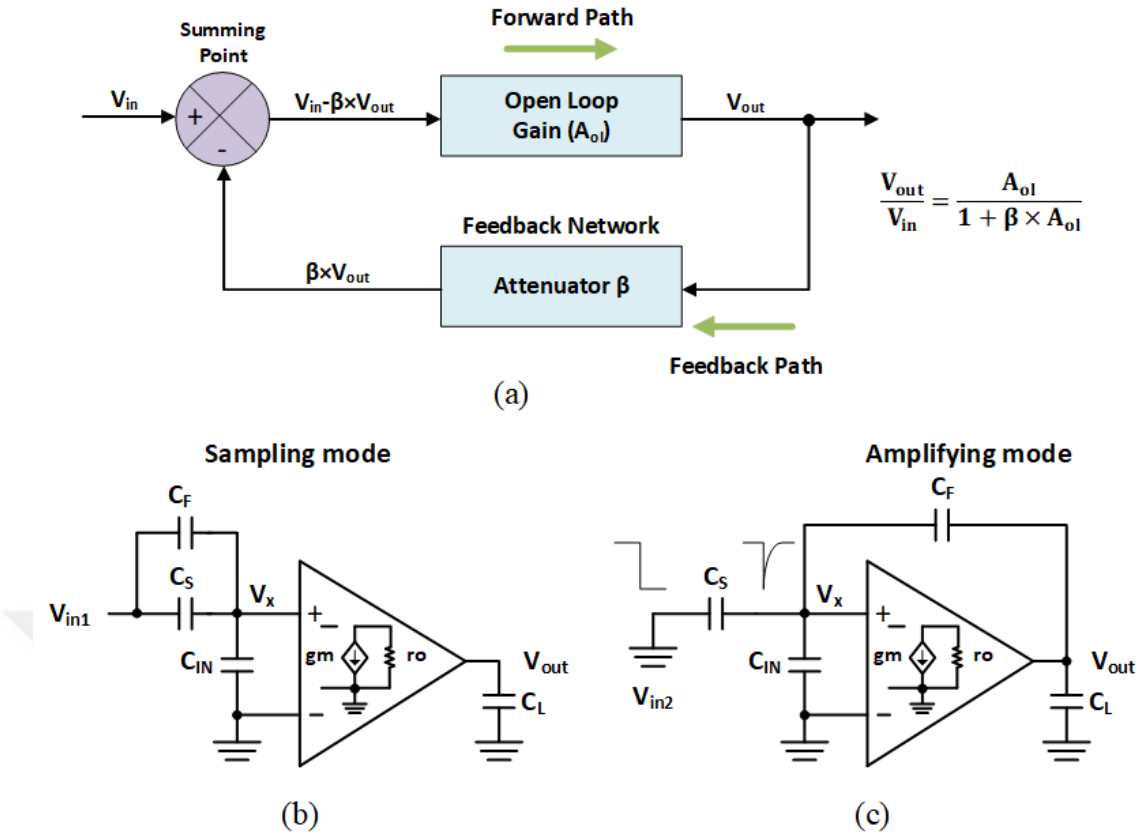


Figure 4.1 : (a) Negative feedback, (b) sampling mode for a charge amplifier, (c) amplifying mode for a charge amplifier.

configuration [34]. The input capacitance at the summing node, is a dominant factor, which limits accuracy and settling of the ResAmp, as depicted Fig. 4.1c.

4.3 Design of Residue Amplifier

In this thesis, the proposed ResAmp has two stages as depicted in Fig. 4.3 [6]. The first stage is a common collector buffer (CCB) circuit. The input transistors of the CCBs are HV-BJTs. The second stage is a fully differential telescopic operational transconductance (OTA), having LV-BJT input devices. Those input transistors are cascoded by LV-BJTs to boost up the gain and reduce the Miller effect. At the upper side, PMOS cascode transistors are used, and additionaly, gain boosting technique is applied to augment the overall voltage gain. The gain boosting amplifier is depicted in Fig. 4.5.

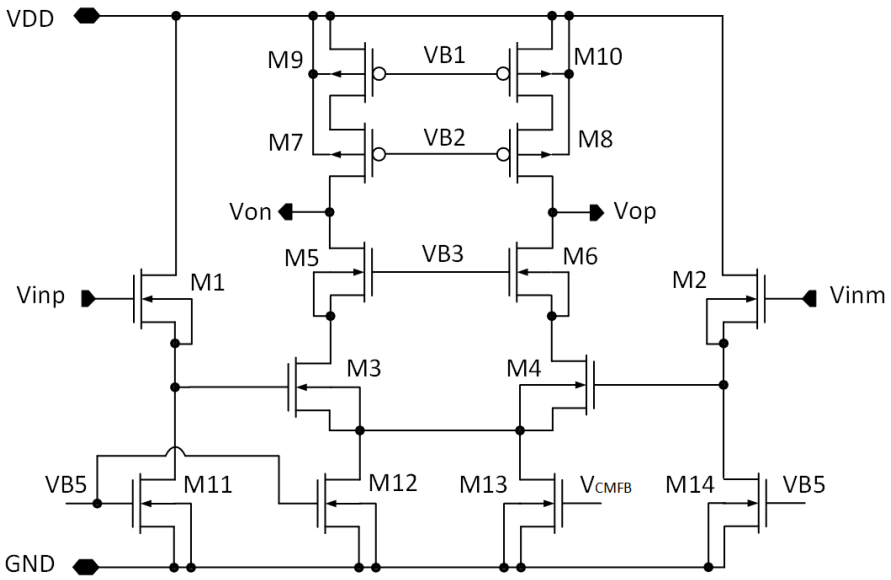


Figure 4.2 : A two stage residue amplifier in [34].

4.3.1 Motivation for the common collector buffer

The ResAmp is composed of two cascaded stages. The first stage is a CCB circuit, and the second stage is a telescopic OTA. The CCB is deployed mainly for two reasons:

- Minimizing the input capacitance (C_{IN}) of the ResAmp.
- Reducing the amount of the base currents ($I_{B1,leak}$) and ($I_{B2,leak}$) of the B1 and B2 BJTs in Fig. 4.4.

Based on charge redistribution view in Fig. 4.1b and Fig. 4.1c, the static transfer function of the ResAmp in the amplifying mode can be derived as follows:

$$V_{out} \approx \left[V_{in1} - V_{in2} \times \left(\frac{C_S + C_{IN}}{C_S + C_F}\right)\right] \times \left(1 + \frac{C_S}{C_F}\right) \times \left(1 - \frac{1}{A_{ol} \times \beta}\right) \tag{4.1}$$

$$\beta \approx \frac{C_F}{C_S + C_F + C_{IN}} \tag{4.2}$$

Above equation includes, parasitic input capacitor (C_{IN}), the open loop gain of the ResAmp (A_{ol}). β is the feedback factor. As understood from (4.2), C_{IN}, as a first order parameter, affects the feedback factor, thus, close-loop gain, and exhibits itself as gain error.

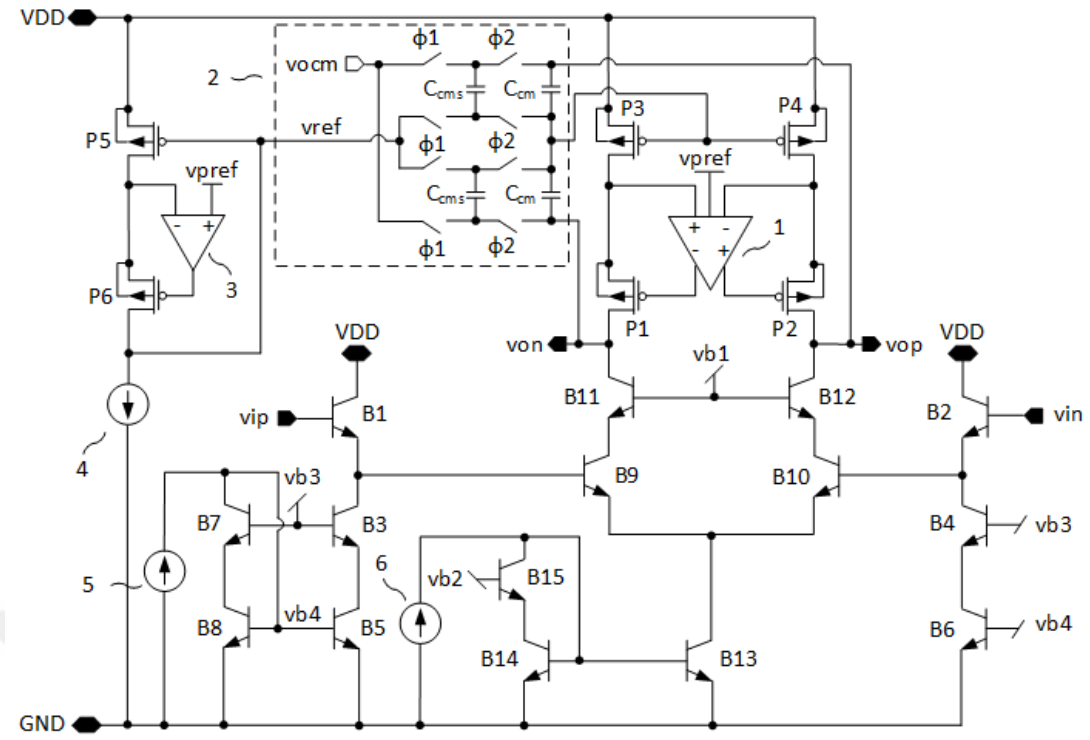


Figure 4.3 : The proposed two stage ResAmp.

Due to the leakage currents ($I_{B1,leak}$ and $I_{B2,leak}$) into the input pairs of the CCB stages, the held signal stored at C_S and C_F is not constant over time. For instance, $I_{B1,leak}$ is composed of DC and AC currents:

$$I_{B1,leak} = I_{B1} + i_{B1,leak}, \tag{4.3}$$

where I_{B1} is the DC base current of B1, and $i_{B1,leak}$ is the AC current flowing into the base terminal of B1. Fig. 4.4a illustrates the situation with leakage currents. The decreased held voltage at the end of one amplifying period T_{A-end} with respect to the value at the moment $T_{A-begin}$ can be expressed as [35]:

$$V_{C_X} \times T_{A-end} = V_{C_X} \times T_{A-begin} \times \left(1 - e^{\frac{-1}{R_P \times C_X}}\right) - \frac{I_{B1,leak} \times T_{A-end}}{C_X}, \tag{4.4}$$

where R_P is the input resistance of the CCB and C_X is the equivalent capacitance at node X in Fig. 4.4a. In this design, the discharging current was minimized by using CCBs in the first stage. As such the input resistance of the CCB, RP, as seen by node X, is improved by a factor of

$$R_P \approx (h_{fe,1} + 1) \times r_\pi, \tag{4.5}$$

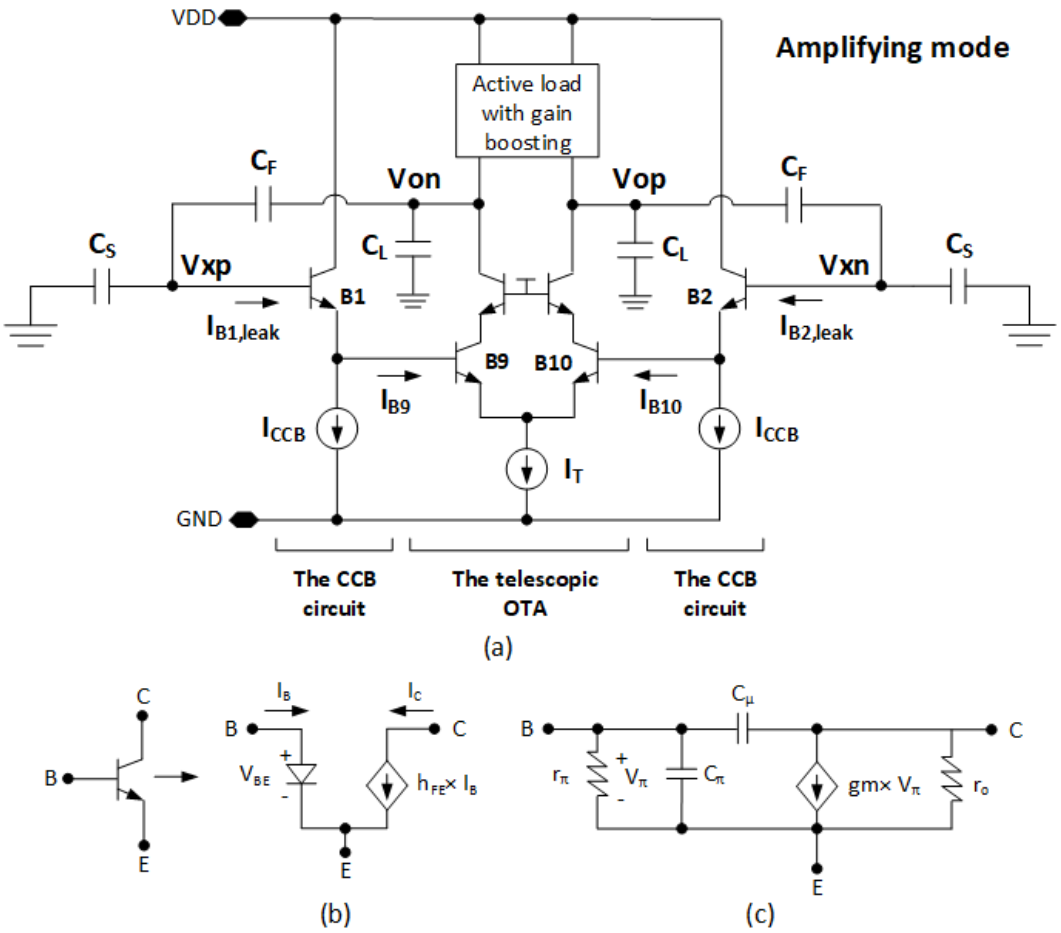


Figure 4.4 : (a) The leaking current mechanism of the proposed residue amplifier, (b) Large-signal model of a BJT, (c) Small-signal high frequency model of a BJT

where h_{fe} is the small-signal current gain, and r_π is the input resistance as illustrated in the small-signal model of a BJT in Fig. 4.4c. Since the second stage is responsible to drive heavily C_L and capacitive feedback network, it needs tens of mA as biasing current. For the proposed ResAmp, regarding the large-signal model of a BJT in Fig. 4.4b, the relation between I_T and I_{CCB} is given as:

$$I_{CCB} < \frac{I_T}{15}. \tag{4.6}$$

I_{B1} is the DC base current of B1, and can be expressed in terms of $h_{FE,1}$, $h_{FE,9}$, I_T and I_{CCB}:

$$I_{B1} < \frac{1}{h_{FE,1}+1} \times \left(\frac{I_T}{2 \times (h_{FE,9}+1)} + I_{CCB} \right). \tag{4.7}$$

where $h_{FE,1}$ and $h_{FE,9}$ are the large signal current gain of B1 and B9, respectively. Consequently, $I_{B1,leak}$ and $I_{B2,leak}$ of the ResAmp are lessened to mitigate charge loss

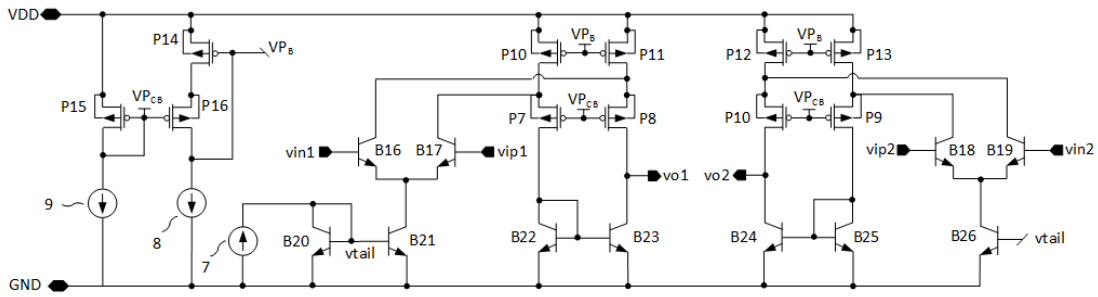


Figure 4.5 : The proposed wide-band folded cascode gain boosting amplifier.

by employing CCBs. The amount of $I_{B1,leak}$ (or $I_{B2,leak}$) is obtained as several hundreds of nA in the simulations.

The common mode input voltage (V_{ICM}) of the ResAmp is eventually increased with the usage of CCBs and can be expressed as

$$V_{ICM} \geqslant V_{th,B1,2} + V_{th,B9,10} + V_{CE,B13}. \tag{4.8}$$

Regarding $V_{th,B1,2}$ and $V_{th,B9,10}$, V_{ICM} is chosen around 1.9V to operate BJTs in active region. Another concern for the input BJTs is voltage violation. Since the base terminals of the B1 and B2 are biased at 1.9V, those transistors could remain under voltage stress, that may damage the device, irreversibly. Thereof, HV-BJTs in UMC 0.13 μm were deployed as input transistors for the ResAmp.

Regarding the small-signal AC model of a BJT in 4.4c, the DC output resistance of the CCB is expressed as:

$$\begin{aligned} r_{o,CCB} \approx [(1 + g_{m,B1,2} \times (r_{o,B5,6} || r_{\pi,B3,4})) \times r_{o,B3,4} + r_{o,B5,6} || r_{\pi,B3,4}] \\ || \frac{1}{g_{m,B1,2}} || r_{o,B1,2} || (r_{\pi,B9,10} + (\beta_{B1,2} \times +1) \times R_T). \end{aligned} \tag{4.9}$$

where R_T represents the resistance at the output of the tail current source B13.. As understood from (4.9), the input resistance at one of the input transistor of the second stage is also included. Hence, the DC voltage gain of CCB is obtained as

$$A_{v,CCB} = g_{m,B1,2} \times r_{o,CCB}. \tag{4.10}$$

4.3.2 Motivation for the fully differential telescopic OTA

A fully differential telescoping operational transconductance amplifier (FDT-OTA) is used for the second stage of the ResAmp to provide broad bandwidth, strong phase

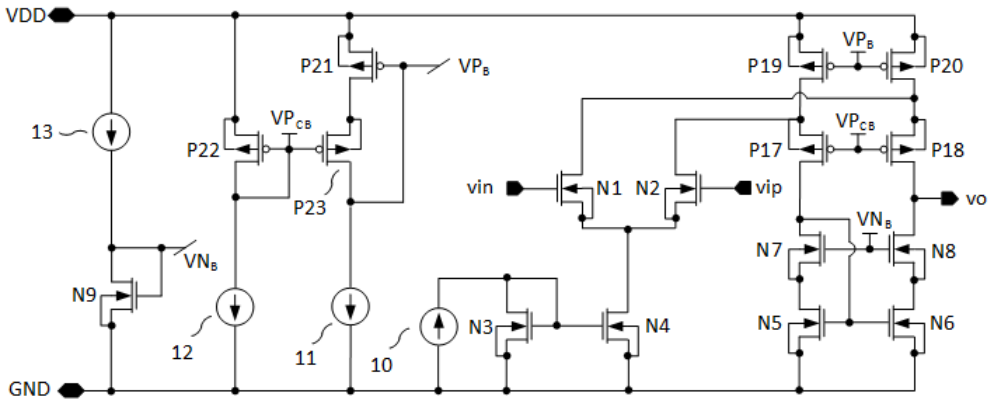


Figure 4.6 : The proposed folded cascode amplifier for active current mirror.

margin, and low noise, as shown in Fig. 4.3. High amplifier gain necessary for 11-b linearity is achieved by a telescoping cascode construction aided by gain boosting [19, 36]. The gain-boosting circuit utilizes LV-BJT for its input devices to enhance the bandwidth.

The output resistance of FDT-OTA can be given as

$$r_{o,FDT-OTA} \approx [(1 + g_{m,B9,10} \times (r_{o,B9,10} || r_{\pi,B11,12})) \times r_{o,B11,12} + r_{o,B9,10} || r_{\pi,B11,12}] \\ || (A_{GB} \times g_{m,P1,2} \times r_{o,P1,2} \times r_{o,P3,4}). \tag{4.11}$$

where A_{GB} is the DC voltage gain of the gain boosting amplifier as depicted in Fig. 4.5. Concerning (4.11), the DC voltage gain of the FDT-OTA is expressed as

$$A_{v,FDT-OTA} = -g_{m,B9,10} \times r_{o,FDT-OTA}. \tag{4.12}$$

Concerning (4.10) and (4.12), the overall DC gain of the proposed two stage ResAmp can be given as

$$A_{v,ResAmp} = -g_{m,B9,10} \times r_{o,FDT-OTA} \times g_{m,B1,2} \times r_{o,CCB}. \tag{4.13}$$

4.3.3 Switched mode common mode feedback

By employing negative feedback, an operational amplifier configuration known as a switched-mode common-mode feedback (SM-CMFB) circuit determines the common-mode voltage at the amplifier outputs (V_{OCM}), compares it to a known reference voltage, and subsequently adjusts the V_{OCM} to match the reference voltage [37]. This feedback loop serves as a mechanism for detecting and correcting common-mode voltage errors in amplifier circuits [37]. .

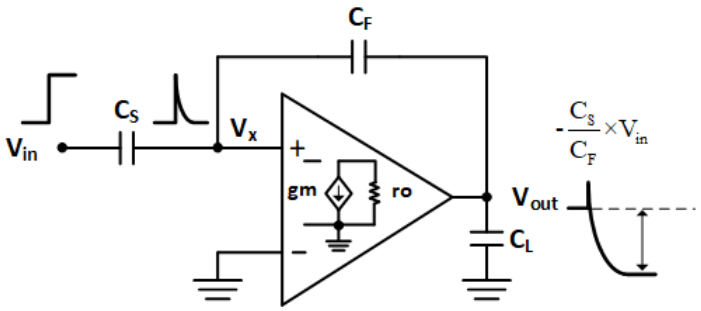


Figure 4.7 : The charge Amp_{cl}.

The SM methodology offers a number of benefits in comparison to the continuous-time approach [37]. Firstly, due to the feedback loop being intermittently activated rather than constantly active, the power consumption of the SM-CMFB circuit is considerably lower when compared to that of a continuous-time CMFB circuit. Secondly, as the feedback loop is discrete-time, it does not possess any poles, thereby eliminating the need for compensation to ensure stability. Finally, the input signal range of the common-mode detector is far greater than the output voltage swing of the amplifier, resulting in SM-CMFB circuits being less vulnerable to linearity issues than their continuous-time equivalents [37].

Overall, SM-CMFB circuits are a more efficient and robust solution for detecting and correcting common-mode voltage errors in amplifiers [37].

In the SM-CMFB, the feedback factor is determined by the proportion of C_{cm} to the parasitic gate capacitance, and this factor ought be no less than 1/2. The SC-CMFB technique has a disadvantage in that C_{cm} directly loads the ResAmp, resulting in a slight slow down. Additionally, the V_{OCM} experiences an offset due to charge injection and clock feedthrough from the switches. Nevertheless, this approach allows for a broad range of input and output voltages, rendering it highly applicable in various amplifier applications.

4.3.4 Settling behaviour

As depicted in Fig. 4.7, negative feedback amplifiers are frequently utilized to render the gain more impervious to PVT variations [21, 33, 38, 39]. In this configuration, the feedback network recirculates the amplifier's output to its input. A virtual ground results from the boostering of the output signal at the input nodes when the amplifiers have a high intrinsic gain, which eliminates any signal at those nodes. Feedback

factor, expressed as a ratio of passive components, dictates the A_{cl} in its entirety. This mitigates the effects of environmental variables such as temperature drift, process fluctuations, and process instability on the amplifier [21, 33, 38, 39].

In the circuits of the negative feedback Amp, illustrated in Fig. 4.7, the feedback loop performs the function of comparing the output signal with the input signal [21, 33, 38, 39]. This negative feedback guarantees the stability of the entire output voltage, $V_{out}(t)$, and could be precisely computed by employing the subsequent sequence of equations [38, 39]:

$$V_x(t) = V_{in}(t) - \beta \times V_{out}(t) \tag{4.14}$$

$$I_o(t) = g_m \times V_x(t) = C_L \times \frac{dV_{out}}{dt} + g_o \times V_{out}(t) \tag{4.15}$$

where $V_x(t)$ represents the voltage signal located at the virtual ground inputs of the Amp, $I_o(t)$ corresponds to the output current that is produced by the input transconductance, gm, and g_o donates to the output transconductance of the Amp_{ol}. This consequently results in a A_{ol}, equivalent to g_m/g_o. In the event that the input signal is once again deemed to be a step function with an amplitude of V_{in}, then, by utilizing Laplace transform, (4.15) can be employed to determine $V_{out}(t)$, as stated by [38, 39].

$$V_{out}(t) = \frac{A_{ol}}{1 + A_{ol} \times \beta} \times (1 - e^{-t/\tau_f}),\ t \geq 0 \tag{4.16}$$

where τ_f is the loop time-constant and can be expressed as

$$\tau_f = \frac{\tau}{1 + A_{ol} \times \beta}. \tag{4.17}$$

In 4.17, τ is the time constant of the $ResAmp_{ol}$ [38, 39]. It is defined as the product of $(r_o \times C_L)$. When the product of $A_{ol} \times \beta \gg 1$ is much greater than 1, the A_{cl} of ResAmp settles to $1/\beta$, which is not affected by the values of ResAmp's g_m and r_o. In addition to the output voltage, the virtual ground signal, $V_X(t)$, is also a significant indicator of the settling behavior in a Amp_{cl}. The expression for $V_X(t)$ can be obtained by combining (4.16) and (4.17), as stated in the reference by [38, 39]:

$$V_x(t) = V_{in}(t) - \beta \times V_{out}(t) = \frac{1 + A_{ol} \times \beta \times e^{-t/\tau_f}}{1 + A_{ol} \times \beta} \tag{4.18}$$

As evidenced by (4.18), the virtual ground signal undergoes a decay over time at a rate of 8.6 dB per settling, ultimately arriving at a residual value of $V_{in}/(1 + A_o)$. This

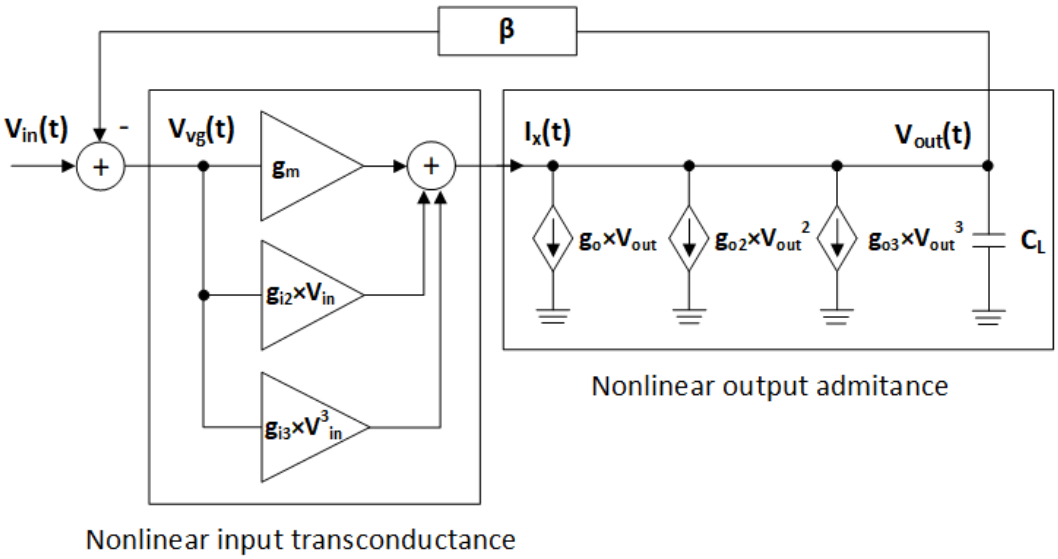


Figure 4.8 : A distortion model for the ResAmp

decay rate is exclusively a consequence of first-order exponential settling, which is a direct outcome of the amplifier's single-pole nature.

4.3.5 Gain error

To determine the gain error over time, $\varepsilon_g(t)$, of the Amp_{cl} depicted in Figure 4.4, we may use equation (4.18) with the desired gain set as $1/\beta$ [38, 39]:

$$\varepsilon_g(t) = \frac{1}{\beta} - \frac{A_{ol}}{1 + A_{ol} \times \beta} \times (1 - e^{-t/\tau_f}),\ t \geq 0 \tag{4.19}$$

The aforementioned expression for the gain error comprises both a static and a dynamic component [21, 33, 38, 39]. The static aspect pertains to the remaining steady-state gain error brought about by the limited loop gain. On the other hand, the dynamic component of the gain error delineates the initial phase of amplification, wherein the amplifier is still undergoing settlement at a pace of $8.6\text{dB}/\tau_f$.

In order to clarify the bandwidth and loop gain specifications for a ResAmp_{cl} in an ADC stage, (4.19) can be utilized to represent the required resolution as follows [38, 39]:

$$\text{Relative gain error} = \frac{1 + A_{ol} \times \beta \times e^{-t/\tau_f}}{1 + A_{ol} \times \beta} \leqslant \frac{1}{2^{1+r_{i+1}}} \tag{4.20}$$

where r_{i+1} is the combined ADC resolution remaining after the i-th stage. Therefore, the calculation for the minimal required DC loop gain in a totally settled amplifier is

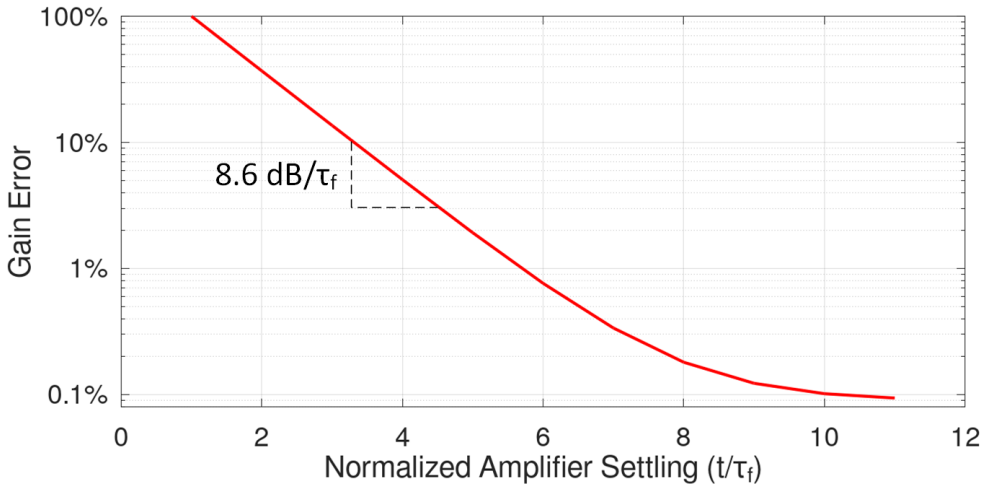


Figure 4.9 : Settling behaviour of gain error in CL amplifier

as follows [21, 38, 39]:

$$\frac{1}{1+A_{ol}\times\beta} \leqslant \frac{1}{2^{1+r_{i+1}}} \text{ or}$$
$$A_{ol} \geq \frac{2^{1+r_{i+1}}}{\beta} \tag{4.21}$$

To provide further context, it is critical that the ResAmp, which possesses a 2x gain, achieves a minimum relative accuracy of $1/2^{11}$ for the initial level of an 11-b pipelined ADC featuring a 1-bit per stage configuration. To achieve this without calibration, the amplifier must possess an A_{ol} of more than 8192 or 78 dB.

In order for an amplifier to attain the desired gain with the necessary precision within a specific amplification duration, it is imperative that the amplifier possess a certain bandwidth, in addition to sufficient DC gain [21, 38, 39]. This requisite bandwidth can be calculated by utilizing (4.19) and assuming that the op-amp has an adequately high DC gain ($A_{ol}\times\beta$). Consequently, for an amplification duration of t_s, (4.19) can be simplified, as [21]:

$$e^{-t_s/\tau_f} \leqslant \frac{1}{2^{1+r_{i+1}}} \tag{4.22}$$

or,

$$t_s \geqslant (1+r_{i+1})\times\tau_f\times\ln 2 \tag{4.23}$$

By considering t_s to be equivalent to half of the ADC clock period, one can express the Amp_{cl}'s 3-dB bandwidth as

$$f_{-3dB} \geqslant \frac{(1+r_{i+1})\times f_s\times\ln 2}{\pi} \tag{4.24}$$

or,

$$f_u \geqslant \frac{(1+r_{i+1}) \times f_s \times \ln 2}{\pi \times \beta} \tag{4.25}$$

where f_u is the unity-gain frequency of the ResAmp and f_s is the ADC sampling frequency.

If one were to operate the 11-b pipelined ADC from the previous design example at a speed of 1.6 GS/s, it would be necessary for the amplifier in the first stage to possess a unity-gain bandwidth of approximately 6.8 GHz in order to completely stabilize to the desired gain with the necessary precision.

4.3.6 Noise

If the noise bandwidth is restricted exclusively by the parameter denoted as C_L, then the noise power with reference to the output at a particular moment t can be ascertained by employing the analysis outlined in [40]:

$$\overline{v_{out,n}^2(t)} = \frac{k \times T}{C_L} \times \frac{A_{ol}}{1+\beta \times A_{ol}} \times (1 - e^{-(2\times t)/\tau_f}) + \frac{k \times T}{C_L} \times e^{-(2\times t)/\tau_f} \tag{4.26}$$

In the previous equation, A_{ol} refers to the A_o of the amplifier, while β is the feedback factor, which may be expressed as $C_F/(C_S + C_F)$. It should be noted that, similar to the scenario of an OL amplifier, the second term in equation (4.26) is a consequence of the noise power of the C_L voltage at t = 0. Assuming that this noise power is completely reset, it can be calculated as $(k \times T)/C_L$. By taking into account the condition $A_{ol} \times \beta \gg 1$, we are able to derive the following expression [21, 38, 39]:

$$\begin{aligned} \overline{v_{out,n}^2(t)} &\approx \frac{k \times T}{C_L} \times \frac{1}{\beta} \times \left(1 - (1-\beta) \times e^{-(2\times t)/\tau_f)}\right) \\ &\approx \frac{k \times T \times (C_S + C_F)}{C_F/C_L} \times \left(1 - \frac{C_S}{C_S + C_F} \times e^{-(2\times t)/\tau_f}\right) \end{aligned} \tag{4.27}$$

As the output of the amplifier invariably exceeds zero during its development from the primary feed forward impulse to its ultimate magnitude, the output power at first declines to zero before increasing at an exponential rate [21, 38, 39]. Conversely, the noise power experienced at the output undergoes a relatively insignificant alteration during the amplifier's stabilization process [21, 38, 39].

4.3.7 Distortion

Earlier studies have demonstrated that the utilization of feedback leads to the desensitization of the overall amplifier gain in relation to the intrinsic gain of the amplifier, with a proportionate factor of $1+\beta \times A_{ol}$ [21, 38, 41]. Consequently, any input-dependent fluctuations in the A_{cl} caused by nonlinear appliance in the amplifier are additionally suppressed by the loop-gain. This capability to suppress amplifier distortion is a fundamental advantage of negative feedback and has established it as a vital technique in the design of high-precision amplifiers [21, 38, 39].

The extensive documentation in literature has established the mitigating impact of negative feedback on harmonic distortion [21, 38, 39, 41, 42]. However, the majority of these studies use methods that evaluate the distortion in the frequency domain. This means that they focus on analysing the amplifier's performance after it has reached a stable state, and do not consider its behavior during the early settling period. In order to successfully create and improve discrete-time amplifiers for high-speed applications, it is crucial to perceive the development of the negative feedback impact as the amplifier stabilizes [21, 38, 39].

A nonlinear amplifier with negative-feedback can be assessed through employment of the non-linear amplifier model depicted in Figure 3.4, by integrating it into the CL configuration as demonstrated in Fig.4.9. By commencing with the nonlinear input transconductance, (3.12) can be reformulated to incorporate the gm nonlinearity, in the manner outlined below [21, 38, 39]:

$$\begin{aligned} V_{vg}(t) &= V_{in}(t) - \beta \times V_{out}(t) \\ I_x(t) &= gm \times V_{vg}(t) + g_{i2} \times V_{vg}(t) + g_{i3} \times V_{vg}(t) \\ I_x(t) &= C_L \times \frac{dV_{out}(t)}{dt} + g_o \times V_{out}(t) \end{aligned} \tag{4.28}$$

It is important to observe, as indicated in equation(4.28), that the correlation between $I_x(t)$ and $V_{vg}(t)$ [21, 38, 39]. This is due to the fact that the sole memory element present within the circuit is related with the C_L. Utilizing certain simplifications to solve equation (4.28), the input HD_2 component, $V^2_{out,in}(t)$, can be computed as [21,

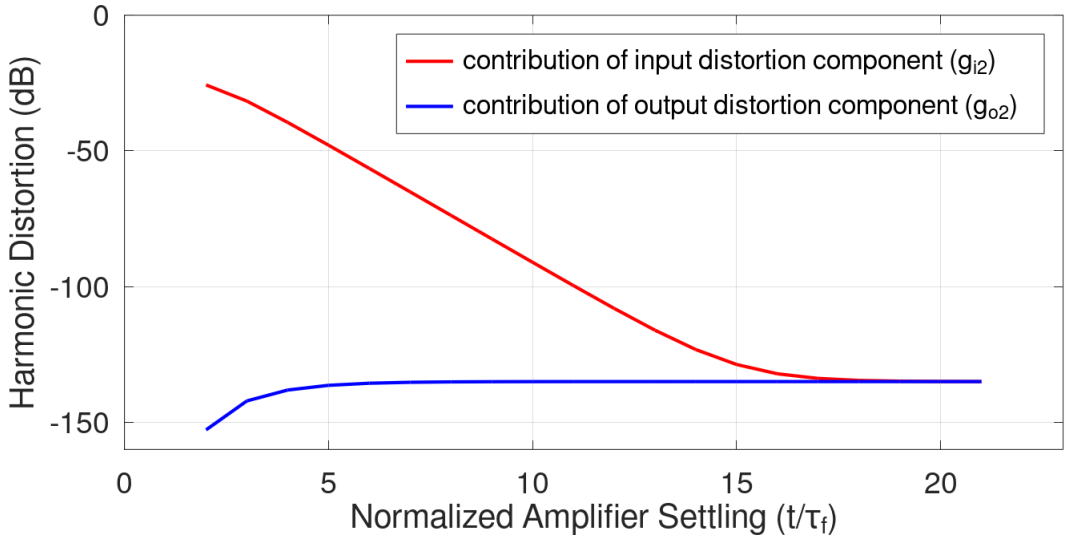


Figure 4.10 : Analysis of the convergence of harmonic distortion in CL amplifiers.

38, 39]:

$$V^2_{out,in}(t) = \frac{g_{i2}}{g_o \times (1 + A_{ol} \times \beta)^3} \times V^2_{in} \times \left((1 - e^{-t/\tau_f}) + (A_{ol} \times \beta)^2 \times e^{-t/\tau_f} \times (1 - e^{-t/\tau_f}) + 2 \times A_{ol} \times \beta \times e^{-t/\tau_f} \times \left(\frac{t}{\tau_f} \right) \right) \tag{4.29}$$

This is an illustration of the transient behavior of the HD_2 component, which arises due to the nonlinear input g_m, in response to a step input at $t = 0$. Once the initial settling has taken place, the distortion component moves towards a stable-state value of $\frac{g_{i2}}{g_o \times (1 + A_{ol} \times \beta)}$, which is consistent with the findings in [38]. Similarly, the input HD_3 component, $V^3_{out,in}(t)$, can be expressed in a comparable manner [21].

$$V^3_{out,in}(t) = \frac{g_{i3}}{g_o \times (1 + A_{ol} \times \beta)^4} \times V^3_{in} \times \left((1 - e^{-t/\tau_f}) + 3 \times (A_{ol} \times \beta)^2 \times e^{-t/\tau_f} \times (1 - e^{-t/\tau_f}) + \frac{(A_{ol} \times \beta)^3}{2} \times e^{-t/\tau_f} \times \left(1 - e^{(-2 \times t)/\tau_f} \right) + 3 \times A_{ol} \times \beta \times e^{-t/\tau_f} \times \left(\frac{t}{\tau_f} \right) \right) \tag{4.30}$$

It is observable from (4.32) that the HD_3 constituent, denoted as $V^3_{out,in}(t)$, exhibits a comparable settling pattern as $V^2_{out,in}(t)$, with both components being curbed by the loop at the aforementioned rate of $8.6dB/\tau_f$, as previously suggested [21, 38, 39].

The inclusion of HD_2 and HD_3 coefficients, g_{o2} and g_{o3}, respectively, in equation (4.15) can serve to model the impact of a non-linear output impedance [21, 38, 39]. This can allow for a revised representation of the correlation between $I_x(t)$ and $V_{out}(t)$

[21, 38, 39]:

$$I_x(t) = g_o \times V_{out}(t) + g_{o2} \times V_{out}^2(t) + g_{o3} \times V_{out}^3(t) + C_L \times \frac{dV_{out}}{dt} \tag{4.31}$$

The solution for (4.33) may be facilitated through a comparable method as the input distortion, culminating in the ensuing declaration for the output HD_2 [21, 38, 39]:

$$V_{out,out}^2(t) = \frac{g_{o2}}{g_o} \times \frac{A_o^2}{(1 + A_{ol} \times \beta)^3} \times V_{in}^2 \times \left((1 - e^{-t/\tau_f}) + e^{-t/\tau_f} \times (1 - e^{-t/\tau_f}) - 2 \times e^{-t/\tau_f}) \times \left(\frac{t}{\tau_f} \right) \right) \tag{4.32}$$

The HD_3 component in the output voltage, $V_{out,out}^3(t)$, can similarly be calculated as [21]:

$$V_{out,out}^3(t) = \frac{g_{o3}}{g_o} \times \frac{A_o^3}{(1 + A_{ol} \times \beta)^4} \times V_{in}^3 \times \left((1 - e^{-t/\tau_f}) + 3 \times e^{-t/\tau_f} \times (1 - e^{-t/\tau_f}) - \frac{1}{2} \times e^{-t/\tau_f} \times (1 - e^{(-2 \times t)/\tau_f}) - 3 \times e^{-t/\tau_f} \times \left(\frac{t}{\tau_f} \right) \right) \tag{4.33}$$

It is evident from (4.32) and (4.33) that the two distortion components, namely, $V_{out,out}^2(t)$ and $V_{out,out}^3(t)$, conform to the settling characteristics of the output voltage [21, 38, 39]. Figure 4.10 illustrates a comparison between the settling characteristics of input and output HD_2 components. The normalization of these components is performed in relation to the primary output signal. The amplifier distortion coefficients are deliberately selected to ensure that the input and output distortion components have equal values in a stable condition. The output distortion quickly achieves its maximum level, but the input distortion takes more time to stabilize and reach its ultimate value. The primary source of this phenomenon is the implementation of a negative-feedback mechanism, which reduces the signal strength at the virtual-ground nodes and mitigates the distortion resulting from the nonlinearity of the amplifier input [21, 38, 39].

5. A NOVEL 1.5-b FLIP AROUND MDAC WITH ISI CLEARING SWITCHES

Chapter 5 mentions about a novel 1.5-b flip-around multiplying digital-to-analog converter (MDAC) circuit, developed against the problem of inter-symbol interference (ISI). The proposed MDAC topology is protected by a patent at TPTMO [5].

5.1 Purpose

Pipelined ADCs basically consist of cascade connected multiple stages operating in continuous time or discrete time [3]. Typically, each stage of a pipeline ADC involves a sub-ADC, sub-DAC, and residue amplifier (ResAmp), as shown in Fig. 3.1a. The block formed by the ResAmp and the sub-DAC is called Multiplying DAC or MDAC in short.

Since the mismatch and process variation of capacitors, in particular C_{mim}, (up to 0.2% for mismatch $\pm 3\sigma$ in IHP SiGe 0.13μm technology [43]) are much better than the on-chip resistors, and the capacitors in switched capacitor circuits do not consume DC current, pipelined ADCs are usually implemented with a switched capacitor amplifier in an MDAC circuit, based on the discrete-time operating principle [3]. The ResAmps can be either open loop or closed loop situations in MDAC. Due to its high linearity performance, MDAC circuits with closed-loop amplifiers come to the fore. Considering the closed loop, there are two main types of MDAC topologies with switched capacitor amplifiers:

- Flip-around MDAC.
- Non-flip-around MDAC.

Fig. 5.1 shows 1.5-b MDAC topologies [44]. In the flip-around MDAC circuit in Fig. 5.1a, the feedback capacitor (C_F) is used as the sampling capacitor in the sampling phase ($\phi 1$) and as the feedback capacitor in the boost phase ($\phi 2$). In the non-flip-around circuit in Fig. 5.1b, the feedback capacitor (C_F) and sampling capacitor (C_S) operate in their fixed places.

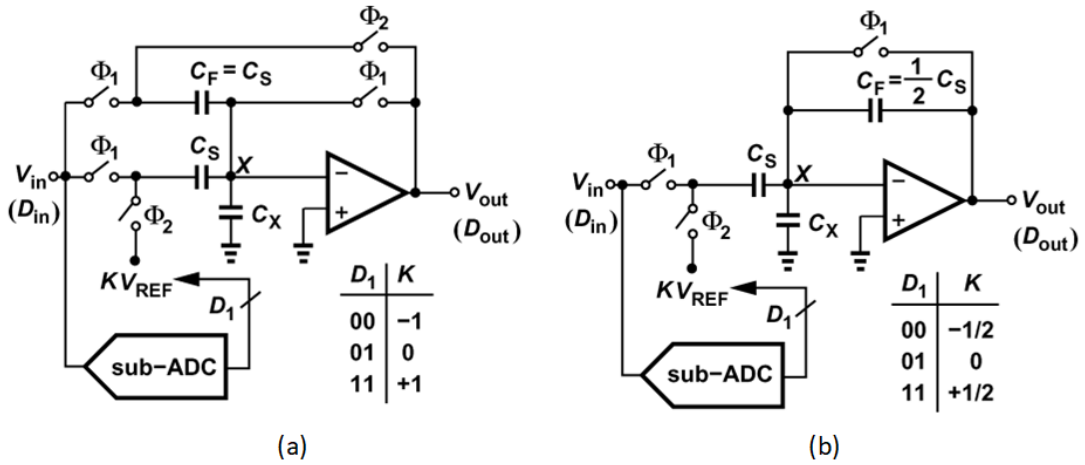


Figure 5.1 : Two fundamental MDAC topologies [44]: (a) A conventional 1.5-b flip-around MDAC, (b) A conventional 1.5-b non-flip-around MDAC.

For both MDAC topologies, let the total size of the sampling capacitor be C_S, and assume that the same ResAmps are used. The non-flip-around MDAC lags behind the flip-around-MDAC in terms of power consumption, bandwidth, settling time and occupancy on the chip.

5.2 ISI Effect on Switched Capacitor

Intersymbol interference (ISI) is a kind of signal distortion in telecommunication when one symbol disrupts the next signals. This is an undesirable occurrence, since the preceding symbols have a comparable impact to noise, hence reducing the reliability of transmission.

ISI also occurs in switched capacitor circuits mainly because the capacitor element is a memory element [45]. Capacitor is an electronic device that can store electrical charge. Correlation occurs between a charge that has already been stored on a capacitor and a new charge that is intended to be stored on that capacitor. This correlation is called ISI problem. The most dramatic performance decrease in our ADC, which will sample at GS/s levels, is due to the ISI effect.

Upon the sudden applied of the DC source, the voltage or current may be represented as a step function. The step response of a circuit refers to its reaction when it is stimulated by a step function, which may be either a voltage or a current source. Examine the circuit shown in Figure 5.2a and b. Let's consider the initial voltage at the capacitor as

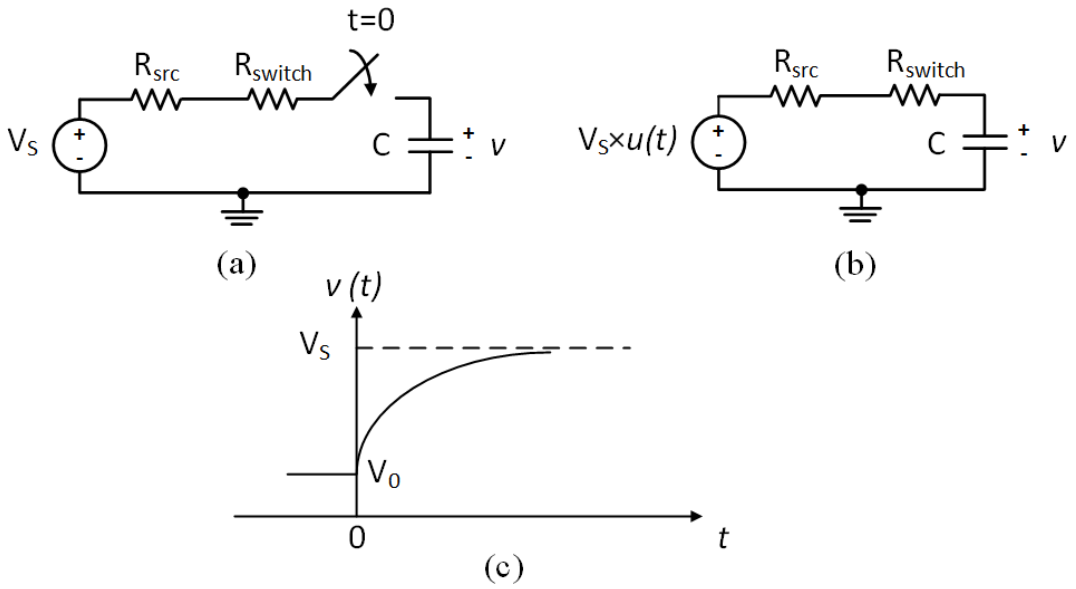


Figure 5.2 : Step response of an RC circuit: (a) Open switch, (b) Closed switch, (c) Transient response of the voltage across the capacitor.

V_0. Due to the inherent characteristics of capacitors, the voltage across them cannot undergo quick changes,

$$v(0^-) = v(0^+) = V_0. \tag{5.1}$$

Applying KVL,

$$\begin{aligned} C \times \frac{dv}{dt} + \frac{v - V_s \times u(t)}{(R_{src} + R_{switch})} &= 0. \\ \frac{dv}{dt} + \frac{v}{(R_{src} + R_{switch}) \times C} &= \frac{V_S}{(R_{src} + R_{switch}) \times C} \times u(t) \end{aligned} \tag{5.2}$$

where v is the voltage across the capacitor. For t$>$ 0,

$$\begin{aligned} \frac{dv}{dt} + \frac{v}{(R_{src} + R_{switch}) \times C} &= \frac{V_S}{(R_{src} + R_{switch}) \times C}, \\ \frac{dv}{dt} &= -\frac{v - V_S}{(R_{src} + R_{switch}) \times C}, \\ \frac{dv}{v - V_S} &= -\frac{dt}{(R_{src} + R_{switch}) \times C}. \end{aligned} \tag{5.3}$$

Integrating both sides and introducing the initial conditions,

$$\begin{aligned} \ln(v - V_S)\Big|_{V_0}^{v(t)} &= -\frac{t}{(R_{src} + R_{switch}) \times C}\Big|_0^t \\ \ln(v(t) - V_S) - \ln(V_0 - V_S) &= -\frac{t}{(R_{src} + R_{switch}) \times C} + 0 \end{aligned} \tag{5.4}$$

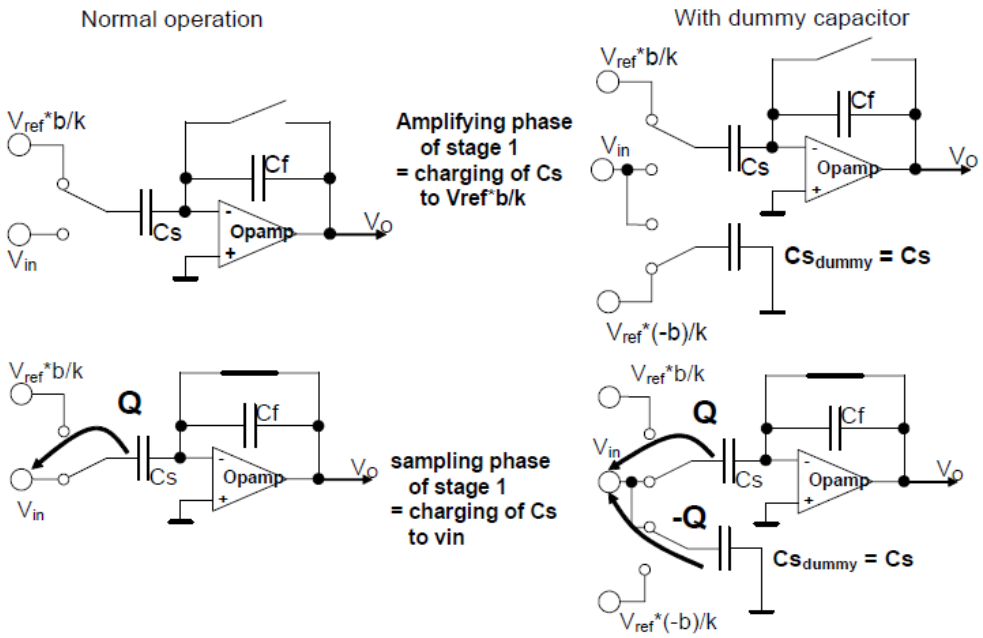


Figure 5.3 : Dummy capacitors for charge cancellation in a non-flip-around MDAC [45].

After arranging (5.5)

$$\ln\frac{v-V_S}{V_0-V_S}=-\frac{t}{(R_{src}+R_{switch})\times C} \qquad v(t)=V_S+(V_0-V_S)\times e^{-t/\tau} \tag{5.5}$$

is obtained. Thus,

$$v(t)=\begin{cases}V_0, & t<0\\ V_S+(V_0-V_S)\times e^{-t/\tau}, & t>0\end{cases} \tag{5.6}$$

Considering the capacitor is at first charged, Equation (5.6) represents the complete response (or entire response) of the RC circuit to a rapid DC voltage source. The general artefacts in S/H can be counted as noise, distortion, settling limitation, jitter and divers interferers such as low CMRR, low PSRR, and coupled substrate noise. The typical artefacts can be given as charge dump, droop and hold mode feed-through. Concerning those non-idealities, the previous charge, stored on the capacitor, varies, and accordingly, the next settling voltage level changes as well. In the next section, several analog and digital techniques are mentioned about how to mitigate ISI.

5.3 Previous MDAC Architectures for Mitigating ISI

One of the major problems encountered in a classic 1.5-b flip-around MDAC topology is ISI. In this phenomenon, the visibility of a quantized charge, coming from sub-DAC,

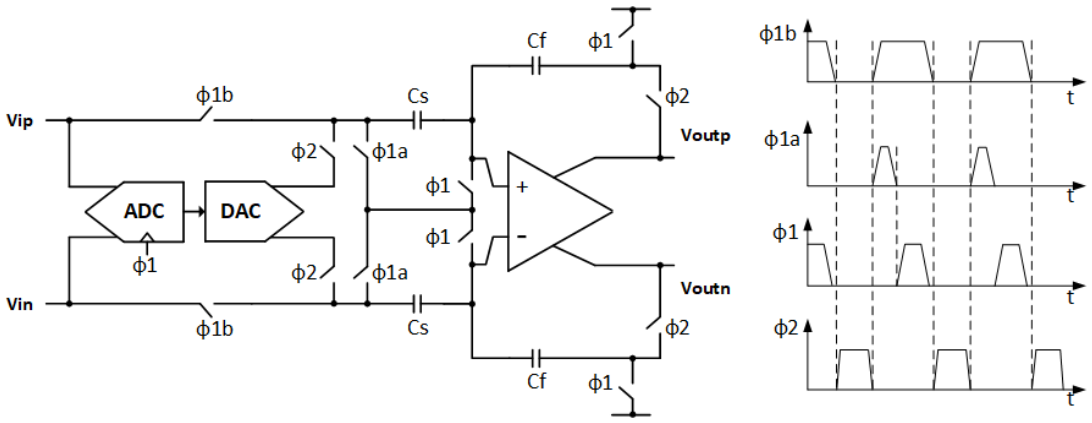


Figure 5.4 : A reset switch controlled by ϕ1a for removing history in a non-flip-around MDAC [46].

at the sampling capacitor, is visible at the input during the next sampling period. The new charge is correlated to the previous sample. Namely, in the ϕ_2 amplification phase, the signal at the DAC output accumulates as a load on the sampling capacitor. In the next sampling phase ϕ_1, the input signal correlates with the charge still preserved in the sampling capacitor. This correlation results in strong distortion tones in the spectrum. ISI, which occurs with the first stage of the ADC, continues to spread throughout the spectrum, increasing its effect throughout the cascade stages.

Including the ISI effect, the pre-calibration of pipeline ADC exhibits low SNDR and SFDR performance. In addition, it is very difficult to achieve the expected SNDR and SFDR increase for high frequency input signals in the Nyquist band with calibration.

In [45], where a non-flip around MDAC is deployed, a dummy capacitor is used to mitigate the ISI effect as depicted in Fig. 5.3. The negative charge is connected to the input during the next sampling period and cancels completely the charge of the real sampling capacitor. However, this technique brings a dummy capacitor and two switches for a single ended configuration.

In [46], a non-flip around MDAC is illustrated in Fig. 5.4. A reset switch, clocked by ϕ_{1a}, is placed to clear the sampling capacitor before the sampling period. The reset switch removes history and provides the sampling essentially independent of previous samples, thus alleviating ISI and distortion.

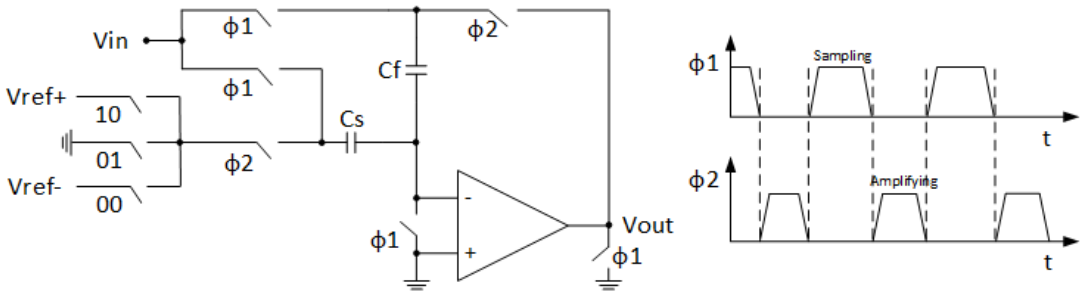


Figure 5.5 : A conventional single-ended 1.5-b MDAC and its switching phases.

5.4 Design of 1.5-b Flip-around MDAC

Fig. 3.1a shows a pipeline ADC and Fig. 3.1b shows a classic 1.5bit flip-around MDAC topology. This circuit basically has two separate operations: sampling and amplification. In Fig. 5.5, a conventional single-ended 1.5-b MDAC is illustrated. The circuit behavior is partitioned into two clock phases, denoted as ϕ_1 and ϕ_2. In ϕ_1, the input signal is sampled on the sampling capacitor, C_S, while the ResAmp is in reset mode with its inputs and outputs connected to ground. The electric charge stored in the two capacitors may be determined using the following equation:

$$Q_{C_S} = C_S \times V_{in},\ C_F \times V_{in}. \tag{5.7}$$

The sub-DAC has access to the sub-ADC's output code at the beginning of ϕ_2. Suitably, appropriate reference levels are linked to C_S's input. During this phase, the feedback capacitor, C_F, is connected in feedback across the ResAmp after being turned around. The difference between the input signal and the DAC output is amplified through charge transfer between C_S and C_F. Applying charge conservation: $C_F \times V_{out} + C_S \times V_{ref} = C_S \times V_{in} + C_F \times V_{in}$

$$V_{out} = \frac{C_S + C_F}{C_F} \times V_{in} - \frac{C_S}{C_F} \times V_{ref}. \tag{5.8}$$

For $C_S = C_F$,

$$V_{out} = \begin{cases} 2 \times V_{in} + V_{ref}, & \text{if } -V_{ref}/4 > V_{in} \geq -V_{ref} \\ 2 \times V_{in}, & \text{if } V_{ref}/4 > V_{in} \geq -V_{ref}/4 \\ 2 \times V_{in} - V_{ref}, & \text{if } V_{ref} \geq V_{in} \geq V_{ref}/4 \end{cases} \tag{5.9}$$

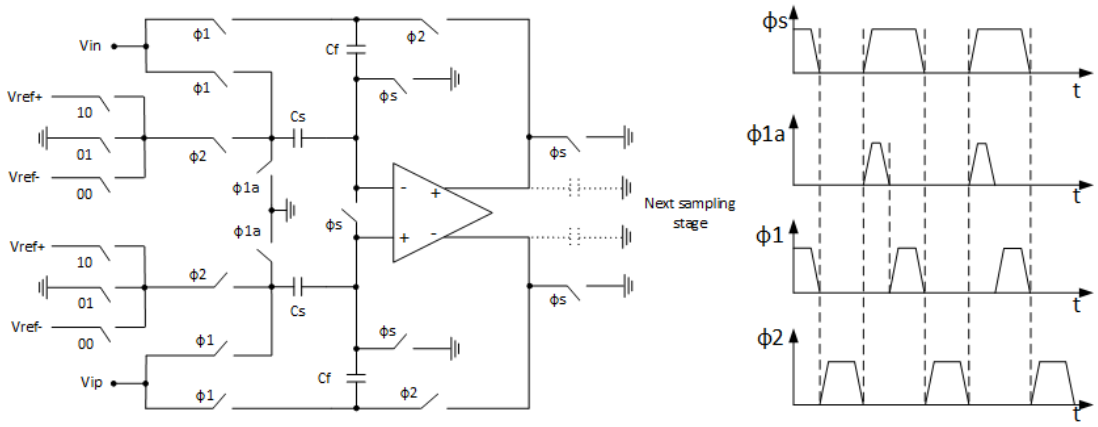


Figure 5.6 : The proposed 1.5-b MDAC switch configuration with ISI clear.

5.4.1 Error sources in a pipelined stage with 1.5-b flip-around MDAC

In order to understand the Capacitor mismatch, ResAmp gain, and ResAmp UGBW are taken into account

5.5 Front-end SHA-less Stage with 1.5-b Flip-around MDAC

As ISI problem is defined above, our MDAC has a similar problem, which deteriorates the SNDR and SFDR. The proposed 1.5-b MDAC and its clock phases are shown in Fig. 5.6. The reset switches, clocked by ϕ_{1a}, are placed to clear the sampling capacitor before the sampling period, ϕ_1. The ϕ_2 is the amplification phase. There are a total of ten switches controlled in these two phases. In addition to the ϕ_1 and ϕ_2, there is a clock phase, namely, ϕ_S. In this phase, bottom-plate sampling is used by shutting off the switches connected to the op-amp's inputs early in order to lessen the impact of charge injection from the switches. By doing this, the signal-dependent offset is nearly completely eliminated, and a differential implementation may cancel the independent component.

In the ϕ_2, the input terminals of the ResAmp are connected to the DAC outputs and the differential signal is amplified. The switches located at the outputs of the ResAmp pull the output terminals to the common mode level after the ϕ_2 phase is over. Thus, the signal in the next amplification clock phase does not mix with the previous sample when it comes to the amplifier output.

6. BACK-END 3-b FLASH ADC

In chapter 6, a 3-b fully differential flash ADC is presented, which is used as a back-end ADC to resolve extra 3 bits for the pipeline ADC.

6.1 Purpose

In this work, a 3-b Flash ADC is proposed as a back-end ADC to digitize the final residue of the 8 cascaded pipelined stages. As the stage number of the pipelined ADCs increases, the complexity of the clock distribution, overall power and silicon are increase [3, 19].

The flash ADC design has to handle significant voltage variations and achieve a digital output at a sampling frequency of up to 1.6 GHz, all while maintaining a minimal input capacitive load to optimize the signal bandwidth. The IHP SiGe 130 nm CMOS thin-oxide devices provide a significant benefit for Flash ADCs compared to thick-oxide devices due to their much lower regeneration time, which may be ten times faster.

6.2 A 1.6 GS/s Fully Differential 3-b Flash ADC

Flash ADCs serve primarily two functions. This ADC is capable of attaining the greatest conversion velocities for modest (6-b) resolutions when operated independently. The application in a multitude of additional analog-to-digital architectures, including subrange converters, is an additional crucial area. In order to achieve additional resolution, a 3-b flash ADC is suggested as the back-end ADC, as illustrated in Fig. 6.1.

6.2.1 Two stage strong-arm clocked comparator

In Fig. 6.2, the schematic of the comparator circuit is depicted. A fully differential pre-amplifier stage with positive feedback connected diode loads is used to reduce the kickback noise, emerging from clocked comparator stage. Clock comparator section is

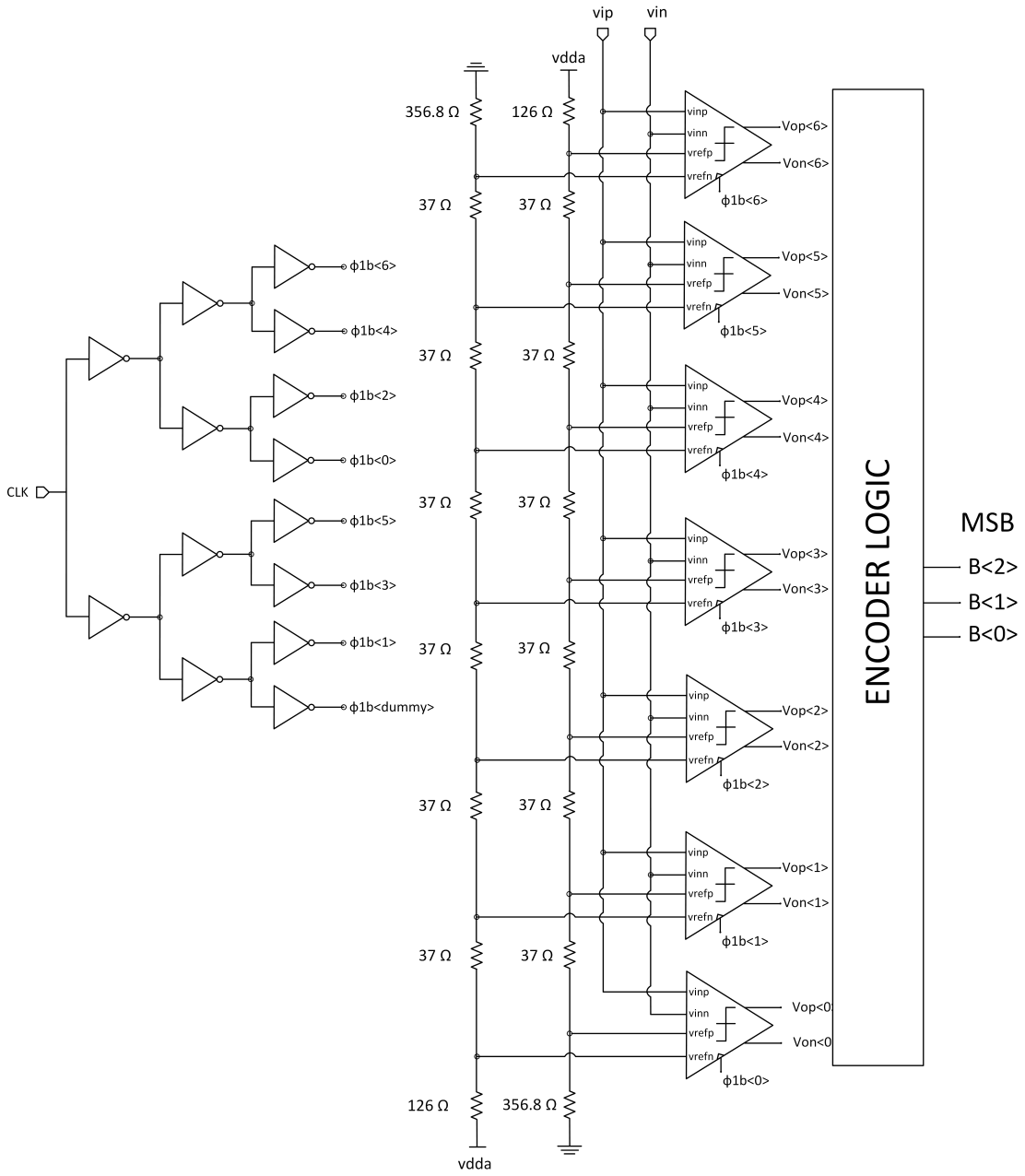


Figure 6.1 : The proposed 3-b back-end Flash ADC.

a strongARM latch. Moreover, PMOS switches are connected to latch nodes to reset those nodes faster so that the overall circuit can operate up to 1.6 GHz.

For monotonic behavior in $\pm 3\sigma$ confidence level, the 1σ offset voltage of the clocked comparator should satisfy the following formula:

$$\frac{V_{LSB}}{\sigma_{comparator} \times \sqrt{2}} = 3, \tag{6.1}$$

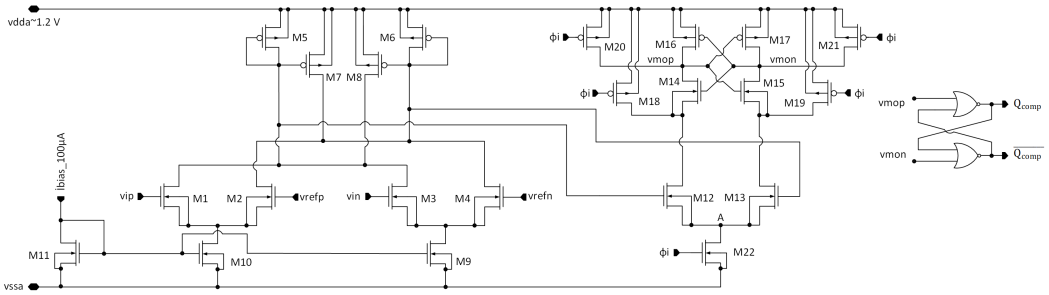


Figure 6.2 : A two stage strongARM clocked comparator with SR latch.

where V_{LSB} is $2^{-N} \times$ single ended full scale input range (FSIR). Then, an approximate 1σ offset voltage for each comparator can be obtained as:

$$\sigma_{\text{comparator}} = \frac{62.5\,\text{mV}}{3 \times \sqrt{2}} = 14.75\,\text{mV}, \tag{6.2}$$

6.2.2 Resistive ladder

The design of a 3 bit Flash ADC can be accomplished by 7 comparators meaning that 7 taps for resistive ladder are required at least. In Fig. 6.3a, a simple model of resistive ladder with tap capacitance is shown. Rough RC estimate of transmission line can be given as [3]:

$$\tau = \frac{2^N \times C_{Tap}}{2} \times \frac{2^N \times R}{4} = \frac{R_{Tot} \times C_{Tot}}{8}, \tag{6.3}$$

The maximum sampling frequency is assumed as 1.6 GHz for which the settling requirement is the most stringent. Thus, the settling time for the resistive ladder should be within 312.5 ps, regarding the following estimations:

- C_{tap} = 100 fF (Tap capacitor for each resistor).
- τ = 312.5 ps (settling time for the half of the sampling period).
- N = 3 (Number of bit).

We can substitute the variables in (6.3) for the given values aforementioned as follows.

$$312.5\,\text{ps} = \frac{2^3 \times 100\,\text{fF}}{2} \times \frac{2^3 \times R}{4} = \frac{R_{Tot} \times 800\,\text{fF}}{8}, R_{tot} = 3125\,\Omega, \tag{6.4}$$

Actually, we may want 4 times faster settling time. For example, we may reduce the settling time towards 72.125 ps. Then, the total resistor is 781.25 Ω. The design specification for the resistive ladder is remarked in Table 6.1.

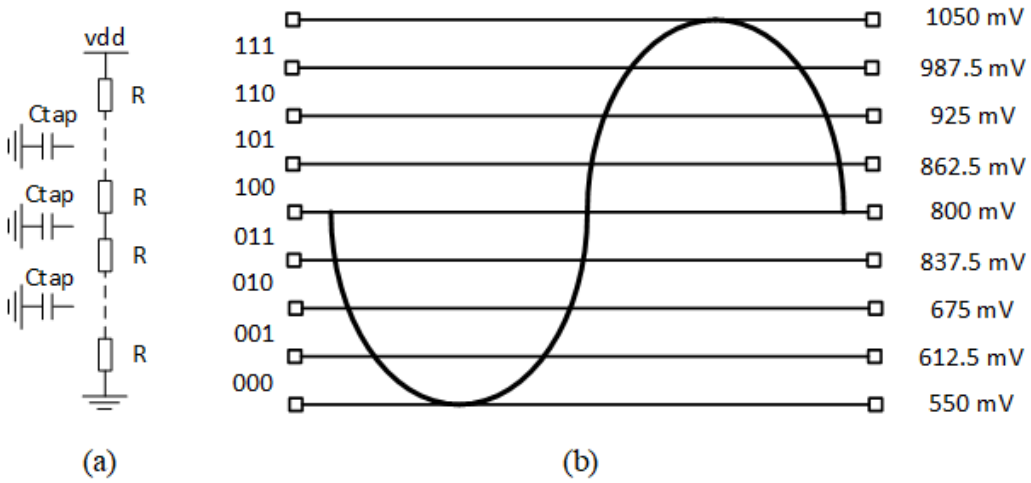


Figure 6.3 : (a) Resistive ladder RC model, (b) Quantization levels for the single-ended input signal of the proposed 3-b Flash ADC.

The quantization levels according to the single-ended FSIR are depicted in Fig. 6.3b. The common mode level is 800 mV. The peak-to-peak voltage of the single ended input signal is 500 mV. The resistive ladder, shown in Fig. 6.1, is designed with respect to those voltage levels.

Table 6.1 : Specification for the resistive ladder

Description	**Specification**
VDD	1.2 V
Single-ended full scale input range (FSIR)	from 550 mV to 1050 mV
Vcm	800 mV
Total number of tap	7 or 8
Differential operation	Yes

6.3 Simulation Results

The simulation aims to characterize the Flash ADC in terms of $\pm 3\sigma$ offset voltage of the clocked comparator, the input signal bandwidth, ENOB, SNDR, latency, and power consumption. The transient noise is activated for the transient simulations so that the active and passive components contribute to noise level.

6.3.1 Timing diagrams and dynamic offset voltage of a clocked comparator

As shown in Fig. 6.4a, the comparator is evaluated on the dynamic offset test bench (DOTB) [17]. DOTB is influenced by transient effects, including mismatches caused by charge injection and parasitic capacitances, as well as DC offset mechanisms, including threshold voltage mismatch. For the purpose of calculating the standard

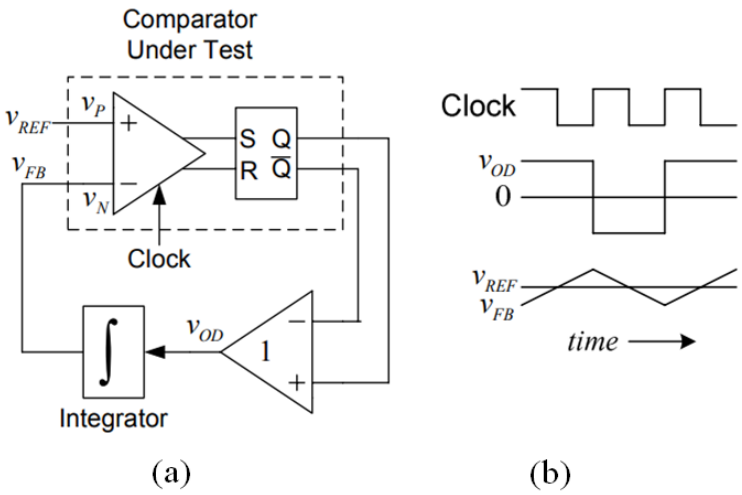


Figure 6.4 : (a) DOTB block diagram, (b) DOTB waveforms.

deviation of the input offset voltage, these deterministic outcomes can be collected using statistical methods like Monte Carlo simulations. An additional advantage of this methodology is that it permits the simulation of offsets individually, thereby distinguishing what factors significantly contribute to the input offset voltage.

Differential amplifier and integrator are from the verilogA library. Differential amplifier is a voltage buffer. V_{REF} is set to 800mV. As specified by the DOTB, the peak values of the waveform V_{FB} ought to be below the desired resolution. Integrator gain and clock period influence the highest value of V_{FB}. To observe the offset, we should run Monte Carlo. In the simulation V_{FB} increases slowly until it reaches the flip voltage where V_{REF} is 800 mV. After that we can see that comparator output is jump around from logic low to logic high.

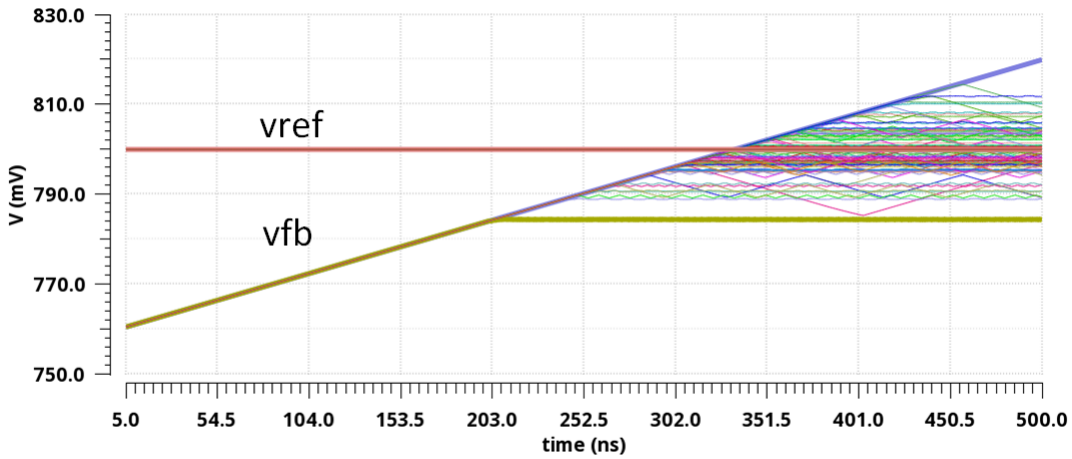


Figure 6.5 : Monte Carlo 100 samples for V_{FB}, process and mismatch.

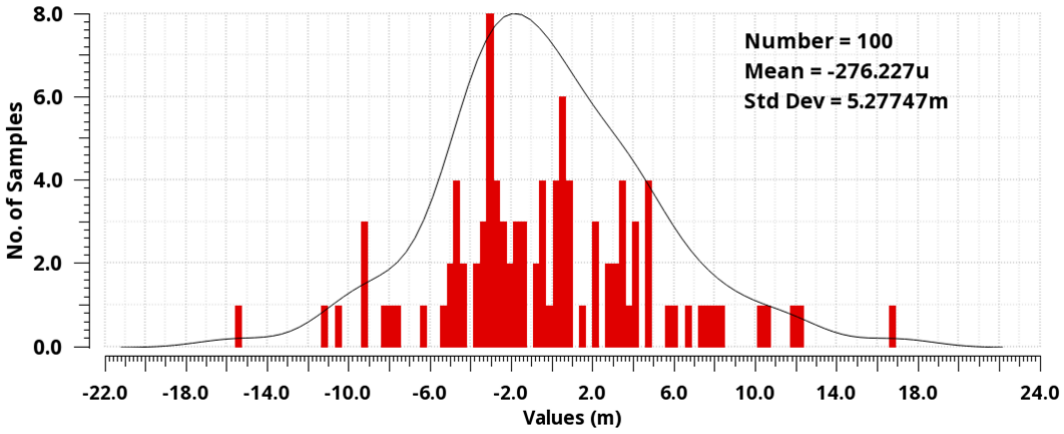


Figure 6.6 : Monte Carlo 100 samples, $\sigma_{comparator}$, process and mismatch.

In Fig. 6.5, V_{FB} and V_{REF} are depicted for 100 samples of Monte Carlo simulation. For σ analysis, the crossing point is taken at 450 ns for V_{FB}. The loop is settled around V_{REF}. $1\times\sigma_{comparator}$ is obtained as 5.3 mV, and $3\times\sigma_{comparator}$ is 15.9 mV. DNL should be 0.5×LSB that means a monotonic behaviour. V_{LSB} is 62.5mV, and thus, 0.5×LSB is 31.25 mV. $3\times\sigma_{comparator}$ is lower than 0.5×LSB.

Transient waveforms for the clocked comparator with SR latch is depicted in Fig. 6.7. The sampling clock frequency is at 1.6 GHz. The input signal frequency is at 400 MHz. The peak-to-peak value of the single-ended input signal is 500 mV. As depicted in Fig. 6.7c, the maximum latency from $clock_{riseedge}$ to Q_{comp} is 279 ps.

6.3.2 Ramp test

In Fig. 6.8, the ramp response of the flash ADC is depicted for 1.6 GHz sampling clock and the ramp single-ended amplitude from 550 mV to 1050 mV in 16 clock cycle, as fast as possible.

6.3.3 Sinus test

The sinus test is performed with an ideal sine waves. A model MDAC block is prepared to produce residue signals that will be the inputs of the flash ADC in the real design. By this modelling, the clock synchronization between the 8th stage MDAC and the back-end Flash ADC is accomplished.

For a sine wave with 800 mV common mode voltage and single-ended 500 mVp-p over it, the transient simulation is performed. Output bits are summed and SNR calculations

Table 6.2 : Specification for the sinus test

f_s	f_{in}	**Coherent** Fin	**FFT Size**
1.6 GHz	50 MHz	48.4375 MHz	1024
1.6 GHz	400 MHz	401.5625 MHz	1024
1.6 GHz	780 MHz	779.6875 MHz	1024

are done in Cadence environment. FFT plots for 50 MHz, 400 MHz and 780 MHz input signals are given in Fig. 6.9. ENOB and SINAD versus the input signal frequencies are shown in Fig. 6.10. Actual frequency values and calculated by using coherent input signal frequencies are given in Table 6.2.

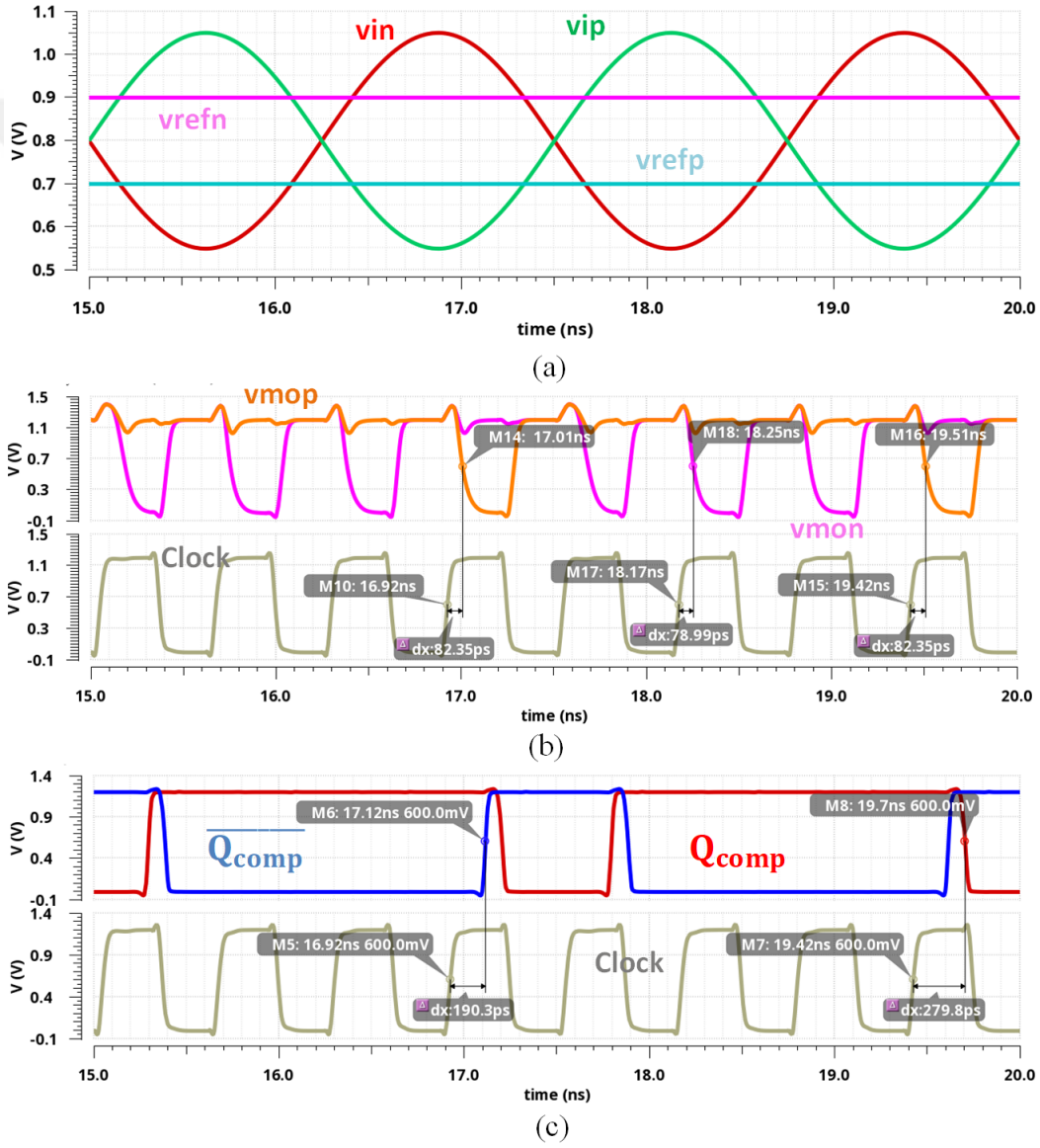


Figure 6.7 : (a) Single-ended input signals and reference voltages, (b) transient waveforms of the two stage clocked comparator output terminals, (c) transient waveforms of SR-latch.

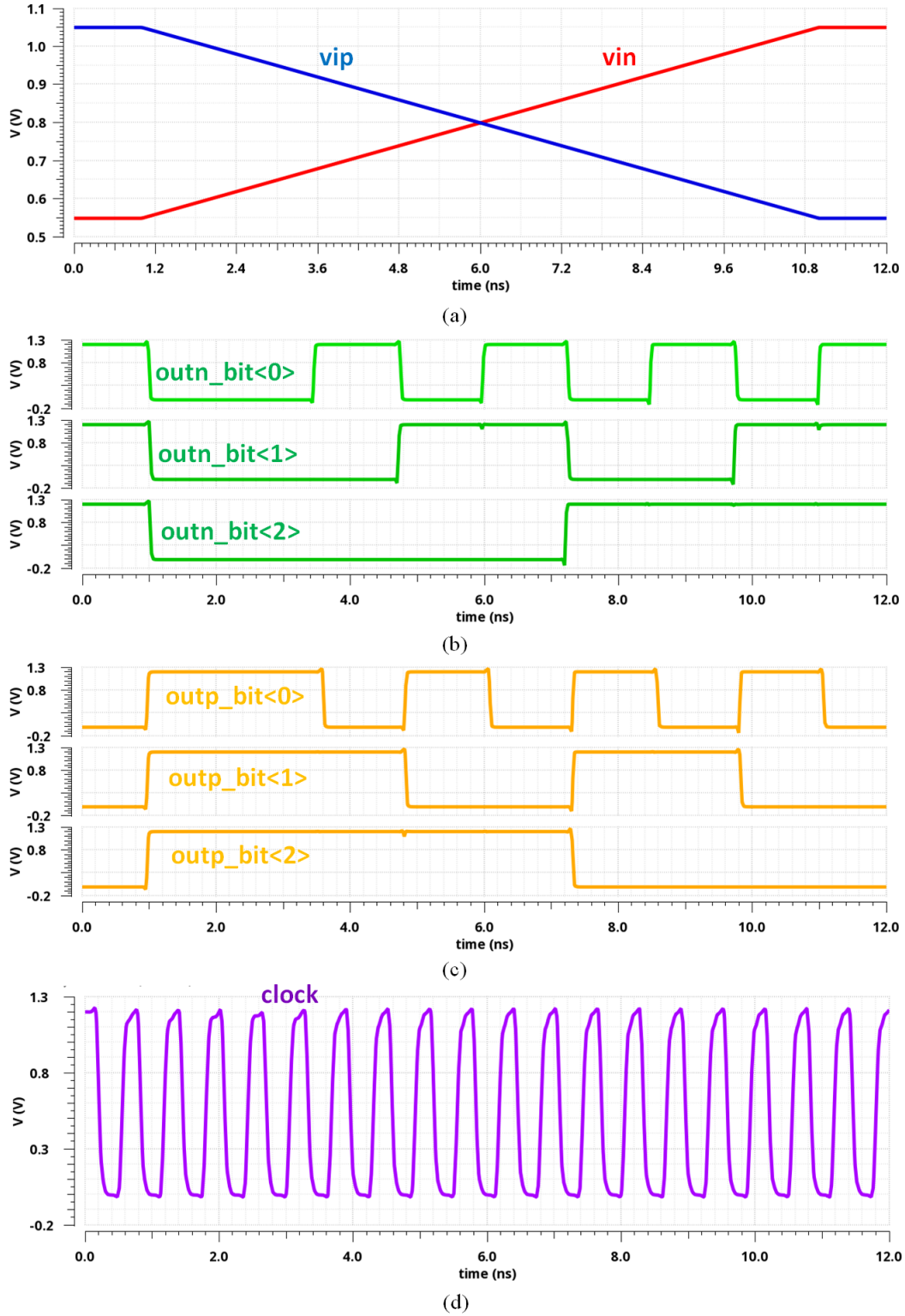


Figure 6.8 : Ramp test for the 3 bit Flash ADC at 1.6 GHz sampling clock: (a) The differential ramp signal, (b) The negative outputs of 3 bits, (c) The positive outputs of 3 bits, (d) 1.6 GHz sampling clock signal. .

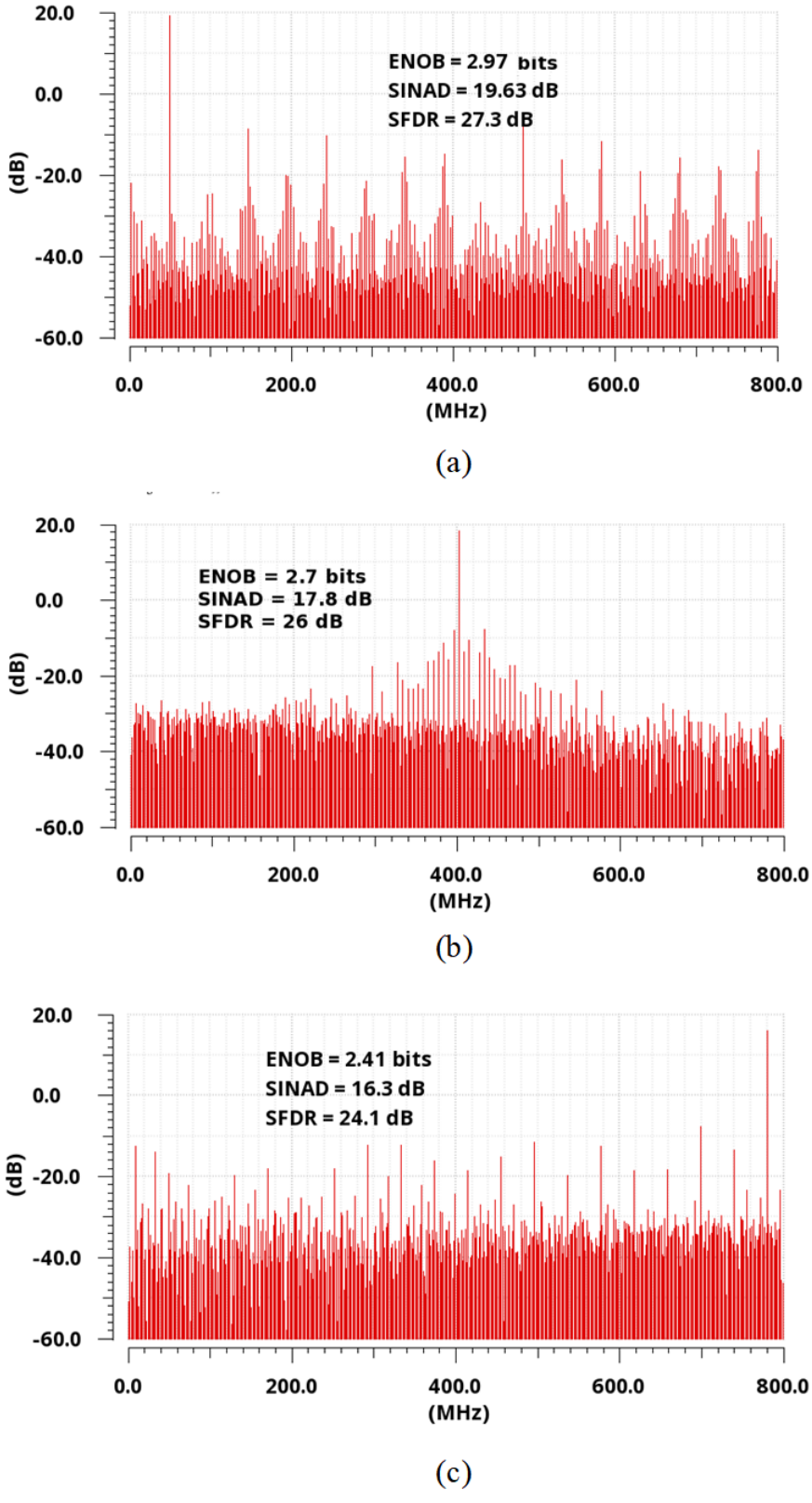
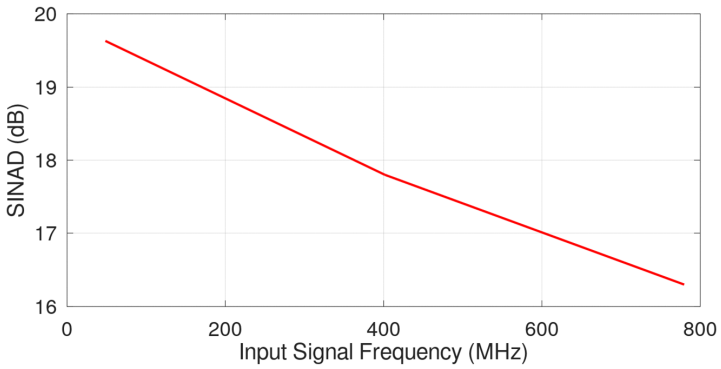
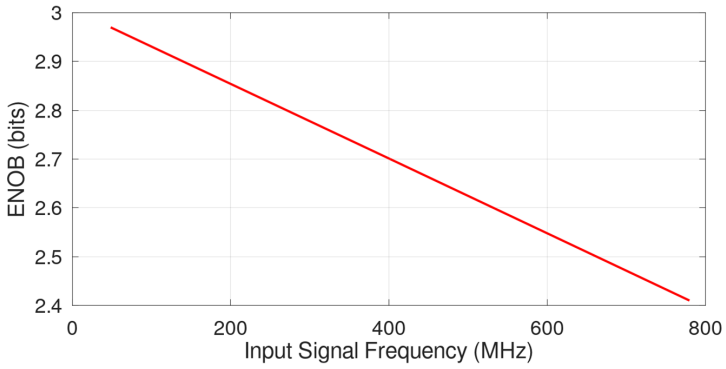


Figure 6.9 : 1.6 GHz sampling clock, single-ended 500 mVpp input signal, 1024 point FFT and the coherent input signal frequencies at: (a) 48.4375 MHz, (b) 401.5625 MHz, (c) 779.6875 MHz .



(a)



(b)

Figure 6.10 : (a) SINAD vs input signal frequency, (b) ENOB vs input signal frequency.

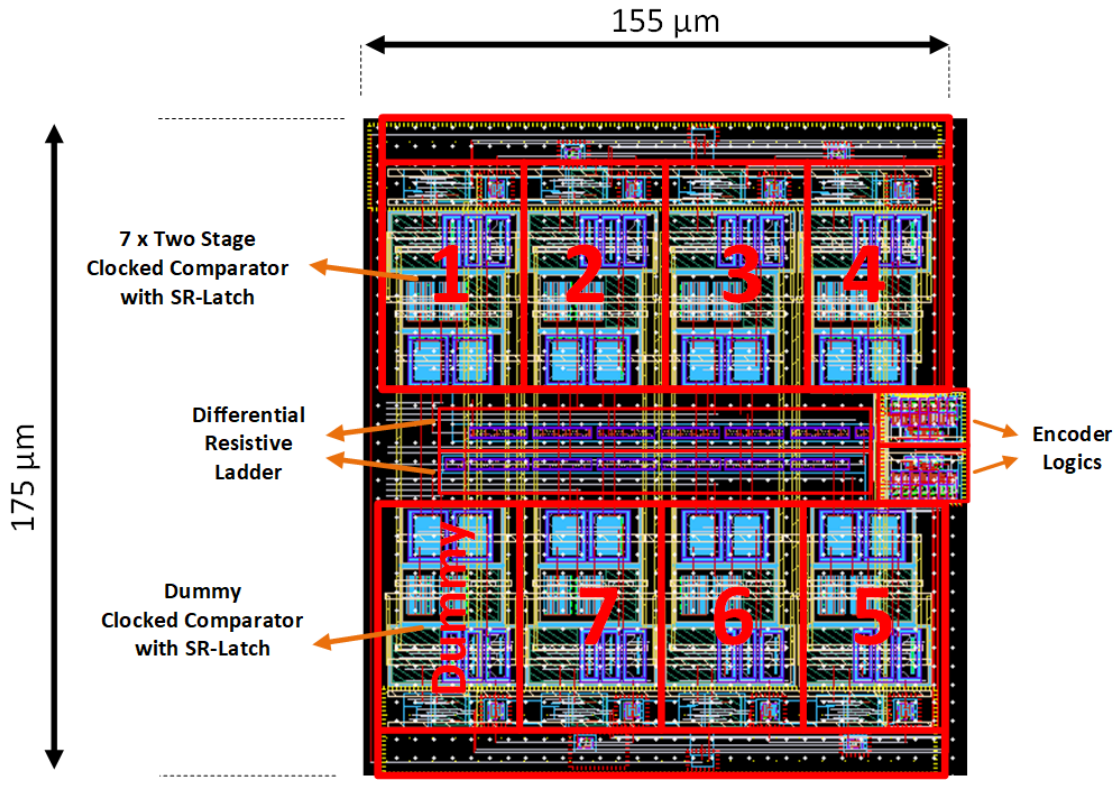


Figure 6.11 : Layout view of the 3-b Flash ADC with 155 μm $\times$ 175 μm .

6.3.4 Conclusion

The performance summary of the proposed 3-b back-end flash ADC is remarked in Table 6.3. It totally consumes 14.7 mA at a supply of 1.2 V when the sampling frequency is at 1.6 GHz. The latency of the ADC is greater than 480 ps. The complete layout area of the ADC is 155 μm $\times$ 175 μm, as shown in Fig. 6.11. It, as a back-end ADC, fulfils the speed, power and layout area requirements to be used in the pipeline ADC.

Table 6.3 : Performance summary of the 3-b flash ADC

f_s **(Sampling clock frequency)**		1.6 GHz		
f_{in} **(Input signal frequency)**		50 MHz	400 MHz	780 MHz
Clocked Comparator with SR-latch	**Dynamic input offset voltage**	5.3 mV		
	Silicon area	36 μm $\times$ 60 μm		
	Current consumption @ 1.2 V	1.22 mA		
Differential resistive ladder	**Maximum voltage variation (σ)**	2.8 mV		
	Current consumption @ 1.2 V	2 $\times$ 1.6 mA		
Encoder logics	**Current consumption @ 1.2 V**	2.9 mA		
3-b Flash ADC	**ENOB**	3 bits	2.7 bits	2.41 bits
	SINAD	19.63 dB	17.8 dB	16.3 dB
	SFDR	27.3 dB	26 dB	24.1 dB
	Maximum latency	> 480 ps		
	Silicon area	155 μm $\times$ 175 μm		
	Current consumption @ 1.2 V	14.7 mA		

7. NON-OVERLAPPING CLOCK PHASE GENERATOR WITH MULTI VOLTAGE LEVEL

This chapter introduces a new design for generating clock phases with multiple voltage levels, using a differential clock driver. The device has a condensed and completely integrated power management system, which includes low-dropout regulators (LDOs) and a bandgap reference circuit [1, 7]. The PVT fluctuation could be controlled by SPI programming [APPENDIX-C]. The device operates effectively throughout the frequency range of 50 MHz to 1 GHz and is specifically designed for use in pipelined ADCs. The core chip attains an SNR of around 72 dB for clock frequencies ranging from 50 MHz to 150 MHz. For clock frequencies between 150 MHz and 400 MHz, the SNR is over 68 dB. Furthermore, for clock frequencies up to 1 GHz, the SNR remains above 60 dB. The central component draws a current of 19 mA at a frequency of 1 GHz, powered by a 3 V external source. The chip has dimensions of 1235 µm x 1300 µm and is fabricated using a SiGe BiCMOS 0.13 µm technology. The clock generating system occupies a silicon area of 400 µm × 360 µm, without including I/O pads and interface circuitry. The device is packaged in a QFN32 package sized 5 mm x 5 mm [APPENDIX-B] and is mounted onto a FR4 board.

7.1 Introduction

The proliferation of incorporated devices, the expansion of the Cloud and the Internet, and the utilization of satellite and networking applications, wireline and wireless communications, instrumentation, and medical imaging have all contributed to the rising demand for GS/s data rate applications in recent years [1, 47–49]. Larger data rates and faster data interfaces necessitate timers that are outfitted with superior synchronization components for high bandwidth networks. .

A frequent use of non-overlapping clock phase generator is in discrete time ADCs, where the clock phases are utilized to ascertain acquisition and conversion [1, 2, 13]. An example of such use is seen in Fig. 7.1. The suggested design includes many different parts such as a passive BALUN, an external matching network, a differential

to single-ended converter (DSEC), clock level shifters, low drop-out (LDO) regulators, a band gap reference (BGR) circuit, and a serial peripheral interface (SPI). These parts are shown in Fig. 7.2a. There are primarily two techniques to establish a clock source for minimal jitter purposes.

One such source of clock signals is phase-locked loops (PLLs) that are integrated into the same integrated circuit (IC) as the ADC system [50]. Accelerated fluctuations in the voltages of the power and ground supply lines, in addition to the voltage of the substrate on which the PLL circuits are manufactured, may not have an impact on the phase and frequency of the produced oscillation. However, integrating a PLL in the same IC as the ADC might be costly in terms of design intricacy, since both the PLL and ADC need precise control mechanisms.

The second kind of clock sources may arise from an externally connected PLL-based device, which may be conveniently calibrated to match the IC externally [50, 51]. An external clock source with little variation in timing may be used to operate the IC, as shown in Fig. 7.1. A passive BALUN is used to drive a differential quasi-sine wave into the chip [7, 20, 51]. The use of an external clock source is favored in this task.

The technique of shifting the voltage level has been addressed in numerous methods in literature. The first category consists of clock level shifters that use charge-pump circuits and bootstrap capacitors [1, 2, 52–54]. The clock signal with level shift specifically follows the input signal. The bootstrap switch subsequently samples it. The primary application of bootstrap switches is in sample and hold operations that require exceptional linearity. The second set of clock boosters consists of charge pump capacitors. However, the clock swing is dictated by the adaptive power/ground voltages. The level shifter circuit described in [55] employs charge-pump capacitors and leverages low voltage transistors in a digital 1.2 V CMOS 0.13 μm technology for high-speed switching purposes. The device translates the input signal's nominal range, which spans from 0 to 1.2 V, into the desired output range of 2.4 V to 3.6 V. AC coupling capacitors, as the third set of level shifters, are used to elevate the clock level. The paper by [19] introduces an adaptive power/ground approach for a CMOS 40 nm technology, with a supply voltage of 1 V specifically for the thin oxide transistors. The power and ground levels are internally created via the use of two Low Dropout Regulators (LDOs). The input swing range, ranging from 0 to 1 V, is adjusted

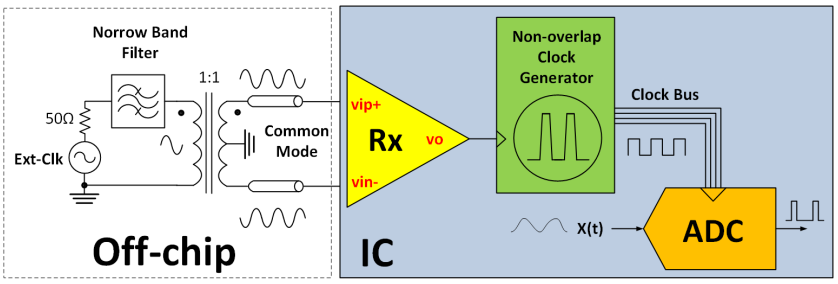


Figure 7.1 : Block diagram illustrating a clock generating system designed for high-speed ADCs. [1].

to the desired swing range, which falls between 0.75 V and 1.75 V. Furthermore, a DC common mode voltage is precisely set at 1.25 V. This voltage is isolated from the input using a coupling capacitor.

This work presents the first-ever implementation of the innovative architecture in the IHP SiGe BiCMOS 0.13 μm technology, in the published academic journals. Given that the clock source is supplied from an external source, a front-end DSEC, as shown in Fig. 7.2a, is used to take advantage of the differential operation, which is resistant to common mode noise and nonlinearity [51]. The timing diagram shown in Fig. 7.2b may be generated using a clock phase generator circuit, which is based on the design described in [1, 7]. The purpose of this research is to modify the range of the clock fluctuation by employing low-voltage transistors that experience minimal performance degradation and do not exceed voltage specifications. The methodology employed in this study is the adaptive power/ground approach, which was outlined by [19]. Instead of a single shifting swing range, there are two distinct voltage ranges: The first swing range extends from 0.4 to 1.6 V, while the subsequent extends spans from 1.6 to 2.8 V. An AC coupling capacitor is incorporated into each clock level converter, which functions using a DC bias voltage for the common mode. To maximize control during post-processing, adjustments are made to the LDOs and BGR to account for fluctuations in PVT. This study proposes the use of several analog and digital design methodologies to create a new clock phase generating architecture that is completely integrated [1, 7].

This research paper presents a groundbreaking, fully integrated architecture for a multi-level non-overlapping clock phase generator. It provides an exhaustive description of the generator's design as well as the results of jitter measurements [1, 7]. The architecture is specifically developed for pipeline ADCs operating at different

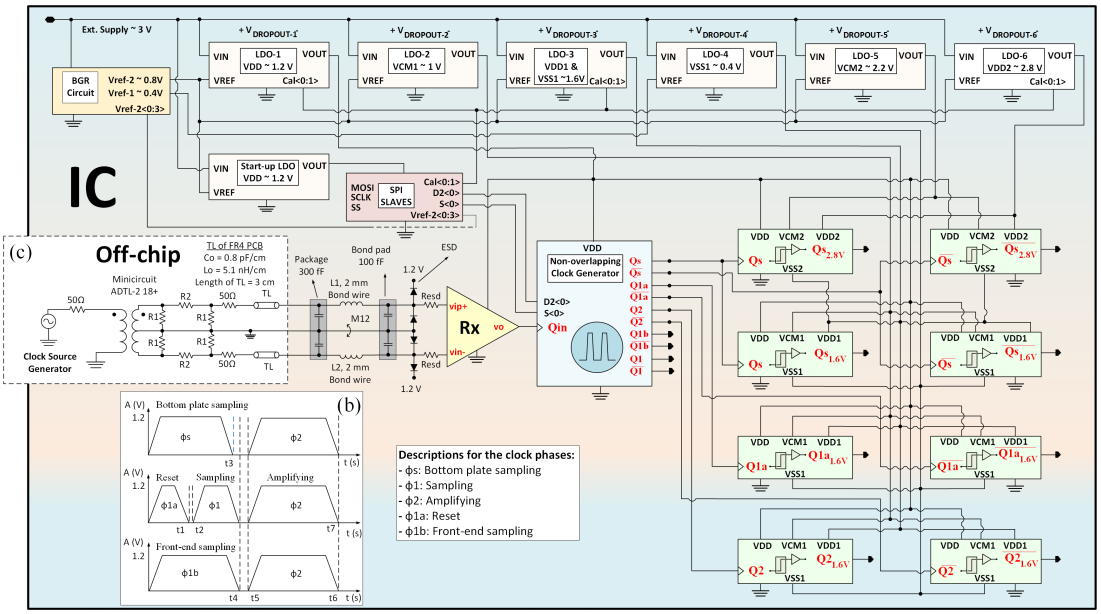


Figure 7.2 : (a) The suggested design for generating non-overlapping clock phases [1], (b) diagram of clock phases [1], (c) external input matching network [1].

sampling frequencies ranging from 50 MS/s to 1 GS/s. A partial publication of this work can be found in reference [1, 7]. The suggested design, as seen in Fig. 7.1, offers many clock phases with a notional swing range of 0 to 1.2 V. Additionally, some clock phases in this context serve as level shifters, facilitating rapid switching, enhancing the SNR of the ADC, and reducing switching noise [2, 5, 6, 52].

7.2 Clock Level Shifters Differential Clock Driver and Non-Overlapping Clock Generator

The study proposes the use of several digital and analog design methods in a constructive manner, resulting in the development of a unique and completely integrated clock phase generating architecture [1, 7]. Figure 7.2a illustrates the suggested design, which includes clock buffer and clock level shifters. Several clock phases can be generated while the device is capable of regulating PVT fluctuations via instructions for SPI. The circuitry has three distinct voltage levels and a tiny, fully integrated power management system that includes six low-dropout regulators (LDOs) and a bandgap reference circuit. The following sections define and elaborate on the sub-blocks.

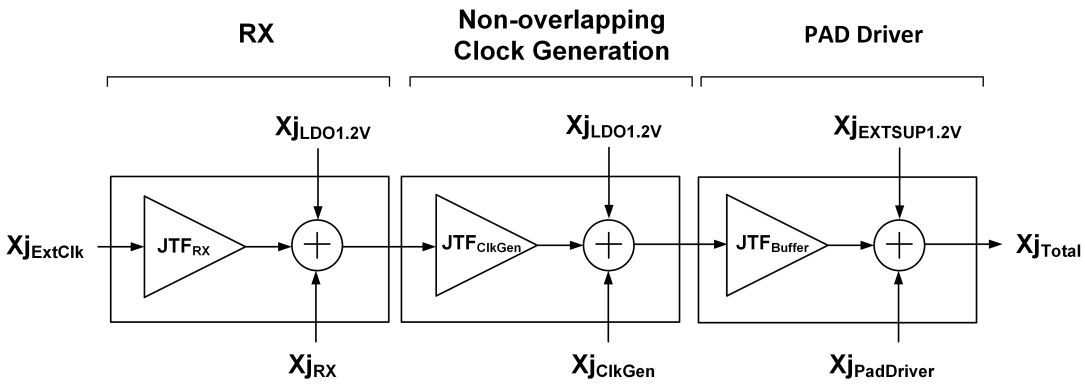


Figure 7.3 : Model of jitter for the design that sets the clock phase suggested for the supply range of 0-1.2 V [1].

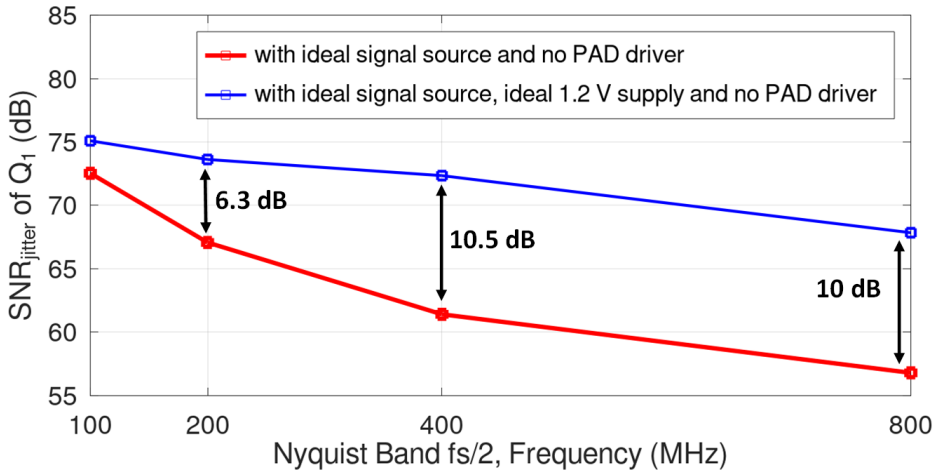


Figure 7.4 : RCX simulations: SNR_{jitter} of ϕ_1 (Integration bandwidth for phase jitter: 10 kHz to 20 MHz) [1].

7.2.1 Clock phase generator jitter model

In the suggested architecture, shown in Fig. 7.2a, a jitter model is created to detect the sources of noise, as indicated in Fig. 7.3 [1,7]. The model consists of three consecutive stages: the RX stage, the non-overlapping clock phase generation stage, and the pad driver stage. These stages operate in the 1.2 V supply voltage domain, which is supplied by an inbuilt low-dropout regulator (LDO). Within the supply domain of the architecture, there exist three clock phases: ϕ_1 (sampling phase), ϕ_2 (amplifying phase), and ϕ_{1b} (front-end sampling). These phases are crucial for signal processing in the pipeline ADCs and have a direct impact on the SNR. Jitter is particularly significant in these phases. In the given scenario, the jitter transfer function (JTF) of each stage measures the degree of jitter reduction throughout an integration bandwidth ranging from 10 kHz to 20 MHz. In the frequency domain, the input jitter is represented

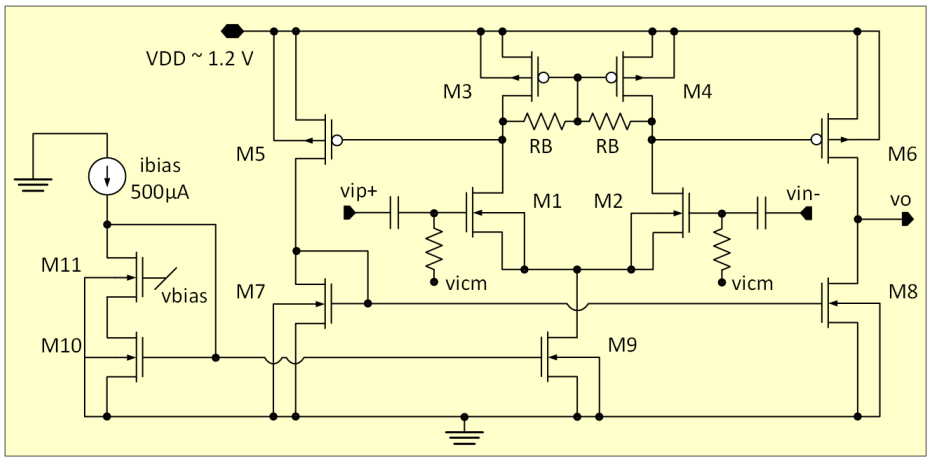


Figure 7.5 : DSEC [1].

Xj_{ExtClk}. In order to compute the overall output jitter (Xj_{Total}), the following method may be used [56, 57]:

$$Xj_{Total} = \sqrt{[((Xj_{ExtClk} \times JTF_{RX})^2 + Xj_{RX}^2 + Xj_{x,LDO_{1.2V}}^2) \times JTF_{ClkGen}^2 + Xj_{ClkGen}^2 + Xj_{y,LDO_{1.2V}}^2] \times JTF_{PadDriver}^2 + Xj_{PadDriver}^2 + Xj_{EXTSUP_{1.2V}}^2}, \tag{7.1}$$

where the associated blocks are denoted by subscripts. According to the model, the jitter contribution of the $LDO_{1.2V}$ ($Xj_{LDO_{1.2V}}$) is noted in two sub-blocks and multiplied by the associated JTFs until it reaches the output terminal. When the clock frequency surpasses 800 MHz, simulations demonstrate a 10 dB fall in SNR, as seen in Fig. 7.4. It is assumed that these sub-blocks are subjected to $Xj_x, LDO_{1.2V}$ and $Xj_y, LDO_{1.2V}$ in (7.1), which may represent the combined effect of $LDO_{1.2V}$ on the overall jitter of the clock generation architecture. In (7.1), JTFs are assumed to be 1, indicating that the jitter contribution of each stage is considered to be independent of one another [58]. Consequently, the total RMS-jitter ($\sigma_{jChip,Total}$) recorded at the spectrum analyzer may be split down as follows [1]:

$$\sigma_{jChip,Total} = \sqrt{\sigma_{jExtClk}^2 + \sigma_{jPadDriver}^2 + \sigma_{jCore}^2 + \sigma_{jx,LDO_{1.2V}}^2 + \sigma_{jy,LDO_{1.2V}}^2}, \tag{7.2}$$

where σ_{jCore} denotes the RMS-jitter from RX to one of the clock phase outputs in a non-overlapping circuit, $\sigma_{jExtClk}$ represents the RMS-jitter of the external source of signal, and $\sigma_{jPadDriver}$ originates from the associated pad driver, illustrated in Fig. 7.11. The sub-blocks are expected to be exposed to $Xj_x, LDO_{1.2V}$ and $Xj_y, LDO_{1.2V}$. The combined values of $Xj_x, LDO_{1.2V}$ and $Xj_y, LDO_{1.2V}$ in (7.1) represent the total

		D2	D1	Operating Freq.
S=1	**D2=1**	2.3 ns	60p	75 MHz
	D2=0	575 ps	60p	250 MHz
S=0		0	0	50 MHz - 1 GHz

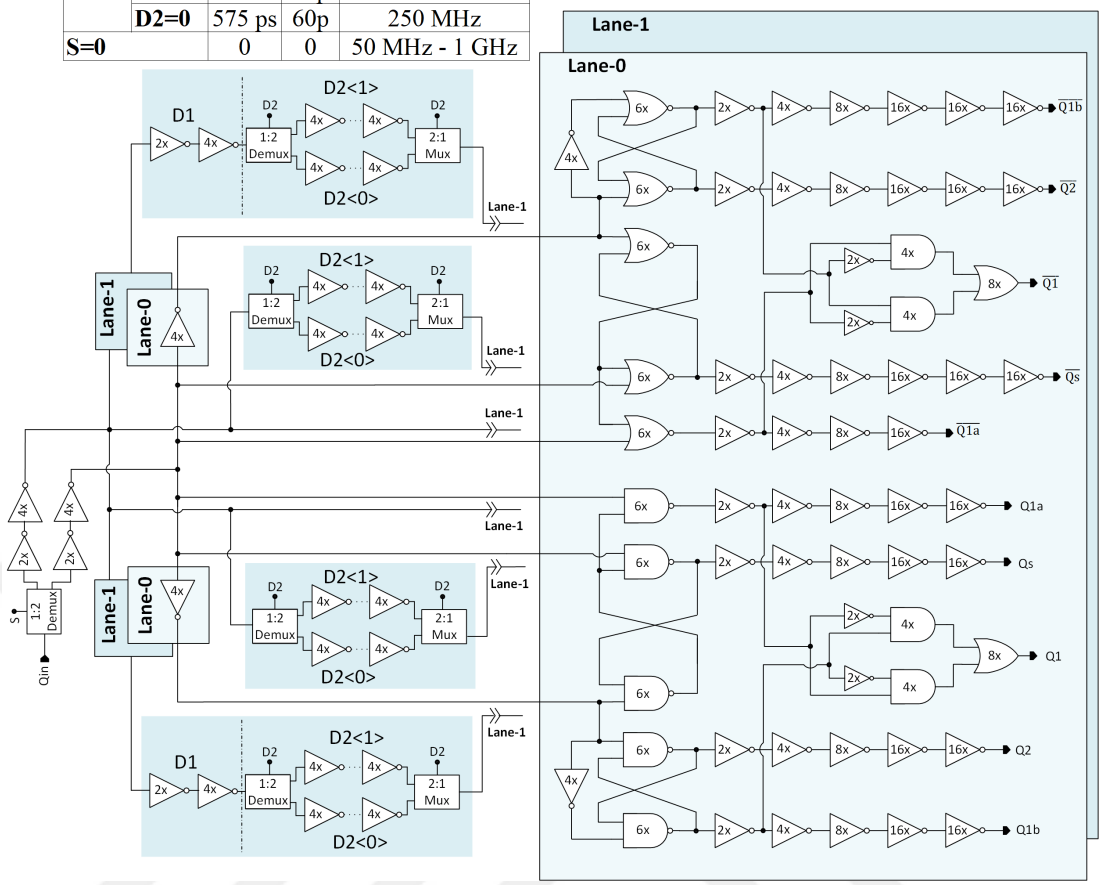


Figure 7.6 : Circuit for generating nonoverlapping clock phases [1].

amount of jitter that $LDO_{1.2V}$ contributes to the overall jitter of the clock generation architecture [1]. Within the simulation, the signal generator is assumed to be devoid of noise and has an internal impedance of 50 Ω. Additionally, the PAD drivers are omitted from consideration. The external source of signal is configured to provide a power of -0.46 dBm, which is equivalent to a voltage of 600 mVp-p at a load impedance of 50 Ω. Periodic steady state (PSS) and periodic noise (PNOISE) simulations are conducted to acquire the phase noise as a function of frequency. The frequency range for calculating the root mean square (RMS) phase jitter is from 10 kHz to 20 MHz. The SNR of ϕ_1 is achieved for both scenarios, as shown in Figure 7.4 [1].

7.2.2 External matching network for inputs

Figure 7.2c exhibits a clock source generator, an ADTL-2 18+ passive balun, a -8 dB pi-network attenuator with a characteristic impedance (Zo) of 50 Ω serving as a matching network, and a differential clock transmission line (TL) model for a FR4 test PCB. To mitigate the inductive peaking, which mostly arises from the TL and bondwire, a 50 Ω series resistor is used on each clock line [1]. The bondwires for the clock I/Os of QFN32 have a length of about 2 mm, resulting in a mutual inductance of 1.46 nH and a corresponding inductance of 2.57 nH [59]. The differential transmission line, which transmits input clock signals, spans a length of 3 cm from the SMA connections to the QFN32 package on a 2 layer FR4 PCB. The PCB has a thickness of 0.6 mm, and the line width is 0.381 mm (equivalent to 15 mils), resulting in a capacitance (Co) of 0.8 pF/cm and an inductance (Lo) of 5.1 nH/cm. The process information and dielectric constant (ε_r) of the PCB are supplied into ADS to extract the touchstone file for exact transmission line models of the differential clock lines in simulations [1]. As stated in Section 7.3, the reflection coefficient S_{11}, which represents the reflection between the impedance of the port and the input impedance of the network, is found to be below -10 dB within the frequency range of 100 MHz and 1 GHz..

7.2.3 Signal conversion: differential to single-ended

The receiver circuit, shown in Fig. 7.2a, transforms the differential signal (vip and vin) into a single-ended signal [1, 51]. The way it operates significantly affects the slopes of the clock edges, and hence, the amount of jitter that can be achieved. This study utilizes a fully-differential stage with an active load (SAL) that incorporates a continuous-time passive common-mode feedback circuit (CMFB), as seen in Fig. 7.5. The contribution of the RX jitter ($\sigma_{j_{Rx}}$) to the overall jitter of the core IC may be described using equations (7.1) and (7.2) as stated in the reference [1]:

$$\sigma_{j_{Core,Total}} = \sqrt{\sigma^2_{j_{RX}} + \sigma^2_{j_{ClkGen}} + \sigma^2_{j_{x,LDO_{1.2V}}} + \sigma^2_{j_{y,LDO_{1.2V}}}}, \tag{7.3}$$

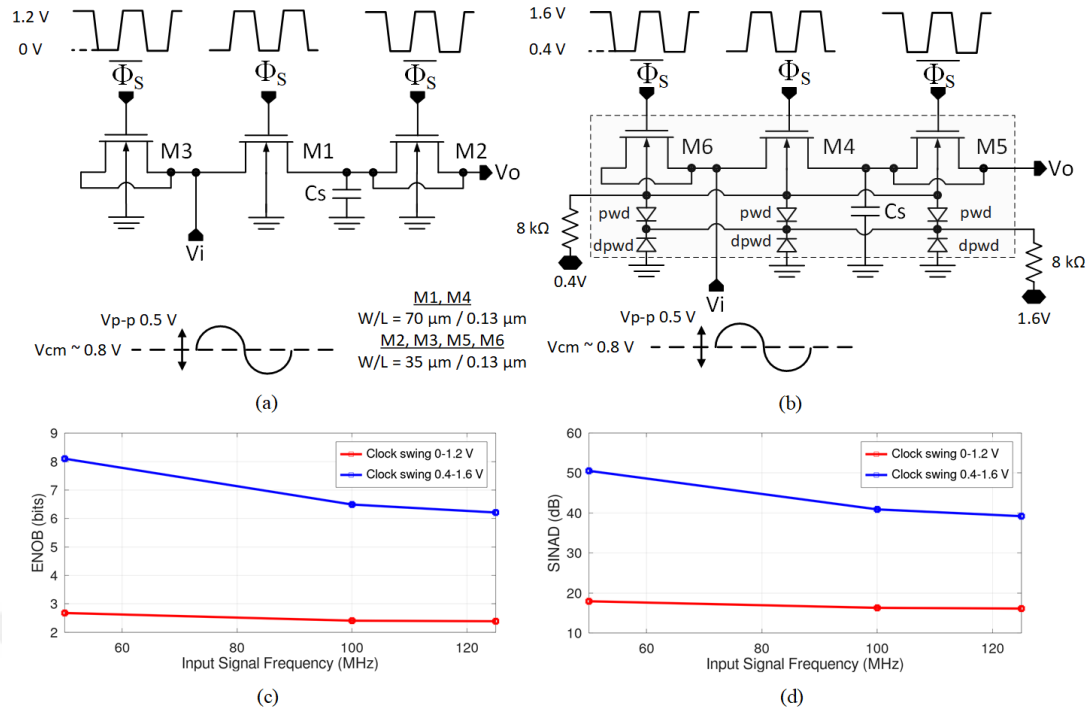


Figure 7.7 : Two dissimilar LV 1.2V thin oxide NMOS switch structures [1]: (a) usual level of the clock 0-1.2 V, (b) 0.4-1.6 V of the boosted clock level, (c) ENOB of Cs = 625 fF and fs = 250 MHz, (d) SINAD of Cs = 625 fF and fs = 250 MHz.

7.2.4 Non-overlapping clock phase generator

The timing diagram seen in Fig. 7.2b may be acquired by a simple circuit known as a clock generator, as illustrated in Fig. 7.6 [1, 7, 11]. Two lanes, lane-0 and lane-1, may be chosen by using a 1:2 demultiplexer. Lane-0 is nonproductive for ϕ_{1a}, but lane-1 generates every phase. Each delay block in lane-1 consists of a series of inverters. D1 generates a distinct transition from a high voltage level to a low voltage level, creating a distinction between the signals ϕ_S and ϕ_{1b} at the falling edge. D2 introduces an extra interval of time between the falling edge of ϕ_{1a} and ϕ_S. Additionally, ϕ_{1a} may be used to produce ϕ_1. An XOR gate may produce the output ϕ_1 by performing the XOR operation on inputs ϕ_{1a} and ϕ_{1b}. The non-overlap clock generator is implemented using a 1.2 V standard digital library in CMOS technology with a feature size of 0.13 µm.

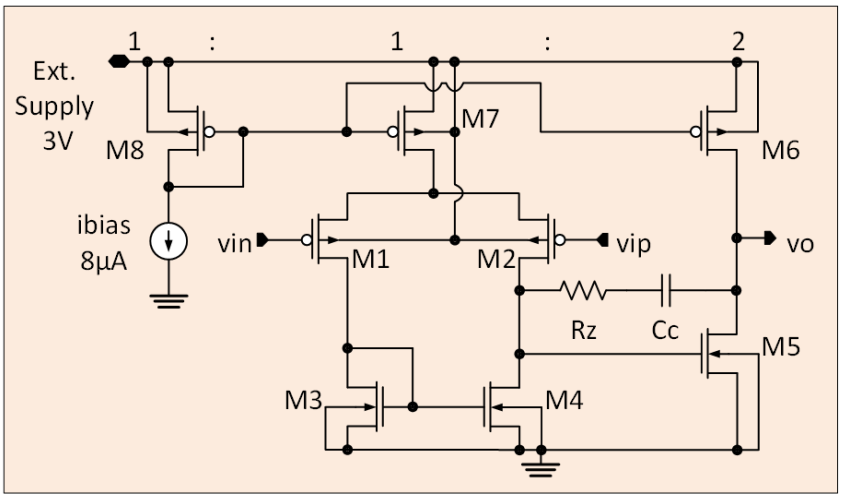


Figure 7.8 : Error amplifier [1].

7.2.5 Power management and clock level shifters

The clock level shifters are the central concept of the suggested design [1]. In addition to clock boosting, the power management system has the ability to adjust post-processing for high accuracy. As an example, the voltage reference $Vref_2$, which is set at 0.8 V, has a 3b trim. On the other hand, a 2b trim to account for PVT fluctuation is applied to each of the LDOs LDO_1, LDO_3, and LDO_6. This is shown in Fig. 7.2a, and these trims are programmed using the SPI.

7.2.5.1 Adapting level shifting technique to double-well body floating (DWBF) switches

The triple-well (TW) NMOS process is offered in the IHP SiGe BiCMOS 0.13 µm technology for mixed-signal and analog circuits. This process provides improved performance in terms of noise, linearity, isolation, and bulk control [1]. Figure 7.12a illustrates that the inclusion of the deep N-well (DNW) layer results in the formation of two additional diodes: one between the P-well (PW) and DNW, and another between DNW and P-substrate (PSUB). The diagram illustrating the TW NMOS transistor with two diodes can be seen in Fig. 7.12b. Meanwhile, the schematic representations of the DWBF NMOS switch in the on-state and off-state are shown in Fig. 7.12c. By using DNW technology, it is possible to connect huge resistors to the PW of NMOS (N-channel Metal-Oxide-Semiconductor) transistors. This allows the transistors to float at high frequencies without experiencing latch-up issues that would often occur

in a regular CMOS (Complementary Metal-Oxide-Semiconductor) process without a TW. The transient voltage of PW is really amplified by the signal voltage via a process called bootstrapping. The resistance while the switch is in the on-state, known as Ron, is responsible for the level of signal loss during insertion, particularly at lower frequencies. At high frequencies, the different capacitors will add to the overall insertion loss. The isolation of the switch in the off-state is limited because of the signal coupling that occurs via the parasitic capacitance C_{ds}, C_{gd}, C_{gs}, as well as through the junction capacitance C_{db} and C_{sb}. The parasitic capacitance resulting from PW and DNW diodes is represented by the values of C_{pw} and C_{dnw}, respectively. Due to the high frequencies at which the PW and DNW are floating, the capacitances C_{pw} and C_{dnw} are linked in series. Consequently, the corresponding parasitic well capacitance is degraded [1].

When the source and PW terminals are linked as shown in Fig. 7.12d, the source terminal is directly affected by C_{pw}, which is much bigger than the junction capacitance of C_{sb} [1]. As shown in Fig. 7.12e, the capacitance C_{pw} is present in the circuit model of the TW linked to the source NMOS switch, both in the on-state and off-state. Due to the short connection between the DNW and its bias voltage, the capacitance C_{dpw} may be disregarded. During operation, the presence of C_{pw} negatively impacts both the performance of the switch in terms of linearity and bandwidth. Similarly, when the switch is not in use, the reverse isolation is compromised. Therefore, the source terminal is often not linked to the PW terminal for applications involving high frequency [1].

Figure 7.7a illustrates the configuration of the LV 1.2 V NMOS switch, M1, which is equipped with two dummy transistors, M2 and M3, to minimize clock feedthrough at its two I/O terminals. Additionally, a sampling capacitor, C_S, is connected to V_o [1]. The switch M1, with its body terminal grounded, is controlled by a standard clock signal ranging from 0 to 1.2 V. If we assume that M1 exhibits square law behavior and that the value of V_{DS} is minimal, the expression for R_{on} can be derived as [54]:

$$R_{on} = \frac{1}{\mu_n \times C_{ox} \times \frac{W}{L} \times (V_{GS} - V_{th})}, \tag{7.4}$$

where V_{th} is threshold voltage, C_{ox} is the gate oxide, and μ_n is the mobility of the NMOS transistor. During the conduction phase with a gate voltage of 1.2 V, R_{on} will vary based on the input signal, V_i, in two ways [1]. First, V_{GS} is equal to V_{DD} - V_i.

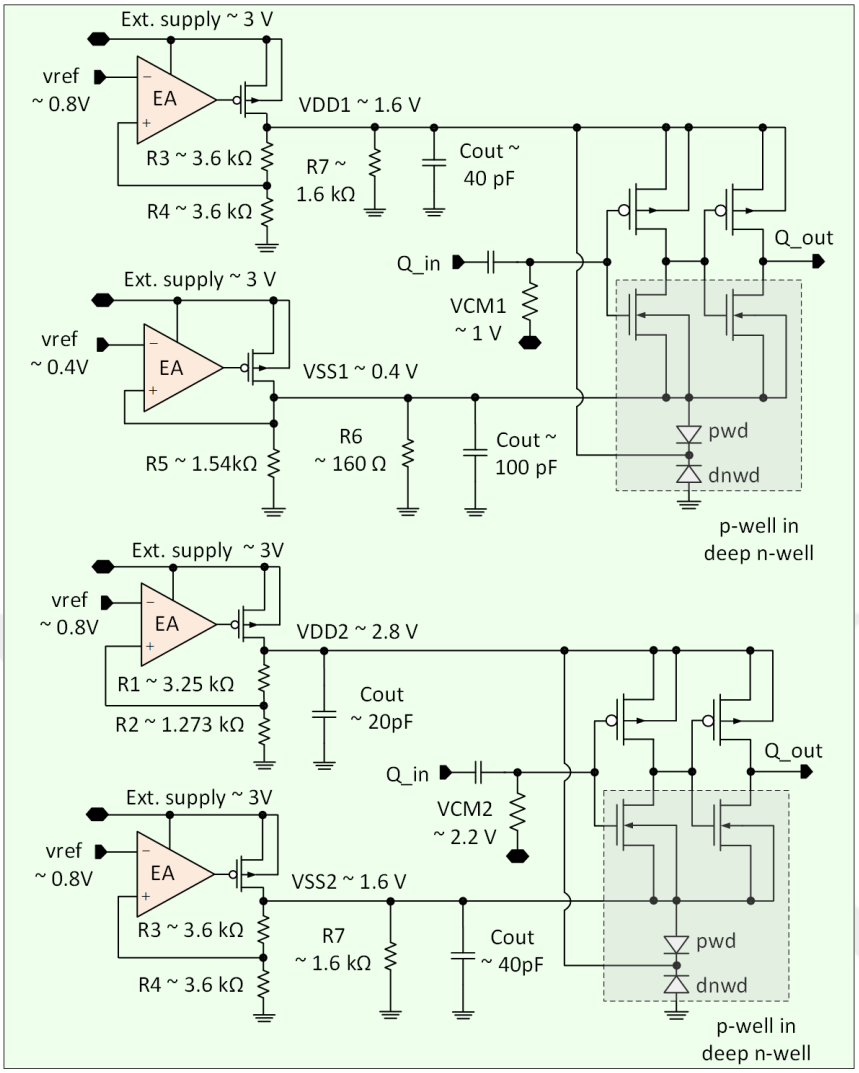


Figure 7.9 : Clock level shifters [1].

Second, V_{th} is influenced by V_i via the source-body voltage, V_{SB} [54]:

$$V_{th} = V_{tho} + \gamma_n \times \left(\sqrt{2 \times |\phi_f| + V_{SB}} - \sqrt{2 \times |\phi_f|} \right), \tag{7.5}$$

where γ_n is the back gate effect parameter and V_{tho} is threshold voltage with $V_{SB} = 0$. Elimination of first-order fluctuations in V_{th} could be obtained by setting V_{SB} to zero, which implies that the source and body of M1 are connected. Nevertheless, this can only be achieved if the device M1 is integrated into its own distinct PW. However, it may not be preferable to shorten the body and source because of the significant parasitic capacitance linked to the PW. To achieve optimal performance in applications that involve rapid processing of data, it is crucial to minimize the negative effects of parasitic capacitances as much as feasible [1]. One common design approach is to enlarge the width of device M1 such that even at the highest and lowest levels of the input signal, V_i, the value of R_{on} stays within an acceptable range [1]. The bandwidth

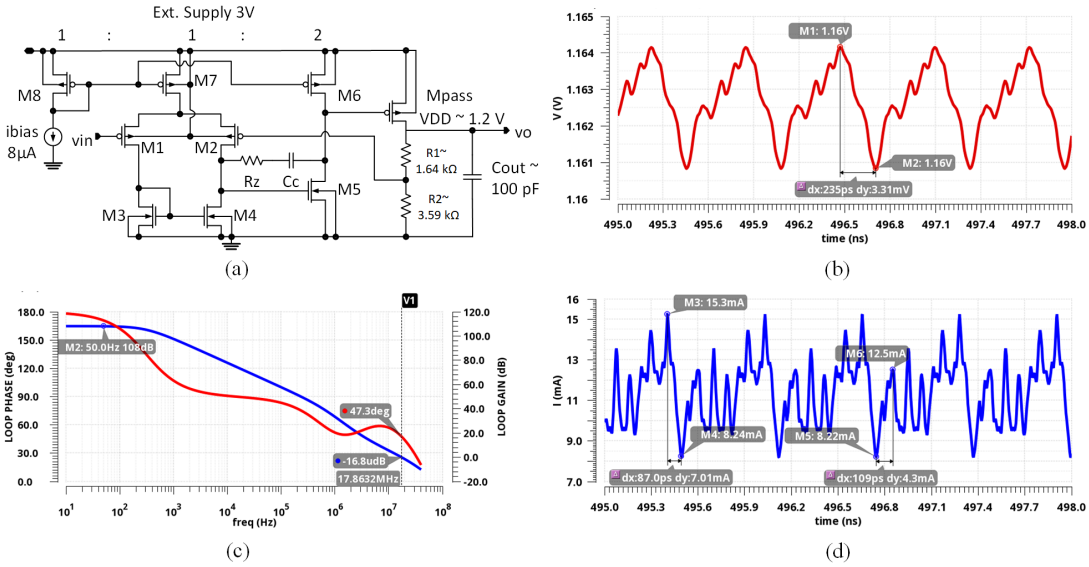


Figure 7.10 : The performance of the LDO operating under 1.2 V [1]: (a) The circuit structure of the LDO, (b) Load transient voltage regulation when the clock signal is at 1 GHz, (c) Diagrams of the loop transfer function quantifying magnitude and phase, (d) Load transient current when the clock signal is at 1 GHz.

of the sampling circuit in Fig. 7.7a, denoted as f_{-3dB}, is given by the expression provided in the reference [54]:

$$f_{-3dB} = \frac{1}{2\pi \times R_{on} \times Cs} = \frac{1}{2\pi} \times \frac{\mu_n \times C_{ox} \times \frac{W}{L} \times (V_{GS} - V_{th})}{Cs}. \tag{7.6}$$

To provide adequate performance for resolutions between 8-14b, it is recommended to size M1 so that the minimum -3 dB cut off frequency is roughly 5x to 10x larger than the bandwidth (fb) of the input signal [1]. Nevertheless, this poses a challenge when the dimensions of the technology decrease with the power supply voltage. As the gate lengths of conventional devices decrease, the scaling of V_{th} is not as fast as that of V_{DD}. Consequently, the gate-source overdrive on M1 decreases. Hence, based on (7.4), it can be deduced that the width of M1 has to be enlarged in order to maintain Ron at the previously accepted low level. Eventually, the self-loading caused by the parasitic capacitance from M1 will reduce the -3 dB bandwidth of the circuit by an unacceptable degree. Moreover, when the size of switches increases, there is a subsequent rise in charge injection mistakes and clock driver loads [1]. When it comes to the limitations on parasitic capacitance and charge injection, achieving a suitably low value for Ron over the whole input signal range only by using large device sizes may be challenging [1]. This challenge is compounded by the fact that although the

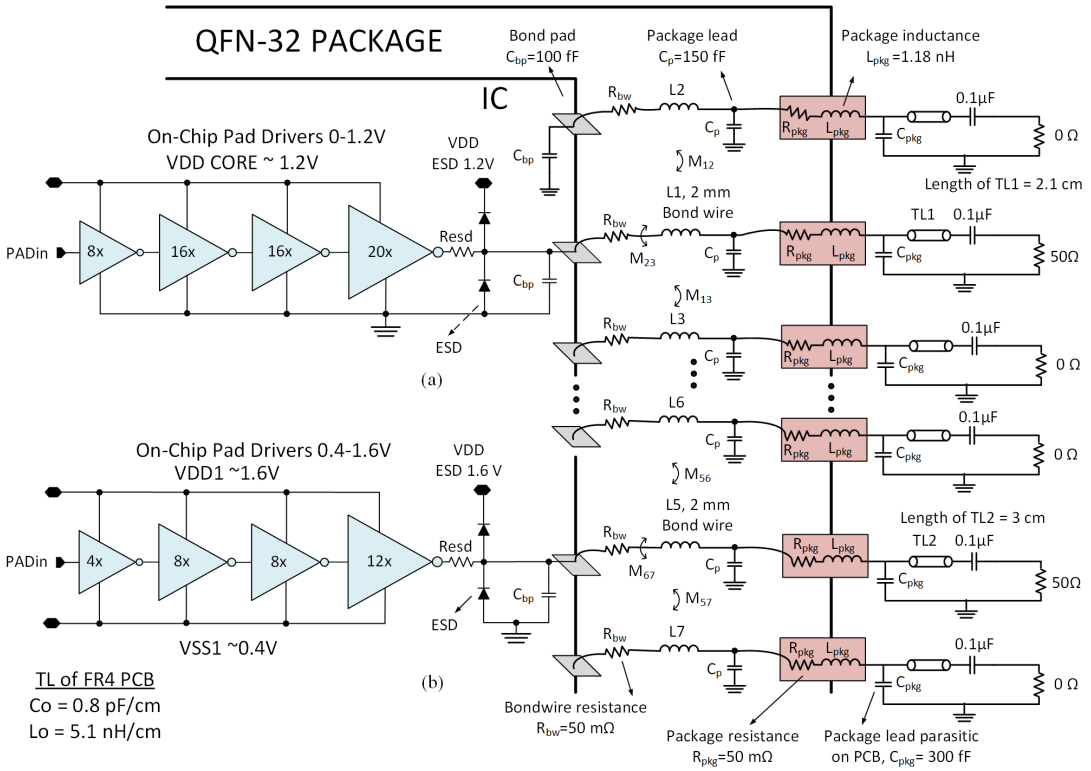


Figure 7.11 : The voltage ranges for the pad drivers [1]: (a) ground-power (0-1.2 V), (b) ground-power (0.4-1.6 V).

supply voltage may decrease with technological advancements, the input signal range must stay reasonably consistent to prevent a decrease in dynamic range [1].

As previously stated, just extending the width of the standard switch does not significantly enhance the bandwidth and SINAD of the sampling circuit [1]. The triple-well switch shown in Fig. 7.7b is suggested for optimal performance. The operation is governed by a clock signal ranging from 0.4 to 1.6 V. By connecting the body terminal of the triple-well switch, M4, to a large floating resistor that is attached to 0.4 V, the activation of the source-bulk and drain-bulk diodes by large signals is prevented, resulting in enhanced linearity [60]. Nevertheless, the diode connecting the PW and deep N-well remains vulnerable. In order to overcome the limitation of the body-floating, it is necessary to float the deep N-well using an 8 kΩ resistor, which should be connected to a voltage of 1.6 V. The diode between the P-well and deep N-well is safeguarded when both terminals are floating [1]. The DWBF approach results in a little contribution of parasitic capacitance from the P-well and deep N-well to the signal channel of the switch [1].

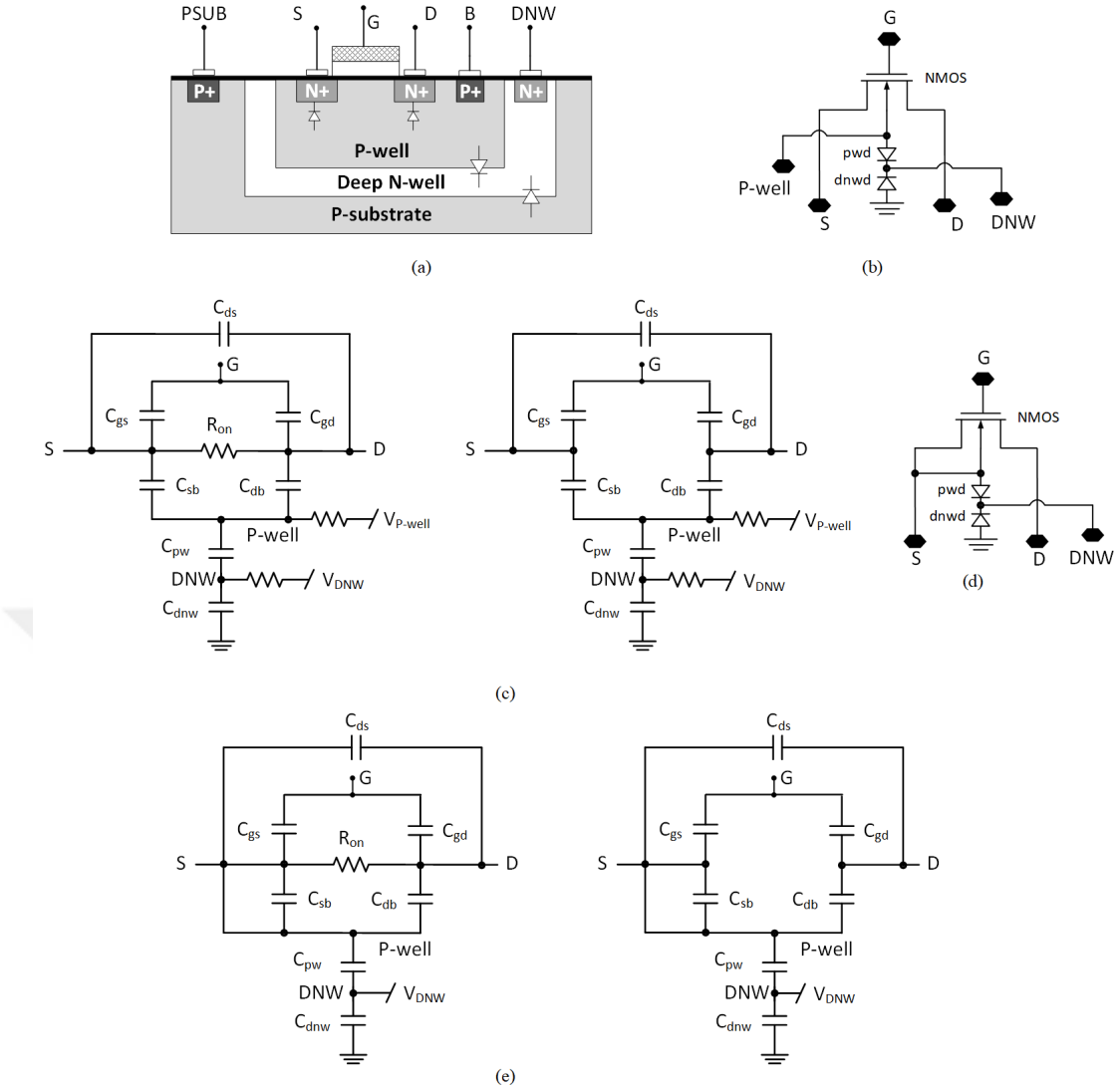


Figure 7.12 : (a) Basic transverse illustration of a NMOS transistor in TW technology [1], (b) Model schema of the NMOS transistor in TW [1], (c) Model schema of the DWFB NMOS switch in on-state and off-state [1], (d) Model schema of the PW tied to source terminal of the NMOS transistor [1], (e) Model schema of the PW tied to source terminal of the NMOS switch in on-state and off-state [1].

As seen in Fig. 7.7c and d, the level shifted switch exhibits better SINAD and ENOB performance compared to the standard switch [1]. The clock boosting approach involves increasing the gate voltage, which leads to a drop in Ron and a rise in f_{-3dB}, as described by (7.4) and (7.6), respectively. Additionally, the M4 exhibits superior performance in terms of noise reduction, isolation, and body stability [1]. The DWBF switches with the clock-boosted technique are deployed in the residue amplifier and bootstrap switches, and multiplying digital-to-analog converters (MDAC) of the pipelined ADC, as described in [1, 2, 5, 6].

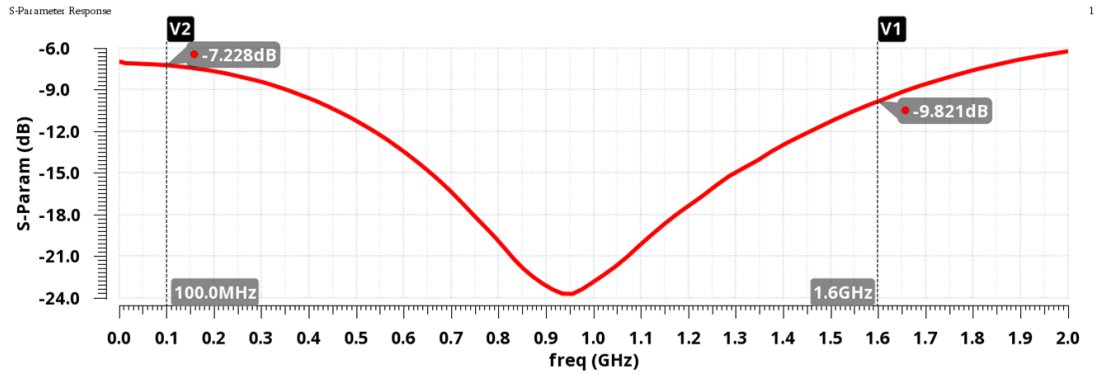


Figure 7.13 : S11 of the clock generation system [1].

7.2.5.2 Power management

The voltage between the transistors' terminals must stay within the specified voltage limitations of the technology [1, 2, 7, 19, 55]. The clock level shifters, shown in Fig. 7.2e, adjust the voltage levels of the clock phases ϕ_S, ϕ_{1a}, and ϕ_2 to the desired levels, as seen in Fig. 7.2a. The integrated circuit (IC) is powered by a 3 V external source and this voltage is divided into various voltage levels using six low-dropout regulators (LDOs). The method utilizes thick oxide transistors to adjust the required voltage levels. The thick oxide transistors have the ability to withstand a voltage stress of up to 3 V across their terminals. The non-overlap clock generator and Rx are powered by LDO_1. The voltage levels for the clock level shifters are generated by the LDO_{2-6}. In Fig. 7.2f, the two-stage error amplifier (EA) used in the LDO_{2-6} is made stable by using a compensation capacitor, Cc, with a value of 2.25 pF, and a nulling resistor, Rz, with a value of 23.7 kΩ. In Fig. 7.2e, two distinct voltage ranges can be observed: The first range spans from 0.4 to 1.6 V, while the subsequent range extends from 1.6 to 2.8 V. Each clock used in the level shifter [19] is equipped with an AC coupling capacitor that operates with a DC bias voltage of $VCM_{1,2}$ for thin-oxide inverters. These inverters are responsible for driving the switches of the pipeline ADC [7]. The LDO_2 and LDO_5 produce the VCM_1 and VCM_2 signals, respectively. The clock level shifters use NMOS transistors that are implemented in pwell. Each pwell is linked to either VSS_1 or VSS_2. The LDO_3 sets VSS_1 and the LDO_4 sets VSS_2. R_6 and R_7 serve as dummy load resistors, which expedite the discharge time for the accumulated charge on the load capacitors.

The RX and clock phase generating circuits are powered by LDO_1, which supplies a voltage of 1.2 V, as shown in Fig. 7.10a. The stabilization is achieved by using a compensating capacitor, Cc, with a capacitance of 4.8 pF, in conjunction with a nulling resistor, Rz, with a resistance of 20 kΩ. The controlled voltage at the output of the low-dropout regulator LDO_1 will be used to charge the load capacitor C_{Load} and provide power to the sub-circuits. The stability and load control performance of the LDO_1 are directly influenced by this capacitor. Increasing the capacitor value enhances the responsiveness of the LDO_1 to sudden variations in the load current, leading to improved transient regulation performance [61]:

$$\Delta V_{tr,max} = \frac{I_{o,max}}{C_{Load}} \times \Delta t_1. \tag{7.7}$$

where Δt_1 represents to the closed loop bandwidth. An on-chip load capacitor of 100 pF is used to reduce fluctuations at the output terminal. The MOS capacitors were used to construct the 100 pF capacitor. The design analysis concluded that a single NMOS with a width of 10 μm and a length of 10 μm could provide a capacitance of roughly 400 fF. By connecting 250 cells in parallel, the total capacitance may reach up to 100 pF. Due to regulation of the output, the capacitance value of the MOS capacitor stays constant. The LDO_1 exhibits a unity gain bandwidth of 17.8 MHz and a phase margin of 47^o while operating under a DC load current of 12 mA, as seen in Fig. 7.10c. The dynamic load current exhibits a maximum instantaneous change of 7 mA during a 90 ps timeframe, when subjected to a 1 GHz clock signal. The change causes a voltage fluctuation of 3.3 mV at the LDO's output terminal. As shown by the simulations, the ripples mostly result in a drop of 10 dB in SNR beyond a clock frequency of 800 MHz, as shown in Fig. 7.4. Although the output of LDO_1 does not use any current, it exhibits a power supply rejection ratio (PSRR) performance of over 48 dB at 10 Hz and 43 dB at 10 kHz. When a current of 60 mA is taken from the output of the LDO_1, the PSRR is 47 dB at a frequency of 10 Hz and 40 dB at a frequency of 10 kHz.

7.2.6 Level shifted pad drivers

Pad drivers are equipped with two distinct voltage ranges for measuring purposes: 0 - 1.2 V and 0.4 V - 1.6 V, as seen in Fig. 7.11 [1]. ESD diodes provide protection for both driver inverters [1]. To ensure accurate jitter estimation in the simulations, various electrical components are modeled. The electrical model is depicted in Fig. 7.11 [1].

After designing the pad frame of the IC, there was a need to allow several output clock signals concurrently [1]. The signals are sent from the IC pads to the package leads by bondwires. Using this method, we could individually or collectively measure various signals. Alternatively, a n:1 multiplexer could be used to decrease the quantity of output pads. However, this will introduce more jitter. The measured clock signal could suffer degradation in its jitter over time [1].

Within an IC package, signals are introduced and discharged by signal leads, while they are routed back via power leads [59]. Inductance may be computed for either an unconnected pathway or a segment of a complete circuit. This study specifically examines the open circuit route, which consists of a signal lead and two neighboring signal leads, as seen in Fig. 7.11 [1]. The bondwire length from the IC clock output pad to its equivalent QFN32 lead in our design measures around 2 mm, resulting in an inductance of roughly 2.57 nH. In order to examine the impact of inductive coupling on jitter performance, we have created models for the three mutual inductance characteristics of the closest three bondwires. For example, L_1 is positioned between L_2 and L_3, resulting in the definition of M_{12}, M_{13}, and M_{23}. Like L_1, L_5 is positioned between L_6 and L_7, thus enabling the determination of mutual inductance parameters M_{56}, M_{57}, and M_{67}. In our simulation, we make the assumption that the values of M_{12}, M_{13}, M_{56}, and M_{67} are all equal to 1.46 nH. When testing one of the output clock terminals, the neighboring clock outputs are terminated with a 0 Ω resistance to reduce cross talk caused by mutual inductance and PCB traces [1].

7.3 Review of Simulations

In this section, the performance metrics of the clock phase generator are given such as power consumption, silicon area, S11, RMS phase jitter, transient waveforms, duty cycle, operating frequency range. In order to report those metrics, transient and periodic steady state simulations are run for RC-typical layout extraction.

Moreover, the pad drivers are not included into the simulations, thus the jitter performance of the core system is reported.

The simulations are run under the following conditions: typical corner, 25^{o}C, and typical supply voltage levels.

7.3.1 Simulations: AC s-parameter

In Fig. 7.2c, the input matching network is depicted. By utilizing a minicircuit ADTL2-18 balun, differential input clock signals can be produced. The touchstone file of the passive balun is imported into the simulation environment. S11 is obtained below -10 dB from 0.4 GHz up to 1.6 GHz as in Fig. 7.13.

7.3.2 Simulations: transient

During the transient simulations, the signal generator is considered to be free of noise and has an internal impedance of 50 Ω. The external source of signal is configured to provide a power of -0.46 dBm, which is equivalent to a voltage of 600 mVp-p at a load impedance of 50 Ω. The transient voltages at the input terminal of the passive balun, each of the input terminals, and the differential input signal of RX are shown in Fig. 7.14. The optimal power transfer occurs at a clock frequency of 800 MHz.

The time-varying patterns of ϕ_{1b}, ϕ_1, ϕ_2 are acquired at input frequencies of 0.2 GHz, 0.4 GHz, 0.8 GHz, and 1.6 GHz, as shown in Fig. 7.15. The figures in Fig. 7.16 represent $\phi_{S,1.6V}$, $\phi_{S,2.8V}$, and $\phi_{2,1.6V}$ for the same operating frequencies.

There is also ϕ_{1a} and $\phi_{1a,1.6V}$, which are the inter-phases for ISI clearing and functional at 75 MHz and 250 MHz.

7.3.3 Simulations: periodic steady state

periodic noise (PNOISE) and Periodic steady state (PSS) simulations are conducted in order to get the phase noise as a function of frequency. The frequency range for calculating the root mean square (RMS) phase jitter is from 10 kHz to 20 MHz. Figure 7.18 illustrates the phase noise of the ϕ_1 at different frequencies of the external source of signal, with an amplitude of 600 mVp-p.

Higher input clock frequency leads to an increase in the rise and fall period of the clock phases. Except for the jitter component caused by PAD drivers, as in (7.2), SNR_{jitter} of ϕ_1 is 72 dB for f_{clk} at 100 MHz, and 60 dB for f_{clk} at 1 GHz as shown in Fig. 7.19. Reducing slew rate makes the asynchronous logics to be more vulnerable to changes in the zero crossing point of the clock signal [62].

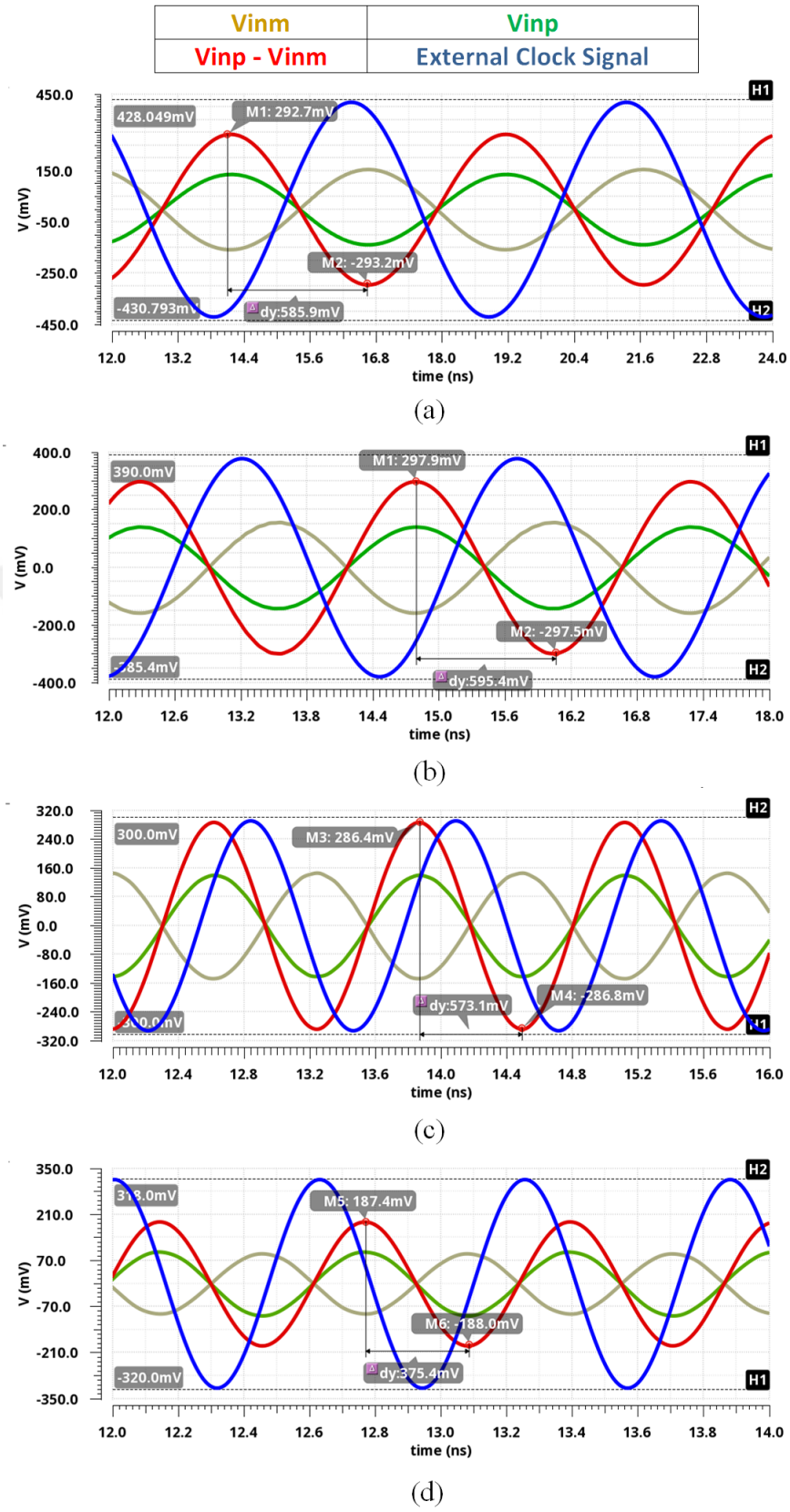


Figure 7.14 : f_{clk} of external source of signal with an amplitude of 600 mVp-p, simulated for [1]: (a) 0.2 GHz, (b) 0.4 GHz, (c) 0.8 GHz, (d) 1.6 GHz.

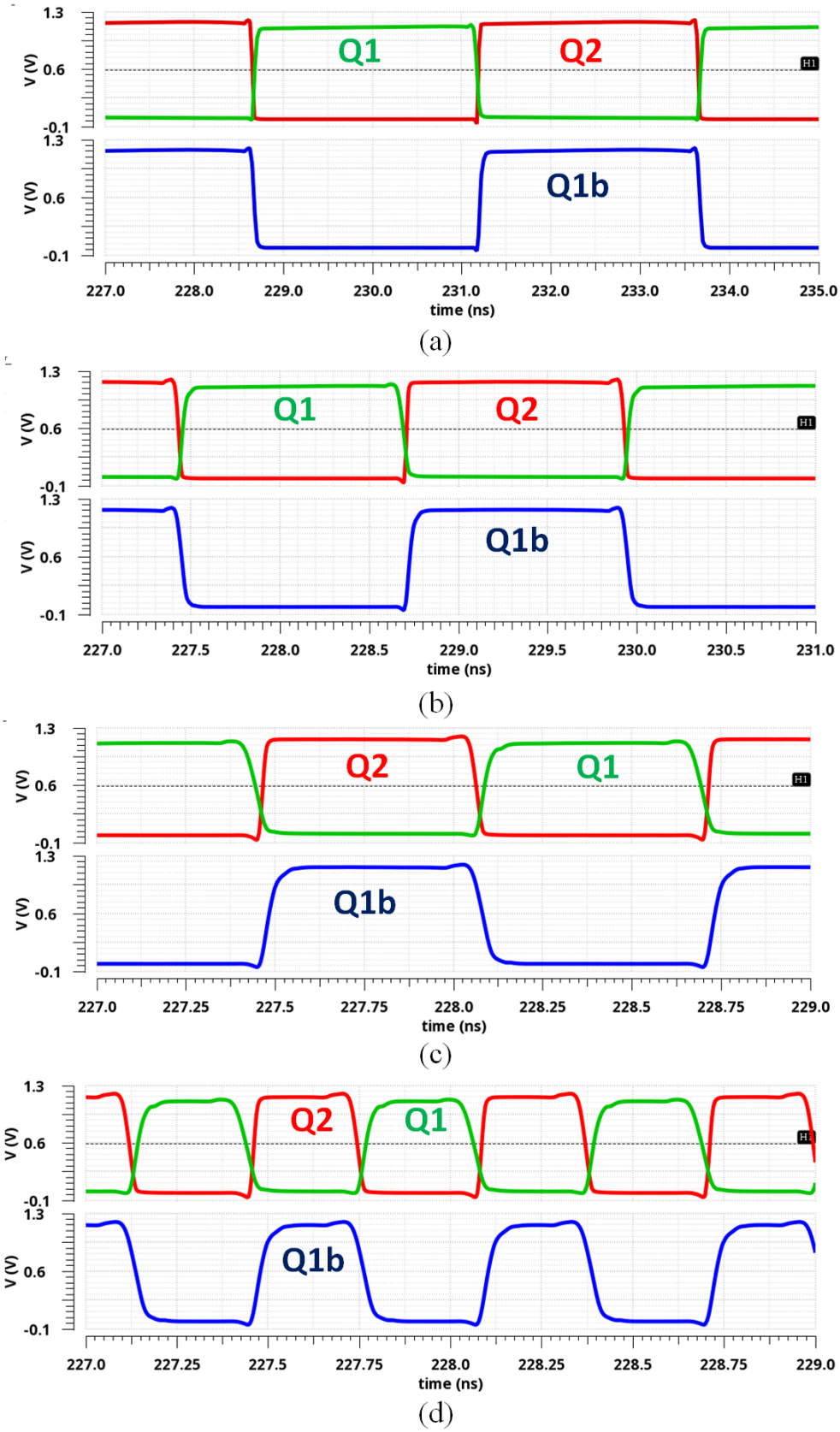


Figure 7.15 : ϕ_1, ϕ_{1b} and ϕ_2 for f_{clk} of external source of signal with amplitude of 600 mVp-p when S=0 [1]: (a) 0.2 GHz, (b) 0.4 GHz, (c) 0.8 GHz, (d) 1.6 GHz.

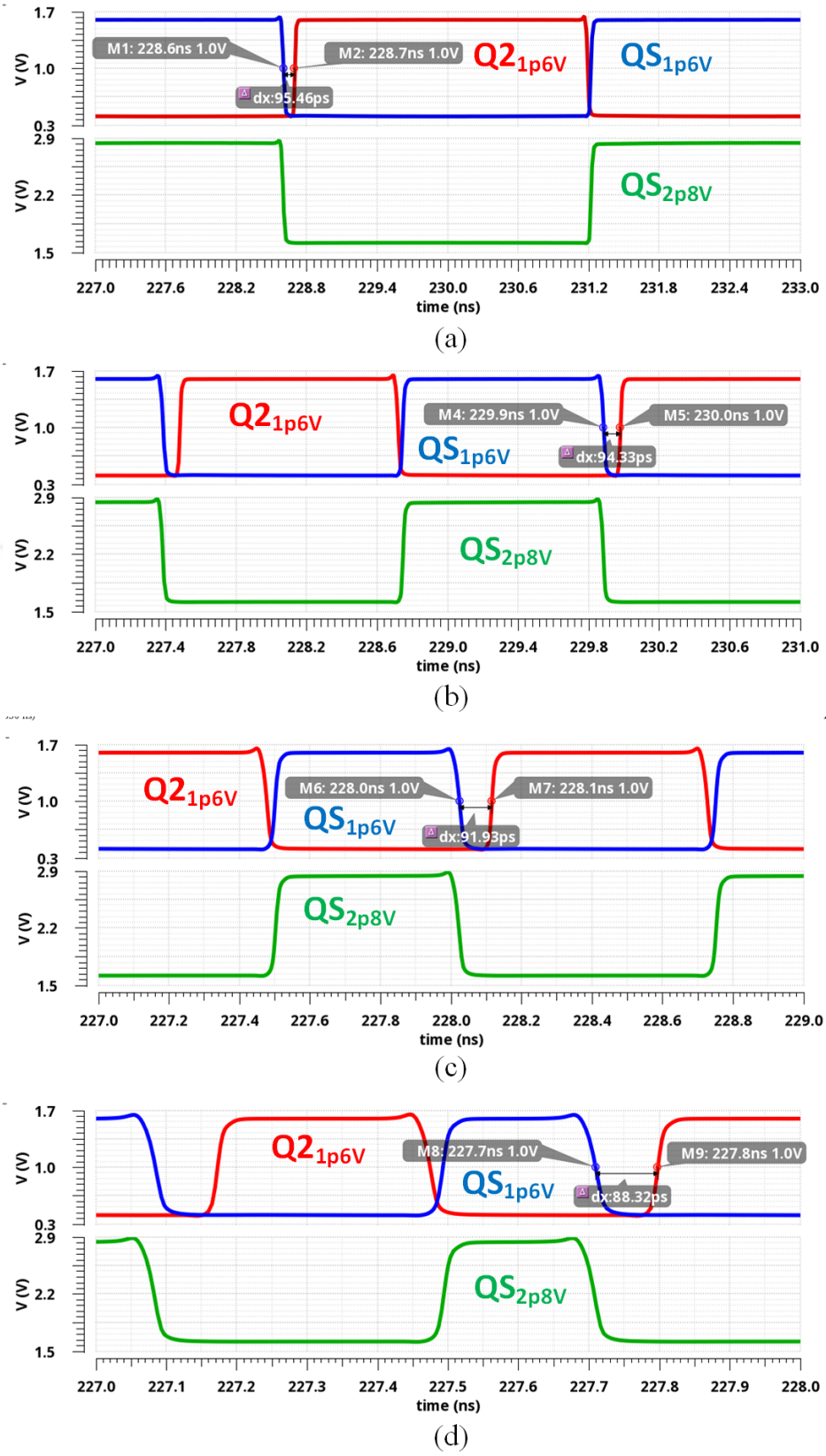


Figure 7.16 : $\phi_{S,1p6V}$, $\phi_{S,2p8V}$ and $\phi_{2,1p6V}$ for f_{clk} of external source of signal with an amplitude of 600 mVp-p when S=0 [1]: (a) 0.2 GHz, (b) 0.4 GHz, (c) 0.8 GHz, (d) 1.6 GHz.

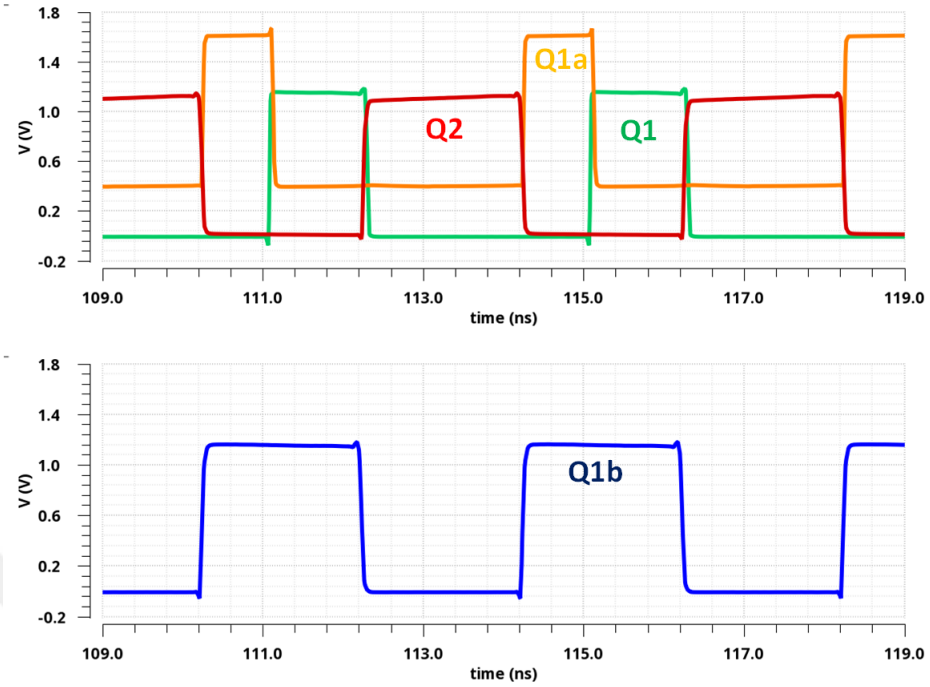
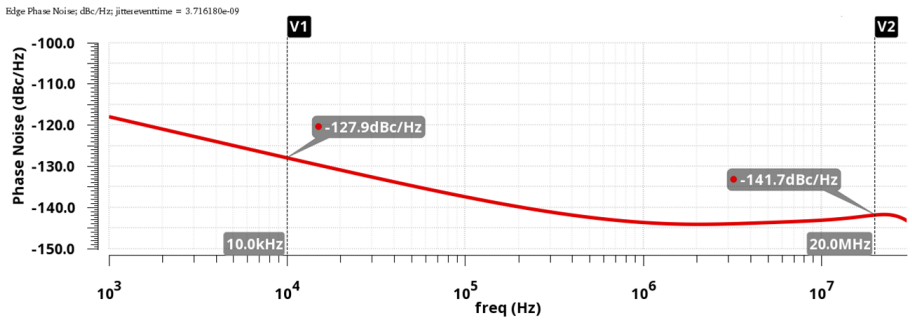


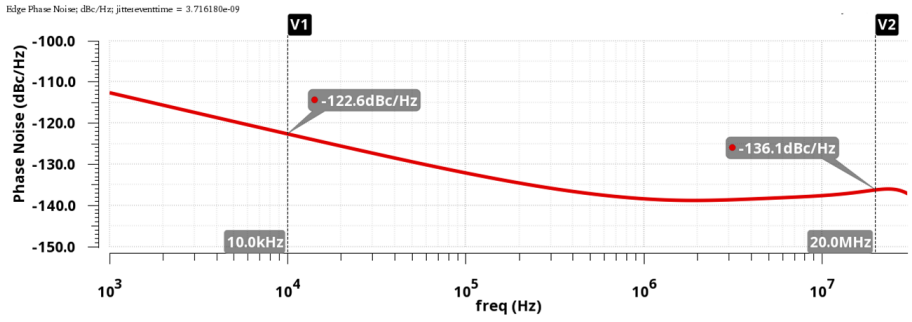
Figure 7.17 : $\phi_{1a,1p6V}$, ϕ_2 and ϕ_1 for f_{clk} of external source of signal at 250 MHz with an amplitude of 600 mVp-p when S=1, D=1 [1].

Table 7.1 : Performance summary [1]

	Description
Supply voltage	3-3.3 V
Architecture	Ext. Clock + Phase Gen
Measurement	Simulation
$\sigma_{j_{ext,clk}}$ (RMS)	0.249 ps @200 MHz, 62 fs @1 GHz (10 kHz-20 MHz)
fclk	50 MHz to 1 GHz
Number of Phase	11
Multi-level	0-1.2V, 0.4-1.6V, 1.6-2.8V
Power	57 mW @1 GHz)(BGR+LDOs+RX+ClkGen)
Silicon area	360 μm $\times$ 460 μm
$\sigma_{j_{\phi_{1,2,1b}}}$ (RMS)	0.51 ps @200 MHz, 0.29 ps @1 GHz, $\phi_{1,2,1b}$ (10 kHz-20 MHz)
S_{11}	-10dB @ 0.1-1 GHz



(a)



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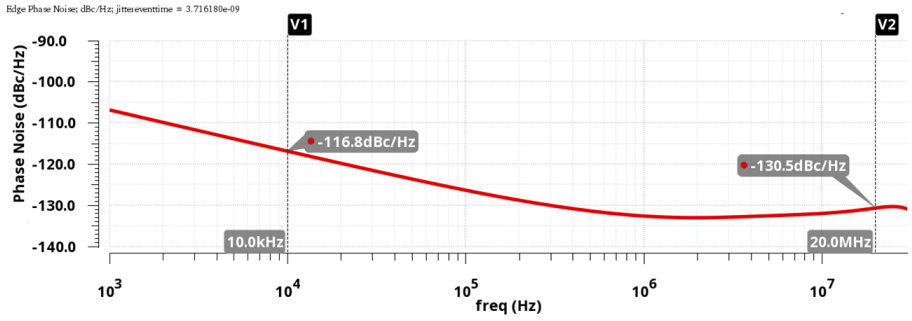

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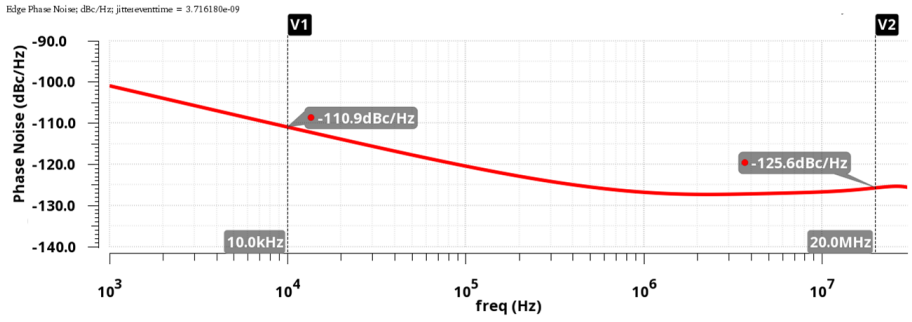


(d)

Figure 7.18 : Phase noise of Q_1 for various f_{clk} of external source of signal with 600 mVp-p, simulated by PSS+PNOISE for f_{off} between 10 kHz and 20 MHz [1]: (a) 0.2 GHz, (b) 0.4 GHz, (c) 0.8 GHz, (d) 1.6 GHz.

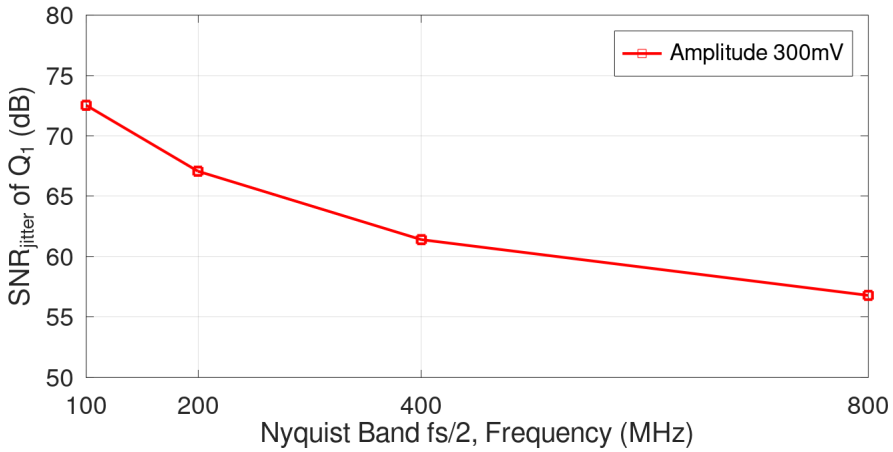


Figure 7.19 : SNR_{jitter} of ϕ_1 vs fs/2 for signal amplitude at 600mVp-p [1].

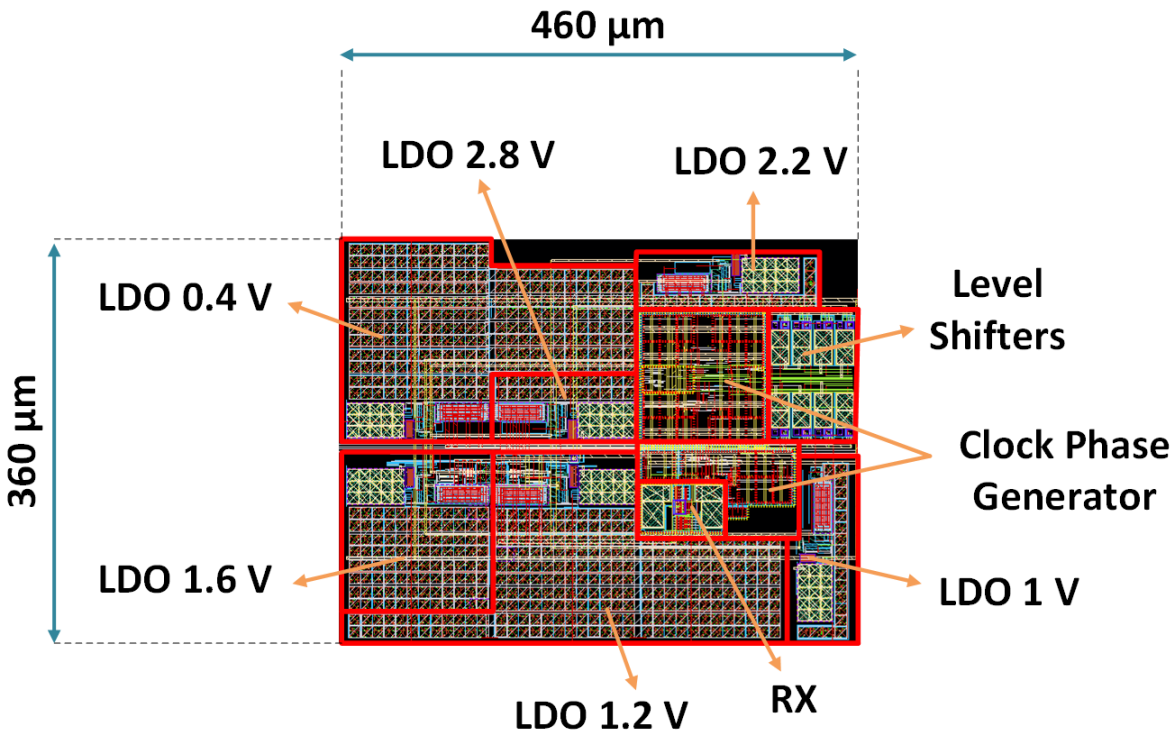


Figure 7.20 : Clock generation core layout with 360 μm$\times$ 460 μm [1].

7.3.4 Conclusion

In Table 7.1, the performance metrics of the clock generation circuit are summarized. The clock generating system draws a current of 19 mA when operating at a frequency of 1 GHz and being powered by an external source of 3 V. The design occupies a silicon area of 360 μm × 460 μm in a SiGe BiCMOS 0.13 μm process, excluding interface circuitry and I/O pads. The suggested integration of RF-analog approaches may be used in creating a high-speed, completely integrated, cost-effective, and low-power non-overlapping clock generator architecture.

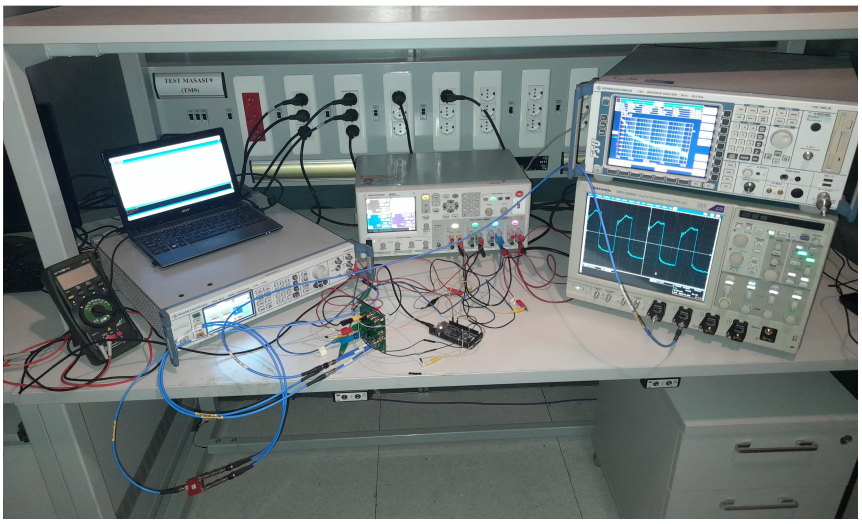
8. SIMULATION AND EXPERIMENTAL RESULTS

In this work, a one way pipeline ADC, having sampling frequencies up to 1.6 GS/s in a SiGe BiCMOS 0.13 μm is presented. For our ADC, sample-and-hold amplifier-less (SHA-less) architecture was preferred since the SHA was one of the most power-consuming sub-blocks, and brought inevitable noise and distortion. A composite ADC architecture, having 8x 1.5-b cascaded stages and a back-end 3-b flash ADC is designed to reach up to 11-b resolution. The entire ADC, which is supplied with 1.6 V and occupies a silicon area of 2.2 mm × 3 mm, is fabricated using a SiGe BiCMOS 0.13 μm process [APPENDIX-A].

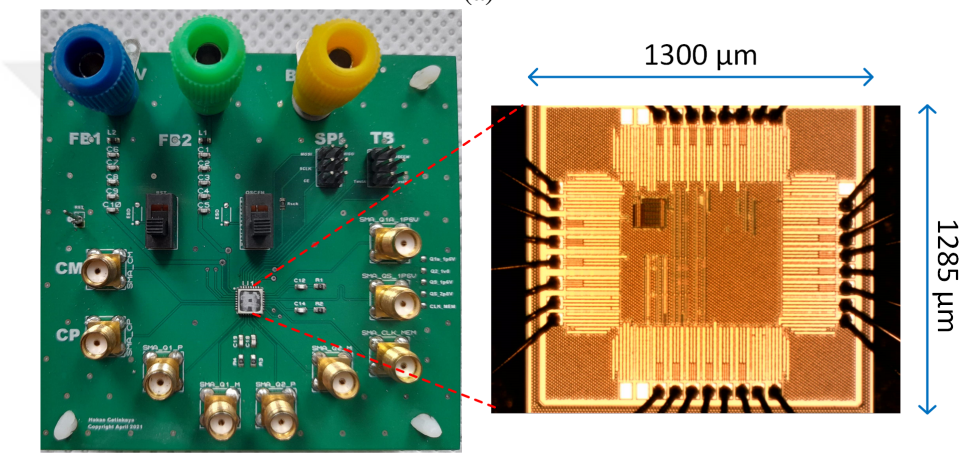
8.1 Measurement Results for Clock Phase Generation

The measurement was performed at the ITU VLSI Labs. The measuring equipment was set up in the Faraday Cage, as shown in Fig. 8.1a, to provide protection from ambient electromagnetic interferences (EMI) [1]. In Fig. 8.1a, the R&S SMA100A signal generator was used to provide the input clock signals for the test PCB, which had a QFN32 package mounted on it. The Agilent N6705B DC power supply, demonstrated in Fig. 8.1a, offers various power supply levels for the test PCB. The Mini-circuit ADTL2-18 balun was used to acquire differential input clock signals, which were then linked to the clock input SMA connectors of the PCB. The Arduino Due microcontroller was used for programming the SPI [APPENDIX-C]. Figure 8.1b shows the 2 layer FR4 PCB and the chip photograph.

The transient waveforms of QFN32-ϕ_1 and QFN32-ϕ_2 are shown in Fig. 8.2, for external signal sources with frequencies of 200 MHz, 400 MHz, 700 MHz, and 1 GHz, and amplitudes of 600 mV_{p-p}. The QFN32-$\phi_{S_{1.6V}}$ is shown in Fig. 8.3 with the same f_{clk} and input signal power. Figure 8.4 illustrates the process of adjusting the duty cycle for QFN32-ϕ_1 at frequencies of 75 MHz and 250 MHz. With an increase in the input clock frequency (f_{clk}), the rise and fall time of the clock phases also increase at the package output terminals. A decrease in the pace at which the pad drivers change



(a)



(b)

(c)

Figure 8.1 : (a) İTÜ VLSI Laboratories' Faraday Cage measurement apparatus, (b)QFN32 package mounted on a test PCB along with an image of the prototype chip, (c) Thermal chamber ESPEC BTZ-175E for PCB testing.

their output voltage makes them more vulnerable to changes in the point at which the clock signal crosses zero [62]. Regarding the transient waveforms, we detect ground

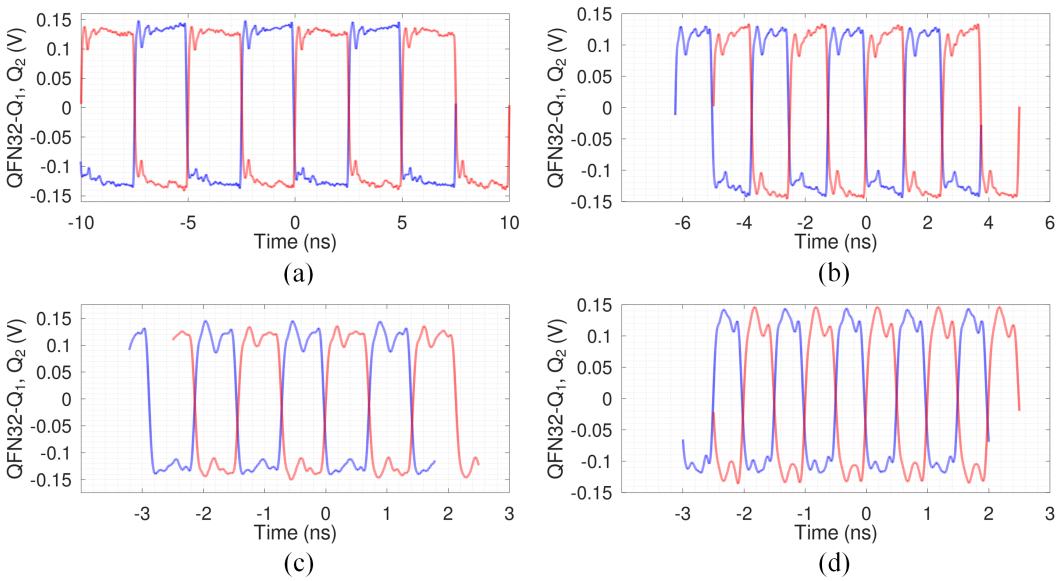


Figure 8.2 : For diverse f_{clk}, measured by oscilloscope, QFN32-ϕ_1 (blue) and QFN32-ϕ_2 (red): (a) 0.2 GHz, (b) 0.4 GHz, (c) 0.7 GHz, (d) 1 GHz.

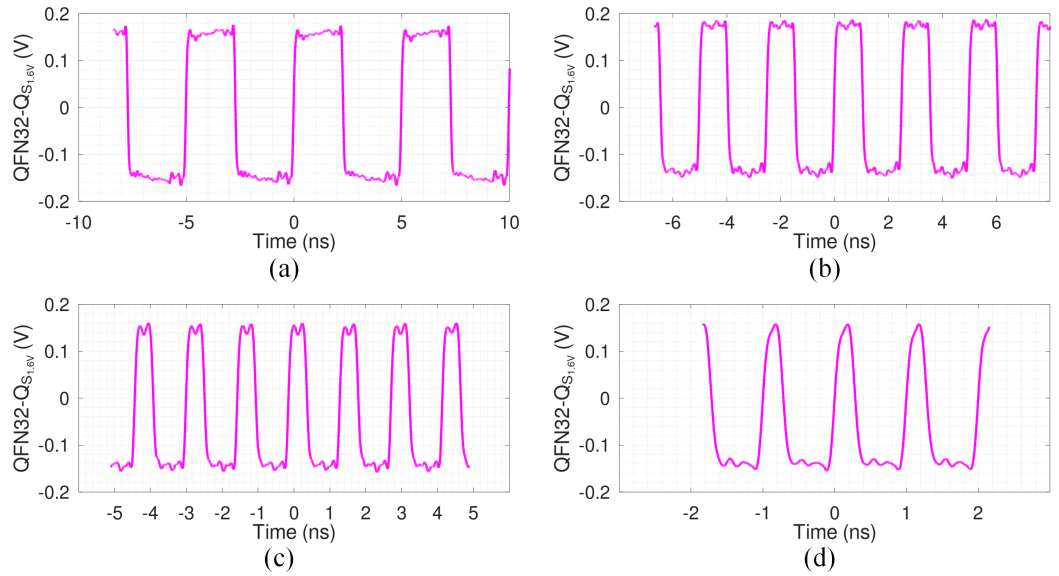
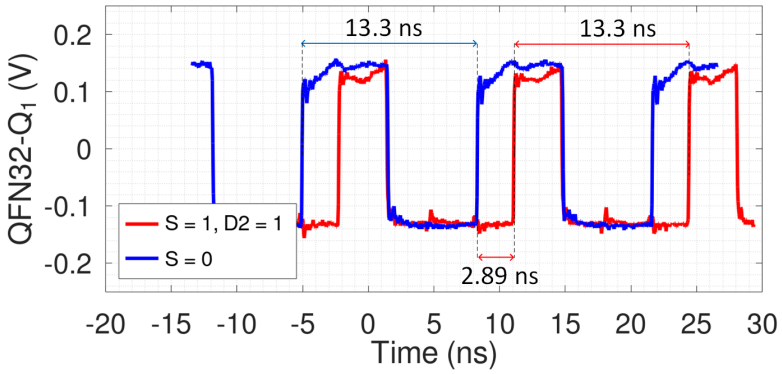
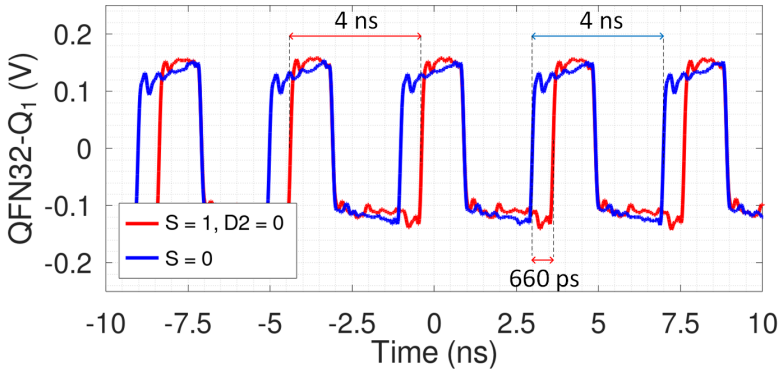


Figure 8.3 : For diverse f_{clk} measured by oscilloscope, QFN32-$\phi_{S,1.6V}$: (a) 0.2 GHz, (b) 0.4 GHz, (c) 0.7 GHz, (d) 1 GHz.

bouncing during clock-low and supply ripples during clock-high. These deterministic interferences directly contribute to the jitter, as stated in the study by [1]. The phase jitter of QFN32-ϕ_1 is explained in Fig. 8.5, within the integration bandwidth of 10 kHz to 20 MHz. The external clock source exhibits a flat band SNR_{jitter} of 78 to 75 dB, as depicted in Fig. 8.6a. The SNR of QFN32-ϕ_1 is 66 dB for a f_{clk} of 100 MHz, and 54.1 dB for a f_{clk} of 1 GHz, as seen in Figure 8.6b. Excluding the jitter contribution of PAD



(a)



(b)

Figure 8.4 : Changing of duty cycle for QFN32-ϕ_1: (a) 75 MHz f_{clk}, (b) 250 MHz f_{clk}.

drivers, the SNR of ϕ_1 is 72 dB for a f_{clk} of 100 MHz, and 60 dB for a f_{clk} of 1 GHz, as seen in Fig. 8.6b. The value of S_{11} is below -10 dB within the frequency range of 100 MHz to 1 GHz, as shown in Fig. 8.7. The simulation and testing of matching networks can reveal slight discrepancies due to the unregulated impedance of the PCB and the variations in the FR4 manufacturing process, which can depart from the assumptions predicted by the model [63].

The EspecBTZ − 175E thermal chamber is used for temperature measurement. The recorded data for the BGR circuit spans from -40^{o}C to $+90^{o}$C. The three tiers of the 3-b trim for BGR 0.8 V are shown in Fig. 8.8a. The green lines represent the bounds that include about $\pm 20\%$ of the variance, which is equivalent to a variation of $\pm 3\sigma$, as determined using a Monte Carlo simulation with 100 samples. The critical reference voltage for LDO_1, LDO_2, LDO_3, LDO_5, and LDO_6 is BGR 0.8 V. When the calibration is adjusted to $< 100 >$, the BGR's output voltage reaches its intended value of 0.8 V. At a temperature of $+25^{o}$C, the measured output voltage is 0.785 mV. The

BGR 0.4 V is not adjusted and its temperature characteristics are shown in Figure 8.8b. The BGR 0.4 V is measured as 0.435 mV at a temperature of $+25^{o}$C.

The performance comparison is shown in Table 8.1. Our design for pipeline ADCs stands out from existing non-overlapping clock phase generators mentioned in [19, 20, 64, 65] due to its incorporation of three distinct clock swing levels, multiple non-overlapping phases, and adjustable duty cycle for ϕ_1 and ϕ_{1a}. It is important to note that the reported jitter in these existing designs only takes into account $\sigma_{j_{ext,clk}}$ and the clock circuitries within the chips. Based on the test findings, including a supply filter near the power pins of the package, using a stack-up structure, maintaining regulated impedance, and employing an advanced high-speed process like Rogers 4003C may effectively reduce deterministic jitter [63].

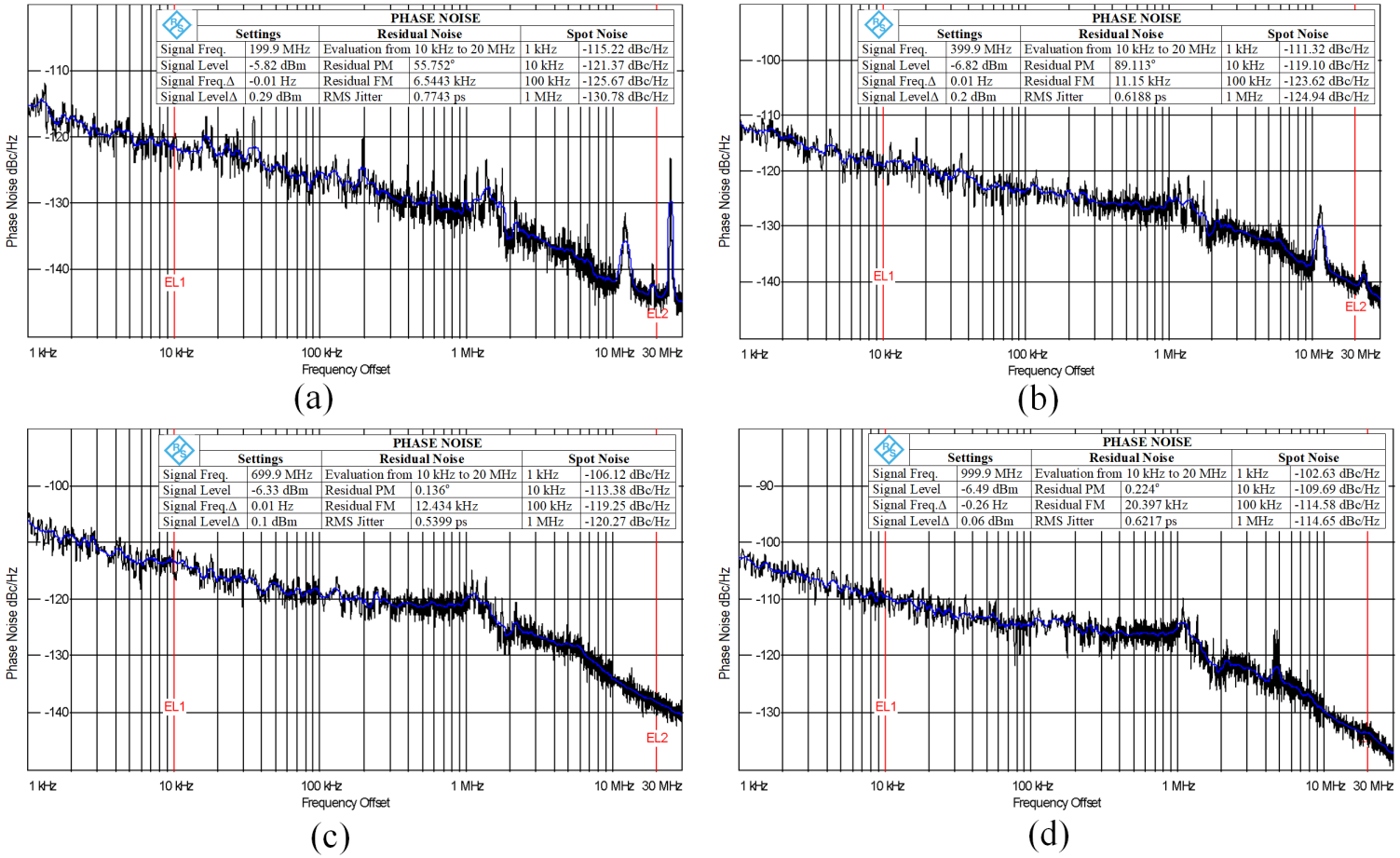
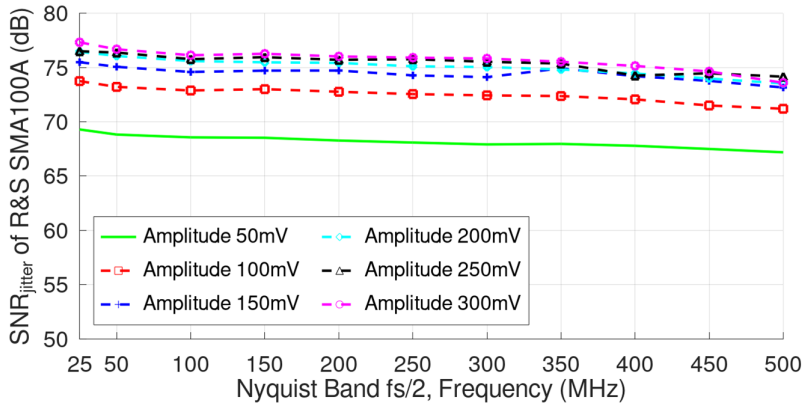
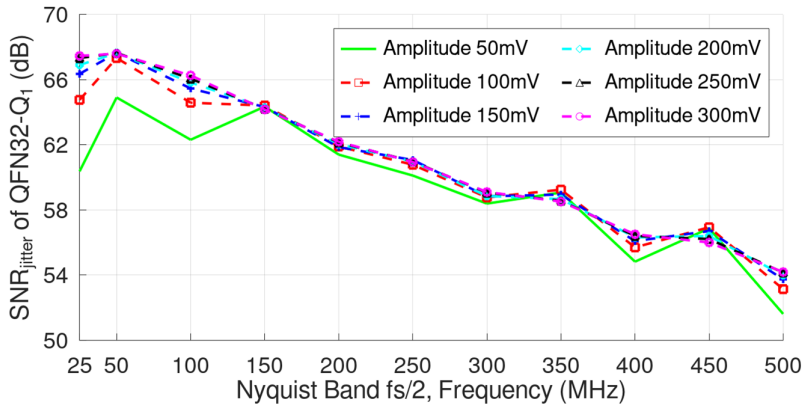


Figure 8.5 : Phase jitter of QFN32-ϕ_1 for diverse f_{clk} of external signal source with 600 mVp-p, measured by spectrum analyser for f_{off} within 10 kHz and 20 MHz: (a) 0.2 GHz, (b) 0.5 GHz, (c) 1 GHz.



(a)



(b)

Figure 8.6 : (a) SNR_{jitter} of R&S SMA100A signal generator vs fs/2 in changing of signal amplitude at external signal source, (b) SNR_{jitter} of QFN32-ϕ_1 vs fs/2 in changing of signal amplitude at external signal source.

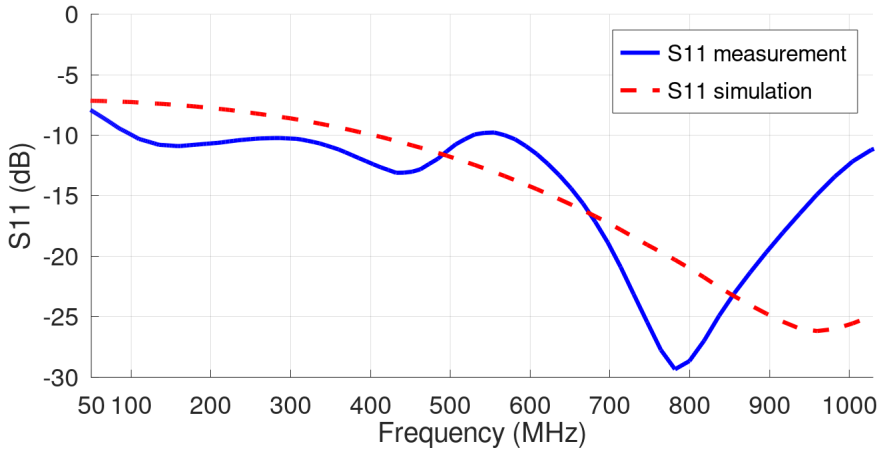
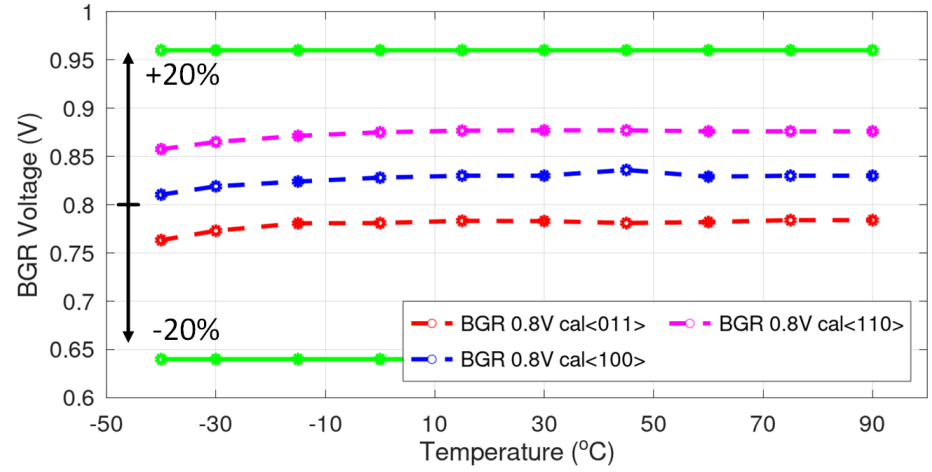
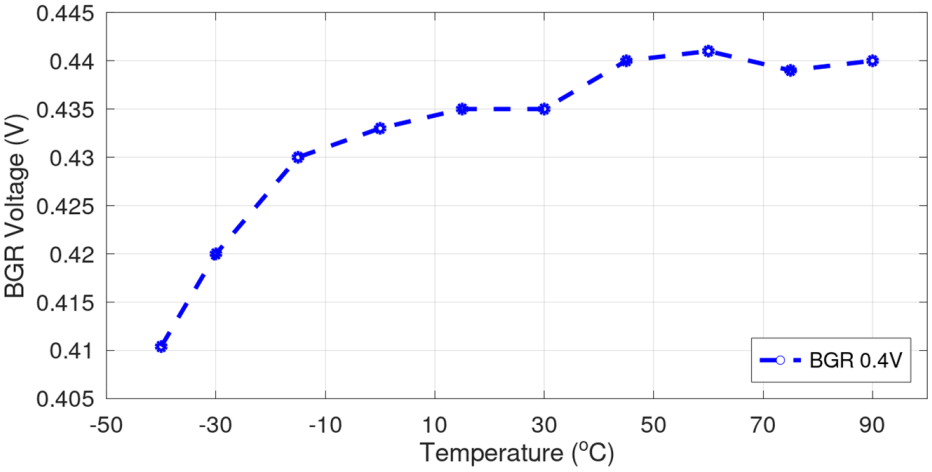


Figure 8.7 : Results of measurement and simulations for S11 wrt f_{clk}



(a)



(b)

Figure 8.8 : Temperature measurement for BGR in the ESPECBTZ – 175E thermal chamber: (a) Voltage of BGR: 0.8 V 3 – b trim, (b) Voltage of BGR: 0.4 V.

Table 8.1 : Performance Comparison

	This Work	JSS '05 [20]	JSSC '08 [64]	JSSC '13 [65]
Process	SiGe 0.13µm	SiGe 0.4µm	CMOS 130nm	CMOS 65nm
Supply voltage	3-3.3 V	3.3 V	1.2 V	1.2 V
Architecture	Ext. clock + Phase Gen.	Ext. clock + Phase Gen.	Ext. clock + Phase Gen.	Ext. clock + Phase Gen.
Measurement	Yes	Yes.	Yes	Yes
$\sigma_{j_{ext,clk}}$	0.249 ps @200 MHz, 62 fs @1 GHz (10 kHz-20 MHz)	25 fs @65 MHz After a 300 kHz bandpass filter	NaN	40 fs @2.8 GHz
f_{clk}	50 MHz to 1 GHz	65 MHz	1.35 GHz	2.8 GHz
Number of Phase	11	NaN	NaN	NaN
Multi-level	0-1.2V, 0.4-1.6V, 1.6-2.8V	No	No	No
Power	57 mW @1 GHz (BGR+LDOs+RX+ClkGen)	NaN	34 mW	8.47 mW
Silicon area	0.144 mm^2	NaN	NaN	NaN
Jitter (RMS)	0.51 ps @200 MHz, 0.29 ps @1 GHz $\phi_{1,2,1b}$(10 kHz-20 MHz)	0.18 ps @65 MHz Evaluation of SNR calculation	0.2 ps @84.4 MHz	0.32 ps @116.7 MHz
S_{11}	-10dB @ 0.1-1 GHz	NaN	NaN	NaN

9. CONCLUSIONS

9.1 Summary

In this dissertation, a fully differential 11-b pipelined ADC sampling at 1.6 GS/s was designed in IHP SiGe 0.13 μm BiCMOS technology. The pipelined ADC was created with programmable features for consuming power and stage amplifier settling, enabling it to be utilized for testing efficiency and power conservation.

In addition to error correction, attempts were undertaken to enhance the power efficiency of the ADC. An in-depth examination and comparison of opamp configurations and their efficiency in BiCMOS technology revealed that a two-stage design was the most optimal topology. Utilizing a CCB stage as the initial stage reduces leakage current without compromising the amplifier's speed.

The new architecture is based on eliminating the sample-and-hold amplifier, as the front-end of the ADC, so that the power consumption was further reduced. The input signal is directly sampled at the first stage. Thus, the mismatch between the sampling network of the MDAC and the sub-ADC is critical, and any mismatch between those networks results in an aperture error. In our design, the sampling network of the sub-ADC is designed as a replica of that of the first stage MDAC in order to alleviate the aperture error. A 1.5-bit per stage architecture was implemented to handle aperture error and comparator offset by offering a significant overrange. A modified timing method introduced in [5] was adopted to eliminate ISI in the sampling time of the MDAC. Stage scaling was employed to reduce the power dissipation of the pipelined stages.

The revised comparator design from [14] was utilized in the sub-ADC for its improved offset and speed, providing additional overrange from 1.5-b per stage. Meanwhile, the resolution in the final flash ADC was enhanced to 3-b. A pre-amplifier was used to reduce the clock kick-back, emerging from the clocked comparators.

Clock level converters were utilized to ensure adequate linearity and discharge time for the switches due to the limited supply voltage. A configurable bandgap reference circuit was used to produce the necessary bias voltages for the ResAmp and LDOs.

In this work, a one way 11-b pipeline ADC, designed in a SiGe BiCMOS 0.13 μm, is presented. It has sampling frequencies up to 1.6 GS/s and can provide above 8-b ENOB for the low input signal frequency and 6.4-b ENOB for the highest input frequency of 799 MHz according to the simulation results obtained without calibration. For our ADC, sample-and-hold amplifier-less (SHA-less) architecture was preferred since the SHA was one of the most power-consuming sub-blocks, and brought inevitable noise and distortion. A composite ADC architecture, having 8x 1.5-b cascaded stages and a back-end 3-b flash ADC is designed to reach up to 11-b resolution. A novel MDAC is proposed to mitigate ISI. Moreover, a novel BiCMOS RA, which performs 6.43 GHz UGBW and 80 dB DC gain, is implemented. A non-overlapping clock generation architecture at 1.6 GHz is devised, incorporating a differential clock driver and clock level converters. The clock generation system attains an SNR_{jitter} of 57 dBc when the external clock signal is transmitted at 1.6 GHz. The complete ADC, having supply of 1.6 V, and, occupying 2.2 mm $\times$ 3 mm silicon area, is realized in a SiGe BiCMOS 0.13 μm process. This makes our pipelined ADC an ideal choice for evaluating calibration techniques.

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APPENDICES

APPENDIX A : 11-b Pipelined ADC Chip Layout View
APPENDIX B : Sempac, Inc. 32 Lead QFN 5 mm $\times$ 5 mm.
APPENDIX C : Arduino Due SPI Communication.
APPENDIX D : The Test PCB for the Clock Generation Packed in a 32 Lead QFN 5 mm $\times$ 5 mm.

APPENDIX A : 11-b Pipelined ADC Chip Layout View

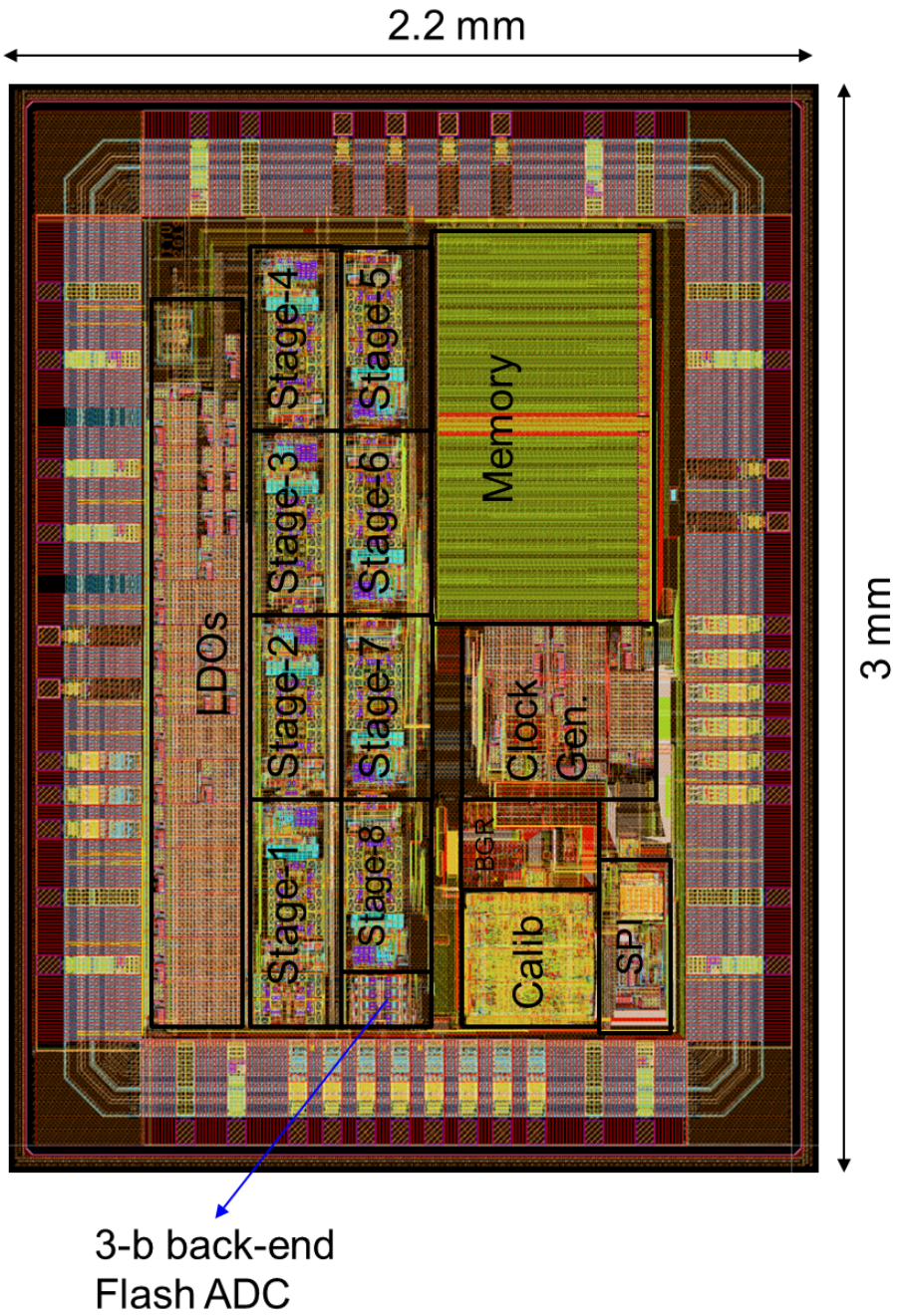

Figure A1 : The proposed 11-b pipelined ADC die area: 2 mm $\times$ 3 mm.

APPENDIX B : Sempac, Inc. 32 Lead QFN 5 mm x 5mm

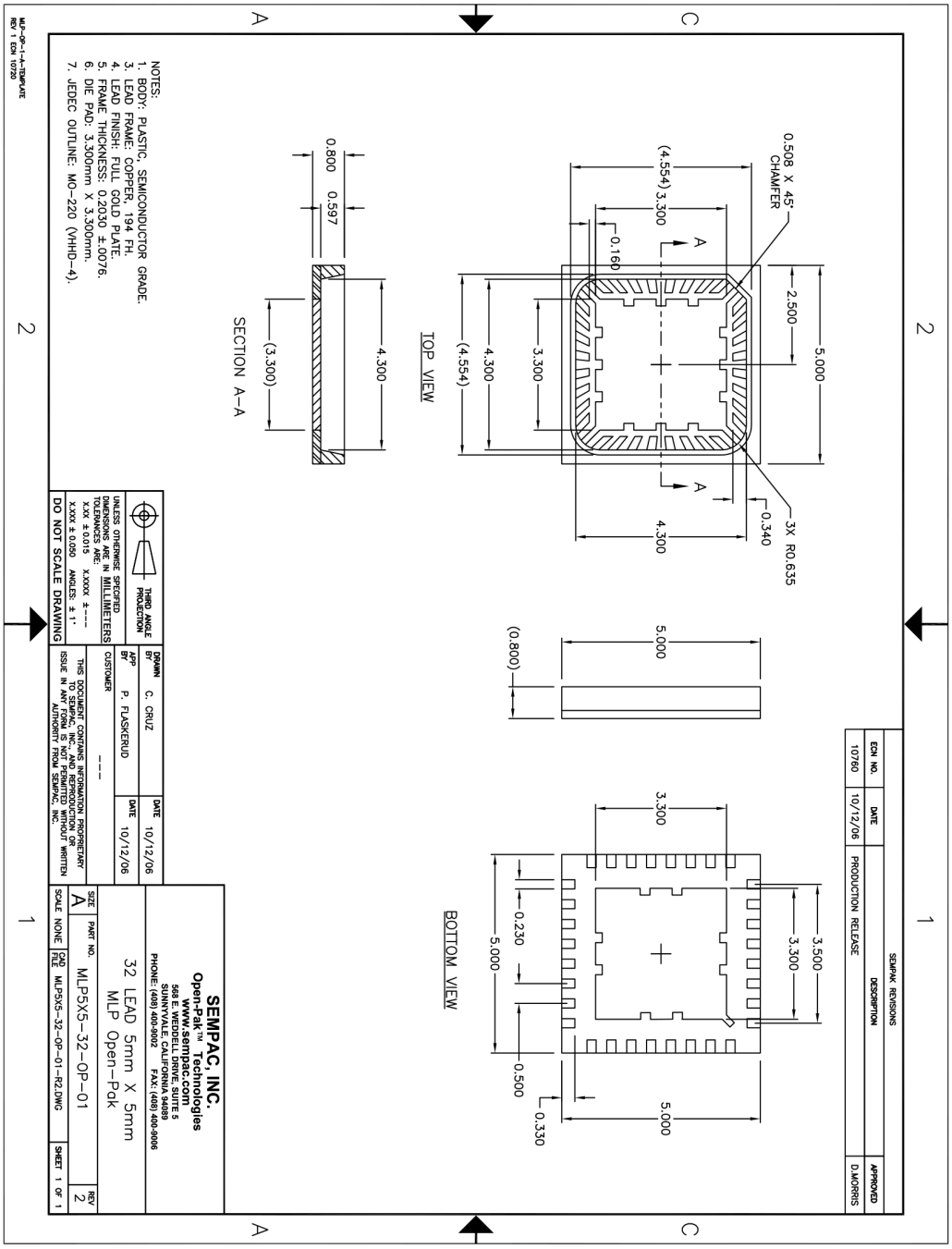

Figure B1 : Sempac, Inc. 32 lead QFN 5 mm × 5 mm.

APPENDIX C : Arduino Due SPI Communication

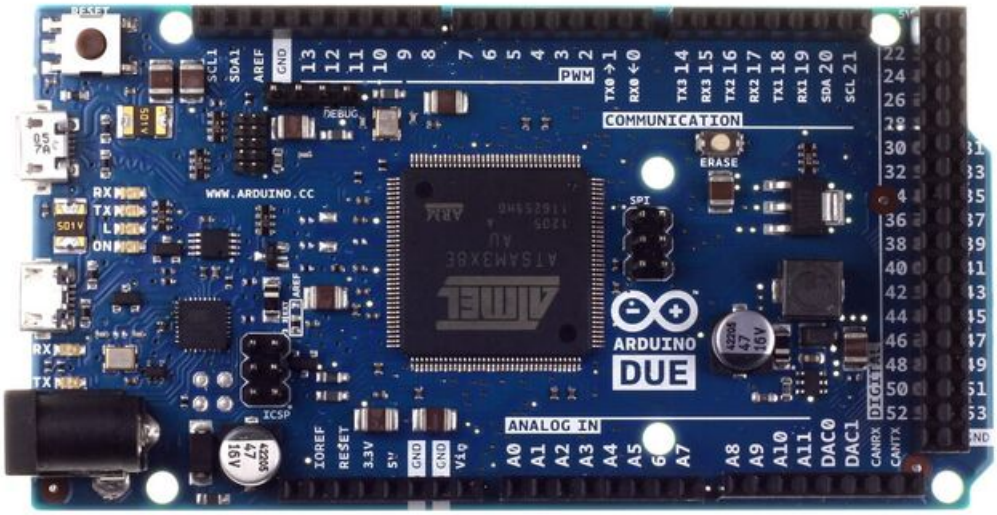

Figure C1 : Arduino Due 3.3V is used for SPI communication.

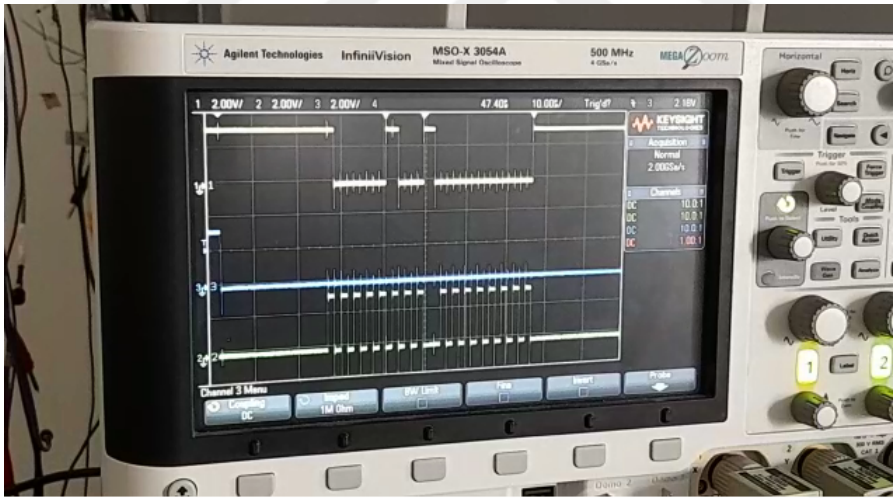

Figure C2 : Chip Enable (CE), Serial Clock (SCLK) and Master Out Slave In (MOSI, 8400 HEX Spi Code) are demonstrated in the Agilent Oscilloscope InfiniiVision MSO-X3054A.

Table C1 : SPI 16 bit data codes for two cases

Hexadecimal SPI Code															
Binary 16 bit SPI Codes: 8400 HEX															
Binary 16 bit SPI Codes															
1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W	Address				Data										
Hexadecimal SPI Code															
Bias generation Power Up: 8000 HEX															
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W	Address				Data										

APPENDIX D : The Test PCB for the Clock Generation Packed in a 32 Lead QFN 5 mm x 5 mm

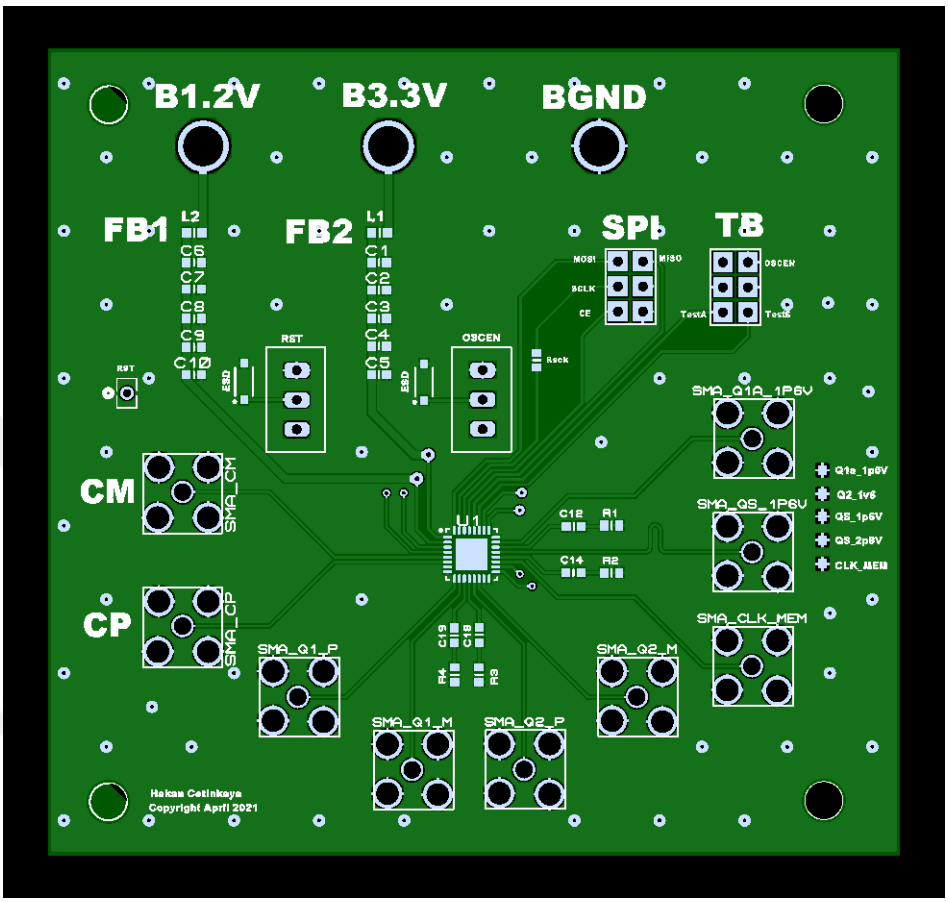

Figure D1 : PCB with SMA connectors for output clock terminals.

The front view of the PCB with SMA connectors is depicted in D1. CM and CP are the differential clock signal inputs. SMA $-\phi_{1,\mathrm{P}}$, SMA $-\phi_{1,\mathrm{M}}$, SMA $-\phi_{2,\mathrm{P}}$, SMA $-\phi_{2,\mathrm{M}}$, SMA-CLK-MEM, SMA $-\phi_{\mathrm{S},1.6\mathrm{V}}$, SMA-$\phi_{2,1.6\mathrm{V}}$ are the output clock terminals. There are two power supply sockets, namely, B1.2V and B3.3V and one ground socket BGND. SPI pins are MOSI, MISO, SCLK and CE. There are two test pins as Test-A and Test-B. RST and OSCEN activate the digital circuitry and internal oscillator for SPI, respectively.

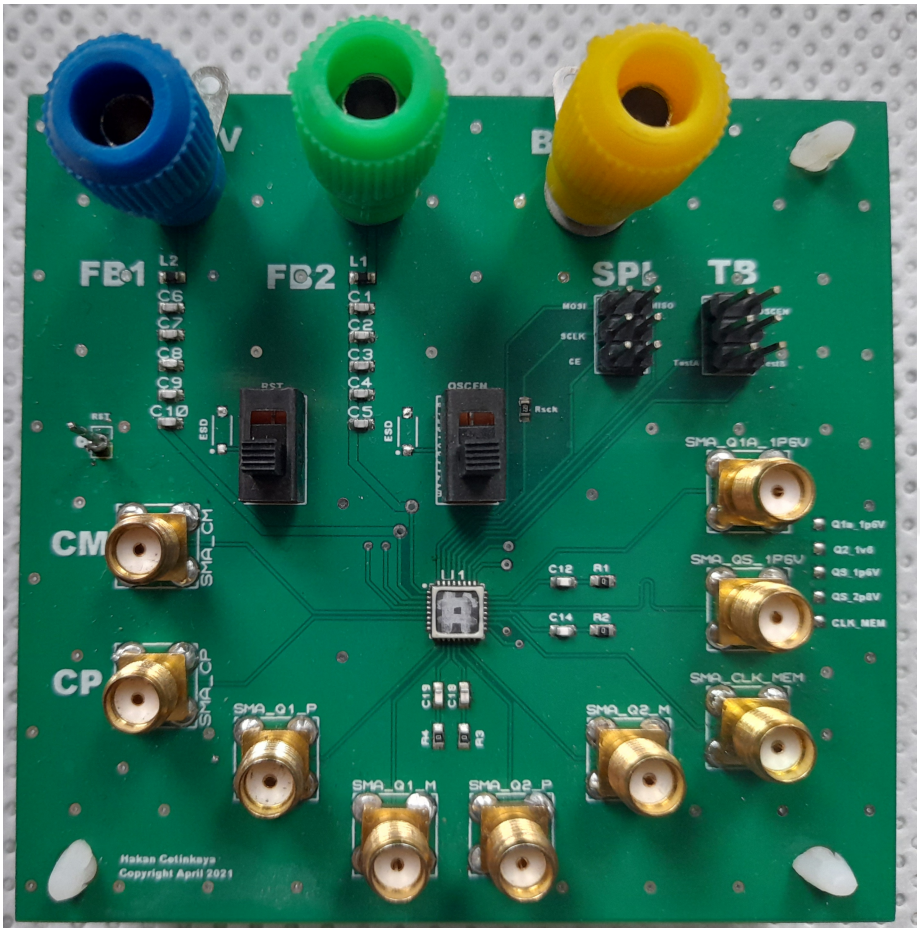

Figure D2 : PCB with SMA connectors for output clock terminals.

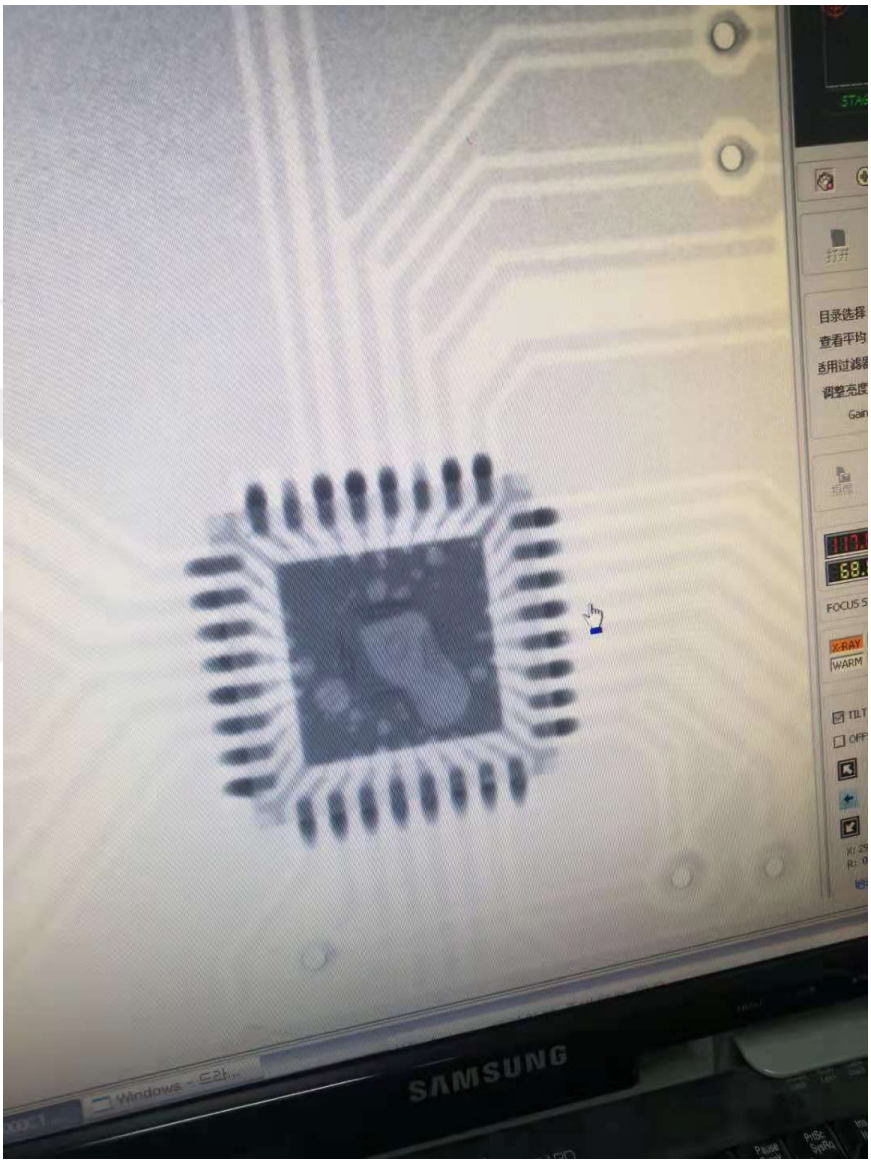

Figure D3 : X-RAY of the PCB with SMA connectors shows the clearness of the soldering and no short circuits.

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