LOW POWER CMOS OPTOELECTRONIC TRANSMISSION SYSTEM DESIGN

by

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ABSTRACT

LOW POWER CMOS OPTOELECTRONIC TRANSMISSION SYSTEM DESIGN

Catheter based endovascular operations are used for diagnosis and treatment as minimally invasive procedures. Most of these operations are held under X-ray fluoroscopy which is harmful due to incident radiation and chemical agents used for increasing contrast ratio. However, MRI, with high soft tissue contrast and eliminates ionizing radiation, is a candidate to replace old techniques which are used for catheter based operations. An optoelectronic system to be used in a MR environment as a part of a catheter detection system is proposed. The optoelectronic system is composed of an external laser driver, an optoelectonic CMOS power supply, an LED driver and an optical transmission path which is fabricated by using MEMS techniques. The external laser driver enables modulation of power laser which has a power up to 200 mW with a wave length 660 nm. The CMOS power supply, fabricated in UMC 0.18 μm process, is composed of photodiodes, which have an efficiency of 5% optical-to-electrical conversion, and a DC/DC converter to boost photodiode voltage of 0.6 V to 1.2 V. A supply independent LED driver, which supplies 2 mA to an IR LED with a current consumption of 138 μA, has been designed. A Si platform which is composed of a V-groove and a mirror, is designed and fabricated by using wet etching techniques. Finally, a front-end circuit is described to detect optical signals which carry catheter localization data on their frequency.

ÖZET

DÜŞÜK GÜÇTE CMOS OPTOELEKTRONİK İLETİM SİSTEMİ TASARIMI

Kateter bazlı endovasküler işlemler minimal invaziv prosedürler olarak tanı ve tedavi için kullanılır.Bu operasyonların çoğu radyasyon ve kontrast oranı için kullanılan kimyasal maddeler nedeniyle zararlı olan X-ışını floroskopi altında yapılır. Bununla birlikte, MRI, yüksek yumuşak doku kontrastı ve iyonlaştırıcı radyasyonu ortadan kaldırması ile kateter bazlı işlemler için kullanılan eski tekniklerin yerini almaya adaydır. MR ortamında bir kateter izleme sisteminin bir parçası olarak kullanılacak bir optoelektronik sistem önerilmiştir. Optoelektronik sistem, harici bir lazer sürücü, bir optoelektonik CMOS güç kaynağı, bir LED sürücü ve MEMS teknikleri kullanılarak üretilen bir optik iletim yolundan oluşur. Harici bir sürücü devre, dalga boyu 660 nm ile gücü maksimum 200 mW olan güç lazerinin modülasyonunu sağlar. UMC 0.18 μm süreci ile üretien CMOS güç kaynağı, % 5 optik-elektrik dönüşüm verimliliğinde fotodiyotlar, 0.6 V fotodiyot gerilimini artırmak için kullanılan DC/DC dönüştürücü,1.2 V'ta 138μA akım tüketimi ile IR LEDe 2 mA sağlayan besleme geriliminden bağımsız LED sürücü tasarlanmıştır. V-kanal ve bir aynadan oluşan bir Si yapı, ıslak aşındırma teknikleri kullanılarak tasarlandı ve üretildi. Son olarak, bir ön uç alıcı devresi, frekans ile kateter yer verisini taşıyan optik sinyalleri algılamak için anlatıldı.

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LIST OF SYMBOLS

Al	Aluminum
As	Arsenic
Au	Gold
B	Magnetic Field
Cr	Chromium
d	Distance Between the Fiber and the Mirror
g	Gap Between Surfaces
g_m	Device transconductance
Ga	Gallium
f	Outer Radius
d	Diameter
h	Height
H_2O_2	Hydrogen Peroxide
H_2SO_4	Sulfuric Acid
I	Current
In	Indium
IPA	Isopropyl Alcohol
KOH	Potassium Hydroxide
R	Resistance
r	Inner Radius
rpm	Round per Minute
Si	Silicon
T	Transistor
V	Voltage
v	Photon Frequency
α	Plane Angle
β	Aperture Angle

γ	Larmor Frequency
ε	Electric Field

LIST OF ACRONYMS/ABBREVIATIONS

AC	Alternating Current
ADS	Agilent Advanced Design System
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DC/DC	Direct Current-to-Direct Current
DI	Deionized
HDMS	Hexamethyldisilazane
IC	Integrated Circuit
IR	Infrared
LED	Light Emitting Diode
LO	Local Oscillator
MEMS	Micro-electromechanical Systems
MNL	Micro Nano Characterization Laboratory
MR	Magnetic Resonance
MRI	Magnetic Resonance Imaging
NA	Numerical Aperture
PD	Photodiode
PR	Photoresist
RF	Radio Frequency
UMC	United Microelectronics Corporation
UV	Ultraviolet

1. INTRODUCTION

The use of minimally invasive procedures also is expanding in recent times. In many applications, a catheter is used to treat vascular diseases and medical testing applications in veins or tissues. Tracking of catheters are done under X-ray fluoroscopy guidance which has harmful effects to both patients, doctors and medical staff. The whole project aims to achieve an optoelectronic integrated system which can be used for tracking a catheter tip in magnetic resonance imaging environment. Current commercial localization options generally are implemented in computed tomography (CT), which uses X-ray and due to ionized radiation damage, the operation time, to locate a catheter, is limited. In addition, some chemical agents are also used for increasing contrast of the image while tracking a catheter. Moreover, these chemicals can be harmful for the human body [1]. In the recent years, high resolution intravascular (magnetic resonance imaging) MRI is emerging as an option for diagnose about atherosclerotic plaques in blood vessels by using micro scale radio frequency (RF) coils at the tip of the catheter [2, 3, 4] . Since MRI takes images as slices, unlike the conventional methods like X-ray fluoroscopy, tracking of the catheter tip is more essential in order to extract catheter location. [5]. The aim of this thesis is to propose a low power optoelectronic transmission system that is used in a microscale biomedical application which aims to locate a catheter inside MRI.

The working principle of a magnetic resonance imaging is as follows. When placed in a magnetic field of strength B, a particle with a net spin can absorb a photon, of frequency v. The frequency v depends on the gyromagnetic ratio, γ of the particle as shown in Equation 1.1. For hydrogen, γ=42.48 MHz/T.

$$v = \gamma B \tag{1.1}$$

If each of regions of the spin was to experience a unique magnetic field, it is possible to image their positions. A magnetic filed gradient is a variation in the magnetic field

with respect to position. A one-dimensional magnetic field gradient along the x-axis in a magnetic field, B_o, indicates that the magnetic field is increasing in the x direction as it is shown in Figure 1.1 [1]. The point in the center of the coil magnet where (x,y,z)

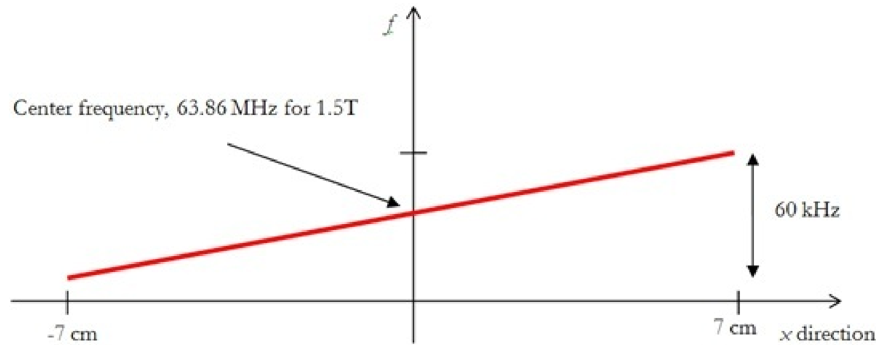

Figure 1.1. An example magnetic field gradient and related positions in a 1.5 T system.

= (0,0,0) is called the isocenter of the magnet. The magnetic field at the isocenter is B_o and the resonant frequency is v_o. The amplitude of the signal is proportional to the number of spins in a plane perpendicular to the gradient. This procedure is called frequency encoding and causes resonance frequency to be proportional to the position of the spin.

$$v = \gamma(B_o + xG_x) = v_o + \gamma x G_x \quad (1.2)$$

$$x = (v - v_o)/(\gamma G_x). \quad (1.3)$$

Therefore, if the spin frequency is detected at a point, it is possible to detect its relative position to the isocenter reference point. The tracking architecture uses this property of MRI.

MRI has a medium which is subjected to high RF fields, magnetic fields [6], electromagnetic interference (EMI) [7]. In such an environment, it more appropriate to power the system via optical, rather than electrical means. The same applies for the transmission of signals as well. For example, in MRI, due to applied magnetic and RF

pulses induced ε-fields in long conducting cables can cause tissue heating [8]. However, a transformer-based cable has been proposed recently, such that, the heating problems are reduced yet with a cost of signal-loss [6]. Although there are recent developments to use electrical means to use inside MR like environments, it is not completely safe to use them and there is a huge cost of signal loss. Due to the reasons explained,use of light is a brilliant option to carry information and power in harsh environments for electrical means, where conductor cables are used. Since light is guided inside an optical fiber, the optical power losses in long ranges are extremely low. Another reason to use optical means is that, the medium, which is light is guided inside, is an optical fiber, which is not causing heating by the electromagnetic interference, RF fields and the magnetic field. The proposed optoelectronic system, Figure 1.2, is used

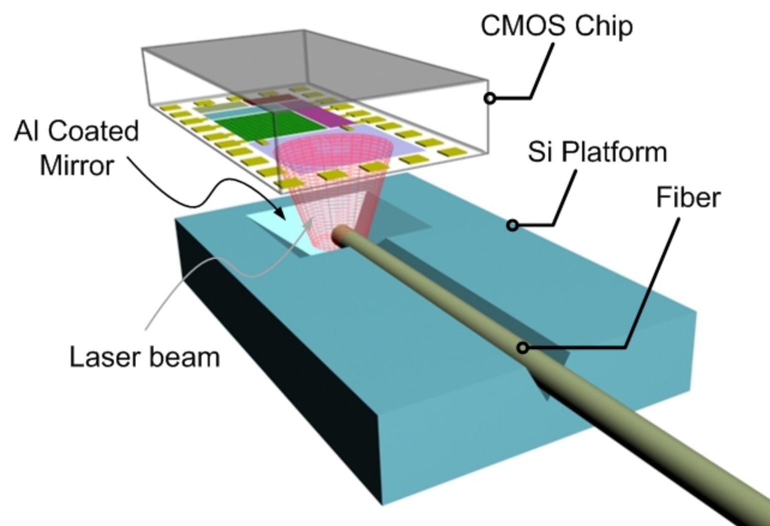

Figure 1.2. Sketch of the physical realization of the integrated system.

as a link for the integrated catheter localization circuit and the outer world. A system containing an optical power source, transmission medium, and an optical to electrical converter forms the power up part. The LED driver, connected to a transmission medium via fiber butt-coupling or a micro electromechanical system (MEMS) stage forms the signal transmitter part. To sum up, the overall structure is composed of a optoelectronic power supply, which is composed of an on-chip complementary metal oxide semiconductor (CMOS) photodiode, direct current to direct current (DC/DC)

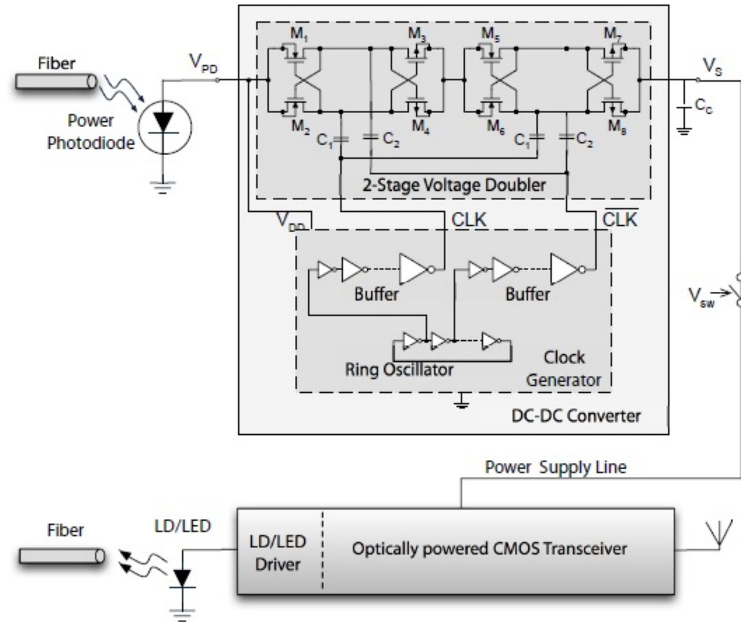

Figure 1.3. Schematic of the optically powered CMOS transceiver.

converter and a MEMS stage as guide for the light rays for planar packaging, catheter localization circuit, which is composed of an low-noise amplifier (LNA), a mixer, an optional local oscillator which is an on chip photodiode, and an LED driver to transmit processed signals to front end in order to obtain data, i.e. in this case frequency value to show the catheter tip location.

This thesis work presents a low power optoelectronic system which is a part of a catheter tracking system. Novelty of this work can be summarized as that it integrates the transceiver and the power supply into a single IC die with cost of power and the LED driver proposed is an application specific design that is designed to have minimum power consumption and supply insensitive. This thesis work also has a multidisciplinary side in a way so that the author had deal with wide range of areas from MEMS, photonics to analog circuit design. The thesis is organized in five chapters. First being the introduction that explains the purpose of the work and connections through different tasks are explained. In the second chapter, the back end part of the system is presented. In mentioned chapter, an external laser driver, which is used to power up the power laser of the system, is presented. Then, the

CMOS optoelectronic power supply is mentioned mainly focusing on the optical side. Afterwards, an LED driver, which is located at the end part of the back-end circuit, converts the electrical signals to optical signals in order to transmit them out of the MRI. In the latter chapter, optical transmission path is explained in two separate parts. In the first part, coupling and fiber alignment is shortly explained and the silicon (Si) platform used to couple light on the power supply is explained in detail. In Chapter 4, front end designs are expressed. Finally, in the last chapter conclusions are made and achievements are summarized. At the end of the last chapter possible future works are expressed.

2. BACK END PART

This part of the system is mainly located on the integrated circuit except for the power laser driver which is used to modulate the powering laser in order to supply optical power to the chip. In this chapter, firstly, external laser driver and smart on-off modulation is explained. Then, on chip optical power supply will be explained. At the next part, reasons to choose an LED instead of a laser and their electrical modeling will be shown. Afterwards, various LED driver topologies will be explained. Finally, an LED driver circuit, which designed using UMC 0.18 μm technology is examined starting from schematic design to layout design and comparison their simulations.

2.1. External LASER driver

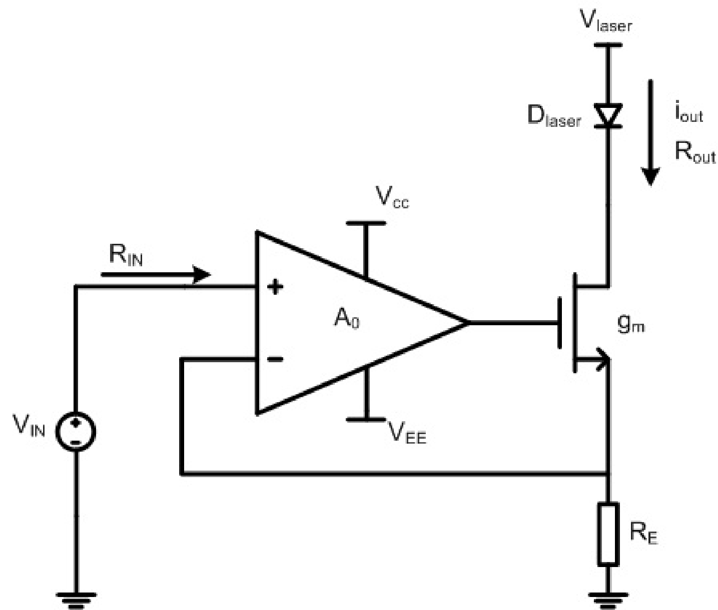

Figure 2.1. Schematic view of the external LASER driver.

The external laser driver has been designed in order to modulate an external 200 mW laser in order to obtain optical power which is converted to electrical power on the CMOS optoelectronic power supply. The driver circuitry is simply a voltage to current converter based on series-series feedback transconductance amplifier. The schematic of the circuit is given in Figure 2.1. The circuit is one of the simplest ways

to convert voltage into a current, with very high accuracy [9]. The negative feedback works in a manner such that the applied input voltage increases the output voltage of the operational amplifier in the circuit, which is connected to the gate of the driving transistor, and increased current also gives rise to the the voltage on the resistor R_E, which is connected to the source of the driving transistor and the negative input of the operational amplifier, that limits the output current to a value in Equation 2.1.

$$i_{out} = \frac{V_{IN}}{R_E} \tag{2.1}$$

and the loop gain (LG) is defined as,

$$LG = A_0 \tag{2.2}$$

where A_0 is the open-loop gain of the opamp used in the circuit. The input resistance of the driver is

$$R_{IN} \approx \infty \tag{2.3}$$

due to metal oxide semiconductor (MOS) differential pair input stage. Open-loop output resistance is defined as

$$R_{outOL} \approx r_o(1 + g_m R_E) \tag{2.4}$$

where g_m is the transconductance of the transistor at the circuit and R_E is the current defining resistor. The output resistance is then

$$R_{out} = R_{outOL} \cdot LG. \tag{2.5}$$

As it is seen in Equation 2.1, the voltage-to-current conversion is only dependent on resistor R_E. In addition, the input resistance is high (Equation 2.3) and so is

the output resistance (Equation 2.4 and 2.5). The circuit in Figure 2.1, has been constructed by using a HA17741 opamp, 5.5 Ω ceramic resistor and a IRFZ44N power MOSFET in order to supply a current up to a few amperes. The operating points of the driver circuitry are $V_{CC} = -V_{EE} = V_{laser} = 15V$ and the input signal can be rail-to-rail unless the laser is harmed. But, the AC response of the circuit limited by the opamp at the kHz level. However, this situation is enough to modulate the powering laser for optical switching which is described in the optoelectronic power supply part.

2.2. Optoelectronic CMOS power supply

The optoelectronic power supply is the most vital part in the catheter tracking system [10], since it defines the power budget for operation. The most limiting part was the low power budget during the work. Due to that fact, first an IC has been designed [1, 10] for proof of concept work and a second IC designed later with additional electronic circuitry for catheter tracking inside an MRI [1, 10]. In those studies [1, 5, 10, 11] same theoretical facts used as basis in the design of the power supply.In this work second architecture has been used as a basis for the power supply, in order to predict the power budget for electronic circuits which are used for determine the localization data of a catheter tip inside an MRI device. The CMOS power supply unit operates on the principle of enhancement of the photo-diode voltage, that is induced by the light (e.g. from a laser) transferred through a medium (in air or through fiber-optic cable) to its light-sensitive region. This induced voltage on the photodiode is quite low to be directly used in microelectronics circuits, thus it is stepped up by the DC/DC voltage converter, a higher level, which is sufficient to serve as a power supply for an electronic system. The output voltage V_S could be used directly or with an additional bypass capacitor which alters out the noise generated in the output voltage. Furthermore, the capacitor could work as a storage device and it could be used together with an additional switch (controlled by a switching voltage) to achieve higher current values for intermittently powered applications [12].

2.2.1. CMOS photodiodes

For harvesting low levels of power, standard CMOS technologies can be used to obtain integrated optoelectronic converters [13]. In this work, a triple-well CMOS process, where both twin-well and triple-well field effect transistors (FETs) is are implemented on the same substrate, is exploited to build photodiodes as shown in Figure 2.2. The photodiodes are implemented on triple-well transistors, whereas DC/DC converter and other electronic circuitries, like LNAs, mixers and the LED driver, are implemented by using low threshold voltage (twin-well) MOS transistors.

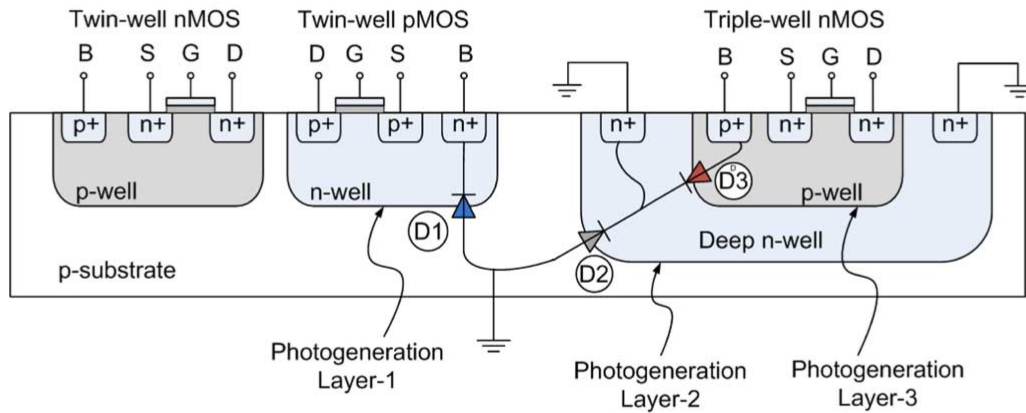

Figure 2.2. Cross section of the triple-well CMOS process.

As can be seen in Figure 2.2, low-threshold-voltage transistors share the same substrate, which serves as the anode of the n-well photodiode (D1). When this diode is used in photovoltaic mode to induce a positive voltage drop between the anode and the cathode terminal, the input of the dc/dc converter circuitry is effectively grounded. Therefore, it is not possible to the anode of the n-well photodiode (D1) as an input for the DC/DC converter [11].

Triple-well photodiode (D3) and deep n-well photodiode (D2) have common cathode connection. During the normal operation of D3, the junction between the deep n-well and p-well diffusion of the triple-well transistor is illuminated, which means that the junction between the deep n-well and the substrate receives light as well. As a result, whenever D3 is optically turned ON, D2 turns ON too, acting as a parasitic

photodiode, which steals the useful photo-induced current of D3. As a solution, p-type substrate and the n+ contact diffusion of the deep n-well are shorted at the ground potential, which avoids current to be stolen from D3. Because of the necessity to tie cathode of D3 to ground level, it is not possible to have a series connection of triple-well photodiodes. Although it is allowed to tie n-well (D1) and triplewell (D3) photodiodes in series, this connection puts a severe restriction to the usage of triple-well nMOS transistors [7, 11]. In the first IC, in order to define the efficiency of the photodiode

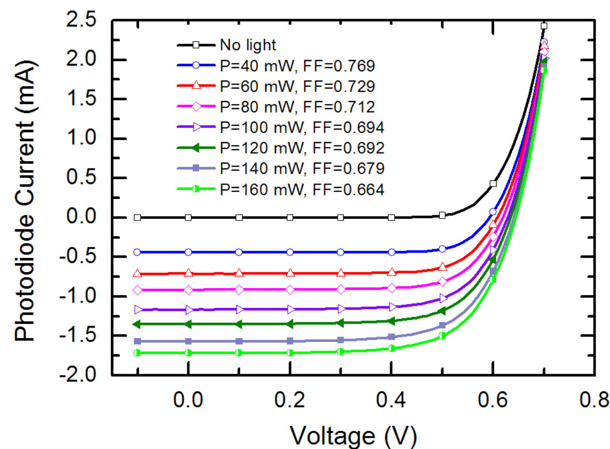

Figure 2.3. Current-Voltage characteristics and fill factor values of metal covered n-well photodiode in the first IC illuminated with a laser by varying the optical power.

to convert optical power to electrical power, 300 μm$\times$300 μm n-well photodiodes has been added to the layout. However, the dummy metal patterns with gaps, which were placed in the foundry to keep the uniformity of the metallization process during fabrication, efficiency thus, the effective area has been shrunk. Firstly, initial test were made on the metal pattern covered n-well photodiodes. Characterization results belonging to them can be seen in Figure 2.3. From Figure 2.3, a short circuit current of of around 0.93 mA is measured at an optical power of 80 mW. The fill factor, which is a key parameter in evaluating the performance of solar cells, is defined as the ratio of the actual maximum obtainable power, to the product of the open circuit voltage and short circuit current. The fill factor values in this characterization varies between 0.769 and 0.664 as the optical power is swept between 40 mW and 160 mW. This

phenomenon is observed due to the reduction of equivalent shunt resistance and the increase in the equivalent series resistance of the photodiode with increasing optical power [11].

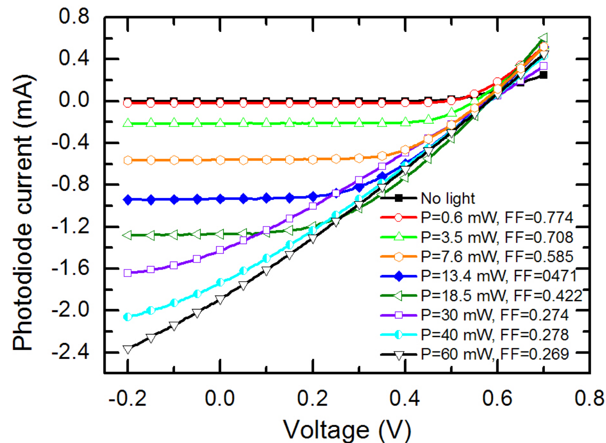

Figure 2.4. Current-Voltage characteristics and fill factor values of uncovered n-well photodiode in the first IC illuminated with a laser by varying the optical power.

In order to see the maximum capacity of the n-well photodiode, metal layer patterns over them has been removed by in-house chemical wet etching. In Figure 2.4, the current voltage characteristics of the n-well photodiode after metal patterns removed, can be seen. In the measurement results shown in Figure 2.4, the photodiode goes into saturation after 30 mW optical power. After 30 mW of optical power series resistance of the diode becomes dominant resulting the linear behavior in Figure 2.4. The fill factor (FF) of this device is extracted to be between 0.774 and 0.269, for the optical power levels between 0.6 and 60 mW, due to severe changes in the shunt and series resistances. A short circuit current of 0.91 mA is achieved from an optical power of 13.4 mW indicating a responsivity of 0.068 A/W. Thus, removing the metal patterns over the n-well photodiode increases its capacity by a factor of 6 meaning that metal patterns over the photodiode reduces its area to 1/6 (122 μm $\times$ 122 μm). That is why the metal covered n-well results in figure 2.3 do not show any saturation even at measured optical power of 160 mW [11].

Measuring the factor caused by metal patterns is essential, since triple-well photodiodes are covered with metal as well. The effect of metal pattern put a severe

restriction on the operation of DC/DC converter operation and circuits supplied by it. However, the metal pattern problem has been resolved in the second IC.

The triple-well photodiode on the chip is one of the most determinant elements of the system, since it allows integration of other circuitry (dc/dc converter in this case) on the same die. In the first generation IC, even though the triple-well photodiode used to power the DC/DC converter circuit consumes an area of 300 μm $\times$ 300 μm, it can be deduced from the experimental results of n-well photodiodes presented in Figure 2.4 that the effective area is reduced to 122 μm $\times$ 122 μm due to the dummy metal patterns put on top of them at the foundry. During the characterization of the triple-well photodiode, the cathode of the photodiode, deep n-well, and the p-substrate are shorted to eliminate the effects of the parasitic current due to deep n-well/substrate junction (D2) in Figure 2.2.

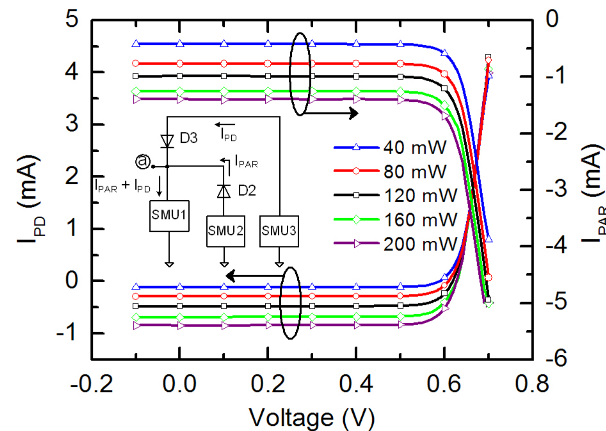

Figure 2.5. Currentvoltage characteristics of the parasitic photodiode (D2) and the metal-covered triple-well photodiode (D3) in the first IC at different optical power levels of illumination.

During the measurements, optical power of the laser is varied from 40 to 200 mW with a step value of 40 mW. Results of the measurements are shown in Figure 2.5, where both parasitic current (IPAR) due to D2 and the useful photodiode current (IPD) of D3 are plotted. Generated photodiode current increases linearly with the optical power level of the illumination. These current levels permit the DC/DC converter to function properly with an efficiency around 50%. At 200 mW of incident

light power, 0.85 mA of photodiode current is measured, indicating a responsivity of 0.0043 A/W. From the results of the n-well photodiode covered with metal patterns, it is extrapolated that the same photocurrent can be generated at an optical power of around 33 mW, indicating a responsivity of 0.026 A/W. This implies that n-well photodiodes are roughly 2.5 times (at high optical power levels) to 3.8 times (at low optical power levels) more efficient than the triple-well photodiodes. The triple-well photodiode current is lower than the n-well photodiode measured at the same optical power levels, mainly due to the regions, where photogeneration occurs. This is expected, since the junction depth of the n-well photodiode is deeper than the one of triple-well diode. The reason for the variation of the efficiency difference between these two photodiodes is that the n-well photodiode enters into saturation regime more rapidly than the triple-well diode [11]. In the second generation IC, of which micro-

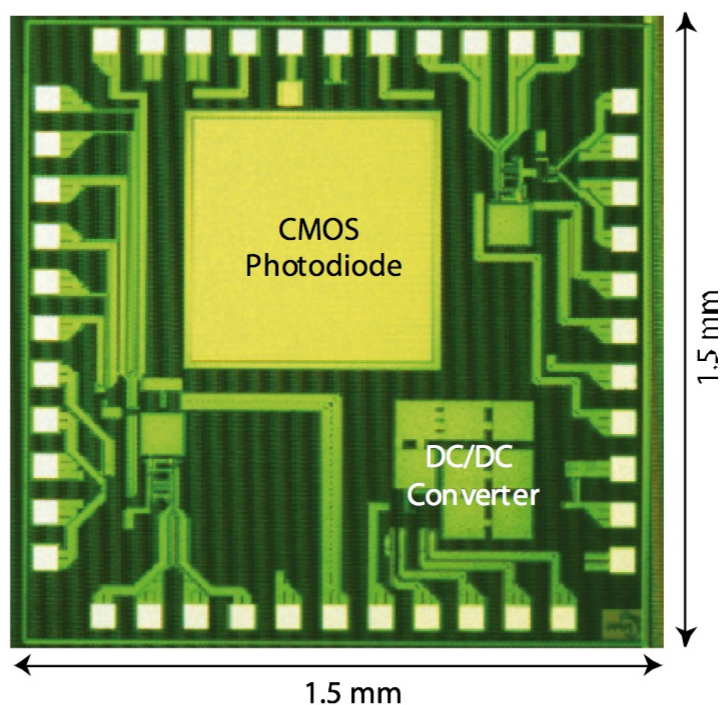

Figure 2.6. Micrograph of the second generation CMOS based optical power supply and transceiver chip.

graph is shown on Figure 2.6, the dimensions of the n-well and triple-well photodiodes has been changed and the metal patterns on top of them had not been implemented in the foundry. The integrated triple-well photodiode has an area of approximately

600 μm $\times$ 600 μm. The characterization results of the second generation triple-well photodiode is given in Figure 2.7 At 40 mW incident optical power, given by a 660 nm red laser source, the photodiode has a responsivity value of approximately 0.102 A/W. The current-to-voltage characteristics at various optical power levels indicate that the harvested electrical power is enough to operate the DC/DC converter and the transceiver circuitry on the mentioned IC which requires 5mW. The n-well photodiodes on the second IC are used for optical switching and as a source for the local oscillator signal. Two n-well photodiodes in the second IC has dimensions of 50 μm $\times$ 50μm. Furthermore, the uncovered n-well photodiode can be seen at the top of huge triple-well photodiode in Figure 2.6. The current-to-voltage characteristics,as shown in Figure 2.8 of the uncovered n-well photodiode shows the fact that it can supply enough current to gates of a transmission gate which is used as a switching circuit at the DC/DC converter output. The optical switching scheme by using the n-well photodiodes are given in Figure 2.9. The output voltage of the triple well photodiode is

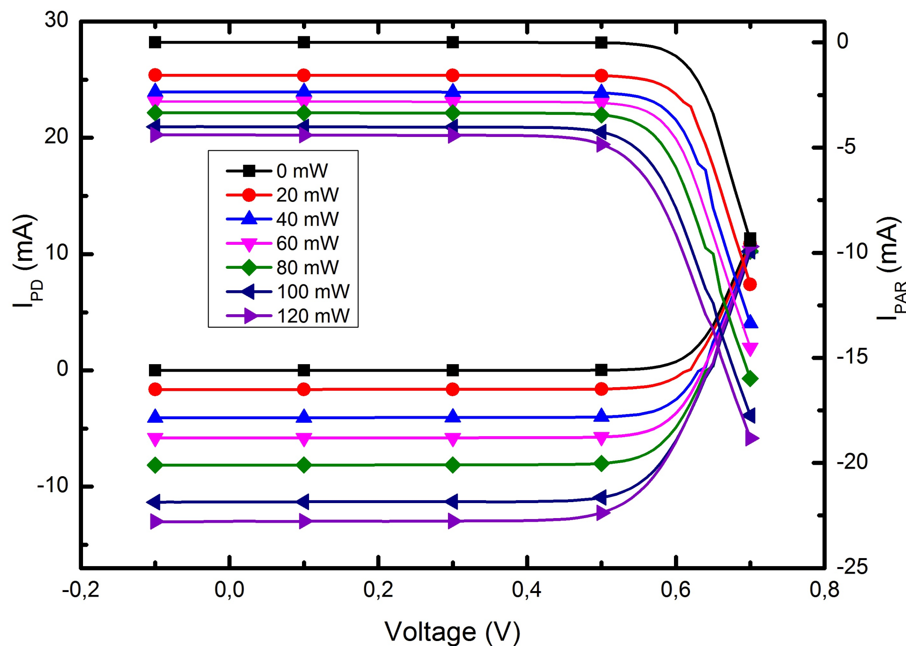

Figure 2.7. Currentvoltage characteristics of the parasitic photodiode and the triple-well photodiode in the secon IC at different optical power levels of illumination.

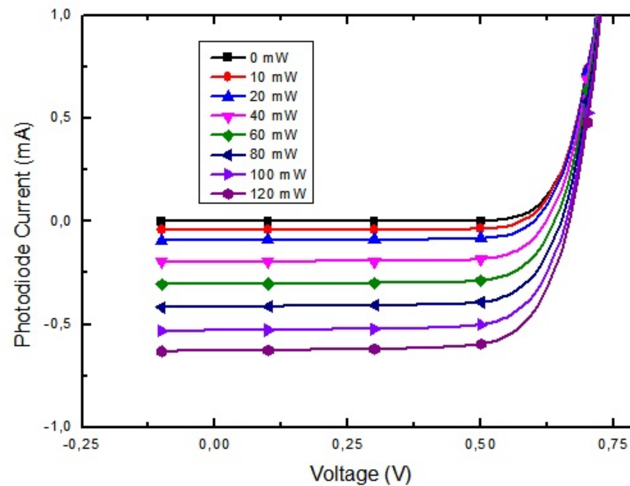

Figure 2.8. Currentvoltage characteristics of the uncovered n-well photodiode in the second IC at different optical power levels of illumination.

boosted in the DC/DC converter in order to have a sufficient supply voltage for the operation of the circuits. Then the DC/DC converter output current charges the storage capacitor at the output. In addition, an n-well photodiode, which is connected with a series resistance, is used in the photoconductive mode. When there is no light, the voltage between the terminals of the n-well photodiode is equal to the supply voltage which turns on the transmission gate and the transceiver circuit at the end operates. On the other side, when there is an incident light on the n-well photodiode, it becomes conductive and the voltage between the terminals falls off and the transmission gate is turned off. The n-well photodiode, which is covered with metal patterns as in the first IC, was added on the IC for test purposes and to obtain a differential signal for the local oscillator. The current-to-voltage characteristics of the metal covered n-well photodiode is shown in Figure 2.10.

2.2.2. DC/DC Converter

The DC/DC converter one of the essential blocks in the whole system, since it determines the supply voltage of the circuits in it. Low threshold twin-well transistors

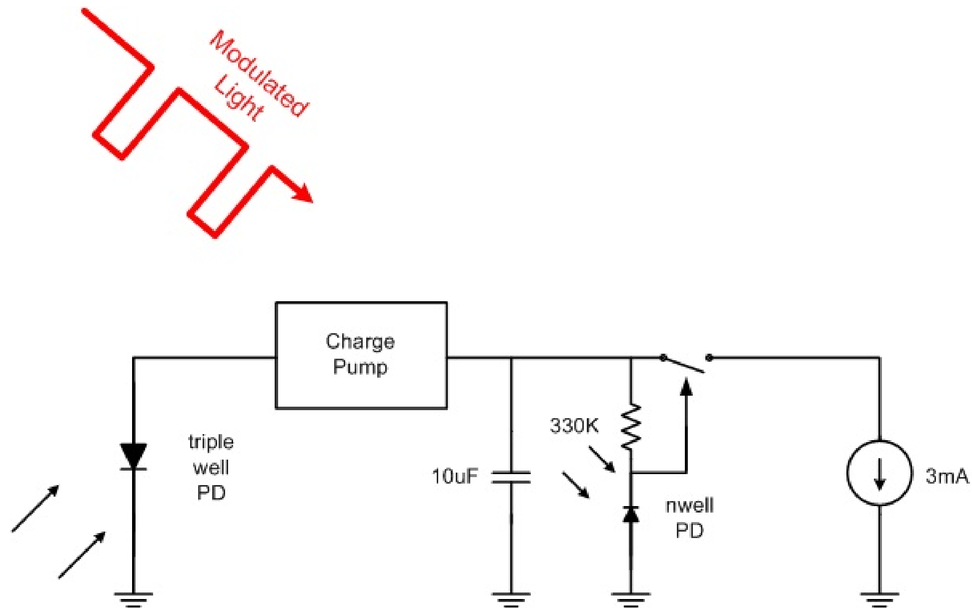

Figure 2.9. Optical switching of the transceiver circuit and DC/DC converter output.

are used to boost the voltage value that is sufficient to operate other blocks. Because of the input voltage value, around 0.5 V and 0.6 V, obtained by the triple-well photodiodes, a design that is efficient around those input levels is a major constraint for the system level. The DC/DC converter circuit this study is composed of a 2-stage voltage doubler and a ring oscillator [10]. Further theoretical information about this block is provided in [10, 11]. The characterization of the DC/DC converter circuit is given in Figure 2.11. According to the results given in the mentioned figure, the charge pump has a maximum efficiency about 56% at the input voltage level of 0.55 V. The DC/DC converter can convert 0.5 V with an input current of 0.54 mA to 1.19 V with an output current of 0.14 mA [11]. In contrast to the first generation IC, in the second IC, the input voltage and current values were much higher than the former one. In response the input values, such as in Figure 2.7, since the DC/DC converter is designed to supply an output voltage of 1.19 V at a load current of 0.3 mA. This fact reduced the efficiency of the DC/DC converter in the second IC. The characterization results obtained in the second IC is given in Figure 2.12. As it is seen on Figure 2.12, when the input voltage of the DC/DC converter circuit is 0.5 V, the output can supply an output current of 60 μA with a voltage level of 1 V. Moreover, the value

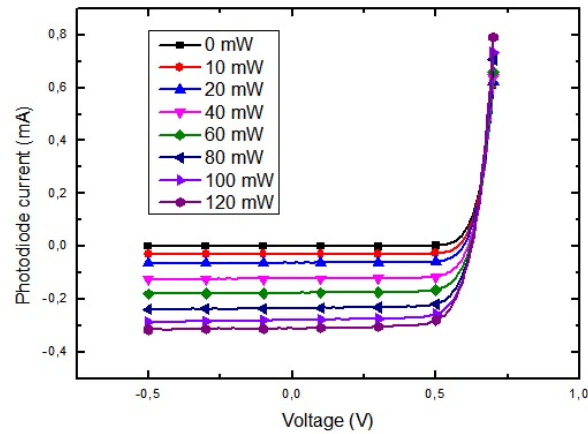

Figure 2.10. Currentvoltage characteristics of the metal covered n-well photodiode in the second IC at different optical power levels of illumination.

of output current rises up to 119 μA with an output voltage value of 1.2 V, when the input voltage is 0.55 V. Finally, 261 μA of output current has been measured with an output voltage of 1.2 at 0.6 V of input voltage. However, by adjusting the optical switching period and pulse with, it is possible to use the optoelectronic power supply for a micro scale application.

2.3. LED Driver

In this part, the most outer block of the back-end part of the system is explained. Firstly, the reason for using an LED die, instead of a laser die is presented, with modeling data. In the second subsection, current source design topologies will summarized. Afterwards, design of the implemented circuit on the third generation IC will explained. Finally, schematic and post layout simulations are explained.

2.3.1. LED vs LASER

For the reasons explained in the introduction, transmitted optical signals through a fiber is used for sending the output of the transceiver circuit. In the project the sig-

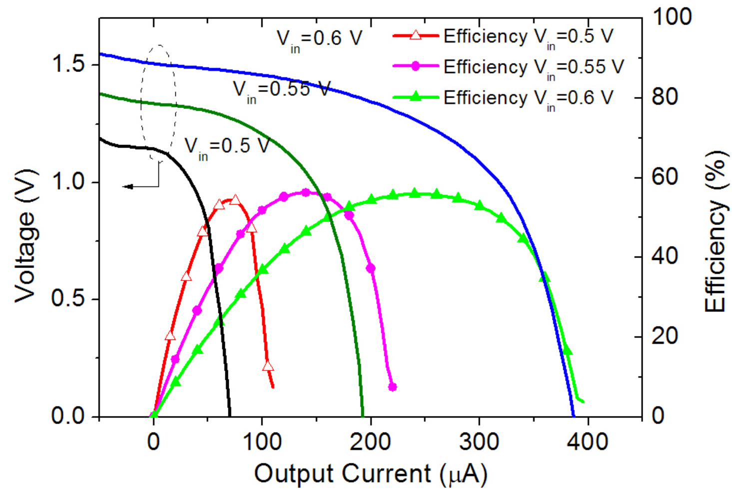

Figure 2.11. Output voltage and the efficiency of the DC/DC converter as a function of the current drawn from the output of the circuitry for different values of the input voltage to be boosted.

nals carry position information of a catheter tip as mentioned before. However, it was unclear at the beginning of the project that whether the light source should be a laser or an LED. A laser can transmit high frequency signals at cost of power in an effective way such that optical signals having a frequency at hundreds of MHz can be generated. However, the power budget limits the project to choose lasers with low threshold current values. On the other hand, LED is another effective choice to generate optical signals at relatively low frequencies compared to a laser. The explanation is as follows. Since in LEDs the photons are generated by spontaneous emission, which is the process a light source in an excited state undergoes a transition to a state with a lower energy, whereas in a laser diode photons are generated by stimulated emission, which is the process an atomic electron interacting with an electromagnetic wave of a certain frequency, may drop to a lower energy level transferring its energy to that field, the radiative lifetime of an LED is always longer than a laser [14].

In this study the wavelength of the illuminating module candidates were in the order of 1310 nm and 1550 nm. One candidate was a laser die, Roithner Chip-1310-P5, which can emit an light with maximum optical power of 5 mW at 1310 nm up to 2.5 GHz. The other one was a LED die, Roithner C155-30, which can emit light at a

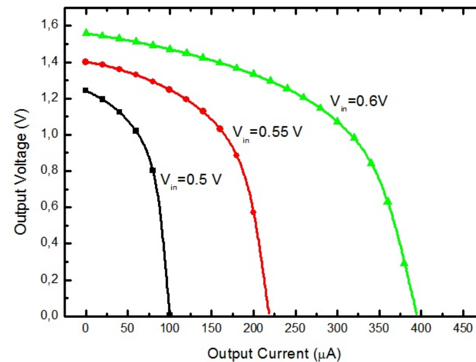

Figure 2.12. Output voltage of the DC/DC converter, in the second IC, as a function of the current drawn from the output of the circuitry for different values of the input voltage to be boosted.

wavelength of 1550 nm.

According to the methods given in [15] and [16] an LED or a laser diode can be modeled as equivalent circuits as given in Figure 2.13 and 2.14. The LED and laser diode dies, both from Roither, has been characterized by using a semiconductor parameter analyzer (Keithley SCS4200) as shown in Figure 2.15 and a network analyzer (Rohde&Schwarz ZVB4). The model parameters has been calculated by using the formula given in [16] as in equations 2.6 and 2.7 and by a curve fitting program called I-V fit.

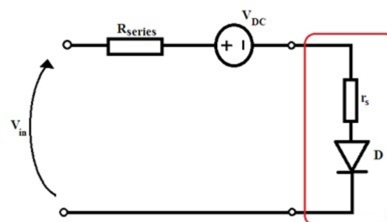

Figure 2.13. Equivalent circuit model for DC analysis of an LED/Laser diode die in I-V fit.

In Figure 2.13, the parameter R_{series} represents the ohmic series resistance which

is added by the instrumentation setup and the parameter V_{DC} is added to represent the turn-on voltage of the LED which generally higher than a diode. The r_s parameter represents the series resistance on the device and an ideal diode completes the model.

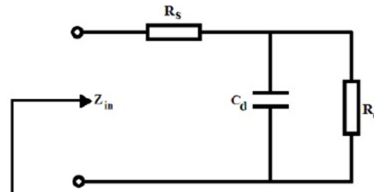

Figure 2.14. Equivalent circuit model for AC analysis of an LED/Laser diode die.

$$|Z_{in}| = R_s + \frac{R_d}{1 + sR_dC_d} \tag{2.6}$$

$$|Z_{in}| = R_s + R_d = mV_T/I_b \text{ at low frequencies} \tag{2.7}$$

After modeling the laser diode and LED diode parameters, minimum detectable signal measurements were done by using a FC fiber connector coupled photodiode(PD) (Roithner PF-521) and a PD die(Roithner EPD-1300) by using butt coupling on the illuminating elements. The results such that 0.5 mA of diode current with a voltage of 0.62 V across the terminal of the photodiode where as minimum detectable light level achieved at current of 1.5 mA on the laser diode die, showed that using an LED die is much more power saving due than the laser diode die. The simplest explanation for this result is the threshold current of the laser diode die as shown in Figure 2.16. The threshold current is where stimulated emission starts in a laser. However, optical behavior of a laser diode, as explained in [14] below threshold current also explains

this fact since the power budget is limited in a few milliwatts [14]. The bandwidth of the wavelength of the emitted light expands such that the emitted light might not cause a detection signal on the photodiode used during the measurements.

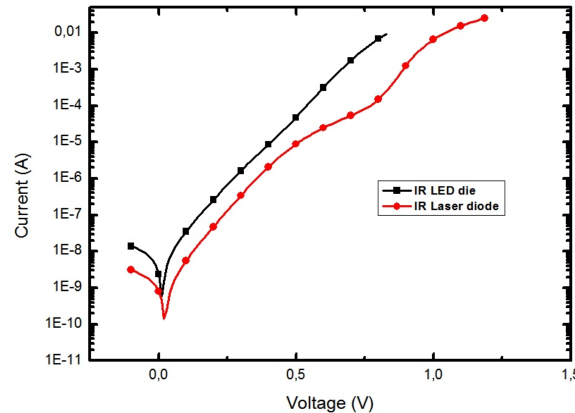

Figure 2.15. Current versus voltage characteristics of LED(Roithner C155-30) and Laser diode (Roithner Chip-1310-P5) dies.

2.3.2. LED/Laser Driver Topologies

In this part, some driver topologies are explained as a guideline to the final design. Furthermore, the reasons for elimination is explained at each circuit. In most of the publications surveyed such as [17, 18, 19, 20, 21] , designed circuits were unique to drive a specific laser diode or an LED as part of an application like communications, imaging etc.

The simplest way to drive a current mode nonlinear circuit element, like an LED or a laser diode, is using a series resistor or a transistor as a voltage dependent current source. Yet, these techniques lack in efficiency since using a resistor is a power hungry solution and variations between transistors and exponential behavior of drain currents versus applied gate voltages to them.

The trivial solution for driving the IR LED die is designing the on chip version

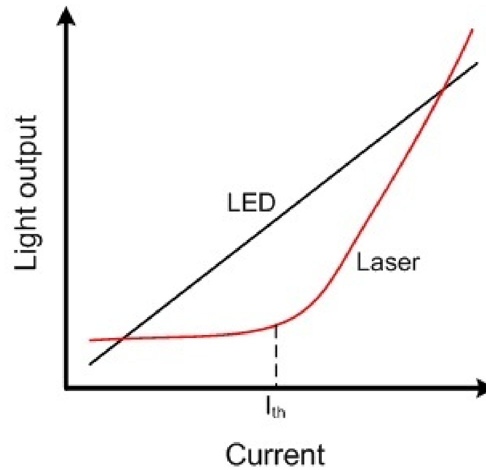

Figure 2.16. Light output characteristics of LED/Laser diode die with respect to the driving current.

of the circuit in Figure 2.1. First, an on chip operational amplifier has been designed in ADS design tool using UMC 0.18 μm technology parameters. The schematic of the designed opamp is given in Figure 2.18. The on-chip opamp used with a DC input offset voltage in the feedback loop since the supply voltages are 0 V and 1.2 V. Then, a large load transistor (W = 160 μm and L = 1 μm) compared to the technology used and a feedback resistor a with a low resistance value of 5 Ω has been used to drive the subcircuit of the LED model. Despite the fact that the voltage-to-current conversion is as expected, the current consumption of the LED driver is approximately 0.5 mA in the simulations. The current consumption of the proposed LED driver circuit is much more current than the desired value which on the order of 100 μA. Furthermore, the current output of circuit is very sensitive to the voltage variations. However, the supply voltage and the proposed signal voltage is measured to decrease during the operation, as in the Figure 2.17 since the circuit is supplied by a capacitor. Consequently, due to its power consumption, area cost and sensitivity to shifts in the supply and the signal, this circuit is not a successful candidate to implement on silicon.

The decreasing supply voltage problem has led to a design that is insensitive to changes in the supply voltage. Self biasing can greatly reduce this problem. Instead of of connecting a resistor to the the supply, the input current is made to depend

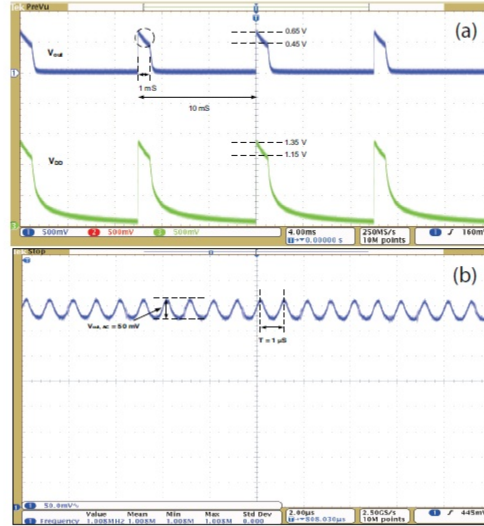

Figure 2.17. (a) The measured output voltage of the primitive LED driver circuitry in the second IC (Vout) and the supply voltage, (VDD) (b) Vout shown in a larger scale.

on the output current of the current source itself. Such feedback loop can be seen on the schematic diagram, Figure 2.19, of the circuit. However, a starter circuit is needed to assure that the circuit operates in non-zero current value. In Figure 2.19, the schematic of the self-biasing V_t reference is given. The circuit composed of T_1, T_2 and R dictates that the current I_{OUT} depends on I_{IN}. Equation 2.8 and 2.9 show this relationship between the currents. The bias currents are independent of the supply voltage without including the finite output resistances of the transistors. Transistors T_6 and T_3 forms a current mirror with transistors T_5 and T_1, respectively such that they supply current to other circuits [22].

$$I_{OUT} = \frac{V_{BE1}}{R_2} = \frac{V_T}{R_2} \ln \frac{I_{IN}}{I_{S1}} \tag{2.8}$$

$$I_{OUT} = \frac{V_{GS1}}{R_2} = \frac{V_t + V_{ov1}}{R_2} = \frac{V_t + \sqrt{\frac{2I_{IN}}{k'(W/L)_1}}}{R_2} \tag{2.9}$$

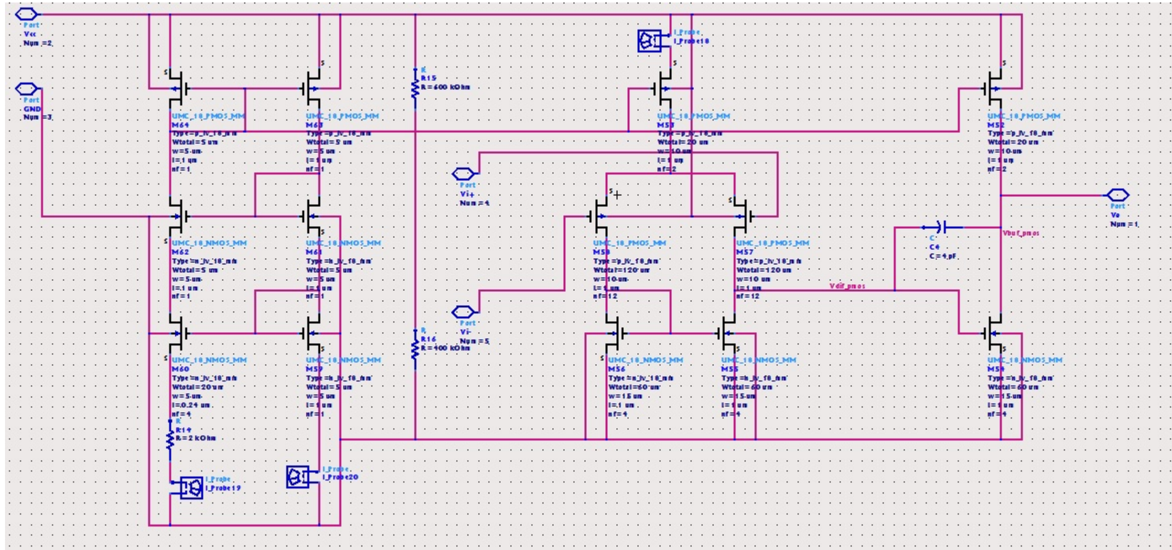

Figure 2.18. Schematic of the opamp as seen in ADS design tool.

2.3.3. Supply Insensitive LED Driver

The LED driver implemented on the third IC is inspired from the self-bias current source in order to have a supply insensitive current source. The input signals coming from the catheter localization circuit are digitized with a comparator at the end [1]. This led to a more efficient input signal to be converted to a current because in the former studies [12], the AC component of the light was very low, making it harder to detect the dimming of light. The supply insensitive current source has been implemented with a starter circuit at first. The starter circuit consists of an inverter, which is connected between the gate of the T_1 and the gate of feedback pull down transistor, and a feedback pull down transistor, aforementioned, which is connected to gates PMOS current mirror transistors from its drain and its gate connected to the output of the inverter. In steady state, the gate voltage of pull-down transistor in the inverter rises to $I_{OUT}R$, which turns on it and reduces the gate voltage of the PMOS current mirrors when the reference circuit is on. The inverter output should be low enough to keep the feedback pull-down transistor off in the steady state. To satisfy this, the aspect ratio of the pull down transistor in the inverter is chosen much higher than the pull up transistor [22].

Figure 2.19. Self-biased current source.

In the designed circuit shown in Figure 2.20, an inverter to the input port is added in order to keep the output current in phase with the input voltage. Furthermore, two pull-down transistors are added in order to modulate LED current by turning the supply insensitive current source on and off. The input signal to the LED driver is expected be around 1 MHz with a bandwidth value of 400 kHz. The frequency shift, as mentioned before, gives the information of relative displacement of a catheter tip inside an MRI device. Transient simulations with an input voltage value of 1 MHz at at different supply values are done with schematic in Mentor Graphics. The simulation data belonging to schematic designs are given in Figure 2.21, 2.22 and 2.23. The DC simulation results of the schematic design, as shown in Figure 2.21, state that a peak of LED current of 2 mA is achieved at a supply voltage of 1.075 V. On the other hand, in the saturated operation, which starts at 1.15 V, range the current change versus the supply voltage is 0.263 mA/V according to the DC simulation results. Thus, the LED driver can safely operate at a supply voltage of value more than 1 V. The transient simulation results at a supply voltage value of 1 V, as shown in Figure 2.22, states that the peak current of 1.904 mA is achieved. The rise

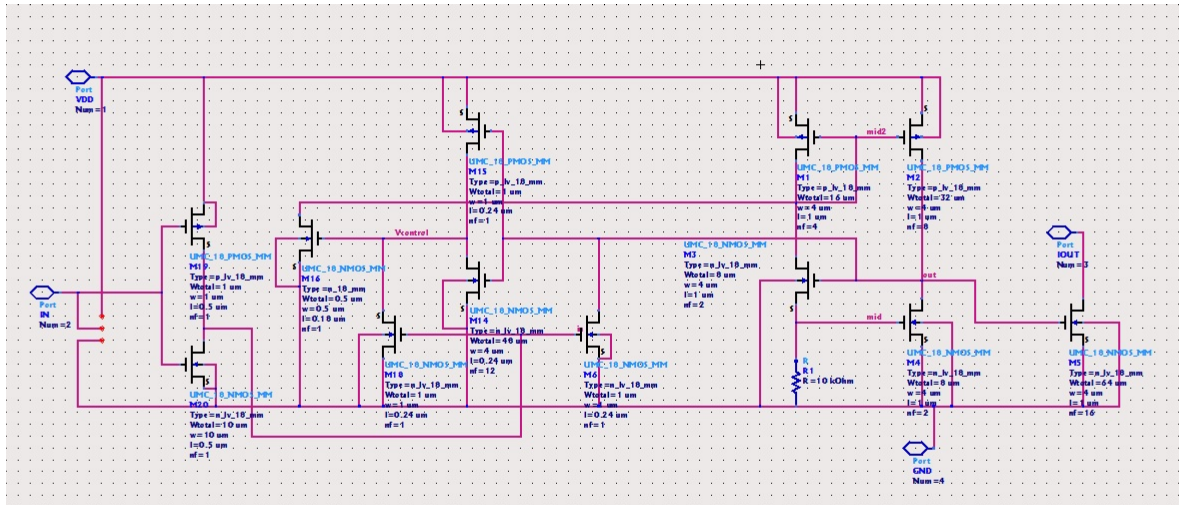

Figure 2.20. Schematic of the designed LED driver as it looks in ADS schematic design tool.

time of the LED current is simulated to be 3.968 ns whereas the fall time is 1.32 ns. In the transient simulation, at a supply voltage value of 1.5 V, as shown in Figure 2.23, a peak current of 2.233 mA is observed. The rise time, in the simulation, is 1.62 ns, whereas the fall time is 1.18 ns.

After validating the electrical operation of the LED driver with the schematic simulations a layout has been designed. The layout of LED driver is given Figure 2.24 The length of the metal lines from the inverter at the input to controlling pull-down transistors kept equal as much as possible. The reason for that is if one pull down transistor tries to turn off the circuit while the other one is turning it on, the output current oscillates. Simulations, on the other hand, also show that the delay is negligible such that no oscillation occurs during transition. The layout of the LED driver, as shown in Figure 2.24, is designed in Mentor Graphics with UMC 0.18 μm design parameters. The transistors of the supply insensitive current source are merged in order to minimize area cost. In addition, the switching transistors, which are added to modulate the output current at the input and output terminals of the feedback inverter, have been placed at equal distances to their connections in order to minimize the switching time difference between them.

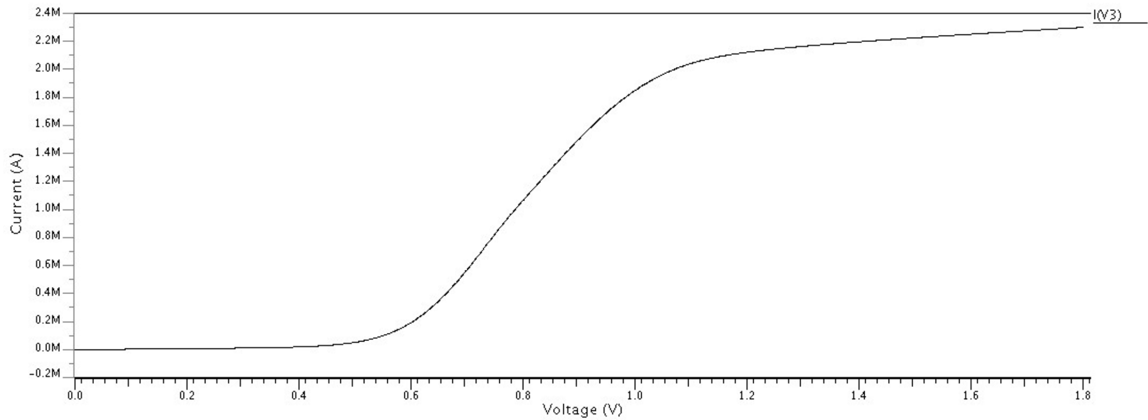

Figure 2.21. The DC characteristics, driving current versus the supply voltage, of the LED driver.

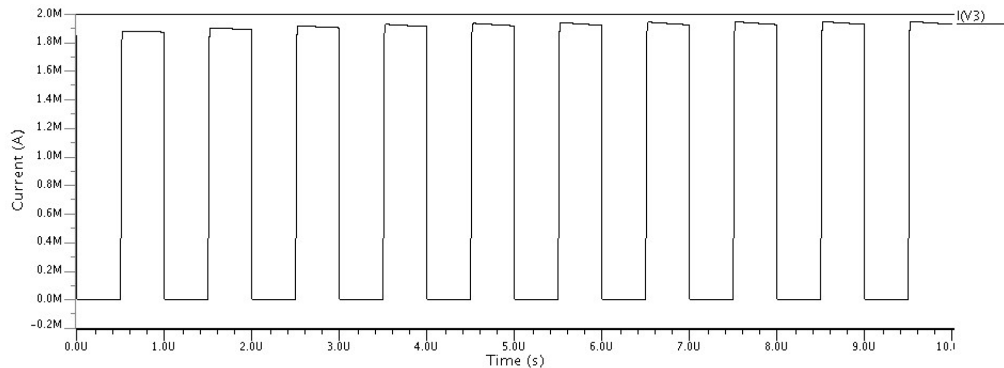

Figure 2.22. Transient simulation data at supply voltage value of 1 V.

The post-layout simulation results are also consistent with the schematic simulation results. In Figure 2.25, 2.26 and 2.26, the transient and DC simulations results can be seen such that the LED current is modulated between 0 and approximately 2 mA. This current value can also be detected without need to a complex front-end circuitry. In addition, both schematic and post layout simulations show that the current consumption of the LED driver is approximately 135 μA such that the most of the current goes to the feedback inverter.

The DC simulation of the post-layout, as shown in Figure 2.25, states that a

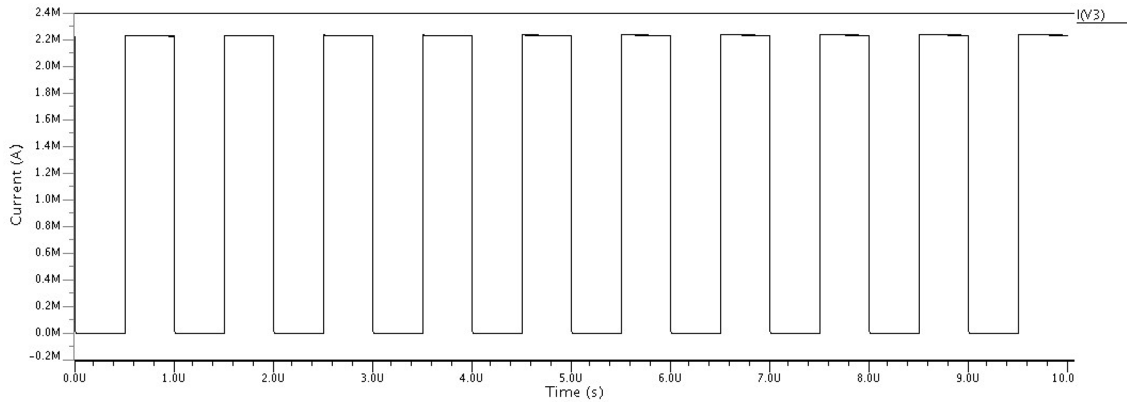

Figure 2.23. Transient simulation data at supply voltage value of 1.5 V.

peak current of 2 mA is achieved at 1.14 V of supply voltage. The change of current with respect to the supply voltage is 0.262 mA/V at saturation level which starts at 1.12 V. Thus, the LED driver can operate safely with a supply voltage value of more than 1.12 V.

In the post layout transient simulation with a supply voltage of 1 V, as shown in Figure 2.26, a peak current of 1.825 mA has been observed. The rise time of the current is observed as 4.68 ns whereas the fall time is 1.16 ns in the transient simulation. The value of observed peak LED current is 2.119 mA, in the post layout simulation shown as in Figure 2.27, when the supply voltage is 1.5 V. The measured rise time of the current, in simulation, is 1.84 ns whereas the fall time is 1.17 ns.

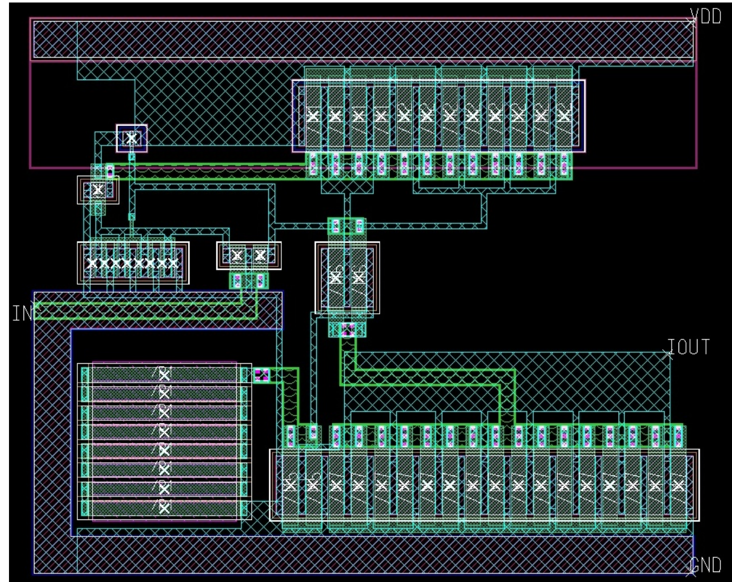

Figure 2.24. Layout of the LED driver implemented on the third generation IC before the post layout simulations.

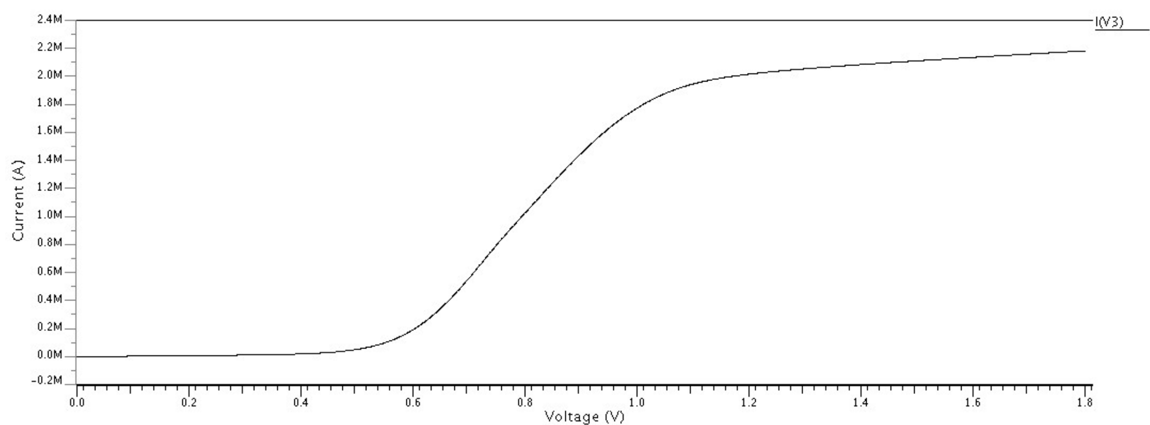

Figure 2.25. The DC characteristics of the post-layout circuit, driving current versus the supply voltage, of the LED driver.

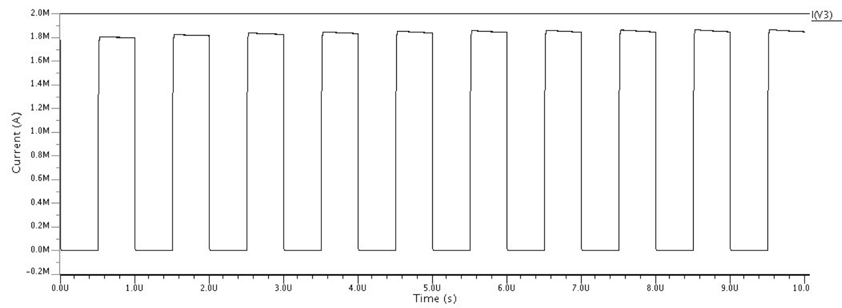

Figure 2.26. Transient simulation data of the post-layout circuit, at supply voltage value of 1 V.

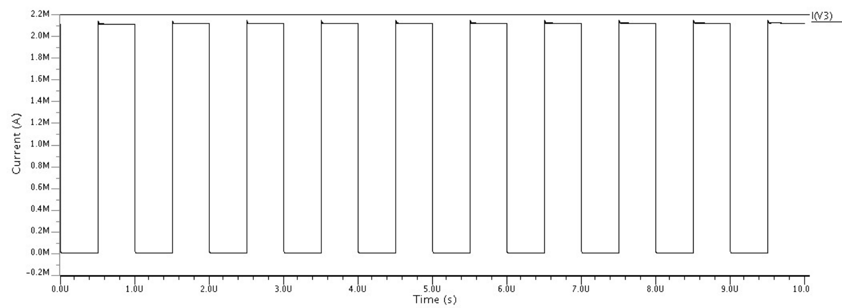

Figure 2.27. Transient simulation data of the post-layout circuit, at supply voltage value of 1.5 V.

3. OPTICAL TRANSMISSION PATH

In order to align light to the chip, an optical transmission path consisting of fibers, aligners and a silicon micromirror has been developed. Firstly, fiber alignment issues are explained with photonics approach. Afterwards, design, manufacturing and characterization issues related to silicon micromirror are covered.

3.1. Fiber Alignment for Directing Light Beams

In the project light coming from a modulated laser source is used for powering the circuitry and generating the signal for driving the local oscillator input. The light beam coming from the laser is directed into a multi-mode fiber in order to have a flexible transmission path and control the beam area. Another application is using butt coupling for the light output of the IR LED which gives the localization information to front end circuit outside the catheter.

To reduce the number fiber aligned on the IC, a novel photodiode structure has been proposed such that a donut-shaped triple well photodiode surrounds the small n-well photodiodes, which are used for smart on-off and as an optional LO input signal source, in the middle. The structure can bee seen from the layout of the third generation IC, in Figure 3.1.

3.2. Silicon Platform

In the literature, there are several examples integrating Si V-grooves and optoelectronic circuits like optoelectronic comminucation modules [23] and optically powered circuits [5]. Guiding light beams to the CMOS-integrated photodiodes is done by using a bulk micromachined silicon mirror which allows efficient coupling of the light beams coming out of the multi-mode fiber optic cable. Design of the silicon fiber platform is performed by running geometrical optics simulation in order to predict beam geometry, optical design parameters and efficiency of light capture. In the fur-

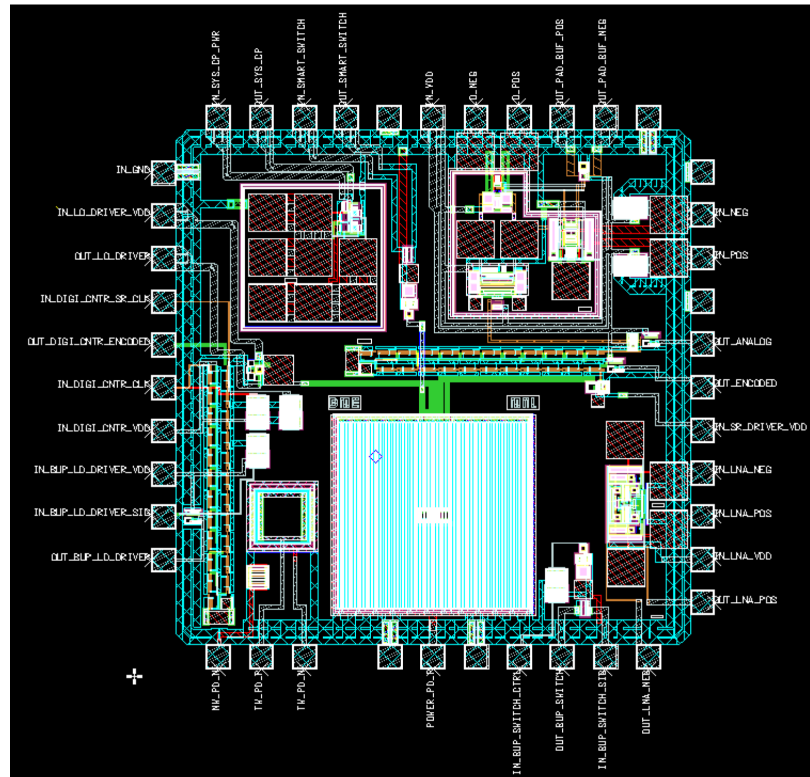

Figure 3.1. Layout of the third generation IC.

ther subsection, the manufacturing process, its effects on the optical properties are expressed. In the final subsection, the measurement results of the mirror regarding its efficiency and beam shape are expressed with integration and packaging effects in the whole system.

3.2.1. Design of Silicon Platform

At the beginning of the design, to have an insight of the the problem, information about the target IC, which contains the CMOS-integrated photodiode, is obtained. The dimensions of the integrated circuit dies were 1.5 mm x 1.5 mm. Moreover, the photodiode dimensions and positions were different at each generation of IC design. In addition, the behavior of the fiber and mirror surface were effective on the design as well. However, even the fabrication process limits the number of parameters to be manipulated, beam spot size and position can be fitted to each generation of integrated circuits.

3.2.1.1. Hand Calculations. In the design of the silicon platform, one of the dominant parameters on the layout were the numerical aperture (NA) of the optical fiber. The numerical aperture of NA = 0.275 of the fiber corresponds to an aperture angle β of

$$\beta = sin^{-1}(NA) = 15.96° \quad (3.1)$$

Another constraint on the design was caused by the fabrication method, i.e. KOH etching. The mirror structure was anisotropically wet-etched into a 500μm silicon substrate by KOH, which stops etching at the (111) crystal plane, thus leaving the reflective plane under an angle $\alpha = 54.7°$. Under these constraints, the distance and the height of the fiber relative to the photodiodes on the optoelectronic power supply can be calculated to achieve optimum illumination on the photodiodes.

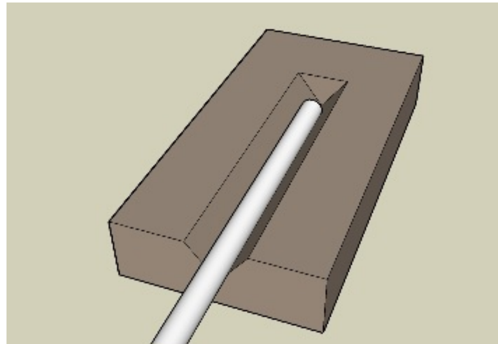

Figure 3.2. 3D sketch of the fiber placed on the first structure.

At the first glance, using a V-groove may be seen appropriate. Yet, the aperture angle β sets a constraint on the distance between the fiber tip and silicon surface. Since the aperture angle $\beta = 15.96°$ and from the trigonometric relations in a right triangle which has sides of the fiber radius, side wall of the V-groove and the light beam, maximum distance from the reflective surface of the fiber tip in a simple V-groove is;

$$l_{max} = f \times \cot \beta \tag{3.2}$$

$$l_{max} = 62.5 \times \cot 15.96^\circ \tag{3.3}$$

$$l_{max} \simeq 100 \mu m. \tag{3.4}$$

Due to the the aperture angle, after 100μm distance to the fiber tip, the light beam reflects not only from the desired mirror surface but also from the sidewalls. This phenomenon disrupts the beam spot as well. Furthermore, such structure needs to placed at a higher level than the chip surface, which is not practical. As it is shown in Figure 3.2, the structure has a simple geometry, but does not satisfy optical constraints. To satisfy the optical constraints, the scheme in Figure 3.3 is proposed.

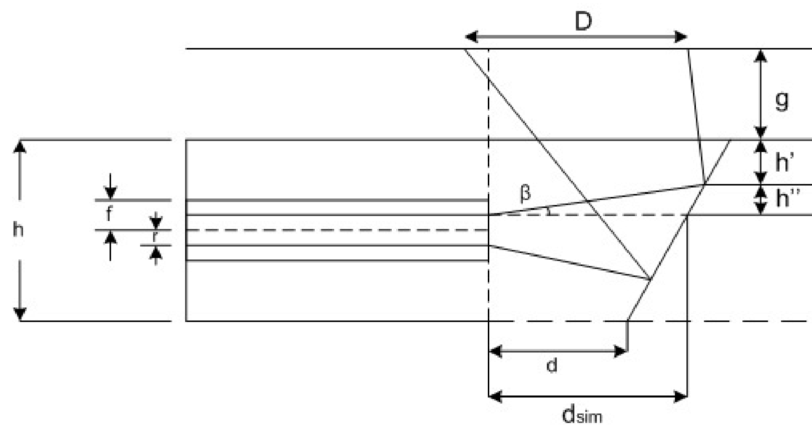

Figure 3.3. Side view and the geometric design variables.

In order to have a equation showing the relation between the position of the optical fiber tip, groove depth and beam spot size, the geometry of the optical setup is drawn and every geometric parameter is listed. According to drawings, geometric and trigonometric relations, finally, formulas for calculating the width of the V-groove and opening width of the mirror are obtained. The whole system was simulated by using 20 parameters where 6 of them are independent design parameters. The parameters used in equations are as follows:

- d: Distance between the fiber and the mirror
- h: Height of the V-groove
- f: Outer radius of the fiber (62.5 μm)
- r: Inner radius of the fiber (31.25 μm)
- β: Angle of aperture
- g: Gap between the Si die surface and the chip surface

Remaining 14 parameters are named as $x_0, x_1, x_2, ..., x_{11}, h', h''$, which are intermediate variables used in order to represent side lengths and heights on the geometrical drawings.

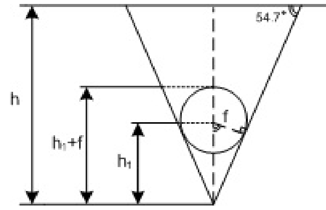

Figure 3.4. The cross sectional geometry of the V-groove with the fiber inside.

As it is seen on Figure 3.4 the value of h_1, which is height of the fiber core from the bottom of the V-groove, is directly related to the fiber radius due to trigonometric relations. Thus, using Equation 3.5, the value of h_1 is found to be $108.16\mu m$. As a result, the depth of the V-groove on the fiber platform can not exceed the height of the Si wafer and the minimum depth of the V-groove must satisfy the condition that the fiber optical cable lies under the surface of the wafer. This situation is explained in the Equation 3.6.

$$\frac{f}{h_1} = \cos 54.7°, f = 62.5\mu m \tag{3.5}$$

$$h_1 + f \leq h < h_{SiDie} \tag{3.6}$$

$$h_1 + f = 170.66\mu m \tag{3.7}$$

$$h_{SiDie} = 500\mu m \tag{3.8}$$

After deciding the geometry and and listing the conditions, an equation giving the illumination diameter can be achieved by using geometrical and optical relations. The optical behavior of the system has been inspected in two parts. In the first part, the light leaving the optical fiber with aperture angle of β travels through the mirror surface which is a 111-plane on the Si platform. This part is shown on Figure 3.5. The numbers inside circles represent the triangles in Figure 3.5. By using the geometric and trigonometric relations in the triangles, it is possible to obtain the values of the parameters in the design.

Figure 3.5. Rays leaving the optical fiber and reflecting from the mirror surface.

The first three triangles, in Figure 3.6, 3.7 and 3.8 are used to find x_2 (the height of bottom point of reflection from the mirror) and x_4 (the length between the bottom point of reflection and the inner optical fiber core). The fourth triangle is used for finding the uppermost reflection point at the mirror surface on the Si platform. By using relations between all of the four triangles, beam spot size diameter on the mirror surface is found. In the first triangle, shown in Figure 3.6, the value of x_0 can

Figure 3.6. The first triangle.

be determined by Pythagorean theorem as it is shown in Equation 3.9.

$$x_0 = \sqrt{d^2 + x_1^2}, \quad x_1 = d \cdot \tan \beta \tag{3.9}$$

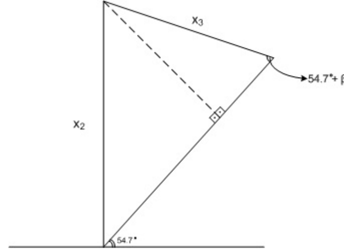

Figure 3.7. The second triangle.

In the second triangle, shown in Figure 3.7, parameters x_2 and x_3 derived in order to get the height of the bottom point of reflection on the mirror surface. Obviously, those parameters were derived by using Pythagorean theorem and trigonometric relations as in Equation 3.10 and 3.11.

$$x_2 = h_0 + f - r - x_1 \tag{3.10}$$

$$x_3 = \frac{x_2 \cdot \sin(35.3^\circ)}{\sin(54.7^\circ + \beta)} \tag{3.11}$$

The third triangle in Figure 3.8 is used for calculating the length of the bottom part of beam spot which is being reflected from the mirror. The triangle is used for calculating the value of x_5 which denotes the bottom part of the reflected beam.

From the triangle in Figure 3.8, values of the parameters x_4, x_5, and x_8 are calculated in Equation 3.12, 3.14 and 3.13, respectively.

$$x_4 = (\sin \beta) \cdot (x_0 + x_3) \tag{3.12}$$

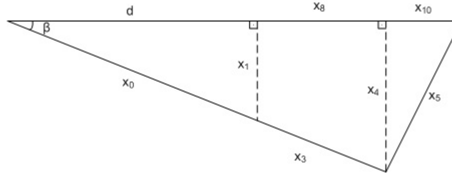

Figure 3.8. The third triangle.

$$x_8 = \frac{d \cdot (x_4 - x_1)}{x_1} \tag{3.13}$$

$$x_5 = \frac{x_4}{\cos(35.3°)} \tag{3.14}$$

Values of the parameters x_6, x_7, and x_{11} are calculated in Equation 3.15, 3.16 and 3.17 by using the similarities in triangles and trigonometric relations.

$$x_6 = \frac{2r}{x_4} \cdot x_5 \tag{3.15}$$

$$x_7 = (x_5 + x_6) \cdot \sin(35.3°) \tag{3.16}$$

$$x_{11} = \frac{r}{\tan(54.7°)} \tag{3.17}$$

In Figure 3.9, the triangle is used to obtain the value of x_9, which presents the length of the uppermost part of the beam on the mirror surface. The upper part of the incident light beam leaving the fiber with aperture angle β hits the mirror surface and it is reflected to the surface of the CMOS-integrated photodiode on the IC.

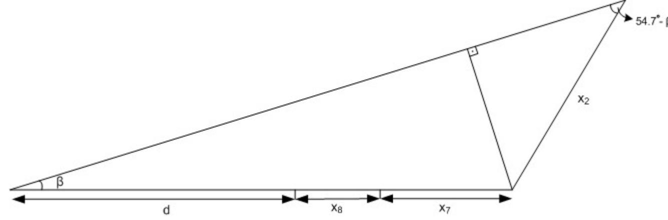

Figure 3.9. The fourth triangle.

The value of x_9 is obtained by the trigonometric relations on the right triangles inside the triangle shown in Figure 3.9.

$$x_9 = \frac{(d + x_8 + x_7) \cdot \sin(\beta)}{sin(54.7° - \beta)} \tag{3.18}$$

$$h'' = x_9 \cdot \sin 54.7° \tag{3.19}$$

Finally, to find the diameter of the incident light beam illuminating the IC surface, geometric scheme in Figure 3.10 is used. By using the figure, it is possible to define the diameter value D as a function of the design parameters d, h, f, r, g and β.

Figure 3.10. Reflected light beam from the mirror surface illuminates the surface of the IC.

$$
\begin{aligned}
D &= f(d, h, f, r, g, \beta) \\
D &= m + l + n \\
D &= [h' + g + (x_5 + x_6 + x_9) \cdot \tan(35.3°)] \cdot \tan(19.4° + \beta) + \\
&+ (x_5 + x_6 + x_9) \cdot \sin(35.3°) - (h' + g) \cdot \tan(19.4° - \beta) \quad (3.20)
\end{aligned}
$$

3.2.1.2. CAD Simulations. After completing the hand calculations on the basis of ray optics and geometry, the validity of the equations were verified using an optical design tool called ZeMax [24]. By using the simulation tool, it is possible to control such parameters like NA of the fiber, index of refraction of all mediums, distance between the fiber and the mirror, tilt angle of the mirror and depth of the V-groove. Optical media in ZeMax are defined as surfaces and the volume between the surfaces forms the optical space where the light travels. The rendered model of the optical setup is shown in Figure 3.11.

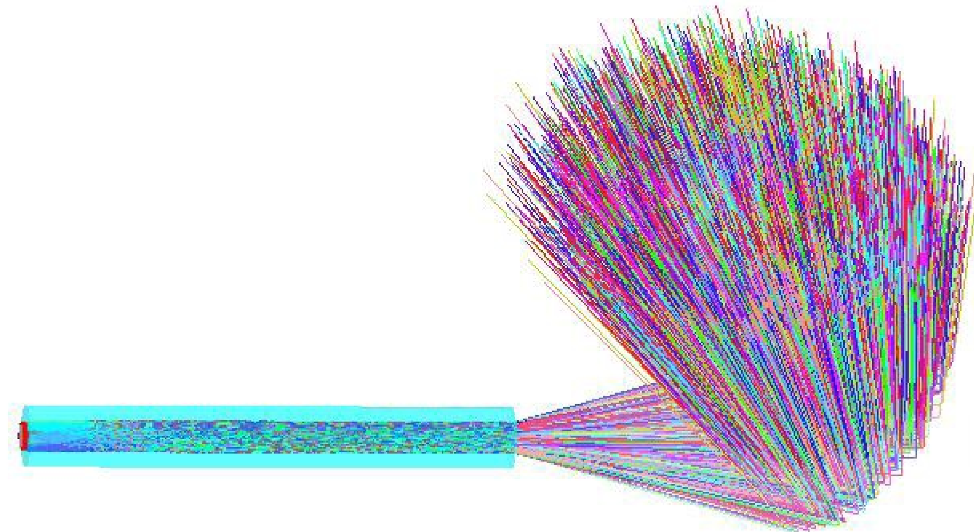

Figure 3.11. Rendered model of the optical setup.

In the same work [24], the effect of changes in the index of refraction of the mediums are also shown. With these results, it gave the foresight for changing the spot size by means of using transparent mineral oils as a result of Snell's Law. The simulated layouts for different mediums are added in Figure 3.12 and 3.13.

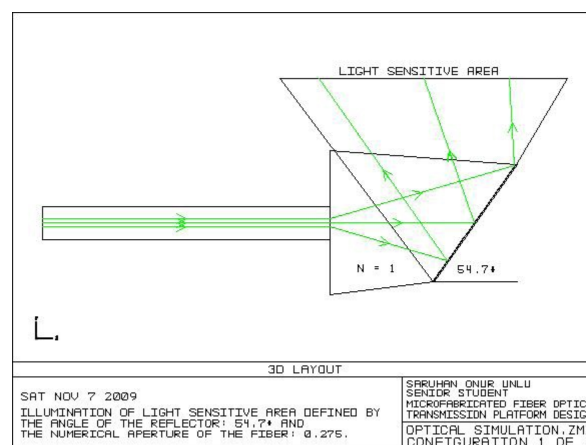

Figure 3.12. Simulated 3D layout for n = 1.

3.2.1.3. Layout Design. The final design step is the layout design of the mask for lithography. In the layout design, the important design parameters of the fiber platform are width (w) and depth (h) of the V-groove, width of the mirror opening (y),

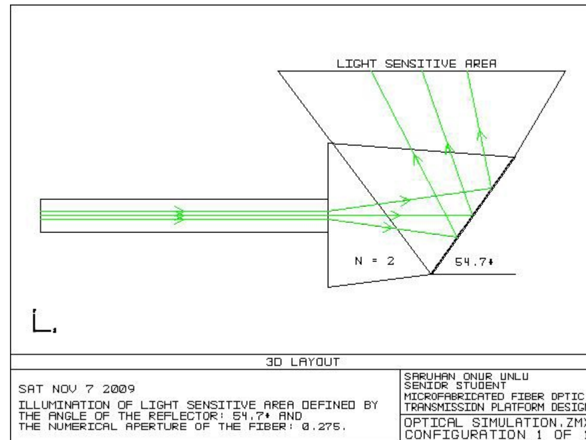

Figure 3.13. Simulated 3D layout for n = 2.

separation between the fiber tip and the mirror opening (d) and the distance between the center of the fiber core and the bottom of the V-groove (h_1) as it is shown in Figure 3.14. Numerical aperture of the mirror defines the mirror size and the separation between the mirror and the fiber. Then, the width of the V-shaped groove can be calculated as in Equation 3.21 which is only dependant on the height of the channel where the fiber is placed. Opening width of the fiber is also calculated is in Equation 3.22 [11]. According to these equations the calculated values for w and y are 420 μm and 690 μm, respectively. In addition, to prevent the undercuts in the concave corners of the mask etch compensation structures are also added. Finally, three versions of masks are drawn differing in lengths of V-grooves as $l = 1$ cm, $l = 6$ mm and $l = 3$ mm. Before fabrication, two versions of masks, one for positive photo resist and one for negative photo resist were prepared and printed.

$$w = \frac{2h}{\tan(54.7^\circ)} \tag{3.21}$$

$$y = d + \frac{2(h - h_1)}{\tan(54.7^\circ)} \tag{3.22}$$

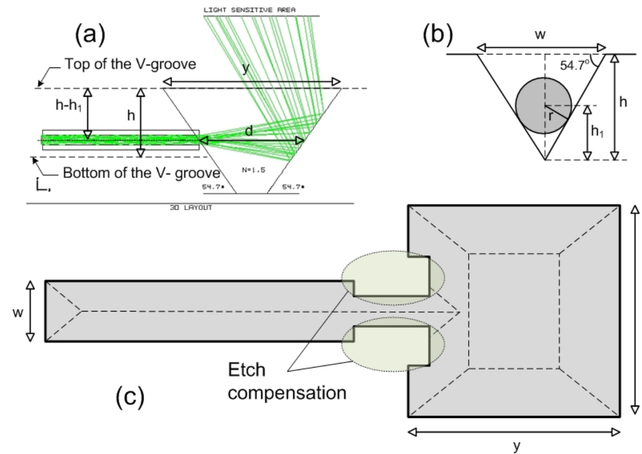

Figure 3.14. (a) Optical simulation of the micro machined fiber optic platform.(b) Cross section of the groove where fiber is placed. (c) Geometry of the silicon-based fiber platform.

3.2.2. Fabrication of Silicon Platform

After being finished with the design process and obtaining the masks, the fabrication step started. A 4-inch 500 μm wafer with Cr/Au coating has been used during the process. The fabrication steps were shown in Figure 3.15. Simply, these steps are cleaning the wafer, coating it with photo resist, lithography, developing the photo resist, mask etching, KOH etching, striping the photo resist and the Cr/Au mask and finally, Al coating and final clean.

3.2.2.1. Cleaning Before Photolithography. The 4-inch Cr/Au coated wafer used in the fabrication was an old wafer used before. There were some photo resist residues on the wafer that needed to be cleaned. The old undesirable PR residues were clean by using acetone which is a solvent for the photo resist. After solving the old PR by acetone, the wafer is cleaned in IPA (Isopropyl Alcohol) bath and it is dried by using pressured nitrogen. Furthermore, in order to get rid of the last residues of old PR, the wafer has also cleaned by using PR-remover chemical. After using the PR-remover chemical, cleaning steps involving use of acetone and IPA has been repeated on the wafer. After the cleaning step, the wafer has been heated up at 250 ^oC for 20 minutes,

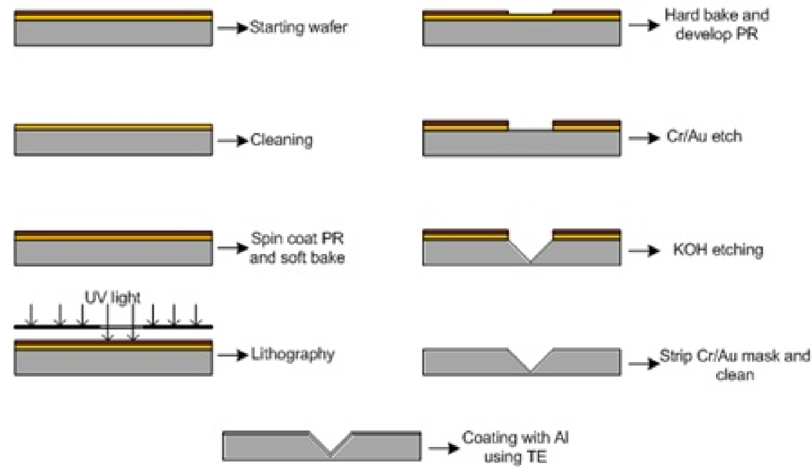

Figure 3.15. Fabrication steps to produce silicon fiber platform.

in order to dehydrate it.

3.2.2.2. Spin coating the photo resist and soft baking. Before coating the surface of the Cr/Au coated wafer, in order to improve the adhesion of the PR chemical, HDMS (Hexamethyldisilazane) priming is done. If the wafer has not been coated with HDMS, the PR would adhere to water vapor rather than the surface. During this fabrication step, liquid priming is done by using spin coater. However, using vapor priming of HDMS, which involves the use of HDMS vapor in an oven, gives better adhesion results than the former one explained. In the liquid priming done, the wafer is spin coated with half a pipet of HDMS at 4000 rpm for 30 seconds. After being finished with HDMS priming, the wafer has been coated with the photo resist chemical by using the spin coater in Figure 3.16 in order to have uniform thickness of PR on it. In this process the wafer has been spin coated with one pipet of PR 1828 at 2000 rpm for 30 seconds [24].

The final step before lithography was soft bake, i.e. pre-exposure bake, which is used to drive solvent from the resist. This step is crucial before lithography since it affects the resist profile. In this step, the wafer has been soft baked at 90 $^{\circ}C$ for one minute.

Figure 3.16. Spin coater.

3.2.2.3. Lithography. Before starting the UV photolithography, the ink side of the mask has been lined in order to minimize the alignment errors. Then the wafer has been exposed to UV light.

3.2.2.4. Developing PR and hard bake. As a second step to form the layout pattern on the wafer, the PR on the wafer surface has been developed in a solution. At the beginning of the process, custom made MF-319 PR developer has been used for 2 minutes. Then, the wafer has been washed with deionized (DI) water. However, after inspecting the wafer surface under microscopy it has been observed that there were some PR material, which has not been developed. Later, with same solution used at the beginning, PR development has been done in three sessions which have durations of 15 seconds, 30 seconds, 30 seconds, respectively. After these three sessions, PR developer solution started to saturate and it is renewed. Again, three sessions of PR developing has been done as 35 seconds, 1 minute and 75 seconds, respectively. After, each step of PR development the surface of the wafer has been inspected under microscopy [24].

Being finished with the PR development, the remaining PR has been hard baked in order to increase it's etch resistance. Moreover, hard baking cures the possible fractures on the remaining PR. Hard baking process has been done by baking the wafer at 120 $^{\circ}C$ for 30 minutes. After this process the wafer looked as in Figure 3.17.

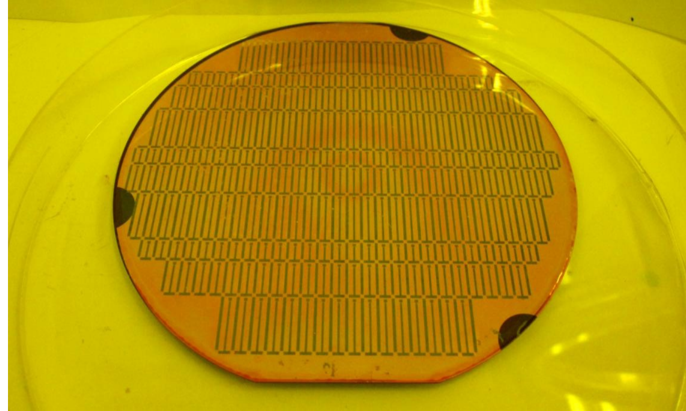

Figure 3.17. The wafer after hard baking.

3.2.2.5. KOH Etching. Before starting the KOH etch process, exposed Cr/Au layer on the wafer has been etched in gold etchant and Cr etchant, respectively. To keep the back side of the wafer from KOH solution a holder structure, made of plexiglass, with an O-ring has been designed and manufactured by using a laser cutter. Afterwards, KOH mixture has been prepared by adding 2000 g of KOH pellets to 2000 mL of DI water. The solution has been heated up after dissolving all of KOH pellets because of exothermic dissolution of KOH in DI water. Then, 800 mL of IPA has been poured on the solution in order to keep the concentration of the KOH solution from evaporation due to heating. Final KOH mixture can be seen on Figure 3.18 Following the preparation of the KOH solution, the wafer has been cleaned by using HF, in order that any oxide grew on the Si surface has been etched in it. Before putting the wafer into the KOH solution, the PR on the wafer is cleaned to prevent clouding in the KOH solution by using acetone, IPA and pressured nitrogen drying, respectively. Finally, the wafer placed into the plexiglass holder to rest in the solution. However, the density of the solution had been increased, the wafer and the holder was floating and this was not foreseen. Fortunately, this problem has been solved by putting additional weight to the holder. In 84 $^{\circ}C$ to have a etch depth of 300 μm the calculated time was approximately 5 hour 33 minutes. However, the etching took more time than expected since the temperature was slightly below 84 $^{\circ}C$ and it was affecting the time in an exponential manner. The wafer kept in the KOH solution about 6 six hours and taken out at the end of the process. In Figure 3.19, the wafer and the holder, just after

being taken from the solution, can be seen.

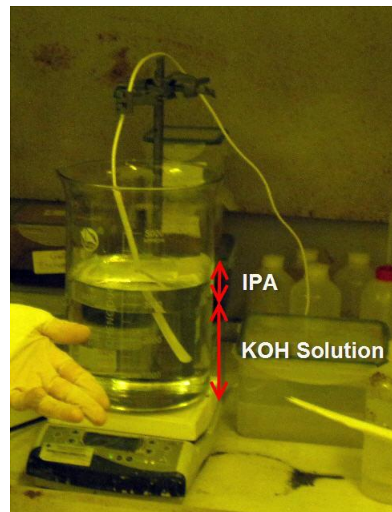

Figure 3.18. The KOH mixture prepared for etching.

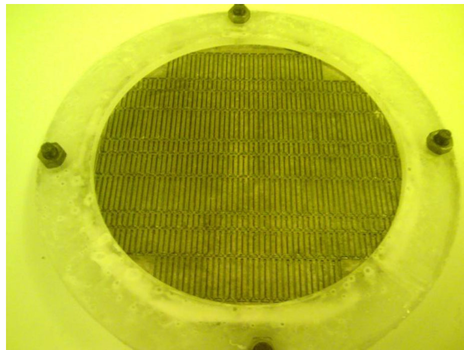

Figure 3.19. The wafer and the plexiglass holder just after the etching process.

3.2.2.6. Removing Cr/Au mask and cleaning the wafers. The wafer has been taken out of the holder and the O-ring. Then, it has been etched in gold etchant and Cr etchant, respectively. After striping the Cr/Au mask, to clean the dust on the mirror surface, wafer has been clean with acetone inside an ultrasonic cleaner. Besides, the wafer broke in the ultrasonic cleaner (luckily) from the die edges. Finally, mirrors were cleaned by using $HSO_4 + H_2O_2$ solution, i.e. piranha etch. In the Figure 3.20 a photograph of the mirrors can be seen after clean.

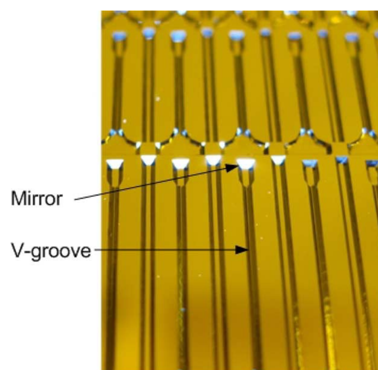

Figure 3.20. Photograph of the fabricated silicon-based fiber optical platform.

3.2.2.7. Al coating. Since low reflectivity of the mirror surface is an important constraint for integration of the micromachined Si platform and the IC die, platforms are coated with 25-nm-thick aluminum film, using a high-vacuum thermal evaporator, which has more reflectivity than Si. Thickness of the evaporated film is monitored by a quartz mass sensor. Since the CMOS chip is covered with an insulating protective film, short-circuit failure of the electronics circuit is not an issue; therefore, Al is deposited all over the platform surface, including the angled walls [11].

3.2.3. Characterization Results

Microfabricated silicon mirror platform for the fiberoptic cable is separately characterized, before it is integrated to the CMOS circuit die. After the optical fiber is placed into the V-groove of the Si platform, reflectivity measurements of the mirrors are done. As the optical power inside the fiber is changed and measured, the reflected power from the silicon mirror surface is measured by the optical power meter. The measurements are done by using two samples to see the variance caused by the processes [11].

The uncoated micromachined Si mirrors had a reflectivity of 33% for the laser input at a wavelength of 650 nm which is also described in [25]. Addition of the 25 nm-thick Al film increased the reflectivity up to 80% and decreased the variance between the mirrors as it is seen in Figure 3.21.

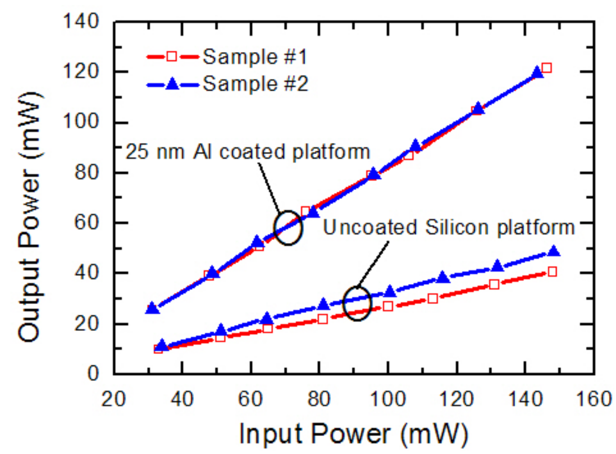

Figure 3.21. Reflectivity measurements on uncoated and Al-coated mirrors.

4. FRONT END PART

This part of the project is a circuit composed of discrete circuit elements and is used to detect the optical signal at IR wavelength. First proposed structure was using a transimpedance amplifier in order to boost up the measured signal at the IR photodiodes.

However, an IR receiver module, with a transimpedance amplifier shown in the Figure 4.1, (Avago HFBR-2316-TZ) has been used with the receiver test circuit shown in Figure 4.2.

The optical sensor module is composed of an InGaAs PIN photodiode that can detect light beams having a wavelength between 1000 nm and 1650 nm, and a low-noise transimpedance amplifier to convert the current value on the PD to a voltage. The PD on the sensor module is used in photoconductive mode, i.e. reverse bias, in order to reduce the effect of junction capacitance.

The measurement result given in Figure 4.3 is obtained by using the test circuit. The experimental setup is made by using the power laser with the driver circuit, the 2nd generation IC, and a LED die (Roithner C155-30), and the optical module test circuit. The light beam coming out of lasers are focused using convex lenses (Edmund Optics f = 75 mm and f = 50 mm with dia. 25 mm) to FC connectors which are placed on XYZ stages. Then, fiber optical cables guiding light beams are coupled on

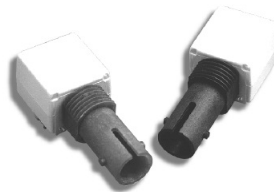

Figure 4.1. Avago HFBR 2316 TZ, optical receiver module.

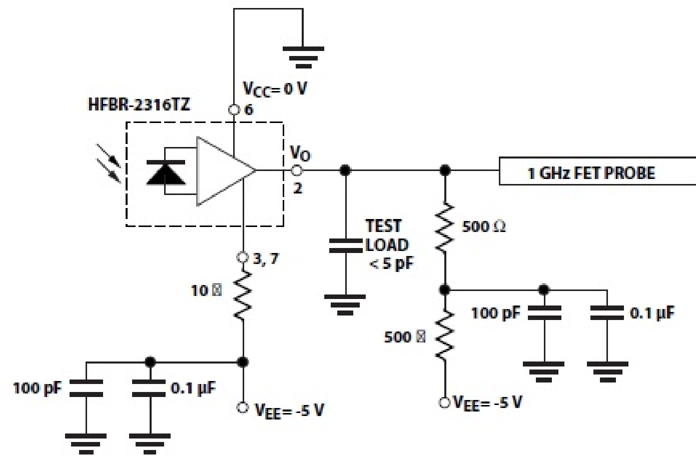

Figure 4.2. optical receiver module test circuit.

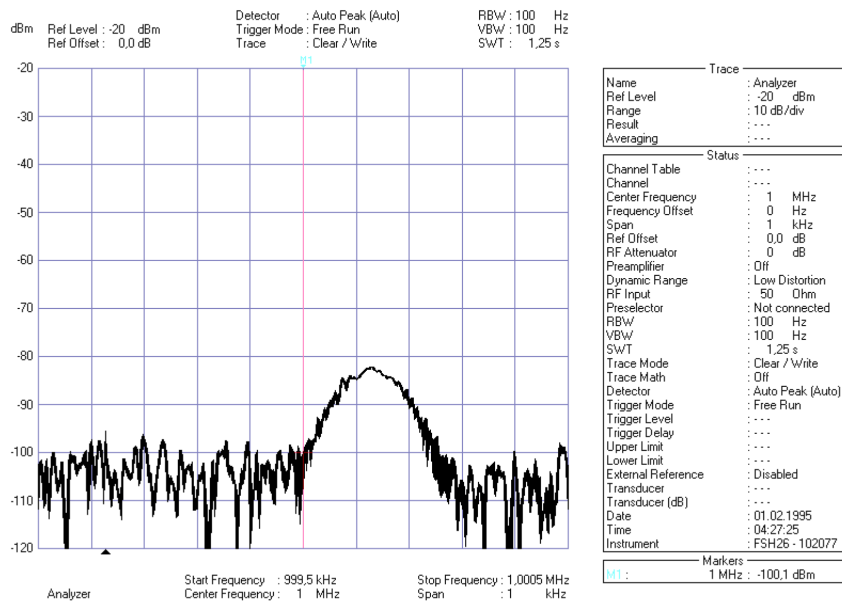

Figure 4.3. Catheter localization signal measured with full optical operation in the MNL.

n-well PD and triple-well PD. The peak optical power of the power laser is adjusted to 50 mW. Finally, the IC operated as shown in Figure 2.17. The LED die has been coupled to a multimode fiber, with a core diameter 62.5 μm. At the other end, an ST connector is connected to the optical receiver module (Avago HFBR-2316-TZ), with its test circuit. The obtained output from the test circuit, in a spectrum analyzer, from the 50 mV analog dimming is given in the Figure 4.3.

A discrete LNA has been designed with a BJT (Infineon BFP540). However, the designed circuit has not been manufactured simply because, another amplifier has been designed and it has been decided to use in the MRI measurements. The designed amplifier has noise figure of 0.4 dB and a voltage gain around 850 V/V.

Nevertheless, the final LED driver supplies a peak current of 2 mA. Since the AC signal on the simulation results(sch1V postl1V) are higher than measured results in Figure 2.17, and the measurement result about the IR LED mentioned in Section 2.3.1 proves that the signal can be directly measured by the mentioned PD die.

5. CONCLUSIONS

5.1. Conclusions

In the thesis work, a high power output laser driver, which is made of discrete components, has been designed and manufactured. The designed laser driver enabled the modulation of power laser for optical switching. The external laser driver can supply currents on the order of amperes. In addition, by using the external laser driver circuit, the power laser can be modulated to give a maximum value of 200 mW optical power.

Characterization and integration of the optoelectronic power supply have been performed. The CMOS photodiodes have an efficiency of 5% of optical-to-electrical conversion efficiency. however, the DC/DC converter cannot supply output current values more than 500 μA. This fact reduces the overall optical-to-electrical conversion efficiency to a level of 1%. However, the low output current problem has been resolved by modulating the power laser and the circuit operation by optical switching. Integration of the CMOS power supply was one of the major obstacles on the project, and this integration has been made in a novel way that triple-well CMOS PDs and DC/DC converter enabled placing all electronic circuits and the power supply on the same IC die.

A supply insensitive LED driver has been made such that there is no longer need for a complex front end circuit. The supply insensitive LED driver is designed to supply a peak current of 2 mA and it consumes 138 μA at 1.5 V supply. The optical transmission path, on the other hand, resolved the planar packaging and integration issues. The reflectivity of the mirrors were increased 80% by using Al coating. Nevertheless, the packaging efficiency were on the order of 33% because the light beam is scattered from the mirror surface and optical misalignment occurred [11].

In the front end part, examined optical sensing schemes are presented. The

sensing circuit can monitor optical signals from the LED die which was driven with the signals as shown in Figure 2.17. However, the AC component of the third LED driver is 2 mA which is much more than the former one.

5.2. Future Work

Up to now, many major obstacles, like integration of power supply and electronics circuits on a single die and optical power harvesting and switching, in the project are resolved. Nevertheless, still some improvements can be done in several ways. First, the design of the DC/DC converter can be altered to supply higher current with a cost of maximum available energy. This can be done by altering the frequency of the ring oscillator and the capacitances on the voltage doubler. This can enable continuous operation of the catheter localization system. Second, instead of a wet etched Si platform, another waveguide can be manufactured using fabrication techniques ,such as DRIE, which allow to fabricate high aspect ratio structures, in order to have more dense packaging. On the other hand, such change brings a high cost of manufacturing. If a higher voltage level on the order of few volts, is desired at the output of the front end, other possible transimpedance amplifier or LNAs can be designed.

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