

WAFER LEVEL PACKAGING OF MEMS DEVICES USING MICROALLOYED
LEAD-FREE SOLDERS

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MICROALLOYED LEAD-FREE SOLDERS**

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ABSTRACT

WAFER LEVEL PACKAGING OF MEMS DEVICES USING MICROALLOYED LEAD-FREE SOLDERS

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The growing popularity of MEMS devices makes packaging methods and processes essential. The need for packaging and lower costs push wafer-level packaging to be more appealing for several applications such as microbolometers, resonators, and micromirrors.

Cu-In-Sn gains attraction among various wafer-level packaging methods. due to its low bonding temperature compared to other transient liquid phase bonding systems. Ternary alloy allows improvement upon the lacking aspects of binary TLP bonding. Bonding at temperatures below 200°C becomes possible with the combination of In-Sn. Reducing the thermal stress and combining with low temperature bonding makes Cu-In-Sn system suitable candidate for CMOS packaging. In this regard, the applicability of the system was studied in this thesis for wafer-level packaging.

Throughout this study, the possibility of Cu-In-Sn bonding has been examined in detail. Bonding methods showed promising results. Sputtered Cu and thermally evaporated Sn and In layers were used on both device and cap wafers. Bonding attempts at 200°C and 250°C yielded inadequate outcomes. Examination after annealing re-

vealed that sluggish diffusion due to incorrect processing parameters were the reason, such as bonding temperature. Process optimizations were performed and the resulting mechanical properties and final melting temperatures of wafers bonded between 200-350°C were investigated in detail. Bonds that have melting temperatures up to and higher than 550°C were obtained with bonding procedures that take place at 250°C and 350°C. It was observed that bonding at higher temperatures yielded higher mechanical strength. An average shear strength of 19.1 MPa was obtained when processed at 350°C and an average shear strength of 8.5°C was obtained with a processing temperature of 250°C.

Keywords: Wafer-level Packaging, Cu-In-Sn ternary alloy, MEMS Packaging, TLP Bonding, SLID Bonding

ÖZ

MİKROALAŞIMLANMIŞ KURŞUNSUZ LEHİMLER KULLANILARAK MEMS CİHAZLARININ PUL SEVİYESİNDE PAKETLENMESİ

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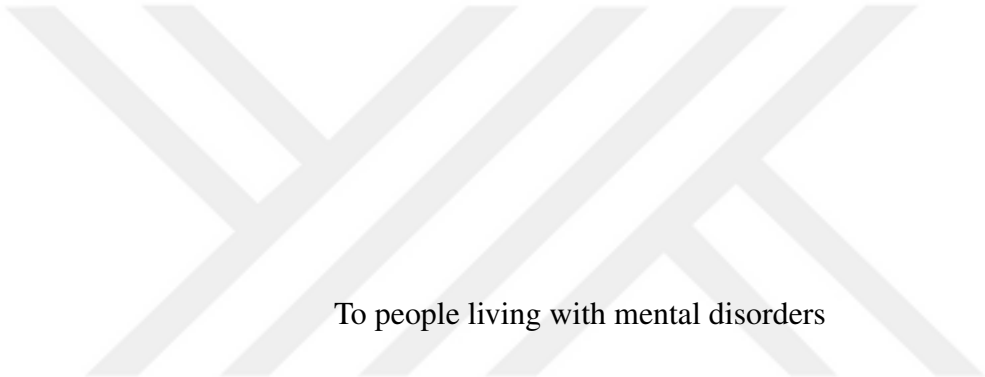
MEMS cihazlarının büyüyen popülaritesi paketleme metotları ve süreçlerini gerekli hale getirmektedir. Paketleme ve masrafların düşürülmesine duyulan ihtiyaç, pul-seviyesi paketleme yöntemlerinin mikrobolometre, rezonatör, ve mikroayna gibi birçok alanda daha ilgi çekici hale gelmesine sebep olmakta.

Cu-In-Sn alaşımı, TLP kullanarak yapılan pul-seviyesi paketleme metotları içerisinde düşük bağlama sıcaklığı ile öne çıkan bir sistemdir. Üçlü alaşım sistemi yüksek bağlama sıcaklığı ve boşluk oluşumu gibi ikili alaşım problemlerini çözüm sunmaktadır. In-Sn ötektik kombinasyonu ile 200°C derece altında bağlama mümkün hale gelmektedir. Termal streslerin azaltılması ve düşük sıcaklıkta bağlama yapılabilmesi Cu-In-Sn alaşımının CMOS paketlenmesi için aday bir sistem yapmaktadır. Bu bağlamda Cu-In-Sn alaşımının pul-seviyesi paketleme için uygulanabilirliği değerlendirilmiştir.

Bu çalışmada Cu-In-Sn bağlama sistemi olarak detaylı bir şekilde incelenmiştir. Bağlama yöntemi başarılı sonuçlar vermiştir. Bakır saçtırma, kalay ve indiyum termal

buharlaştırma yöntemi ile hem cihaz hem de kapak diskleri kaplanmıştır. 200°C ve 250°C’de gerçekleştirilen bağlamalar yetersiz sonuçlar göstermiştir. Isıl işlem sonrası gerçekleştirilen incelemelerde sıcaklık gibi doğru olmayan süreç parametrelerinin yavaş difüzyon mekanizmasını tetiklediği tespit edilmiştir. Süreç geliştirmelerinden sonra 200 ve 350°C arasında deneyler tekrar edilmiş olup, mekanik özellikler ve tekrar erime sıcaklıkları detaylı bir şekilde incelenmiştir. Erime sıcaklığı 550°C’tan yüksek olan paketler 250 ve 350°C’ta yapılan paketlemeler sonucu elde edilmiştir. Yükselen bağlama sıcaklığı ile mekanik mukavemeti daha yüksek paketler elde edildiği gözlenmiştir. 250°C’de gerçekleştirilen bağlama sonucu ortalama kesme dayancı 8.5 MPa, 350°C’de ise ortalama kesme dayancı 19.1 MPa olarak tespit edilmiştir.

Anahtar Kelimeler: Pul-seviyesi Paketleme, Cu-In-Sn alaşımı, MEMS Paketlenmesi, TLP Bağlama, SLID Bağlama



To people living with mental disorders

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TABLE OF CONTENTS

ABSTRACT	v
ÖZ	vii
ACKNOWLEDGMENTS	x
TABLE OF CONTENTS	xi
LIST OF TABLES	xiv
LIST OF FIGURES	xv
CHAPTERS	
1 INTRODUCTION	1
1.1 Overview	1
1.2 MEMS Packaging	3
1.2.1 Wafer-Level Packaging Methods	6
1.2.1.1 Fusion Bonding	7
1.2.1.2 Anodic Bonding	8
1.2.1.3 Adhesive Bonding	8
1.2.1.4 Glass Frit Bonding	9
1.2.1.5 Thermocompression Bonding	11
1.2.1.6 Eutectic and TLP Bonding	11
2 LITERATURE REVIEW	15

2.1	Binary TLP Bonding	15
2.1.1	Cu-Sn TLP	15
2.1.2	Cu-In TLP	23
2.2	Ternary TLP Bonding	25
2.2.1	Au-In-Bi TLP	25
2.2.2	Cu-In-Sn Bonding	28
3	EXPERIMENTAL PROCEDURE	31
3.1	Fabrication Methods	31
3.1.1	Lithography	31
3.1.2	Metallisation	33
3.1.3	Liftoff	38
3.2	Process Flow	39
3.3	Bonding Methods	41
3.3.1	Unpatterned Wafers	42
3.3.2	Patterned Wafers	44
3.4	Characterisation Methods	48
3.4.1	Scanning Acoustic Microscopy	48
3.4.2	Shear Testing	49
3.5	Scanning Electron Microscopy	51
3.6	Differential Scanning Calorimetry	51
4	RESULTS & DISCUSSION	53
4.1	Unpatterned Wafer Bonding Test	53
4.1.1	Bonding at 300°C	53

4.1.2	Bonding at 250°C	56
4.1.3	Annealing at 350°C	60
4.2	Patterned Wafer Bonding Tests	64
4.2.1	Bonded at 200°C	64
4.2.2	Bonded at 350°C	65
4.2.3	Bonded at 250°C	70
5	CONCLUSION & FUTURE WORK	77
	REFERENCES	79



LIST OF TABLES

TABLES

Table 1.1	Table of common eutectic bonding pairs and their process temperatures.	11
Table 1.2	Table of common TLP bonding pairs and their process temperatures.	13
Table 3.1	Table of elements and weight percentages of elements used in patterned bondings.	45
Table 4.1		61
Table 4.2	Table of elements and weight percentages of elements in Figure 4.20	73
Table 4.3	Table of shear strengths of the tested samples according to their processing temperatures.	74

LIST OF FIGURES

FIGURES

Figure 1.1	SEM images (a) MEMS accelerometer; (b) microbolometer. . . .	2
Figure 1.2	Schematic diagram illustrating positive and negative photore- sists in lithography.	3
Figure 1.3	MEMS market size forecast.	3
Figure 1.4	(a) schematic view of a single suspended bolometer pixel with 50 μ m pitch size, (b) effect of pressure on noise equivalent temperature difference.	5
Figure 1.5	Q-factor values as a function of the air pressure (datapoints) for the three investigated configurations.	5
Figure 1.6	MEMS cost distribution for wafer-level packaging(left); die- level ceramic/metal package (right).	7
Figure 1.7	Mechanism of anodic bonding.	8
Figure 1.8	Examples of localized polymer adhesive wafer bonding.	9
Figure 1.9	Stages of glass frit paste during bonding process.	9
Figure 1.10	Fabrication steps of a MEMS resonator alongside a cap wafer to be bonded via glass frit.	10
Figure 1.11	Schematic binary eutectic phase diagram.	12
Figure 1.12	Gold-Indium binary phase diagram.	14

Figure 2.1	Phase Diagram of Cu-Sn.	16
Figure 2.2	Schematics of three scenarios on the effect of critical thickness. .	17
Figure 2.3	SEM image of cross-sections of samples bonded at 340°C a) for 3 minutes b) for 3 hours.	17
Figure 2.4	Schematic representation of Kirkendall a) void formation and b) progression.	18
Figure 2.5	Photographs of cross sections through a bonded frame (full top side metal frame, railed bottom frame) after annealing at 350°C and 400°C respectively.	19
Figure 2.6	Schematic bonding profile indicating temperature and pressure times.	20
Figure 2.7	SEM images of bond interface with desired Cu/Cu ₃ Sn/Cu struc- ture(left) and squeezed out Cu ₆ Sn ₅	20
Figure 2.8	The bond line after bonding as aimed it consists of Cu/Cu ₃ Sn/Cu.	21
Figure 2.9	SEM image of the fractured surface with different fracture modes.	22
Figure 2.10	Copper-Indium phase diagram.	24
Figure 2.11	Schematic representation of metallization and thicknesses for Cu-In bonding	25
Figure 2.12	SEM images of the cross-sections: a) as bonded b) after HTS testing.	25
Figure 2.13	Phase diagram of Bismuth and Indium.	26
Figure 2.14	SEM image of the bond line taken from edge and centre showing different phases after bonding at 90°C.	27
Figure 2.15	SEM image of the bond line taken from edge and centre showing different phases after bonding at 110°C.	28

Figure 2.16	Sn-In phase diagram.	29
Figure 2.17	Variation of copper consumption depending on the $\text{Sn}_x\text{In}_{100-x}$ concentration.	30
Figure 2.18	Effect of bonding temperature on voiding. a) bonded for 5 minutes, b) bonded for 20 minutes.	30
Figure 2.19	Multilayer material structure on cap wafer and base wafer.	30
Figure 3.1	Schematic comparison of positive and negative photoresists after development.	32
Figure 3.2	SUSS MicroTec Spinner and Torrey Pines hotplate.	32
Figure 3.3	EVG6200 contact aligner.	33
Figure 3.4	Schematic representation of sputtering chamber and process.	34
Figure 3.5	AJA DC sputter system.	35
Figure 3.6	Schematic representation of the cross-section after sputtering.	35
Figure 3.7	Schematic representation of evaporation chamber and process.	36
Figure 3.8	Planets used in thermal evaporation for uniformity.	37
Figure 3.9	Varian 3119 thermal evaporator.	37
Figure 3.10	Nanovak NVTH-350 thermal evaporator and inside view of the chamber.	38
Figure 3.12	Schematic of the microfabrication flow.	40
Figure 3.13	EVG 520IS wafer bonder.	41
Figure 3.14	Schematic of the bonding chuck used in the experiments. Flags are in violet, and the clamps are in green.	42
Figure 3.15	Temperature, time, and pressure used for the initial testing	43

Figure 3.16	Temperature, time, and pressure used for the initial testing	44
Figure 3.17	Layout of the patterned wafer, coloured parts indicated metal- lization.	45
Figure 3.18	Bonding profile of bonding at 200°C.	46
Figure 3.19	Bonding profile of bonding at 350°C.	46
Figure 3.20	Alignment procedure of marks of the mask and wafer within and against each other.	47
Figure 3.21	Examples of SAM inspections. The change in the wave a) going through the bond rings, b) going through the cavity.	48
Figure 3.22	PVA TePla 301HD Scanning acoustic microscope.	49
Figure 3.23	Dage Nordson 4000 Bond Tester.	50
Figure 3.24	View of the shear test of the package during shear testing.	50
Figure 3.25	Hitachi Regulus 8230 SEM	51
Figure 3.26	Perkin Elmer Diamond Differential Scanning Calorimetry (DSC).	52
Figure 4.1	SAM image of unpatterned wafer pair after bonding at 300°C	54
Figure 4.2	Shear strength results after bonding of unpatterned wafers at 300°C for 1 hour.	55
Figure 4.3	DSC results of bonding performed at 300°C	56
Figure 4.4	SAM image of unpatterned wafer pair after bonding at 250°C	57
Figure 4.5	Shear strength results after bonding of unpatterned wafers at 250°C.	58
Figure 4.6	SEM image of the bond and EDS line for the sample as bonded at 250°C(left), compositional analysis(right).	59
Figure 4.7	DSC analysis of samples bonded at 250°C.	60

Figure 4.8	Shear test results after annealing at 350°C	62
Figure 4.9	SEM image of the bond after annealing at 350°C.	63
Figure 4.10	Three constituting elements and their colour maps from EDS. . .	63
Figure 4.11	SAM image of bonding performed at 200°C.	65
Figure 4.12	SAM image of bonding performed at 350°C.	66
Figure 4.13	Shear strength results after bonding of patterned wafers at 350°C for 1 hour.	67
Figure 4.14	DSC analysis after bonding at 350°C.	68
Figure 4.15	Second DSC analysis after bonding at 350 °C.	69
Figure 4.16	Microscope image of the fracture surface after shear testing. Glass substrate (left) and silicon substrate (right).	69
Figure 4.17	SAM image of bonding performed at 250°C with thicker met- allisation.	70
Figure 4.18	Close up of the SAM image of dies near the right alignment mark.	71
Figure 4.19	Shear strength results after bonding of patterned wafers at 250°C for 1 hour.	72
Figure 4.20	SEM image of the fracture surface.	73
Figure 4.21	DSC analysis of patterned wafer after bonding at 250 °C.	75



CHAPTER 1

INTRODUCTION

1.1 Overview

Microelectromechanical systems, also known as MEMS, microsystem technology, or micromachines, are devices fabricated using micromachining methods instead of conventional ones. The term MEMS was first used by R. Howe in 1989. They may be considered as miniaturized machines that interact with the physical world. That interaction could be limited to sensing, as in a sensor, or it may actuate a change, as in actuators. MEMS sensors and actuators has become widespread in the industry and consumer products[1].

As the name implies, MEMS devices combine electronics, usually ROIC(Read Out Integrated Circuit) or ASIC(Application Specific Integrated Circuit), with mechanical components such as moving bodies or suspended structures in a single device smaller than 100 μm . The smaller sizes allow MEMS devices to be integrated heavily into personal and professional areas. A wide variety of mems devices are present in laptops, smartphones, wearable tech products, and cars[2, 3]. Specific examples of these devices include accelerometers, gyroscopes, MEMS microphones, micromirrors, and microbolometers. Figure 1.1 below shows a MEMS accelerometer and a microbolometer where both designs employ suspended parts to achieve different goals[4, 5].

Microfabrication methods are employed to fabricate MEMS structures, similar to the semiconductor industry. A batch-process approach is taken for the fabrication in which thin-film coating, lithography and pattern transfer steps are taken. Thin-film coatings include conductors and insulators, depending on the application. Physi-

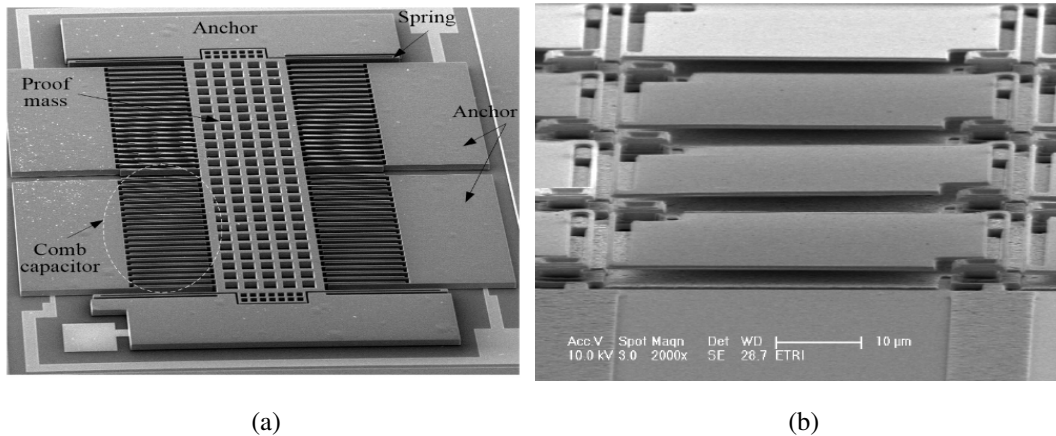


Figure 1.1: SEM images (a) MEMS accelerometer; (b) microbolometer.

cal vapour deposition(PVD), chemical vapour deposition(CVD), and electroplating methods are extensively used to deposit an array of films. Silicon and its nitride and oxide forms, Si_xN_y and Si_xO_y are the most common insulators coated with CVD methods[6]. Most metals used in the MEMS industry, such as gold, have high melting temperatures and are coated with PVD methods such as sputtering and evaporation[7].

Lithography and etching steps are the most common for microfabrication after a layer is deposited. Lithography is a crucial process for obtaining desired designs in which a photoresist material is spun or sprayed over the wafer, which later will be exposed to UV light through a mask or a reticle resulting in a chemical change in the PR material. Figure 1.2 shows a typical lithography process in which the image on the mask/reticle will be transferred to the wafer for further processing[8]. In a standard microfabrication flow, coating and lithography are followed by etching.

Two different types of etching can be employed, namely, wet and dry. In wet etching, a wafer is submerged in a chemical etchant that is selective to the specific layer so that other layers are not damaged. However, dimension control in wet etching is limited. In dry etching, plasma technologies are used to bombard the surface with ions in a process called reactive-ion etching or RIE for short. Anisotropic or isotropic etching could be achieved with greater dimensional control surface quality.

As MEMS technology gains more popularity and attraction, the development of micromachining methods continues. Improvement in device compactness and cost con-

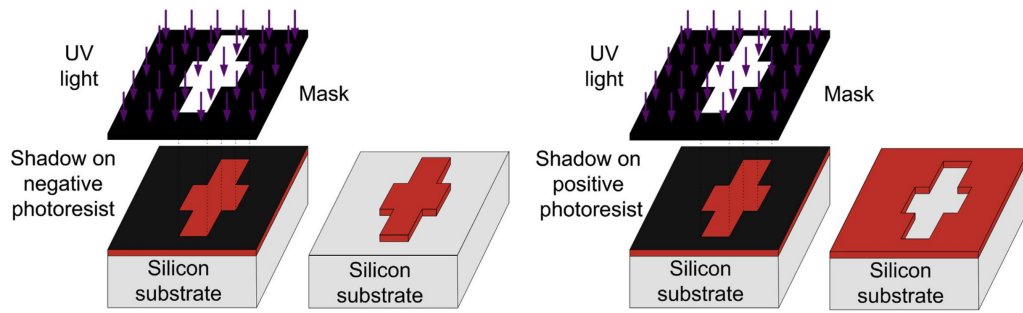


Figure 1.2: Schematic diagram illustrating positive and negative photoresists in lithography.

tinues, such that MEMS devices find their place in everyday products even more than before. This trend is proved by the increasing market share of MEMS devices as shown in Figure 1.3[9]. In less than a decade, market share doubled from approximately \$11 bn to \$25 bn, showing a steady growth over the years with different devices.

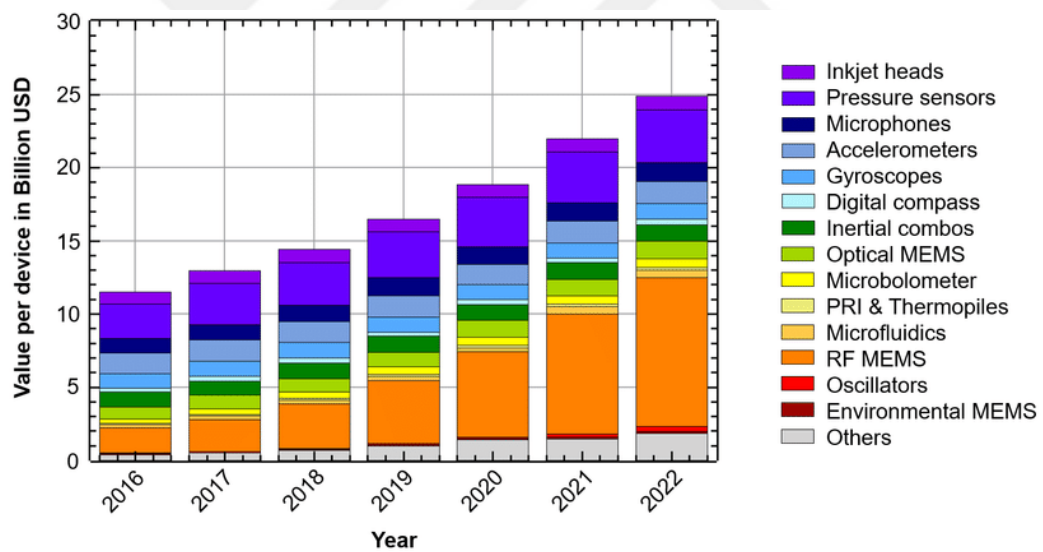


Figure 1.3: MEMS market size forecast.

1.2 MEMS Packaging

MEMS devices, with their decreasing sizes and complex delicate structures, must be encapsulated. This encapsulation is often called packaging and makes up for a

significant amount of the device's cost. As microfabrication methods improve and chips get smaller, the cost decreases. However, ever-shrinking package sizes have a negative effect on costs if traditional methods are used.

The packaging of devices serves several purposes. MEMS devices must be able to interact with the world to some extent. The first of these interactions is the electrical connections required by most devices, also known as fan-out. Therefore, a package should be versatile enough where vertical or lateral fan-out is possible but other factors do not affect the device. The importance of MEMS packaging and protection from potential external damage and degradation originates from many MEMS structures performing optimally under certain conditions. Vacuum, hermeticity, conduction, and insulation are some examples of situations that a package may need. Since the devices are designed considering reliability and performance, the same criteria should be applied to the package design and application where it can compensate for unexpected conditions and still provide the best possible conditions.

In the case of microbolometers, a film with a negative temperature coefficient of resistance, such as YBCO (Yttrium barium copper oxide) or VO_x , is used for thermal imaging. Infrared radiation (IR) from any heat source changes the temperature of the thin film such that under constant current or voltage conditions, any change could be read by an ROIC as shown in Figure 1.4[10]. Suspended pixels with low thermal conductance prevent heat loss due to conduction. However, convection should be reduced to further increase performance as air molecules within the package will lead to heat dissipation.

Another device that requires vacuum conditions for optimum performance is micromirrors. However, their vacuum needs stem from other factors, as they can be considered small oscillators. During the oscillations, the presence of air leads to damping, which reduces the performance and image quality. Higher input powers become necessary in the case of air-damping to obtain a steady oscillation. Packaging in a vacuum environment means that energy loss will be reduced in every cycle, increasing the efficiency severalfold. Getter materials are used to ensure that the package will retain its vacuum environment. Getter materials are generally metals that can form oxides quickly, they are heated to increase oxidation further and as a result, they will

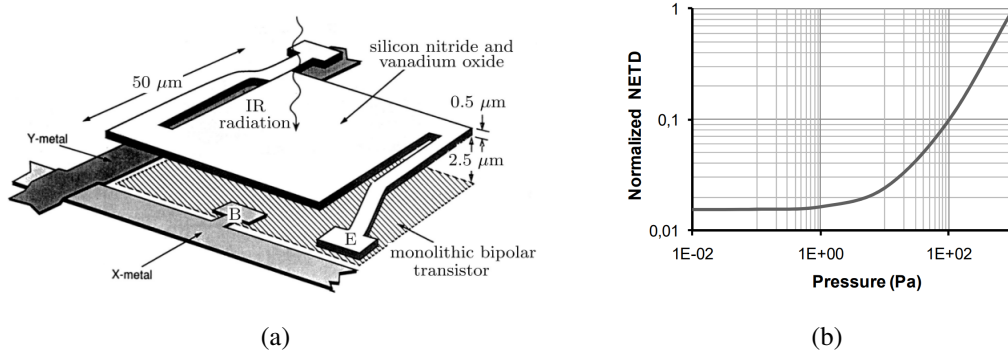


Figure 1.4: (a) schematic view of a single suspended bolometer pixel with $50\ \mu\text{m}$ pitch size, (b) effect of pressure on noise equivalent temperature difference.

rid the package of the remaining gaseous species[11, 12]. In Figure 1.5 below, the effect of pressure on a device is shown[13].

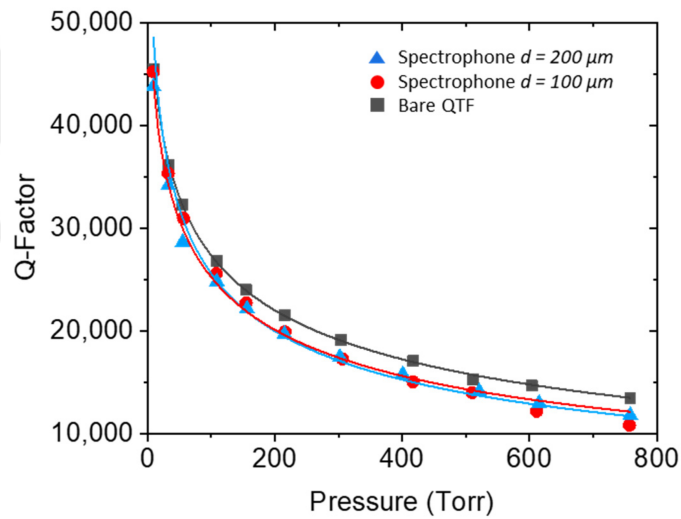


Figure 1.5: Q-factor values as a function of the air pressure (datapoints) for the three investigated configurations.

The increasing market share and popularity of MEMS sensors would not have been possible if not for improved packaging technologies. Wafer-level packaging methods have allowed pressure sensors, accelerometers, and gyros to become widespread as their working conditions require hermeticity to reach optimum performance. A challenge in bonding technology is that the footprint or size of packages or the MEMS components inside are continuously getting smaller, and being able to reduce pack-

aging size further puts a restraint on the process. Packaging technology should keep up with the miniaturization of MEMS sensors to increase profit and throughput.

1.2.1 Wafer-Level Packaging Methods

Wafer-level packaging utilizes a cavity opening on a wafer beside the device wafer, also referred to as a cap wafer. The cap wafer specifications can be decided depending on the application, such that glass or silicon could be chosen. Necessary bonding operations are executed on either one of the wafers or on both the device and cap wafer. The cap and device wafer are bonded prior to any dicing procedure after the completion of the device wafer. Any related process should be considered beforehand to prevent issues. The cap and device wafers are brought together in different conditions to achieve bonding, utilizing either an additional layer for bonding or using the base layer of the cap and devices.

Another aspect that helps reduce costs is that in traditional processing, chip singulation takes place before packaging, however; for specific MEMS structures, such as membranes or suspended parts, there exists a risk of damaging the structure during the dicing process. Two approaches can be taken to prevent this issue. First, laser dicing can be considered instead of using the industry standard of water jet or blade cutting for dicing. Laser dicing offers better precision and safety, but the higher cost may only be necessary for some applications. The second option for preserving delicate structures is employing a wafer bonding method before the dicing process to ensure that there will be no mechanical damage if the bond and package can withstand leakage issues. Different bonding methods are readily available and may be chosen depending on the application area. These methods include anodic bonding, direct, glass frit, metal thermo-compression, eutectic, and transient liquid phase (TLP) bonding.

The importance of wafer bonding or packaging stems from the fact that the cost of a single device in production and packaging is nearly equal. Hence, cheap packaging methods have become crucial in the industry as developing such bonding methods is also costly and takes time. A comparison of the divide in packaging costs for chip-level and wafer-level packaging is in Figure 1.6[3]. In more advanced structures, the bonding can also be utilized to improve or generate new three-dimensional de-

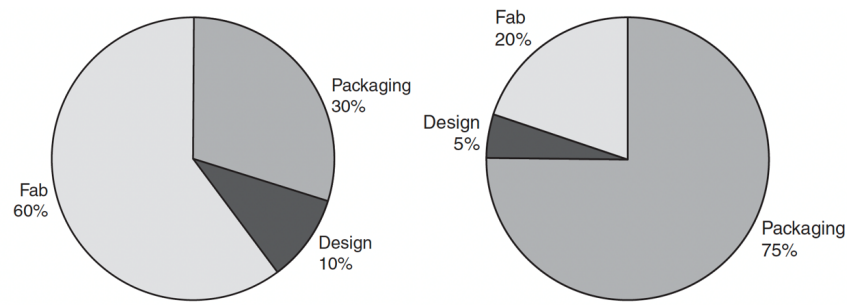


Figure 1.6: MEMS cost distribution for wafer-level packaging(left); die-level ceramic/metal package (right).

signs, depending on the bonding material and method. Adapting packaging methods for miniaturization through wafer-level packaging methods is easier since packaging steps could be integrated into the microfabrication steps, decreasing the time required to package chips one at a time.

1.2.1.1 Fusion Bonding

Fusion bonding makes use of the substrate itself for bonding application, and an additional bonding layer is not required for direct bonding. The Si-Si or SiO₂-SiO₂ fusion is employed for bonding. The requirements for direct bonding are pretty demanding; a bonding temperature of around 1000°C is necessary for fusion to take place; Moreover, pristine surfaces in terms of both topography and cleanliness are a must since any contaminants/defects on the surface, such as organics and metals can affect bonding quality [14, 15]. Bonding starts where a tip touches, and then it radiates through the wafers, similar to a wave. Surface activation of the pairs to prepare the surfaces before the bonding operation allows for decreased bonding temperatures in the range of 300-400°C[3]. Following the aforementioned necessary steps, the wafers are brought into contact, and pressure is applied. As the system heats up while the contact is still present, the pair of wafers bond to each other.[16].

1.2.1.2 Anodic Bonding

Anodic bonding is another bonding method in which there are no additional layers for bonding. It requires materials that differ in conductivity such that one conducts electrons and the other conducts ions. The most common combination for anodic bonding is silicon wafers to Na-containing glass wafers, especially Corning 7740[17]. The reliability of anodic bonding has been proven in terms of wafer-level bonding, and it is extensively used in microelectromechanical systems(MEMS) as a method[18]. The bonding mechanism requires temperatures around 300 — 450°C. Na^+ ions present in the borosilicate glass move towards the negative side when voltage is applied as shown in Figure 1.7 and a strong covalent bond is formed between silicon and oxygen[19, 20]. However, due to the requirement that the pair has to be silicon and glass as well as bonding temperatures that may exceed 400°C, anodic bonding has its limitations as a bonding method.

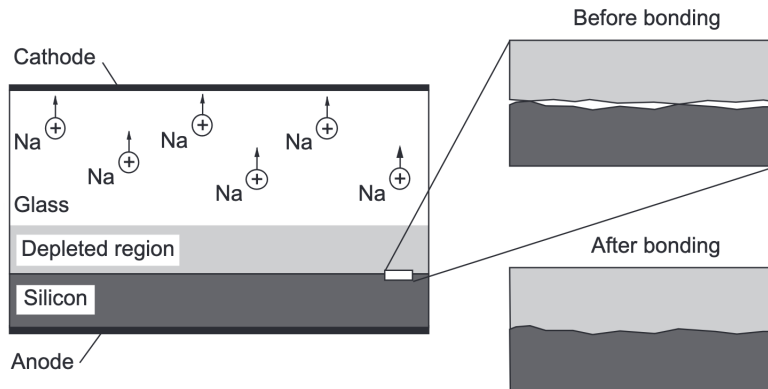


Figure 1.7: Mechanism of anodic bonding.

1.2.1.3 Adhesive Bonding

Adhesive bonding is a technique that involves using an intermediate layer as an adhesive for bonding. The adhesive options vary, but polymers such as Benzocyclobutene(BCB), polyimides, and UV epoxies are mainly used. In a standard bonding process, the adhesive is applied to wafers only, caps, or both. Different applications of adhesive bonding are seen in Figure 1.8[21]. After the wafers are brought together, pressure is applied to keep them together, and additional processes such as heating or

UV exposure are used to transform the adhesive into a solid state. Adhesive bonding is available for different wafers without special surface conditioning[22]. While adhesive bonding may seem simple, it can become more complex when introducing an additional layer with a different structure. This is due to differences in coefficients of thermal expansion (CTE), which can decrease the reliability of the bond over time as the devices are used. Another downside of adhesive bonding is that the bonds obtained are not hermetic.

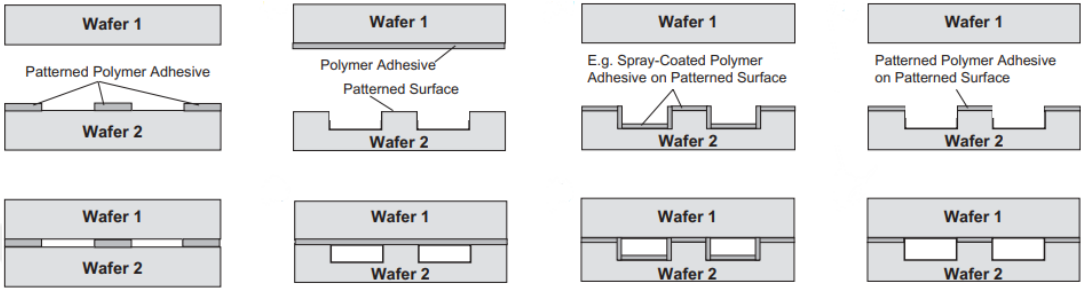


Figure 1.8: Examples of localized polymer adhesive wafer bonding.

1.2.1.4 Glass Frit Bonding

Glass frit bonding provides a bonding method for temperatures below 450°C to a wide range of systems. An intermediate layer is employed for bonding, compatible with most surfaces used in the MEMS industry. The advantage originates from the fact that glass formed provides hermeticity and high yield after bonding. Only a cap wafer could form a strong bond without additional processing of the device wafer. Glass frit is a powder mixture that must be screen printed onto the cap wafer. The screen printing process allows for deep cavities to be formed without the traditional microfabrication methods[23, 24].

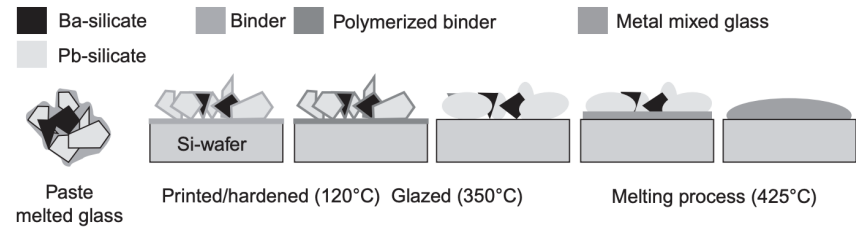


Figure 1.9: Stages of glass frit paste during bonding process.

During the bonding process, the paste wets the surface as its viscosity decreases with increasing temperatures. Wetting the surface with proper paste selection makes glass frit bonding ideal for bonding rough surfaces. After wetting is complete during cooling, a strong bond is obtained, the mechanism of which is shown in Figure 1.9[24]. Pressure during bonding so the paste can spread over the interfaces to properly wet the required areas. The obtained bond is highly reliable, robust, electrically insulating, and hermetic. Process flow for a resonator to be bonded with glass frit is shown in Figure 1.9[25]. Despite these upsides, glass frit bonding can not be used for sensitive and small packages as screen printing alignment limits the accuracy of the bond rings. Another important limiting factor is the lead content in most of the paste materials, posing environmental and safety issues.

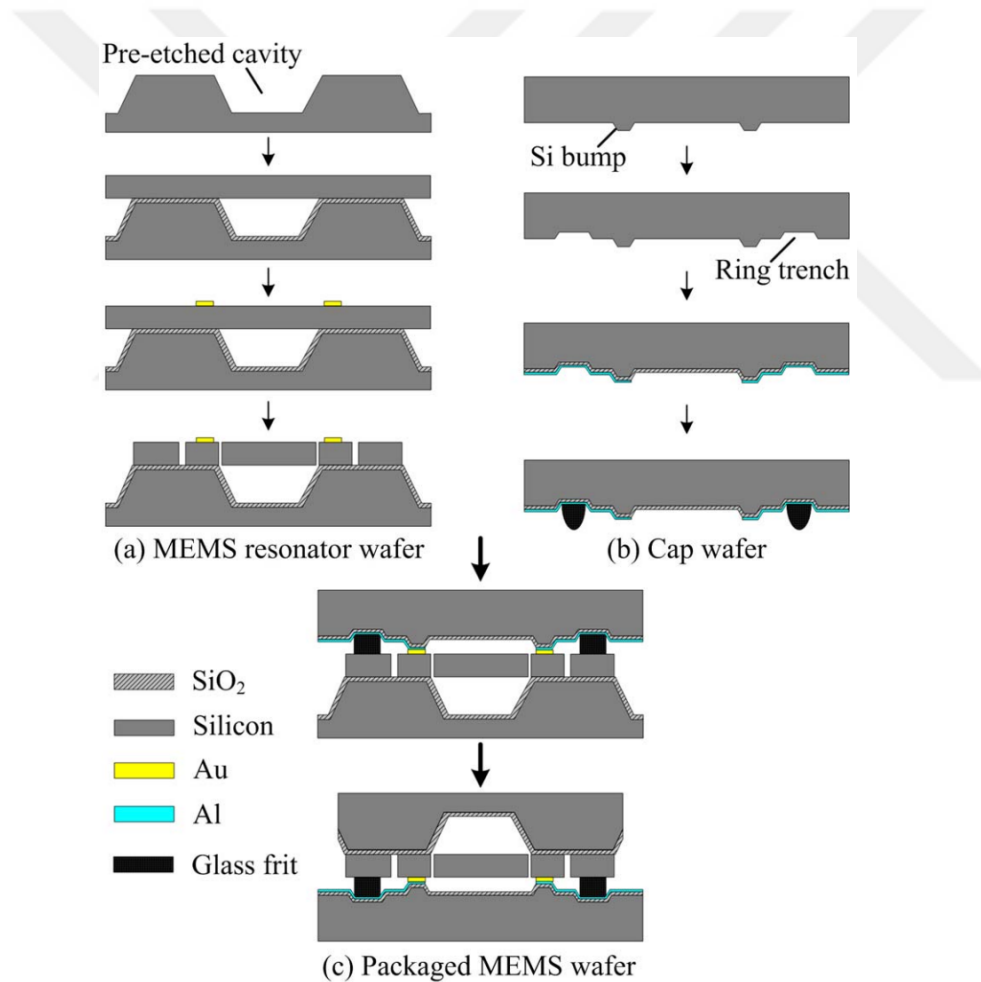


Figure 1.10: Fabrication steps of a MEMS resonator alongside a cap wafer to be bonded via glass frit.

1.2.1.5 Thermocompression Bonding

Thermocompression bonding utilizes a method similar to solid-state welding in which two layers of the same metal are brought together under high temperatures and pressures to form a bond. The most common metals for thermocompression are Aluminum, Copper, and Gold [26, 27]. The bond attained after thermocompression is a metallic bond; high pressures in the range of 10-15 MPa are required to bring the atoms into contact to initiate bonding. Thermocompression bonding's advantage stems from the fact that the bonds obtained are mostly hermetic, and their reliability over other methods, such as glass frit bonding, is exponentially higher in terms of lifetime[28].

1.2.1.6 Eutectic and TLP Bonding

Eutectic and TLP bonding are methods in which a solder-like material, either in bulk form or thin film form, is used to create a liquid to bond the cap and device wafers to each other under pressure and heating. Heating to a specific temperature ensures that liquid formation and applying pressure to both wafers during bonding mixes the metals and spreads them over the surface. The choice of metals determines the possible bonding temperature for a system. Binary or ternary systems are employed to achieve bonding. Common eutectic systems with their bonding temperatures are shown in Table 1.1[29].

Table 1.1: Table of common eutectic bonding pairs and their process temperatures.

Metal Pair	Bonding Temperature(°C)
Au - Si	400
Au - Ge	400
Al - Ge	425
Au - Sn	300

Eutectic bonding, as implied by the name, makes use of the eutectic point of alloys. In eutectic composition and at eutectic temperature, the metal is in liquid form below the melting temperature of both metals. This point is used such that either a certain

composition of thin film or a layered metal stack can be made to be the bond material. If a thin film of eutectic composition is used by co-sputtering, reaching the eutectic temperature causes melting, as in soldering. In the case of separate layers of metals, as temperature increases and with the help of pressure, metal species start to diffuse into each other. At surface points that reach eutectic composition, liquid formation starts, and eventually, the whole interface turns into liquid. During the cooling of the wafers, a bond is formed as the liquid solidifies below the eutectic point.

In Figure 1.11, the phase diagram of an arbitrary eutectic A-B binary alloy is shown. The red line indicates the eutectic composition of the alloy. A mixture of A and B at a given composition will melt at T_E . If separate layers are used, the diffusion between A and B will occur as indicated with red arrows on the phase diagram. After a certain amount of time, the solution will melt at certain locations when it reaches the eutectic composition. However, phase diagrams of such systems are generated for bulk materials and the eutectic composition for thin films may differ from data in the literature.

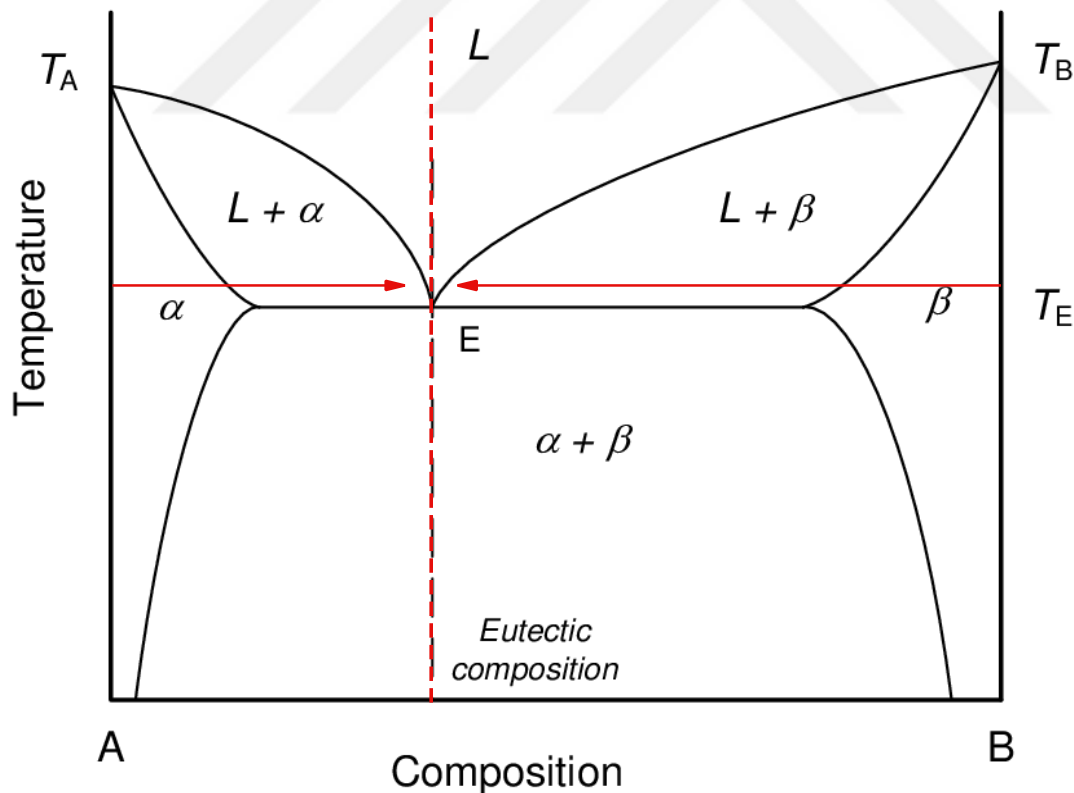


Figure 1.11: Schematic binary eutectic phase diagram.

Transient liquid phase (TLP) bonding is a bonding method in which the employed metals have a large difference in their melting temperatures, such as gold at 1064°C and tin at 231.9°C. The low melting point metal can be classified as the interlayer metal, and the higher melting point metal is considered the parent material. The advantage of this method arises from the fact that the bonding takes place at lower temperatures compared to other bonding variations, and the obtained bond has a melting temperature much higher than the bonding temperature. Table 1.2 below shows the bonding and remelting temperatures of systems that can be bonded with the TLP method[30].

Table 1.2: Table of common TLP bonding pairs and their process temperatures.

Material System	Process Time and Temperature	Remelt Temperature
Copper – Indium	4 mins at 180°C	>307°C
Gold – Indium	0.5 mins at 200°C	>495°C
Silver – Indium	120 mins at 175°C	>880°C
Copper – Tin	4 mins at 280°C	>415°C
Gold – Tin	15 mins at 260°C	>278°C
Silver – Tin	60 mins at 250°C	>600°C
Nickel – Tin	6 mins at 300°C	>400°C

For TLP bonding to be viable, the two metals must form certain intermetallic compounds (IMCs) according to their phase diagram. The similarity of TLP bonding to eutectic bonding lies in the fact that during the bonding process, liquid formation occurs, which is implied by the name TLP. However, in TLP bonding, only the melting of the interlayer occurs while the high melting point metal remains solid. The bonding occurs through the interdiffusion of the liquid phase into the solid atoms at the interface between solid and liquid. In Figure 1.12 below, the mechanism of TLP is indicated through a phase diagram of Au-In[31]. As evident from the phase diagram, the gold-indium system contains two different intermetallics, AuIn and AuIn₂, respectively. The red arrows indicate the diffusion of In atoms into the Au after the melting of indium takes place while pressure is applied. The first IMC formed is the AuIn₂. Given enough indium in the system, the diffusion will continue and AuIn

phase will also form. Depending on the process conditions, AuIn and AuIn₂ may be present in the bond region.

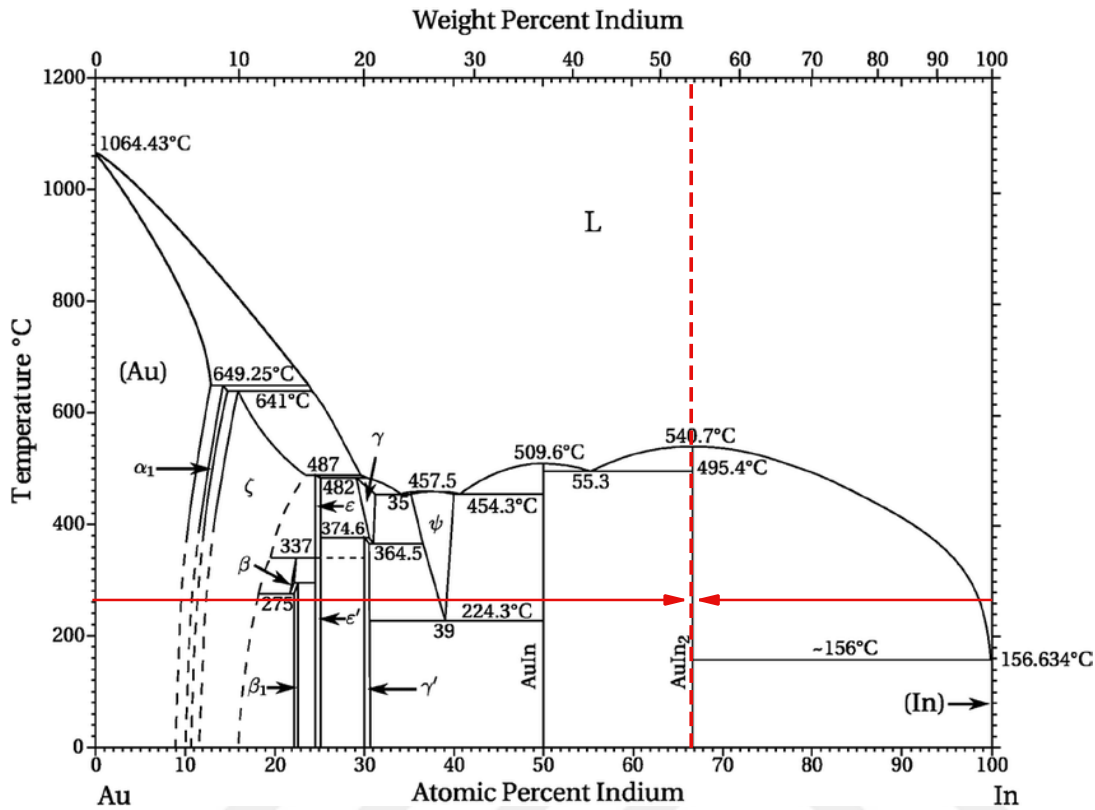


Figure 1.12: Gold-Indium binary phase diagram.

As appealing as TLP bonding sounds, there are obvious downsides that must be considered for a proper bond. The intermetallic compounds (IMCs) mentioned are closer to ceramics in their nature, meaning they are brittle. The increased brittleness in the bond may lower the reliability of the bond. A counter for this brittleness is the ductility of the high melting temperature metal since the IMCs are sandwiched in between. Another risk during TLP bonding is that the low melting temperature metal may be depleted too quickly before any melting occurs, given that the solid-state diffusion between the species is sufficient. This issue can be eliminated by designing the stack structure so that there will always be enough interlayer material to form liquid during heating. This is called the critical interlayer thickness[32].

CHAPTER 2

LITERATURE REVIEW

In this section, the literature review will be conducted regarding binary and ternary systems to act as the basis of wafer-level Cu-Sn-In TLP bonding. The binary systems chosen are Cu-Sn and Cu-In. Ternary systems are rare in the literature; therefore Au-In-Bi and Cu-Sn-In system is reviewed.

2.1 Binary TLP Bonding

In this section, binary systems of copper will be explained for the purposes of TLP bonding

2.1.1 Cu-Sn TLP

The phase diagram of the copper-tin system, which is used readily in the packaging industry, is shown in Figure 2.1 below[33]. As can be seen from the diagram, the phase transformations in the system are quite complex as there are many phases present. Two target phases for TLP bonding are present in the Cu-Sn system, and they are η -Cu₆Sn₅ and ϵ -Cu₃Sn with 47 at% Sn and 33 at% Sn, respectively. Diffusion of these species into each other occurs at every temperature, but the diffusion rate increases with increasing temperature. ϵ has a melting point of 676°C and η has a melting point of 415°C[34].

From Figure 2.1, red lines indicate the formation of different phases starting from pure metals. The first phase to form is Cu₆Sn₅ which is a monoclinic lattice system. The thicknesses of the metals in the design affect the outcome of the bond quality.

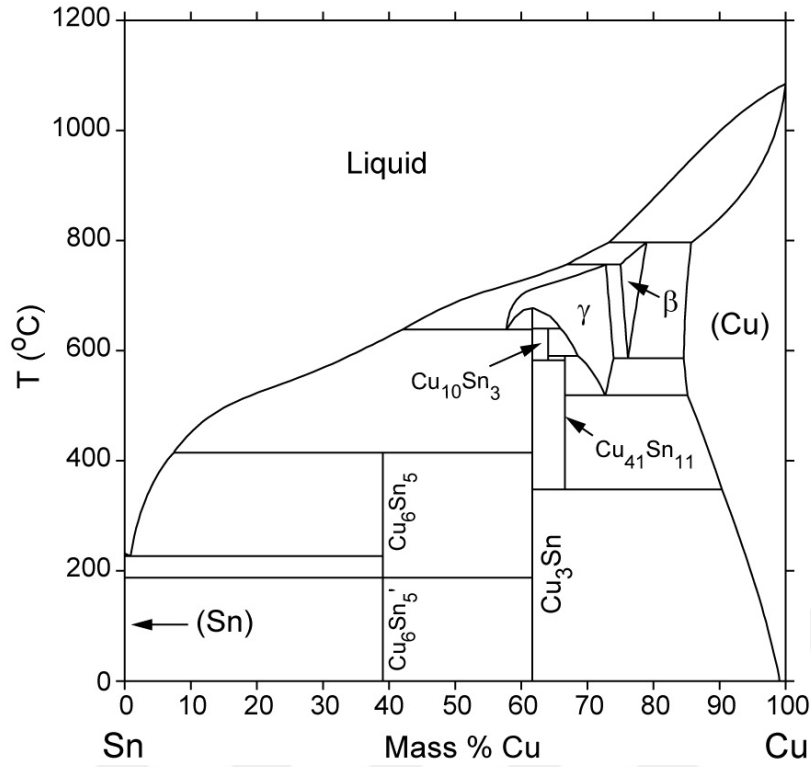


Figure 2.1: Phase Diagram of Cu-Sn.

Bosco et al. and Wang et al. showed that pore formation depends on the interlayer thickness, and there is a critical thickness such that below the critical thickness, there will not be enough Sn present in the system leading to premature consumption and resulting in poor bonds[32, 35]. Bosco et al. employed a stacked layer of 25 μm Cu and 5 μm Sn, deposited in a continuous vacuum. Bonding at 550 $^{\circ}\text{C}$ and 10^{-5} torr pressure with a bonding pressure of 0.001 MPa yielded a bond line with pores in the midsection. The explanation for this phenomenon was given by Bosco et al. in three scenarios.

1. The Cu_6Sn_5 growth is planar and the remaining Sn melts above the melting point during bonding. No pores occur depending on the thickness of Cu_6Sn_5 at the time of Sn melting.
2. If the Cu_6Sn_5 phase is growing in a non-planar fashion and the thickness below the critical thickness as shown above, Cu_6Sn_5 scallops connect, creating pockets where Sn cannot diffuse into, resulting in a porous mid-plane.

3. If Sn thickness is above the critical thickness, scallops of the first forming phase will not meet, and the bond will be free of pores.

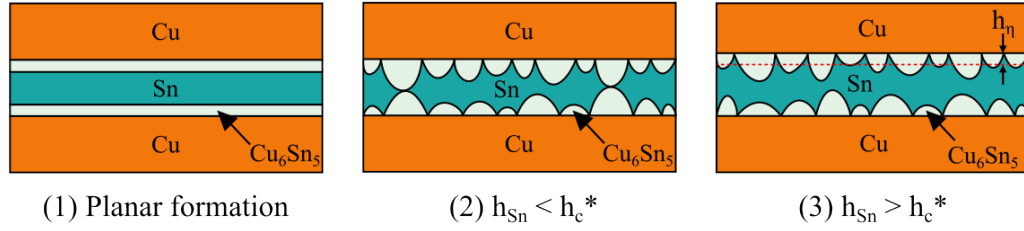


Figure 2.2: Schematics of three scenarios on the effect of critical thickness.

In cases where a porous midsection is not observed, Chiu et al. found that thin channels of unreacted Sn could span across the bondline from Cu-to-Cu. These channels occur due to Cu_3Sn scallops that start originating in the copper and as diffusion continues meeting scallops may leave channels behind as seen in Figure 2.3. However, these channels are not inherently damaging to the bond structure. In later stages of homogenization and solidification, Cu is transported to unreacted areas by way of these channels. This drastically alters the diffusion mechanism in the later stages of the bonding and explains the deviation from regular diffusion kinetics[36].

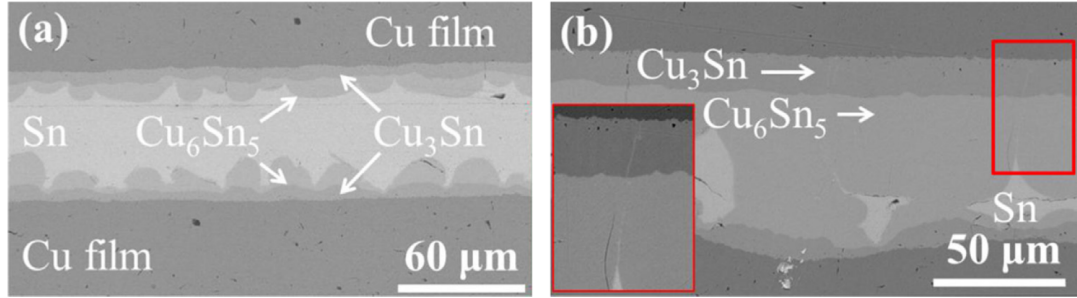


Figure 2.3: SEM image of cross-sections of samples bonded at 340°C a) for 3 minutes b) for 3 hours.

Liu et al. studied the CuSn system considering the final bond structure desired, Cu_3Sn . In their work, a Cu-to-Sn ratio was selected to be 1.3 since both squeeze-out and poor wetting of Sn yield unsatisfying results[37]. Their calculation was done below in the equation with the molecular weights and densities of the two constituting metals.

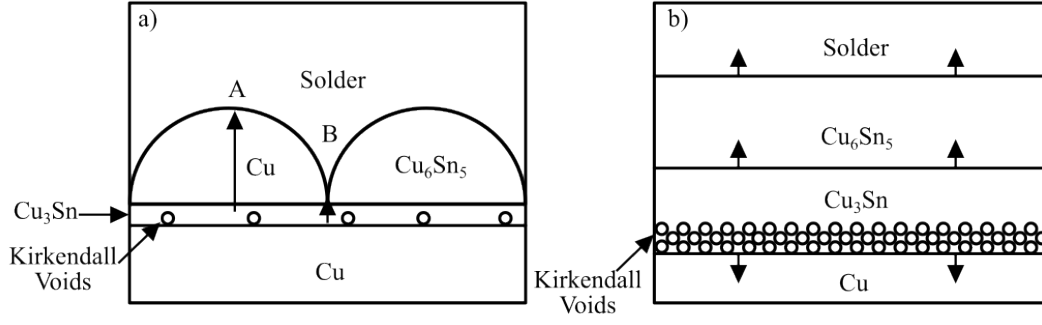


Figure 2.4: Schematic representation of Kirkendall a) void formation and b) progression.

They have chosen to use 5 μm of Cu and 3 μm Sn. Since the desired bond structure for this work was Cu/Cu₃Sn/Cu. Liu et al. founded that the formation of Cu₃Sn is the limiting factor since conversion from Cu₆Sn₅ to Cu₃Sn is a solid-state diffusion process. In accordance with the conclusions of Bosco et al., they noted that Cu/Cu₃Sn interface has Kirkendall voids due to a difference in diffusion rate.

$$\frac{d_{\text{Cu}}}{d_{\text{Sn}}} = \frac{3M_{\text{Cu}}\rho_{\text{Cu}}}{M_{\text{Sn}}\rho_{\text{Sn}}} = 1.31$$

Lapadatu et al. proposed and executed a Cu-Sn package for microbolometer focal plane arrays[38]. Similar to other works involving the Cu-Sn system, they used a TiW adhesion layer and Cu/Sn stack of 5 μm and 1.5 μm respectively. In their work, they state that Sn can be used as an alternative to gold for the oxidation prevention layer on top of the Cu layer since the oxide of tin can be broken apart with pressure during bonding resulting in a cheaper bond. More importantly, annealing at 350°C and 400°C revealed no significant difference in microstructure between the samples as shown in Figure 2.5. The conversion of Cu₆Sn₅ to Cu₃Sn depends on the process time and bonding profile since the diffusion rate increases exponentially with temperature in the Arrhenius-type equation.

In a diffusion couple consisting of Cu and Sn, diffusion occurs such that the first forming phase is η depending on the temperature. The solid-solid diffusion takes place even at room temperature, which should be considered in the design of the Cu-Sn system. Long storage times may consume Sn and prevent liquid formation during

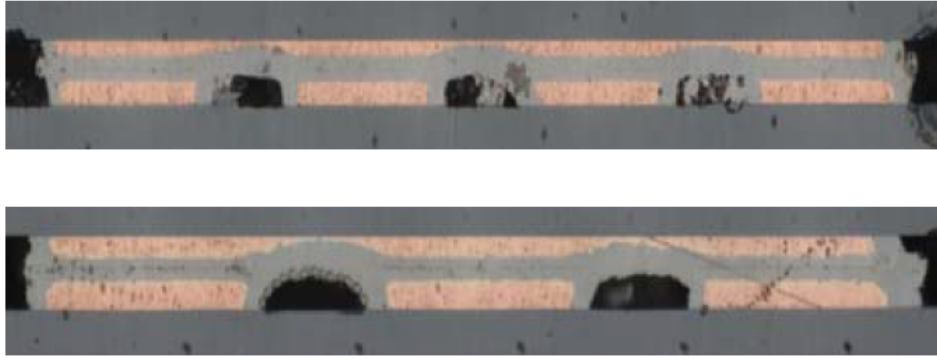


Figure 2.5: Photographs of cross sections through a bonded frame (full top side metal frame, railed bottom frame) after annealing at 350°C and 400°C respectively.

bonding operation[32, 39]. The critical thickness is important in the design of the stack for bonding in Cu-Sn. However, another aspect that should be considered is the solid-state interstitial diffusion between Cu and Sn if no diffusion barrier is present. Lee et al. found that the formation of Cu_6Sn_5 occurs at a rate of 3-6nm/day even at room temperature[40]. For bonding applications that require packages with less volume, the consumption of Sn could pose a problem if not calculated correctly.

Marauska et al., working with gold and copper systems combined with Tin, found that bonding between 240-280°C and applying constant pressure during dwell and bonding resulted in bonds that either averaged or exceeded 100 MPa in shear strength that satisfied the MIL-STD-883 shear strength standards[41, 42]. Figure 2.6 shows the bonding profile for such a system in which $T_I = 100^\circ\text{C}$ and $T_B = 240-280^\circ\text{C}$. The heating rate for this study was 30K/min. The importance of heating rate stems from the fact that the formation of Cu_6Sn_5 starts at even room temperature and accelerates above 150°C according to Flötgen et al. and to prevent premature consumption of all the Sn, high rates are required. The final bond given enough time, consisted of Cu and Cu_3Sn as seen in Figure 2.7[43].

Xu et al. used an electroplated Cu and Sn setup with 6 μm and 4 μm thicknesses, respectively. Bonding at 300°C for 30 mins under 3.5kN force that was applied after a uniform temperature below melting was obtained[44]. Bonding with the given conditions yielded bonds that were mostly Cu_3Sn and had some retained Cu_6Sn_5 at the edges of bonds where squeeze-out would be observed, Figure 2.7 illustrates an exam-

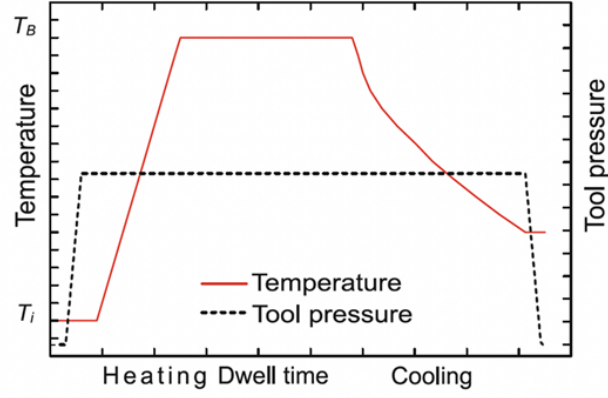


Figure 2.6: Schematic bonding profile indicating temperature and pressure times.

ple of such a structure. One of the important findings of Xu et al. is concerning the shear strength variation over the whole wafer. The thickness uniformity of the layers plays a role in the final strength of the bonds. They found that straying away from the center point resulted in lower shear strength as the mismatch in terms of thickness leads to non-uniform bonding pressure over the wafer.

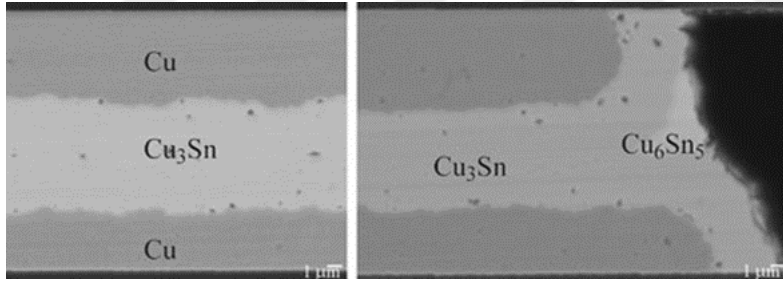


Figure 2.7: SEM images of bond interface with desired Cu/Cu₃Sn/Cu structure(left) and squeezed out Cu₆Sn₅.

Another important aspect that is present almost in all bonding works is surface oxidation which prevents proper bonding. Different approaches have been taken to eliminate oxidation of the top metal which is generally the low melting point one that oxidizes rapidly. The oxide layer must either be cleaned or the formation of oxides should be inhibited. Cleaning the metal oxide brings new challenges to the processing depending on the metals and substrate used. Certain chemicals or processing techniques may, for example, damage the CMOS, electrical connections, and the bond rings themselves. Hence, the second option of preventing initial oxidation gains at-

traction. A thin layer of Au with a thickness of 10-20 nm is used as the standard, as the gold layer does not interrupt or change the diffusion kinetics but prevents oxidation when subjected to ambient atmospheres[45]. For electroplated systems, the use of correct chemicals overcomes the oxidation problem. Thin films that are coated with PVD methods (sputtering, evaporation, etc.) require that the gold layer be coated without breaking the vacuum in the chamber.

Rautiainen et al. studied the mechanical stability of the CuSn system as well as contributed to the extensively researched characterization of the bond structure[46]. Symmetrical layer structures of Cu/Sn were used with 6 μm and 2 μm thicknesses, respectively. The ratio of Cu to Sn is 3, which is higher than the proposed critical thickness ratio of 1.3 of Liu et al. The layers were electroplated on top of a 40 nm TiW adhesion/diffusion barrier layer. A relatively high bonding temperature of 350°C and a long bonding time of 60 minutes was used, combined with the high Cu-to-Sn ratio temperature and time, allows all the Cu_6Sn_5 to be transformed to the desired phase Cu_3Sn . In their study, EDS from at least 5 spots was taken to determine and ensure phases. To observe the grain structure of the Cu_3Sn , a dilute solution of HNO_3 (3.5%), HCl (1%), and methanol was used as an etchant.

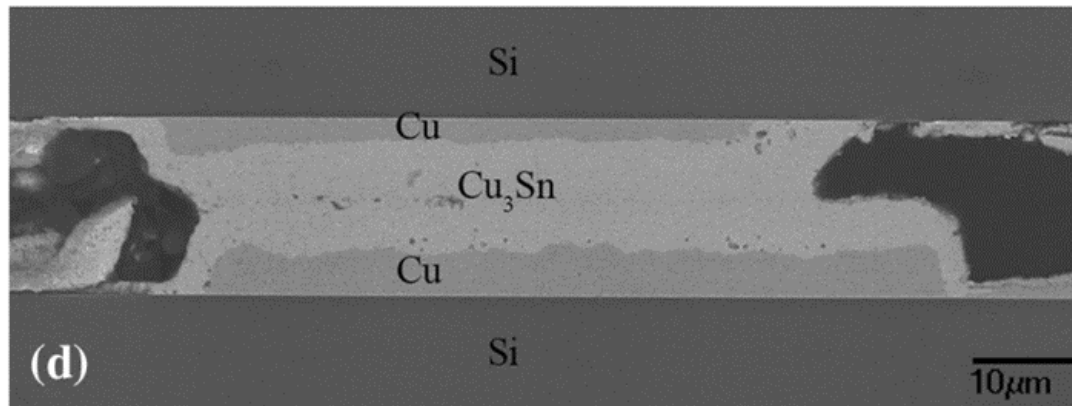


Figure 2.8: The bond line after bonding as aimed it consists of Cu/Cu₃Sn/Cu.

In figure 2.8, a Cu_3Sn is sandwiched between Cu as desired with close minimal voiding and Cu_6Sn_5 is not present in the system, indicating that a total transformation took place during bonding. Four different tests were conducted, namely shear strength, tensile strength, high-temperature storage test, and thermal shock testing. Mechanical tests revealed a shear strength of 275 ± 42 MPa and tensile strength of 91 ± 27

MPa on the samples that were not subjected to any other processing. These values are higher than the ones in the literature, and they may be attributed to the absence of Cu_6Sn_5 phase, which is present in other Cu-Sn TLP studies. Rautiainen et al. also inspected the fractured surfaces to determine the modes of fracture and explained them in three categories.

1. Interfacial failure.

- (a) At the interface between adhesion layer and the bond layer.
- (b) At the interface between adhesion layer and the substrate
- (c) At the interface between Cu and Cu_3Sn

2. Cohesive bond failure.

3. Cohesive substrate failure.

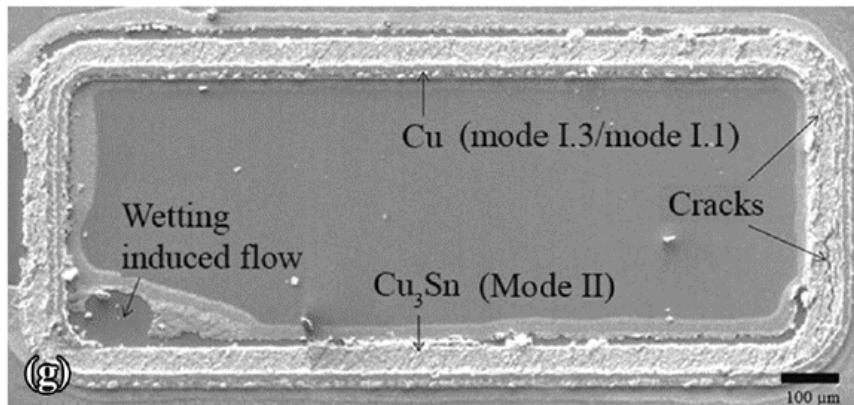


Figure 2.9: SEM image of the fractured surface with different fracture modes.

Out of these three failure modes, in shear testing mode II and mode I.(a)/(c) was found to be present. Figure 2.9 shows different modes from a fractured sample[46]. These findings indicate that the bond line should consist of Cu/ Cu_3Sn /Cu for a mechanically reliable bond.

High-temperature storage (HTS) tests were done by storing the samples at 150°C for 1000 hours. HTS tests revealed no statistical change in the mechanical strength of the Cu-Sn bonds, and no change in the fracture mode was observed. This is attributed to the long bonding time and the microstructure reaching a state of stability in which

the driving forces are very low for any change to occur in the system—resulting in high reliability at high-temperature working conditions. Thermal shock tests were performed between -40°C and $+125^{\circ}\text{C}$ with a hold time of 10 minutes at each temperature and 10 minutes of ramping, meaning that a cycle was set up to be 30 minutes. A total of 1000 and 3000 cycles were used also to compare their results. Regarding shear strength, Rautiainen et al. observed no significant change, and the failure mode was consistent with as-bonded samples. However, a substantial decrease in the tensile strength was observed, which was attributed to the increase in I.(a) and I.(b) failure modes also, transversal crack propagation was present in the samples after tensile testing. A significant reduction of 45% in tensile strength was observed with samples tested for 3000 cycles. However, packages are not subjected to tensile environments for most applications, and the strength values are still within military standards[46].

2.1.2 Cu-In TLP

Cu-In TLP bonding is another copper and low melting temperature metal combination that is available in the literature. Indium has a melting temperature of 156°C , offering lower temperature bonding approaches that wouldn't be otherwise available. As seen from the phase diagram in Figure 2.10 Cu-In system has several high melting point IMCs[47]. Generally, the 30 at. % In is aimed with a melting temperature of 632°C . The rectangle indicates the possible bonding temperatures; they are all above the melting temperature of indium. If bonding is performed above 305.8°C , the process parameters must be optimised carefully. Since failure to transform to η will result in liquid formation in service above 305°C . In the literature, studies about Cu-In for packaging applications are severely restricted.

Chen et al. investigated the Cu-In system as a fluxless alternative for packaging applications[48]. They employed an asymmetrical design with one side having both indium and copper and the other side having only copper. Figure 2.11 below schematically shows their stack design. The total concentration is 70 wt. % In and 30 wt. % Cu. If total transformation occurs, this will result in $\text{Cu}_{11}\text{In}_9$ phase. However, this phase would partially melt when above 155°C hence their initial stack design was lacking in reliability.

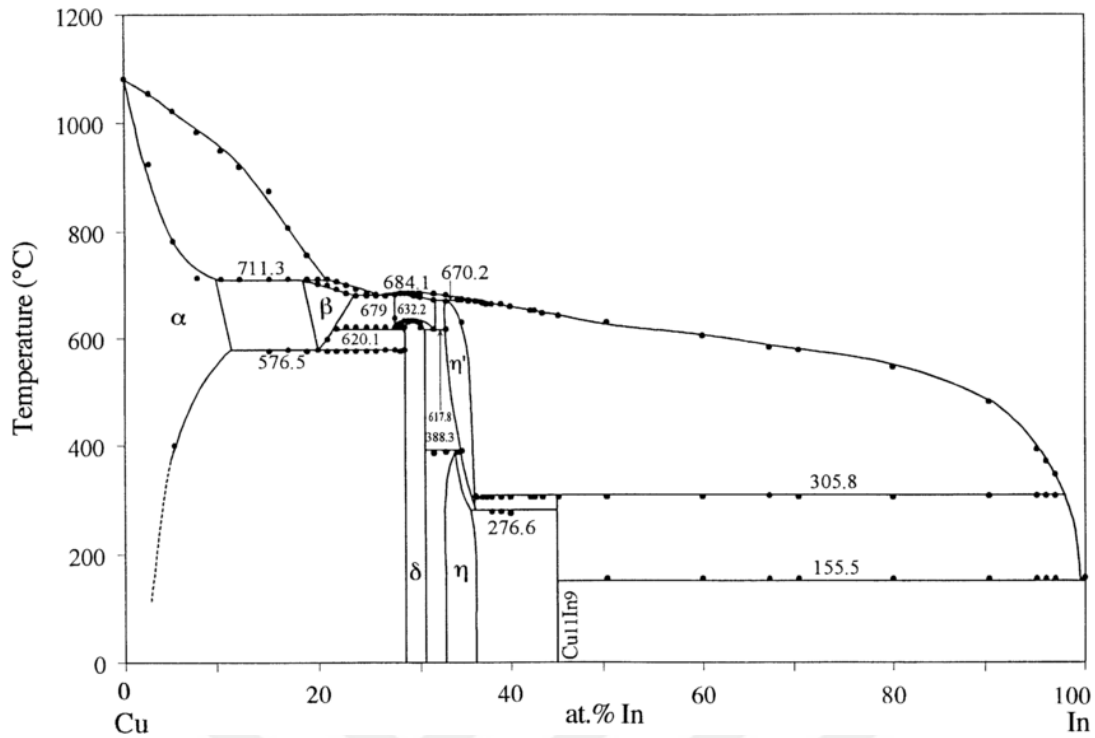


Figure 2.10: Copper-Indium phase diagram.

Cu-In system should contain Cu₇In₃ IMCs for a strong and reliable bond that will have higher melting temperature[49]. Lee et al. managed to obtain a bond line consisting only of Cu₇In₃. For their bonding, they used a Cu/In multilayer stack on both dies. Figure 2.11 shows the details of the design, as an adhesion layer Ti was employed, and a 0.2 μm Cu was used as a seed layer for electroplating. 20 nm thick Au is used to prevent oxidation of the indium layer. In₂O₃ has a negative Gibbs formation energy of 620 kJ/mol, compared to that of SnO, which has a Gibbs formation energy of -260 kJ/mol the necessity of an oxide prevention layer becomes apparent.

During HTS testing, Lee et al. discovered that holding at high temperatures led to an increase in shear strength. This suggests that the transformation from thin film to IMC was not fully completed, and that additional time at high temperatures allowed for further solid-state diffusion to occur and complete the IMC formation. After bonding, SEM showed the presence of two distinct phases, as seen in figure 2.12a). The light grey areas were identified as Cu₉In₁₁ or δ, with 42-46 at. % In, while the darker grey areas were found to be Cu₇In₃ with 29-31 at. % In, according to EDS analysis. This suggests that the bonding time was insufficient and that there was a lower remelting

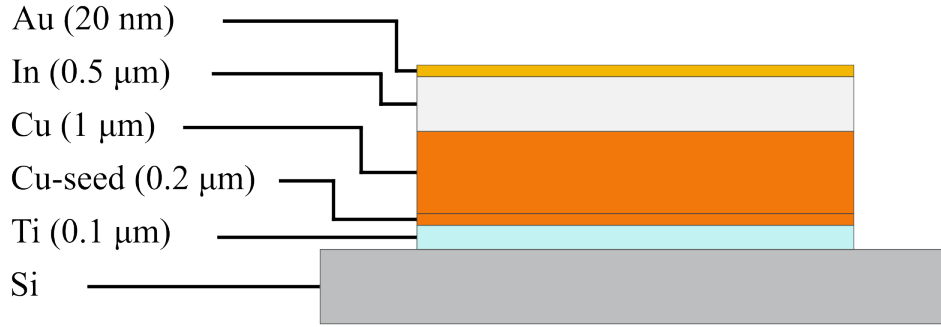


Figure 2.11: Schematic representation of metallization and thicknesses for Cu-In bonding

temperature IMC, δ , present in the bond. HTS testing further confirmed that given more time at higher temperatures, all the remaining $\text{Cu}_9\text{In}_{11}$ would be transformed to Cu_7In_3 through solid-state diffusion, as seen in 2.12b).

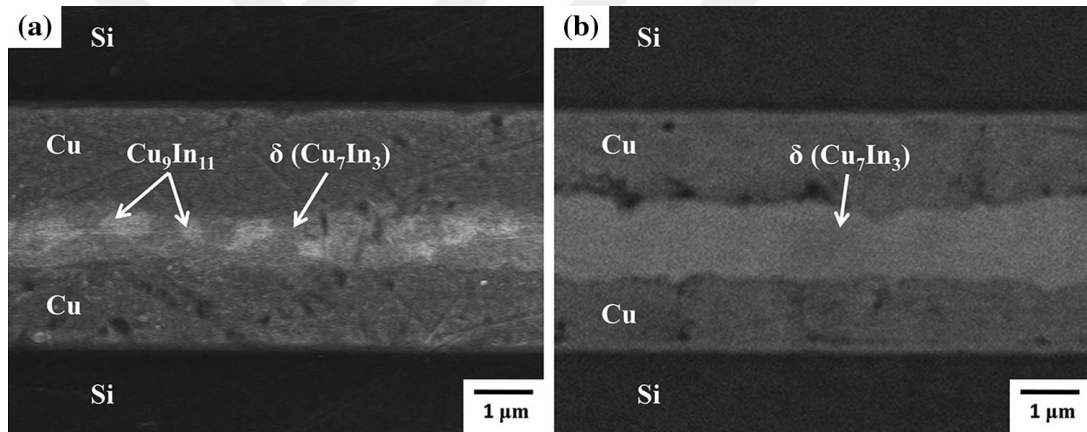


Figure 2.12: SEM images of the cross-sections: a) as bonded b) after HTS testing.

2.2 Ternary TLP Bonding

2.2.1 Au-In-Bi TLP

For applications with tighter restrictions on the bonding temperature rather than the high melting point, Aasumendveit et al. studied a gold-indium-bismuth system for a possible low-temperature bonding alternative. Lower process temperatures are made possible by employing a eutectic mixture with a low eutectic temperature T_E . Bi-

Bi-In system has a eutectic point around 78 at % In with a eutectic temperature of 71.8°C[50]. Low-temperature eutectic allows TLP bonding if a eutectic mixture of Bi-In is used as the interlayer. The binary phase diagram of Bi-In is shown in Figure 2.13[51].

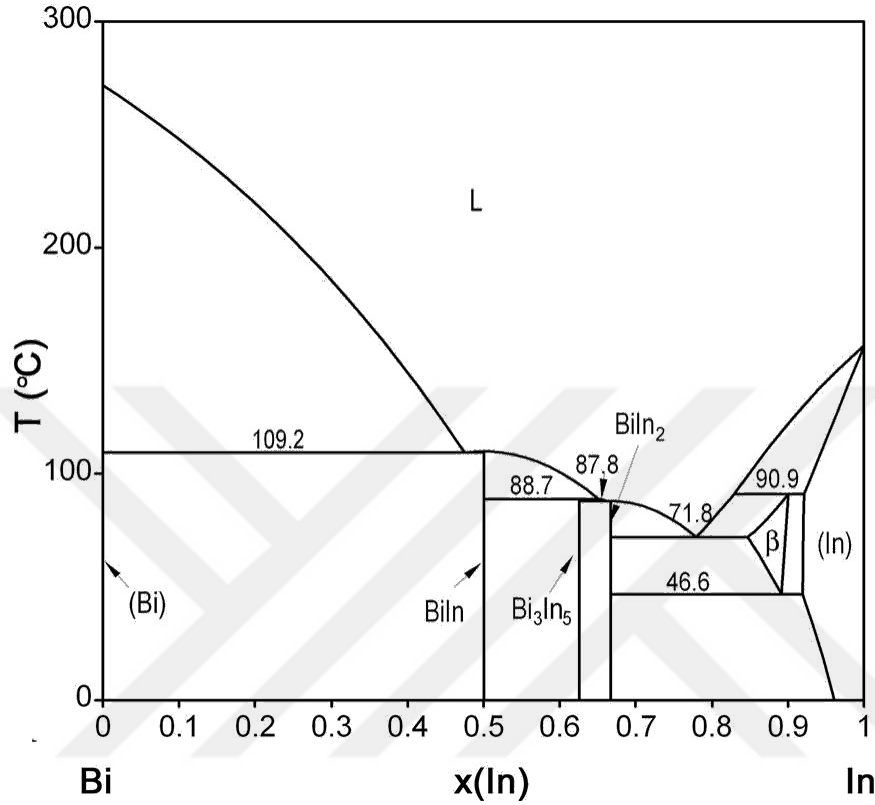


Figure 2.13: Phase diagram of Bismuth and Indium.

Gold and Bismuth don't have any IMCs that are stable at room temperature; hence the bond line is expected to be consisting of Au_xIn_y intermetallics with free bismuth in the bond line. This bonding will result in the melting temperature being the same as bismuth's, $T_m=271^\circ\text{C}$ [52]. Even though AuIn IMCs have higher melting points, liquid formation during service is considered catastrophic for the device, and the reliability will be limited due to Bi melting.

Aasmundveit et al. used 140 μm of eutectic Bi-In between Au and tested bonding at 90°C, and 110°C and bonding time also varied between 15 minutes to an hour. It was found that using a high heating rate of 20°C/min resulted in scallop formation, which, as mentioned before, is generally detrimental to bond strength and soundness and decreased the rate to 2°C/min.

Interdiffusion starts at the gold-preform interface since Au-Bi does not have any stable IMCs at that temperature; it only occurs between gold and indium. Bonding at 90°C resulted in multiple gold-indium intermetallics, AuIn, AuIn₂, and Au₇In₃ and BiIn₂ as seen in figure 2.14. Retained BiIn₂ in the bond leads to premature melting since it has a melting temperature of 89.5°C. However, it is seen that with this bonding temperature, unless process time is extended, sufficient amounts of indium will not be spent out of the preform leading to remaining BiIn IMCs.

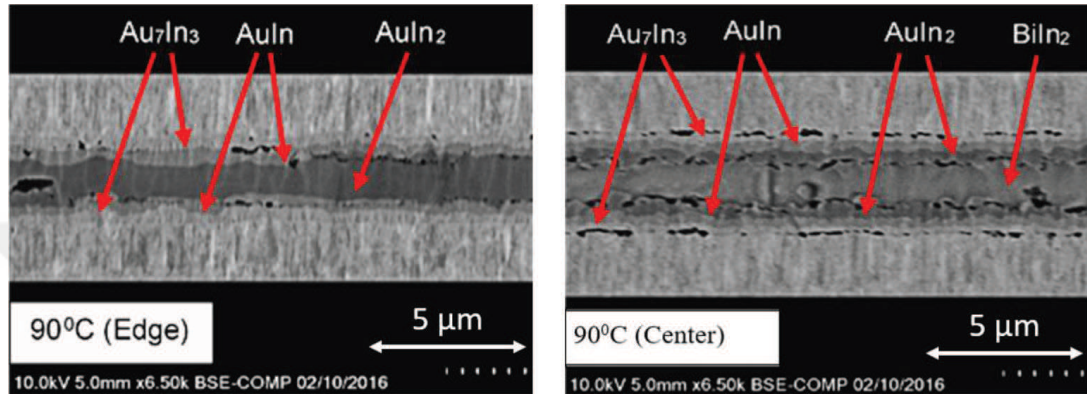


Figure 2.14: SEM image of the bond line taken from edge and centre showing different phases after bonding at 90°C.

Increasing the bonding temperature to 110°C, more indium is diffused with Au to form AuIn IMCs, namely AuIn and Au₇In₃. When the indium content is below 33 wt. %, BiIn IMCs can not be present since it is not stable above 109°C and in the bond line, only retained Bi can be found from isothermal solidification, which is seen in the figure 2.15. Further decrease in bonding time was achieved by thermally evaporating Bi-In at eutectic composition rather than using a preform which slows the diffusion. Mechanical testing revealed shears strengths up to 50 MPa, well above the standard package requirements. Additional testing with electrical impedance spectroscopy confirmed very limited voiding in the bond[53].

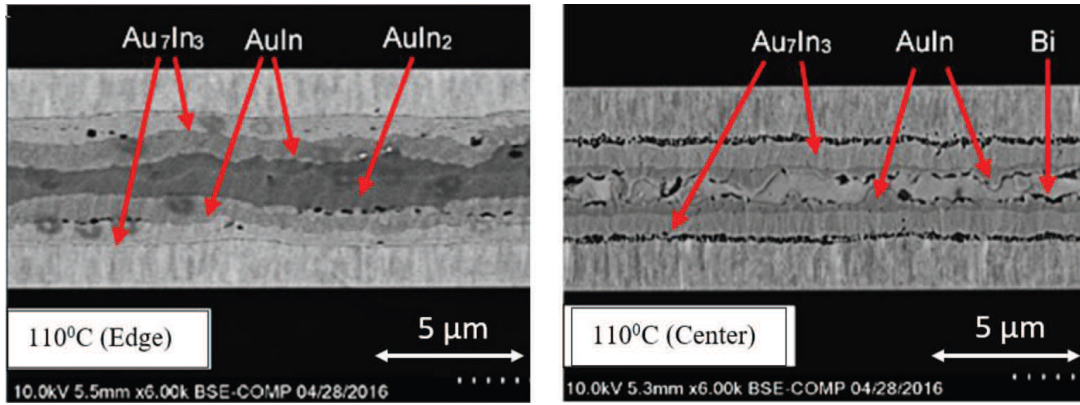


Figure 2.15: SEM image of the bond line taken from edge and centre showing different phases after bonding at 110°C.

2.2.2 Cu-In-Sn Bonding

The addition of In to Cu-Sn or vice versa is found to decrease the bonding temperature of the system down to at least 200°C[54]. An increase in mechanical strength was also an advantage of combining In and Sn for Cu-IMC systems[55]. The kinetics of diffusion plays a crucial role in the bond quality and process optimization for ternary systems as the number of IMCs and their effect on the kinetics get more complex. At the eutectic temperature of Sn-In, 120°C[56], the tin and indium that have mixed up through solid-state diffusion melt. As temperature further increases and $\text{Cu}_x(\text{In},\text{Sn})_y$ IMCs start to form depending on the Sn-In concentration[57].

The rate at which intermetallic form is essential for the process parameter selection because after IMCs start forming, enough time should be given to the system to get a homogenous system free of voids. Sasangka found in their research that Cu is consumed the fastest when a eutectic composition of $\text{Sn}_{48}\text{In}_{52}$ is used as the intermediate layer. The time it takes to consume a 583 nm Cu layer is given in the figure 2.17 below, and it is concluded that the fast consumption is due to a low melting temperature corresponding to higher atomic mobility[58].

Yan et al. studied the Cu In Sn ternary system for chip-to-chip bonding. Metallization was performed by electroplating for Cu and evaporation for In/Sn composite solder. Only the device wafer was prepared such that it had the whole metallization; the cap side only had Cu in their design, which is seen in figure 2.19. Bonding of 10 mm x 10

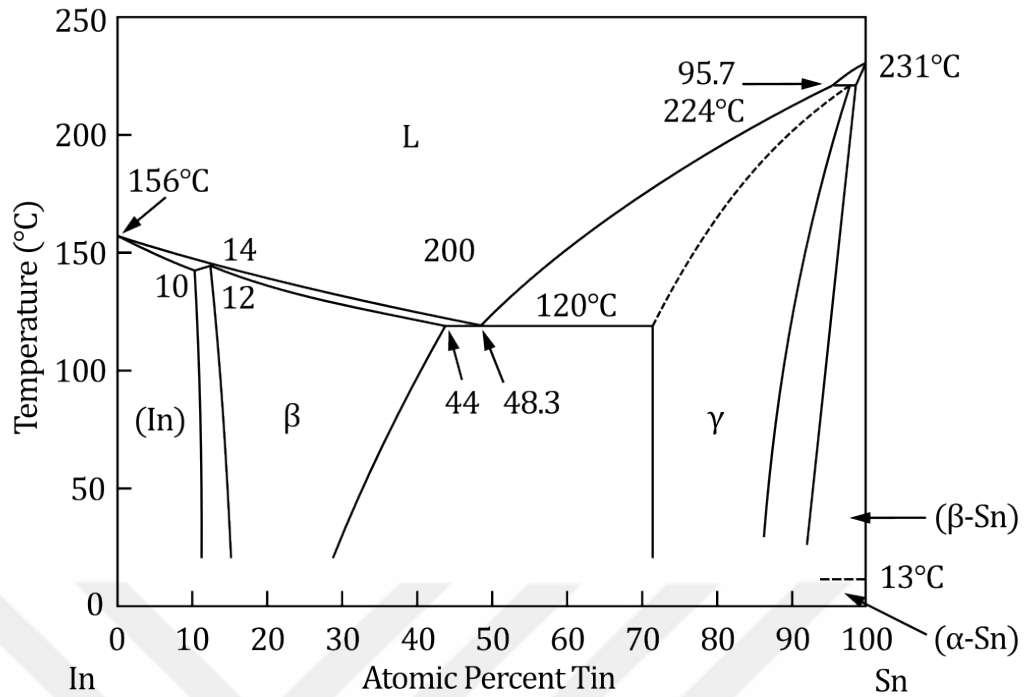


Figure 2.16: Sn-In phase diagram.

mm dies in flip-chip between 140°C and 180°C under 1.5 MPa. On the device-side dies, a flux was applied to facilitate soldering. It is shown in their study that bonding in short periods, 5 minutes, resulted in voids in the centre of the bond. Increasing the temperature and bonding time resulted in better bond quality; as seen from Figure 2.18, voids present after 5 minutes are gone when the bonding time is 20 minutes.

In the Cu-Sn-In system, several fracture modes, as mentioned before, are present due to the fact that any unreacted Sn or In will add another interface where failure may occur. Study by Yan et al. found that even at a relatively low bonding temperature of 180°C the fracture occurs in a mixed mode, meaning cohesive and adhesive fractures proving that the bond is viable under proper conditions. The maximum bond strength obtained was 7.3 MPa, and the average value was 6.5 MPa[59, 60]. They concluded that the melting temperature of the bond was 300°C using the phases present in the bond and the phase diagrams. Two dominant phases were present in the bond η -Cu₆(In,Sn)₅ and Cu₁₁(In,Sn)₉.

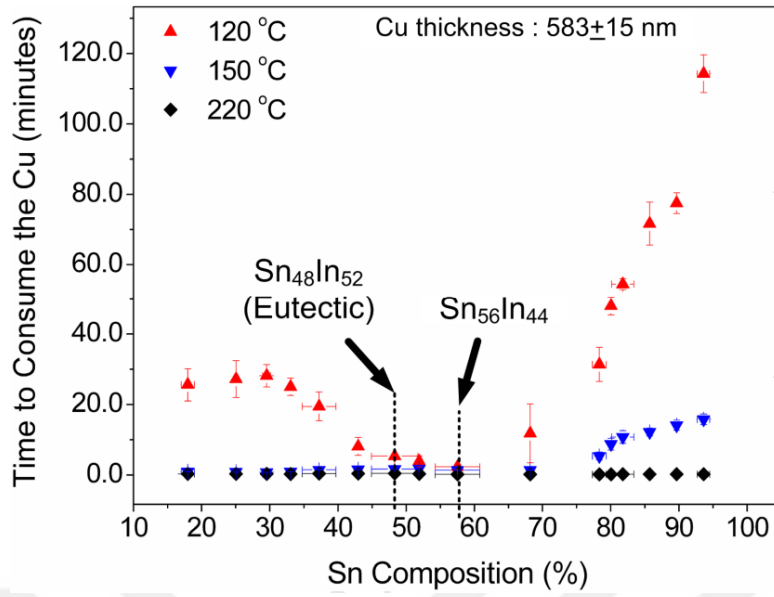


Figure 2.17: Variation of copper consumption depending on the $\text{Sn}_x\text{In}_{100-x}$ concentration.

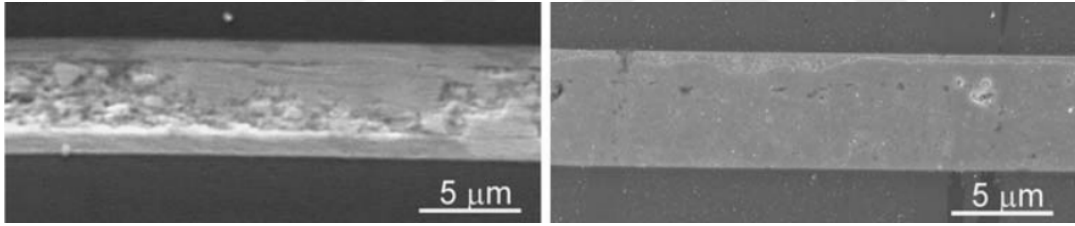


Figure 2.18: Effect of bonding temperature on voiding. a) bonded for 5 minutes, b) bonded for 20 minutes.

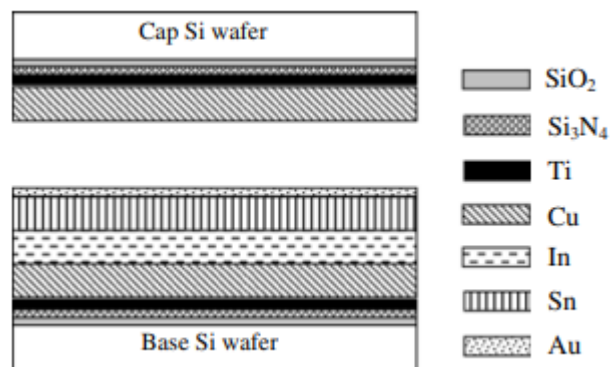


Figure 2.19: Multilayer material structure on cap wafer and base wafer.

CHAPTER 3

EXPERIMENTAL PROCEDURE

In this section, the experimental procedure is explained. Single-side polished silicon and glass wafers are used for bonding experiments. Bonding parameter optimisation is performed. After bonding, the characterisation tests of the bond in terms of microstructure and mechanical properties are explained.

3.1 Fabrication Methods

3.1.1 Lithography

For the lithography process AZ® nLOF 2070, a negative tone photoresist was chosen to form the bond rings on the wafers. The choice for negative photoresist arose from using a bond ring mask used before at METU MEMS. Negative photoresists, after exposure and development, end up with a narrower opening at the top and a wider opening at the bottom from the desired width, which is depicted in Figure 3.1. The narrow space and the wall establish that the subsequent coatings will have a more right-angled wall structure, which is desired to increase the bonding yield. Focusing on the quality of lithography with the chosen resist means that etching is not required. Fabrication of the bond rings without wet etching and a process optimised for negative photoresists yields sharper structures since the different layers do not have to be etched separately.

First, the wafers are dehydrated at 110°C for 10 minutes to remove any moisture that might be present. The reason for dehydration is to enhance the adhesion of subsequent layers to the surface; any moisture present will reduce the adhesion. The

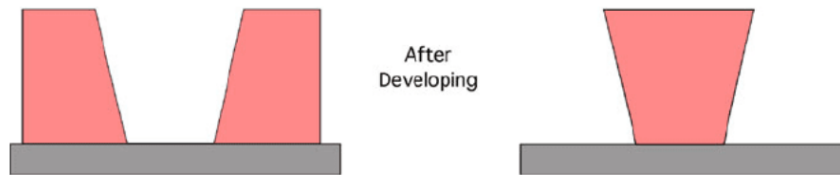


Figure 3.1: Schematic comparison of positive and negative photoresists after development.

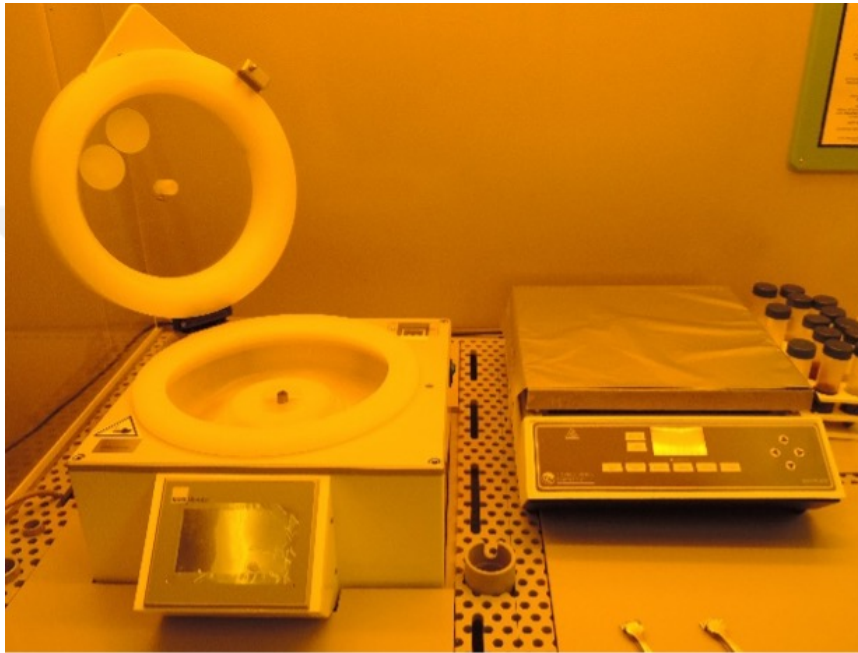


Figure 3.2: SUSS MicroTec Spinner and Torrey Pines hotplate.

dehydration process is done in a nitrogen environment in a drying oven. The wafers are then cooled to room temperature in a desiccator to prevent moisture. The wafers must be cooled beforehand since any change in size affects the photoresist coating. The wafers are primed using HDMS that promotes adhesion of the photoresist. The photoresist is spun at 3000 rpm in a SUSS Lab spin coater and soft-baked at 110°C in a Torrey Pines hotplate seen in Figure 3.2. The backside is cleaned with acetone and isopropyl alcohol. Backside cleaning is performed to prevent sticking of the wafer to the aligner that is used to shape the photoresists.

UV exposure is performed in an EVG6200 contact mask aligner, as shown in Figure 3.3. The wafer did not have any alignment marks; hence, the bond ring structures

were exposed without alignment. The mask used for the bond-ring lithography is aligned within itself such that the alignment marks are levelled in one direction. Exposure was performed with 2.5 seconds exposure and 5 seconds delay continuing for three cycles. Immediately after exposure, wafers were baked on a hotplate at 110°C for 90 seconds. Post-exposure bake allows for the links in the photoresist to set; otherwise, during development, the photoresist is removed completely. The photoresist undergoes chemical and physical changes after UV exposure and development. If not developed, the photoresist will not retain its structure, similar to a thermosetting polymer that requires curing to be finalized. Development was done by hand in 2-litre beakers using MF-24A as the developer. Development time was 90 seconds; afterwards, wafers were rinsed in DI water beakers.

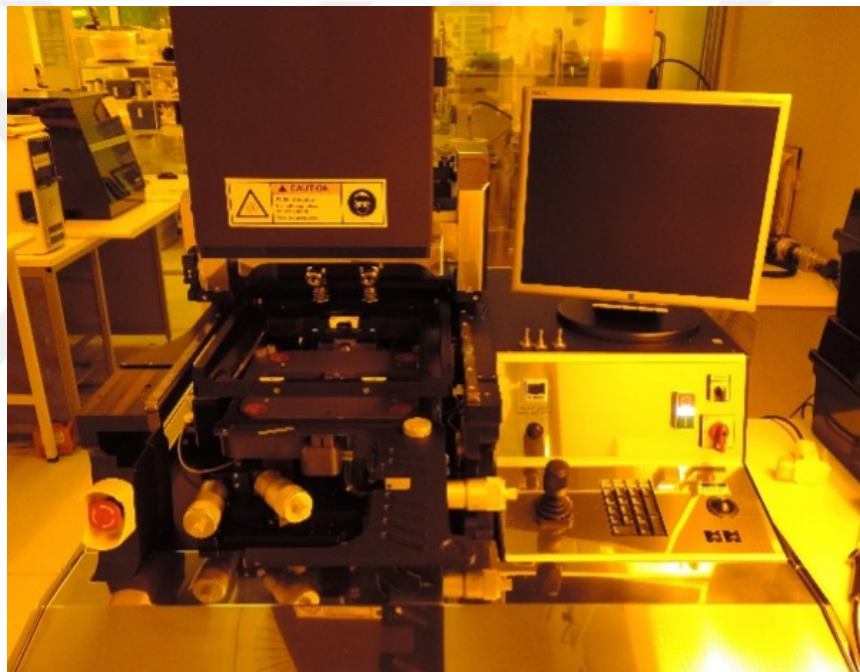


Figure 3.3: EVG6200 contact aligner.

3.1.2 Metallisation

Metallisation was performed in three steps. The copper layer was sputtered, and the tin/indium layers were evaporated.

Sputtering works on the principle that a target metal is bombarded by ions inside a

plasma, generally Argon, formed between the target metal and the wafer. The ions that are charged are accelerated towards the target, which is inversely charged, and they remove atoms from the surface of the target; no melting or evaporation is required for coating. Therefore, it is suitable for high melting temperature metals. The sputtering process is shown schematically in figure 3.4.

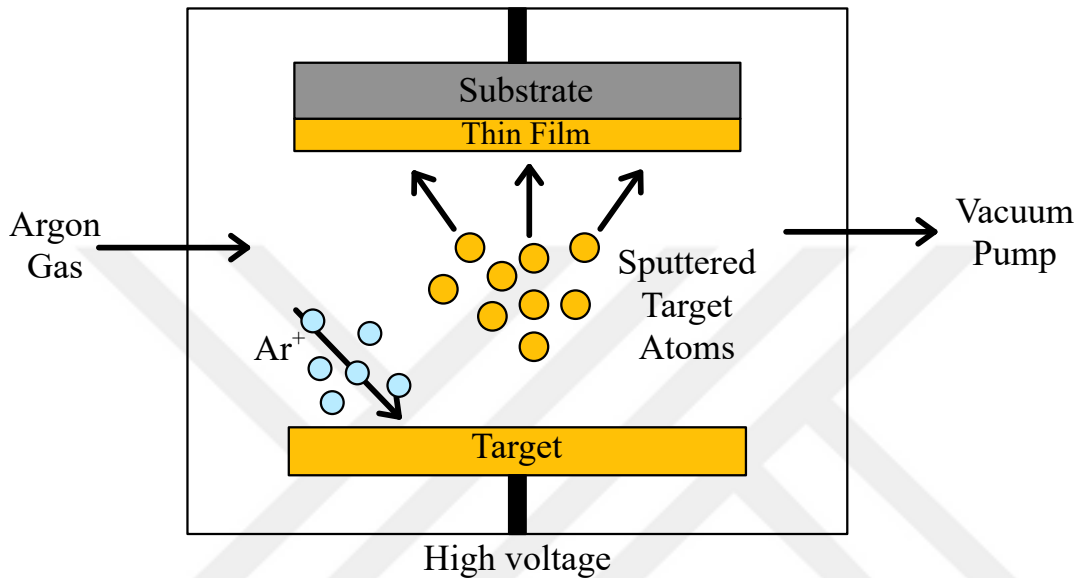


Figure 3.4: Schematic representation of sputtering chamber and process.

Copper was deposited using AJA DC sputter system as seen in Figure 3.5. In sputtering, Argon gas was used to form a plasma, which is then directed towards the target metal. The metal atoms separated from the surface are flung towards the wafer. 100 nm of Ti10W90 is sputtered first at 300 Watts as an adhesion and barrier layer and followed by Cu at 600 Watts sputtering under Argon plasma with a DC source. The deposition was done in two parts to allow the wafers to cool down after 600 nm is coated. Because the following layers will be coated in different systems, a 25 nm layer of gold is coated with a power of 350 watts to prevent oxidation during transfer.

In the AJA sputtering system, an 8" holder is used with three 4" slots. The targets are inclined, and the wafer is rotated during bonding to ensure deposition uniformity. Chamber pressure during deposition was 2.8×10^{-3} mTorr. The deposition rate was 5.5

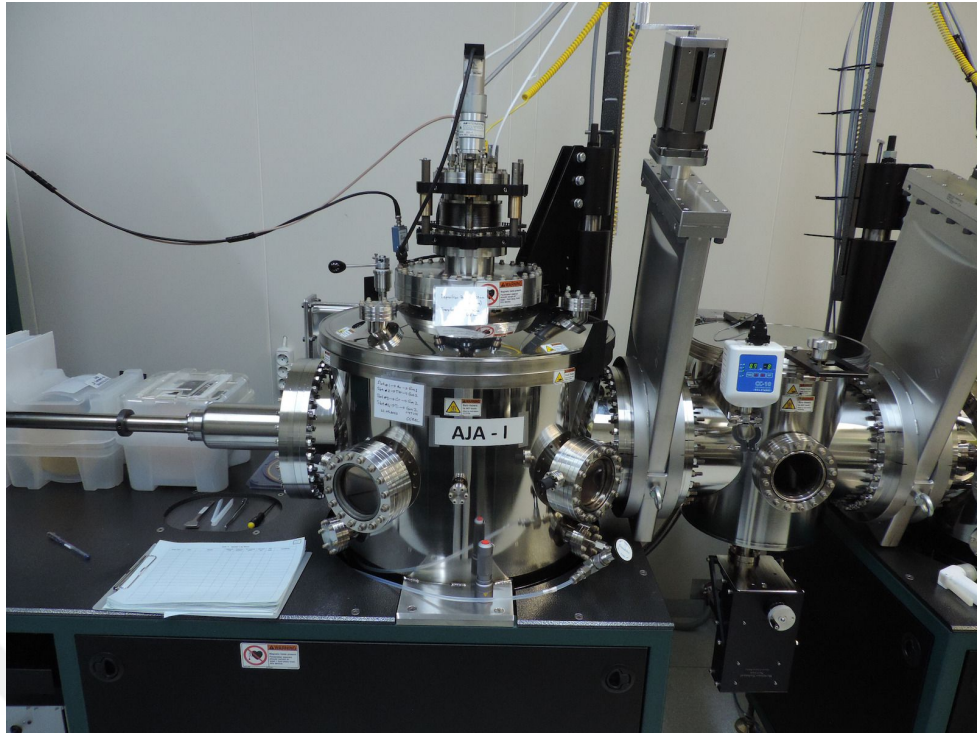


Figure 3.5: AJA DC sputter system.

$\text{\AA}/\text{sec}$, and the thickness difference between the centre and the edge was 15 nm at maximum. Configuration of the wafer in terms of the layer is schematically shown in Figure 3.6.

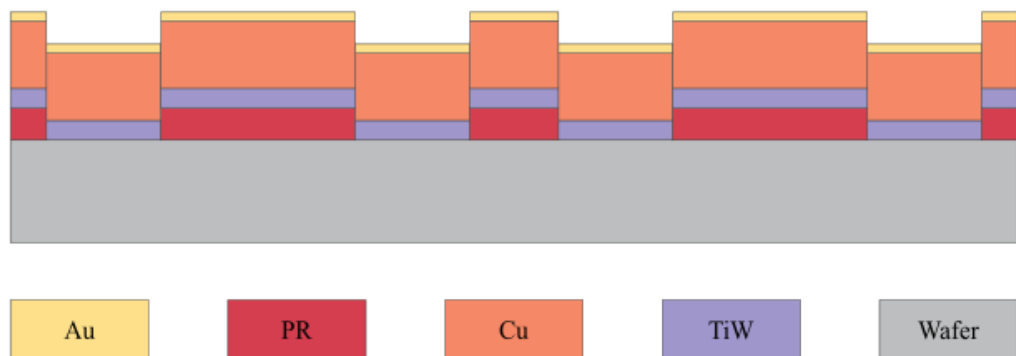


Figure 3.6: Schematic representation of the cross-section after sputtering.

In evaporation, as the name suggests, the deposition is made by the evaporation of the target material, which is performed by applying a current to the metal. This technique

requires that the boiling temperature and the vapour pressure of the metal be on the low end between other metals for maximum efficiency. Both Indium and Tin fall into this category in this work. Although gold requires more power to be evaporated, it is still an applicable method. The mechanism of deposition, as well as chamber structure, is shown in Figure 3.7.

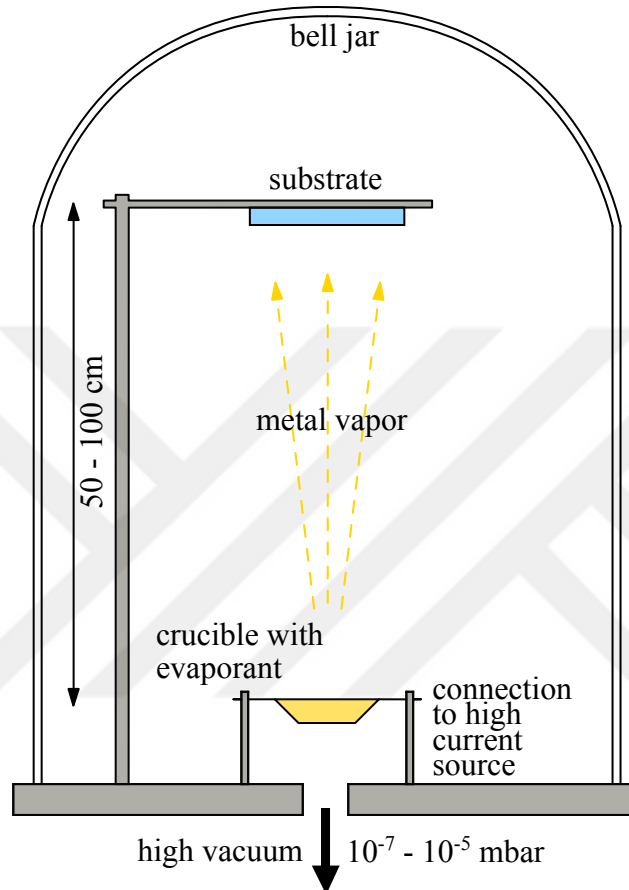


Figure 3.7: Schematic representation of evaporation chamber and process.

Separate evaporators were used to prevent contamination between Indium and tin. Tin was deposited in a Varian 3119 Thermal Evaporator under vacuum conditions seen in Figure 3.9. 2.5 grams of Sn in pellet form was placed in Tungsten boats. 200 watts was chosen as the power for the coating. There are seven 4" slots on a planet, and wafers were loaded such that the centre was left empty. The deposition rate was chosen as $4 \text{ \AA}/\text{sec}$, and fluctuations in the rate were corrected during evaporation by fine-tuning the power. The shutter was opened only after stable power was obtained. Wafers were placed on the planet, as seen in Figure 3.8.

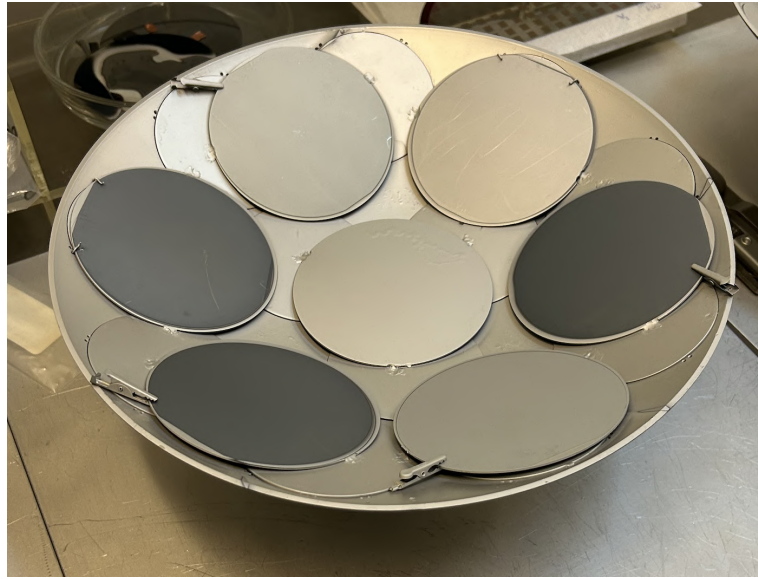


Figure 3.8: Planets used in thermal evaporation for uniformity.



Figure 3.9: Varian 3119 thermal evaporator.

A gold layer of 25 nm was coated on top as an oxidation barrier. For gold, coating power was chosen as 250 watts, and the coating rate was kept at $2\text{\AA}/\text{sec}$. Gold and Indium were placed in different boats. During deposition, the vacuum was not broken and remained at 7.5×10^{-7} Torr.

Indium was coated in a Nanovak NVTH-350 thermal evaporation system as seen in Figure 3.10. A maximum of two 4" wafers could be coated in this system with an 8" chuck. Two diagonal boats were filled with Indium, and 200 watts of power was used. However, due to a mechanical issue, given the same power, one of the sources would deposit at a higher rate; hence, one of the sources was kept at 160 watts during the coating to have a $20\text{\AA}/\text{sec}$ rate across both sources. The total thickness of the Indium was 500 nm. As with other layers, a 20 nm Gold layer was coated on top to prevent oxidation before bonding.

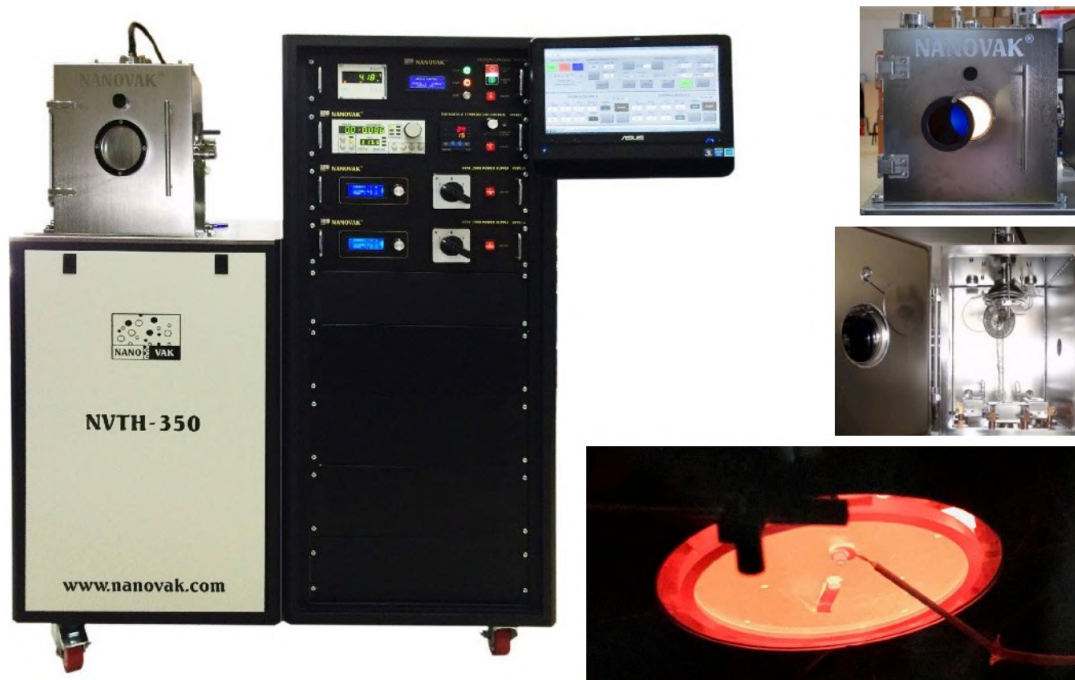


Figure 3.10: Nanovak NVTH-350 thermal evaporator and inside view of the chamber.

3.1.3 Liftoff

For the liftoff process, wafers were placed in an acetone tank in a cassette. To ensure all the metal was stripped, they were soaked in acetone overnight. Cleaning the

remaining residue was done using an ultrasonic buzzer for 10 minutes at least. The buzzer is seen in Figure 3.11a. After that, to ensure cleanliness, wafers are sprayed with acetone, followed by IPA. The drying was performed in an SRD-drying system in a nitrogen environment; SRD is as seen in Figure 3.11b.



(a)



(b)

3.2 Process Flow

Process flow employed in this thesis is summarized in Figure 3.12 starting with photoresist coating, then consecutive exposure and development. Followed by the metalization of individual Cu, Sn and In. Preparations are then finished by lift-off.

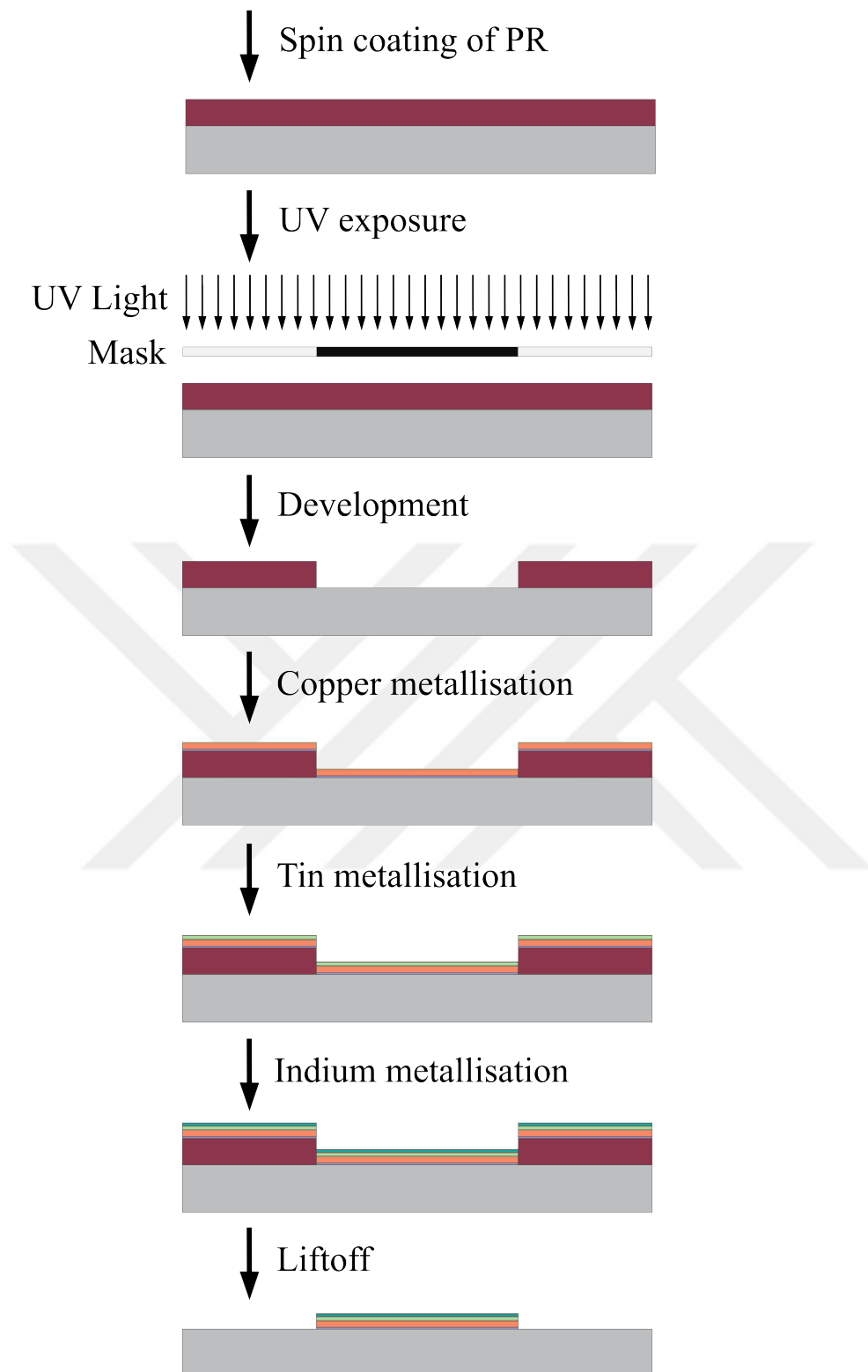


Figure 3.12: Schematic of the microfabrication flow.

3.3 Bonding Methods

Bonding was carried out in an EVG 520 IS wafer bonder, which can be seen in Figure 3.13. The maximum force capability for this thesis was 20 kN, and the maximum heating rate was 20°C/min. Forming gas was used for all the bondings, a gas mixture of 95% nitrogen and 5% hydrogen. Forming gas is utilized for eliminating moisture and oxygen. The bonding chuck has three flags that keep the wafers separated until bonding. The pressure uniformity of the bonder is crucial for the success of bonding for TLP bonding.

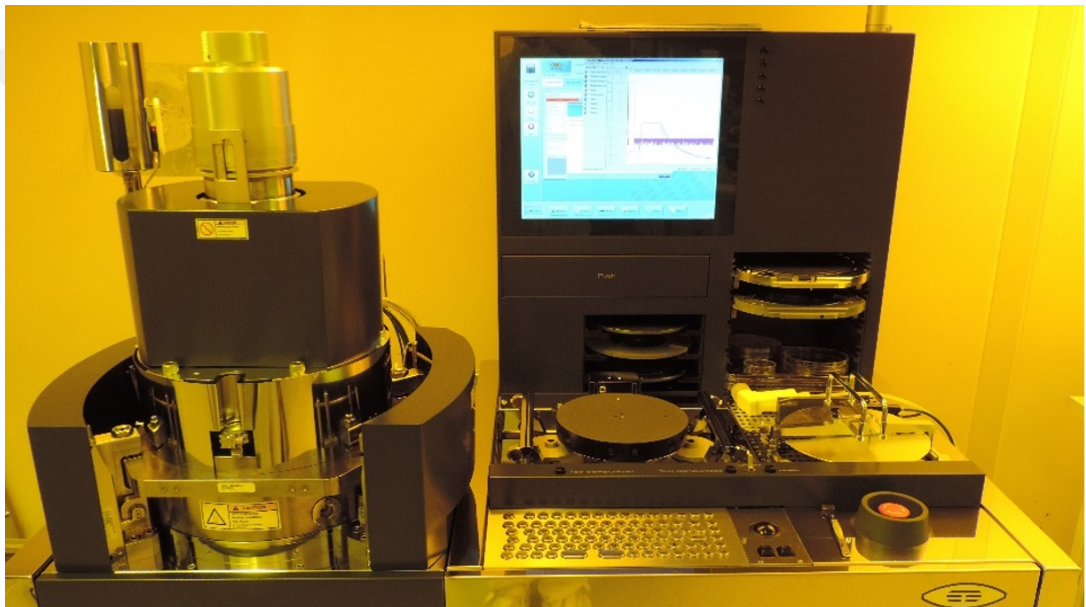


Figure 3.13: EVG 520IS wafer bonder.

The bonding tool or chuck and its alignment play a crucial role in the success of the bond. Clamps hold the wafers in place during bonding; skewing of the wafers towards any side will result in the misalignment of the bonding apparatus and, therefore, the wafers. Three flags separate the wafers before the bonding operation, and they are drawn back before pressure is applied. Figure 3.14 shows the schematic of the bond chuck[3]. To ensure pressure and temperature uniformity, a graphite plate is placed on top of the aligned wafer complex on the bonding chuck. The bottom side of the chuck is already equipped with the same graphite plate.

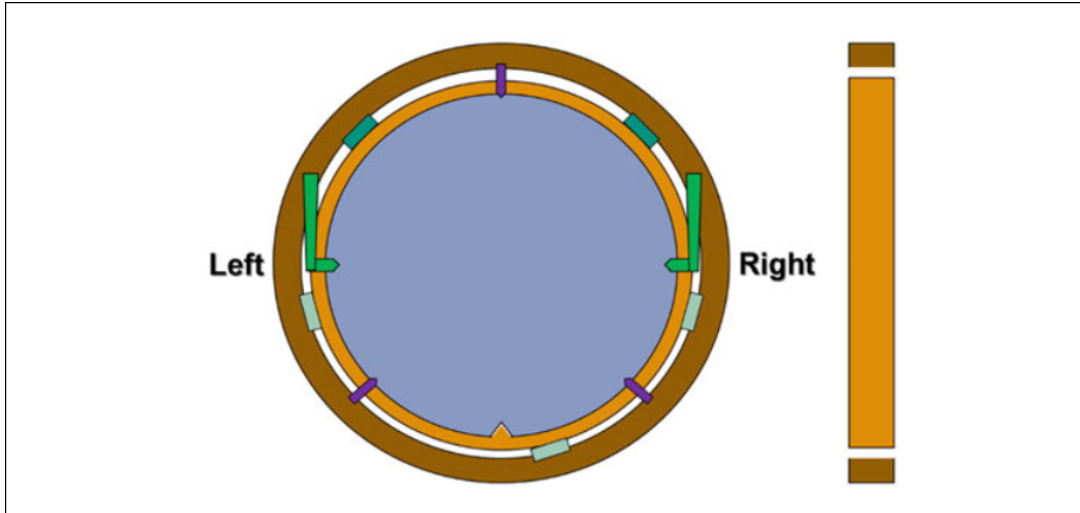


Figure 3.14: Schematic of the bonding chuck used in the experiments. Flags are in violet, and the clamps are in green.

3.3.1 Unpatterned Wafers

Initial experiments were designed to test whether a bonding could occur or not. For this purpose, the most straightforward and most logical approach was to use the whole surface of the wafer as the bonding area instead of trying to achieve bonding area instead of trying to achieve bonding by using bond-rings formed by lithography. To that end, the whole wafer trials, due to not having any patterns for the following part of the thesis, will be referred to as unpatterned wafers.

Theoretically, from the phase diagrams, bonding could be achieved at lower temperatures. However, as process optimizations are required, two moderate temperatures of 250°C and 300°C were chosen as the starting point for the experiments. To achieve maximum wetting so that proper bonding could take place more easily, the pressure applied was chosen to be 2.2 MPa. Using higher pressures could result in smoother bonding. However, the pressure is determined by the maximum force output of the EVG520 bonder, which is limited to 20 kN. The wafers are first heated to an intermediate temperature below the melting points of both Sn and In which gives time for solid-state diffusion to get closer to the eutectic Sn-In composition. It also provides temperature uniformity since, under vacuum conditions only conduction and radiation is responsible for the heating. At this point a force of 5 kN(0.4 MPa) is

applied to further increase the solid-solid diffusion by physically driving the metals together. After temperature uniformity is obtained during the pre-heating, the wafers are brought to the designated bonding temperature and pressure applied. The heating rate for all heating parts is the maximum 45°C/min available to the EVG 520 Bonder. After 30 minutes at the given temperature, the pressure is lifted and the wafers cooled in the chamber to room temperature.

Unpatterned silicon wafers were first used to try and see if bonding would occur in a way such that copper-tin-indium have sufficient strength. Two 4" wafers were coated with 500 nm Cu, 250 nm Sn, and 250 nm In. Two different bonding profiles were executed for this test. Two bonding temperatures of 250°C and 300°C were chosen. The temperatures were chosen to be higher to make sure that bonding was possible before lowering them further. A maximum tool force of 18 kN was used for the bonding. For an unpatterned wafer with an area of approximately 7800 mm², the pressure is found to be 2.2 MPa. Bonding temperatures and pressures are seen in Figure 3.16 & 3.15.

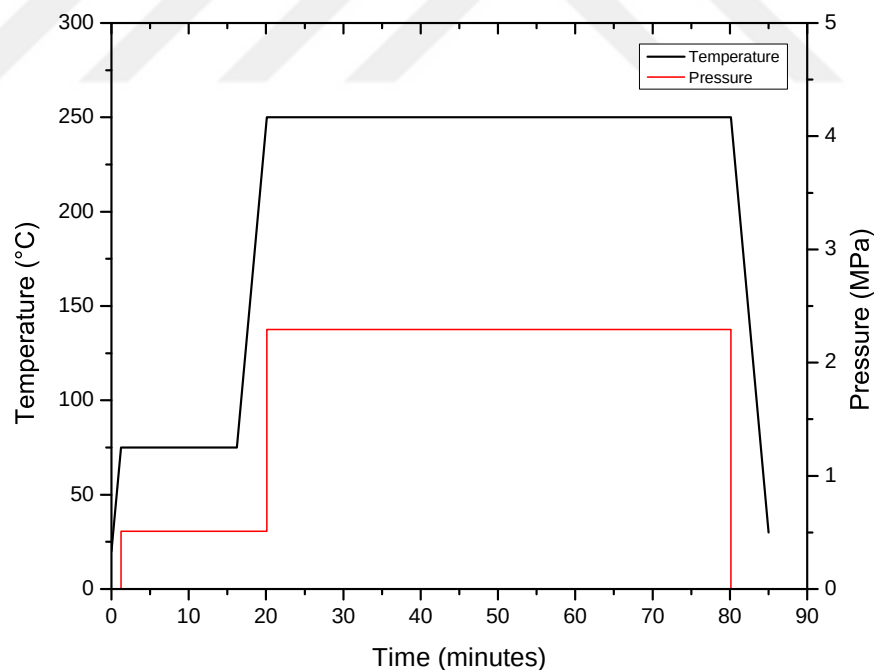


Figure 3.15: Temperature, time, and pressure used for the initial testing

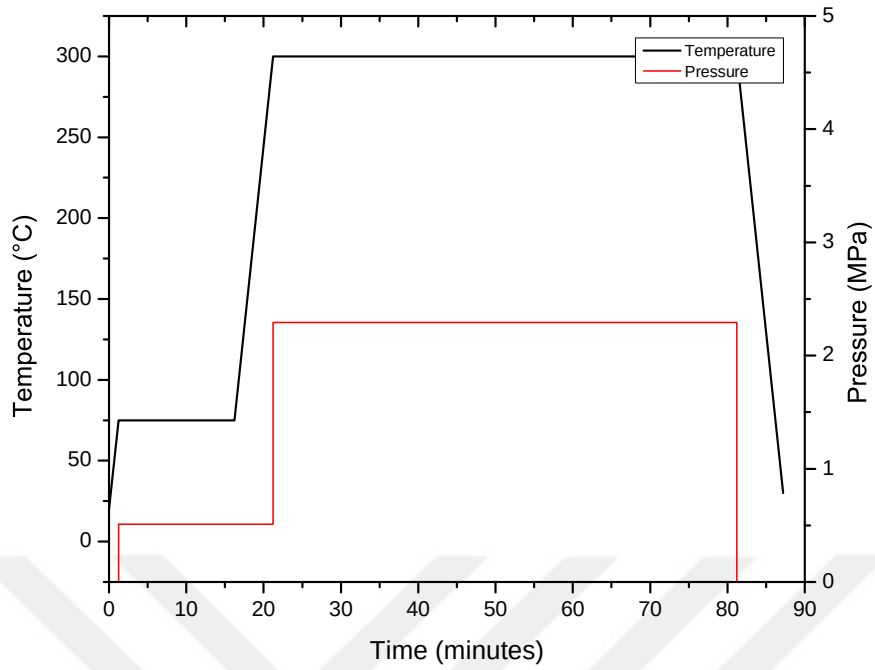


Figure 3.16: Temperature, time, and pressure used for the initial testing

3.3.2 Patterned Wafers

The second part of the experiments was designed to assess the bonding for packaging applications. For that purpose, a design of square bondrings is employed which was previously used at the METU MEMS Center. The layout of the wafer is given in Figure 3.17. The width of the rings is 250 μm , and the sides are 5 mm. The outside of the wafer has a buffer section to increase the effective bonding area. The increase in the area means that lower pressure could be applied, however, the pressure uniformity over the whole wafer is gained with this method. As otherwise, the outside of the wafer would bend and be more susceptible to failure during bonding. For patterned wafers, several bonding profiles were used which are given in Figure 3.18 & 3.19. Silicon and glass wafer pairs were used for the experiments. Two thickness profiles were employed for bonding. Different thicknesses are given below in Table 3.1.

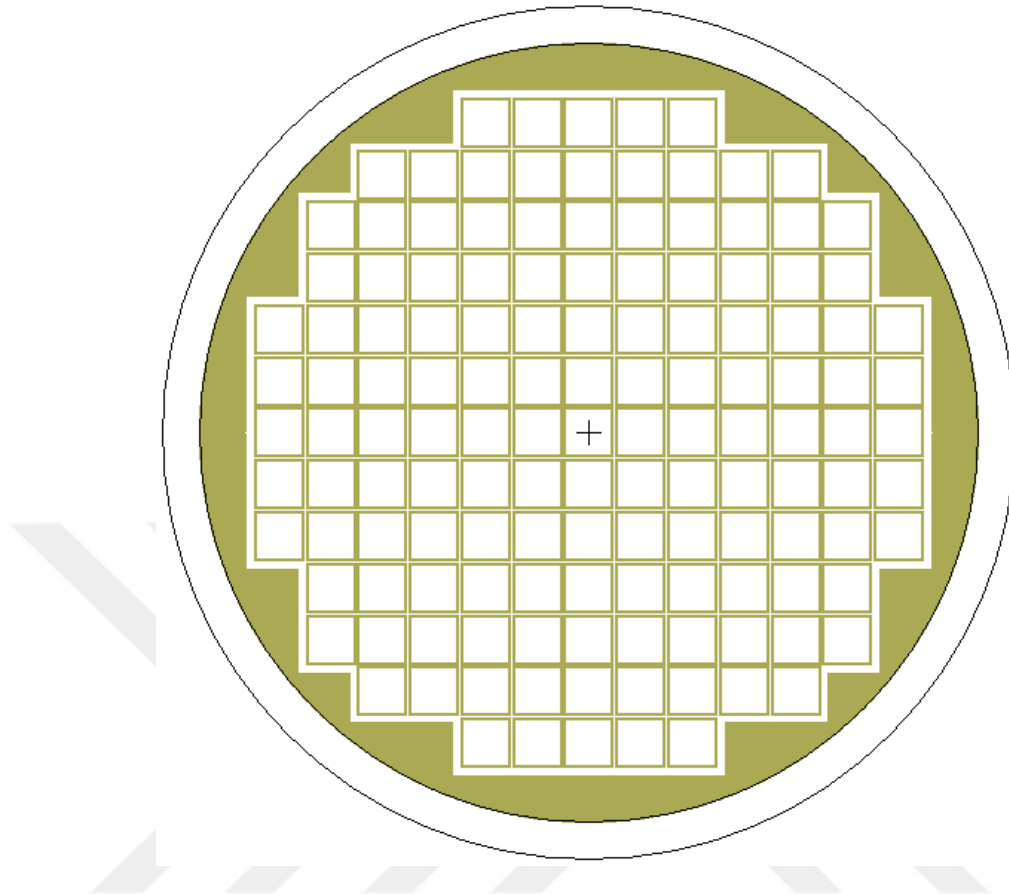


Figure 3.17: Layout of the patterned wafer, coloured parts indicated metallization.

Table 3.1: Table of elements and weight percentages of elements used in patterned bondings.

Bonding at 200°C		Bonding at 250 and 350°C	
Element	Thickness	Element	Thickness
Cu	500 nm	Cu	1 μm
Sn	250 nm	Sn	500 nm
In	250 nm	In	500 nm

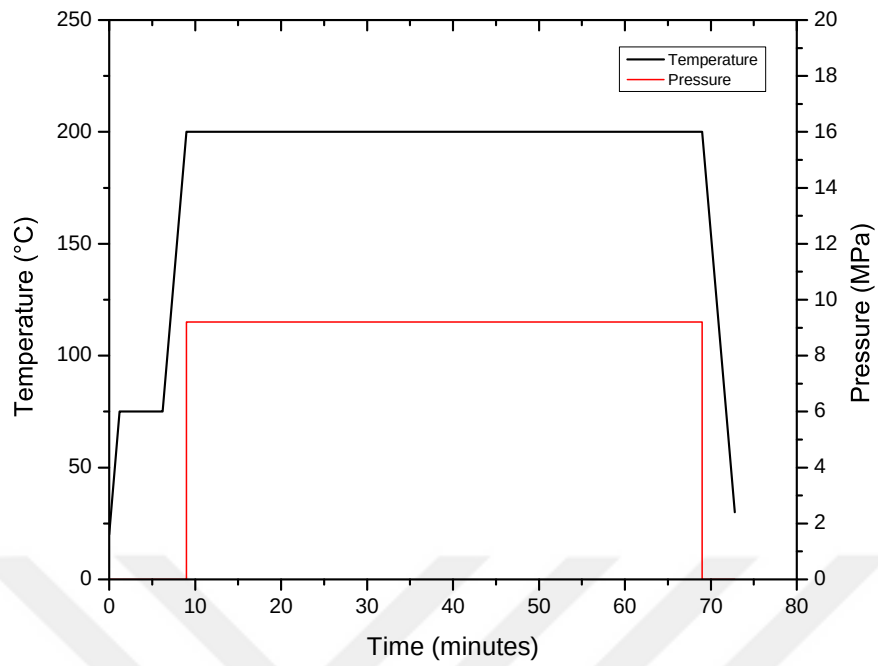


Figure 3.18: Bonding profile of bonding at 200°C.

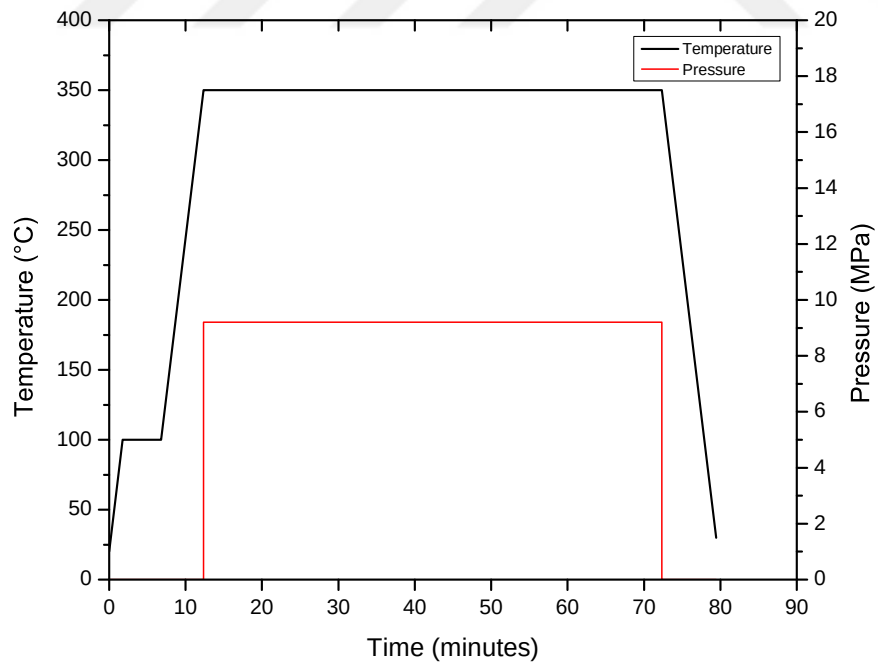


Figure 3.19: Bonding profile of bonding at 350°C.

A thicker variation of the bond stack was used to examine the effect of the amount of material in the bond ring. Temperatures for bonding were chosen between 200-350°C. For all the experiments, the force was kept at 18 kN. For the patterned wafer, the area of bond rings and buffers is 1955 mm². The pressure applied for bonding is then 9.2 MPa. Silicon and glass wafer pairs were aligned using EVG6200, seen in Figure 3.3. Since backside alignment marks are not present on Si-wafers, the alignment was with bottom optics from bond rings. Extensive effort was put into the alignment to limit that pressure non-uniformity.

Alignment is performed by first placing the silicon wafer's device side down and aligning in the X direction. Flags to keep the wafers separated until bonding are brought in, and the glass wafers are placed backside down and aligned in the same way again. After separation is lifted, marks on the glass and silicon wafers are aligned such that they sit on top of each other. Clamps are used to hold the whole fixture together, and the holder is removed from the mask aligner. The fixture is placed on a microscope and examined to ensure that alignment is not off.

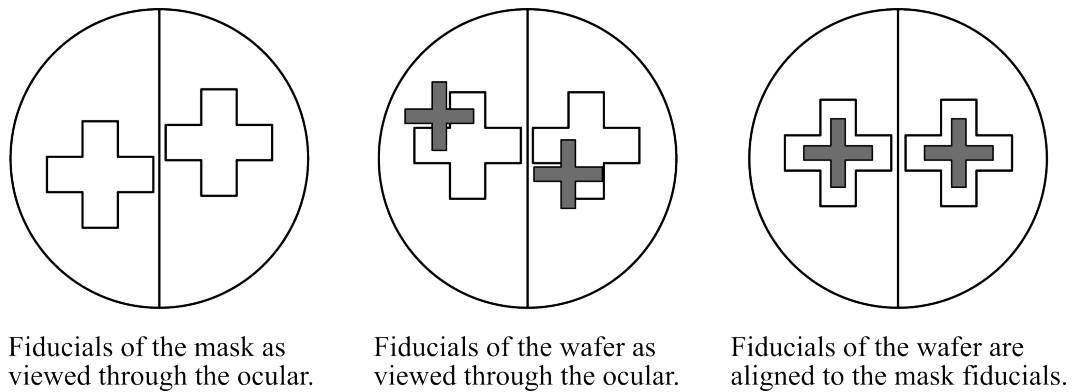


Figure 3.20: Alignment procedure of marks of the mask and wafer within and against each other.

3.4 Characterisation Methods

3.4.1 Scanning Acoustic Microscopy

Scanning acoustic microscopy is used as a method to determine bond integrity without damaging the structure. A PVA-TePla SAM 301HD scanning acoustic microscope is used, which can be seen in Figure 3.22. SAM operates on the principle that sound waves interact with the wafer they propagate through and are reflected back to the transducer. High-frequency sound waves are sent through the wafer via a transducer. Depending on the surface they meet, the amplitude, frequency or phase of the wave is altered. Moving the transducer over the whole surface allows an image to be formed from the collected data. The waves that encounter bond rings or defects are transmitted through with a slight change, whereas they change drastically when going through the cavity. This is visualized in Figure 3.21 below.

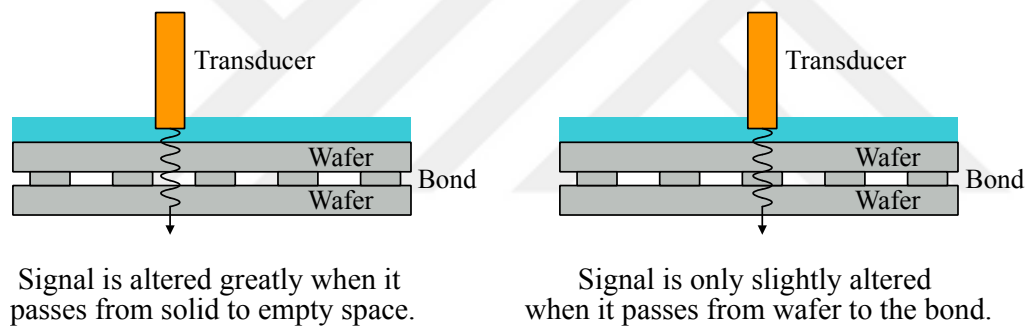


Figure 3.21: Examples of SAM inspections. The change in the wave a) going through the bond rings, b) going through the cavity.

For this thesis, hermeticity is also essential; hence, the wafer pair is submerged in DI water, and a quick scan is taken. Then they are left in the tank for an extended period. The change in the submerged scan is that a third tone is obtained when the waves propagate through the water. If dies are not hermetically sealed, they will have water in them. Two gates are placed to mark the areas of the top and bottom wafers since the waves will also change when they encounter the wafers. The bond ring will appear dark, the cavity without water will appear light grey, and parts with liquid will appear in a medium grey tone. SAM scans to increase quality are set up slower in this

work.



Figure 3.22: PVA TePla 301HD Scanning acoustic microscope.

3.4.2 Shear Testing

Shear testing was performed using a Dage Nordson 4000 Bond Tester as shown in Figure 3.23. Dies are placed against a block with the same thickness as the wafers, and the chisel pushes against the cap part of the chip. Force versus displacement is graphed in the software, and shear strengths are calculated using the maximum force before fracture. Some packages are completely shattered depending on the sample strength, making fracture surface investigation impossible.



Figure 3.23: Dage Nordson 4000 Bond Tester.

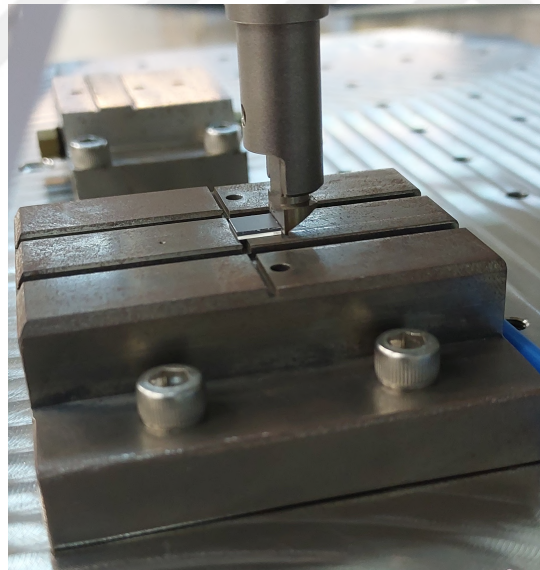


Figure 3.24: View of the shear test of the package during shear testing.

For all packages, at least 10 points are chosen to test shear strength. The shear strength calculation is performed using not the whole area of the cap but the bond area connected with the bottom substrate. The dies have an effective bond area of 8 mm^2 .

3.5 Scanning Electron Microscopy

Scanning electron microscopy makes use of a beam of accelerated electrons to examine samples and to obtain high-resolution surface morphology and texture images. Combining with other detectors, elemental analysis of the samples can also be performed. In this thesis, SEM and EDS are employed to obtain microstructures of the bonds and their compositional analysis. A Hitachi Regulus 8230 SEM and Oxford Instruments EDS are used; both are seen in Figure 3.25



Figure 3.25: Hitachi Regulus 8230 SEM

3.6 Differential Scanning Calorimetry

Differential Scanning Calorimetry or DSC, is a method in which the heat capacity of the material in question is employed. DSC can be applied for a wide range of materials to determine different aspects, such as behaviour in terms of being amorphous or

crystalline, and phase transitions such as melting or solidification. In glasses or polymers, glass transition temperature, as well as curing and degree of cure, is observable via DSC.

DSC uses the heat capacity of the material, which, in short is the amount of heat required to change the temperature of the material by 1°C. Another definition of DSC made by Höhne et al. explains it through the change of the different heat flow rates going in or out of the sample material and the reference material under a known temperature routine[61]. This means that due to the difference in heat capacity of the sample and the reference, even though the heat flow going in is identical. There will be a temperature difference between the two, and the difference in heat absorbed or transmitted gives information about the nature of the change occurring in the sample.

DSC temperature program was chosen to reach a maximum equipment temperature of 550 °C with a heating rate of 10 °C/min. The DSC equipment is seen in Figure 3.26. For each sample, the heating-cooling cycle was performed twice. The doubling of the cycles was to ensure that any reactions obtained during the first heating and cooling are, in fact, melting and solidification.



Figure 3.26: Perkin Elmer Diamond Differential Scanning Calorimetry (DSC).

CHAPTER 4

RESULTS & DISCUSSION

4.1 Unpatterned Wafer Bonding Test

4.1.1 Bonding at 300°C

The sample bonded at 300°C showed a single, primarily uniform layer in SAM images. The dark areas in the Figure 4.1 suggest that bonding took place, as otherwise, the unbonded region would result in a colour gradient. The highlighted defects on the image are contamination that could have occurred at several stages during fabrication. However, their existence helps to distinguish the bonding better. Areas numbered I and II in Figure 4.1 show some of the non-uniform bonding regions.

Several explanations for this are possible; first, during PVD operations, sputtering or evaporation, even with rotating the wafer, some difference in thickness exists between the centre and the outer edges, where the boundaries are slightly thinner than the centre. In that case, the pressure uniformity over the wafer during the bonding operation is non-uniform, which could result in the seen bonding defects. The solution for this problem is applying enough pressure, and when melting occurs, the wafers would be brought closer, and uniformity could be obtained. In this case, the whole wafer area was coated, and the pressure that can be applied is limited.

Shear testing of results of the bonding performed at 300 °C is given in Figure 4.2 below. The average shear strength of the bond was found to be 10.4 MPa; however, there existed a vast fluctuation between the highest and lowest points. The maximum was 39.7 MPa, and the minimum was 1.8 MPa. These changes indicate that the colour changes observed in Figure 4.1 express the presence of distinct phases with varying

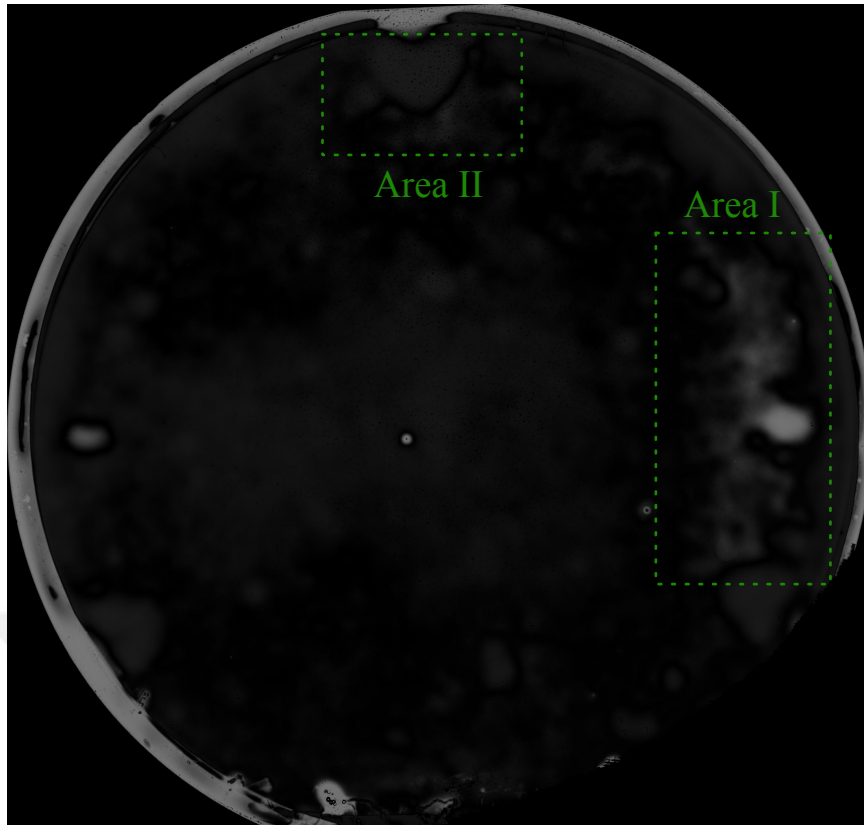


Figure 4.1: SAM image of unpatterned wafer pair after bonding at 300°C

strength values. As mentioned above, the factors that might cause such an issue can be classified as uniformity issues. Yet, for this sample, the centre part giving lower values indicates that another problem interfering with IMC formation must be present.

Another focus would be on the process parameters, as bonding time was chosen as one hour due to the high bonding temperature of 350°C. The non-uniformity over the whole surface could also indicate that there was not enough time for transformation to take place to the final point of the target IMC. To enhance bonding quality without increasing time, higher pressure could be applied when the temperature was kept at 75 °C to allow the temperature gradient to disappear. On a similar note, the temperature of homogenisation could be increased. Instead of keeping the wafers at 75°C the wafers could be heated to just below the melting point of indium. This would allow more diffusion to occur in the solid-state, and when melting takes place, the formation of necessary IMCs occurs more rapidly.

Bonding at 300 °C showed an exothermic reaction at 497.82 °C rather than a melting

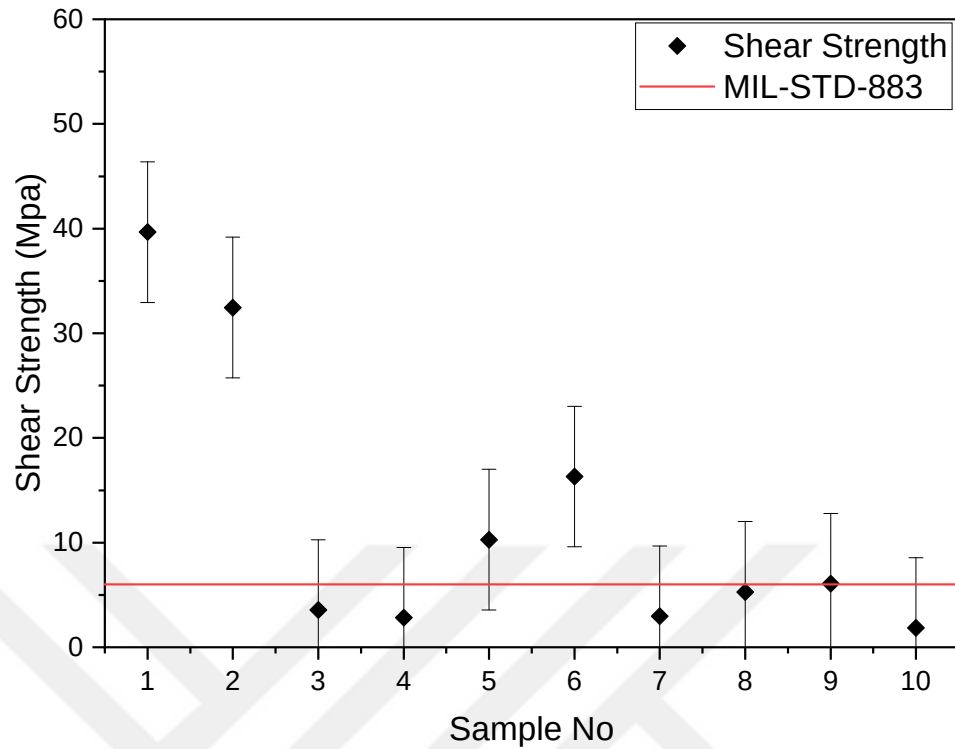


Figure 4.2: Shear strength results after bonding of unpatterned wafers at 300°C for 1 hour.

reaction as expected. Melting is an endothermic process whereas on the DSC curve on 4.3 is an exothermic peak during the first heating of the package. This reaction indicates that crystallisation took place during heating. For the bonding presented in this thesis, crystallisation indicates the formation of IMCs from metals in the bond line. During the second heating and both cooling, no reactions took place, meaning that the bond was completely solid after the formation of IMCs after the first heating. As a result, it is possible to conclude that the bond will not melt up to a temperature of 550 °C, which is the aim of the bonding. The formation of a new IMC does not pose an issue for the reliability of the bond, as no melting was seen in the system. Both of the low melting metals have previously formed IMCs that have higher melting temperatures and stabilised.

Although, high shear values were obtained in this trial, the consistency and yield

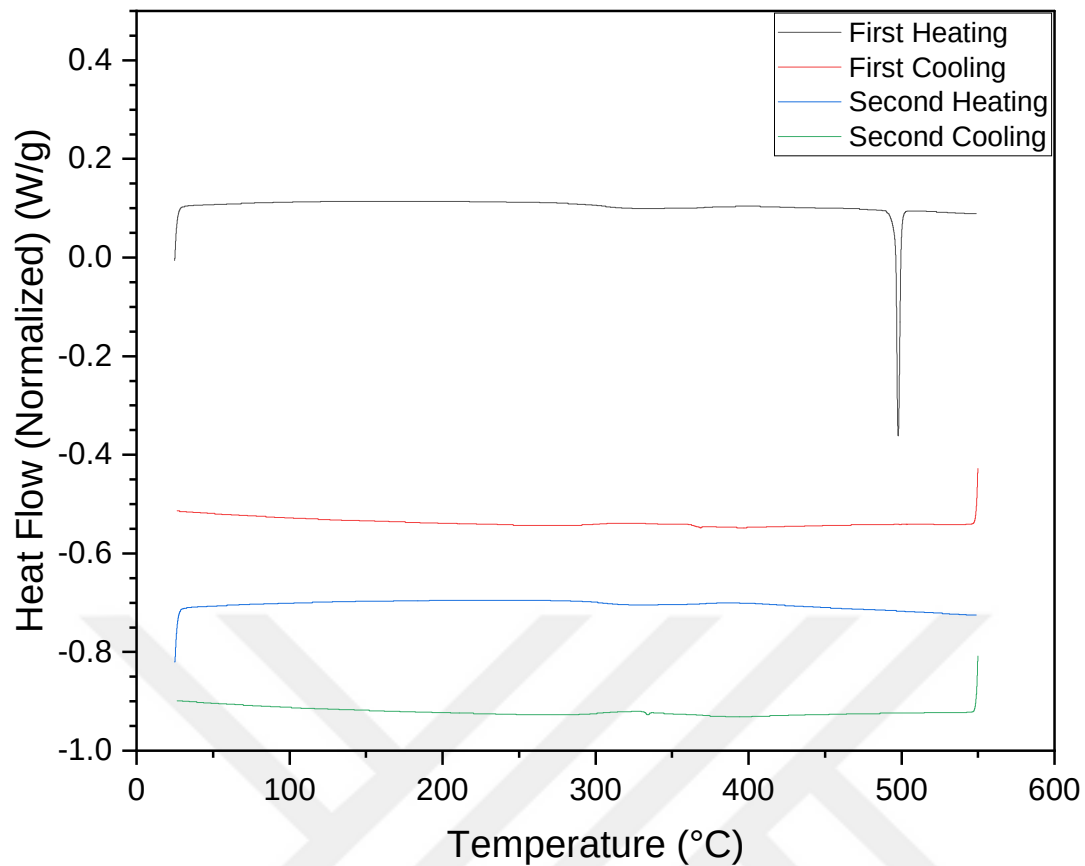


Figure 4.3: DSC results of bonding performed at 300°C

were not satisfying. However, the test revealed that the Cu-Sn-In system was a valid candidate for wafer-level bonding through the TLP method.

4.1.2 Bonding at 250°C

SAM image of the bonding performed at 250°C was similar to the bonding at 300°C. More defects are seen to be present in this bond. The areas closer to the boundaries of the wafer were found to be more defective, as the highlighted parts show that bonding either didn't take place or was insufficient, and water was able to penetrate the bond. The bonding was deemed non-uniform compared to bonding at 300°C, Figure 4.1. The colour gradient in Figure 4.4 indicates that the obtained structure is not the same everywhere, and IMCs could have formed in island-like structures. To summarise, SAM imaging suggests that bonding is taking place, yet the coherency and strength of the bond may differ.

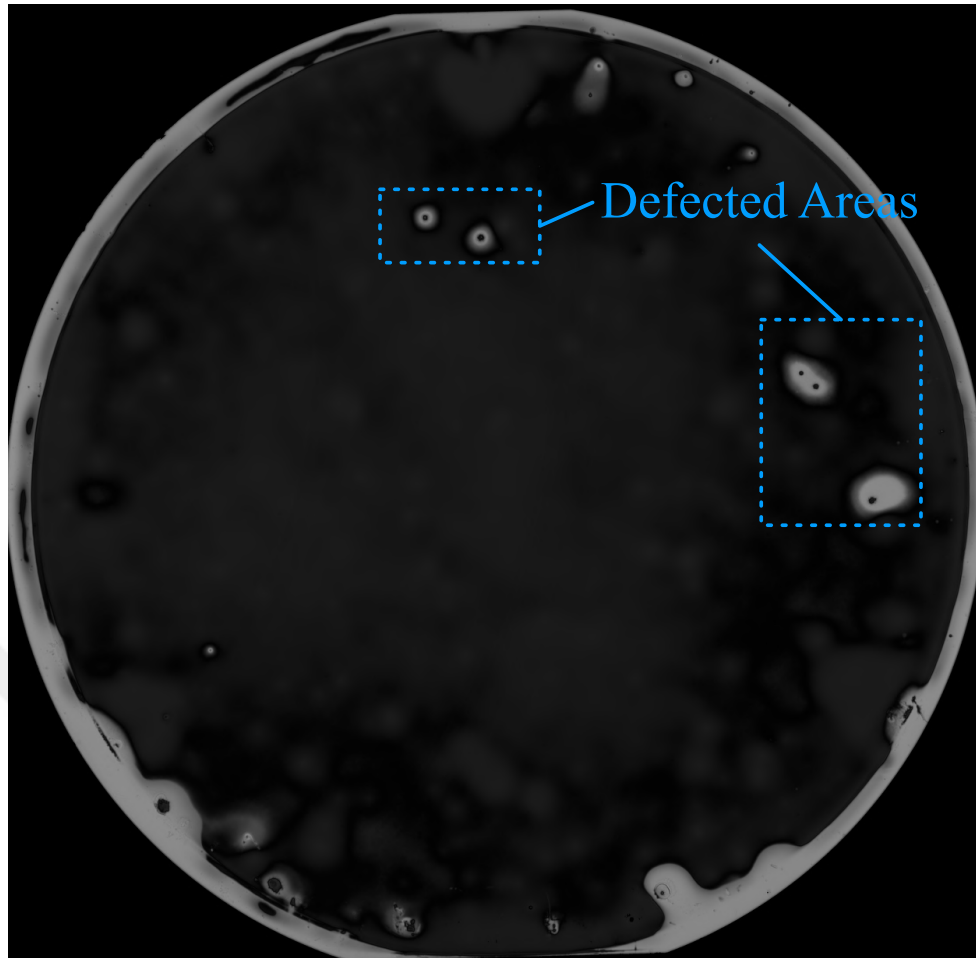


Figure 4.4: SAM image of unpatterned wafer pair after bonding at 250°C

The shear strength results from ten points are given in Figure 4.5 below. The shear strength values are below the military standard of 6 MPa with an average value of 2 MPa. The inadequate shear values regarding the military standards of chip packaging indicate that the results drawn from the SAM image are accurate. The most probable cause for such values is the formation of different phases from the target. Confirmation will be done with SEM/EDS analysis.

The composition in the centre part of the bond, as seen from figure ??, when converted to atomic weight per cent the point is 63.1% Cu, 28.5% In and 8.4% Sn. From the In-Sn phase diagram in Figure 2.16, the indium to tin ratio indicates β phase to be present. The resulting composition on the mid-section of the bond is different from the aimed $\text{Cu}_3(\text{In},\text{Sn})$. The formation of the aimed phase is not complete, which can be explained by two factors that affect bonding: temperature and time, respectively.

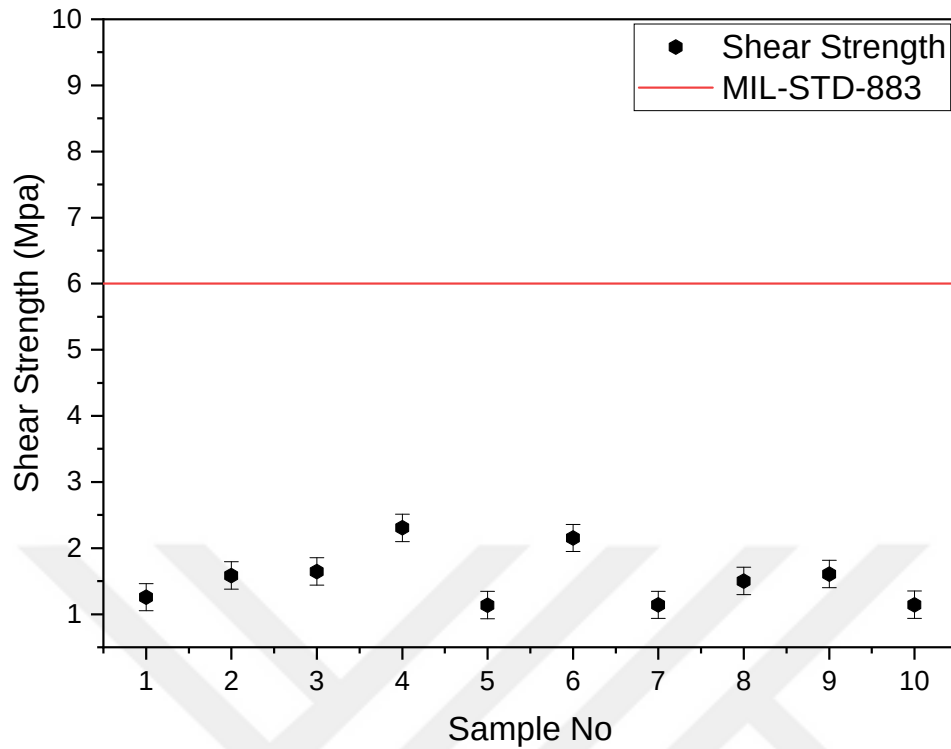


Figure 4.5: Shear strength results after bonding of unpatterned wafers at 250°C.

Increasing the bonding temperature would increase the thermal stress on the wafer, which is not preferable.

The compositional analysis in Figure ?? proves there was not enough time for the diffusion of Cu into the centre parts of the bond. The disproportionate amounts of indium to tin indicate that the eutectic composition for Sn-In was not present. The failure to form $\text{Sn}_{48}\text{In}_{52}$ means that during bonding, instead of melting of the eutectic, the indium would melt and form IMCs with copper. The distribution of elements throughout the bond is seen in Figure 4.6. As with the results above, line analysis shows that the indium and tin have stayed in the middle where some Cu diffused into however, the bond structure is not made of the targeted $\text{Cu}_x(\text{In},\text{Sn})_y$ being sandwiched by Cu on both sides.

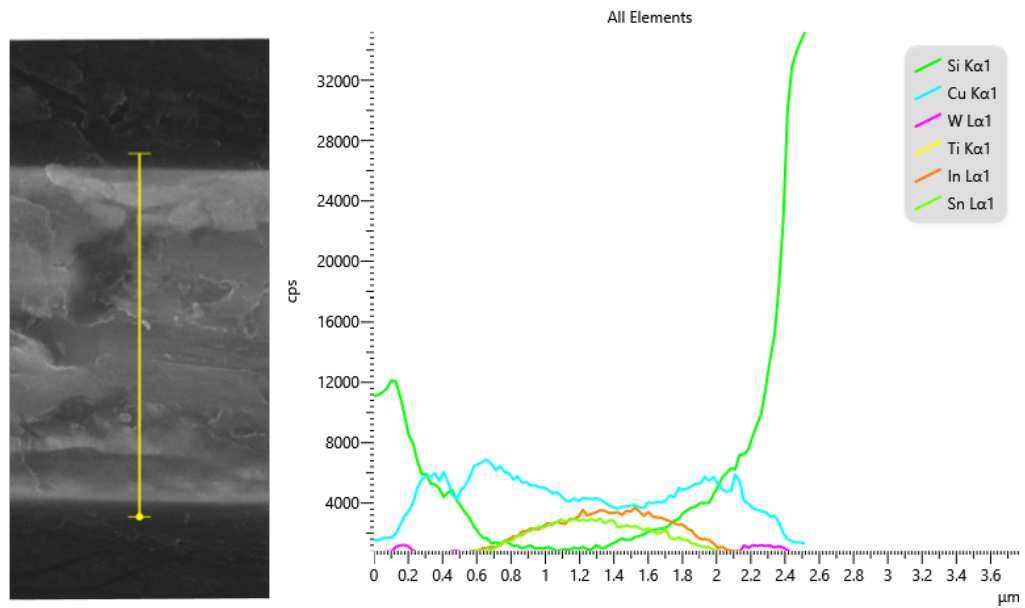


Figure 4.6: SEM image of the bond and EDS line for the sample as bonded at 250°C(left), compositional analysis(right).

The solution inferred from this result was to increase the bonding time further. Allowing for homogenisation to occur just below the melting point of In, and since the diffusivity of In and Sn are higher, they approach their eutectic composition when the temperature uniformity requirements are being fulfilled.

The DSC analysis of the unpatterned sample bonded at 250 °C reveals only a single endothermic peak during the initial heating of the temperature program. The endothermic reaction indicates that a crystallisation reaction took place during the heating, as evident from the breadth and the depth of the peak present in Figure 4.7. This crystallisation is similar to the bonding at 300 °C. The formation of IMC in this sample took place at 504.78 °C. The IMC formation in the sample indicates that the IMC formed during the bonding operation has transformed into a different one during the DSC, which could be considered similar to annealing.

The temperatures of 497°C and 504°C are close enough that the crystallisation during the first heating of both unpatterned samples bonded at 250 °C and 300°C are found to have formed the same intermetallic compound. The fact that during the cooling and

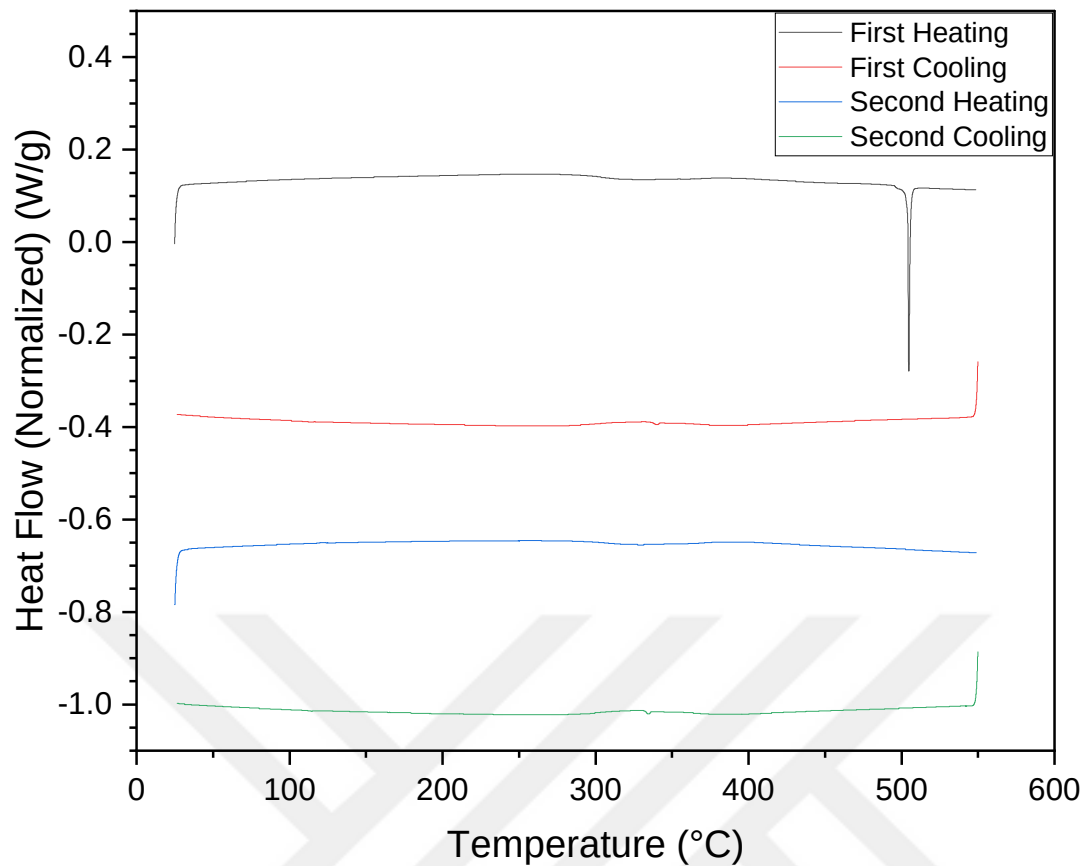


Figure 4.7: DSC analysis of samples bonded at 250°C.

the second cycle, no other reactions took place further proves the point. The melting point of the final bond after bonding at 250°C exceeds both the bonding temperature as designed and the maximum temperature capability of 550°C of the apparatus.

4.1.3 Annealing at 350°C

Shear test results of the sample bonded at 250°C did not meet the MIL-STD-883 requirements on all ten measurement points. Weak bonds were thought to result from insufficient bonding time for the given configuration of relatively thin metals. To mend the situation and investigate if the bond could occur after optimising the process parameters. Ten dies were annealed at 350°C to examine the change in shear strength and give sufficient time for $\text{Cu}_x(\text{In},\text{Sn})_y$ to further advance via diffusion of In and Sn to the IMCs.

After annealing at 350°C for 60 minutes, the shear test on the dies was performed again. A drastic increase in the shear strength was observed as seen in Figure 4.8. This is associated with giving more time for diffusion to occur and allowing homogenisation to take place. Although the kinetics of the reaction have not been studied, the increase in shear strength indicates that the bonding process could be achieved even at lower temperatures when temperature, time, and pressure parameters are balanced. Table ??below summarises the mean strength values after the unpatterned wafer bonding experiments.

Table 4.1

Bonding Temperature	Bonding Force	Median Shear Strength
250°C	18 kN	2.0 MPa
300°C	19 kN	10.4 MPa
250°C	Annealed at 350°C	45.2 MPa

Next, SEM and EDS data from the cross-sections of the bonds will be examined; for both wafer pairs, a cross-section examination was performed. For the pair bonded at 250°C and annealed at 350°C, the compositional analysis revealed that the bond line consisted of 66.3 wt. % Cu, 18.7 wt. % In and 15 wt. % Sn. Converting to atomic weight per cent shows that the bond line consists of $\text{Cu}_3(\text{In},\text{Sn})$. The indium and tin ratios are consistent with the eutectic composition of $\text{Sn}_{48}\text{In}_{52}$. Figure 4.9 below shows the bond line, and Figure 4.10 shows the colour map of the elements present in the bond.

After annealing, Figure 4.10 shows that the bond consists of copper, indium, and tin dispersed evenly over the whole area. In and Sn migrated outwards and bonded with Cu to form the targeted IMCs. From Figure 4.10, the effect topography of the bond is also seen. However, the results of all three elements are consistent with each other. The change from the as-bonded state is clearly seen in Figure 4.10. The elements that have not had enough time to diffuse into each other are dispersed over the bond. This homogeneous dispersion indicates that the bonding reached the last stage with the required IMCS.

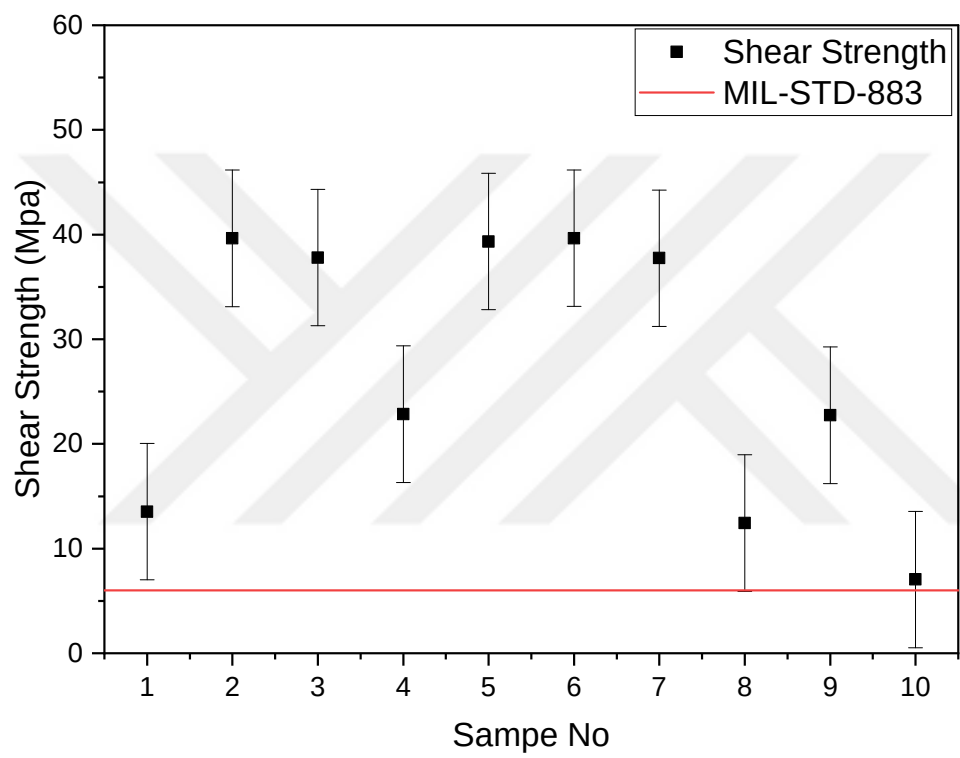


Figure 4.8: Shear test results after annealing at 350°C

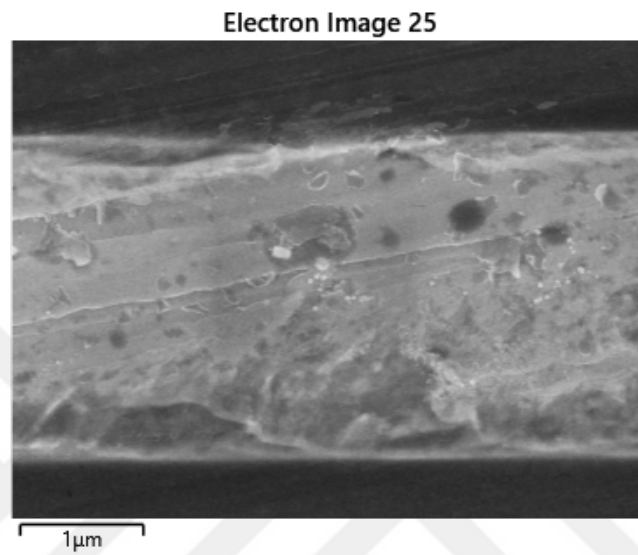


Figure 4.9: SEM image of the bond after annealing at 350°C.

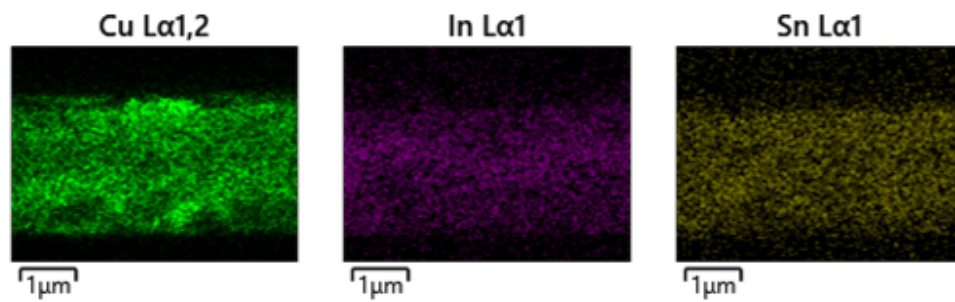


Figure 4.10: Three constituting elements and their colour maps from EDS.

4.2 Patterned Wafer Bonding Tests

4.2.1 Bonded at 200°C

The first bonding was performed at 200°C which was chosen to be different from the initial bonding temperatures of 250°C and 300°C. Keeping the bonding force at 18 kN, the bonding pressure comes out as 9.2 MPa. This pressure increase is considered sufficient to allow bonding at lower temperatures. The metal stack selection for this bonding process was 500 nm Cu, 250 nm Sn, and 250 nm In. The oxidation barrier was once again gold with a thickness of 25 nm.

The SAM image of the wafer after bonding is given in Figure 4.11. It is clear from the SAM that the bond is incomplete. For starters, the buffer ring of the wafer has only formed bonds in several areas highlighted with green in the Figure 4.11. There also existed incomplete bonds in all four quadrants of the wafer.

Shear testing of the sample bonded at 200°C couldn't be performed as the glass wafer broke during the dicing operation. This indicates that the bonds were weak. During dicing, the blade moves to cut the wafers; however, since two wafers are poorly bonded. The glass wafer moves with the force of the blade and shatters as a result. This outcome is expected when dicing starts from unbonded regions of the given SAM image in Figure 4.11. After the glass broke, the rest of the wafers separated perfectly from each other. Such a separation showed that bonding had not taken place at all, most probably due to bonding at a lower temperature with insufficient time for diffusion.

Another theory that explains the non-uniformity is related to the EVG 520 wafer bonder. Application of pressure non-uniformly will lead to sluggish diffusion in such areas. However, the effect of temperature in such a case is much greater than the pressure non-uniformity. For this bonding to be effective, further process optimizations are required. Increasing the soak time and temperature would increase the initial diffusion and, therefore, make the liquid formation easier. Allowing the liquid to form at the start of the designated process temperature increases the success of the bonding.

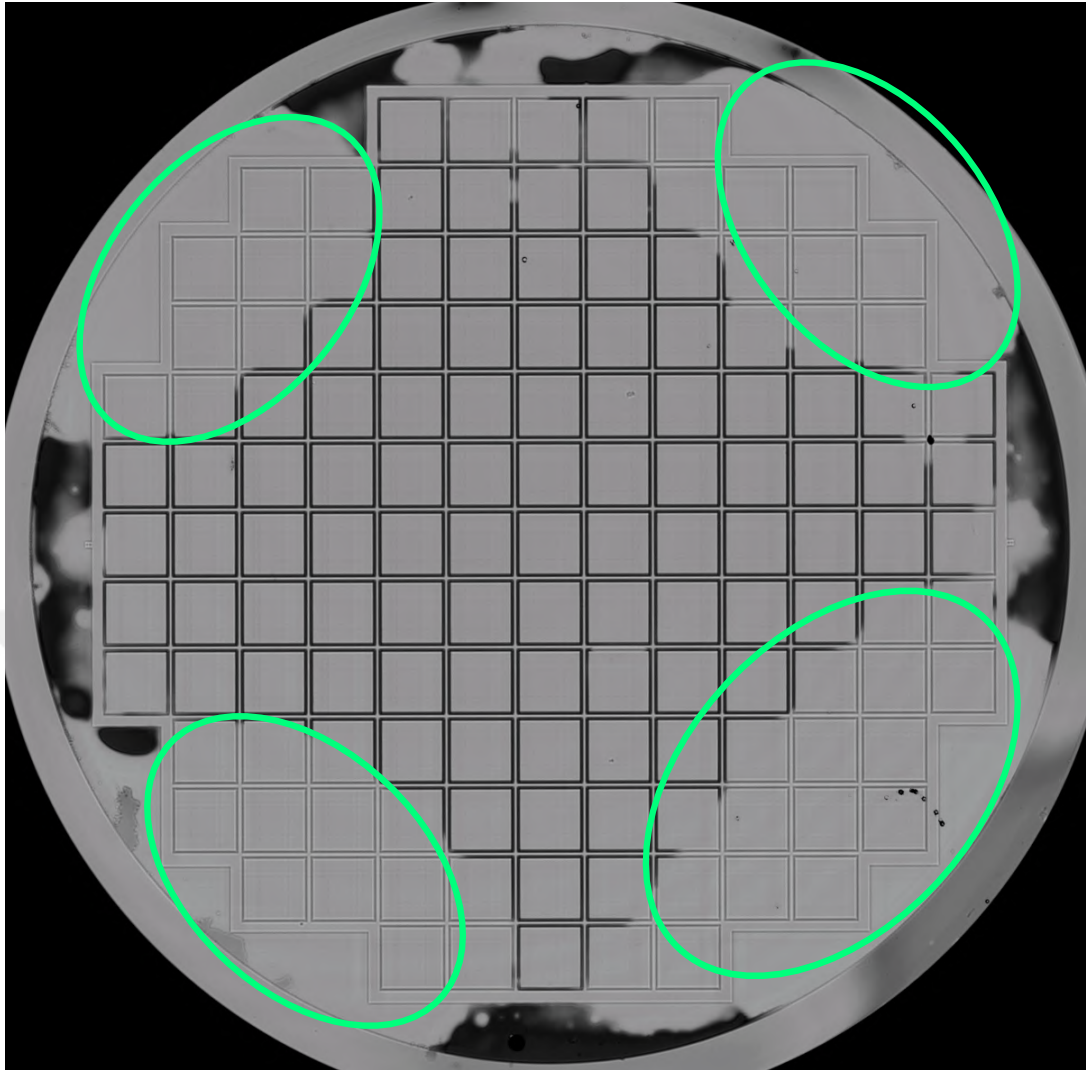


Figure 4.11: SAM image of bonding performed at 200°C.

4.2.2 Bonded at 350°C

The second bonding with the stack of 500-250-250nm design was done at a high temperature, 350°C, for several reasons. The gold layer to prevent oxidation after evaporation of the indium was not coated. High temperature and high pressure were then employed to break the oxide layer on top physically during bonding.

SAM images in Figure 4.12 show that bond rings, as well as the buffer area, have bonded successfully in terms of leakage and more significant defects. Discontinuities in the bond do not exist. After the initial fast scans, the wafer pair was submerged for two days. There are a few areas in the buffer region where the bond is inconsistent and

complete. These problems are due to the alignment marks and defects that occurred during the handling of the wafer. The circular gradient present in the left half of the wafer pair is thought to be due to the bowing that took place during bonding. The quality of bonds for individual dies was identical in SAM imaging.

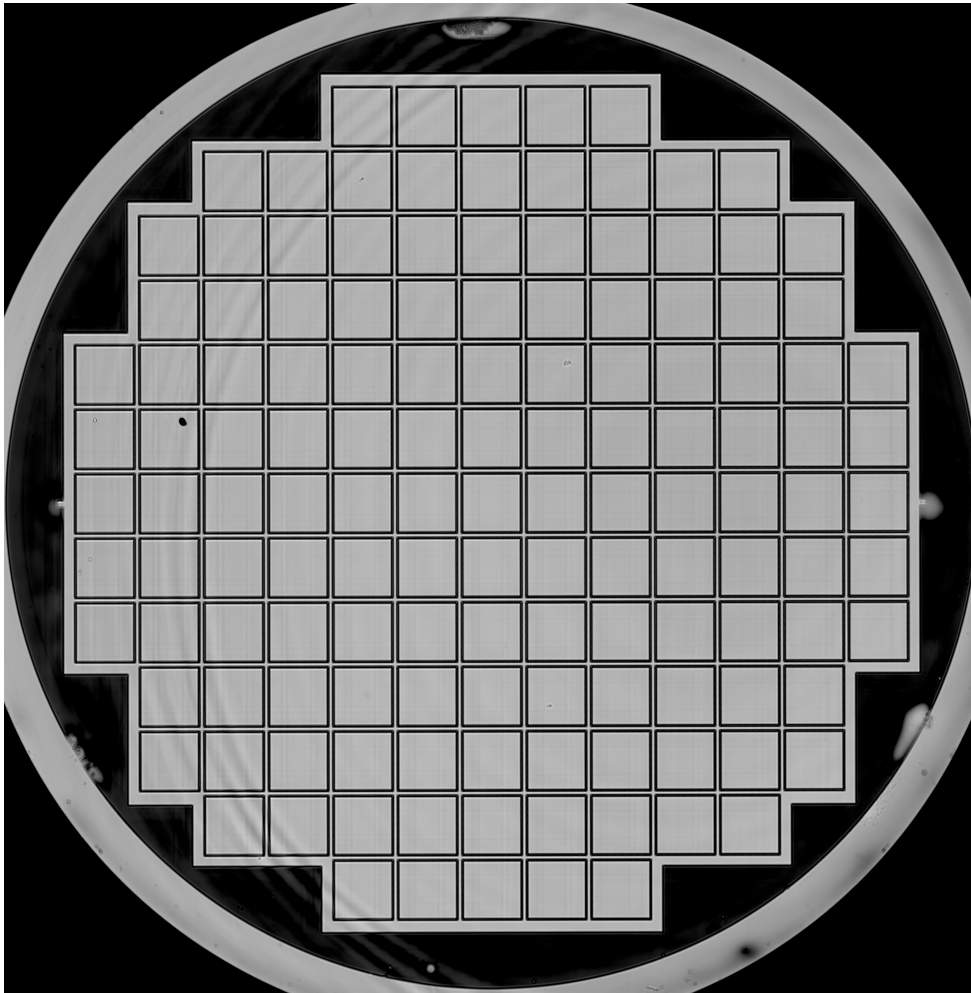


Figure 4.12: SAM image of bonding performed at 350°C.

Shear testing of the sample was done from 10 spots, starting from the centre and going outwards. The selected dies were tested with their glass side down at the start. However, reversing the placement revealed a change in the shear strength values. The increase in shear strength values was due to the bond being more robust than the glass, and by military standards, the fractures of the substrate are not counted towards the strength of the bond. The mean shear strength was 19.1 MPa with a standard deviation of 4.9 MPa. The distribution of strength values per sample is given in Figure 4.13. The

shear values obtained from bonding at 350 °C indicate that the bonding is achieved adequately at high temperatures.

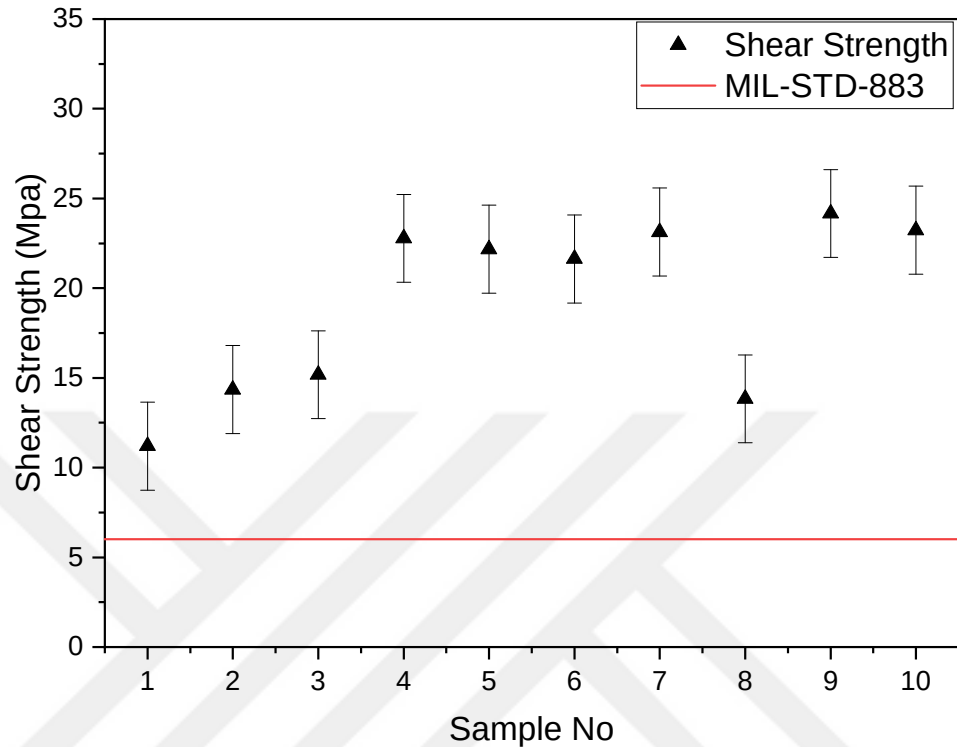


Figure 4.13: Shear strength results after bonding of patterned wafers at 350°C for 1 hour.

DSC analysis of the samples bonded at 350 °C are presented in Figure 4.14. The analysis shows the presence of an endothermic reaction taking place at around 480°C. The endothermic reaction that could take place within the confines of the experiment is only melting. Following the first heating, during the cooling and the second cycle, any reactions, neither endothermic nor exothermic, were not observed. However, the lack of reactions after the first heating indicates that the reaction taking place may have been partial melting of a combination of remaining metals.

Partial melting after bonding at higher temperatures indicates that a eutectic phase formed during the heating, which leads to partial melting. During the second heating, no reactions were observed in the sample, which affirms the belief that the melting

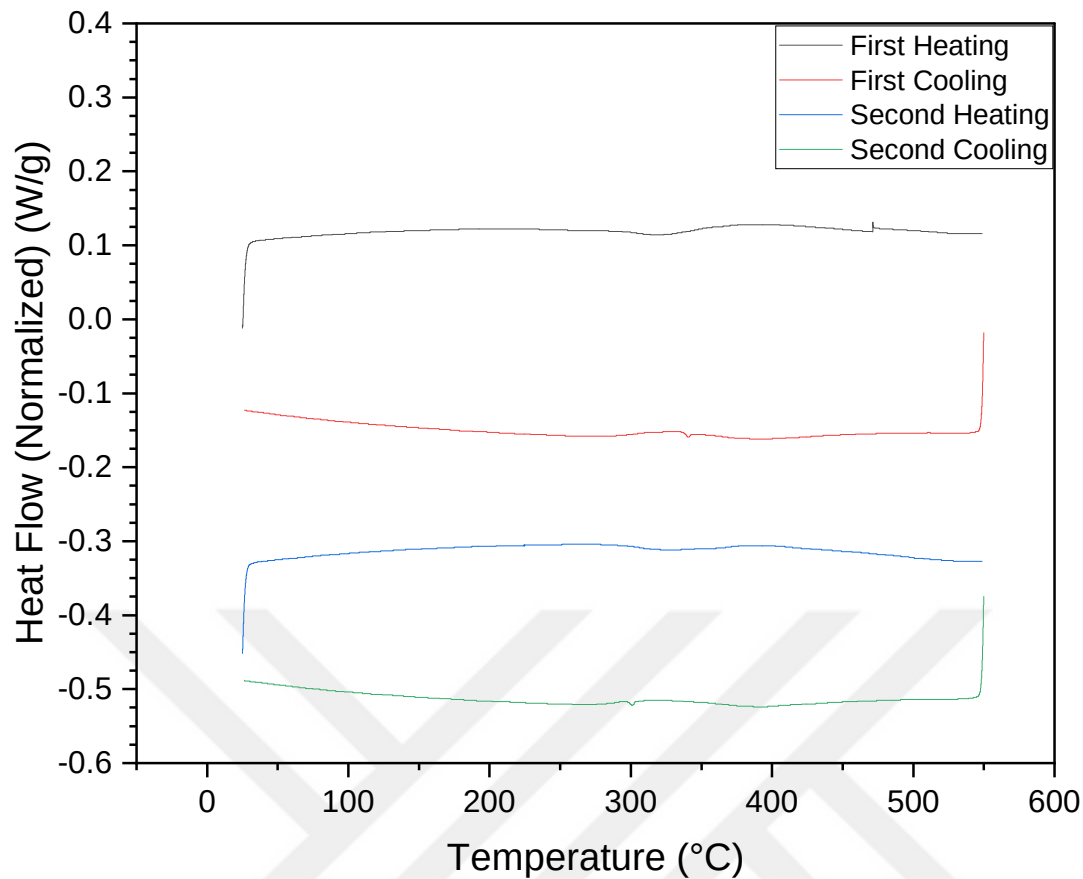


Figure 4.14: DSC analysis after bonding at 350°C.

is partial. To establish the correct relation, namely to ensure that the reaction was not stemming from squeeze-out, a second sample from the same wafer was also subjected to DSC analysis, the result of which is seen in Figure 4.15. A similar result was obtained after the second DSC with a slight change in the reaction temperature from 480°C to 450°C. The difference in the melting temperature indicated that the melting resulted from a partial melting where the compositional changes lead to liquid formation at different temperatures depending on the phase diagram of the system.

From the fracture modes mentioned in the literature review, the fracture mode was found to consist of cohesive failure of the substance. The cracks that formed during dicing would propagate further during shear testing. When the dies were placed such that the chisel would push on the glass, which was previously affected by dicing, the shear strength increased. This explains why how the dies were placed affected the overall shear strength values.

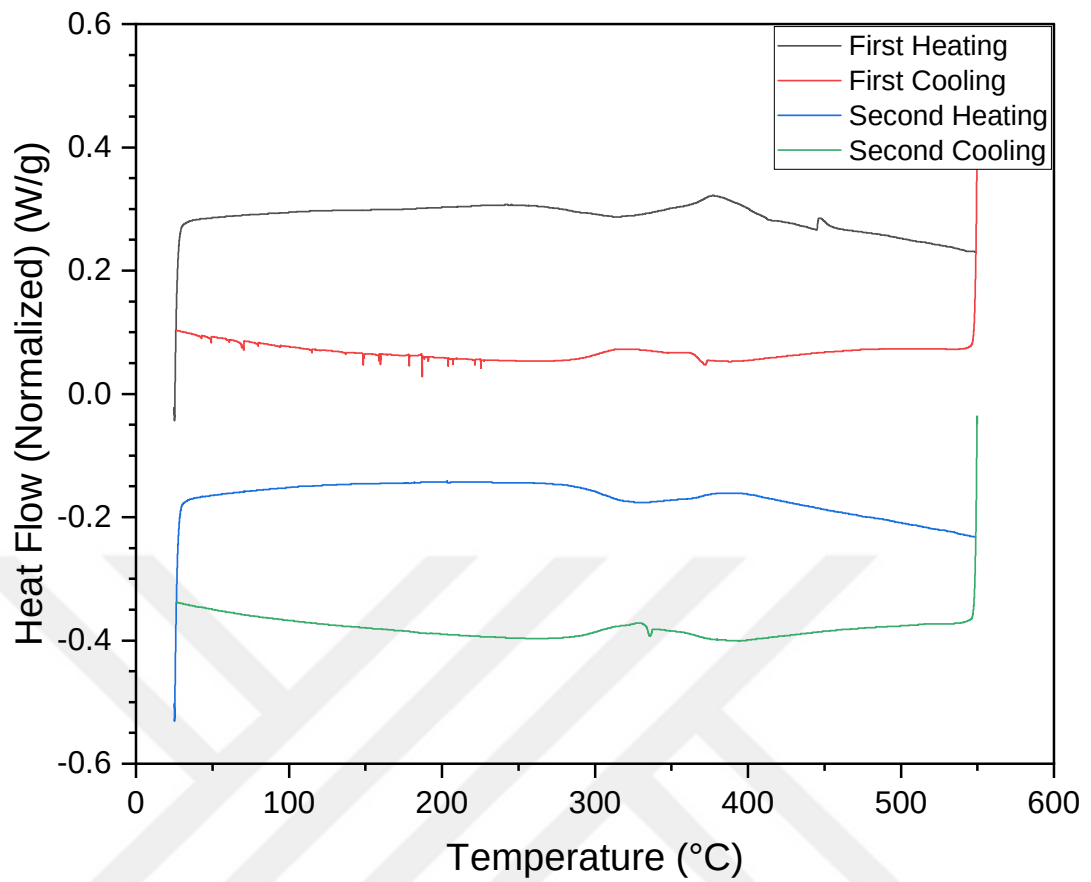


Figure 4.15: Second DSC analysis after bonding at 350 °C.

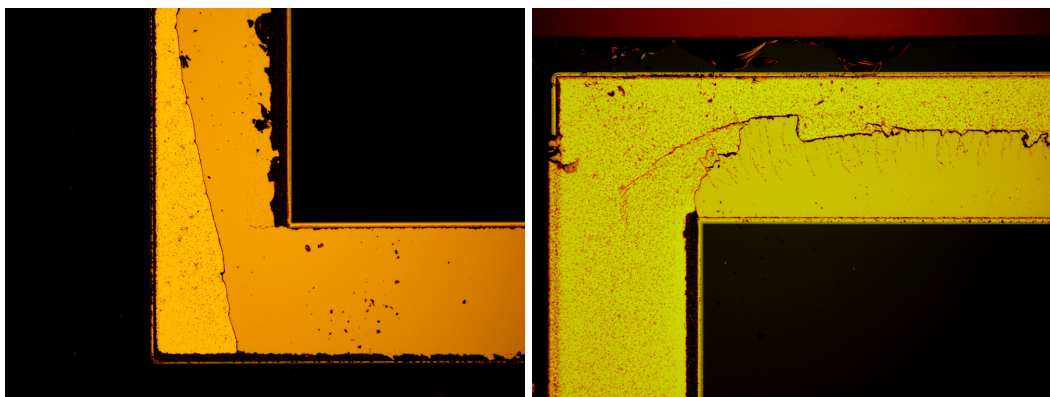


Figure 4.16: Microscope image of the fracture surface after shear testing. Glass substrate (left) and silicon substrate (right).

4.2.3 Bonded at 250°C

The SAM image of the whole wafer is seen in Figure 4.17. The bonding is uniform throughout the area except for deformities at the alignment marks. The dies and the wafer as a whole do not show water penetration even after being submerged for at least 48 hours. There still exists an arc over the wafer that is seen on the SAM image. This is thought to be originating from the bending of the top glass. However, the arc seen in the image does not contribute negatively to any aspect of the bonding.

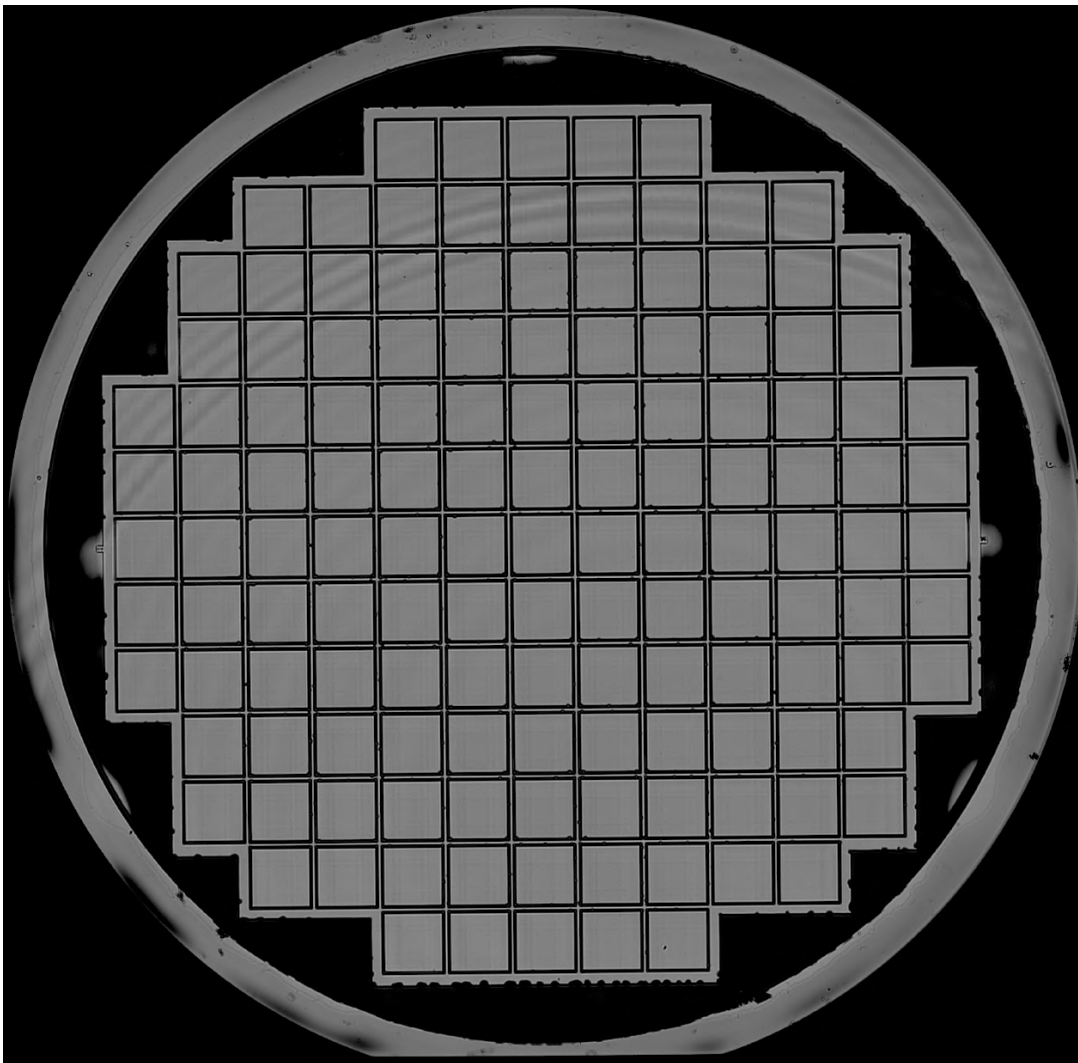


Figure 4.17: SAM image of bonding performed at 250°C with thicker metallisation.

On closer inspection of the dies, some defects were found, as seen in Figure 4.18. There is a squeeze-out visible from the edges of the dies. The reason for squeeze-out

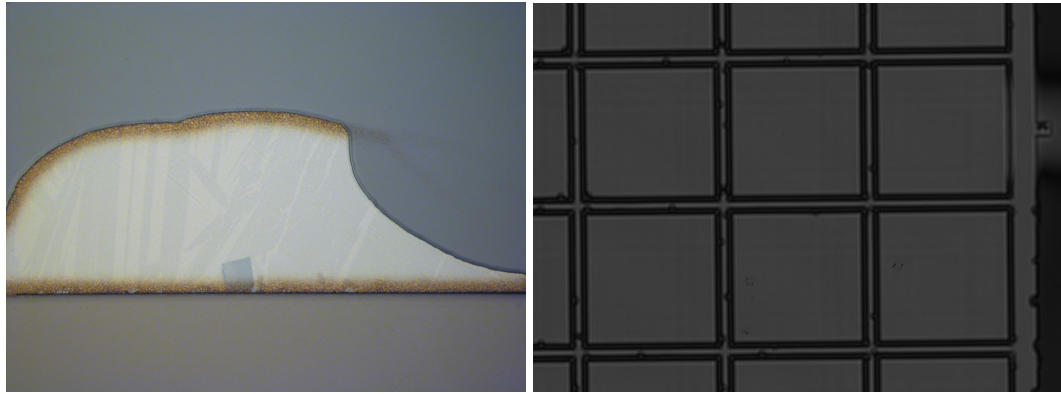


Figure 4.18: Close up of the SAM image of dies near the right alignment mark.

in this pair is thought to be from the thickness of the metals. In previous trials, the combined thickness of tin and indium was $0.5\ \mu\text{m}$, whereas in this setup, the low melting metal thickness was $1\ \mu\text{m}$, which is distributed equally. The amount of liquid in the bond line after melting has increased, and the pressure was kept the same as before, $9.2\ \text{MPa}$. This results in the liquid being pushed out during isothermal solidification as the interface is the part where IMCs are forming at the start. The microscope view of the squeeze-out is seen in Figure 4.18. The leaked metal is a combination of tin and indium.

Excessive amount of squeeze-out may lead to structural defects in the bond and hinder its reliability over its service life. Reducing the squeeze-out can be done in multiple ways. The most common method is decreasing the pressure of the bonding operation. However, lowering the pressure too much impacts the formation of IMCs through sluggish diffusion; hence, process optimizations must be done to maximize pressure while keeping the squeeze-out to a minimum.

Shear testing was performed the same way as the previous testing, such that the silicon sides were placed down and the chisel pushed the glass part. The shear strength values are shown in Figure 4.19. The average shear strength is $8.5\ \text{MPa}$, which satisfies the military standards. The standard deviation was found to be $1.5\ \text{MPa}$. Bonding at $250\ ^\circ\text{C}$ yielded lower shear strength values; however, the consistency of the values has improved. Significant outliers in the data are not present.

However, compared to the wafers bonded at 350°C there is a significant change in

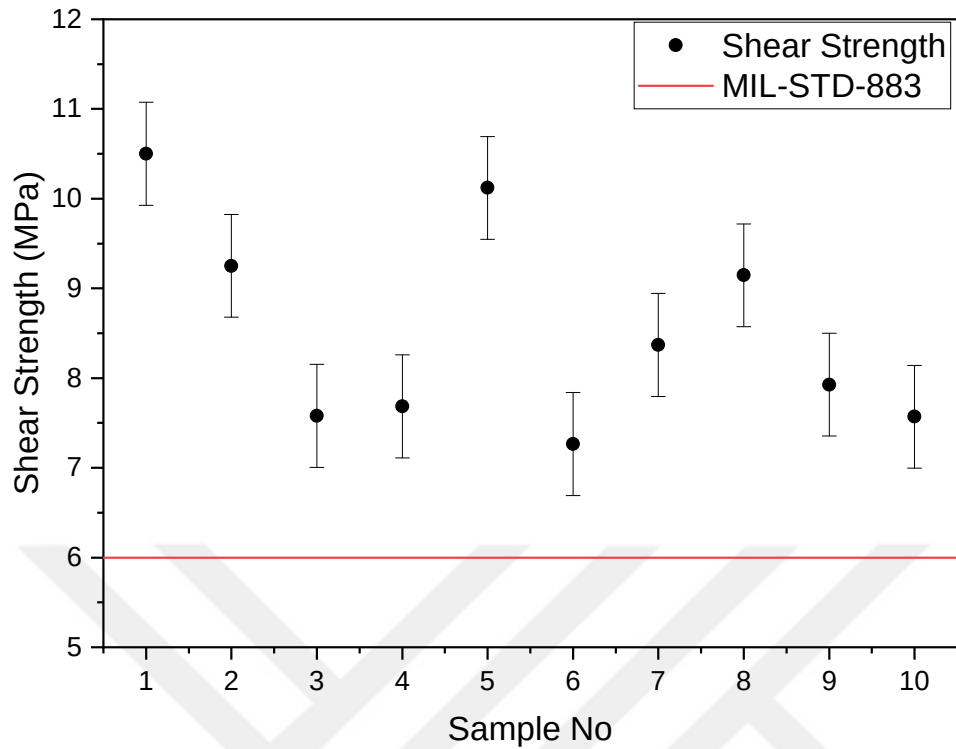


Figure 4.19: Shear strength results after bonding of patterned wafers at 250°C for 1 hour.

the shear strength. Considering the EDS results of the samples annealed at 350°C to be the target IMC for Cu-Sn-In bonding. The values show that the transformation to the target IMC has not taken place. Two possible reasons are put forth to explain this. First, the thicker variation of metals used in the bond design required more time for bonding to occur as diffusion paths are increased. The second explanation is the gold oxidation barrier used in the process preventing diffusion when AuIn IMCS has formed in the top layers of both wafers. The analysis of the fracture surfaces further advances this theory. The SEM image of the silicon die is seen in Figure 4.20.

From SEM imaging, two different fracture surfaces are observed. Compositional analysis reveals that the surface is 95 wt % Tungsten. The composition of the adhesion layer was $\text{Ti}_{10}\text{W}_{90}$. Hence, the fracture mode is identified as an interfacial fracture between the adhesion layer and the bond. However, the area where this mode

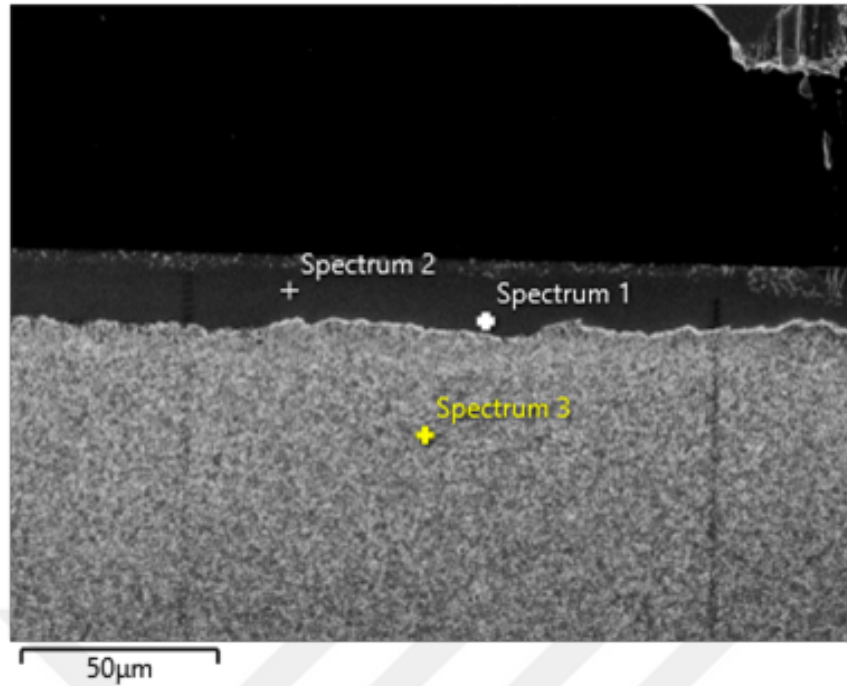


Figure 4.20: SEM image of the fracture surface.

of fracture is seen is minuscule. To prevent this kind of fracture, a different adhesion layer could be employed, such as Ti and Cr. The properties of the coated TiW also matter. During a lengthy coating in a sputtering system, the wafer heats up as the temperature rises on the substrate, and the uniformity and structure of the TiW start to change. This problem is resolved by allowing the substrate to cool down by coating in cycles instead of a lengthy single deposition.

Spectrum 1		Spectrum 3	
Element	Weight %	Element	Weight %
W	94.1	In	55.5
C	3.4	Au	35
Si	1.6	C	2.7
O	0.9	Cu	2.7

Table 4.2: Table of elements and weight percentages of elements in Figure 4.20

The principal fracture surface reveals that the surface contains indium and gold, as seen in Table 4.2. The presence of gold and indium indicates that the fracture has

occurred right between the cap and device chips. The total thickness of gold where the two wafers meet for bonding is 40 nm; this thickness would not hinder bonding. However, during the time till bonding, gold and indium would mix even at room temperature to form AuIn IMCs. These intermetallics could then act as an interface which the fracture is facilitated from. The same intermetallic when formed at room temperature, may dampen the diffusion of species into each other during bonding and, therefore, hinder the mixing of liquids.

Table 4.3: Table of shear strengths of the tested samples according to their processing temperatures.

Sample	Mean Shear Strength (MPa)
Bonded @ 200°C	NA
Bonded @ 250°C	8.5
Bonded @ 350°C	19.1

DSC analysis of the sample bonded at 250°C indicates that the melting temperature of the bond is above the limit of the DSC apparatus. There existed no reactions in during both heatings and coolings as seen in below Figure 4.21. This indicates that IMC formation that was seen in samples bonded at 350°C. The difference stems from the processing temperature of the wafer stack prior to bonding. To ensure bonding quality, the soaking time of the wafer prior to heating was increased from 5 minutes to 15 minutes. The increased time allowed the temperature uniformity over the metal stack to increase and the solid-state diffusion was given more time. Meaning that the IMC formation took place readily at 250°C. Bonding at 250°C yielded a package that can sustain temperatures upto 550°C without melting.

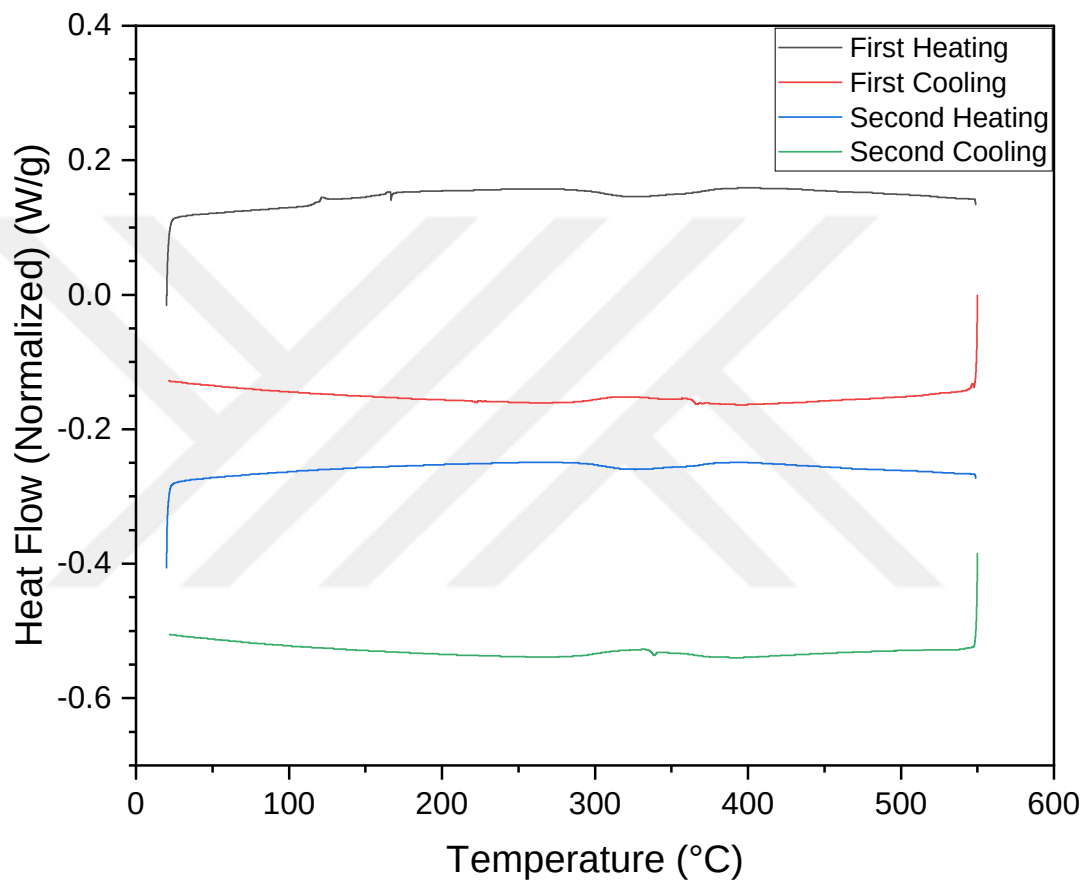


Figure 4.21: DSC analysis of patterned wafer after bonding at 250 °C.



CHAPTER 5

CONCLUSION & FUTURE WORK

The Cu-Sn-In ternary material system has been investigated for low temperature wafer-level vacuum packaging of MEMS-devices. Several advantages of ternary systems exist for packaging of devices. First of all, the temperature requirements required for bonding are less demanding due to In-Sn eutectic compared to binary systems in which the liquid formation depends on the low melting metal such as Sn. Secondly, problems such as sluggish diffusion can be solved with the additional element. Lastly, all the metals(Cu,Sn, and In) are CMOS-compatible. The main disadvantage of the ternary TLP bonding is that the complexity of the system. Number of IMCs increase and kinetics of their formation are not well-known.

Initial experiments revolved around proving that bonding is taking place in the system as designed. The aim was to substitute the Sn in Cu-Sn system with an eutectic combination of In,Sn. Wafers were deposited with the metals using sputtering and evaporation on wafers without any patterning to assess the bonding potential. The thicknesses of Cu, Sn, and In were 500 nm, 250 nm, and 250 nm, respectively. Keeping the number of parameters to a minimum, symmetrical bond designs were used. Bonding at two different temperatures, 250°C and 300°C were performed. The First group resulted in dies with an average shear strength of 2 MPa and the second group ended up with an average shear strength of 10 MPa. The low shear strength was suspected to be resulting from process parameters. Confirmation was done by annealing the dies at 350°C for an hour. Annealing increased the shear strength values to an average of 30 MPa.

The following experiments aimed to establish a usable package for electronic devices was performed using a bonding with dimensions of 5 mm x 5 mm with a width of

250 μm . The metal thicknesses deposited with the same methods were 1 μm , 500 nm, and 500 nm for Cu, In, and Sn, respectively. Three different bonding procedures were employed. The lowest bonding temperature of 200 °C showed promising results in SAM imaging; however, the wafer pair broke during the dicing operation, indicating that the bonding resulted in residual stresses due to the CTE mismatch between glass and silicon wafers. Bonding at 250°C with a pressure of 9.2 MPa yielded a mean shear strength value of 8.5 MPa. The wafer showed significant squeeze-out, which means that the pressure for bonding operation could be lowered. The fracture analysis revealed that the fracture occurred between the interface where the two metal stacks meet and consist of gold and indium. From DSC analysis the melting temperature of the bond in the package was found to be over 550°C which satisfies the temperature conditions for CMOS packaging which has a processing temperature limit of 400°C

Bonding at 350°C with the same layout and metal thicknesses was performed to evaluate the effect of temperature on the bonding. The higher bonding temperature yielded a higher shear strength of 19.1 MPa, as expected. The more the species are allowed to diffuse the more they approach to the theoretical IMC of $\text{Cu}_3(\text{In}, \text{Sn})$. The combination of the IMC with the sandwich of Cu leads to higher strength values. There was partial melting taking place during DSC analysis between 450—480°C. Although partial melting causes the package to lose its function, the high temperature at which the reactions takes place the package is viable for use in service or the bond is successful as above 400°C is outside the working conditions of the device.

As a continuation of this study, the vacuum performance of the packages can be investigated using He-leak testing and cap deflection methods. Another important follow up would be to test the lowest theoretical bonding temperature. Bonding below the melting point of indium is possible according to the phase diagrams. Design of such a process can lower the bonding temperature further to allow packaging to be performed with a lower disadvantage in terms of heat input to the devices. Squeeze-out that was observed should be a topic a topic of interest in the future as well. Process optimizations in terms of soak temperature, bonding temperature, and pressure profile can solve this issue. Instead of constant pressure, alternating pressure profile at critical times can be helpful to preventing liquid squeeze-out during bonding.

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