

DOKUZ EYLÜL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED
SCIENCES

FILTERS WITH ACTIVE TUNING FOR
SWITCHED-MODE CONVERTERS

by
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February, 2007
İZMİR

FILTERS WITH ACTIVE TUNING FOR SWITCHED-MODE CONVERTERS

**A Thesis Submitted to the
Graduate School of Natural and Applied Sciences of Dokuz Eylül University
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in Electrical and Electronics Engineering**

**by
Seyhan MUTLU**

February, 2007

İZMİR

M.Sc. THESIS EXAMINATION RESULT FORM

We certify that we have read this thesis "**FILTERS WITH ACTIVE TUNING FOR SWITCHED-MODE CONVERTERS**" completed by **Seyhan MUTLU** under supervision of **Prof. Dr. Haldun KARACA** and that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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ABSTRACT

In this thesis Switched-Mode Power Converters basic's, output voltage ripples are analyzed and control feedback loop between the resonant filter network and switching circuit is provided by using Phase Locked Loop (PLL).

There are more effective ripples on Switching-Mode Power converters according to linear converters. The ripples can be reduced by adjusting low pass filter cut off frequency below the fundamental harmonic ripple. But this state may not provide exact attenuation. In this thesis resonant filters are designed as additional to the low pass filter. If the switching frequency is selected equal with resonant frequency an important attenuation is provided at fundamental harmonic frequency.

To provide an effective attenuation resonant filter network must be stay on resonance frequency. The operating conditions or component tolerances sometimes cause the missing attenuation of resonant filter. In this study the feedbacks control is designed by Phase Locked Loop to avoid this state. With the feedback loop the switching frequency is controlled as a resonance frequency and continuous ripple attenuation is provided.

In this thesis, resonant networks models, Switched Mode Buck Converters and PLL control loop for switching circuit are simulated by using MATLAB and B2 Spice.

This study shows the necessity and importance of PLL circuit. If the switching frequency changes from resonance frequency, output voltage ripples amplitude increasing rapidly.

Keywords: Switched Mode Power Converters, Resonant filter, Phase Luck Loop, Resonator.

ANAHTARLAMALI GÜÇ KAYNAKLARINDA REZONANS FİLTRENİN AKTİF OLARAK TUTULMASI

ÖZ

Bu çalışmada Anahtarlama güç kaynakları, çıkış gerilimindeki dalgalanmaların filtrelenmesi ve rezonans filtrelerin Faz kilitleme devresi(PLL) ile kontrol edilmesi incelenmiştir.

Anahtarlama güç kaynaklarında çıkış gerilimindeki dalgalanmalar doğrusal dönüştürücülere oranla genelde daha yüksektir. Tasarım aşamasında kesim frekansı temel harmonik frekansının altında olan bir alçak geçiren filtre seçimi ile dalgalanmalar belli seviyede giderilebilmektedir. Bu tez çerçevesinde alçak geçiren filtreye ek olarak belirli frekanslarda filtreleme gerçekleştirmek için rezonans filtreleme işlemi tasarlanmıştır. Anahtarlama frekansı rezonans frekansına eşit seçildiğinde temel harmonik frekansında önemli bir zayıflatma sağlanmaktadır.

Rezonans devresinin etkin olarak filtreleme gerçekleştirmesi için sürekli olarak anahtarlama frekansının rezonans frekansına eşit olması gerekmektedir. Çalışma koşulları ya da malzemelerin toleransları rezonatörlerin tasarlanan frekansı yakalayamamasına ve gerekli zayıflatmaları yapamamasına neden olabilmektedir. Bu durumu engellemek için tez çerçevesinde faz kilitleme devresi (PLL) ile kontrol işlemi gerçekleştirilmiştir. Bu şekilde anahtarlama frekansının sürekli rezonans frekansına eşit olarak kalması ve tasarlanan harmoniklerin zayıflatılması sağlanmıştır.

Simülasyon programıyla anahtarlama güç kaynağı, rezonans devresi ve rezonans devresinin faz kilitleme devresi ile kontrol modelleri gerçekleştirilmiştir.

Yapılan çalışmada PLL devresinin gerekliliđi de gör÷lmektedir. Anahtarlama frekansı rezonans frekansından uzaklaştıđında çıkıřtaki dalga(ripple) genlikleri de hızla artmaktadır.

Anahtar sözcükler: Anahtarlama Güç kaynakları, Rezonans Filtre, Faz Kilitleme Devresi(PLL), Rezonatör.

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CHAPTER ONE

INTRODUCTION

DC-DC converters are electronic devices used whenever it is aimed to change a DC supply voltage efficiently from one level to another. They are needed because unlike AC, DC can not simply be stepped up or down by using a transformer. In many ways, a DC-DC converter is the DC equivalent of a transformer.

The power supply technology can really be divided into two distinct forms firstly, the linear or series regulator and secondly the switched-mode conversion technique. Linear power supplies were the mainstay of power conversion until the late 1970's when the first commercial switch-mode became available. Now apart from very low power wall mount linear power supplies used for powering consumer items like cell phones and toys, switch-mode power supplies are dominant(Anonymous,2002).

Switched mode power supplies (SMPS) present an important subject of power electronics. They are used for conversion, conditioning and control of electrical power. There is an increasing demand for SMPS in computer, telecom, automotive and domestic applications. In all of these applications the aim is to change the DC energy from one voltage level to another, while wasting as little as possible in the process. In other words, we want to perform the conversion with the highest possible efficiency (Anonymous, 2002).

A SMPS offers three main advantages over a conventional linear power supply:

- 1) High efficiency & less heat generation
- 2) Tighter regulation,
- 3) Smaller size and weight

Of these, greater efficiency is the biggest advantage.

Conventional “linear” power supplies are inefficient because they regulate by dumping the excess power in to heat. The AC power transformer, operating at 60 Hz,

also contributes to the inefficiency of some power supplies. When all the inefficiencies are added, conventional, linear power supplies are typically 40- 50% efficient, while switchers have efficiencies from 60 to 90%. This is very important when the designer wants to reduce generated heat, reduce power costs, or increase battery life.

Another key benefit of a SMPS is their ability to closely regulate the output voltage. Switchers adjust for changes in input voltage or load current, with little change in efficiency. Switch mode supplies regulate continuously, and follow load changes almost immediately. In addition, switchers have the unique ability to maintain the correct output under low input voltage conditions. In fact switchers can actually produce an output voltage that is higher than the DC voltage applied to the input.

A final advantage of switchers is their relatively small size and weight. Because switchers operate at high frequencies, the parts are physically smaller than those needed for a conventional, 60 Hz power supply of the same power rating. The transformers, capacitors and coils are both physically smaller and lighter. This makes them ideal for use in portable equipment.

In other words an SMPS design can produce very compact and lightweight supplies. This is essential requirement for the majority of electronic systems.

Although the benefits of switched-mode techniques are great, there is a penalty paid in the increased noise present at both input and output of the supply due to the power switching techniques (Cyril, 1993). Also the associated control circuitry is much more complicated than its linear counterpart. In this project our aim is dealing with this state.

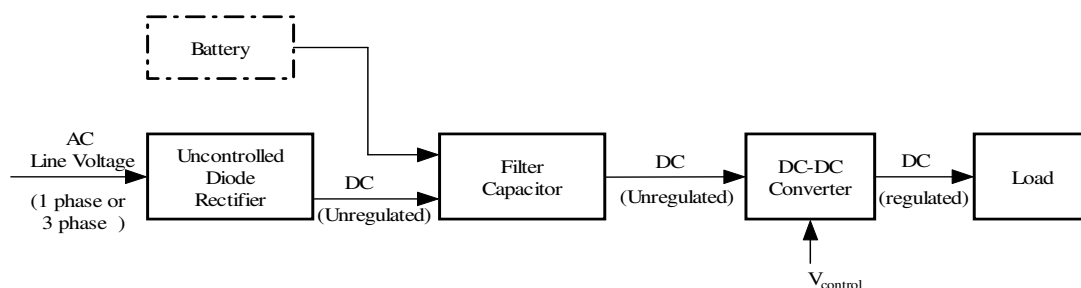


Figure 1.1 A typical block diagram for a SMPS

CHAPTER TWO

SWITCH MODE CONVERTER TOPOLOGIES

There are many different types of DC-DC converter, each of which tends to be more suitable for some types of application than for others. For convenience they can be classified into various groups. For example some converters are only suitable for stepping down the voltage, while others are only suitable for stepping it up; a third group can be used for either.

Another important distinction is between converters which offer full dielectric isolation between their input and output circuits, and those which don't. Needless to say this can be very important for some applications, although it may not be important in many others (R. Erickson, 1998).

DC-DC converters are used with an electrical isolation transformer in the DC power supplies, and without an isolation transformer in case of dc-motor drives. In this project, only the non-isolated converters are considered, since the electrical isolation is an added modification. The following dc-dc converters are discussed in this chapter:

1. Step-down (buck) converter
2. Step-up (boost) converter
3. Step-down/ up (buck-boost) converter
4. Cuk converter
5. Full-bridge converter

Of these five converters, only the step-down and the step-up are the basic converter topologies. Both the buck-boost and the Cuk converters are combinations of the two basic topologies. The full-bridge converter is derived from the step-down converter.

2.1 Non Isolating Converters

The non-isolating type of converter is generally used where the voltage needs to be stepped up or down by a relatively small ratio (say less than 4:1), and there is no problem with the output and input having no dielectric isolation (Keng, 2005). Examples are 24V/12V voltage reducers, 5V/3V reducers and 1.5V/5V step-up converters. There are five main types of converter in this non-isolating group, usually called the buck, boost, buck-boost, Cuk and charge-pump converters. The buck converter is used for voltage step-down/reduction, while the boost converter is used for voltage step-up. The buck-boost and Cuk converters can be used for either step-down or step-up, but are essentially voltage polarity reversers or inverters as well. (The Cuk converter is named after its originator, Slobodan Cuk of Cal Tech University in California.). The charge-pump converter is used for either voltage step-up or voltage inversion, but only in relatively low power applications (Pressman, 1998).

2.2 Buck Converter

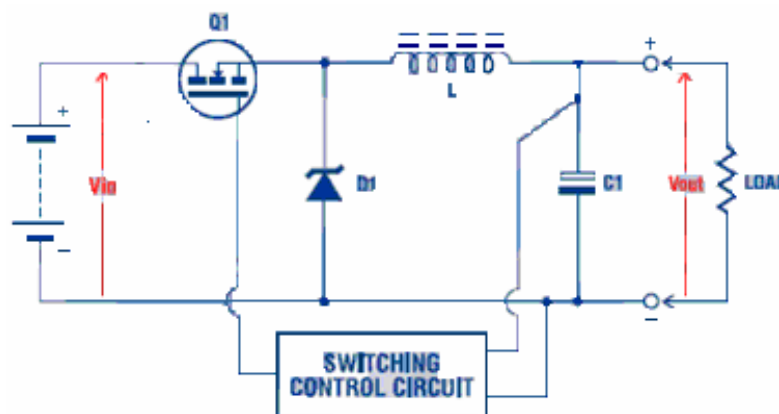


Figure 2.1 A Buck converter circuit

The basic circuit configuration used in the buck converter is shown in Fig.2.1. As you can be seen there are only four main components: switching power MOSFET Q1, flywheel diode D1, inductor L and output filter capacitor C1. A control circuit (often a single IC) monitors the output voltage, and maintains it at the desired level

by switching Q1 on and off at a fixed rate (the converter's operating frequency), but with a varying duty cycle (the proportion of each switching period that Q1 is turned on). When Q1 is turned on, current begins flowing from the input source through Q1 and L, and then into C1 and the load. The magnetic field in L therefore builds up, storing energy in the inductor with the voltage drop across L opposing or bucking part of the input voltage. Then when Q1 is turned off, the inductor opposes any drop in current by suddenly reversing its EMF, and now supplies current to the load itself via D1. Without going too deeply into its operation, the DC output voltage which appears across the load is a fraction of the input voltage, and this fraction turns out to be equal to the duty cycle. So we can write:

$$V_{out}/V_{in} = D \quad (2.1)$$

$$V_{out} = V_{in} \times D \quad (2.2)$$

Where D is the duty cycle, and equal to T_{on}/T , where T is the inverse of the operating frequency (Keng, 2005). So by varying the switching duty cycle, the buck converter's output voltage can be varied as a fraction of the input voltage. A duty cycle of 50% gives a step-down ratio of 2:1, for example, as needed for a 24/12V step-down converter. How about the current ratio between output and input? Well, not surprisingly that turns out to be the reciprocal of the voltage ratio. Ignoring losses for a moment, and assuming our converter is perfectly efficient. So a quick rule of thumb is (Keng, 2005).

$$I_{out}/I_{in} = V_{in}/V_{out} \quad (2.3)$$

So when we are stepping down the voltage by 2:1, the input current is only half the value of the output current. Or it would be, if it were not for the converter's losses. Because real-world converters aren't perfect the input current is typically at least 10% higher than this.

2.3 Boost Converter

The basic boost converter is no more complicated than the buck converter, but has the components arranged differently in order to step up the voltage.

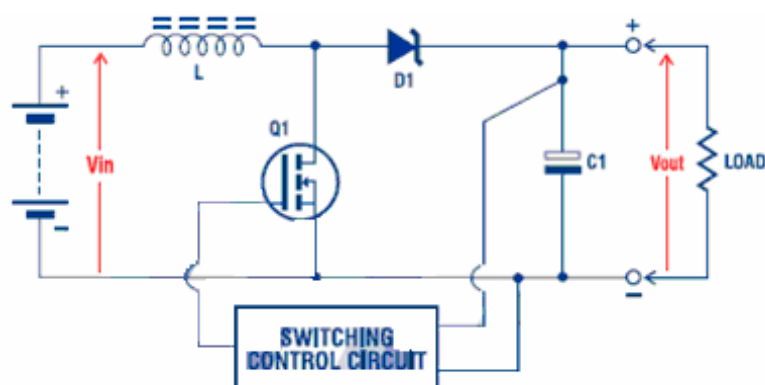


Figure 2.2 the basic circuit for a Boost converter, which uses virtually the same components but arranged to step the voltage up rather than down. This time the voltage ratio depends on the proportion of the time that Q1 is off.

The operation consists of using Q1 as a high speed switch, with output voltage control by varying the switching duty cycle. When Q1 is switched on, current flows from the input source through L and Q1, and energy is stored in the inductor's magnetic field. There is no current through D1, and the load current is supplied by the charge in C1. Then when Q1 is turned off, L opposes any drop in current by immediately reversing its EMF. So that the inductor voltage adds to (i.e., .boosts.) the source voltage and current due to this boosted voltage now flows from the source through L, D1 and the load, recharging C1 as well. The output voltage is therefore higher than the input voltage, and it turns out that the voltage step-up ratio is equal to:

$$V_{out}/V_{in} = 1/(1-D) \quad (2.4)$$

where 1-D is actually the proportion of the switching cycle that Q1 is off, rather than on. So the step-up ratio is also equal to (Vithayathil J., 1995):

$$V_{out}/V_{in} = T/T_{off} \quad (2.5)$$

It can be found that in this converter a 2:1 step-up ratio is achieved with a duty cycle of 50% ($T_{on} = T_{off}$), while a 3:1 step-up needs a duty cycle of 66% (Pressman, 1998). Again, if it is assumed that the converter is 100% efficient the ratio of output current to input current is just the reciprocal of the voltage ratio:

$$I_{in}/I_{out} = V_{out}/V_{in} \quad (2.6)$$

So if we step up the voltage by a factor of 2, the input current will be twice the output current. Of course in a real converter with losses, it will be higher again.

2.4 Buck Boost Converter

The main components in a buck-boost converter are again much the same as in the buck and boost types, but they're configured in a different way again. This allows the voltage to be stepped either up or down, depending on the duty cycle.

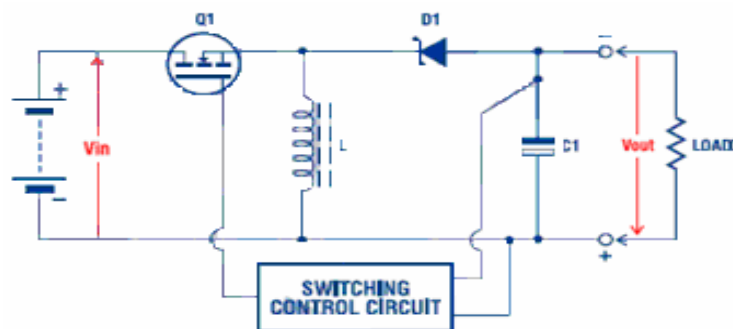


Figure 2.3 In the Buck-Boost converters, the components are used in yet another way, to provide either voltage step-up or step-down but with polarity reversal or inversion as well.

Here when MOSFET Q1 is turned on, inductor L is again connected directly across the source voltage and current flows through it, storing energy in the magnetic field. No current can flow through D1 to the load, because this time the diode is connected so that its reverse biased. Capacitor C1 must supply the load current in this T_{on} phase. But when Q1 is turned off, L is disconnected from the source. Needless to say L again opposes any tendency for the current to drop, and instantly reverses

it's EMF. This generates a voltage which forward biases D1, and current flows into the load and to recharge C1. With this configuration the ratio between the output and input voltages turns out to be (Keng, 2005):

$$V_{out}/V_{in} = -D/(1-D) \quad (2.7)$$

This again equates to

$$V_{out}/V_{in} = -T_{on}/T_{off} \quad (2.8)$$

So the buck-boost converter steps the voltage down when the duty cycle is less than 50% (i.e., $T_{on} < T_{off}$), and steps it up when the duty cycle is greater than 50% ($T_{on} > T_{off}$). But note that the output voltage is always reversed in polarity with respect to the input. So the buck-boost converter is also a voltage inverter. When the duty cycle is exactly 50%, for example, V_{out} is essentially the same as V_{in} except with the opposite polarity. So even when it's not being used to step the voltage up or down, the buck boost converter may be used to generate a negative voltage rail in equipment operating from a single battery. As before, the ratio between output and input currents is simply the reciprocal of the voltage ratio, when the losses are ignored (Vithayathil, 1995).

2.5 Cuk Converter

The basic circuit of a Cuk Converter is shown in Fig.2.4, and it has an additional inductor and capacitor. The circuit configuration is in some ways like a combination of the buck and boost converters, although like the buck-boost circuit it delivers an inverted output. Note that virtually all of the output current must pass through C1, and as ripple current. So C1 is usually a large electrolytic with a high ripple current rating and low ESR (equivalent series resistance), to minimize losses.

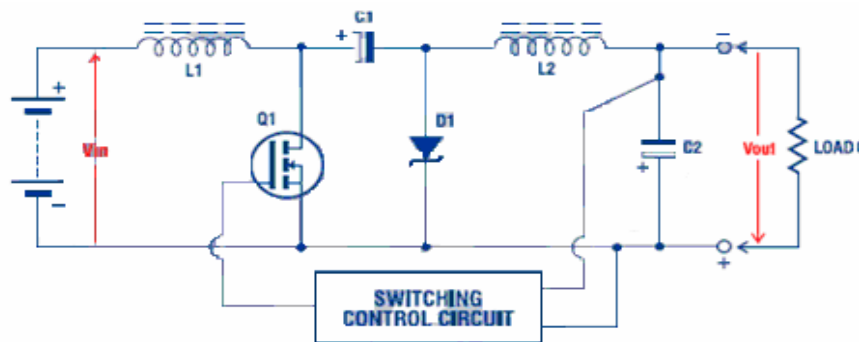


Figure 2.4 The Cuk converter, which can again step the voltage either up or down, also inverting the polarity. In this case there's also less ripple at both input and output.

When Q1 is turned on, current flows from the input source through L1 and Q1, storing energy in L1's magnetic field. Then when Q1 is turned off, the voltage across L1 reverses to maintain current flow. As in the boost converter current then flows from the input source, through L1 and D1, charging up C1 to a voltage somewhat higher than V_{in} and transferring to it some of the energy that was stored in L1. When Q1 is turned on again, C1 discharges through via L2 into the load, with L2 and C2 acting as a smoothing filter. Meanwhile energy is being stored again in L1, ready for the next cycle (Keng, 2005).

As with the buck-boost converter, the ratio between the output voltage and the input voltage again turns out to be:

$$V_{out}/V_{in} = -D/(1-D) \quad (2.9)$$

$$= -T_{on}/T_{off} \quad (2.10)$$

The minus sign again indicates voltage inversion. So like the buck-boost converter, the Cuk converter can step the voltage either up or down, depending on the switching duty cycle. The main difference between the two is that because of the series inductors at both input and output, the Cuk converter has much lower current ripple in both circuits. In fact by careful adjustment of the inductor values, the ripple in either input or output can be nulled completely.

CHAPTER THREE BUCK CONVERTERS

3.1 Buck Converters General Structure

Buck converter is a dc-to-dc converter that steps down the dc voltage from its fixed high level to a desired low level. It is also called the forward converter and its circuit topology is given in Figure 3.1.

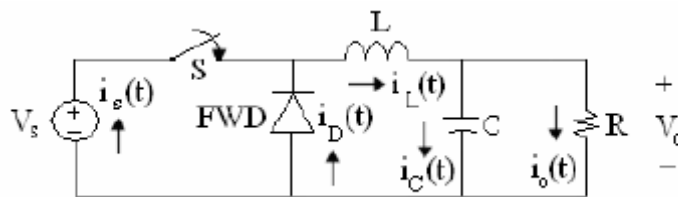


Figure 3.1 Buck Converter Topology

The switch S is usually an electronic device that operates either in the conduction mode (on) or the cut-off mode (off). The on and off time-periods are controlled by the suitably designed gating circuits, which are usually not shown. The on time of the switch is a fraction of its time period T such that $T_{ON} = D T$, where D is the duty cycle. During the off time $T_{OFF} = (1 - D) T$ the freewheeling diode FWD provides a path to maintain the continuity of the current through the inductor. The inductor controls the percent of the ripple and determines whether or not the circuit is operating in the continuous mode. The capacitor C provides the filtering action by providing a path for the harmonic currents away from the load. In addition, its value is large enough so that voltage ripple is very small.

It must be clear from Figure-3.1 that there are two energy storing elements L and C in a sequentially-switching circuit. These elements results in a second order differential equation either in terms of the inductor current or the capacitor voltage. The differential equation in terms of the capacitor voltage, when the switch S is closed, may be written as

$$LC \frac{d^2 V_C(t)}{dt^2} + \frac{L}{R} \frac{dV_C(t)}{dt} + V_C(t) = V_S \quad (3.1)$$

The solution of the above second-order differential yields the voltage during the time switch is closed. A similar equation may be written when the switch is in its open position.

The above differential equation can be simplified if we make an assumption that the voltage across the load, and thereby across the capacitor, is fairly constant. The differential equation in terms of the current through the inductor, when the switch is closed, may now be written

$$L \frac{di_L(t)}{dt} = V_S - V_O \quad (3.2)$$

Let assumed that the circuit has been operating for quite some time and has attained its steady state. In other words, there may already be some current in the inductor, $I_{L\min}$, just prior to the closing of switch S. With this understanding, the solution of the above equation, for $0 \leq t \leq T_{ON} = DT$ yields

$$I_L(t) = \frac{V_S - V_O}{L} t + I_{L\min} \quad (3.3)$$

The inductor current increases linearly with time and attains its maximum value $I_{L\max}$ as $t \rightarrow T_{ON} = DT$ such that

$$I_{L\max} = \frac{V_S - V_O}{L} DT + I_{L\min} \quad (3.4)$$

$$i_L(t) = \frac{V_S - V_O}{L} t + I_{L\min} \quad (3.5)$$

The inductor current increases linearly with time and attains its maximum value $I_{L\max}$ as $t \rightarrow T_{\text{ON}} = DT$ such that

$$I_{L\max} = \frac{V_s - V_o}{L} DT + I_{L\min} \quad (3.6)$$

Defining the change in the current from its minimum to maximum value as the peak-to-peak current ripple ΔI_L , the above equation yields an expression for ΔI_L as

$$\Delta I_L = I_{L\max} - I_{L\min} = \frac{V_s - V_o}{L} DT \quad (3.7)$$

Note that the current ripple is directly proportional to D , the duty cycle, upon which we may not have any control because of the output voltage requirement. However, it is inversely proportional to the inductance L upon which we can exert some controls. Thus, the current ripple can be maintained within its bounds by a proper selection of the inductor.

Let us now analyze the circuit when the switch is in its open position. The inductor current completes its path through the freewheeling diode and the corresponding differential equation, for $0 < t < T_{\text{OFF}}$, is

$$L \frac{di_L(t)}{dt} = V_s - V_o \quad (3.8)$$

From the solution of the above first-order differential equation, it is obtained

$$i_L(t) = \frac{-V_o}{L} t + I_{L\max} \quad (3.9)$$

Where $I_{L\max}$ is the maximum value of the current in the inductor, $I_{L\max}$ at the opening of the switch or the beginning of the off period. As $t \rightarrow T_{\text{OFF}} = (1-D)T$ the inductor current decreases to its minimum value $I_{L\min}$ such that

$$I_{L\min} = \frac{-V_o}{L}(1-D)T + I_{L\max} \quad (3.10)$$

This equation yields another expression for the peak-to-peak current ripple as

$$\Delta I_L = I_{L\max} - I_{L\min} = \frac{V_o}{L}(1-D)T \quad (3.11)$$

The current ripple as given by (3.6) must be the same as given by (3.10) Therefore, equating the two equations, we get

$$\frac{V_s - V_o}{L}DT = \frac{V_o}{L}(1-D)T \quad (3.12)$$

This equation upon simplification yields

$$V_o = DV_s \quad (3.13)$$

Equation (3.12) states that the output voltage of the buck converter is directly proportional to the duty cycle and the source voltage. Since the duty cycle is usually less than unity, the output voltage is smaller than the source (applied or input) voltage. This is the reason why a buck converter is commonly called the step-down converter. Since the power flow is from the source to the load and there is no power flowing back to the source, it is also called the forward converter.

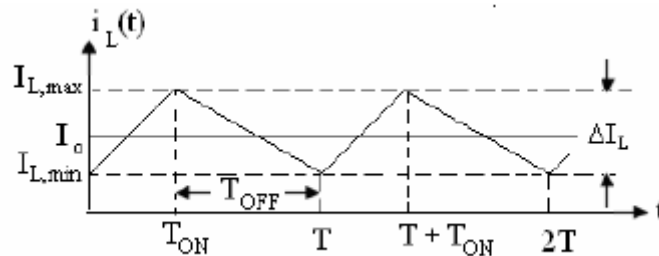


Figure 3.2 Inductor current

The current through the inductor as given by (3.3) during the on time and by (3.8) during the off time is sketched in Figure 3.2.

The average current in the inductor must be equal to the dc current through the load. That is

$$I_{Lavg} = I_o = \frac{V_o}{R}$$

The expressions for the maximum and minimum currents through the inductor may now be written as

$$I_{Lmax} = I_{Lavg} + \frac{\Delta I_L}{2} = \frac{V_o}{R} + \frac{V_o}{2L}(1-D)T \quad (3.15)$$

$$I_{Lmin} = I_{Lavg} - \frac{\Delta I_L}{2} = \frac{V_o}{R} - \frac{V_o}{2L}(1-D)T \quad (3.16)$$

The current supplied by the source varies from I_{Lmin} to I_{Lmax} during the time the switch is closed and is zero otherwise as shown in Figure 3.3.

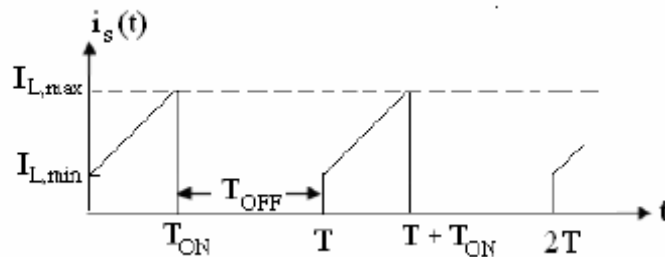


Figure 3.3 The Source current

When the switch, the inductor, and the capacitor are treated as ideal elements, the average power dissipated by them is zero. Consequently, the average power supplied by the source must be equal to the average power delivered to the load. That is,

$$V_s I_s = V_o I_o = D V_s I_o$$

This equation helps us express the average source current in terms of the average load current as

$$I_S = DI_0 \quad (3.17)$$

The current through the freewheeling diode is shown in Figure 3.4. Its average value is

$$I_D = (1-D)I_0 \quad (3.18)$$

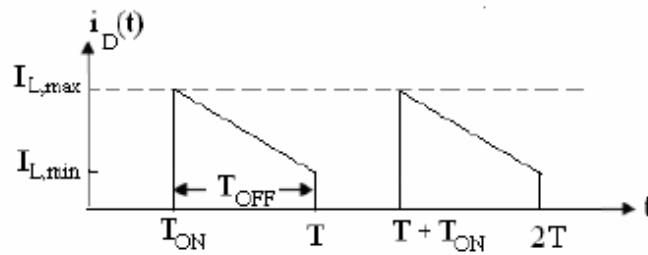


Figure 3.4 The Freewheeling diode current

When the load current is subtracted from the inductor current, we obtain the time-varying current through the capacitor. Its minimum and maximum values from (3.14) and (3.15) are

$$I_{C,max} = \frac{\Delta I_L}{2} = \frac{V_o}{2L}(1-D)T \quad (3.19)$$

$$I_{C,min} = -\frac{\Delta I_L}{2} = -\frac{V_o}{2L}(1-D)T \quad (3.20)$$

The corresponding waveform for the capacitor current is given in Figure 3.5. The average current through the capacitor is zero.

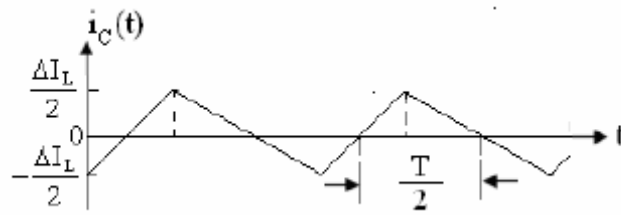


Figure 3.5 Current trough capacitor

The current waveform of Figure 3.5 helps us determine the change in the voltage across the capacitor. During one-half the time period, the current is charging the capacitor and the increase in the charge can be computed from Figure 3.5 as

$$\Delta Q = \frac{1}{2} \frac{\Delta I_L}{2} \frac{T}{2} = \frac{1}{8} \Delta I_L T \quad (3.21)$$

Substituting for ΔI_L from (3.8), we obtain an expression for the increase in charge on the capacitor as

$$\Delta Q = \frac{V_o}{8L} (1-D) T^2 \quad (3.22)$$

Therefore, increase in the capacitor voltage is

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{1-D}{8LC} V_o T^2 = \frac{1-D}{8LCf^2} V_o \quad (3.23)$$

When we define the capacitor ripple as the ratio of the increase in the capacitor voltage to its average value, it can then be expressed as

$$\frac{\Delta V_o}{V_o} = \frac{1-D}{8LCf^2} \quad (3.24)$$

Note that the capacitor ripple define by (3.24) is not the same as the peak-to-peak voltage ripple for the rectifiers. The peak-to-peak voltage ripple for the buck

converter will be twice of that given by (3.24). Equation (3.24) may be viewed as one-sided voltage ripple.

The buck converter can operate either in its continuous conduction mode or discontinuous conduction mode. When it operates in the continuous conduction mode, there is always a current in the inductor. The minimum current in the continuous conduction mode can be zero at the time of switching. Consequently, there is a minimum value of the inductor that ensures its continuous conduction mode. It can be obtained from (3.15) by setting $I_{L\min}$ to zero as

$$\frac{V_o}{R} - \frac{V_o}{2L_{\min}}(1-D)T = 0 \quad (3.25)$$

Hence,

$$L_{\min} = \frac{1-D}{2}RT = \frac{1-D}{2f}R \quad (3.26)$$

From the peak-to-peak current ripple, we can obtain an expression for the percent current ripple as

$$\%CR = \frac{\Delta I_L}{I_{L\text{avg}}} \times 100 = \frac{100(1-D)}{Lf}R \quad (3.27)$$

3.2 Output Voltage Ripple

The variation in output voltage, or ripple, is computed from the voltage-current relationship of the capacitor. The current in the capacitor is

$$i_C = i_L - i_R \quad (3.28)$$

shown in Fig. 3.6a.

While the capacitor current is positive, the capacitor is charging. From the definition of capacitance,

$$Q = CV_o \quad (3.29)$$

$$\Delta Q = C\Delta V_o \quad (3.30)$$

$$\Delta V_o = \Delta Q/C. \quad (3.31)$$

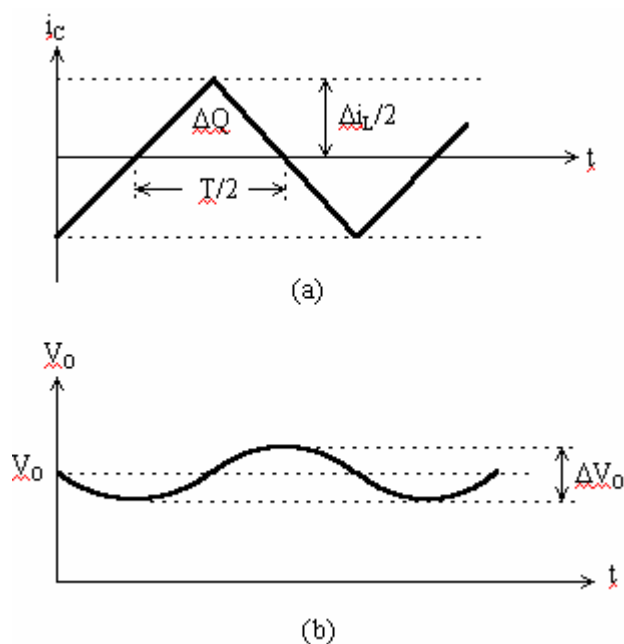


Figure 3.6 Buck converter waveforms

(a) Capacitor current (b) Output voltage

The change in charge, ΔQ , is the area of the triangle above the time axis:

$$\Delta Q = \frac{1}{2} \left(\frac{T}{2} \right) \left(\frac{\Delta i_L}{2} \right) = \frac{T\Delta i_L}{8} \quad (3.32)$$

Resulting in

$$\Delta V_o = \frac{T\Delta i_L}{8C} \quad (3.33)$$

Using Eq. 3.11 for Δi_L ,

$$\Delta V_o = \frac{T}{8C} \frac{V_o}{L} (1-D)T = \frac{V_o(1-D)}{8LCf^2} \quad (3.34)$$

In this equation, V_o is the peak-to-peak ripple voltage at the output, as shown in Fig.3.6 It is also useful to express the ripple as a fraction of the output voltage:

$$\frac{\Delta V_o}{V_o} = \frac{1-D}{8LCf^2} \quad (3.35)$$

If the ripple is not large, the assumption of a constant output is reasonable and the preceding analysis is essentially valid.

Since the converter components are assumed to be ideal, the power supplied by the source must be the same as the power absorbed by the load resistor:

$$P_s = P_o \quad (3.36)$$

$$V_s I_s = V_o I_o \quad (3.37)$$

$$V_o/V_s = I_s/I_o \quad (3.38)$$

Note that the preceding relationship is similar to the voltage-current relationship for a transformer in ac applications. Therefore, the buck converter circuit is equivalent to a dc transformer.

CHAPTER FOUR THE PLL DESIGN THEORY

4.1 General Architecture and Operational Principle

The basic phase locked loop consists of three building blocks: the phase detector (PD), the loop filter (LF) and the voltage controlled oscillator (VCO) (Lindsey W.C. & Chie C.M., 1985). The phase detector has two inputs. One is the incoming signal from an external source and the other is from VCO, they enter the phase comparator.

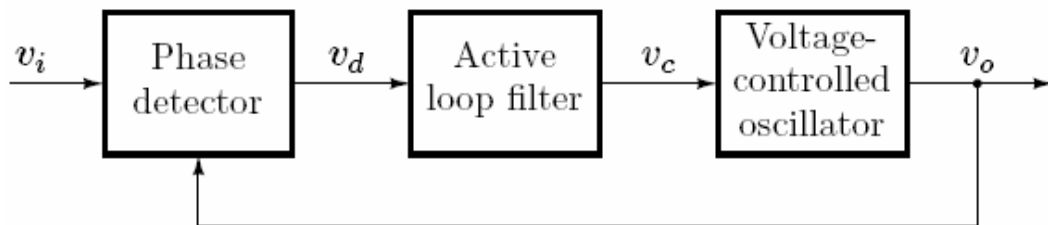


Figure 4.1 The Basic components of a Phase-Lock Loop

The PLL works by comparing the reference signal with the VCO's output. The PD measures any difference in phase between the incoming signal and the local signal (VCO output), and produces a signal whose amplitude is proportional to this phase difference. After appropriate filtering by the LF to remove unwanted high frequency components and to produce the desired dynamical characteristic, the signal is fed into the VCO whose frequency changes in response to this input. An error signal is produced that is proportional to the phase difference of the reference signal and the output signal. By changing the VCO frequency, the phase of its output is controlled until it matches that of the incoming signal, at which point the fed back error signal goes to zero. This error signal is filtered to generate the VCO control voltage. The loop is setup in a negative feedback fashion so the VCO control voltage will force the output of the VCO to lock with the input reference signal within certain frequency limits (Nash, 1994).

4.2 Phase Locked Loop Components

Generally speaking, the PLLs can be classified into two groups, digital and analog. While both perform as PLLs, the digital circuits are more suitable for the synchronization of digital signals, clock recovery from encoded digital data streams, and other digital applications. Analog monolithic PLLs are used quite extensively in communication systems since they maintain linear relationships between input and output quantities (Connelly, 1988).

A PLL has three core components. They are

1. Phase Detector (PD) or the multiplier
2. Voltage controlled Oscillator or VCO
3. The Loop filter (LF)

4.2.1 Phase/Frequency Detectors

A phase detector must be able to detect a change in the state of one of the two inputs and tell which input stayed constant. This is important in the basic function of the phase detector. The circuit must have the ability to detect if the reference (or the feedback signal of the PLL) changed. As a result, the phase detector will adjust its output to cause the VCO to raise or lower the frequency and phase accordingly.

Phase detector: compares the phase at each input and generates an error signal, $V_e(t)$, proportional to the phase difference between the two inputs. K_D is the gain of the phase detector (V/rad) (Best, 1997)

$$v_e(t) = K_D [\phi_{out}(t) - \phi_{in}(t)] \quad (4.1)$$

There are different types of phase detectors. In this chapter we deal with three type detectors on pll: Analog multipliers, Exclusive OR Gates, Sequential phase detectors.

4.2.1.1 Analog Multiplier as a Phase Detector

The multiplier PD is especially useful in applications where the reference frequency is too high and where the loop bandwidth is sufficiently narrow so that the filtering of the undesired components can be effective.

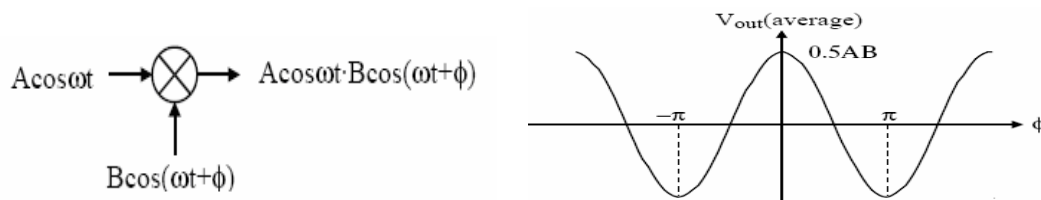


Figure 4.2 Classical analog multiplier phase detector

$$AB \cos(\omega t) \cos(\omega t + \phi) = \frac{AB}{2} \{ \cos(\phi) - \cos(2\omega t + \phi) \} \quad (4.2)$$

If we look only at the low frequency or dc component, the output of the multiplier is;

$$V_{out} = \frac{AB}{2} \cos(\phi) \quad (4.3)$$

and is a phase detector

Phase detector gain “constant” is given as;

$$K_d = \frac{d}{dt}(V_{out}) = -\frac{AB}{2} \sin(\phi)(V / rad) \quad (4.4)$$

Note that K_d is zero when ϕ is zero and greatest when ϕ is $\pm 90^\circ$. To maximize the useful phase range, the loop should be arranged to lock to a phase difference of 90° . This is a *quadrature* phase detector.

4.2.1.2 Exclusive-OR-gate as a Phase Detector

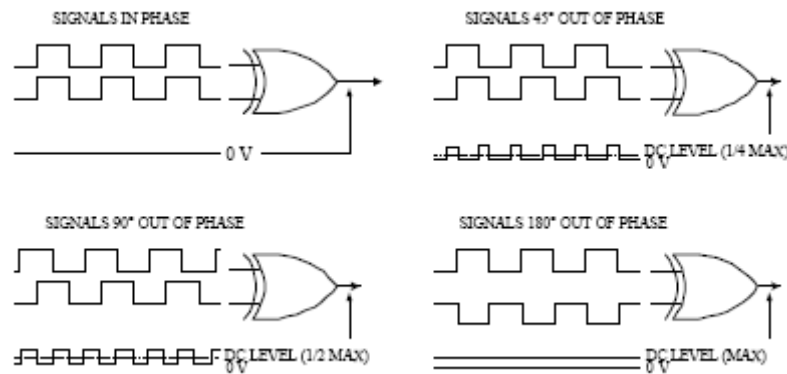


Figure 4.3 Phase detection using an XOR gate.

For a variety of reasons, it may be desirable to have a loop which does not produce a sinusoidal clock but instead a square wave clock. If one over-drives the mixer circuit, which is if one uses signals so large that the amplifiers saturate, the output signals stop looking like sinusoids and start looking like Walsh functions (rectangular signals). Such a phase detector is shown in Figure 4.2. Understanding the output of such a phase detector relies on a combination of averaging analysis and heuristics. However, one of the more interesting features of such a phase detector is that it can be implemented using an Exclusive-OR (XOR) gate as shown in Figure 4.3. One advantage of such a phase detector is that the loop gain is now independent of input signal amplitude. Furthermore, an XOR phase detector's response can have a larger linear range than a sinusoidal detector (mixer). The disadvantage is that the linearity of the base band response is affected by the relative duty cycles of the input and VCO signals.

The way the circuit works as PD is shown in Figure 4.3. The on time of the output signal increases as the phase relations of the two signals increase toward 180° . Above 180° , the DC output voltage decreases and becomes zero when the two signals are back in phase. For this system to function correctly, the two inputs must have a 50% duty cycle (the on time must equal the off time) [Adamson, 1992]

The two input signals XOR PD, u_1 and u_2 , the average output signals of XOR PD, Q , and the characteristics of XOR PD are shown in Figure 4.4. θ_e is the phase error at the output of the PD as seen in Figure 4.4. The maximum average DC output is at 180° . Thus, as with the analog PD, the average DC output voltage is

proportional to the phase difference of the input signals. The PD characteristic is strongly dependent on the duty cycle of u_1 and u_2 .

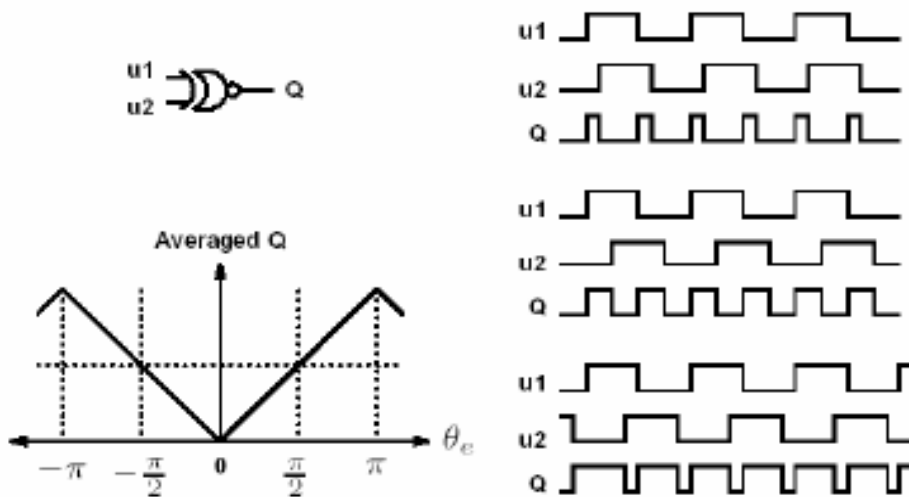


Figure 4.4 Phase detection signals by using an XOR gate.

$$V_{out(average)} = V_{min} + \frac{V_{max} - V_{min}}{\pi} \phi \Rightarrow Kd = \frac{V_{max} - V_{min}}{\pi} \tag{4.5}$$

4.2.1.3 Sequential Phase Detectors

Sequential phase detectors generate error voltages proportional to the phase difference by detecting the zero crossing of the input and VCO signals (Best, 1997).

SR flip-flop implementation; Positive going one sets the flip-flop, Negative going one resets it. Average output voltage:

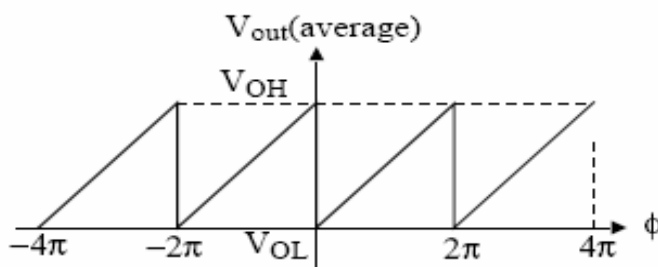


Figure 4.5 Output signals for sequential phase detectors

$$Kd = \frac{V_{oh} - V_{ol}}{2\pi} \tag{4.6}$$

4.2.1.4 Phase Detectors Versus Frequency Detectors

A frequency detector determines the difference between two frequencies. Multiplier detectors cannot detect frequency differences. Sequential phase detectors can detect both frequency and phase difference (PFD).

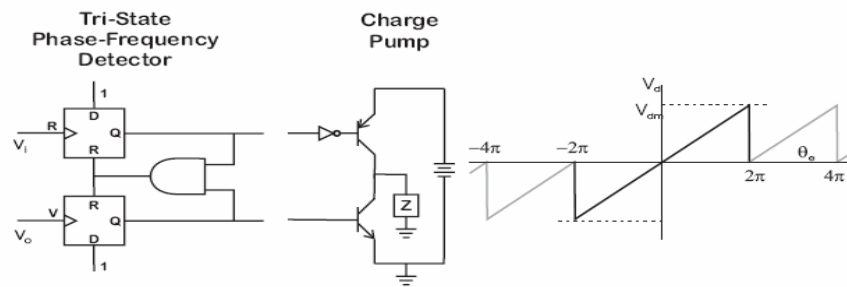


Figure 4.6 The Combination of a tri-state phase frequency detector and a charge pump

An extremely popular phase detector is the combination of the tri-state phase-frequency detector (PFD) with a charge pump shown in Figure 4.7. The charge pump can be viewed as a 3 position switch controlled by the phase frequency detector. The action of the charge pump is to alleviate any loading of the phase detector in driving the rest of the circuit. This allows the response to be smoother than without the charge pump. Note that the loop filter is often implemented within the charge pump as shown at the right of Figure 4.6.

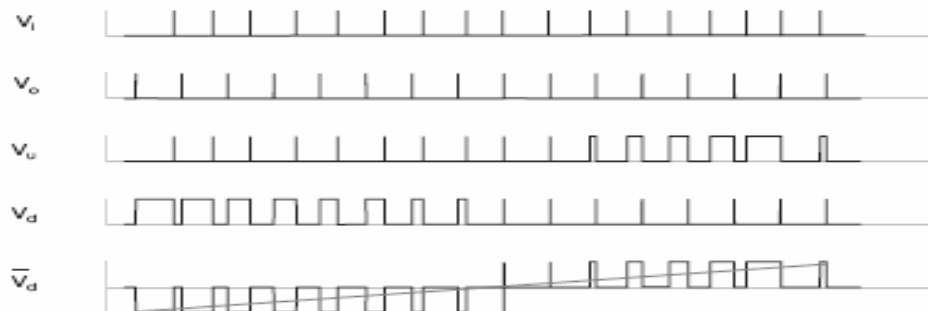


Figure 4.7 Phase detection using a phase-frequency detector (PFD). As only the leading edges are significant, these are compared to show the phase behavior of the detector.

4.2.2 Voltage Controlled Oscillators

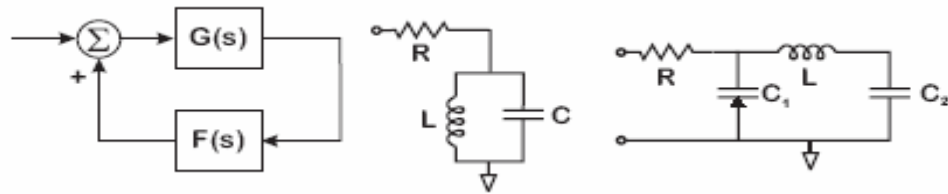


Figure 4.8 On the left, a block diagram of an oscillator implemented as a positive feedback loop between a voltage to current amplifier through a resonant circuit. On the right, examples of resonant circuits: a LC tank and a π network.

The actual clock generated by a PLL comes from the voltage controlled oscillator (VCO). The VCO is a nonlinear device which generates a periodic oscillation. The frequency of this oscillation can be controlled by modulating some control voltage (hence the name). In a PLL, the control voltage corresponds to some filtered form of the phase error. In response to this, the VCO adjusts its frequency. As the VCO frequency is slewed by the control voltage, the phase error is driven towards 0. This frequency adjustment to achieve phase lock results in the model of a VCO as an integrator. VCOs are generally of the form of a ring oscillator, relaxation oscillator or a resonant oscillator. The ring oscillator, common in monolithic topologies takes the form of an odd number of inverters connected in a feedback loop (Razavi 1996). The relaxation oscillator uses a Schmitt-trigger to generate a stable square wave (Wolaver, 1991). The latter puts a resonant circuit in the positive feedback path of a voltage to current amplifier as shown in Figure 4.8. The amplifier shown for these circuits is a voltage to current amplifier with close to unity gain. The resonant circuit in the positive feedback path has poles close to the $j\omega$ axis.

Consider the band pass filter:

$$F(s) = \frac{2\zeta\omega_0 s}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \quad (4.7)$$

and $G(s) = K < 1$. Then;

$$VCO(s) = \frac{Gs}{1 - G(s)F(s)} = K \frac{s^2 + 2\zeta\omega_0 s + \omega_0^2}{s^2 + 2\zeta_1\omega_0 s + \omega_0^2} \quad (4.8)$$

Where $\zeta_1 = (1 - K)\zeta$. The lowering of the damping ratio is called “Q amplification” ($Q = 1/2\zeta$) and moves the poles even closer to the $j\omega$ axis. (In the case of the π network, there is a complex pair of poles and one pole on the negative real axis. The dominant effect, Q amplification, takes place on the complex pair.) The frequency is controlled by altering the capacitance of the resonator, typically by using a varactor diode as a capacitor. Other forms of VCOs, such as crystal oscillators and YIG oscillators essentially run on the same principle, but modify the resonant circuit.

4.2.3 Loop Filters

Typical analysis ignores the high frequency low pass filter and other dynamics that do not affect the behavior of the loop at the time constants of the phase. As the vast majority of PLLs are second order and as the actions of the VCO are modeled as an integrator, loop filters are typically first order. More specifically, since a Type II system will track a phase ramp and this corresponds to tracking a step in frequency, the loop filter almost always contains an integrator. For a double integrator system, the loop filter needs a minimum phase zero to obtain stability. This is true whether the filter is implemented as an analog or digital filter. Higher order loops (which are rarer) can be obtained by adding extra pole/zero pairs to the filter.

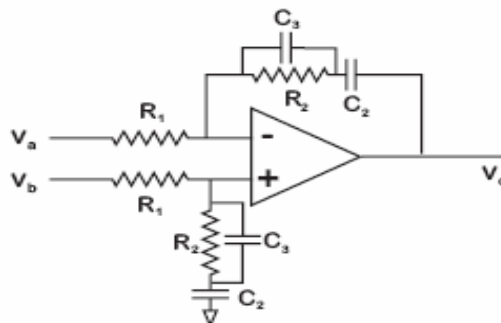


Figure 4.9 Analog loop filters for differential inputs. For single ended input, the + terminal can be tied directly to ground.

The analog circuit (classical or classical digital PLL) has shown in Figure 4.9 shows the general form of a loop filter. This particular filter is fairly general with a transfer function of (Best, 1997):

$$\frac{V_o}{V_a - V_b} = -\frac{sR_2(C_2 + C_3) + 1}{sR_1C_2(sR_2C_3 + 1)} \quad (4.9)$$

4.3 PLL Operating Ranges

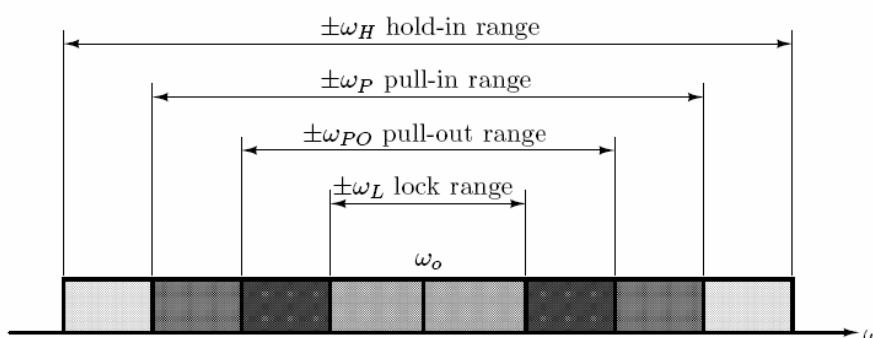


Figure 4.10 PLL Operating ranges

4.3.1 The Hold Range

The hold range, $\Delta\omega_H$, is defined as that frequency range at which the PLL is able to statically maintain phase tracking. It is determined by calculating the frequency offset at the reference input that causes the phase error to be beyond the range of linear analysis. For a multiplying or XOR phase detector, this phase error is $\pi/2$. For sequential detectors, it will be larger. Best states that since loops will be permanently out of lock if the frequency offset at the input is greater than the hold range, this quantity is more of an academic matter than a practical one, but it can be calculated for a classical PLL (sinusoidal phase detector) as:

$$\Delta\omega_H = K_o K_d F(0). \quad (4.10)$$

4.3.2 The Lock Range

The lock range, $\Delta\omega L$, is defined as that frequency range within which the PLL locks within one single-beat note between the reference frequency and output frequency. The lock range must be calculated from a nonlinear equation, but there are several useful approximations that are made. In particular, if the relative order of numerator and denominator of the PLL are 1, then the loop can be said to behave like a first order loop at higher frequencies, and thus the lock range can be estimated as:

$$\Delta\omega L \approx \pm K_o K_d F(\infty) \quad (4.11)$$

4.3.3 The Pull-In and Pull-Out Range

The pull-in range, $\Delta\omega P$, is defined as the frequency range in which the PLL will always become locked. The pull-out range, The pull-out range represents the dynamical limits to PLL stability, i.e. the frequency step which, when applied to the PLL input, causes lock-out. An exact expression for $\Delta\omega PO$ has never been derived for the analog PLL, though simulation yield good approximations, and verify that $\Delta\omega P > \Delta\omega PO > \Delta\omega L$ in a typical design.

CHAPTER FIVE

RESONANT CIRCUITS AND PHASE- LOCK TUNNING

5.1 Resonant Circuits as Filter Circuits

The principles of series- or parallel-resonant circuits have many applications in radio, television, communications, and the various other electronic fields throughout the Navy. By making the capacitance or inductance variable, the frequency at which a circuit will resonate can be controlled. In addition to station selecting or tuning, resonant circuits can separate currents of certain frequencies from those of other frequencies. Circuits in which resonant circuits are used to do this are called resonant filter circuits. If we can select the proper values of resistors, inductors, or capacitors, a filter network, or "frequency selector," can be produced which offers little opposition to one frequency, while blocking or attenuating other frequencies (Misra, 2001).

A filter network can also be designed that will "pass" a band of frequencies and "reject" all other frequencies. Most electronic circuits require the use of filters in one form or another. As an example of a filter being applied is in a rectifier circuit or in dc-dc converters. An alternating voltage is changed by the rectifier to a direct current. However, the DC voltage is not pure; it is still pulsating and fluctuating. In other words, the signal still has an AC component in addition to the DC voltage. By feeding the signal through simple filter networks, the AC component is reduced. The remaining DC is as pure as the designers require.

Resonant circuits may be designed as series resonant or parallel resonant. Each has the ability to discriminate between its resonant frequency and all other frequencies.

5.1.1 Parallel LC Resonant Circuit

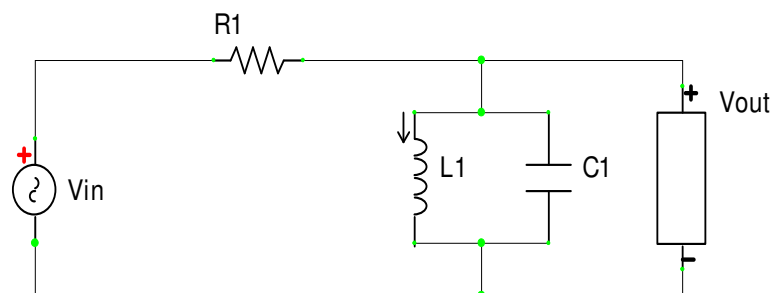


Figure 5.1 LC Parallel Resonant Circuit.

Treating as a voltage divider, we have:

$$V_{\text{out}} = \frac{|Z_{LC}|}{|R + Z_{LC}|} V_{\text{in}} \quad (5.1)$$

Calculating the complex impedance Z_{LC} :

$$\frac{1}{Z_{LC}} = \frac{1}{Z_L} + \frac{1}{Z_C} = \frac{1}{j\omega L} - \frac{\omega C}{j} = j\left(\omega C - \frac{1}{\omega L}\right) \quad (5.2)$$

$$Z_{LC} = \frac{j}{\frac{1}{\omega L} - \omega C} = \frac{j\omega L}{1 - \omega^2 LC} \quad (5.3)$$

$$|Z_{LC}| = \sqrt{\left(\frac{-j\omega L}{1 - \omega^2 LC}\right)\left(\frac{j\omega L}{1 - \omega^2 LC}\right)} = \sqrt{\frac{(\omega L)^2}{(1 - \omega^2 LC)^2}} = \frac{\omega L}{1 - \omega^2 LC} \quad (5.4)$$

Notice that this expression is always imaginary and is equal to ∞ when

$$\begin{aligned} \omega^2 LC &= 1 \\ \omega &= 1/(LC)^{1/2}. \end{aligned} \quad (5.5)$$

This means that if the angular frequency is adjusted to this special frequency, generates a voltage of infinitely large amplitude across this simple circuit. This

phenomenon is called resonance, and the frequency $f_0 = 1/2\pi(LC)^{1/2}$ or $\omega_0 = 1/(LC)^{1/2}$ is called the resonance frequency. A resonating circuit formed by a capacitor and an inductor in parallel, is called a parallel resonant circuit.

Where there is R serial to resonant circuit:

$$|R + Z_{LC}| = \sqrt{\left(R - \frac{j\omega L}{1 - \omega^2 LC}\right) \left(R + \frac{j\omega L}{1 - \omega^2 LC}\right)} = \sqrt{R^2 + \frac{(\omega L)^2}{(1 - \omega^2 LC)^2}} \quad (5.6)$$

$$\frac{V_{out}}{V_{in}} = \frac{\omega L}{(1 - \omega^2 LC) \sqrt{R^2 + \frac{(\omega L)^2}{(1 - \omega^2 LC)^2}}} = \frac{\omega L}{\sqrt{(\omega L)^2 + R^2 (1 - \omega^2 LC)^2}} \quad (5.7)$$

Note that for $\omega = \omega_0 = \frac{1}{\sqrt{LC}}$ resonant frequency $\frac{V_{out}}{V_{in}} = 1$

Other wise is $\frac{V_{out}}{V_{in}}$ small.

5.1.2 Series LC Resonant Circuit

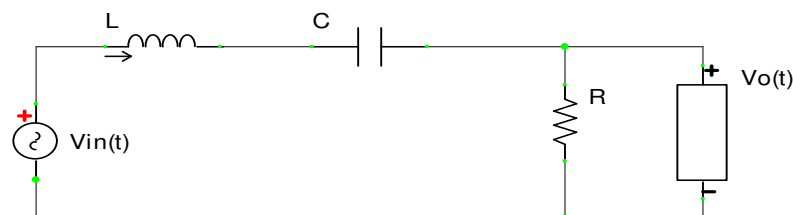


Figure 5.2 A series R-L-C circuit with input-output terminals.

Since the inductive reactance is directly proportional to signal frequency, it tries to block the high-frequency contents of the signal. On the other hand, capacitive reactance is inversely proportional to the frequency. Therefore, it tries to stop its lower frequencies. If the input signals frequency is equal to the resonant frequency,

maximum current will flow through the resistor and it will be in phase with the input voltage. In this case, the output voltage V_o will be equal to the input voltage V_{in} . It can be analyzed as follows.

5.2 Fourier Analysis

Any function can be written as the sum of sine and cosine functions of different frequencies and amplitudes. In this project we are dealing with dc to dc conversion and there is switching operation which causes a square wave periodical signal. Using resonant filter it is very important to make Fourier analyze of square wave signal to calculate fundamental harmonic ripples.

We can apply this technique to periodic voltage waveforms:

$$V(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos \frac{2\pi n t}{T} + \sum_{m=1}^{\infty} b_m \sin \frac{2\pi m t}{T} \quad (5.8)$$

Where T = minimum time voltage waveform repeats itself and $1 / T$ = fundamental frequency = f_0

Could instead substitute $w = 2\pi / T$

- The a_n and b_m constants are determined from:

$$a_n = \frac{2}{T} \int_{-T/2}^{T/2} V(t) \cos n\omega t \, dt \quad b_m = \frac{2}{T} \int_{-T/2}^{T/2} V(t) \sin m\omega t \, dt \quad (5.9)$$

- For a symmetric square wave voltage (assuming $V(t)$ odd):
 - $a_n = 0 \quad n = 0, 1, 2, 3, \dots$

$$b_m = \frac{4}{T} \int_0^{T/2} V(t) \sin m\omega t \, dt = \begin{cases} b_m = 0 & m \text{ even} \\ b_m = \frac{4V_0}{m\pi} & m \text{ odd} \end{cases} \quad (5.10)$$

$$V(t) = \frac{4V_0}{\pi} \left(\frac{\sin \omega t}{1} + \frac{\sin 3\omega t}{3} + \frac{\sin 5\omega t}{5} + \dots \right) \quad (5.11)$$

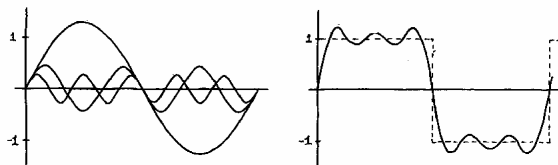


Figure 5.3 Harmonic Components of Square Wave Signal

When we apply an input square wave voltage of frequency ω_0 to the parallel LC circuit, we are in essence applying frequencies ω_0 , $3\omega_0$, $5\omega_0$, etc. simultaneously with relative amplitudes 1, $1/3$, $1/5$, etc. (respectively)

The LC circuit is a “detector” of its resonance frequency f_0 , including contributions from the harmonics of the input fundamental frequency “Mini-resonance” peaks will occur in the output voltage at driving frequencies of $f_0/3$, $f_0/5$, etc.

5.3 Phase-Lock Tuning For Resonant Converters

Resonant excitation is equivalent to maintaining a resistive phase relationship (0°) between resonator voltage and current which is seen in figure 5.4. Because the phase response of a series- or parallel-tuned circuit monotonically increases or decreases around the 0° tuning point, it can be used as an error signal to control for excitation at the point of maximum immittance.

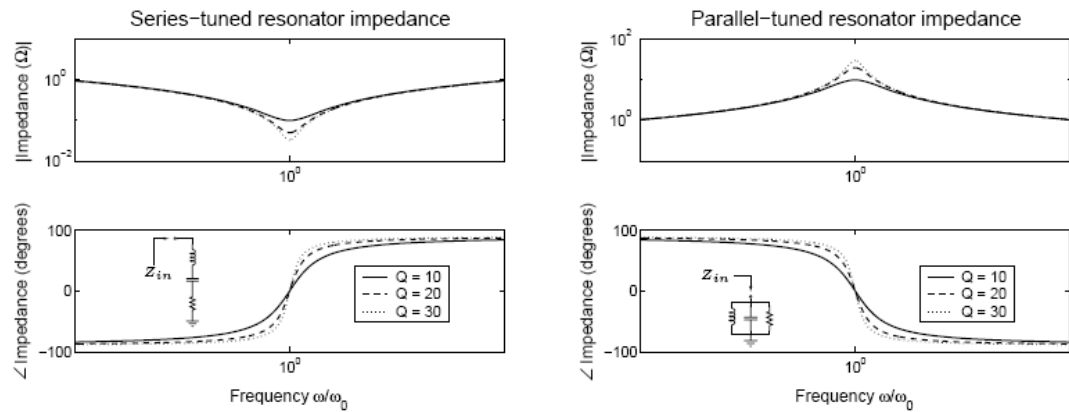


Figure 5.4 Frequency response of second-order tuned circuits, normalized to the natural frequency.

$\omega_n = 1/\sqrt{LC}$ The impedance magnitude at a single frequency can indicate proximity to resonance (with calibration) but not whether resonance lies above or below the stimulus frequency. The impedance phase, however, increases or decreases monotonically, and its difference from 0° is an error signal indicating the distance and direction to resonance.

A control topology to excite a series resonance at its minimum-impedance point is shown in Fig. 5.5a. The dual of this tuning system is shown in Fig. 5.5b, which drives a parallel resonance at its maximum-impedance point. The control circuitry in either case generates the frequency command shown at the right. This command specifies the fundamental but not the harmonic content or DC level of the sources on the left of the block diagrams. In a power converter, the frequency command would represent an adjustable PWM frequency (Phinney, 2001).

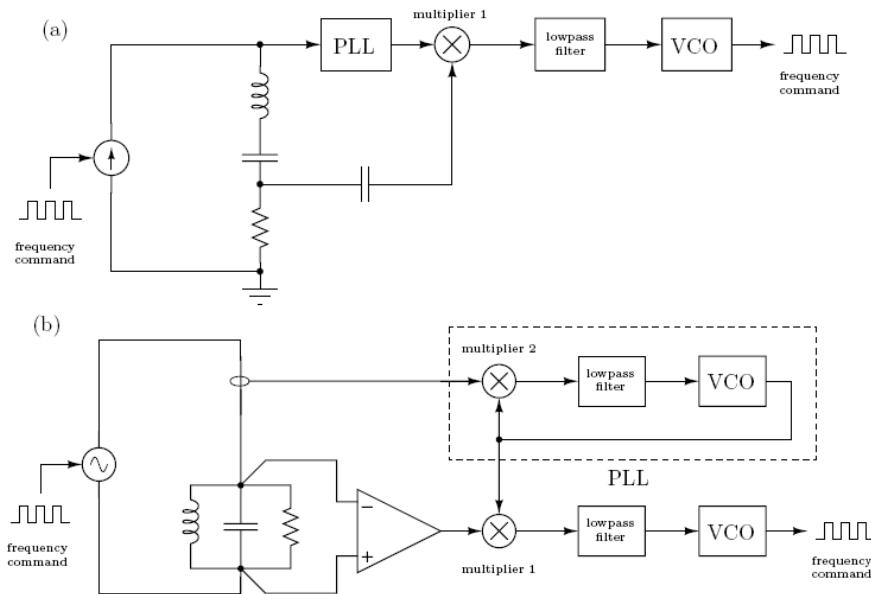


Figure 5.5 Block diagram of the phase-lock tuning system, demonstrating two possible methods of sensing resonator AC voltages and currents.

To excite the parallel- and series-tuned resonators, the controller must, in either case, adjust the fundamental drive frequency such that the resonator current and voltage Fundamentals are in phase. The inner-loop PLLs in Figs. 5.5a and b serve two functions in this regard. They provide, first of all, a 90° phase shift in lock, which allows a subsequent phase detector (multiplier 1) to develop zero average output for a 0° V-I resonant condition in the resonators. By itself, this phase shift is poor motivation for introducing the complexity of a PLL, as the designer could employ a phase detector with 0° offset.¹ The more significant function of the inner-loop PLLs, then, is to reject harmonics by locking on the fundamental component of an input waveform.

Consider, for example, the parallel-resonator tuning system of Fig. 5.5b. The differential amplifier measures the AC voltage across parallel-tuned tank, a signal with, presumably, a large fundamental component. The current through the parallel-tuned circuit, however, is dominated by its harmonic content, since the resonator suppresses the fundamental inasmuch as its Q is large. The PLL effectively filters this harmonic content, extracting a signal proportional to the fundamental current only. The AC tank currents can have arbitrary harmonic content as long as the phase-

lock loop employs a VCO with sinusoidal output. i.e., as long as one input of multiplier 2 is sinusoidal, the product waveform is a useful phase-detector signal when the AC tank current is any periodic waveform with roughly the same fundamental frequency. The low-pass PLL dynamics ensure that the multiplier develops an average detector voltage proportional to the phase error between the fundamental frequencies of its inputs: all other sum or difference frequencies are effectively attenuated.

With proper selection of gains, the PLL will apply negative feedback to drive its phase error to zero, producing a quadrature replica of the fundamental AC resonator current even when this current is dominated by harmonics.

Multiplier 1 accepts at its inputs the phase-lock replica of the fundamental AC tank-current waveform (shifted by 90° from the original), and a measurement of the AC tank voltage. Again, only the fundamental components of the the multiplier inputs produce an average output, a product in this case proportional to the phase difference between the Fundamentals of resonator voltage and current. Multiplier 1 has zero average output (zero error) for a 90° phase shift between its inputs, or zero error for a 0° V-I phase relationship at the resonator. Because of the resonator's monotonic phase slope, loop gains with the proper sign always push the outer-loop VCO (and hence the controlled AC source) towards the resonator's tuning frequency (Phiney 2001).

CHAPTER SIX

SIMULATION RESULTS

Modern power components are designed and analyzed by using computer simulation as a tool for conducting transients and control studies. Simulation can be especially helpful about the dynamic behavior and interactions that are often not readily apparent from reading theory. Simulation is often chosen by engineers to study transient and control performance or to test conceptual designs, before the experiment of actual system (Ong, C., 1998).

In this chapter, design procedures of a buck converter are explained and applications are analyzed in three parts. The first part contains simulation of the resonant filter and its characteristic according to frequency. The buck converter and ripple attenuation with resonant filter are simulated in the second part. Finally, simulation of PLL feedback control to desired buck converter with resonant filter is done.

6.1 Resonant Circuit Filter Simulation

L-C resonant filter carries an important point in this study. The circuit as shown in Figure 6.1 is simulated to analyze ripple attenuation effect of the L-C resonant filter by using offset voltage which includes sinusoidal components.

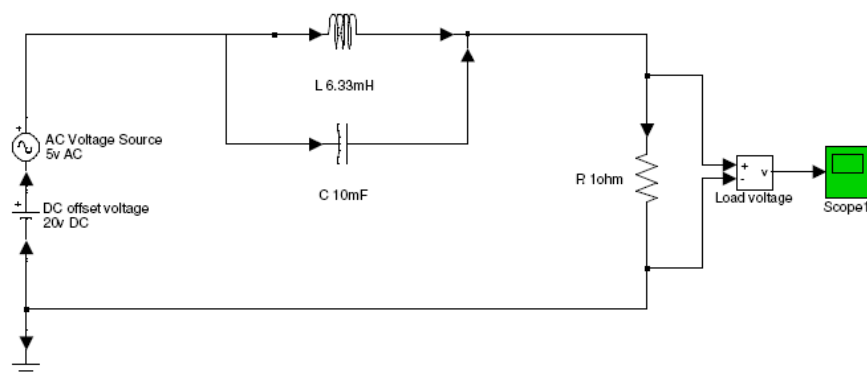


Figure 6.1 Simulink of a parallel resonance circuit

The characteristic analyze for the attenuation effect of the resonant circuit which is depend on the change of input frequency and/or change of component values caused by tolerances is performed below. This simulation gives feedback to the second and third part simulations.

The AC voltage source is fixed to 5V with frequency 20 KHz. DC voltage level is adjusted to 10V and the output resistance is taken 1 ohm.

The resonance frequency is 20 KHz so the resonant filter capacitor and inductor values are calculated from Chapter 5 Equation 5.5;

$$\omega = \omega_0 = \frac{1}{\sqrt{LC}} \quad (6.1)$$

$$20000 \times 2 \times \Pi = \frac{1}{\sqrt{LC}} \Rightarrow 125663 = \frac{1}{\sqrt{LC}} \quad (6.2)$$

For resonance $L=6.33\mu\text{H}$ and $C=10\mu\text{F}$ is adjusted.

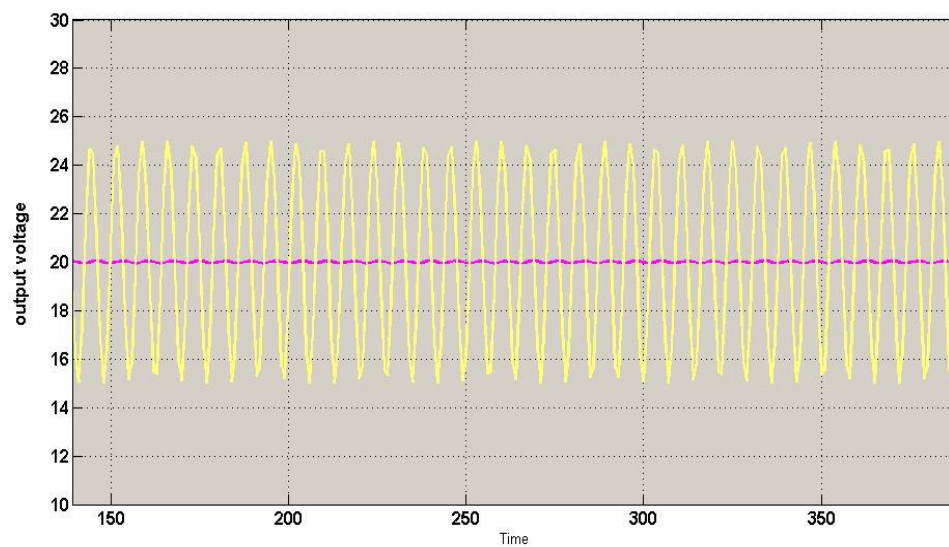


Figure 6.2 The waveforms of output voltage with and without resonant filter.

The figure 6.2 shows that all ac components are blocked when the parallel resonant filter is driven at resonance frequency. So only dc offset voltage remains at the output voltage.

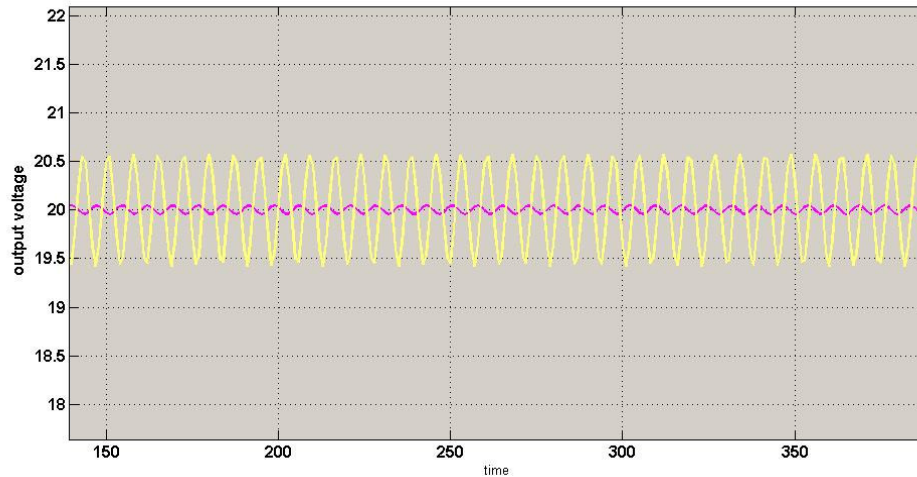


Figure 6.3 The waveforms of output voltage when AC voltage frequency is change to 20200Hz and at resonance frequency 20000Hz.

If there is any change of driving frequency, the resonant filter begins to loss its attenuating effect as seen in figure 6.3.

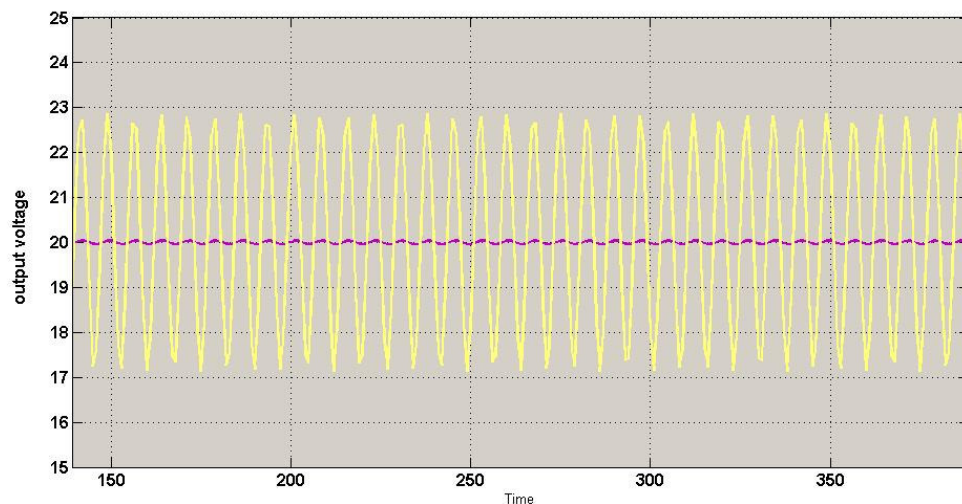


Figure 6.4 The waveforms of output voltage when resonance circuit capacitance changes to $6\mu\text{H}$ and at resonance value $6.33\mu\text{H}$.

As already known, component parameters/attributes are depend on the ambient temperature or moisture etc. So, the change in the ambient conditions affects and changes the values of components. The figure 6.4 shows that the resonance frequency of the filter circuit is changed accordingly when the value of resonance circuit components is changed due to the ambient conditions. Besides, the attenuation effect of the LC circuit is affected due to the change of the resonance frequency and this causes that AC components may be passed through the filter.

From this analyze it seen that to provide resonance filtering all the conditions must be satisfied to resonance frequency operation.

6.2 DC-DC Buck Converter Simulation

Design of buck converter is depends on choosing switching frequency, switching circuit and filter components parameters according to needed output voltage and current levels.

In the thesis a design of buck converter that has 10 V output voltage level is studied .It is assumed that input voltage is DC 20V unregulated voltage. For this;

Duty ratio is adjusted as 50%. Because according to harmonic attenuation efficient performance is provided at this duty ratio.

Selection the switching frequency: switching frequency is chosen as a 20 KHz. 20 KHz and upper of these frequencies eliminate the acoustic noise and it provides optimal inductance and capacitance choosing levels.

As a switching element Mosfet transistor is selected. They provide the best performance at these frequencies and they can not affect much from operation conditions.

The inductor is chosen as 250 μ H and capacitor is chosen as 100 μ F to operate in continues mode and provide attenuation as a low pass filter.

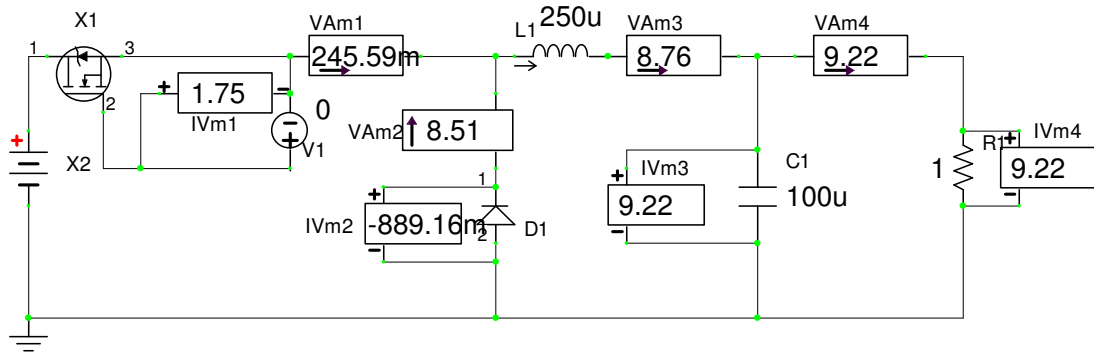


Figure 6.5 Dc-Dc Buck converter circuit without resonant filter.

Simulation results for 20 KHz:

The following results are obtained by simulating the circuit of figure 6.5 with the B2 Spice Simulation program.

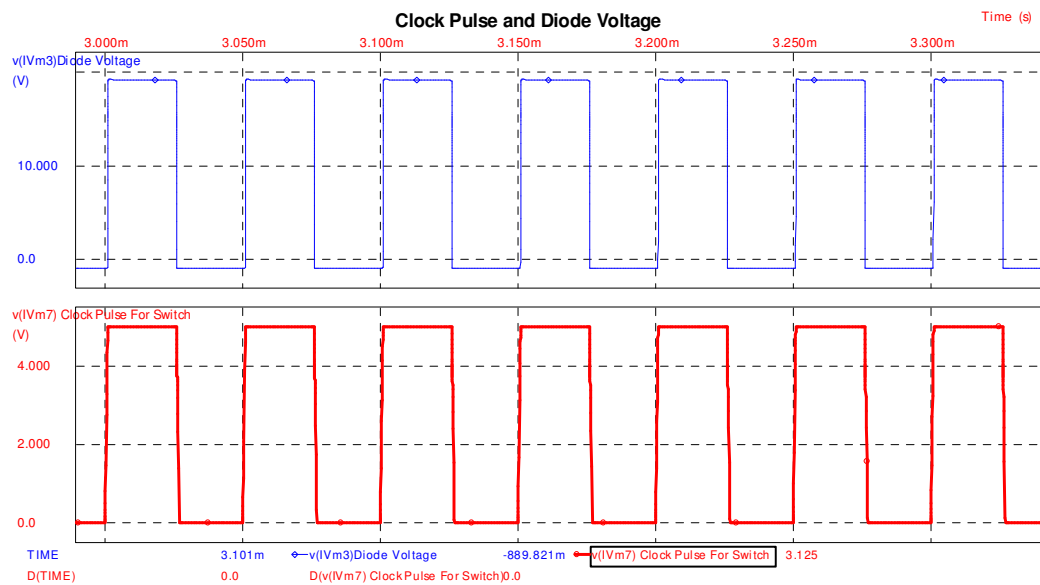


Figure 6.6 The waveforms of driving pulse and diode voltage.

According to Dc-Dc Buck converter operation clock pulse provides control to switching circuit. The diode voltage and clock pulse simulations are shown in Figure 6.6. When the clock pulse is on high level switching circuit is at on position and the input voltage is seen on diode. When the clock pulse is on low level switching circuit is at off condition and diode is forward biased according to stored inductor current and there is -0.6V drop on it.

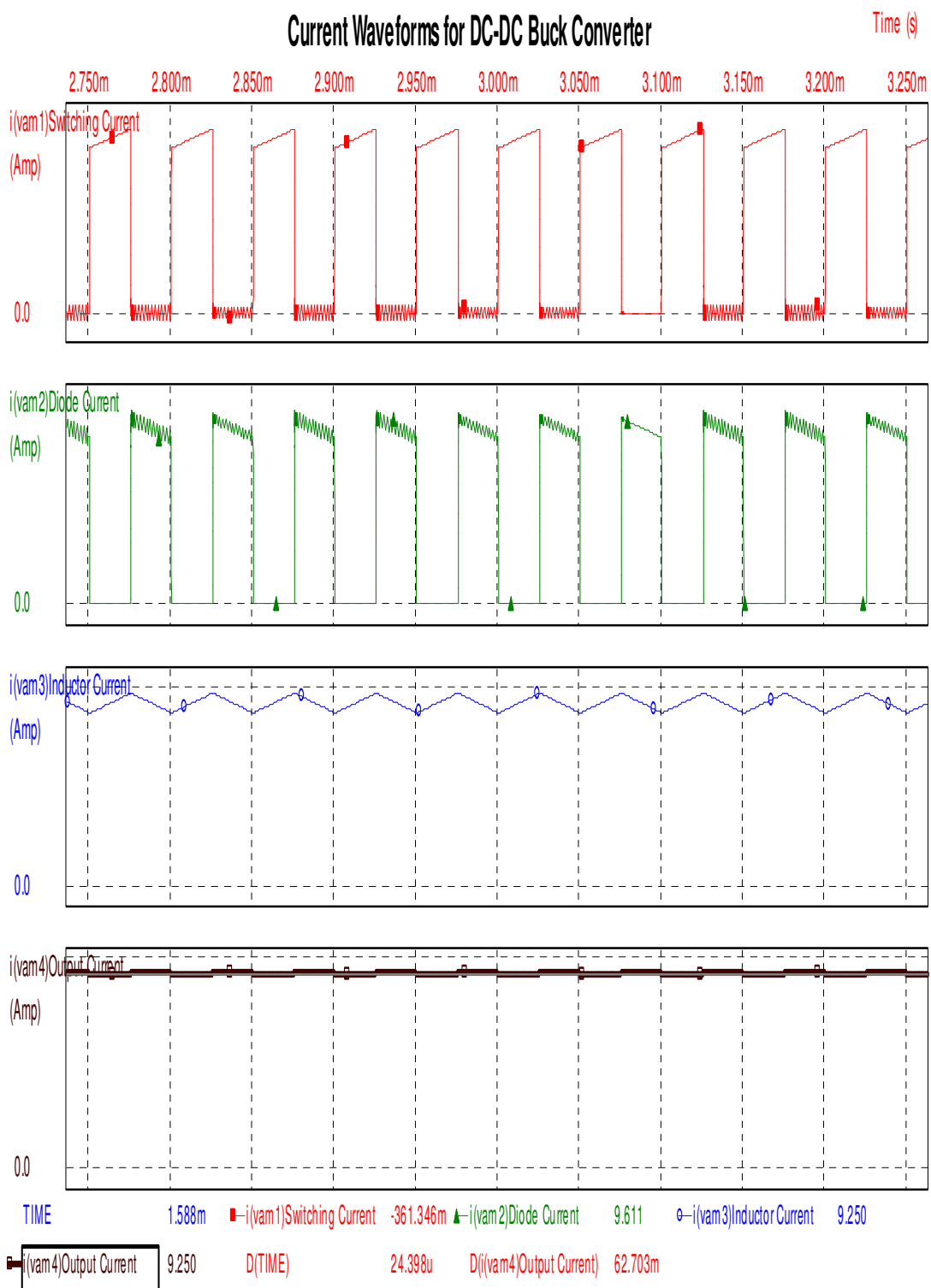


Figure 6.7 The waveforms of switching current, inductor current, diode current pulse, and the load current.

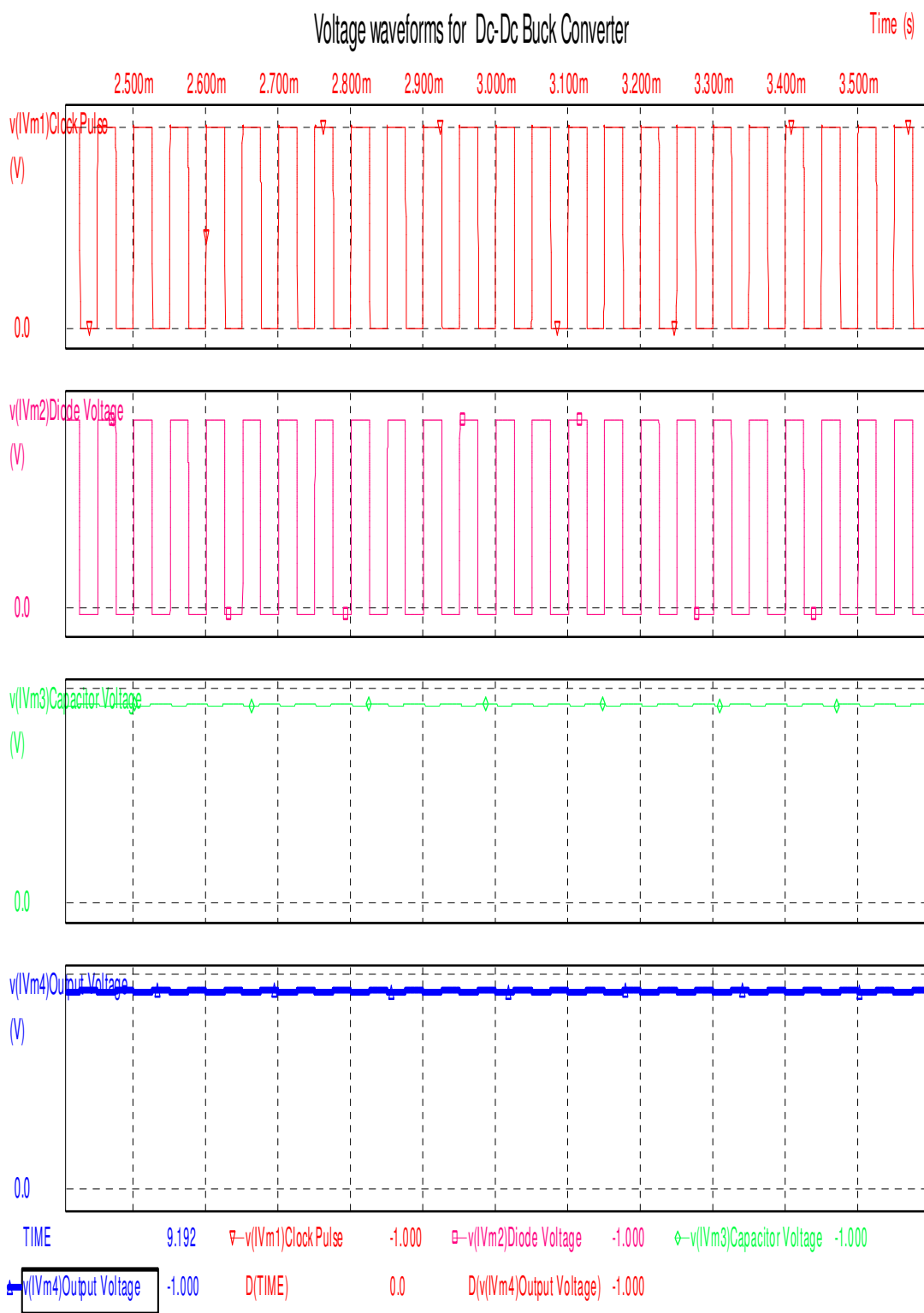


Figure 6.8 The waveforms of clock pulse voltage, diode voltage, capacitor voltage and the output voltage.

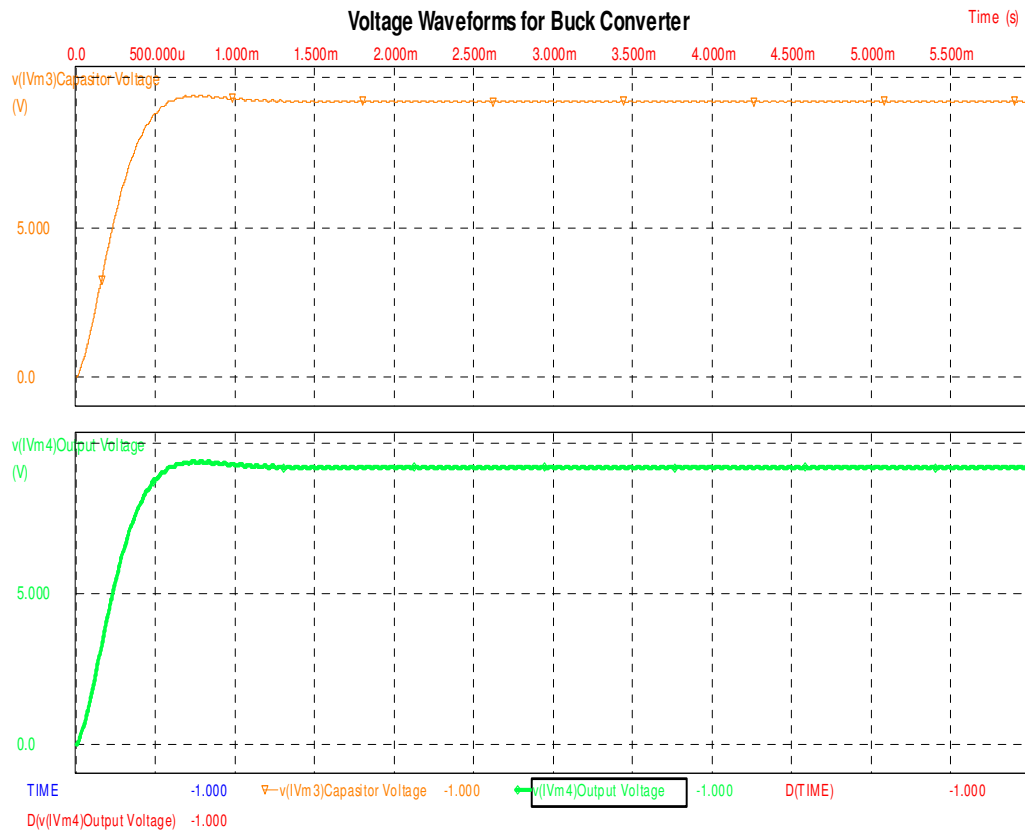


Figure 6.9 The transient waveforms of output voltage and capacitor voltage

In the analyze clock pulse with 5V amplitude is used as a driving signal. As seen from figure 6.7, figure 6.8 and figure 6.9 the buck converter operates in continues mode and it reaches to its steady state operations.

6.2.1 Resonant Output Ripple of Buck Converter

The Buck Converter output voltage is not pure dc voltage. There is an AC ripple component which is caused by switching frequency and its harmonics as seen from the simulation results of figure 6.10 and figure 6.11. These ripples are unwanted components and must be eliminated as possible.

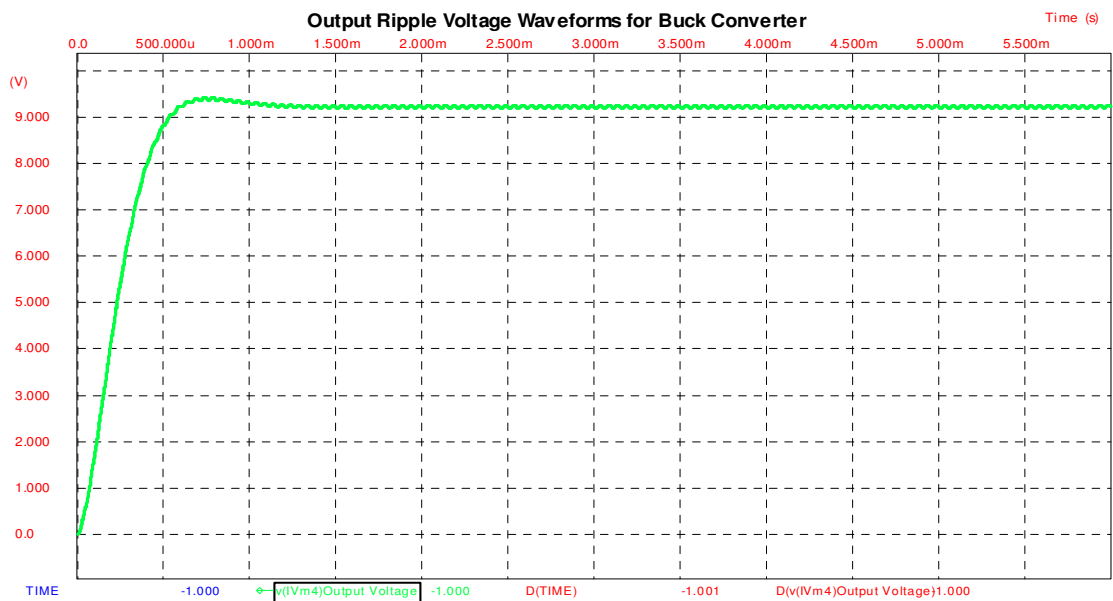


Figure 6.10 The waveforms output ripple voltages at transient.

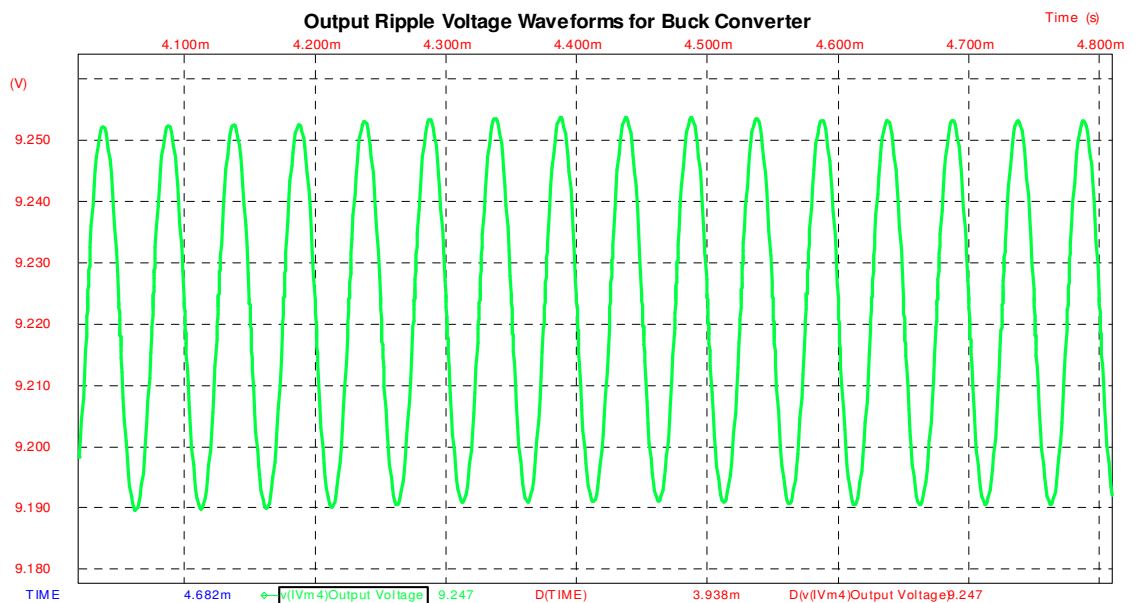


Figure 6.11 The waveforms of output ripple voltage at steady state conditions.

6.2.2 Simulation of Buck Converter with Resonant Filter

The resonant filter is designed to attenuate output ripple voltages as shown in figure 6.12. At resonance frequency the resonant filter effectively reduces the ripples (at the fundamental frequency) on the output voltages. The remaining ripples can be caused by third and other harmonic components.

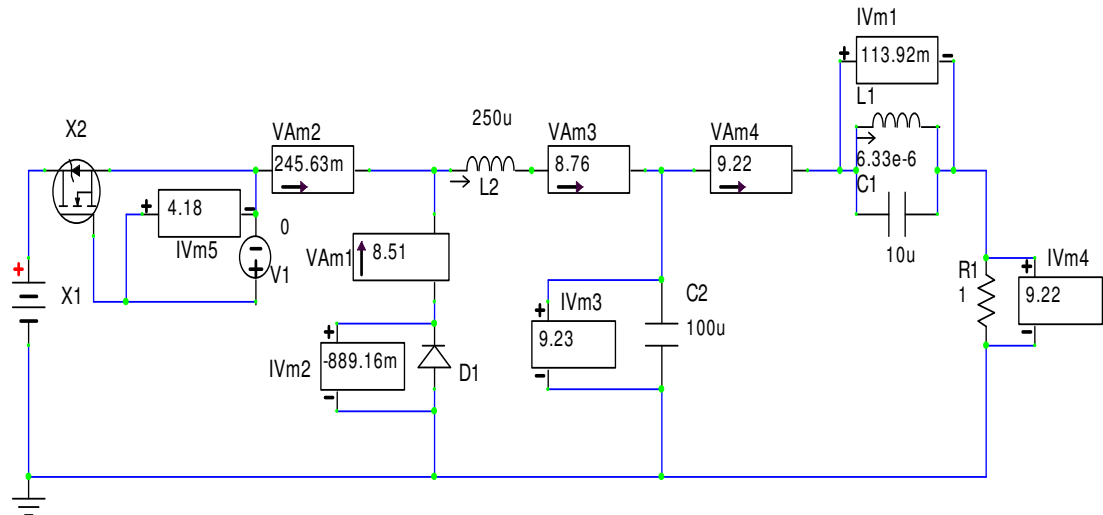


Figure 6.12 Dc-Dc Buck converter with resonant filter

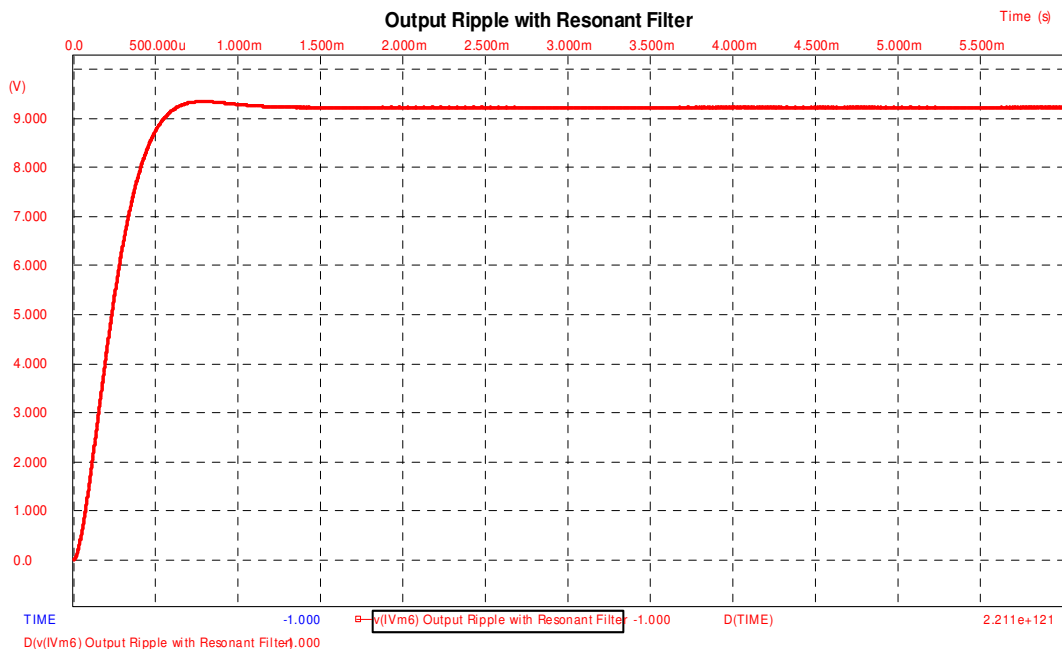


Figure 6.13 The waveforms of output ripple after resonant filtering of the circuit of figure 6.12.

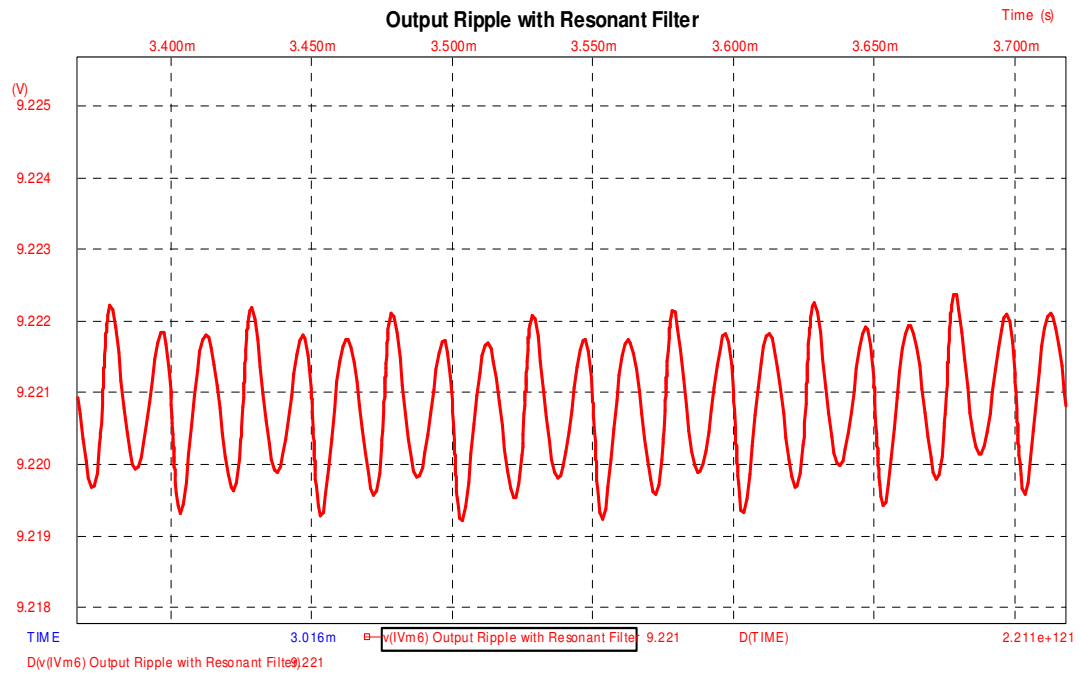


Figure 6.14 The waveforms of output ripple at steady state of the circuit of figure 6.12

The simulation result of figure 6.13 and figure 6.14 shows that with resonant filter the fundamental harmonic ripple attenuation is provided. There is small ripple which is caused by the combination other harmonic components.

To see the effect of resonant filter the simulation of figure 6.12 and 6.5 are madden together. The results of simulation are shown in figure 6.15 and 6.16 and as seen from the results the resonant filter effectively reduces the ripples.

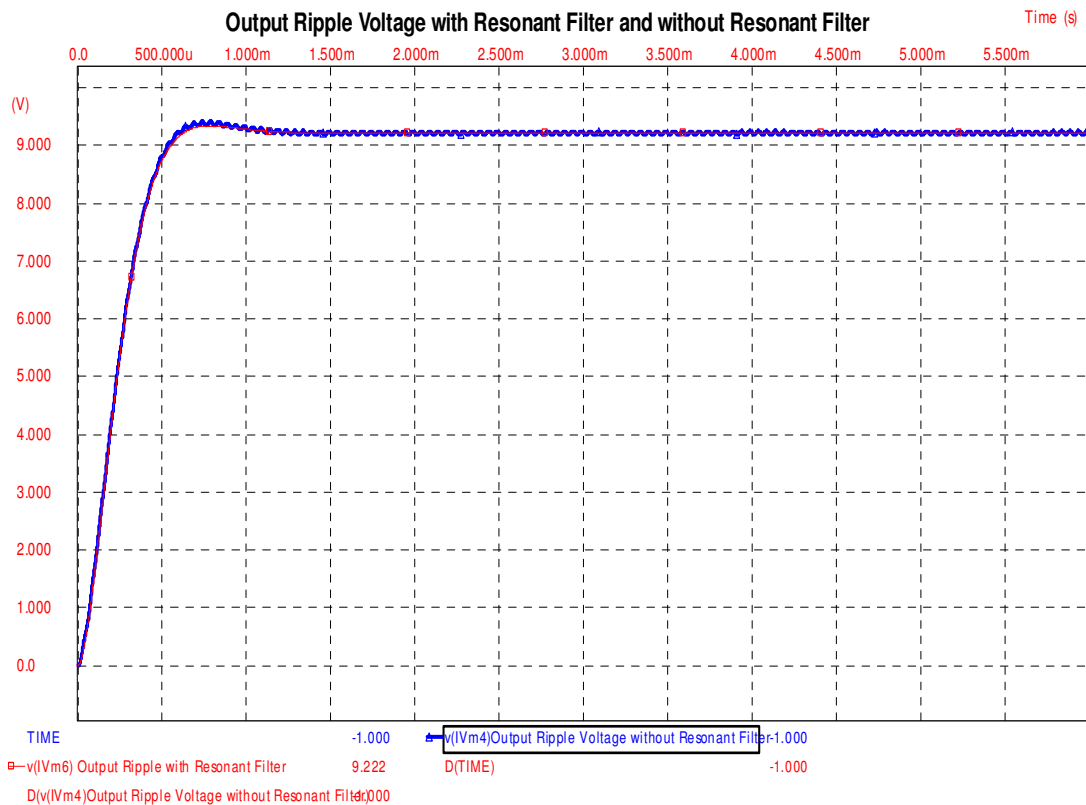


Figure 6.15 Comparison waveforms of output ripple with resonant and without resonant filter of the circuits of figure 6.5 and figure 6.12.

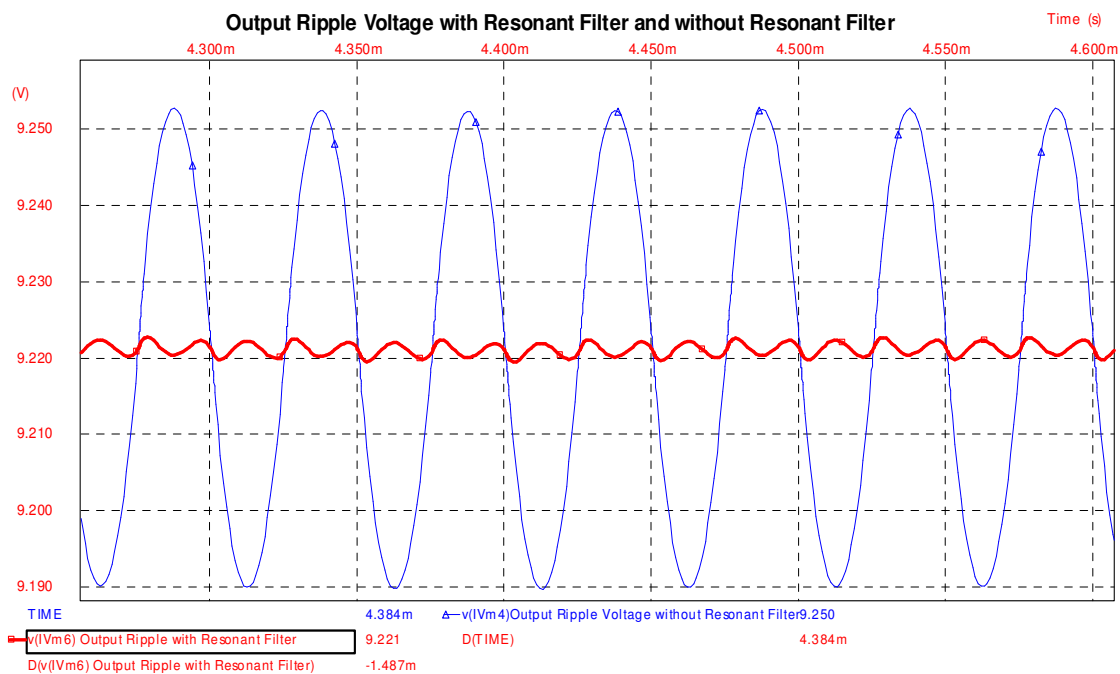


Figure 6.16 Comparison waveforms of output ripple at steady state with resonant and without resonant filter of the circuits of figure 6.5 and figure 6.12.

6.3 The PLL Control of Resonant Filter and Driving Frequency

It is important keeping the switching frequency at resonance frequency to use effectively the resonant filter. Because of this, switch mode converters with parallel resonant filter needs a frequency control circuit. According to this purpose PLL control circuit is used in this project as with most of similar applications (Hamill, 1998)

In this study resonant filter is designed before the load. Resonant filter provides attenuation of ripples which are on the capacitor. At resonance frequency resonant filter attenuates the ripples on capacitor and there is no phase difference between capacitor ripple voltages and resonant filter voltages.

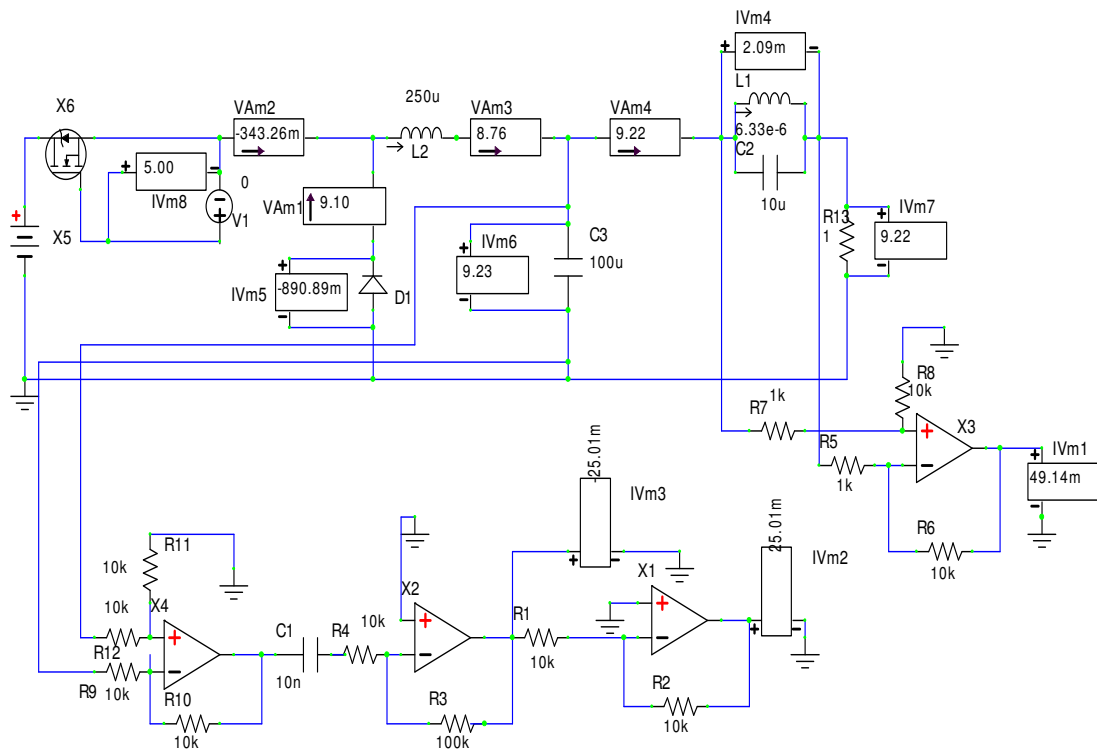


Figure 6.17 Dc-Dc Buck converter circuit for phase control.

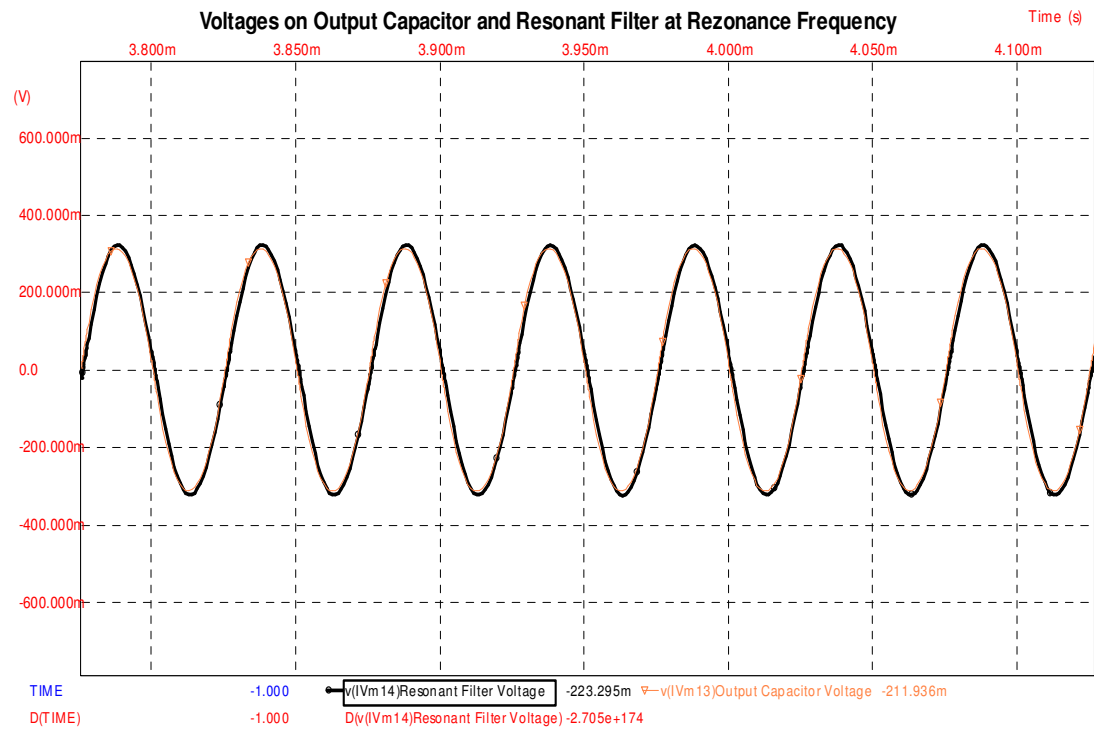


Figure 6.18 The waveforms of phase differences between resonance network and output capacitor voltage at resonance frequency (20KHz)

If the resonance filter is driven by resonance frequency the ripple voltages on capacitor and resonant filter are at same phase and magnitude as seen from figure 6.18. This means all the ripples are blocked by the resonant filter.

But if there is any frequency change or resonant filter components value change there appears a phase differences between the voltage phases as seen figure 6.19 and Figure 6.20. In this case resonant filter could not attenuate all the ripples and at the output voltage there occur a more ripples.

The comparison the output ripple voltages at resonance and without resonance are shown in figure 6.20. As it seen there is a significant difference between the output ripple voltages.

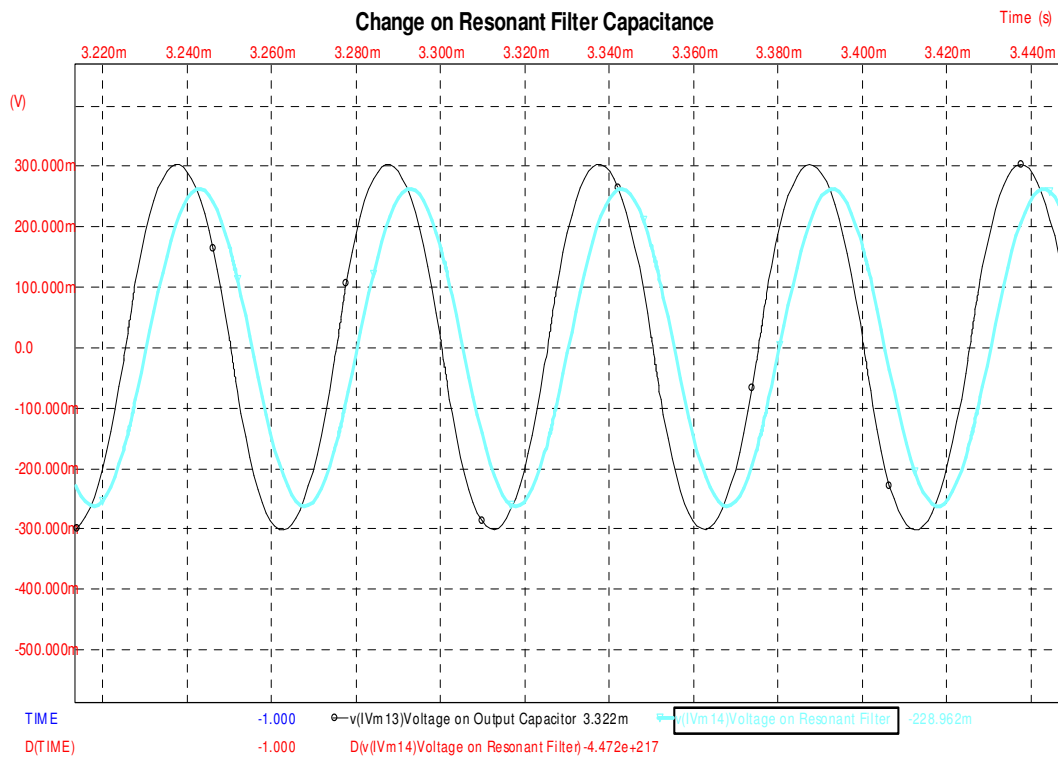


Figure 6.19 The waveforms of phase differences between resonance network and output capacitor voltage when the capacitance value is change to 15uF.

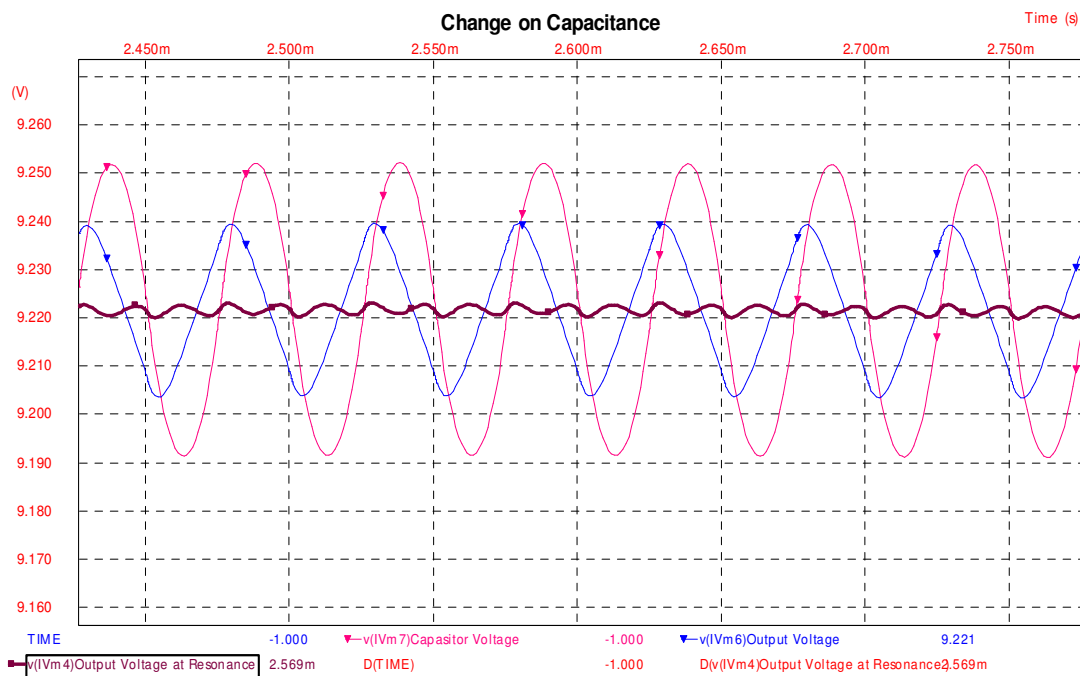


Figure 6.20 The waveforms of phase differences between resonance network and output capacitor voltage when the capacitance value is change to 5uF.

In this study a phase control between the resonant filter voltage phase and output capacitor voltage phase is provided. With this application a continually resonance frequency detection is fulfilled. The PLL application controls the frequency as Figure 6.21.

There is an Exclusive-Or Phase Detector which checks the phase differences between resonant filter and output capacitor voltage. By using opamp circuits as comparator the digital inputs for exclusive or gate is provided. Exclusive-Or phase detector gives output voltage according to phase difference. To control if the signal phase is lagging or lead it is fulfilled to lock at 90° phase difference. This is provided by the integrator circuit as a low pass filter. The integrator non inverting input is adjusted to half of exclusive-or reference voltage. In this case the integrator output voltage doesn't change at lock range when the phase difference is 90° . Finally VCO produces a driving signal by changing its frequency according to integrator output voltage which is produced by phase error signal.

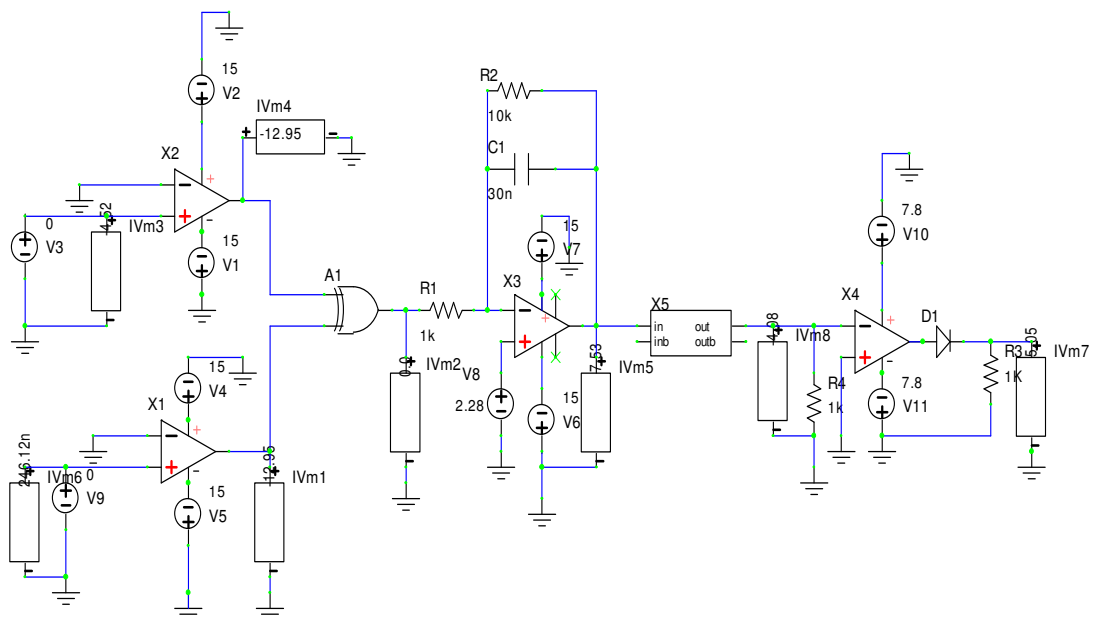


Figure 6.21. PLL with exclusive-or phase detector.

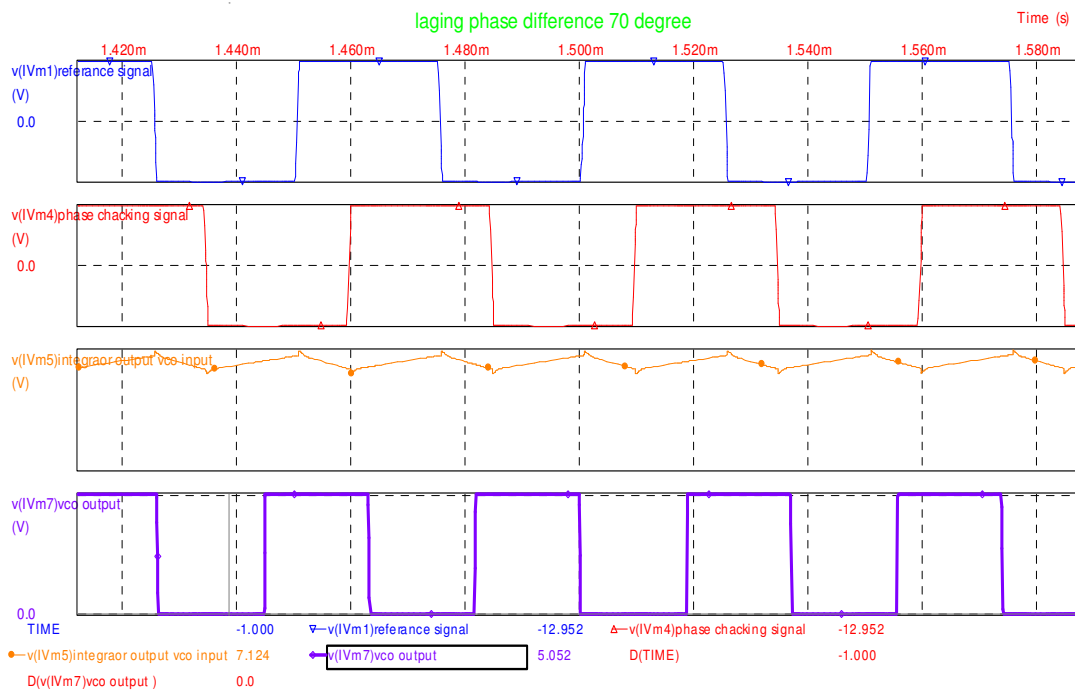


Figure 6.22 Phase detector input output waveforms at 70 degree lagging

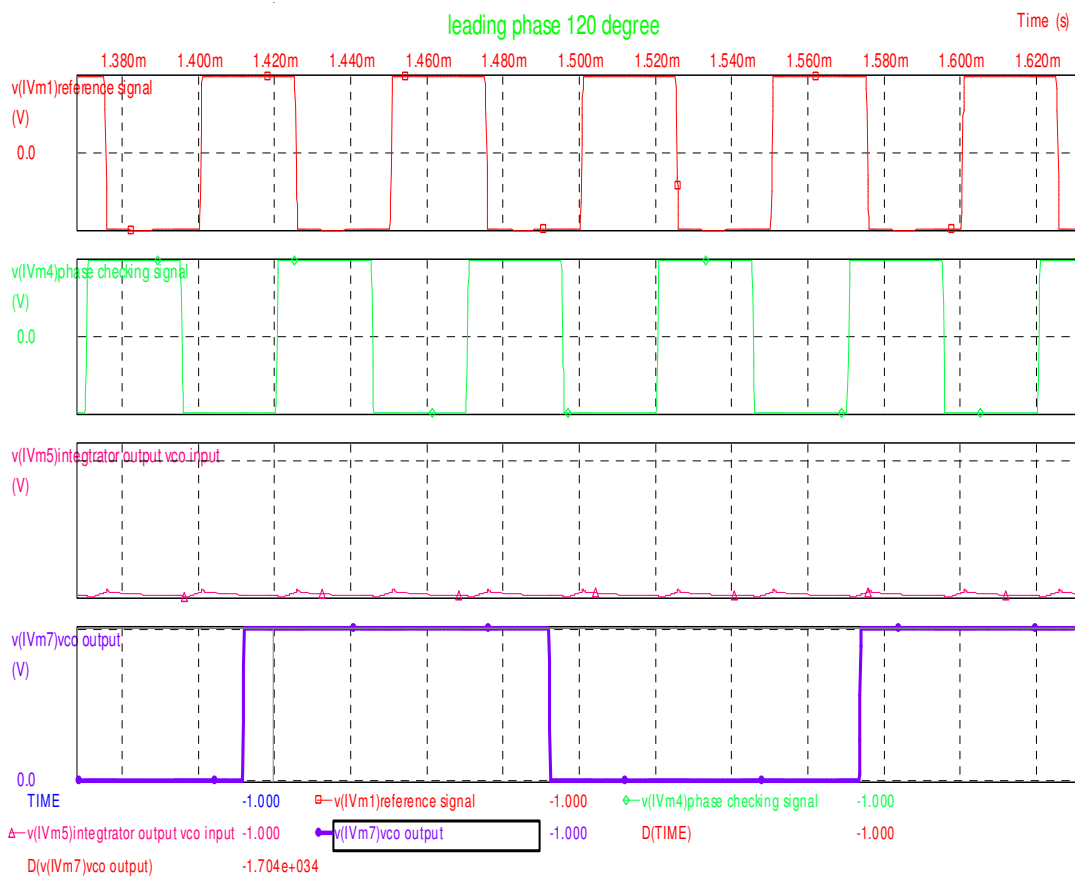


Figure 6.23 Phase detector input output waveforms at 120 degree leading.

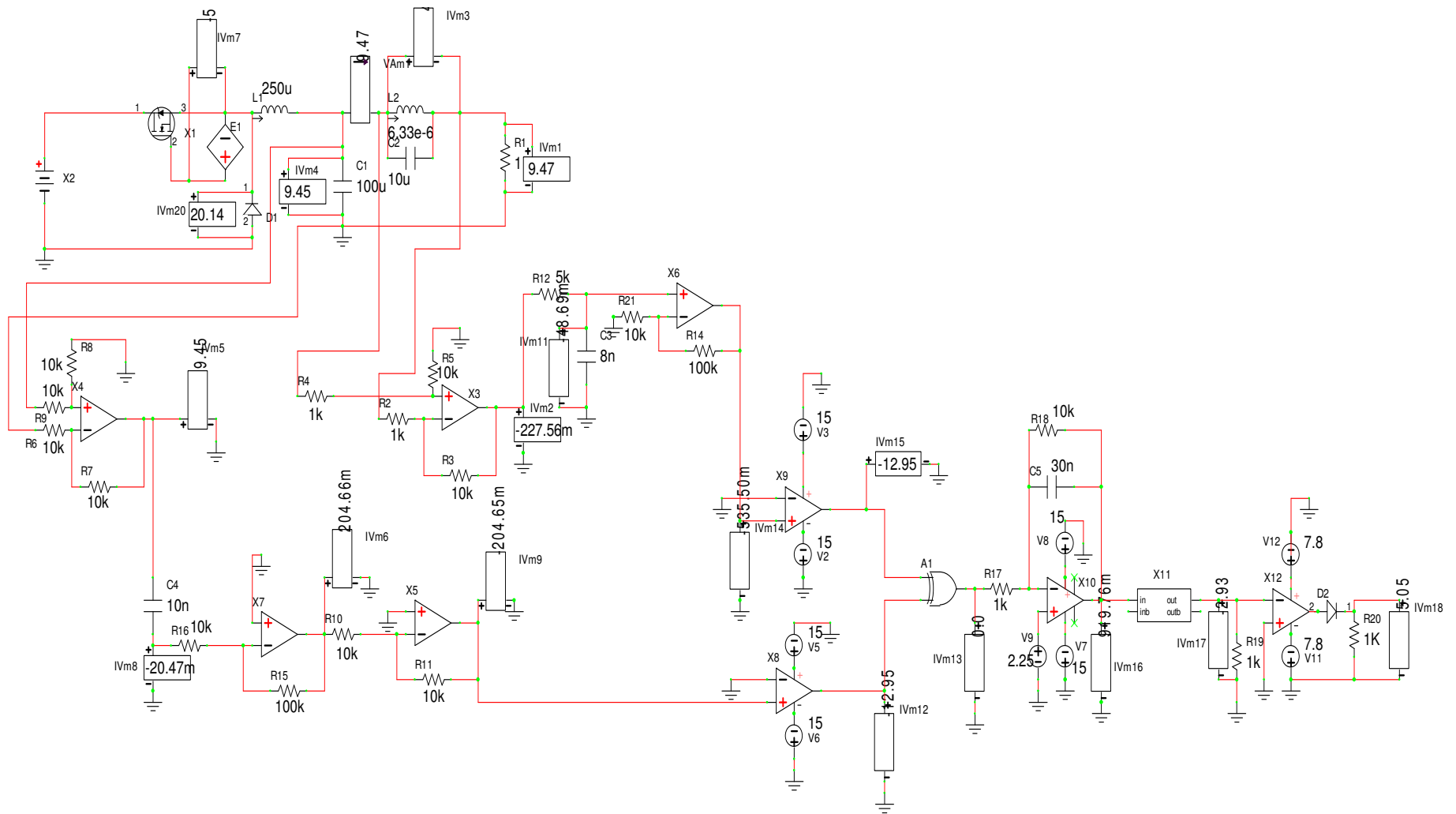


Figure 6.24 A PLL control of switching frequency in a way that it tracks resonant frequency of the filter.

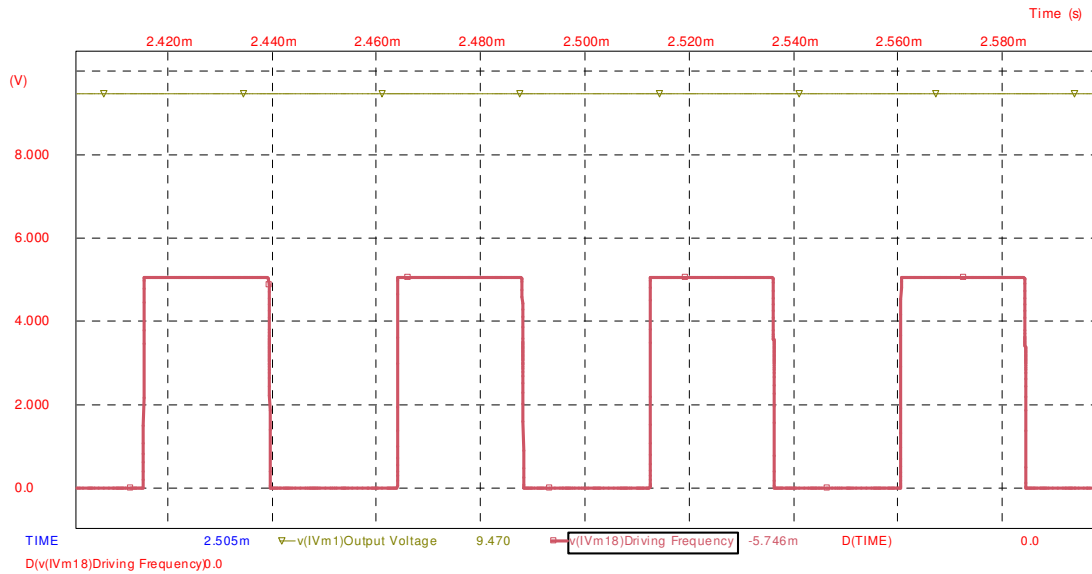


Figure 6.25 PLL VCO Output Driving Frequency and Output voltage when the Capacitor value is 10uF.

If there is not any change on capacitor or inductor values the resonant frequency remains on 20 KHz.

From the simulation results of figure 6.25 the PLL VCO output voltage locks at free running frequency 20 KHz which is the driving frequency for Buck Converter.

From figure 6.25:

$$\text{Period } T = 2.488 - 2.438 = 0.05 \text{ms} \leftrightarrow \text{Frequency is } 1/0.05 = 20 \text{KHz}$$

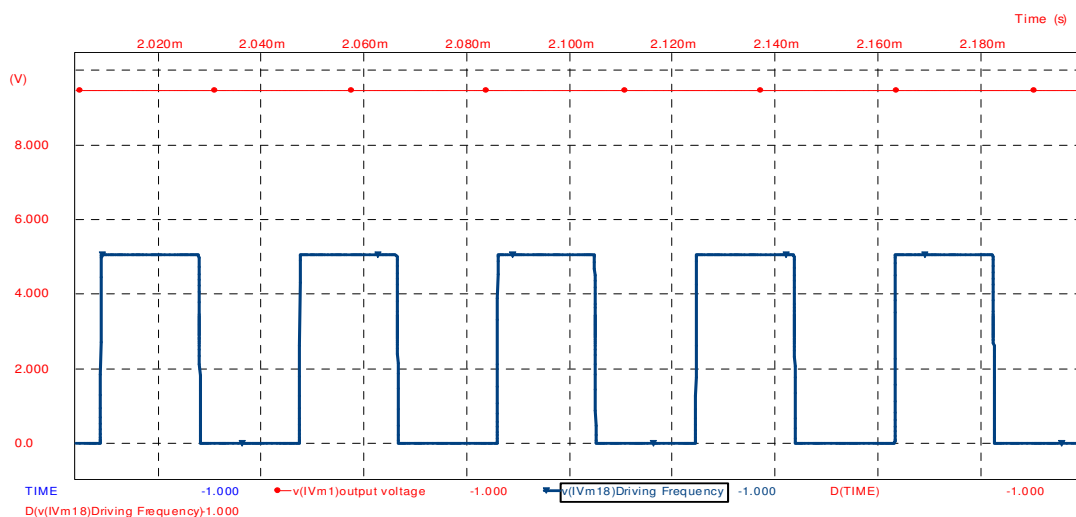


Figure 6.26 PLL VCO Output Driving Frequency and Output voltage when the Capacitance value is change to 5 uF

When the capacitor value is change to 5uF the resonance frequency of resonant filter is change to:

$$\omega_o = 1/(LC)^{1/2}$$

$$\omega_o = 1/(5\mu\text{F} * 6.33\mu\text{H})^{1/2}$$

$$\omega_o = 177751$$

$$f_o = 28\text{KHz}$$

From figure 6.26 the lock frequency of PLL feedback can be calculated as

$$\text{Period } T = 2.065 - 2.030 = 0.035\text{ms} \leftrightarrow \text{Frequency is } 1/0.035 = 28\text{KHz}$$

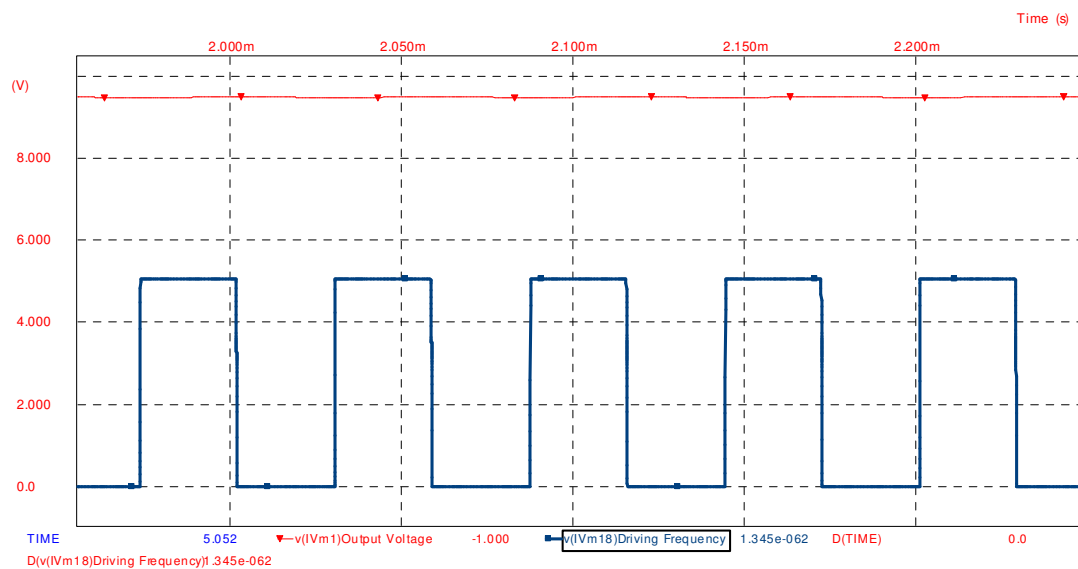


Figure 6.27 PLL VCO Output Driving Frequency and Output voltage when the Capacitance value is change to 15 uF

If the capacitor value is change to 15uF the resonance frequency of resonant filter is change to

$$\omega_o = 1/(LC)^{1/2}$$

$$\omega_o = 1/(15\mu\text{F} * 6.33\mu\text{H})^{1/2}$$

$$\omega_o = 102624$$

$$f_o = 16.7\text{KHz}$$

From figure 6.27 the lock frequency of PLL feedback can be calculated as

$$\text{Period } T = 2.062 - 2.002 = 0.06\text{ms} \leftrightarrow \text{Frequency is } 1/0.06 = 16.6\text{KHz}$$

The simulation results show that there is closed loop Feedback Control which controls the Buck converter driving frequency as the resonance filter resonance frequency. In this case the continuous ripple attenuating is provided and there is no loss from any change.

The PLL feedback loop effect is analyzed by comparison of the circuit which has a PLL feedback control loop and the same circuit but has a constant driving frequency.

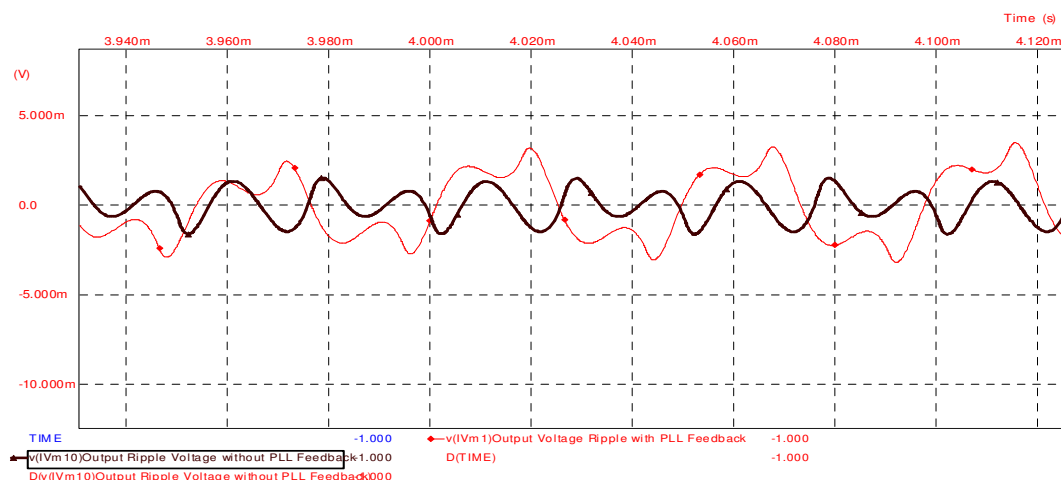


Figure 6.28 Output Voltage Ripples with and without PLL feedback control at resonance frequency (20 KHz)

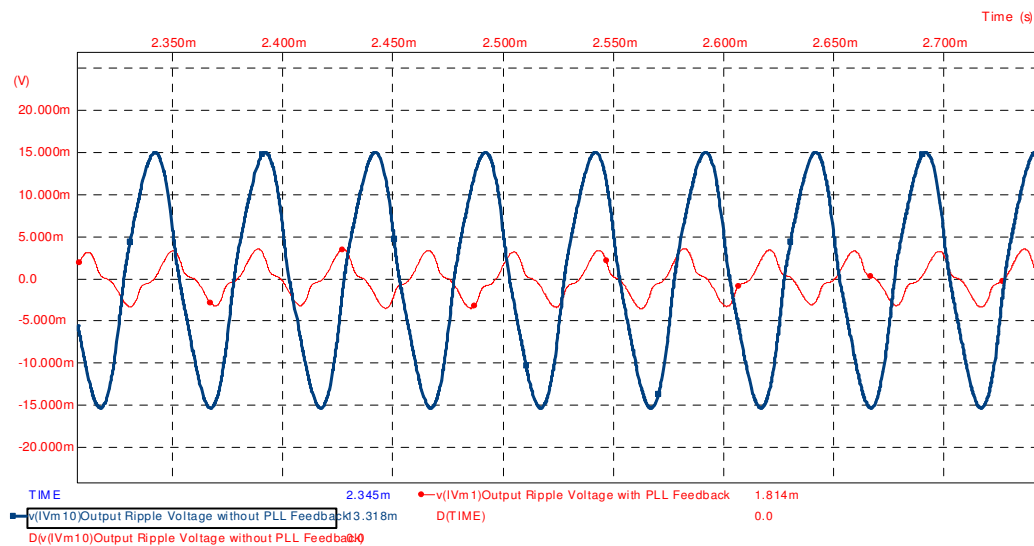


Figure 6.29 Output Voltage Ripples with and without PLL feedback control at reactance capacitor is 5uF.

The importance of PLL feedback control for attenuating the ripples is shown in figure 6.28 and 6.29. If there is not any change on operation condition the fundamental

ripple harmonic are eliminated by both circuits and there is a little ripples as seen from figure 6.28. If the operation conditions are change like capacitor value to 5uF the circuit which has no feedback control begins to lose its attenuation effect of the ripples as figure 6.29. But with PLL feedback control the resonance frequency is controlled and continuous ripple attenuation is provided.

6.4 Simulation Circuits with Matlab

In this study the Matlab simulations are realized similar to Spice. There is obtained the same results as previous B2 Spice simulation and here only the simulation circuits with the basic results are given.

There is an Analog Multiplier as a Phase Detector which checks the phase differences between resonant filter and output capacitor voltage. The low pass filter attenuates a higher frequency component according to production of multiplier. Gain units increase the value which is caused by phase difference error signal. Finally VCO produces a driving signal by changing its frequency according to phase error signal.

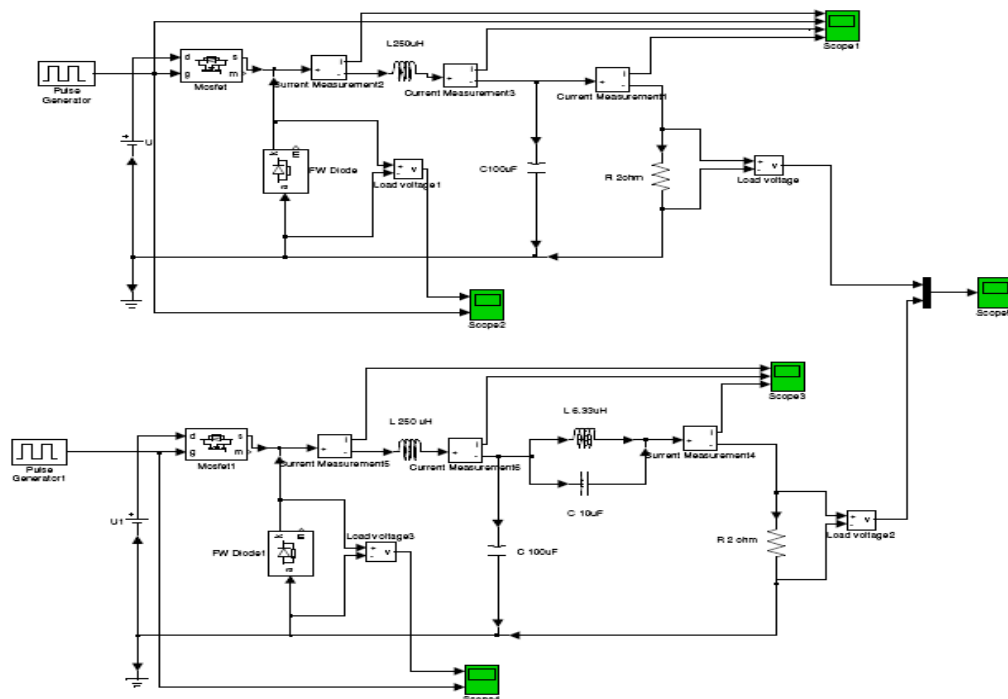


Figure 6.30 Buck converter circuits with and without resonant network.

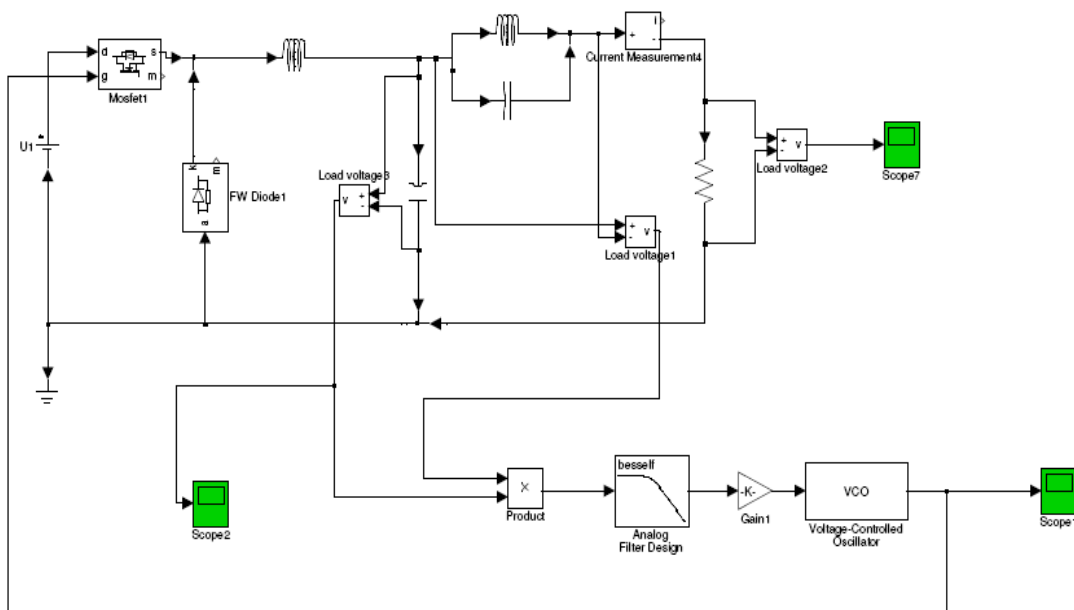


Figure 6.31 A PLL control of switching frequency in a way that it tracks resonant frequency of the filter.

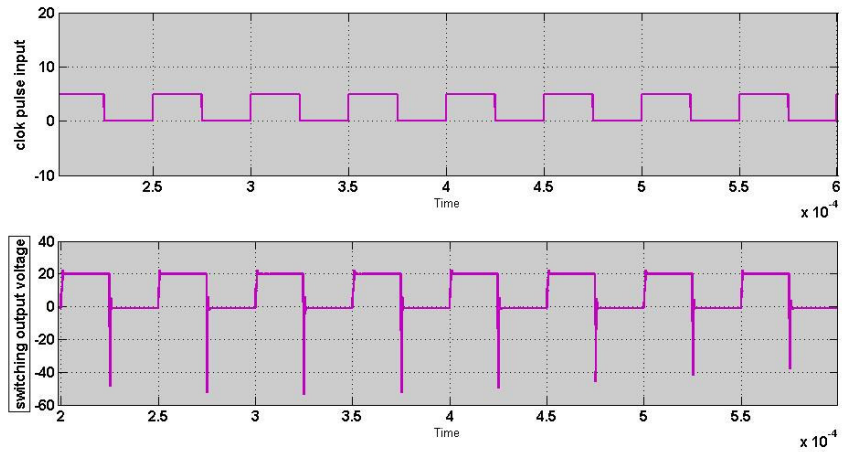


Figure 6.32 The waveforms of driving pulse and diode voltage.

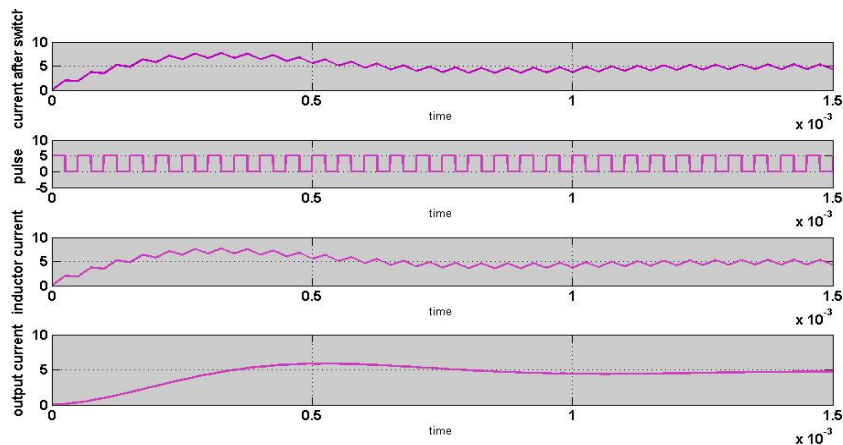


Figure 6.33 The waveforms of inductor current driving pulse, and the load current

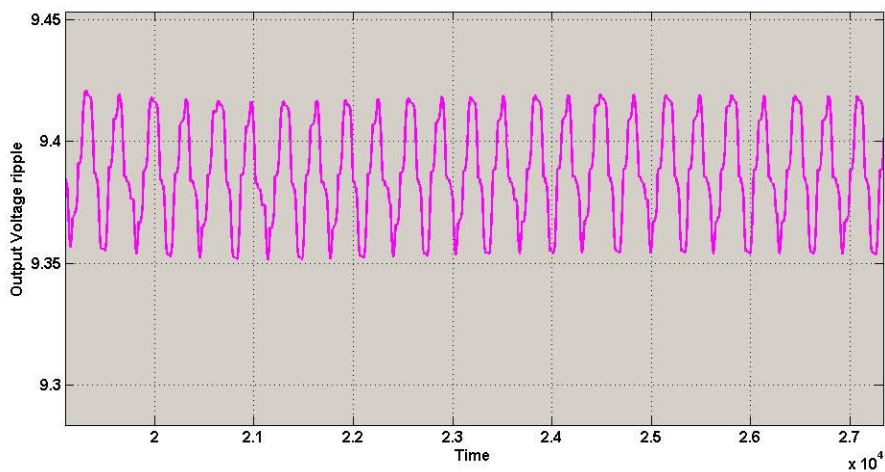


Figure 6.34 The waveforms output ripple

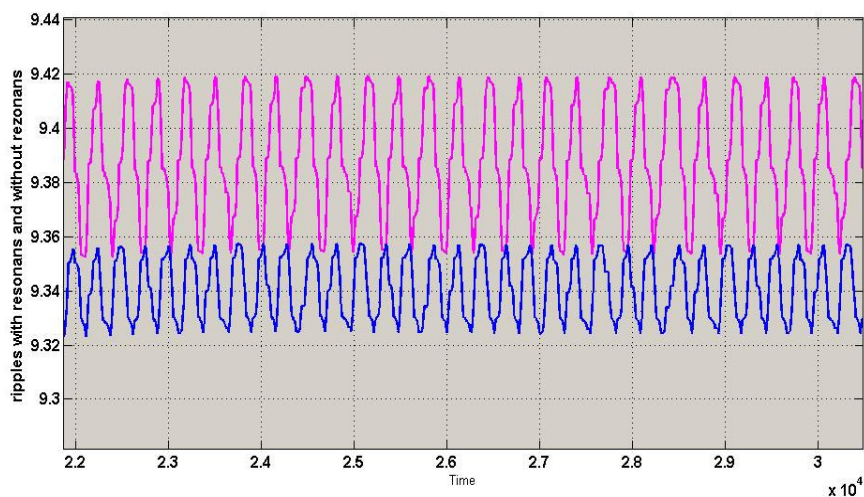


Figure 6.35 Comparison waveforms of output ripple with resonant and without resonant filter.

CHAPTER SEVEN

CONCLUSION

Switched Mode DC-DC Converters have most advantages according to linear power converters. They provide high efficiencies, reduction of component size and less power consumption. But there is a problem in the increased noise present at both input and output of the supply due to the power switching techniques. This noise is known as ripple voltages. The most application circuits need a pure dc voltage levels to operate in its stable range. In the circuit design an important side effect could appear if there is an unwanted ripple on the output voltages.

This thesis study on to provide extra ripple attenuation on a switch mode DC-DC converter output. For this there is used an extra resonant network filter to provide attenuation at operating frequency. According to switching operation there occurs a lot of ripple harmonics. The most significant ripple is caused by the fundamental harmonic whose frequency is equal to switching frequency. It is seen that from simulations by adjusting resonant filter frequency to the switching frequency provide a substantial attenuation on the output voltage ripple of the converter.

Using resonant filter provide extra reduction the size and value of conventional low pass network to have same attenuation effect. Designs which do operate for smaller passive elements enjoy improved transient performance and, possibly, the replacement of large capacitors with less expensive, lower-value elements.

Resonant network can not provide good attenuation for ripple components if it is not tuned to resonance frequency. To ensure the resonant filters resonance frequency equal to switching frequency a Phase Lock Loop control circuit is used. The phase-lock system tuning is general means of controlling the phase relationship among arbitrary frequency components of periodic signals, and has broad utility beyond power-filtering applications. Resonant networks resonant frequency and switching frequency phases are compared and controlled by PLL circuit. In the thesis the PLL

provides feedback to the switching driving circuits. With this feedback resonant network was satisfied to provide usually attenuation on switching frequency.

By using MATLAB and B2Spice software's the attenuation effect of resonant network is simulated. The analysis is made in three part resonant network filter, DC-DC Buck converter and PLL feedback driving circuits. One of the results of the study is that duty cycle has an importance on the resonant filter attenuation level. Theoretical this can be explained by the Fourier series expansion of the switched voltage waveform. When the Duty-Cycle of the waveform is around 0.5 the fundamental component dominates and also 2nd harmonic has low amplitude. On the other hand when D differs much from 0.5 fundamental component magnitude decreases relatively and 2, 3...harmonic voltage amplitudes increases. Since the resonant filter is designed for fundamental component caused ripple voltages. Its effectiveness obviously decreases when D increases or decreases from D=0.5.

For this reason the converters in conjunction with resonant filters as in this study should be designed in a way that D should get values around D=0.5.

REFERENCES

- Adamson, T. A. (1992). *Electronic Communications (2nd ed.)*. New York. Delmar Publishers Inc.
- Anonymous, (2002). *Switch Mode Power Supplies Reference Manual and design Guide On Semiconductor*. Retrived July 2004 from <http://onsemi.com>.
- Best R. E. (1997) *Phase-Locked Loops (3rd Ed)*. New York. McGraw-Hill.
- Connelly, J. A. (1988) An overview of the phase-locked loop (PLL.) *Philips Semiconductors Application Note, AN177*
- Cyril W. Lander (1993). *Power Electronics (3rd. Ed)*. New York Mc Graw Hill.
- Erickson R., (1998) DC-DC Power Converters. *Tutorial article in Wiley Encyclopedia of Electrical and Electronics Engineering*.
- Harts, D. W. (1997). *Introduction to Power Electronics*. New York. Prentice-Hall.
- Hamill D. C. (1988) Phase Locked in Induction Heating Inverter Employing Power Mosfets *Electronic Letters 31st March 1988 Vol. 24 No. 7*
- Keng W C (2005) *Switch Mode Power Converters*. New York. Academic Press
- Lindsey W.C. & Chie C.M.,(1985) *Phase-Locked Loops*. New York.IEEE Press
- Misra D.K (2001) *Radio Frequency and Microwave Communication Circuit*, John Wiley&Sons, Inc
- Mohan, N.,& Undeland, T. M.& Robbins, W. P. (1989). *Converters, Applications, and Design*. John Wiley & Sons.

- Nash G,(1994). Phase Locked Loop Design Fundamentals.*Application Note AN535, Motorola, Inc.*
- Phinney J. W. (2001) Filters with Active Tuning for Power Applications.*S.M. thesis, Dept. of Elect. Comput. Eng., Mass. Inst. of Technol., Lab. Electromagn. Electron. Syst., Cambridge, MA.*
- Pressman A I (1998). *Switching Power Supply Design (3rd Ed)*. New York McGraw-Hill
- Razavi B. (1996.).Design of monolithic phase-locked loops and clock recovery circuits. *IEEE PRESS Selected ReprintSeries, pp. 1–39, New York, NY: IEEE Press,*
- Severn R.& Bloom, E. (1995). *Modern Dc to Dc Switchmode Power Converter Circuit*. Van Nostrand Reinhold Company.
- Shirsavar S. A.(2004) Teaching Practical Design of Switch-Mode Power Supplies. *IEEE transection on education , Vol . 47, NO. 4,*
- Upadhye S. D. & Atre Y. R. (1998) “Determination of the design parameters of passive harmonic filters using nonlinear optimization,” in *Proc. 1998 IEEE Ind. Comm. Power Syst. Tech. Conf.*, pp. 155–164.
- Vithayathil J.,(1995) *Power Electronics Principles and Applications*, Mc Graw-Hill,
- Wolaver D. H. (1991) *Phase-Locked Loop Circuit Design*.Englewood Cliffs, New Jersey: Prentice-Hall.