DOKUZ EYLÜL UNIVERSITY
GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES

NEW APPLICATIONS OF CURRENT CONVEYOR

by

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İZMİR

NEW APPLICATIONS OF CURRENT CONVEYOR

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M.Sc. THESIS EXAMINATION RESULT FORM

We have read the thesis entitled **"NEW APPLICATIONS OF CURRENT CONVEYOR"** completed by **MEHMET İNCEKARAOĞLU** under supervision of **ASSOC. PROF. DR. UĞUR ÇAM** we certify that in our opinion it is fully adequate, in scope and in quality, as a thesis for the degree of Master of Science.

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NEW APPLICATIONS OF CURRENT CONVEYOR

ABSTRACT

As current-mode signal processing techniques improve, several active networks are being developed by using current conveyor in published literature. Amplifiers, filters and oscillators are the most famous applications of current conveyors. In this thesis, novel Differential Voltage Current Conveyor (DVCC) and Differential Difference Current Conveyor (DDCC) based immitance simulator circuits are proposed.

The main objective is the synthesis of immitance simulator circuits using single active device and minimum number of passive components. Taking advantage of the given methodology, DVCC and DDCC based Series and Parallel Immitance simulator circuits are proposed. As the application of constructed immitance simulator circuits, filter systems and parasitic cancellation circuits are built using the proposed immitance simulator circuits. Proposed Series R-L immitance circuits are applied in construction of current-mode second-order low-pass filter systems, whereas, proposed parallel R-L immitance simulators are used in order to build voltage-mode second-order high-pass filters. Besides, parallel (–R)-(–L) immitance simulator circuit is used in parasitic cancellation application. Simulations have been realized and results are expressed in terms of circuit performance.

The methodology in synthesis of immitance simulators is explicitely mentioned. For future work, by following the steps of the given methodology, synthesis of new immitance simulator circuits using new active devices will be possible**.**

Keywords: Current, conveyor, immitance, simulator, DVCC, DDCC

AKIM TAŞIYICI ELEMANININ YENİ UYGULAMALARI

ÖZ

Akım modlu devre uygulamalarının gelişmesiyle birlikte akım taşıyıcı tabanlı pekçok aktif devre uygulaması literatürde yerini aldi. Kuvvetlendiriciler, filtreler ve osilatörler bunların en önemlilerini oluşturmaktadırlar. Bu tez çalışmasında DVCC ve DDCC akım taşıyıcı elemanlarıyla özgün R-L imitans simülatör devreleri önerilmiştir.

Tezin temel amacı tek aktif eleman ve asgari sayıda pasif eleman kullanılarak imitans devreleri sentezlenmesidir Verilen metodolojiden faydalanılarak, DVCC ve DDCC bazlı paralel ve seri imitans devreleri önerilir. Önerilen devrelerin uygulaması olarak da filtre devreleri ve parazitik yokedici devreleri oluşturulur. Önerilen seri R-L imitans devreleri akım modlu ikinci dereceden alçak geçiren filtre uygulamasında kullanılırken, buna karşın, paralel R-L imitans devreleri ise gerilim modlu ikinci dereceden yüksek geçiren filtre uygulamasının oluşturulmasında kullanılır. Bununla birlikte önerilen paralel (–R)-(–L) devresi ise parazitik yokedici uygulamasında yer almaktadır. Simülasyonlar gerçeklenmiş ve devrelerin frekans cevabı kriter alınarak sonuçlar verilmiştir.

R-L imitans simülatör devrelerinin oluşturulması için kullanılan metod ayrıca açıklanmıştır. Geleceğe yonelik çalışmalar için bu metod takip edilerek, literatüre yeni giren farklı aktif elemanlarla özgün R-L imitans simülatör devrelerinin oluşturulması mümkün olacaktır.

Keywords: Akım, taşıyıcı, imitans, simülatör, DVCC, DDCC

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CHAPTER ONE

INTRODUCTION

1.1 Historical Background of Current Conveyors

Recent researches on integrated circuits and systems in last decade have presented a new trend in integrated circuit design which is regarded as "Current-Mode Signal Processing". Unlike in Voltage-Mode signal processing, current-mode signal processing techniques mostly focus on current that is to be used as input and output signals. As circuit designers show a dense interest to current-mode signal processing, new building blocks appear in academic papers. As an obvious result of these efforts, Current Conveyor was introduced in academic papers to be one of the most powerful building blocks for the future of current-mode signal processing (Smith&Sedra, 1968).

The first current conveyor was introduced by A.S. Sedra & K.C.Smith in 1968. However, at the time of the introduction, designers and researchers mostly dedicated their attention to op-amp based integrated circuits and systems. Recent development of current-mode signal processing makes this early invention an important item for today's analog integrated circuit design theory and practice. In 1970, A.S. Sedra and K.C. Smith introduced a more versatile building block named as CCII (Sedra&Smith, 1970) having many different features over CCI which no doubt made it a shining star for active network synthesis. By the year 1995, a new version of current conveyor named as CCIII was introduced (Fabre, 1995) which as well relies on the common current conveying approach behind the invention of CCI. All the mentioned conveyors and the derived conveyor types have been used in construction of many complex circuits and systems so far. For today, current conveyor can be regarded as one of the most famous building blocks for analog integrated circuit and system design.

1.2 Types of Current Conveyors

1.2.1 CCI

The current conveyor is a 3-port device whose black-box representation can be seen in figure 1.1. The device shows such an operational characteristic that if you apply a voltage to the terminal Y, the same voltage appears on terminal X. Similarly, if a current is forced to pass through terminal X, the same current is seen on terminal Y. Moreover, the same current is conveyed through terminal Z, behaving as a current source with high output impedance (Sedra, Roberts & Gogh, 1990).

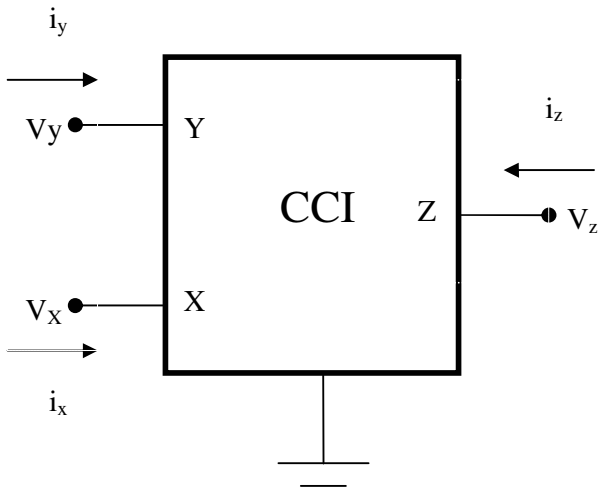

Figure 1.1 Black Box Representation of CCI.

The input-output characteristics of the CCI can be explained in terms of mathematical expressions (1.1). + sign in the matrix equation denotes CCI+ which implies both i_x and i_z flows into the device whereas – sign denotes CCI- in which an opposite polarity of output current i_z is assumed (Sedra, Roberts & Gogh, 1990).

$$\begin{bmatrix} i_y \\ V_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ i_x \\ V_z \end{bmatrix} \tag{1.1}$$

1.2.2 CCII

Second generation current conveyor which has a different implementation with an input node Y having infinite input impedance was introduced as the successor of CCI. As seen in figure 1.2, no current flows through terminal Y. This additional feature makes CCII a more versatile conveyor type when compared to CCI. CCII has proved to be a more useful building block than CCI over years. Published literature provides CCII realization for almost all known active network building blocks. (Sedra, Roberts & Gogh, 1990))

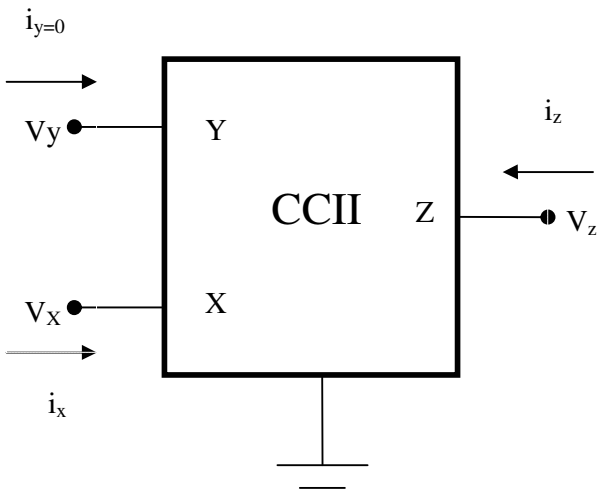

Figure 1.2 Black Box Representation of CCII.

The matrix equation (1.2) explicitly shows no current flowing into terminal Y. +/- sign in the equation identifies the polarity of the output current flowing through terminal Z. + sign in the matrix equation denotes CCII+ which implies both i_x and i_z flows into the device whereas – sign denotes CCII- in which an opposite polarity of output current i_z is conveyed to the output terminal Z (Sedra, Roberts & Gogh, 1990)

$$\begin{bmatrix} i_y \\ V_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ i_x \\ V_z \end{bmatrix} \tag{1.2}$$

1.2.3 CCIII

Third generation current conveyor being the newest current conveyor introduced is more like CCI in device functionality point of view. Black box representation is given in figure 1.3. Here it is seen that CCIII has no infinite input impedance node like CCII but provides a current having an inverse polarity to flow through terminal Y. Hybrid matrix equation for input-output relationship is given in (1.3).

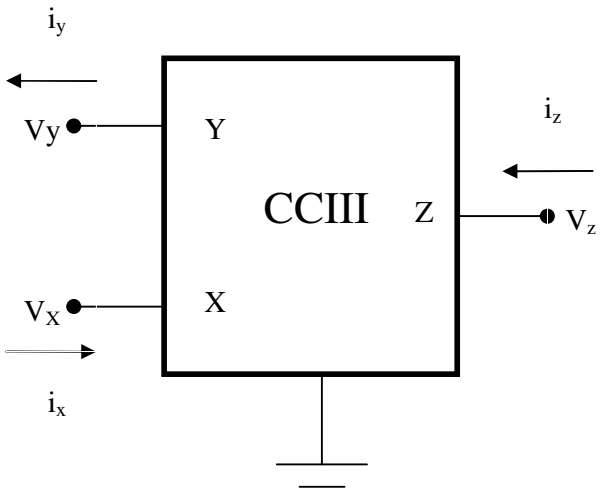

Figure 1.3 Black Box Representation of CCIII.

$$\begin{bmatrix} i_y \\ V_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ i_x \\ V_z \end{bmatrix} \tag{1.3}$$

1.3 Thesis Motivation and Aim of the Thesis

One of the most important items in active network synthesis is the realization of immitance functions by using active devices. Simulation of immitance functions is an important research area for analog integrated circuit design.

Immitance simulator circuits are constructed in order to realize special functions of series or parallel combinational circuits including resistive, inductive or capacitive elements. Especially designers often need to realize inductor function by using active elements. As integrated circuits and systems show improvement as a response to the

need of more powerful and more compact devices, it has become necessary to replace larger inductor elements with transistor based active simulator circuits. Taking the immitance circuits proposed in academic papers into consideration, it is not possible to realize a pure inductor function using a single well-known active device. Furthermore, in many cases, it is not a desirable approach to realize a pure inductive effect by using many active devices. Instead of this, realizing parallel or series combinations of resistive, inductive and capacitive elements by using transistor based active devices can be very useful because usage of the transistors gives designers more capabilities to change the equivalent input-output functions of the circuits.

As the result, taking all the mentioned points into account, realization of immitance simulator circuits by using active devices can be regarded as an important research area in analog integrated circuits and systems.

CHAPTER TWO

SYNTHESIS OF DVCC BASED NOVEL IMMITANCE SIMULATORS

2.1 Introduction of DVCC

2.1.1 Historical Background of DVCC

Differential Voltage Current Conveyor (DVCC) was proposed by H.O. Elwan and A.M. Soliman at 1997. DVCC is an extension of the second-generation current conveyor (CCII). CCII has proven to be a versatile building block which gives designers the opportunity to implement many high-performance circuits. However, since CCII has only one input terminal with infinite impedance, it does not allow the designers to construct circuits which are supposed to handle differential inputs by using a single CCII (Elwan & Soliman, 1997). Furthermore, one of the most efficient dual CCII based amplifier circuits proposed in academic papers which is supposed to handle differential input signals -despite its high Common Mode Rejection Ratio- brings a disadvantage as the result of the non-zero input impedance of X terminal of CCII (Elwan & Soliman, 1997).As the result, DVCC was proposed based on the idea of overcoming the disadvantages of having a unique high impedance input terminal

2.1.2 Black Box Representation of DVCC

DVCC is a five terminal device as given in fig 2.1. DVCC is a versatile building block specifically designed for floating inputs. Thus, it was formed up to have two distinct infinite impedance input terminals (Y1 and $Y_{2)}$ which allows no current flowing through Y terminals. As DVCC has mainly been designed for differential inputs, X terminal has the equal potential to the potential difference between terminals Y_1 and Y_2 (Elwan & Soliman, 1997).

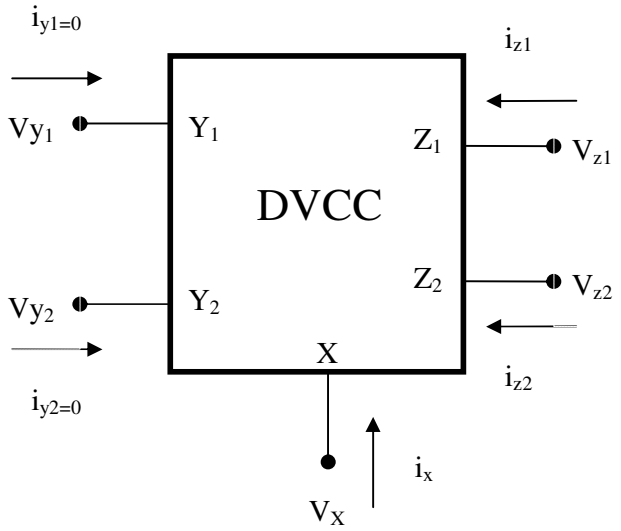

Figure 2.1 Black Box Representation of DVCC.

Regarding the current conveying functionality, current flowing through terminal X is conveyed to the dual Z terminal, one with identical and the other with inverse polarity as given in matrix equation (2.1).

$$\begin{bmatrix} V_x \\ i_{Y1} \\ i_{Y2} \\ i_{Z1} \\ i_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_x \\ V_{Y1} \\ V_{Y2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix} \tag{2.1}$$

2.1.3 CMOS Implementation of DVCC

Conventional CMOS implementation of DVCC is given in figure 2.2 (Elwan & Soliman, 1997). All FETs are operating in saturation region and the sources are connected to bulk/substrate.M17-M18 and M19-M20 pairs shift the Y inputs so that M1 is kept on steadily (Elwan & Soliman, 1997). Consequently,

$$V_{G2} - V_{G1} = V_{Y1} - V_{Y2} \tag{2.2}$$

Taking the current mirror formed by M6 and M7 into consideration,

$$V_{G1} - V_{S1} = V_{G2} - V_X \tag{2.3}$$

Since V_{S1} is grounded,

$$V_X = V_{Y1} - V_{Y2} \tag{2.4}$$

By taking advantage of the current mirrors formed by M10-M11and M12-M13 pairs, current flowing through Z_1 is mirrored to Z_2 terminal in an inverted form. Therefore, both DVCC- and DVCC+ are realized simultaneously.

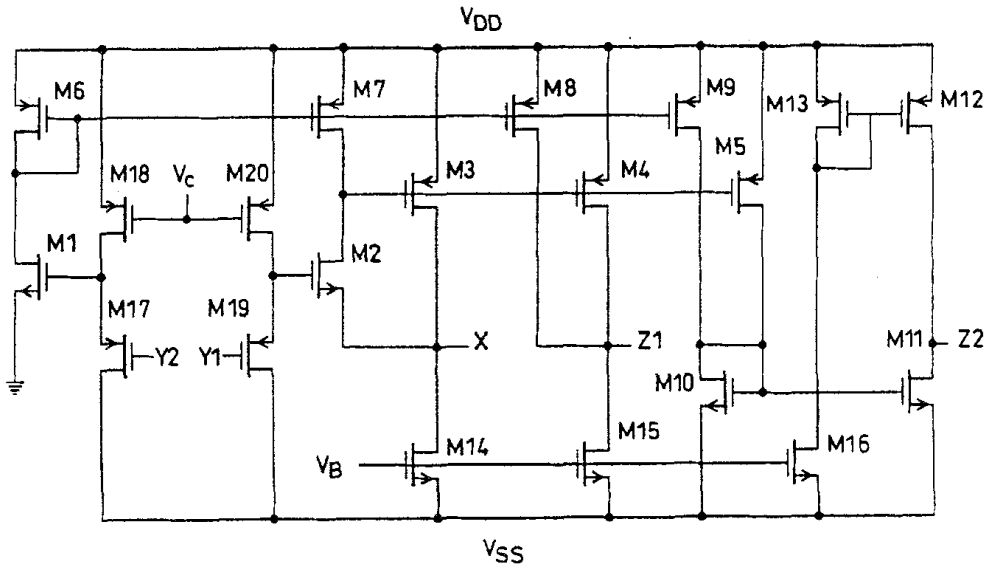

Figure 2.2 CMOS Implementation of DVCC.

2.2 Immitance Simulators Based on DVCC

2.2.1 Methodology in Construction of Immitance Simulators

In order to extract immitance simulator circuits using DVCC, a methodology in which all terminals of DVCC are connected to each other and to the ground with the specified passive components has been used. Ground connection is necessary because the methodology is mainly based on the synthesis of grounded immitance simulator circuits. Relying on the mentioned methodology, the admittance equivalents of the passive components are used to build up node equations. Note that the inverse polarity output Z has been neglected and left as floating in order to simplify the node equations and to reduce the number of passive components to be dealt with. The methodology to obtain immitance circuits is given below:

a. Every terminal of DVCC is connected to the other terminals and to the ground via a passive component whose admittance equivalent is given in table 2.1.

Table 2.1 Specified admittances of passive components

	V_{Y1}	V_{Y2}	V_X	V_Z	GND
V_{Y1}	-	Y_1	Y_2	Y_3	Y_4
V_{Y2}	Y_1	-	Y_5	Y_6	Y_7
V_X	Y_2	Y_5	-	Y_8	Y_9
V_Z	Y_3	Y_6	Y_8	-	Y_{10}
GND	Y_4	Y_7	Y_9	Y_{10}	-

b. One of the terminals of DVCC is specified as the input node of immitance simulator to represent the V_{in} of the equivalent circuit of grounded immitance simulator given in figure 2.3.Note that, only one of the terminals of DVCC should be considered to be the input node as seen in figure 2.4 with the dashed lines.

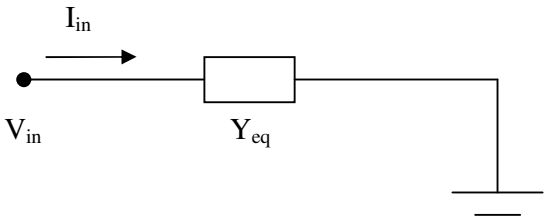

Figure 2.3 Equivalent Circuit Representation of Immitance Simulator.

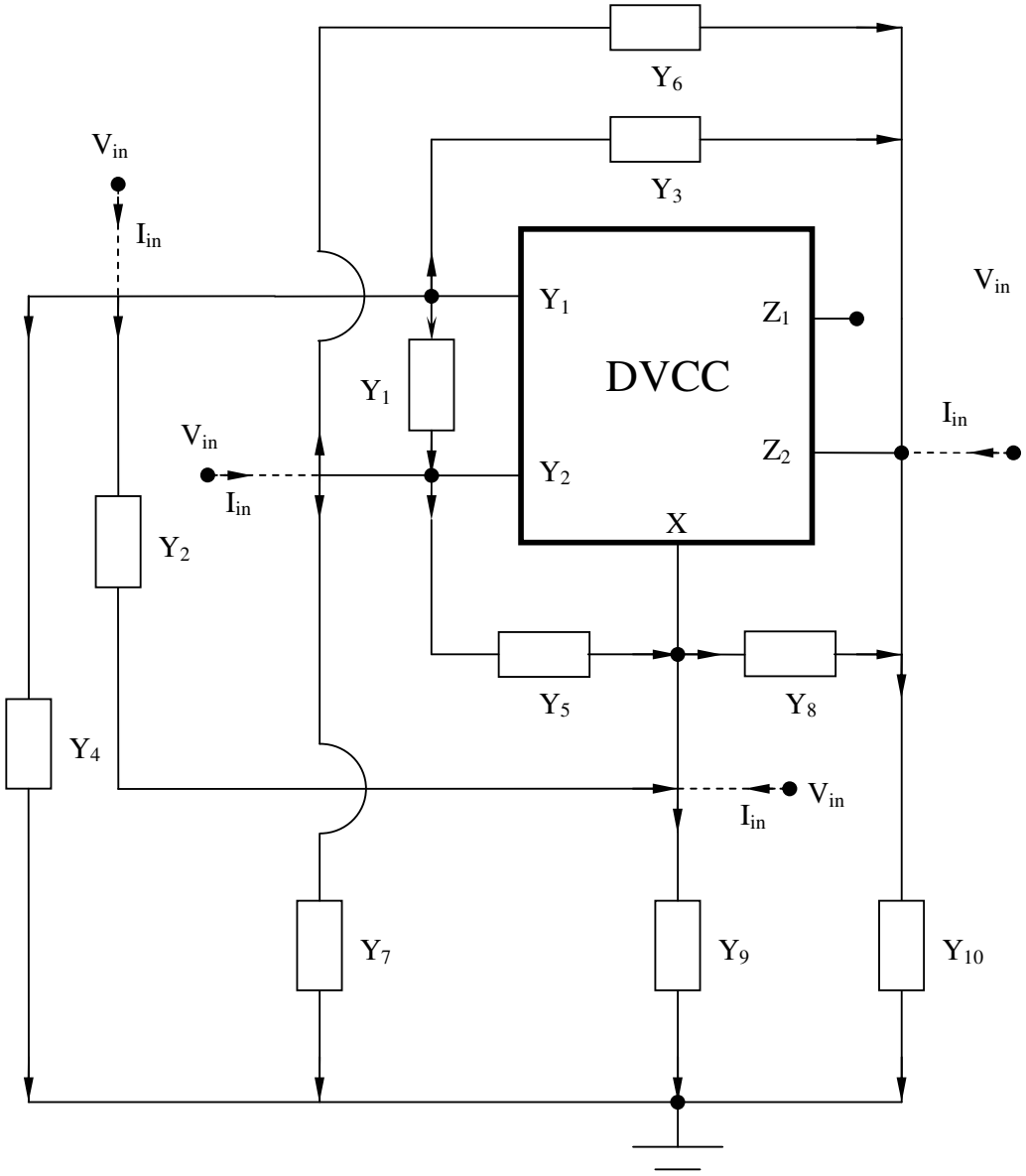

Figure 2.4 Interconnection of the terminals of DVCC.

c. Relying on the node hierarchy assumed, all currents are assigned with the specified polarities as given in figure 2.4. Regarding to the node hierarchy, potentials are ordered as $V_{y1} > V_{y2} > V_x > V_z$.

d. Node equations are created by assuming each terminal of DVCC as an independent node. This results in n+1 number of equations as n denotes the number of terminals of DVCC that have been taken into account.

e. By using a general purpose PC software for solving linear equations, $Z_{eq} = V_{in} / I_{in}$ equation is extracted for series combinations whereas $Y_{eq} = I_{in} / V_{in}$ equation is extracted for parallel combination immitance simulators.

f. Relying on the objective of building the immitance simulators with the minimum number of passive components, this critical step is to simplify the Y_{eq} and Z_{eq} in order to achieve a parallel immitance function given in (2.5) or a series immitance function given in (2.6). In order to achieve this goal, admittance values of some of the passive components are supposed to be assigned to infinity by which some of the terminals are shorted to each other. Similarly, admittance values of some of the passive components are supposed to be assigned to zero by which some of the terminals are isolated from the other ones.

$$Y_{eq} = \frac{Y_A Y_B + Y_A Y_C + Y_B Y_C}{Y_C} \tag{2.5}$$

$$= Y_A + Y_B + \frac{Y_A Y_B}{Y_C}$$

$$Z_{eq} = \frac{Y_D + Y_E + Y_F}{Y_D Y_E} \tag{2.6}$$

$$= \frac{1}{Y_D} + \frac{1}{Y_E} + \frac{Y_F}{Y_D Y_E}$$

g. At the final stage, admittances of the passive components which take place in the obtained Z_{eq} and Y_{eq} expressions are converted into conductive or capacitive equivalents to finalize the circuit synthesis. By substituting $Y_A = G_A$,$Y_B = G_B$ and $Y_C = sC$ in (2.5), equivalent admittance expression is given in (2.7). Applying the same convention, substituting $Y_D = G_D$, $Y_E = G_E$ and $Y_F = sC$ in (2.6) will result in the equivalent impedance of the circuit as given in (2.8).

$$Y_{eq} = G_A + G_B + \frac{G_A G_B}{sC} \tag{2.7}$$

$$Z_{eq} = \frac{1}{G_D} + \frac{1}{G_E} + \frac{sC}{G_E G_F} \tag{2.8}$$

2.2.2 Proposed Immitance Simulator Circuits

2.2.2.1 Proposed Series Immitance Simulator Circuits

The circuit seen in figure 2.5 is composed of two resistive and single grounded capacitive components. The equivalent input impedance of the circuit is given in (2.9).

The circuit seen in figure 2.5 is the active DVCC based equivalent of the circuit given in 2.6. In figure 2.6, R_{eq} and L_{eq} denote the equivalent resistive and inductive components of the circuit. In (2.10) and (2.11), equivalent resistive and inductive components are shown explicitly in terms of resistive and capacitive elements which take place in DVCC based active series immitance simulator. Besides, by using the Z_1 output with the same topology, Series R - (–L) Immitance Simulator can be obtained. (See Appendix)

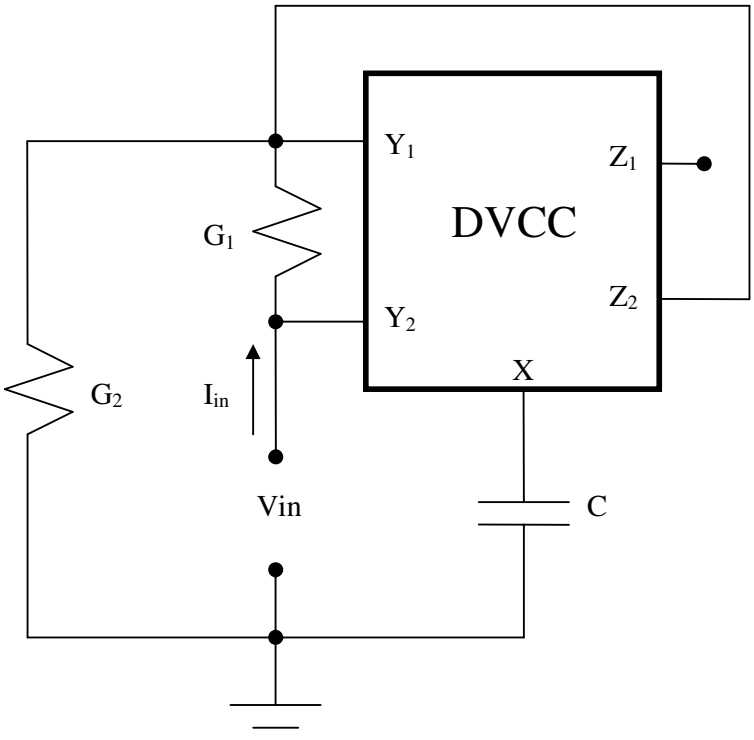

Figure 2.5 Series R-L Immitance Simulator.

$$Z_{eq} = \frac{1}{G_1} + \frac{1}{G_2} + \frac{sC}{G_1 G_2} \tag{2.9}$$

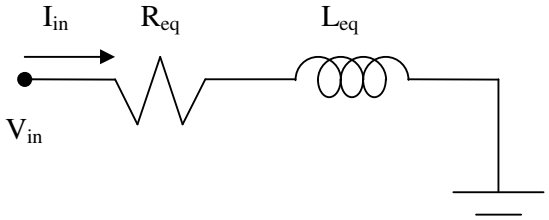

Figure 2.6 Series R-L Passive Circuit.

$$R_{eq} = \frac{1}{G_1} + \frac{1}{G_2} \tag{2.10}$$

$$L_{eq} = \frac{C}{G_1 G_2} \tag{2.11}$$

The circuit seen in figure 2.7 is composed of three resistive and single capacitive components. By connecting Vx and Vy1, there appears a virtual ground on terminal Vy2. Thus, the capacitance C should be considered to be a grounded capacitance. The equivalent input impedance of the circuit is given in (2.12).

$$Z_{eq} = -\frac{G_1}{G_2 G_3} - \frac{sC}{G_2 G_3} \tag{2.12}$$

In equations (2.13) and (2.14), equivalent resistive and inductive components are shown explicitly in terms of resistive and capacitive components used in series –R- – L immitance simulator.

$$R_{eq} = \frac{G_1}{G_2 G_3} \tag{2.13}$$

$$L_{eq} = \frac{C}{G_2 G_3} \tag{2.14}$$

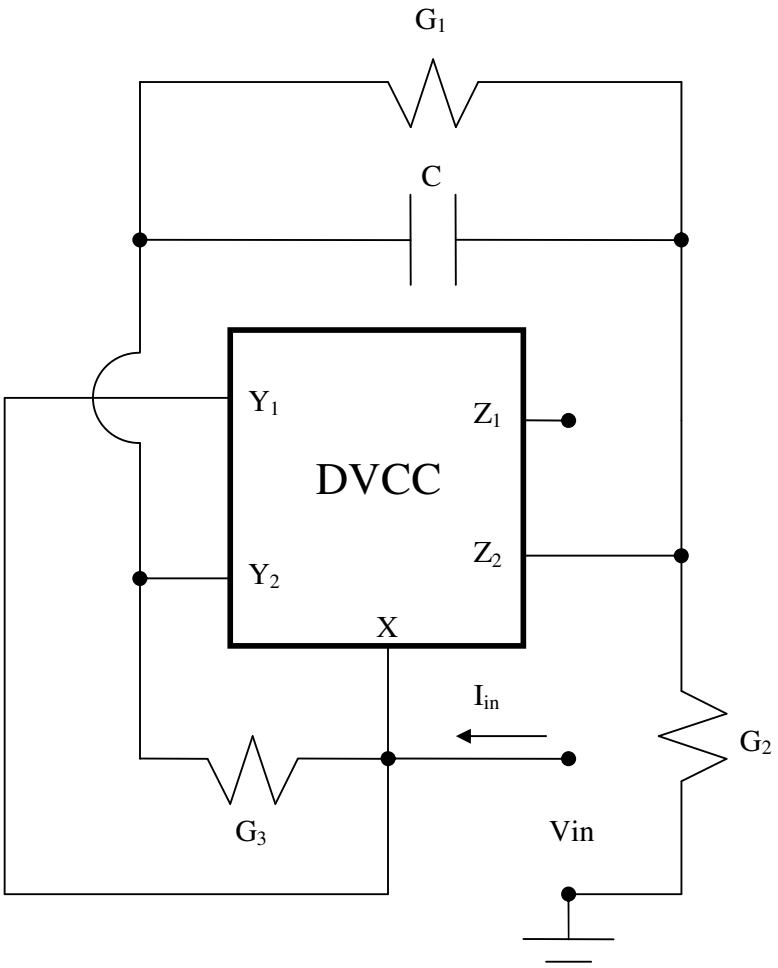

Figure 2.7 Series (–R) - (–L) Immitance Simulator.

2.2.2.2 Proposed Parallel Immitance Simulator Circuits

The circuit seen in figure 2.8 is composed of two resistive and single grounded capacitive components. The equivalent input admittance of the circuit is given in equation (2.15).

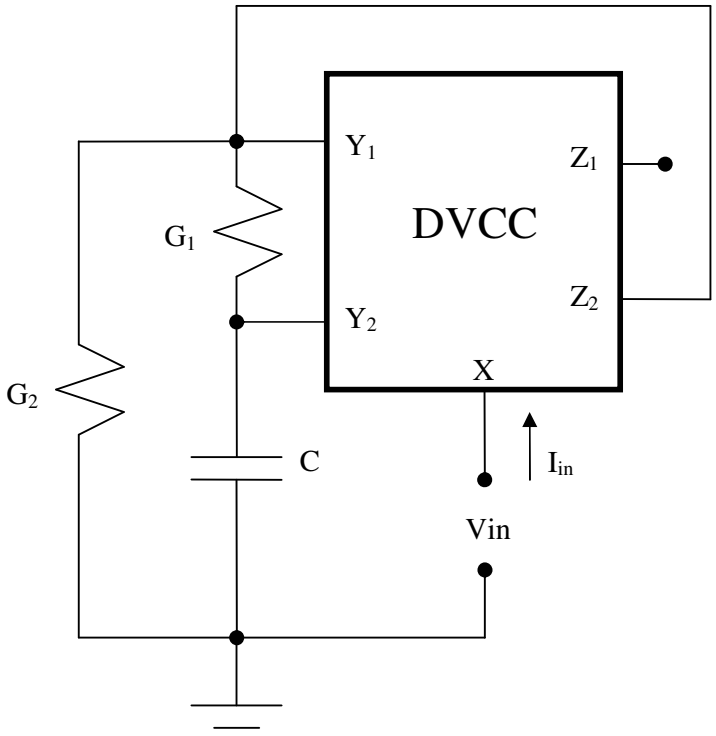

Figure 2.8 Parallel R-L Immitance Simulator.

$$Y_{eq} = G_1 + G_2 + \frac{G_1 G_2}{sC} \tag{2.15}$$

The circuit seen in figure 2.8 is the active DVCC based equivalent of the circuit given in figure 2.9. In figure 2.9, R_{eq} and L_{eq} denote the equivalent resistive and inductive components of the circuit. In equations (2.16) and (2.17), equivalent resistive and inductive components are shown explicitly in terms of resistive and capacitive elements which take place in DVCC based active parallel immittance simulator. Furthermore, the same topology can be converted into a Parallel (–R)-(–L) immitance if positive polarity output terminal Z_1 is used instead of Z_2. (See Appendix)

$$R_{eq} = \frac{1}{G_1 + G_2} \tag{2.16}$$

$$L_{eq} = \frac{C}{G_1 G_2} \tag{2.17}$$

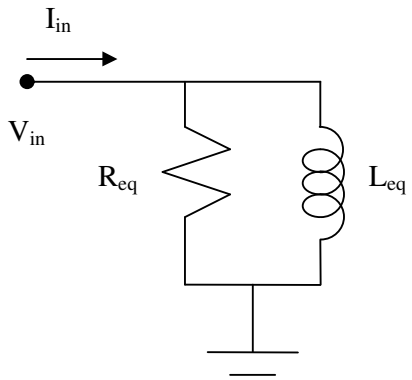

Figure 2.9 Parallel R-L Passive Circuit.

The circuit seen in figure 2.10 is composed of two resistive and single grounded capacitive components. The equivalent input admittance of the circuit is given in (2.18). Proposed parallel (–R) - (–-L) simulator can be converted into a Parallel R-L simulator if Z_1 output is used instead of Z_2. (See Appendix)

$$Y_{eq} = -G_1 - G_2 - \frac{G_1 G_2}{sC} \tag{2.18}$$

In equations (2.19) and (2.20), equivalent resistive and inductive components are shown explicitly in terms of resistive and capacitive elements which take place in DVCC based active parallel immitance simulator.

$$R_{eq} = \frac{1}{G_1 + G_2} \tag{2.19}$$

$$L_{eq} = \frac{C}{G_1 G_2} \tag{2.20}$$

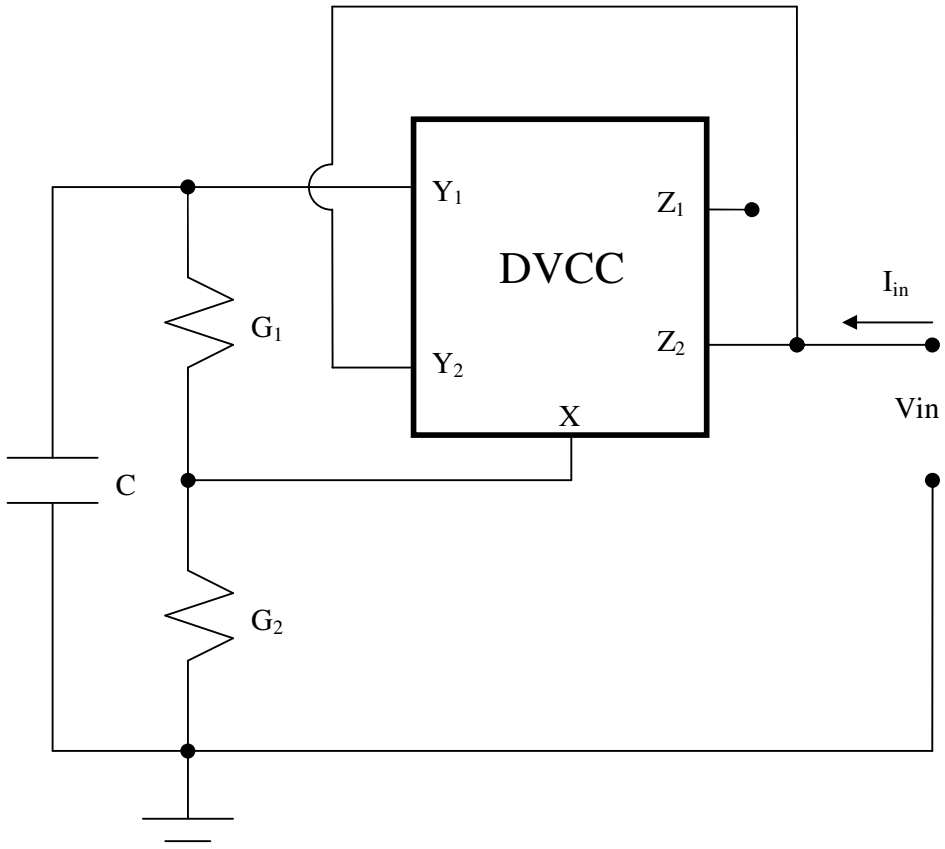

Figure 2.10 Parallel (–R) - (–L) Immitance Simulator.

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CHAPTER THREE

SYNTHESIS OF DDCC BASED NOVEL IMMITANCE SIMULATORS

3.1 Introduction of DVCC

3.1.1 Historical Background of DDCC

Differential Difference Current Conveyor (DDCC) was proposed by W.Chiu, S.-I.Liu, H.-W.Tsao and J.-J.Chen in 1996. Since CCII was proposed in 1970, it has proven to be a versatile building block and the invention of the powerful CCII resulted in many application circuits like amplifiers, filters and oscillators to be constructed based on CCII (Chiu, Liu, Tsao & Chen, 1996). In 1987, a new building block called DDA was proposed (Sackinger & Guggenbuhl, 1987). Taking advantage of the high input impedance and the arithmetic operation capability, designers have been able to construct new applications with a reduced number of components by using DDA. The advantages of CCII and DDA are combined to build the new versatile block called DDCC (Chiu, Liu, Tsao & Chen, 1996).

3.1.2 Black Box Representation of DDCC

DDCC is a five terminal device as given in figure 3.1. DDCC was designed to have three distinct infinite impedance input terminals (Y_1, Y_2 and Y_3) which allows no current flowing through Y terminals. X terminal has the equal potential to the potential difference between terminals Y_1 and Y_2 plus the potential of Y_3. (Chiu, Liu, Tsao & Chen, 1996)

Relying on the common current conveying characteristic, current flowing through terminal X is conveyed to the Z terminal. DDCC is named as either DDCC+ or DDCC- depending on the polarity of the current flowing through Z terminal. In DDCC+, the current flowing through terminal Z has the same polarity with the current flowing through X terminal, whereas in DDCC- current is conveyed from X

terminal to Z terminal with an inverse polarity. The hybrid matrix equation of DDCC is given in (3.1). (Chiu, Liu, Tsao & Chen, 1996).

$$\begin{bmatrix} V_x \\ i_{Y1} \\ i_{Y2} \\ i_{Y3} \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \pm 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_x \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_Z \end{bmatrix} \tag{3.1}$$

In 2004, a novel CMOS implementation of DDDC was proposed.(Jianping, Yinshui & Tiefeng, 2004) The implementation covers the current conveying functionality of both DDCC- and DDCC+ devices as the proposed CMOS implementation has two high impedance output terminals as given in figure 3.2

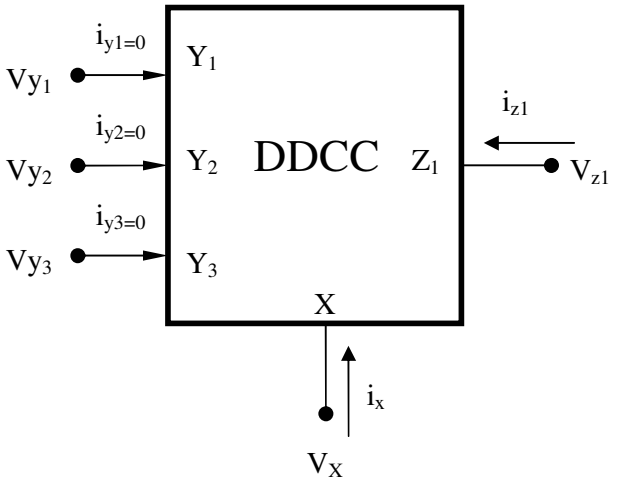

Figure 3.1 Black Box Representation of DDCC.

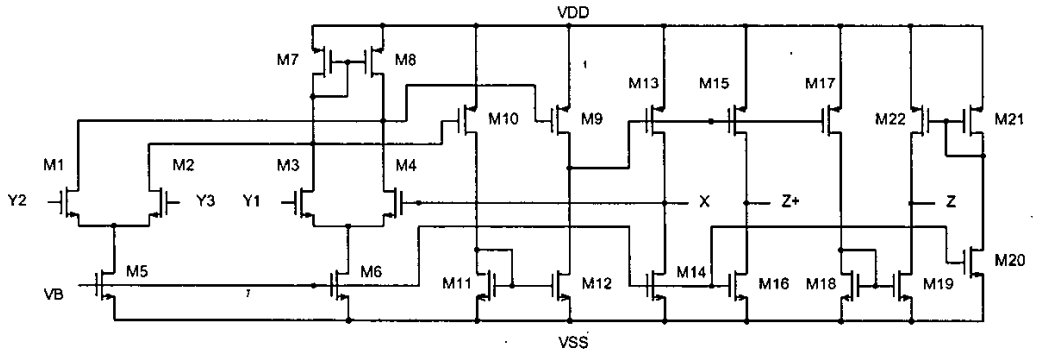

Figure 3.2 CMOS Implementation of DDCC.

3.1.3 CMOS Implementation of DDCC

3.2 Immitance simulators based on DDCC

3.2.1 Methodology in construction of Immitance Simulators

The methodology in immitance simulator synthesis using DDCC is based on the construction of immitance circuits using single DDCC device and minimum number of surrounding resistive and capacitive elements. Regarding this objective, all terminals of DDCC are connected to each other and to the ground with the specified passive elements. Since the study is focused on grounded immitance simulator synthesis, all terminals of DDCC are connected to ground via a passive component as well. Relying on the mentioned methodology, the admittance equivalents of the passive components are used to build up node equations. The methodology to obtain immitance circuits is given below:

a. Every terminal of DDCC is connected to the other terminals and to the ground via a passive component whose admittance equivalent is given in figure 3.3.

b. One of the terminals of DDCC is specified as the input node of immitance simulator to represent the V_{in} of the equivalent circuit of grounded immitance simulator given in figure 3.3. Note that, only one of the terminals of DDCC should be considered to be the input node as seen in figure 3.4 with the dashed lines.

Table 3.1 Specified admittances of passive components

	V_{Y1}	V_{Y2}	V_{Y3}	V_X	V_Z	GND
V_{Y1}	-	Y_1	Y_2	Y_3	Y_4	Y_5
V_{Y2}	Y_1	-	Y_6	Y_7	Y_8	Y_9
V_{Y3}	Y_2	Y_6	-	Y_{10}	Y_{11}	Y_{12}
V_X	Y_3	Y_7	Y_{10}	-	Y_{13}	Y_{14}
V_Z	Y_4	Y_8	Y_{11}	Y_{13}	-	Y_{15}
GND	Y_5	Y_9	Y_{12}	Y_{14}	Y_{15}	-

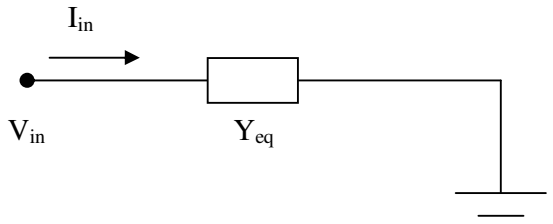

Figure 3.3 Equivalent Circuit Representation of Immitance Simulator.

c. Relying on the node hierarchy assumed, all currents are assigned with the specified polarities as given in figure 3.4. Regarding to the node hierarchy, potentials are ordered as $V_{y1} > V_{y2} > V_{y3} > V_x > V_z$.

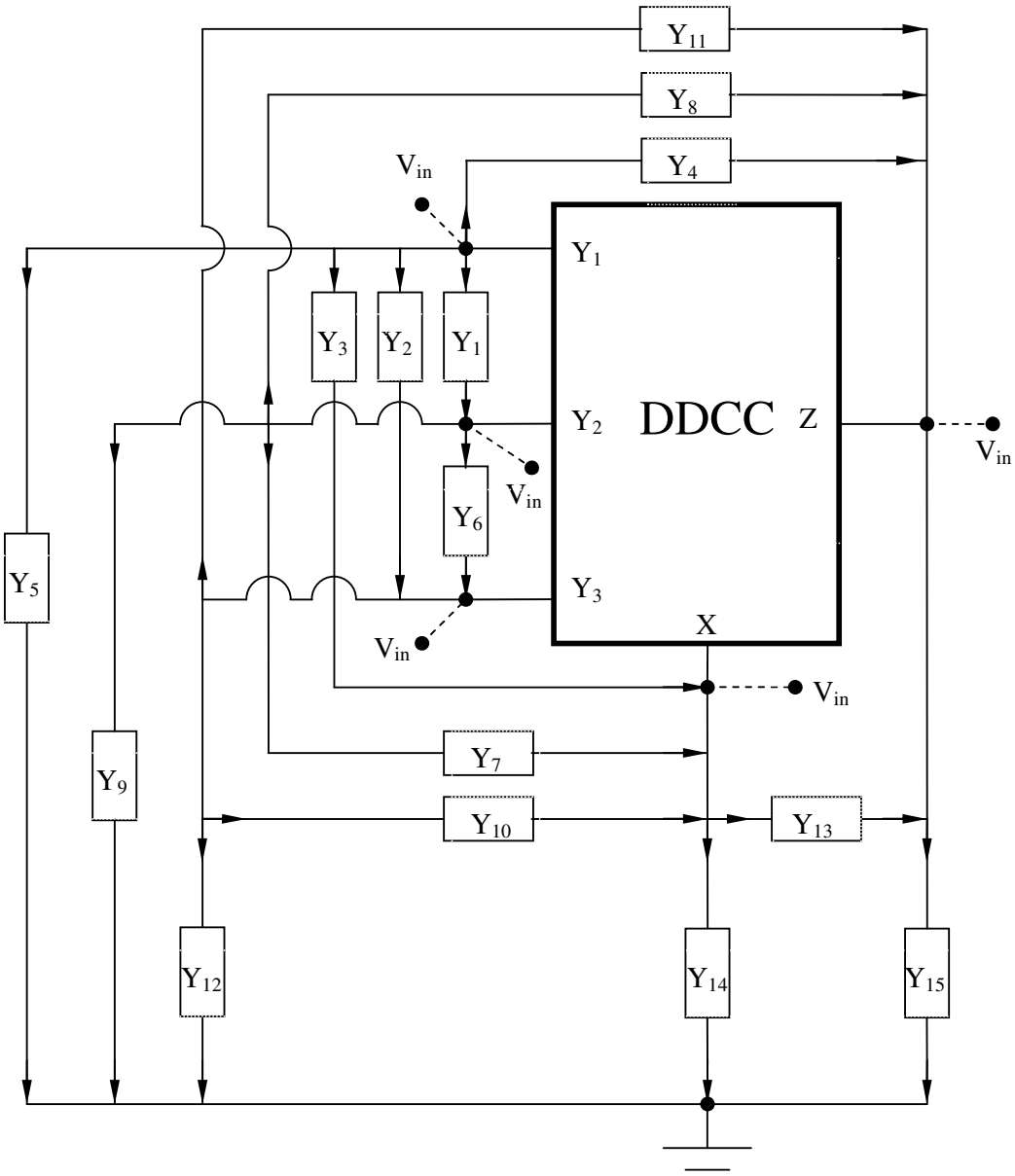

Figure 3.4 Interconnection of the terminals of DDCC.

d. Node equations are created by assuming each terminal of DDCC as an independent node. This results in n+1 number of equations as n denotes the number of terminals of DDCC that have been taken into account.

e. The step that is mentioned in 2.2.1. (e) is followed.

f. The step that is mentioned in 2.2.1. (f) is followed.

g. The step that is mentioned in 2.2.1. (g) is followed.

3.2.2 Proposed Immitance Simulators

3.2.2.1 Proposed Series Immitance Simulator Circuits

The circuit seen in figure 3.5 is composed of two resistive and single grounded capacitive components. The equivalent input impedance of the circuit is given in (3.2). The circuit seen in figure 3.5 is the active DDCC based equivalent of the passive series R-L circuit. In equations (3.3) and (3.4), equivalent resistive and inductive components are shown explicitly in terms of resistive and capacitive elements which are used in DDCC based active series immitance simulator.

$$Z_{eq} = \frac{1}{G_1} + \frac{1}{G_2} + \frac{sC}{G_1 G_2} \tag{3.2}$$

$$R_{eq} = \frac{1}{G_1} + \frac{1}{G_2} \tag{3.3}$$

$$L_{eq} = \frac{C}{G_1 G_2} \tag{3.4}$$

The circuit seen in figure 3.6 is composed of three resistive and single capacitive components. By connecting V_x and V_{y1}, there appears a virtual ground on terminal V_{y2}. Thus, the capacitance C should be considered to be a grounded capacitance. The equivalent input impedance of the circuit is given in (3.5). Proposed circuit is constructed by using DDCC- , however, by using using DDCC+ , same circuit topology turns out to be Series R - (–L) immitance simulator. (See Appendix)

$$Z_{eq} = \frac{1}{G_3} - \frac{sC}{G_1 G_2} \tag{3.5}$$

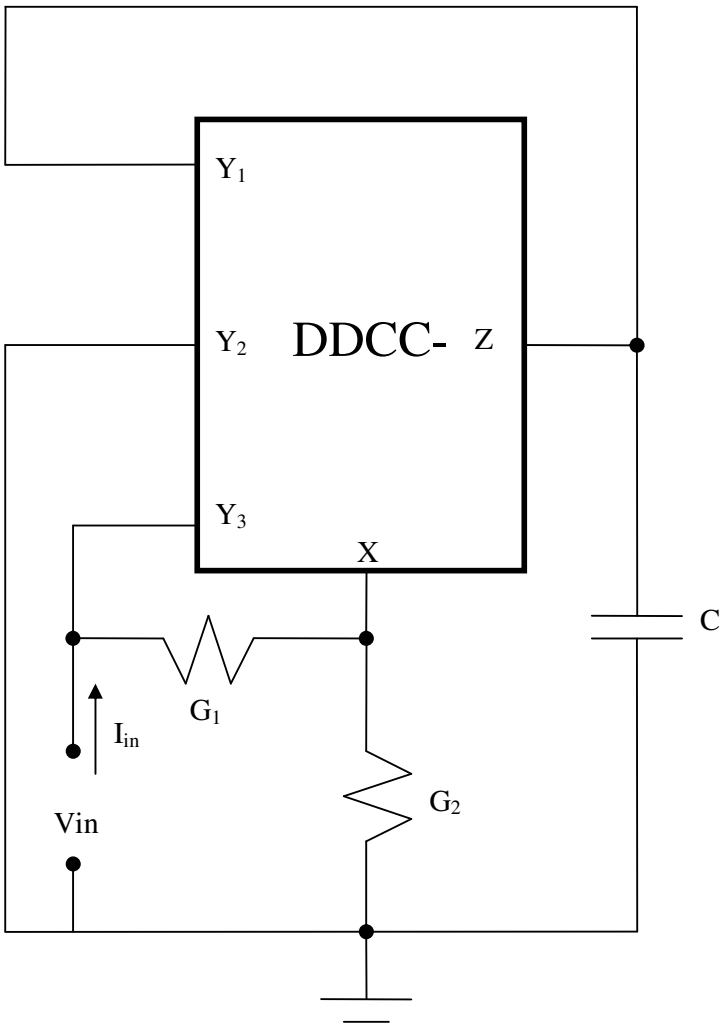

Figure 3.5 Series R-L Immitance Simulator.

In equations (3.6) and (3.7), equivalent resistive and inductive components are shown explicitly in terms of resistive and capacitive components that take place in series R-(–L) immitance simulator.

$$R_{eq} = \frac{1}{G_3} \tag{3.6}$$

$$L_{eq} = \frac{C}{G_1 G_2} \tag{3.7}$$

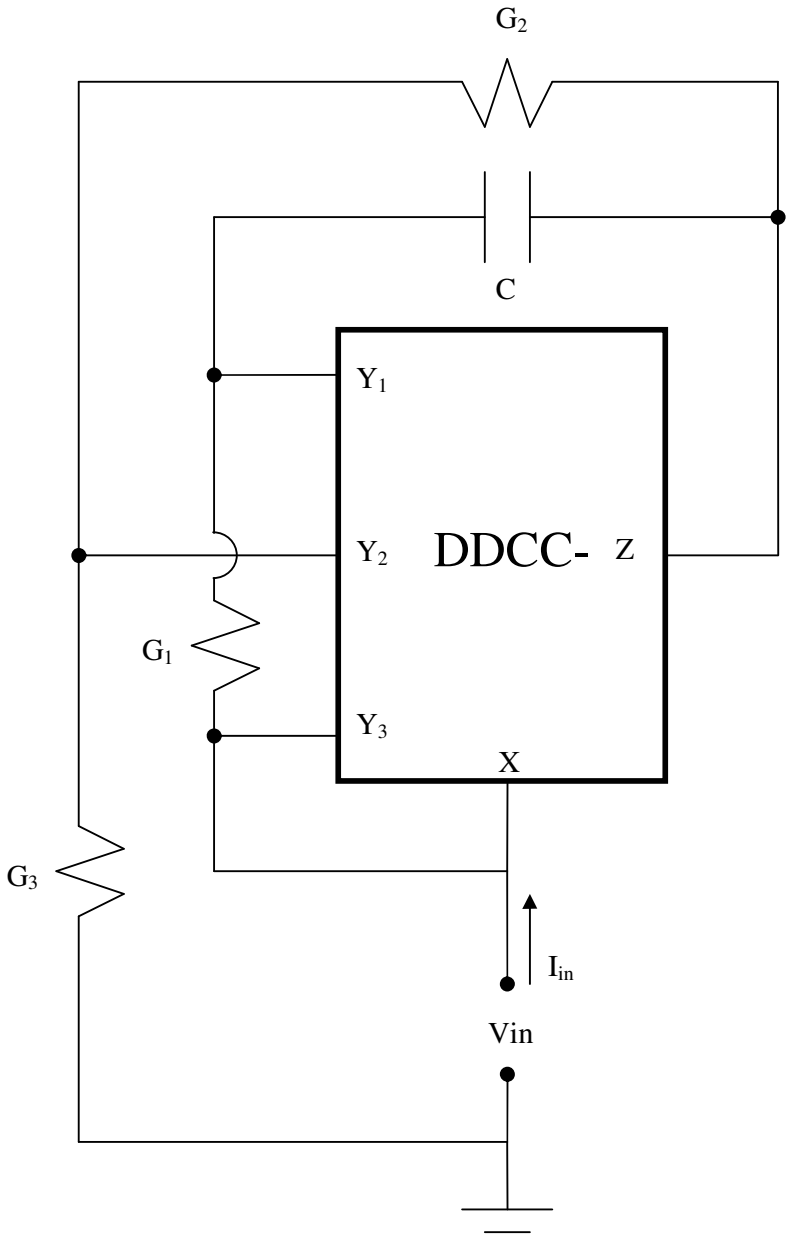

Figure 3.6 Series R - (–L) Immitance Simulator.

3.2.2.2 Proposed Parallel Immitance Simulator Circuits

The circuit seen in figure 3.7 is composed of two resistive and single grounded capacitive components. The equivalent input admittance of the circuit is given in (3.8). Proposed parallel R-L immitance circuit can be converted into a Parallel (–R) - (–L) immitance by using DDCC+ instead of DDCC-. (See Appendix)

$$Y_{eq} = G_1 + G_2 + \frac{G_1 G_2}{sC} \tag{3.8}$$

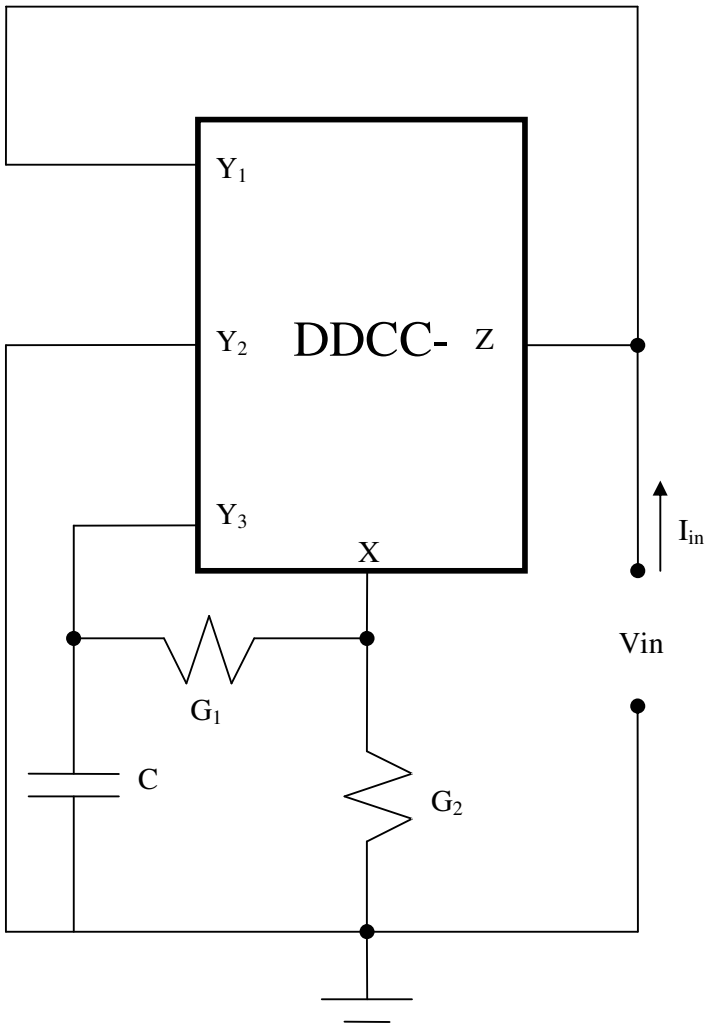

Figure 3.7 Parallel R - L Immitance Simulator.

In equations (3.9) and (3.10), equivalent resistive and inductive components are shown explicitly in terms of resistive and capacitive elements which take place in DDCC based active parallel immitance simulator.

$$R_{eq} = \frac{1}{G_1 + G_2} \tag{3.9}$$

$$L_{eq} = \frac{C}{G_1 G_2} \tag{3.10}$$

The circuit seen in figure 3.8 is composed of two resistive and single floating capacitive components. The equivalent input admittance of the circuit is given in (3.11). By using DDCC+ instead of DDCC- , the circuit can be converted into a Parallel (–R) - (–L) with the same passive component topology. (See Appendix)

$$Y_{eq} = \frac{G_1 + G_2}{2} + \frac{G_1 G_2}{2sC} \tag{3.11}$$

In equations (3.12) and (3.13), equivalent resistive and inductive components are shown explicitly in terms of resistive and capacitive elements which take place in DDCC based active parallel immitance simulator.

$$R_{eq} = \frac{2}{G_1 + G_2} \tag{3.12}$$

$$L_{eq} = \frac{2C}{G_1 G_2} \tag{3.13}$$

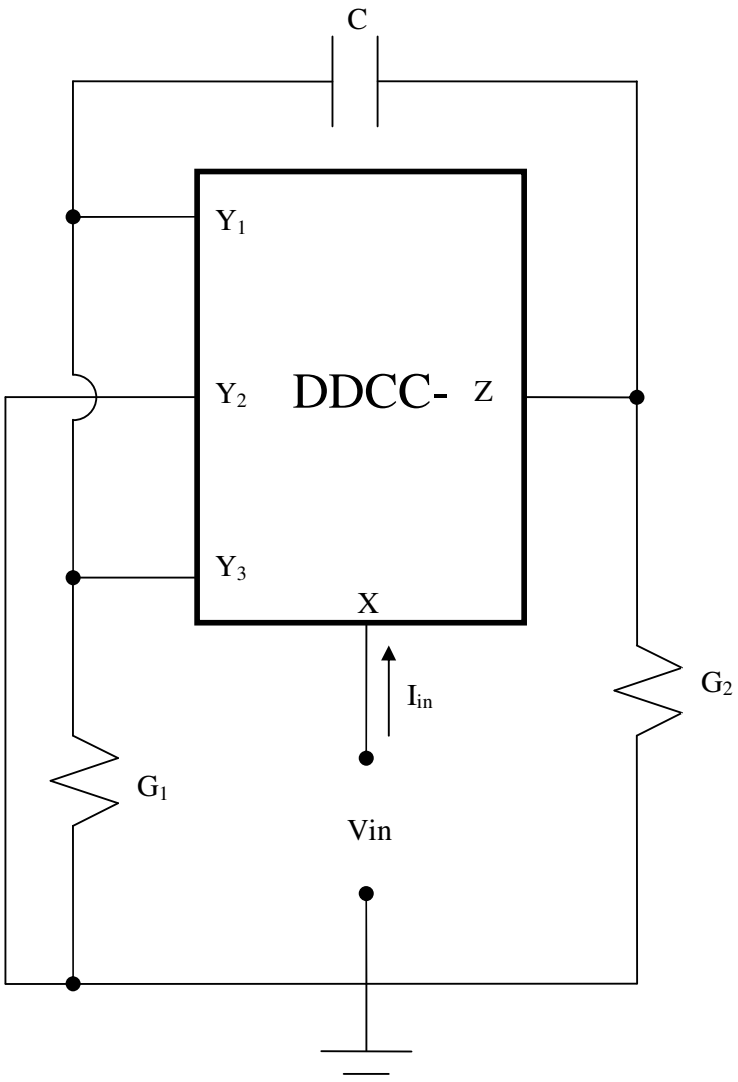

Figure 3.8 Parallel R - L Immitance Simulator.

CHAPTER FOUR

APPLICATIONS OF DVCC AND DDCC BASED IMMITANCE SIMULATORS

4.1 Construction of Filter Systems using Immitance Circuits

4.1.1 Filter Application of Series R-L Immitance Circuits

As the application of series immitance simulator circuits, current mode low pass filter implementation is used as seen in figure 4.1 to prove the functionality of constructed series immitance simulator circuits. According to this approach, replacing dashed box representing R-L series equivalent with the active R-L immitance simulator, a second-order current-mode low-pass filter is obtained. The corresponding filter transfer function is given in (4.1). Spice simulations are realized and the graphical results of obtained filter systems are presented.

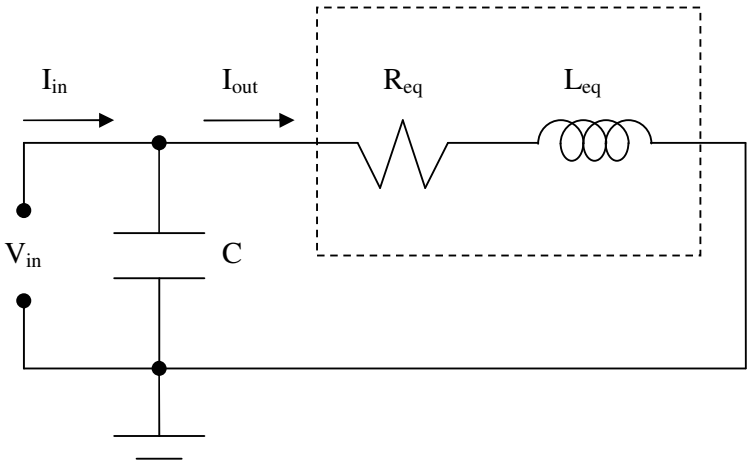

Figure 4.1 Current-Mode Low-Pass Filter Implementation using Series R-L Immitance Circuit.

$$\frac{I_{out}}{I_{in}} = \frac{1/LC}{s^2 + s(R/L) + 1/LC} \tag{4.1}$$

4.1.2 Filter Application of Parallel R-L Immitance Circuits

In order to prove the functionality of the constructed parallel R-L immitance simulators, the proposed immitance circuits are used in construction of second-order voltage-mode filter. A well-known voltage-mode high-pass filter implementation which is based on parallel R-L immitance circuit is shown in figure 4.2. The filter transfer function is given in (4.2). Relying on the same convention that is used in current-mode filter, the dashed box is replaced with the active immitance simulator circuits in order to build up the active voltage-mode high-pass filter. Finally, the performance of the constructed high-pass filter is presented by taking advantage of computer aided simulations using Spice.

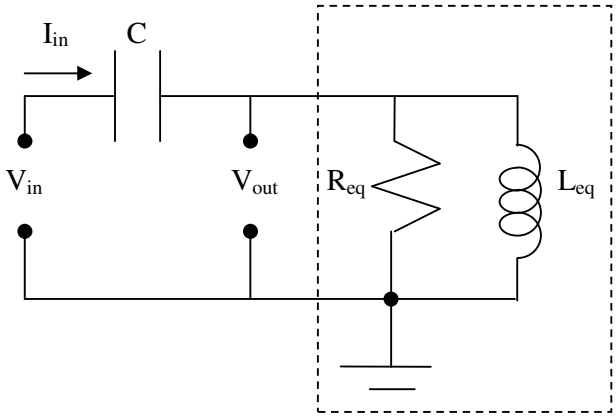

Figure 4.2 Voltage-Mode High-Pass Filter Implementation Using Parallel R-L Immitance Circuit.

$$\frac{V_{out}}{V_{in}} = \frac{s^2}{s^2 + s/RC + 1/LC} \tag{4.2}$$

4.2 Constructed Application Circuits based on Immitance Simulators

4.2.1 DVCC Based Filter Applications

4.2.1.1 Applications of DVCC Based Series R-L Immitance Simulators

The circuit seen in figure 4.3 is the realization of Current-Mode Low-Pass filter using DVCC based Series R-L Immitance simulator. Additional shunt capacitor C' is connected to the input node of the grounded immitance simulator in order to realize a low-pass filter function. The performance of the filter is presented by taking advantage of Spice simulation results seen in figure 4.4.

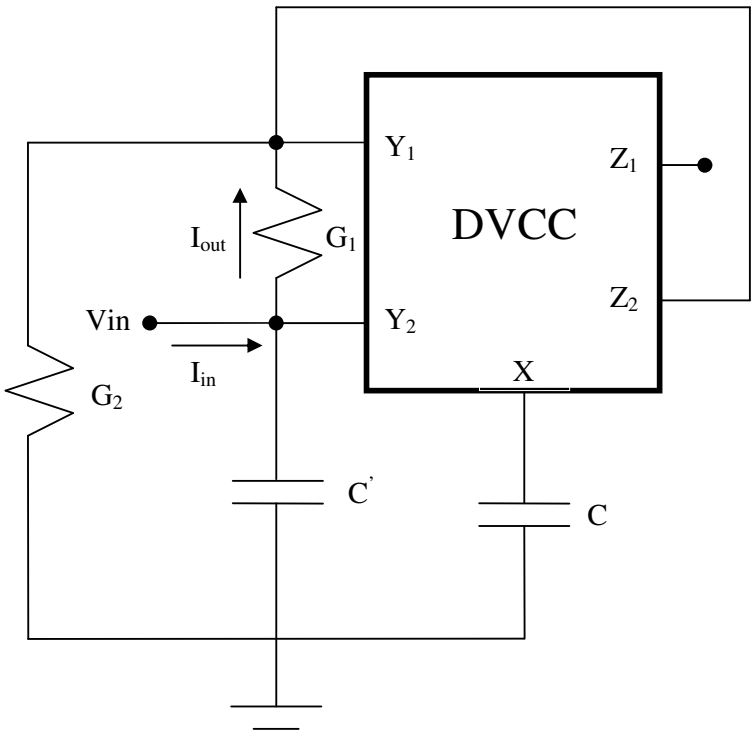

Figure 4.3 Current-Mode Low-Pass Filter using DVCC Based Series R-L Immitance.

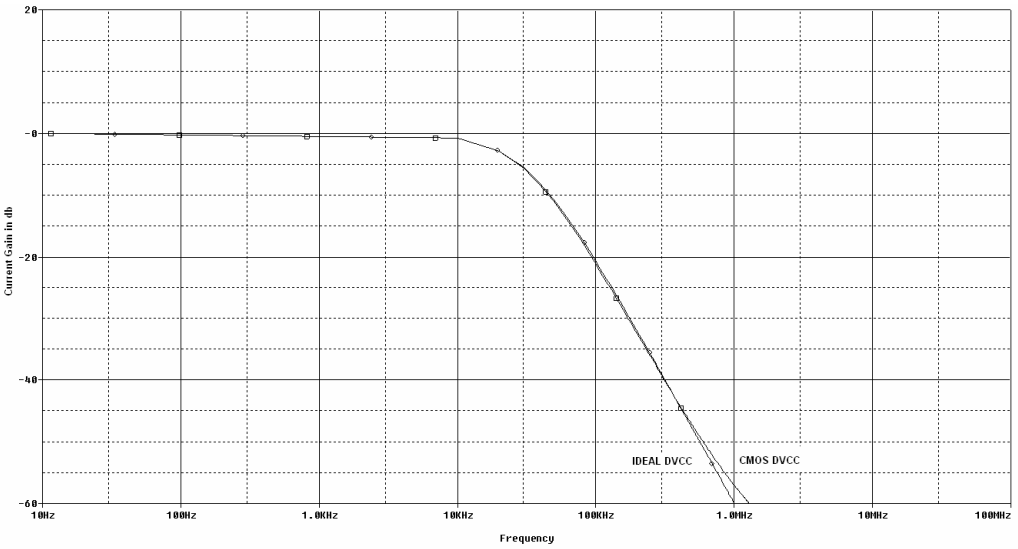

Figure 4.4 Spice Simulation Results Presenting Current Gain of Current-Mode Low-Pass Filter using DVCC Based Series R-L Immitance.

4.2.1.2 Applications of DVCC Based Parallel R-L Immitance

Realization of Voltage-Mode High-Pass Filter using DVCC based Parallel immitance circuit is given in figure 4.5. As seen in the figure, Parallel R-L Immitance simulator is combined with the series capacitance C' in order to provide a High-Pass Filter function. Spice simulation result is given in figure 4.6.

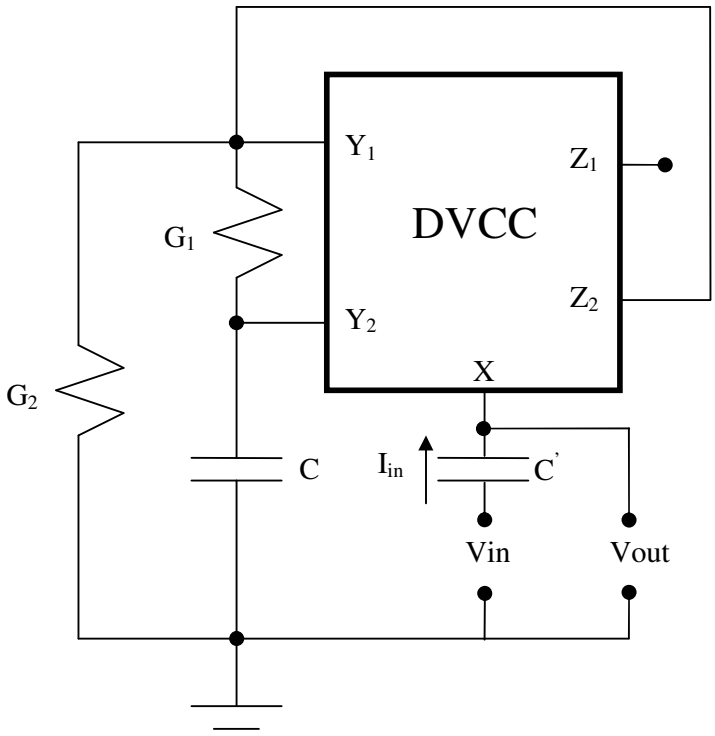

Figure 4.5 Voltage-Mode High-Pass Filter using DVCC Based Parallel R-L Immitance.

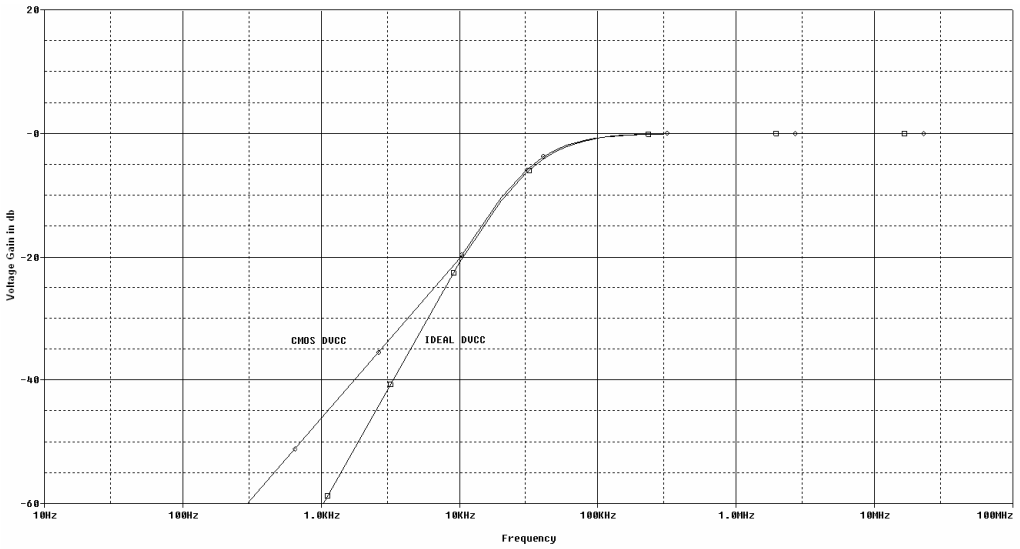

Figure 4.6 Spice Simulation Result Presenting Voltage Gain of Voltage-Mode High-Pass Filter Using DVCC Based Parallel R-L Immitance.

4.2.2 DDCC Based Filter Applications

4.2.2.1 Applications of DDCC Based Series R-L Immitance Simulators

The circuit seen in figure 4.7 is the realization of Current-Mode Low-Pass filter using DDCC- based Series R-L Immitance simulator. By following the same convention used in DVCC Based Current-Mode filters, shunt capacitor C' is connected to the input node of the grounded immitance simulator in order to realize a low-pass filter function. Performance of the filter is given in figure 4.8.

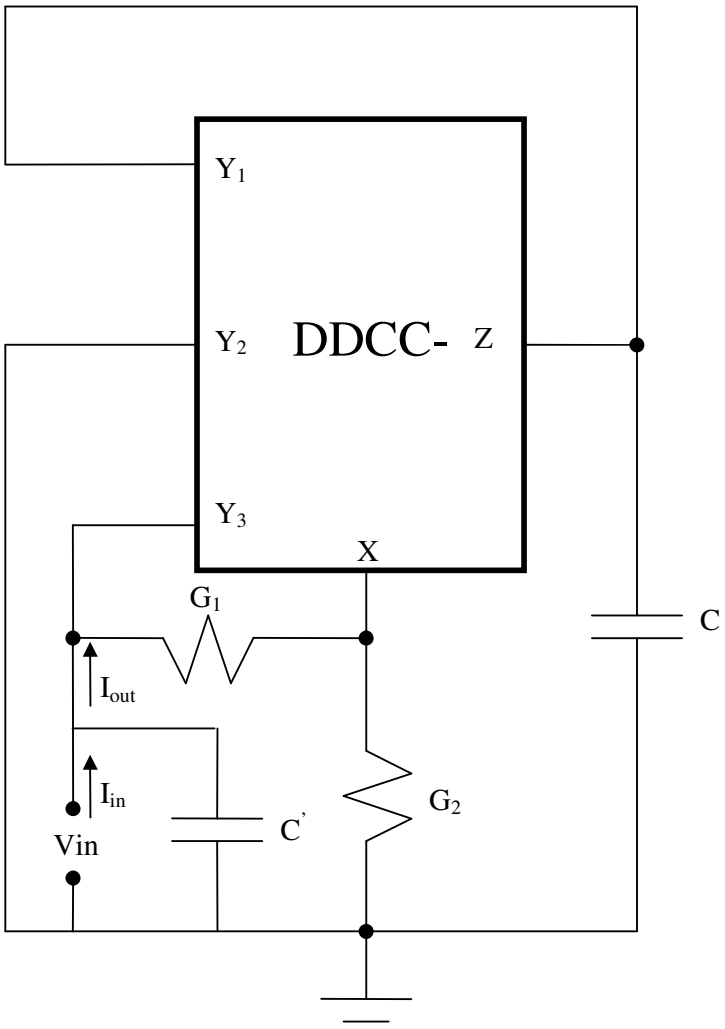

Figure 4.7 Current-Mode Low-Pass Filter using DDCC Based Series R-L Immitance.

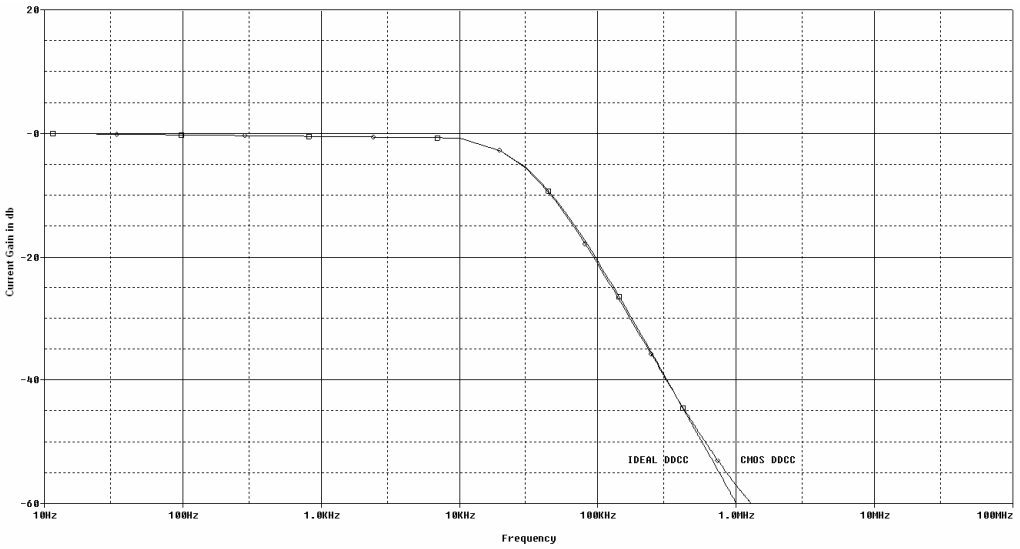

Figure 4.8 Spice Simulation Results Presenting Current Gain of Current-Mode Low-Pass Filter using DDCC Based Series R-L Immitance.

4.2.2.2 Applications of DDCC Based Parallel R-L Immitance Simulators

In figure 4.9, implementation of the Voltage-Mode High-Pass filter using DDCC-based parallel R-L immitance simulator is given. The filter gain V_{out}/V_{in} over the given frequency range is presented in figure 4.10.

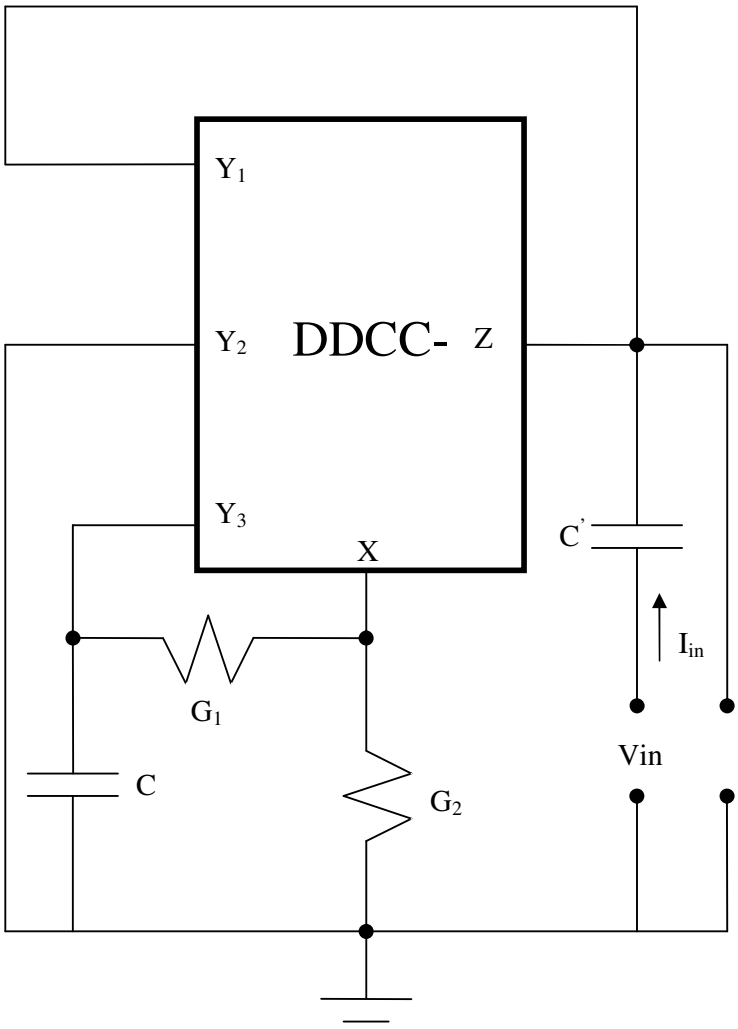

Figure 4.9 Voltage-Mode High-Pass Filter using DDCC Based Parallel R-L Immitance.

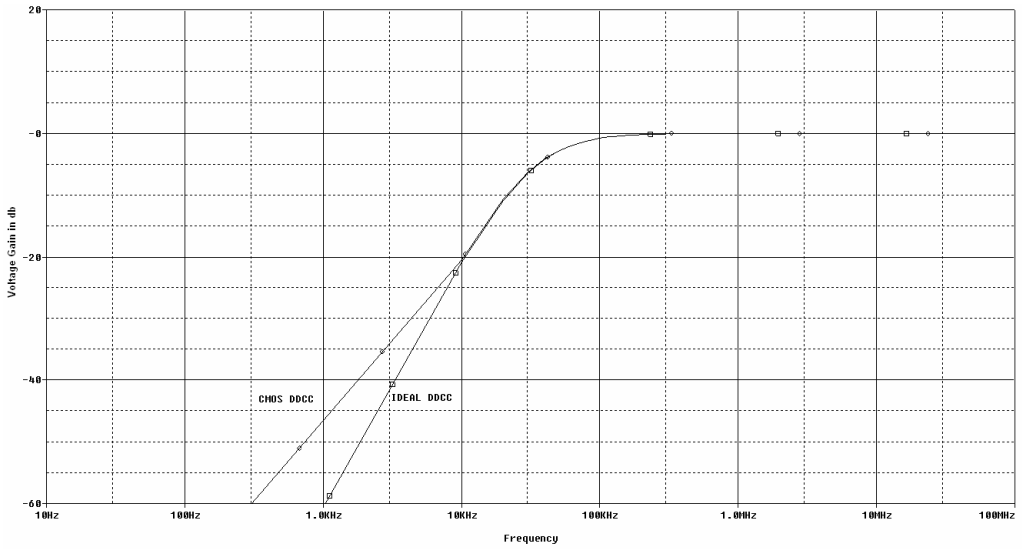

Figure 4.10 Spice Simulation Result Presenting Voltage Gain of Voltage-Mode High-Pass Filter using DDCC Based Parallel R-L Immitance.

DDCC- based Parallel R-L Immitance with a different component topology is applied in a Voltage-Mode High-Pass filter in figure 4.11. Spice simulation result of the constructed filter is given in figure 4.12.

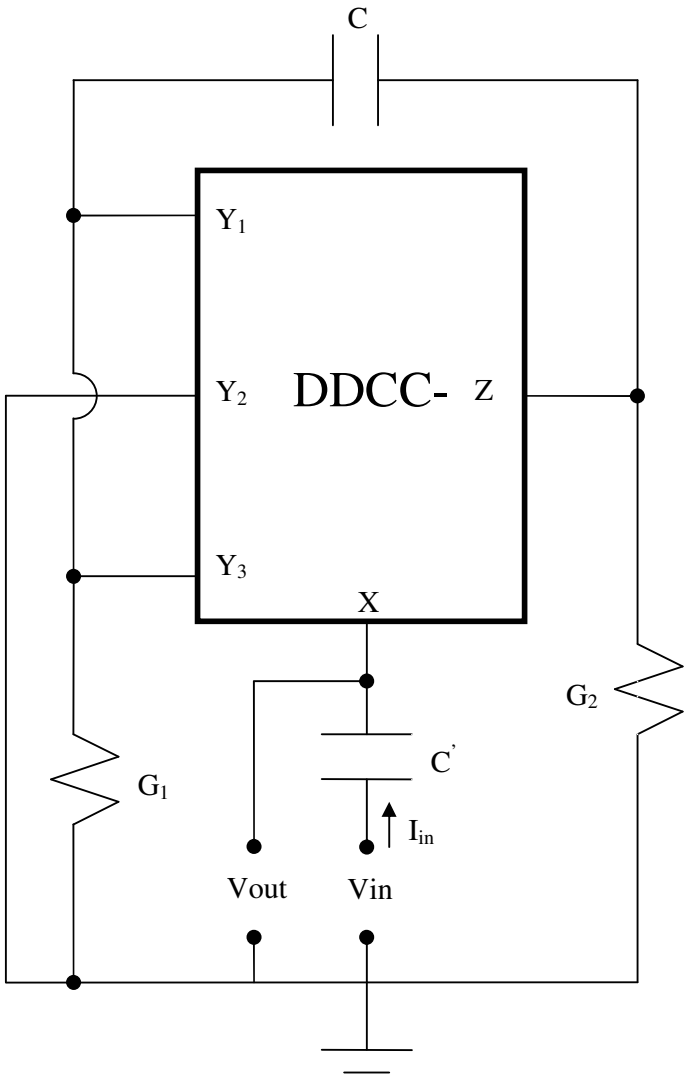

Figure 4.11 Voltage-Mode High-Pass Filter using DDCC Based Parallel R-L Immitance.

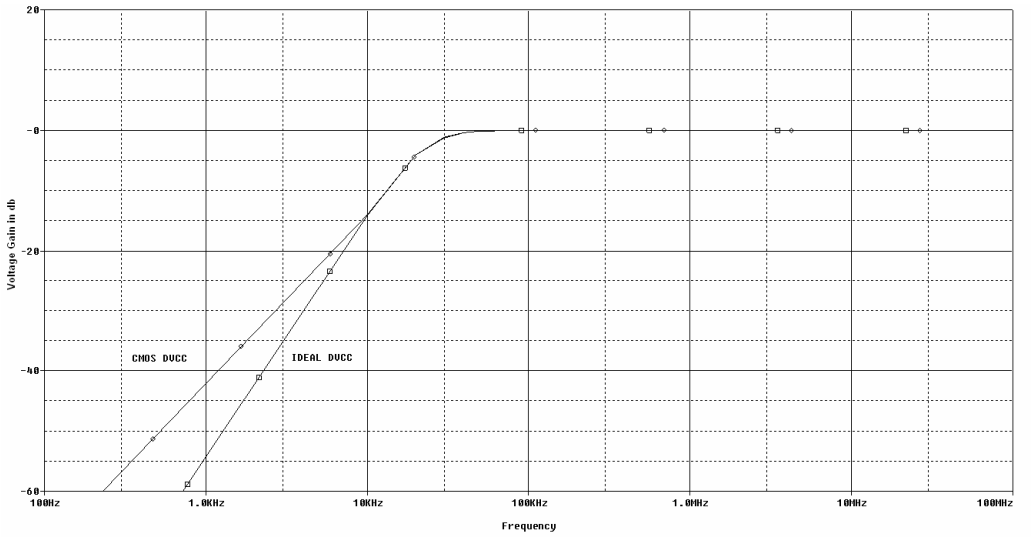

Figure 4.12 Spice Simulation Result Presenting Voltage Gain of Voltage-Mode High-Pass Filter using DDCC Based Parallel R-L Immitance.

4.2.3 Parasitic Cancellation using Parallel (–R)-(–L) Immitance Simulator

In figure 4.13, parallel (–R)-(–L) immitance simulator is connected to passive parallel R-L network Result of parasitic cancellation presenting input admittance of the circuit simulated on Spice is given in figure 4.14.

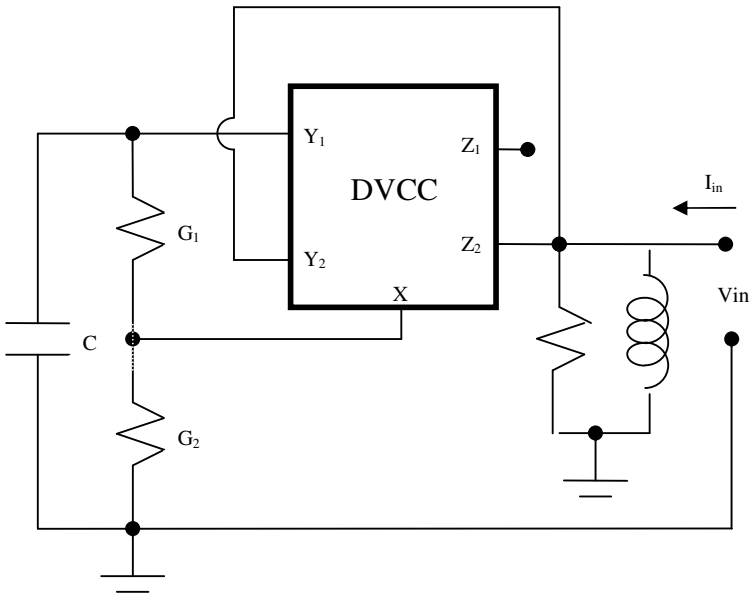

Figure 4.13 Parasitic Cancellation Application Circuit using DVCC Based Parallel (-R)-(-L) Immitance Simulator.

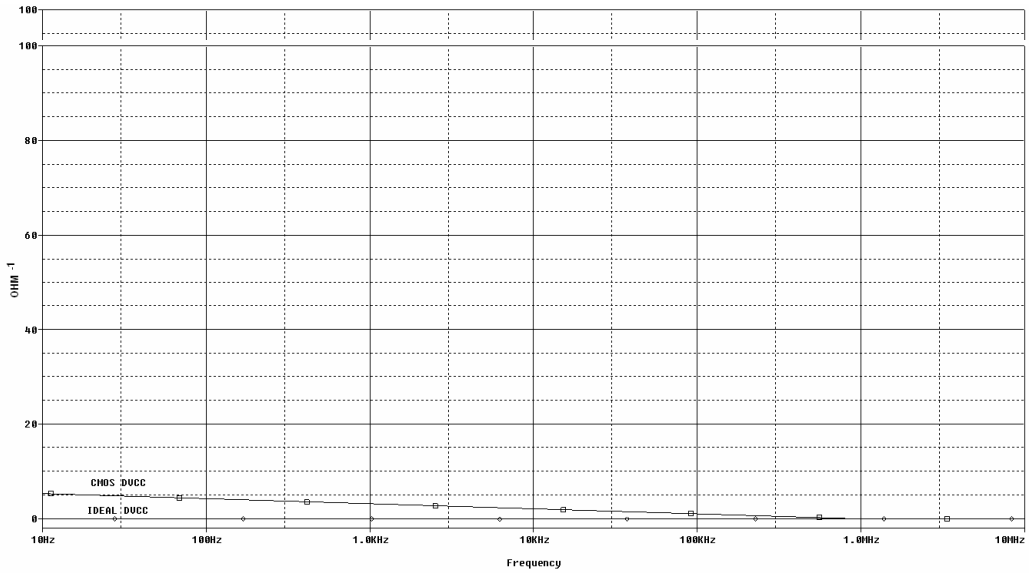

Figure 4.14 Spice Simulation Result Presenting the Parasitic Cancellation Performance of DVCC Based Parallel (–R)-(–L) Immitance Simulator.

CHAPTER FIVE

CONCLUSION

In this thesis, DVCC and DDCC based novel immitance simulator circuits are proposed. By using a single DVCC and DDCC active device and minimum number of passive components, Series and Parallel Immitance Simulators are constructed. The immitance circuits bring no restriction in passive component values like the necessity of matching some resistor elements that take place in the circuit and additionally, inductive components of the proposed immitance circuits are adjustable regardless of the resistive part.

Immitance simulators are used in construction of filter systems and parasitic cancellation applications. Spice simulation results are given in order to present the performance of filter systems constructed using DVCC and DDCC based Immitance simulators. Differences in circuit performance between ideal DVCC / DDCC based applications and CMOS DVCC / DDCC based applications are shown explicitly. The difference in performance arises as the result of non-ideal characteristics of active devices for rather low and high frequencies.

Methodology followed in building immitance simulators is explained step-by-step. As an extension of this study, by relying on the methodology given in synthesis of proposed immitance simulators, new active devices introduced in academic papers can be used to construct novel immitance circuits based on a single active device and minimum number of passive components.

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APPENDIX A

Figures of Immitance Simulator Pairs Obtained By Applying Simple Output Terminal Conversion

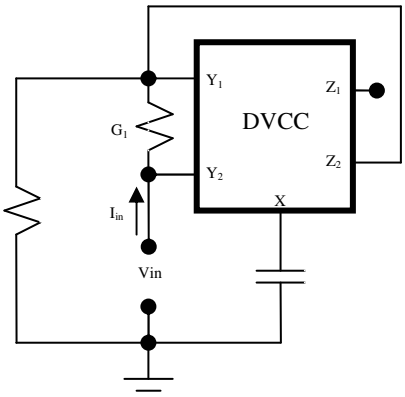

Figure A.1. Series R-L.

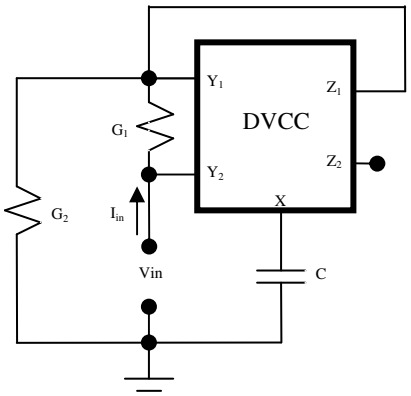

Figure A.2. Series R -(–L).

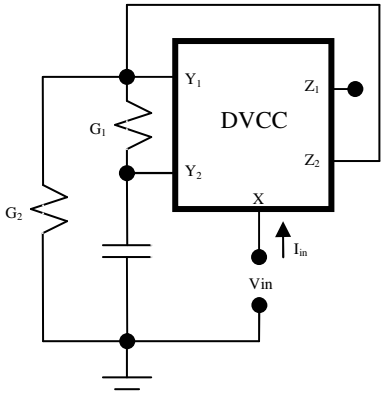

Figure A.3. Parallel R-L.

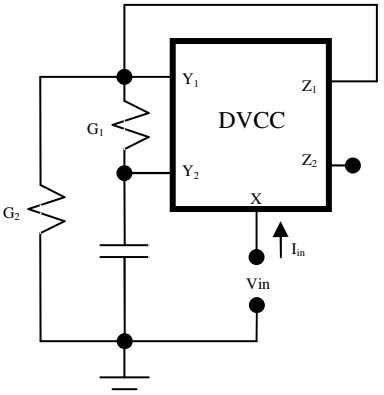

Figure A.4. Parallel (–R)-(–L).

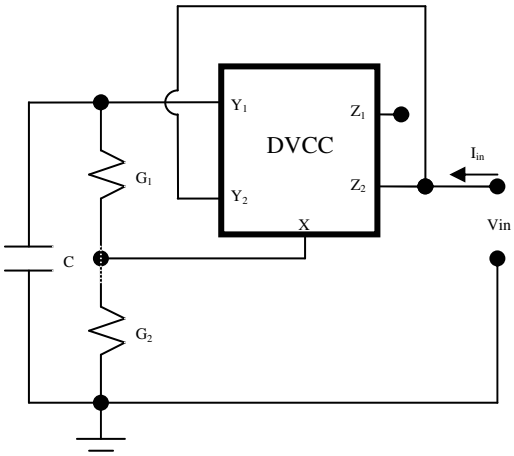

Figure A.5. Parallel (–R)-(–L).

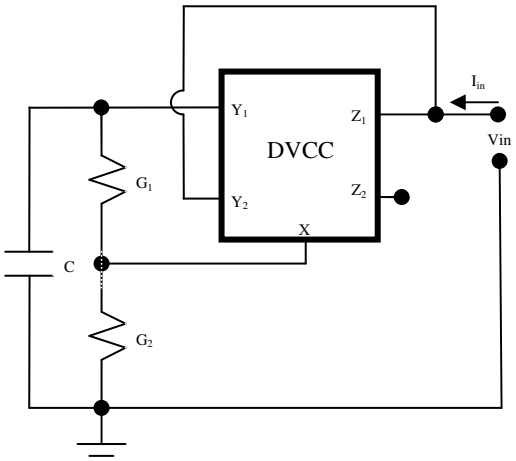

Figure A.6. Parallel R-L.

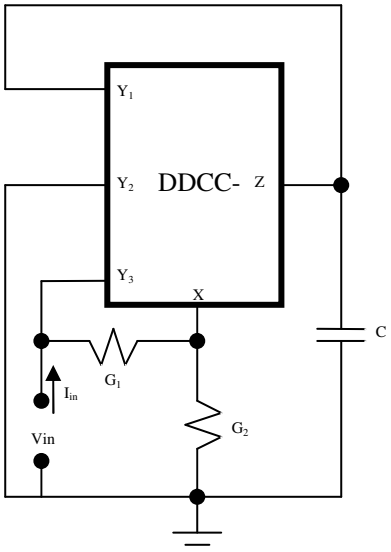

Figure A.7. Series R-L.

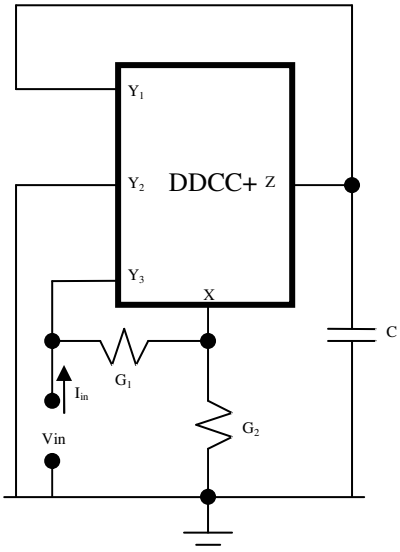

Figure A.8. Series R-(–L).

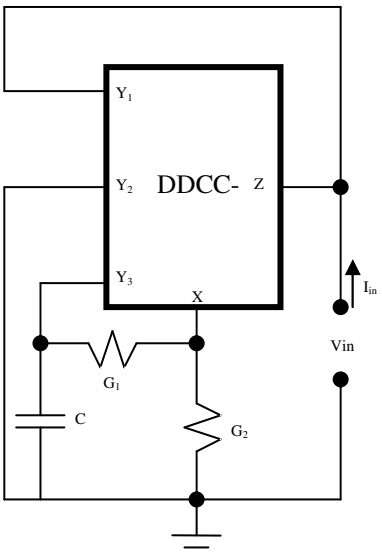

Figure A.9. Parallel R-L.

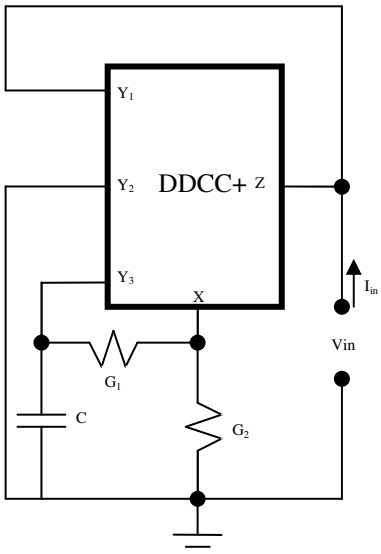

Figure A.10. Parallel (–R)-(–L).

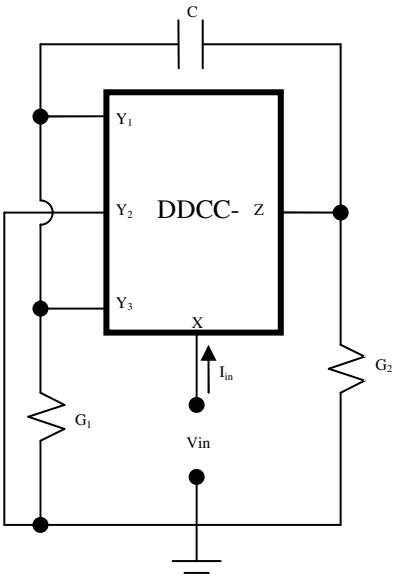

Figure A.11. Parallel R-L.

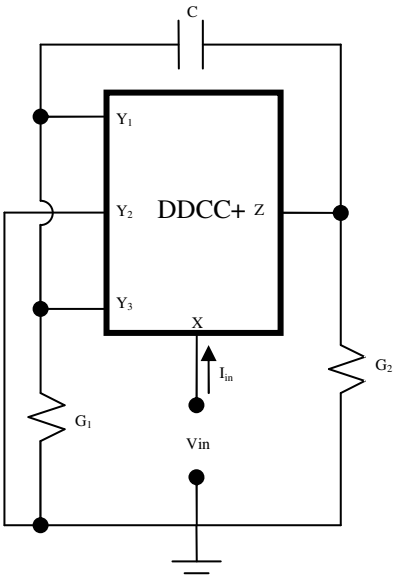

Figure A.12. Parallel (–R)-(–L).