DESIGN AND IMPLEMENTATION OF ALL-SIC MPPT BOOST CONVERTER FOR GRID CONNECTED PHOTOVOLTAIC SYSTEMS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

ELIF TUĞÇE KOÇ

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2019

Approval of the thesis:

DESIGN AND IMPLEMENTATION OF ALL-SIC MPPT BOOST CONVERTER FOR GRID CONNECTED PHOTOVOLTAIC SYSTEMS

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ABSTRACT

DESIGN AND IMPLEMENTATION OF ALL-SIC MPPT BOOST CONVERTER FOR GRID CONNECTED PHOTOVOLTAIC SYSTEMS

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September 2019, 92 pages

Output power generated by a photovoltaic array is prone to fluctuations during utilization due to varying solar irradiance exposure throughout the day and changes in cell temperature; therefore, maximum power point tracking is essential for overall system efficiency. For this purpose, DC-DC Maximum Power Point Tracker (MPPT) Converters are used in photovoltaic systems connected to the grid in order to extract the available power. SiC semiconductors are favorable new devices that enable greater power conversion efficiency than Si semiconductors; therefore, these devices have become strong candidates in new photovoltaic converter designs.

In this thesis, design, implementation and functional testing of a 10 kW All-SiC MPPT Boost Converter is presented. For power conversion efficiency comparisons, the converter was implemented in such a way that the power and control stages could be operated in four different configurations of which are Two-Phase Interleaved Boost Converter, Two-Phase Interleaved Synchronous Boost Converter, Conventional (Single-Phase) Boost Converter, Synchronous (Single-Phase) Boost Converter.

The designed converter was tested with a DC supply with photovoltaic power emulation capability at different input powers to analyze the operation and gather power conversion efficiency data of each configuration option. A calorimeter was designed and implemented as part of the thesis in order to estimate power conversion efficiency values.

Keywords: Maximum Power Point Tracking, Boost Converter, Interleaving, Silicon Carbide, Calorimeter

ÖZ

ŞEBEKE BAĞLANTILI FOTOVOLTAİK SISTEMLER İÇİN SIC MPPT BOOST DÖNÜŞTÜRÜCÜ TASARIM VE UYGULAMASI

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Eylül 2019, 92 sayfa

Bir fotovoltaik dizi tarafından üretilen güç, fotovoltaik dizinin maruz kaldığı farklı güneş ışınımı seviyeleri ve hücre sıcaklıklarından dolayı değişir; bu nedenle, sistem seviyesinde güç verimliliği için maksimum güç noktası takibi esastır. Bu amaçla, şebeke bağlantılı fotovoltaik sistemlerde DA-DA Maksimum Güç Noktası İzleyici (MPPT) Dönüştürücüler kullanılır. Silikon Karbür (SiC) yarı iletkenler, silikon (Si) yarı iletkenlerden daha fazla güç dönüşüm verimliliği sağlayan yeni cihazlardır; bu nedenle, bu cihazlar yeni fotovoltaik dönüştürücü tasarımlarında kullanım amaçlı güçlü adaylar haline gelmiştir.

Bu tez çalışmasında, 10 kW'lık ve tüm yarı iletkenleri SiC olan MPPT Boost Dönüştürücünün tasarım, uygulama ve fonksiyonel testleri sunulmaktadır. Güç dönüşüm verimliliklerini mukayese amaçlı, tasarlanan dönüştürücünün güç ve kontrol katı dört faklı konfigürasyonda çalıştırılabilir şekilde tasarlanmıştır. İlgili farklı konfigürasyonlar şöyledir; İki-Faz Dönüşümlü (Interleaved) Boost Dönüştürücü, İki Faz Dönüşümlü (Interleaved) Senkron Boost Dönüştürücü, Konvansiyonel (Tek Fazlı) Boost Dönüştürücü, Senkron (Tek Fazlı) Boost Dönüştürücü.

Tasarlanan dönüştürücünün, çalışma durumlarını analiz etmek için, farklı giriş güçlerinde, fotovoltaik güç emülasyon yeteneğine sahip bir DC beslemesi ile testler gerçekleştirilmiştir. Güç dönüşüm verimliliği değerlerini doğru bir şekilde elde etmek için tezin bir parçası olarak bir kalorimetre tasarlanıp kullanılmıştır.

Anahtar Kelimeler: Maksimum Güç Noktası İzleyici, Boost Dönüştürücü, Silikon Karbür, Kalorimetre

To my husband, family and everyone who is family to me

ACKNOWLEDGEMENTS

It is a genuine pleasure to express my deepest gratitude to my supervisor Prof. Dr. Muammer ERMİŞ, for his guidance and belief in me throughout this research and also since the day I enrolled master's program.

It is my privilege to thank Prof. Dr. Işık ÇADIRCI for her guidance and support in this work.

I am very grateful to Artı Endüstriyel Elektronik A.Ş. for supporting my enrolment to master's program and also making all the equipment for this thesis available, as well as sharing technical guidance.

I also would like to thank my husband Atila KOÇ, my family, and my friend Selen POSTACI for their never-ending support, patience, and confidence in me.

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LIST OF ABBREVIATIONS

ABBREVIATIONS

ADC	Analog to Digital Converter
CCM	Continuous Conduction Mode
DSP	Digital Signal Processor
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
PV	Photovoltaic
PWM	Pulse Width Modulation

CHAPTER 1

INTRODUCTION

1.1. Background and Motivation

From an environmental and reliability point of view, renewable energy, thanks to wind and solar power's modular and geographically spread-out installation nature, has hard to ignore benefits; however, until recently, renewable energy was an expensive source when compared to other energy sources.

This changed shortly before 2011 for wind power and 2013 for solar power, as both sources became cheaper than coal and nuclear power. As of 2018, the cost of wind and solar power is less than 50 USD/MWh.[1] This steep cost reduction resulted in tremendous amount of added renewable power generating capacity for some years now.

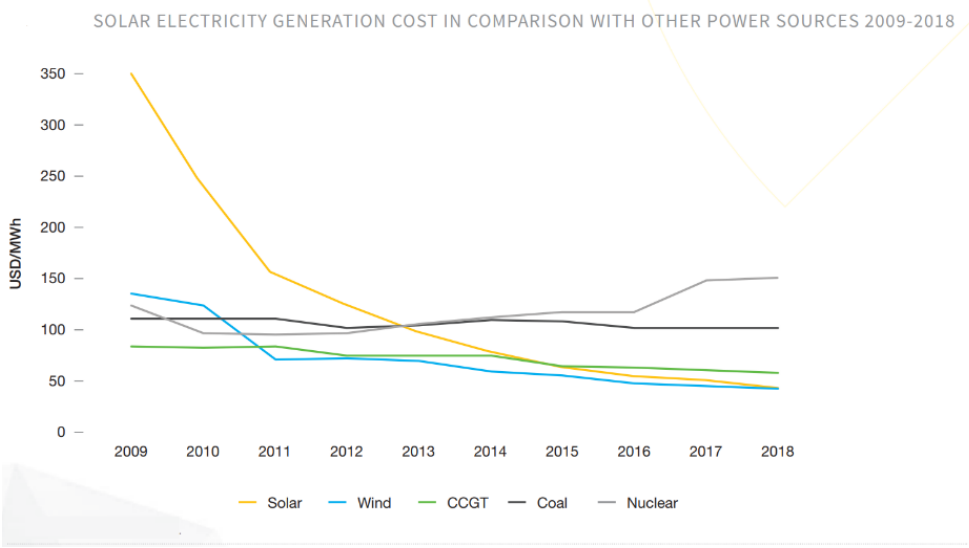


Figure 1.1. Electricity Generation Cost of Different Sources[1]

Taking a look at the 2018 data, solar power capacity added globally is 102 GW, surpassing all other energy sources by a considerable amount. [1]

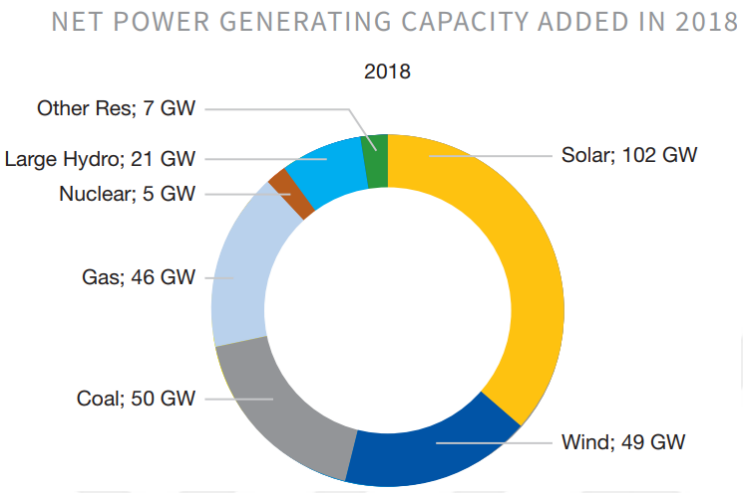


Figure 1.2. Power Capacity Added in 2018[1]

From these projections, it is safe to guess that renewables are going to power the future and create a lot of economic boost to countries that will not ignore this trend and make an investment. It is important to remember that wind and sunlight, unlike imported energy sources, will indeed increase a nation's energy independence.

In this thesis, an All-SiC MPPT converter's design and implementation are presented and MPPT converters are important system components when harvesting solar energy.

The first photovoltaic inverter application involving SiC semiconductors are reported in [2]. A review paper is presented in [3] on SiC based semiconductors and its applications in Photovoltaic Systems.

Several Boost Converters for photovoltaic applications with SiC semiconductors were previously published in the literature. In [4], a SiC diode based Interleaved Boost Converter is presented with a rated power of 2.5 kW. In [5], a SiC BJT and SiC diode

based (All-SiC) Conventional Boost Converter is reported with 98.2% efficiency and 5 kW of rated power. In [6], another All-SiC Interleaved Boost Converter is reported with 99% efficiency and 2.5 kW of rated power. In [7], an All- kW Interleaved Boost Converter is presented for a comparative study of Si IGBTs and SiC MOSFETs.

In this thesis work, for performance evaluation, the All-SiC MPPT Boost Converter presented was implemented in such a way that the power and control stages could be operated in four different configurations of which are Two-Phase Interleaved Boost Converter, Two-Phase Interleaved Synchronous Boost Converter, Conventional (Single-Phase) Boost Converter, Synchronous (Single-Phase) Boost Converter. This way a previously not reported, synchronous rectification action of an All-SiC Boost Converter is analyzed.

The resultant All-SiC MPPT Boost Converter was designed for interfacing with a grid-connected inverter in a multi-string photovoltaic system as seen in Figure 1.3.

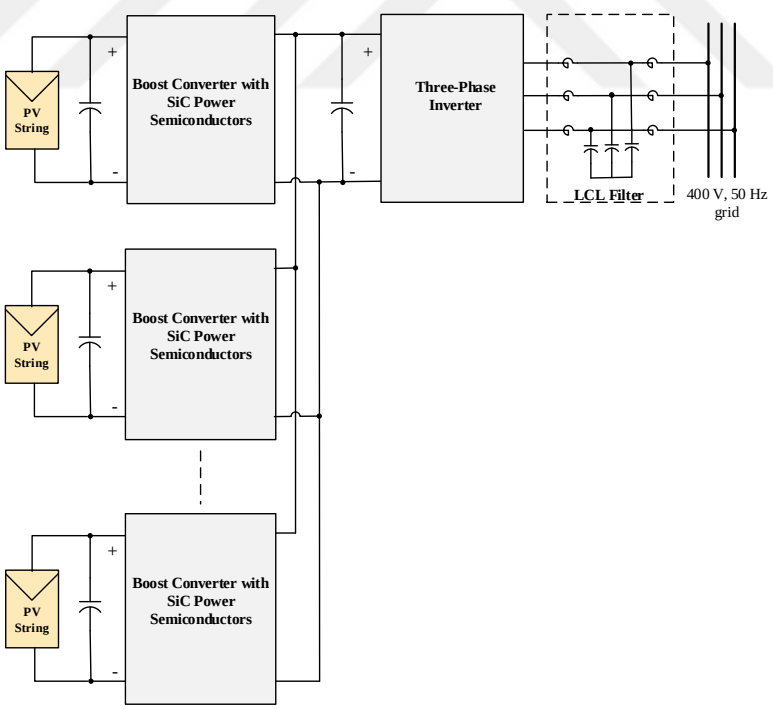


Figure 1.3. Photovoltaic System Integration with All-SiC MPPT Boost Converter

1.2. Necessity of MPPT

The electrical equivalent of a PV cell is given in Figure 1.4. Ideally, the circuit would only consist of a current source in parallel with a diode (that is no current flowing through the shunt resistor and having an Rs value of zero value). The resultant current produced by the solar cell is equal to the current provided by the current source deducted by the diode and shunt resistor currents.

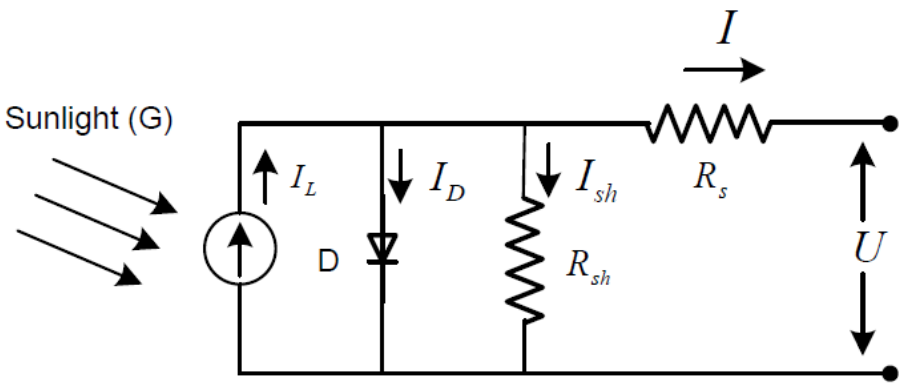


Figure 1 PV Cell Model

Figure 1.4. Equivalent Electrical Circuit of a PV Cell*[8]*

From this equivalent circuit, the I-V characteristic equation arrived is given as:

$$I = I_L - I_O(e^{\frac{q(V+IR_s)}{nkT}} - 1)$$

Equation 1-1[8]

The parameters I, I_L, I_O, q, n, k, and T denote the PV Cell output current, photo-generated current, reverse saturation current of the diode, electronic charge, diode ideality factor, Boltzmann constant and temperature in Kelvin respectively.

According to the equation, the I-V characteristic of a solar cell is non-linear and possess a maximum power point. In order to get the most utilization out of the system, module operation at the maximum power point is necessary.

The I-V curves and the maximum power point depend on cell temperature and irradiance. A typical module datasheet provides the I-V curves for different temperatures and irradiance levels. These curves also change from module to module. In Figure 1.5, I-V curves of a commercial module are given to demonstrate the issue. Due to the reasons mentioned, it is clear that the maximum power point must be tracked.

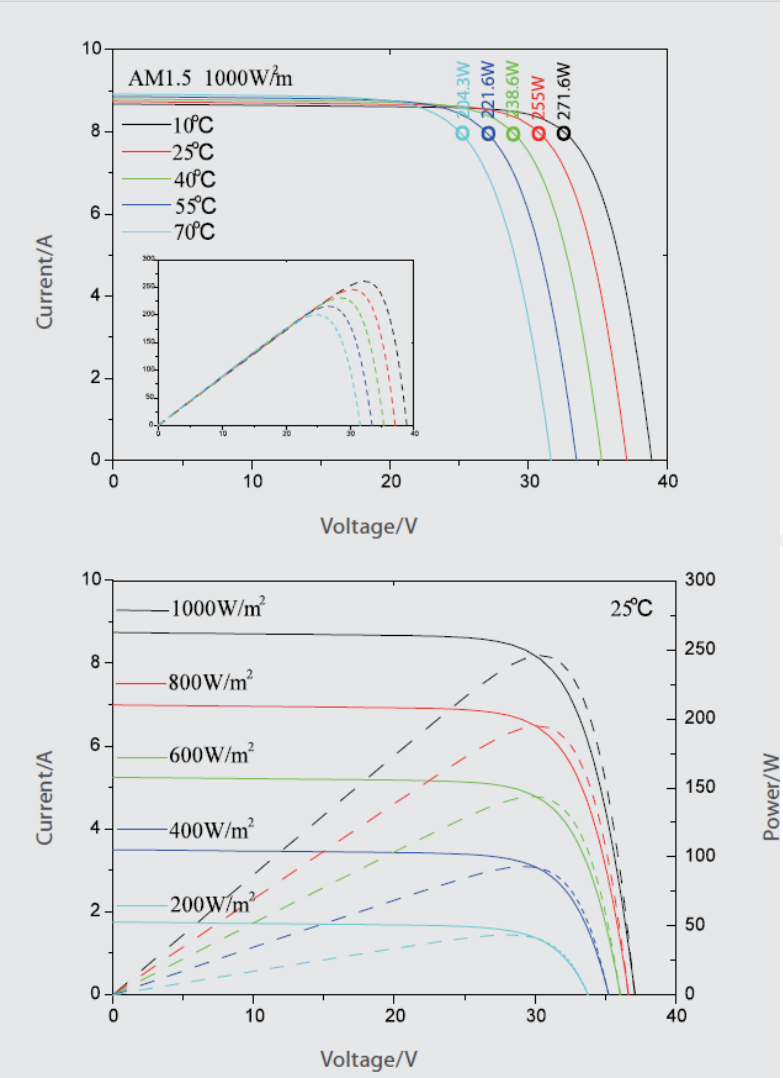


Figure 1.5. CSUN255-60P I-V Curves[9]

1.3. Utilization of SiC Devices

MPPT converter implemented as part of this thesis work utilizes SiC semiconductors. In this part, a briefing is given on SiC devices to explain this design choice.

Power electronics applications heavily rely on semiconductors. Power electronics semiconductors in use so far mostly constitute devices constructed from silicon (Si) material. Nowadays, this trend is slowly but surely changing, adapting the use of wide-band-gap (WBG) materials in manufacturing of power devices instead of Si devices.

What is considered a WBG material, is a material with an energy bandgap of 2 electron volts or more. That is the energy required by an electron to jump from the highest part of the valence band to the lowest part of the conduction band. With Si, this bandgap is 1.1 electron volts.

WBG technology enables greater voltage blocking capability at a shorter drift width thanks to a higher electrical field supported by it before the device enters avalanche breakdown. This allows, even with high voltage devices built by WBG materials to have a low drift resistance. This decrease in resistance ultimately mean, lower conduction losses. In terms of comparison, SiC material which is a WBG can be exposed to ten times more field than Si material before it breaks down. This means SiC devices can operate at the same voltage as the Si material with a material ten times thinner. Higher current density is archivable with SiC material this way. [10]

The speed achieved by an electron under a given electrical field is a measure of electron mobility. Electron mobility is a property that affects the electrical resistance of a material. With WBG, electron mobility is also another advantage that decreases electrical resistance and conduction losses.

Terminal capacitances are lower in WBG materials owing to electric field permittivity, enabling achievement of lower losses at faster switching speeds. [11]

WBG material is also favourable when it comes to thermal management, as the energy bandgap is high, higher junction temperatures do not disrupt the electrical properties

of the material to a certain extent. Operation at higher temperatures is permitted owing to this.

It also turns out that similar design methodology to that of Si devices applies to WBG materials, as long as the faster switching dynamics of these devices are taken into the account in terms of managing the circuit parasitics. This makes the use of such devices even more attractive, as design conventions are long developed and therefore easily adaptable.

Silicon Carbide (SiC) and Gallium Nitride (GaN) materials are examples of wide-band-gap materials. Whilst GaN-based power semiconductors are considered for use in 200 to 900 V range, SiC-based devices are strong candidates for the 900 to 15000 V rated applications. Even more availability and better reliability is expected to carry WBG devices in the place of Si devices in the near future, especially for 600 to 1700 V range. [12]

This change of convention is thanks to the emerging availability of WBG technology from several suppliers. With the increase in production and therefore the decrease in prices, performance advantages of WBG materials are making its way into the industry, as the designers can now consider these devices as valid and value-for-money options. [13]

Discussion on Utilization of SiC MOSFETs and Si IGBTs in Boost Converters:

In [14], for Voltage Source Inverter design, it is demonstrated that, due to significantly reduced switching losses, a SiC MOSFET of a certain current rating could replace a Si IGBT of a much higher current rating. It is also explained that, because rated SiC current ratings do not equal rated Si current ratings at the system level, SiC-based designs require evaluation of price per system power ($/kW) as the key cost metric rather than price per rated Ampere.

To illustrate the cost/kW and power conversion efficiency benefits that can be obtained with the utilization of SiC MOSFETs in boost converters, two hypothetical converter design cases are presented.

In the first case, a conventional boost converter implementation with a Si IGBT switch is analyzed. In the second case, a conventional boost converter implementation with a SiC MOSFET is studied.

For a fair comparison, the devices selected for this discussion which have the same module configuration are mechanically and electrically similar in terms of module size, maximum nominal current and maximum blocking voltage ratings. Summary of important device parameters are given in Table 1.1. For the first case, a Si IGBT switch by Infineon with part number FF150R12KT3G was chosen. For the second case, a SiC MOSFET switch by CREE with part number CAS120M12BM2 was selected.

Table 1.1. *Summary of Device Parameters*

Specification Type	***Si IGBT*** ***FF150R12KT3G***	***SiC MOSFET*** ***CAS120M12BM2***
Maximum Switch Voltage	1200 V	1200 V
Nominal Current Rating	150 A	120 A
Conducting Voltage	$V_{CE(on)}$ = 1.7 V	$V_{DS(on)}$ = 1.56 V
at T_J = 25 ˚C	at V_{GE} = 15 V, I_C = 150 A	at V_{GS} = 20 V, I_{DS} = 120 A
Conducting Voltage	$V_{CE(on)}$ = 1.9 V	$V_{DS(on)}$ = 2.76 V
at T_J = 125 ˚C and T_J = 150 ˚C	at T_J = 125 ˚C, V_{GE} = 15 V, I_C = 150 A	at T_J = 150 ˚C, V_{GS} = 20 V, I_{DS} = 120 A
Switching Energy	E_{on} = 11 mJ, E_{off} = 22 mJ	E_{on} = 1.7 mJ, E_{off} = 0.4 mJ
	at T_J = 125 ˚C, V_{CE} = 600 V, I_C = 150 A	at T_J = 150 ˚C, V_{DE} = 600 V, I_{DS} = 120 A

For the quantitative analysis carried out in this discussion, Infineon's IPOSIM Design Simulator and CREE's Speedfit Design Simulator were used.

Switching frequency was decided as 20 kHz. A heatsink temperature of 70 ˚C was assumed. Input supply voltage was decided as 630 V, whilst the output voltage was selected to be 700 V.

Another assumption made was that the energy storage elements were ideal and of same value for both designs. Diode of the boost converters were also assumed as ideal diodes.

The simulations were run for operations close to maximum permissible junction temperatures, to be able to determine the maximum output power achievable using the selected devices. From this, the cost/kW was calculated.

Table 1.2. *Theoretical Performance Comparison of Conventional Boost Converters Implemented with Si IGBT and SiC MOSFET*

	Si IGBT	*SiC MOSFET*
Part Number	*FF150R12KT3G*	*CAS120M12BM2*
Input Power (kW)	24.72	150.07
Output Power (kW)	24.50	149.90
Switching Losses (W)	218.40	117.60
Conduction Losses (W)	4.10	50.51
Efficiency (%)	99.1	99.89
Cost per Module ($)	90	330
Cost per kW ($)	3.67	2.20

From Table 1.2, it can be seen that, for the same module size, a superior efficiency, a higher converter output power, and lower cost per kW can be achieved with a SiC MOSFET when compared to Si IGBT for use with boost converters.

CHAPTER 2

BOOST CONVERTER OPERATION

2.1. Introduction

To extract the maximum power available by the photovoltaic array and convert the DC voltage of the PV array to an acceptable level by the inverter, in a grid-connected system, a front-end converter is used. One of the most popular non-isolated converter utilized for this type of application is an MPPT converting boost converter.

At operation, the boost converter output voltage is always greater than the input voltage. This is achieved thanks to the inductor in the topology. The stored energy in the inductor is dumped to the load at a higher voltage. A standard boost converter is shown in Figure 2.1.

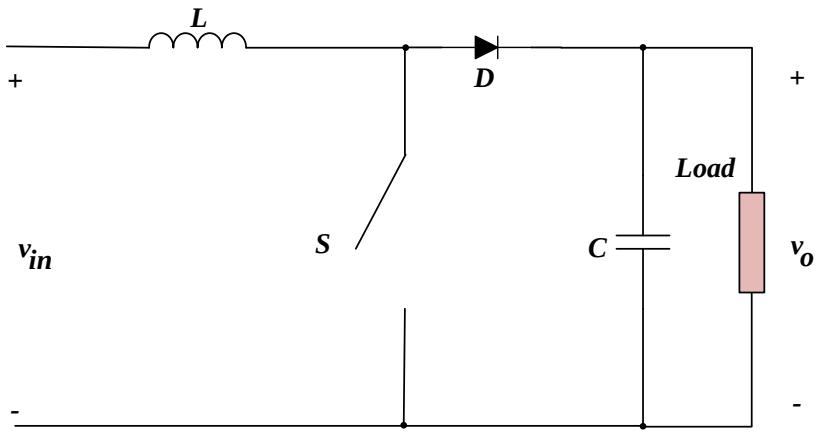


Figure 2.1. Conventional Boost Converter Diagram

The ideal operational case desired for this front-end converter in a photovoltaic system would be the converter running with almost zero input current ripple so that there are no oscillations around MPP. Also, converter efficiency minimally decreasing with lighter loads is wanted quality since the input power constantly changes during the day. The simplicity of boost converters allows for designs that meet these specifications to some extent.

In this chapter, conventional boost converter and multiphase interleaved boost converter power stages are analyzed and discussed. To aid the discussions, some simulations were carried out with GeckoCIRCUITS (a light-weight open-source and cross-platform (JAVA) power electronics simulator) to obtain operational waveforms of importance.

2.2. Conventional Boost Converter

In this section, the conventional boost converter operation for the continuous conduction mode (CCM) is described. In this thesis the boost converter is designed to operate in CCM mode for a wide power range. Boost converter equations commonly derived in power electronics references are not produced once again in this thesis, as it is readily available. One can always refer to [15], [16].

If the boost converter switch is left unoperated (when the duty cycle is zero), the output capacitor gets charged to the input voltage (minus the voltage drop in the diode); and therefore, the output voltage becomes the same as the input voltage. This is the minimum voltage achievable at the output of a boost converter.

The switch of the boost converter is controlled with a PWM signal. Two operational modes arise from turning the switch “on” and “off” with the PWM signal. Each mode is given in Figure 2.3 and Figure 2.4.

Figure 2.5 is obtained by the GeckoCIRCUITS simulator tool with a current source as the load. Individual graphs are obtained by zooming in the y-axis at different scales,

for readable measurements in order to be able to compare the waveforms. The circuit simulated is given in Figure 2.2.

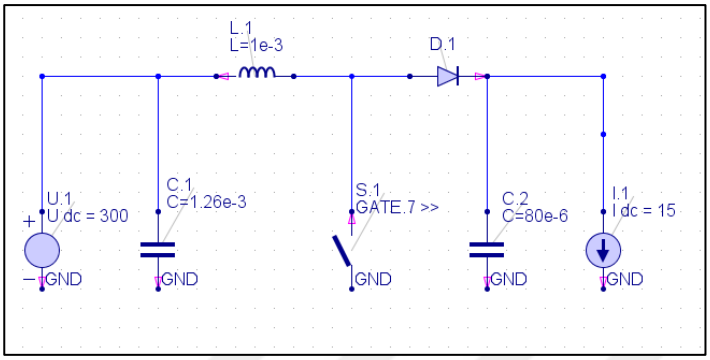


Figure 2.2. Simulated Boost Converter Circuit Diagram, Input Voltage Source: 300 V, Output Current: 15 A, C1: 1.26 mF, L1: 1 mH, C2: 80 uF

From Figure 2.5, it can be seen that the input voltage of 300 V (see the source in Figure 2.2) is boosted to 500 V at the output.

In Mode-1, where the switch is made “on” by a “high” gate signal, the diode is reverse biased, and the inductor is storing energy by creating a magnetic field, thus its current rises. The load is supplied from the output capacitor; therefore, at this mode the capacitor discharges. This operational mode is depicted in Figure 2.3.

In Figure 2.5, it can be seen that, when the gate signal is high, as explained, the inductor current rises and the output voltage ripple slope is negative due to capacitor discharging through the load.

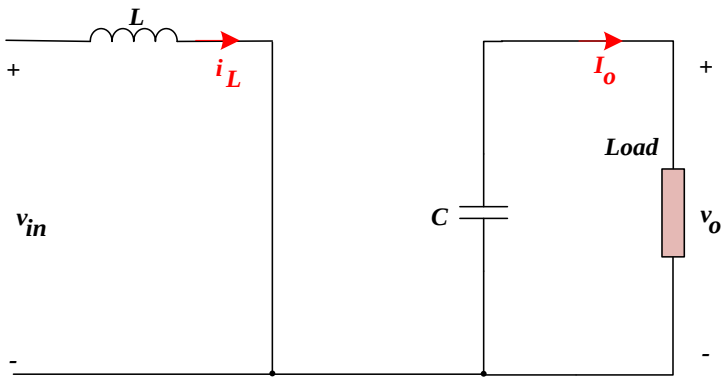


Figure 2.3. Conventional Boost Converter Operational Mode-1 Representation

In Mode-2, where the switch is made “off” by a “low” gate signal, the magnetic field created in Mode-1 collapses, and the current through the inductor starts falling. The change of polarity in the slope of the inductor current translates to change of voltage polarity across the inductor since the voltage across an inductor is the product of inductance of the inductor and the rate of change of current. In this mode, the capacitor is charged via the diode in the circuit to a higher voltage, which is the sum of the supply voltage and the voltage formed across the inductor due to the change of current. This operational mode is depicted in Figure 2.4.

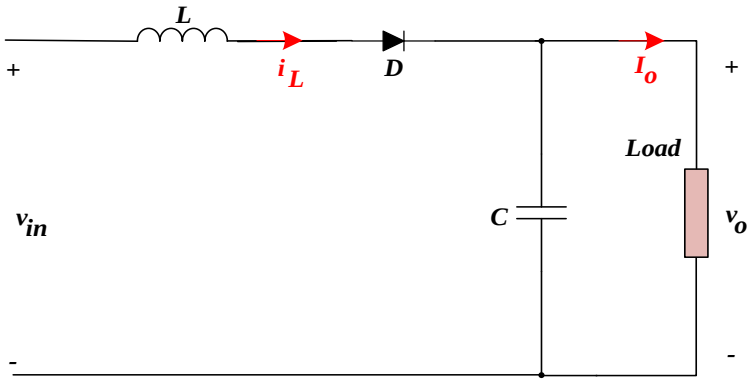


Figure 2.4. Conventional Boost Converter Operational Mode-2 Representation

In Figure 2.5, it can be seen that, when the gate signal is low, as explained, the inductor current falls and the output voltage ripple slope is positive due to capacitor charging from the source.

The duration in which the switch is made “on” (i.e. duty cycle), controls the value of the output voltage (in this case the duty cycle is set to 40%); however, the switch can never be made fully “on”, (ie. duty cycle being 100%). If this happens, the output voltage plummets, and the circuit is damaged as a consequence.

Some important findings to note here (which is compared with the case in the next section) is that the ripple frequency of all waveforms is the same as the switching frequency. The input current ripple is 6 A which is 24 % of the mean input current of 25 A. The output capacitor current ripple is 28 A, and the output voltage ripple is 3.5 V.

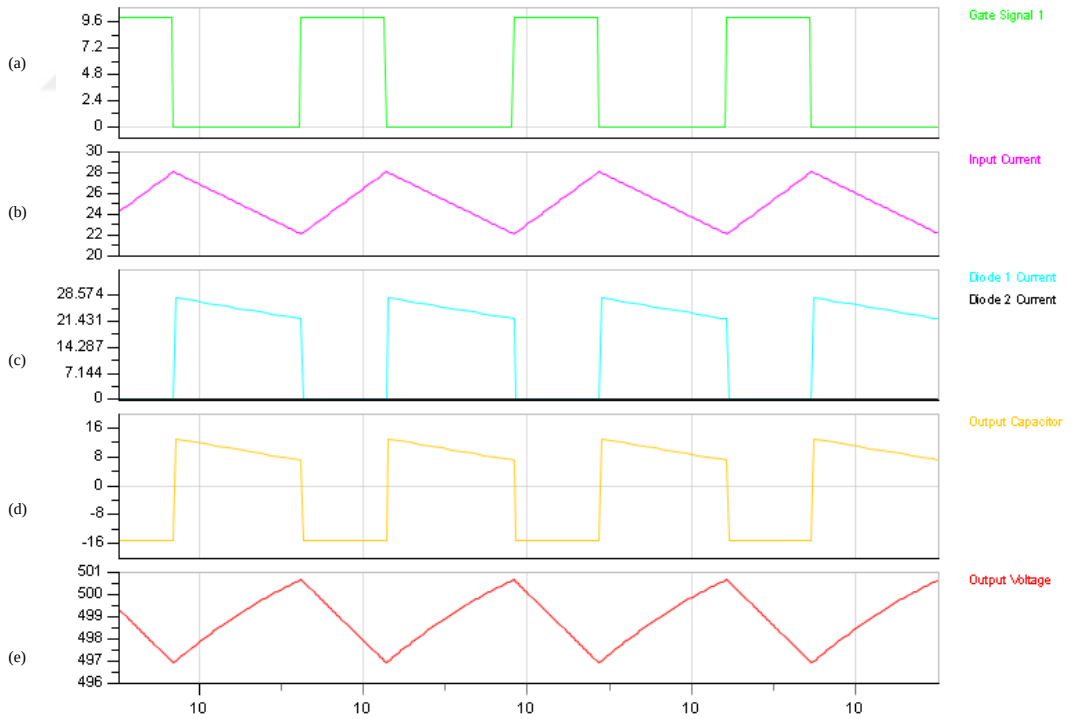


Figure 2.5. Conventional Boost Converter Critical Operational Waveforms Obtained with Power Electronics Simulator (24 us time division) Y-Axis: (a) 20 kHz Gate Signal (V), (b) Inductor Current (A), (d) Output Capacitor Current (A), (e) Output Voltage (V)

2.3. Multiphase Interleaved Boost Converter

Interleaving is a power stage paralleling technique in which the power converter switches are operated at the same duty ratio in a phase shifted manner with respect to each other.

An "N" phase interleaved converter, is a power converter consisting of "N" number of identical power stages paralleled at the input and at the output. The phase difference between each gate signal depends on the number of phases and is 360º/N. If a balance of phases is ensured by careful design, the current is shared among phases equally, having a positive effect on conduction losses.

Phase shifting is essential as it reduces the overall current ripples in the input and output stages.[17] Simply paralleling without phase-shifting, (that is the same control signal applied to each stage) results in ripple multiplication. In other words, it is "N" times more than what would result if the same power stage is implemented in a single-phase manner.

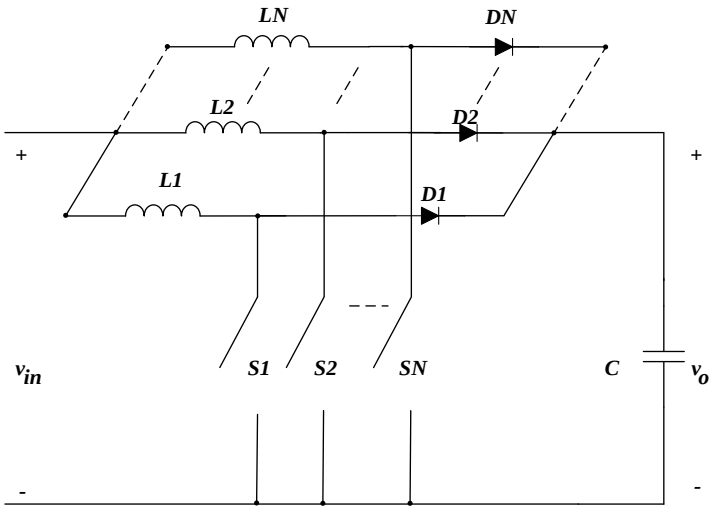


Figure 2.6. "N" Phase Boost Converter Diagram

In this section, multiphase interleaved boost converter topology is analyzed. A depiction of an “N” phase boost converter is given in Figure 2.6.

Similar to the conventional boost converter, if all the switches of the interleaved boost converter are left unoperated (when the duty cycle is zero), the output capacitor gets charged to the input voltage. The duration in which the switches are made “on” (i.e. duty cycle), controls the value of the output voltage, just like in conventional boost converter, with the same input to output voltage transfer ratio.

More than two operational modes arise in a multiphase boost converter unlike the conventional boost converter. To elaborate on this, a two-phase boost converter circuit is presented in Figure 2.7.

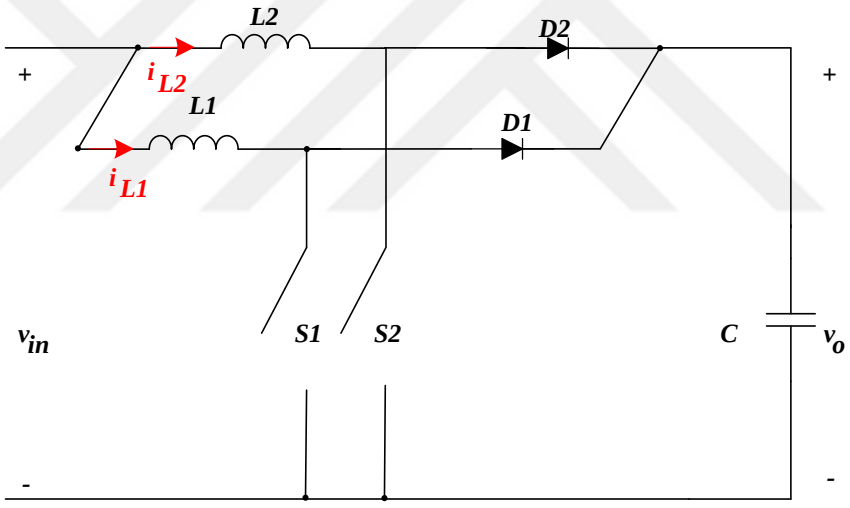


Figure 2.7. Two-Phase Boost Converter Diagram

Operational modes for the two-phase boost converter, operating with a duty cycle less than 50%, are given in Figure 2.9. For duty cycle larger than 50%, another mode arises where both of the switches are conducting at the same time; however, the converter designed in this thesis work is not operated in this mode.

To explain the modes, Figure 2.10 obtained by the GeckoCIRCUITS simulator tool with a two-phase boost converter implementation is made use of. This circuit is obtained by paralleling the same power stage presented in Figure 2.2. Individual graphs are obtained by zooming in the y-axis at different scales, for readable measurements in order to be able to compare waveforms. The circuit simulated is given in Figure 2.8.

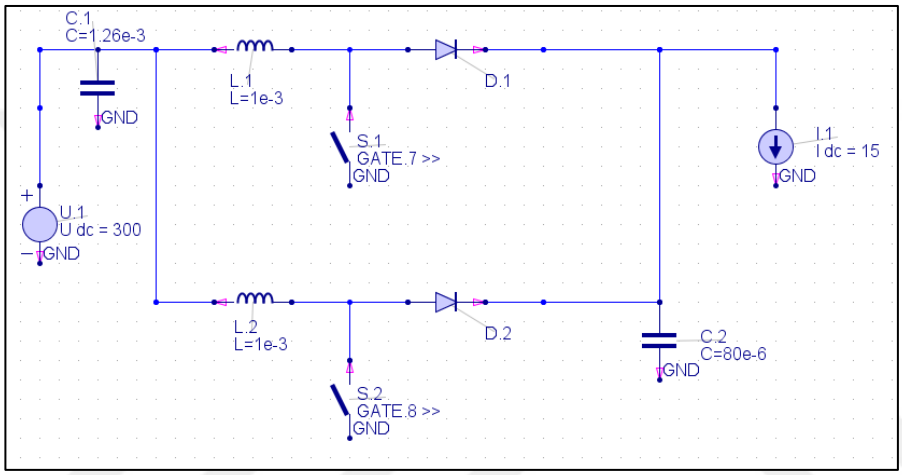
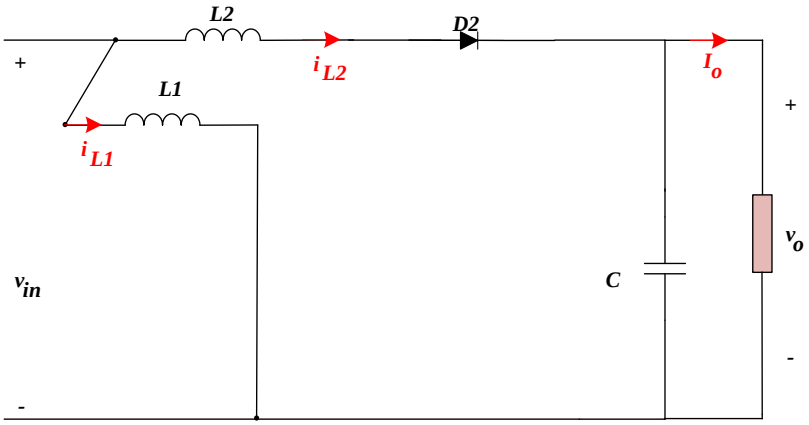


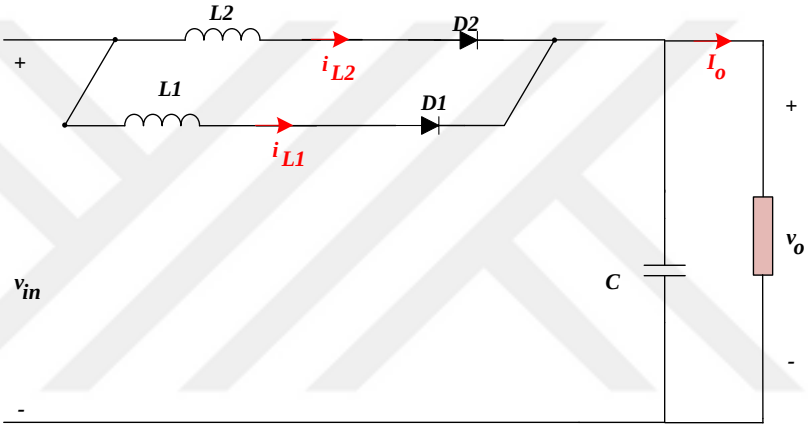
Figure 2.8. Simulated Two-Phase Interleaved Boost Converter Circuit Diagram, Input Voltage Source: 300 V, Output Current: 15A, C1: 1.26 mF, L1: 1mH, L2: 1mH, C2: 80 uF

From Figure 2.10, it can be seen that the input voltage of 300 V (see the source in Figure 2.8) is boosted to 500 V at the output. As once again the duty cycle is set to 40%, to be able to make a comparison with the conventional boost converter.

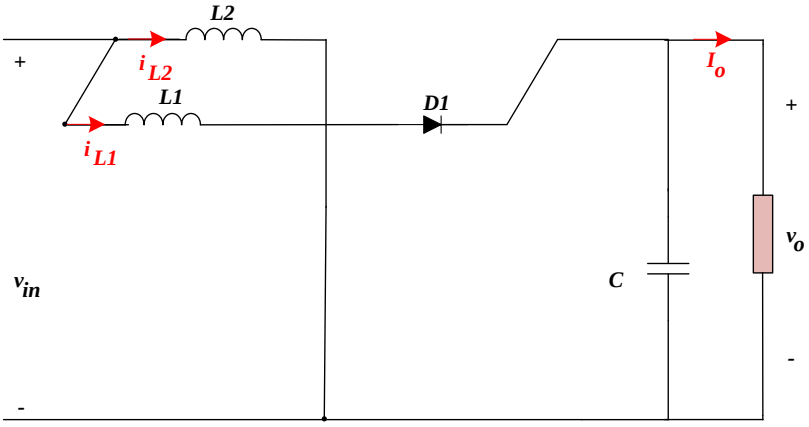
In Mode-1, where the S1 switch is made "on" (at that instant S2 is "off" and L2 current is falling), the diode D1 is reverse biased, and the inductor L1 current rises. In this mode, the capacitor is charged via diode D2 in the circuit to a higher voltage, which is the sum of the supply voltage and the voltage formed across the inductor due to the change of current. This operational mode is depicted in Figure 2.9 (a).



(a) Mode-1



(b) Mode-2 and Mode-4



(c) Mode-3

Figure 2.9. Two-Phase Boost Converter Modes of Operation for Duty Cycles Less Than 50%, (a) Mode-1, (b) Mode-2 and Mode-4, (c) Mode-3

In Mode-2, the switch S1 is made “off” (when S2 is already not conducting), and the magnetic field of L1 collapses, and the current through the L1 starts falling (whilst L2 current is still falling). In this mode the load is supplied from the output capacitor; therefore, at this mode the capacitor discharges. This operational mode is depicted in Figure 2.9 (b).

In Mode-3, is similar to Mode-1. Only this time S2 is “on” instead of “S1”. This operational mode is depicted in Figure 2.9 (c). After Mode-3, converter goes into Mode-4 which is exactly the same as Mode-1; therefore, completion of this mode starts Mode-2 once again and the cycle is repeated.

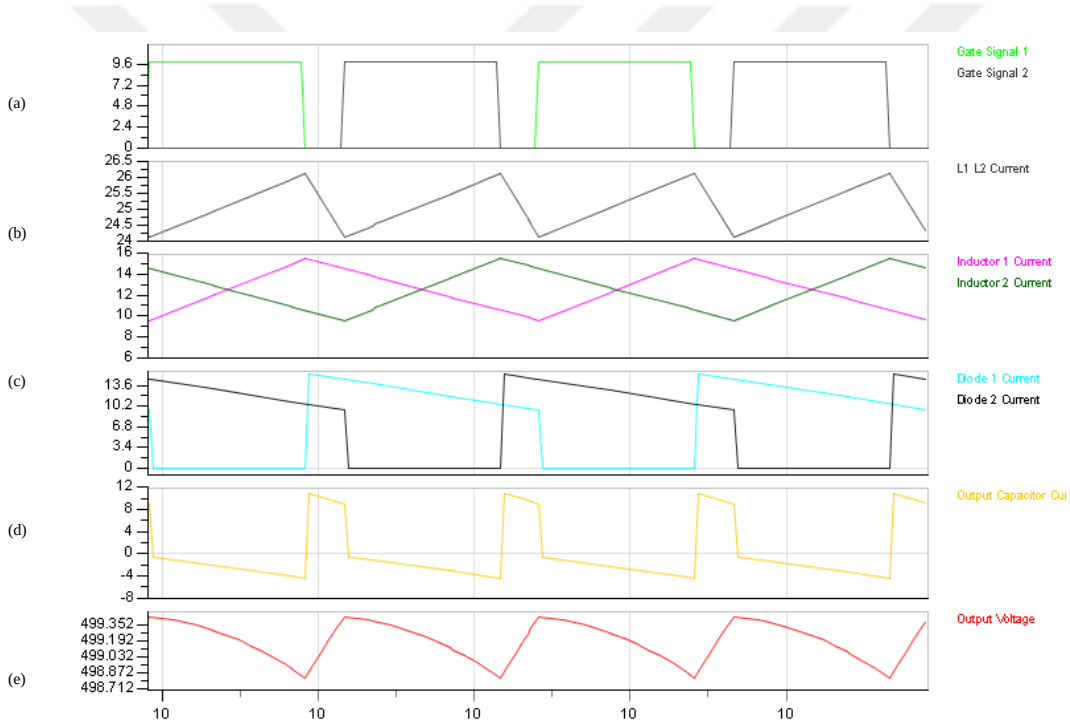


Figure 2.10. Two-Phase Interleaved Boost Converter Critical Operational Waveforms Obtained with Power Electronics Simulator (20 us time division) Y-Axis: (a) 20 kHz Gate Signals (V), (b) Input Current (A), (c) Inductor Currents (A), (d) Output Capacitor Current (A), (e) Output Voltage (V)

Please note that in Figure 2.10, the average inductor and diode currents are halved when compared to Figure 2.5, as two phases share the currents equally. In addition, the effective switching frequency is doubled when input and output currents are

investigated. Because of the ripple canceling effect of multiphase topology, the input current ripple, the output capacitor current and voltage ripple are all reduced. The input current ripple is reduced to 2 A from 6 A when compared to the conventional boost converter case which is a reduction from 24% to 8%. The output capacitor current ripple is 15 A, and the output voltage ripple is less than 1 V.

To explain this ripple cancellation phenomenon further, with the aid of the generalized current and voltage ripple equations derived in [17], normalized graphs in Figure 2.11 and Figure 2.12 are obtained for converters with one, two and three phases.

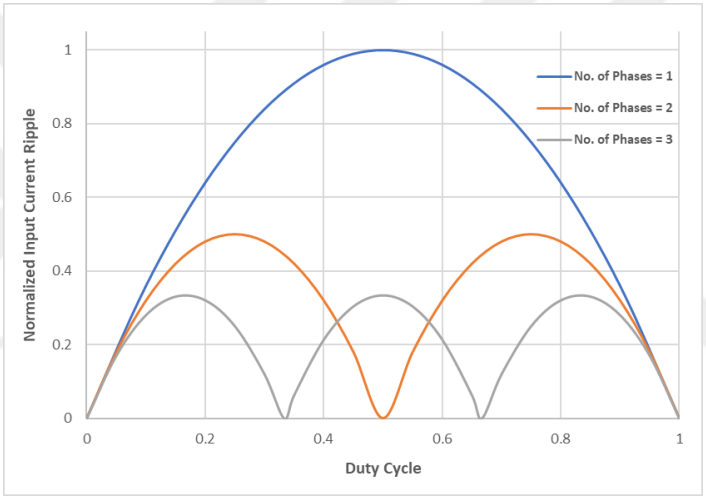


Figure 2.11. Normalized Input Current Ripple vs. Duty Cycle for Different Number of Phases

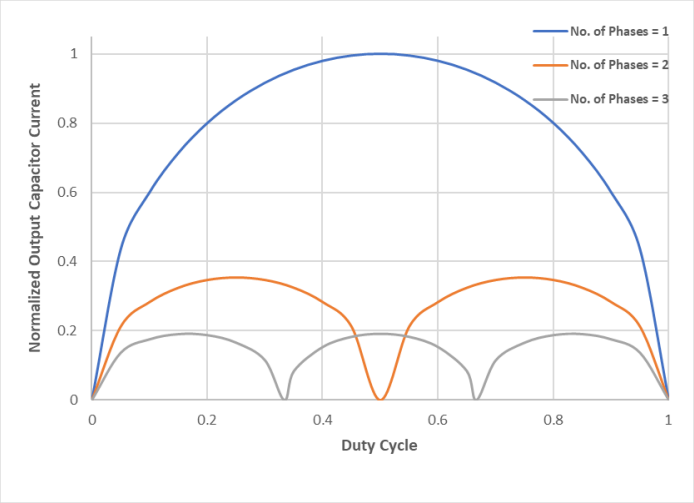


Figure 2.12. Normalized Output Capacitor Current Ripple vs. Duty Cycle for Different Number of Phases

From the graphs, it can be seen that both the input current ripple and the output capacitor current ripple depend on the operating duty cycle and the number of phases. With each phase added, the maximum ripple gets smaller and smaller.

CHAPTER 3

DESIGN AND IMPLEMENTATION OF POWER AND CONTROL STAGE

3.1. Introduction

In this chapter, the design and implementation processes are explained in detail, and in this introduction section, a description of the whole implementation is given in a simplified manner, so that the design decisions are better understood in the following sections of this chapter.

The power and control stages were designed in mind for accommodating four different configuration options. Mentioned options are listed below:

- Two-Phase Interleaved Synchronous Boost Converter
- Two-Phase Interleaved Boost Converter
- Synchronous Boost Converter
- Conventional Boost Converter

In order to allow the device to operate in any four of the options with minimum alteration, embedded software, mechanical and electrical design were altogether developed to allow this requirement. Doing this enabled the thorough investigation of all the design options by testing and collecting data.

As a result, the device had one large bill of materials that includes the necessary resource for all four of the arrangements and reduced bill of materials for individual options. Figure 3.1 to Figure 3.4 shows the power and control stages of implemented device configurations. From Table 3.1 to Table 3.3, all the resulting bill of materials are given. Designators given in tables and “Power and Control Stage” figures are matched for clarity.

It is seen from the figures and Bill of Materials tables that; some components are common for all the configurations. For the power stage, the input and output capacitors are common. In terms of thermal design, the heatsink is the same for all. Sensor data acquisition, signal conditioning, and MPPT algorithm are matching for all four options, as well as the overvoltage protection.

Owing to MOSFET's reverse conduction capability (unlike IGBTs), boost converters diode can be replaced with a MOSFET for synchronous rectification. Synchronous rectification enables lower conduction losses.

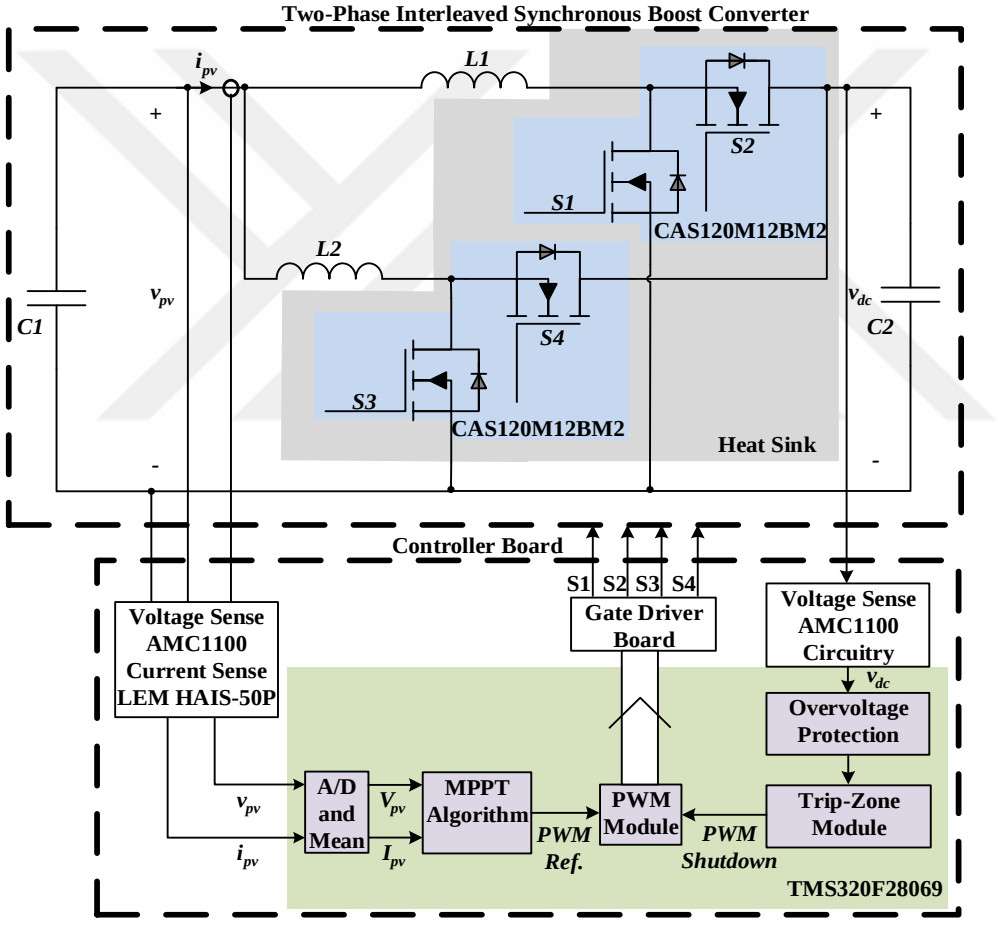


Figure 3.1. Two-Phase Interleaved Synchronous Boost Converter Power and Control Stages

In Figure 3.1, it is seen that two inductors and four MOSFETs of two SiC half-bridges are utilized to implement the Two-Phase Interleaved Synchronous Boost Converter. Instead of the conventional way of using a diode in the boost converter, in order to make use of the benefits of synchronous rectification, upper MOSFETs of the half-bridges are used. Control stage of this configuration produces four PWM signals which are transformed into gate signals via four gate driver circuitries.

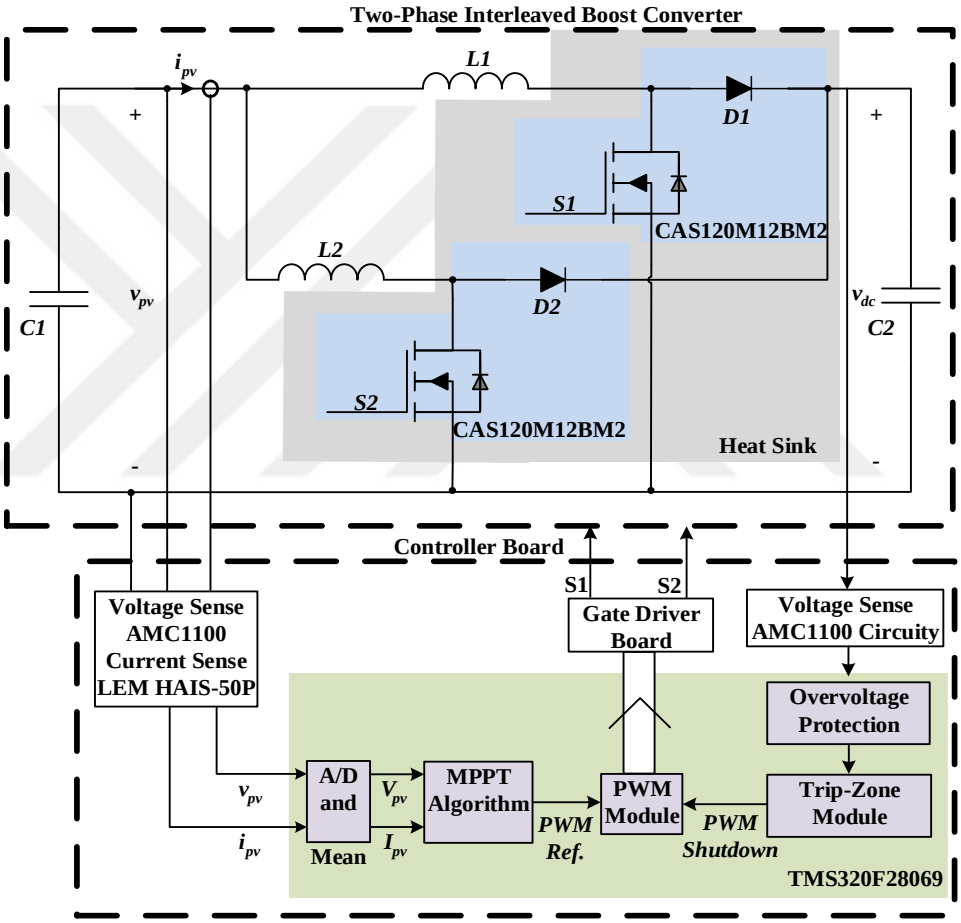


Figure 3.2. Two-Phase Interleaved Boost Converter Power and Control Stages

In Figure 3.2, it is seen that, two inductors and two MOSFETs of two SiC half bridges are utilized to implement the Two-Phase Interleaved Boost Converter. For each

interleaved converter, body diodes of upper MOSFETs of the half bridges are made use of, and upper MOSFETs are never activated in this configuration. The control stage of this configuration produces two PWM signals which are transformed into gate signals via two gate driver circuitries.

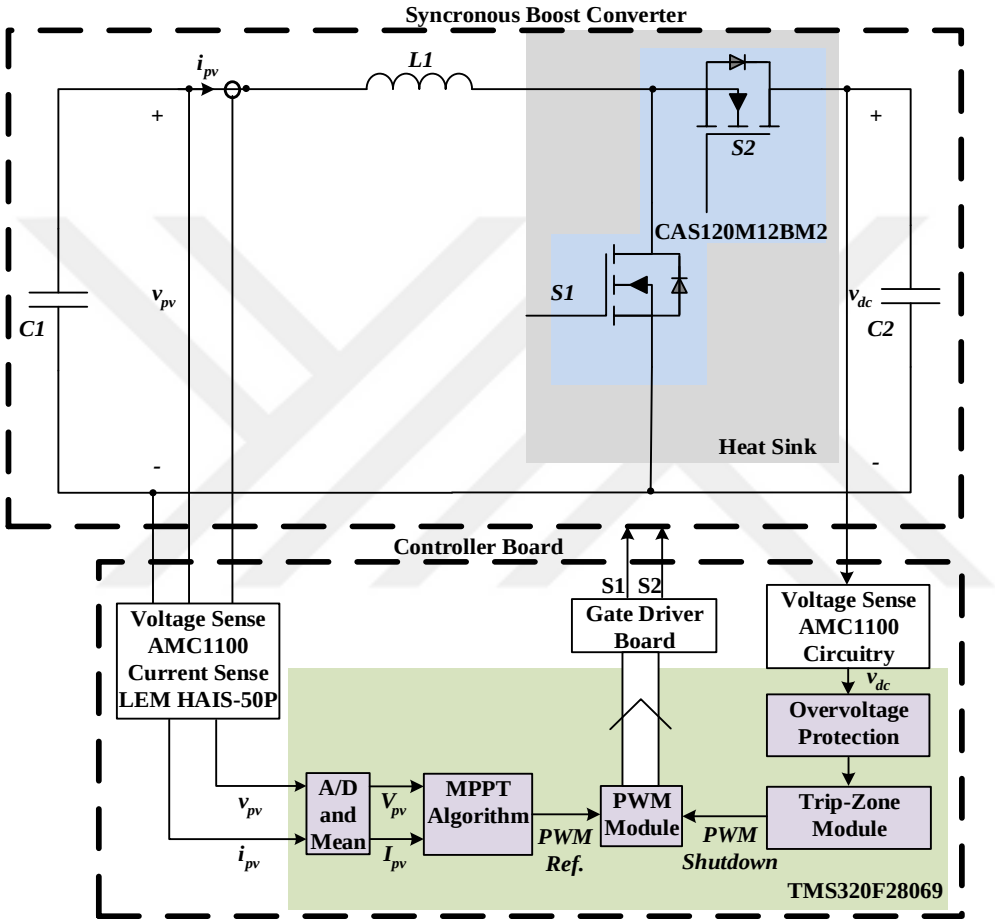


Figure 3.3. Synchronous Boost Converter Power and Control Stages

In Figure 3.3, it is seen that one inductor and two MOSFETs of one SiC half-bridge are utilized to implement the Synchronous Boost Converter. Instead of the conventional way of using a diode in the boost converter, in order to make use of the benefits of synchronous rectification, upper MOSFET of the half-bridge is used. The

control stage of this configuration produces two PWM signals which are transformed into gate signals via two gate driver circuitries.

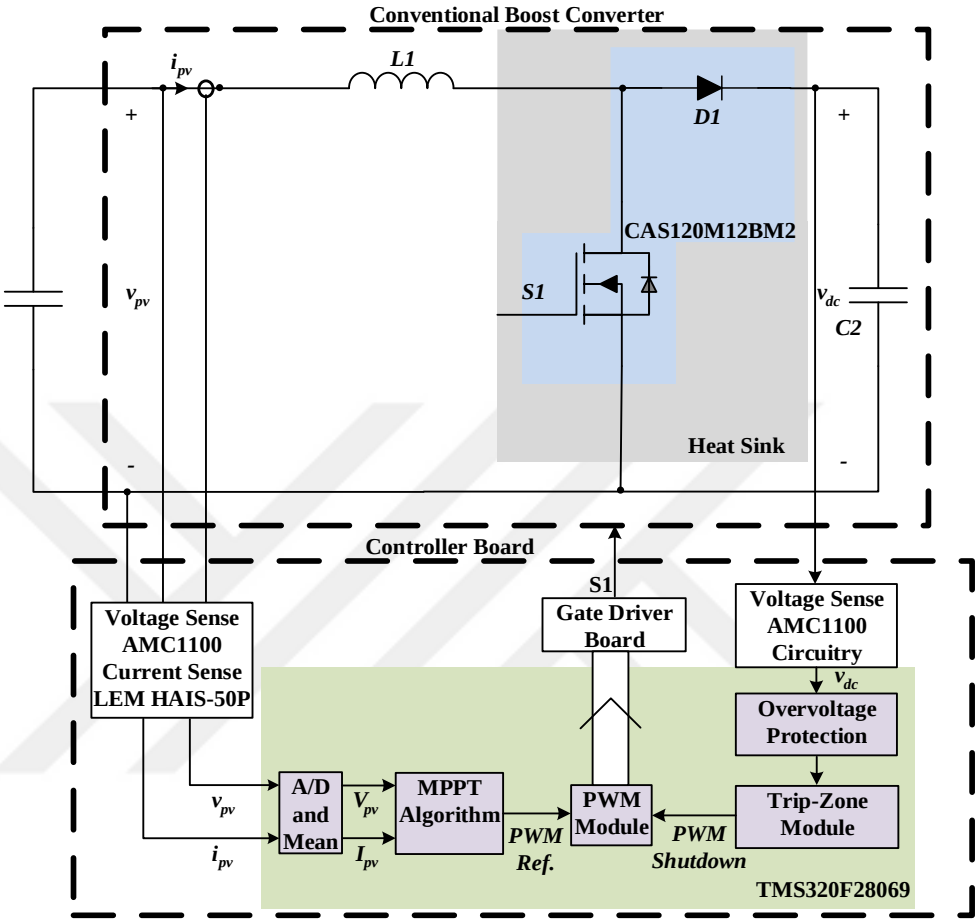


Figure 3.4. Conventional Boost Converter Power and Control Stages

In Figure 3.4, it is seen that one inductor and one MOSFET of one SiC half-bridge are utilized to implement the Conventional Boost Converter. Body diode of upper MOSFET of the half-bridge is made use of, and upper MOSFET is not activated in this configuration. The control stage of this configuration produces one PWM signal which is transformed into a gate signal via a gate driver circuit.

In Table 3.1 Bill of Materials for all the components used are given along with their description and quantity.

Table 3.1. *Bill of Materials for All the Parts*

Part Number	*Description*	*Quantity*
HAS-50S	LEM Current Sensor	1
78907-A7	Magnetics Core	2
CAS120M12BM2	Wolfspeed SiC Half-Bridge	2
Gate Driver Board	4 Gate Drive Circuits	1
Control Board	MCU and Digital/Analog IOs	1
B32778G306K	EPCOS 30 µF Film Capacitor	2
B32778G0406K000	EPCOS 40 µF Film Capacitor	2
LA 10 250 24	Fischer Heatsink with Fan	1

In Table 3.2 Bill of Materials for the two kinds of Two-Phase Interleaved Boost Converters are given and as well as the corresponding designators for the components utilized. The implemented converters have a theoretical power rating of 20 kW and the total cost (excluding the electronic boards and the heatsink) is 890 $. This yields a cost/kW of 44 $.

Table 3.2. *Bill of Materials for Two-Phase Interleaved Boost Converter (TPIBC) and Two-Phase Interleaved Synchronous Boost Converter (TPISBC)*

Part Number	*Designator for TPIBC*	*Designator for TPISBC*	*Quantity*
HAS-50S	LEM1	LEM1	1
78907-A7	L1, L2	L1, L2	2
CAS120M12BM2	S1, S2, S3, S4	S1, D1, S2, D2	2
Gate Driver Board	U1	U1	1
Control Board	U2	U2	1
B32778G306K	C1	C1	2
B32778G0406K000	C2	C2	2
LA 10 250 24	M1	M1	1

In Table 3.3 Bill of Materials for the two kinds of Boost Converters are given and as well as the corresponding designators for the components utilized. The implemented converters have a power rating of 10 kW and the total cost (excluding the electronic boards and the heatsink) is 500 $. This yields a cost/kW of 50 $.

Table 3.3. *Bill of Materials for Conventional Boost Converter (CBC) and Synchronous Boost Converter (SBC)*

Part Number	*Designator for CBC*	*Designator for SBC*	*Quantity*
HAS-50S	LEM1	LEM1	1
78907-A7	L1	L1	1
CAS120M12BM2	S1, S2	S1, D1	1
Gate Driver Board	U1	U1	1
Control Board	U2	U2	1
B32778G306K	C1	C1	2
B32778G0406K000	C2	C2	2
LA 10 250 24	M1	M1	1

The implemented device is given in Figure 3.5. Numbered items in the figure are elaborated respectively as 1: Gate Driver Board, 2: Control Board, 3: Output Capacitors (B32778G0406K000), 4: LEM Current Sensor (HAS-50S), 5: Fischer Heatsink (LA 10 250 24), 6: Magnetics Core (78907-A7), 7: Input Capacitors (B32778G306K), 8: Wolfspeed SiC Half-Bridge (CAS120M12BM2).

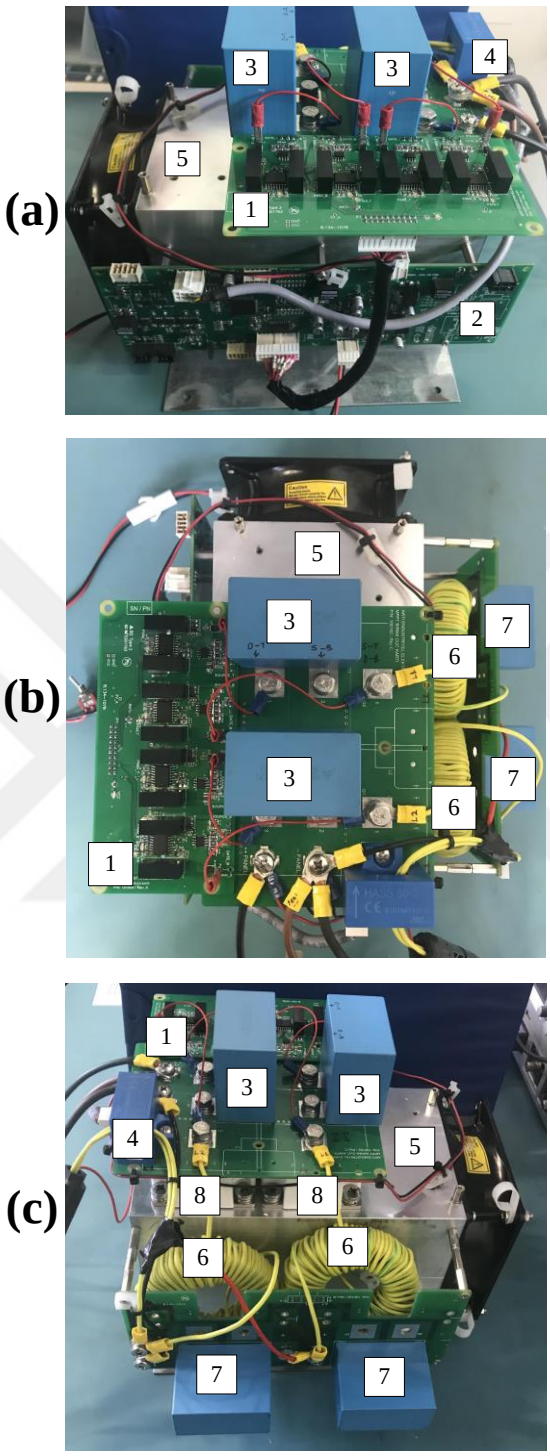


Figure 3.5. (a) Side-1 View (b) Top View (c) Side-2 View of the Boost Converter

3.1.1. Design Decisions and Parts Selection

Design was shaped by some constraints. For this design project, since the intention is to develop an MPPT converter for grid-connected photovoltaic systems, the output interface of it must be ultimately compatible with a grid-connectable photovoltaic inverter. For starters, it was chosen to be compatible with the All SiC Grid-Connected Three Phase Inverter designed in [18]. Therefore, the output voltage of the MPPT converter was decided to be 700 VDC.

Another constraint for the design was the testability. For the input supply, Magna-Power TSD800-24 High Power DC Power Supply was available with its Photovoltaic Power Profile Emulation Tool. CSUN255-60P photovoltaic panel was chosen to be emulated. Since the programmable supply and the emulator has its own current and voltage constraints for the panel data input, the panel configuration were decided accordingly to give the maximum power available by Magna-Power when emulating CSUN255-60P. Finally, 2 parallel strings of 19 series panels configuration was used, which enables 10.3 kW at MPP in 0º, 1000W/m^2 test conditions. The relevant datasheet section for the CSUN255-60P is given in Figure 3.6.

Electrical characteristics at Standard Test Conditions (STC)

Module	CSUN 255-60P	CSUN 250-60P	CSUN 245-60P	CSUN 240-60P	CSUN 235-60P
Maximum Power - Pmpp (W)	255	250	245	240	235
Positive power tolerance	0~3%	0~3%	0~3%	0~3%	0~3%
Open Circuit Voltage - Voc (V)	37.5	37.3	37.1	36.9	36.8
Short Circuit Current - Isc (A)	8.88	8.81	8.74	8.67	8.59
Maximum Power Voltage - Vmpp (V)	30.1	29.9	29.7	29.6	29.5
Maximum Power Current - Impp (A)	8.47	8.36	8.25	8.11	7.97
Module efficiency	15.70%	15.40%	15.09%	14.78%	14.47%

Electrical data relates to standard test conditions (STC) : irradiance 1000W /m² ; AM 1.5 ; cell temperature 25°C measuring uncertainty of power is within ±3%. Certified in accordance with IEC61215, IEC61730-1/2 and UL 1703

Electrical Characteristics at Normal Operating Cell Temperature (NOCT)

Module	CSUN 255-60P	CSUN 250-60P	CSUN 245-60P	CSUN 240-60P	CSUN 235-60P
Maximum Power - Pmpp (W)	188	185	181	178	175
Maximum Power Voltage - Vmpp (V)	28.0	27.9	27.5	27.2	27.0
Maximum Power Current - Impp (A)	6.72	6.64	6.58	6.54	6.48
Open Circuit Voltage - Voc (V)	34.6	34.5	34.2	34.0	33.8
Short Circuit Current - Isc (A)	7.16	7.10	7.02	6.95	6.90

Electrical data relates to normal operating cell temperature (NOCT): irradiance 800W /m²; wind speed 1 m/s ; cell temperature 45°C; ambient temperature 20°C measuring uncertainty of power is within ±3%.

Temperature Characteristics

Voltage Temperature Coefficient	-0.292%/K
Current Temperature Coefficient	+0.045%/K
Power Temperature Coefficient	-0.408%/K

Maximum Ratings

Maximum system voltage (V)	1000
Series fuse rating (A)	20
Reverse current overload (A)	27

Figure 3.6. CSUN255-60P Datasheet Parameters [9]

3.1.1.1. Common Parameters for the Design

For the worst case, the input current of the converter and maximum duty cycle the converter operates at, 60 °C cell temperature was selected for calculations. With increasing cell temperature, the output current of panels increases, therefore the highest operable cell temperature creates the worst realistic case in terms of losses and therefore selecting parts for the design. Also, the output voltage of the panels decreases with temperature, resulting in the converter operating at a higher duty cycle to meet the output voltage requirement of 700 VDC.

For 2 parallel strings of 19 series panels configuration, input current and voltage at MPP for 60 °C cell temperature is calculated as: $I_{MPP\_60C} = 17.20\ A$ and $V_{MPP\_60C} = 513.45\ A$ respectively. These values are calculated using the temperature coefficients given in the CSUN255-60P datasheet.

From the voltage at MPP for 60 °C, the maximum duty cycle is calculated as: $D_{max} = 0.27$.

Switching frequency is another common parameter that affects the design.

For this design, keeping in mind the core loss of the inductor and the switching loss of semiconductors, 20 kHz, switching frequency was chosen. A higher frequency allows the use of smaller inductors; however, the efficiency was the deciding factor for this project.

In Figure 3.7, loss distribution for the Two Phase Interleaved Boost Converter is given to demonstrate how the efficiency is affected by the choice of switching frequency of individual switches. The total of the switching losses increased from 36 W to 77 W (whilst the conduction losses remain unaffected and are approximately 23 W) and the total loss becomes approximately 100 W if the frequency is selected as 40 kHz. Efficiency is affected by nearly 0.3 %.

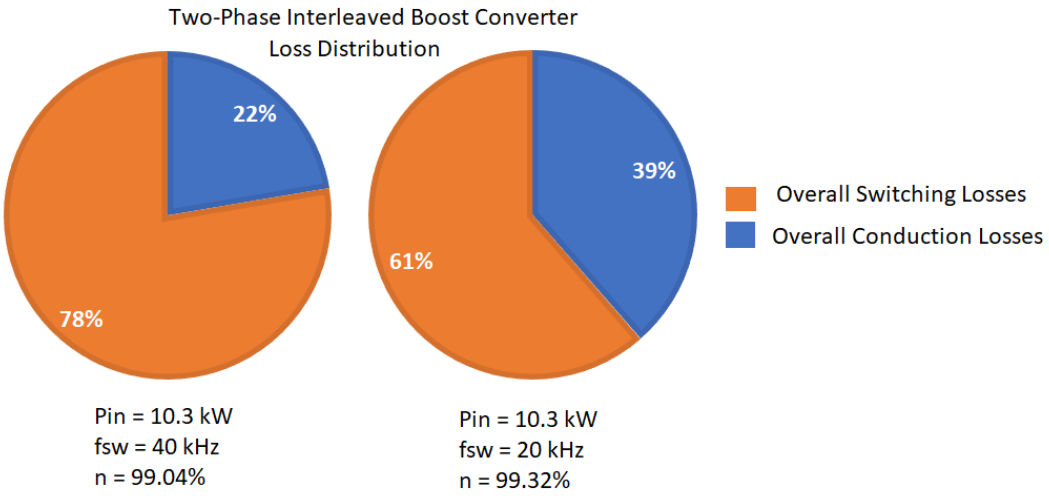


Figure 3.7. Loss Distribution of Two-Phase Interleaved Boost Converter at 20 kHz and 40 kHz at 10.3 kW Input Power

3.1.1.2. Input Capacitor Selection

The input capacitor is not essential for the boost converters operation; however, it is a good idea to filter out the high-frequency current ripple at the input.

It helps with two things. Firstly, in transformerless grid-connected PV systems, the high common-mode voltage ripple on the photovoltaic side can lead to dangerously high capacitive leakage currents from the photovoltaic panel, to the earth[19]. Secondly, due to the fact that photovoltaic panels are nonlinear sources, the current ripple effectively means a fluctuation in the operating point. An MPPT converter highly fluctuating close to MPP wastes valuable power and reduces overall system efficiency. [20]

The input capacitor in this application was sized to supply the ripple of the input current. Assuming a 40 m, 3.5 mm wire is used to carry the PV current to the converter, a wire self-inductance of 80 uH is estimated. The use of 60 uF capacitors was proven to be sufficient for this purpose with a simulation.

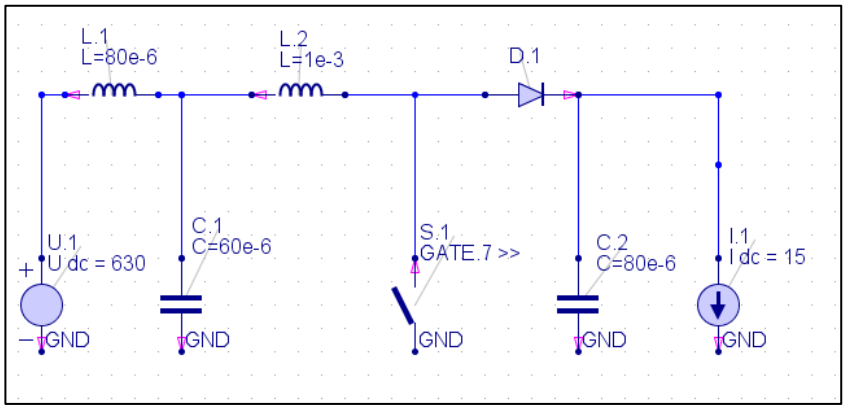


Figure 3.8. Simulation Circuit with Wire Inductance

From the waveforms generated by the simulation, it can be seen that the supply current is in DC form as desired, whilst all the ripple current drawn by the inductor is supplied from the input capacitor.

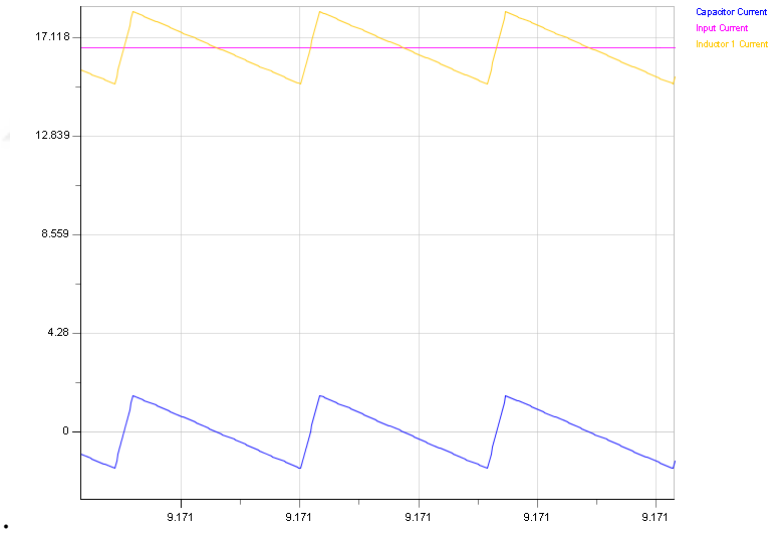


Figure 3.9. Conventional Boost Converter Input Current Waveforms Obtained with Power Electronics Simulator Y-Axis: (Pink) Input Current (A), (Blue) Capacitor Current (A), (Yellow) Inductor Current (A)

Two EPCOS B32778G306K 30 µF capacitors were used in parallel to achieve 60 µF of capacitance for all four configuration options of the boost converter.

3.1.1.3. Inductor Design

For the single-phase boost converter configuration, the worst-case inductor current is equal to the worst-case input current, and it is calculated as $I_{MPP_{60C}} = 17.20\ A$.

For the two-phase interleaved boost converter design, the worst-case inductor current is half of the worst-case input current, and it is calculated as $\mathrm{I_{L,max}} = 8.6\ A$.

It was decided that the converter should operate at continuous conduction mode for a wide power range. The boost converter inductor current waveform in CCM operation is given in Figure 3.10.

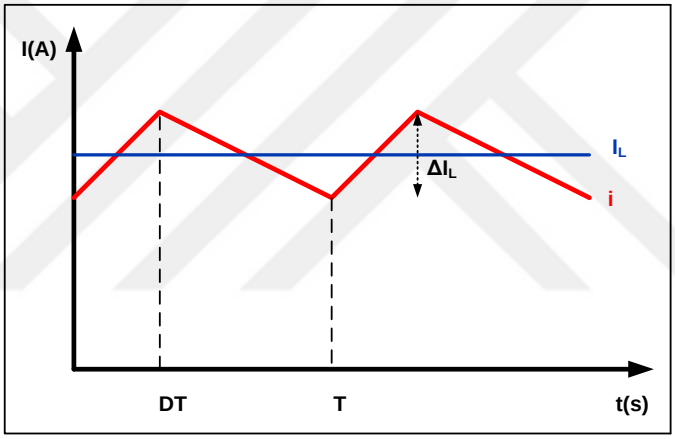


Figure 3.10. Boost Converter Inductor Current Waveform for CCM Operation

Accepted input current ripple was selected as 25% for two-phase boost converter topology: $\Delta I_{MPP\_60C} = 4.30\ A$.

It is well known that this percentage is higher for the single-phase configuration if the same inductance value is used. This is because the out of phase inductor current ripples partially cancel each other out in interleaved operation, depending on the value of the duty cycle.

For duty cycles smaller than 0.5, for two-phase interleaved topology, the inductance required is found by the below equation, where, L, is inductance, V_O is output voltage, f is the switching frequency:

$$L = \frac{V_O \times D \times (1 - 2D)}{\Delta I_{in} \times f}$$

Equation 3-1[17]

Making use of the maximum duty cycle value that is found earlier, and the calculated input ripple current value for the two-phase interleaved boost converter topology, the required inductance is found as $L = 1.013\ mH$.

Boost converter inductor current ripple can be found by utilizing the below equation, with the inductance value found for the inductor to be designed:

$$\Delta I_{\mathrm{L}} = \frac{V_{\mathrm{i}} \times D}{L \times f}$$

Equation 3-2

Equation yields the following ripple value for two-phase interleaved boost converter topology: $\Delta I_{L,max} = 6.76\ A$.

To produce the inductor to be used in the application, a core from Magnetics Inc. powdered alloy core collection was selected. The XFlux sub-series of powdered alloy cores was decided to be suitable for the design. The XFlux material choice is one of the two most suitable materials from Magnetics for high flux capacity, the other being the High Flux material.

For selecting a core, once the core material is chosen, only two parameters are essential. Those parameters are the minimum inductance required under worst-case DC bias condition, and the maximum DC current the inductor will be subjected to. From those parameters, LI^2 value is computed (which is double the energy stored in the inductor) and using this indicator, from core selector charts given by Magnetics, a core can be selected. Following the procedure outlined in [21], the core was selected as 78907-A7. The relevant core specifications are given in Table 3.4.

Table 3.4. *Xflux 78907-A7 Core Properties*

Core Properties	*Value*
Permeability	60 μ
Inductance Factor, A_L	$78.20\ \mathrm{nH/T^2}$
Path Length, I_e	196 mm
Cross Section, A_e	$221\ \mathrm{mm^2}$
Volume	$43400\ \mathrm{mm^3}$

The inductance factor, A_L, for the core is obtained for the core part number selected from the specific core datasheet. As suggested in [21], the worst-case negative tolerance of -8% is considered for computing minimum A_L. At this stage, the number of turns required to generate the required inductance is computed for zero DC bias condition with the help of Equation 3-3, later on, the DC bias is also considered and the number turns determined is iterated.

$$N = \sqrt{\frac{L}{\mathrm{A}_L}}$$

Equation 3-3

For zero DC bias condition, the required number of turns is 114.

To obtain the number of turns required at full load, the DC bias is calculated in terms of magnetizing force. From DC bias vs. permeability curves given in [21], the roll-off in per unit of initial permeability for the calculated bias level is determined. Utilizing this value, the number of turns is updated as 123. With 123 turns, at no-load conditions the inductance will be 1.18 mH and at full load DC bias level, the inductance will be 1.08 mH. Since the full load inductance value is close enough to the previously obtained required inductance, the updated number of turns is acceptable to proceed with the production of the inductor.

3.1.1.4. MOSFET and Diode Selection

In terms of power losses, the boost converter diode (or synchronous rectifying MOSFET, depending on the configuration selected) and boost converter switch selection is important. A slow type diode with its excessive reverse recovery time introduces a significant switching-on loss on boost converter switch and switching-off loss on itself. If turn-on and turn-off time of the boost converter switch is high, it also results in a massive power loss. Forward conduction voltage of the diode and the boost converter switch is also another important factor to consider in terms of efficiency.

When the boost converter switch is “on”, the diode (or the synchronous rectifying MOSFET) is “off”, and the blocking voltage is the output voltage of the converter. When the boost converter switch is “off”, the current waveform of the diode (or the synchronous rectifying MOSFET) is in the shape as seen as in Figure 3.11 and the peak current the diode is subjected to is the same as the peak current of the inductor.

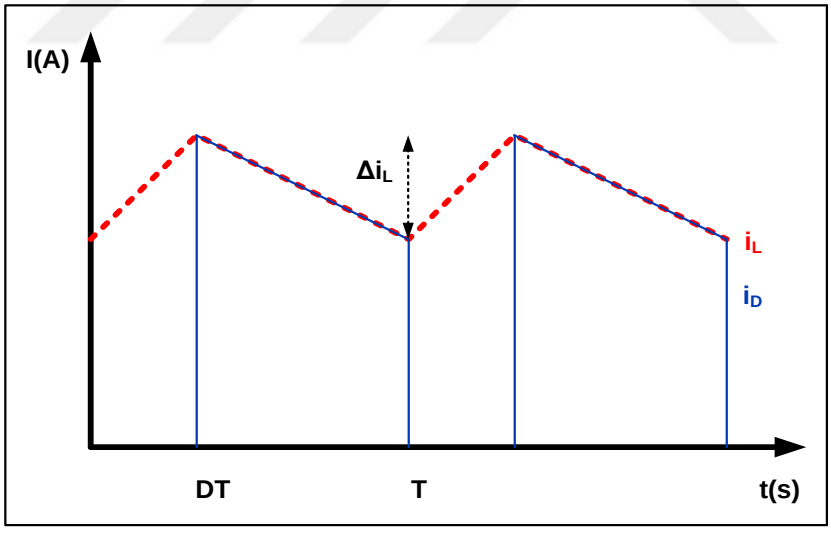


Figure 3.11. Boost Converter Diode (or Synchronous Rectifying MOSFET) Current Waveform

The Mean value of the current passing through the device can be found with the below equation.

$$I_D = I_L \times (1 - D)$$

Equation 3-4

When choosing a part number, the voltage and current ratings of the diode (or the synchronous rectifying MOSFET) must be more than the output voltage of the converter and the mean value of the current passing through it respectively, with a safety margin added. The safety margin ensures the device does not get damaged by transients.

When the diode (or the synchronous rectifying MOSFET) is "on", the boost converter switch is "off", and the blocking voltage is the output voltage of the converter. When the boost converter switch is "on", the current waveform of the switch is in the form as seen as in Figure 3.12 and the peak current the switch it is subjected to is the same as the peak current of the inductor.

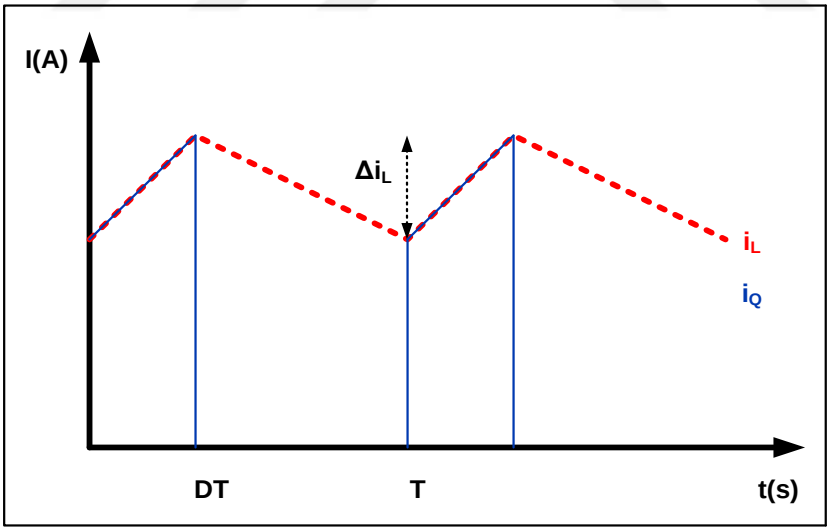


Figure 3.12. Boost Converter Switch Current Waveform

The mean value of the current passing through the device can be found with the below equation.

$$I_D = I_L \times D$$

Equation 3-5

When choosing a part number, the voltage and current ratings of the boost converter switch must be more than the output voltage of the converter and the mean value of the current passing through it respectively, with a safety margin added.

3.1.1.5. Control Board and Gate Driver Board

Gate driver board given in Figure 3.13 is based on the Isolated Gate Driver application note supplied by the Wolfspeed for SiC MOSFETs[22]. The board was designed by "Artı Endüstriyel Elektronik A.Ş." for TEYDEB 1511 Photovoltaic System Project for All SiC HF-Link MPPT Converter, that was carried out with the joint collaboration of Hacettepe University and Middle East Technical University.

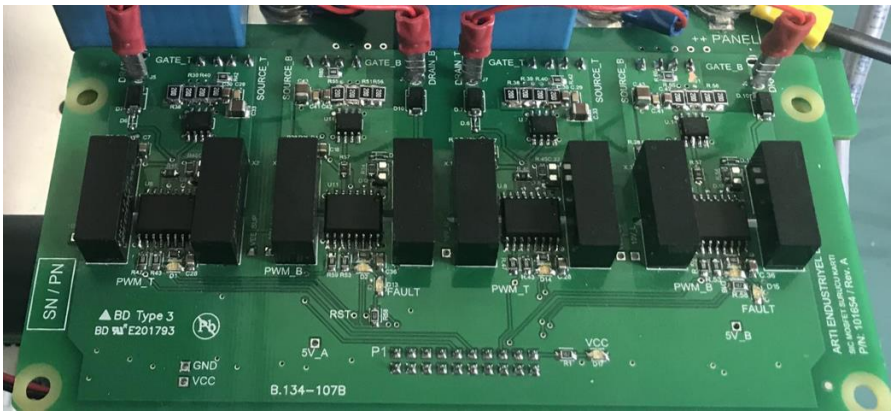


Figure 3.13. Gate Driver Board Top-Side

Gate driver board has four isolated and independent channels to drive four SiC MOSFETs. It was designed especially for CAS120MBM12 as a plug and play type driver as seen in Figure 3.14, to keep any parasitic circuit components to a minimum.

For this project, the gate resistance is chosen as 2.5 Ω to keep the switching losses at a minimum.

For each channel, the circuit consists of two isolated DC-DC converters and the gate driver integrated circuit. The integrated circuit, by IXYS IXDN609SI can provide 35V output swing and up to 9A of current with a typical output resistance of 0.8 Ω. Power is provided by isolated DC-DC converters. One of the converters is for the positive bias and the other one is for negative bias. In addition to the circuit described in the application note, Infineon 1ED020I12-B2 driver is used to drive the PWM signal, and collect reference from the MOSFET drain terminals for desaturation detection and protection.

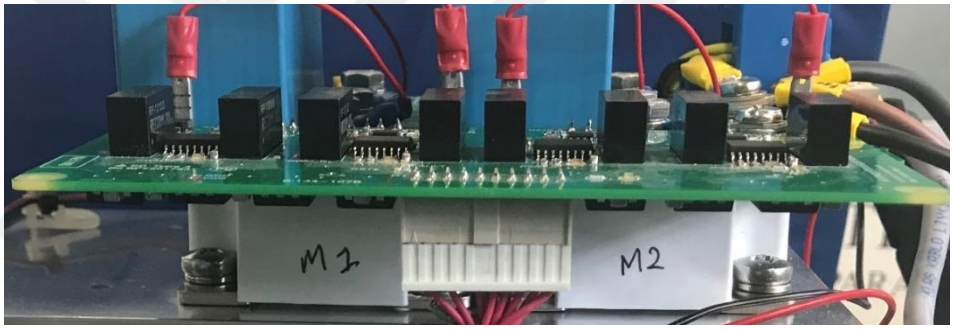


Figure 3.14. Gate Driver Board as Plugged-In to the MOSFETs

The control board is a board designed previously for the same project mentioned as the Gate Driver Board. It is a generic board that has resources for digital control of power circuits; such as Texas Instruments TMS320F28069UPZ DSP, two current sensor inputs that are conditioned and fed to DSP's ADC, two high voltage acquisition inputs that are isolated from controllers ground reference and each other, isolated JTAG interface for debugging, RS485 ICs for UART communication, optional Flyback converter for supplying the board from a high voltage source and six PWM outputs.

For this design project, a single current sensor input is connected to the LEM HAS-50S sensor, for the MPPT algorithm's PV current input. Two of the isolated high voltage acquisition inputs are used to acquire PV voltage input and the converter's output voltage. PV voltage input is used in MPPT control and the converter's output voltage is used as feedback for over-voltage protection. If the output voltage is more than the threshold value set by the DSP, the PWM outputs are latched to low-level to prevent MOSFETs from being in the conducting state.

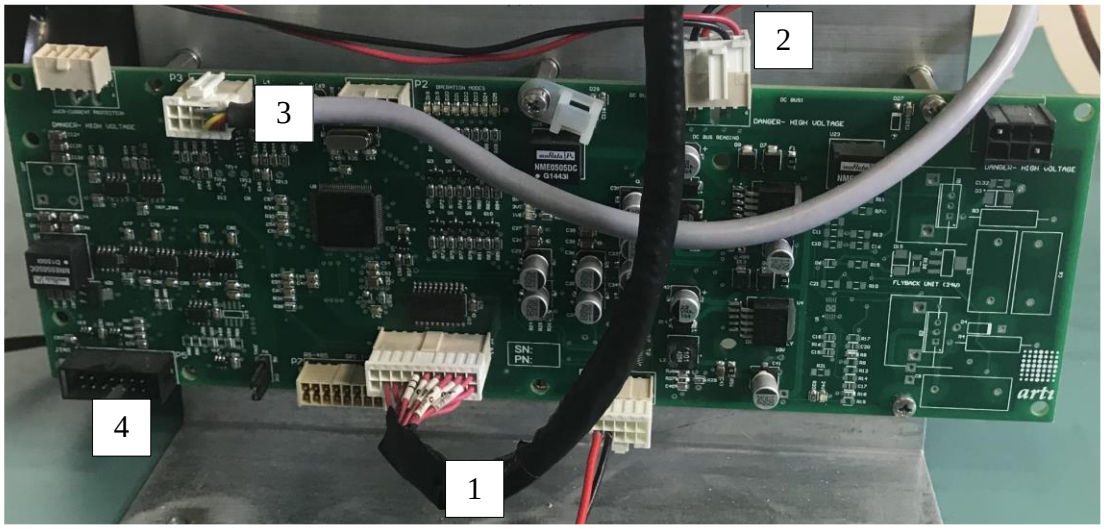


Figure 3.15. View of Control Board with the Necessary Connections

Control Board used is given in Figure 3.15. Numbered items in the figure are elaborated respectively as 1: PWM Signal Carrying Shielded Cable, 2: Two High Voltage Inputs Connection Cable, 3: LEM HAS-50S Current Sensor Input, 4: Isolated JTAG Connector.

3.1.1.6. Control Software Design

Control Scenario:

At the beginning of the code, DSP's enhanced PWM, EPWM, module is initialized for the PWM generation of the control loop. The time-base counter of the EPWM module is configured to run in count-up-and-down mode, with a frequency of 20 kHz which is the switching frequency. When the time-base counter reaches the software specified "Event A" value (depicted in figures as "CA") during count-up, the module is programmed to set the specified PWM pin to "high" level. During count-down, time-base counter reaching "Event A" value once again, sets the specified PWM pin to "low" level. The time-base counter rolling down to value "0" initiates "The Start of Conversion" of ADC. ADC is used to convert the input voltage and current from the PV string for MPPT control and output voltage for over-voltage protection. "End of Conversion" on the other hand, generates ADC interrupt, where the samples are accumulated at 20 kHz frequency. 100 samples are taken to calculate the normalized mean values of input voltage and current, and; MPPT algorithm is run at 100 ms. If the mean output voltage of the converter reaches above 800 VDC, over-voltage protection is activated by the Trip-Zone submodule, to stop the PWM generation immediately, and set PWM pins to the safe "low" level.

Figure 3.16 summarizes the control scenario.

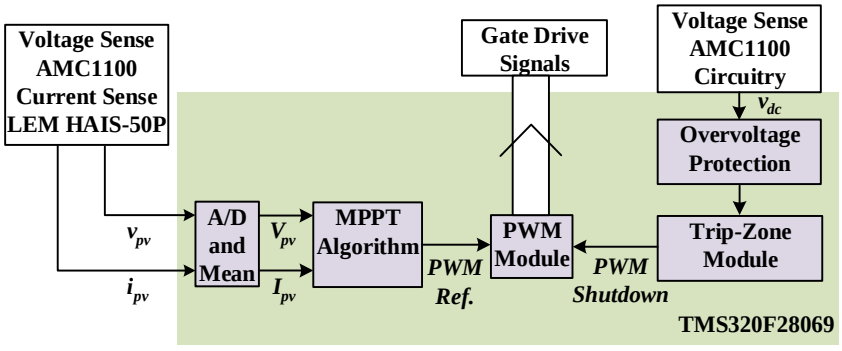


Figure 3.16. Main Control Block

PWM Generation:

The software was implemented to have four options of PWM generation for Boost converter configuration options explained in the beginning of the chapter. Duty cycle input to the PWM generation directly comes from the MPPT control algorithm.

From Figure 3.17 to Figure 3.20, example PWM signal waveforms are given for all the four boost converter configuration options. In all the figures, the TMS320F28069 DSP EPWM module's timer value counter status is represented with a triangular waveform. EPWM timer was chosen to count in up-down mode, hence the triangular waveform is symmetrical. The frequency of the waveform is the same as the switching frequency of the device. When the timer value reaches a "Compare-A" value (depicted in figures as CA), an event is triggered, and a chosen PWM signal changes it states to comply with the duty cycle (or Compare-A value) that is decided by the MPPT control algorithm.

For Synchronous Boost Converter options, EPWM module PWM signal pairs were used, e.g. EPWM1A and EPWM1B of the TMS320F28069 DSP. As the MOSFET that replaces the Boost Converter diode, needs to be "on" when the inductor charging MOSFET is turned "off", and vice versa, Dead-band generator submodule was utilized; so that the two MOSFET's were never turned on at the same time. Signal pairs were programmed as "Active High Complementary", meaning EPWM1B was inverted from EPWM1A with rising and falling edge dead-band delays (depicted in figures as RED and FED). Although the MOSFET turn-off and turn-on times are much shorter for full-load condition, for very light loads, it can delay up to 1.5 µs as experienced empirically; therefore, a dead-band time of 2 µs was used.

For Two-Phase Interleaved Boost Converter options, the interleaving is done by turning on the inductor charging MOSFETs with a 180º phase difference with respect to one another; therefore, PWM module was programmed for this purpose via Time-Base Phase Registers.

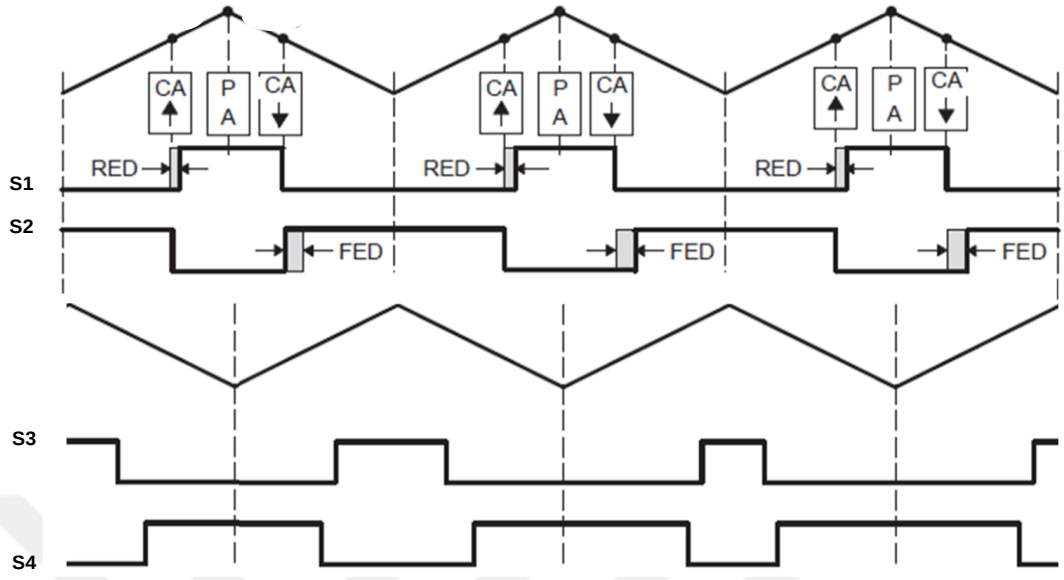


Figure 3.17. Two-Phase Interleaved Synchronous Boost Converter PWM Signal Generation Example

In Figure 3.17, signals for S1 and S2 are a PWM signal pair (eg. EPWM1A and EPW1B) and S3 and S4 are a PWM signal pair (eg. EPWM2A and EPWM2B). As explained earlier, the signal pairs are programmed as “Active High Complementary”. The signal for S1 and S3 is programmed to be 180º out of phase with respect to each other. Since the signal of S2 is generated with respect to the signal of S1, and the signal of S4 is generated with respect to signal of S3, the signals of S2 and S4 automatically become 180º out of phase with respect to each other.

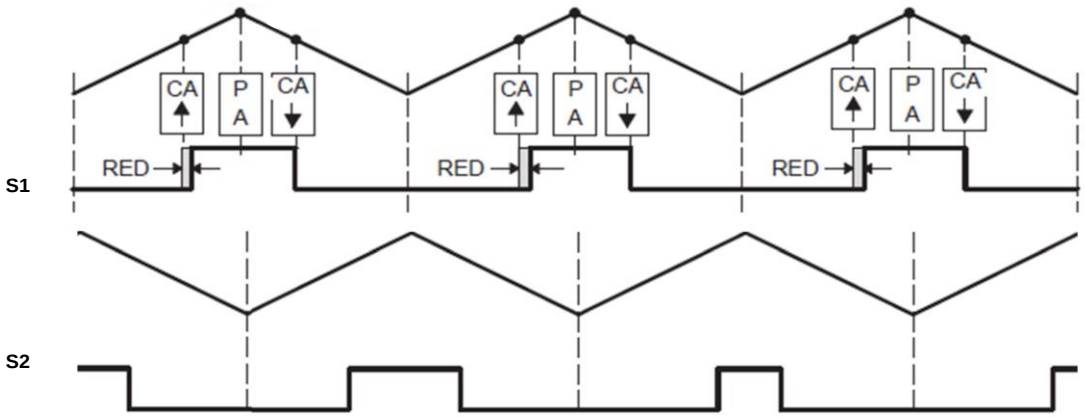


Figure 3.18. Two-Phase Interleaved Boost Converter PWM Signal Generation Example

In Figure 3.18, the signal for S1 and S2 is programmed to be 180º out of phase with respect to each other.

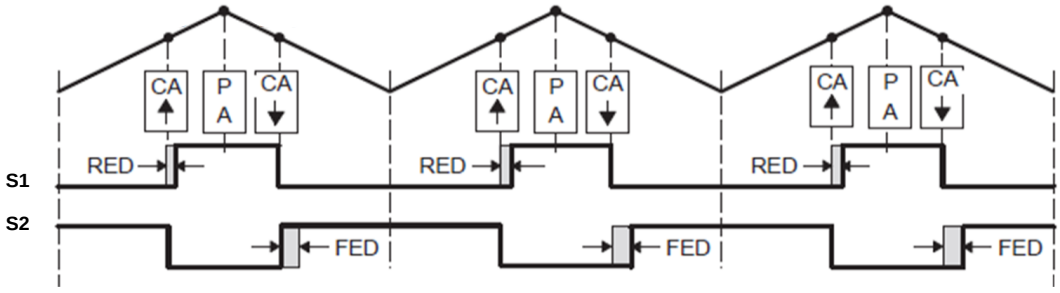


Figure 3.19. Synchronous Boost Converter PWM Signal Generation Example

In Figure 3.19, signals for S1 and S2 are a PWM signal pair (eg. EPWM1A and EPW1B) and the signal pair is programmed as “Active High Complementary”.

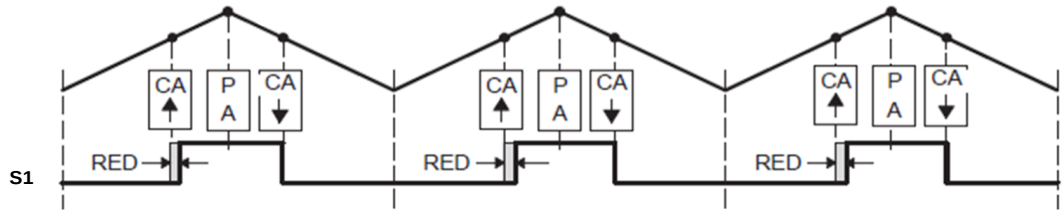


Figure 3.20. Conventional Boost Converter PWM Signal Generation Example

In Figure 3.20, the signal for S1 is seen.

MPPT Algorithm:

As MPPT Control Algorithm, the well-known Perturb and Observe Algorithm [8] was chosen; as it is easy to implement; and it can find MPP with high accuracy as long as the step size for the duty cycle is not very high. The disadvantage of this method is seen in partial-shading conditions of the PV panels; where more than one MPP-like points arise in the characteristic curve, and; it becomes less trivial to locate the correct MPP. For those conditions, the sweeping method can be employed where the array characteristic is swiped by changing the duty cycle over a larger range gradually with a fixed period. That way, because all the MPP-like points are detected by swiping, the actual MPP can be decided.

The flow-chart of the algorithm itself is given in Figure 3.21. The Perturb and Observe algorithm, increments and decrements the current drawn from the panel to observe the change in power. First, a perturbation is applied in one direction and power is observed, if the power increases, the same direction is chosen for the next perturbation. If power decreases the perturbation is applied in the other direction this time. When MPP is located by the algorithm, the system starts oscillating near the MPP. The oscillation can be minimized for accuracy by keeping the step size as low as possible. However, this means an increase in time for detecting the MPP, and it can be too slow for changing lighting conditions.

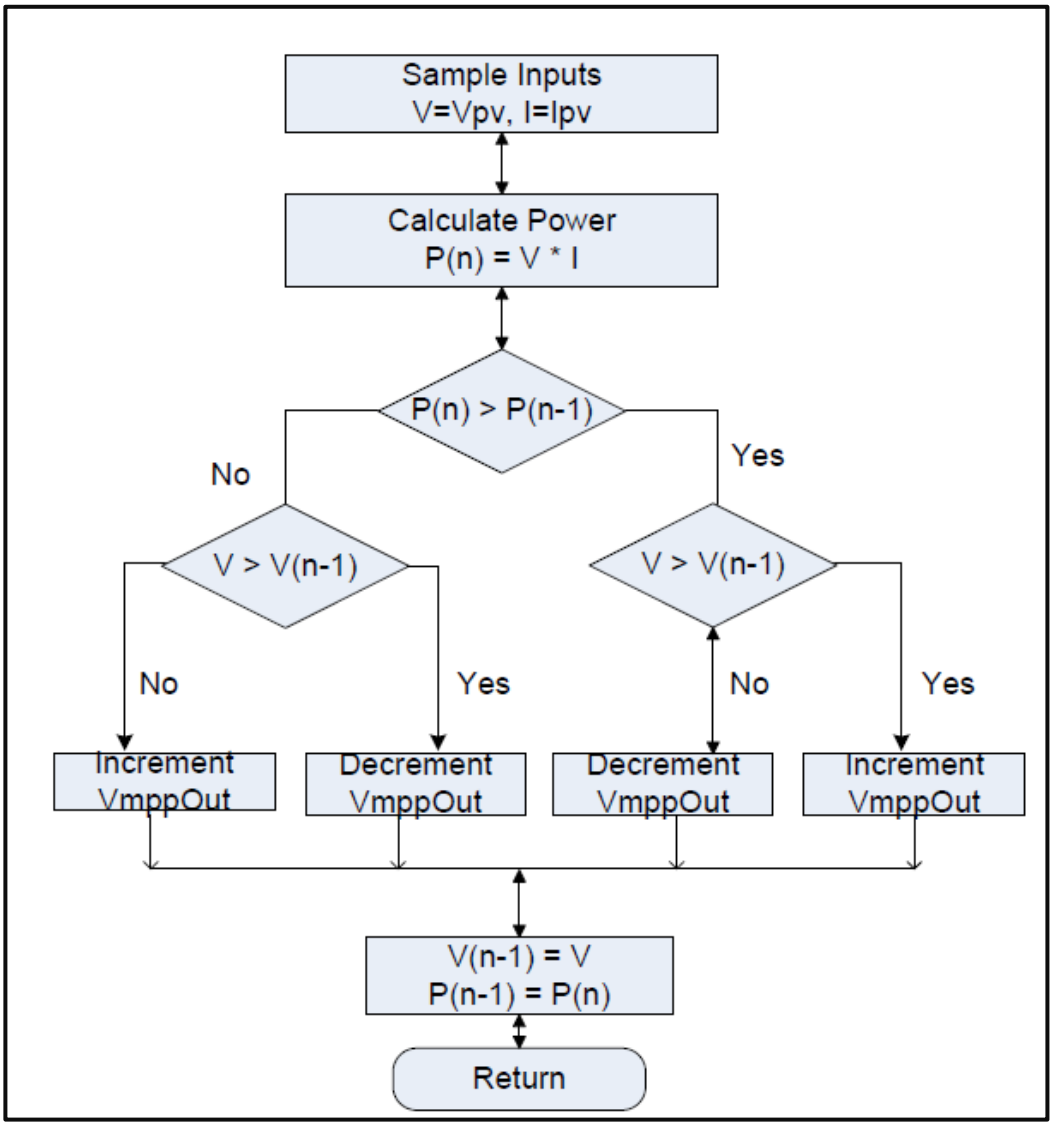


Figure 3.21. Perturb and Observe Algorithm [8]

3.1.2. Theoretical Efficiency

For all four Boost Converter configuration options, the following loss components are calculated to determine the theoretical overall efficiency for photovoltaic input power ranging from 3 kW to 10 kW:

- Inductor Copper Loss
- Inductor Core Loss
- Semiconductor Conduction Losses
- Semiconductor Switching Losses

In addition to those loss components listed, the power consumption of the heatsink fan, and the control and gate driver boards are measured and added as loss components when calculating overall efficiency.

As the intention is operating the converter at MPP the majority of the time, and keeping the MPP finding period as short as possible, the loss calculations are based on operation at different MPPs ranging from 3kW to 10kW. The chosen MPPs are based on the 2 parallel strings of 19 series panels configuration of CSUN225-60P exposed to different insolation levels at 0 ºC panel temperature. In Table 3.5 the operating points are summarized.

Table 3.5. *Operating Points for Loss Calculations*

Maximum Power Point [kW]	*Insolation [W/m^2]*
3.28	325
5.67	550
8.54	825
10.33	1000

For Inductor Copper and Core Loss, “Inductor Design Tool” spreadsheet supplied by Magnetics Inc. is made use of. The methodology of the design tool loss calculations is given in [21] Section 2 “Core Selection”.

For semiconductor conduction and switching losses, relevant graphs supplied in CAS120M12BM2 datasheet [23] is made use of for manual calculations. The results are then cross-checked with CREE's SpeedFit Design Simulator specifically for CAS120M12BM12 SiC MOSFET; although this could not be done for all the configurations as the SpeedFit Design Simulator is limited to conventional boost converter topology. As a result, the efficiency vs. power pattern given in Figure 3.22 is produced and summarized in Table 3.6.

To summarize all the data before further elaboration, a simple explanation for each table given in this section is presented below.

- In Table 3.7, inductor losses (core loss and copper loss combined) are given for all four boost converter configurations at different power levels.
- In Table 3.8, inductor losses are detailed in terms of copper and core losses once again for all four boost converter configurations at different power levels.
- In Table 3.9, conduction losses (the copper loss of the inductor, and the conduction loss of the semiconductors) are given for all power stages at increasing power levels.
- In Table 3.10, switching losses (the core loss of the inductor and turning "on/off" losses of the semiconductors) are given for all boost converter options at increasing power levels.

Further analysis shows consistency with what is normally seen with these converters in terms of decreasing efficiency with power. It should also be noted that, at these high values for efficiency, it is hard to measure efficiency accurately with measurement tools, due to error ratings of standard equipment. Therefore; it is beneficial to previously calculate and elaborate on these findings.

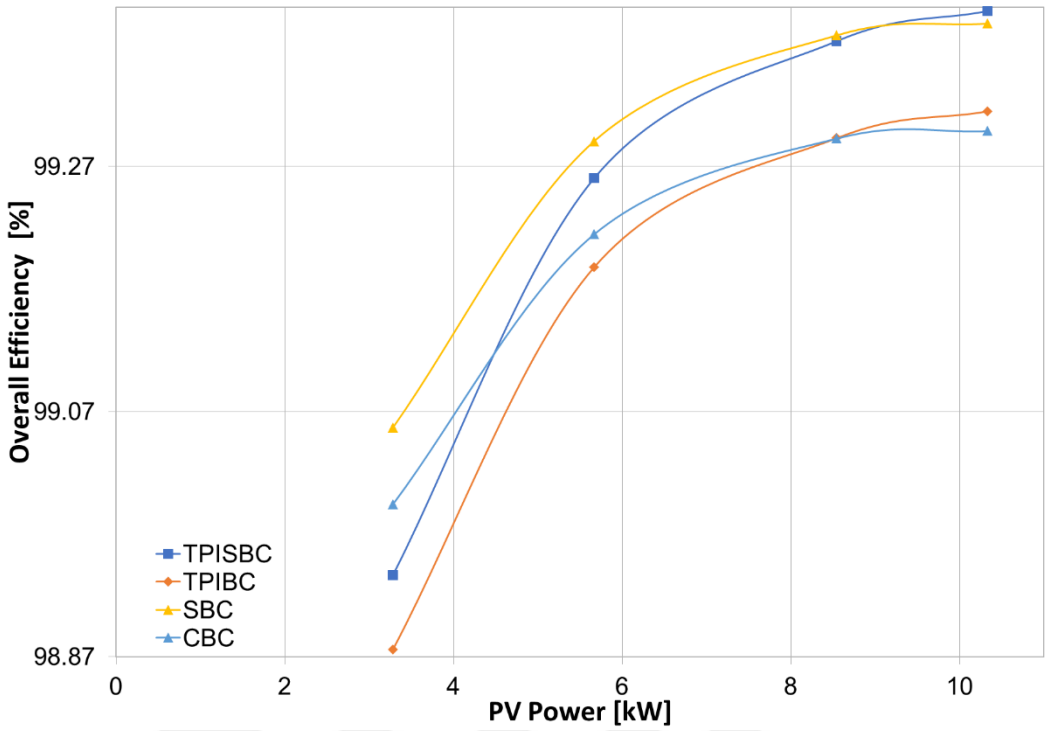


Figure 3.22. Effect of Operating Power on Overall Efficiency for Four Configuration Options: Two-Phase Interleaved Synchronous Boost Converter (TPISBC), Two-Phase Interleaved Boost Converter (TPIBC), Synchronous Boost Converter (SBC) and Conventional Boost Converter (CBC)

Table 3.6. Effect of Operating Power on Overall Efficiency for Four Configuration Options: Two-Phase Interleaved Synchronous Boost Converter (TPISBC), Two-Phase Interleaved Boost Converter (TPIBC), Synchronous Boost Converter (SBC) and Conventional Boost Converter (CBC)

Power [kW]	*Efficiency [%] TPISBC*	*Efficiency [%] TPIBC*	*Efficiency [%] SBC*	*Efficiency [%] CBC*
3.28	98.94	98.88	99.06	98.99
5.67	99.26	99.19	99.29	99.21
8.54	99.37	99.29	99.38	99.29
10.33	99.40	99.32	99.39	99.30

As expected, the efficiency is greater at higher powers. This is due to the fact that, even though the conduction losses significantly increase with power, the switching losses which are significant, slightly increases for this design.

To explain this power and efficiency relationship further, the following points are highlighted:

- Switching losses (the core loss of the inductor and turning “on/off” losses of the semiconductors) makes up most of the loss when compared with the conduction losses (the copper loss of the inductor, and the conduction loss of the semiconductors), with the exception of SBC configuration operating at high power due to its less number of switches. This can be seen in Table 3.9 and Table 3.10.
- The conduction loss in the boost converter low side switch and high side switch (diode or MOSFET depending on the configuration) both increase with power, as both the mean current passing through them, and the “on” voltage increases.
- The switching loss for the high side switch is negligible. For configurations with diode, because it is SiC, the switching loss is zero. For high-side MOSFET, at the turn-on instant the SiC body diode of it turns-on before it is made “on” (due to dead-band). Also, at turn-off of the high-side MOSFET, before the lower MOSFET is made “on” (due to deadband), once again the body diode of the high-side MOSFET takes on the current. Therefore with the help of the high-side body diode, the high-side MOSFET is switched with almost-zero losses, as the voltage across the diode is very close to zero, it can be considered as zero-voltage switching. However, the switching loss of the low side switch slightly increases with power, as this loss component not only depends on the “on” voltage (which is the same for all powers, as the DC link is kept constant) but also on the “on” current which increases with power.
- Inductor copper losses increase with power; however, the larger portion of the power is lost in the core of the inductor, and the core losses become more severe at lower powers. This can be seen in Table 3.7 and Table 3.8.

To compare interleaved configurations with the non-interleaved options, the following points are presented.

- Because the average current through each semiconductor halves in two-phase interleaved options when compared with the non-interleaved converter configurations, individual switching losses of each switch slightly decreases (but does not become half); therefore, due to the number of switches doubling, the overall switching losses are more in two-phase power stages.
- When the conduction losses of TPISBC is compared with SBC, each conduction loss component is halved (as the resistances are halved); therefore, overall conduction losses are less than half of SBC.
- When the conduction losses of TPIBC is compared with CBC, each conduction loss component is halved, except for the component arising from conduction of diodes (due to diode threshold voltage); therefore, overall conduction losses are less than CBC but not halved.
- When interleaved converter options are compared with non-interleaved converter options in high powers, conduction losses in TPISBC and TPIBC being less than SBC and CBC compensates for switching losses being more than SBC and CBC; however for lower powers because the switching losses are more dominant, conduction losses don't compensate anymore. Therefore, whilst at high powers efficiency of TPISBC is greater than the SBC and efficiency of TPIBC is greater than CBC, at low powers it is the opposite.

To compare synchronous options with non-synchronous options, the following points are made:

- The efficiency gain from synchronous rectification is due to approximately 10 W of less loss at 10.3 kW power; however, this amount decreases at lower powers; therefore, efficiencies of TPISBC and TBIBC gets closer with respect to each other. The same applies to SBC and CBC. This can easily be observed from the curves given in Figure 3.22.
- As seen in Figure 3.22 TPISBC and CBC efficiency curves intersect even though the conduction losses are less for TPISBC. This is due to the total

switching losses of TPISBC being more than the total switching losses of CBC and the switching losses dominating.

Table 3.7. *Power vs. Inductor Loss: Two-Phase Interleaved Synchronous Boost Converter (TPISBC), Two-Phase Interleaved Boost Converter (TPIBC), Synchronous Boost Converter (SBC) and Conventional Boost Converter (CBC)*

Power [kW]	*Inductor Loss [W] TPISBC & TPIBC*	*Inductor Loss [W] SBC & CBC*
3.28	12.7	7.6
5.67	11.54	8.63
8.54	13.36	13.73
10.33	15.66	18.68

Table 3.8. *Power vs. Inductor* Copper and Core *Loss: Two-Phase Interleaved Synchronous Boost Converter (TPISBC), Two-Phase Interleaved Boost Converter (TPIBC), Synchronous Boost Converter (SBC) and Conventional Boost Converter (CBC)*

Power [kW]	*Inductor Core Loss [W] TPISBC & TPIBC*	*Inductor Copper Loss [W] TPISBC & TPIBC*	*Inductor Core Loss [W] SBC & CBC*	*Inductor Copper Loss [W] SBC & CBC*
3.28	11.58	1.12	5.71	1.89
5.67	8.82	2.72	3.48	5.15
8.54	7.44	5.92	2.25	11.48
10.33	7.1	8.56	1.84	16.84

Table 3.9. *Power vs. Conduction Loss for Four Configuration Options: Two-Phase Interleaved Synchronous Boost Converter (TPISBC), Two-Phase Interleaved Boost Converter (TPIBC), Synchronous Boost Converter (SBC) and Conventional Boost Converter (CBC)*

Power [kW]	*Conduction Loss [W] TPISBC*	*Conduction Loss [W] TPIBC*	*Conduction Loss [W] SBC*	*Conduction Loss [W] CBC*
3.28	1.30	5.06	2.25	6.07
5.67	3.26	9.83	6.23	12.98
8.54	7.13	17.17	13.91	24.36
10.33	10.33	22.57	20.39	33.22

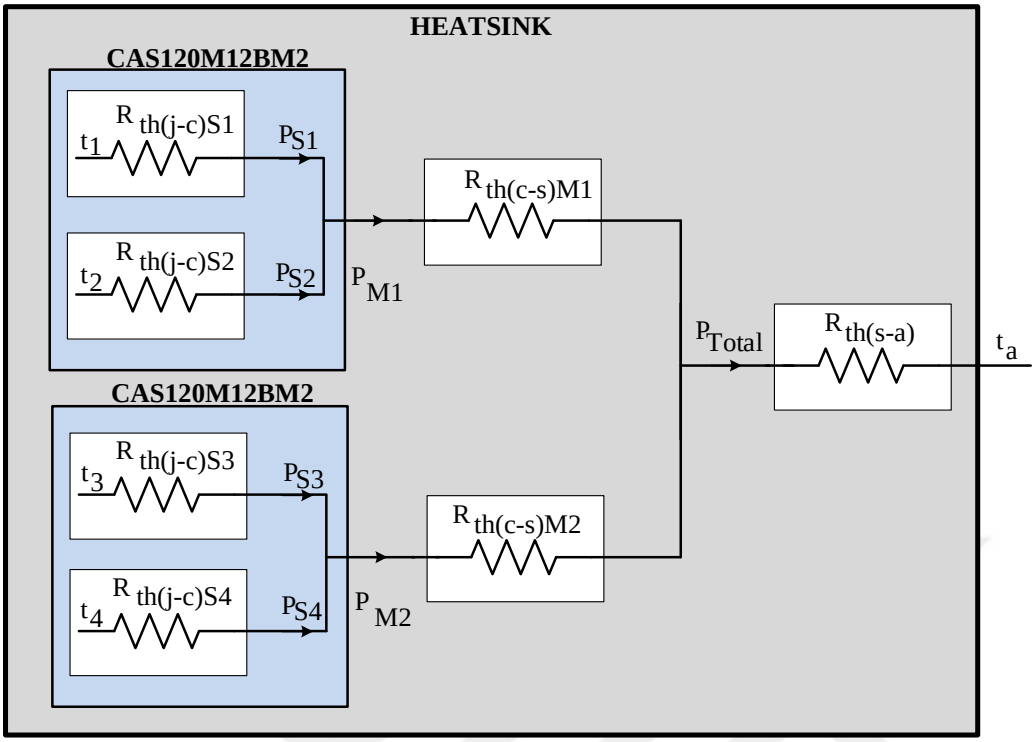
Table 3.10. *Power vs. Switching Loss: Two-Phase Interleaved Synchronous Boost Converter (TPISBC), Two-Phase Interleaved Boost Converter (TPIBC), Synchronous Boost Converter (SBC) and Conventional Boost Converter (CBC)*

Power [kW]	*Switching Loss [W] TPISBC*	*Switching Loss [W] TPIBC*	*Switching Loss [W] SBC*	*Switching Loss [W] CBC*
3.28	20.50	19.56	15.60	14.66
5.67	25.56	23.94	20.89	19.27
8.54	33.40	30.96	26.23	23.79
10.33	38.87	35.92	29.89	26.94

3.1.3. Thermal Design

In Figure 3.23, a simple thermal model of the implemented device is given.

When the LA 10 250 24 heatsink is used, which has a thermal resistance of 0.06 K/W, according to this thermal model, the maximum temperature difference between the junction of one switch and the ambient is 10ºC, excluding the temperature rise arising from case to sink thermal resistance. This maximum value is obtained for TPIBC configuration.



POWER DISSIPATIONS

P_{S1} : power dissipation on switch 1
P_{S2} : power dissipation on switch 2
P_{S3} : power dissipation on switch 3
P_{S4} : power dissipation on switch 4
P_{M1} : total power dissipation on module 1
P_{M2} : total power dissipation on module 2
P_{Total} : total power dissipation on heatsink

TEMPERATURE OF VARIOUS POINTS

t_a : ambient temperature
t_1 : junction temperature of switch 1
t_2 : junction temperature of switch 2
t_3 : junction temperature of switch 3
t_4 : junction temperature of switch 4

THERMAL RESISTANCES

$R_{th(j-c)S1}$: junction to case constant of switch 1
$R_{th(j-c)S2}$: junction to case constant of switch 2
$R_{th(j-c)S3}$: junction to case constant of switch 3
$R_{th(j-c)S4}$: junction to case constant of switch 4
$R_{th(c-s)M1}$: case to sink constant of module 1
$R_{th(c-s)M2}$: case to sink constant of module 2
$R_{th(s-a)}$: sink to ambient constant

Figure 3.23. Thermal Model of the Implemented Device

3.1.4. Discussion on Synchronous Rectification

Thanks to MOSFET's reverse-current-conducting capability, in boost converters, the diode can be replaced with a MOSFET (unlike an IGBT). Theoretically, synchronous rectification is proved to be beneficial for boost converters in section 3.1.2. In operations discussed in section 3.1.2, when synchronous rectification occurs, both the turn-on and off losses are negligible for the high-side MOSFET. This is because, at the turn-on instant the SiC body diode of the MOSFET turns-on before it is made "on" (due to dead-band). Also, at turn-off of the high-side MOSFET, before the lower MOSFET is made "on" (due to deadband), once again the body diode of the high-side MOSFET takes on the current. Therefore, with the help of the high-side body diode, the high-side MOSFET is switched with almost-zero losses, as the voltage across the diode is very close to zero, it can be considered as zero-voltage switching. The benefit of synchronous rectification, in this case, is due to conduction loss decreasing that is due to enabling the MOSFET, which has a very low drain-to-source resistance.

However, there is even a better operation scenario that occurs at even higher powers. That is when the MOSFET and the body diode is conducting at the same time, sharing the current in accordance with their conducting resistance. This operation occurs when the current through the MOSFET is high and therefore the voltage drop across the MOSFET is equal or larger than body diodes forward conducting threshold. This phenomenon was not possible to demonstrate in this thesis experimentally, as the power required for this is beyond the rating of the power supply used in this thesis work.

This phenomenon is illustrated with a simulation run in Powersim software for SBC configuration, for the hypothetical case of the power converter (with the semiconductors modeled as CAS120M12BM2) running at 46.5 kW input power (MPP Power of 19 series, 9 parallel strings of CSUN panels at 1000W/m^2 0ºC condition).

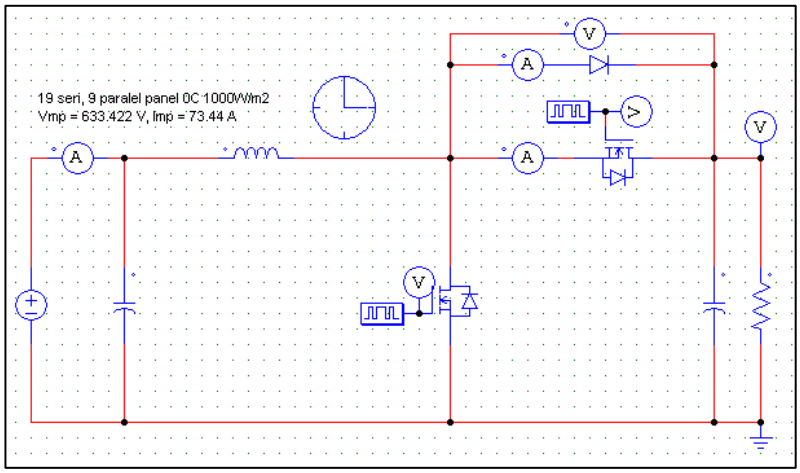


Figure 3.24. Simulated Circuit

The simulated circuit is given in Figure 3.24. Note that to be able to read the current of the diode, the body diode of the upper MOSFET is given a very high on-resistance to disable it (as it is impossible to connect a current measurement block to it), and instead an external diode is added to simulate the body diode which is connectable to a current measurement block.

The resultant current waveforms are presented in Figure 3.25. As can be seen, the current is shared among the upper MOSFET and its body diode.

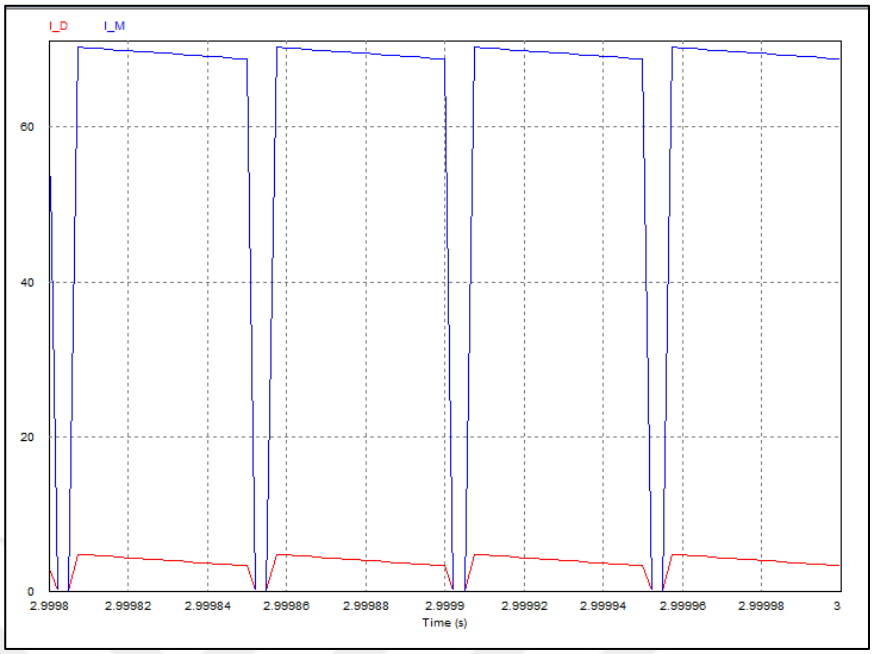


Figure 3.25 Current Through Synchronous Boost Converter Upper MOSFET and Body Diode Obtained with Power Electronics Simulator: MOSFET Current in Blue (A), Diode Current in Red (A)

To illustrate benefits further, theoretical loss calculations are carried out for three hypothetical cases for single-phase boost converter in two different power levels. In the first case (case A), instead of synchronous rectification with the MOSFET, the diode is used. In the second case (case B), upper MOSFET is used for synchronous rectification but the body diode is disabled (removed from the circuit by making its threshold very high, so it does not share the current with the MOSFET) to demonstrate how this affects the losses. In the third case (case C), upper MOSFET and its body diode conducting at the same time are analyzed.

The hypothetical cases are investigated for the converter running at 46.5 kW input power (MPP Power of 19 series, 9 parallel strings of CSUN panels at 1000W/m^2 0ºC condition) and the converter running at 67.2 kW input power (MPP Power of 19 series, 13 parallel strings of CSUN panels at 1000W/m^2 0ºC condition).

The results are summarized in Table 3.11.

Table 3.11. *Theoretical Losses*

Power [kW]	*Loss [W] Case A Diode*	*Loss [W] Case B MOSFET*	*Loss [W] Case Diode&MOSFET*
46.5	173	130	126
67.2	290	229	202

From this quantitative study, it can be seen that a significant power loss is eliminated if the diode conducts together with the MOSFET, making a difference of 90W approximately.

CHAPTER 4

EXPERIMENTAL SETUP DESCRIPTION AND EXPERIMENTAL RESULTS

4.1. Experimental Setup

For a thorough analysis of all the four boost converter configurations, a common and identical experimental setup was used. A simple block diagram of the test setup is given in Figure 4.1.

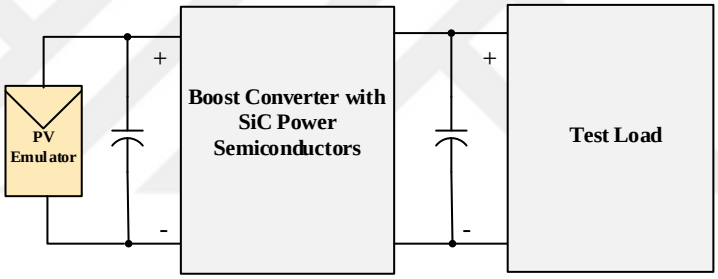


Figure 4.1. Test Setup Block Diagram

The setup involved the use of Magna-Power TSD800-24 High Power DC Power Supply and its Photovoltaic Power Profile Emulation Tool Software running on a computer communicating with it via the RS232 communication interface.

TSD800-24 supply is able to modulate the voltage or current setting using the piecewise linear approximation. This enables programmability of the supply for user needs. The emulator utilizes photovoltaic panel technology characteristics to create a 50 point piecewise linear approximation table for use with the modulation feature available in the power supply.

For computer connectivity of the power supply and the photovoltaic power emulator, an RS232 to USB converter and its computer driver from DIGITUS had to be also included in the setup. CSUN255-60P photovoltaic panel was chosen to be emulated; and therefore, the profiles generated for two parallel strings of 19 series panels were derived from datasheet values of CSUN255-60P entered manually to the software.

Figure 4.2 the main window of the emulation software is presented. In results section, correct MPP operation is documented with screenshots of this main window, hence the utilization of this software as a part of the experimental setup is further elaborated in the figure with numbered items as 1: Power Supply Status and Control, 2: Reference Parameters (from datasheet), 3: Generated Profiles, 4: Profile Parameters (to generate profiles according to different panel temperatures and insolation levels), 5: Power Profile Datapoints (50 point piecewise linear approximation of the profiles), 6: Power Profile Graph (with the green crosshair showing the current position of operation, and black cross on the actual MPP)

For the load, instead of an inverter connected to the grid that is providing load regulation (and making sure all the available MPP power is sunk from the MPPT converter and the DC link voltage is regulated), a test load consisting of wire wound resistors and were used. For the chosen operation point of 700 V DC link voltage, the test load value is adjusted for each different input power the test was carried out. Along with different sets of resistors, for fine-tuning, a rheostat is used. In Figure 4.3 (a) rheostat and resistors can be seen. To keep the bulky resistors and the rheostat at a manageable temperature so that the overall load resistance does not deviate to higher values, fan cooling method was employed as a mean of keeping the test conditions stable.

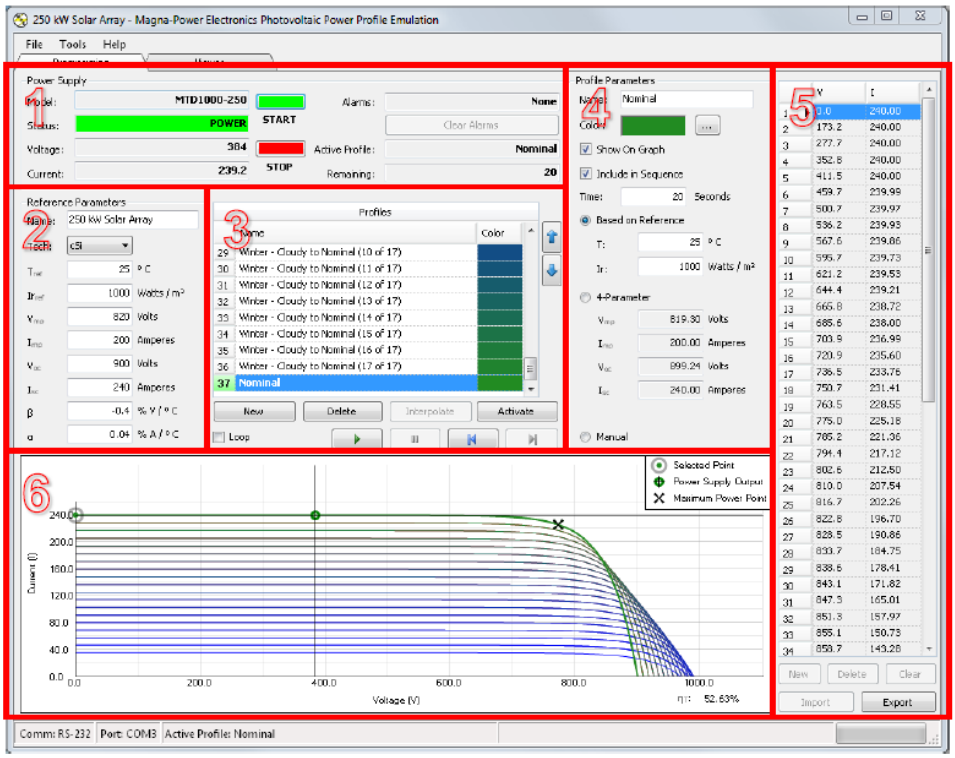


Figure 4.2. Main Window of Photovoltaic Power Profile Emulation Tool Software for Magna-Power TSD800-24 High Power DC Power Supply

a) b)

Figure 4.3. Experimental Setup Equipment (a) Rheostat and Resistors as the Test Load (b) Measurement Equipment

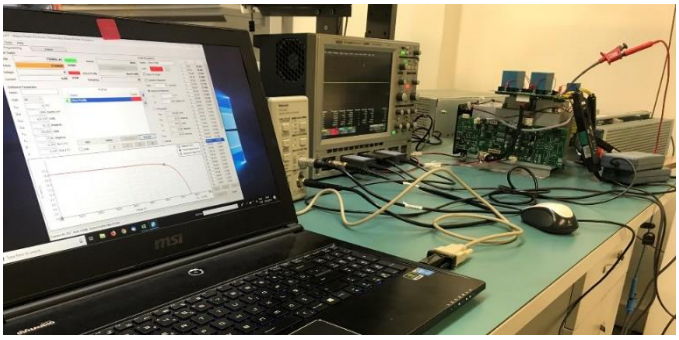


Figure 4.4. Overall Experimental Setup with Emulator Software Connection via RS232

Measurement equipment selected for the experimental setup included an oscilloscope, current probes and differential voltage probes as well as a thermal camera to monitor the thermal management of the power stage. The measurement equipment is given in Table 4.1.

Table 4.1. *Measurement Equipment*

Equipment	*Description*
Oscilloscope	LeCroy Waverunner 104MXI
Voltage Probes	ADP300 High Voltage Differential Probe
Current Probe Type 1	TCP305 AC/DC Current Probe
Amplifier for Current Probe Type 1	TCPA300 Current Amplifier
Current Probe Type 2	LeCroy CP030 AC/DC Current Probe
Thermal Camera	Fluke Ti125 Thermal Imager

4.2. MPP Operation of the Converter at Various Input Power Levels

In this section, power conversion and MPP finding performance of the implemented system is evaluated. For this purpose, the data taken from Magna-Power Photovoltaic Emulator and input and output voltage and current oscilloscope readings are presented.

The power and control stages of each of the four boost converter configurations were tested for MPP operation at power and insolation levels summarized in Table 4.2,

with the photovoltaic panel temperate set to 0 ºC in Magna-Power Photovoltaic Emulator.

Table 4.2. *Operating Points*

Maximum Power Point [kW]	*Insolation [W/m^2]*
3.28	325
5.67	550
8.54	825
10.33	1000

Implemented MPPT algorithm successfully located different MPPs for the four power profiles generated by Magna-Power Photovoltaic Emulator software for the custom CSUN255-60P array (2 parallel strings of 19 series panels) configuration. The power stage of each configuration delivered the necessary power at each profile.

Although the tests are carried out for all the four power stage configurations, to avoid repetition, from the operational data collected, only TPISBC configuration's data for the four different power and insolation levels are given in this subsection. Screenshots taken from Magna-Power Photovoltaic Emulator and the oscilloscope waveform confirm the correct operation of the device at each different power profile, from low power to high power.

From Figure 4.5, Figure 4.7, Figure 4.9 and Figure 4.11, screenshots taken from Magna-Power Photovoltaic Emulator for TPISBC configuration subjected to different photovoltaic profiles can be seen. The MPP finding accuracy can be monitored from η_T value. Overlap of the green crosshair which indicates the power supply output and black cross that depicts MPP on the profile curve shows the MPP is successfully located by the MPPT algorithm and the operation is carried out at the MPP. Also, the power drawn from the input can be monitored from the voltage and current values given in the screenshots.

The input and output voltage and current waveforms are shown in Figure 4.6, Figure 4.8, Figure 4.10 and Figure 4.12 for TPISBC configuration subjected to a different photovoltaic profiles. Notice that the output voltage is boosted and kept nearly at the decided 700 V DC-Link voltage (taking into ±1% measurement error of the probe).

The oscilloscope's math functions were also used to calculate the input and the output power in real-time, as well as efficiency. Due to the ±1% error rate of each oscilloscope probe, it is not possible to measure efficiency correctly for a fair efficiency comparison of the four boost converter configurations, likewise done in theoretical efficiency results in section 1.1. However, looking at the efficiency at different powers from the oscilloscope figures for a single configuration, the same trend of efficiency decreasing at lower powers (discussed in theoretical efficiency results in section 1.1) can still be observed. For this trend please see corresponding oscilloscope screenshots for the TPISBC configuration given in this section.

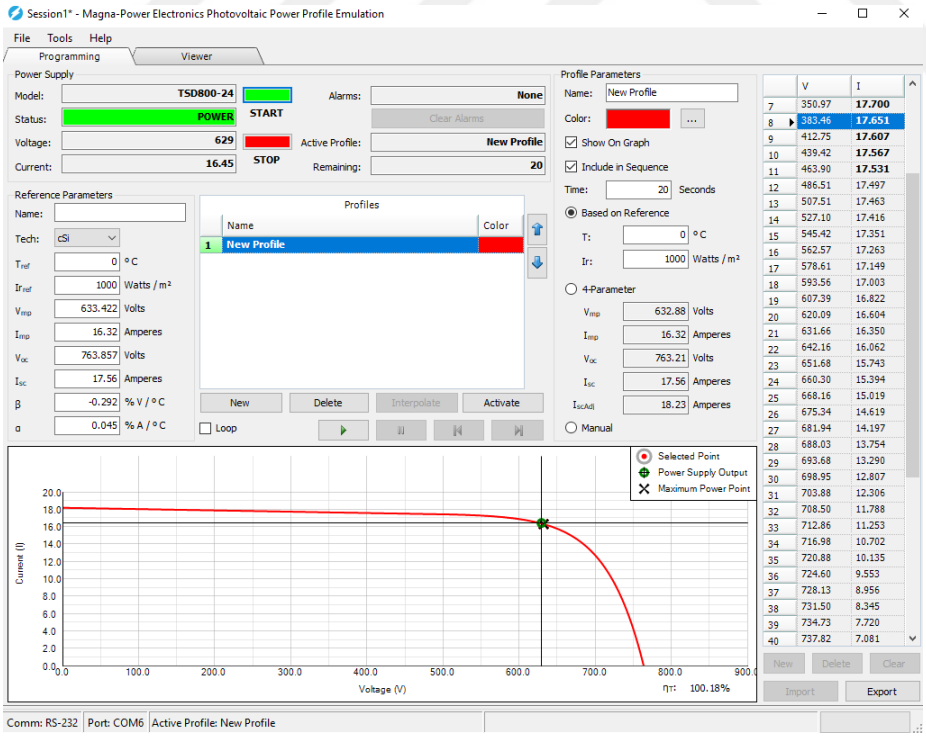


Figure 4.5. TPISBC Power Stage 1000 W/m^2 operation at MPP

Figure 4.5 is a screenshot taken from the Magna-Power Photovoltaic Emulator whilst the TPISBC configuration is subjected to a 1000 W/m^2 power profile. It is monitored from the screenshot that 10.3 kW power is drawn from the input of the power supply and the green crosshair which indicates the power supply output overlaps with the cross that depicts MPP on the profile curve. At the time, the screenshot was taken, the input voltage and current were 629 V, and 16.45 A respectively. Although MPP is entered as 633.42 V and 16.32 A, the profile generated by Magna-Power's 50 points piecewise linear approximation placed the MPP to 631.66, 16.350 A point. Because Magna-Power's Photovoltaic Power Emulation Tool control loop found to be slightly lagging; at the time of the screenshot was taken, as the drawn power is slightly more than the profiles calculated MPP, the MPP finding accuracy in the figure resulted in 100.18% (normally this value should be less than 100%, this is due to emulator error).

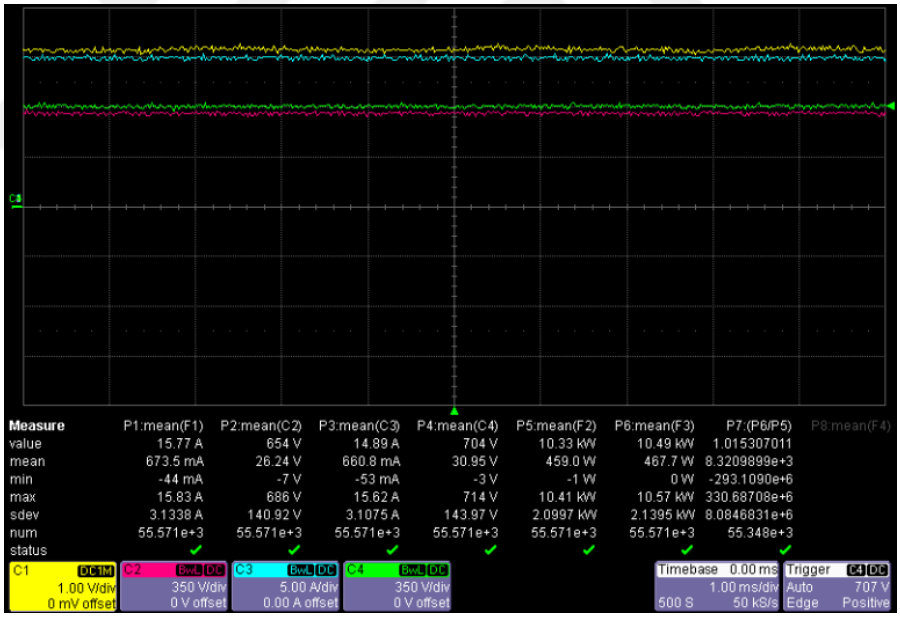


Figure 4.6. TPISBC Power Stage 1000 W/m^2 operation at MPP: C1- Input Current (5A/V), C2-Input Voltage, C3-Ouput Current, C4-Output Voltage, P1 to P4-mean of channels C1 to C4, P5-Input Power, P6-Output Power, P7-Efficiency

The input and output voltage and current waveforms are shown in Figure 4.6 for the TPISBC configuration subjected to 1000 W/m^2 power profile. It is seen from the figure that the input power is 10.3 kW, which is the power at MPP for the entered profile. Efficiency value calculated by math functions of the oscilloscope is slightly over 100%, this error arises from the ±1% error rate of each oscilloscope probe.

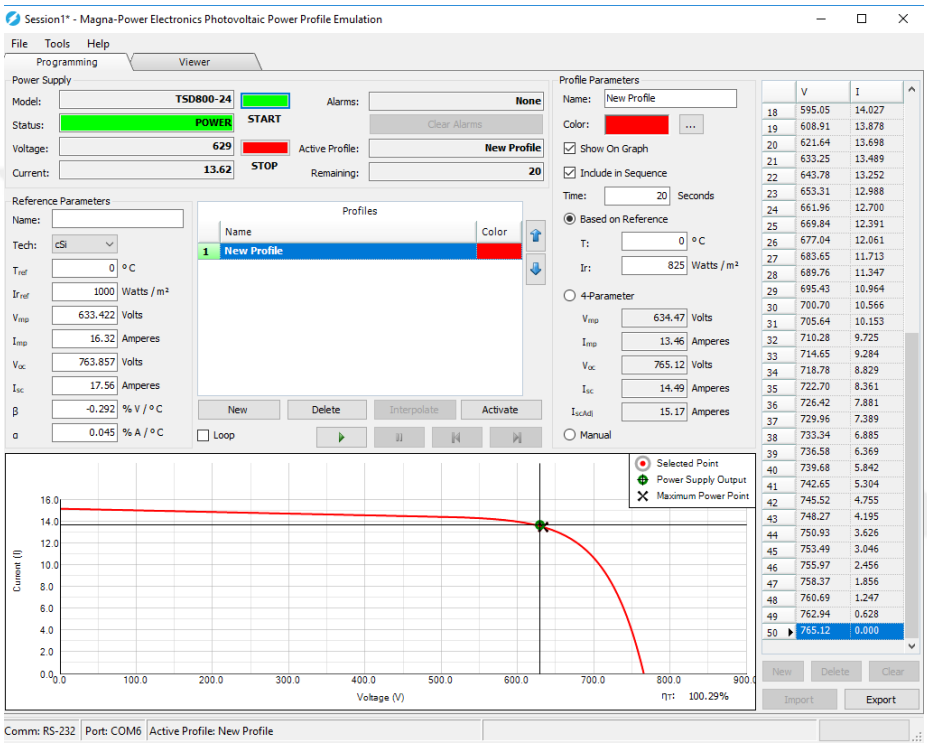


Figure 4.7. TPISBC Power Stage 825 W/m^2 operation at MPP

Figure 4.7 is a screenshot taken from the Magna-Power Photovoltaic Emulator whilst the TPISBC configuration is subjected to a 825 W/m^2 power profile. It is monitored from the screenshot that 8.5 kW power is drawn from the input at MPP.

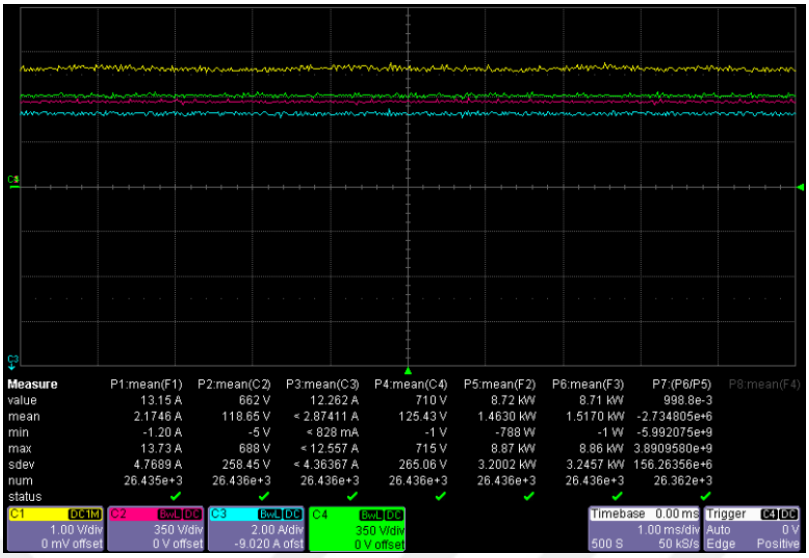


Figure 4.8. TPISBC Power Stage 825 W/m^2 operation at MPP: C1- Input Current (5A/V), C2-Input Voltage, C3-Ouput Current, C4-Output Voltage, P1 to P4-mean of channels C1 to C4, P5-Input Power, P6-Output Power, P7-Efficiency

The input and output voltage and current waveforms are shown in Figure 4.8 for the TPISBC configuration subjected to 825 W/m^2 power profile. It is seen from the figure that the input power is 8.7 kW. Efficiency value calculated by math functions of the oscilloscope is slightly over expected, this error arises from the ±1% error rate of each oscilloscope probe.

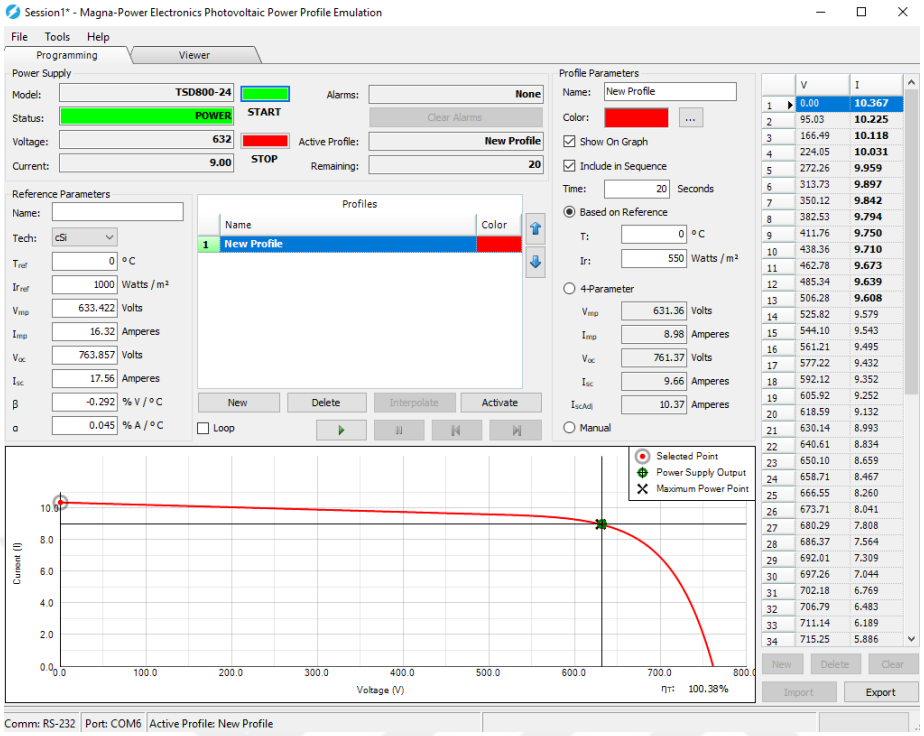


Figure 4.9. TPISBC Power Stage 550 W/m^2 operation at MPP

Figure 4.9 is a screenshot taken from the Magna-Power Photovoltaic Emulator whilst the TPISBC configuration is subjected to a 550 W/m^2 power profile. It is monitored from the screenshot that 5.7 kW power is drawn from the input at MPP.

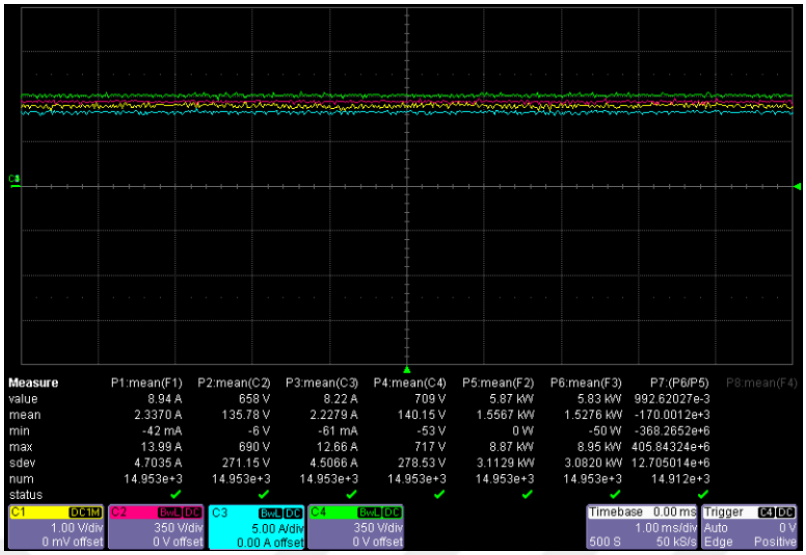


Figure 4.10. TPISBC Power Stage 550 W/m^2 operation at MPP: C1- Input Current (5A/V), C2-Input Voltage, C3-Ouput Current, C4-Output Voltage, P1 to P4-mean of channels C1 to C4, P5-Input Power, P6-Output Power, P7-Efficiency

The input and output voltage and current waveforms are shown in Figure 4.10 for the TPISBC configuration subjected to a 550 W/m^2 power profile. It is seen from the figure that the input power is 5.9 kW. Efficiency value calculated by math functions of the oscilloscope is slightly over expected, this error arises from the ±1% error rate of each oscilloscope probe.

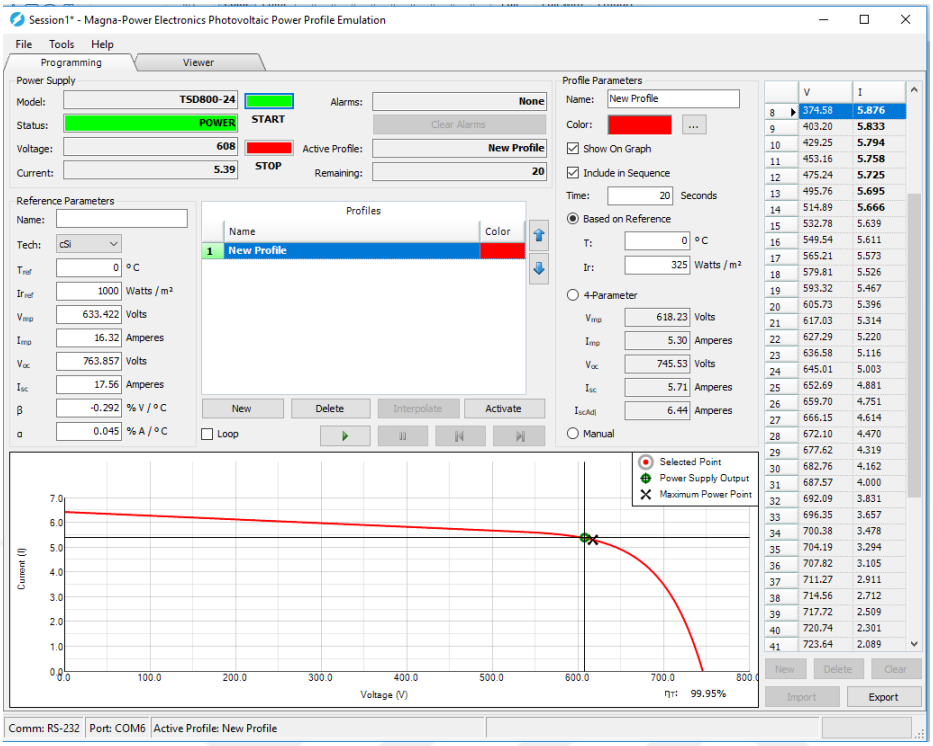


Figure 4.11. TPISBC Power Stage 325 W/m^2 operation at MPP

Figure 4.11 is a screenshot taken from the Magna-Power Photovoltaic Emulator whilst the TPISBC configuration is subjected to a 325 W/m^2 power profile. It is monitored from the screenshot that 3.3 kW power is drawn from the input at MPP.

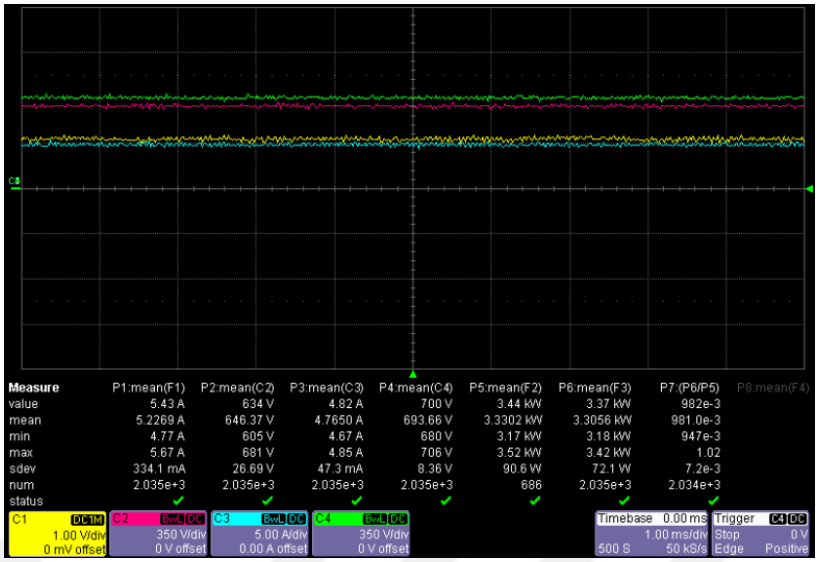


Figure 4.12. TPISBC Power Stage 325 W/m^2 operation at MPP: C1- Input Current (5A/V), C2-Input Voltage, C3-Ouput Current, C4-Output Voltage, P1 to P4-mean of channels C1 to C4, P5-Input Power, P6-Output Power, P7-Efficiency

The input and output voltage and current waveforms are shown in Figure 4.12 for the TPISBC configuration subjected to 325 W/m^2 power profile. It is seen from the figure that the input power is 3.4 kW. Efficiency value calculated by math functions of the oscilloscope is slightly over expected, this error arises from the ±1% error rate of each oscilloscope probe.

4.3. Switching Waveforms

At high voltages and currents, fast switching speeds of the semiconductor switches results in higher dV/dt and dI/dt. Combined with the stray inductances and capacitances that form unintentional resonant circuits, this effect is often vital, exposing the circuit elements to voltage and current overshoot and ringing.

The aim is to always limit the circuit parasitics as much as possible by a careful board layout design; however, there is nothing that can be done about the parasitics that are

already included in the semiconductor module used in terms of minimizing them, as it is a natural result of the device's physics.

The voltage overshoot at turn-on could expose the device underuse to a voltage higher than its defined maximum device voltage rating damaging the device permanently. Overshoots can be dampened by reducing the switching speed by choosing a higher gate resistance; although this increases switching losses. [24]

In this section critical waveforms that are observed during switching are given. MOSFET drain to source voltage (V_{DS}) indicates the switching performance of the design. In and Figure 4.14, V_{DS} waveform taken from the low-side boost converter switch of TPISBC configuration is given (very similar waveforms are observed in other four configurations as the driver circuitry, gate resistance and parasitics involved are the same for all), when the DC-Link voltage is as high as 740 V, which creates a scenario worse than the normal operating voltage of 700 V. It is seen that the switching performance is satisfactory with very low overshoot and acceptable oscillation.

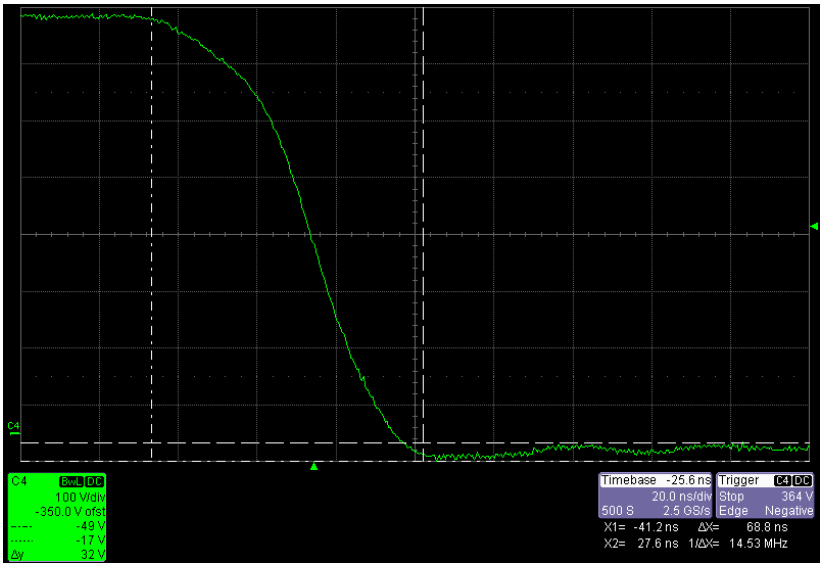


Figure 4.13. TPISBC Power Stage: Zoomed-in MOSFET VDS waveform during turn-on instant

In Figure 4.13, the zoomed-in VDS waveform during turn-on instant is given. While keeping the switch turn-on time as low as 70 ns as seen from the figure (from horizontal cursor measurement), it was possible to achieve relatively clean drain-source behavior.

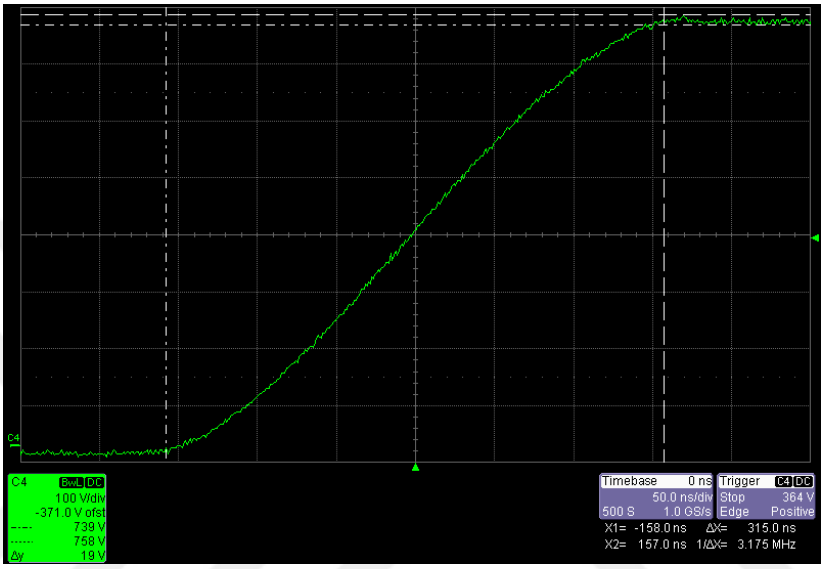


Figure 4.14. TPISBC Power Stage: Zoomed-in MOSFET V_{DS} waveform during turn-off instant

In Figure 4.14, the zoomed-in V_{DS} waveform during turn-off instant is given. It is seen from the vertical cursor measurement that only a 19 V overshoot is present, which does not put the device at risk of damage, and the voltage settles at 740 V. The turn-off time is longer than the turn-on time as it also depends on the output capacitance of the MOSFET discharging with the load connected to the system. At near 10 kW output power, the MOSFET turn-off time is measured as 315 ns from the horizontal cursor measurement.

For Synchronous Boost Converter options, as the high-side switch is also turned on, to prevent both switches conducting at the same time and short-circuiting the DC-Link and GND return path, a dead-band time is added.

In Figure 4.15, a single cycle of High-Side and Low-Side MOSFET VGS waveforms are shown. In actual operation, the body diode of the high-side MOSFET starts conducting immediately after the low-side MOSFET is turned off. When the dead-band time is over, high-side MOSFET is turned on while its drain-source voltage is at body-diodes conduction voltage. As the voltage of its drain-source is very low, the turning-on loss at this instant is negligible and can be considered zero-voltage-switching. Spike seen in Figure 4.15 at half time of the high-side switch's "turn-on" time is due to the noise generated when the other low-side switch of the interleaved power-stage starts conducting, and it is an oscilloscope measurement error.

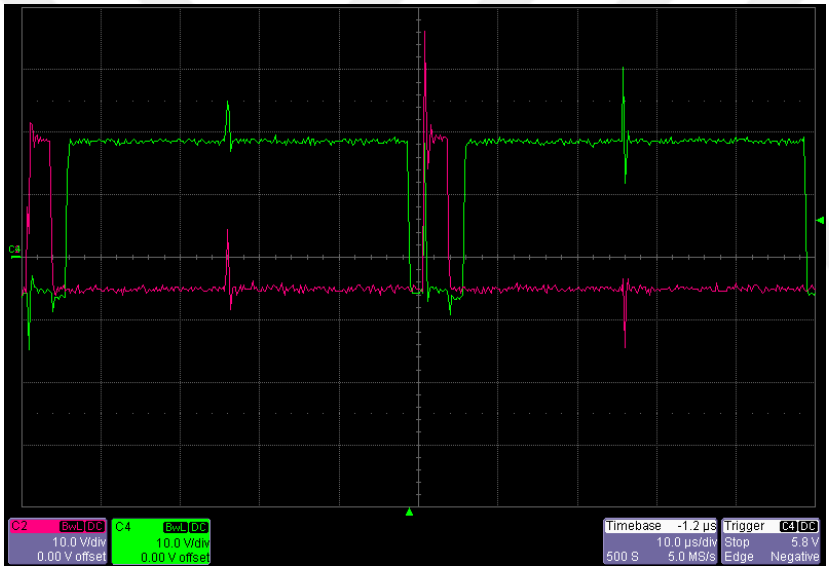


Figure 4.15. TPISBC Power Stage: One-Cycle High-Side and Low-Side MOSFET V_{GS} waveforms

Although the MOSFET turn-off and turn-on times are much shorter for full-load condition, for very light loads, it can delay up to 1.5 µs as experienced empirically; therefore, a dead-band time of 2 µs was used. It is seen in Figure 4.16 that the dead-band is measured as 2 µs from horizontal cursor measurement.

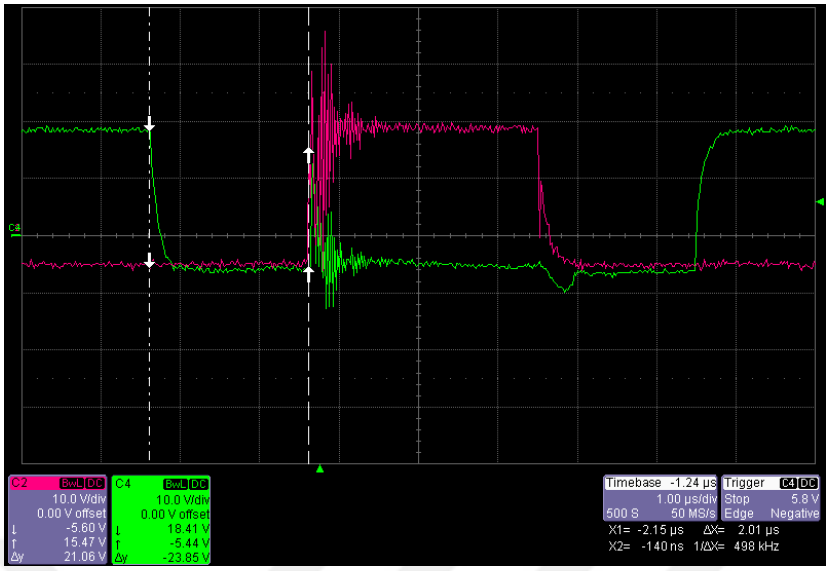


Figure 4.16. TPISBC Power Stage: Zoomed-In High-Side and Low-Side MOSFET V_{GS} waveforms with dead-band: C2 - Low-Side MOSFET V_{GS}, C4 - High-Side MOSFET V_{GS}

4.4. Operational Waveforms

In this section, device operation is discussed based on the critical operational waveforms measured during tests.

In Figure 4.17, waveforms given are for the TPISBC power stage configuration. The interleaved operation can clearly be seen from the phase difference of inductor current waveforms and their corresponding low-side MOSFET V_{DS} waveforms. It should also be noted that the test was done at 10.3 kW input power conditions and the two inductors shared the input current almost equally in a balanced manner. Often with interleaved topologies, due to impedance mismatch, interleaved legs end-up sharing the current in an unbalanced manner if the same duty cycle is applied; however, with this design, that was not the case; therefore a load-balancing control-loop that modifies duty cycle slightly for each leg was not necessary to implement.

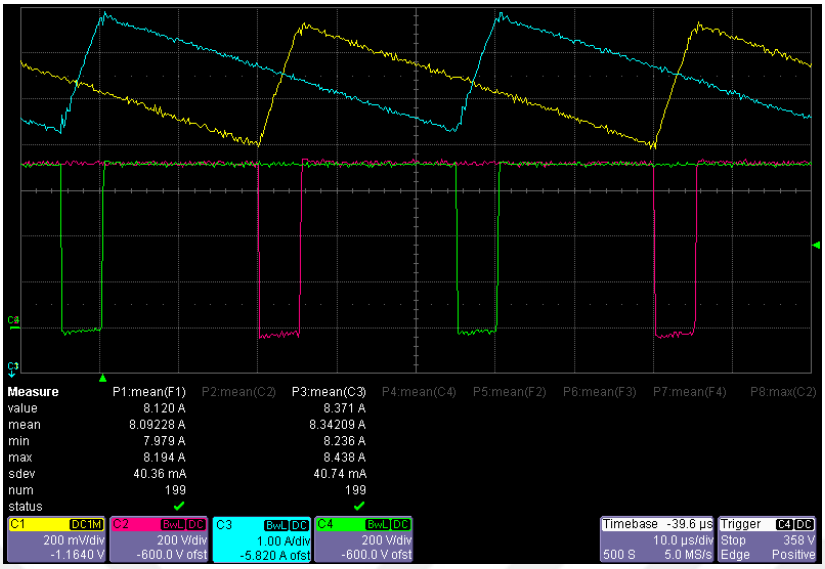


Figure 4.17. TPISBC Power Stage Operational Waveforms: C1- Inductor-1 (L1) Current Waveform (5A/V), C3 – Inductor-2 (L2) Current Waveform, C2 – S1 V_{DS} waveform, C4 – S3 V_{DS} waveform

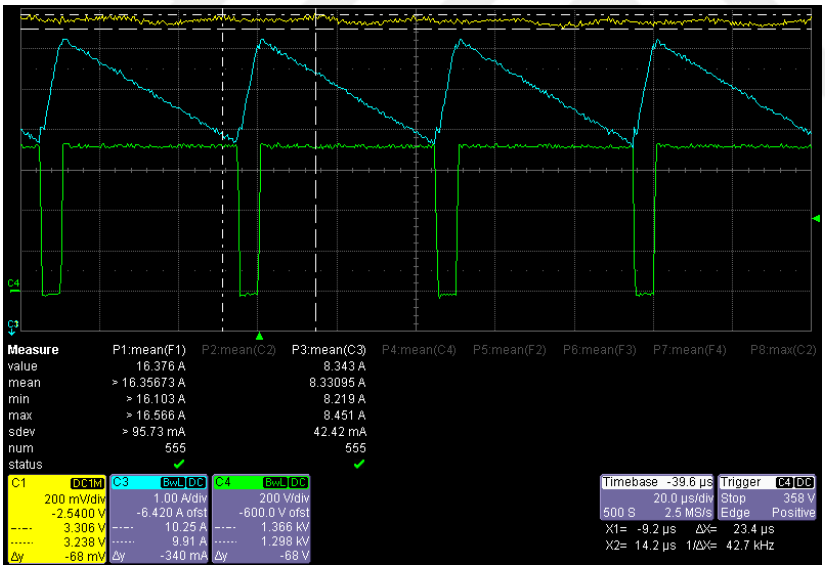


Figure 4.18. TPISBC Power Stage Operational Waveforms: C1- Input Current Waveform (5A/V), C3 – Inductor-1 (L1) Current Waveform, C4 – S1 V_{DS} waveform

In Figure 4.18, input current waveform vs. inductor current waveform is given for the TPISBC power stage configuration. The waveforms are taken at the same condition

as Figure 4.17 in terms of input power being 10.3 kW. The device is operated at MPP. It is seen that the input current ripple is much less when compared to the inductor current. The input current is 16.4 A (from measurement P1) with 0.34 A ripple (from vertical cursor measurement for C1 where 200 mV corresponds to 1 A) with ripple frequency being 40 kHz (from horizontal cursor measurement). The inductor current is 8.3 A with 2.6 A ripple with ripple frequency being 20 kHz. At MPP, the input current ripple is 2%, (whilst the inductor ripple is as high as 31%) which aids the overall system efficiency by causing less oscillation around MPP point, and therefore losing less of the valuable solar energy.

In Figure 4.19, the input current waveform which is the same current flowing through the inductor is given for the SBC power stage configuration. The waveforms are taken at the same condition as Figure 4.17 in terms of input power being 10.3 kW and the converter operating at MPP. Input current is 16.5 A (from measurement P1) with 3.9 A ripple (from vertical cursor measurement for C1 where 200 mV corresponds to 1 A) with ripple frequency being 20 kHz. When compared to Figure 4.18, in terms of input current ripple, it can be concluded that interleaved configurations are more advantageous.

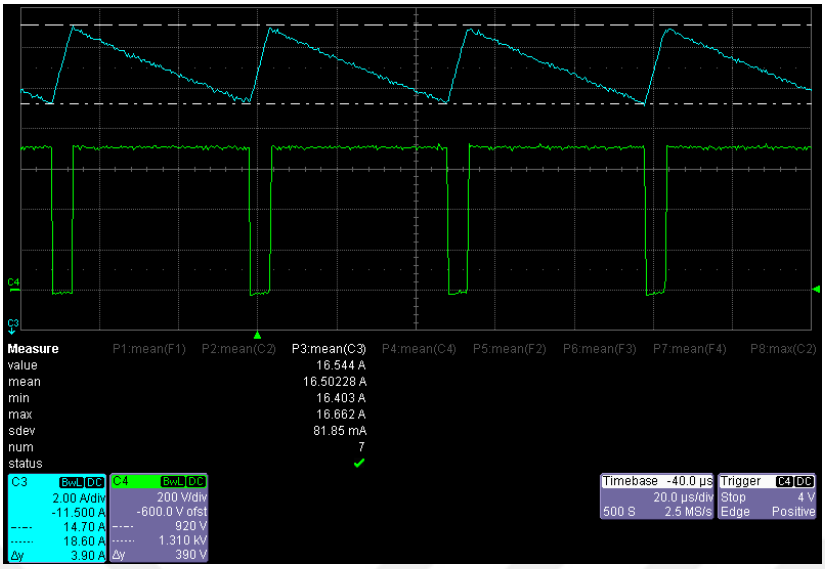


Figure 4.19. SBC Power Stage Operational Waveforms: C1- Input (Inductor) Current Waveform (5A/V), C4 – S1 V_{DS} waveform

4.5. Thermal Management

A test was done to identify the thermal management issues of the designed system. For this test, an interleaved configuration (TPISBC) and a non-interleaved configuration (SBC) was chosen. Both configurations were operated at MPP at the same input power of 10.3 kW, and the power was delivered for the same amount of time, which was 10 minutes.

Fluke Ti125 Thermal Imager is used to capture images in Figure 4.20. The temperature scale given on the right-hand side of the infrared images is in Celsius unit.

It is seen from Figure 4.20 (b) that the maximum temperature point for the inductor core of SBC configuration got as high as 79.4 ºC. Looking at Figure 4.20 (d), for TPISBC configuration, the maximum temperature point for inductor core only got to 43.1 ºC.

It can be concluded that, due to the current sharing nature of the interleaved operation, power loss that turns into heat is evenly distributed into interleaved legs, and therefore it is easier to thermally manage the interleaved configuration.

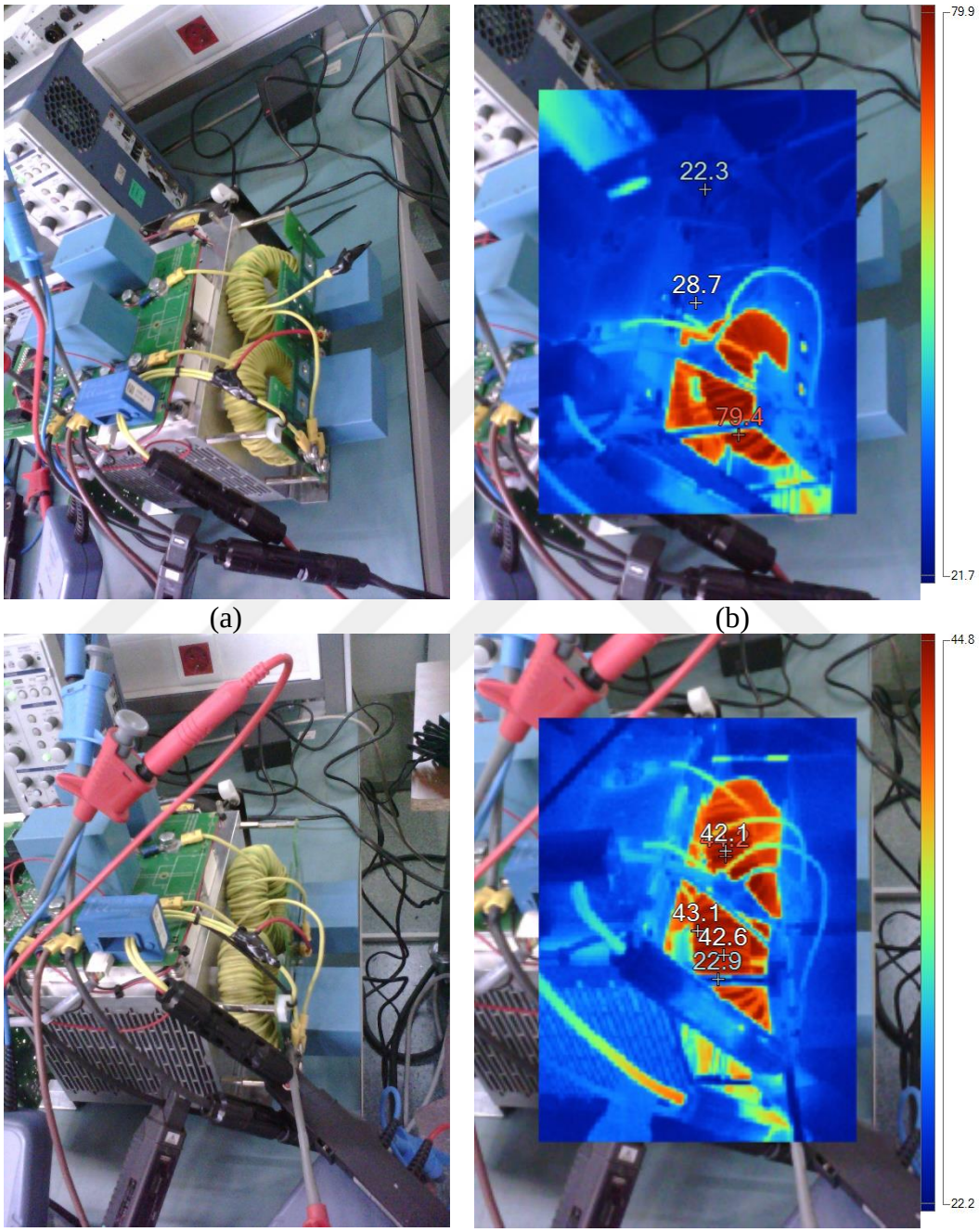


Figure 4.20. (a) Visible Light Image of SBC, (b) Infrared Image of SBC, (c) Visible Light Image of TPISBC, (d) Infrared Image of TPISBC

4.6. Calorimeter Setup

As seen in section 4.2, due to the ±1% error rate of each oscilloscope probe, it was not possible to measure efficiency correctly (in some cases, the output power was measured to be even more than the input power). For a fair efficiency comparison of four boost converter configurations mentioned in this work, a calorimeter setup was constructed out of a styrofoam box. Styrofoam was used for its insulating properties. Inside of the box, including the lid was covered with aluminum tape for aluminum's low emissivity (aluminum reflects thermal infrared radiation).

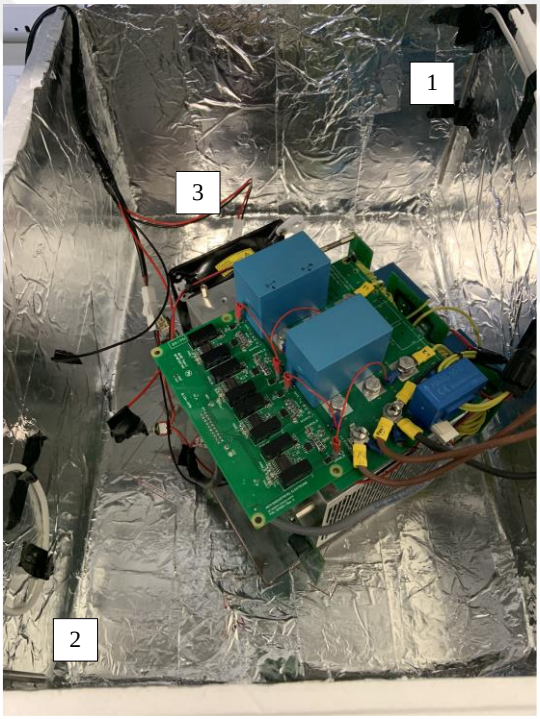


Figure 4.21. Calorimeter Setup 1: PT-100 Sensor 1, 2: PT-100 Sensor 2, 3: Heat Sink Fan

The device under test was located inside the Styrofoam calorimeter, and its lid was shut so that all the power dissipated as heat is measured with PT-100 type platinum resistance temperature detectors. PT-100 sensors were measured with multimeters

connected outside of the box (Agilent U1273A). PT-100 measurement, power input and load connection cables were run through the sides of the lid in a tight manner to avoid heat escaping through it to the outside of the box.

In Figure 4.22, the temperature profile of four boost converter configurations obtained with the calorimeter implemented is given for 10.3 kW input power (MPP Power of 19 series, 2 parallel strings of CSUN panels at 1000W/m^2 0ºC condition). The profile was obtained from PT-100 Sensor 1 readings, as it was more stable (whereas in PT-100 Sensor-2 readings due to the sensor being at close proximity to the fan output, a slight oscillation was present).

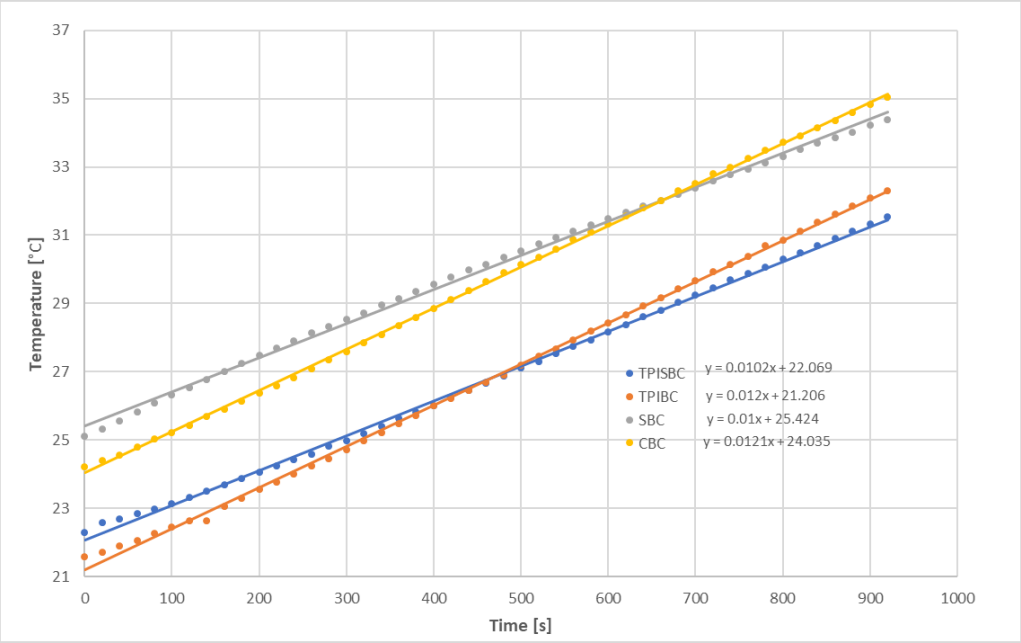


Figure 4.22. Temperature Profile of Boost Converter Configurations

The slope of the temperature profile indicates the power dissipation level. The steeper the slope, the more the dissipation; and hence implies less power conversion efficiency. From the slope of the temperature profiles (given in Figure 4.22 trendline

equations), it is seen that the synchronous converter options outperforms the other two configurations.

The efficiency rankings do not differ from what was found theoretically in section 3.1.2 Theoretical Efficiency.

In addition to temperature profiles of the converter configurations, with the use of the same heat-sink and chassis mount resistors, power profiles for known power levels are generated using the same calorimeter (with the same PT-100 sensor locations) to get an idea quantitively. The setup described is given in Figure 4.23.

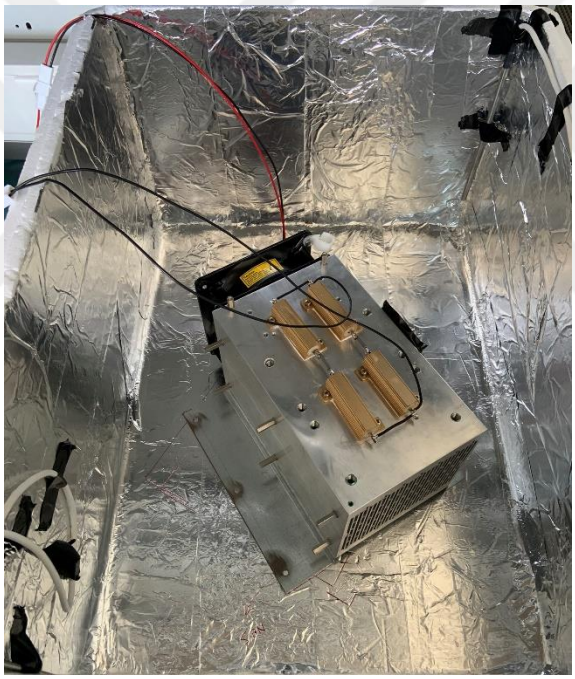


Figure 4.23. Resistor Setup

The resultant profiles are given in Figure 4.24. By comparing the slope of the temperature profiles given in Figure 4.24 trendline equations and Figure 4.22 trendline equations, it is understood that for TPISBC and SBC configurations, the dissipation is around 65 W, and for TPIBC and CBC configurations, the dissipation is around 80 W. This yields an estimated efficiency of 99.37% for TPISBC and SBC configurations,

and 99.22% for TPIBC and CBC configurations. These results correlate with the theoretical values obtained in section 3.1.2 Theoretical Efficiency.

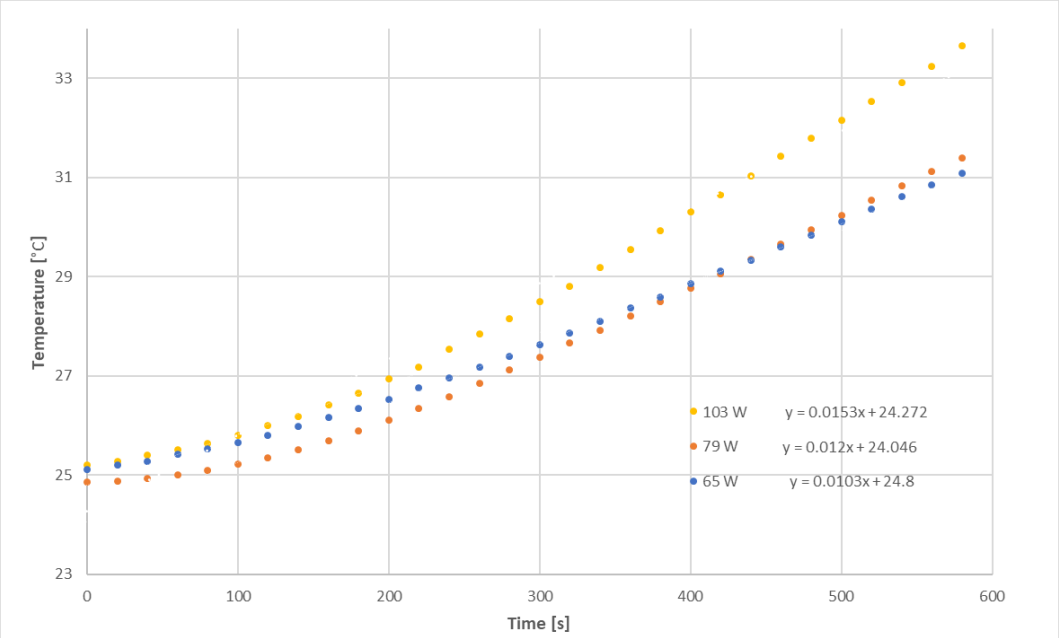


Figure 4.24. Temperature Profiles for Known Powers

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1. Conclusions

In this thesis work, design, implementation and functional testing of a 10 kW All-SiC MPPT Boost Converter were conducted. For comparison purposes in terms of power conversion efficiency, the power and control stage implemented was operated in four different configurations of which are Two-Phase Interleaved Boost Converter, Two-Phase Interleaved Synchronous Boost Converter, Conventional (Single-Phase) Boost Converter, Synchronous (Single-Phase) Boost Converter.

As part of the research, a calorimeter was also designed and implemented to estimate the power conversion efficiency values of each configuration option.

The designed hardware was then tested with a DC supply with photovoltaic power emulation capability at different input powers in order to analyze the operation of each device configuration.

Together with the calorimeter designed, each option was run on 10.3 kW power to estimate its efficiency. For synchronous options, an estimated efficiency of 99.4% is reached; whilst for non-synchronous options, an estimated efficiency of 99.2%

is observed. These results correlated with theoretical findings.

The resultant observations of importance gathered from this research are summarized in this section.

Utilization of SiC MOSFET promises decreased switching losses for the same switching frequency when compared to Si IGBTs; therefore, a higher switching frequency can be used to reach competitive efficiencies with higher power density. This also reduces the cost/kW of the power converters implemented using SiC MOSFET instead of a Si IGBT.

Owing to MOSFET's reverse conduction capability from its source to its drain, it is possible to use a MOSFET half-bridge module instead of a switch and diode separately to construct the boost converter power-stage. This way, synchronous rectification can be performed to lower conduction losses. This would not possible with an IGBT half-bridge module as IGBTs do not allow for reverse currents from emitter to collector.

When synchronous rectification is employed with a SiC MOSFET that has a SiC body diode, with the help-of dead-band between lower and upper MOSFETs, zero voltage switching can be applied to the high-side MOSFET. For high-side MOSFET, at the turn-on instant the SiC body diode of it turns-on before it is made "on" (due to dead-band). Also, at turn-off of the high-side MOSFET, before the lower MOSFET is made "on" (due to deadband), once again the body diode of the high-side MOSFET takes on the current. Therefore, with the help of the high-side body diode, the high-side MOSFET is switched with almost-zero losses, as the voltage across the diode is very close to zero, it can be considered as zero-voltage switching. This way, best of both worlds is achieved in terms of zero-losses due to utilization of SiC diode, and lower conduction losses due to transferring the current to SiC MOSFET.

Furthermore, at higher powers, the body diode of the synchronous rectifying MOSFET conducts together with the MOSFET itself. This phenomenon further reduces conduction losses.

Interleaving is a type of power-stage paralleling method that increases effective switching frequency without increasing switching losses. Whilst individual switches are switched at a frequency f_{sw}, the frequency of input current ripple and the output capacitor current ripple f_{sw} times the number of phases. The benefit of this is increased power density without efficiency reduction.

With interleaving, for the same power rating and input current, both the average and peak inductor and semiconductor currents get divided by the number of phases available. Due to this, if the same parts are used, the number of phases times more

power can be converted, or for the same power rating, parts with slighter ratings can be used.

In an interleaved boost converter, the input ripple current and output capacitor currents get reduced owing to the ripple cancellation effect. Inductor current ripple remains unchanged for the same inductance value; however, because the input current ripple is reduced, inductors with lower inductance can be used.

Interleaving also increases the reliability of the system with built-in redundancy. If one of the phases fails, the system could still operate in certain conditions at reduced power.

For systems with higher reliability and power density employing TPISBC configuration is a decent choice at the cost of the increased part count. For a cost-oriented design with less competitive power density requirements, SBC or CBC could be employed.

5.2. Future Work

In terms of efficiency, the resultant converter configurations are all satisfactory; however, to test the effects and improve the hardware and software to be able to develop this research work into a usable product, additional work can be conducted.

In terms of experimenting, as in interleaved options, each phase actually supports 10.3 kW input power, the interleaved options could be tested with a 20 kW power supply. If the inductors are redesigned, with the current semiconductors involved, even higher powers could be tested. This way, the hypothetical scenario presented in section 3.1.4 Discussion on Synchronous Rectification can be investigated. The load used was a passive load during tests. An actual inverter could be used to fully test the device and its integration with the inverter and the grid.

A comparison study could be conducted between the boost topology and High Frequency Link MPPT Converter presented in [25]. Both the device presented in this

work, and the hardware described in [25] possess the same CAS120M12BM2 MOSFETs.

At lower powers phase-shedding method could be employed in interleaved configurations to achieve better efficiency. Phase-shedding can be done with the software by simply disabling the gate signals of one of the phases. As seen in section 3.1.2 Theoretical Efficiency, the efficiencies of non-interleaved (single-phase) configurations, are expected to outperform interleaved configurations in lower powers.

In synchronous options, the dead-band between upper and lower MOSFET's could be adjusted by the software according to the power. This will allow less dead-band to be used at higher powers, as at lower powers MOSFET turning-off times increase.

In general, the MPPT algorithm could be improved to include partial-shading detection. Depending on the inverter's dynamic performance, full or partial sweeping of operable duty cycles can be done to determine which local MPP delivers more power.

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