ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

A DESIGN OF SUB-mW-POWER 2.4 GHZ CMOS CASCODE LOW NOISE AMPLIFIER WITH HIGH LINEARITY

M.Sc. THESIS

Didem EROL AS

Department of Electronics and Communications Engineering

Electronics Engineering Programme

SEPTEMBER 2021

ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

A DESIGN OF SUB-mW-POWER 2.4 GHZ CMOS CASCODE LOW NOISE AMPLIFIER WITH HIGH LINEARITY

M.Sc. THESIS

Didem EROL AS
(504181208)

Department of Electronics and Communications Engineering

Electronics Engineering Programme

Thesis Advisor: Assoc. Prof. Dr. Mustafa Berke YELTEN

SEPTEMBER 2021

ISTANBUL TEKNİK ÜNİVERSİTESİ ★ LİSANSÜSTÜ EĞİTİM ENSTİTÜSÜ

YÜKSEK DOĞRUSALLIĞA SAHİP mW ALTI GÜÇ İLE ÇALIŞAN 2.4 GHZ CMOS KASKOD DÜŞÜK GÜRÜLTÜLÜ KUVVETLENDİRİCİ

YÜKSEK LİSANS TEZİ

Didem EROL AS
(504181208)

Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

Elektronik Mühendisliği Programı

Tez Danışmanı: Doc. Dr. Mustafa Berke YELTEN

EYLÜL 2021

Didem EROL AS, a M.Sc. student of ITU Graduate School of Science Engineering and Technology student ID 504181208, successfully defended the thesis entitled “A Design of sub-mW-Power 2.4 GHz CMOS Cascode LNA with High Linearity”, which she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

Thesis Advisor : **Assoc. Prof. Dr. Mustafa Berke YELTEN**
Istanbul Technical University

Jury Members : **Assoc. Prof. Dr. Metin YAZGI**
Istanbul Technical University

Assoc. Prof. Dr. Engin AFACAN
Gebze Technical University

Date of Submission : 02.09.2021
Date of Defense : 06.09.2021

FOREWORD

I would like to express my gratitude to my advisor, Assoc. Prof. Dr. Mustafa Berke YELTEN for his great support and immense knowledge. He has always answered my questions with great patience. I have shaped my academic career with his encouragement and guidance.

I would like to thank Assoc. Prof. Dr. Metin YAZGI and Assoc. Prof. Dr**.** Engin AFACAN for serving in my thesis committee.

I express my gratitude to Res. Assist. M.Sc. Ali Doğuş GÜNGÖRDÜ for his co-operation. We were often in contact with him throughout the semester. It was a pleasure to work together.

I would like to express my deepest appreciation to Berk AS. He has always believed me at the desperate moments. I could finish my thesis with his endless support. He has always encouraged me intellectually and emotionally. This thesis would not have been possible without his special effort. Finally, I owe my gratitude to my parents for their love and support. They have always encouraged me and supported my decisions regardless of the outcome.

This thesis is supported by TUBITAK (Scientific and Technical Research Council of Turkey) under Contract 118E253. I would like to thank TUBITAK for the support of this thesis.

September 2021

Didem EROL AS
(Res. Assist.)

TABLE OF CONTENTS

Page

ABBREVIATIONS

ADC : Analog-Digital Converter
BJT : Bipolar Junction Transistor
BLE : Bluetooth Low Energy
CG : Common Gate
CMOS : Complementary Metal Oxide Semiconductor
CS : Common Source
DS : Derivative Superposition
ESL : Equivalent Series Inductance
ESR : Equivalent Series Resistance
IIP2 : Second-order Intercept Point
IIP3 : Third-order Intercept Point
IM : Intermodulation
IoT : Internet of Things
ISM : Industrial Scientific Medical
LNA : Low Noise Amplifier
LO : Local Oscillator
NF : Noise Figure
NF_{min} : Minimum Noise Figure
NMOS : N-channel Metal Oxide Semiconductor
OIP3 : Third-order Output Intercept Point
P1dB : 1-dB Compression Point
PD : Post-distortion
PMOS : P-channel Metal Oxide Semiconductor
PSD : Power Spectral Density
PVT : Process Voltage Temperature
RF : Radio Frequency
SNR : Signal to Noise Ratio
VCO : Voltage Controlled Oscillator

SYMBOLS

C	**:** Capacitance
dB	**:** Decibel
F	**:** Farad
H	**:** Henry
Hz	**:** Hertz
K	**:** Kelvin
k	**:** Boltzmann Constant
L	**:** Inductance
m	**:** meter
R	**:** Resistance
P	**:** Power
W	**:** Watt
Ω	**:** Ohm
g_m	**:** Transconductance
g_3	**:** Third-order Transconductance
S_{11}	**:** Input Reflection Coefficient
S_{12}	**:** Reverse Transmission Coefficient
S_{22}	**:** Output Reflection Coefficient
S_{21}	**:** Transmission Coefficient

LIST OF TABLES

Page

LIST OF FIGURES

Page

DESIGN OF AN ULTRA LOW POWER 2.4 GHZ CMOS CASCODE LOW NOISE AMPLIFIER WITH HIGH LINEARITY

SUMMARY

Radiofrequency (RF) communication systems are rapidly growing in the telecommunication industry. Nowadays, wireless technology is also used for health applications, Internet of things (IoT), Bluetooth low energy (BLE) applications. These applications require the design of low-power devices. Taking into these considerations, research studies of complementary metal-oxide-semiconductor (CMOS) RF front-end circuits increase with the demand for a low-cost but high-performance wireless front-end. The implantable medical devices enable monitoring of physiological information, diagnosing diseases, and providing treatment to patients. These medical devices, such as wireless transceivers and implantable antennas, need to operate ultra-low power.

Linearity plays an important role in the performance of the receiver systems. The receiver performance is disrupted by interfering the unwanted components at the adjacent frequency channels to the transmitted signal. There are some linearization techniques aiming to cancel these distortions.

Low noise amplifiers (LNA), which are typically first and one of the most important stages of the receiver, greatly influence the overall receiver performance. Therefore, LNAs aim to amplify the weak signal with as little noise as. Additionally, the voltage gain and linearity are significant performance metrics of LNAs. However, power consumption limits these performance criteria. Thus, the main goal is to minimize the tradeoff between power consumption and high performance.

This thesis focuses on the design of low-power LNA with high linearity. Different LNA topologies operating with sub-mW power consumption at 2.4 GHz have been implemented in TSMC 40 nm technology. The cascode common source LNA (cascode CS LNA) has a voltage gain of 12.22 dB, a noise figure (NF) of 4.35 dB, and a third-order input intercept point (IIP3) of -12.68 dBm at 9995.6 μW while the proposed LNA with improved linearity has a 5.68 dB voltage gain, 5.13 dB NF, and a -0.107 dBm IIP3. The difference between both final designs, which consist of improved linearity and voltage gain, stems from the location of the gate inductance (L_g) in the chip. The proposed LNA with an on-chip (L_g) has a voltage gain of 11.1 dB, an NF of 4.27 dB, and an IIP3 of -0.816 dBm. Moreover, the post-layout results of the proposed LNA with an off-chip (L_g) are 10 dB voltage gain, 3.87 dB NF, and 2.19 dBm IIP3 at 989.6 μW . Comparing the LNAs, the proposed LNA with an off-chip (L_g) has the best figure-of-merit (FOM). This work aims to achieve improved linearity figures at sub-mW power.

Although the performance metrics of LNA4 are the best among the four topologies, it may not be suitable for medical equipment due to the off-chip input matching circuit. The fully integrated LNA3 topology is more suitable for medical applications. However, its performance metrics are needed to be improved.

YÜKSEK DOĞRUSALLIĞA SAHİP ULTRA DÜŞÜK GÜÇ İLE ÇALIŞAN 2.4 GHZ CMOS KASKOD DÜŞÜK GÜRÜLTÜLÜ KUVVETLENDİRİCİ

ÖZET

Radyo frekansı (RF) iletişim sistemleri telekomünikasyon endüstrisinde hızla büyümektedir. Günümüzde kablosuz teknoloji sağlık uygulamaları, nesnelerin interneti (IoT), Bluetooth düşük enerji uygulamaları için de kullanılmaktadır. Bu uygulamalar, düşük güçlü cihazların tasarımını gerektirir. Tüm bu durumlar dikkate alındığında, CMOS RF ön uç devreleri araştırmaları, düşük maliyetli ancak yüksek performanslı kablosuz ön uç talebi ile artmaktadır.

Vücuda yerleştirilebilir tıbbi cihazlar, fizyolojik bilgilerin izlenmesini, hastalıkların teşhis edilmesini ve hastalara tedavi verilmesini sağlar. Kablosuz alıcı-vericiler ve implante edilebilir antenler gibi bu tıbbi cihazların ultra düşük güçte çalışması gerekir.

Günümüzde teknolojideki önemli gelişmelere rağmen, doğrusal olmayan cihazlar nedeniyle kablosuz sistemlerin ve cihazların performansı hala kısıtlıdır. Radyo alıcılarının tasarımında, doğrusal olmama, radyoların güçlü sinyallerin yanı sıra zayıf sinyalleri de alma kapasitesini sınırlar. Radyo vericilerinde doğrusal olmama sorunu, iletilen sinyalin diğer kullanıcı sinyalleriyle etkileşime girmesine ve komşu frekans kanallarına yayılmasına neden olur. Bu durumlar sistemlerde bozulmaların meydana gelmesine neden olur. Bahsedilen bozulmaları azaltmak için sistemlere uygulanan bazı doğrusallaştırma teknikleri vardır.

CMOS düşük gürültülü yükselteçlerde lineerleştirme teknikleri 8 kategoriye ayrılmıştır. Bu teknikler; geri besleme, harmonik sonlandırma, optimum sapma, ileri besleme, türev süperpozisyonu (TS), ikinci dereceden intermodülasyon (IM2) enjeksiyonu, gürültü/bozulma iptali ve bozulma sonrasıdır. Türev süperpozisyonu, IM2 enjeksiyonu ve gürültü/bozulma iptali, geri besleme tekniğinin özel durumlarıdır.

Türev süperpozisyonu transistörlerin farklı bölgelerde çalışmasına dayanan bir tekniktir. Türev süperpozisyon olarak adlandırılmasının nedeni, distorsiyonu ortadan kaldırmak için ana ve yardımcı transistörün savak akımlarının üçüncü türevinin (g_3) eklenmesidir. g_3'ün işareti, orta ve güçlü inversiyon bölgesinde değişir. Geleneksel türev süperpozisyonu gibi bu teknikler, üçüncü dereceden bozulmayı iyileştirirken, genellikle ikinci dereceden bozulmayı kötüleştirir. "Tamamlayıcı türev süperpozisyon tekniği", ikinci dereceden kesişme noktasının (IIP2) değerini düşürmeden IIP3'ü iyileştirmek için NMOS/PMOS çiftini kullanır. Bu teknikte, zayıf evirme bölgesindeki transistör yüksek frekanslarda etkin bir şekilde çalışmayabilir. Ayrıca büyük sinyalleri işleyemeyebilir. Zayıf inversiyonda çalışan transistör modelleri, simülasyon ve ölçüm sonuçları arasındaki önemli tutarsızlıktan dolayı problemli olabilir. Farklı bölgelerde çalışan transistörler nedeniyle, doğrusallık iyileştirmeleri, proses gerilim sıcaklığı değişimleri ile değişir.

Düşük gürültü kuvvetlendiricisi, filtrelenmiş RF sinyalini fazla gürültü ve bozulma eklemeden yükseltmeyi amaçlayan alıcıların ilk aşamasıdır. Bir süperheterodin alıcı 5 ana bloktan oluşur: bir anten, bir RF filtresi, bir düşük gürültülü kuvvetlendirici, bir

karıştırıcı ve bir gerilim kontrollü osilatör. Antenden alınan filtrelenmiş RF sinyali, bir RF alıcı zincirinde bir yerel osilatör ile karıştırılarak karıştırıcı ile dönüştürülmeden önce LNA tarafından yükseltilir. Aşağı dönüştürülen sinyal demodüle edildikten sonra, bir analog-dijital dönüştürücü tarafından dijitalleştirilir.

Tipik olarak alıcının ilk ve en önemli aşamalarından biri olan düşük gürültülü kuvvetlendiriciler, genel alıcı performansını büyük ölçüde etkiler. Bu nedenle, düşük gürültülü kuvvetlendiricilerin amacı, zayıf sinyali olabildiğince az gürültü ile yükseltmektir. Ek olarak, güç kazancı ve doğrusallık, düşük gürültülü kuvvetlendiricilerin önemli performans ölçütleridir. Ancak, güç tüketimi bu performans kriterlerini sınırlar. Bu yüzden ana amaç, güç tüketimi ve yüksek performans arasındaki ödünleşimi en aza indirmektir.

Bu tez, düşük güçlü düşük gürültülü kuvvetlendiricilerin tasarımına odaklanmaktadır. Düşük gürültülü yükselteç sinyalinin çalışma frekansı 2,4 GHz Endüstriyel Bilimsel Tıp (ISM) bandında almalıdır. Düşük güçte çalışma, düşük akım seviyesinden dolayı gürültü ve gerilim kazancı için bir tasarım problemidir. Ayrıca, doğrusallık, gürültü rakamı ve gerilim kazancı ile bir ödünleşim içindedir. Bu nedenle, doğrusal, düşük güçlü LNA tasarımları ortaya çıkarmak için doğrusallık iyileştirme teknikleri kullanılmalıdır. 2.4 GHz'de mW altı güç tüketimi ile çalışan farklı düşük gürültülü kuvvetlendirici topolojileri, TSMC 40 nm teknolojisinde uygulanmıştır. Düşük güçlü kuvvetlendirici'nın özellikleri en az 10 dB gerilim kazancı ve 4 dB'den düşük gürültü değeri olarak belirlenmiştir. Giriş ve çıkış yansıma katsayılarının -10 dB'den düşük olması hedeflenir. Düşük gürültü kuvvetlendirici toplam 1 mW'tan daha az güç tüketirken IIP3 -1 dBm'den yüksek olması istenir.

Kaskod ortak kaynaklı düşük gürültülü kuvvetlendirici 12.2 dB güç kazancına, 4.35 dB gürültü faktörüne ve 995.6 μW'de -12.68 dBm üçüncü dereceden giriş kesişme noktasına (IIP3) sahipken, önerilen doğrusallığı geliştirilmiş düşük gürültülü kuvvetlendirici 5.68 dB güç kazanca, 5.13 dB gürültü faktörüne ve -0.107 dBm IIP3'e sahiptir. Geliştirilmiş doğrusallık ve güç kazancından oluşan her iki nihai tasarım arasındaki fark, çipteki kapı endüktansının (L_g) konumundan kaynaklanmaktadır. Kapı endüktansı (L_g) çip içinde olacak şekilde tasarlanan düşük gürültülü kuvvetlendiricinin güç kazancı 11.1 dB, gürültü faktörü 4.27 dB ve IIP3 değeri -0.186 dBm'dir. Ayrıca, kapı endüktansı (L_g) çip dışında olacak şekilde tasarlanan düşük gürültülü kuvvetlendirici, 989.6 μW güç tüketiminde 10 dB güç kazancı, 3,87 dB gürültü faktörü ve 2.19 dBm IIP3'e sahiptir. Önerilen düşük güçlü düşük gürültülü kuvvetlendiriciler karşılaştırıldığında, kapı endüktansı (L_g) çip dışında olacak şekilde tasarlanan düşük gürültülü kuvvetlendirici en iyi performansa sahiptir. Bu çalışma, mW altı güçte geliştirilmiş doğrusallık değerleri elde etmeyi amaçlamaktadır.

CMOS teknolojileri küçüldükçe, düşük güçlü kuvvetlendiricinin kazanç ve gürültü performansları düştü. Bunun yanı sıra, doğrusallık ve güç tüketimi arasındaki ödünleşim, ultra düşük güçlü LNA tasarımı için ana zorluklardan biridir. Derin mikron altı teknolojilerde tasarlanan düşük güçlü kuvvetlendiricilerin tıbbi uygulamalar gibi ultra düşük güçlü cihazlara entegrasyonu, geliştirilmesi gereken bir çalışma ve araştırma alanıdır.

Kapı endüktansı (L_g) çip dışında olacak şekilde tasarlanan düşük gürültülü kuvvetlendiricinin performans metrikleri dört topoloji arasında en iyisi olmasına rağmen, çip dışı giriş eşleştirme devresi nedeniyle tıbbi cihazlar için uygun olmayabilir. Tam entegre Kapı endüktansı (L_g) çip içinde olacak şekilde tasarlanan

düşük gürültülü kuvvetlendirici topolojisi, tıbbi uygulamalar için daha uygundur. Ancak, performans ölçütlerinin iyileştirilmesi gerekmektedir.

1. INTRODUCTION

Low noise amplifier (LNA) is the first stage of receivers, which aims to amplify the filtered RF signal without adding much noise and distortion. As seen in Figure 1.1, a superheterodyne receiver is composed of 5 main blocks: an antenna, an RF filter, a low noise amplifier, a mixer, and a voltage-controlled oscillator (VCO). The LNA amplifies the filtered RF signal received from the antenna before it will be down-converted with the mixer by mixing with a local-oscillator (LO) in an RF receiver chain [1]. After the downconverted signal is demodulated, it is digitalized by an analog-digital converter (ADC).

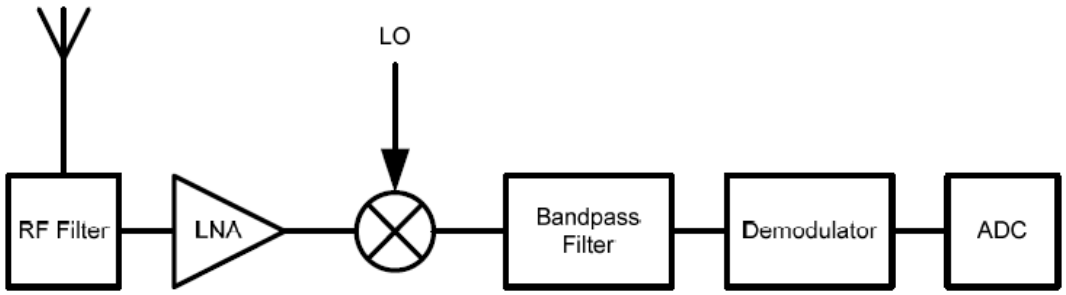


Figure 1.1: Block diagram of the simplified RF receiver.

The sensitivity and noise performances of the whole receiver system are affected by the performance of the LNA since the receiver consists of the cascaded stages in Figure 1.1. As it is known from the Friis expression, the noise and gain performances of each cascaded block contribute to the total noise of the system as equation (1.1).

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots \tag{1.1}$$

The noise figure of the low noise amplifier is the most dominant parameter for the noise of the overall receiver system because the first term of Friis equations represents the first stage of receivers. Therefore, the amplified RF signal at the output of the LNA needs to have low noise and distortion. Finally, the LNA must have a large voltage gain to suppress the noise of the subsequent stages [2].

CMOS technology has become more dominant in wireless applications due to the shrinking in channel geometry, which enables easy integration and large-scale production [3]. In recent years, wireless technology has been used in not only consumer electronics but also health applications, such as body temperature and heart rate sensors. For instance, monitoring instant body signals through portable and wireless devices can be performed using the Bluetooth low energy (BLE) technology with less power than the classical Bluetooth [4]. Biomedical applications have also increased the need for low-power transceiver circuits. The main problems of these systems and devices are portability, device size, and low power operation lasting for several days or even a year. Thus, ultra-low power and small-size wireless transceivers have been developed with a focus on radio frequency (RF) circuit design techniques using the standard CMOS technology [5].

Noise figure, gain, input and output reflection coefficients, linearity, and stability are the main performance metrics of the LNA. While the output reflection coefficient of the LNA is not significant in the system, it is critical for stability if the LNA is measured separately since strong reflection waves at the outputs have an impact on stability by sneaking through the LNA input.

LNA performance is mostly based on the process technology and the design strategy. Although the process technology limits the performance, the design strategy improves it. Therefore, the selection of the process technology and the design optimization are significant.

1.1 Purpose of Thesis

The implantable medical devices enable monitoring of physiological information, diagnosing diseases, and providing treatment to patients. These medical devices, such as wireless transceivers and implantable antennas, need to operate ultra-low power.

Despite the significant advances in technology today, the performance of wireless systems and devices is still constrained due to the nonlinear devices. In the design of radio receivers, non-linearity limits the capability of radios to receive weak signals as well as strong signals. Nonlinearity in radio transmitters causes the transmitted signal to interfere with other user signals and spread to neighboring frequency channels.

There are some linearization techniques applied to the systems to reduce the mentioned distortions.

This thesis aims to design an ultra-low power LNA with high linearity. The designed LNA should receive the signal at the 2.4 GHz Industrial Scientific Medical (ISM) band. Low-power operation is a design problem for the noise figure and the voltage gain due to the reduced current level. Moreover, linearity is in a tradeoff with the noise figure and the voltage gain [6]. Therefore, linearity improvement techniques should be employed to come up with linear, low-power LNA designs.

This thesis is a part of the TUBITAK project "Scalable Time-Based Degradation, Cryogenic, and Radiation Modeling of 40 nm Transistor Technology for Analog Circuit Applications in Internet-of-Things, Defense and Innovative Computational Methods Industries". Specifications of the LNA are designated as the voltage gain of 10 dB, the noise figure of lower than 4 dB. Input and output reflection coefficients are targeted to be lower than -10 dB. The input IP3 is desired to be higher than -1 dBm while the amplifier consumes a total power of less than 1 mW.

1.2 Literature Review

Linearization techniques in CMOS low-noise amplifiers are divided into 8 categories. These techniques are feedback, harmonic termination, optimum biasing, feedforward, derivative superposition (DS), second-order intermodulation (IM2) injection, noise/distortion cancellation, and post-distortion. Derivative superposition, IM2 injection, and noise/distortion cancellation are special cases of the feedback technique. The advantages and disadvantages of derivative superposition, noise/distortion cancellation, and post-distortion techniques will be discussed.

The derivative Superposition technique is a special type of feed-forward technique. With this technique, an amplifier design with very low third-order interconnection distortion can be realized.

It is a technique based on the operation of transistors in different regions. The reason why it is called "derivative superposition" is that the main and auxiliary transistor add the third derivative (g_3) of the drain current to eliminate the distortion. The sign of g_3 changes in its moderate and strong inversion region. This ensures that g_3 is zero with proper biasing, as shown in Figure 1.2 (b). Linearity is improved within a finite bias-

voltage range instead of just one operating point. In this technique, power consumption is very low due to the transistor operating in a weak inversion region in the auxiliary path. Since the positive and negative characteristics of g_3 are not the same, the operating area of g_3 is very narrow with a single auxiliary transistor. However, this area can be expanded by using auxiliary transistors for input impedance matching, noise expression, and gain. This technique is also called the "multi-gate transistor technique" because it works with multiple transistors whose gates are connected in parallel together. Figure 1.2 (a) shows the dual-channel NMOS implementation of the derivative superposition technique. M_A and M_B denote main and auxiliary transistors respectively, and the input matching circuit is excluded for simplicity.

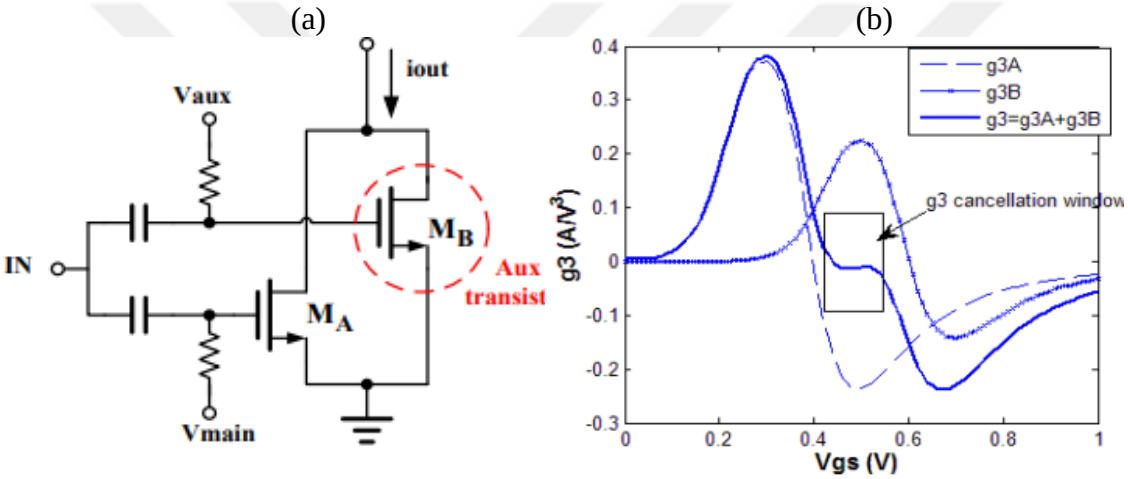
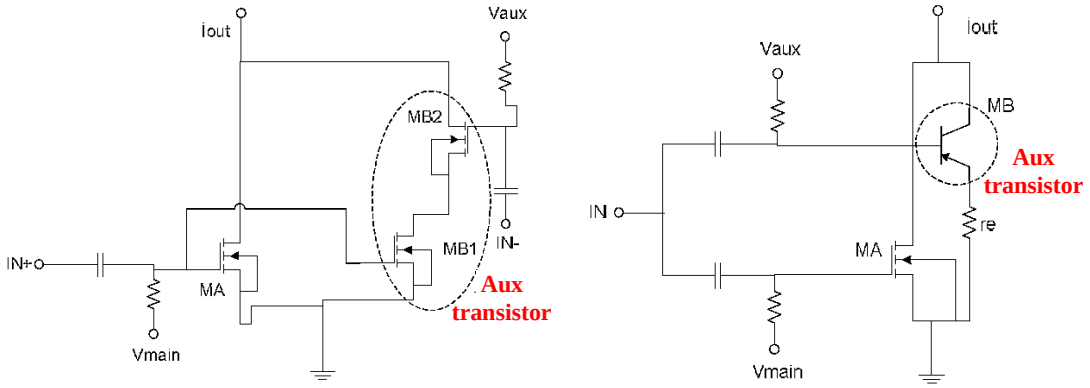


Figure 1.2: (a) Conventional DS topology (b) The graph of the 3^{rd} derivatives (g_3) of drain current from the main and auxiliary transistors [7].

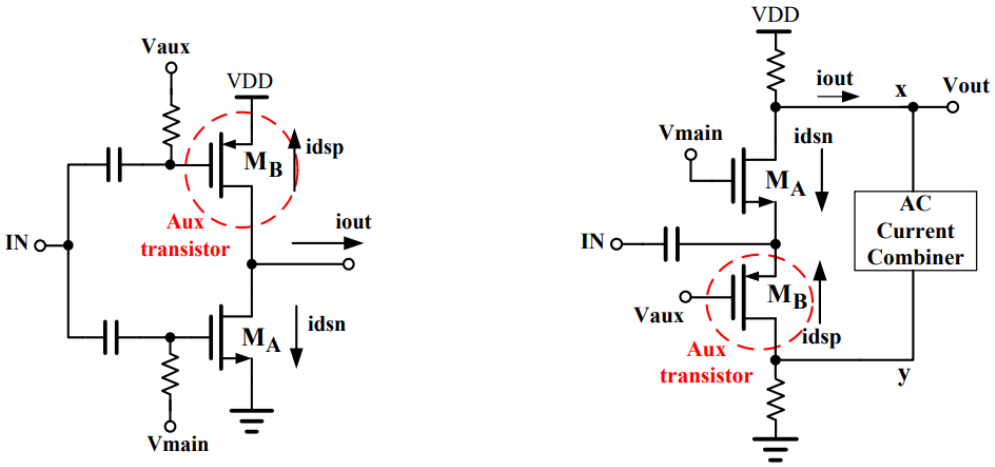
Figure 1.3 (a) and 1.3 (b) show the alternative implementations of the derivative superposition technique using a transistor in the triode region [8] and a BJT [9] as an auxiliary transistors, respectively. In Figure 1.3 (a), transistors M_{B1} and M_{B2} are driven by differential input signals. M_{B1} is biased in the deep triode region and M_{B2} helps to increase the positive peak of g_3 of M_{B1} to effectively eliminate the negative peak of g_3 of the input transistor M_A. In Figure 1.3 (b), M_B provides a positive value of g_3 in the bipolar transistor and the emitter degeneration resistor reduces g_3 to match the M_A for optimum distortion cancellation.



(a) (b)

Figure 1.3: DS technique using a transistor (a) in triode region [8] and (b) BJT [9].

Figure 1.3 shows that the second-order transconductance (g_2) for the transistor operating in the weak or the strong inversion region has a positive sign. Thus, these techniques, such as conventional derivative superposition, often worsen the second-order distortion while improving the third-order distortion. The "complementary derivative superposition technique" uses the NMOS/PMOS pair to improve IIP3 without degrading the value of the second-order intercept point (IIP2) [10,11].



(a) (b)

Figure 1.4: (a) Common-source and (b) common-gate complementary DS topologies [7].

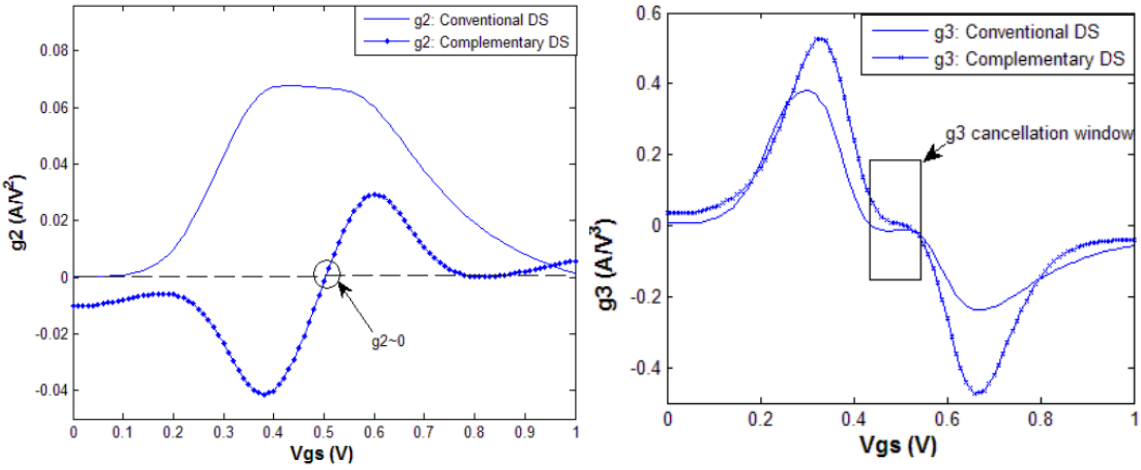
Figure 1.4 shows common-source and common-gate topologies, respectively. Since the input signal for NMOS/PMOS is out of phase, the output current is defined as equation (1.4).

$$i_{dsn} = g_{1A}V_{GS} + g_{2A}{V_{GS}}^2 + g_{3A}{V_{GS}}^3 \quad (1.2)$$

$$i_{dsp} = -g_{1B}V_{GS} + g_{2B}{V_{GS}}^2 - g_{3B}{V_{GS}}^3 \quad (1.3)$$

$$i_{out} = i_{dsn} - i_{dsp} = (g_{1A} + g_{1B})V_{GS} + (g_{2A} - g_{2B}){V_{GS}}^2 + (g_{3A} + g_{3B}){V_{GS}}^3 \quad (1.4)$$

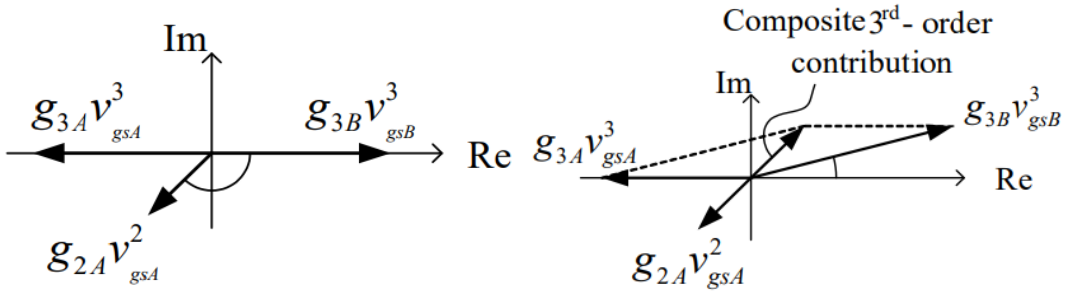
Since g_{2A} and g_{2B} have the same sign, the total transconductance increases, the IM2 term decreases, and because g_{3A} and g_{3B} have different signs, the IM3 term decreases. In Figure 1.5, conventional and complementary derivative superposition are compared in terms of the second (g_2) and the third-order (g_3) distortion of the output current. As shown in Figure 1.5 (b), g_3 becomes zero around 500 mV of V_{GS}, hence third-order distortion is canceled. At this bias point, the value of g_2 for the conventional derivative superposition technique is maximum, while it is approximately equal to zero for the complementary superposition technique. V_{GS} range of complementary derivative superposition, which makes g_3 zero, is narrower compared to conventional derivative superposition. Because PMOS and NMOS have different linearity characteristics, so IIP3 improvement is not as good as in dual channel NMOS implementations. As shown in Equation 1.4, for optimum IIP3 value, the sum of g_{3A} and g_{3B} values should be as close to zero as possible, while for optimum IIP2 value, the sum of g_{2A} and g_{2B} values should be as close to zero as possible. This indicates that there is not the same optimum bias point for IIP2 and IIP3. The differential derivative superposition technique, which alleviates the IIP2 problem, is essentially the same as the complementary derivative superposition [12,13].



(a) (b)

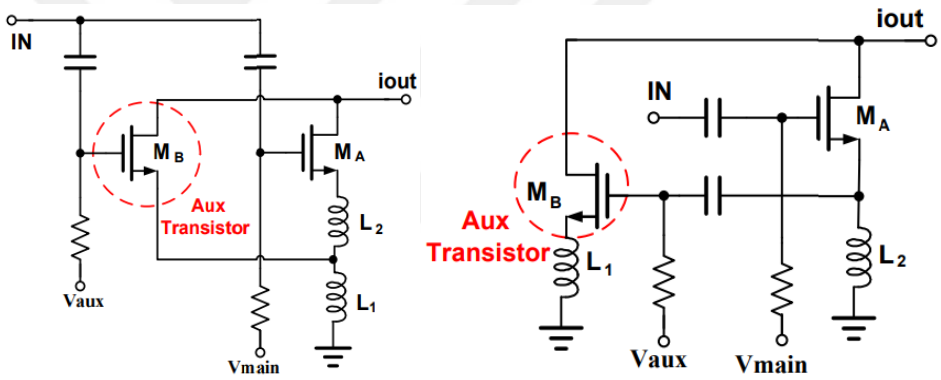
Figure 1.5: Comparison of conventional DS and complemantary DS (a) g_2 vs. V_{GS} (b) g_3 vs. V_{GS} [7].

Modified Derivative Superposition technique is an on-chip solution to minimize source-to-gate feedback. The vector diagram in Figure 1.6 graphically explains the concept of modified derivative superposition. Circuit implementations of the improved TS technique are shown in Figure 1.7. The value of inductances determines the angle of g_{3B}.



(a) (b)

Figure 1.6: The vector diagram of (a) conventional DS and (b) modified DS methods [7].



(a) (b)

Figure 1.7: Modified DS implemantation (a) [14] (b) [15].

Although the channel noise of transistor B in weak inversion is negligible, the gate-source noise of the transistor is inversely proportional to the drain current and added directly to the gate noise of the M_A due to their gates connected each other. M_B also affects input impedance matching. An alternative implementation of the modified DS technique is shown in Figure 1.6 (b). In this topology, the input is not directly applied to the gate of the M_B. It is connected to the source of the M_A via a coupling capacitor. This technique helps to minimize the noise figure and avoid the degradation of the input matching.

The disadvantages of the DS technique should also be considered by the designers. In this technique, the transistor in the weak inversion region may not operate effectively

at high frequencies. It also may not be able to handle large signals. The transistor models operating in weak inversion may be problematic due to the significant discrepancy between simulation and measurement results. Due to the transistors operating in different regions, the linearity improvements change with process voltage temperature (PVT) variations.

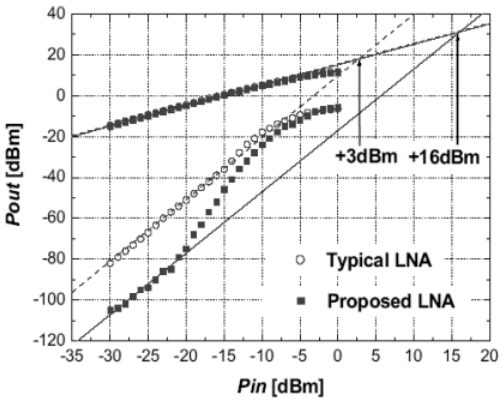


Figure 1.8: IIP3 with/without DS method [7].

A measurement result of the IIP3 is shown in Figure 1.8. Although this result belongs to the conventional DS technique, similar properties can also be observed in the complementary, differential, and modified DS techniques. DS technique works well in the cancellation window of g_3 described in Figure 1.2 (b) and 1.5 ($P_{in} < -20$ dBm). Even if the inputs are outside the distortion window of g_3, the DS method can still pull the third-order tone lower than conventional LNAs where the g_3 of the main transistor is negative as long as the g_3 of the auxiliary transistor remains positive. DS technique does not improve compression point (P1dB) as well.

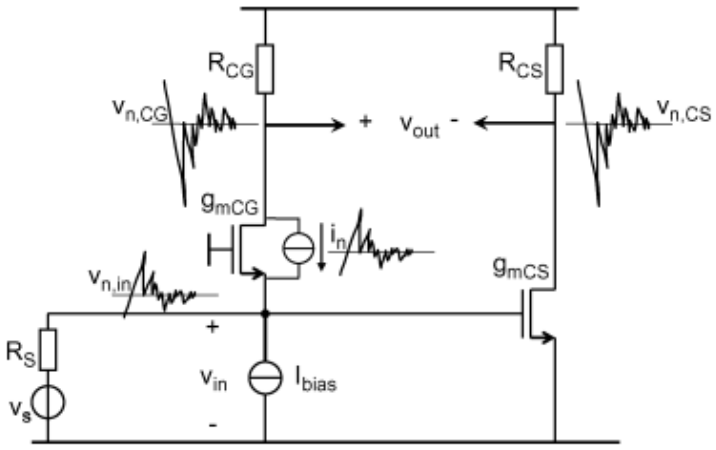


Figure 1.9: Noise cancellation technique in common-source topology using common-gate transistor [16].

Figure 1.9 shows that noise/distortion cancellation is a common-gate (CG) stage parallel to a common-source (CS) stage. The current noise (i_n) generated by the common-gate (CG) transistor causes a voltage noise at the input node ($v_{n,in}$) and the CG output node ($v_{n,CG}$).

$$v_{n,in} = \alpha_1 i_n R_S \tag{1.5}$$

$$v_{n,CG} = -\alpha_1 i_n R_{CG} \tag{1.6}$$

The factor α_1 equals the voltage division between the input resistance ($R_{in,CG}$) and the source resistance (R_S), which equals ½ in the case of impedance matching.

$$\alpha_1 = \frac{R_{in,CG}}{R_{in,CG}+R_S} \tag{1.7}$$

$v_{n,in}$ at the common-source (CS) input multiplied a voltage gain of the CS transistor generates a voltage noise at the CS output node ($v_{n,CS}$).

$$v_{n,CS} = v_{n,in} A_{v,CS} = v_{n,CG} \tag{1.8}$$

As a voltage gain of CS ($A_{v,CS}$) approaches a voltage gain of CG ($-A_{v,CG}$), the noise of the common-mode signal at the differential output is eliminated.

The same mechanism of the noise cancellation at the output utilizes to eliminate distortion components. Voltage variations (v_{gs} and v_{ds}) influence nonlinearly a drain-source current (i_{ds}) of the CG stage. As in the noise cancellation mechanism, a nonlinear voltage at the input (v_{in}) is converted from a nonlinear drain-source current (i_{ds}) generated by source signal (v_s) using the source resistor (R_S). The nonlinear input voltage (v_{in}) can be written as a Taylor expansion of the signal source voltage (v_s) [16].

$$v_{in} = \alpha_1 v_s + \alpha_2 {v_s}^2 + \alpha_3 {v_s}^3 + \alpha_4 {v_s}^4 + \cdots = \alpha_1 v_s + v_{NL} \tag{1.9}$$

where v_{NL} includes all undesirable nonlinear terms and α is Taylor coefficients.

As seen in Fig 1.10, the output voltage of the CG-stage can be written as equation (1.10).

$$v_{out,CG} = i_{in} R_{CG} = \frac{v_s - v_{in}}{R_S} R_{CG} = ((1-\alpha_1)v_s - v_{NL})\frac{R_{CG}}{R_S} \tag{1.10}$$

The output voltage of the CS stage can be written as (1.11).

$$v_{out,CS} = -v_{in}\frac{R_{CG}}{R_S} = -(\alpha_1 v_s + v_{NL})\frac{R_{CG}}{R_S} \tag{1.11}$$

$$v_{out,diff} = v_{out,CG} - v_{out,CS} = v_s\frac{R_{CG}}{R_S} \tag{1.12}$$

In equation 1.12, the unwanted nonlinear signal v_{NL} is canceled at the differential output.

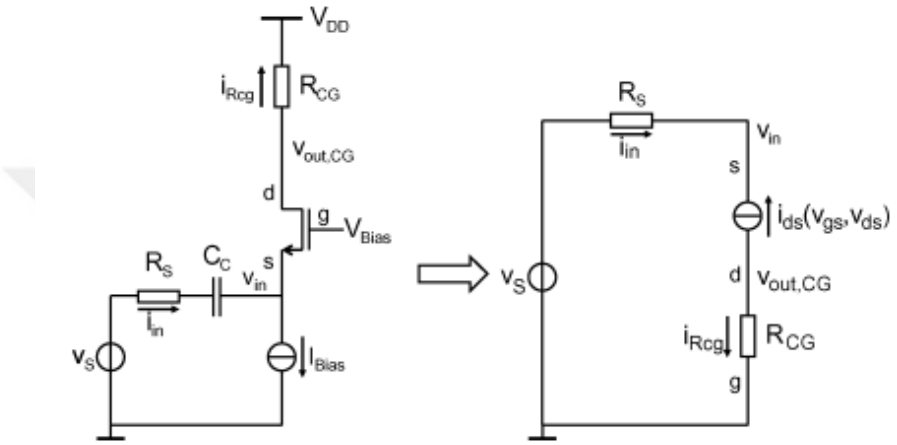


Figure 1.10: Small-signal equivalent of a common-gate transistor [16].

Similar to the derivative superposition technique, the post-distortion technique (PD) benefits from the nonlinearity of the auxiliary transistor to remove the nonlinearity of the main element. The auxiliary transistor is connected to the output of the main transistor instead of directly connected to the input so as to prevent the disturbance of the input matching. Also, the operation of all transistors at saturation provides better linearity. Figure 1.11 illustrates the conceptual idea of the post-distortion technique and the circuit schematics [17−19].

According to Figure 1.11 (b), the nonlinear drain currents of M_1 and M_{1a} can be modeled as follows.

$$i_1 = g_m v_1 + g_2 {v_1}^2 + g_3 {v_1}^3 \tag{1.13}$$

$$i_{1a} = g_{ma} v_2 + g_{2a} {v_2}^2 + g_{3a} {v_2}^3 \tag{1.14}$$

V_2 can be expressed in terms of V_1 as follows.

$$v_2 = b_1 v_1 + b_2 {v_1}^2 + b_3 {v_1}^3 \tag{1.15}$$

$b_1 - b_3$ is usually frequency-dependent. The nonlinear currents of i_1 and i_{1a} is sum up at V_2 and i_{OUT} is obtained.

$$i_2 = i_1 - i_{1a} = (g_m - b_1 g_{ma})v_1 + (g_2 - {b_1}^2 g_{2a} - b_2 g_{ma}){v_1}^2$$

$$+(g_3 - {b_1}^3 g_{3a} - b_3 g_{ma} - 2b_1 b_2 g_{2a}){v_1}^3 \qquad (1.16)$$

$(g_2 - {b_1}^2 g_{2a} - b_2 g_{ma}){v_1}^2$ and $(g_3 - {b_1}^3 g_{3a} - b_3 g_{ma} - 2b_1 b_2 g_{2a}){v_1}^3$ expressions represent the second and third-order distortion of the output current, respectively. The third-order distortion expression should be closer to zero to obtain high linearity.

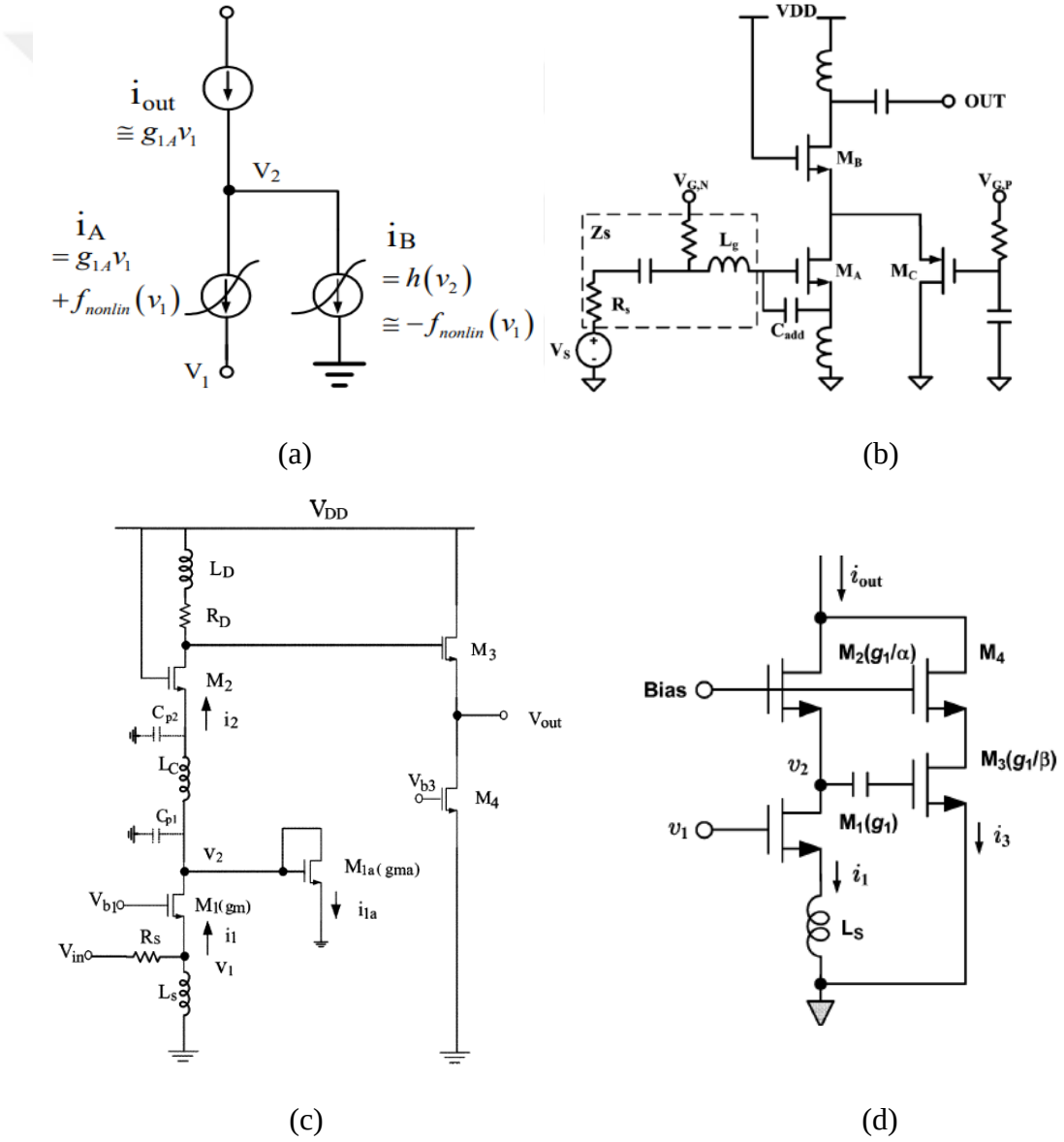


Figure 1.11: (a) The conceptual idea of the post-distortion technique [17] and circuit implemantiton (b) [18] (c) [17] (d) [19].

1.3 Contribution of the Thesis and its Organization

LNA linearity indirectly depends on power consumption. This thesis shows that IIP3 performance is improved without increasing power consumption (LNA1 and LNA2). However, taking into consideration NF and gain limitations, more power has to be delivered to LNA. In this thesis, LNA3 and LNA4 topologies demonstrate that the performance of LNA can be preserved and enhanced by keeping the constant power consumption. The design of this LNA presents a perspective on the sub-mW power CMOS LNA design with a 40 nm technology. A 2.4 GHz, 10 dB voltage gain, 3.88 dB noise figure, 2.19 dBm IIP3 low noise amplifier is designed with a power budget of 989.6 μW. The designed LNA yields good performance compared to its counterparts.

Chapter 1 introduces the role of LNAs in receiver systems and their design requirements. The challenges of ultra-low-power LNAs are discussed. Also, the linearity improvement techniques are mentioned. Finally, it presents the novelty of this study and its contribution to the literature.

Chapter 2 explains the design parameters such as noise, input and output matching, gain, and linearity.

Chapter 3 starts the noise, input matching and gain theories about classical cascode LNA with inductive degeneration. It includes the design procedure of an ultra-low-power 2.4 GHz CMOS cascode low noise amplifier with high linearity.

Chapter 4 discusses simulation results and compares the proposed LNAs and clearly explains the drawbacks and benefits of the proposed LNA designs.

Chapter 5 presents the conclusion of the thesis and the novelty of this study.

2. STATE OF ART

2.1 Design Parameters

2.1.1 Noise

Noise is the distortion of the signal processed by an amplifier. Signal to noise ratio is defined as the ratio between the average signal power and the average signal noise, which provides information about signal quality [20]. The noise of sources caused by electronic components consists of the thermal noise, which is also known as Johnson-Nyquist noise, the shot noise, and the flicker noise. The random motion of charge carriers results in thermal noise. It is the main noise for the CMOS LNA design. The shot noise resulted from pn junctions is based on DC bias current. The shot noise mainly occurs LNA design utilized Bipolar junction transistors (BJT). The flicker noise known as $1/f$ noise stems from the traps in the semiconductor. The flicker noise influences both bipolar and MOSFET transistors. The quality of the conductive medium is determined by the flicker noise due to macroscopic defects of materials. The flicker noise occurs with the trapping and releasing of the charge carriers in the impurities and defects of the MOS channel region. The larger gate capacitance reduces the fluctuations in the channel charge, so the flicker noise is exhibited in the larger MOS devices. As seen in Figure 2.1, the power spectral density of the flicker noise is inversely proportional to the frequency. While the flicker noise is more dominant than thermal noise for low frequencies, it can be neglected at high frequencies, which is over the corner frequency ($1/f$). The noise performance of the LNA is not contributed by the flicker noise at the linear operation region since LNAs mostly operate at higher frequencies than corner frequency which is in the range of the megahertz [21].

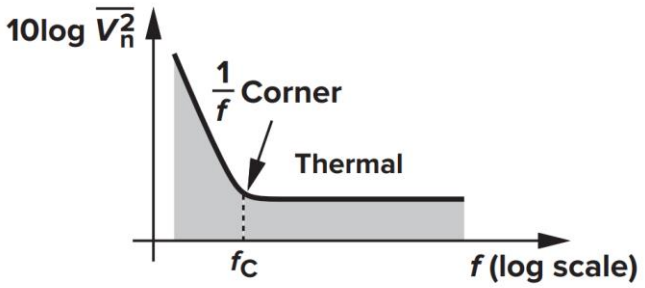


Figure 2.1: Flicker noise corner frequency f_C [20].

2.1.1.1 Resistors

The resistor is the major source of thermal noise which depends on temperature because charge carriers are vibrated only temperature change. The noise power is related to bandwidth. A generalized equation of the is noise voltage within a given bandwidth can be defined as shown in equation 2.1.

$$V_n{}^2 = 4kT \int_{f1}^{f2} R\, df \tag{2.1}$$

where V_n is noise voltage integrated RMS voltage between frequencies f_1 and f_2, R is resistive component of the impedance (or resistance) Ω, T is the temperature in degrees Kelvin, f_1 and f_2 are lower and upper limits of required bandwidth, k is the Boltzmann's constant ($1.38 \times 10^{-23} JK^{-1}$) [20]. For most cases, the resistive component of the impedance will remain constant over the required bandwidth. Therefore, equation (2.1) can be simplified into equation (2.2).

$$V_n = 4kTR \tag{2.2}$$

The noise can be modeled as a current source, $I_n{}^2(f)$, as illustrated in Figure 2.2.

$$I_n{}^2(f) = \frac{4kT}{R} \tag{2.3}$$

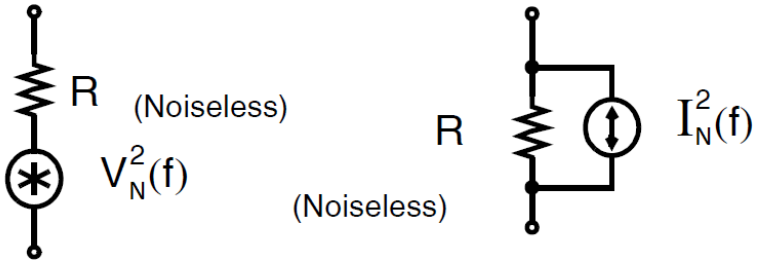


Figure 2.2: Noise model of a resistor [21].

2.1.1.2 MOSFETs

MOSFET transistors mainly produce two different types of noise: thermal and flicker noise. Flicker noise dominates the noise spectrum at a frequency which is lower than corner frequency (f_C). Otherwise, thermal noise is dominant.

The flicker noise can be modeled as a voltage source in series with the gate.

$$V_g{}^2(f) = \frac{K}{WLC_{OX}f} \tag{2.4}$$

The flicker noise can be modeled as a current source between source and drain.

$$I_g{}^2(f) = \frac{Kg_m{}^2}{WLC_{OX}f} \tag{2.5}$$

where K is a device-specific constant. The variables W, L, g_m, and C_{ox} represent the transistor's width, length, transconductance, and gate capacitance per unit area, respectively [21]. The thermal noise in MOSFET transistors operating in the saturation region can be modeled as a current source tied between drain and source terminals, as shown in Figure 2.3.

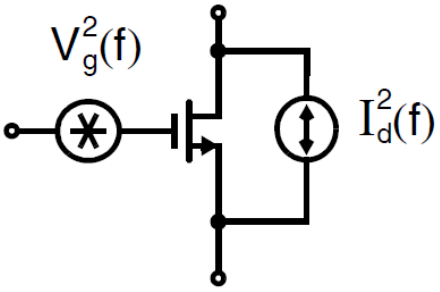


Figure 2.3: Noise model of a transistor [21].

Power spectral density (PSD) value is given in 2.6.

$$I_d{}^2 = 4kT\gamma g_m \tag{2.6}$$

where γ is the noise coefficient which is $2/3$ for long channels and 2 for short-channel transistors.

2.1.1.3 Capacitors and inductors

Ideal capacitors and inductors are lossless circuit elements. Therefore, they can be considered noise-free components. Generally, capacitors are utilized to filter the noise. Ohmic losses of the capacitors cause thermal noise generation. Some types of capacitors, such as stacked-foil film and ceramic, which have a typical equivalent series resistance (ESR) value less than 0.015 Ω, are very low ohmic losses. Such capacitors have excellent noise performance. Certain capacitor types are sensitive to vibrations. Especially mechanical vibrations lead to modify the distance between elements or generated unwanted charge flow. Consequently, this phenomenon produces noise. Besides the ESR value of a capacitor, its equivalent series inductance ESL affects the noise level of the capacitor. The lower the ESL, the lower the noise. The quality factor (Q) of an inductor determines its noise performance. Compared to other types of inductors, ferrite beads have characteristics of higher resistance and low-quality factor. Ferrite beads can be used in noise reduction due to this property. Like capacitors, filtering by using inductors reduce the noise [21].

2.1.1.4 Noise figure (NF)

The noise figure (NF) is a measure of the amount of noise added to the signal by the circuit components and measured on a dB scale. On the other hand, the noise factor (F) is the value of NF on a linear scale and is defined as the ratio between the SNR_{out} and SNR_{in} of the circuit component [20]. Noise figure can be expressed as in 2.7.

$$NF = 10logF \tag{2.7}$$

The noise factor (F) of an LNA can be shown as in 2.8.

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{{}^{S_i}/_{N_i}}{{}^{S_o}/_{N_o}} = \frac{S_i}{N_i} \times \frac{G \times N_i + N_a}{G \times S_i} = 1 + \frac{N_a}{G \times N_i} \tag{2.8}$$

where SNR is the signal-to-noise ratio, S_i and S_o are signal levels available at the input and output, N_i and N_o are noise levels available at input and output, N_a is an additional noise signal and G is the network gain.

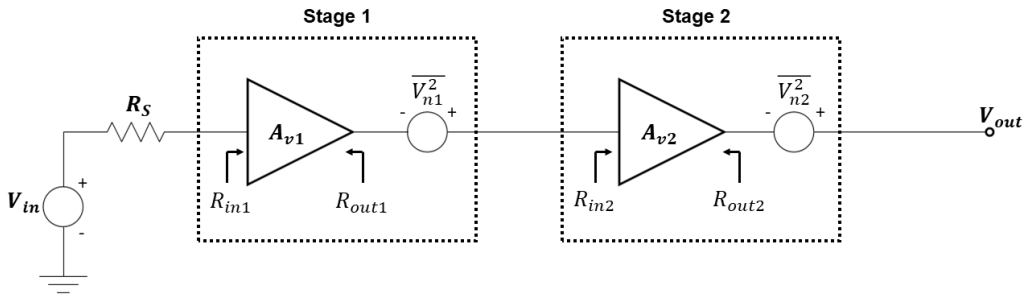


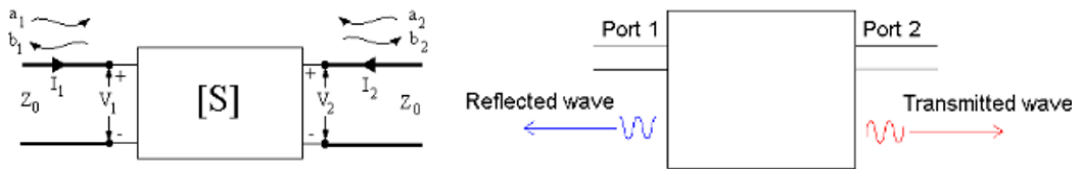
Figure 2.4: Noise in a cascade of stages [20].

For a cascade system of N stages, as shown in Figure 2.4, the overall noise factor can be expressed in terms of the noise factor and gain of each stage. The total noise factor can be obtained by Friis's equation as in 2.9.

$$F_{sys} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_N - 1}{G_1 G_2 \cdots G_{N-1}} \tag{2.9}$$

2.1.2 S-parameters

Scattering parameters known as s-parameters give information about traveling waves. These waves are transmitted and reflected with an introduced nport network to the transmission line [22]. S-parameters are a common way to introduce nport network. While the voltage and current at the terminal change along the transmission line, the traveling waves are not influenced in comparison to the magnitude at the terminal. The 2-port network is used to define S-parameters, as shown in Figure 2.5.



(a) (b)

Figure 2.5: 2-port network with transmitted waves (a_1, a_2) and reflected waves (b_1, b_2) used in S-parameters definition.

The voltages and currents in the 2-port network are divided into transmitted and reflected ones.

$$V(x) = V^+(x) + V^-(x) \tag{2.10}$$

$$V^+(x) = Ae^{-j\beta x} \quad ; \quad V^-(x) = Be^{j\beta x} \tag{2.11}$$

$$I_x = \frac{1}{Z_o}[V^+(x) - V^-(x)] \tag{2.12}$$

The reflection coefficient can be expressed as equation (2.13).

$$\Gamma(x) = \frac{V^-(x)}{V^+(x)} \tag{2.13}$$

Transmitted and reflected voltages are normalized with normalized impedance. Normalized impedance is usually chosen the same as the characteristic impedance.

$$v(x) = \frac{V(x)}{\sqrt{Z_o}} \quad ; \quad i(x) = \sqrt{Z_o} I(x) \tag{2.14}$$

$$a(x) = \frac{V^+(x)}{\sqrt{Z_o}} \quad ; \quad b(x) = \frac{V^-(x)}{\sqrt{Z_o}} \tag{2.15}$$

$$v(x) = a(x) + b(x) \tag{2.16}$$

a and b are the normalized transmitted and reflected voltages, respectively.

For 1-port system, the reflected voltage can be expressed as equation (2.17).

$$b(x) = \Gamma(x) a(x) \tag{2.17}$$

For 2-port system, the reflected voltages can be expressed as equation (2.18).

$$b_1 = s_{11} a_1 + s_{12} a_2 \tag{2.18}$$

$$b_2 = s_{21} a_1 + s_{22} a_2 \tag{2.19}$$

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.20}$$

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \qquad S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \tag{2.21}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \qquad S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \tag{2.22}$$

S-parameters S_{11} and S_{22} are identical to optical reflection coefficients; S_{12} and S_{21} are identical to optical transmission coefficients. Overall, S-parameters help designers to predict circuit behavior in terms of the desired performance.

2.1.3 Network gain

The available and maximum power that can be delivered to the load is represented input power KGT_0B. The input mismatch leads to loss of transferred power since the network gain depends on input matching. Also, network gain is essential for the noise figure, as seen in (2.8). The reflection coefficient ($\Gamma_{in}, \Gamma_s, \Gamma_{out}, \Gamma_L$) shown in Figure 2.6 is used power, transducer, available gain, and insertion gain [23].

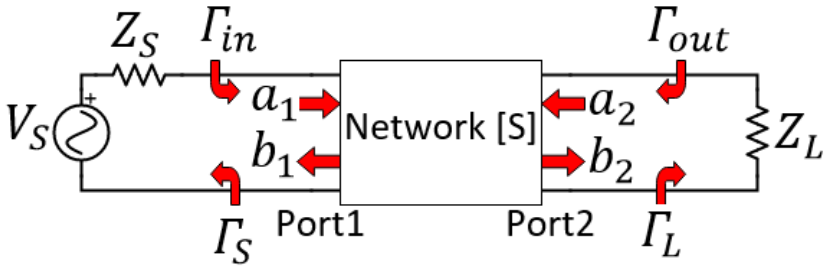


Figure 2.6: For a 2-port network, the input and output traveling waves are measured in a Z_0 system [23].

Consider a network with the source and load reflection coefficients Γ_S and Γ_L measured in a Z_0 system (assuming $Z_0 = 50\ \Omega$ in RF circuits) as illustrated in Figure 2.7.

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} \tag{2.23}$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.24}$$

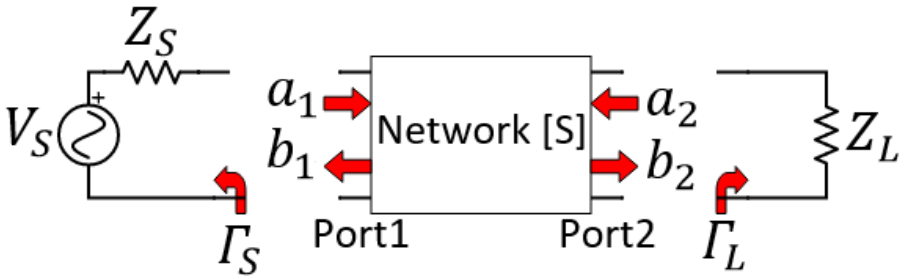


Figure 2.7: The reflection coefficients, Γ_S and Γ_L, are measured separately [23].

The Γ_{in} and Γ_{out} can be expressed as in 2.25 and 2.26, respectively.

$$\Gamma_{in} = \frac{b_1}{a_1} = s_{11} + \frac{s_{12}s_{21}\Gamma_L}{1 - s_{22}\Gamma_L} \tag{2.25}$$

$$\Gamma_{out} = \frac{b_1}{a_2} = s_{22} + \frac{s_{12}s_{21}\Gamma_S}{1 - s_{11}\Gamma_S} \tag{2.26}$$

2.1.3.1 Power gain (G_P)

Power gain (G_P) is the ratio of the power delivered to the load (P_L) to the power delivered to the network from the source (P_{in}) as illustrated in Figure 2.8 [23].

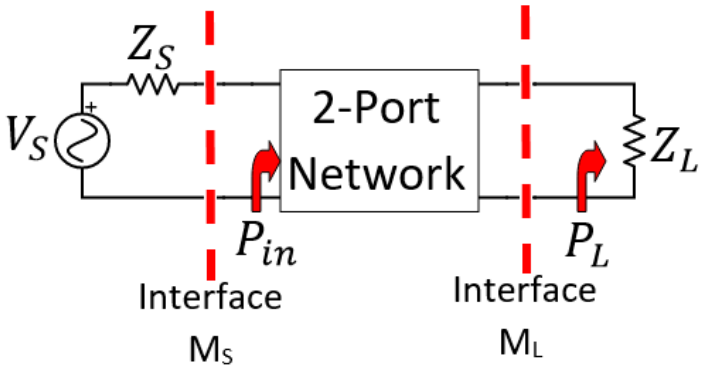


Figure 2.8: 2-port network indicates that the G_P is obtained from the network input to the load [23].

$$G_P = \frac{P_L}{P_{in}} \tag{2.27}$$

The P_L and P_{in} can be written in terms of Γ_L and Γ_{in} as in 2.28 and 2.29.

$$P_L = \frac{1}{2}|b_2|^2(1 - |\Gamma_L|^2) \tag{2.28}$$

$$P_{in} = \frac{1}{2}|a_1|^2(1 - |\Gamma_{in}|^2) \tag{2.29}$$

where $b_2 = \frac{S_{21}a_1}{1-S_{22}\Gamma_L}$, so G_P can be expressed as in 2.30.

$$G_P = \frac{1}{1-|\Gamma_{in}|^2}|s_{21}|^2\frac{1-|\Gamma_L|^2}{|1-s_{22}\Gamma_L|^2} \tag{2.30}$$

2.1.3.2 Transducer gain (G_t)

The transducer gain (G_t) is the ratio of the power delivered to the load (P_L) to the maximum power available from the source (P_{as}) as shown in Figure 2.9. An interface (M_s) known as the source mismatch factor between the source and network input is defined as the ratio of the power delivered to the network from the source (P_{in}) to the maximum power available from the source (P_{as}).

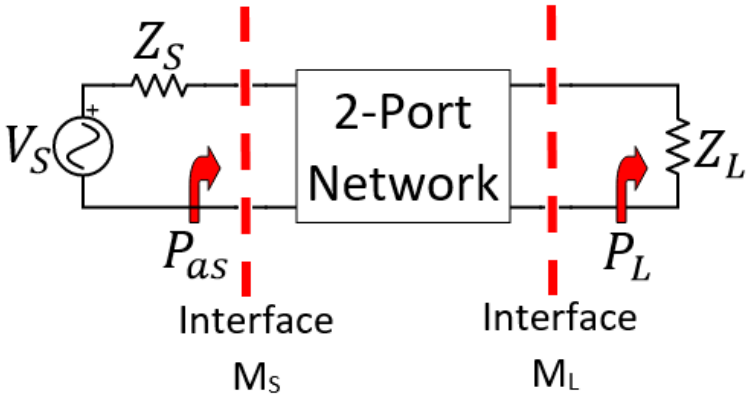


Figure 2.9: 2-port network indicates that the G_t is obtained from the source to the load [23].

$$M_s = \frac{P_{in}}{P_{as}} = \frac{(1-|\Gamma_s|^2)(1-|\Gamma_{in}|^2)}{|1-\Gamma_s\Gamma_{in}|^2} \tag{2.31}$$

$$G_t = \frac{P_L}{P_{as}} = \frac{P_L}{P_{in}}\frac{P_{in}}{P_{as}} = G_P M_s \tag{2.32}$$

$$G_t = \frac{1-|\Gamma_s|^2}{|1-s_{11}\Gamma_s|^2}|s_{21}|^2\frac{1-|\Gamma_L|^2}{|1-\Gamma_{out}\Gamma_L|^2} \tag{2.33}$$

2.1.3.3 Available gain (G_a)

The available gain (G_a) is the ratio of the available power of network output (P_{ao}) to the maximum power available from the source (P_{as}) as shown in Figure 2.10. An interface (M_L) known as the load mismatch factor between the network output and the load is defined as the ratio of the power delivered to the load (P_L) to the available power of network output (P_{ao}) [23].

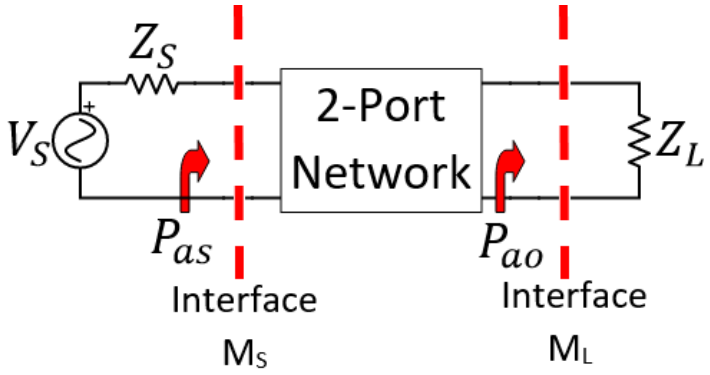


Figure 2.10: 2-port network indicates that the G_a is obtained from the source to the network output [23].

$$M_L = \frac{P_L}{P_{ao}} = \frac{(1-|\Gamma_L|^2)(1-|\Gamma_{out}|^2)}{|1-\Gamma_{out}\Gamma_L|^2} \quad (2.34)$$

$$G_a = \frac{P_{ao}}{P_L} = \frac{P_L}{P_{as}}\frac{P_{ao}}{P_L} = \frac{G_t}{M_L} \quad (2.35)$$

$$G_a = \frac{1-|\Gamma_s|^2}{|1-s_{11}\Gamma_s|^2}|s_{21}|^2\frac{1}{1-|\Gamma_{out}|^2} \quad (2.36)$$

2.1.4 Linearity

The aim of obtaining high linear systems is to avoid producing harmonic distortion or intermodulation distortion. Ideally, a linear amplifier is expected to amplify the frequency components that make up the input signal with the same gain. This means that an output of an ideal linear amplifier exactly replicates the waveform of an input signal. Due to the nature of the transistors, which have nonlinear $I_D - V_{GS}$ characteristics, linearity cannot be achieved perfectly. Linearity is one of the most critical performance metrics for LNA. Two main parameters are used to measure the linearity of LNA: 1-dB compression point (P_{1dB}) and third-order intercept point (IP3).

2.1.4.1 1-dB compression point (P_{1dB})

When a sinusoid input signal is applied to a non-linear system as in 2.37, an input-output relation is illustrated in 2.38.

$$x(t) = A\cos(\omega t) \quad (2.37)$$

$$y(t) = a_1 A\cos(\omega t) + a_2 A^2[\cos(\omega t)]^2 + a_3 A^3[\cos(\omega t)]^3 \quad (2.38)$$

$$y(t) = \frac{a_2 A^2}{2} + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos(\omega t) + \frac{a_2 A^2}{2}\cos(2\omega t) + \frac{a_3 A^3}{4}\cos(3\omega t) \quad (2.39)$$

$\cos(\omega t)$ is the desired signal and others are called harmonic distortion. If $a_1 a_3 < 0$, the circuit has the compressive characteristics that are more suitable for LNA [20].

2.1.4.2 Third order intercept point (IP3)

When two signals with different frequencies (also known as “two-tones”) are applied to a nonlinear system, many undesired components will be produced at the output because of the harmonics and intermodulation of these two signals. If these components are very close to the desired signal, as in Figure 2.11, they are called

intermodulation (IM). If one of the IM products is produced in the band of interest, the desired signal is degraded.

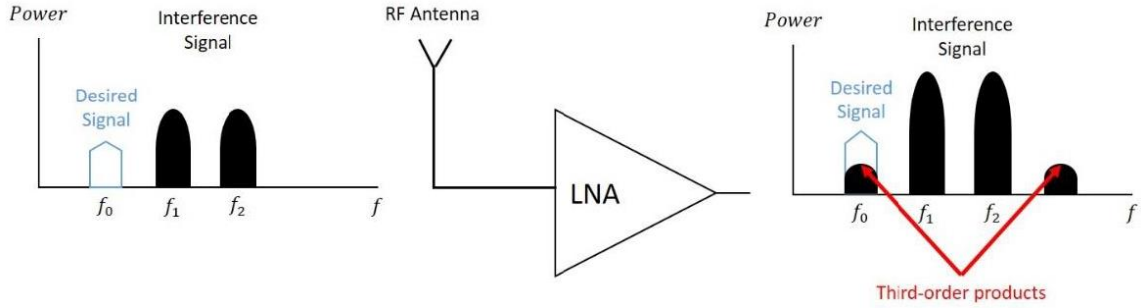


Figure 2.11: Corruption due to third-order intermodulation [20].

Assume that the two-tones input signal is $x(t) = A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)$. The output of the system will be as equation (2.40).

$$y(t) = a_1(A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t)) + a_2(A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t))^2 + a_3(A_1 \cos(\omega_1 t) + A_2 \cos(\omega_2 t))^3 \quad (2.40)$$

Intermodulation products can be obtained using equation (2.40).

$$\omega = \omega_1 \pm \omega_2 : \; a_2 A_1 A_2 \cos(\omega_1 + \omega_2)t + a_2 A_1 A_2 \cos(\omega_1 - \omega_2)t \quad (2.41)$$

$$\omega = 2\omega_1 \pm \omega_2 : \; \frac{3a_3 {A_1}^2 A_2}{4} \cos(2\omega_1 + \omega_2)t + \frac{3a_3 {A_1}^2 A_2}{4} \cos(2\omega_1 - \omega_2)t \quad (2.42)$$

$$\omega = 2\omega_2 \pm \omega_1 : \; \frac{3a_3 {A_2}^2 A_1}{4} \cos(2\omega_2 + \omega_1)t + \frac{3a_3 {A_2}^2 A_1}{4} \cos(2\omega_2 - \omega_1)t \quad (2.42)$$

Fundamental components are given as equation (2.43).

$$\omega = \omega_1, \omega_2 : \left(a_1 A_1 + \frac{3}{4} a_3 {A_1}^3 + \frac{3}{2} a_3 {A_1}^2 A_2\right) \cos \omega_1 t + \left(a_1 A_2 + \frac{3}{4} a_3 {A_2}^3 + \frac{3}{2} a_3 {A_2}^2 A_1\right) \cos \omega_2 t \quad (2.43)$$

As shown in Figure 2.12, if $f_2 - f_1$ is small, the third-order IM products at $2f_1 \pm f_2$ and $2f_2 \pm f_1$ is very close to f_1 and f_2, so these products cause nonlinearities.

As illustrated in Figure 2.13, the linear parts of the two gain curves interpolated so that the first-order (or fundamental) and the third-order signal will intersect at the IP3. The IP3 is where the first-order input is equal to the third-order input The corresponding

input and output are called the third-order input intercept point (IIP3) and third-order output intercept point (OIP3) [20].

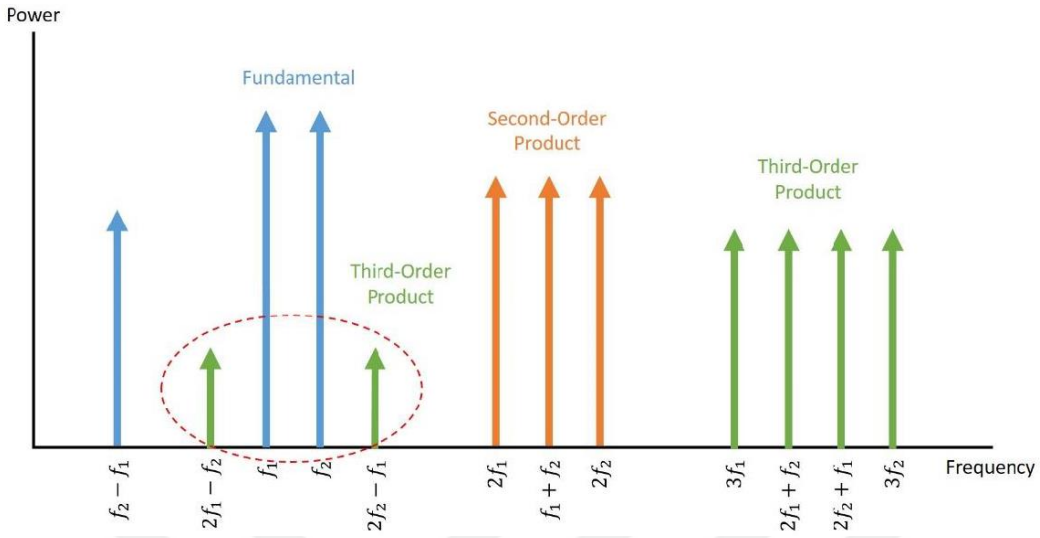


Figure 2.12: Two input signals, f_1 and f_2, amplified by an amplifier that produces the second and third harmonics [20].

$$|a_1 P_{IIP3}| = \left|\frac{3a_3 {P_{IIP3}}^3}{4}\right| \tag{2.44}$$

$$P_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|} \tag{2.45}$$

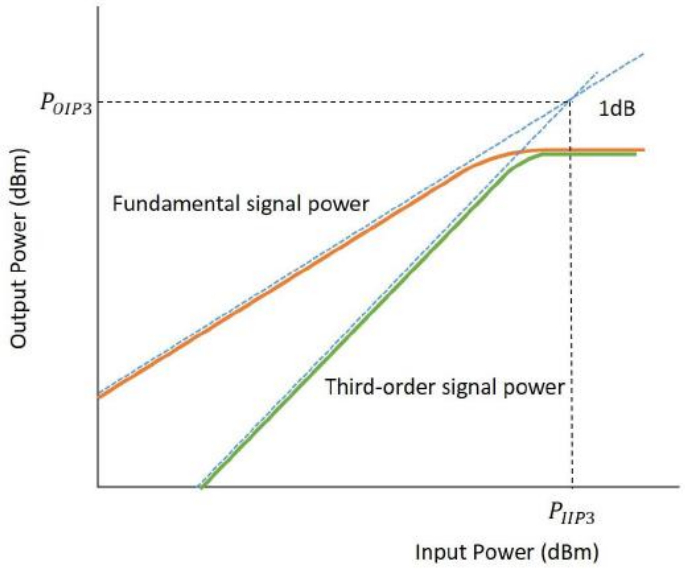


Figure 2.13 The IP3 is a theoretical point at which the third-order distortion signal amplitudes equal the input signals [20].

3. LOW NOISE AMPLIFIER DESIGN

3.1 Theory of a Cascode LNA

3.1.1 The noise figure of a cascode LNA

The noise figure of the conventional cascode LNA in Fig. 3.1 is given in 3.1.

$$NF \cong 1 + \frac{R_l}{R_S} + \frac{R_g}{R_S} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_0}{\omega_T}\right) \tag{3.1}$$

where γ is the coefficient of channel thermal noise and α is one for long-channel devices while it is less than one for short-channel devices [24].

$$\chi = 1 + 2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1 + {Q_L}^2) \tag{3.2}$$

where δ is the coefficient of gate noise, and c is the correlation coefficient between drain and gate noise.

$$Q_L = \frac{\omega_0(L_S + L_g)}{R_S} = \frac{1}{\omega_0 R_S C_{gs}} \tag{3.3}$$

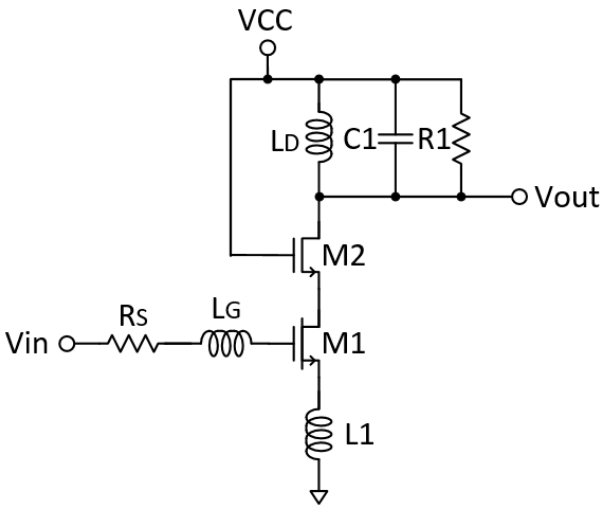


Figure 3.1: Classical cascode LNA with inductive degeneration.

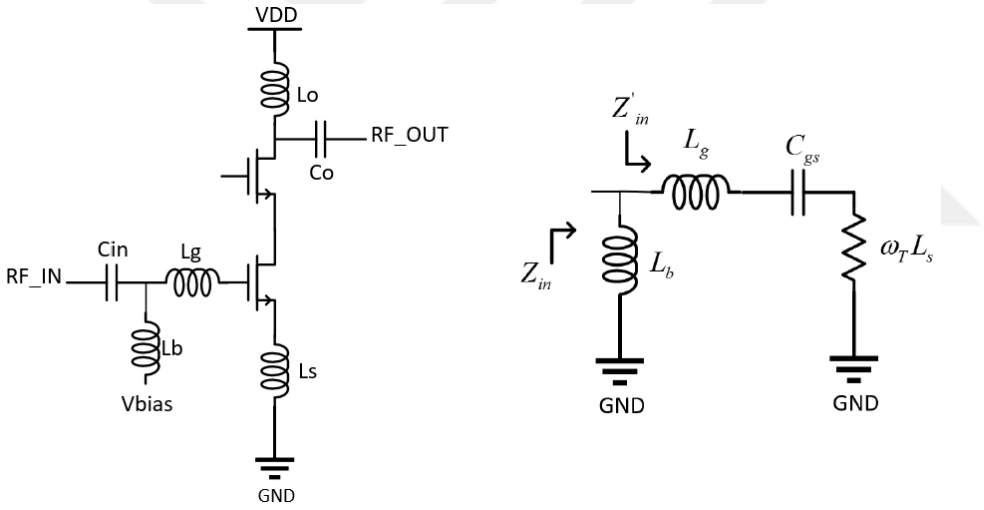
In equation 3.1, R_l is the gate resistance of M_1 depends on the quality factor L_G. If an inductor with a high value is used to provide input matching, R_l/R_S can be a dominant noise figure. According to equation (3.1), larger transconductance decreases NF due to $\omega_T = g_{m1}/C_{gs1}$.

3.1.2 Input power matching of LNA

As shown in Figure 3.2 (a), an inductance L_b is used to obtain a better input match and a higher gain. Shunt inductance L_b in Figure 3.2 (b) provides to achieve a higher Z_{in} with lower $\omega_T L_S$, which is illustrated in 3.4 and 3.5.

$$Z'_{in} = s(L_S + L_g) + \frac{1}{sC_{gs}} + (\frac{g_m}{C_{gs}})L_s \tag{3.4}$$

$$Z_{in} = \frac{Z'_{in} sL_b}{Z'_{in} + sL_b} \tag{3.5}$$



(a) (b)

Figure 3.2: (a) Cascode LNA with inductive degeneration and inductive bias. (b) Input matching circuit.

3.1.3 Gain of a cascode LNA

The voltage gain of an LNA is given equation (3.6) is the multiplication of equivalent transconductance and output resistance [20].

$$A = G_m R_L \tag{3.6}$$

$$G_m = \frac{\omega_T}{2\omega_0 R_S} \tag{3.7}$$

where $R_S = (g_{m1}L_S)/C_{GS}$. This means that the input impedance is matched to the output impedance of the input source. Also, output resistance must be 50 Ω for a voltage gain due to measurement using a probe station. As clearly seen in 3.8, the gain is increased with reducing L_S.

$$A = \frac{\omega_T R_L}{2\omega_0 R_S} \tag{3.8}$$

where

$$\boldsymbol{\omega_0 = \sqrt{\frac{1}{(L_1+L_G)C_{GS}}}} \tag{3.9}$$

3.2 LNA Design Procedure

Four low-power LNA topologies have been presented in this work. The first design, which is a cascode CS-LNA has a high voltage gain and low IIP3 figure, whereas, through linearity-improving techniques, the second design yields better IIP3 performance. However, the voltage gain is significantly decreased when IIP3 goes up. To increase the gain, a third topology has been developed without degrading the IIP3 performance. The difference between the third and last LNA circuits resides in whether L_g is included on the chip or not.

Comparing all LNA circuits, there is no significant change in the noise figure for all LNAs, and IIP3 is significantly improved in all of them except the first one. The voltage gain of the last two LNAs is higher than the second one, while they are slightly lower than that of the first LNA. The cascode CS LNA with high linearity is designed in Figure 3.3, with versions of L_g being on and off-chip. The aim of the off-chip L_g is to obtain a high-quality factor, thereby reducing the occupied chip estate.

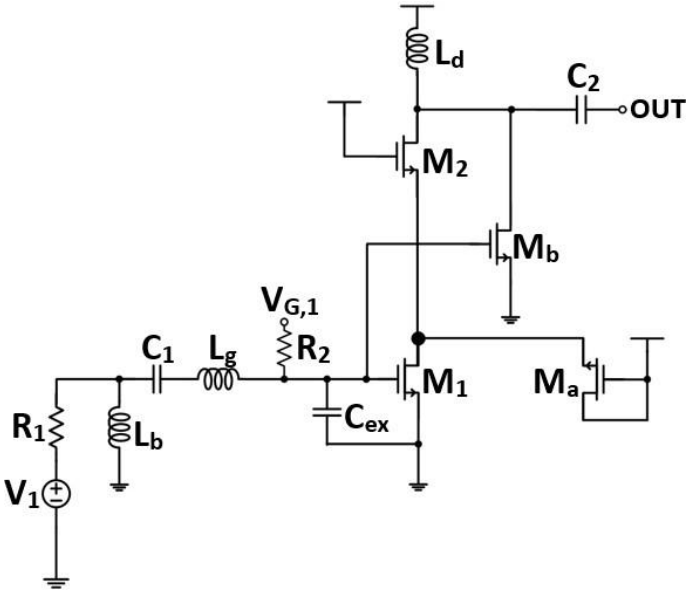


Figure 3.3: The schematic of the proposed LNA (adopted in LNA3 and LNA4) with improved linearity and gain.

Input matching is important for the noise figure. Also, additional inductance L_b improves input matching. Figure 3.4 shows that L_g = 2.2 nH and L_b = 750 pH (drawn with the black line), provides best S_{11} value at 2.4 GHz. If we check the noise figure of the LNA with these values, it is seen in Figure 3.5 that these inductor values also provide a reasonable noise figure. L_g = 2.2 nH and L_b = 750 pH enable S_{11} to be lower than −10 dB and realize NF = 3.87 dB.

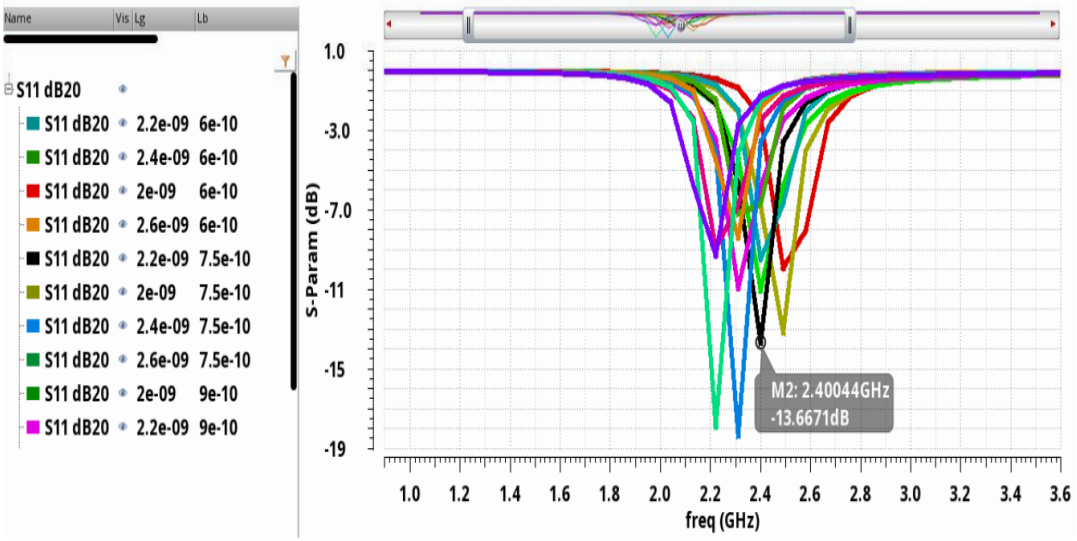


Figure 3.4: S_{11} vs. frequency for different L_g and L_b values.

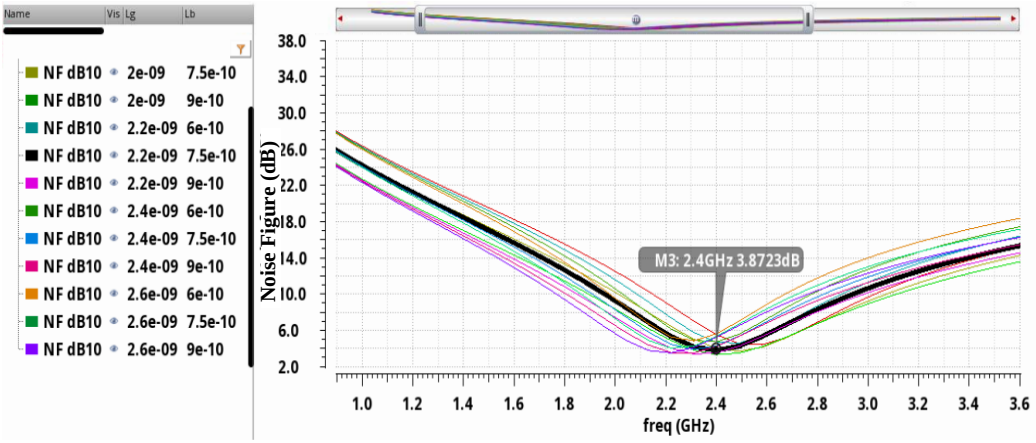


Figure 3.5: NF vs. frequency for different L_g and L_b values.

As transistor channel lengths (L) are scaled-down, gate-to-source capacitances (C_{GS}) become smaller. Thus, C_{GS} depends on the width of transistors at the constant L. Also, the larger gate width of the CS transistor (M_1) provides to improve NF and IIP3 while it leads to increase power consumption. As illustrated in Figure 3.3, an additional capacitance (C_{ex}) is connected between the gate and source of M_1 transistor for NF matching due to power limitation. Minimum NF is obtained only at a matching point. As seen in Figure 3.6, an additional capacitance (C_{ex}) enables better input matching with increasing C_{GS}. Thus, additional C_{GS} shifts the frequency where NF is minimum owing to input matching. Figure 3.7 demonstrates that C_{GS} improves NF although increasing C_{GS} degrades minimum NF according to equation (3.1).

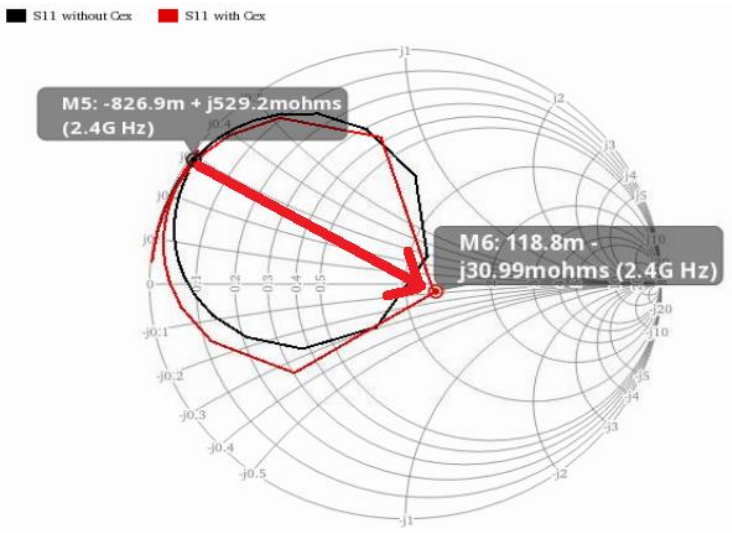


Figure 3.6: S_{11} without and with C_{ex} on Smith Chart.

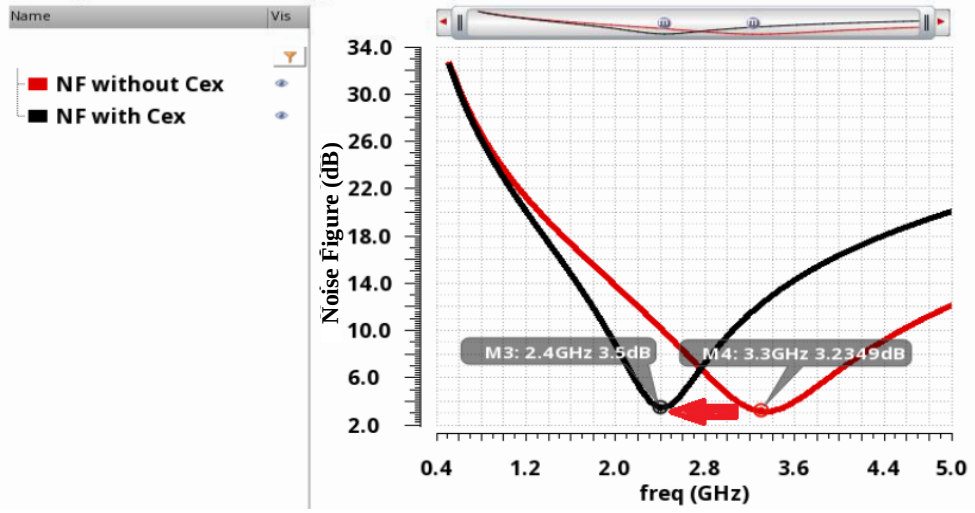


Figure 3.7: NF without and with C_{ex}.

M_b is directly connected to the input, so we must check the stability. The conditions for unconditional stability in terms of S-parameters [25] are shown in 3.10 and 3.11.

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{3.10}$$

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|S_{11}S_{22}-S_{12}S_{21}|^2}{2|S_{12}S_{21}|} > 1 \tag{3.11}$$

In Figure 3.8, Kf and $B1f$ values which refer to K and $|\Delta|$ are 3.24 and 0.162 at 2.4 GHz, respectively. Thus, M_b does not degrade the stability of LNA.

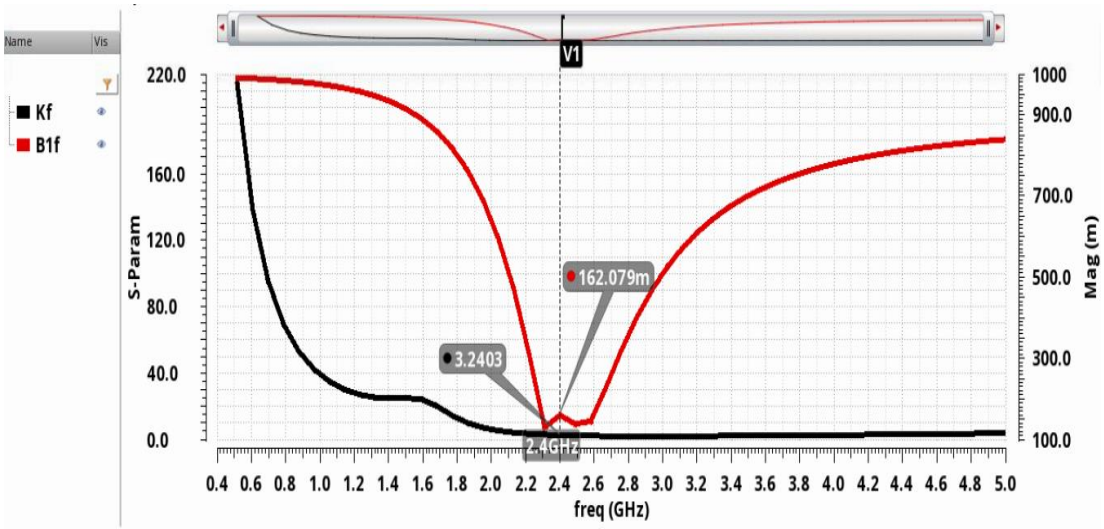


Figure 3.8: K and $|\Delta|$ values for the stability of LNA.

In addition, M_1 is the main transistor and the diode-connected transistor M_a is used to cancel the third-order intermodulation distortion (IMD3), as shown in Figure 3.9. Also, i_2 can be expressed as equation (3.12).

$$i_2 = i_1 - i_a \tag{3.12}$$

where i_1, i_2 and i_a are the drain currents of M_1, M_2, and M_a, respectively.

A major source of IMD3 is the third-order nonlinearity of M_1 since the nonlinear current generated in M_1 is fully transferred to M_2 which acts as a current buffer. If the drain of M_1 has an additional current path that selectively cancels to the IMD3 current component, less IMD3 current component is transferred to M_2. Therefore, the diode-connected transistor M_a, which acts as an IMD3 sinker, is added to the cascode CS LNA as the Figure 3.9.

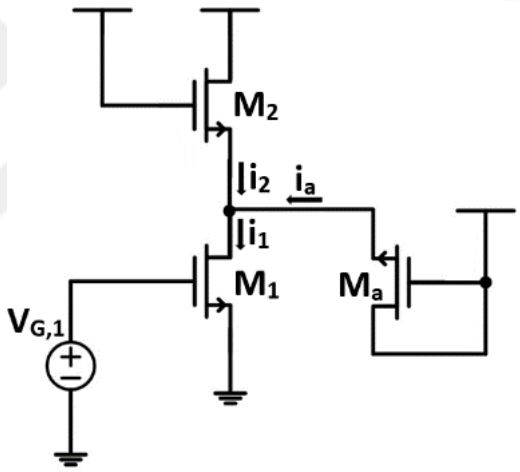


Figure 3.9: The LNA with an NMOS IMD sinker (adopted in LNA2).

The drain current of the NMOS transistor can be expressed using power-series expansion.

$$i_d = g_1 V_{gs} + g_2 (V_{gs})^2 + g_3 (V_{gs})^3 \tag{3.13}$$

where g_i is n^{th} order transconductance. Also, i_1 and i_a can be expressed.

$$i_1 = g_{1,m1} V_{gs1} + g_{2,m1} (V_{gs1})^2 + g_{3,m1} (V_{gs1})^3 \tag{3.14}$$

$$i_a = g_{1,ma} V_{gs,ma} + g_{2,ma} (V_{gs,ma})^2 + g_{3,ma} (V_{gs,ma})^3 \tag{3.15}$$

where V_{gs1} and $V_{gs,ma}$ are the gate-source voltage of M_1 and M_a, respectively. V_{sg2} is a function of V_{gs1}, so V_{gs2} can be expressed using power-series expansion.

$$V_{sg2} = c_1 V_{gs1} + c_2 (V_{gs1})^2 + c_3 (V_{gs1})^3 \tag{3.16}$$

Where c_i is the frequency-dependent coefficient. Also, $V_{gs,a}$ is equals to V_{gs2}, so i_a can be expressed in terms of V_{sg2}.

$$i_a = g_{1,ma}(-V_{sg2}) + g_{2,ma}(-V_{sg2})^2 + g_{3,ma}(-V_{sg2})^3 \tag{3.17}$$

Taking equations (3.13)-(3.17) to equation (3.12), i_2 will be as in 3.18.

$$i_2 = (g_{1,m1} + c_1 g_{1,ma}) V_{gs1} + (g_{2,m1} + {c_1}^2 g_{2,ma}) (V_{gs1})^2$$
$$+ (g_{3,m1} + {c_1}^3 g_{3,ma}) (V_{gs1})^3 \tag{3.18}$$

C_1, C_2, and C_3 depend on frequency, and C_1 has a negative value from basic circuit theory [18]. Also, it is tried to cancel $(g_{3,m1} + {c_1}^3 g_{3,ma})$ expression by adjusting the gate biasing and size of M_a. However, IMD3 is not fully canceled due to limited power, so the circuit is designed to minimize the IMD3 component.

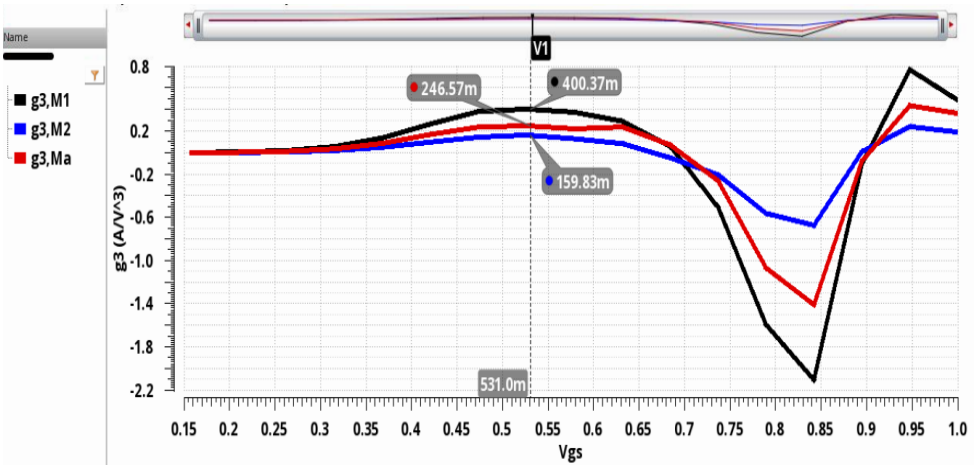


Figure 3.10: The third-order transconductance of M_1, M_2, and M_a.

The graphs of the third-order transconductance in Figure 3.10 confirm the above analysis were obtained by taking the third-order derivative of the drain currents with respect to V_{gs} [18].

$$g_{3,M1} = \frac{1}{6}\frac{\partial^3 i_1}{\partial^3 V^3{}_{gs,1}} \tag{3.19}$$

$$g_{3,M2} = \frac{1}{6}\frac{\partial^3 i_2}{\partial^3 V^3{}_{gs,1}} \tag{3.20}$$

$$g_{3,Ma} = \frac{1}{6}\frac{\partial^3 i_a}{\partial^3 V^3{}_{gs,1}} \tag{3.21}$$

$g_{3,m2}$ is decreased from 400 mA/V^3 to 160 mA/V^3 at V_{gs1} = 531 mV and P = 986.6 μW. However, the gain is reduced due to lowering $(g_{1,m1} + c_1 g_{1,ma})$ expression. Therefore, M_b is added to increase gain as in Figure 3.3. As you have seen in equation 3.8, since both circuits have the same R_L, R_S, and ω_o, the gain depends on cut-off frequency (ω_T). g_m in the LNA without gain improvement technique is equals to the transconductance of M_1 $g_{m,1}$ 11.24 mS while g_m in the LNA with gain improvement technique is the sum of $g_{m,1}$ and $g_{m,b}$ 13.31 mS. This improves the gain with increasing ω_T. Sizing of M_b should be done not to disturb the IMD current balance so that the linearity performance can be preserved.

Also, the addition of M_a reduces the output resistance of the LNA, R_{OUT}. When looking down into the drain of M_2 and ignoring the source inductance L_1 in Figure 3.1 without loss of generality, R_{OUT} roughly equals to $g_{m2}r_{o2}r_{o1}$ for LNA1. Now, when the diode-connected M_a is connected to the source of M_2, its output resistance appears in parallel with r_{o1}. Hence, R_{OUT} becomes $g_{m2}r_{o2}(r_{o1} // \frac{1}{g_{ma}} // r_{oa})$ in LNA2. Since $\frac{1}{g_{ma}} \ll r_{o1}, r_{oa}$, it can be stated that R_{OUT} of LNA2 will be small compared to that of LNA1. However, when M_b is introduced, the operating current of the cascode stage slightly decreases so that the overall power consumption does not exceed 1 mW. Reduction of the cascode stage current yields an increase in R_{OUT} although r_{ob} comes in shunt with the output resistance of the cascode. Also, g_m of M_b boosts G_m of the LNA since it provides a voltage gain path in the shunt with the cascode amplifier. An increase in both R_{OUT} and G_m improves the voltage gain of LNA3.

The layout of the designed LNA is given in Fig. 3.11. After parasitic extraction of the layout is performed, component values in the LNA design are shown in Table 3.1 have been optimized. It occupies an area 0.082 mm^2.

Table 3.1: Device sizes W/L ($\mu m/nm$) and circuit component values.

M_1	32/40	C_1	200 pF
M_2	16/150	L_b	750 pH
M_a	8/40	C_{ex}	712 fF
M_b	44/40	L_d	8.5 nH
L_g	2.2 nH	C_2	483 fF

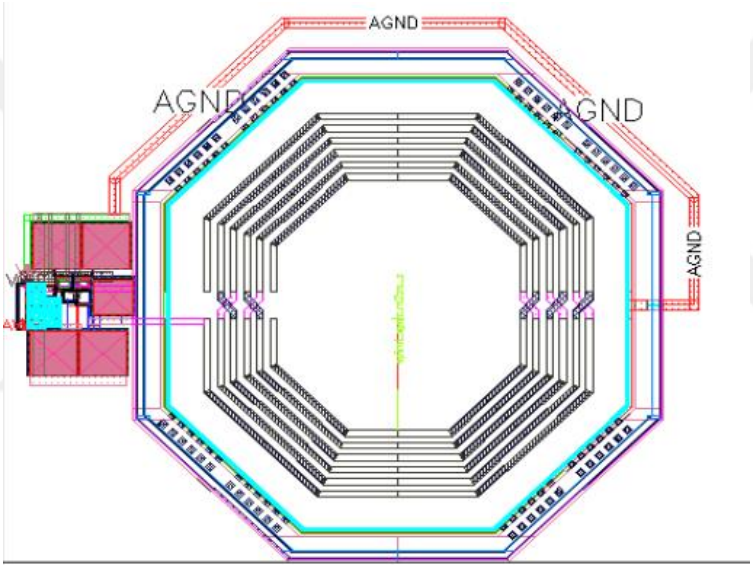


Figure 3.11: The layout of the designed LNA4.

4. SIMULATION RESULTS AND DISCUSSION

The proposed LNA with high linearity was designed in TSMC 40 nm technology with a supply voltage of V_{DD} = 1 V. The current consumption was 989.6 μA. All LNAs were designed and optimized to operate at 2.4 GHz.

In Figure 4.1 – Figure 4.5, the performance of the cascode CS LNA (LNA1) is demonstrated when tuned to operate at 2.4 GHz. As seen in Figure 4.1 and Figure 4.2, it has a matched input and output impedance (S_{11} = −27 dB and S_{22} = −16.93 dB, respectively). Figure 4.3 shows that it achieves a voltage gain of 12.217 dB. Also, the noise figure equals 4.35 dB. Figure 4.5 presents an IIP3 of −12.68 dBm.

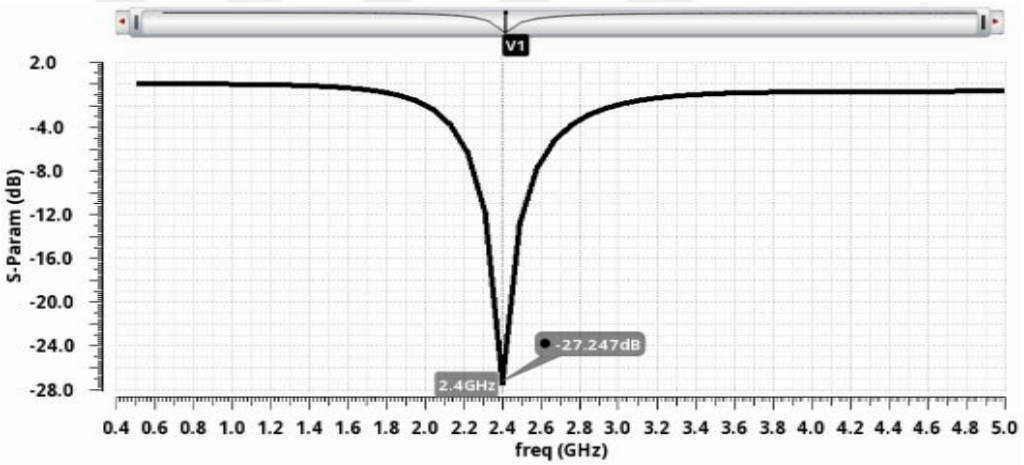


Figure 4.1: S_{11} of the cascode CS LNA (LNA1)**.**

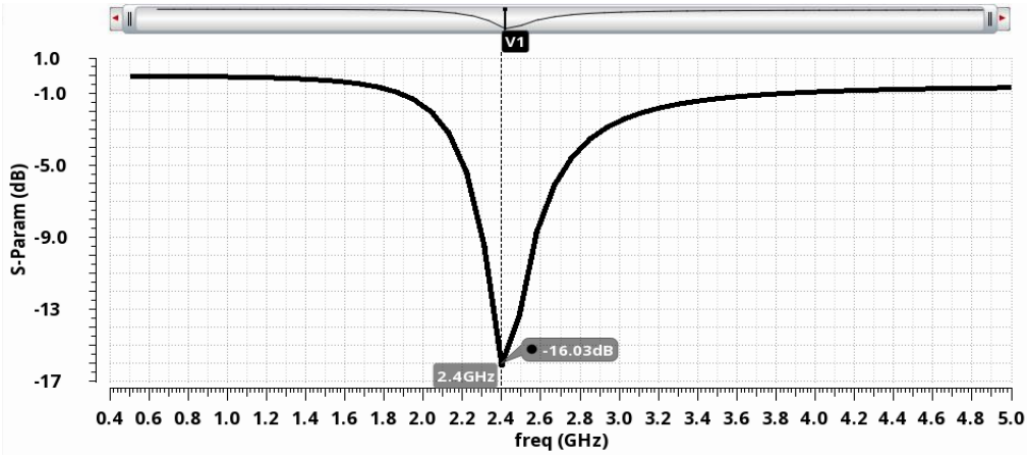


Figure 4.2: S_{22} of the cascode CS LNA (LNA1)**.**

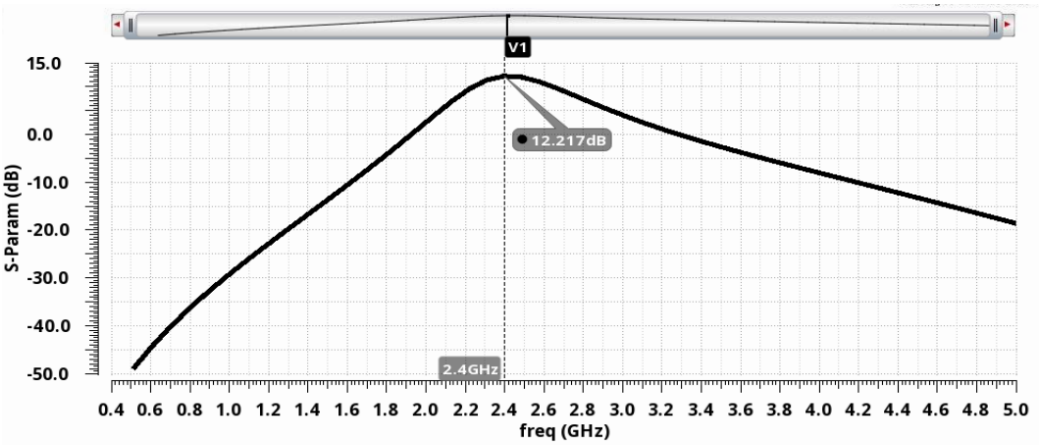


Figure 4.3: The voltage gain (S_{21}) of the cascode CS LNA (LNA1)**.**

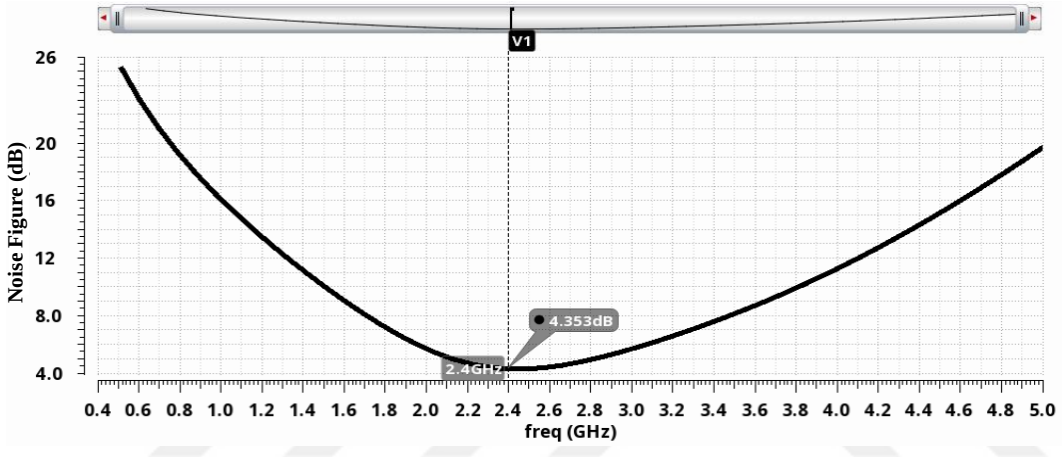


Figure 4.4: NF of the cascode CS LNA (LNA1)**.**

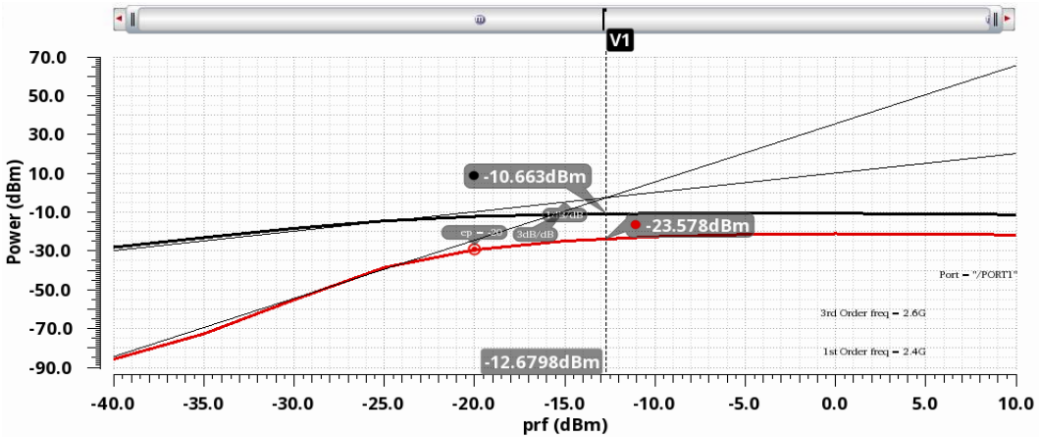


Figure 4.5: IIP3 of the cascode CS LNA (LNA1).

Figure 4.6 – Figure 4.10 demonstrate the performance of the LNA with improved linearity at 2.4 GHz. Input and output reflection coefficients are satisfactory (S_{11} = -17.97 dB and S_{22} = -22.9 dB, respectively) according to Figure 4.6 and Figure 4.7. In Figure 4.8, a gain is reduced from 12.2 dB to 5.68 dB while IIP3 is raised by

approximately 12.5 dBm in Figure 4.10, from −12.68 dBm to −0.107 dBm. Also, NF increased to 5.126 dB.

As seen in Figure 3.3, M_a is added to LNA1 to improve IIP3 performance. M_a is used to decrease IMD3 of M_2 transistor with the injected current. $g_{3,M2}$ is decreased with subtraction of M_1 and M_a g_3 values, which have the same sign. The gate biasing and M_a sizing are adjusted to eliminate $g_{3,M2}$. Taking into consideration power consumption constraint, $g_{3,M2}$ is not fully eliminated. However, $g_{3,M2}$ has been reduced enough to increase the IIP3 value by approximately 12.5 dBm.

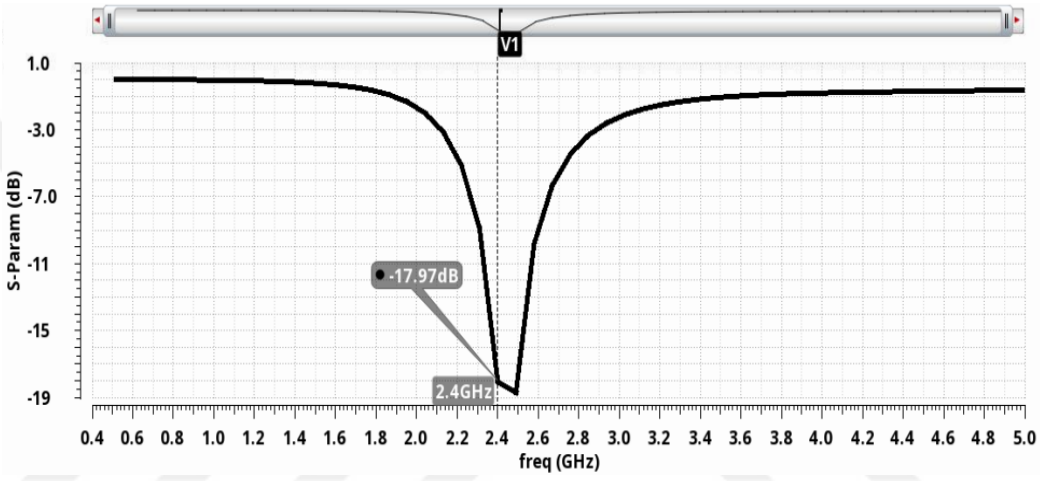


Figure 4.6: S_{11} of LNA2 with improved linearity.

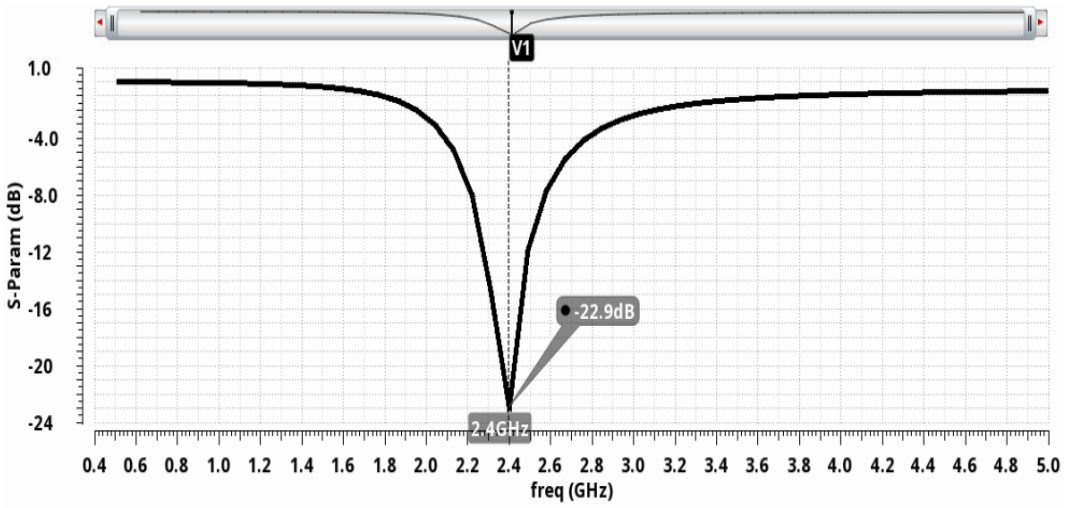


Figure 4.7: S_{22} of LNA2 with improved linearity.

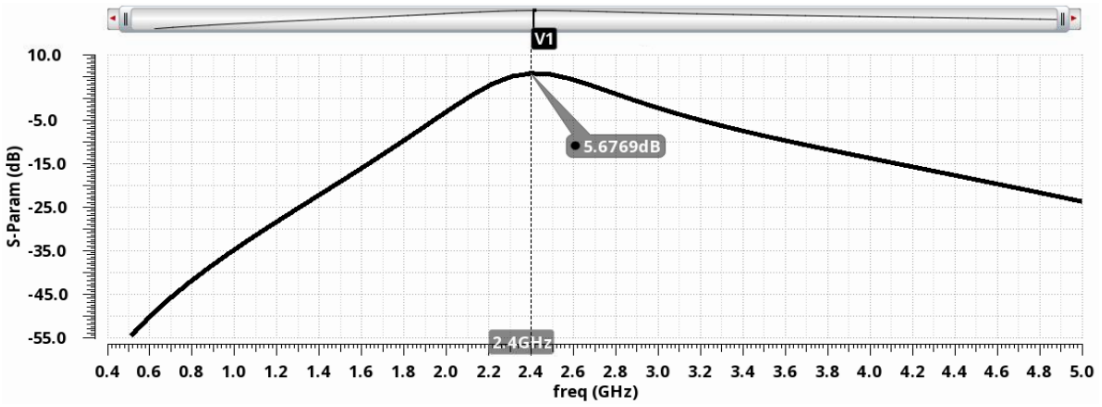


Figure 4.8: The voltage gain (S_{21}) of LNA2 with improved linearity.

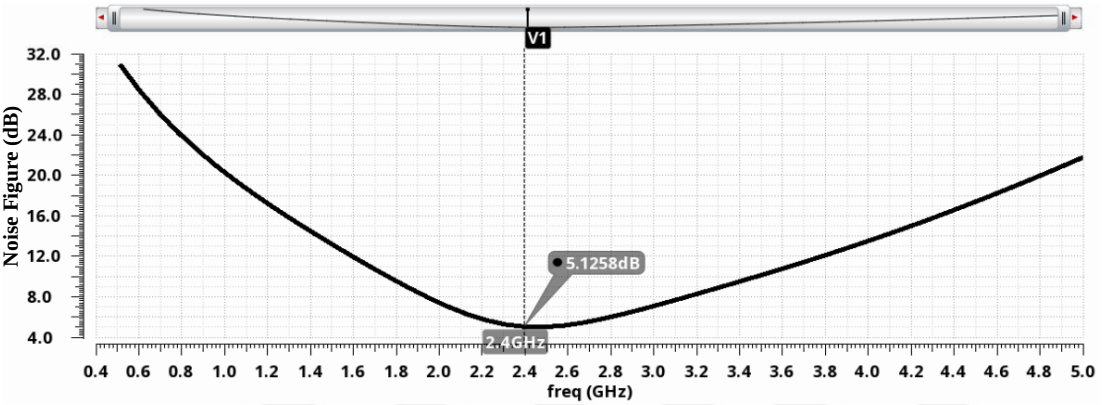


Figure 4.9: NF of LNA2 with improved linearity.

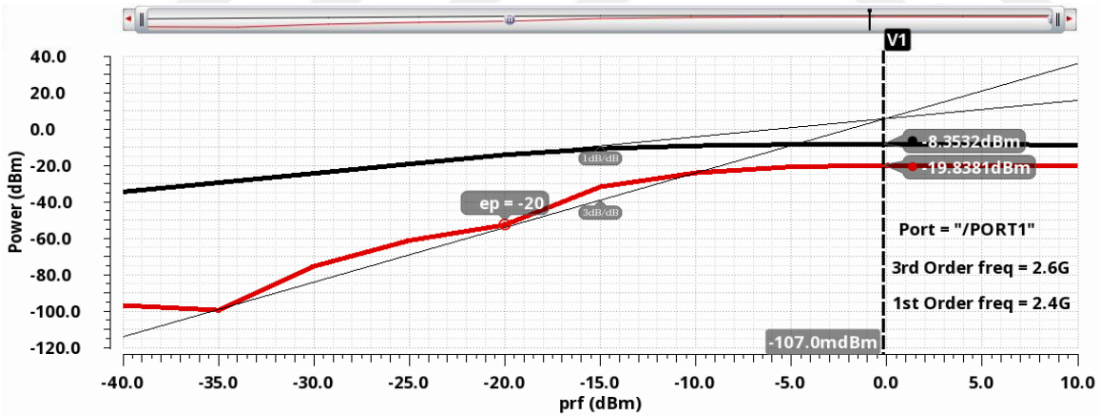


Figure 4.10: IIP3 of LNA2 with improved linearity.

In Figure 4.11−Figure 4.15, the performance metrics of the LNA with improved linearity and gain are depicted. Figure 4.11 and Figure 4.12 demonstrate that S_{11} and S_{22} have their values below −11 dB. Figure 4.13 reveals that the voltage gain is boosted by 6 dB without degrading the IIP3 performance, which is equal to 11.1 dB. Furthermore, NF has reduced to 4.27 dB based on increased voltage gain, as illustrated in Figure 4.14. In Figure 4.15, IIP3 is found to be −0.816 dBm. L_g is kept on-chip in this LNA.

While IIP3 is improved with decreasing $g_{3,M2}$, gain is degraded by decreasing $g_{m,M2}$ which is obtained by subtracting the $g_{m,M1}$ by $g_{m,Ma}$ as shown in equation 3.18. M_b is added to LNA2 to increase gain as illustrated in Figure 3.3. However, M_b reduces the isolation (S_{12}) of cascode CS LNA. Thus, M_b transistor should be sized to increase the gain without being so dominant that it spoils the isolation. As seen in Figure 4.16, S_{12} is increased by 13 dB, but this change is not so much that the input and output are affected by each other.

In contrary to the IIP3 graph of LNA1, the slope of 3^{rd} order curve varies in different ranges of the input power. In LNA1, the linear and nonlinear current components of M_2 can be expressed as in equation 4.1.

$$i_2 = g_{m,M1}V_{gs1} + g_{2,M1}(V_{gs1})^2 + g_{3,M1}(V_{gs1})^3 \tag{4.1}$$

Here, the third order terms are only related to M_1. However, in LNA2, i_2 can be expressed as in equation (3.18). There, the 3^{rd} order term includes $(g_{3,M1} + {c_1}^3 g_{3,Ma})$. Thus, IIP3 is now related to M_a, as well as, to M_1. Also, it should be noted that M_a operates in the weak inversion region. Changes in the slope of the overall 3^{rd} order curve of the LNA may stem from the of 3^{rd} order terms of both M_1 and M_a, according to their operation regions. While the 1^{st} and 3^{rd} order curves settle at approximately -20 dBm of input power in LNA1, they settle at approximately -15 dBm of input power in LNA2. The settling points shift by 5 dBm for both curves. It is shown that correspondingly, the LNA IIP3 is improved by approximately 10 dBm.

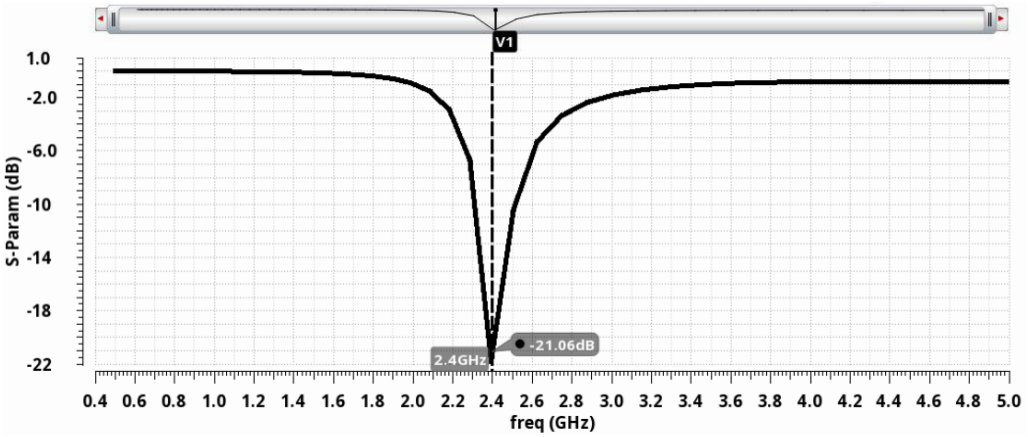


Figure 4.11: S_{11} of LNA3 with improved linearity and gain.

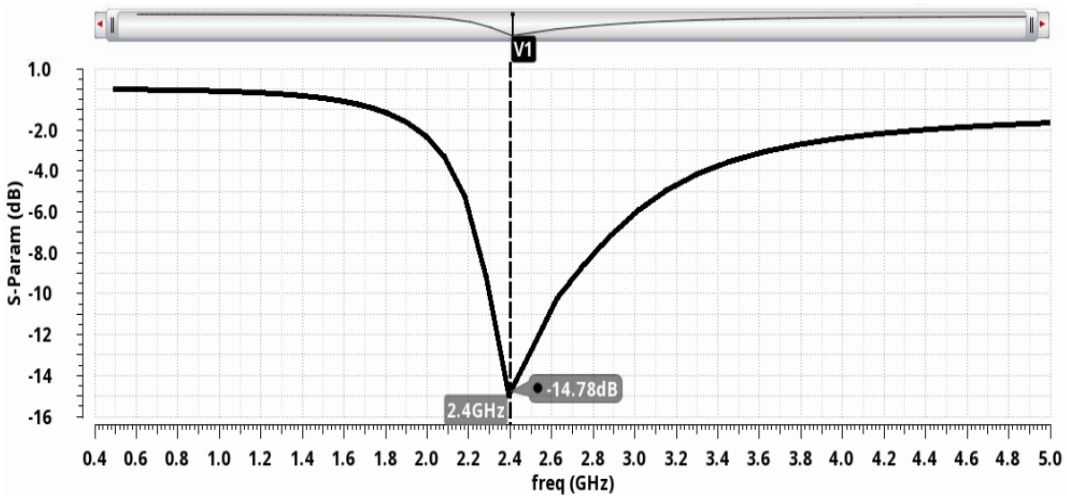


Figure 4.12: S_{22} of LNA3 with improved linearity and gain.

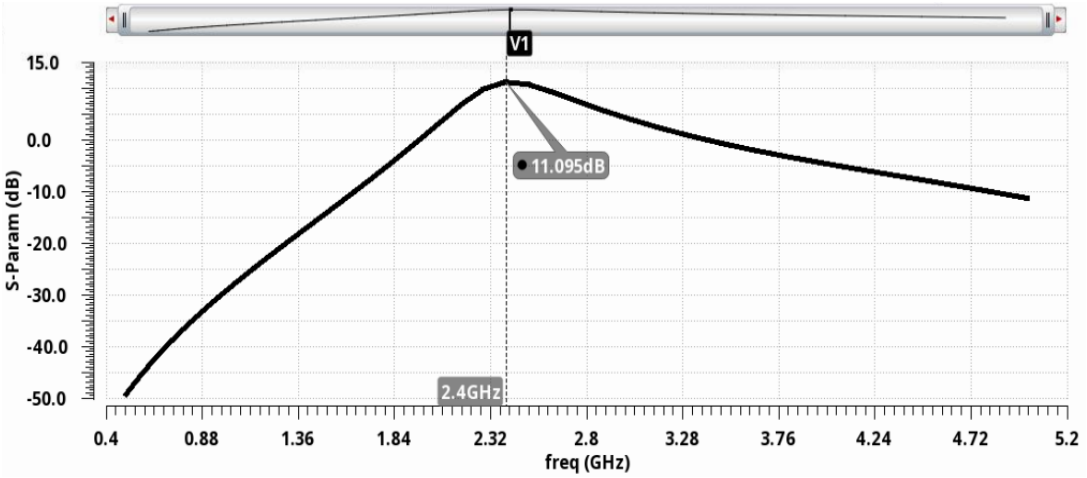


Figure 4.13: S_{21} of LNA3 with improved linearity and gain.

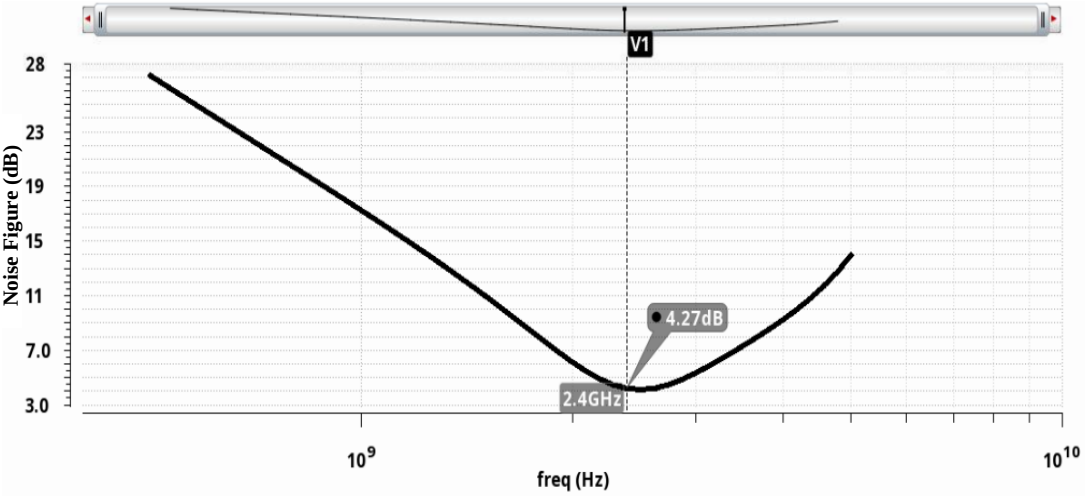


Figure 4.14: NF of LNA3 with improved linearity and gain.

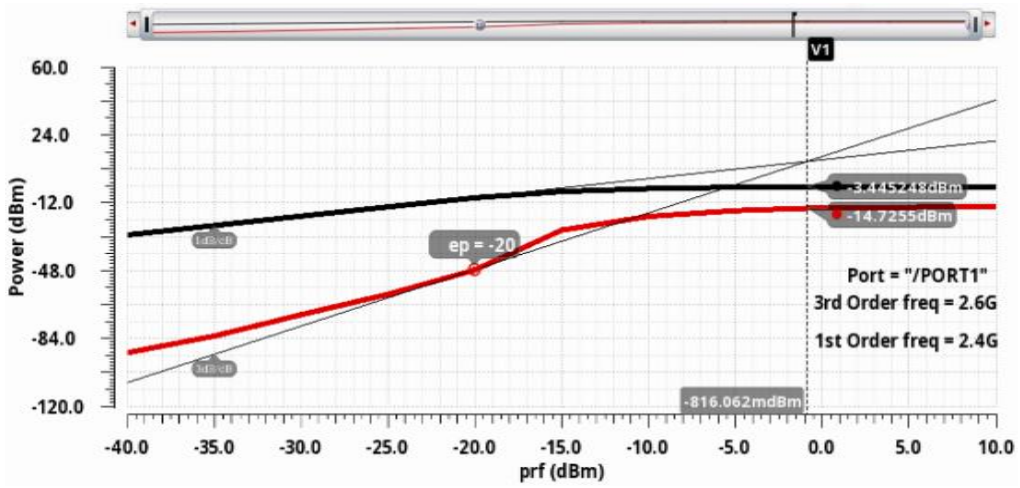


Figure 4.15: IIP3 of LNA3 with improved linearity and gain.

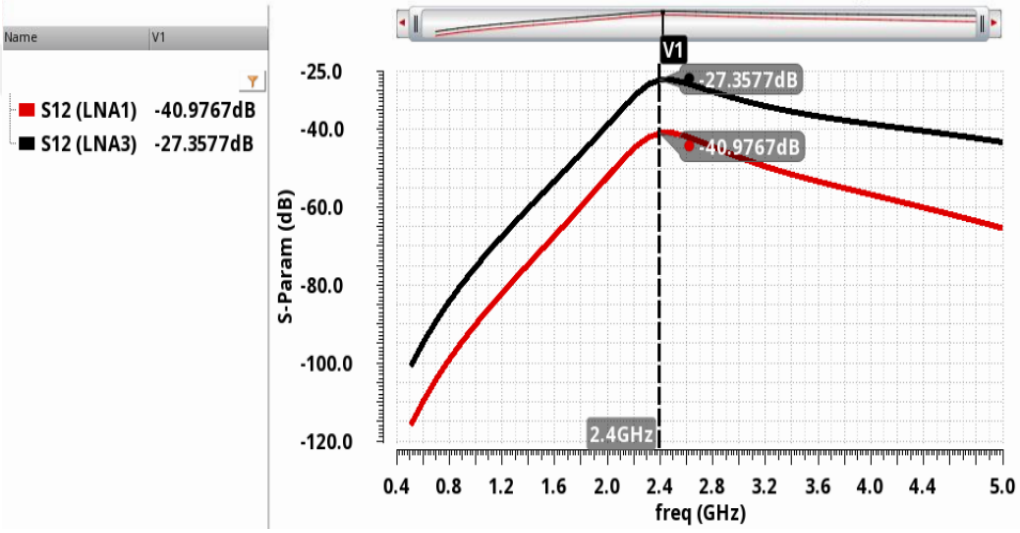


Figure 4.16: S_{12} of LNA1 and LNA3.

Figure 4.17–Figure 4.22 demonstrate the post-layout simulation results of the LNA with improved linearity and gain (off-chip L_g). According to Figure 4.17 and 4.18, input and output reflection coefficients at 2.4 GHz are acceptable, with (S_{11} = −18.54 dB (pre-layout) and −13.63 dB (post-layout)) (S_{22} = −20.45 dB (pre-layout) and −12.85 dB (post-layout)).

DC lines that cross the input RF path are more critical in the LNA performance. Thus, these paths are drawn wider to decrease parasitic resistance as well as input and output path. Thus, no significant changes of S_{11} and S_{22} are observed.

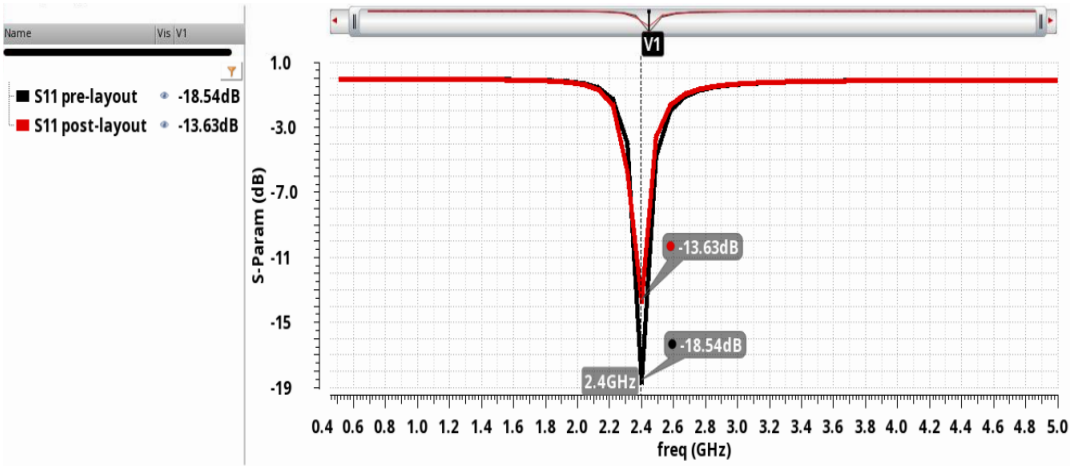


Figure 4.17: S_{11} of LNA4 with improved linearity and gain (off-chip L_g).

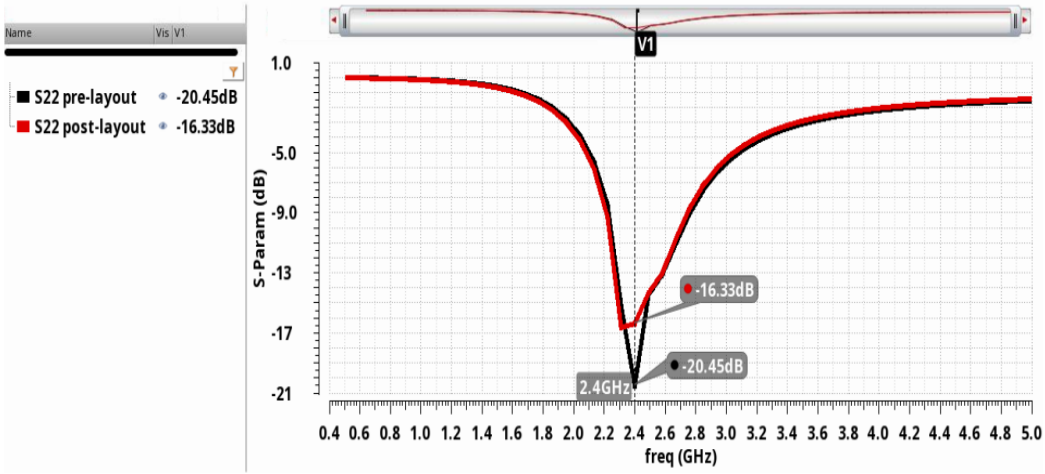


Figure 4.18: S_{22} of LNA4 with improved linearity and gain (off-chip L_g).

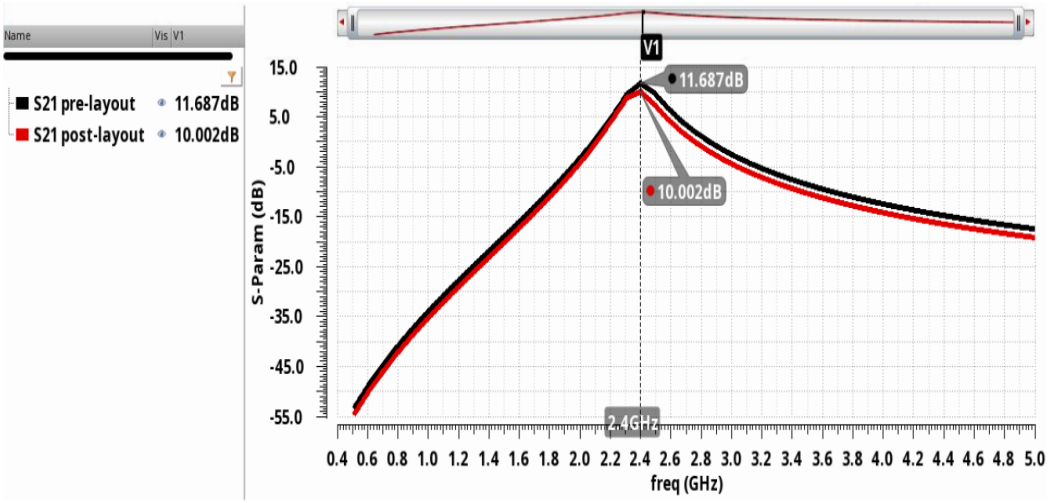


Figure 4.19: S_{21} of LNA4 with improved linearity and gain (off-chip L_g).

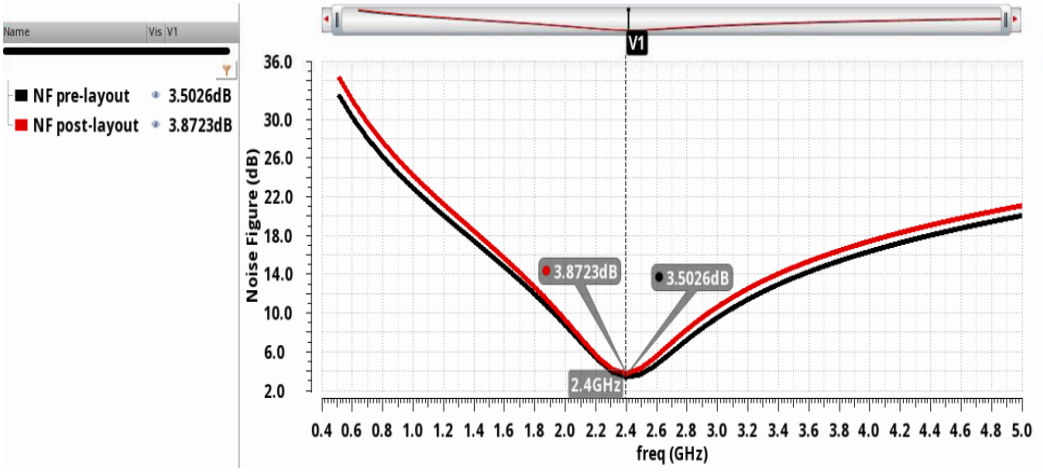


Figure 4.20: NF of LNA4 with improved linearity and gain (off-chip L_g).

As can be seen in Figure 4.19, it achieves a voltage gain of 10 dB in the post-layout simulation. The gain reduction in the post-layout simulation results from the parasitic resistance. It is seen in Figure 4.20 that the noise figure increases with a decrease in gain. The wider ground and power lines are drawn to minimize the parasitic effect. Finally, IIP3 has been shown to be enhanced in post-layout simulation compared to in pre-layout simulation as in Figure 4.21 and Figure 4.22. The inductive effect between the source and the ground increases the linearity while decreasing the gain. The reason for the increase in linearity in the post layout is the effect of parasitic components.

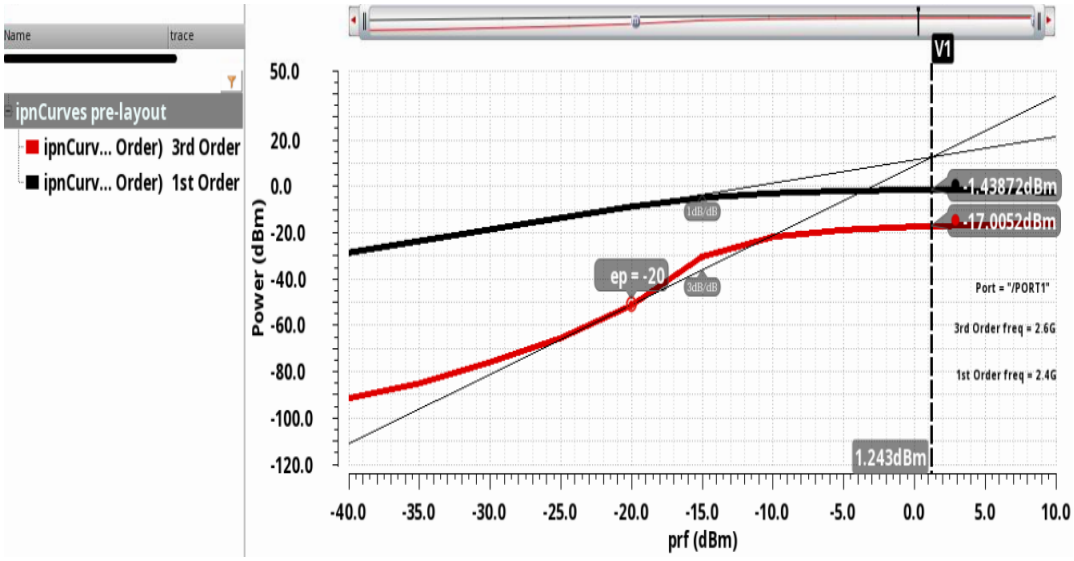


Figure 4.21: IIP3 (pre-layout) of LNA4 with improved linearity and gain (off-chip L_g).

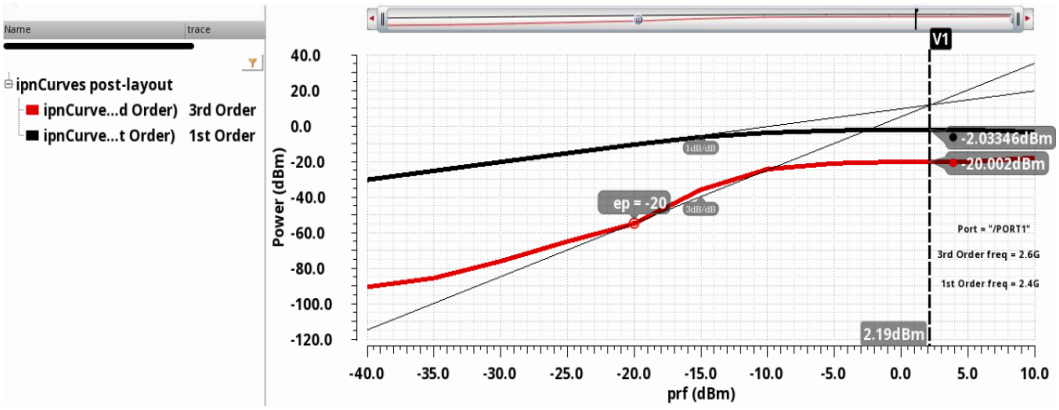


Figure 4.22: IIP3 (post-layout) of LNA4 with improved linearity and gain (off-chip L_g).

Table 4.1 summarizes the performances of four different LNAs. While classical cascode CS LNA (LNA1) is not suitable in terms of IIP3 for our specification, IIP3 performance has been improved by approximately 12.5 dBm, confirming to specification. However, gain in LNA2 is well below specifications as well as NF. Although both gain and IIP3 performances are enhanced in LNA3, this topology may occupy a huge area due to the on-chip input matching circuit. Thus, all performance metrics of LNA4 are suitable, and L_g is obtained a high-quality factor by reducing the occupied chip estate. Compared tot the FOM of four LNA topologies, LNA4 is acceptable and is suitable for our specifications. Based on the figure of merit (FOM) expression provided in (4.1), LNA4 achieves the higher FOM value.

$$FOM = \frac{S_{21}(dB) \times IIP3(\mu W)}{(NF(dB)-1) \times P_{dc}(\mu W)} \tag{4.1}$$

Table 4.1: Performances of the proposed LNAs.

	LNA1	***LNA2***	***LNA3***	***LNA4***	
S_{21} (dB)	12.22	5.68	11.1	11.69	10*
NF (dB)	4.35	5.13	4.27	3.5	3.87*
S_{11} (dB)	−27.25	−17.97	−21	−18.54	−13.63*
S_{22} (dB)	−16	−23	−14.78	−20.45	−16.33*
IIP3 (dBm)	−12.68	−0.107	−0.816	1.24	2.19*

***Post-layout simulation results**

Table 4.1 (continued): Performances of the proposed LNAs.

P_{dc} (μW)	995.6	986.6	997.2	1079	989.6*
FOM	0.198	1.36	2.82	5.76	5.83*

***Post-layout simulation results**

In Table 4.2, performance metrics of LNA4 are compared with the results of various low-power LNAs reported in the literature with an operating frequency in the range of 0.1 GHz to 7 GHz. Although FOM of [26] and [29] is higher than that of LNA4, NF of [26] is excessively high for LNA compared to literature, and IIP3 of [29] is almost equal to that of the classical cascode CS LNA. Except for these researches, LNA4 is the best of all when compared to the FOM of others. Also, the power consumption of [34] is remarkably low; however, NF of the first study [34] is extremely high while IIP3 of the second study [34] is excessively lower than our LNA4 design. Also, [36] and [37] are remarkable in terms of using new CMOS technologies. However, NF of [36] is too high while gain of [37] is significantly low.

Table 4.2: Performance of the proposed LNA regarding its counterparts.

	Gain (dB)	**NF** (dB)	**IIP3** (dBm)	P_{dc} (μW)	f_C (GHz)	**Tech.** (nm)	**FOM**
This Work*	10	3.87	2.19	989.6	2.4	40	5.83
[26]**	11	6.8	-2.2	174	2.4	65	6.56
[27]*	18.2	3.38	-4.32	967	2.4	180	2.93
[28]*	14	3.45	-8	980	2.4	180	0.92
[29]***	14	5.2	-8.6	30	2.4	40	15.2
	14.2	3.3	-11.6				14.2

Table 4.2 (continued): Performance of the proposed LNA regarding its counterparts.

[30]**	12.6	5.5 – 6.5	−9	750	0.1 – 7	90	0.47
[31]**	12.3	4.9 – 6	−9.5	400	0.1 – 2.2	130	0.87
[32]**	14	4 – 6	−10	250	0.6 – 4.2	130	1.87
[33]***	17.4	2.8	−10.7	480	2.4	65	1.71
[34]**	13.9	8.9	−13	69	2.4	65	1.27
	26.3	5.5	−24	64			0.37
[35]***	12.2	1.9 – 2.2	−16	350	3 – 5	130	0.97
[36]**	21.5	6.3	−16	900	2.4	28	0.11
[37]**	6.9	3	−18	44	2.4	16	1.25

***Post-layout simulation results**

****Measurements results**

*****Pre-layout simulation results**

5. CONCLUSION

An ultra-low-power design is highly critical in many applications such as wireless sensor networks, WSNs, and portable devices. Especially, the LNA is one of the power-hungry blocks in transceivers used in wireless systems. There are two main challenges for these systems: device size for portability and ultra-low-power design which is able to operate for the required time that may be a year for medical devices. Therefore, ultra-low power and small size wireless transceivers have been remarkably enhanced as a consequence of immense researches on transceiver topologies and RF circuit design using standard CMOS technology. In addition, as power consumption decreases, high-performance metrics like gain, bandwidth, linearity, and noise should not be degraded.

This thesis focuses on the design of a sub-mW LNA with high linearity. It has been demonstrated that IIP3 improvements can be achieved without degrading gain. Specifications of the LNA are designated as the IIP3 of higher than -1 dBm and total power less than 1 mW. The voltage gain is desired to be higher than 10 dB and the noise figure is lower than 4 dB. Input and output reflection coefficients are targeted to be lower than -10 dB. In this thesis, four LNAs using two different techniques to improve linearity and voltage gain are designed at sub-mW power in TSMC 40 nm process for operation at 2.4 GHz. The proposed LNA, LNA4, powered by a 1 V supply, achieves an IIP3 figure of 2.19 dBm and dissipates 989.6 μW at 2.4 GHz. It has a voltage gain of 10 dB and a noise figure of 3.87 dB. Based on its design metrics, LNA4 is suited for ultra-low-power, high-performance receivers.

Literature research shows that as CMOS technologies have been scaled down, the gain and noise performances of the LNA have degraded. Also, the tradeoff between linearity and power consumption is one of the main challenges for ultra-low-power LNA design. Integration of LNAs designed in deep sub-micron technologies into ultra-low power devices such as medical applications is a field of study and research that needs to be developed.

Although the performance metrics of LNA4 are the best among the four topologies, it may not be suitable for medical equipment due to the off-chip input matching circuit. The fully integrated LNA3 topology is more suitable for medical applications. However, its performance metrics are needed to be improved.

REFERENCES

[1] **Nadia, A., Belgacem, H. and Aymen, F.,** 2013, September. A low power low noise CMOS amplifier for Bluetooth applications. In 2013 International Conference on Applied Electronics (pp. 1-4). IEEE.

[2] **Yelten, M.B. and Gard, K.G.,** 2009, April. A novel design procedure for tunable low noise amplifiers. In 2009 IEEE 10th Annual Wireless and Microwave Technology Conference (pp. 1-5). IEEE.

[3] **Fan, X., Zhang, H. and Sánchez-Sinencio, E.,** 2008. A noise reduction and linearity improvement technique for a differential cascode LNA. IEEE Journal of Solid-State Circuits, 43(3), pp.588-599.

[4] **Hsiao, C.T.,** 2017. Design of a 2.4 GHz CMOS LNA for Bluetooth low energy application using 45 nm technology.

[5] **Liu, H.J. and Zhang, Z.F.,** 2017. An ultra-low power CMOS LNA for WPAN applications. IEEE Microwave and Wireless Components Letters, 27(2), pp.174-176.

[6] **Çağlar, A. and Yelten, M.B.,** 2019. Design of cryogenic LNAs for high linearity in space applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 66(12), pp.4619-4627.

[7] **Sánchez-Sinencio, E.** 2017**.** Linearization Techniques for CMOS LNAs: A Tutorial. Analog and Mixed Signal Center, Texas A&M University, retrieved Feb, 17, 76.

[8] **Youn, Y. S., Chang, J. H., Koh, K. J., Lee, Y. J. and Yu, H. K.,** 2003. A 2 GHz 16 dBm IIP3 low noise amplifier in 0.25 μm CMOS technology, in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, 452–453.

[9] **Xin, C. and Sánchez-Sinencio, E.,** 2004. A linearization technique for RF low noise amplifier, in Proc. IEEE Int. Circuits Syst. Symp., Vancouver, BC, Canada, 313–316.

[10] **Im, D., Nam, I., Kim, H., and Lee, K.,** 2009. A wideband CMOS low noise amplifier employing noise and IM2 distortion cancellation for a digital TV tuner, IEEE J. Solid-State Circuits, 686–698.

[11] **Chen, W., Liu, G., Zdravko, B. and Niknejad, A. M.,** 2008. A highly linear broadband CMOS LNA employing noise and distortion cancellation, IEEE J. Solid-State Circuits, 1164–1176.

[12] **Geddada, H. M., Park, J. W. and Silva-Martinez, J.,** 2009. Robust derivative superposition method for linearizing broadband LNAs, IEE Electron. Lett., 435–436.

[13] **Kim, T. W. and Kim, B.,** 2006. A 13-dB IIP3 improved low-power CMOS RF programmable gain amplifier using differential circuit

transconductance linearization for various terrestrial mobile D-TV applications, IEEE J. Solid-State Circuits, 945–953.

[14] **Aparin, V. and Larson, L. E.,** 2005. Modified derivative superposition method for linearizing FET low-noise amplifiers, IEEE Trans. Microw. Theory Tech., 571–581.

[15] **Ganesan, S., Sánchez-Sinencio, E. and Silva-Martinez, J.,** 2006. A highly linear low noise amplifier, IEEE Trans. Microw. Theory Tech., 4079–4085.

[16] **Blaakmeer, S. C., Klumperink, E. A., Leenaerts, D. M., & Nauta, B.** 2008. Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling. *IEEE journal of solid-state circuits*, *43*(6), 1341-1350.

[17] **Zhang, H., Fan, X. and Sánchez-Sinencio, E.,** 2009. A low-power, linearized, ultra-wideband LNA design technique, IEEE J. Solid-State Circuits, 320–330.

[18] **Kim, T.-S. and Kim, B.-S.,** 2006. Post-linearization of cascode CMOS LNA using folded PMOS IMD sinker, IEEE Microw. Wireless Comp. Lett., 182–184.

[19] **Kim, N., Aparin, V., Barnett, K. and Persico, C.,** 2006. A cellular-band CDMA CMOS LNA linearized using active post-distortion, IEEE J. Solid-State Circuits, 1530–1534.

[20] **Razavi, B., & Behzad, R.** 2012. RF microelectronics (Vol. 2, pp. 255-333). New York: Prentice hall.

[21] **Johns, D. A., & Martin, K.** 2008. Analog integrated circuit design. John Wiley & Sons.

[22] **Packard, H.** 1996. S Parameter Techniques for Faster, More Accurate Network Design. Test & Measurement, Application Note, 95-1.

[23] **Agilent Technologies**. 2010. "Fundamentals of RF and Microwave Noise Figure Measurements", Agilent Technologies. U.S.

[24] **Shaeffer, D.K. and Lee, T.H.** 1997. A 1.5-V, 1.5-GHz CMOS low noise amplifier, IEEE Journal of Solid-State Circuits, 32(5), 745–759.

[25] **Gonzalez, G.** 1997. Analysis and Design. MICROWAVE TRANSISTOR AMPLIFIERS.

[26] **Xu, K., Yin, J., Mak, P. I., Staszewski, R. B., & Martins, R. P.** 2020. A single-pin antenna interface RF front end using a single-MOS DCO-PA and a push–pull LNA. *IEEE Journal of Solid-State Circuits*, *55*(8), 2055-2068.

[27] **Karimlou, A., Jafarnejad, R., & Sobhi, J.** 2016. An inductor-less sub-mW low noise amplifier for wireless sensor network applications. *Integration*, *52*, 316-322.

[28] **Rastegari, F., Dousti, M., & Ghalamkari, B.** 2021. A 0.75 V Sub-mW CMOS LNA employing transmitted signal suppression technique in a full-duplex wireless brain-machine interface transceiver. *AEU-*

International Journal of Electronics and Communications, *132*, 153632.

[29] **Kargaran, E., Manstretta, D., & Castello, R.** 2017. Design and Analysis of 2.4 GHz μW CMOS LNAs for Wearable WSN Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 65(3), 891-903.

[30] **Parvizi, M., Allidina, K., & El-Gamal, M. N.** 2014. A sub-mW, ultra-low-voltage, wideband low-noise amplifier design technique. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *23*(6), 1111-1122.

[31] **Parvizi, M., Allidina, K., & El-Gamal, M. N.** 2016. An ultra-low-power wideband inductorless CMOS LNA with tunable active shunt-feedback. *IEEE Transactions on Microwave Theory and Techniques*, *64*(6), 1843-1853.

[32] **Parvizi, M., Allidina, K., & El-Gamal, M. N.** 2015. Short Channel Output Conductance Enhancement Through Forward Body Biasing to Realize a 0.5 V 250 μW 0.6–4.2 GHz Current-Reuse CMOS LNA. *IEEE Journal of Solid-State Circuits*, *51*(3), 574-586.

[33] **Rahman, M., & Harjani, R.** 2018. A 2.4-GHz, Sub-1-V, 2.8-dB NF, 475-μW Dual-Path Noise and Nonlinearity Cancelling LNA for Ultra-Low-Power Radios. *IEEE Journal of Solid-State Circuits*, *53*(5), 1423-1430.

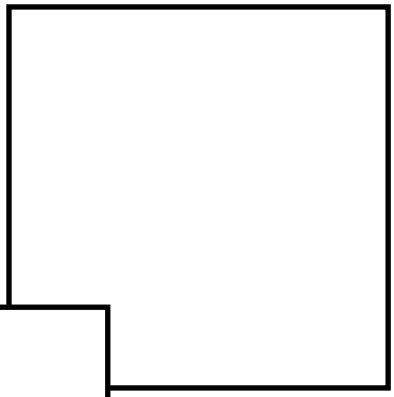
[34] **Dissanayake, A., Seok, H. G., Jung, O. Y., Han, S. K., & Lee, S. G.** 2017, June. A 64 μW, 23 dB gain, 8 dB NF, 2.4 GHz RF front-end for ultra-low power Internet-of-Things transceivers. In *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)* (pp. 184-187). IEEE.

[35] **Saied, A. M., Abutaleb, M. M., Eladawy, M. I., & Ragai, H.** 2018. Ultra-low power LNA design technique for UWB applications. AEU-International Journal of Electronics and Communications, 97, 149-153.

[36] **Zaini, J., Hameau, F., Taris, T., Morche, D., Audebert, P., & Mercier, E**. 2017, July. A tunable Ultra Low Power inductorless Low Noise Amplifier exploiting body biasing of 28 nm FDSOI technology. In 2017 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED) (pp. 1-6). IEEE.

[37] **Lu, Y. T., & Jin, J. D.** 2016, May. 100-mV 44-μW 2.4-GHz LNA in 16 nm FinFET technology. In 2016 IEEE MTT-S International Microwave Symposium (IMS) (pp. 1-3). IEEE.

CURRICULUM VITAE



Name Surname **:** Didem EROL AS

EDUCATION **:**

- **B.Sc.** **:** 2017, Istanbul Technical University, Faculty of Chemical and Metallurgical Engineering, Food Engineering Department
- **B.Sc.** **:** 2018, Istanbul Technical University, Electrical and Electronics Engineering Faculty, Electronics and Communications Engineering Department

PROFESSIONAL EXPERIENCE AND REWARDS:

- 2020 Research assistant at Istanbul Technical University
- 2017 TEV Higher Education Performance Award
- 2017 Ömer Duruk Performance Award
- 2016 Pelin Köz Performance Award
- 2016 TEV Higher Education Performance Award
- 2015 Food Industry Performance Award
- 2015 TEV Higher Education Performance Award
- 2014 TEV Higher Education Performance Award

PUBLICATIONS, PRESENTATIONS AND PATENTS ON THE THESIS:

OTHER PUBLICATIONS, PRESENTATIONS AND PATENTS:

- **Xhafa, X., Güngördü, A. D., Erol, D., Yavuz, Y., & Yelten, M. B.** 2021. An Automated Setup for the Characterization of Time-Based Degradation Effects Including the Process Variability in 40 nm CMOS Transistors. *IEEE Transactions on Instrumentation and Measurement*.

- **Erol, D., Güngördü, A. D., Dündar, G., & Yelten, M. B.** 2021. A switchable DC offset cancellation circuit for time-based degradation correction. *Analog Integrated Circuits and Signal Processing*, *106*(3), 485-491.

- **Erol, D., Güngördü, A. D., Dündar, G., & Yelten, M. B.** 2019, November. An Offset Cancellation Set-up for Amplifiers Subject to Aging. In *2019 11th International Conference on Electrical and Electronics Engineering (ELECO)* (pp. 384-387). IEEE.