

ULTRA-LOW POWER RISC-V MICROPROCESSOR SYSTEM DESIGN FOR
WIRELESS MICROSYSTEMS USING DYNAMIC LEAKAGE SUPPRESSION

by

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ABSTRACT

ULTRA-LOW POWER RISC-V MICROPROCESSOR SYSTEM DESIGN FOR WIRELESS MICROSYSTEMS USING DYNAMIC LEAKAGE SUPPRESSION

Monitoring pulmonary arterial pressure is crucial for the early detection of cardiovascular problems. A specialized microprocessor is viable since it enables flexibility and power efficiency. Therefore, it is desirable to have a processor implanted in the body, powered by a battery or energy harvesting system. Here, an ultra-low-power RISC-V microprocessor design with a standby power of tens of nanowatts is proposed. It utilizes a “Dynamic Leakage Suppression technique,” dramatically reducing static power. The processor also has its on-chip clock generator and power-on-reset to operate without additional ICs. It has only two off-chip interfaces: a UART receiver to program the processor and an SPI interface to communicate with the off-chip pressure sensor to measure the pulmonary arterial pressure. Ultra-low leakage I/O drivers are also employed in the design to drive the sensor. The processor achieves noticeably higher energy efficiency for workloads with long standby times than those with conventional methods.

ÖZET

KABLOSUZ MİKROSİSTEMLER İÇİN DİNAMİK SIZINTI BASTIRMA KULLANAN ULTRA DÜŞÜK GÜÇLÜ RISC-V MİKROİŞLEMCİ SİSTEM TASARIMI

Pulmoner arter basıncının izlenmesi kardiyovasküler sorunların erken tespiti için çok önemlidir. Bu görev için özel bir mikroişlemci kullanmak, esneklik ve güç verimliliği sağladığından uygulanabilir. Bu nedenle, vücuda implante edilmiş, bir batarya veya enerji hasadı sistemi ile çalışan bir işlemciye sahip olunması istenir. Burada, onlarca nanowatt bekleme gücüne sahip ultra düşük güçlü bir RISC-V mikroişlemci tasarımı önerilmektedir. "Dinamik Sızıntı Bastırma" adı verilen bir teknik kullanan bu işlemci, statik güç tüketimini önemli ölçüde azaltmaktadır. İşlemcinin ayrıca çip üzerinde saat üretici ve güç açık sıfırlama devresi vardır, böylece ek bir entegre olmadan çalışabilir. Sistem yalnızca iki çip-dışı arayüze sahiptir; biri işlemciyi programlamak için kullanılan bir UART alıcısı ve pulmoner arter basıncını ölçen çip dışı basınç sensörü ile iletişim kurmak için bir SPI arayüzüdür. Tasarımda sensörü sürmek için ultra düşük sızıntılı I/O sürücüleri de kullanılmıştır. Uzun bekleme sürelerine sahip iş yükleri için işlemci, geleneksel yöntemlere kıyasla belirgin ölçüde daha yüksek enerji verimliliği elde etmektedir.

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LIST OF ACRONYMS/ABBREVIATIONS

ASIC	Application-specific Integrated Circuit
DLS	Dynamic Leakage Suppression
EDA	Electronic Design Automation
FFT	Fast Fourier Transform
FIFO	First-in First-out
FLSL	Feedforward Leakage Self-suppression Logic
FSM	Finite State Machine
HDL	Hardware Description Language
HF	Heart Failure
LUT	Look-up Table
MEMS	Micro-Electro Mechanical Systems
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MRI	Magnetic Resonance Imaging
NLDM	Non-Linear Delay Model
PDP	Power-Delay Product
PnR	Place-and-Route
POR	Power-on-Reset
PVT	Process Voltage Temperature
RF	Radio-frequency
SAIF	Switching Activity Interchange Format
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
STA	Static Timing Analysis
UART	Universal Asynchronous Receiver/Transmitter
ULP	Ultra Low Power
VCD	Value Change Dump
VCO	Voltage-Controlled Oscillator

1. INTRODUCTION

Heart failure is a severe condition in which the heart is unable to pump blood effectively throughout the body. Early detection is crucial for diagnosing potential problems such as coronary artery disease, arrhythmia, or high blood pressure. A proven approach is to routinely assess the heart's pumping capacity, measuring how much blood the heart can pump. While devices such as smartwatches offer convenience, they cannot be relied upon for advanced medical purposes. The most accurate way to measure blood pressure is at a point very close to the heart, such as the aorta.

Monitoring the heart is particularly important in elderly individuals, as they have a higher risk of HF [1]. It is even better to perform monitoring continuously to detect failures as effectively as possible. However, frequent visits to medical centers can negatively impact their quality of life. Therefore, there is a need for a system that can collect blood pressure data at home and send it to medical professionals for analysis.

CardioMEMS [2] serves as a commercial product designed for HF monitoring. The system incorporates an implantable MEMS pressure sensor in aorta and a coil for system power and communication. When the patient lies on a platform, the system is powered via the coil, and the pressure data is sent through RF. However, CardioMEMS presents certain drawbacks. Firstly, the antenna size must be at least 2-3 cm for RF signals to penetrate the human body with high water content. This causes the total volume of the CardioMEMS system to be significant. Among many other ways of wireless power transmission, ultrasonic and photovoltaic power transmission methods stand out as they eliminate the huge coil in RF-based systems. For example, [3] proposes an ultrasonically powered, 1 mm cube-sized piezo capsule that uses passive elements for HF monitoring. Similarly, [4, 5] uses optically powered systems for interventional MRI applications, where low volume systems are sought, as in HF.

This work aims to develop a system to overcome the drawbacks of the CardioMEMS. First, the system was designed and built around ultrasonic for data transmission instead of RF. This eliminates the need for a large coil and reduces the overall volume. Secondly, the system is equipped with a low-power microprocessor to be programmable. The microprocessor measures the pressure using a commercially available pressure sensor [6]. The sensor not only provides pressure but also temperature data, which can be helpful for analysis. Moreover, CardioMEMS is a passive system, so it does not have helpful features like calibration and auto-correction. On the other hand, using a digital pressure sensor would enable using such features. Also, since the data is transmitted digitally, the results will be more reliable and robust.

Unlike CardioMEMS, which does not consume power in its inactive state, microprocessors consume power even in its idle state. Considering that the time between measurements is at least 60 seconds, it is important to reduce idle power as much as possible. The processor design uses a circuit-level technique called dynamic leakage suppression, which reduces idle power consumption, enabling long battery life. The processor also has its clock generator and power-on-reset, eliminating the need for crystal oscillators and reset generators. It communicates with the sensor through commonly used SPI protocol. The microprocessor has its own memory and can be programmed through UART.

The thesis will be structured as follows: a detailed explanation of power consumption sources and reduction techniques will be provided initially. Subsequently, ultra-low power circuit techniques will be explained. Lastly, the microprocessor system design and its results will be presented.

2. BACKGROUND

2.1. Power Consumption in Integrated Circuits

Power is a key metric in integrated circuits, like speed and area. The power consumption of CMOS circuits can be divided into two categories: dynamic and static power. The former is the power dissipated during the transitions in the circuit, while the latter is consumed when the circuit is not actively transitioning.

2.1.1. Dynamic Power

A circuit draws current from its supply when capacitances are charged or discharged. The current drawn leads to power consumption. Dynamic power is the type of power consumed when the state of the circuit changes. The state is the combination of all node voltages within a circuit, including all the internal and output nodes. The current drawn from a node capacitance during charging is expressed as

$$I_{charge} = Q_{node}/T = C_{node}V_{DD}/T = C_{node}V_{DD}f. \quad (2.1)$$

Using the expression obtained in Equation 2.1, the power dissipated during the change in node voltage can be calculated as

$$P_{dynamic} = I_{charge}V_{DD} = C_{node}V_{DD}^2f, \quad (2.2)$$

where C is the capacitance at the node, V is the supply voltage, and f is the frequency of the switching. However, the equation assumes that node voltage changes every period, which might not be the case. Depending on the circuit's overall state, a node within it may charge every N period. To demonstrate this detail mathematically, the dynamic power is multiplied by the activity factor, which modifies the expression as

$$P_{dynamic} = \alpha CV_{DD}^2f. \quad (2.3)$$

The activity factor is a number between 0 and 1 and indicates the switching probability of a node. For example, for $\alpha = 0.05$, the node voltage can change with a probability of 0.05 for the current period. In other words, it changes every 20 cycles. A comprehensive

understanding of dynamic power can be achieved by thoroughly examining a NAND gate, as illustrated in Figure 2.1(a). Assuming that input A is fixed at logic 1, output Y depends on input B. When B transitions from logic 0 to 1, the M3 transistor is activated, leading to a current flow from the output capacitance C_{Load} to ground. Consequently, this flow results in power dissipation.

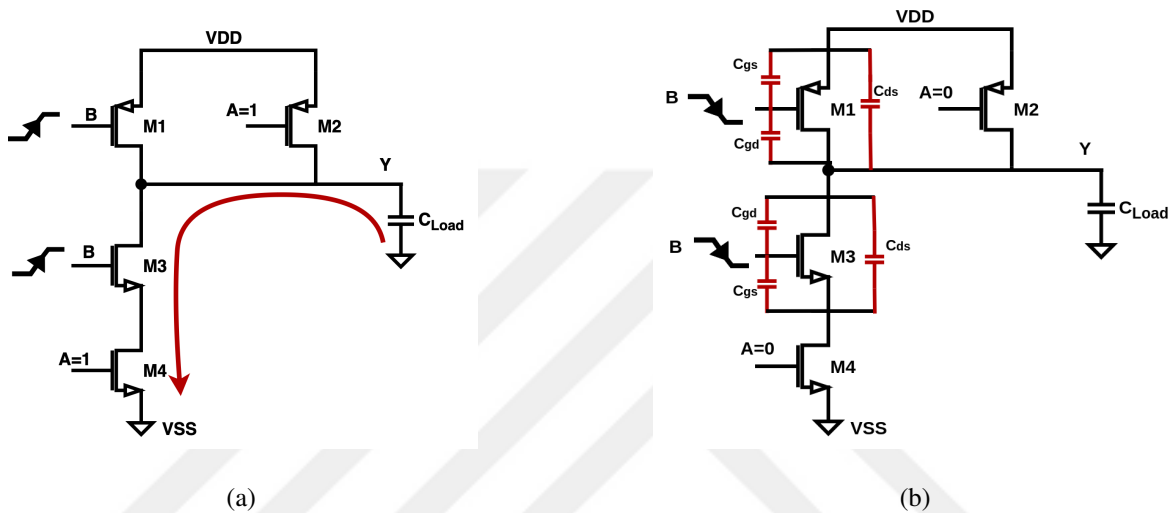


Figure 2.1. Case of dynamic power consumption in a NAND2 gate. (a) Output transition, (b) Hidden power.

However, this is not the only case of dynamic power consumption. Hidden power, a special case of dynamic power, is also quite common. The concept is shown in Figure 2.1(b). Assuming that instead of logic 1, input A is fixed at logic 0, keeping the output Y at logic 1. There will be no current flow from C_{Load} when B changes. However, parasitic capacitances like C_{gs} , C_{gd} , and C_{ds} of transistors M1 and M3 are charged, leading to relatively low but non-negligible power consumption.

In addition to capacitance charging, there is another reason for dynamic power consumption. Short-circuit power refers to the power dissipated in a circuit during a short-circuit condition. A short circuit occurs when a low-resistance path is created, typically unintentionally, between different nodes in the circuit. This low-resistance path allows for a significant amount of current to flow. To reduce it, the rise/fall times of the circuit, supply voltage, or short circuit current should be reduced. Since the short-circuit condition occurs when the transistors are in the linear region, the short-circuit current depends on the threshold voltage

of the transistors. Therefore, the threshold voltage (V_{Th}) of the MOSFETs also affects the power. Using low V_{Th} NMOS and high V_{Th} PMOS would lower the current and thus the power.

To decrease the dynamic power consumption, it is relatively easy to decrease the supply voltage, frequency, or both. Dynamic power is linearly related to capacitance, which is the sum of the output capacitance of the driver cell, the input capacitance of the receiver cell, and the wire capacitance. Using smaller transistors reduces the input and output capacitances. Wire capacitance is technology-specific, but it is possible to reduce it by using shorter wires for routing.

It is also possible to reduce the dynamic power by reducing the activity factor. This can be performed using logic restructuring. Logic restructuring rearranges the structure of logic gates within a circuit without changing its overall logic function. It is often used to optimize circuits for factors such as speed, power, or area. Logic restructuring for the boolean function $Y = ABCD$, whose inputs have a switching probability of 0.5, is a good example of it. The function could be implemented in two different ways: either three 2-input AND gates or a 3-input AND with two 2-input AND gates. For a 2-input AND gate, the switching probability at the output can be calculated as

$$P_{0 \rightarrow 1} = (1 - P_A P_B) P_A P_B, \quad (2.4)$$

where P_A and P_B are the switching probabilities of inputs A and B, respectively. Figure 2.2 shows the logic restructuring for $Y=ABCD$. It is clear that by employing 3-input AND gates, the switching probability at the output is halved, thus reducing the dynamic power. For digital circuits, restructuring is usually performed by the EDA synthesis tool.



Figure 2.2. Logic restructuring of the $Y=ABCD$ function.

2.1.2. Static Power

Static power, unlike dynamic power, is dissipated when the circuit is in an idle state. It occurs because of leakage currents within the MOSFET. Static power consumption is expressed as

$$P_{static} = V_{DD} I_{Leakage}. \quad (2.5)$$

When the gate-to-source voltage (V_{GS}) of a MOSFET is less than its threshold voltage (V_{th}), it operates in a cut-off region, also known as a sub-threshold region. Despite the absence of the channel, there is a small current flowing in the device, also known as the leakage current $I_{leakage}$. Many factors affect the leakage current, such as the physical dimensions of the MOSFET, its doping profile, threshold voltage, junction depth, gate oxide thickness, and lastly, temperature. Figure 2.3 shows the various leakage current sources in a MOSFET device.

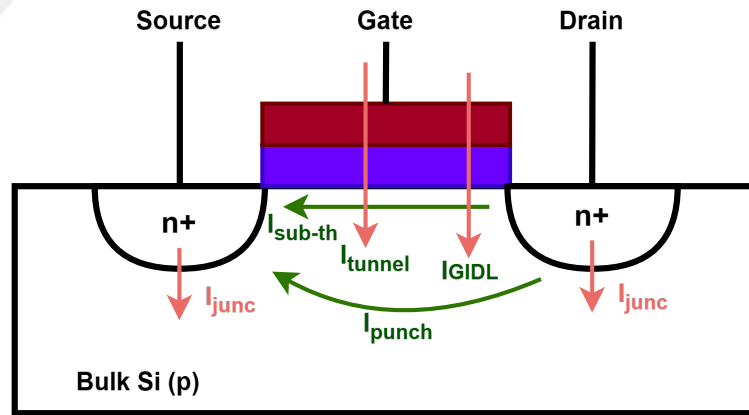


Figure 2.3. Leakage currents in MOSFET [7].

Advanced process technologies pursue smaller transistors with lower threshold voltages, which results in higher leakage current. Figure 2.4 shows the relationship between the subthreshold and the gate oxide leakage current with the gate length of the MOSFET. It can be seen that below 250 nm, the leakage current, thus static power, becomes comparable with dynamic power consumption. Therefore, especially in advanced nodes, static power needs special treatment for reduction.

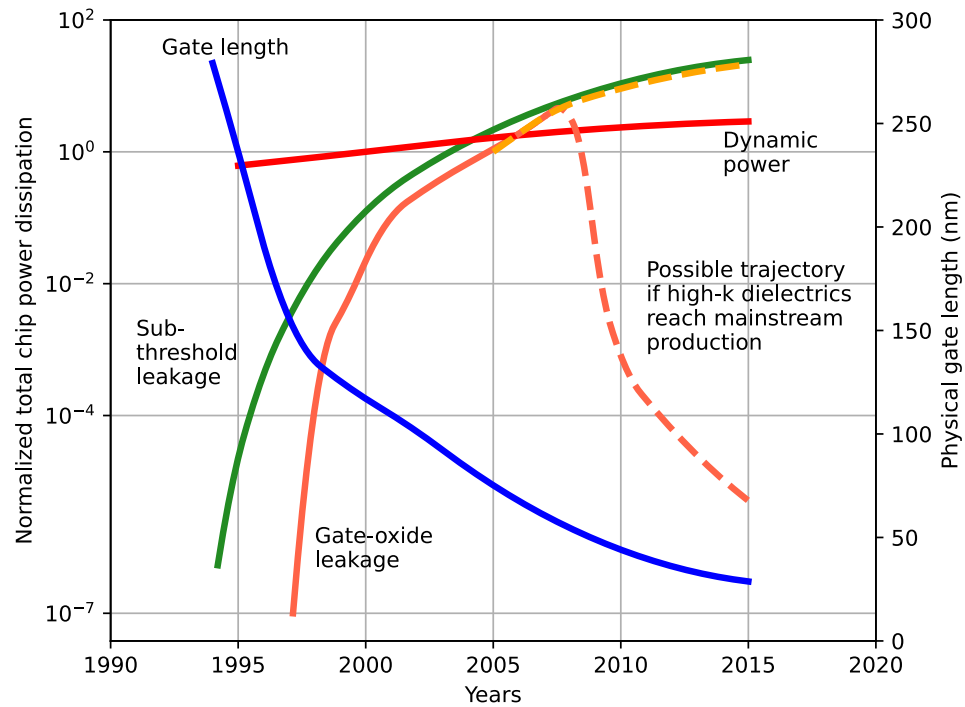


Figure 2.4. Static and dynamic power versus process technology [8].

Static power can be reduced by reducing the supply voltage. Power-gating is a power-reduction technique used in modern system-on-chips. When a circuit is not being used, its connection with the supply voltage is switched off using a power switch, as shown in Figure 2.5. Supply voltage, so the static and dynamic power of the circuit become zero. The downside of this method is the long transition times between power modes. Moreover, power gating is a technique to implement during the design stage, increasing the design costs of the chip.

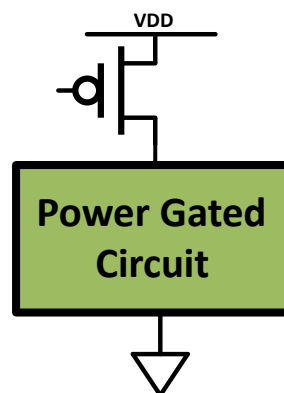


Figure 2.5. Power gating.

Other techniques leading to static power reduction are multi-threshold voltage gates and back-biasing techniques. The former is a common optimization method used in digital circuits. It uses multiple versions of logic gates, each with a different threshold voltage. Low-threshold gates have higher static power but a lower delay. Conversely, high threshold gates have lower static power but a higher delay. The method optimizes the static power of the circuit based on the utilization of the multi-threshold gates. For example, if replacing a transistor would not decrease the maximum operating frequency, i.e., it is not a critical path, the optimization method would replace the gate with a high-threshold voltage version. This increases the delay of the path but reduces the power consumption.

The back-biasing method also makes use of a variable threshold voltage. It uses the body effect of the MOSFET device. Since threshold voltage is inversely proportional to body voltage, the static power consumption of the circuit can be controlled by biasing the body.

2.2. Ultra-low Energy Circuit Design Techniques

As power emerged as the primary design constraint for modern devices, the importance of ultra-low power and energy circuits became increasingly critical. In ordinary systems without specific power consumption requirements, dynamic power typically dominates static power due to the higher clock frequencies. To reduce the power, operating the system at a slower clock may be beneficial. However, as dynamic power decreases with the frequency, dynamic and static power becomes comparable. Beyond this stage, it becomes necessary to reduce both dynamic and static power. Voltage scaling has proven to be an effective method for reducing power and energy consumption to ultra-low levels. The emergence of sub-threshold circuit design is a consequence of voltage scaling trends [9]. Compared to the linear region, the current flowing through MOSFET in the subthreshold region is very low, resulting in longer delays. Therefore, subthreshold design techniques are not the first choice in high-performance systems. However, in systems where minimal performance is acceptable but low power is crucial, subthreshold design becomes an indispensable technique. Implementing many types of circuits using subthreshold design techniques is possible, but ultra-low-power digital circuits stand out significantly.

Feasibility of subthreshold circuits for digital circuit design has emerged with Soeleman and Roy [10]. One of the first applications of digital subthreshold circuits was an FFT processor [11], which achieved functionality only with a 180 mV supply. In 2002, Deen et al. showed that it is possible to design a ring VCO with 80 mV supply voltage [12].

Ultra-low-power processors also gained attention with the emergence of subthreshold design techniques. Subthreshold logic cells have very high propagation delay, due to low current in the weak-inversion region. There is an energy-optimal V_{DD} point where the PDP is the minimum. Especially for battery-operated devices, minimum PDP is pursued for the longest battery lifetime. Zhai et al. tried to find the minimum energy point by evaluating microprocessors with different microarchitectural configurations [13]. These configurations include the width of the data path, the depth of the pipeline, or the architecture for register files and memory. Micro-controller class processors became the main target of subthreshold techniques as their need of low power operation with minimal performance requirement [14–16].

Subthreshold design techniques are applied not only to microprocessors but also to other digital circuits. SRAM-based memory circuits [17–19] are also important to minimize energy consumption. In addition to SRAMs, it is possible to design various sets of digital circuits, such as a JPEG coprocessor [20], a baseband processor for RFID processors [21], a mixed-signal system-on-chip for electrocardiogram applications [22], or a VCO-based analog-to-digital controller [23] using subthreshold techniques.

2.2.1. Transistor Stacking

Transistor stacking is a circuit technique to reduce leakage current. Each transistor in the logic gate is placed in series, acting as a single transistor with multiplied length, as shown in Figure 2.6. The technique increases the resistance of each transistor, thus reducing the leakage current.

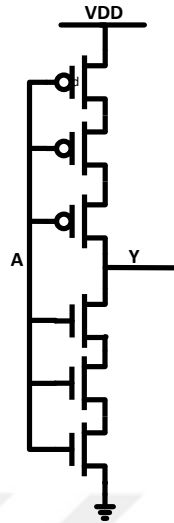


Figure 2.6. Stacked inverter example with three stacks.

As Figure 2.7 shows, the leakage current is inversely proportional to the number of stacks. It should be noted that the gain of power saving decreases with each stack. Also, the total silicon area increases with stacks, limiting the number of them the designer can use.

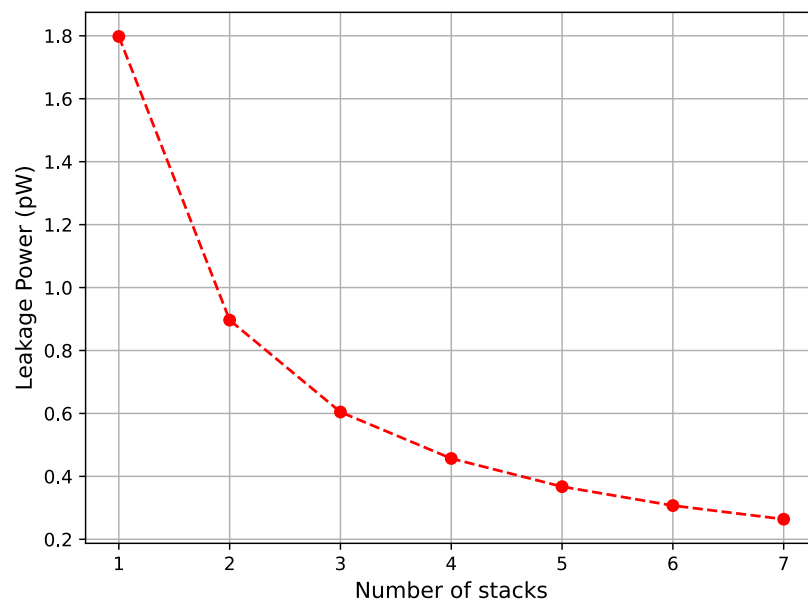


Figure 2.7. Leakage power of stacked inverter, $V_{DD}=0.3V$.

2.2.2. Negative Body Biasing

The leakage current is negatively correlated with threshold voltage, which depends on the bulk voltage of the MOSFET, which is shown in

$$V_{Th} = V_{Th0} + \gamma \sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}. \quad (2.6)$$

For the n-channel MOSFET, there is a positive relationship between body voltage and leakage current, and vice versa for the p-channel MOSFET.

In the negative body biasing technique, a negative voltage is applied to the bulk of NMOS transistors, and a positive voltage (higher than the source voltage) is applied to PMOS transistors. Therefore, the threshold voltage of each transistor increases, thus decreasing the leakage current. Figure 2.8 shows the leakage currents of an inverter for different values of bulk voltages, with a supply voltage of 0.3V. The voltage applied to V_{NB} matters when the input is 0V, i.e. NMOS is off. It can be seen that it is possible to reduce leakage power by eight times. However, it should be noted that even though it is possible to achieve low power with this technique, one requires a bias generation circuit.

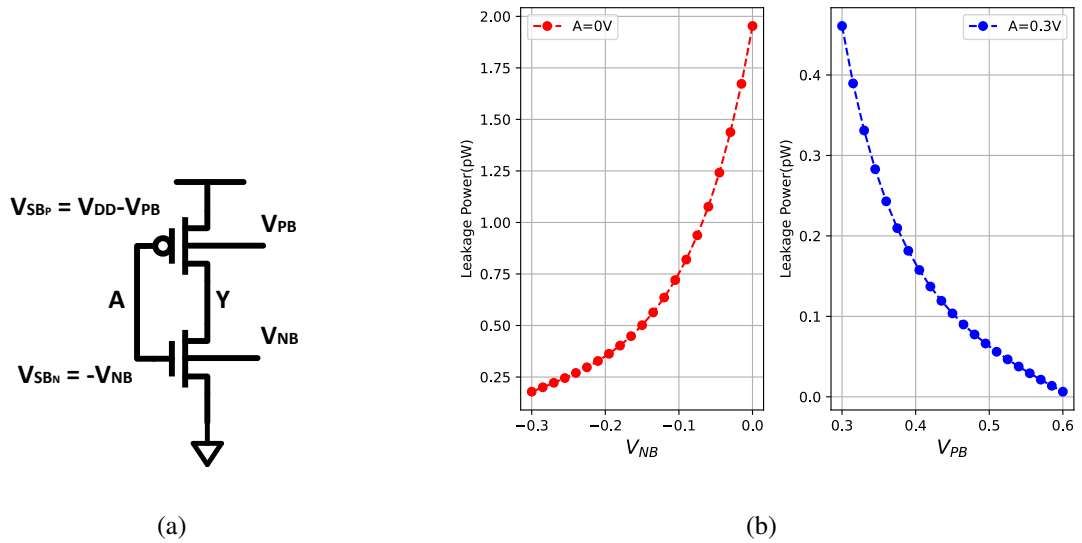


Figure 2.8. Negative body bias implementation. (a) Biasing bulk voltages, (b) Effect on leakage power.

2.2.3. Schmitt Trigger Logic

Schmitt trigger logic [24] enables ultra-low voltage operations with acceptable noise sensitivity. It resembles the transistor stacking technique, with two additional transistors forming positive feedback. A hysteresis is created by the positive feedback, enhancing the noise immunity of the gate.

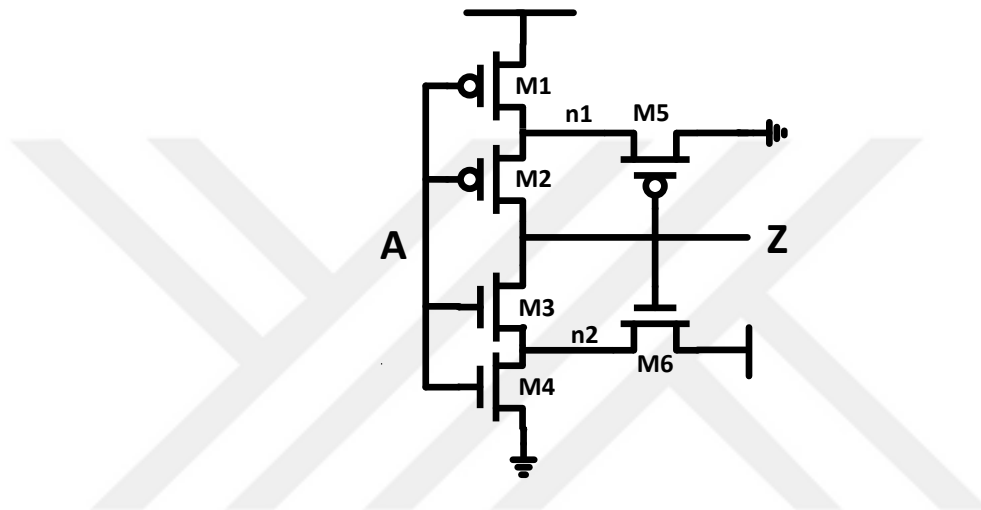


Figure 2.9. Schmitt trigger logic.

Figure 2.9 shows an inverter with Schmitt trigger logic. When the input A is 0, M6 will be on, M3 and M4 will be off. M6 will pull node n2 to V_{DD} , making V_{GS} of M3 to $-V_{DD}$, thus significantly reducing its leakage. However, the gate-source voltage of M4 is 0, still allowing a leakage to be drawn through M6 to M4. The same applies to the M5 to M1 path when input is high. So there will always be a leakage current from supply to ground, regardless of the input.

2.2.4. Dynamic Leakage Suppression

When a static CMOS logic gate is idle, either pull-up or pull-down network is on, while the other is off. Therefore, there will be a current flow from the supply to the output load, resulting in static power. Reducing the supply of static logic gates could reduce the power, but it will be difficult to maintain rail-to-rail output voltage levels in static CMOS logic. Dynamic leakage suppression technique allows for reducing supply voltage down to 200 mV,

thus enabling femtowatts of power consumption. It was first proposed in [25], without its current name DLS. Later, the technique became popular with [26]. It is straightforward to implement a logic function with the DLS technique. Normally, PMOS is used for the pull-up network in a static CMOS gate, and NMOS for the pull-down network. With this technique, an NMOS is put on top of the pull-up, and a PMOS underneath the pull-down, as shown in Figure 2.10. The structure with two additional transistors, whose gates are connected to the output node, forms a feedback mechanism.

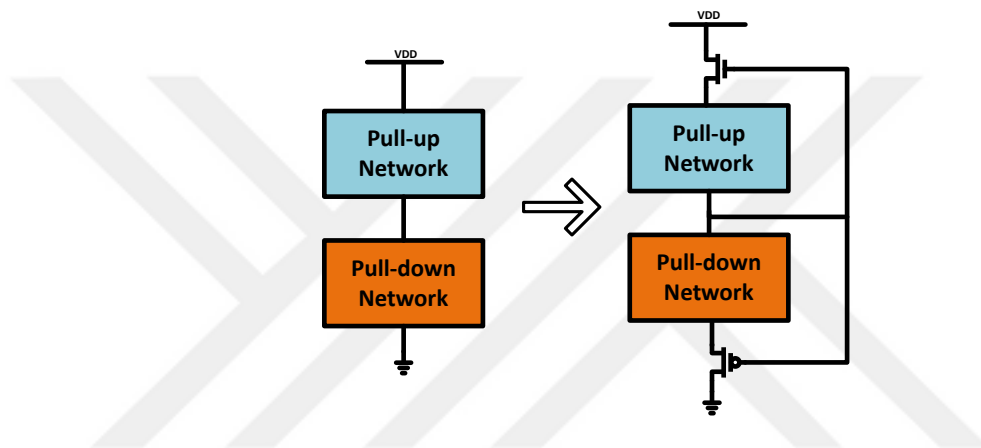


Figure 2.10. Converting a static CMOS gate to DLS gate.

There are two possible steady states in an inverter, either $IN=0$ & $OUT=V_{DD}$ or $IN=V_{DD}$ & $OUT=0$, as shown in Figure 2.11. A DLS inverter behaves differently in each of these states. Simulating the node voltages $n1$ and $n2$, the operating regions of each transistor will be better investigated.

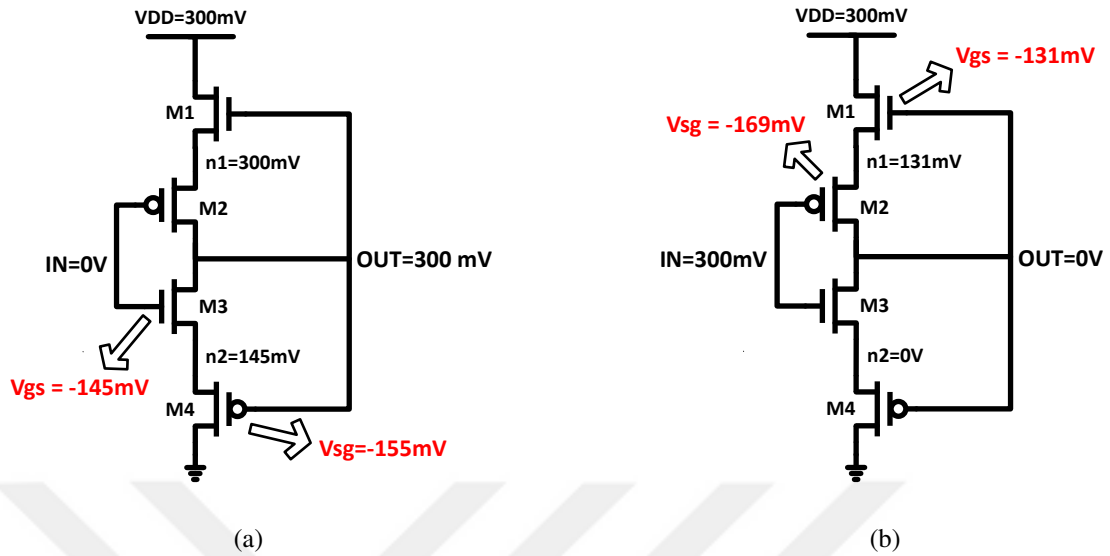
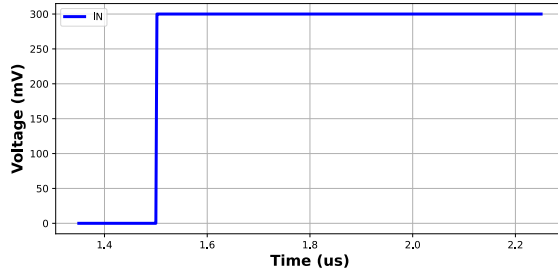
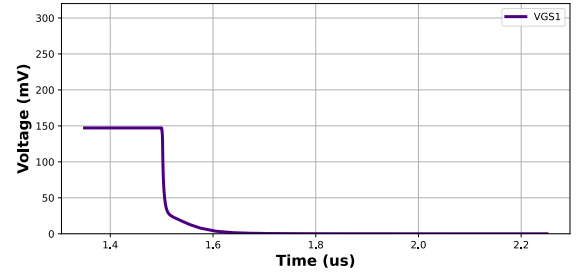


Figure 2.11. DLS inverter steady states. (a) IN=0, (b) IN=300mV.

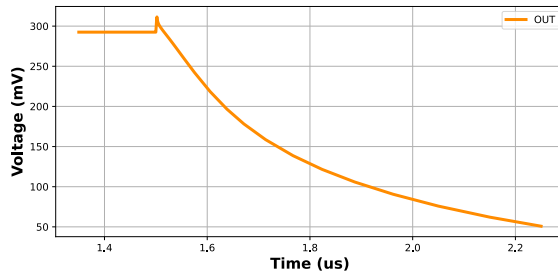
When the input is 0V and the output is 300mV, M1 & M2 are on, and M3 & M4 are off, so the leaking part is the pull-down logic. M3 and M4 are sized so that their impedances will be equal, stabilizing the n2 voltage at approximately $V_{DD}/2$, as shown in Figure 2.12. Therefore, gate-to-source voltages of M3 and M4 become negative, putting them in a super-cutoff region. The super cutoff region indicates that the V_{GS} voltage of the transistor is negative. Similarly, when the IN voltage is 300mV, M3 and M4 will be on, and M1 & M2 will be off. The simulations show that the n1 voltage sits at 131 mV, so the gate-source voltages of M1 and M3 are negative, putting them in the super-cutoff region.



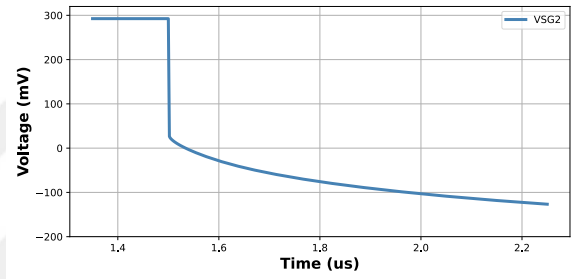
(a)



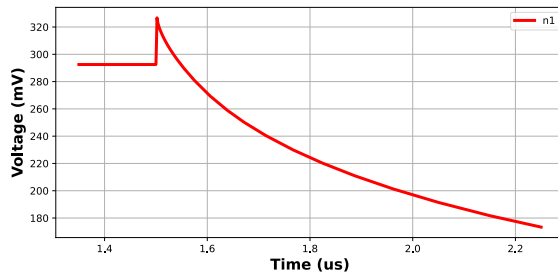
(b)



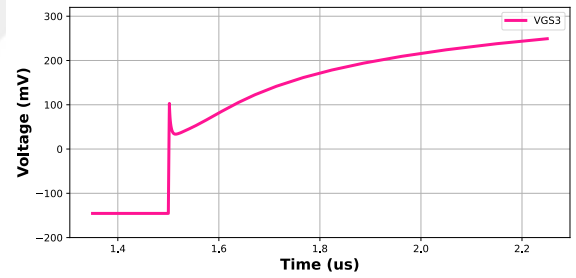
(c)



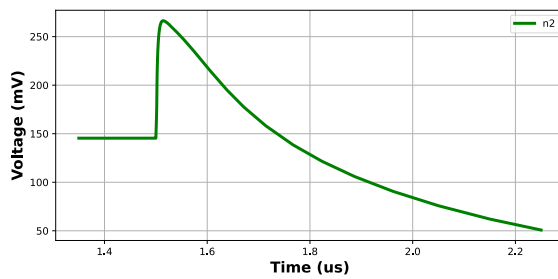
(d)



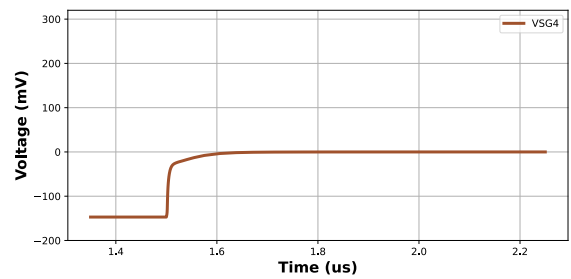
(e)



(f)



(g)



(h)

Figure 2.12. Node voltages in DLS inverter during transition. (a) IN, (b) V_{GS1} , (c) OUT, (d) V_{GS2} , (e) $n1$, (f) V_{GS3} , (g) $n2$, (h) V_{GS4} .

Figure 2.13 presents the I_D of a MOSFET against V_{GS} . It can be seen that I_D decreases exponentially for negative V_{GS} values. Due to this relationship, a transistor in the super-cutoff region leaks current in the order of picoamperes, enabling low power consumption during the steady state.

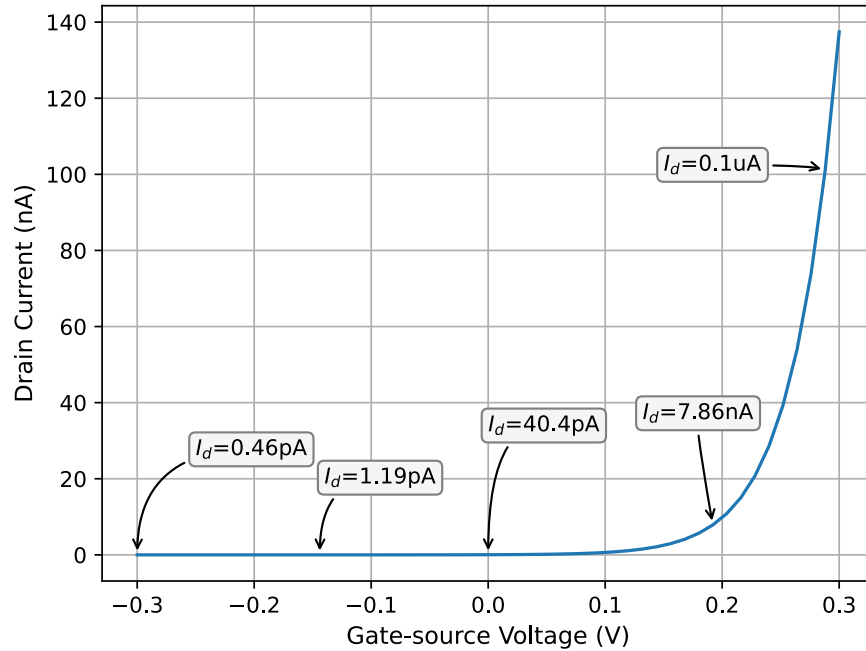


Figure 2.13. Drain current against gate-source voltage ($V_D=0.3V$).

The dynamic operation in the DLS inverter is as follows, assuming that the voltage I_N goes from 0V to 300mV:

- (i) V_{GS} of M3 increases with I_N . And at some point, it switches from super cutoff to weak inversion.
- (ii) Since M3 is in weak inversion, it will allow the charge to move from OUT to n2 until the voltages are equal.
- (iii) During the same time, as OUT drops, M4 is in a weak inversion. Thus, M4 will allow current flow from n2 to the ground and discharge the node n2.
- (iv) At the same time, M1 and M2 enter into the super-cutoff region. The former is due to an increase in I_N , and the latter is due to a drop in the OUT voltage. Also, before they enter the super-cutoff, the n1 voltage decreases.

Also, the feedback mechanism leads to DLS having different switch points of rise and fall. This increases noise margin due to hysteresis, as shown in Figure 2.14. It can be seen that the noise margin of the DLS inverter is 17% higher.

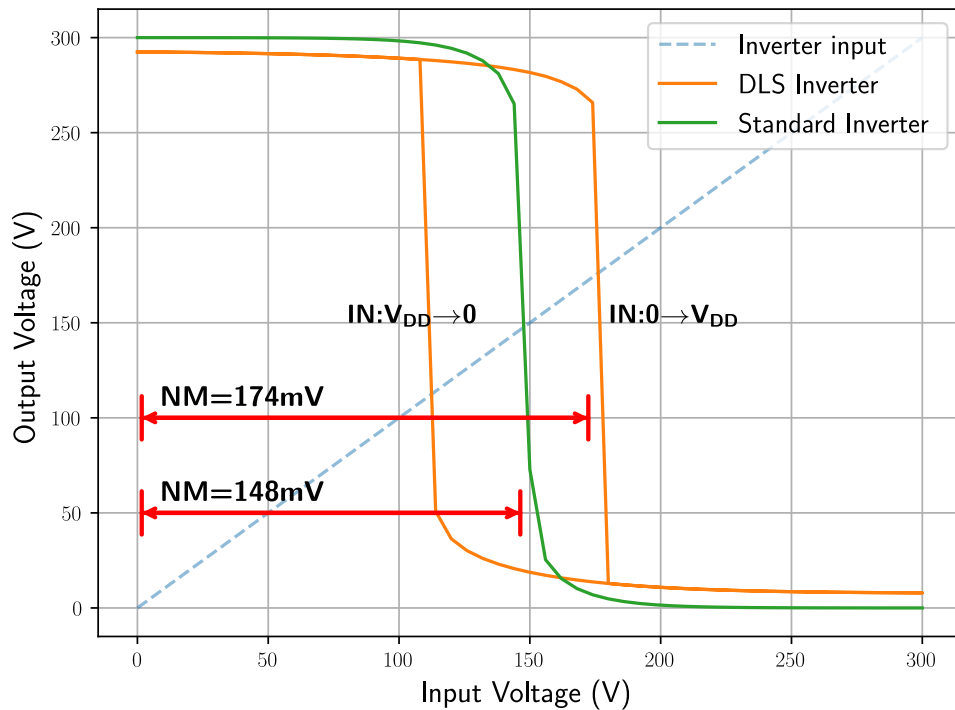


Figure 2.14. DC simulations of DLS and standard inverters.

Furthermore, due to the two cutoff devices in series, there is very low leakage. This results in drastically lower static power consumption compared to a standard CMOS inverter, as shown in Figure 2.15. Depending on the input of the inverter, a DLS inverter consumes up to 54 times less static power compared to a static CMOS inverter.

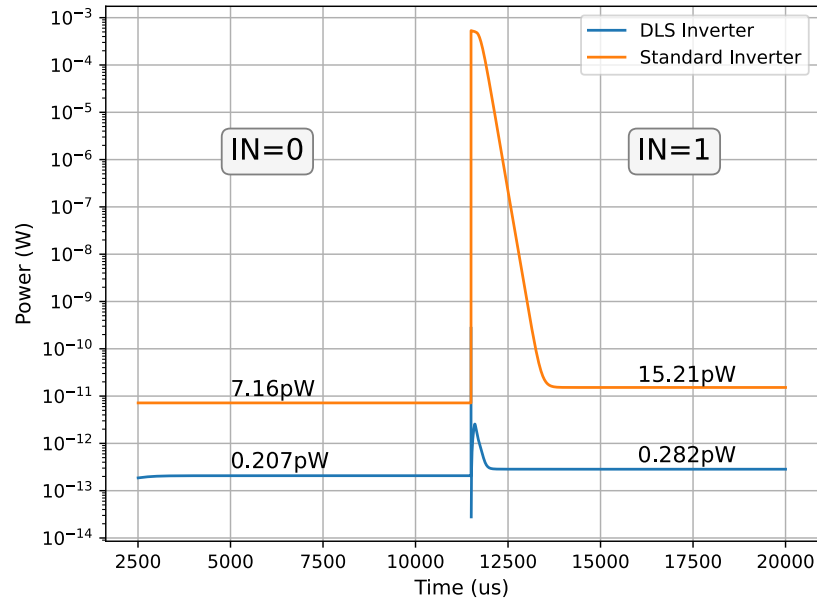


Figure 2.15. Static power consumptions of DLS and standard inverters.

As a consequence of all the benefits of the DLS technique, it is widely adopted for ultra-low energy circuits. [26] first showed the results of DLS on silicon. They implemented the DLS technique to universal logic gates; inverter, NAND, NOR, and flip-flop. Then, they synthesized and fabricated the ARM Cortex M0+ processor using the DLS standard cell library. Truesdell et al. improved the DLS technique by adding two parallel transistors to the header and footer transistors [27,28]. These transistors allow bypassing of the feedback transistors, shown in Figure 2.16. When bypassed, the gate acts as an ordinary static CMOS gate, otherwise as a DLS gate. This allows the processor to switch between fast but power-hungry active mode or slow but low-power sleep mode, improving overall energy efficiency.

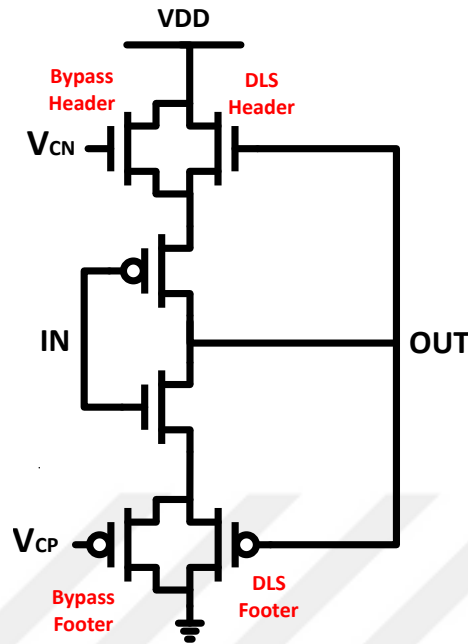


Figure 2.16. Scalable DLS gate [28].

Cerqueir et al. proposed a new logic family, called feedforward leakage self-suppression logic (FLSL), which is based on DLS [29]. The discharging delay in a DLS is very low due to super-cutoff devices, increasing its propagation delay. FLSL tries to improve the delay without sacrificing the leakage power. In FLSL, header and footer transistors are controlled by the inputs, rather than the output, as in DLS logic. So when the input switches from 0 to V_{DD} (or V_{DD} to 0), the header (footer) transistor also switches to cutoff, instead of supercutoff.

Moreover, since DLS is an easy-to-implement technique, it is utilized not only for processors, but also for static random access memories [30–32], oscillators [33–35], or even voltage doubler circuits [36].

Table 2.1. DLS performance against process technology [37].

Technology	Vleak(V)	Leakage Power(pW)	Leakage Power Reduction	Frequency(kHz)	PDP(fJ)	SNM/VDD
180 nm	0.7	0.213	42410	0.248	91.8	66%
130 nm	0.6	3.84	20416	5.92	43.8	67%
90 nm	0.3	2.34	163	0.588	9.6	53%
65 nm	0.4	3.80	365	0.838	12.4	66%
40 nm	0.3	8.97	102	2.50	6.06	58%
28 nm	0.5	466	828	135	12.5	59%
16 nm	0.5	28	1221	19.3	18.1	80%
12 nm	0.5	37	1449	28.7	17.5	80%
7 nm	0.4	95	389	32.5	10.7	74%

A DLS gate uses the subthreshold current of the transistors to discharge its output capacitance. Due to the sensitivity of subthreshold current to process technology, the performance and power of a DLS gate also depend on the process. Li et al. investigated the effect of process technology on the performance of DLS gates [37]. As Table 2.1 shows, the DLS technique reduces the leakage power significantly more in older processes. However, when compared in terms of power-delay products, the best process to use the technique appears to be 40 nm. But in leakage-power-dominated and low-speed applications, the 180 nm technology would be the most suitable choice.

3. DESIGN AND METHODOLOGY

3.1. System Design

The microprocessor system design is built around the task of heart rate monitoring. The task has several characteristics.

- There is no need to sense heart pressure every second. Periodic measurements (e.g., 60 seconds) would be sufficient for accurate monitoring.
- Data analysis is performed outside the sensor. There is no need for floating-point operations.
- Low power consumption is necessary because charging the battery after implanting is difficult.
- Since the sensor is placed in the aorta, the system should be low in volume.
- The system should be as inexpensive as possible.

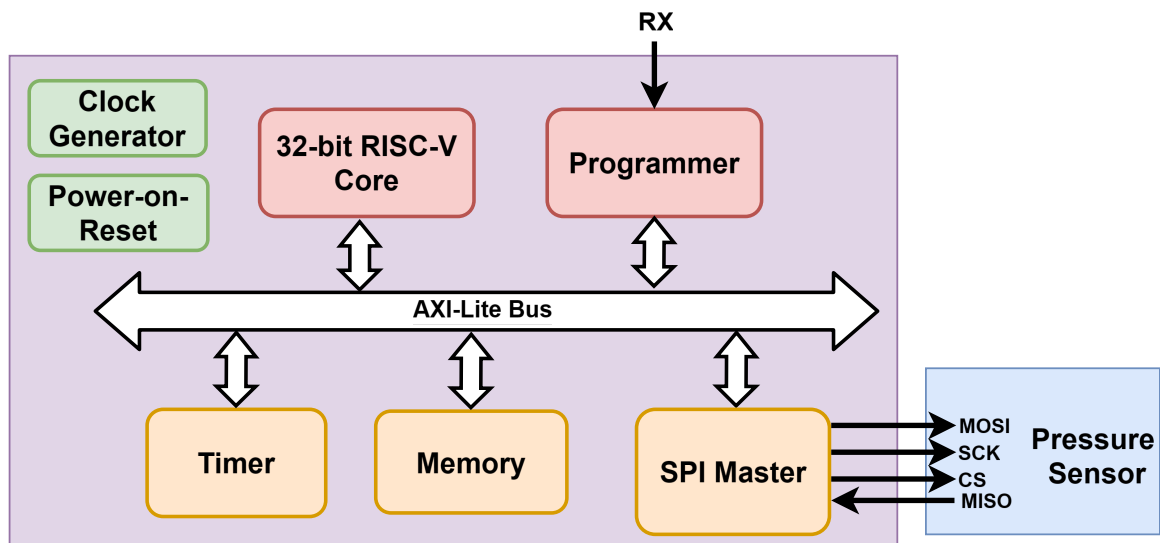


Figure 3.1. Block diagram of the ULP system.

Based on these characteristics, an ultra-low power microprocessor system is designed, as shown in Figure 3.1. The system consists of several modules. First, there is the Ibex core [38], an open-source implementation of the 32-bit RISC-V [39] architecture. The RISC-

V core is connected to peripherals via the AXI-Lite [40] bus. There are three peripherals for various tasks. First, there is the SPI master that enables communication with the Bosch BMP390 [6] to read the pressure and temperature data. Second, a timer module stops the system for a programmed number of seconds. Third, there is register-based memory to hold the instructions and data of the program that the RISC-V core executes. In addition to peripherals, a programmer module programs the RISC-V processor via UART protocol. Finally, two analog blocks, a clock generator and a power-on-reset block, supply clock and reset signals to the system.

The standard cells on the chip are designed using the DLS technique. This reduces the static power consumption of the chip, which helps reduce overall energy, especially considering that the chip sleeps for long periods between measurements. Moreover, the DLS technique reduces the supply voltage, reducing static and dynamic power consumption.

The microprocessor chip is designed using a commercial 180-nm process. This process was chosen for two reasons: First, it has lower subthreshold leakage than the more modern processes, creating an advantage for power consumption, as shown in Table 2.1 and Figure 2.4. Second, it is low-cost and easily accessible, making it a feasible choice for the project.

Although the pressure sensor supports the SPI and I2C protocols, the microprocessor system uses the former. The rationale behind this decision is that I2C requires open-drain I/O, while it is possible to use SPI with a push-pull interface. Because the designed system operates at a low frequency, the pull-down transistor at the I/O would be open most of the time, which creates a current flow through the pull-up resistance. A higher-value resistor could have been chosen to reduce current consumption, but this would have increased the volume of the sensor system. Therefore, the SPI protocol is selected to communicate with the pressure sensor for power and volume reasons.

3.2. Design of Digital Blocks

3.2.1. RISC-V Processor

The Ibex core is the center of the system-on-chip. It is a highly configurable 32-bit RISC-V core written in SystemVerilog. It is suitable for all applications in which a microcontroller is ideal for simple control tasks. It has a two-stage pipeline with an optional third pipeline stage to reduce critical paths. It is RV32I by default but can be configured as RV32E. RV32E decreases the number of registers from 32 to 16, significantly reducing the silicon area. Core also has the RISC-V M extension, which allows it to multiply and divide 32-bit numbers. It can be equipped with the RISC-V B extension, accelerating bit manipulation operations. It also has the option to enable instruction cache, which reduces memory access times. Figure 3.2 shows the block diagram of the Ibex core.

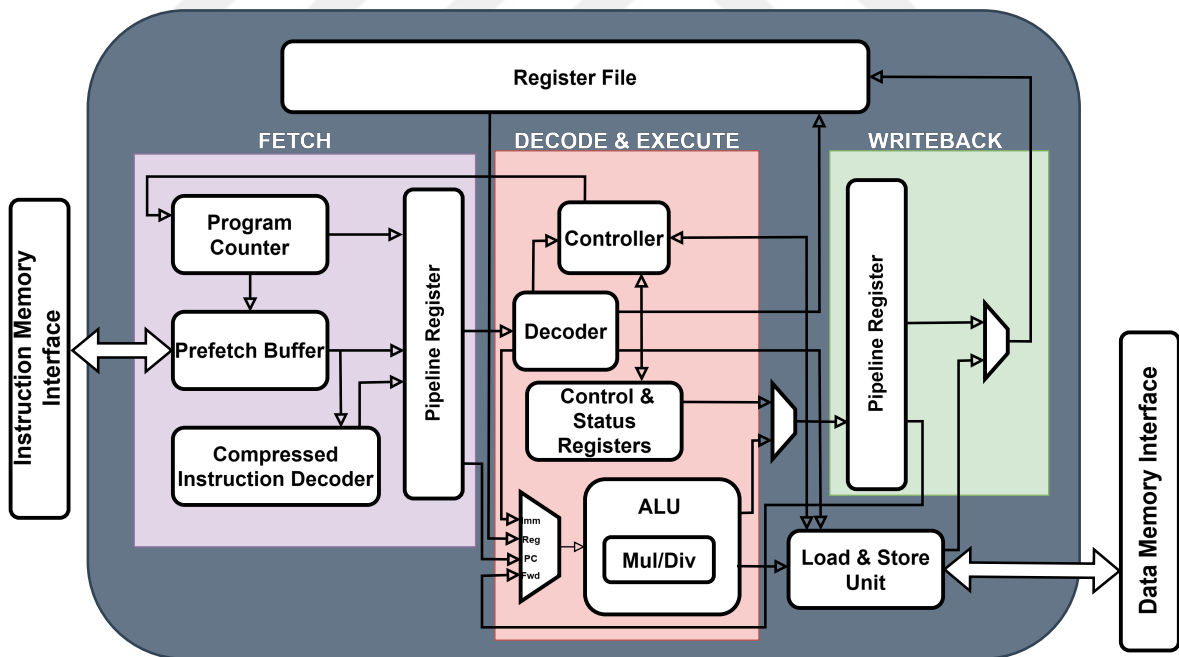


Figure 3.2. Block diagram of the Ibex core [38].

It is possible to configure the parameters based on needs. For instance, the Ibex core is configured for the minimum silicon area possible for the ULP system design. The RISC-V M and B extensions, instruction cache, and branch predictor are disabled to reduce the complexity and, thus, the total number of logic cells. The core is configured as RV32E instead

of RV32I. All these design choices reduce the performance of the Ibex but also significantly reduce the area. Accordingly, the Ibex core is implemented in silicon with three different configurations, called "micro," "small" and "maxperf." The features of these configurations are shown in Table 3.1.

Table 3.1. Ibex configurations.

Config	"micro"	"small"	"maxperf"
Features	RV32EC, no mult	RV32IMC, 3 cycle mult	RV32IMBC, 1 cycle mult, Branch Target ALU, Writeback stage

3.2.2. Programmer

The most important advantage of the system compared with others, such as CardioMEMS [2], is its programmability. The programmer module is a module for that feature. At a high level, it receives the program through the UART protocol and writes the incoming program to memory through the AXI-Lite bus. Figure 3.3 shows the block diagram of the programmer.

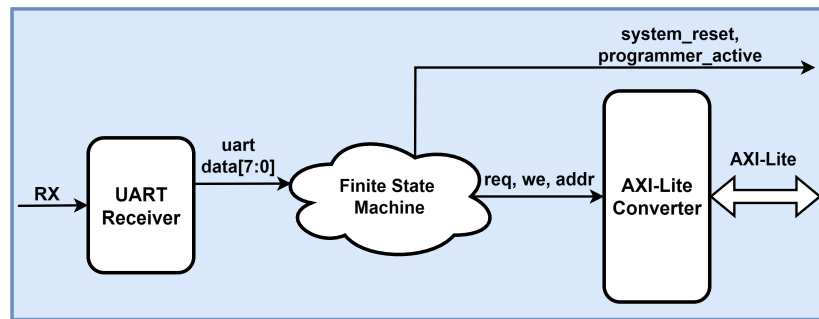


Figure 3.3. Block diagram of the programmer.

The programmer consists of three main blocks. A simple UART receiver produces single-byte data. A finite-state machine operates depending on this data. Initially, FSM waits in the reset state for a predefined word, which is *OPTLINK*. Then, it waits for the number of 32-bit words in the program, which sets an internal counter. Then, the programmer packs four bytes into a single 32-bit word and issues a write request to the memory through the AXI-Lite converter block. There are also two additional output signals: *system_reset* and *programmer_active*. After the programming, the former resets the RISC-V core to ensure execution starts at the correct program address. The latter is a status signal used in clock

gating to reduce the dynamic power of the chip. Figure 3.4 shows the state diagram of the module.

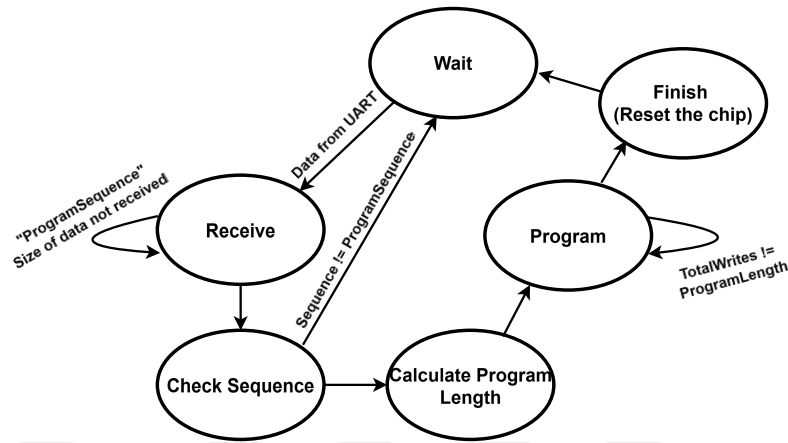


Figure 3.4. State diagram of the programmer.

3.2.3. SPI Master Interface

The SPI block enables communication with the pressure sensor device. It comprises a register file, an SCK clock generator, and a state machine for driving data. Figure 3.5 shows the block diagram of the SPI module. A finite-state machine, configurable through software, drives all SPI signals. In addition, there are two FIFO buffers to hold the read and write data.

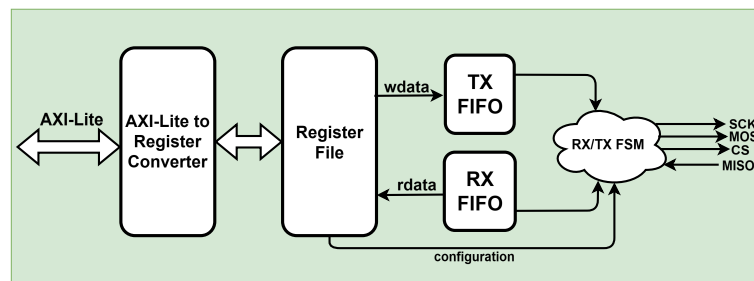


Figure 3.5. Block diagram of the SPI.

3.2.4. Timer

The timer module is fully configurable. The programmer can set the counter's upper limit and step size. It can also divide the frequency of the counter ticks. Figure 3.6 shows the timer block diagram. It consists of three parts: a register file for interfacing with the

software, a prescaler for dividing the master clock, and a counter.

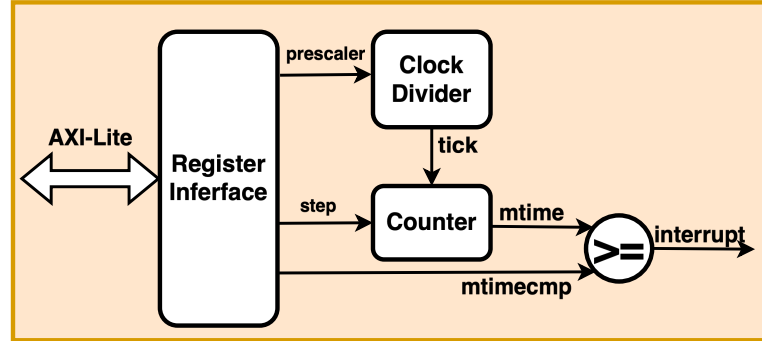


Figure 3.6. Block diagram of the timer.

The clock divider divides the master clock frequency by the *prescaler* value. Then, this divided clock is fed into a counter, which increases the counter by the *step*. The counter value, *mtime*, is compared with *mtimecmp*. If it is higher, the output signal *interrupt* raises high. This signal is connected to the RISC-V core to wake up the core after a long idle period.

3.3. DLS Standard Cell Library

3.3.1. Standard Cell Design

A DLS standard cell library is designed to minimize the system's standby power. Each standard cell is optimized for the lowest power delay product to achieve the highest energy efficiency. It is sufficient to have an inverter, NAND, NOR, and DFF to implement an arbitrary Boolean function. However, this approach increases the total number of cells required. Unlike [26], which has only these four gates in its library, the library designed for this thesis consists of 13.

- Inverter (INV)
- Buffer (BUF)
- D Flip-Flop (DFF)
- AND2/3
- OR2/3
- NAND2/3
- NOR2/3
- And-Or-Invert (AOI22)
- Or-And-Invert (OAI22)

Using a richer set of gates during the logic synthesis reduces the logic depth, i.e., the number of combinational gates between two flip-flops. This increases the maximum operating frequency of the chip and reduces the total power consumption and area. Figure 3.7 shows how an AOI22 gate reduces the logic depth and the number of transistors.

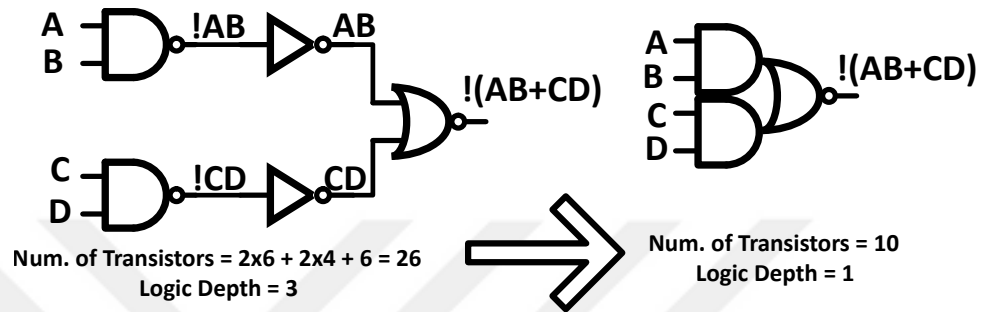


Figure 3.7. Logic optimization with AOI22 gate.

The chip's supply voltage is 0.3 V, which is selected to minimize the power delay product and to converge the rise and fall times of the standard cells. The PDP of the DLS inverter for various supply voltages is shown in Figure 3.8.

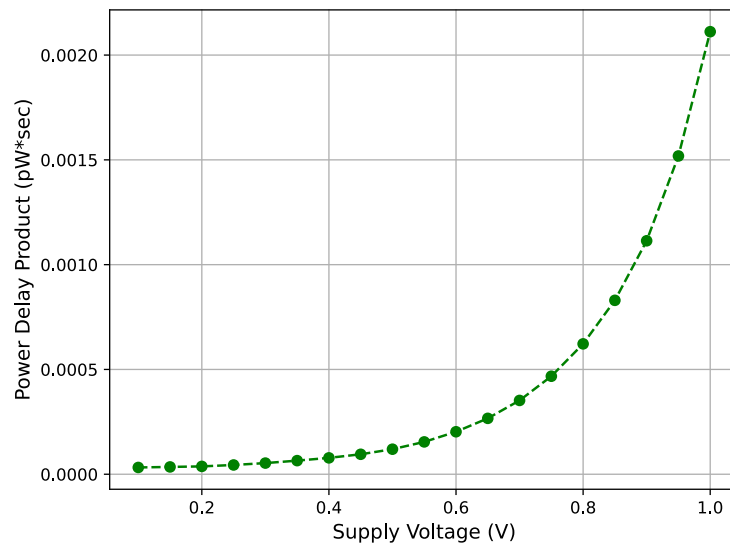


Figure 3.8. Power-delay product of the DLS inverter.

Delay equality, i.e., the adjacency of rise and fall times, is also calculated for different supply voltages. It is a figure of merit expressed as

$$DE = \frac{t_{rise} + t_{fall}}{2|t_{rise} - t_{fall}|}. \quad (3.1)$$

Although 0.1V or 0.2V appears to be the best choice for supply voltage due to low PDP, when delay equality is also taken into account, 0.3V as the supply voltage becomes the most suitable choice, as shown in Figure 3.9.

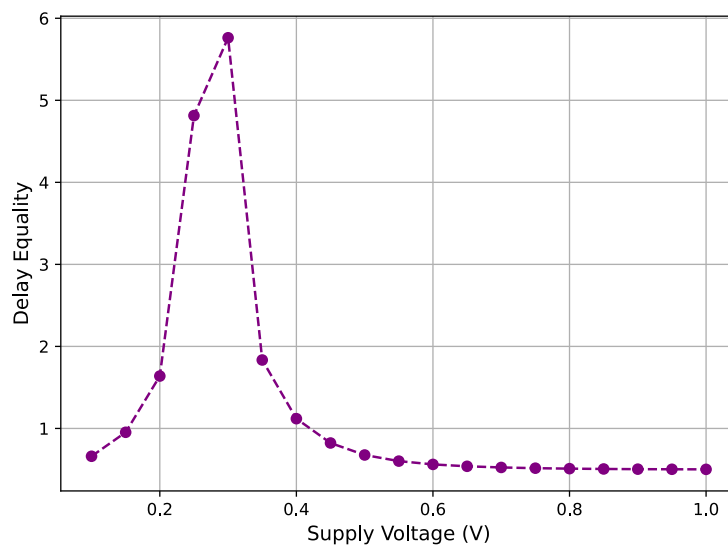


Figure 3.9. Delay Equality of the DLS inverter.

Furthermore, there are multiple restrictions on a standard cell layout design. The automatic place-and-route tools used for the chip require the heights of each standard cell to be constant. The tools place cells into rows with fixed height, reducing placement's computational complexity. The height and width of the cells should be a multiple of $0.56 \mu m$, which is determined by the 180 nm process used. The DLS standard cells have an NMOS on top of the pull-up network and a PMOS on the bottom of the pull-down network. It is implausible to merge all PMOS transistors into a single bulk, as their bulk voltages are different, so they must be separated. This limitation naturally increases the height of the DLS cells. Therefore, the standard cells' height is $7.84 \mu m$, corresponding to 14 tracks. Figure 3.10 shows the comparison of sizes of a DLS inverter and an inverter from the foundry library. Appendix A introduces the symbol, schematic, and layout of each standard cell in the library.

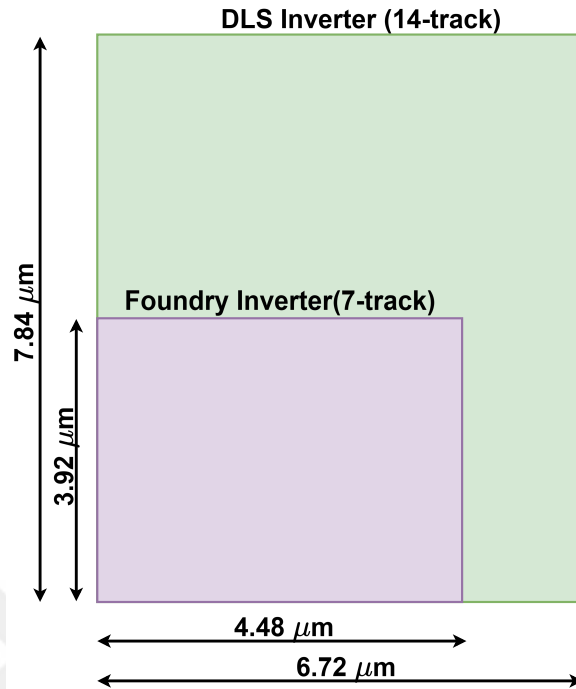


Figure 3.10. Size comparison of DLS and foundry inverters.

Moreover, subthreshold variance is an important aspect that needs to be considered. Since parameters like threshold voltage or leakage current highly depend on the process, the performance of a DLS standard cell also depends on the process. So, a series of Monte Carlo simulations are performed to investigate the tolerance of the DLS standard cell against the process variance. Table 3.2 shows the leakage power of the cells for Monte Carlo simulations with 5000 samples. Also, Figure 3.11 shows the Monte Carlo simulation for the average power consumption of the DLS inverter.

Table 3.2. Mean and standard deviation of standard cell leakage powers.

	INV	BUF	DFP	NAND2	NAND3	AND2	AND3	NOR2	NOR3	OR2	OR3	AOI22	OAI22
$\mu(\text{fW})$	433.6	624	1312	245.5	281.7	260.5	811	188.9	251.1	293.6	530.4	213.2	249.2
σ/μ	0.233	0.352	0.060	0.050	0.082	0.348	0.47	0.055	0.078	0.83	0.255	0.066	0.062

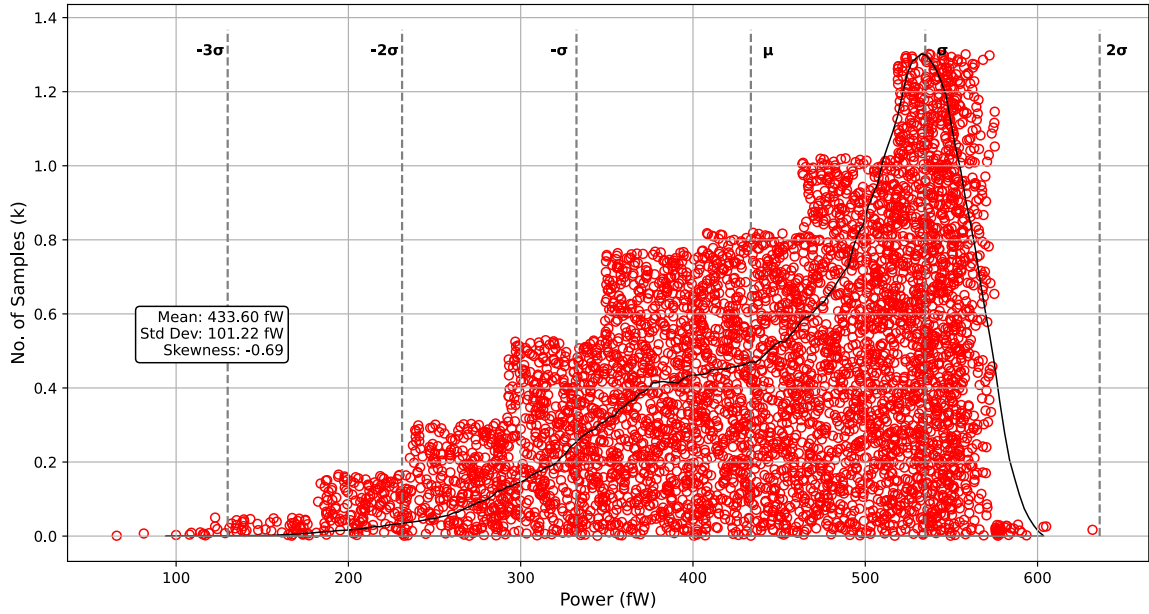


Figure 3.11. Monte Carlo simulation for average power of DLS inverter.

Additionally, to evaluate standard cells against process variation even further, another Monte Carlo simulation is performed against a gate-level full adder circuit. Figure 3.12 shows the full adder circuit built with DLS standard cells.

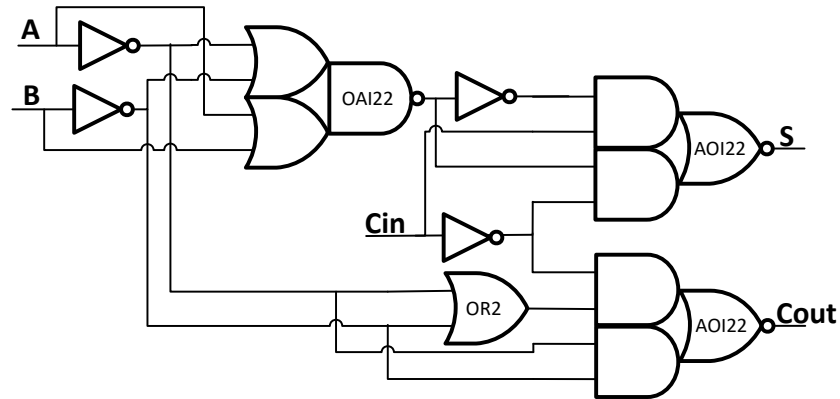


Figure 3.12. Full adder with DLS gates.

For all input combinations of the full adder inputs, the output voltages S and C_{out} are compared against their expected voltage levels. The circuit is assumed to drive a DLS inverter, so logic high voltages are expected to be higher than V_{IH} of the inverter and lower than V_{IL} for logic low voltages. A sample is labeled as passed if it works for 16 combinations

of its inputs. After a Monte Carlo simulation with 5000 samples, 91.32% of them properly work for all combinations of inputs. The distribution of output voltage S when the inputs are $A=1$, $B=1$, and $C_{in}=1$ can be seen in Figure 3.13. The outputs lower than 174 mV, V_{IH} of the inverter, are labeled as failed.

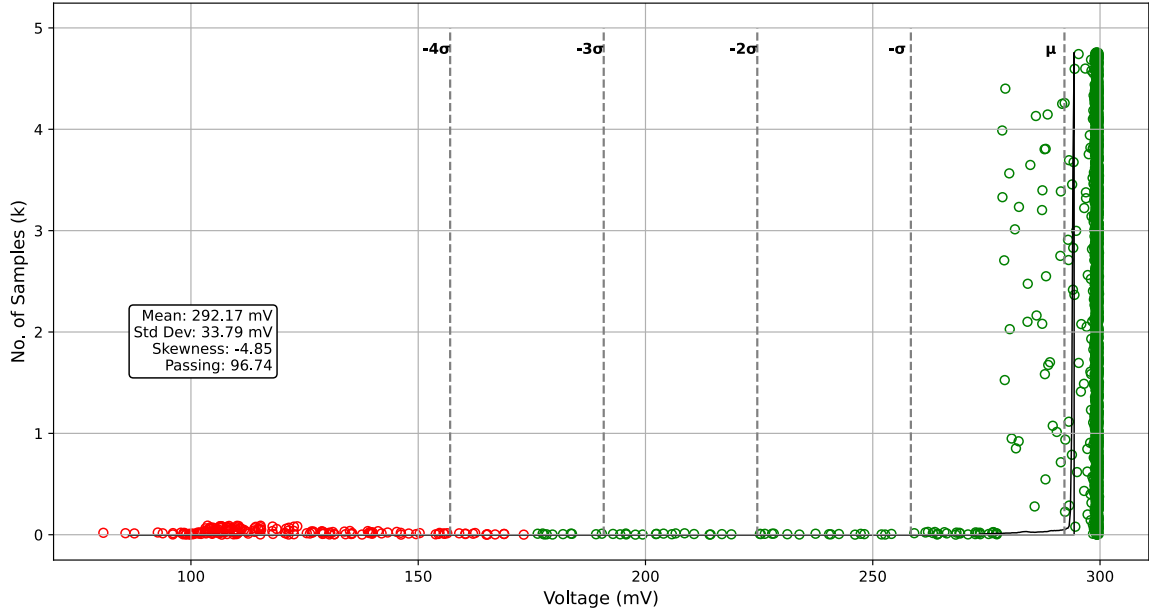


Figure 3.13. Distribution of output voltage S for the case $ABC_{in}=111$.

3.3.2. Library Characterization

Automatic synthesis tools are used during the logic synthesis of the RISC-V processor. During the procedure, the tools need a timing constraint that typically includes the maximum period of the clock signal. STA ensures the synthesized circuit can operate at the given clock frequency. Therefore, the synthesis tool needs to know the propagation delay of each cell in the library. However, the tool does not perform transistor-level analysis during STA. Instead, it uses the timing abstraction of cells, usually stored in Liberty (.lib) files. Library characterization is the process that generates the Liberty files, which makes it an essential step in the design process.

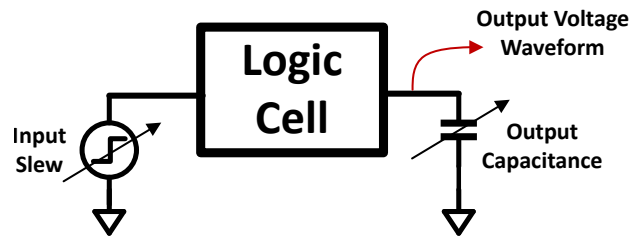


Figure 3.14. NLDM setup.

There are multiple characterization methodologies. However, for the scope of the thesis, the NLDM method is employed. As the setup in Figure 3.14 shows, a stimulus is applied to logic cells with various input slew and output capacitances. Then, the propagation delay for a particular slew/capacitance pair is calculated. The method then creates a 2-D look-up table with input slew and output capacitance indices. The synthesis tool calculates the propagation delay of a cell using this table. The circuit driving the cell determines the input slew. For example, if an inverter drives the NAND2 gate, the inverter's output transition becomes the input slew of the NAND2 gate. Likewise, output capacitance is determined by the gates driven. For instance, if the NAND2 gate drives three other gates, the output capacitance becomes the sum of the input capacitances of these gates and the wire capacitance. The synthesis tools interpolate the delay value for the slew/capacitance values that do not exist in the table. Figure 3.15 shows an example look-up table from a Liberty file, where `index_1` values are input slews and `index_2` values are output capacitances.

Table 3.3. PVT ranges of the characterization.

Process	Voltage (V)	Temperature(° C)
TT, FF, SS	0.27, 0.3, 0.33	25, 30, 35, 40, 45

The ULP heart rate monitoring ASIC is expected to operate in the body temperature range. Thus, standard cell netlists are characterized in this range. Table 3.3 shows the corners where the characterization is performed.

```

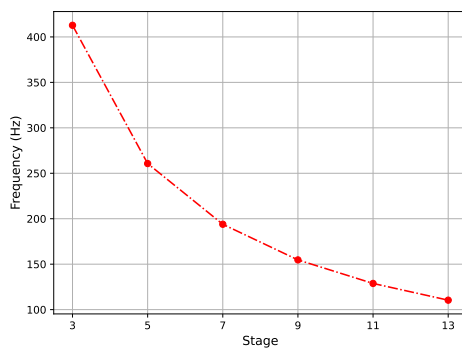
cell_rise (delay_template) {
  index_1 ("2100, 4500, 20000, 50000, 90000, 200000, 500000");
  index_2 ("0.0012, 0.0033, 0.0067, 0.017");
  values ( \
    "208450, 275682, 386729, 724042", \
    "206180, 273106, 384032, 721067", \
    "191212, 256531, 365727, 701246", \
    "159999, 222626, 328093, 659607", \
    "123298, 180898, 281170, 604404", \
    "90212.3, 126968, 197257, 472141", \
    "77994.5, 102327, 146001, 312667" \
  );
}

```

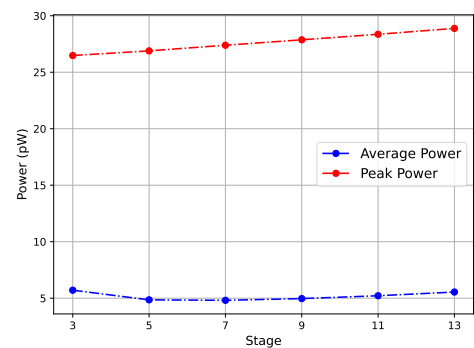
Figure 3.15. Look-up table example.

3.4. Clock Generator

Every synchronous circuit needs a clock signal to operate. Usually, a clock is applied to the chip from a crystal oscillator. However, oscillators can have high volumes, depending on their frequency. Also, considering the system operates below 1 kHz, a crystal oscillator may be unnecessary. Therefore, an on-chip clock generator is designed using the DLS technique. One of the simplest ways to generate a clock signal is by using a ring oscillator, which is a ring structure in which an odd number of inverters are connected. During the design stage, oscillators with different numbers of inverters are simulated. Figure 3.16 shows the oscillation frequency and power consumption for an increasing number of stages. Increasing the number of inverters appears beneficial as it decreases the oscillation frequency with a negligible addition to the static power of inverters.



(a)



(b)

Figure 3.16. Frequency and power of DLS ring oscillator for various number of stages. (a)

Oscillation frequency, (b) Oscillation power.

Moreover, an inverted buffer with a transistor stacking technique is used at the output to obtain a clock signal with sharp clock edges, i.e., low rise and fall times. Figure 3.17 shows the schematic and layout of the DLS ring oscillator.

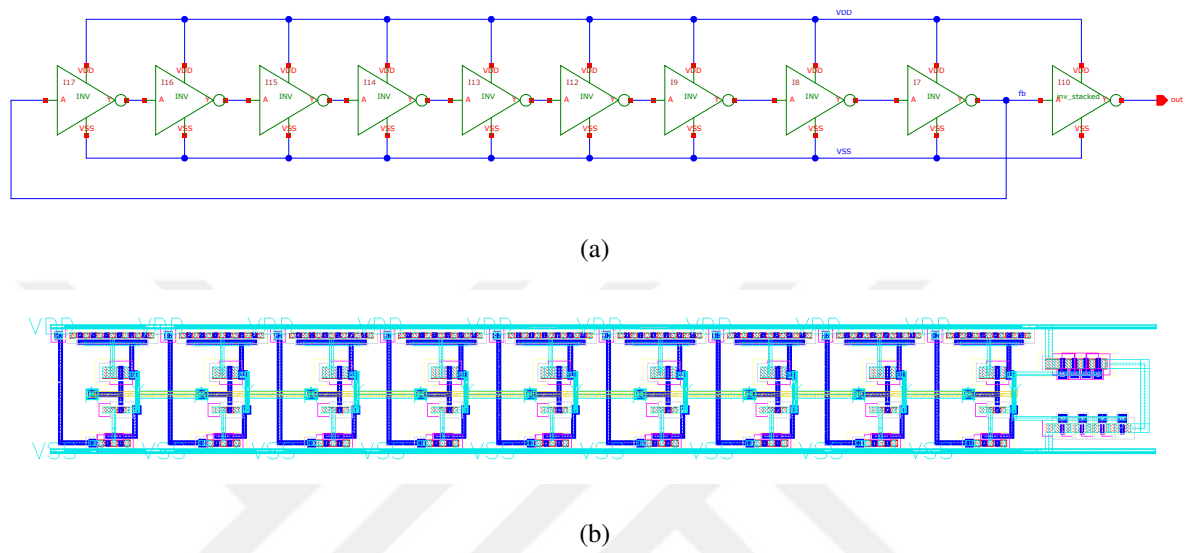


Figure 3.17. Layout and schematic of DLS ring oscillator. (a) Schematic, (b) Layout.

Figure 3.18 shows the power consumption and frequency of the oscillator for different PVT corners. These results show that oscillation frequency, thus the power consumption, increases either with temperature, voltage, or a faster process.

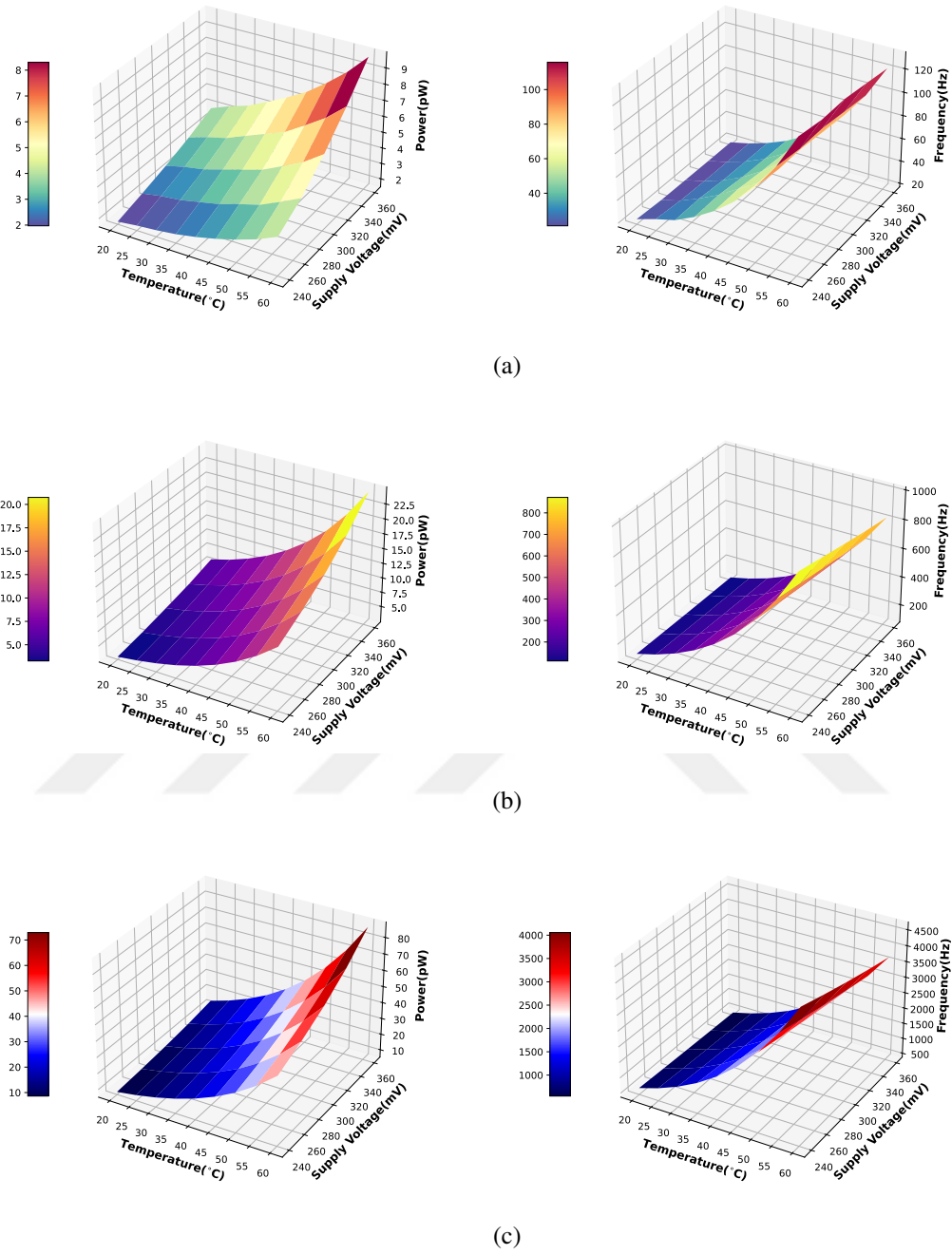


Figure 3.18. DLS ring oscillator power and frequency in different corners. (a) SS, (b) TT, (c) FF.

3.5. Power-on-Reset

Resetting the digital circuits is a crucial task. The state of the supply voltage during the assertion of reset affects the initial logic values of the flip-flops. Therefore, the designer must ensure that reset is asserted after the supply voltage is stable. For this purpose, a power-on-reset circuit is a standard block in ASICs. The reset signal for the entire chip comes from the POR, and the POR asserts the reset until the supply increases to V_{DD} . Therefore, it is ensured that when the reset is de-asserted, the supply is stable, which means the chip starts at a known state initially.

Since the system requires ultra-low power, the quiescent power of the POR is critical. Therefore, [41] is adopted and ported to 180-nm technology. Figure 3.19 and Figure 3.20 show the circuit schematic and layout, respectively.

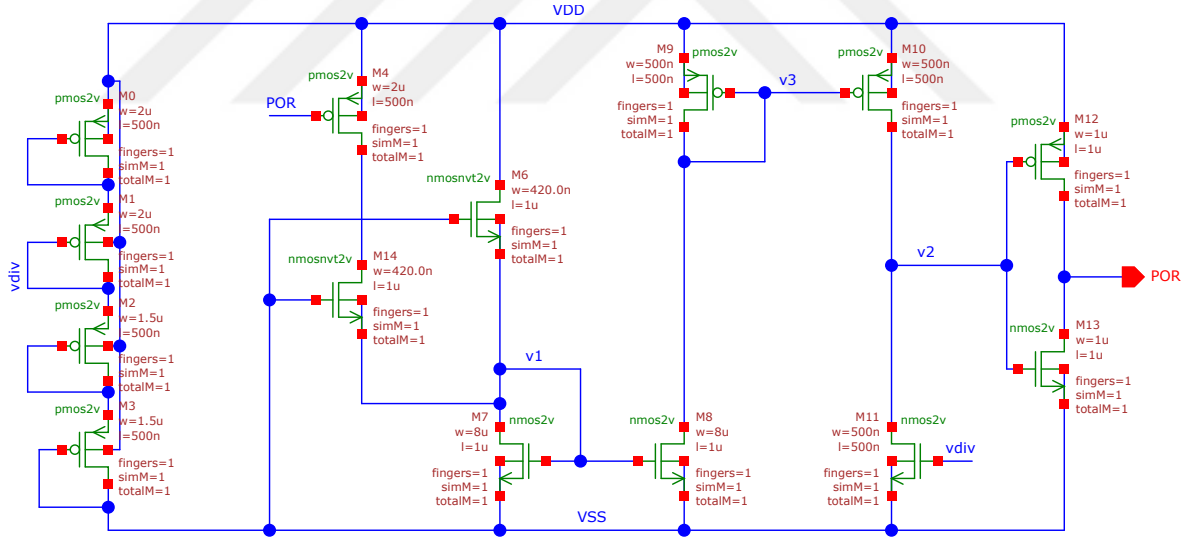


Figure 3.19. Schematic of POR.

There are two native NMOS devices, M6 and M14, whose gates are grounded. Sub-threshold leakage of these two NMOS adds up at M7, which becomes a reference current. Two current mirrors, composed of M7 & M8 and M9 & M10 pairs, replicate this current to the v2 node. Initially, when the value of V_{DD} is low, v2 is pulled to V_{DD} by the current mirror, setting the POR signal to low. The divided voltage V_{DIV} increases with V_{DD} . After a particular value of V_{DD} , called the trip point (V_{POR}), M11 will start to pull v2 to the ground,

raising the POR.

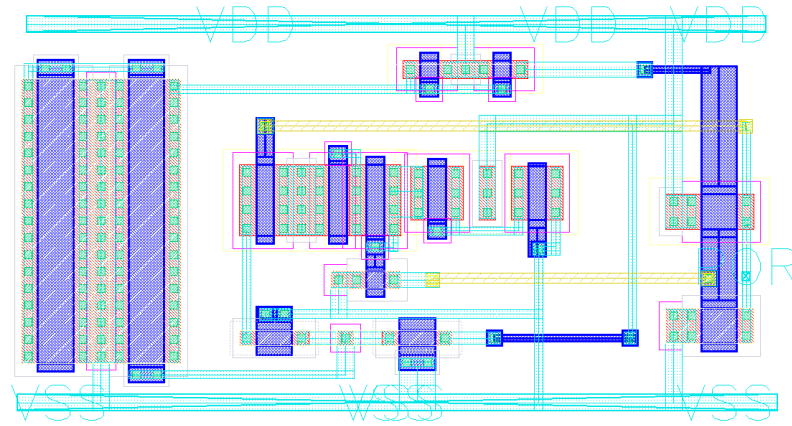


Figure 3.20. Layout of POR.

The POR circuit used also has a brownout detection mechanism. When V_{DD} decreases, M11 will eventually be off with decreasing V_{DIV} . An important point is that the reference current, in this case, is lower due to the inactive M4 transistor. This results in a different trip-voltage for brownout detection (V_{BOD}), thus creating a hysteresis. Figure 3.21 shows the transient simulation of the POR.

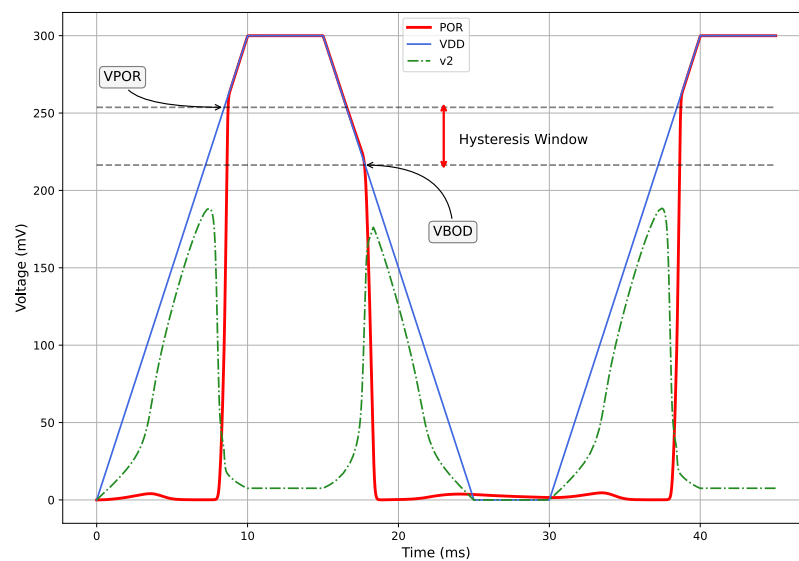
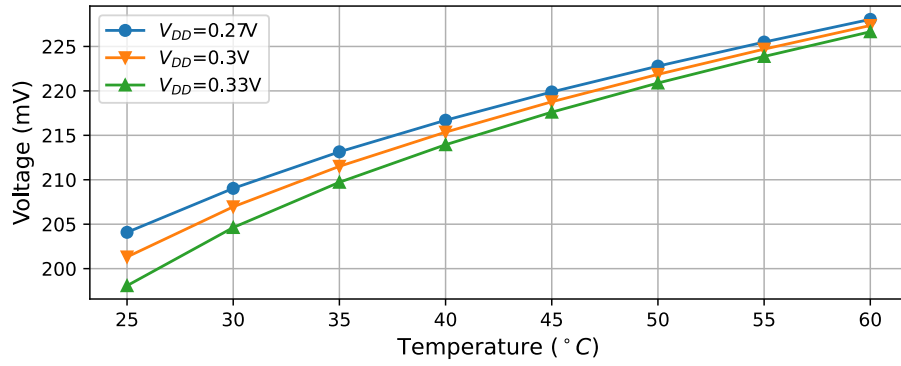


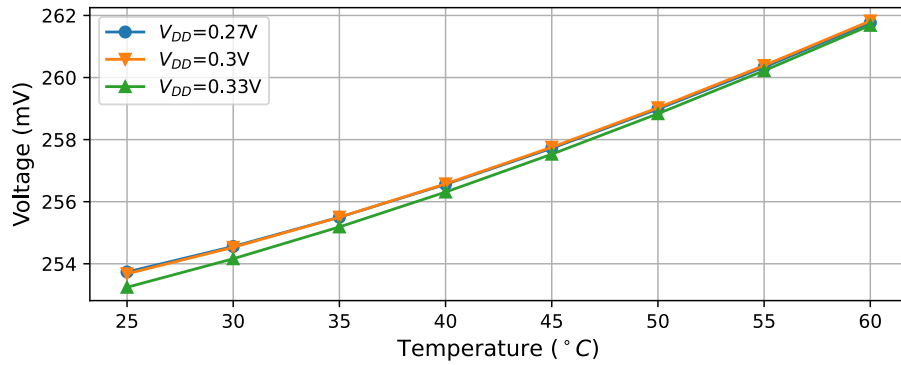
Figure 3.21. Transient Simulation of POR.

The variance of V_{POR} and V_{BOD} against voltage and temperature is another critical point that needs to be investigated. As shown in Figure 3.22, both trip points increase with

the temperature and decrease with the supply voltage. Also, the tolerance of V_{POR} appears to be higher than V_{BOD} .



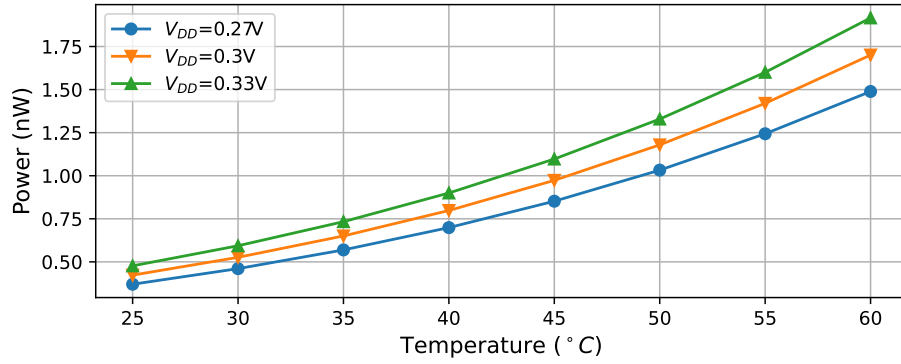
(a)



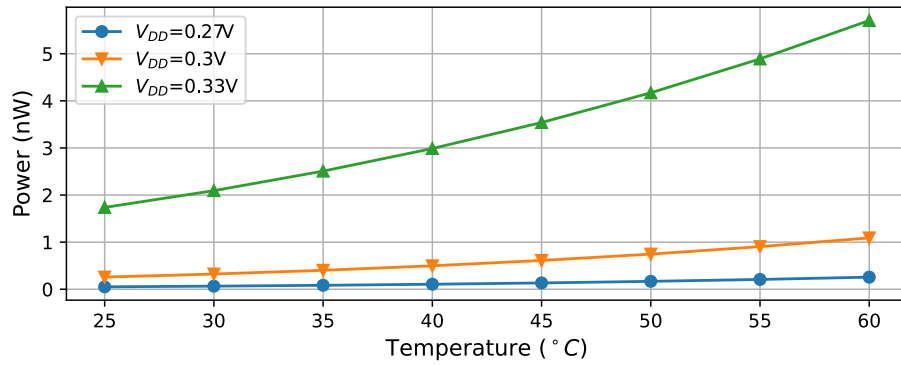
(b)

Figure 3.22. Trip-points of POR versus supply and temperature. (a) Brown-out voltage (V_{BOD}), (b) Power-on-Reset voltage (V_{POR}).

Lastly, the quiescent power of the POR is investigated. When POR is inactive, i.e., V_{DD} is stable, its static power becomes crucial for the overall power consumption of the chip. Figure 3.23 shows the quiescent power of the POR for various PVT corners. The top chart shows the power at a fixed corner (TT), and the bottom chart shows it for a fixed supply voltage (0.3V). It is clear that, especially at the FF corner, POR could take up a vast portion of the total power consumption of the ASIC.



(a)



(b)

Figure 3.23. Quiescent power of the POR circuit for various PVT. (a) Fixed process corner(TT), (b) Fixed supply voltage (0.3V).

3.6. Level-Shifter

Although standard cells on the chip work with a 0.3V supply, I/O signals should be converted to higher voltage levels, labeled as VDDH, to drive off-chip modules. For example, the barometric pressure sensor in the system needs at least 1.2V as the I/O voltage [6]. So, a level shifter circuit is needed for output signals. However, it is not needed for input signals as the transistors in 180 nm technology can work with high voltages like 1.8V. Level shifter by [42] is used for the designed ULP chip, whose schematic is shown in Figure 3.24. It has several parts: M5 acts as a pass-transistor, and M0, M1, and M2 form a Wilson current mirror. The current mirror reflects the I_D of M5 through M3, a diode-connected PMOS.

This diode is also a current limiter as it prevents the simultaneous turn-on of M6 and M7 transistors, eliminating the short-circuit current.

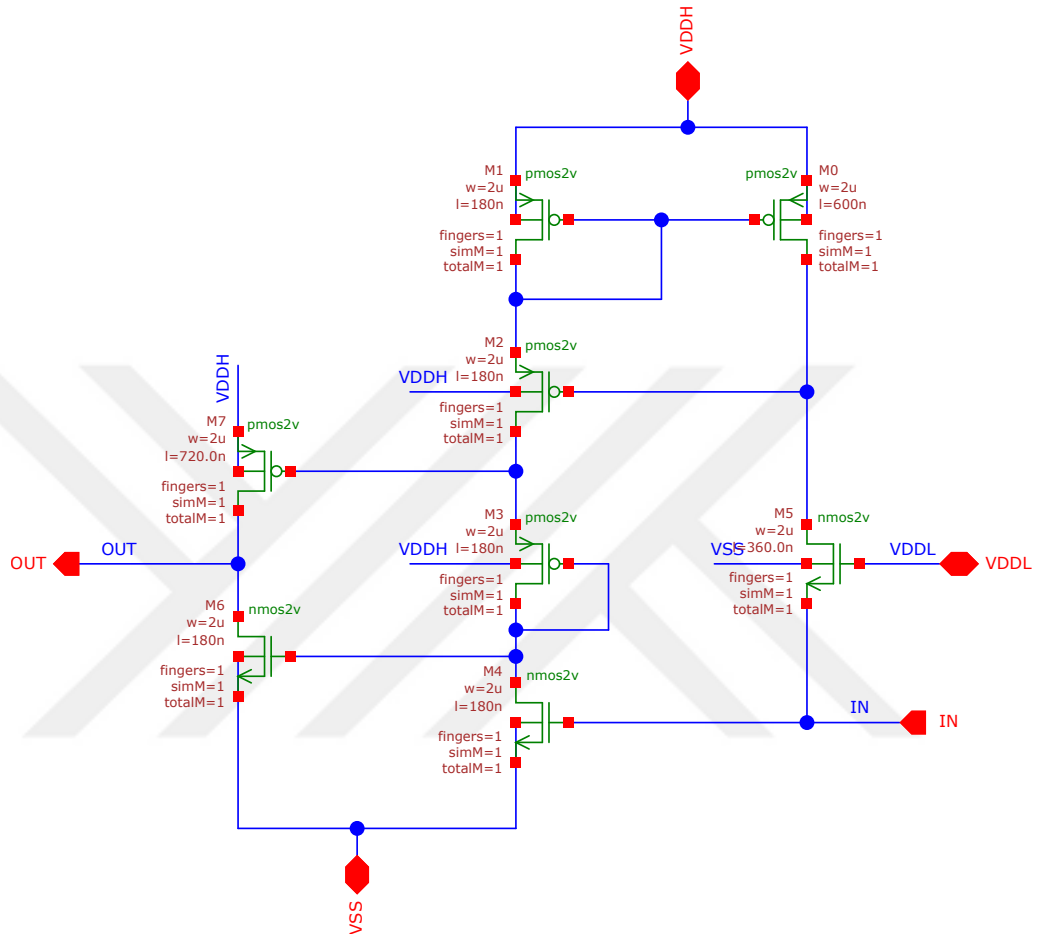


Figure 3.24. Schematic of the level shifter.

When the input is high, M4 turns on, pulling the gate of M3 to the ground, which will turn on M3 and M7, pulling the output high. Conversely, when the input is low, the gate of M2 will be pulled to the ground, thus pulling the source of M3 to high. M3 is a diode, so its drain will also be high, which turns on the M6 and pulls the output to the ground. Figure 3.25 shows the input and output waveforms of the level shifter for various I/O voltage levels.

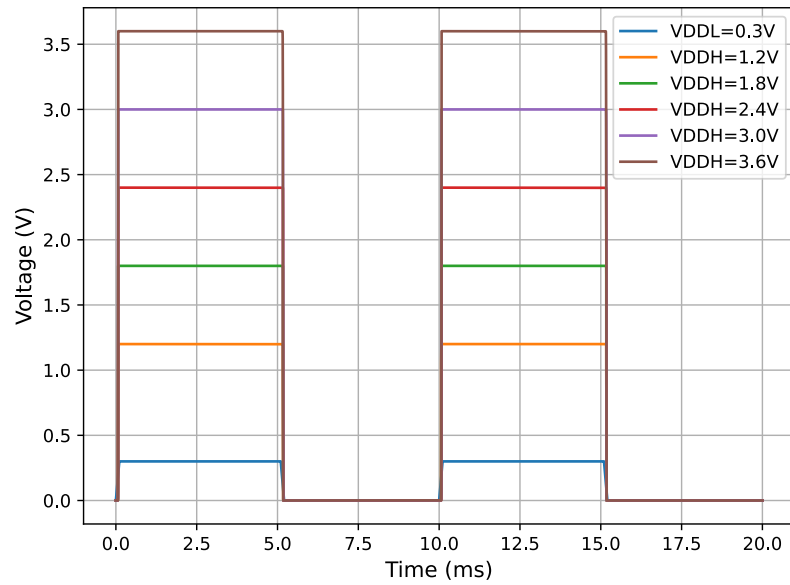


Figure 3.25. Transient simulation of level shifter.

The propagation delay of the level shifter is an essential metric of its performance. Figure 3.26 shows that its delay decreases with temperature and VDDH, except for 3.6 of VDDH.

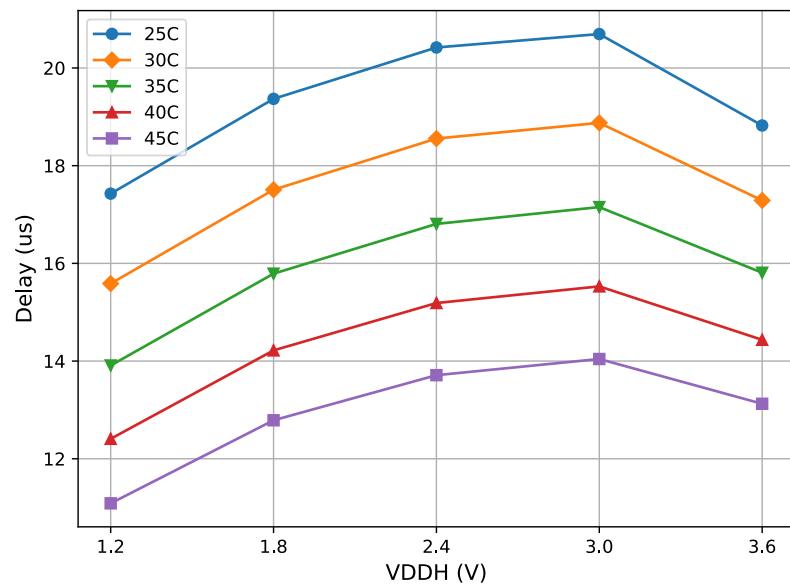


Figure 3.26. Delay of level shifter.

The quiescent power of the level shifter in the steady state is crucial for the chip's overall power. The energy consumed per transition is critical as well. The exponential relation between VDDH and static power and transition energy of the level shifter can be seen in Figures 3.27(a) and Figure 3.27(b), respectively.

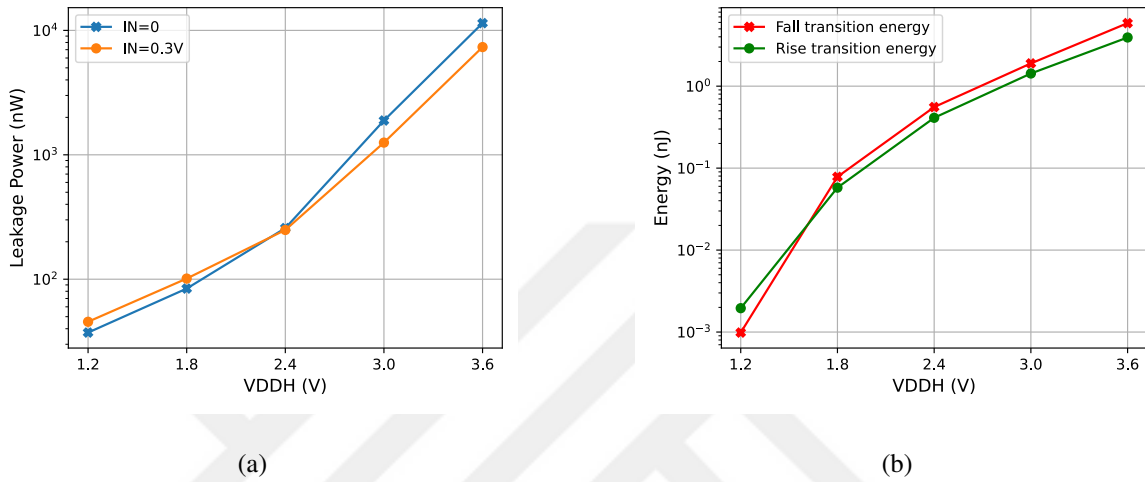


Figure 3.27. Power and energy of level shifter. (a) Quiescent power, (b) Transition energy.

3.7. Physical Design

Physical design is the step where the chip's physical layout is created, making it a crucial procedure. Figure 3.28 shows the physical design flow and its steps. The results obtained from the most crucial ones, synthesis, static timing analysis, place-and-route, and power analysis, are explained in detail. Moreover, to show the strengths and weaknesses of the DLS technique, the same design is passed through the physical design flow but with foundry-designed standard cells. The cells work with a 1.8V supply and do not use any subthreshold design technique, making them faster than DLS gates.

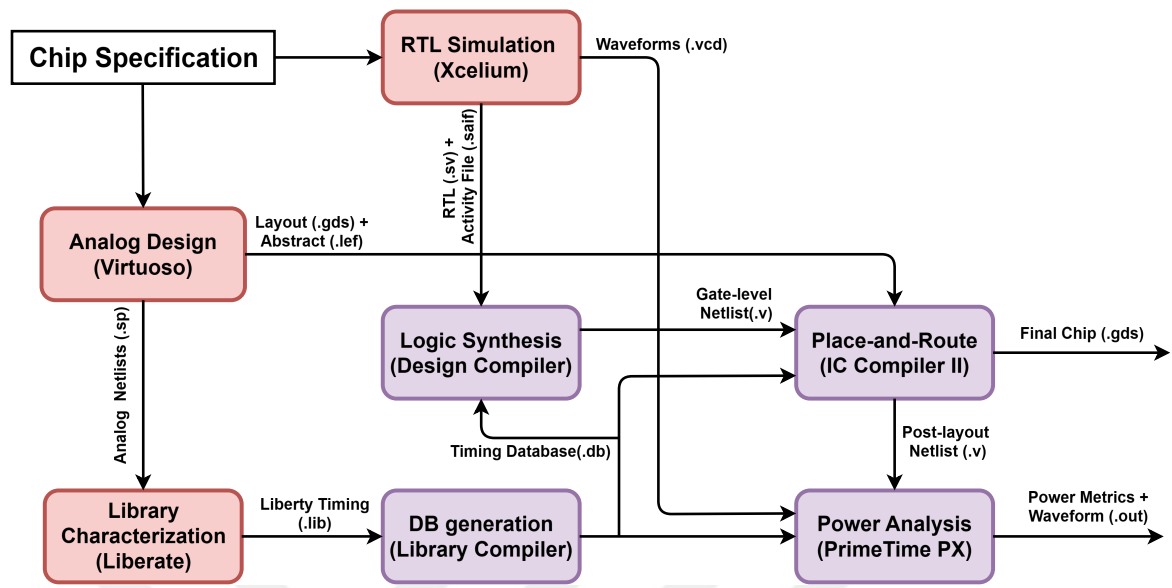


Figure 3.28. Physical design flow.

3.7.1. Synthesis and Static Timing Analysis

Synthesis is the process of transforming behavioral HDL code into its gate-level equivalent. The SystemVerilog code of the RISC-V core and peripherals and the Liberty file obtained from the characterization are given to the synthesis tool. The tool translates code into standard cells while trying to satisfy timing constraints, such as the minimum target clock frequency. It also tries to optimize power and area.

The configurations from Table 3.1 are synthesized using DLS and foundry standard cell libraries to determine the best setup for the processor core. Maximum frequency, static power consumption, and gate count for each configuration are shown in Table 3.4. The configuration *micro* is chosen for the rest of the physical design to save silicon area while reducing power.

Table 3.4. Synthesis results.

Processor Configuration	Standard Cell Library	Gate Count	Worst		Typical		Best	
			Power (nW)	Freq. (Hz)	Power (nW)	Freq. (Hz)	Power (uW)	Freq. (Hz)
micro	DLS	14912	16.82	61.53	25.6	188.08	76.91	564.63
	Foundry	2289	658.765	$47.03 * 10^6$	1170	$63.64 * 10^6$	1710	$101.52 * 10^6$
small	DLS	21071	20.03	38.81	29.86	127.17	89.63	307.59
	Foundry	2600	739.38	$43.40 * 10^6$	1310	$56.58 * 10^6$	1920	$93.08 * 10^6$
maxperf	DLS	24102	25.93	10.35	35.33	88.05	111.46	207.78
	Foundry	2700	819.903	$29.87 * 10^6$	1450	$50.7 * 10^6$	2130	$77.08 * 10^6$

Moreover, the DLS technique can reduce static power up to 40 times compared to foundry standard cells. However, the gate count with DLS cells is significantly higher than the design synthesized with foundry cells, because the DLS logic library only has 13 gates, while the foundry library has 562 standard cells, including cells with different driving strengths. This increases the required DLS gates per combinational path, severely affecting the power, area, and maximum frequency.

3.7.2. Place-and-Route

The gate-level netlist created in the synthesis is presented to the place-and-route tool. Based on the number of standard cells in the netlist, the Place-and-Route (PnR) tool first creates a floorplan, i.e., the dimensions of the chip. Then, it determines the metal layers used for power routing, which is called power planning. Then, it places and connects all standard cells and analog blocks in the layout. During these steps, the PnR tool uses the LEF files of

the standard cells, which store their physical information, like pin locations, cell dimensions, etc. Similar to synthesis, systems with different configurations of the Ibex RISC-V core are passed through the PnR. Figure 3.29 shows the layout of the designs.

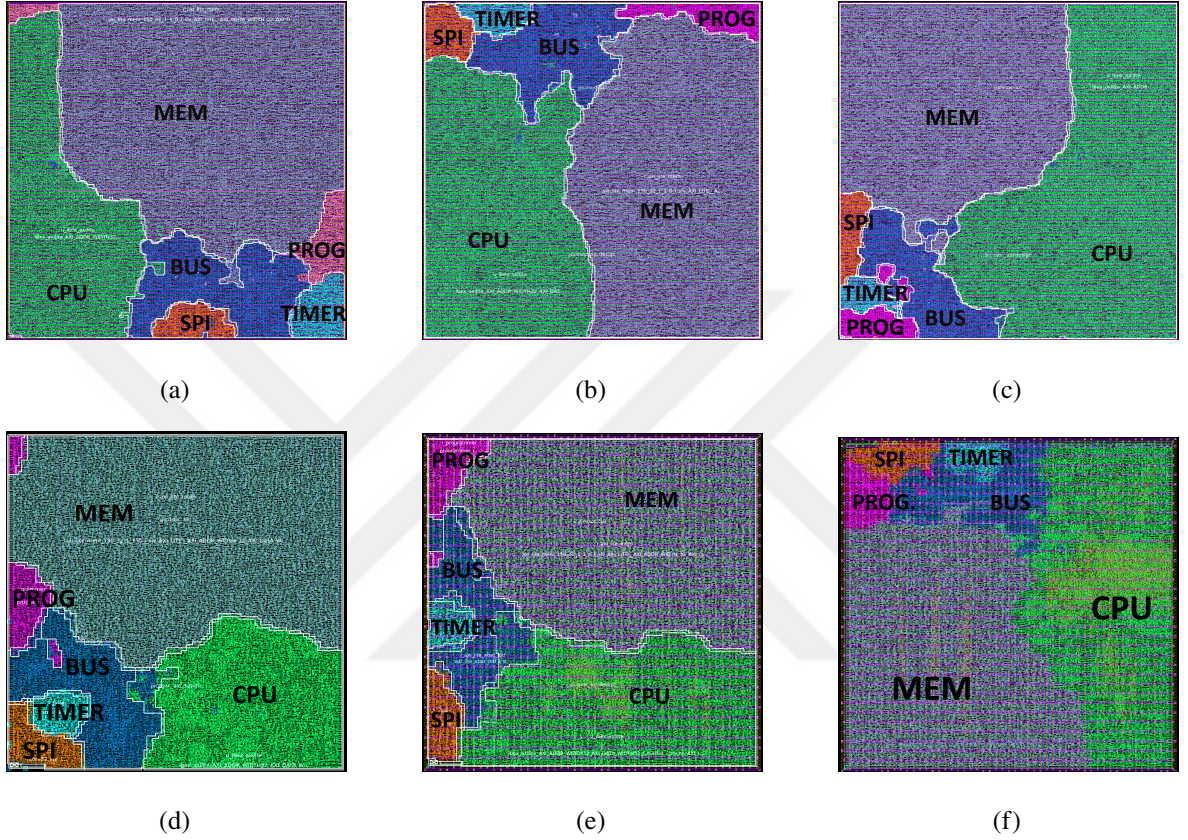


Figure 3.29. Layout of each processor configuration. (a) micro, DLS, 7.18 mm², (b) small, DLS, 8.32 mm², (c) maxperf, DLS, 9.98 mm², (d) micro, Foundry, 0.86 mm², (e) small, Foundry, 0.97 mm², (f) maxperf, Foundry, 1.07 mm².

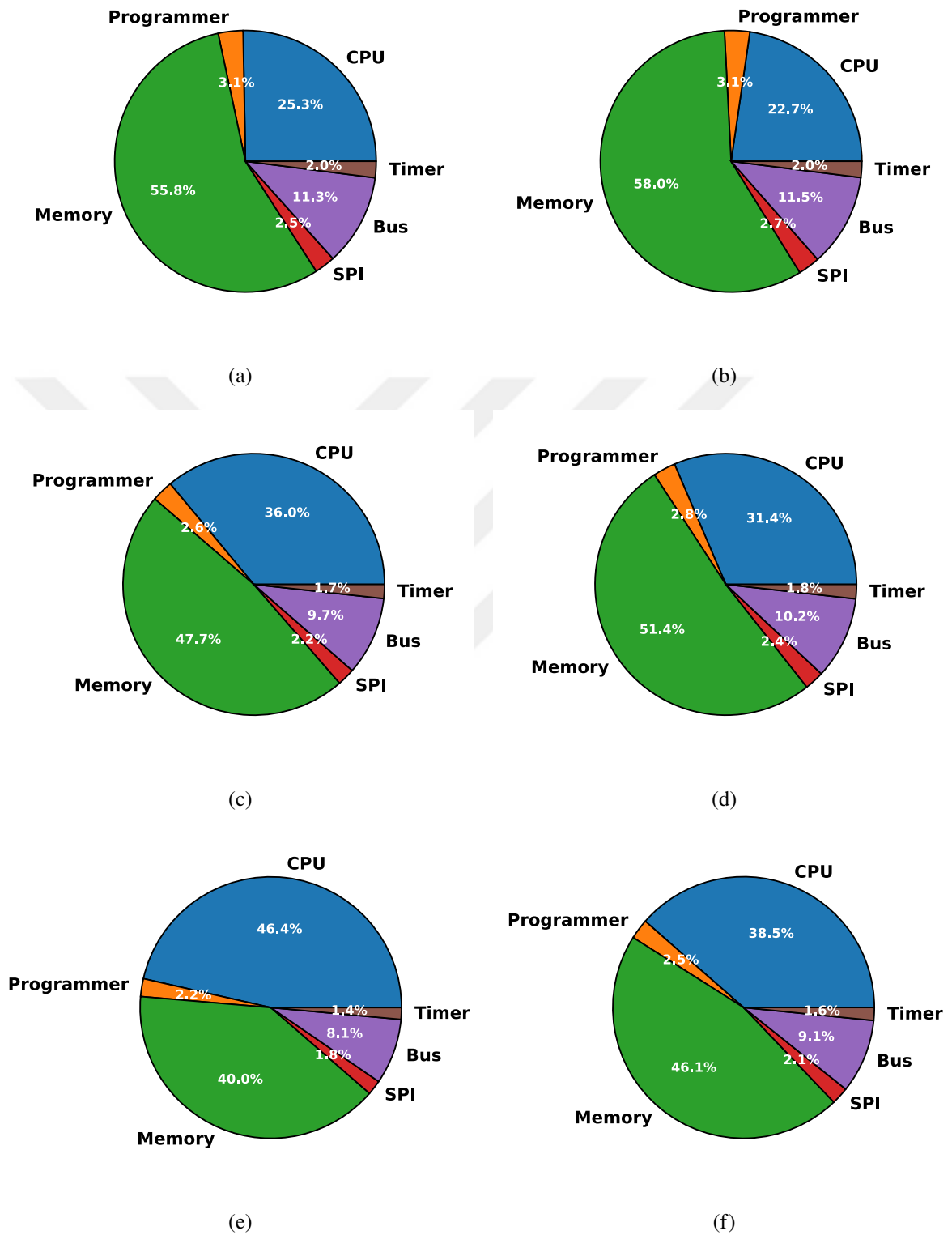


Figure 3.30. Area ratio of sub-blocks. (a) micro, DLS, (b) micro, Foundry, (c) small, DLS, (d) small, Foundry, (e) maxperf, DLS, (f) maxperf, Foundry.

Figure 3.30 shows the area ratio of sub-blocks to the entire design. It is noticeable that memory occupies a large part of the chip since it is register-based. A custom SRAM macro would shrink its size considerably.

3.7.3. Power Analysis

Power analysis is another crucial step that will prove the low-power capabilities of the designed chip. There are a couple of methods to estimate the power.

- Averaged power analysis: The chip's power consumption is calculated based on the activity factors of its inputs, which are propagated to the standard cell inputs. This method needs the gate-level netlist in Verilog, the Liberty file for power information, and the SAIF file for the activity factors.
- Time-based power analysis: This method utilizes the input/output waveforms instead of activity factors. Like the averaged analysis, inputs are propagated to the standard cells. However, the power estimation is time-dependent, i.e., it is possible to see the power consumption at a given time. Therefore, time-based analysis is more accurate than averaged power analysis. Instead of SAIF, a VCD file is used for such analysis.

Time-based power analysis is performed on the chip to increase accuracy in power estimation. In this case, the program running on the processor becomes essential. Figure 3.31 shows the flowchart of the program. For the processor configurations *small* & *maxperf*, the written C program is compiled for RISC-V RV32IMC architecture, indicating the support of 32 base registers with multiplication support. On the other hand, the program for *micro* configuration is RV32EC, which has no multiplication support with 16 base registers. However, because the program does not execute any analysis of the sensor data, the Assembly code produced by the RISC-V compiler does not include any instructions from the RISC-V M (multiplication) extension. Therefore, the only benefit *small* & *maxperf* obtains from the change of compiler options is the extra utilization of 16 base registers.

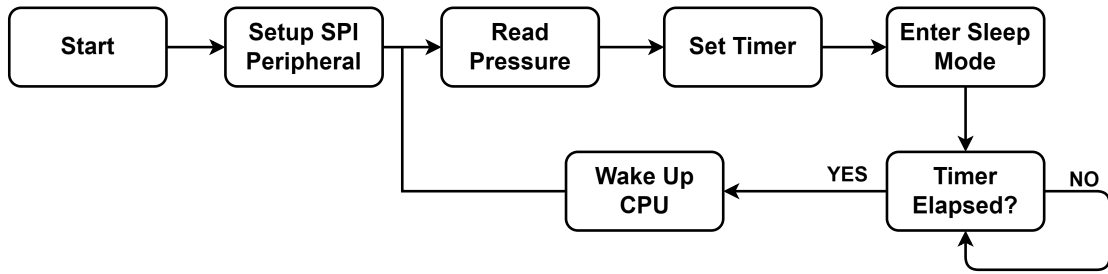


Figure 3.31. Flowchart of the pressure measurement program.

The simulation is performed where the processor runs the program. The simulation has three primary operations: programming, pressure measurement, and waiting in idle mode. Only the *micro* processor configuration is simulated. Both DLS cells and foundry cells are tested in power analysis. The only difference is that the chip with foundry standard cells operates at 1 MHz, which shows how taking faster pressure measurements would affect the total energy. Figure 3.32 shows the power waveforms.

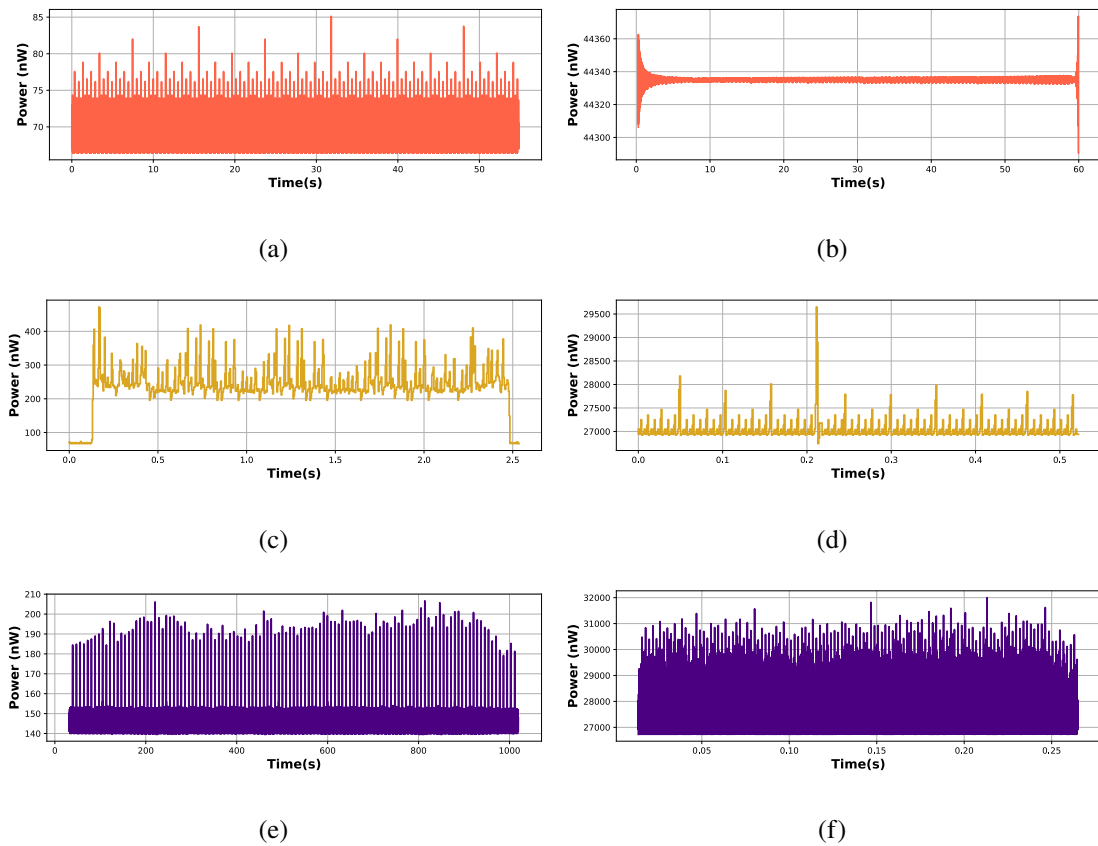


Figure 3.32. Power waveforms for tasks. (a) Idle, DLS, (b) Idle, Foundry, (c) Sensor read, DLS, (d) Sensor read, Foundry, (e) Programming, DLS, (f) Programming, Foundry.

Table 3.5. Energy and power consumption of the tasks.

Task	Duration (s)		Average Power (uW)			Peak Power (uW)			Total Energy (uJ)	
			ASIC		Pressure Sensor	ASIC		Pressure Sensor	DLS Cells & Sensor	Foundry Cells & Sensor
	DLS	Foundry	DLS	Foundry		DLS	Foundry			
Idle	59.96	60.44	0.0689	44.33	2.52	0.454	82.27	2.52	155.23	2831.614
Sensor Read	3.13	0.0005	0.2304	27.06	5.76	0.23	29.65	1188	18.75	0.016
Prog.	1021	0.265	0.1418	29.09	2.52	0.14	81.6	2.52	2717.70	8.376

It can be seen that, especially in the waiting mode, the system with DLS cells consumes considerably less power than foundry-designed cells. However, since DLS cells are much slower than foundry cells, sensor reading takes much more time, increasing the total energy consumption. The difference in energy increases even more if the energy consumed by the temperature sensor is also considered. Table 3.5 shows each case's power and energy consumption. It can be seen that, due to its low speed, the ASIC with DLS cells dissipates considerably more energy than the one with foundry cells. However, there is a large difference in energy during idle periods. Therefore, it is possible to conclude that DLS cells become viable in cases where there are long waiting times between the measurements. Otherwise, especially if quick measurements are vital, foundry-designed standard cells stand out. Also, due to its significantly lower peak power, the chip with DLS cells would be more suitable for energy harvesting systems.

3.8. FPGA Implementation

To validate digital blocks in the design, they are tested on an FPGA. It also allows us to compare implementation results with their ASIC counterparts. The Vivado Design Suite 2023.2 tool is used with its default settings for implementation. As in ASIC implementation, each configuration of the RISC-V core is implemented for the Artix-7 FPGA. For similar reasons as foundry standard cells, the clock frequency in the FPGA implementation is chosen to be 1 MHz. Figure 3.33 shows the FPGA resource utilization for different configurations. Also, static power, number of resources used, and slack for each configuration are shown in Table 3.6. It can be seen that FPGA power consumption is dramatically higher than ASICs, the ones with both DLS and foundry standard cells. The results show that for ultra-low power applications like HF monitoring, it is best to use a custom ASIC instead of an FPGA.

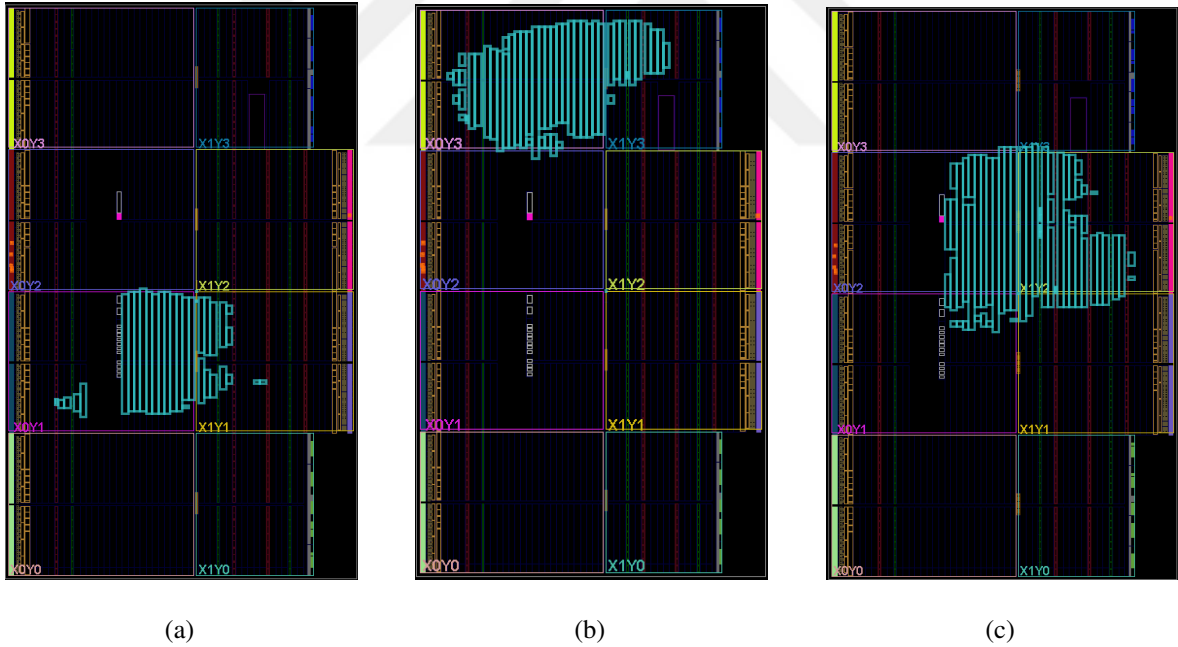


Figure 3.33. FPGA implementation of different configurations. (a) micro, (b) small, (c) maxperf.

Table 3.6. FPGA implementation results.

Processor Configuration	Resource Utilization				Total Power (mW)	Worst Negative Slack (ns)
	LUT	FF	BRAM	DSP		
Micro	3427	2888	0.5	0	97	976
Small	4340	3546	0.5	1	97	965
Maxperf	6094	3658	0.5	4	98	960

4. DISCUSSION AND FUTURE WORK

In this thesis, a system with an embedded RISC-V core is designed for HF monitoring applications. Since the system will operate in an energy-constrained environment due to its nature, minimizing power consumption is of utmost importance. A small set of standard cells is designed using the dynamic leakage suppression technique, which allows for dramatically decreased cell leakage power. The cells are characterized as being useful for digital physical design tools. Not only standard cells but a set of critical analog blocks, like the oscillator, power-on-reset, and level shifter, are designed. The main design focus on these blocks is minimizing leakage power. The digital blocks are implemented in a 180-nm process using the standard cells designed. Lastly, a time-based power analysis was performed on the chip to estimate its power consumption for different tasks, such as sensor reading, programming, or waiting in sleep mode. The results are compared with power analysis results with foundry standard cells. It is concluded that DLS standard cells can reduce power and energy consumption, especially if idle time is long.

Even though substantial savings in power consumption are achieved, there are several points in the design where there is room and a need for improvement.

- The register-based memory takes up a substantial portion of the design in terms of both silicon area and power consumption. An SRAM operating in the subthreshold regime would improve the power, area, and performance.
- Standard cells are designed using the most basic form of dynamic leakage suppression technique. Even though they give satisfactory results in idle mode, they need to be improved since the charge and discharge times of the cells are high, increasing the total energy. Modifications on the standard cells like [27–29] will improve performance and energy consumption.
- DLS standard cells are severely affected by the variations in supply voltage. Therefore, a low-dropout regulator with low quiescent current is needed to have a stable supply voltage through the design.

- Now that nanowatt-scale power consumption is achieved with the ULP chip, the barometric pressure sensor dominates the overall power consumption, as seen in 3.5. Therefore, a custom circuit capable of measuring pressure would considerably improve overall power and energy consumption.



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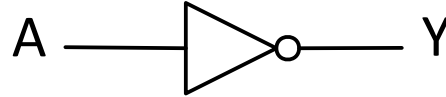
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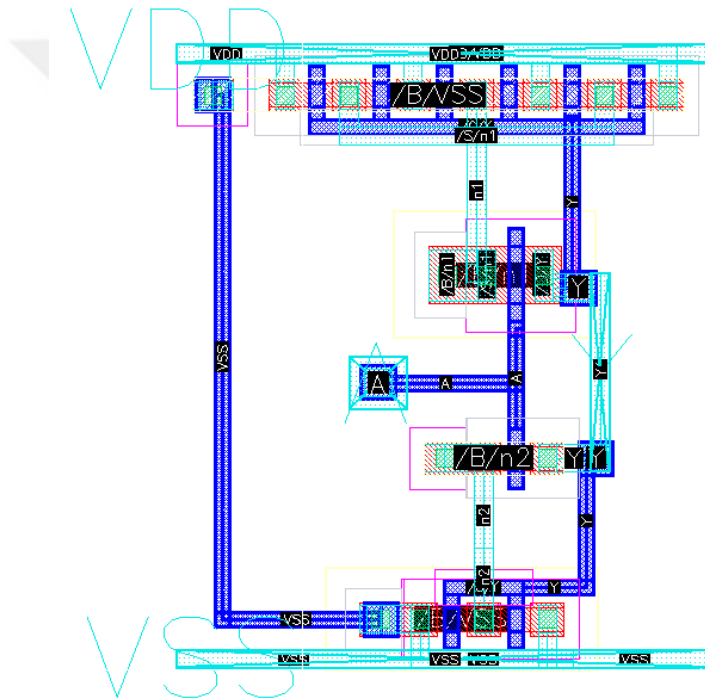
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APPENDIX A: PRESENTATION OF STANDARD CELLS

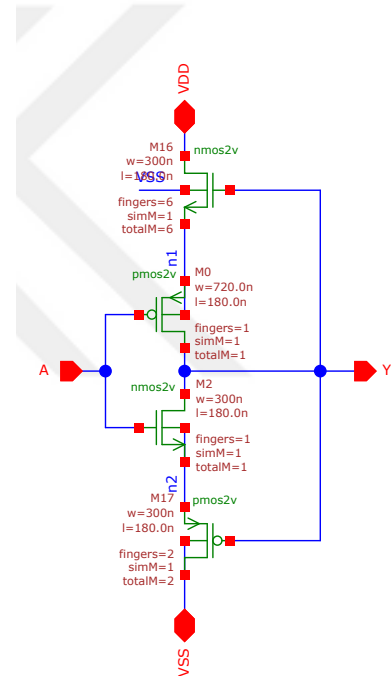
Symbols, schematics, and layouts of DLS standard cells will be presented in this section.



(a)

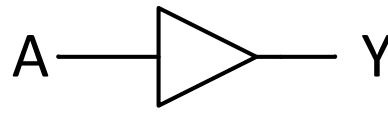


(b)

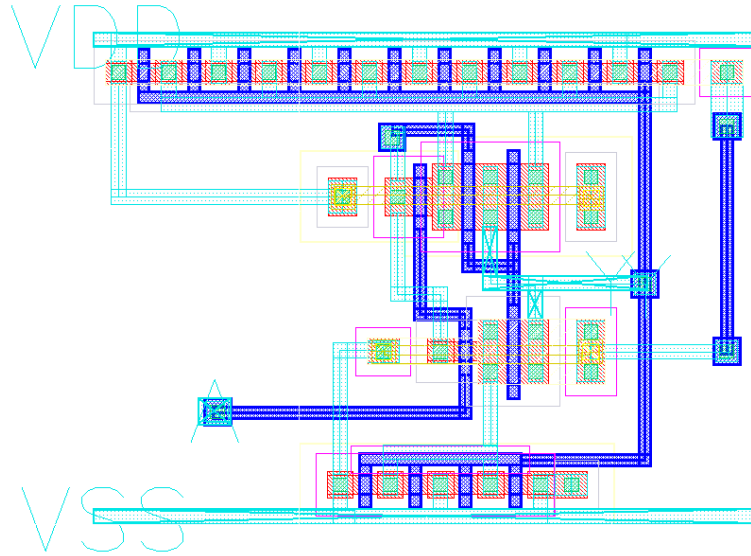


(c)

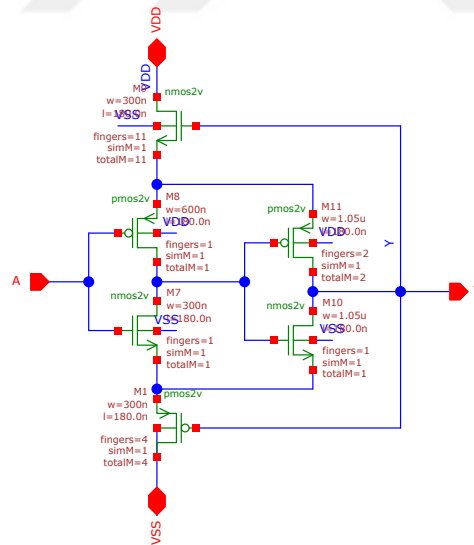
Figure A.1. Standard cell: INV. (a) Symbol, (b) Layout, (c) Schematic.



(a)

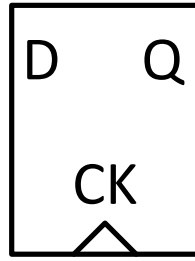


(b)

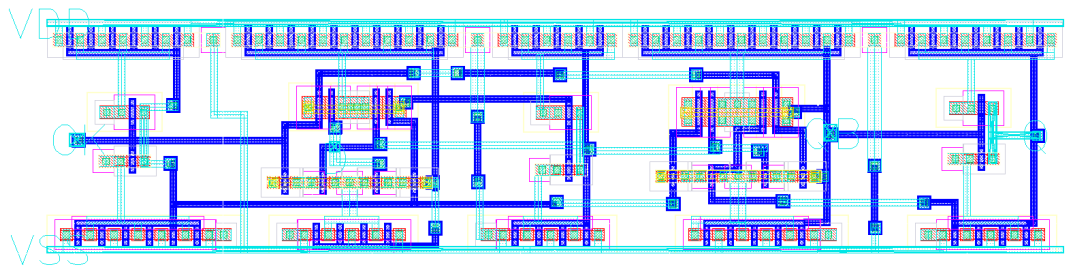


(c)

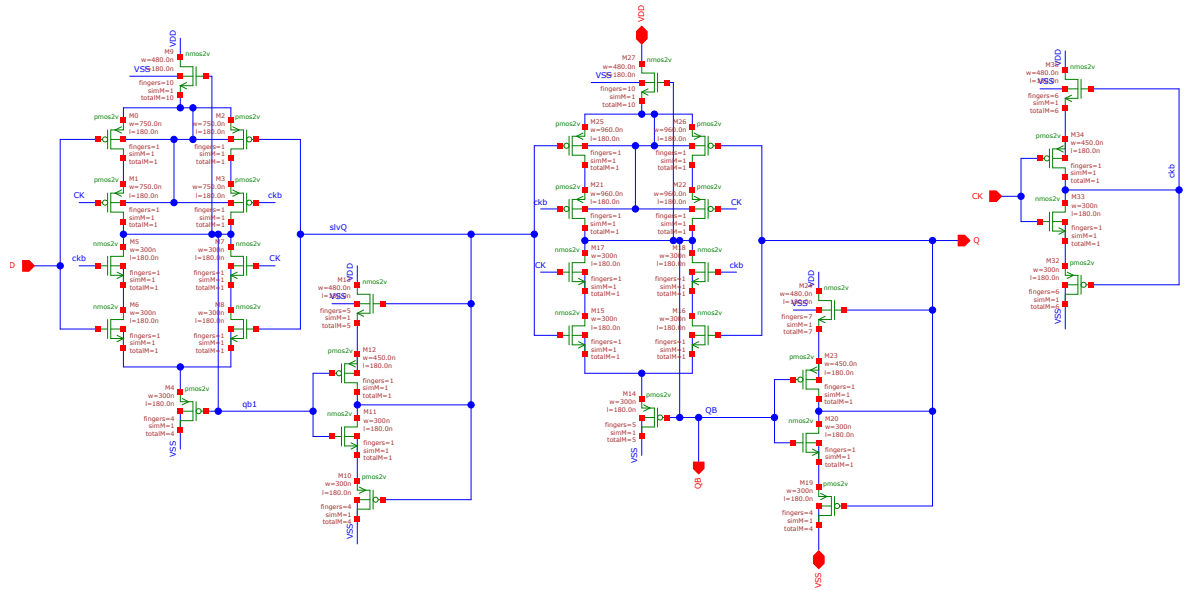
Figure A.2. Standard cell: BUF. (a) Symbol, (b) Layout, (c) Schematic.



(a)

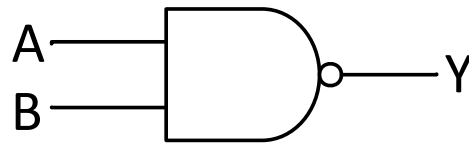


(b)

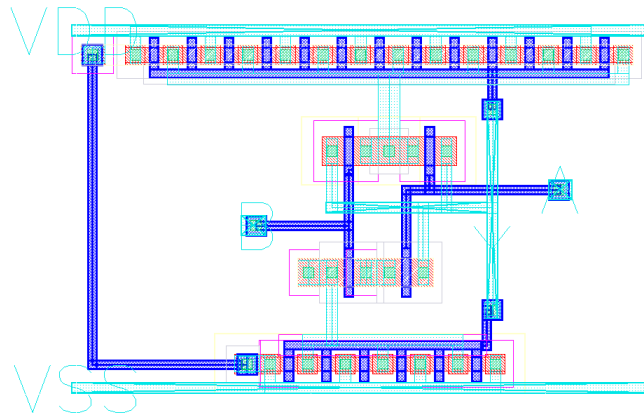


(c)

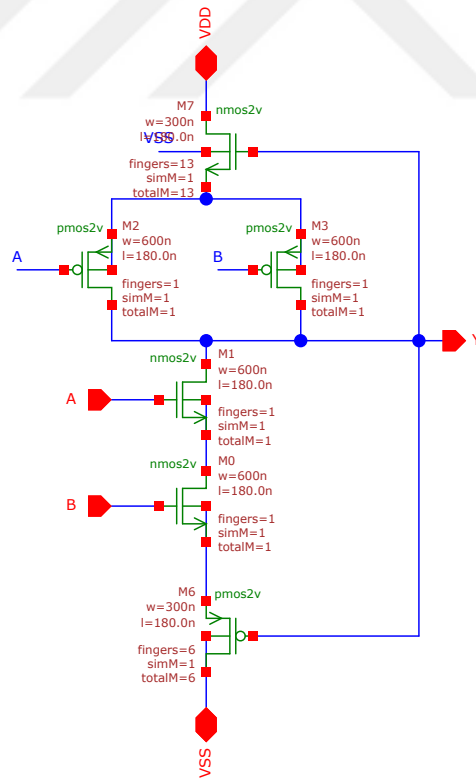
Figure A.3. Standard cell: DFF. (a) Symbol, (b) Layout, (c) Schematic.



(a)

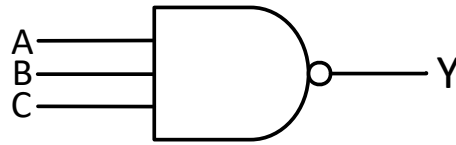


(b)

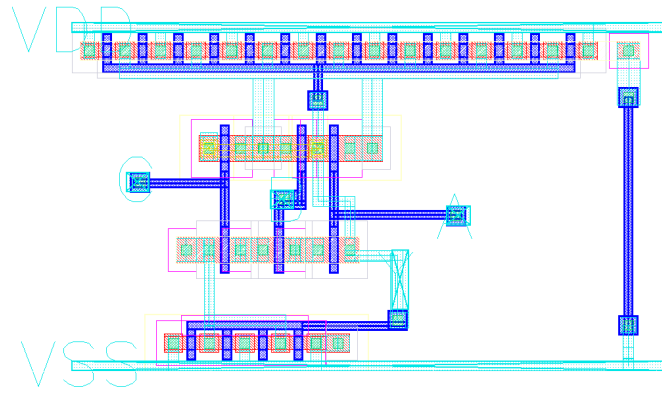


(c)

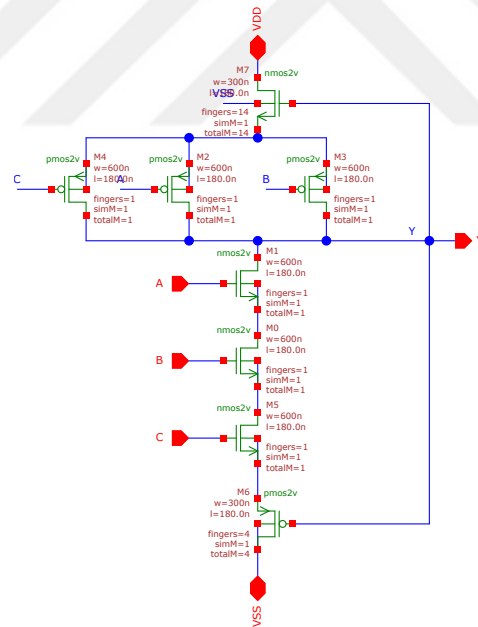
Figure A.4. Standard cell: NAND2. (a) Symbol, (b) Layout, (c) Schematic.



(a)

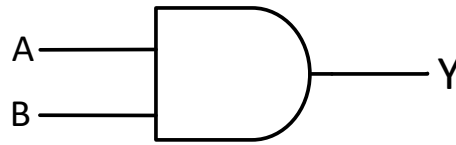


(b)

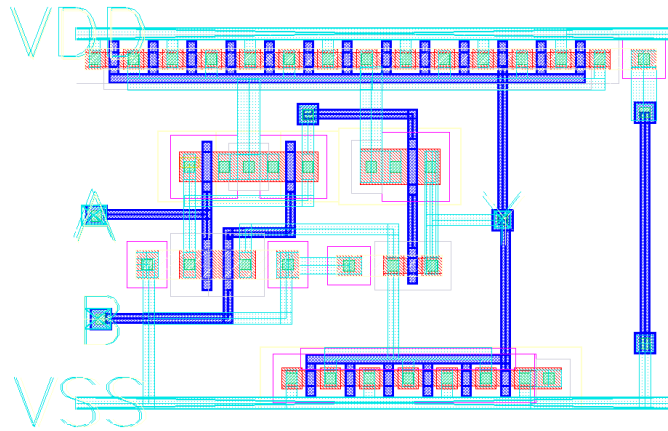


(c)

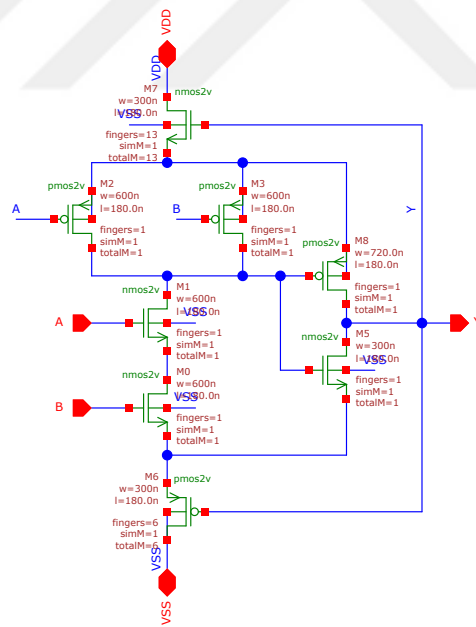
Figure A.5. Standard cell: NAND3. (a) Symbol, (b) Layout, (c) Schematic.



(a)

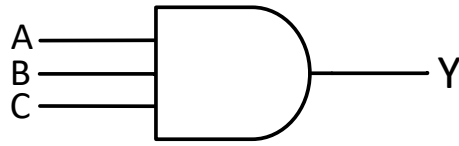


(b)

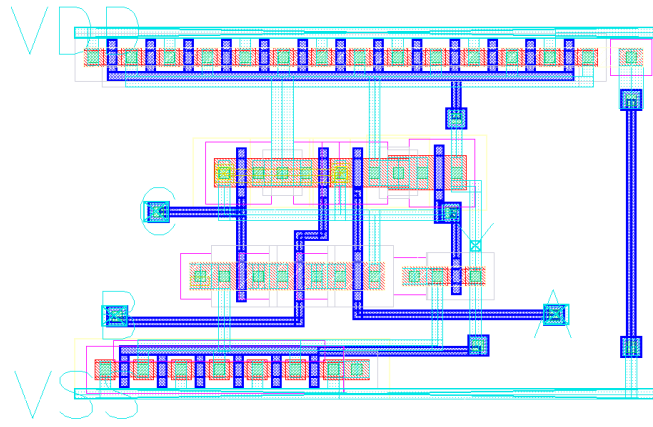


(c)

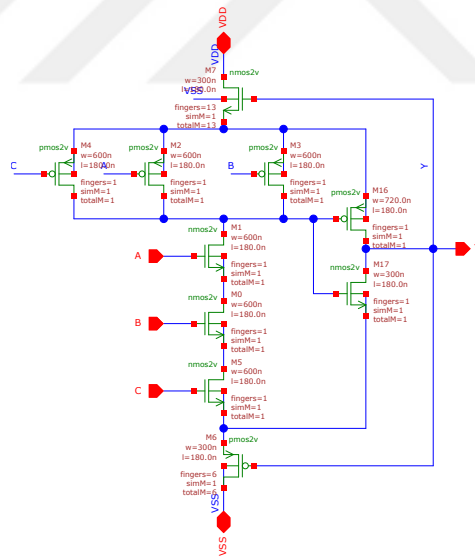
Figure A.6. Standard cell: AND2. (a) Symbol, (b) Layout, (c) Schematic.



(a)

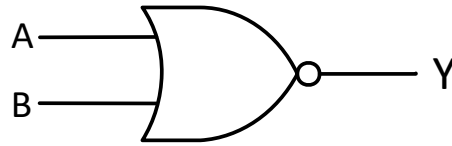


(b)

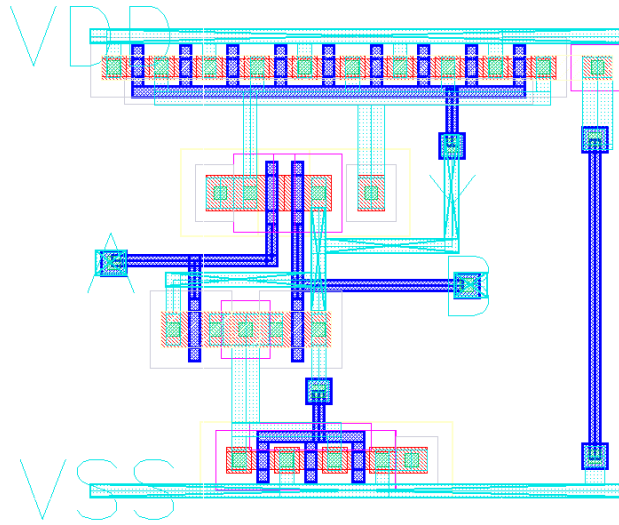


(c)

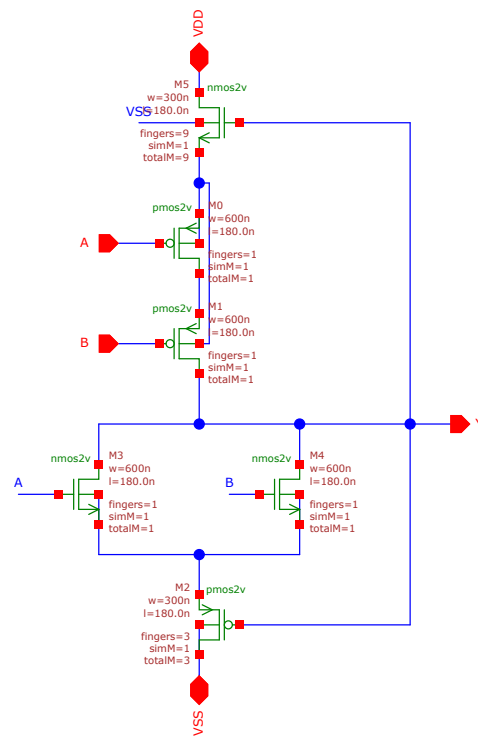
Figure A.7. Standard cell: AND3. (a) Symbol, (b) Layout, (c) Schematic.



(a)

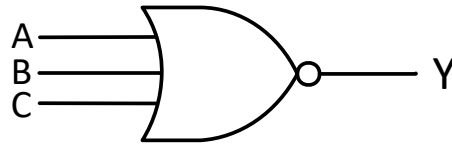


(b)

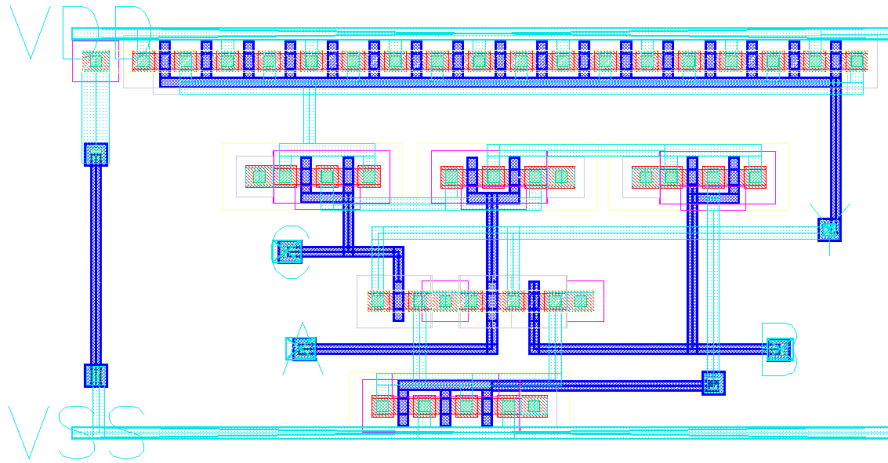


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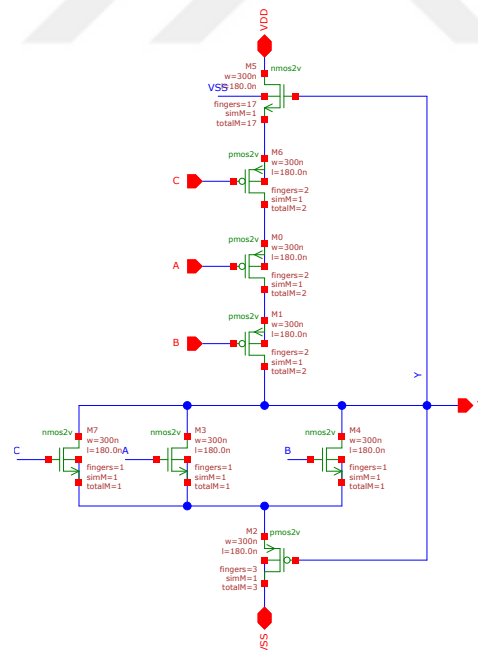
Figure A.8. Standard cell: NOR2. (a) Symbol, (b) Layout, (c) Schematic.



(a)

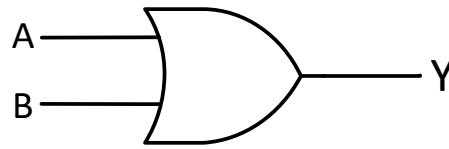


(b)

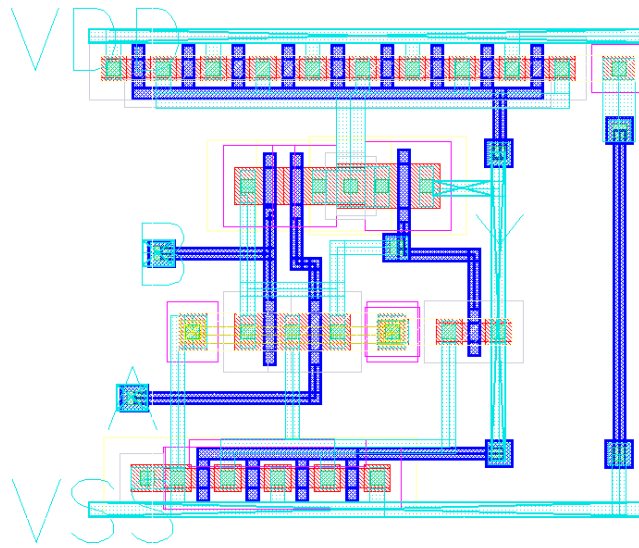


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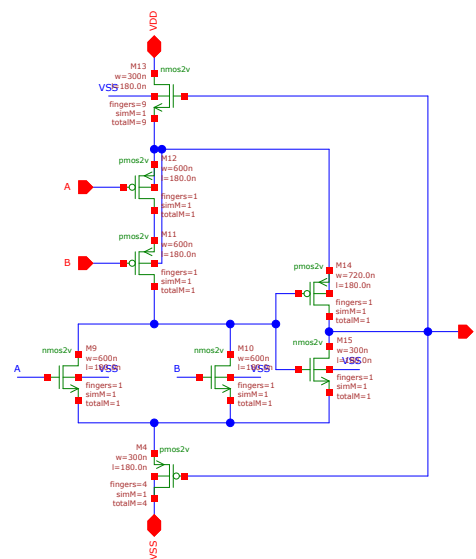
Figure A.9. Standard cell: NOR3. (a) Symbol, (b) Layout, (c) Schematic.



(a)

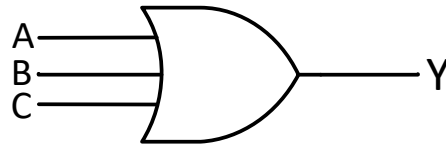


(b)

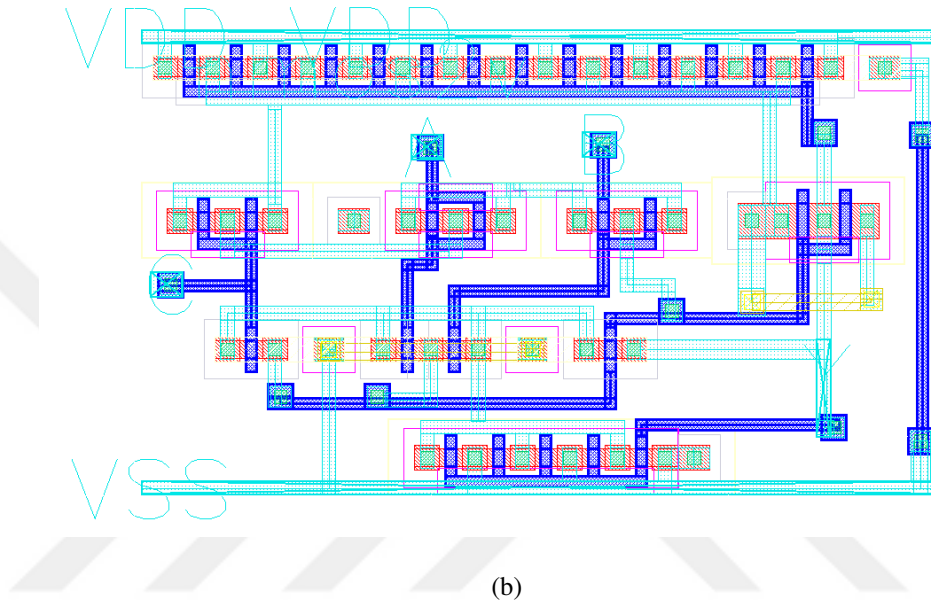


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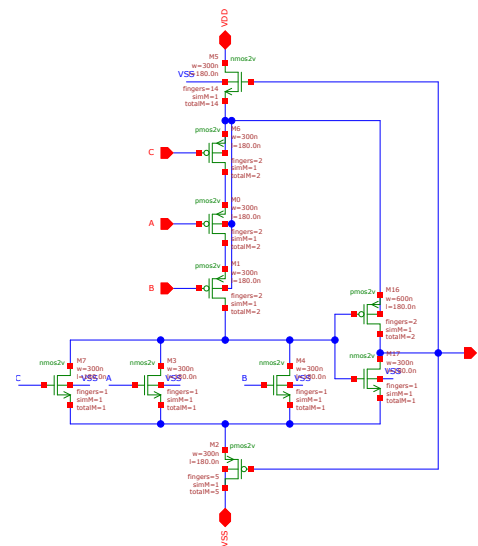
Figure A.10. Standard cell: OR2. (a) Symbol, (b) Layout, (c) Schematic.



(a)

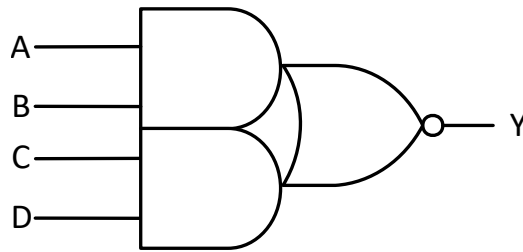


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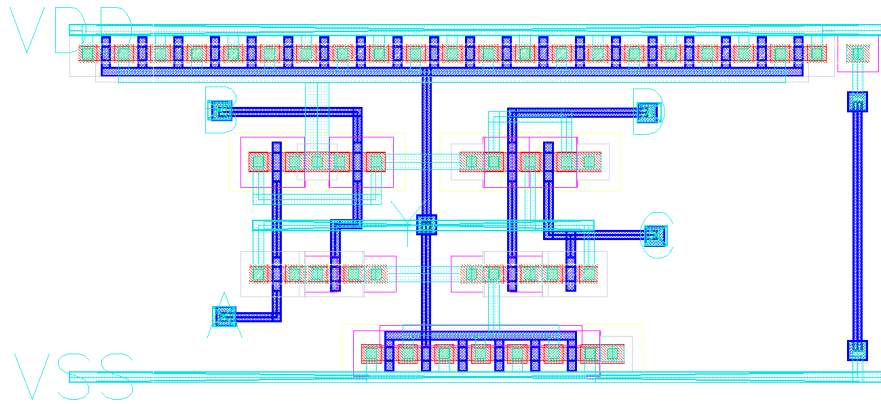


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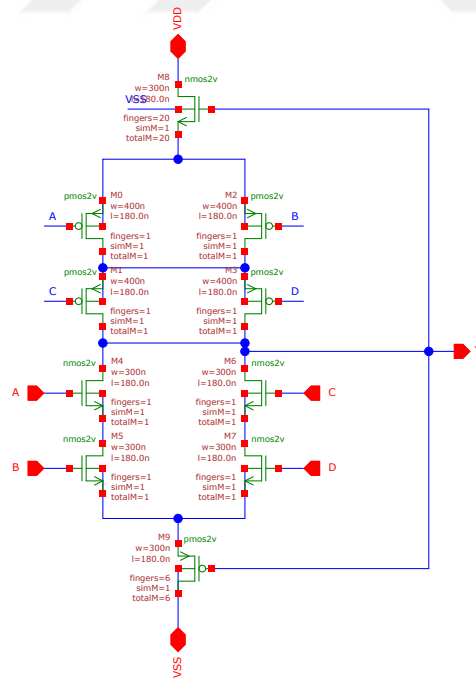
Figure A.11. Standard cell: OR3. (a) Symbol, (b) Layout, (c) Schematic.



(a)

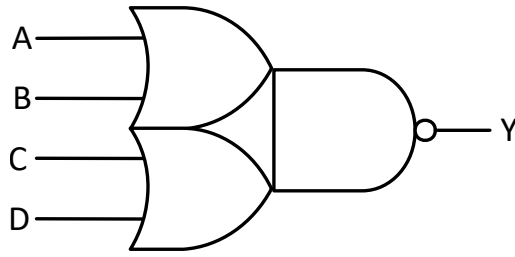


(b)

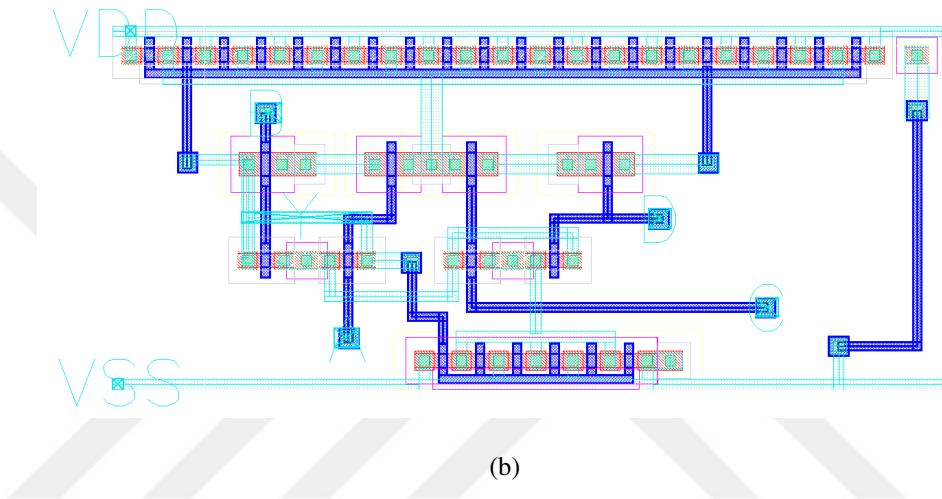


(c)

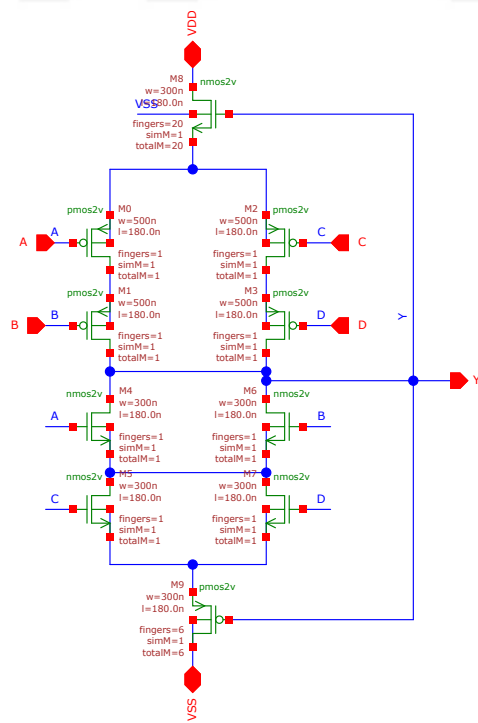
Figure A.12. Standard cell: AOI22. (a) Symbol, (b) Layout, (c) Schematic.



(a)



(b)



(c)

Figure A.13. Standard cell: OAI22. (a) Symbol, (b) Layout, (c) Schematic.