BROADBAND HIGH EFFICIENCY RF POWER AMPLIFIER DESIGN BASED ON MODIFIED CLASS-J APPROACH WITH APPLICATIONS USING GAN HEMT TECHNOLOGY

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ABSTRACT

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RF power amplifiers have been the essential elements of any transmit/receive block. Especially in the transmit chain, some applications require high RF power, such as radar, jammer, telecommunication signals targeting a wide range of coverage. High power requirements in RF broadcast mean high supply power to feed RF PA. The efficiency parameter of a high-power transmission system becomes an issue due to heating problems and performance degradation depending on rising temperatures. The heating problem is commonly solved using active cooling plants. Cooling plants add extra cost demanding discrete power supplies and considerable amount of design labor. With these problems at hand, industrial and academic environments have turned to look for more efficient amplifier topologies. In this thesis, modified class-J schemes proposed to enhance operating bandwidth are studied. A modification called "normalized resistive-reactive class-J" (NRRCJ) approach is proposed. Detailed parametric analysis is presented. The effects of parameters in governing equations are discussed. A related engineering design procedure is demonstrated with an ultra-broadband GaN PA. Prototype PA operating at 400-3200 MHz capable of at least 10 W saturated output power is fabricated. Measured efficency values of $\%53 - \%69.8$ are obtained at

saturated output power. The average efficiency is calculated as $\%62.45$. The measurement results, theoretical aspects, and expectations are compared. It is shown that the resistive termination of harmonics in a systematic way makes it possible to achieve a broadband and relatively high efficiency performance, simultaneously. The final prototype achieves remarkable compatibility with a practical RF system, compared with similar examples in the literature, in terms of size, gain, efficiency, output power and operating frequency band.

Keywords: RF PA, High Efficiency, UHF, VHF, Broadband, Normalized Resistive-Reactive Class-J

ÖZ

ALTERNATİF J-SINIFI YAKLAŞIMI İLE GAN TEKNOLOJİSİ TEMELLİ GENİŞ BANT YÜKSEK VERİMLİ GÜÇ YÜKSELTECİ UYGULAMALARI

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Radyo frekans güç yükselteçleri gönderme ve alma zincirinin vazgeçilmez elemanlarındandır. Özellikle radar, sinyal karıştırıcı ve uzun menzil haberleşme sinyali iletimi yüksek çıkış gücü gerektiren uygulamalardır. Yüksek RF güç çıkışı isterleri beraberinde daha fazla DC güç tüketimine neden olmaktadır. RF güce dönüşmeyen enerji güç yükselteci etrafında ısıya dönüşerek kritik sıcaklık artışlarına neden olmaktadır. Bu sebele güç yükseltecinin verim parametresi önem arz etmektedir. Isınma problemi birçok sistemde aktif soğutma yöntemleriyle aşılmktadır. Aktif soğutma yöntemleri sistem tasarımında ayrık güç besleme üniteleri kullanılmasını gerektirebilir. Bunun yanında ek tasarım işçiliği bedelleriyle toplam sistem maliyetini artırmaktadır. Endüstriyel ve akademik çevreler, bu etkenleri göz önüne alarak, verimli yükselteç toplolojileri üzerine yoğunlaşmaktadırlar. Bu tez çalışmasında literatürde mevcut, bant genişliğini artırmayı amaçlayan alternatif-J sınıfı tasarım yöntemleri incelenmiştir. Bu fikirlerden yola çıkarak türev bir yaklaşım olan "düzgelenmiş dirençsel-tepkin J sınıfı" alternatifi önerilmiştir. Detaylı parametre analizleri sunulmuştur. Teorik bağıntılarla ilintili olarak geliştirilen tasarım prosedürü ultra geniş bantlı bir GaN güç

yükselteç ile gösterilmiştir. Prototip yükselteç 400-3200 MHz bant aralığında, doygun gücü en az 10W olacak şekilde tasarlanıp üretilmiştir. Verimlilik $53\% - 69.8\%$ arasında elde edilmiştir. Ortalama verim 62.45% olarak hesaplanmıştır. Ölçüm sonuçları ve teorik beklentiler karşılaştırılmıştır. Sistematik şekilde yapılan harmonik empedans uyumlamalarının bant genişliğini artırırken verimi de makul seviyelerde tutmaya olanak sağladığı gösterilmiştir. Kazanç, verim, boyut, bant genişliği, çıkış gücü gibi kriterler çerçevesinde literatürde var olan benzer örneklerle kıyaslama yapıldığında üstün veya denk performans özellikleri gözlenmiştir. Bu kıyaslamalar sonucunda pratik RF uygulamalarına uyumlu bir tasarım çıktısı elde edildiği sonucuna varılmıştır.

Anahtar Kelimeler: RF güç yükselteci, yüksek verim, UHF, VHF, Geniş bant, düzgelenmiş dirençsel-tepkin J sınıfı

TO MY MOTHER...

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LIST OF ABBREVIATIONS

GaN/GAN	Gallium-Nitride
HEMT	high electron-mobility transistor
RRCJ	resistive-reactive class-J
NRRCJ	normalized resistive-reactive class-J
PA	power amplifier
SSPA	solid-state power amplifier
RF	radio frequency
VSWR	voltage standing wave ratio
MMIC	monolithic microwave integrated circuit
ACPR	adjacent channel power ratio
ACLR	adjacent channel leakage ratio
PAR	peak to average ratio
AM	amplitude modulation
PM	phase modulation
EVM	error-vector magnitude
TWTA	traveling-wave tube amplifier
VED	vacuum electronic device
OFDM	orthogonal frequency-division multiplexing
LTE	long-term evolution
WCDMA	wideband code division multiple access
CW	continuous working
FET	field effect transistor
VCCS	voltage-controlled current source

CHAPTER 1

INTRODUCTION

1.1 RF Power Amplifiers

Though RF power amplifier design is a very old subject in the literature, the need for an RF power amplifier is inevitable in most of the microwave systems such as radars, jammers, medical imaging applications, and telecommunications. To put in simplest words, RF power amplifier is an instrument that magnifies the applied input RF signal amplitude using the fed-in DC energy by a gain factor throughout proper transistors whose size depend on the required power at the output of the amplifier. Purpose of using an RF power amplifier is to obtain high RF signal amplitude levels, which cannot be obtained using oscillators or frequency synthesizers, within a predetermined band of frequencies. Due to ongoing and increasing demand for power versus cost issues, the field has been kept always at the heart of the research and advancement in terms of power utility factor, cost effective solutions and ruggedness. The power utility factor is an important subject because it expresses the extent to which the technology of choice for the implementation of power amplifier can be exploited, safely. It generally determines the physical design space for the PA implementation, without any consideration of DC-RF conversion efficiency. The ruggedness and cost-effectiveness are strongly correlated with the power utility factor, mostly being in a trade-off relationship.

1.1.1 Technologies and Terminologies Used in Design of RF Power Amplifiers

In this section of thesis, we aim to give a brief background information about up-to-date technologies and usual parameters for convenience with the later chapters.

Since GaN HEMT technology is chosen for the application of thesis subject, a short overview is presented.

At the heart of any RF power amplifier, there is a transistor technology which predetermines the limits of the design parameters. The main design parameters of an RF PA can be listed as below.

- Frequency Band
- Bandwidth
- RF Power Output
- Gain
- Efficiency
- Ruggedness
- Thermal Management
- Cost

Parameters mentioned above can be identified as first-pass design goals for RF engineer. At the beginning of the design process, specifications are basically described in terms of these fundamental parameters. Choosing the appropriate technology is actually a milestone in the course of design because it will eliminate most of time consuming work and wasted budget. RF PA design requires expensive measurement equipment and qualified engineering experience together with the costly circuit materials such as transistors, resistors, capacitors. All of these resources are expected to be consumed, optimally.

Transistor technologies used to satisfy particular requirements relating some of the preliminary design goals, are generally fixed. For instance, the frequency band of which the transistor is operating, is the first thing to note. Since an attempt to use the device beyond the frequency limit is not meaningfull, correct selection of semiconductor technology is neccessary. Device manufacturers give the frequency information by indicating the cut-off frequency or providing frequency set in which transistor is internally matched to enable reasonable gain.

RF output power is the result that pays back all the investment in design. Hence the maximum RF power that can be both handled and safely extracted from device, makes this indication rather valuable. This thesis focuses on the technologies so-called discrete transistors, mostly unmatched. To build an SSPA(solid-state power amplifier), MMIC(monolithic microwave integrated circuit) or discretely packaged transistors may be cascaded. All of the cascade, combining operations and device decisions are made based on obtaining the required output power. MMIC technology is practical when device has matched input and output but it may not fit demands for RF power. It can require combination of large amount of MMICs, along with unpalatable combination loss, decreasing the efficiency of whole system, leading to increased monetary budget. After these brief considerations, designer ends up with a reasonable architecture, such as balanced amplifier topologies, single-ended amplifier topology, etc. One may,of course, raise whether every topology providing same RF output power is acceptable. A major debate can be conducted on such a subject, however there are lots of other criterion which can be justified only after constructing it, such as the ACPR, AM/PM distortion rate, EVM and linearity measurements, etc. This is a matter of experience for the designer. Transistor manufacturers also guide designers through the process, because manufacturers generally pinpoint certain set of applications and outstanding features of their devices to ease marketing.

There exists various kinds of gain definitions in the literature. RF PA designer, in particular for high power business, is usually concerned with the large signal gain, but it shows strong dependence on design periphery elements. To justify the anticipated performance of the transistor at first glance, small-signal gain parameters are evaluated. Common gain parameters and their brief descriptions with representations in terms of S-parameters are given below with reference to [1]. A simple schematic representation is given in figure 1.1 for better understanding of reflection planes.

- Transducer Gain (G_T)
  - G_T is defined as the ratio of power delivered to the load P_L to the available power from the source P_{av}. It is formulated as in (1.1). G_T is the general gain parameter which describes the gain without any matching effort. Meaning that input and output matching networks are not neccesar-

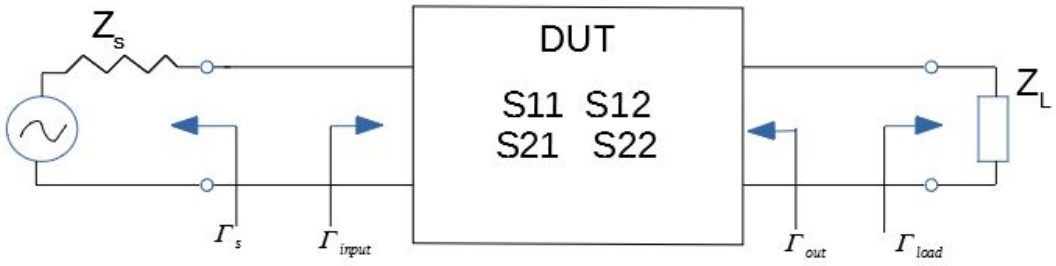


Figure 1.1: Reflection Plane Definitions with a Device Under Test (DUT)

ily designed, it reflects the response of the bare device to the measurement impedance envrionment, usually 50-ohm.

$$G_T = \frac{P_L}{P_{av}} = \frac{(|S_{21}|)^2(1-|\Gamma_s|^2)(1-|\Gamma_L|^2)}{(|1-\Gamma_s\Gamma_{in}|)^2(|(1-S_{22}\Gamma_L)|)^2} \tag{1.1}$$

- Operating Power Gain (G_p)
  - G_p is defined as the ratio of power delivered to the load P_L, to the power delivered from source to the input of device $P_{delivered}$. It is formulated as in (1.2). G_p describes the gain at the condition of matched generator impedance to the input impedance. In other words, generator mismatch is not taken into account. As it is shown in equation (1.2), it only depends on S-parameters of the device and load reflection coefficient Γ_L, since Γ_{in} is dependent on S-parameters and Γ_L. Moreover, it can be deduced from equation (1.1) by setting $\Gamma_s = \Gamma_{in}^*$.

$$G_p = \frac{P_{load}}{P_{delivered}} = \frac{(|S_{21}|)^2(1-|\Gamma_L|^2)}{\left(1-|\Gamma_{in}|^2\right)|1-S_{22}\Gamma_L|^2} \tag{1.2}$$

- Available Power Gain (G_a)
  - G_a is defined as the ratio of power available from the 2-port network P_{avn}, to the power available from source P_{avs}. It is formulated as in (1.3). G_a describes the gain at the condition of matched output impedance to the load impedance. In other words, load mismatch is not taken into account. As it is shown in equation (1.3), it only depends on S-parameters of the

device and source reflection coefficient Γ_s, since Γ_{out} is dependent on S-parameters and Γ_s.

$$G_a = \frac{P_{avn}}{P_{avs}} = \frac{(|S_{21}|)^2(1-|\Gamma_s|^2)}{\left(1-|\Gamma_{out}|^2\right)|1-S_{11}\Gamma_s|^2} \tag{1.3}$$

Applying the above gain definitons, designer is provided with a clue about the small-signal characteristics of the device. In a real application, frequency dependent behavior is the major consideration. Today, manufacturers have strong motivation to present accurate large and small-signal models of the devices. With the help of simulation software, it is easy to get preliminary evaluation of the devices. Large-signal characteristic is the next and most important step in decision process of transistors.

Large-signal capabilities of the transistor and PA determine the final product's performance with various aspects such as signal distortion properties mentioned before. Hence, application-oriented design methods are employed. The optimization of PA occurs throughout the large-signal design steps. Despite the fact that RF PA is a complex device that has many applications and specific requirements, efficiency parameter cannot be overlooked. It is valuable as output power, indeed. It shapes the parameters reflected directly on the cost budget of project. Efficiency affects the thermal management requirements, thermal load of the device thereby the lifetime of device, and power supply capacity. Usually the minimum efficiency that should be maintained in operation can be calculated easily, because device thermal junction to case resistance, maximum allowable junction temperature and thermal load sustainable with the cooling system are well-defined by device manufacturers and system architecture. Employed technology manufacturers exhibit extensive test effort to make sure lifetime specifications are correctly presented. There are reports describing the elaborated qualification process such as [2]. Detailed efficiency related discussions and calculations are provided through the next chapters of this thesis.

For the purposes of verification and qualification of any design, ruggedness is always an issue in terms of PA designer and device manufacturers. Heart of any good design is a reliable transistor with proven capabilities such as Vds breakdown voltage, gate stability and degradation curves under harsh RF, DC, thermal and environmental circumstances. In the literature, various efficiency enhancing methods are shown, but they come along with trade-offs, such as in Class-J method; peaking voltage wave-

forms that may cause irreversible damage to device. About the breakdown mechanisms, extensive investigations can be found in the literature such as the thesis work [3]. Moreover, having the particular interest of this thesis as Class-J approach, specialized study of [4] analyze the hot electron densities and their possible effects on device failure by comparison of DC loading, RF Class-B operation and Class-J operation. It finds out the degradation tendency due to high electric field stress (high Vds), is higher in Class-J operation, possibly affecting the MTBF values. Other than device level tests, PA products are also subject to meet certain constraints one of which is the bad VSWR loading conditions due to antenna itself or in case of a load failure. In short, ruggedness of the amplifier is constantly questioned with particular interest by design process starting from device selection to end-user product.

To sum up, general design parameters and discussion with literature examples are presented within this subsection. A practical approach is adopted to motivate "efficiency" considerations and preliminary ideas about trade-offs. Detailed expressions are left for the next chapters.

1.1.2 GAN HEMT Technology

During the history of RF PA design, various kinds of technologies have been deployed. One of the oldest technology for PA realization is vacuum electronic devices such as TWTAs(traveling-wave tube amplifiers), magnetron, and klystron. Vacuum devices have been utilized for amplification, high-speed switching, and rectifying applications. Their ability to handle high-power makes VEDs good candidates for military and space applications such as RADAR signaling and satellite communications. Along with the benefits they present, some drawbacks are unpalatable such as excessive heat dissipation, bulky structure, high power supply, and complex grid control management [5]. In particular, TWTAs have found a wide range of application areas in satellite communications as downlink power amplifiers, in the 1960s [6]. Though TWTA technology has been the choice over solid-state power amplifiers(SSPA) in space missions due to their unique high rated power and frequency availability[7], SSPAs have been displacing TWTA counterparts rapidly in mid-power radar, jamming [8]. High power particle accelerators are also in demand for SSPA replacements

[9]. Turning to SSPA in those fields are closely related to lower power supply voltages required than TWT operation, design cost, and sustainability issues[8]. Hence the SSPA experiences great advancements in recent years due to increasing market shares and potential usage.

Improvements in semiconductor technologies which are major constituents of SSPA have a significant impact on design dynamics. One of the recent breakthrough materials showing remarkable features is GaN(gallium-nitride). The material has a wider bandgap that is around 3.4 eV, than its competitors as Si(silicon) with 1.12 eV and GaAs(gallium-arsenide) with 1.42 eV [10]. That brings about a higher breakdown voltage which enables operation with a higher drain supply voltage. Higher supply voltage for a specific RF output power means lower current and high output impedance so that it decreases the design complexity of matching networks. Moreover, high saturated drift velocities lead to high power densities, often expressed in watts per unit gate peripheral size. Thereby it takes fewer devices to combine for the specific output power levels than the competing technologies. Reduction in the number of combined devices results in lower capacitance per watts, making the overall device suitable for broadband and high-frequency applications[10]. Table 1.1 shows a comparison of particular parameters for different semiconductor technologies [11].

Table 1.1: Parameters for Microwave Semiconductor Materials

Characteristic Parameter \ Semiconductor Materials	Silicon	Gallium Arsenide	Indium Phosphide	Silicon Carbide	Gallium Nitride
Bandgap (eV)	1.1	1.42	1.35	3.25	3.49
Electron Mobility at 300 ^{0}K (cm^2/ Vs)	1500	8500	5400	700	1000-2000
Saturated Electron Velocity (cm / s) x10^7	1	1.3	1	2	2.5
Breakdown Field (MV / cm)	0.3	0.4	0.5	3	3.3
Thermal Conductivity (W/cm ^{0}K)	1.5	0.5	0.7	4.5	1.5
Relative Dielectric Constant (ϵ_r)	11.8	12.8	12.5	10	9

The higher power density of the material requires careful thermal management to utilize devices safely with optimum performance. For this purpose, GaN is grown upon substrates with reasonable thermal conductivities such as SiC(silicon carbide),

sapphire, and silicon [12]. Accounting for the superior properties of GaN, it seems to be a proper choice for the peaking amplifier classes such as class-J [13]. In summary, GaN technology is gradually improving in its way to challenge existing competents. Although vacuum devices remain the only choice for many high-power applications above kW levels, designers show a strong tendency to employ GaN devices for mid-power and broadband applications in the last decade, especially.

1.2 Resarch Motivations and Objectives

As mentioned in the previous section, an RF PA comes with a large criterion list. The system which involves RF PAs should be carefully established by considering those outlined parameters. The application areas such as jamming, radar, telecommunication, or multi-mission tasks require different conditions to fulfill. In literature, the most prominent parameter is efficiency. Efficiency enhancement methods by continuous modes defining proper harmonic terminations accommodate a remarkable portion of the research. The continuous class-J mode approach is one of the popular subjects of study. J-mode's relatively wide-band potential, almost one-octave, itself, has been investigated to develop methods broadening the bandwidth.

The broadband high-power PAs are attracted to designers for several reasons. Having an amplifier covering a wide range of frequencies decreases the physical size and complexities at the system level. For example, in a jamming application, amplifiers are operated to counteract a particular set of frequency bands. Instead of having multiple narrowband amplifiers, one broadband amplifier does the job more efficiently. Multiple amplifiers require a bulky cable harness, a set of synthesizer RF outputs, and time shared frequency hopping embedded in programming structure and multiple separate antennas leading to shadowing problems. Hence reducing the number of amplifiers by increasing the bandwidth coverage is preferable over multiple PA solutions.

This thesis is not focused on a specific application, though it is generally at the most used communication bands (400-3200 MHz). These frequencies are also the potential targets for jamming in military applications. The communication waveforms have

intrinsic properties such as ACPR(adjacent channel power ratio), PAPR(peak to average power ratio), certain modulation types like OFDM in LTE. In terms of a complete evaluation of linearity, the general design approach of this thesis may remain insufficient to assess the performance of the PA. So, this thesis is not focused on applications demanding high linearity. However, we put high efficiency and broadband in the center of this work, which is the ultimate target for applications in the field of CW(continuous working) amplifiers. The prototype of thesis work is a fine candidate for jamming applications. Although there exists conceptually no burden to use in radar applications, frequency bands in this work are not the same as the well-known military radar bands.

Through this work, we review the existing literature of modified class-J approaches proposing methods to adjust harmonic terminations with resistive parts, with a particular focus on broadband efficiency performance. We combine different perspectives by stating critical measures of performance. A new modification called NRRCJ, "normalized resistive-reactive class-J", is proposed. The theoretical aspects of the approach are analyzed in depth. A design flow for a three-octave amplifier is suggested. The established theoretical flow is experimented with by constructing a prototype RF PA operating in 400-3200 MHz.

The main objectives of this work are are declared as:

- Investigate the continuous mode class-J approach methodologically to enhance operational bandwidth up to more than one octave.
- Present a novel mathematical analysis and comprehension of the proposed method.
- Submit an engineering approach within a detailed design procedure.
- Outline the strong and weak sides of the theory in an objective way.
- Provide the comparison of experimental results and theoretical expectations.

1.3 Contributions

Our contributions are as follows.

- A detailed literature review is presented in the second chapter of this work.
- Existing resitive-reactive class-J proposals are reviewed in detail.
- A novel modification is suggested to remove the "changing DC component" conflict of the theory.
- A novel mathematical analysis is provided by integration of frequency into iterative parametric relations.
- It is shown by theory and applications that there exists a broadband applicable impedance space capable of high efficiency and satisfactory RF output power, without requiring a varying DC component in the voltage waveform.
- A three-octave medium power RF PA , which is operating in the frequently used region of specturm, is prototyped.
- Similar literature examples are compared with the final prototype.
- Future work ideas are suggested to encourage further research on the subject.

1.4 The Outline of the Thesis

In chapter 1, a brief description of RF power amplifiers and basic amplifier parameters are introduced. SSPA and vacuum electronics technologies are compared by considering their usage areas. GaN HEMT technology and other semiconductor technologies are compared by literature search. Thesis motivations and objectives are described. Contributions to the literature are summarized.

Chapter 2 provides an extensive literature review on classical operation modes. The notation convention adopted throughout the theoretical analysis of this work is introduced. Assumptions commonly used in the literature are listed and explained. The load-line theory is described with a detailed explanation.

In chapter 3, we present the modified class-J approaches. The perspectives in the literature are examined. The NRRCJ "normalized resistive-reactive class-J" approach is proposed. Iterative impedance equations are introduced. Voltage waveforms and

impedance spaces are investigated at the current generator plane. Efficiency and power derating curves are introduced with comparsion to existing methods.

Chapter 4 describes the integration of NRRCJ iterative equations into design scheme, at first place. Design parameters are mapped to frequency dependent function forms. To the best of the author's knowledge, a novel parametric analysis is conducted on the subject. After mathematical analysis, a practical procedure is outlined for three-octave PA design. Two prototypes are designed. Simulation and measurement results are discussed. Final prototype is shown to have concurrent performance with the expectations.

Chapter 5 discusses comparison of the similar prototype results with this work. Comparsions show that final prototype shows superior performance than counterparts in many aspects. Achievements of the study, encountered difficulties through the thesis work, strong and weak sides of the study are summarized in conclusions. Some future work ideas are suggested to enhance the research on the subject of this thesis.

CHAPTER 2

LITERATURE REVIEW

This chapter reviews the literature and includes preliminary analysis. Analysis equations are referenced in later chapters, as well. The basic amplifier topologies are overviewed. Basic load-line theory is recalled.

2.1 Conventional Modes of Operation

The classical modes of operation in PA theory is built on ideal FET model which presumes the transistor as a voltage-controlled current source. The assumptions of the ideal FET model are given under classes of operation. Class A, B, AB power amplifiers and general amplifier topology with the widely used parameters are introduced.

2.1.1 Class-A, B and A/B

The basic PA theory starts with the class-A design topology. Conventional classes are generally named in accordance with conduction angle and the loading conditions which shape the matching circuitry at the output. Gain is not considered often since transistors have satisfying gain, mostly. All the features defined for the classes are regarding the ideal transistor model which assumes it as a voltage-controlled current source. The VCCS model assumptions are clearly stated in this section.

For the explanation and analysis of the classes, we use a common circuit schematic in figure 2.1, so that voltage polarities and current directions are consistent. Before going into circuit terms, we recall the fourier series representation of signals for the simplicity of later discussion.

The time harmonic representation of the drain and voltage waveforms can be written as Fourier series expansions of sinusoids. Since both current and voltage are real signals, we use the property of Fourier series given in (2.1)-(2.3).

$$x\left(t\right) = \sum_{n\,=-\infty}^{\infty} c_n exp\left(j2\pi f_0 nt\right) \tag{2.1}$$

If $x\left(t\right)$ is real, then equation (2.1) becomes:

$$x\left(t\right) \; = c_0 + 2Re\left(\sum_{n=1}^{\infty} \left|c_n\right| exp\left(j\varphi_n\right) exp\left(j2\pi f_0 nt\right)\right) \tag{2.2}$$

Where c_n is the complex Fourier series coefficient and can be written as $c_n = a_n + jb_n$, equation (2.2) is rearranged as in (2.3). c_0 is the average(dc) value of the real signal. φ_n is the phase of the nth harmonic content.

$$x\left(t\right) \; = \; c_0 + 2\left(\sum_{n=1}^{\infty} a_n cos\left(2\pi f_0 nt\right) - b_n sin\left(2\pi f_0 nt\right)\right) \tag{2.3}$$

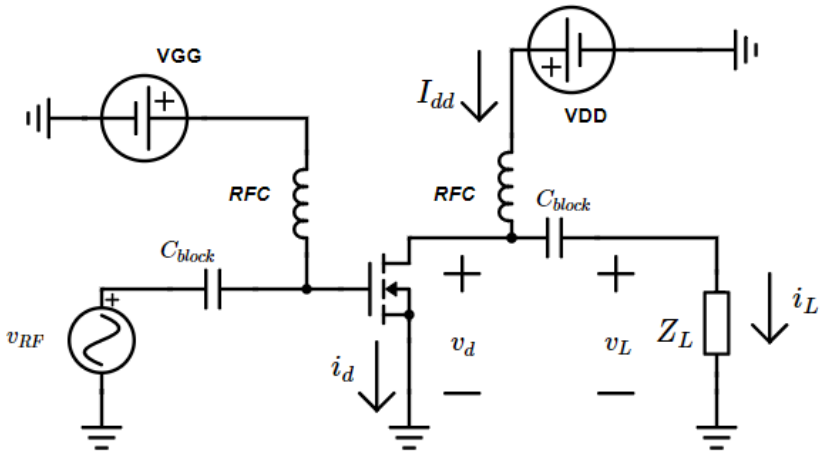


Figure 2.1: Transistor and surrounding RF circuit diagram showing used current conventions.

Using the above short recall, we can define time harmonic expansion of drain voltage $v_d\left(\theta\right)$ and drain current $i_d\left(\theta\right)$ by absorbing the factor "2" into the coefficients. Figure 2.1 is the reference for all of the circuit equations in this section.

$$v_d\left(\theta\right) = \; V_{dd} + \left(\sum_{n=1}^{\infty} V_{n,r} cos\left(n\theta\right) - V_{n,q} sin\left(n\theta\right)\right) \tag{2.4}$$

$$i_d(\theta) = I_{dd} + \left(\sum_{n=1}^{\infty} I_{n,r} cos(n\theta) - I_{n,q} sin(n\theta) \right) \tag{2.5}$$

Equations (2.4)-(2.5) express the current and voltage waveforms by in-phase and quadrature parts, where $\theta = 2\pi f_0 t$. Current and voltage waveforms are all assumed at the intrinsic current generator plane of the transistor. Intrinsic current generator is a hypothetical plane of reference in VCCS model, which will be elaborated under subsection 2.1.2. DC block capacitor in figure 2.1 is assumed ideal so that voltage drop across it is zero. The circuit nodal equations are simply written as in (2.6)-(2.7)

$$i_d(\theta) = I_{dd} - i_L(\theta) \tag{2.6}$$

$$v_d(\theta) = V_{dd} + v_L(\theta) \tag{2.7}$$

Using (2.4) - (2.7), we find load voltage and current expressions at the generator plane.

$$v_L(\theta) = \left(\sum_{n=1}^{\infty} V_{n,r} cos(n\theta) - V_{n,q} sin(n\theta) \right) \tag{2.8}$$

$$i_L(\theta) = -\left(\sum_{n=1}^{\infty} I_{n,r} cos(n\theta) - I_{n,q} sin(n\theta) \right) \tag{2.9}$$

$$I_n = I_{n,r} + jI_{n,q} \tag{2.10}$$

$$V_n = V_{n,r} + jV_{n,q} \tag{2.11}$$

Equations (2.8)-(2.11) shows the general phasor domain expressions which will be exploited in calculations of impedance, power and efficiency.

$$Z_n = -\frac{V_{n,r} + jV_{n,q}}{I_{n,r} + jI_{n,q}} = -\frac{|V_n|}{|I_n|} e^{(j\varphi_{n,v} - \varphi_{n,i})} \tag{2.12}$$

$$P_n = -\frac{1}{2} Re\{V_n I_n^*\} = -\frac{1}{2}(V_{n,r}\ I_{n,r}\ + V_{n,q} I_{n,q}\ ) \tag{2.13}$$

We presented the fundamental equations that we are going to address in explanation of classes. We could move on to identify the classes.

Class-A is generally understood as ideal linear amplifier in the PA designer community. The reason is that the Class-A amplifier output spectrum doesn't include any harmonics, theoretically. Of course, theory is defined such that the overdrive above the linear region of amplifier is not allowed. After a certain drive level it also becomes naturally a nonlinear amplifier. To understand the class-A definition, a generic I-V curve profile is given in figure 2.2. The horizontal axis is the drain-to-source voltage and the vertical axis is the drain current drawn from the supply.

Figure 2.2: I-V current profile of a simple FET

Figure 2.2 reflects a rough representation of a FET DC I-V characteristic. I_{max} is the maximum current that the device can support. V_{knee} is the critical drain-source voltage below where device current is a strong function of V_{gs} and V_{ds}. That region is called the "triode" or "knee region". Above knee voltage level, transistor is in saturation regime and device current is strongly function of V_{gs} with neglected effect of V_{ds}. For any amplifier topology, the gate bias point, which is the constant dc voltage applied to gate, and the drain bias point, which is the supply voltage, determine the "quiescent" point. Q-point is actually a DC boundary condition that should be satisfied by RF load-line. When RF signal is applied to gate, it causes a current and voltage swing at drain terminals around Q-point. In order to have a harmonic-free spectrum, the

current and voltage swing should not be distorted or clipped upto I_{max} and before reaching V_{knee}. Thereby, the Q-point of Class-A is adjusted to the half of maximum drain current. In process of biasing, supply voltage V_{dd} is generally predetermined at the system level, what remains is to decide on gate voltage. By equations (2.6) - (2.13), the RF signal is superimposed onto DC signal and the complex impedance of the load constraints the amplitude and phase of the current and voltage swing.

At this point we should state the assumptions made in the upcoming analysis:

(a) Drain current is directly related to gate voltage excursion by constant transconductance.

(b) Knee region (triode region) where channel current is a strong function of drain-source voltage $v_d(\theta)$ is neglected.

(c) Due to (b), R_{on}, which is on resistance of the channel is neglected.

(d) "DC-RF"dispersion, or alternately referred as “knee walkout” phenomenon; on which there is a great effort to include into transistor models with the studies as in [14], is neglected.

(e) Voltage and current at the intrinsic plane cannot be negative. Since intrinsic plane is hypothetical, this is stated as an assumption. Lots of research and achievements can be found in the literature to model the voltage and current nonnegative at this plane, such as the extensive thesis study in [15].

In the light of assumptions (a)-(e), a basic constant transconductance VCCS model schematic is given in figure 2.3 for the sake of discussion. For the class-A bias we can express the voltage and current equations by modifying (2.6) - (2.11).

$$i_d(\theta) = \frac{I_{max}}{2} - I_L cos(\theta) \tag{2.14}$$

$$v_d(\theta) = V_{dd} + V_L cos(\theta + \varphi) \tag{2.15}$$

(2.14) and (2.15) are the general waveform expressions of which amplitude changes with the driving RF signal level. In addition, (2.15) includes a free phase variable φ that depends on the fundamental load impedance. The phase shift of voltage is an

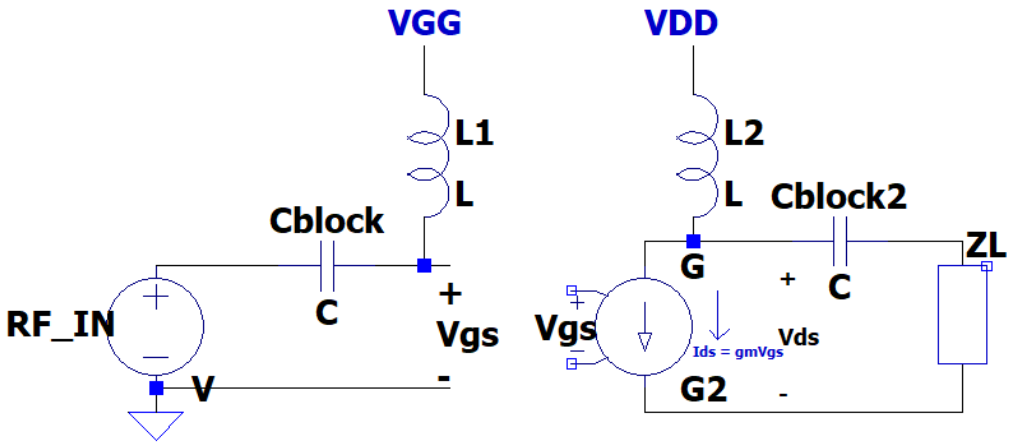


Figure 2.3: Basic Constant Transcoundactance VCCS Model

important parameter because it directly affects fundamental power delivered to load, thereby, the efficieny.

Equation (2.14) tells us the DC power consumption in Class-A is independent of the drive level or output power. It means the more RF power delivered to load, the more efficiency is obtained. Class-A reaches its maximum efficiency point at maximum linear drive level, where it happens at $I_L = I_{max}/2$. To maximize the RF power dissipated at the load, we should have a completely resisitive optimum load which won't cause the voltage swing below zero when current is maximum. Hence the maximum value of $V_L = V_{dd}$ should be reached for the optimum output power,as well. We should emphasize that the knee voltage is assumed as "0". The drain current and voltage waves at maximum drive level are shown in the figure 2.4, in normalized amplitudes. The voltage, current, P_{RF}, P_{DC} and efficiency calculations are expressed in (2.16) - (2.20). The calculations are done, setting $\varphi = 0$. The RF load-line superimosed onto DC I-V curve is seen in figure 2.5.

$$i_d(\theta) = \frac{I_{max}}{2} - \frac{I_{max}}{2} cos(\theta) \tag{2.16}$$

$$v_d(\theta) = V_{dd} + V_{dd} cos(\theta) \tag{2.17}$$

$$P_{RF} = \frac{V_{dd} I_{max}}{4} \tag{2.18}$$

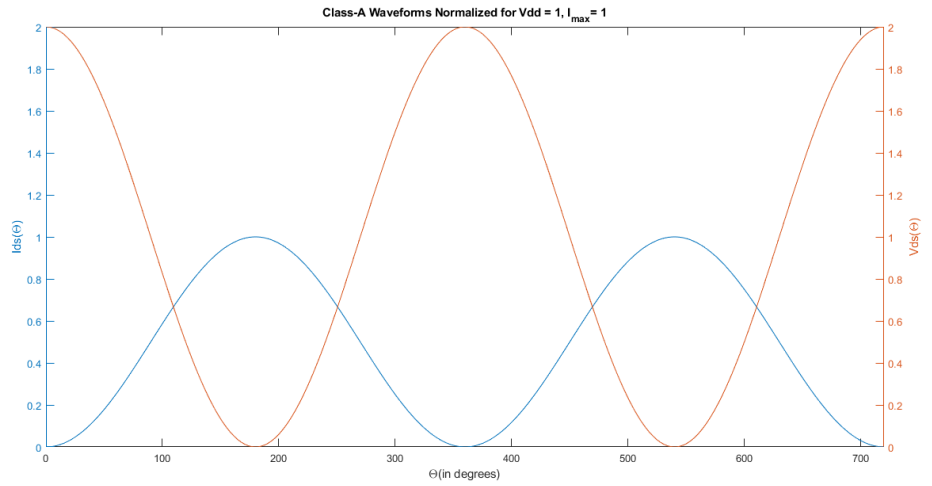


Figure 2.4: Class-A Drain and Current Waveforms for V_{dd} = 1, I_{max} = 1

$$P_{DC} = \frac{V_{dd} I_{max}}{2} \tag{2.19}$$

$$\eta_{max} = \frac{P_{RF}}{P_{DC}} = \%50 \tag{2.20}$$

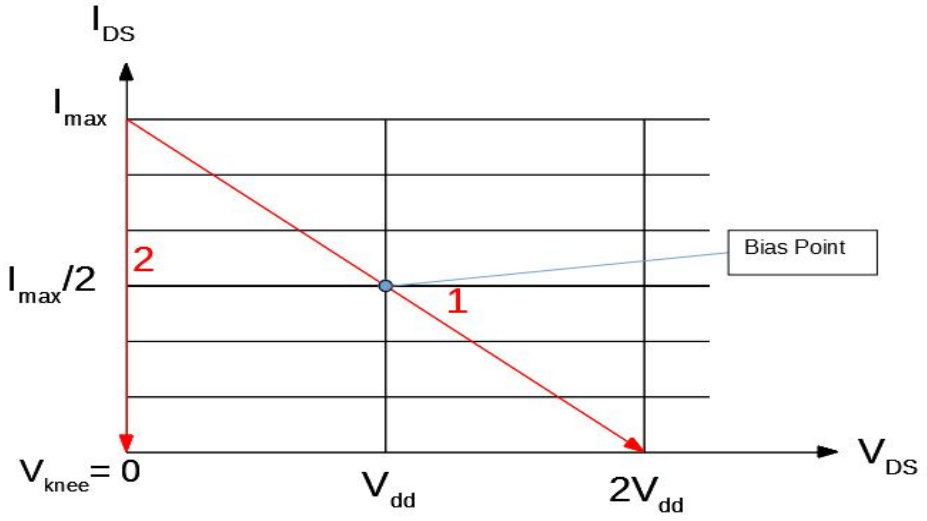


Figure 2.5: Red-line paths showing dynamic I-V loadline. The knee voltage is zero.

In figure 2.5, the I-V trace is divided into two paths numbered as 1, 2. Indeed, path 1 and 2 form a complete one path, but the path 2 is only traced when the amplifier

is overdriven from the gate. Path 2 is a special case which will be reported in the next section. As long as nominal drive signal is applied, the path 1 is traced equidirectional. Agreement is easily seen compared with figure 2.4. The reason of setting $\varphi = 0$, is having the maximum power at the load, thereby maximizing efficiency. It also implies a purely resistive load, which is so-called "optimum class-A load", $R_{opt,A}$. Optimum load is calculated using equation 2.12.

$$R_{opt,A} = \frac{2V_{dd}}{I_{max}} \tag{2.21}$$

Class-B amplifier is the starting point of almost every high efficiency amplifier mode, since it constraints the harmonic loading condition together with the bias state. The outstanding difference from class-A is, high efficiency with the same amount of maximum RF power transfer to the load. In discussion of class-B, "conduction angle" term is widely used in the literature. We will show the conduction angle with α. Coonducting cycle of the transistor means the time or angular time that the transistor drain current i_d is nonzero. In class-A, $\alpha = 2\pi$ as seen from figure 2.4. For the class-B case, transistor Q-point is at "zero current" bias point. Hence, device doesn't conduct until an RF input excitation above the transistor gate threshold.

At the first step of Class-B analysis, we assume current waveform doesn't include quadrature components, meaning that $I_{n,q} = 0$ for all "n". Having quadrature components zero implies the "even" function property around zero conduction angle. The class-B half wave rectified sine current is the usual convention at the beginning of high efficiency mode analysis as in fundamental examples from literature, [16, 17, 18, 19, 20, 21, 22]. In the light of above assumptions (a)-(e), we can express the class-B current waveform and the version of common practical interest which is the class A/B waveform. All the assumptions are valid for class A/B, as well. The class-B waveform can be seen in figure 2.6.

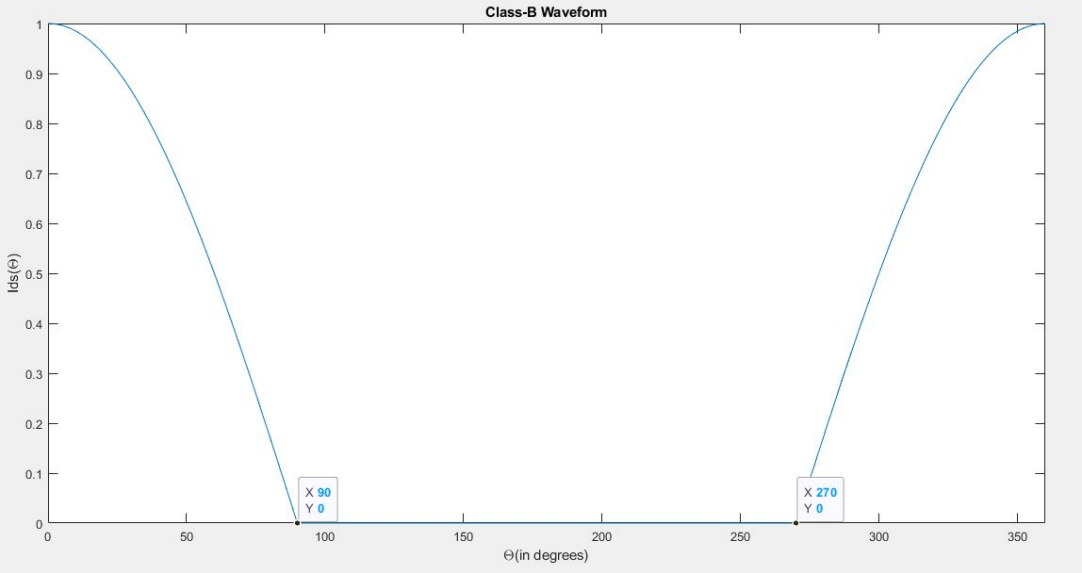


Figure 2.6: Conventional Class-B Waveform (Normalized to Peak Value)

The waveform can be written as a composition of harmonics in equations (2.22) - (2.23). From (2.22) and (2.23) , there only exists even harmonics, and waveform can be written in open form as given by (2.24) - (2.25).

$$i_d(\theta) = \frac{I_{max}}{\pi} + \left(\sum_{n=1}^{\infty} I_{n,r} cos(n\theta) \right) \tag{2.22}$$

$$I_{n,r} = \begin{cases} \frac{I_{max}}{2} & ; n\text{=1} \\ \frac{2I_{max} cos\left(n\frac{\pi}{2}\right)}{\pi(1-n^2)} & ; n\text{= 2, 4, 6, ...} \end{cases} \tag{2.23}$$

$$i_d(\theta) = \frac{I_{max}}{\pi} + \frac{I_{max}}{2} cos(\theta) + \frac{2I_{max}}{3\pi} cos(2\theta) - \frac{2I_{max}}{15\pi} cos(4\theta) + \frac{2I_{max}}{35\pi} cos(6\theta) - \dots \tag{2.24}$$

$$i_L(\theta) = -\frac{I_{max}}{2} cos(\theta) - \frac{2I_{max}}{3\pi} cos(2\theta) + \frac{2I_{max}}{15\pi} cos(4\theta) - \frac{2I_{max}}{35\pi} cos(6\theta) + \dots \tag{2.25}$$

So far, we did nothing but recall the classical analysis steps of class-B type current waveform by stating underlying assumptions. Efficiency and RF power output considerations become totally dependent on the load impedance Z_n at fundamental and harmonics. I_{max} in equations (2.22) - (2.25) expresses the saturated drain

current waveform without clipping. In real conditions, voltage clipping due to harmonic impedances will modify the current waveform, yet we didn't analyze the load impedance. Current waveform is dependent on the drive level (linearly by the assumptions (a)-(e)), and subject to change following the load impedance for reaching the required output power. The load impedance in class-B analysis is assumed to be short circuit at all harmonic frequencies. So, the voltage waveform can be written as in (2.26) and (2.27).

$$v_d(\theta) = V_{dd} + V_{1,r}cos(\theta) - V_{1,q}sin(\theta) \tag{2.26}$$

$$V_d(t) = V_{dd} + \sqrt{V_{1,r}^2 + V_{1,q}^2}cos\left(2\pi f_0 t + atan2\left(\frac{V_{1,q}}{V_{1,r}}\right)\right) \tag{2.27}$$

Equation (2.27) can be expressed in a compact way in (2.28).

$$V_d(t) = V_{dd} + V_1 cos(2\pi f_0 t + \varphi_1) \tag{2.28}$$

Indeed, the formulations with the above analysis cause some constraints on the fundamental load impedance. A few comments must be made at this point for the clarity. These can be ordered as follows:

- Equation (2.28) implies a strong condition on the fundamental swing of drain voltage. By the derivation procedure, we always assumed that voltage clipping doesn't occur and thereby, cannot affect the current waveform shape. If the voltage clipping was accepted, current waveform would be distorted such that it would have the odd harmonics, as well.

- If we would allow the voltage clipping which means to let $V_1 \geq V_{dd}$, then (2.27) couldn't not be the frequency domain representation of the voltage signal. Since we set the load as short circuit for harmonics it could mean infinite current at the harmonics, which is impossible. By forcing load at shorted harmonics, we are confronted with following cases:

  (i) Current waveform should go to zero immediately whenever voltage clipping occurs (trying to go below zero). This implies a discontinuity at I-V waveforms which is physically not possible.

(ii) An instant discontinuity forces voltage wave with non-zero harmonics and this breaks the conditions at the load plane such that harmonic impedances become undefined.

(iii) If the fundamental load magnitude is higher than optimal load, the voltage wave is forced to zero instantly, when maximum drive from input is applied

In figure (2.7), the knee voltage "zero" assumption and the possible trajectories of the I-V curve is plotted in red. Trajectory 1 is analyzed under linear calculations. But in cases where (i-iii) happens, trajectory 2 remains as the only path and, the discontinuity must be defined. Thereby, in order to analyze the overdrive or unconstrained load conditions some assumptions should be released. Before going into that, behavior in path 1 is going to be studied.

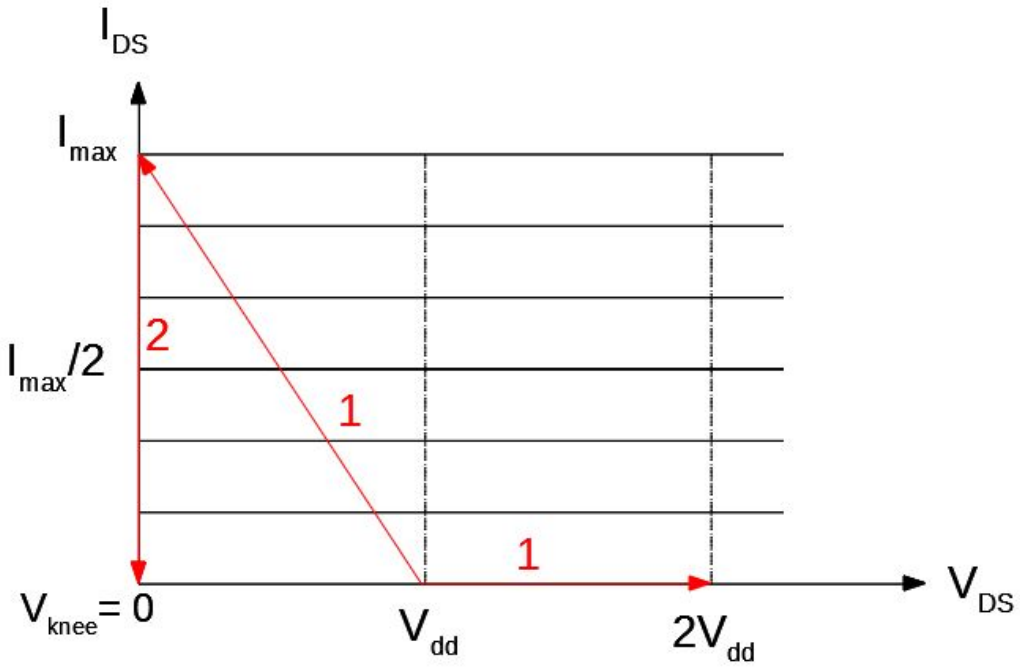


Figure 2.7: Zero-knee load-line trajectory for class-B

By setting $\varphi_1 = 0$, and $V_1 = -I_1 Z_1 = -V_{dd}$ in (2.28); we find the optimum load for maximum power and efficiency expressed in (2.29 - 2.30).

$$R_{opt,B} = Z_1 = \frac{2V_{dd}}{I_{max}} \tag{2.29}$$

$$\eta_{max} = \frac{P_L}{P_{dc}} = \frac{V_{dd}^2 / (2R_{opt,B})}{V_{dd} I_{max}/\pi} = \frac{\pi}{4} \approx \%78.5 \tag{2.30}$$

Due to the current direction adopted in figure 1, the equation (2.28) is re-written for the maximum drive at optimum load in (2.31).

$$V_d(t) = V_{dd} - V_{dd} cos(2\pi f_0 t) \; ; \; V_d(\theta) = V_{dd} - V_{dd} cos(\theta) \tag{2.31}$$

The current and voltage waveforms drawn on top of each other is given in figure (2.8), and the correlation with the I-V curve presented in figure (2.7) can be easily interpreted, whereas path 2 in figure (2.7) is absent.

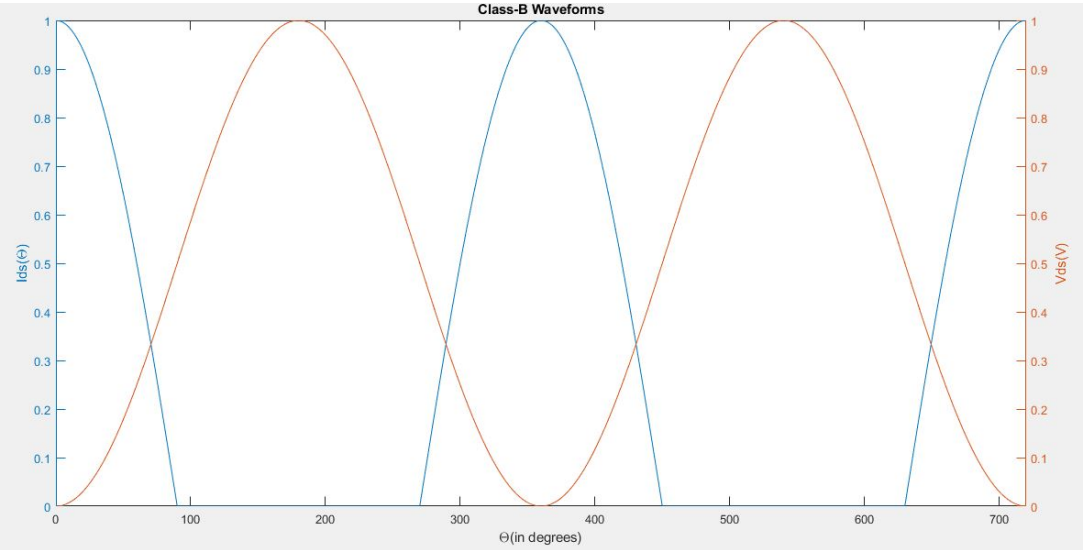


Figure 2.8: Class-B voltage and current waveforms normalized to their peak value ($R_{opt} = 1$,$V_{dd} = 0.5$,$I_{max} = 1$)

In order to encapsulate the overdrive cases in which voltage or current clipping occurs, a knee-region model must be used. Generally, the transistor I-V curve, so-called "fan diagram" looks like in figure (2.9). Dynamic load-line of class-A and B drawn over the figure, as well.

So far, in our review, the region where the drain voltage drops down the knee voltage is not considered, whereas practical linear RF power output and the efficiency is limited by the knee region. Though linearity is not only dependent on the how much the amplifier's operation is into the knee region, the strongest constraint seems as the knee region due to neglected gate and drain nonlinearities. In Rhodes' work [17],

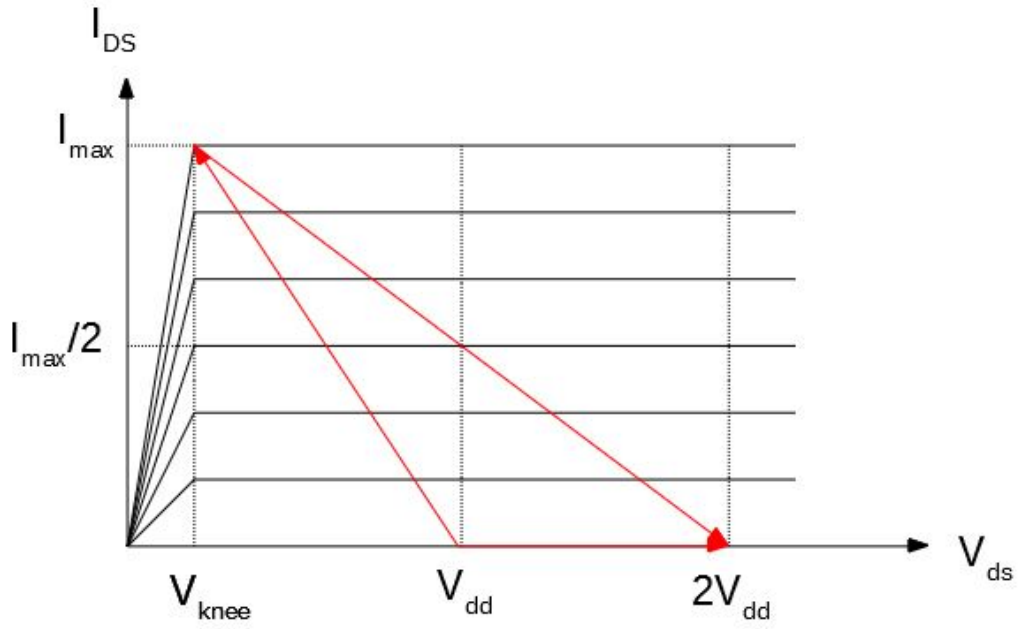


Figure 2.9: Non-zero knee voltage fan diagram

this discontinuity is modeled with a simple delta function. This model is given by equations (2.32) - (2.33) as for a quick reference.

$$H(\theta) = -I_{max}\varepsilon\delta(\theta) \qquad ;0 \leq \theta \leq 2k\pi \tag{2.32}$$

Where ε is the proportionality constant of delta discontinuity for the drain current. We chose to re-write the discontinuity at $\theta = 0$ to be consistent with our analysis approach of which the transition from linear to knee region is at this point, whereas it is defined at $\theta = \frac{\pi}{2}$ in [17]. Equation (2.33) shows the cosine series form. (2.34) is the current waveform after superposition of the delta discontinuity.

$$H(\theta) = \frac{-I_{max}\varepsilon}{(2\pi)}\left[1 + 2cos(\theta) + 2\sum_{n=2,3,4,..}^{\infty} cos(n\theta)\right] \tag{2.33}$$

$$\widetilde{i_d}(\theta) = i_d(\theta) + H(\theta) \tag{2.34}$$

The modified efficiency, optimum load, RF output power equations for the class-B loading according to (2.34) can be written as in (2.35 - 2.38).

$$P_L = \frac{I_{max}}{(4\pi)}(\pi - 2\varepsilon)V_{dd} \tag{2.35}$$

$$P_{DC} = \frac{I_{max}}{(4\pi)}(2-\varepsilon)V_{dd} \tag{2.36}$$

$$\hat{R}_{opt} = \frac{2V_{dd}}{I_{max}}\left(\frac{\pi}{\pi-2\varepsilon}\right) \tag{2.37}$$

$$\hat{\eta}_{max} = \frac{\pi}{4}\left(\frac{1-2\varepsilon/\pi}{1-\varepsilon/2}\right) \tag{2.38}$$

Efficiency and optimum load change vs. proportionality constant are plotted in figure (2.10).

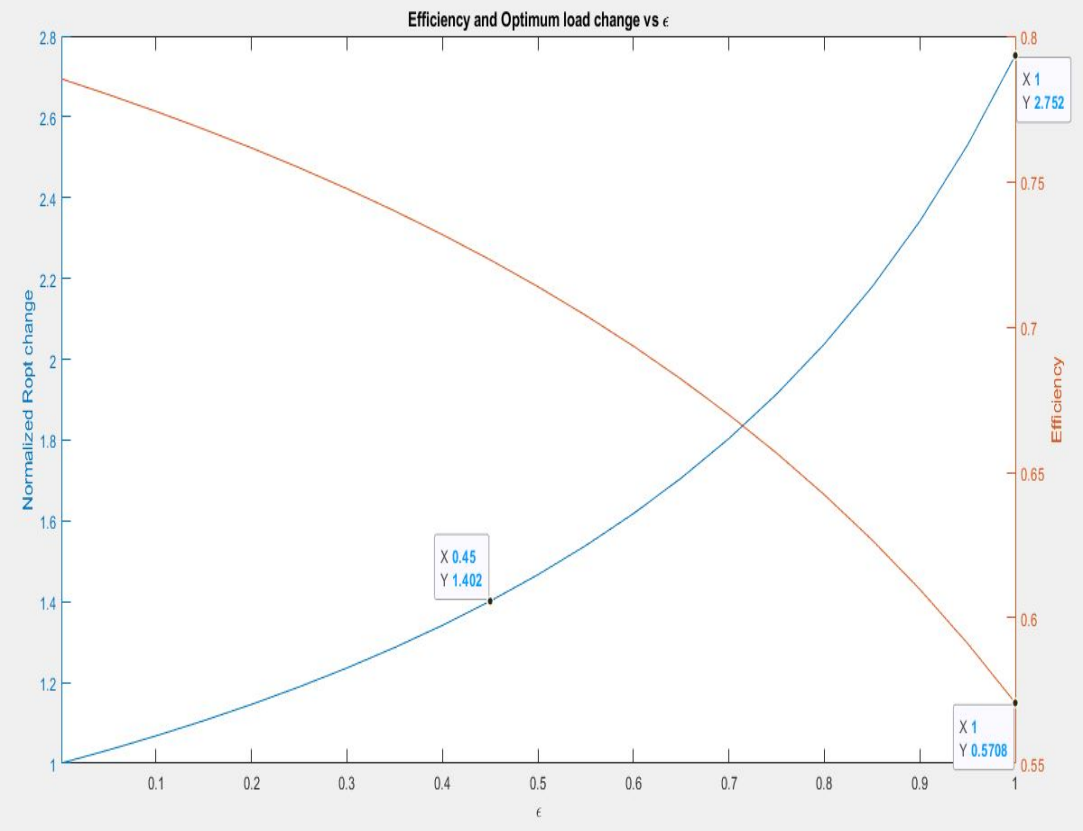


Figure 2.10: Normalized optimum load and efficiency change vs ε factor

By showing this model, we are not justifying the accurateness but emphasizing the effect of knee transition on efficiency. From figure 2.10, it is easily understood that optimum load and efficiency aggressively react to even a small perturbation of drain current. Efficiency approaches from %78 to %58 and optimum required load rises to nearly threefold. In short, the model of the knee region becomes particularly impor-

tant when it comes to drive the PA into saturation region. There are various studies which are involving behavioral or purely mathematical models such as [23, 24, 25]. The brief discussion of this simple zero-knee model is provided for better comprehension of the following sections of the thesis.

Having class-A and B discussion above, we can continue with the class A/B analysis which is the most used class group in practice because of the gain advantages. Up to now, gain is not considered as a parameter for discrimination of classes so as in literature. The gain of the amplifier is an important metric in practical applications as much as power and efficiency but the discussion of gain enforces to account for the gate and drain relation together. We are not going to elaborate on the gain in the theoretical analysis. With very practical thinking, as the conduction angle decreases the gain proportionally decreases since for the same drive level, less fundamental power is generated at the output. The current conduction angle is an important parameter for the drain and CCA(current conduction angle) derivation will be illustrated.

CCA is angular time portion that the transistor drain conducts current. In figure 2.11, the conducting cycle in a period is illustrated with the even current function as it is done in class-B analysis. Equation (2.39) shows the waveform mathematical expression as a piecewise continuous function, where I_{pk} is a temporary variable used to resemble cosine function [26]. In equations (2.40)-(2.42), CCA definition in terms of I_{dq} auxiliary drain bias current and I_{max} is derived. (2.43) gives the fourier series expansion coefficients as in (2.5). Since we maintained the even function property of the current, quadrature components $I_{n,q} = 0$ is still valid.

$$i_d(\theta) = \begin{cases} I_{dq} + I_{pk} cos(\theta) & ; -\frac{\alpha}{2} \leq \theta \leq \frac{\alpha}{2} \\ 0 & ; \text{otherwise} \end{cases} \tag{2.39}$$

$$i_d(\theta = 0) = I_{max} = I_{dq} + I_{pk} \quad \text{, by figure 2.11} \tag{2.40}$$

$$i_d\left(\theta = \frac{\alpha}{2}\right) = 0 = I_{dq} + I_{pk} cos\left(\frac{\alpha}{2}\right) \quad \text{, by figure 2.11} \tag{2.41}$$

$$cos\left(\frac{\alpha}{2}\right) = -\frac{I_{dq}}{I_{max} - I_{dq}} \tag{2.42}$$

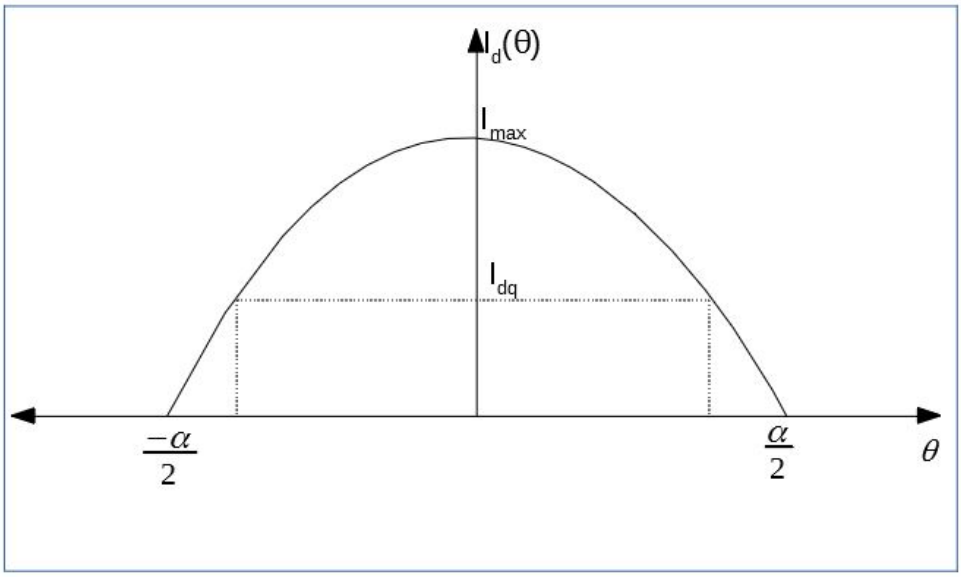


Figure 2.11: Current waveform with α conduction angle

$$I_n = \begin{cases} \frac{I_{max}}{2\pi}\frac{2sin\left(\frac{\alpha}{2}\right)-\alpha cos\left(\frac{\alpha}{2}\right)}{1-cos\left(\frac{\alpha}{2}\right)} & ; n=0 \\ \frac{I_{max}}{2\pi}\frac{\alpha-sin(\alpha)}{1-cos\left(\frac{\alpha}{2}\right)} & ; n=1 \\ \frac{2I_{max}}{\pi}\frac{sin\left(n\frac{\alpha}{2}\right)cos\left(\frac{\alpha}{2}\right)-nsin\left(\frac{\alpha}{2}\right)cos\left(n\frac{\alpha}{2}\right)}{n(n^2-1)\left[1-cos\left(\frac{\alpha}{2}\right)\right]} & ; n\geq 2 \end{cases} \tag{2.43}$$

From series coefficiencts shown in (2.43), it can be easily confirmed that the harmonic amplitudes and phases are strongly dependent on the CCA. Figure (2.12), shwos the current harmonic magnitudes,I_0, I_1, I_2, I_3normalized to I_{max} with respect to conduction angle, where I_0 is the DC current.

Figure (2.12) plots the conduction angle from 0 to 2π, but the class A/B conduction angle is defined in between π to 2π. From (2.43) we see the current fundamental component also varies with α thereby fundamental optimum resistive load changes, respectively. It is necessary to re-state the assumption that we impose short-circuit condition for the load impedance seen by higher harmonics.

Figure (2.13) illustrates the fundamental optimum load change versus conduction angle $\frac{\pi}{2} \leq \alpha \leq 2\pi$. Illustration regime is selected such that the scaling of the graph

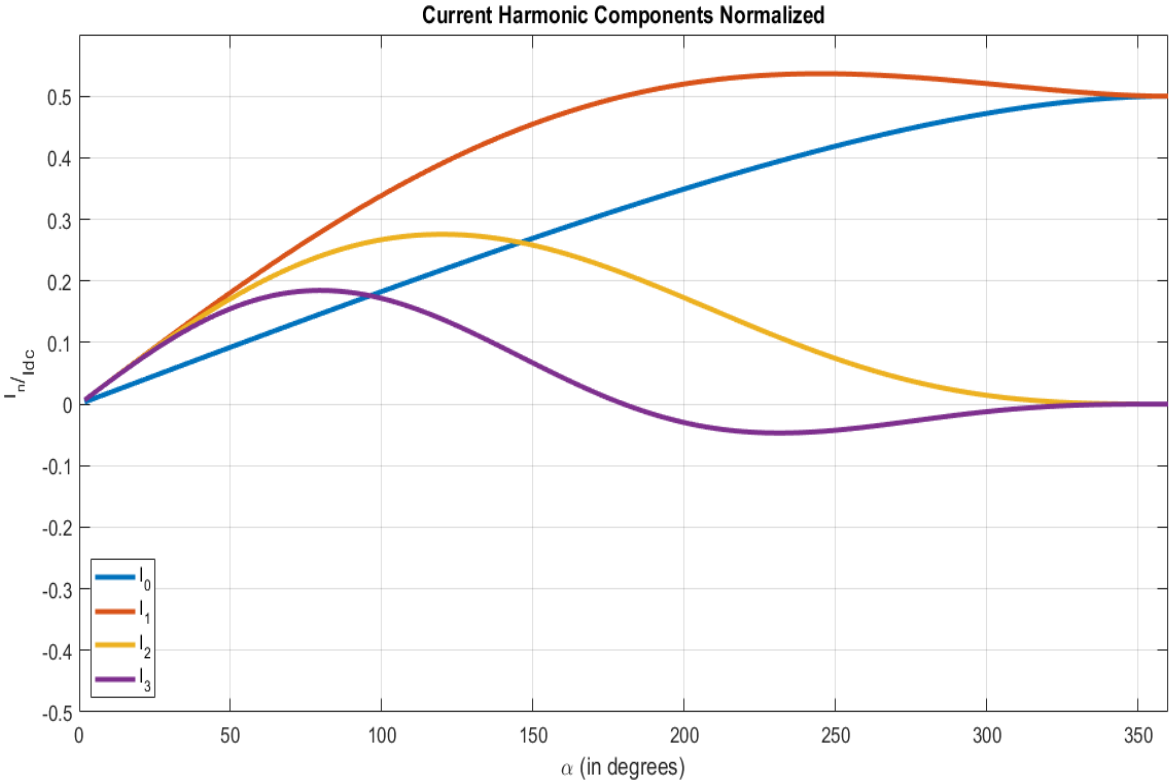


Figure 2.12: Conduction angle versus normalized harmonic amplitudes.

remains in reasonable limits. The optimum load deviates from the class-A, or B load around $\%7$ downwards, at maximum, for $\pi \leq \alpha \leq 2\pi$. On the other hand, for $\alpha \leq \frac{\pi}{2}$, optimum load increases, drastically. As mentioned before, the advantage for class A/B over class-B is the increased available gain due to the conduction angle increase. If the bias point is closer to class-B, then it is referred as "deep" class A/B [13]. The deep class A/B is the most encountered version in CW(continuous working) amplifiers since biasing transistor close to class-A causes overheating for even short periods, in which no RF signal input is present. Below the conduction angle of π, available maximum RF power decreases due to maximum voltage swing limited to V_{dd} by the short harmonic load constraints.

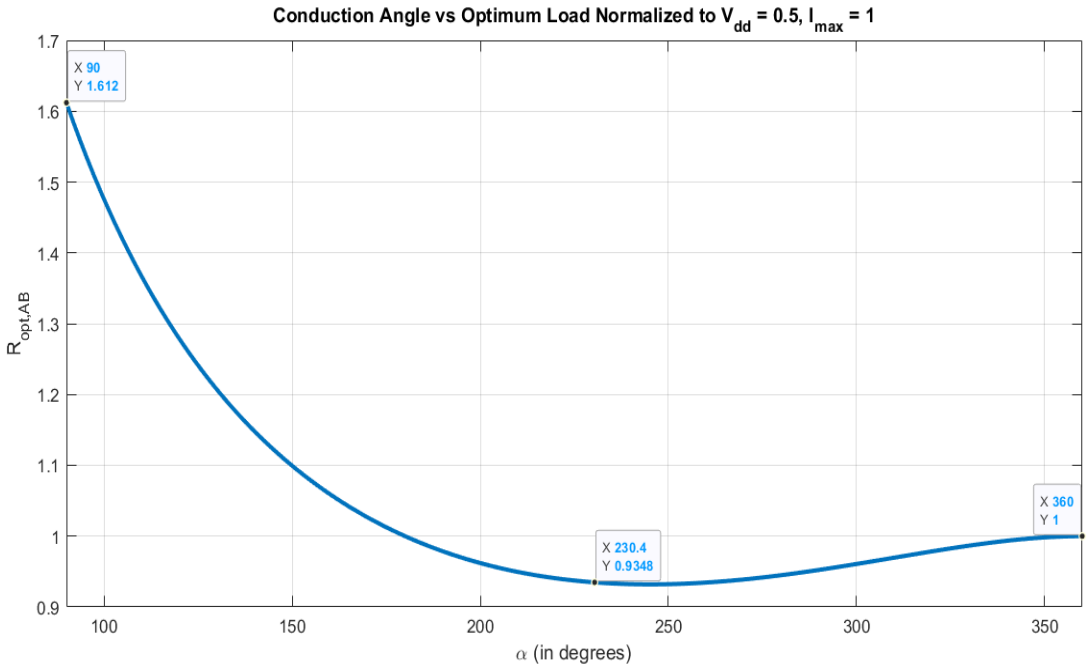


Figure 2.13: Conduction angle versus optimum load.

For the conduction angle values below π, other high-efficiency operation modes exist. Whereas high-efficiency classes are categorized with respect to harmonic loading conditions in addition to the conduction angle bias point. One of these high efficiency modes, class-J, is the particular interest of this thesis. Other well-known high efficiency modes, class C, F and F^{-1} will be roughly mentioned under explanation of class-J theory.

Consequently, this section covered the basic amplifier classes, A, B, A/B which forms the fundamental basis of other classes. The terms, such as knee voltage, transistor operating regimes, conduction angle, load harmonic analysis, vccs model, optimum resistive load, RF output power and efficiency, are explained, in detail with reference to literature. The reader may apply to the resources of this section for further knowledge, whereas the short review of this section is predicted to be sufficient for the upcoming chapters of this thesis.

2.2 Load-Line Theory of Ideal Linear Amplifier

In the previous section, we analyzed the conventional PA classes with a purely resistive fundamental load. In particular, only the optimum load which provides highest RF power, was evaluated. This section considers the fundamental complex load conditions and its systematic explanation by the "Load-line theory of ideal amplifier". This chapter actually re-states the article [18] and, the chapter 2.4 of the book [16] in our formulation. In terms of understanding the complex loading condition, this section conveys strong intuition to reader.

Any PA operates in particular frequency range and this range enforces a load impedance variaton by frequency. The extent of impedance deviation from the optimum loading condition and its effect on performance should be justified. Theoretical load-line approach makes it possible to trace impedance contours indicatiing the boundaries for constant RF power output levels.

We adopt the voltage and current directions in circuit of figure 2.1. The assumptions (a)-(e) in subsection 2.1.1 are still valid for the following analysis. The bias condition is class-A, but the loading condition is changed such that load is allowed to be complex. Since our idealized model is biased in class-A and overdrive (driving beyond linear region) is not considered, harmonics of voltage or current wave don't exist. Equations (2.14) and (2.15) are useful to re-write at this point.

$$i_d(\theta) = \frac{I_{max}}{2} - I_1 cos(\theta) \tag{2.44}$$

$$v_d(\theta) = V_{dd} + V_1 cos(\theta + \varphi) \tag{2.45}$$

Free variables V_1 and I_1 of equations 2.44 and 2.45 are constrained to current and voltage clipping conditions imposed by our linear region analysis. These constraints are expressed as in 2.46, 2.47.

$$i_d(\theta) \geq 0, \quad for\ 0 \leq \theta \leq 2\pi \tag{2.46}$$

$$v_d(\theta) \geq 0, \quad for\ 0 \leq \theta \leq 2\pi \tag{2.47}$$

For V_1 and I_1, conditions can be derived from (2.46-47), as indicated by intervals in (2.48).

$$0 \leq V_1 \leq V_{dd} \ , \ 0 \leq I_1 \leq \frac{I_{max}}{2} \tag{2.48}$$

To trace impedance contour for a constant power output level we use two alternate definitions of RF output power. Reasoning for employment of two equations is unrevealed in the next steps of analysis.

$$P_{RF} = \frac{1}{2} V_1^2 G_L \ \ or \ P_{RF} = \frac{1}{2} I_1^2 R_L \tag{2.49}$$

Where G_L and R_L are real part of load admittance and impedance, respectively. As it is mathematically represented by $Z_L = R_L + jX_L, Y_L = G_L + jB_L$. In our previous analysis it is found that output power of class-A occurs at purely real load, which allows maximum unclipped voltage and current swing, simultaneously. Equations (2.18 -2.21) state the optimum loading case. As we know the maximum power, we need to derive conditions for constant power levels. We start investigation by defining a back-off parameter σ which is employed as $P_{RF} = P_{opt}/\sigma$ for $1 \leqslant \sigma < \infty$.

By equalities in (2.49), it is inferred that constant G_L or R_L contours lead to equal RF power for the same driving conditions. The only missing parameter, relating these two equations is imaginary part of the load impedance. We may start with a simple speculation to account for the effect of imaginary part.

(2.49) is modified by σ as:

$$P_{RF} = \frac{P_{opt}}{\sigma} = \frac{\frac{1}{2} V_{dd}^2 G_{opt}}{\sigma}. \tag{2.50}$$

Hence, denoting $G_L(\sigma) = G_{opt}/\sigma$ is legal by simple substitution untill this point. To check if it is legitimate, it should meet constraints of (2.48). We can express complex load as $Y_L(\sigma) = G_{opt}/\sigma + jB_L$. Contiuning with voltage- current relations, we obtain (2.51).

$$\begin{aligned} V_L Y_L &= I_L, \\ |I_L| &= I_1, \\ \Rightarrow I_1 &= V_1 |Y_L| \\ &= V_1 \sqrt{G_{opt}^2/\sigma^2 + B_L^2} \end{aligned} \tag{2.51}$$

Re-calling again (2.49) and conditions given in (2.48), it is clear that V_1 can be driven up to V_{dd} to obtain maximum linear RF output power, whereas I_1 is a bounding factor on imaginary part of load admittance B_L. Hence, by setting $V_1 = V_{dd}, I_1 = I_{max}/2$, (2.51) is re-written as:

$$\frac{I_{max}}{2} = V_{dd}\sqrt{G_{opt}^2/\sigma^2 + B_L^2} \tag{2.52}$$

The boundary conditions of (2.48) is imposed on to (2.51) to represent the upper bounding case of drain current. We may re-write the inequality as in (2.53) at the maximum input drive power meaning that $V_1 = V_{dd}$ is enforced.

$$I_1 = \frac{I_{max}}{2} \geqslant V_{dd}\sqrt{G_{opt}^2/\sigma^2 + B_L^2} \geqslant 0 \tag{2.53}$$

Hence R.H.S of the inequality is always satisfied due to passivity of the load, the interval for the imaginary part of the load admittance is determined as:

$$-\frac{G_{opt}}{\sigma}\sqrt{\sigma^2 - 1} \leqslant B_L \leqslant \frac{G_{opt}}{\sigma}\sqrt{\sigma^2 - 1} \tag{2.54}$$

(2.54) represents an open contour on Smith Chart that traces the constant $\frac{G_{opt}}{\sigma}$ circle spanning up to the susceptance limits. Constant conductance circles for the degraded power rating by σ reside on right-hand side of the optimum load, wherein real part or resistive part of the load impedance is greater than optimum load. These part of the contours are called as "voltage-clipping" contours due to the fact that increasing the imaginary part of the admittance will result in an admittance magnitude greater than G_{opt}/σ. As the magnitude of admitance increases by growing susceptance, the current drive level allowable for linear operation increases. Because amplitude of voltage swing is kept constant at maximum level V_{dd} to obtain maximum available power, current drive required to keep voltage at this maximum value changes accordingly.

In order to avoid confusion, the "clipping contour" idea is recapped at this point. Throughout the discussion above, the word "input drive" is often used. According to our VCCS model introduced in subsection 2.1, only forcing condition that is independent of the output state is drain current controlled by the gate voltage excursion created via the RF signal. Hence, "input drive" expression implies the controlled drain current. Drain current is controlled such that voltage or current clipping conditions are not violated. For the constant conductance traces, current is backed off up-to $I_1 = I_{max}/\sigma$ at $G_L = G_{opt}/\sigma$ to avoid voltage swing getting over V_{dd}.

Same procedure can be applied by dealing with the current related power equation in (2.49). This time R_L is set to R_{opt}/σ and I_1 is allowed to swing its maximum value and kept constant at $I_{max}/2$. Set of equations can be written as:

$$\begin{aligned} I_L Z_L &= V_L, \\ |V_L| &= V_1, \\ \Rightarrow V_1 &= I_1 |Z_L| \\ &= I_1 \sqrt{R_{opt}^2/\sigma^2 + X_L^2} \end{aligned} \tag{2.55}$$

We may open a different perspective to the discussion of constant power contours by looking into (2.55) from a different view. In the discussion of constant conductance circles which indicate the "voltage-clipping" boundaries, magnitude of addmittance limits are not emphasized but there is something special about the magnitude of admittance or impedance. Magnitude of load impedance Z_L is actually lower and upper bounded by R_{opt}/σ and R_{opt}, respectively on the circle of $R = R_{opt}/\sigma$. It can be mathematically shown as in (2.56).

$$\begin{aligned} max(|V_1|) = V_{dd}\ ;\ \ max(|I_1|) = I_{max}/2 \\ |Z_L| = V_1/I_1\ ;\ I_1 = I_{max}/2\ ,\ \ for\ \ P_{RF} = P_{opt}/\sigma \\ \Rightarrow max(|Z_L|) = max(V_1)/(I_{max}/2) = 2V_{dd}/I_{max} = R_{opt} \\ min(|Z_L| = |Ropt/\sigma + jX_L|) = R_{opt}/\sigma \\ \Rightarrow -\tfrac{R_{opt}}{\sigma}\sqrt{\sigma^2-1} \leqslant X_L \leqslant \tfrac{R_{opt}}{\sigma}\sqrt{\sigma^2-1} \end{aligned} \tag{2.56}$$

By the rigorous proof in (2.56), another open contour is obtained on Smith Chart. There are two finite lengt arcs on the Smith Chart, both of which correspond to same output power level P_{opt}/σ. It can be easily shown that the arcs form a closed contour by (2.57) or graphically on Smith Chart with impedance and admittance lines drawn in figure 2.14.

$$Z_L = R_{opt}/\sigma + j\frac{R_{opt}}{\sigma}\sqrt{\sigma^2-1} = \frac{1}{Y_L} = \frac{1}{G_{opt}/\sigma - j\,(G_{opt}/\sigma)\sqrt{\sigma^2-1}} \tag{2.57}$$

We can also graph the loadline curve which corresponds to I-V trace for different σ values respresenting power back-off ratio. In figure 2.15, loadline curves are drawn for the constant conductance part of the closed impedance contours. $\sigma = 1.25$ corresponds to 1 dB degradation of power output. We have some interesting comments on

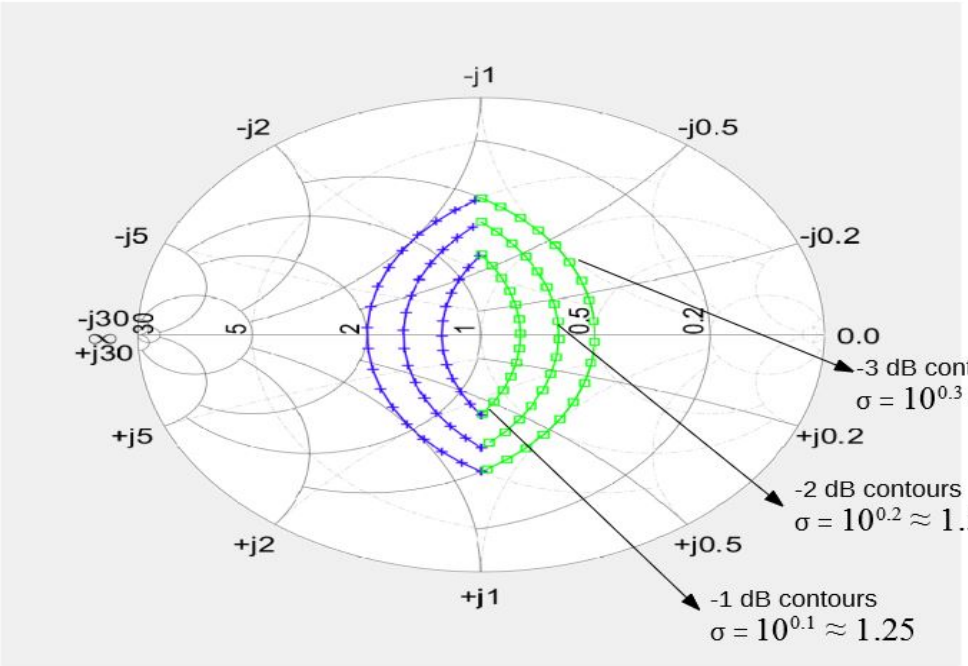


Figure 2.14: Constant power contours at 1-3 dB back-off. Smith Chart is normalized to R_{opt}.

I-V graph in 2.15. In section 2.1, we illustrated the loadline for the case of purely real and optimum loading conditions. However, as we can see in 2.15 I-V traces resemble elliptical shape in which its size enlarges as the imaginary part increases in magnitude. It should be noted that only resistive load draws a line on I-V plane though it is not the optimum resistive load. Moreover, all I-V curves intersect $V_d(\theta) = 1$ that is available maximum linear swing but don't reach the maximum current swing of $I_{max} = 1$. The conjugate loads also follow the same I-V trace as seen in 2.15. This can be easily deduced from equations (2.44)-(2.54). There is, however, one-pair of traces which perform full swings. These traces occur at the points where the magnitude of impedance equals R_{opt}.

In figure 2.16, the completing arc of the closed contour impedances are spanned for $\sigma = 1.25$. Again, we see the entirely resistive load results in a linear I-V curve. All I-V curves swing upto I_{max}, but the voltage swing is limited. This makes great sense as it is the counterpart of the constant conductance contour. In addition, one may easily notice that all the I-V curves, either ellipsoid or lines, are centered at the bias point (V_{dd}, $I_{max}/2$) as seen in figures 2.15 and 2.16.

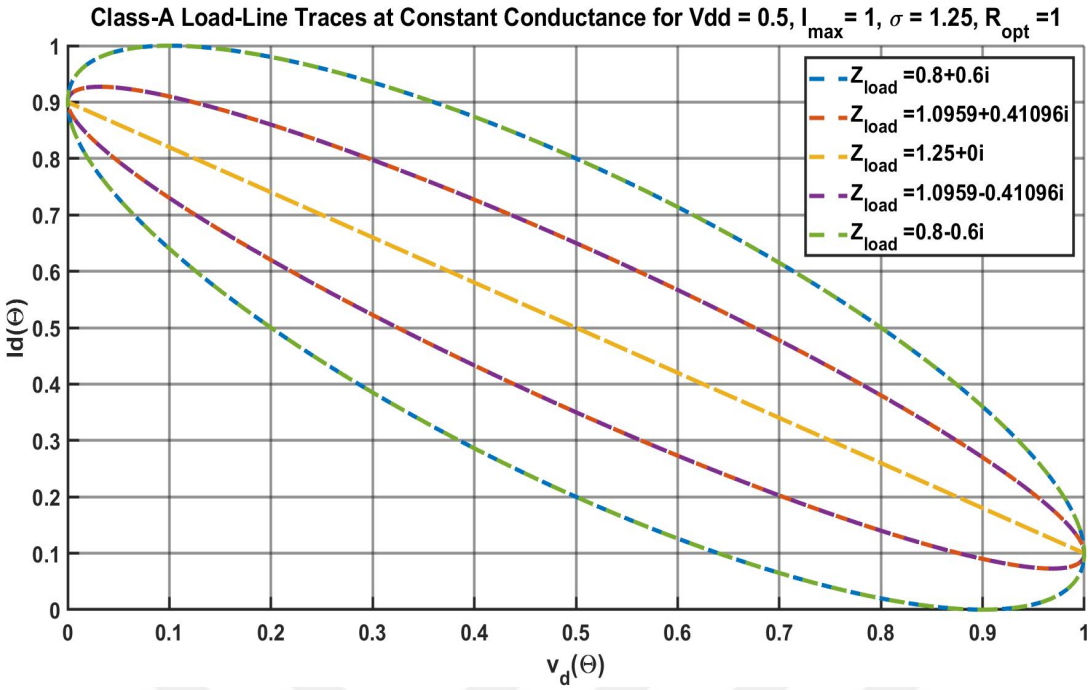


Figure 2.15: Sample loadlines on the P_{-1dB} impedance contour spanning thorugh constant conductance.

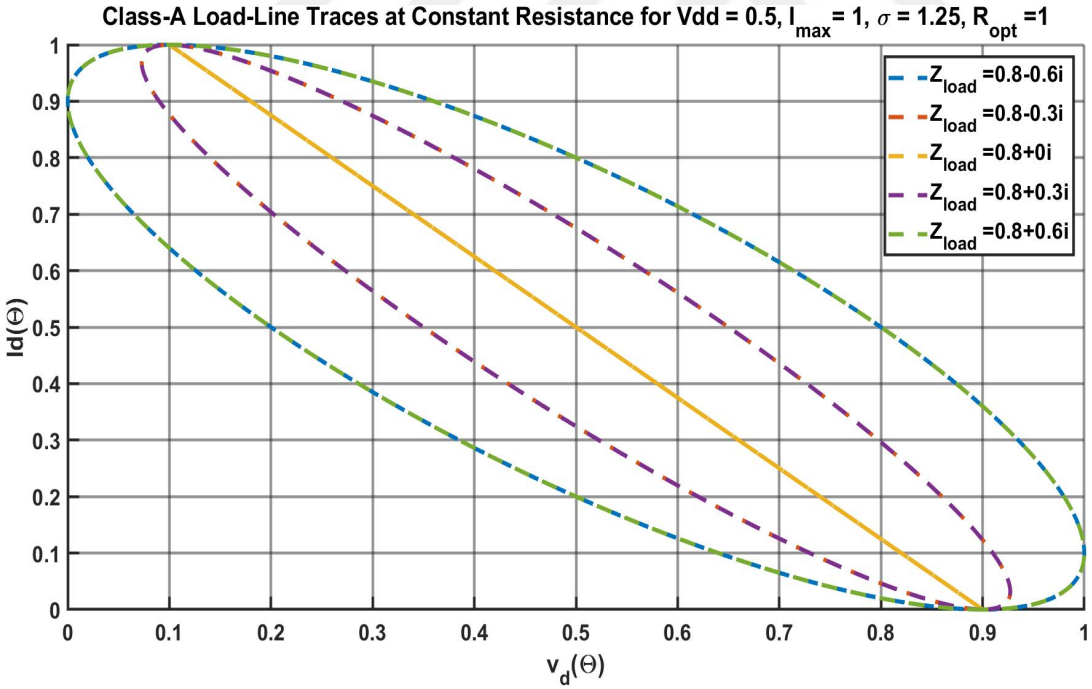


Figure 2.16: Sample loadlines on the P_{-1dB} impedance contour spanning through constant resistance.

In short, this subsection summarizes the basic load-line theory with our formulations. The complex loading conditions are addressed under Class-A bias using an idelized VCCS model of FET devices. It should be re-called that any device parasitics are excluded from the analysis. All analysis is made at hypothetical current generator plane. When the parasitics take effect, the impedance contours are expected to vary by frequency. The parasitic effects are taken into consideration in practical design discussion of this thesis. Complex loading conditions with harmonics included are discussed in next chapters.

CHAPTER 3

METHODOLOGY OF MODIFIED CLASS-J APPROACH

This section aims to explain our design approach using a modified class-J topology. First, classical J-mode theory is reviewed. Some of the existing class-J topology modifications studied in the literature are discussed. Investigating these methods, we establish the theoretical basis of our design approach. Iterative impedance equations at the intrinsic plane are presented. An extensive examination of parameters are provided with tables and figures.

3.1 Class-J Theory

In previous sections, we recognized the classical amplifier topologies and introduced our analysis approach. This section focuses on a special type of amplifier configuration which takes attention in last few years. The class-J design topology gets the major part of inspiration from the studies looking for compensation methods of device drain-source parasitic effects. Although there are many sources of parasitic, the dominant effect is modeled as drain-source capacitance C_{ds}. In [16], author introduces the "J-mode" operation which employs C_{ds} to modify the class-B "short" harmonics. Drain capacitance moves harmonic impedance to purely reactive loads at the generator plane, so the class-B loading condition is violated. It also assumes that the 3rd and higher harmonics may still result in the "short-circuit" impedance due to large capacitance values of devices. The second harmonic study reveals that the compensation is possible by allowing sufficient reactive impedance in addition to fundamental resistive load. In terms of output power and efficiency, the class-B values are achieved with a more flexible topology promising wider bandwidth than class-B [27]. Theo-

retical research of the phenomena pondering on the voltage waveform mathematical expressions leads to voltage waveform equation (3.1). Equation (3.1) is recognized by the Fourier series analysis assuming 3rd and higher harmonics are short-circuited [28]. Furthermore, this equation expresses a family of waveforms parametrized by α, resulting in same output power and efficiency of class-B written as in (3.2).

$$v_d^J(\theta) = (1 - cos(\theta))(1 - sin(\theta)) \tag{3.1}$$

$$v_d^\alpha(\theta) = (1 - cos(\theta))(1 - \alpha sin(\theta)) \tag{3.2}$$

(3.1) is re-written in (3.3) and clarifies that the 2^{nd} harmonic loading is purely reactive. Reactive loading result is inferred from our "even" function property of current waveform assumption stated in class-B discussion. Voltage waveform expression is normalized with respect to V_{dd} supply voltage. We may set $V_{dd} = 1$ and $I_{max} = 2$ for impedance calculations as it enforces $R_{opt,A} = 1$, which is easy to handle in calculations.

$$v_d^J(\theta) = 1 - cos(\theta) - sin(\theta) + \frac{1}{2}sin(2\theta) \tag{3.3}$$

Re-calling class-B current waveform, we find the fundemantal and second harmonic loads as,

$$z_1^J = \frac{V_{1,L}}{I_{1,L}} = \frac{-1+j}{-1} = 1 - j, \tag{3.4}$$

$$z_2^J = \frac{V_{2,L}}{I_{2,L}} = \frac{-\frac{1}{2}j}{\frac{-4}{3\pi}} = j\frac{3\pi}{8}. \tag{3.5}$$

Impedance values in de-normalized form is expressed as,

$$\begin{aligned} Z_1^J &= \tfrac{V_{1,L}}{I_{1,L}} = R_{opt,A} - jR_{opt,A}\ , \\ Z_2^J &= \tfrac{V_{2,L}}{I_{2,L}} = jR_{opt,A}\tfrac{3\pi}{8}. \end{aligned} \tag{3.6}$$

When the continum of modes are considered with α parameter, the optimum impedance set of the modes are given as,

$$\begin{aligned} Z_1^\alpha &= \tfrac{V_{1,L}}{I_{1,L}} = R_{opt,A}(1 - \alpha j)\ , \\ Z_2^\alpha &= \tfrac{V_{2,L}}{I_{2,L}} = j\alpha R_{opt,A}(\tfrac{3\pi}{8}). \end{aligned} \tag{3.7}$$

Essential result of equation set is the one-to-one correlation between harmonic and fundamental impedance. It is obvious that the all waveforms provide the same efficiency and output power. However, it is realized under condition of correct fundamental and harmonic terminations. Actually, "continium of modes" explain the harmony of impedances. Although a continuous change is desirable from the mathematical perspective, practically it is not an easy task to implement exact matching circuit. Optimum impedance set for various α values are drawn on the Smith Chart in figure 3.1. The inverse class-J mode, denoted as J^*, is capable of same efficiency and output power as of other voltage waveforms in the family. However, "J^*" implies an inductively reactive impedance, while "J" is capacitively reactive. Capacitively reactive impedance fits the idea of absorbing drain capacitance C_{ds} into load condition, well. This is why "class-J" is devoted to the loading condition with capacitive imaginary part.

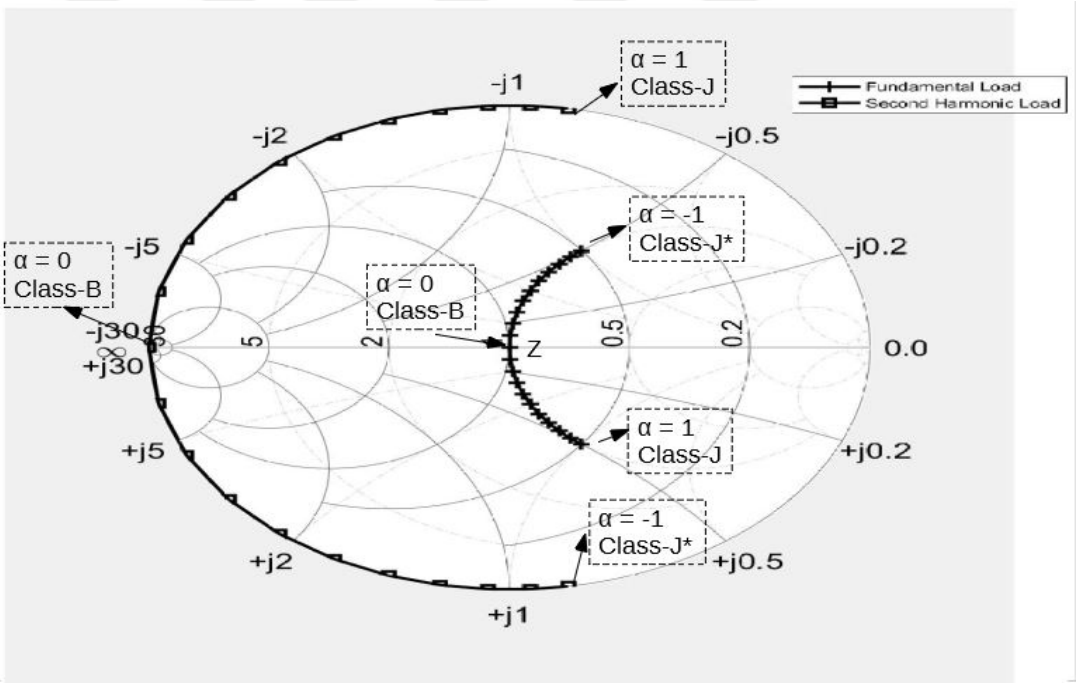


Figure 3.1: Fundamental and second harmonic impedance set for varying α values

Time domain voltage waveform for varying α values are plotted in figure 3.2. Class-J mode voltage and current waveforms are plotted on the same frame in figure 3.3. By figure 3.3, it can be inferred that intersection of the current and voltage waveform are more than the class-B case, hence we may expect lower efficiency at first glance.

However, efficiency keeps standing since dc component of voltage and current are unchanged while RF power output is protected, as well. Power consumption and RF power calculations are stated in (3.8) and (3.9).

As seen in (3.9), the fundamental voltage component magnitude is $\sqrt{2}$ times higher than class-B. Fundamental impedance magnitude is $\sqrt{2}$ times higher than it is in class-B case. This is the so-called waveform engineering part of the class-J approach, which makes the difference. The engineering of second harmonic impedance allows fundamental voltage component to rise upto $\sqrt{2}$ times V_{dd} supply voltage.

$$P_{dc} = V_{dc} I_{dc} = \frac{V_{dd} I_{max}}{\pi} \tag{3.8}$$

$$P_{RF} = \frac{1}{2} Re\left\{V_{1,L} I_{1,L}^{*}\right\} = \frac{1}{2} \frac{|V_{1,L}|^2}{|Z_1|^2} R_1 = \frac{1}{2} \frac{|-V_{dd} + jV_{dd}|^2}{|R_{opt,A} - jR_{opt,A}|^2} R_{opt,A} = \frac{1}{2} \frac{V_{dd}^2}{R_{opt,A}} \tag{3.9}$$

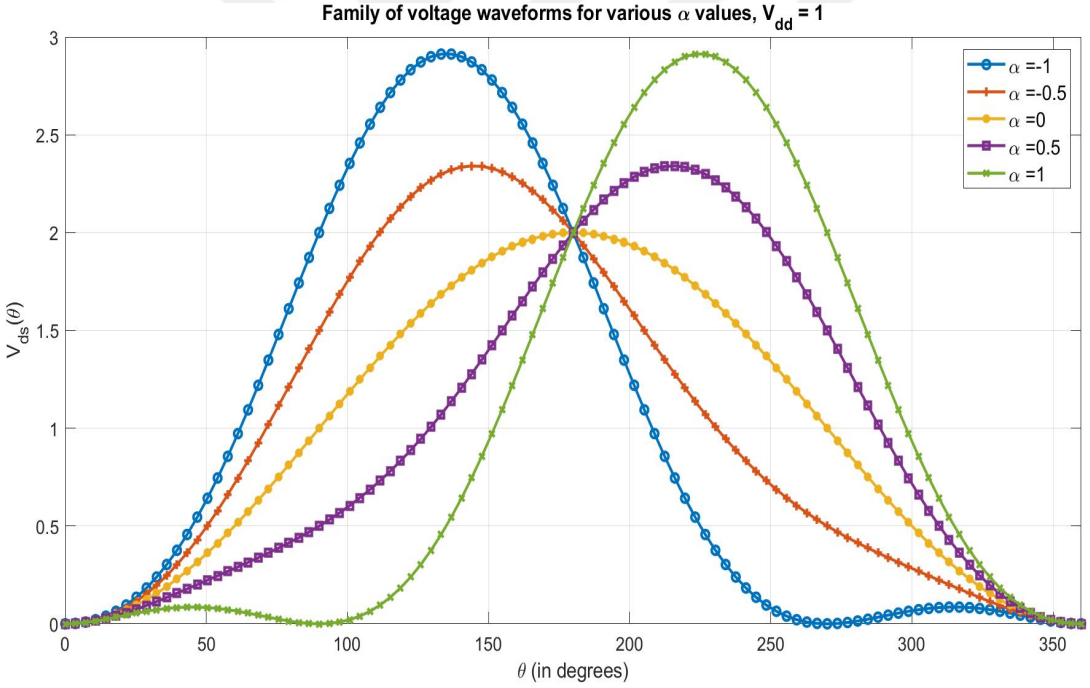


Figure 3.2: α family of voltage waveforms

Providing fundamental with extra swing without violating "zero-grazing" [29] condition costs higher peak voltage around $3V_{dd}$ at the drain of device. Peak drain voltage is a parameter that needs to be managed, carefully for safe operation of device. Current GaN devices available in the market, generally promise $3V_{dd}$ peak voltage endurance.

Discussion of potential harm due to high voltage peaks at the drain has been subject of interest in various research [4].Furthermore, under RF exposure, device characteristics are modified by dispersion mechanisms inherent to process technology. One of them is "electron trapping" phenomena which thematize the current collapse nearby the knee region of device. Study of [14] investigates the effect of "trapping" leading to "virtual gate formation", on the device performance for different RF loading and DC biasing conditions. It shows the knee-walkout phenomena occuring in different forms depending on varying RF stress conditions, such as high drain voltage.

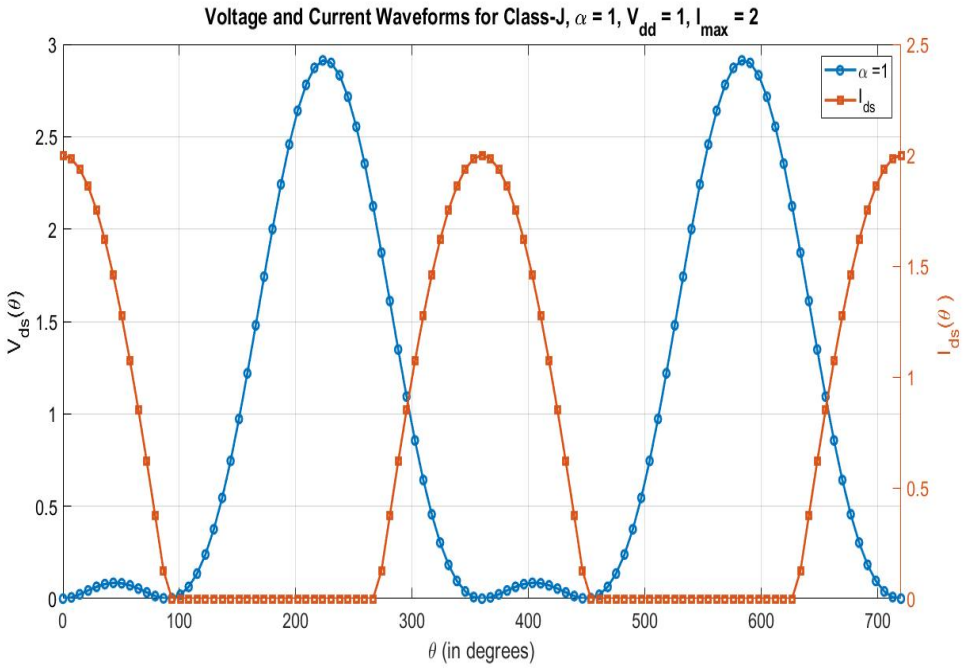


Figure 3.3: Class-J Voltage and Current Waveforms

Formulations given in this section will be referred often in our analysis of modified class-J approach. Table 3.1 summarizes the parameters for well-known operation modes[13]. Class C, F and F^{-1} are also provided in table. Detailed analysis can be found in literature[26].Though J-mode operation is capable of wider bandwidth than other known high efficiency classes, it is upper bounded to one-octave due to reactive second harmonic condition.

To sum up, class-J mode operation and continium of the impedance design space are elaborated. Mission of the second harmonic manipulation is outlined. Voltage

Table 3.1: Summary of important parameters for the well-known classes of operation

S.C. : short-circuit, O.C. : open-circuit, D.N.E : does not exist

Mode of Operation	Peak Efficiency (%)	CCA (Current Conduction Angle)	Z_1	Z_2	Z_3
A	50	$\alpha = 2\pi$	1	D.N.E.	D.N.E.
B	78.5	$\alpha = \pi$	1	S.C.	S.C.
A/B	50- 78.5	$\pi < \alpha < 2\pi$	0.93	S.C.	S.C.
C	78.5- 100	$\alpha < \pi$	≥ 1	S.C.	S.C.
F	90.7- 100	$\alpha = \pi$	1.15	S.C.	O.C.
F^{-1}	90.7- 100	$\alpha = 2\pi$	1.22	O.C	S.C.
J	78.5	$\alpha = \pi$	1- j	j 3π/8	S.C.

peaking effect which can be viewed as "side-effect" is discussed with reference to literature. Bandwidth and efficiency capabilities are explained.

3.2 Modified Class-J Theoretical Approaches

Typical class-J PA bandwidth is limited to one-octave besides its sensitivity to 2^{nd} harmonic reactive impedance. There is a research trend progressing to remove this sensitivity by eliminating the need for purely reactive loading. In [30], performance in case of deviation from reactive loading of 2^{nd} harmonic is evaluated. Study of [30] puts forward new design parameters. Parameters modify (3.2) to obtain equation(3.10). In their successive work [31], they show clipping contours for the non-optimal fundamental and second harmonic loading. The outstanding property of equation (3.10) is its ability to handle non-optimal conditions whereas (3.2) tells us only the single optimum situation. (3.10) utilizes the new parameters to have 3-degrees of freedom. Hence, fundamental phasor $V_{1,L}$ can take on a non-unity real value. Similarly, the 2^{nd} harmonic phasor $V_{2,L}$ may have a real value. Though authors reduce the complexity of calculations by suggesting simplifications, it still requires considerable effort to compute necessary contours. Assessing the waveform in the context of available bandwidth is quite tedious due to coefficients of voltage components including three

parameters.

$$v_d(\theta) = (1 - cos(\theta + \delta))(1 - \beta sin(\theta + \gamma))\,;\ -1 \leq \beta \leq 1 \tag{3.10}$$

More pragmatically, we seek intuitively parametrized waveforms. The mission of getting over one-octave bandwidth requires second harmonic impedance to be the fundamental impedance of the second-octave. Moreover, the second harmonic impedance of the second-octave becomes the fundamental impedance of the third-octave. The notation Z_m^k is defined to prevent confusion of terms. n represents the octave number and m is the harmonic number. For instance, Z_2^3 corresponds to 2^{nd} harmonic impedance of the third-octave. Mathematically, satisfying equation set (3.2) is necessary for our design approach.

$$\begin{aligned} Z_2^1 &= Z_1^2 \\ Z_2^2 &= Z_1^3 \end{aligned} \tag{3.11}$$

In [21], authors reshape voltage waveform by adding another multiplier which they call "resistive class-J term". Although it gives rise to a third harmonic term when expanded, useful results are achieved by simply neglecting this term. (3.12) is the proposed equation for resistive-reactive class-J approach [21].

$$v_d(\theta) = (1 - cos(\theta))(1 - \alpha sin(\theta))(1 + \beta cos(\theta)) \tag{3.12}$$

Expanding (3.12) and re-arranging the harmonic terms in the form of equation (2.4), we get the coefficients in (3.13). Coefficients may seem negated compared to original in [21], this is for convenience with sign convention of ours adopted in (2.4).

$$\begin{aligned} V_{dd} &= 1 - \beta/2 \\ V_{1,r} &= \beta - 1 & V_{1,q} &= \alpha(1 - \beta/4) \\ V_{2,r} &= -\beta/2 & V_{2,q} &= \tfrac{\alpha(\beta-1)}{2} \\ V_{3,r} &= 0 & V_{3,q} &= \tfrac{-\alpha\beta}{4} \end{aligned} \tag{3.13}$$

The normalized impedance set with $I_{max} = 2$ is calculated using the class-B current waveform as in (3.14 -15).

$$z_{1,L} = (1 - \beta) - j\alpha\left(1 - \frac{\beta}{4}\right) \tag{3.14}$$

$$z_{2,L} = \frac{3\pi}{8}(\beta - j\alpha(\beta - 1)) \tag{3.15}$$

Impedance and voltage equations can be normalized again by the dc component $1-\beta/2$ to have a unity value DC. Realizability of impedances and keeping the "zero-grazing" property constrains β to [0,1] interval. The α parameter only deals with the imaginary part of the impedances. Thereby α is not affected by impedance realizability issues. It has a full swing allocated in the interval [-1,1], as in the original class-J. Efficiency and output power are parametrically given by equations in (3.16-18). From (3.16-18), β determines the degradation level of output power and efficiency.

$$P_{dc} = \left(1 - \frac{\beta}{2}\right) V_{dd} \frac{I_{max}}{\pi} \tag{3.16}$$

$$P_{RF} = \frac{1}{4} (1 - \beta) V_{dd} I_{max} \tag{3.17}$$

$$\eta = \frac{\pi}{4} \left(\frac{1 - \beta}{1 - \frac{\beta}{2}}\right) \tag{3.18}$$

For the reason that class-J requires a purely reactive load at the second harmonic, it implies a sharp transition from the operating band impedance to second harmonics. Such a transformation leads to a sharp roll-off at the edge of the band and increases the difficulty of matching circuit design. Usually, in the design process or construction process, a considerable fraction of bandwidth around 30% becomes useless in terms of efficiency or output power[21]. An overlapping region between the fundamental and second harmonic impedance of the starting frequency should be available to avoid band-edge loss. With regard to formulation in (3.14-3.18), increasing β from its class-J value, which is "0", upto some value overlaps the fundemantal and second harmonic real parts by charging with decrease in peak efficiency and output power as shown in figures 3.4-5.

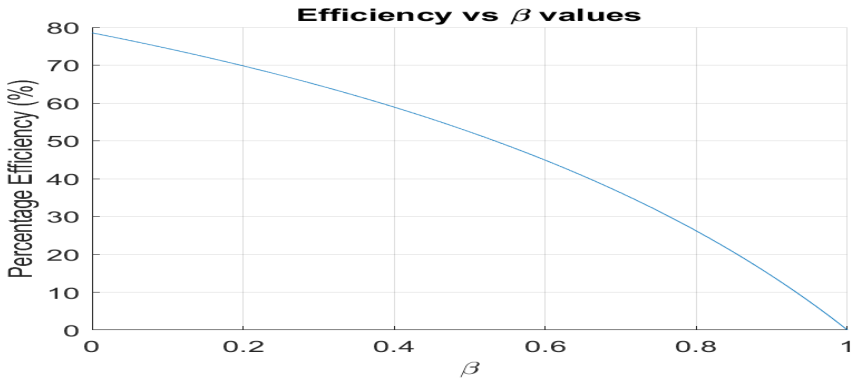


Figure 3.4: β vs efficiency

The degradation curve tells that efficiency is a decreasing function of β, and only a certain range is useful to support reasonable efficiency values. With sacrifice from power output and efficiency, the finishing edge of the band is rescued. The overlap region can be seen in figure 3.6. As β increases, second harmonic impedance space approaches fundamental until β = 0.46. At β = 0.46, fundamental and second harmonic load real parts are equated. Hence, the band edge frequency is matched to an impedance capable of providing remarkable RF output power and efficiency.

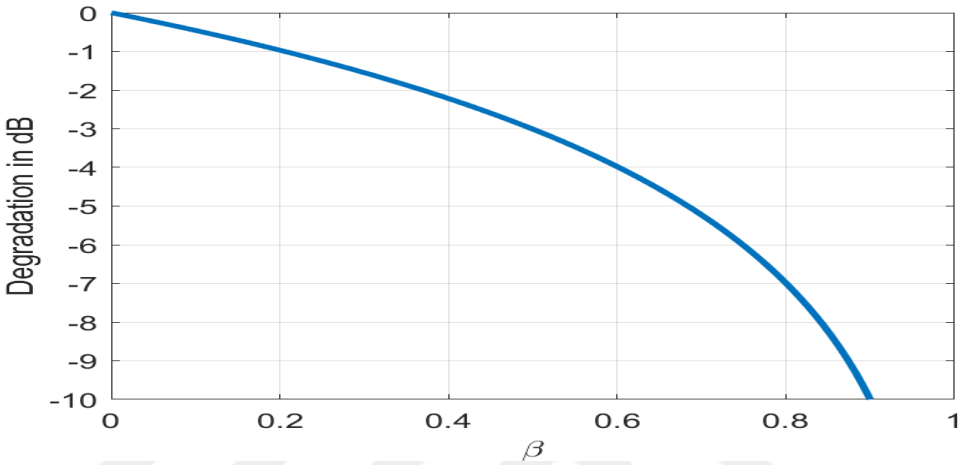


Figure 3.5: β vs power degradation curve.

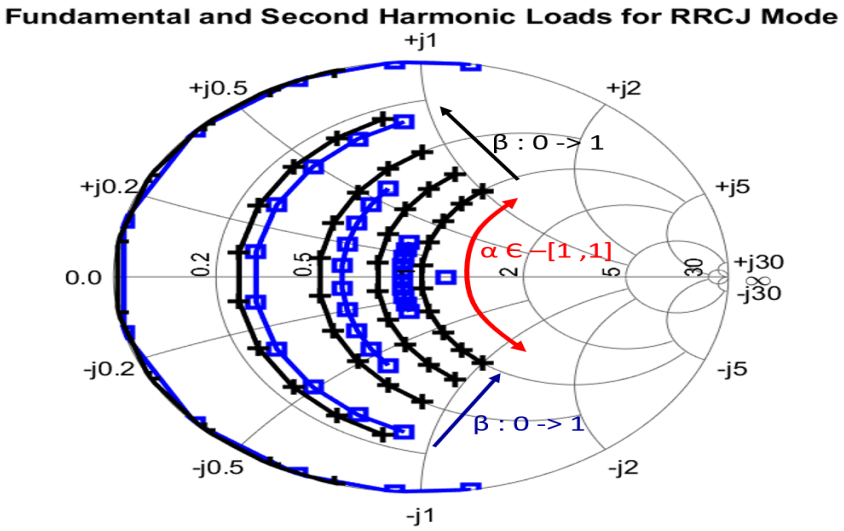


Figure 3.6: β and α swept for fundamental and harmonic impedances(black "+" : fundamental, blue "□" : second harmonic loads)

Since β = 0.46 causes around 2.5 dB power loss, it is plausible to keep β lower than 0.4 so that it supports efficiency greater than 60% and worst-case power degradation of around 2 dB. In this case, a one-octave bandwidth may not be acceptable thoroughly. Due to that operation at finishing frequency, meaning $2f_0$, promises -3.2 dB degraded power at best, the PA is not used at this edge frequency, most probably. However, a significant amount of band edge loss heals with the RRCJ approach.

The missing part in the RRCJ proposal is to leave the DC component unnormalized. That implies a consecutive change in the DC supply voltage as the load impedance changes by frequency and RRCJ parameters. It may be sustainable for a narrowband application because of limited impedance variation. In contrast, changing supply voltage is not feasible for broadband applications. We will emphasize this asset deeply within the upcoming discussion of our modifications.

Another bandwidth enhancement method proposed in [32] introduces a new parameter γ to the RRCJ approach and claims an "extended resistive continuous class B/J mode". ERCB/J mode voltage equation is given in (3.19). In (3.19), V_{dd} multiplier is omitted for simplicity.

$$v_d(\theta) = (1 - cos(\theta))(\gamma - \alpha sin(\theta))(1 + \beta cos(\theta)) \tag{3.19}$$

When it is expanded into terms, we obtain (3.20).

$$v_d(\theta) = \gamma\left(1 - \frac{\beta}{2}\right) + \gamma(\beta - 1)cos(\theta) - \alpha(1 - 0.25\beta)sin(\theta) - \gamma\frac{\beta}{2}cos(2\theta) - \frac{\alpha}{2}(\beta - 1)sin(2\theta) + \frac{\alpha\beta}{4}sin(3\theta) \tag{3.20}$$

Authors of [32] call γ as "boosting parameter". It governs the DC supply voltage and resistive parts of fundamental and second harmonic impedances, along with β. They allow $1 \leq \gamma \leq 1/(1 - \beta)$, $-1 \leq \alpha \leq 1$. The sweep of γ is upper bounded to $1/(1 - \beta)$ because greater values result in voltage peaking greater than $3V_{dd}$. On the other hand, the range of β is more of a design goal than a free choice in [0 1]. (3.21-23) express the peak RF output power, DC power consumption, and efficiency in parametrized form. Note that efficiency is governed solely by β. The power output

and consumed power are a function of both γ and β.

$$P_{dc,extended} = \gamma \left(1 - \frac{\beta}{2}\right) V_{dd} \frac{I_{max}}{\pi} \tag{3.21}$$

$$P_{RF,extended} = \frac{1}{4}\gamma \left(1 - \beta\right) V_{dd} I_{max} \tag{3.22}$$

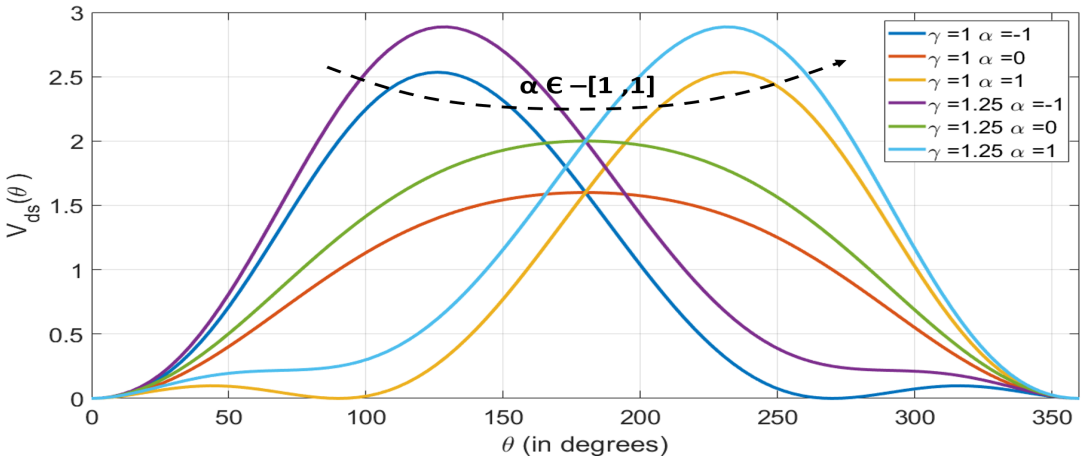
$$\eta_{extended} = \frac{\pi}{4} \left(\frac{1 - \beta}{1 - \frac{\beta}{2}}\right) \tag{3.23}$$

The efficiency curve results in exactly the same as the RRCJ approach depicted in figure 3.4. The major motivation of the extended mode approach is to boost RF output power while protecting the impedance space and efficiency. Thereby, a certain range of β is allowable to realize targeted efficiency values. In case of [32], authors aim to stay above 60% drain efficiency. This corresponds to [0, 0.38] interval for β parameter. As seen in (3.22), output power decreases as β increases for constant γ. The unavoidable fact is that the resistive part of the second harmonic vanishes as β decreases until zero. The smaller β means getting closer to conventional class-J impedance space. It can be deduced from the impedance equations given in (3.24-25), as well.

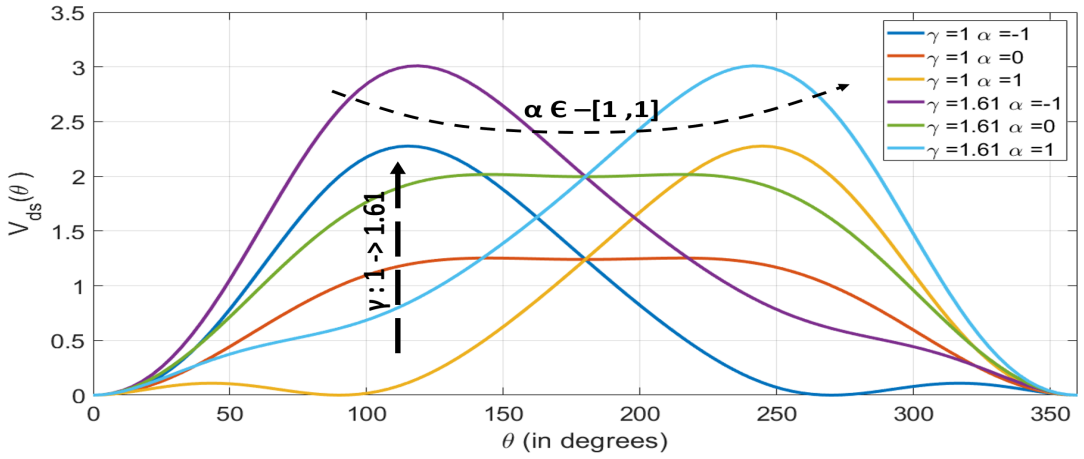
$$Z_{1,L} = R_{opt} \left(\gamma(1 - \beta) - j\alpha \left(1 - \frac{\beta}{4}\right)\right) \tag{3.24}$$

$$Z_{2,L} = \frac{3\pi}{8} R_{opt} \left(\gamma\beta + j\alpha \left(1 - \beta\right)\right) \tag{3.25}$$

Having the same efficiency governing equations implies a similar range of β for RRCJ and ERCB/J. β should be set as great as possible to enhance the bandwidth via increasing the resistive part of the second harmonic termination. Hence the overlapping region in the design space is achieved. However, the γ parameter is a modulator that enlarges the overlapping region of fundamental and second harmonic impedances. Indeed the root cause of resultant wide impedance space is modulation of the DC term of the voltage waveform. DC term is seen as a boundary condition set by the constant supply voltage of the PA, usually. The voltage waveforms for some values of β and γ are depicted in figure 3.7.



(a) $\beta = 0.2$.



(b) $\beta = 0.38$.

Figure 3.7: Family of voltage curves for ERCB/J modes

(3.7) shows that for constant γ and β, the curves drawn for negated α values show even symmetry around $\theta = 180^0$. In addition, increasing γ and β causes higher peaking. Figure (3.7b) includes waveforms for limiting values of $\gamma = 1.61$ and $\beta = 0.38$. In the limiting case, the voltage maxima is $3V_{dd}$ since waveforms are drawn by omitting V_{dd} multiplier or equivalently setting to 1. To make use of the overlapping impedance space, iterative parametric equations in (3.26-27) should be satisfied.

$$\beta_{n+1} = 4 + (1 - \beta_n)\frac{3\pi}{2}\frac{\alpha_n}{\alpha_{n+1}} \tag{3.26}$$

$$\gamma_{n+1} = \frac{3\pi}{8}\frac{\beta_n \gamma_n}{1 - \beta_{n+1}} \tag{3.27}$$

Equations in (3.26) and (3.27) are obtained by equating the real and imaginary parts of (3.24-25) for lower and upper octaves, where n indicates the octave number. These impedance equations are required in each octave to fulfill the zero-grazing property and keep output power and efficiency above the targeted level. In [32], authors tabulate the possible parameter intervals for the common impedance space. They validate the approach by constructing a prototype with a bandwidth of approximately 3-octave. Besides, there are still issues with the theory such as modulated DC supply voltage and neglected third harmonic impedance condition. In the next subsection, we address these issues by proposing some modifications to the voltage equation.

3.3 Proposed Modified Class-J Approach

In this section, we propose a modified class-J approach that enables broadband design strategies aiming at more than an octave bandwidth. The previous section discussed the existing theoretical propositions. For both RRCJ and ERRCB/J modes, there are two main concerns to be handled. One of them is the open-circuited 3rd harmonic impedance which causes ambiguity in designs operating around or more than 2-octaves bandwidth. The latter and fundamental problem is the unnormalized DC component, which causes voltage waveform to contradict the strict physical boundary condition imposed by DC supply rail in real applications.

We deal with the fundamental concern of the non-unity DC component of the voltage waveform. The reason we are putting forward the non-unity DC component as a major issue is its impracticality. Modulating the supply voltage as the frequency of operation changes over a wide bandwidth is a barrier in front of the system design. In particular, for frequency hopping broadband systems, it is not achievable. The similar propositions for extended modes of class-F and inverse class-F are widely discussed in [33], [34], as well. In [33, 34], voltage waveforms are employed as DC normalized, and corresponding impedance spaces are expressed, accordingly.

The derivation process starts with normalizing the equation in (3.20) by $\gamma\,(1-\beta/2)$.

Then we obtain (3.28).

$$v_{d,n}(\theta) = 1 - \frac{1-\beta}{1-\beta/2}cos(\theta) - \frac{\alpha(1-0.25\beta)}{\gamma(1-\beta/2)}sin(\theta) - \frac{\beta}{2(1-\beta/2)}cos(2\theta) - \frac{\alpha}{2\gamma(1-\beta/2)}(\beta-1)sin(2\theta) + \frac{\alpha\beta}{4\gamma(1-\beta/2)}sin(3\theta) \quad (3.28)$$

The de-normalized equation can be written in factorized form as follows.

$$v_d(\theta) = \frac{V_{dd}}{1-\beta/2}(1-cos(\theta))\left(1-\frac{\alpha}{\gamma}sin(\theta)\right)(1+\beta cos(\theta)) \quad (3.29)$$

We can reduce the number of parameters by the interchange $\frac{\alpha}{\gamma} = k$. The final form is obtained as,

$$v_d(\theta) = \frac{V_{dd}}{1-\beta/2}(1-cos(\theta))(1-k\,sin(\theta))(1+\beta cos(\theta)). \quad (3.30)$$

To protect zero-grazing property, k is limited to range [-1,1]. Note that it is similar equation of RRCJ mode of [21], except the normalizing factor $1-\beta/2$. The impedance equations are written in (3.31) by assuming class-B current waveform. We neglect the third harmonic term and impedance, which results in open-circuit, as in RRCJ and ERRCB/J modes.

$$Z_{1,L} = 2\frac{V_{dd}}{I_{max}}\left(\frac{1-\beta}{1-\beta/2} - jk\frac{1-0.25\beta}{1-\beta/2}\right) = R_{opt,A}\left(\frac{1-\beta}{1-\beta/2} - jk\frac{1-0.25\beta}{1-\beta/2}\right)$$
$$Z_{2,L} = 2\frac{V_{dd}}{I_{max}}\frac{3\pi}{8}\left(\frac{\beta}{1-\beta/2} - jk\frac{\beta-1}{1-\beta/2}\right) = R_{opt,A}\frac{3\pi}{8}\left(\frac{\beta}{1-\beta/2} - jk\frac{\beta-1}{1-\beta/2}\right) \quad (3.31)$$

(3.31) is re-written with our notation, n denoting the octave number.

$$Z_1^n = R_{opt,A}\left(\frac{1-\beta_n}{1-\beta_n/2} - jk_n\frac{1-0.25\beta_n}{1-\beta_n/2}\right) \quad (3.32)$$

$$Z_2^n = R_{opt,A}\frac{3\pi}{8}\left(\frac{\beta_n}{1-\beta_n/2} - jk_n\frac{\beta_n-1}{1-\beta_n/2}\right) \quad (3.33)$$

From the impedance equations, β range is limited to [0,1] to enforce passivity by keeping the real parts greater than zero. The output power and efficiency relations are given in (3.34-3.36).

$$P_{dc} = \frac{V_{dd}I_{max}}{\pi} \quad (3.34)$$

$$P_{RF} = \frac{1}{4}V_{dd}I_{max}\left(\frac{1-\beta}{1-\beta/2}\right) \quad (3.35)$$

$$\eta = \frac{\pi}{4}\left(\frac{1-\beta}{1-\frac{\beta}{2}}\right) \quad (3.36)$$

Obviously, from the equations in (3.34-3.36), β is the only parameter left to manage efficiency and power output. In terms of degradation characteristics from the class-B output power and efficiency, power output and efficiency are governed by the same decreasing function of β. Figure 3.8 shows the efficiency and power derating function with respect to class-B mode.

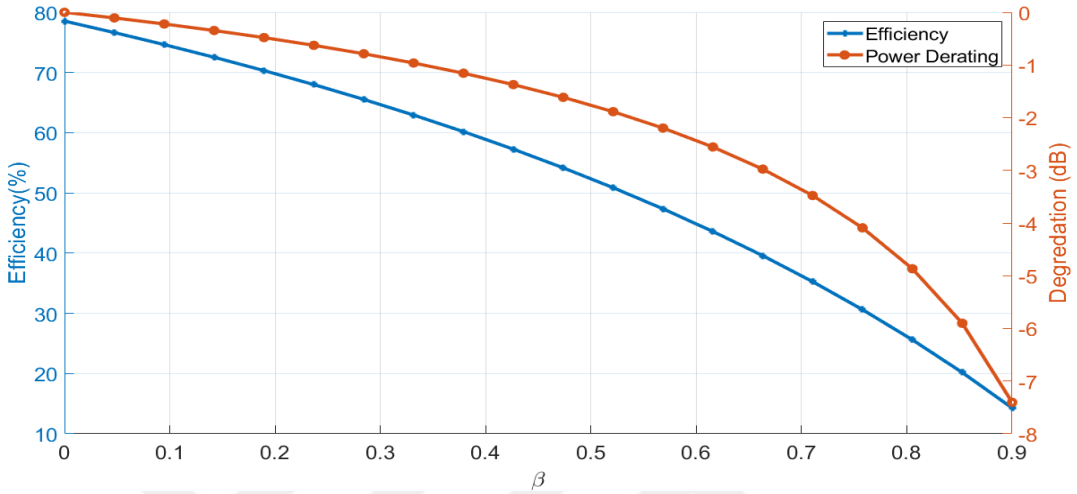


Figure 3.8: Efficiency and power derating dependence on β

RRCJ mode power derating curve and our modified approach are depicted in figure 3.9. Our approach may be called as normalized resistive-reactive class-J approach, which may be abbreviated as NRRCJ. 3.9 shows that NRRCJ promises an enhanced performance by offering less derating than RRCJ.

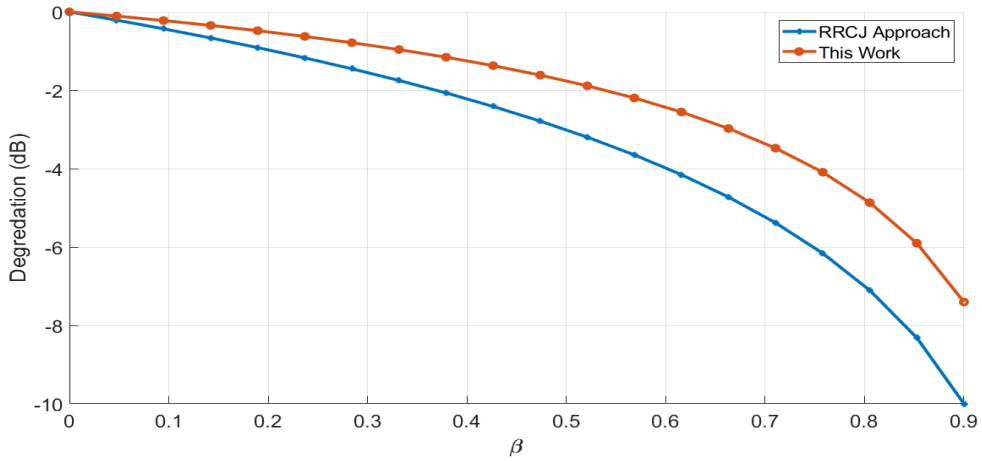


Figure 3.9: Power derating curve comparison with RRCJ and our NRRCJ approach

The voltage family of waveforms are plotted in figure 3.10 for various values of β and $k = -1$. Again, they show even symmetry around $\theta = 180^0$. The k and β values control magnitude and phase of amplitude maximum. The figure is simplified to observe the peaking effect. Finding an analytic upper bound to limit peaking at $3V_{dd}$ for the parameters is cumbersome because it is a three-variable extreme value problem. However, as the waveform is numerically studied it is revealed that the highest-peaking occurs for maximum absolute values of β and k.

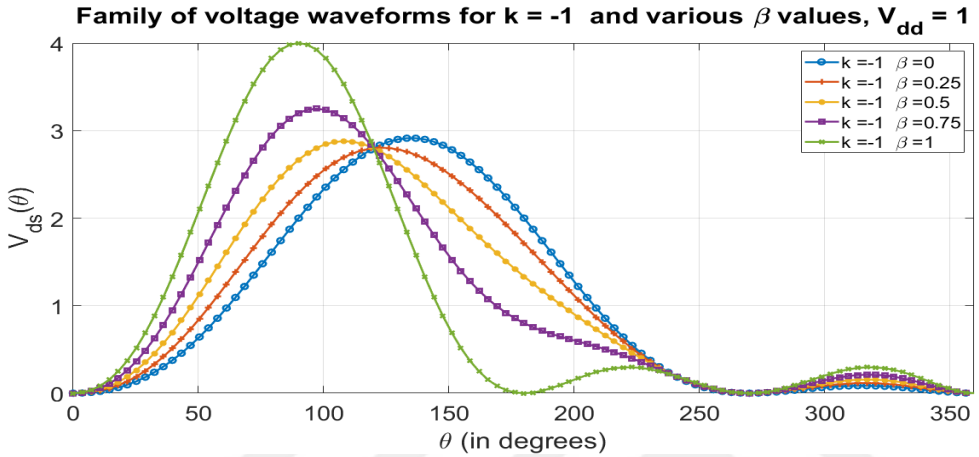


Figure 3.10: Family of voltage waveforms for $k = -1$ and β swept over [0,1].($V_{dd} = 1$)

Figure 3.10 shows that $4V_{dd}$ peak value is reached at $\beta = 1$. On the other hand, the full range of β is not useful since values greater than 0.5 result in severely degraded power output and efficiency as seen from figures 3.8 and 3.9. Another plot is depicted in figure 3.11, which shows voltage waveforms for $\beta \in [0, 6]$. In this subset of β, maximum peaking is $3V_{dd}$. This property serves well for the safe operating conditions.

Having the mathematical properties of the NRRCJ approach investigated, the design equations determining the impedance space can be derived starting from (3.32) and (3.33) as follows.

$$Z_1^{n+1} = Z_2^n \tag{3.37}$$

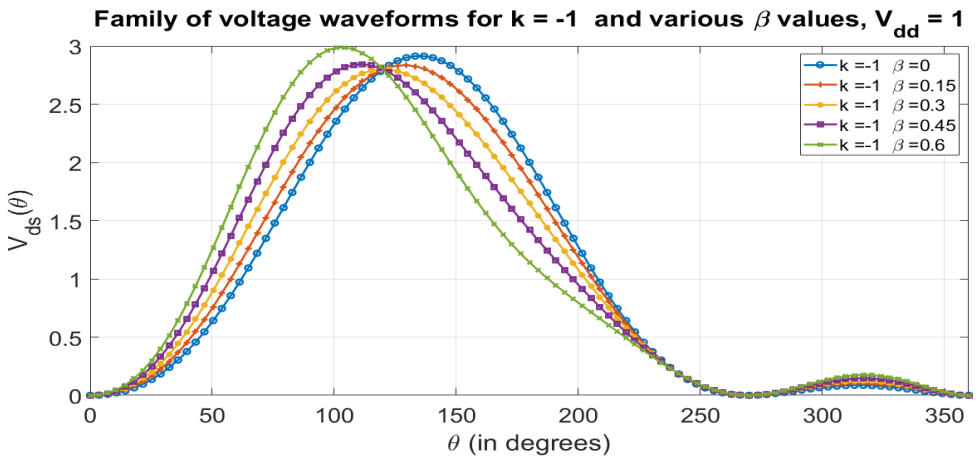


Figure 3.11: Family of voltage waveforms for $k = -1$ and β swept over [0,6].($V_{dd} = 1$)

Equating the real parts by substituting the impedance expressions given in (3.32) and (3.33) into (3.37), we obtain (3.38). To have better-looking equations, the constant $\psi = \frac{3\pi}{8}$ is assigned.

$$\psi \frac{\beta_n}{1 - \beta_n/2} = \frac{1 - \beta_{n+1}}{1 - \beta_{n+1}/2} \tag{3.38}$$

Re-arranging the terms we get the simple iterative relation in (3.39) between β parameters with successive octave numbers.

$$\beta_{n+1} = \frac{(2\psi + 1)\beta_n - 2}{(\psi + 1)\beta_n - 2} \tag{3.39}$$

Repeating the similar steps for the imaginary part, we reach a relatively complicated equation in (3.40).

$$k_{n+1} \frac{1 - 0.25\beta_{n+1}}{1 - 0.5\beta_{n+1}} = k_n \frac{1 - \beta_n}{1 - 0.5\beta_n} \tag{3.40}$$

Since we know the relation between β_{n+1} and β_n, we can simplify this equation to (3.41).

$$k_{n+1} = k_n \frac{\psi\,(1 - \beta_n)}{(0.5\psi + 0.75)\beta_n - 1.5} \tag{3.41}$$

The impedance points of the first and second harmonics for varying k and β values are given in figure 3.12. The second harmonic impedance real part increases beyond the fundamental load after the overlapping region at $\beta = 0.46$. Moreover, the real part of second harmonic impedance exceeds $R_{opt,A}$ for $\beta > 0.6$. Because the second harmonic of the previous octave is fundamental for the next one, it is useful to re-plot the power and efficiency curves of figure 3.8. Figure 3.13 demonstrates the power and

efficiency reduction curves for successive octave fundamental loads i.e. Z_1^n , Z_1^{n+1}. The curves in 3.13 are drawn for $\beta_n \in [0.4, 0.6]$ because it is the interval promising both reasonable efficiency and power output.

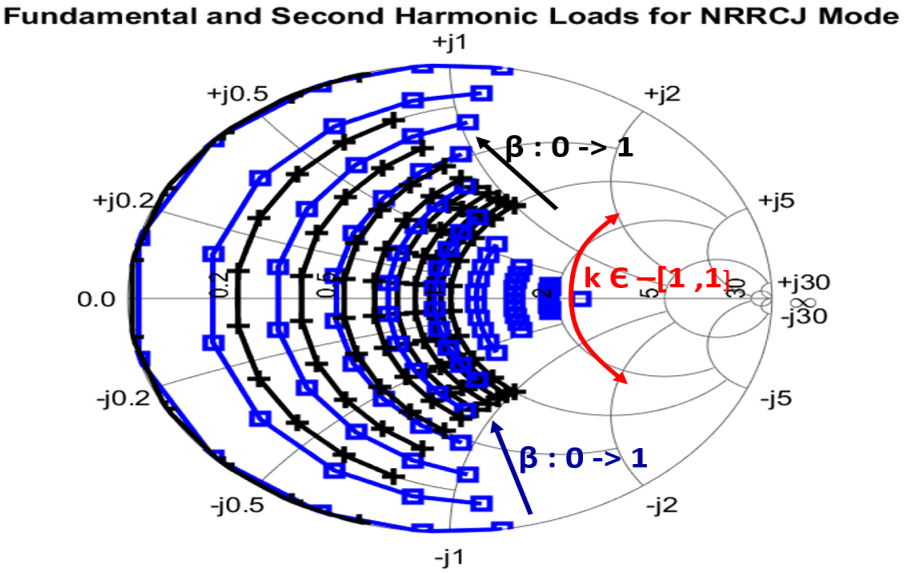


Figure 3.12: β and k swept for fundamental and harmonic impedances(black "+" : fundamental, blue "□" : second harmonic loads

In particular, we see the curves of efficiency and output power intersected around $\beta = 0.46$ in figure 3.13. In addition, whreas efficiency and power output of the same octave behave similiarly, curves of the different octave show opposite behaviour. Hence, multioctave designs require optimization of these curves by proper selection of β. Choice of the parameter k is less restricted because it doesn't have direct effect on power and efficiency.

In order to have a detailed look into impedance space, figure 3.14 is re-generated for $\beta \in [0.4, 0.6]$. Note that fundamental of the first octave has lower resistive part than fundamental of the second octave. This may cause a difficulty in matching circuit design since it may not be possible to construct a foster network following such a trajectory with increasing frequency. In chapter 4, such cases are investigated with practical considerations.

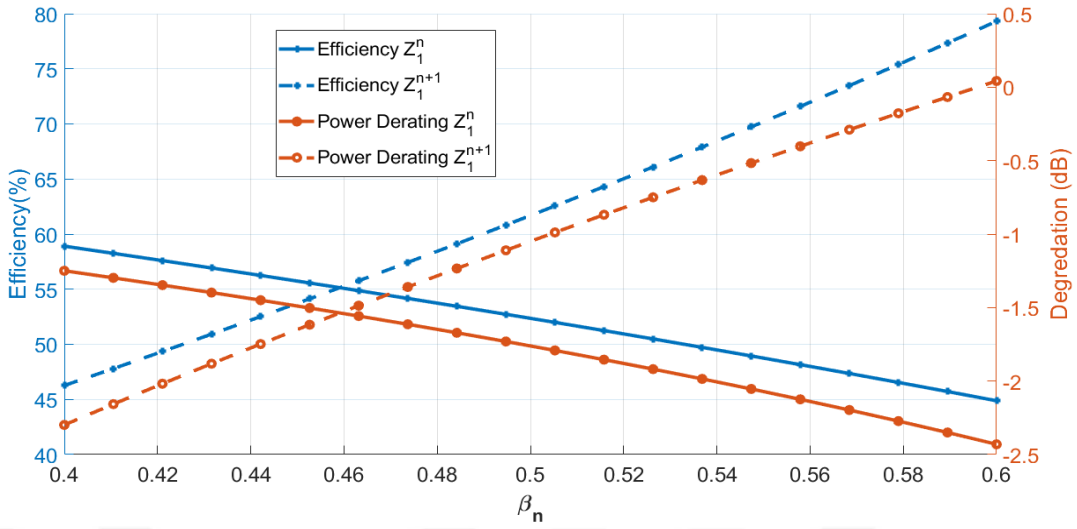


Figure 3.13: Reduction in power and efficiency for fundamental impedance of successive octaves of NRRCJ mode.

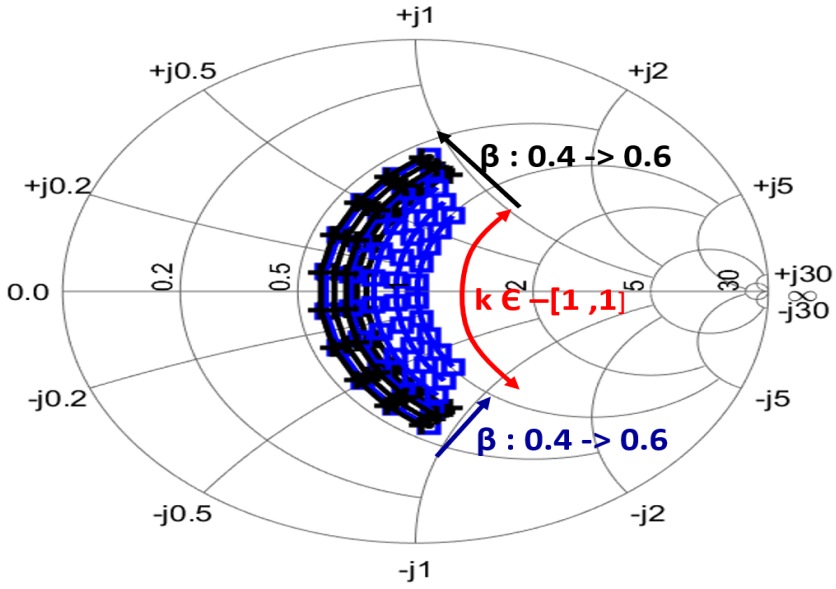


Figure 3.14: $\beta \in [0.4, 0.6]$ and k swept for fundamental and harmonic impedances(black "+" : fundamental, blue "□" : second harmonic loads

In short, this section presented the "normalized resistive-reactive class-J ", NRRCJ, approach theoretical basis. Iterative impedance equations are introduced. Integration of the equations into the design process are explained in the next chapter. The basic theoretical properties of the NRRCJ can be summarized as follows.

- It is practical to in terms of scalability for any V_{dd} voltage and constant drain voltage, in contrary to RRCJ and ERRCJ/B.
- It offers more advantageous power de-rating curve than RRCJ.
- Iterative parameters of impedance equations are simpler than RRCJ and ERRCJ/B.
- Naturally resistant to high-peaking by choice of β.
- Power and efficiency are governed solely by β as a result of normalized form.

CHAPTER 4

PRACTICAL IMPELEMENTATION OF NRRCJ APPROACH

This chapter describes the utilization of the NRRCJ approach in the design process of broadband power amplifiers. First, iterative equations introduced in chapter 3 are re-visited from a practical perspective. The targeted impedance set at the current generator plane is presented. For multi-octave design practice, useful ranges of β and k are investigated. The design of the two prototypes, which are operating at 400-3200 MHz, is explained in detail. Results are compared with the theoretical expectations.

4.1 Design Scheme for Broadband PA Design

In Chapter 3, the iterative equations for β_n and k_n parameters are introduced, n indicating the octave number. Our design strategy can be called design-by-octaves. The nature of NRRCJ and other modified topologies require discretization of the voltage waveform parameters in each sub-band. For the design strategy of ours, it is clear from equations (3.39) and (3.41) that β is the major parameter. Throughout this chapter, we will use f_0 to represent starting frequency of the operation band.

To begin with, we can analyze β for a full-octave design goal, meaning that the operation band is f_0 to $2f_0$. For $f \in (f_0, 2f_0)$, we can select β_n in $[0, 0.6]$, which offers 2.3 dB degraded output power and 45% drain efficiency at worst with regard to figure 3.8. The cost of small β_n is the high-Q second harmonics that increase the difficulty of circuit design. Since an octave bandwidth is aimed, β_2 is considered only for $f = 2f_0$. Hence, it is reasonable to prohibit β_2 being greater than 0.6. As any β_2 at $2f_0$ implies a β_1 at f_0, β_1 is also bounded respectively. The inverse of equation (3.39) is stated in

(4.1) to simplify backward analysis.

$$\beta_n = \frac{2\left(\beta_{n+1} - 1\right)}{(\psi + 1)\beta_{n+1} - (2\psi + 1)} \tag{4.1}$$

Moreover, we can define the function $\beta_n(f)$ as follows.

$$\beta_n\left(f\right) = \{\beta \in [0, 1] \ \mid f \in [nf_0,\ 2nf_0)\} \tag{4.2}$$

By the definition in (4.2), frequency is involved in the calculations. Though it is not preferable to use the full range set $[0, 1]$, (4.2) is expressed as a general definiton. Considering to capture the operation bandwidth $[f_0, 2f_0]$, we need to analyze $\beta_1(f)$ and $\beta_2(f)$. In that respect, $\beta_1(f)$ is undefined at $2f_0$ and $\beta_2(f)$ matters only at $2f_0$. Mathematically speaking, $\beta_1(f) \in [0, 0.6]$ for $f \in (f_0, 2f_0)$ and $\beta_1(f_0)$, $\beta_2(2f_0)$ cases are treated specially. Conditions at $f = f_0$ and $f = 2f_0$ can be summarized as follows.

$$0 \leq \beta_2(2f_0) \leq 0.6 \tag{4.3}$$

$$0 \leq \beta_1(f_0) \leq 0.6 \tag{4.4}$$

Equation (4.3) can be solved for $\beta_1(f_0)$ by substituting (3.39). We obtain the interval for the boundary condition $\beta_1(f_0)$ as

$$0.3904 \leq \beta_1(f_0) \leq 0.5959. \tag{4.5}$$

We treat f_0 and $2f_0$ as boundary conditions because the generalized $\beta(f)$ function, which is defined as in (4.6), should be continuous. Any value of $\beta(f)$ maps to a physically realizable impedance and abrupt impedance changes are not realizable at transition points such as $f = 2f_0$.

$$\beta(f) = \begin{cases} \beta_1(f) & ; f \in [f_0, 2f_0) \\ \beta_2(f) & ; f \in [2f_0, 4f_0) \\ \ldots & \\ \beta_n(f) & ; f \in [2^{n-1}f_0, 2^n f_0) \end{cases} \tag{4.6}$$

In this way, a major part of the impedance trajectory information can be extracted from $\beta(f)$. In addition, there may exist multiple functions to satisfy boundary conditions. However, the trajectories drawn by those functions should be realizable with

foster impedance matching networks [35]. Despite finding or proposing an exact analytic equation is tedious, we show that satisfying the impedance space requirements is achieveable to a great extent in the design process section.

A similar analysis could be carried out for the parameter k_n. Since k_{n+1} is depedent both k_n and β_n, the complete analytic analysis may prevail the explanation of functionality. Thus, we simplify the analysis by paying attention to seperable property of (3.41), where we can pretend $k_{n+1}(f = 2\widehat{f}) = k_n(f = \widehat{f})E(\beta_n(f = \widehat{f}))$. $E(\beta_n)$ is simply defined as in (4.7).

$$E(\beta_n) = \frac{\psi\,(1-\beta_n)}{(0.5\psi + 0.75)\beta_n - 1.5} \tag{4.7}$$

It is easy to show that (4.7) is negative for the full range, $[0, 1]$ of any β_n. Negativity of $E(\beta_n)$ implies that k_n and k_{n+1} takes on opposite signs similar to original class-J. By this property, we can re-arrange the seperated form into (4.8) to emphasize the opposite signs of parameters.

$$k_{n+1}(f = 2\widehat{f}) = -k_n(f = \widehat{f})\left|E(\beta_n(f = \widehat{f}))\right| \tag{4.8}$$

$|E(\beta_n)|$ is a positive function for $\beta \in [0, 1]$. It can also be shown by the derivative tests or numerical calculations that the envelope function $|E(\beta_n)|$ is a monotonically decreasing function of β_n. Local maximum and minimum points of $|E(\beta_n)|$ are located at $\beta_n = 0$ and $\beta_n = 1$ which are 0.7854 and 0, respectively. This feature validates the theoretical and practical usefulness of the k_n parametric iterative equations, as well. Any k_n should not exceed the interval $[-1, 1]$. That is required both for zero-grazing property and continuity. Furthermore, we can easily state that magnitude of k_n decreases as n increases which refers to higher octaves, thereby larger bandwidth designs. This is a quite intuitive result which points out that the span of available impedance space gradually decreases. So, the matching circuit design becomes difficult. $|E(\beta_n)|$ is demonstrated for $\beta_n \in [0, 1]$ in figure 4.1. The $k(f)$

function is defined in a similar way to $\beta(f)$ in (4.9).

$$k(f) = \begin{cases} k_1(f) & ; f \in [f_0, 2f_0) \\ -k_1(f/2)\,|E(\beta_1(f/2))| & ; f \in [2f_0, 4f_0) \\ -k_2(f/2)\,|E(\beta_2(f/2))| & ; f \in [4f_0, 8f_0) \\ \dots & \\ -k_n(f/2)\,|E(\beta_n(f/2))| & ; f \in [2^{n-1}f_0, 2^n f_0) \end{cases} \tag{4.9}$$

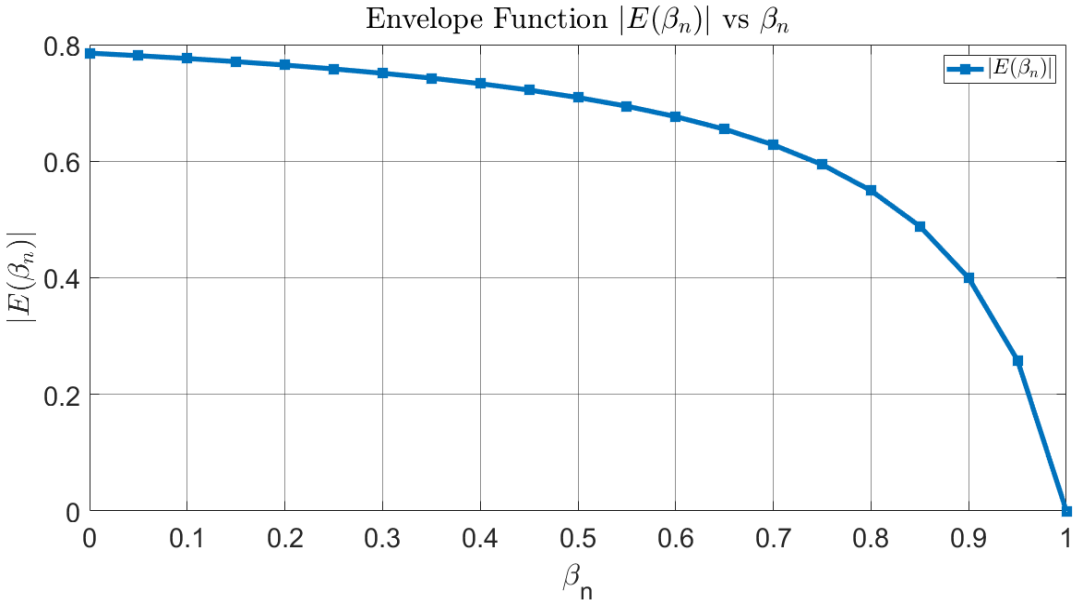


Figure 4.1: $|E(\beta_n)|$ vs β_n

We can turn our attention again to the design of a single octave parametric design. The design procedure starts with the proper selection of boundary conditions for β values. First, it is reasonable to set $0 \leq \beta_2(2f_0) \leq \frac{2}{2\psi+1} = 0.5959$ which results in minimum efficiency of 45%. Though one may use a smaller margin to target higher efficiency, we are covering the largest available set to show the concept. Indeed, the upper bound 0.5959 is not a random number. It is deduced such that β_n should lie in $[0, 0.5959]$, for $0 \leq \beta_{n+1} \leq 1$. In the reverse case, meaning that for $0 \leq \beta_{n+1} \leq 0.5959$, $\beta_n \in [0.3927, 0.5959]$ should be satisfied. We may obtain a continuous $\beta(f)$ for $f \in [f_0, 4f_0]$ function having these properties as in figure 4.2. In the figure, different boundary conditions at $2f_0$ are set in $[0, 0.5959]$ and for the piece of the function

representing $\beta_2(f)$, linear interpolation is used. One may define any other function in those intervals as long as it satisfies the boundary conditions.

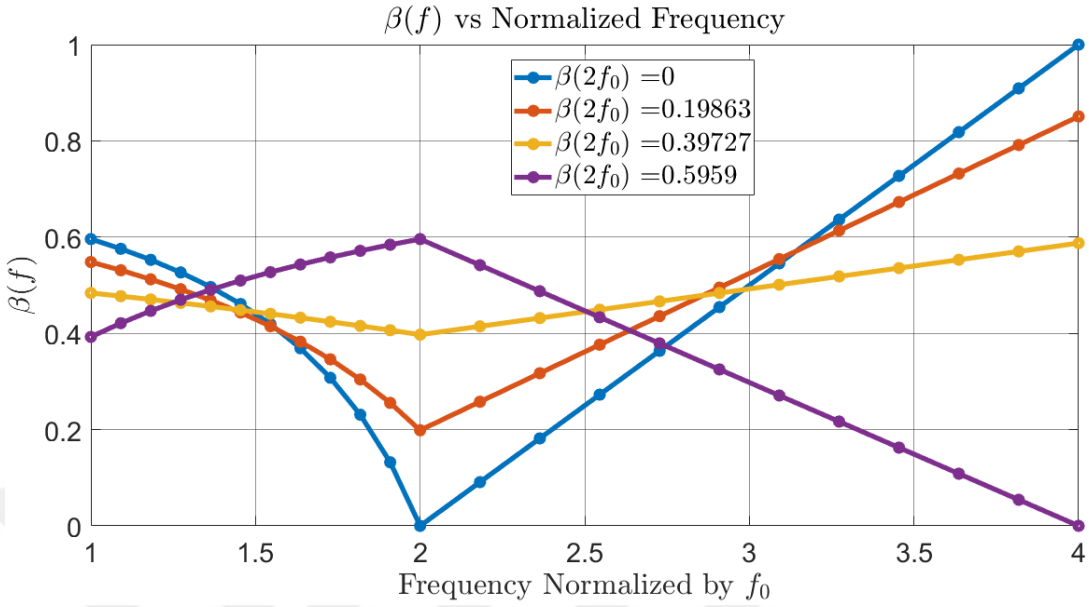


Figure 4.2: $\beta(f)$ for different boundary conditions set at $\beta(2f_0)$

For the $k(f)$, the similar procedure can be followed. Since the envelope function $|E(\beta(f))|$ is continuos, it helps to define a continuous $k(f)$ in $f \in [f_0, 4f_0]$. However, it should be noted that the $|E(\beta(f))|$ is a decreasing envelope. So, the largest allowable span for an inital boundary condition is at f_0. In contrast to $\beta(f)$ analysis, where we define the inital boundary at the band edge, design of $k(f)$ starts from $f = f_0$ to guarantee continuity. Figure 4.3 demonstrates the $k(f)$ functions of different $k(f_0)$ inital conditions for the boundary at $\beta(2f_0) = 0.5959$. Notice that the peak values gradually decrease in magnitude as our analysis of $|E(\beta(f))|$ suggested. As a general comment, though one may find other functions behaving differently within the intervals of boundaries, figure 4.3 shows the linear cases.

Hence a full-octave PA output matching can be designed by using the above procedure. The remaining part is to plot the corresponding impedances on a Smith Chart and test the impedances against the suggested intervals. The three-octave design is discussed under the next subsection, exclusively.

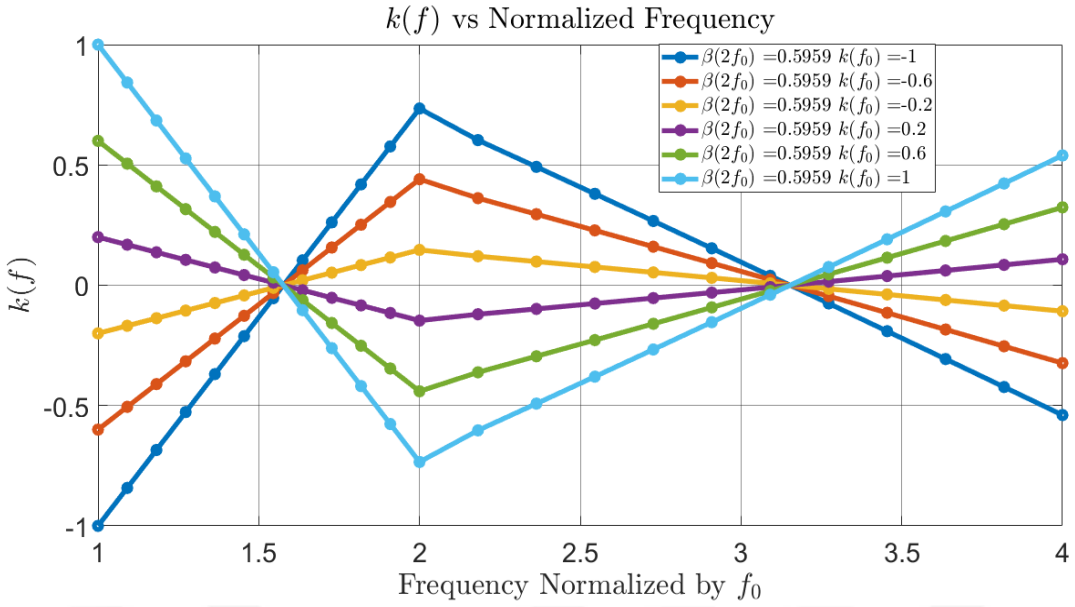


Figure 4.3: $k(f)$ for different boundary conditions set at $\beta(2f_0) = 0.5959$.

4.1.1 Three-Octave Design Scheme

This subsection discusses the parametric NRRCJ design space for a targeted bandwidth of three octaves. Using the analysis at the beginning of this section, the $\beta(f)$ function for $[f_0, 8f_0]$ is designed in the first place. Setting $0 \leq \beta(8f_0) \leq 0.5959$, figure 4.4 is obtained. In figure 4.4, it is clearly seen that as the frequency increases the available span of the function enlarges. This may be utilized to the advantage of the designer due to the fact that parasitics are more effective at higher frequencies. Furthermore, it should not escape from the attention that a conventional class-J mode may appear at $8f_0$ in case of boundary condition $\beta(8f_0) = 0$. $\beta(f)$ is re-plotted for $[f_0, 16f_0]$ in figure 4.5 to encapsulate the harmonics of the third octave. The design space of $\beta(f)$ at lower octaves becomes narrower as the band of operation increases.

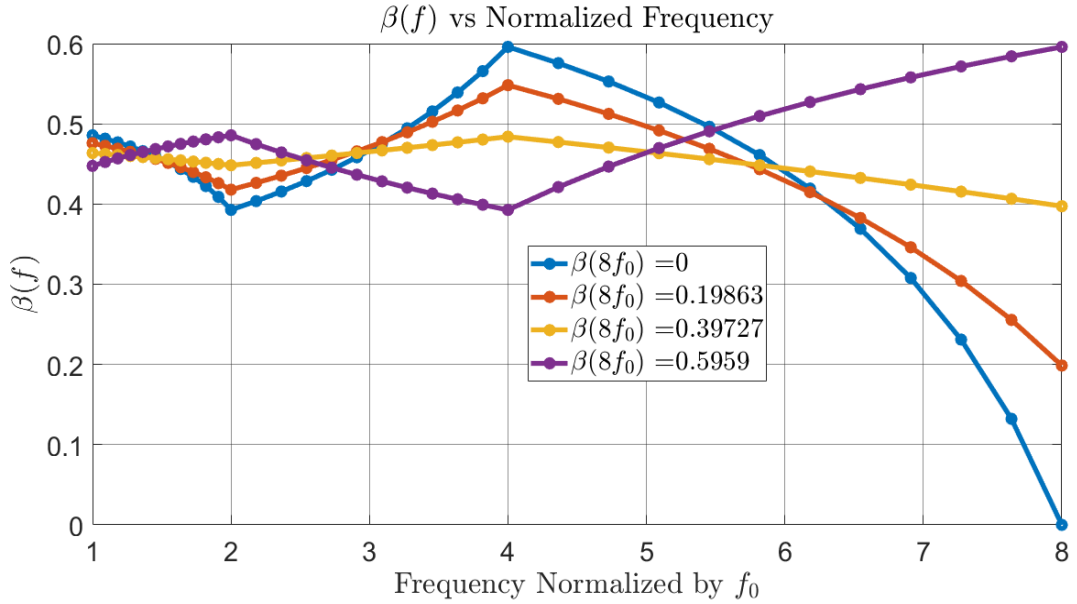


Figure 4.4: $\beta(f)$ for different boundary conditions set at $\beta(8f_0)$

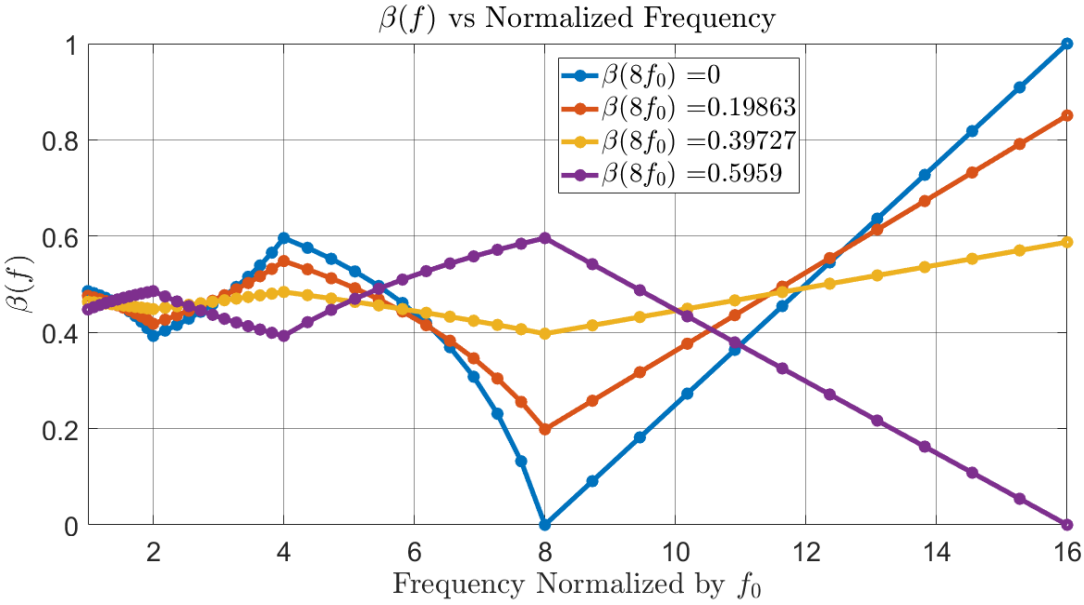


Figure 4.5: $\beta(f)$ for different boundary conditions set at $\beta(8f_0)$ plotted in $[f_0, 16f_0]$

The $k(f)$ is designed after having a valid $\beta(f)$ function. Given that each boundary condition at $8f_0$, thereby a given $\beta(f)$, a valid $k(f)$ function can be constructed by inital condition of $k(f_0)$ as in our previous analysis. Figure 4.6 shows the case for $\beta(8f_0) = 0.5959$ in $[f_0, 16f_0]$. It is obvious from the figure that the available range decreases by increasing frequency. It is not a surprising result that while $k(f)$ squeezes $\beta(f)$ opens up and vice versa. They balance each other in a trade-off relation such that $\beta(f)$ limits the design at lower octaves while $k(f)$ does at higher octaves.

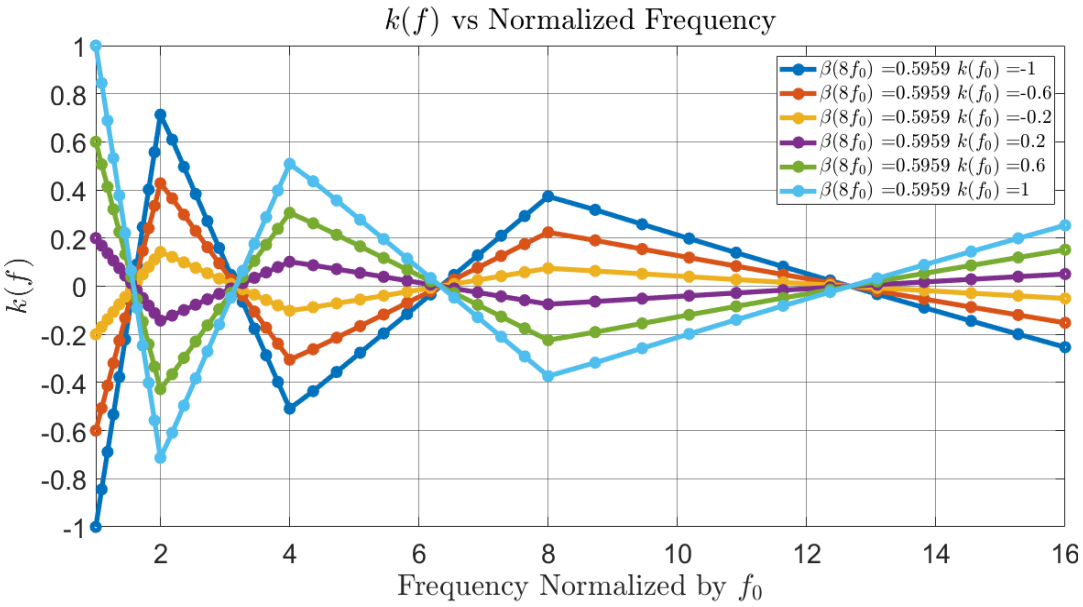


Figure 4.6: $k(f)$ for different boundary conditions set at $\beta(8f_0) = 0.5959$.

Any particular function is not expressed analytically for $\beta(f)$ and $k(f)$. Practical matching circuits are expected to show mismatches to the targeted impedance values. Thus, it is more practical to let the functions be shaped by matching network characteristics. The control over the mode continuum is provided by the range of functions reflected onto impedance space. For the sake of the discussion, we present the impedance space on the Smith Chart in the next section, where we argue the detailed practical design steps of prototypes.

4.2 Design of the Prototype

In this part, a design strategy which integrates described theory into practical application is presented. The NRRCJ approach is implemented with a commercially available RF power device. The final prototype is constructed after second iteration. Both of the manufactured prototypes are examined in terms of power, efficiency and design mindset. The targeted band is 400-3200 Mhz, corresponing to 3-octaves bandwidth. This operation band encompasses most of the frequently used communication channels [36]. First, the impedance space relevant to three octave design scheme is provided at the current generator plane. A general information of the selected device is provided. Impedance space is de-embedded upto package plane. Output and input matching circuits of the two prototypes are explained, seperately. The design of matching circuits includes EM simulations and optimizations. Linear, nonlinear and electromagnetic simulations are performed in AWR Microwave Office design environment. All EM simulations are done using AXIEM planar electromagnetic solver. Layout, mechanical dimensions and schematic of the final design are provided.

4.2.1 Output Matching Design

Targeted output impedances are calculated using the impedance equations in previous subsection. Impedance spaces for the 1^{st}, 2^{nd} and 3^{rd} octave are treated discretely. Harmonic impedance space of the 3^{rd} octave lies in $[8f_0, 16f_0]$, in which $8f_0$ is the last point we intend to obtain RF output power. In practical perpective, it is a quite difficult task to manage impedance up to $16f_0$, due to component limitations. When component limitations are involved such as self-resonance characteristics of coils, capacitors and improper or quite uncertain electrical model of the device at hand, it is plausible to prioritize the fundamental tone matching of the three octaves using NRRCJ design space.

Hence, we plot the design space for fundamentals only for 1^{st} and 2^{nd} octaves. Figure 4.7 depicts the impedance space for $[f_0, 2f_0]$. Impedance space is generated for the parameter set $\beta \in [0.39, 0.49]$ and $k \in [-0.73, 0.73]$. Second octave impedance space is given in figure 4.8, generated for $\beta \in [0.3927, 0.5959]$ and $k \in [-0.5, 0.5]$.

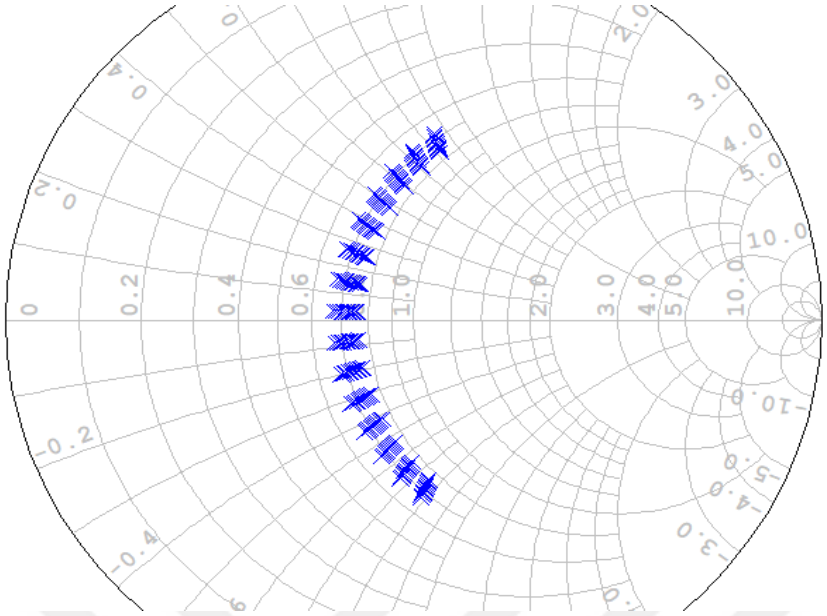


Figure 4.7: First octave impedance space at intrinsic plane.($Z_0 = R_{opt}$)

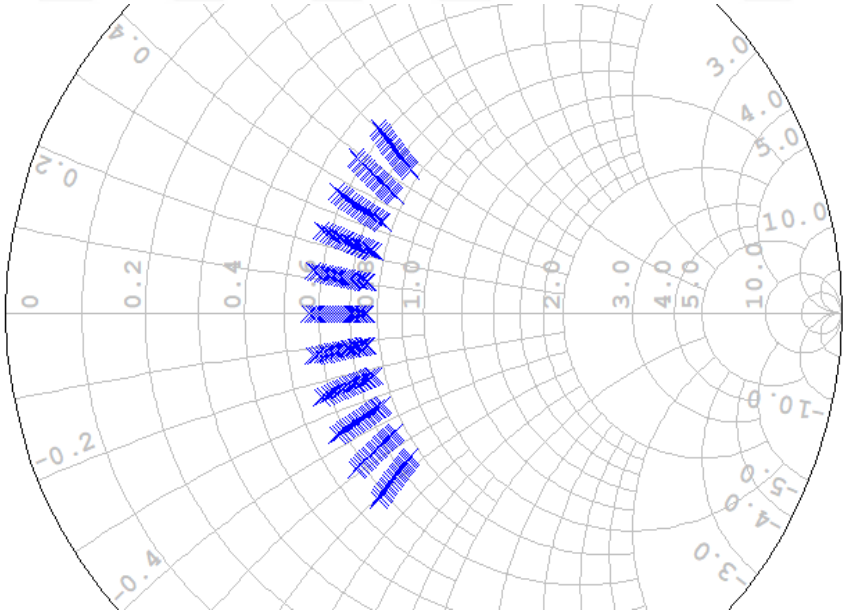


Figure 4.8: Second octave impedance space at intrinsic plane.($Z_0 = R_{opt}$)

Third octave impedance space is given along with the second harmonic points. Figure 4.9 demonstrates the impedance space in $[4f_0, 16f_0]$. Evaluation intervals are $\beta \in [0, 0.5959]$ and $k \in [-0.4, 0.4]$. The parameter set is substituted into equation (3.33) to generate harmonic impedance space located in $[8f_0, 16f_0]$.

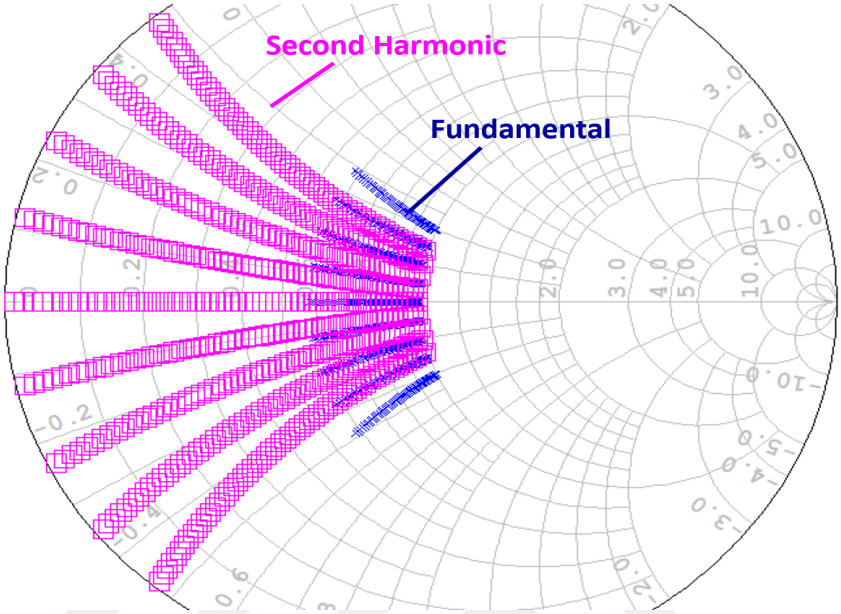


Figure 4.9: Third octave fundamental and harmonic design space at intrinsic plane.($Z_0 = R_{opt}$, blue "x" : fundamental, pink "□" : second harmonic loads)

Since the impedance calculations are done at the intrinsic generator plane, output parasitic model is needed to transform the transistor package plane to generator plane. The selected device CG2H40010F from Cree Inc. is the second-generation version of CGH40010F. First version is a well-studied one in the literature and package plane parasitic de-embedding studies exist such as in [37]. The equivalent circuit of [37] is also employed for broadband design practices such as in[13]. Transistor reference plane equivalent circuit topology is given in figure 4.10. C1 in figure 4.10 is the C_{ds} (drain-source capacitance) of the device given in the datasheet. After work of [37], an update is made by manufacturer in datasheet to 1.3 pF. In recent CG2H40010F product datasheet, it is stated as 1.84 pF which we will use in our work.

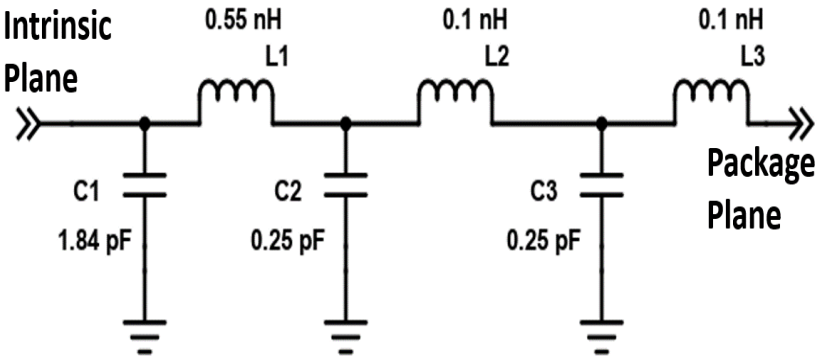


Figure 4.10: Package parasitics equivalent circuit of CG2H40010F (modified from CGH40010F model)

To fully use the impedance equations outlined in the previous section, the class-A optimum resistance needs to be determined. Optimum class-A load is hard to determine due to thermal conditions and I-V knee walkout [38].This phenomenon can be understood from simulated I-V curves in figure 4.11, obtained via the complete large-signal model of manufacturer.

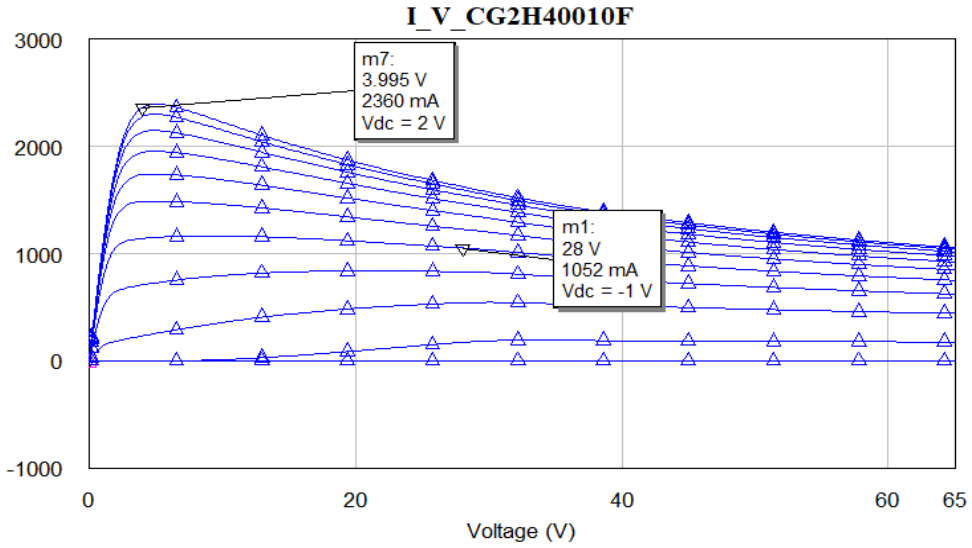


Figure 4.11: Static I-V curve of CG2H40010F under condition of 25 C^0 base temperature with R_{JC} = 8.

Since matching circuit input impedance will result in reactive parts of impedances,

parasitic effects are quite a big deal to compensate for both fundamental and harmonic impedance handling purposes. Figure 4.11 shows the static I-V curve of the device. Knee walkout and current decay is obvious for the regions where heat dissipation increases. I_{max} is found to be around 2.4 A with an accepted knee voltage of 4 Volts. Class-A bias point is chosen to be half the saturated drain current intersected with 28 Volts supply voltage. By using this knowledge, ideal class-A optimum load at the generator plane is approximately calculated as 20 ohms. However, this value may change with the frequency as the related research in [38] suggests. Using the sources at hand, load-pull simulations are carried out at 400 MHz and 3200 MHz, which are edge points of targeted band. The load-pull data for those frequencies are depicted in figures 4.12 and 4.13. The optimum loads for maximum output power are found as $21.35 + j8.16$ and $8.26 + j5.41$, respectively. When the model given in figure 4.10 is used to de-embed the loads to intrinsic plane of the transistor, the impedances transform to $23.64 + j7.47$ and $51.27 + j7.82$, respectively.

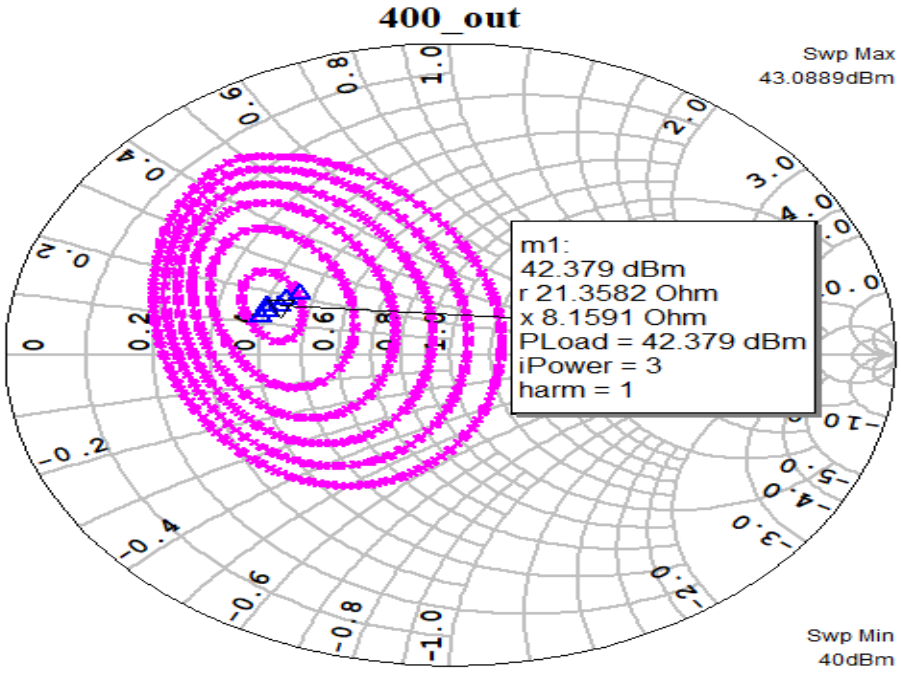


Figure 4.12: 0.4 GHz load contours at package plane with 0.5 dB increments from 40 to 42 dBm.

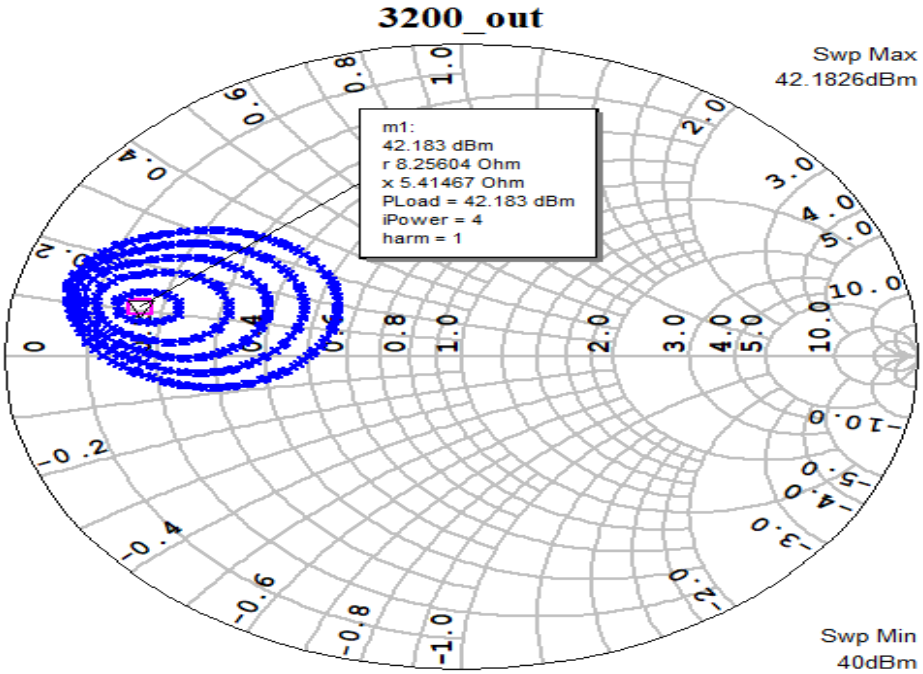


Figure 4.13: 3.2 GHz load contours with 0.5 dB increments from 40 to 42 dBm.

In this case, when real parts of the impedances are taken into account, we see the estimated 20Ω approximates well at the lower edge of the band. In contrast, at the higher edge of the band, the same statement is invalid. To mitigate this conflict, the arithmetic average of the real parts are selected as the $R_{opt,A}$ which is approaximately 37.5Ω. In the work of [39], normalization impedance is chosen 36Ω, for the first generation version CGH40010F, while in [13] authors first calculate as 23Ω and carry out load-pull to mitigate high efficiency and high power impedance contours. Thus, selecting the optimum load as 37.5Ω is a reasonable practical design decision.

Hence, we can de-embed the intrinstic plane loads to the generator plane. De-embedded impedance spaces are shown for 800, 1600, 3200 Mhz together with 6400 MHz in figures 4.14-16, with normalized impedance of 50Ω and $R_{opt} = 37.5\Omega$. Edge points of the octaves are selected because the parasitics are most effective at these points. In addition, those points provide clear provision about the target impedance sets due to our design strategy of β and k paramaters based on boundary conditions swept across the limits.

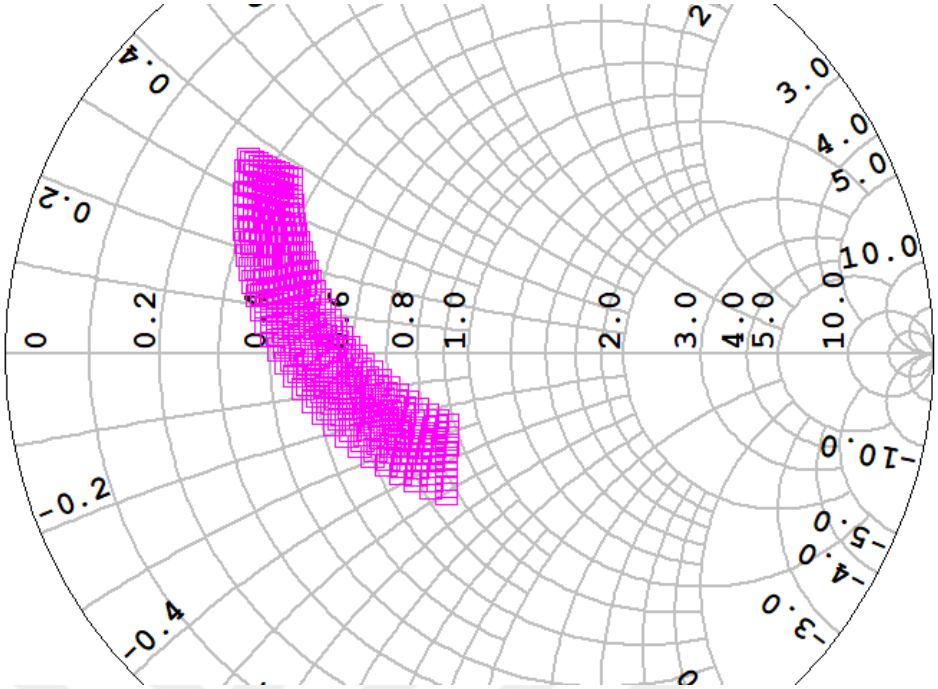


Figure 4.14: First octave loads de-embedded at 800 MHz.

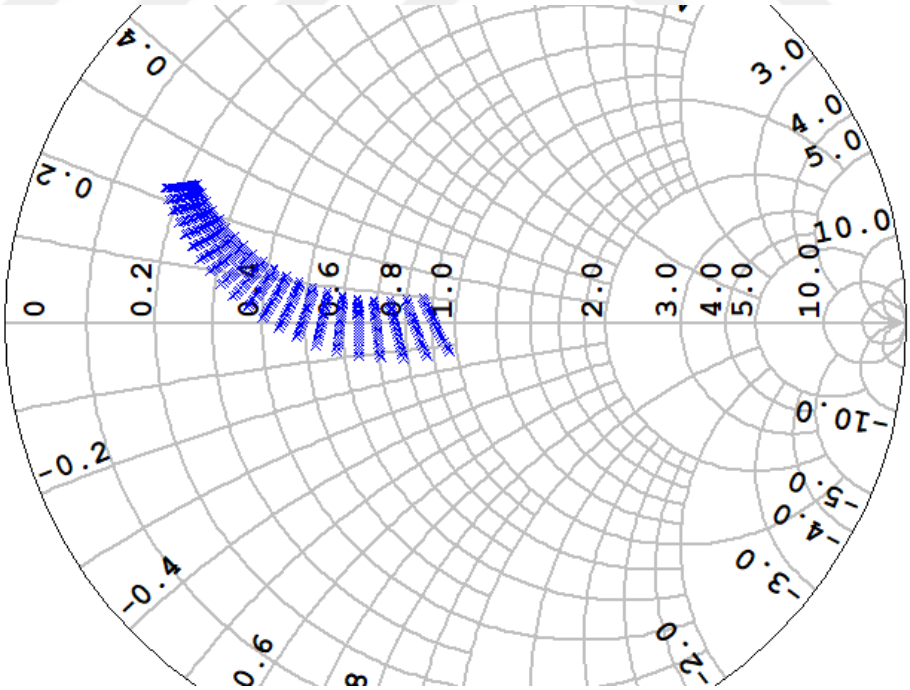


Figure 4.15: Second octave loads de-embedded at 1600 MHz.

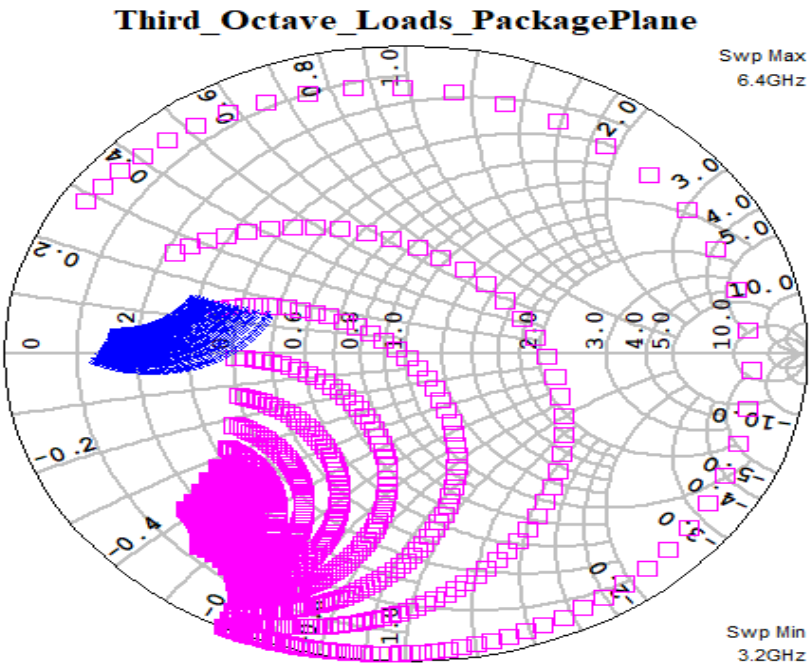


Figure 4.16: Third octave loads de-embedded at 3200 MHz with second harmonic de-embedded at 6400 MHz(blue "x" : fundamental, pink "□" : second harmonic loads).

Considering the fact that we don't have a fully characterized parasitic newtork but an assumed one, a plausible strategy is to first find a matching network that falls in those approximate impeadance borders, then optimize to the profit of power and efficiency. In parallel with the presentend knowledge, our general design procedure can be listed as follows.

- Impedance contours are plotted in the package plane of the device.
- Fabrication technology and material are selected.
- A matching circuit toplogy is determined such as low pass, high pass (usually low pass for broadband operation).
- Toplogy is optimized to within reasonable mismatch limits in the designated impedance space.

  (i) Because a perfectionist approach to the problem may be misleading, a mismatch level such as 15 dB is allowed.

- After linear circuit simulations, EM analysis are performed and re-optimized if there exists a certain difference.
- Compeleted output network is utilized to obtain best possible gain in desgin of the input matching network.
- Stability analysis is done while designing the input matching circuit.
- After obtaining a fully stable and reasonable gain, the power and efficiency are re-considered in comparison with the aimed performance specifications.
- Rough thermal analysis is performed to check whether the design is feasible in terms of thermal conditions.
- Prototype is fabricated and measured.

4.2.2 Prototype I

The fabrication technology is selected as microstrip printed circuit board. The board material is RO6035HTC with a thickness of 0.762 mm and $\varepsilon_r = 3.66$. The first prototype output section is designed with a single stub matching network. EM simulations are done using AXIEM. In figure 4.17 the matching strip dimensions are provided.

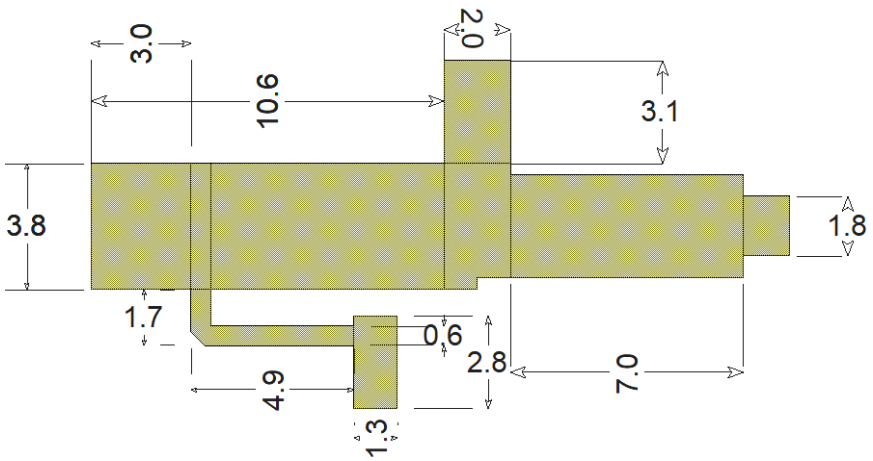


Figure 4.17: Prototype 1 layout dimensions of the output matching (dimensions are in mm).

The last line is nothing but a pad for placement of DC blocking capacitor. Though

most of the matching mission is attributed to microstrip transmission lines, the lumped components have significant effect on the performance, as well. The DC block capacitor and RF choke inductor are selected such that the SRF values and current handling capacity are sufficiently high. Output circuit layout and component reference numbers are depicted in figure 4.18. The transistor footprint is placed accordingly on the figure, for scalable comparison. Component descriptions are given with manufacturer part numbers in table (4.1). Note that $C4$ is an overqualified capacitor. It is used because of easy availability at the moment. One may prefer a lower voltage type which will decrease the cost.

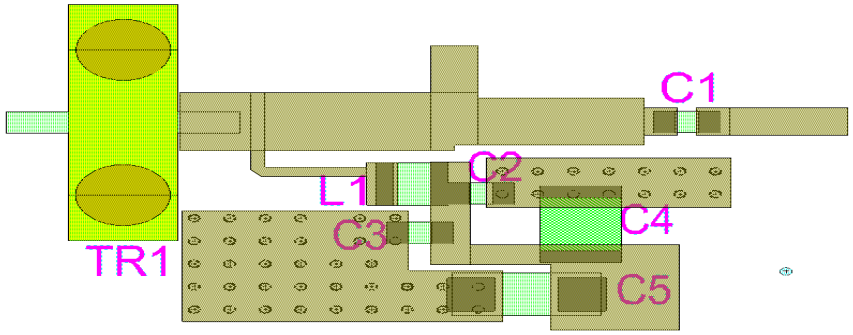


Figure 4.18: Output matching layout with reference numbers of components.

Table 4.1: Bill of Materials List Of Output Circuit

L1	0908SQ27N (Coilcraft 27 nH inductor)
C1	600F220 (ATC 600F series 22 pF capacitor)
C2	600F241 (ATC 600F 240 pf capacitor)
C3	600F121(ATC 600F 120 pF capacitor)
C4	3.9 nF 500V ceramic capacitor
C5	10 uF 50V tantalum capacitor

A full output circuit EM simulation is done with component S-parameters included. Output impedance results are drawn on Smith Chart in figure 4.18. Some of the impedance points are marked on the chart. With a rough inspection, we can observe that some impedance points are not satisfactory when compared with the figures 4.14-16.

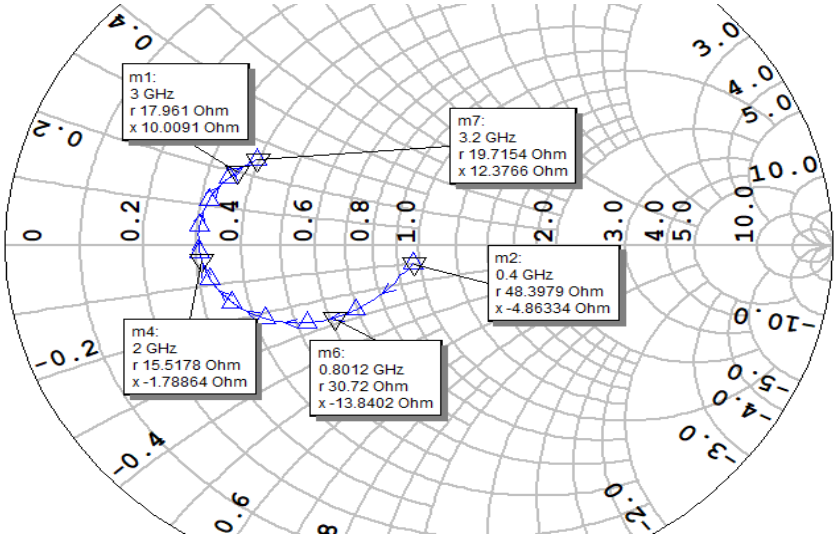


Figure 4.19: Output impedance seen from the package plane($Z_0 = 50\Omega$)

The detailed comparison is done by drawing impedances on the same graph by octaves. Figures 4.20-22 compare the obtained impedances with targeted impedances plotted in 4.14-16.

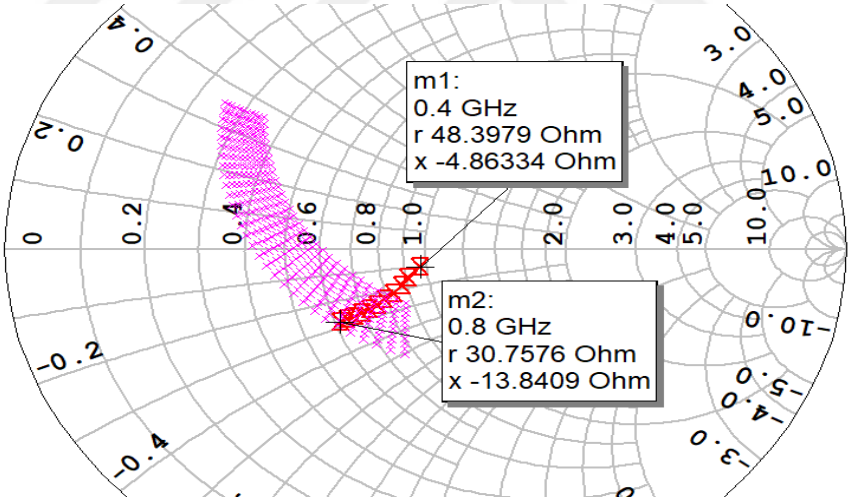


Figure 4.20: Compared impedances at the package plane for de-embedded first octave space at 800 MHz.($Z_0 = 50\Omega$)

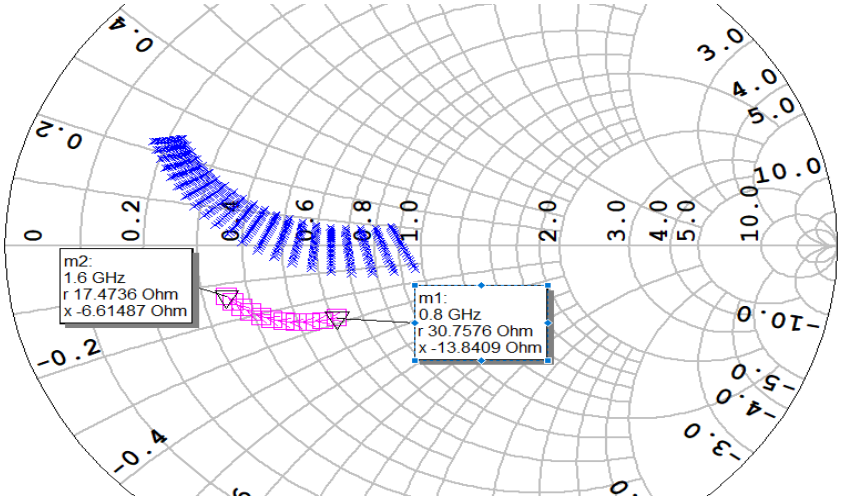


Figure 4.21: Compared impedances at the package plane for de-embedded second octave space at 1600 MHz.($Z_0 = 50\Omega$)

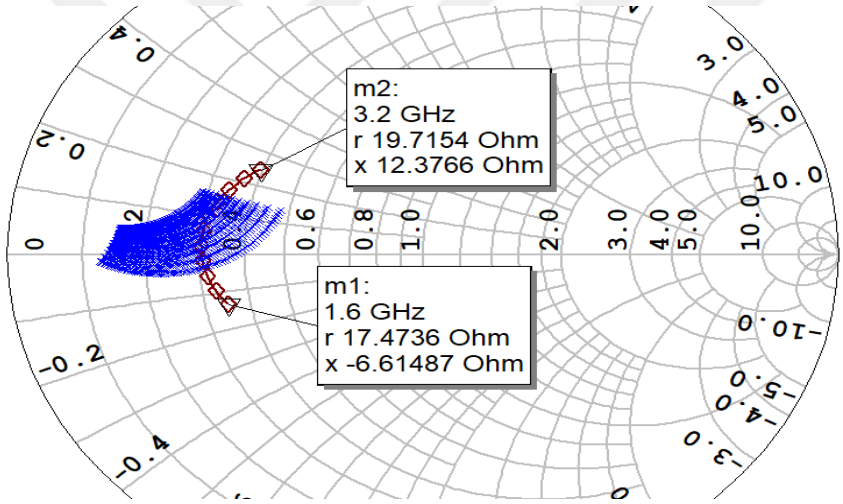


Figure 4.22: Compared impedances at the package plane for de-embedded third octave space at 3200 MHz.($Z_0 = 50\Omega$)

In figure 4.21, a severe deviation from the targeted impedance points occurs. In the first octave and third octave, the deviation seems relatively lighter than the second octave. To clearly justify the third octave, the harmonic space should be included, as well. Figure 4.23 shows comparison with the simulated impedance from 3.2 to 6.4 GHz. It should be noted that the de-embedding for harmonic impedance set applied at 6.4 GHz may not be sufficient. Since the harmonic space follows a counter-clockwise pattern with increasing freqeuncy, some frequencies in third octave may fail to satisfy

the second harmonic conditions. To observe this effect, targeted impedances are de-embedded at 4.4 GHz and 6.4 GHz. 4.4 GHz is particularly chosen because it is approximately the frequency where the harmonic impedances of third octave start to fall into NRRCJ set.

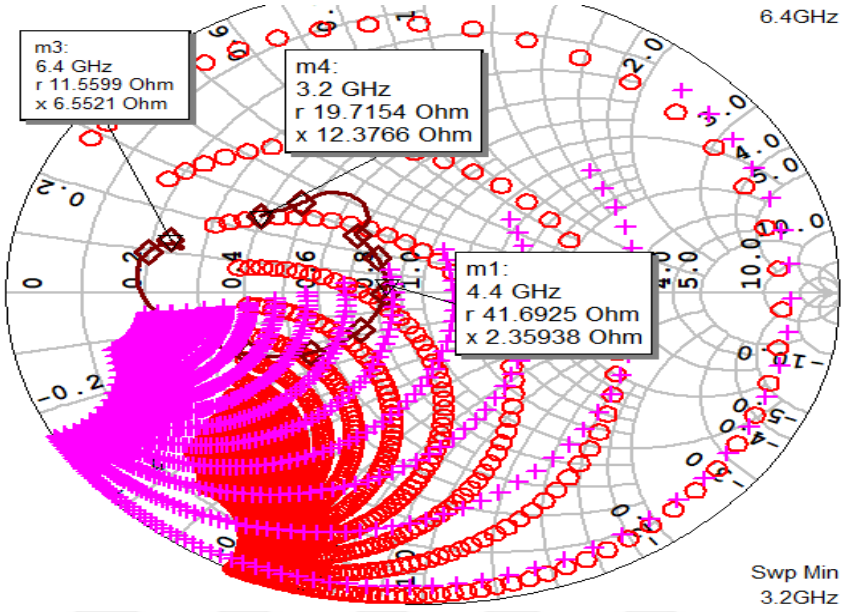


Figure 4.23: Third octave harmonic space comparison.(red "$\circ$": 6.4 GHz, pink "+": 4.4 GHz, brown "$\diamondsuit$": matching circuit) ($Z_0 = 50\Omega$)

In the third octave harmonic space, it is clear that harmonics of some frequencies are not located in the designated region. Counterclockwise rotation of these contours creates extra difficulty, as well. Knowing these, we expect performance degradation at the frequencies of those fundamental or harmonic tones are misaligned with targeted design space. Because this is the first prototype, it is intended to observe the correlation between theory and experiment results.

After the design of output matching, gain optimization and stability analysis are performed. Full circuit layout and dimensions are given in figure 4.24. First manufactured version is demonstrated in figure 4.25. However, as the PCB dimension are very small and soldered feed cables obstruct the tuning process a connectorized version is fabricated, as well. The connectorized version is depicted in figure 4.26. Component values are finalized after manufacturing. Information about finalized components are provided in table 4.2.

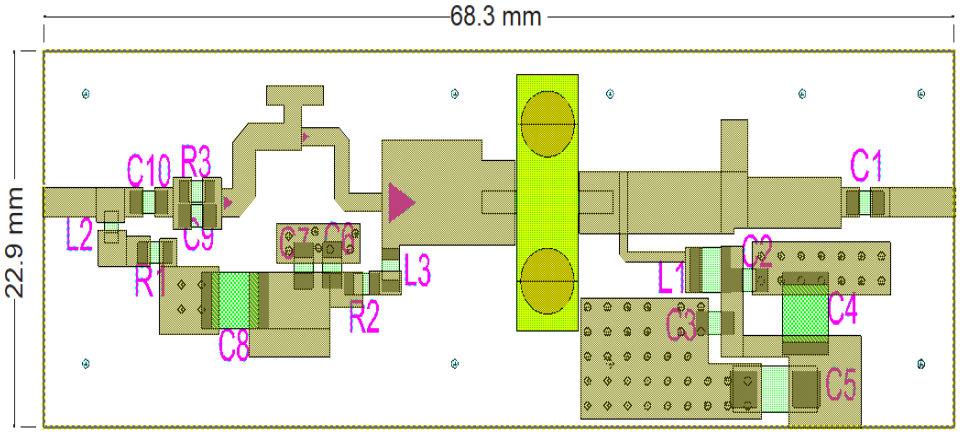


Figure 4.24: Full layout and occupied space for matching network of prototype I

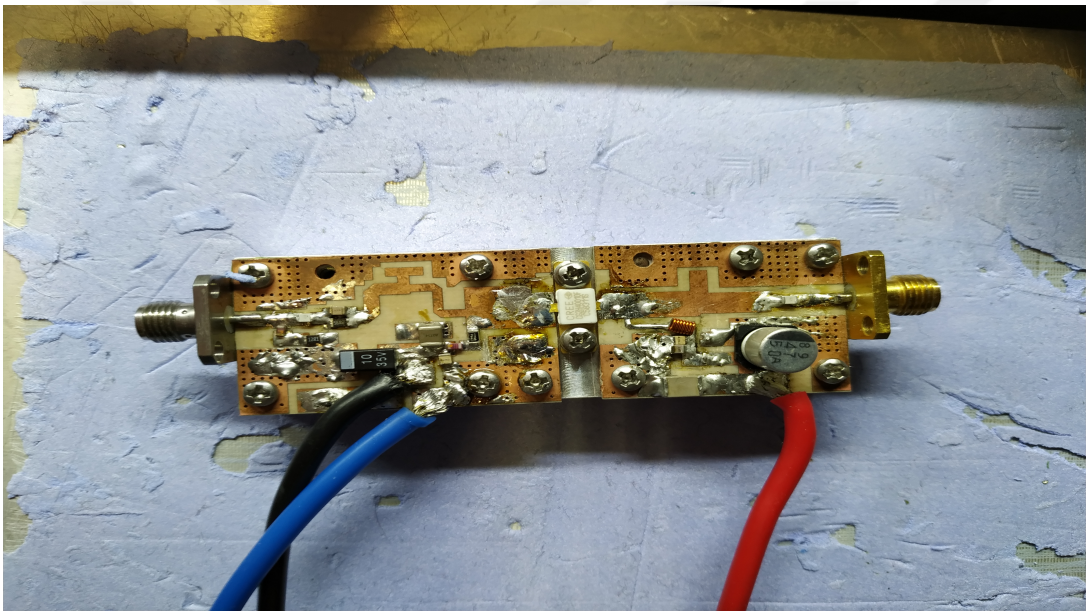


Figure 4.25: First fabricated version (small version) (Dimension are 68 mm x 23 mm)

Note that some components seem different than the footprints seen in figure 4.24. This is because figure 4.24 involves the finalized component footprints given in 4.26. While the same cold plate with the small version is used, board is extended to accomodate a simple connector.

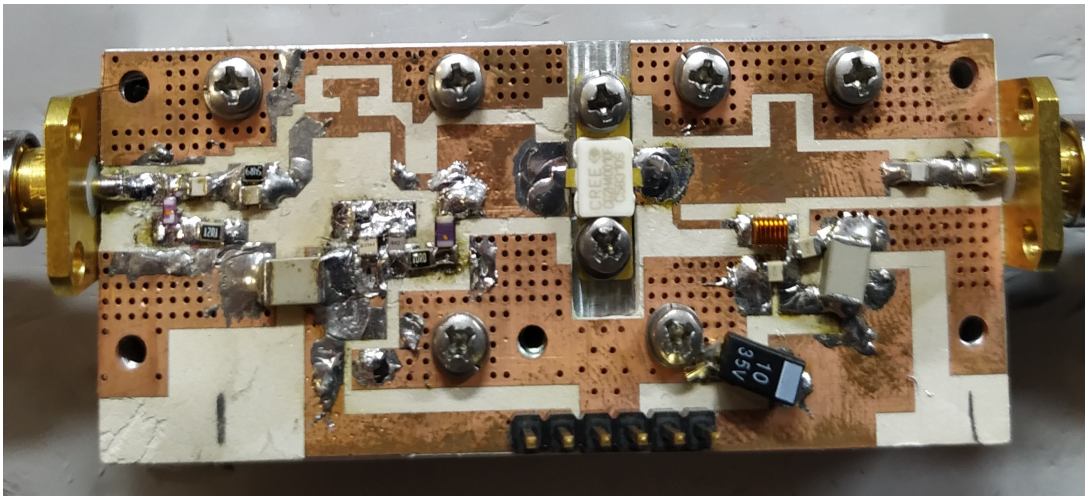


Figure 4.26: Manufactured connectorized version

Table 4.2: Bill of Materials List Of Input Circuit Prototype I

L2	06CS4N3(Coilcraft 0603 4.3 nH inductor)
L3	0805CS10N0 (Coilcraft 0805CS 10 nH inductor)
R1	0805 12.1 ohm resistor
R2	0805 10 ohm resistor
R3	0805 55 ohm resistor
C6	600F241 (ATC 600F 240 pf capacitor)
C7	100A270F (ATC 27 pF 100A series capacitor)
C8	3.9 nF 500V ceramic capacitor
C9	600F2R7(ATC 600F 2.7 pF capacitor)
C10	600F220 (ATC 600F series 22 pF capacitor)

4.2.3 Prototype I Results

After assembling of the pcb, small signal measurments are performed. The bias current is set 150 mA at 28V drain voltage. Measurement and simulation results are depicted in figure 4.27. Minimum 15 dB small-signal gain is achieved. Return loss measurements and simulations are provided in figure 4.28. At worst case, 4 dB return loss is obtained.

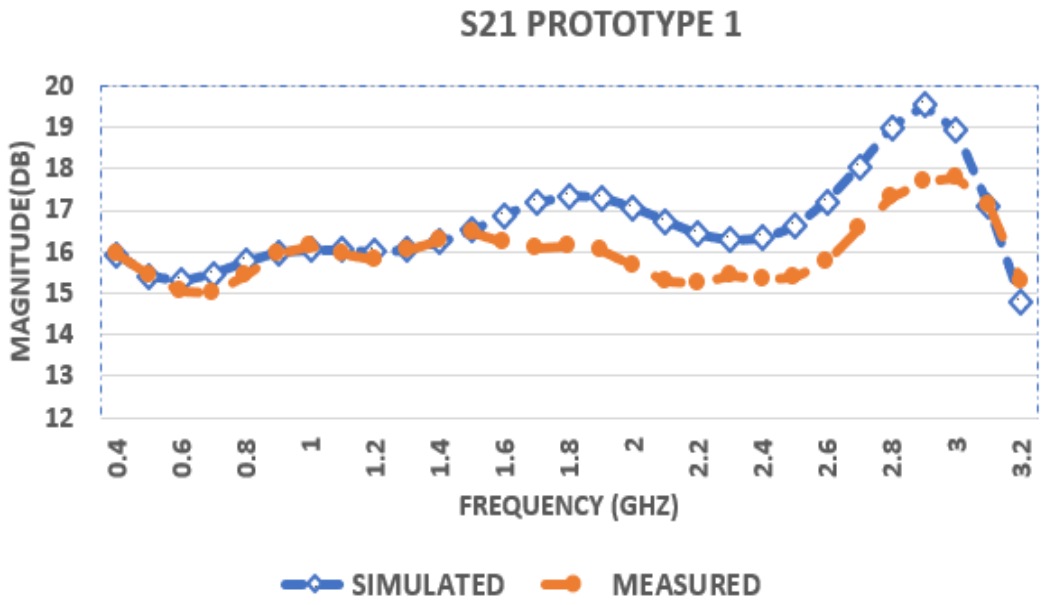


Figure 4.27: Simulated and measured small-signal gain

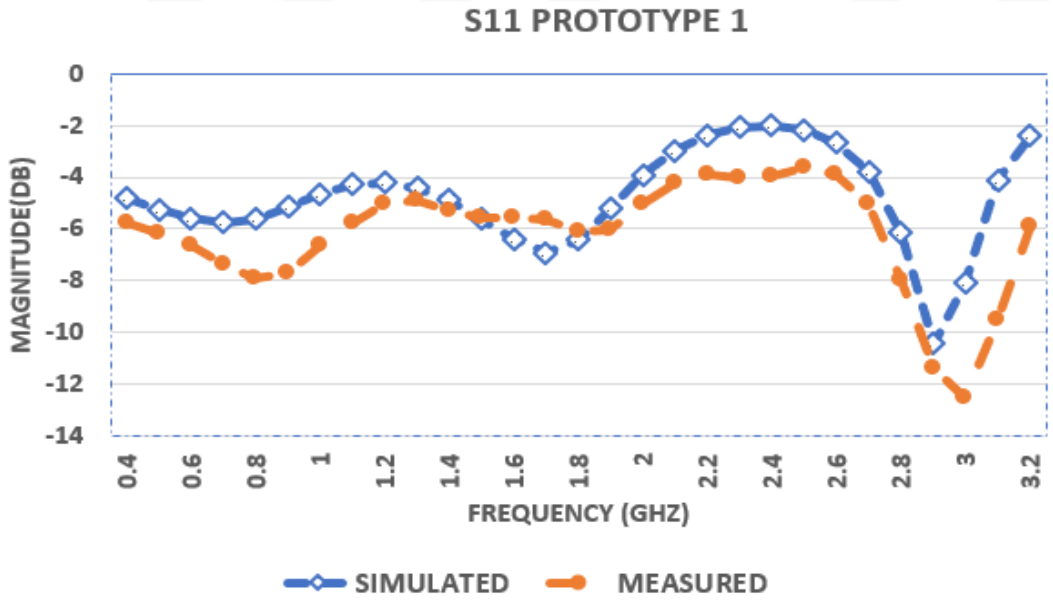


Figure 4.28: Simulated and measured S11

Large signal measurement setup photograph is given in figure 4.29. Input and output power of the PA is measured using average power sensors. Two types of driver amplifiers were used to generate input power signal, because approximately 30 dBm input power was needed over 400-3200 MHz frequency band.

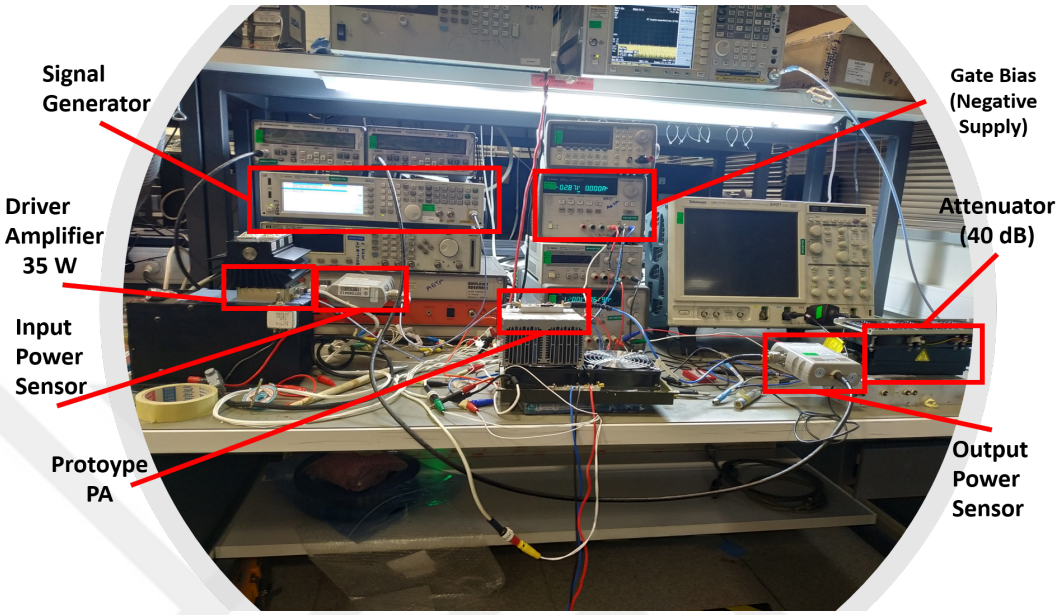


Figure 4.29: Large Signal Measurement Setup

Power output measurements are performed first by keeping the output power constant at 40 dBm using a low-loss short length output cable. Measured drain efficiency and current results are provided in figure 4.30. Simulated efficiency and drain current are plotted in figure 4.31 at 40 dBm output power. A slight difference is seen between simulated and measured results. In particular, it is rooted in the output cable loss. Because the power sensor reads the power after cable loss, the actual output power is higher than 40 dBm. The effect increases as the frequency is increased. This explains the increasing difference between simulation and measured results at upper frequencies. It is important to note that the efficiency performance decays in the second octave as we expected by the impedance analysis which exceeds the impedance space boundaries of NRRCJ. In addition, during the third octave, efficiency recovers again as suggested.

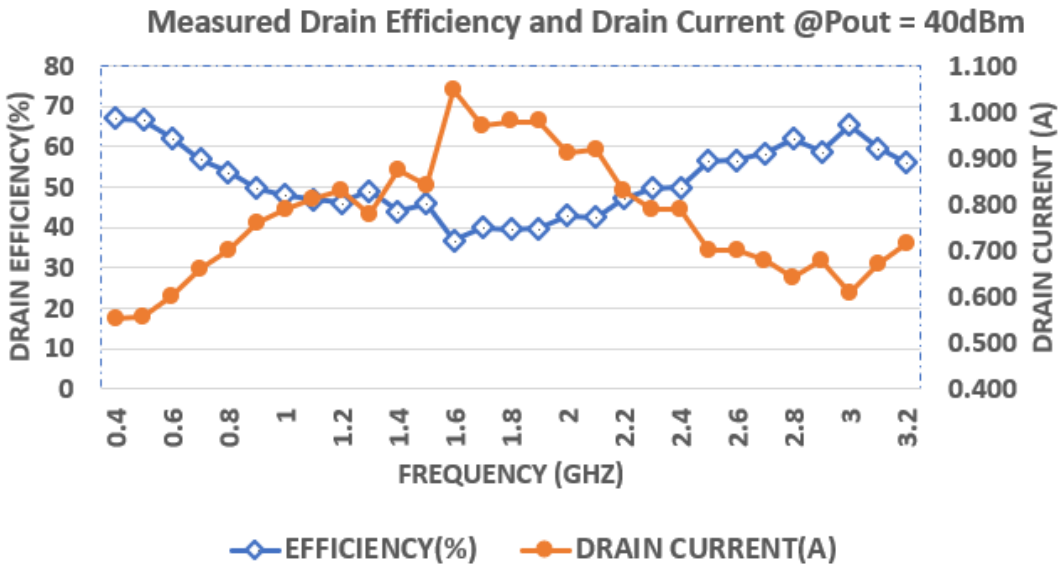


Figure 4.30: Measured drain efficiency and current for $P_{out} = 40dBm$

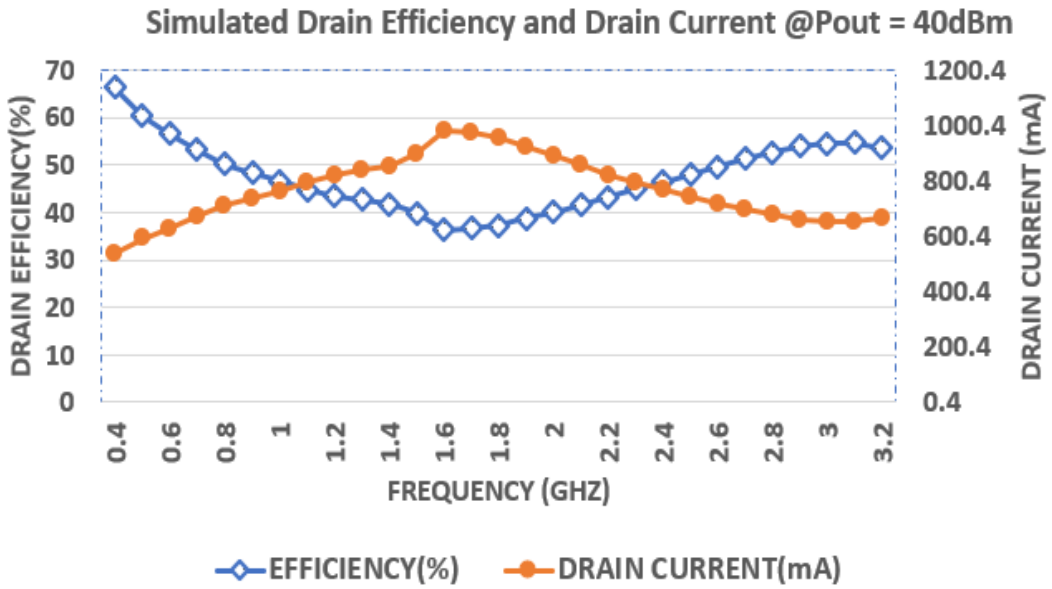


Figure 4.31: Simulated drain efficiency and current for $P_{out} = 40dBm$

While keeping the output power constant may cause underrated power and efficiency performance at some frequencies, oversaturated performance may also occur. Gain compression for 40 dBm output power is plotted in figure 4.32 to justify the performance metrics, accurately. It is observed that operation at 400-600 MHz are saturated over 5 dB compression. There are similar studies accepting higher compression levels for the saturated output power, i.e. over 6 dB and more, as given in [40, 41, 42]. On the other hand, we will adopt 5 dB as the maximum allowable compression level to determine the P_{sat} point.

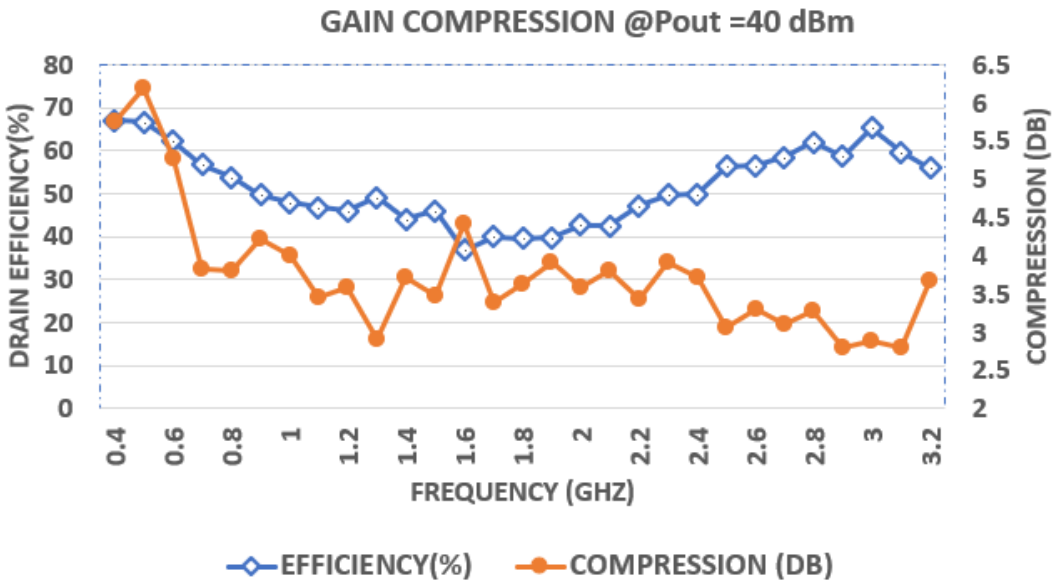


Figure 4.32: Measured gain compression vs drain efficiency for $P_{out} = 40dBm$

Hence, saturated power measurements are performerd to justify peak efficiency performance of the PA. Measured saturated power levels and power gain is plotted in figure 4.33. The gain compression and drain efficiency is plotted in 4.34 measured for the saturated power output levels. Minimum 38.3 dBm and maximum 42.8 dBm saturated output power performance is achieved at maximum 5 dB compressed gain. Minimum power gain is 10.3 dB. Drain efficiency drops as expected under the expected level of 45% in the second octave. It recovers in the mid-region of third-octave then drops again towards 3.2 GHz. This behaviour in third octave was also suggested by the impedance analysis figure 4.23.

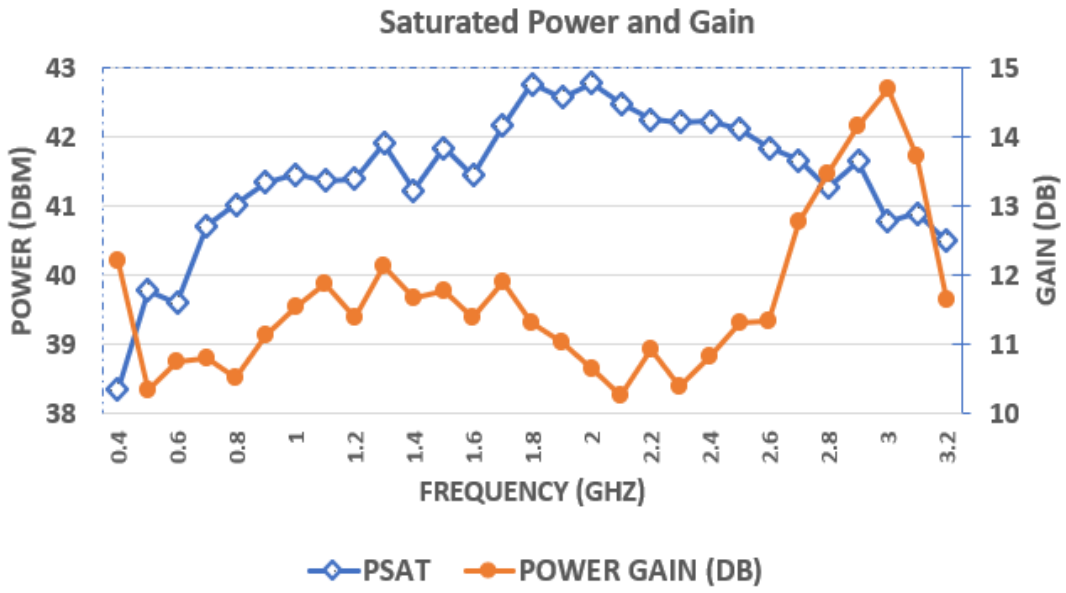


Figure 4.33: Measured saturated output power and gain

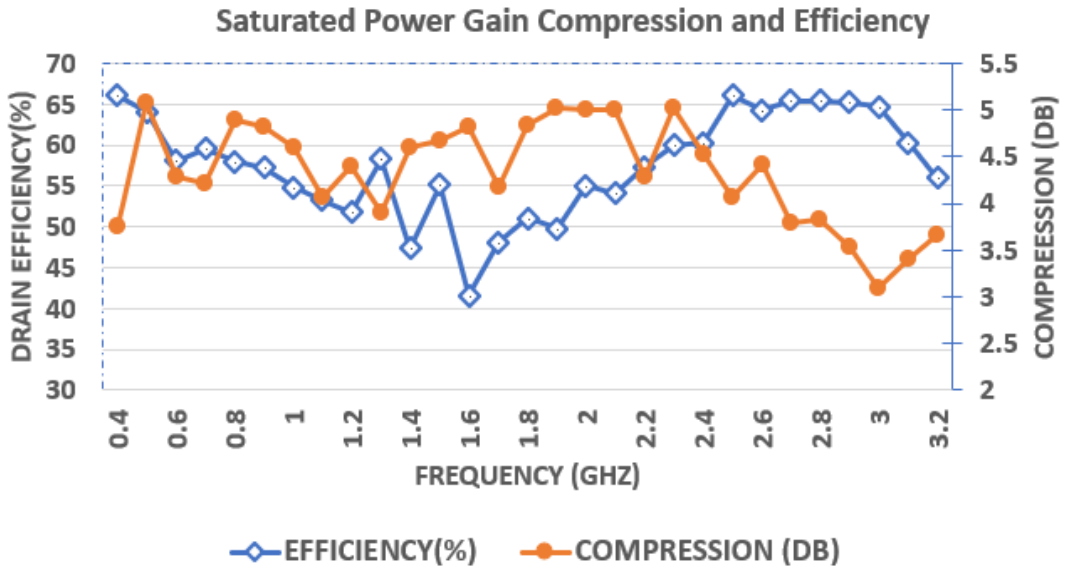


Figure 4.34: Measured drain efficiency and gain compression at saturated output power

The minimum of efficiency is 41.5% and maximum is 66% at the saturated output power. The average drain efficiency over the entire band is calculated as 57.54%. The average output power is 41.5 dBm corresponding to 14.2 W. Average values are provided as a figure of merit for comparison of the future works. Besides, the deviations from the proposed NRRCJ impedance space, we can say that the experimental results are in good agreement with the theoretical expectations.

It is important to note that our design procedure is not established on one-to-one matching of harmonic pair impedances. The NRRCJ theory points out that there exists impedance pairs capable of reasonable output power and efficiency which are sustainable over broadband. Basically, it diminishes the space of impedances in which optimum solutions are searched. Practical design follows by focusing to stay within those prescribed impedance space. The experiments of prototype 1 show that results are not devastating even for the cases of which one-to-one matching is missing. Having these motivations, we proceed to optimize for better performance results, especially for the second octave.

4.2.4 Prototype II

Manufacturing technology and the selected substrate material is the same with the first prototype. The output matching topology is upgraded to double-sectiton double stub tuning. Figure 4.35 shows the output matching layout with rough dimensions.

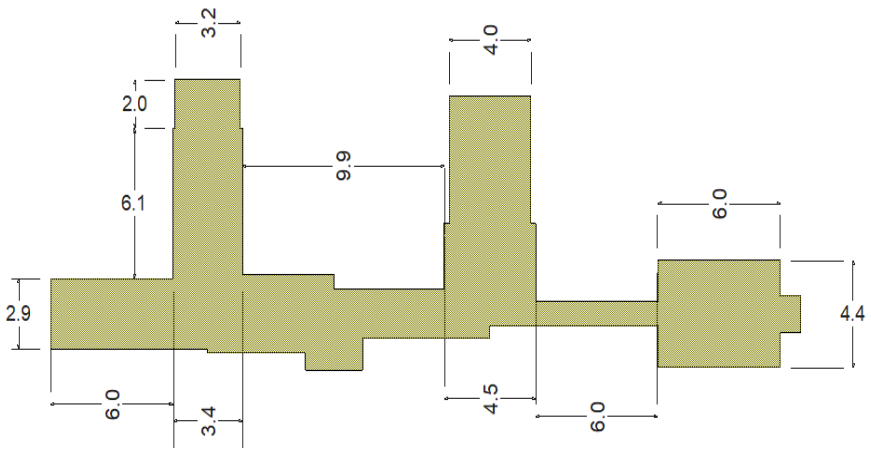


Figure 4.35: Prototype 2 output layout rough dimensions (mm)

Because it is more complicated than the first prototype, full dimensions are not given. The full layout outer dimensions, component placement and reference numbers are demonstrated in figure 4.36. Finalized component values are listed in table 4.3.

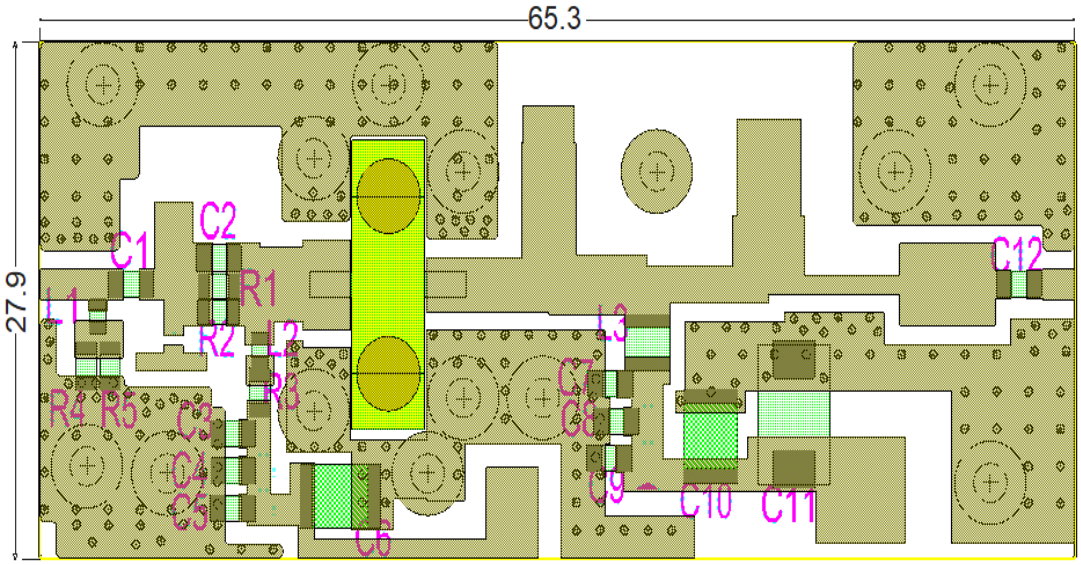


Figure 4.36: Prototype 2 full layout and dimensions(mm)

Table 4.3: Bill of Materials List Of Prototype 2

L1	06CS4N3(Coilcraft 0603 4.3 nH inductor)
L2	0603CS10N0 (Coilcraft 0603CS 10 nH inductor)
L3	0908SQ27N (Coilcraft 27 nH inductor)
R1, R2	0805 42 ohm resistor
R3	0805 10 ohm resistor
R4, R5	0805 96 ohm resistor
C1, C9, C12, C5	600F220 (ATC 600F series 22 pF capacitor)
C2	600F6R8(ATC 600F 6.8 pF capacitor)
C4, C8	600F121 (ATC 600F 120 pF capacitor)
C3, C7	600F241 (ATC 600F series 240 pF capacitor)
C6, C10	3.9 nF ceramic capacitor
C11	10 uF 50V tantalum capacitor

The output matching EM simulations are performed. The component touchstone files provided by the manufacturers are included into simulations. The package plane output impedance is plotted in figure 4.37.

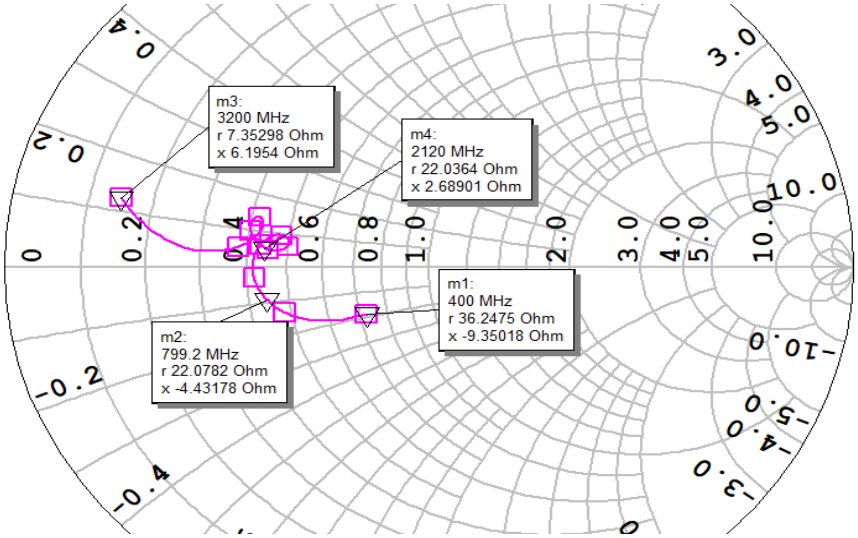


Figure 4.37: Output impedance of prototype 2 ($Z_0 = 50\Omega$)

De-embedding of the NRRCJ impedance space to package plane is done using the same package model. Figures 4.38 - 4.40 shows the comparison of package plane impedances.

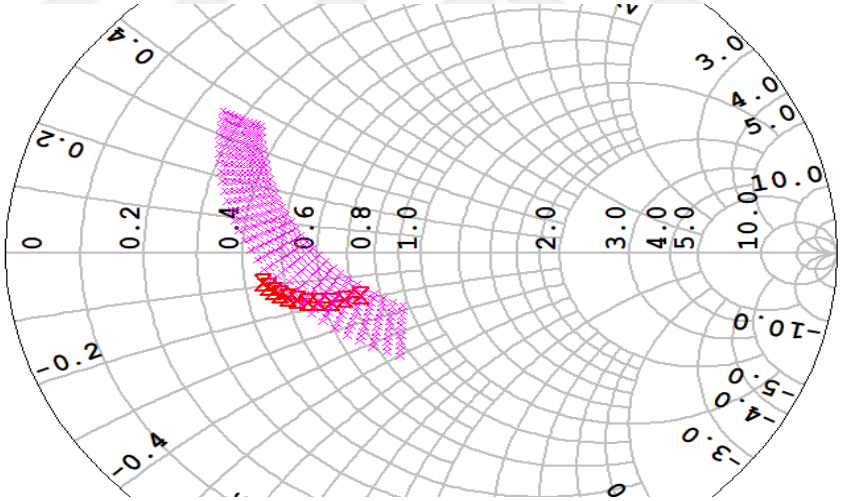


Figure 4.38: Prototype 2 first octave impedance and NRRCJ space de-embedded at 800 MHz.($Z_0 = 50\Omega$)

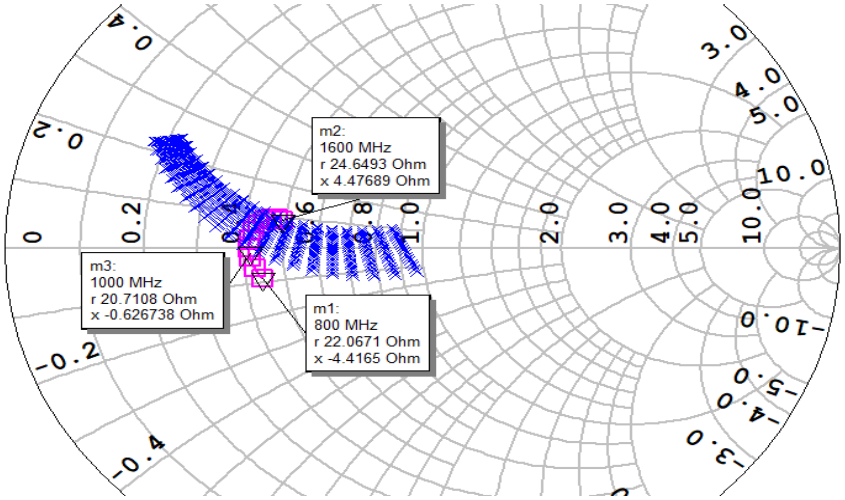


Figure 4.39: Prototype 2 second octave impedance and NRRCJ space de-embedded at 1600 MHz.($Z_0 = 50\Omega$)

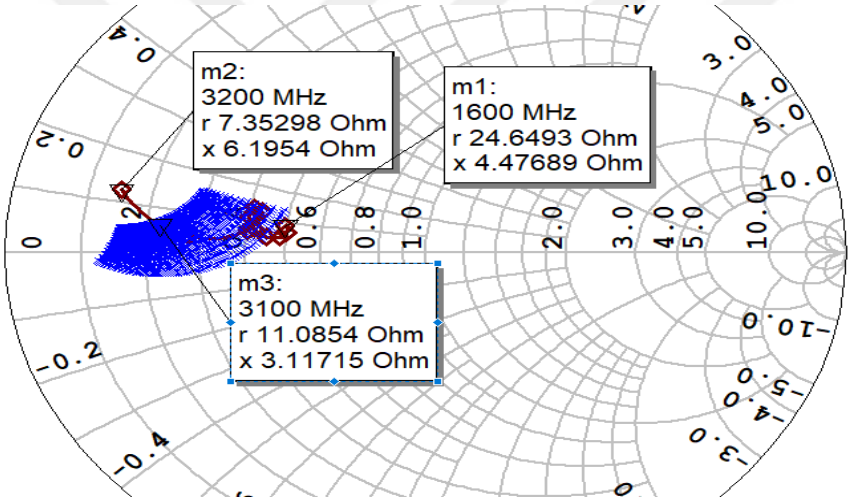


Figure 4.40: Prototype 2 third octave impedance and NRRCJ space de-embedded at 3200 MHz.($Z_0 = 50\Omega$)

When the above figures are compared with counterparts of the prototype 1, obvious improvements are seen. There are still some frequency intervals that lie outside of the impedance boundaries but they are in minority. A locally derated performance can be expected around those points. The third octave impedance space is compared again with the same two frequency method adopted in prototype 1. The same de-embedding frequencies are used for easy comparison in figure 4.41.

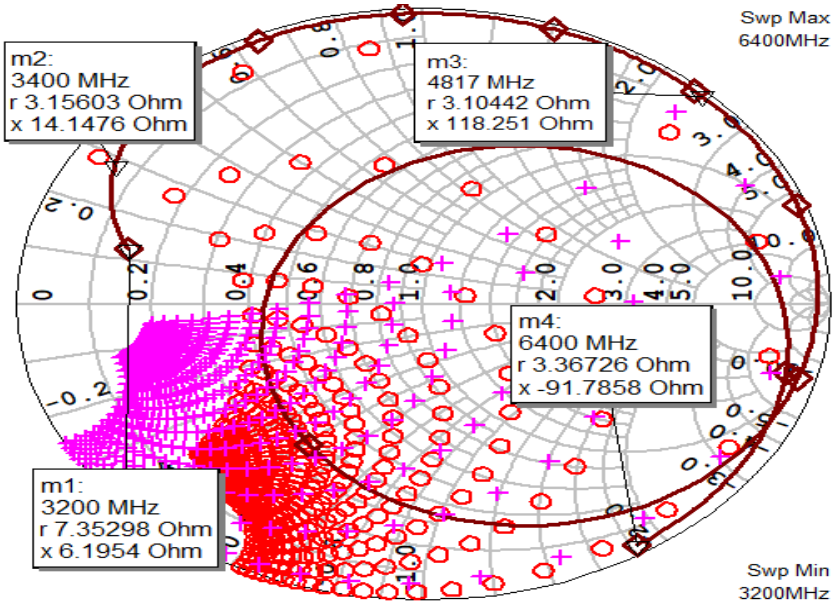


Figure 4.41: P2 third octave harmonic space comparison.(red "○": 6.4 GHz, pink "+": 4.4 GHz, brown "♢": matching circuit) ($Z_0 = 50\Omega$)

At this point we see the harmonic space of the third octave doesn't expose major improvement. However, due to longer matching network, some component resonances operate to move the harmonic impedances to desired region such as around 5.4 GHz. It is also open to discussion that how well the component s-parameter models are accurate for those frequencies. As it is suggested at the beginning of this section, priority of obtaining better match is given to lower octaves. As long as the uncertainity of models remains in such high frequencies, precise statements must be avoided.

Having the satisfactory results of impedance matching, the PCB and mechanics are assembled as in figure 4.42. Note that triple resistor bank connected to input matching via a capacitor is intact. Capacitor was removed to tune the circuit. This is why the components don't appear in the layout drawing depicted in figure 4.36. Photo in figure 4.42 includes the complete finalized components. Measurement results are discussed in the next section.

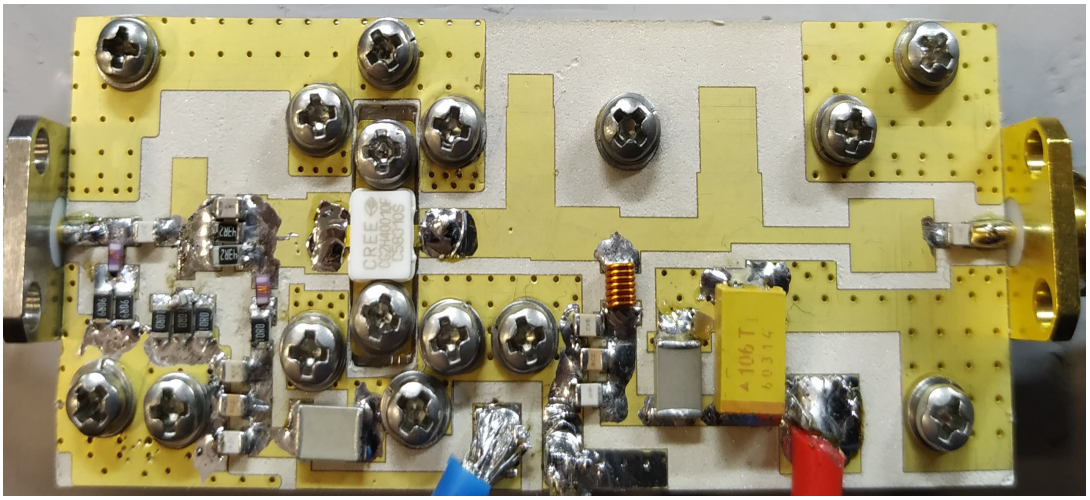


Figure 4.42: Prototype 2 assembled photograph

4.2.5 Prototype 2 Results

The small signal measurements are performed at 28V 150 mA bias conditions. Simulated and measured results of return loss and gain are provided in figures 4.43 and 4.44.

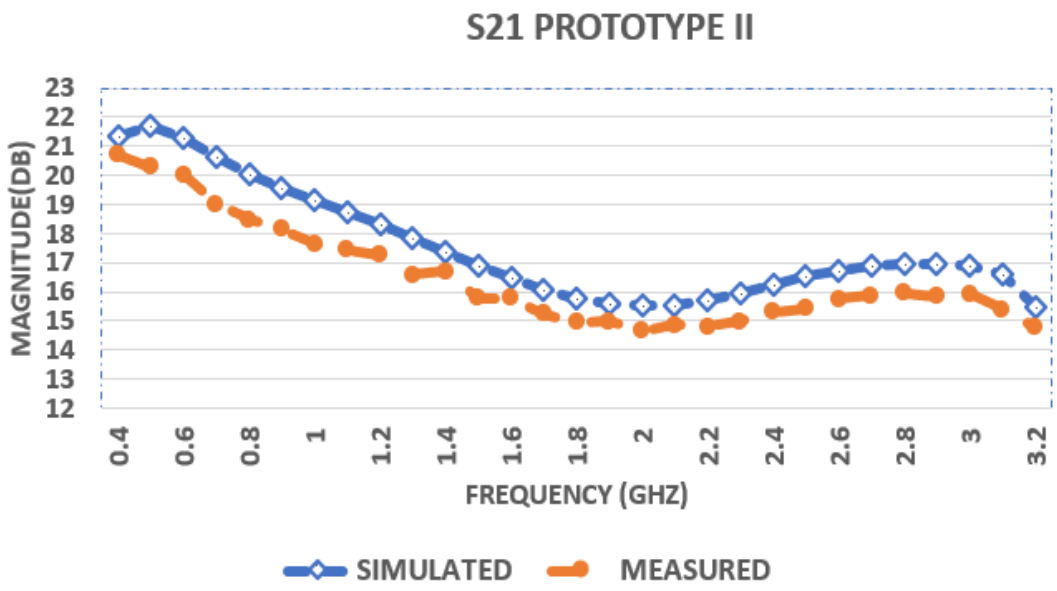


Figure 4.43: Measured and simulated gain of prototype 2

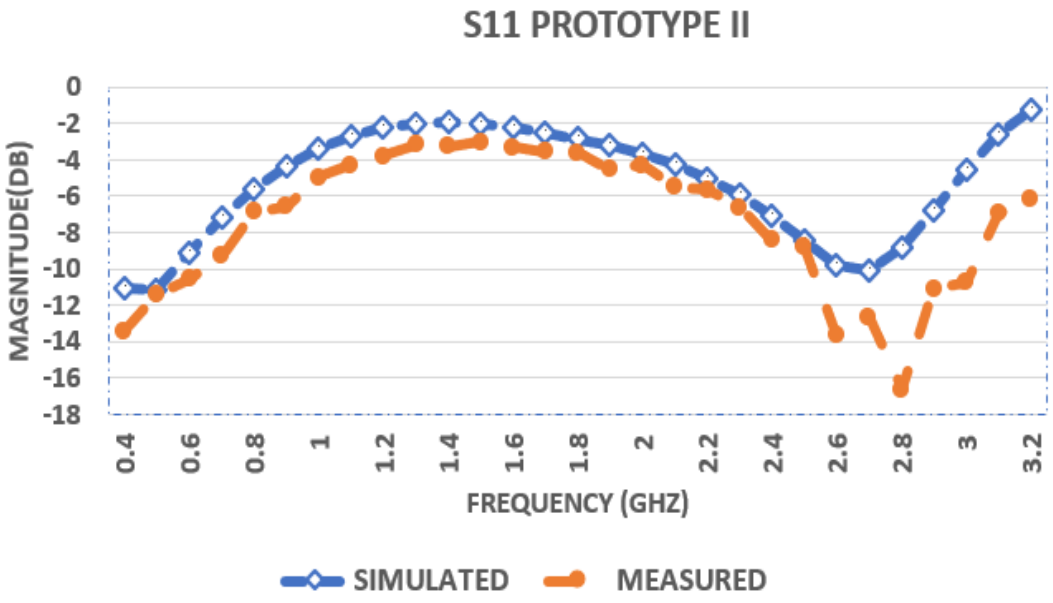


Figure 4.44: Measured and simulated return loss of prototype 2

As the figures 4.43 and 4.44 suggest, minimum of 3 dB return loss and 14.5 dB small-signal gain are achieved. The gain flatness of the prototype II is not considered as a big deal, as long as it doesn't cause stability problems. On the other hand, the excessive gain at the begininng of the band could be tuned out for flatter gain response by optimizing the input circuit series and shunt components. One more thing to note is that while measured and simulated gain agree upto 1 dB deviation as in prototype I, the return loss measurement results deviate from simulation more than in the case of prototype I. Indeed, it was expected due to more stabilizing resistors in series. Because the resistor s-parameters were not available, their parasitics remain excluded from the simulations. More stabilizing resistors than prototype I were employed to enhance the durability against power dissipation.

The large signal measurements were performed using the same test equipment shown in figure 4.29. The saturated output power and gain are plotted in figure 4.45. The saturation points are determined as not to exceed 5 dB compression. In figure 4.46, the gain compression and efficiency are plotted for the saturated output power levels of 4.45.

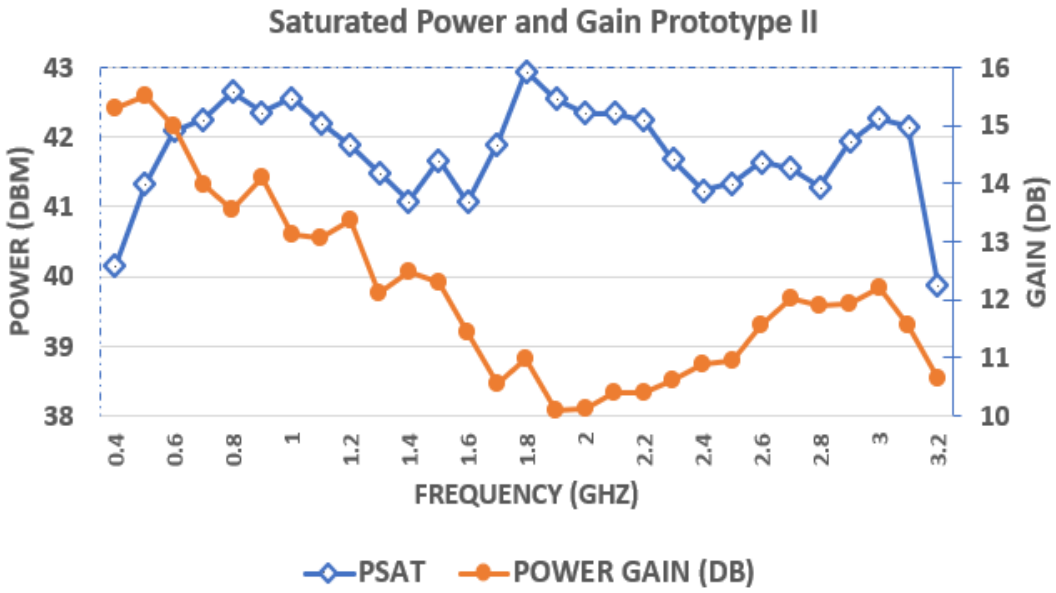


Figure 4.45: Measured saturated output power and gain of prototype II

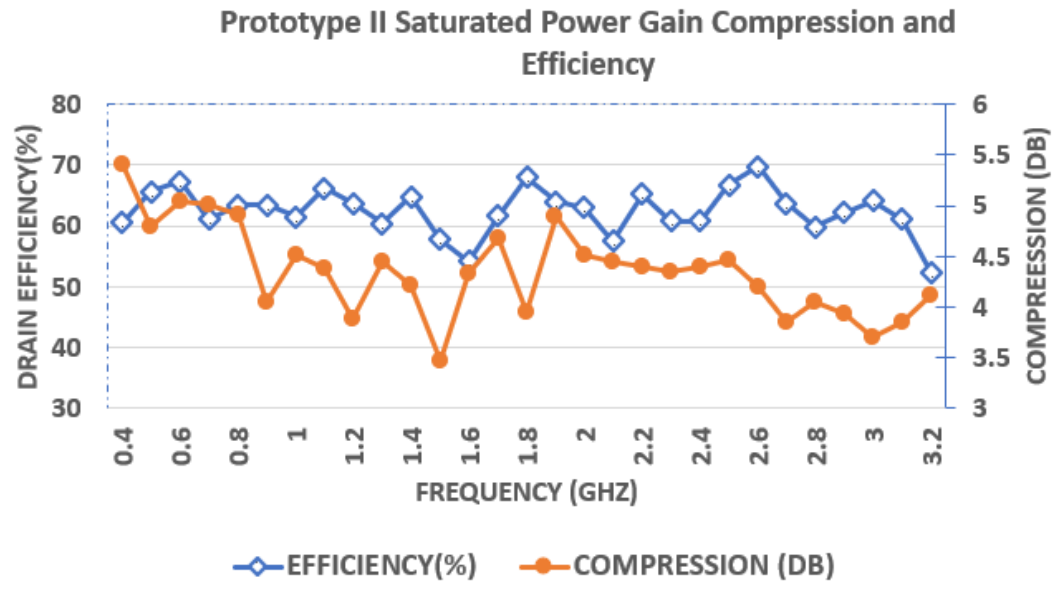


Figure 4.46: Measured saturated gain compression and drain efficiency of prototype II

Minimum efficiency of 53% is achieved over the entire three-octave band. Maximum efficiency of 69.8% is obtained. The maximum gain compression at saturated power is 5.4 dB at 0.4 GHz. Since the measurements are done using an automated setup, 0.4 dB error is made at one measurement point. Minimum saturated output power of 39.88 dBm is obtained at 3.2 GHz, which was an expected derating behaviour by the output impedance analysis given in figure 4.41. Maximum saturated output power is observed as 42.95 dBm with 4 dB compression at 1.8 GHz. The average efficiency is calculated as 62.45%. The average output power is 41.85 dBm. Average values are computed with equal weighting of frequency points spaced by 100 MHz. Prototype I and II saturated output power, gain compression and drain efficieny results are plotted together in figures 4.47-49.

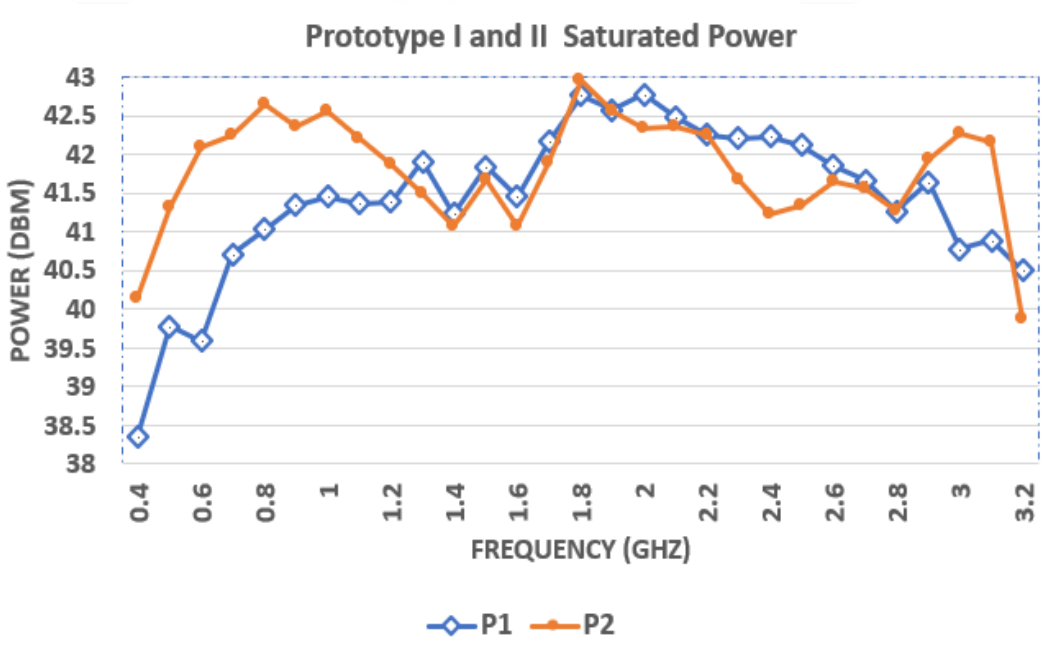


Figure 4.47: Measured saturated output power results of prototypes

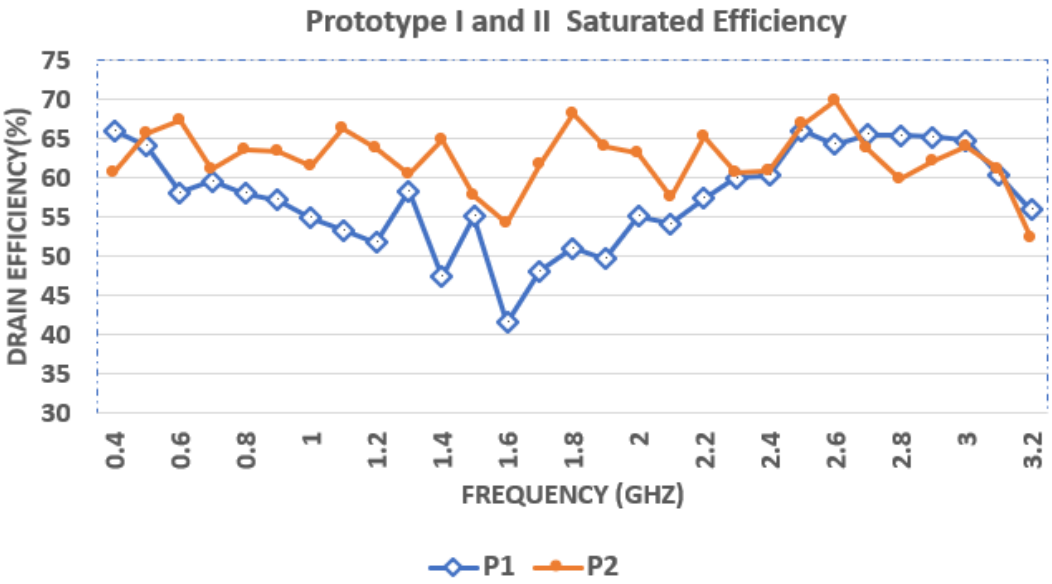


Figure 4.48: Measured saturated efficiency results of prototypes

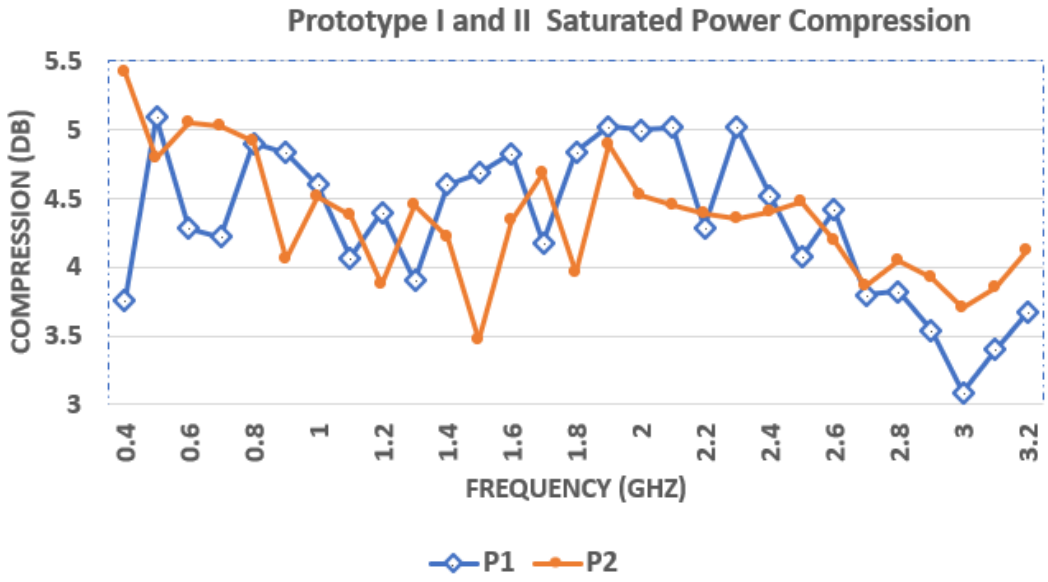


Figure 4.49: Measured saturated power gain compression of prototypes

In figure 4.47, saturated output power is enhanced in the first octave and upto approximately the half of the second octave. This result was suggested by the first and second octave output impedance improvements depicted in figures 4.39 and 4.40. Moreover, there are points in the second and third octave at which there is no power level improvement but there is a significant efficiency enhancement of 15%. Indeed, it is strong evidence that improvements toward NRRCJ design space in harmonics and fundamental are practically useful. Looking at the compression level comparison, similar compression levels are observed. It shows that efficiency improvement is not rooted in overdriving the amplifier. They support the usefulness of the method, as well. It can be concluded that the outcomes get along well with the proposed theory and methodology.

Though there is no linearity promise neither in the saturated operation nor in the NRRCJ approach, a set of measurements are performed with modulated signals. ACLR(adjacent-channel leakage ratio) values are provided to have insight on the linearity performance. Two different signals were used. First one is a WCDMA signal of 5 MHz bandwidth with 10 dB PAR(peak-to-average ratio). Latter is an LTE signal of 10 MHz bandwidth having 11 dB PAR. Measurement results are depicted in figures 4.50-57. Mesaurments are conducted at 30 dBm average carrier power. Figures are presented in photograph format due to lack of neccessary equipment and time constraints. PA output is attenuated by 50 dB. 0.5, 0.9, 1.8 and 3 GHz are selected as carrier frequencies. Worst case ACLR value is found to be 36.7 dBc from the high side of 1.9 GHz carrier LTE signal. The results are promising in terms of linearity. On the other hand, to justify linearity, further measurments should be performed such as EVM, IMD (intermodulation distortion). These values can be improved by the DPD(digital pre-distortion) methods, as suggested in the works like [32].

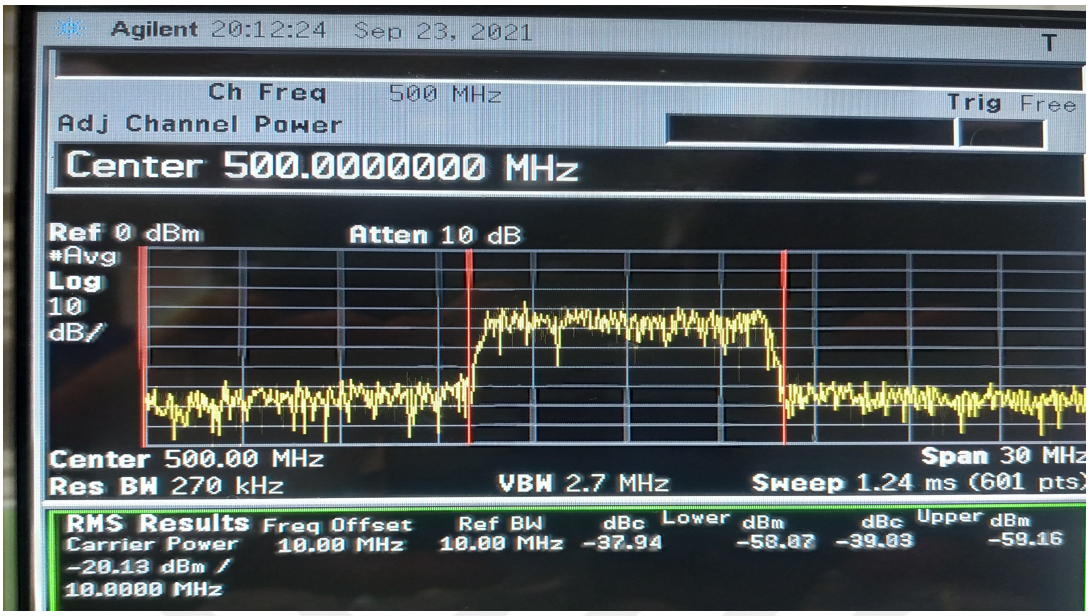


Figure 4.50: Measured ACLR with 500 MHz LTE

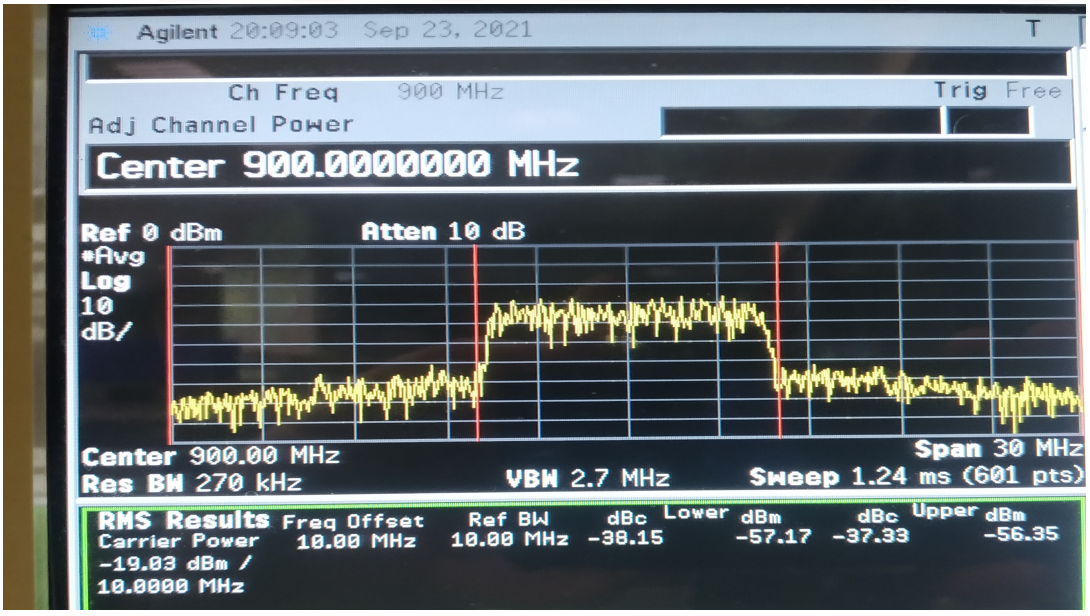


Figure 4.51: Measured ACLR with 900 MHz LTE

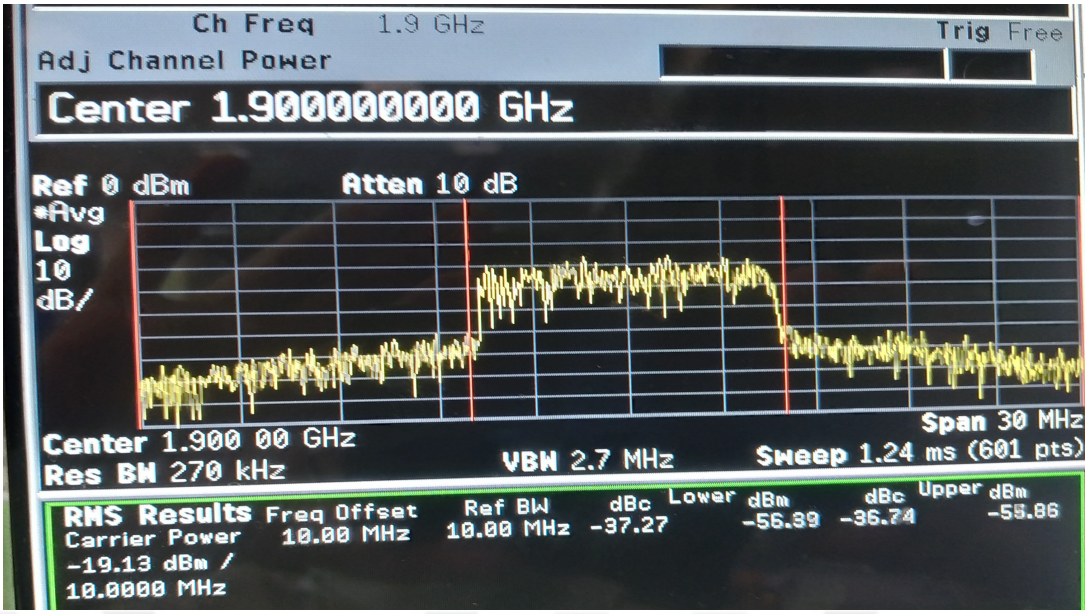


Figure 4.52: Measured ACLR with 1900 MHz LTE

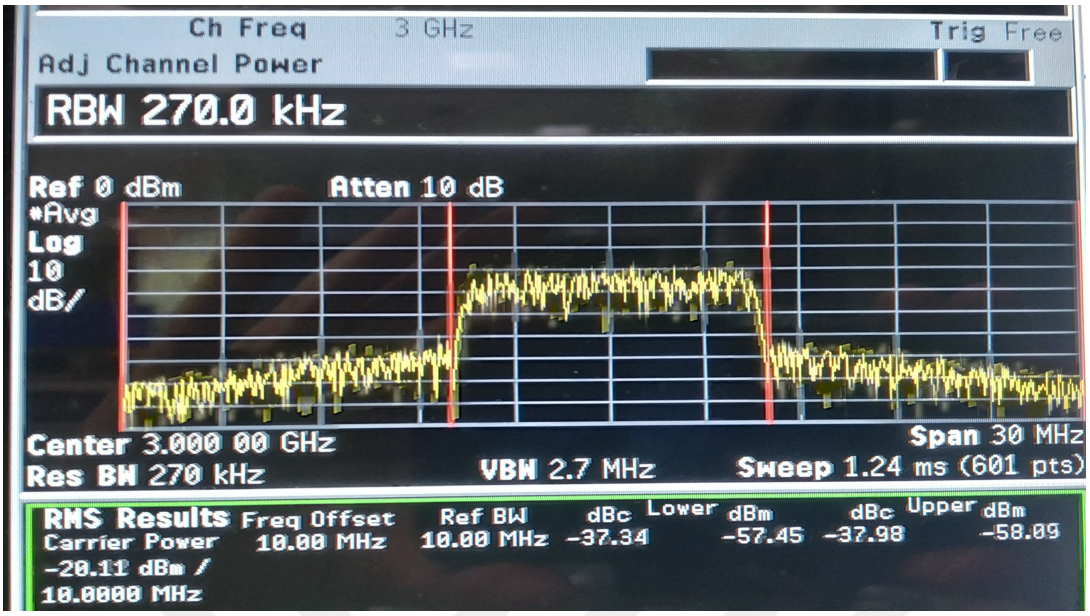


Figure 4.53: Measured ACLR with 3000 MHz LTE

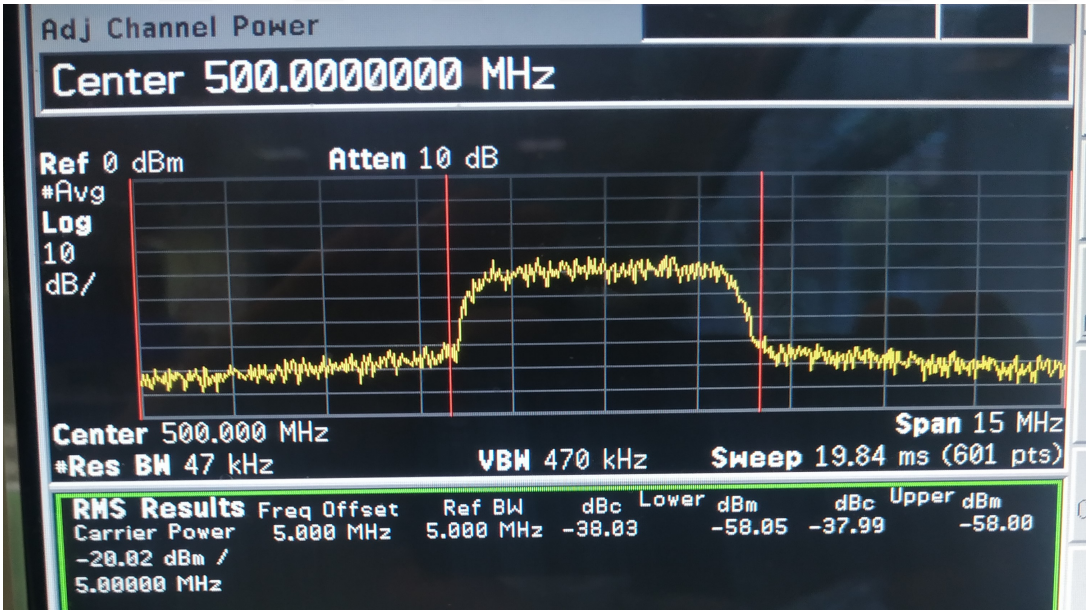


Figure 4.54: Measured ACLR with 500 MHz WCDMA

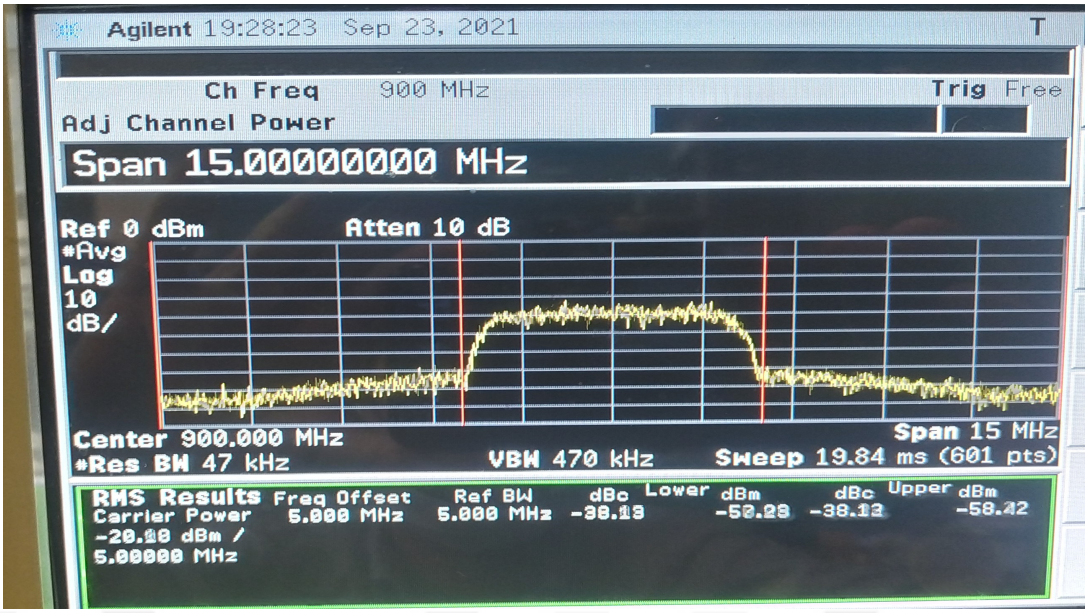


Figure 4.55: Measured ACLR with 900 MHz WCDMA

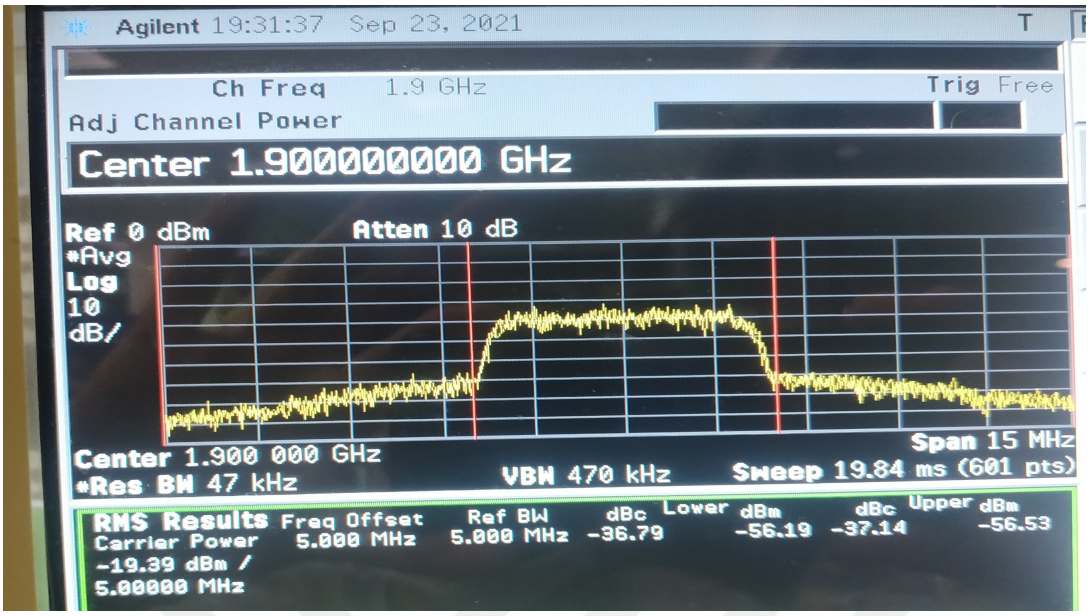


Figure 4.56: Measured ACLR with 1900 MHz WCDMA

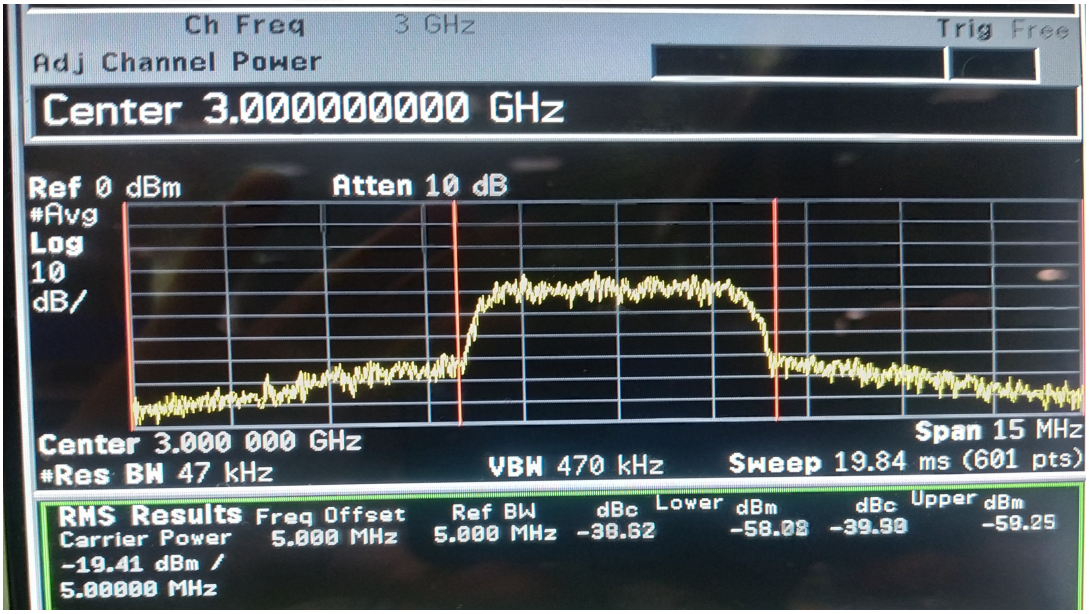


Figure 4.57: Measured ACLR with 3000 MHz WCDMA

CHAPTER 5

CONCLUSIONS

5.1 Comparison with Other Works

Obtained results of the final prototype are compared with the similar studies from the literature. The compared studies use the first generation version CGH40010F. Indeed, one of the novel aspects of this thesis is the usage of second generation version, CG2H40010F, and its large-signal model. Though there is extensive research using the same device, the table presented in [32] is taken as a reference. The selected works for comparison are [41, 43, 39, 44, 45, 46, 47, 48, 49, 42, 50, 40, 51, 32]. General paramters are tabulated in table 5.1.

The table shows that the proposed PA has the highest fractional bandwidth among compared studies together with [42]. The saturated output power is comparable and greater than some of them. The drain efficiencies may seem smaller than other PAs but it should be noted that the bandwidth and efficiency has a trade-off relation. In addition, in works of [42, 40] measurments were taken at gain compression levels of greater than 6 dB. In the work of [32], theoretical formulations suggest changing drain supply voltage but the measurements were takan at constant supply voltage. On the other hand, the proposed PA is one of the smallest size with 65.3x27.9 mm among the other studies. With an effort to have better input VSWR, that compact size makes the PA practically useful in driver stages, as well. The ACLR measurments obtained at worst case 36.7 dBc, is comparable to the those in [32] at 10 MHz offset from LTE carrier. It outperforms [39] in terms of ACLR values.

Table 5.1: Comparsion table

Reference	Frequency Band (GHz)	FBW(%)	Drain Efficiency(%)	Psat (dBm)
[42]	2.2-2.8	24	65.9-79.7	41-43
[44]	1.6-2.2	32	55-68	40-41
[40]	2.85-4.25	39.5	58-78	40.6-41.9
[45]	1.5-2.5	50	60-70	39.5-40.5
[46]	1.3-2.4	59	63-72	40.1-41.2
[47]	1-1.9	62	60-70.9	40.1-42.6
[48]	0.8-2.4	100	61-86	39-41.7
[49]	0.4-2.3	140.7	62.3-80.5	39-42
[50]	0.8-3.05	117	57.4-79.1	40-43.16
[43]	0.5-4	155	60-71	40-42.8
[51]	1.2-3.6	100	60-72	40-42.2
[41]	0.5-2.3	128.5	60-81	39.2-41.2
[52]	1.2-3.6	100	63-73	40.5-42.7
[33]	0.5-3.25	146.7	60-70.1	39.1-41.75
This work	0.4-3.2	155	53-69.8	39.88-42.95

The measured power gain of minimum 10 dB saturated gain over the entire bandwidth is also a comprable result with the similar broadband designs reported in [49, 42, 40, 32]. More specific comments can be made for those broadband designs. In [49], an average drain efficiency of 67.1% is reported which is 62.45% in our case over a wider bandwidth. The gain compression data was not provided. Though the dimensions are not reported, with a scalar look at design photos, our proposed PA has smaller dimensions. In work of [42], a comparable size of 36x60mm PA over a three-octave band is reported. However, the gain compression is not presented. The ACLR is reported better than 33 dBc, which we slightly outperform with 36.7 dBc. In [40], the dimensions are obviously greater than this thesis work. The large dimensions may greatly deduce the usefulness of the design in the applications.

All in all, the important point in our design practice was to introduce the NRRCJ impedance space which provides a compatible method within usage of real applications. In terms of detailed theoretical analysis and implementation procedure, this work contributes one of the well-organized designs among the reported studies.

5.2 Conclusions

The major goal of this thesis work was to present a broadband design methodology while maintaining efficiency and output power at reasonable levels. The second harmonic manipulation method, in particular, a modified class-J method is chosen as the tool to realize this goal. In pursue of develeoping a systmetic approach, a modification to the existing appraoches is proposed. The iterative design equations are derived and mathematical analysis of the parameters are investigated. A practical design procedure is suggested to utilize NRRCJ impedance space in enhancing the power and efficiency. Two prototypes were built to show the validity of the proposed methods. Output impedance matching of the two prototypes are studied in detail.

The evidence which supports the usefulness of the method is provided. The outcome of the experiments are analyzed with respect to theoretical expectations. It is shown that the presented 3-octave PA design scheme using NRRCJ approach enhances the performance. The theory and experiments resulted in good agreement. The final prototype achieved, efficiencies of $53\% - 69.8\%$ with an average value of 62.45% over the entire 400-3200 MHz bandwidth. The FBW(fractional bandwidth) of the design is 155%. The saturated output power varied in between 39.88-42.95 dBm with an average value of 41.85 dBm. The ACLR measurements performed at 10 dB back-off, at 30 dBm, showed promising performance, which is better than 36.7 dBc. In addition, the comparisons provided above this section suggest the promising results of the PA.

By the making use of the inspirational works [32, 21], an alternative approach is contributed to the literature. Based on the facts presented in this thesis work, the NRRCJ modification and suggested practical methods are proven to be succesfull. The future work ideas related with the subject is presented at the end section.

5.3 Future Work

Although the author is satisfied with the results obtained through the proposed theory and practical methodology, some future work ideas can be summarized as follows.

- The neglected third-harmonic effects can be analyzed in depth.
- An additional modification to remove the reactive third harmonic can be proposed.
- The mismatch tolerances from selected impedance space points can be analyzed.
- Due to theoretical implications and assumptions, NRRCJ impedance space lie always in the region with real part smaller than $R_{opt,A}$. In this respect, a more inclusive modification or analysis can be proposed to encapsulate the impedances of real part greater than $R_{opt,A}$.
- The well-known knee effect can be included into waveforms to observe the effects on the impedance space.

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