RF INTEGRATED CIRCUITS FOR UHF TRANSCEIVERS IN BULK AND SOI CMOS

by

Ahmet Tekin

A thesis submitted to the graduate faculty
in partial fulfillment of the requirements for the degree of
MASTER OF SCIENCE

Department: Electrical Engineering
Major: Electrical Engineering
Major Professor: Dr. Numan Dogan

North Carolina A & T State University
Greensboro, North Carolina
2004

School of Graduate Studies
North Carolina Agricultural and Technical State University

This is to certify that the Master's Thesis of

Ahmet Tekin

has met the thesis requirements of
North Carolina Agricultural and Technical State University

Greensboro, North Carolina
2004

Committee Member	Major Professor
Committee Member	Department Chairperson
	Dean of Graduate Studies

DEDICATION

To my father; my mother; my sisters; my brother; my patient wife, Zeynep; and my lovely daughter, Esma, for being such a wonderful family and for always supporting me.

BIOGRAPHICAL SKETCH

Ahmet Tekin was born in Kayseri, Turkey, on December 20, 1979. He obtained his undergraduate degree in Electrical Engineering from Bogazici University, Istanbul, Turkey, in 2002. He joined the Department of Electrical and Computer Engineering at North Carolina A&T State University, Greensboro, North Carolina, in Fall 2002 to pursue a Master of Science degree in Electrical Engineering. Since July 2002, he has worked at the RF Micro Lab at North Carolina A&T State University as a research assistant on the NASA Transceiver project with Dr. Numan Dogan.

ACKNOWLEDGEMENTS

I would like to thank all the faculty and staff of the Department of Electrical Engineering at North Carolina A&T State University, Greensboro, North Carolina, for their help and encouragement in my pursuit of graduate education. I would especially like to thank Dr. Numan Dogan for giving me an opportunity to work on this project and for always supporting me. I would also thank to the other project members, Douglas Huang, Ertan Zencir, Burak Cetin, Rodney Broussard, John Cothern and Kennedy Cherviyot for being such encouraging partners. I would like to thank John Domiano of NCSU for helping with hot-chuck probe measurements, Jefferum Jones and Jaret Liner of RF Microdevices for helping with PA measurements and DC probing, Chris Foye of RF Microdevices for VCO spectrum measurements and Arlene Williams of RF Microdevices for wirebonding my chips. I thank you all very much.

Finally, I would like to give most thanks to the One that has brought me into existence so that I can think and explore.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

SYMBOL	DESCRIPTION
PA	Power Amplifier
PLL	Phase Locked Loop
MOS	Metal Oxide Semiconductors
SOI	Silicon on Insulator
RF	Radio Frequency
CMOS	Complementary Metal Oxide Semiconductor
IC	Integrated Circuit
BGR	Band-gap Reference
VCO	Voltage Controlled Oscillator
ESD	Electrostatic Discharge
PCB	Printed Circuit Board
LLC	Leadless Carrier
IM	Inter Modulation
UHF	Ultra High Frequency
PAE	Power Added Efficiency
PN	Phase Noise
PFD	Phase Frequency Detector
CP	Charge Pump
LF	Low Pass Filter

ABSTRACT

Tekin, Ahmet. RF INTEGRATED CIRCUITS FOR UHF TRANSCEIVERS IN BULK AND SOI CMOS. **(Major Advisor: Dr. Numan Dogan),** North Carolina Agricultural and Technical State University.

This study describes the design implementation and testing of some of the RF front-end blocks of a 435-MHz UHF transceiver.

A 435-MHz 24-dBm class-AB power amplifier and another 435-MHz 22.8-dBm Class-F power amplifier in 0.5-μm standard CMOS were designed, implemented and tested targeting the highest possible output power and efficiency levels. A bandgap based constant-current, constant-voltage multiple bias circuit was designed, implemented and tested to distribute a range of bias conditions required by the blocks of an integrated receiver. An 800-MHz, -121 dBc/Hz at 600 KHz fully on-chip VCO and another 1.736 GHz low power, low phase noise LC VCO in 0.35-μm SOI CMOS were designed, implemented and tested. A 434-MHz low-power, fully-integrated, type-2 4^{th}-order quadrature phase locked loop (PLL) was designed and simulated in a 0.35 μm Silicon-on-Insulator (SOI) CMOS process.

Most of the designs have successfully been tested and the requirements on the performance parameters were fulfilled to a great extent.

CHAPTER 1

INTRODUCTION

As wireless communication advances into the third generation, space communication marches toward the next generation as well. Since power consumption is the primary concern in space communication applications, this work is dedicated to designing low-power receiver front-end blocks for future Mars missions.

Figure 1.1 illustrates a communication link being developed between the orbiter and the lander as the lander detects the orbiter rise more than 20° above the horizon. Because of the motion and location of the orbiter, the received signals (on both the orbiter and the lander) vary in strength and Doppler shift. Since both the maximum signal strength and the minimum Doppler shift take place when the orbiter is directly above the lander, a variable data rate is used in the transceiver scheme. A detailed derivation of the specifications can be found in the National Aeronautics and Space Administration (NASA) and Jet Propulsion Laboratory (JPL) *InterPlanetary Network (IPN) Progress Report* [1].

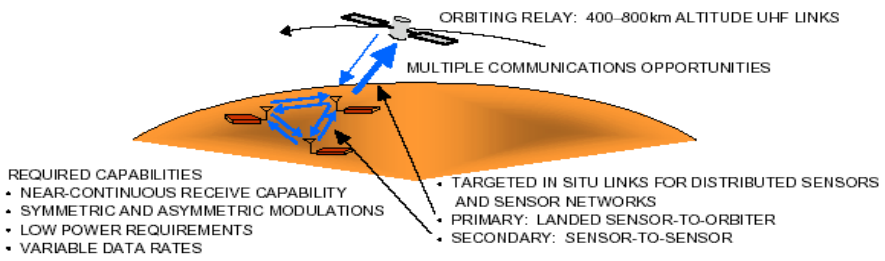


Figure 1.1 Communication links between Martian orbiter and landers

The block diagram of the 435-MHz, Digital Low-IF (1-MHz), Double Differential Phase Shift Keying (DDPSK) Transceiver, which is designed to enable the sensor-to-sensor and sensor-to-orbiter communication of this Mars mission, is given in Figure 1.2. This work tries to address low power solutions for the transceiver blocks given in dashed boxes, namely, Power Amplifier (PA), Bias Distribution Network and Quadrature Phase Locked Loop (PLL).

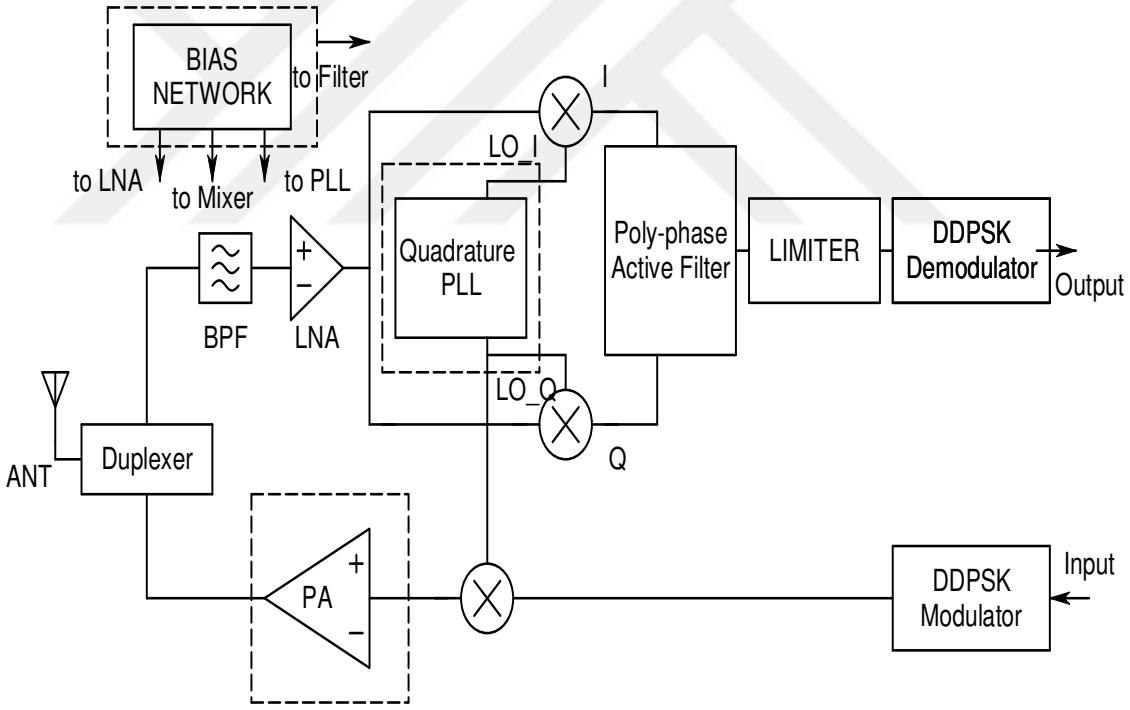


Figure 1.2 Block diagram of 435-MHz Digital Low-IF (1-MHz), DDPSK (DoubleDifferential Phase Shift Keying) Transceiver

The chapters are organized as follows. In Chapter 2, the design, the implementation and the testing of Power Amplifiers in 0.5-μm *Agilent* standard CMOS are discussed. Chapter 3 presents the design, the implementation and the testing of a

band-gap based constant-voltage constant-current bias distribution network in 0.35-µm *Honeywell* SOI-CMOS. The design, implementation and testing of 868-MHz and 1.736-GHz Voltage-Controlled Oscillators (VCO) in 0.35-µm *Honeywell* SOI-CMOS are presented in Chapter 4. The design and implementation of a 434-MHz, 4^{th} order, low power, fully-on-chip Quadrature PLL in 0.35-µm SOI CMOS is discussed in Chapter 5. Chapter 6 presents the conclusions.

CHAPTER 2

DESIGN, IMPLEMENTATION, AND TESTING OF RF POWER AMPLIFIERS

2.1 Introduction

Integration of most of the front-end blocks into a single chip CMOS transceiver has been achieved with comparable performance to those designed in GaAs and other bipolar processes. However, it remains a challenge to integrate a Power Amplifier into a single chip transceiver in standard CMOS. This is mainly due to the poor power capability and very low efficiency of a CMOS Power Transistor. The aim of this work was to design power amplifiers in a standard CMOS process with reasonable performance with a limited number of pads and low cost standard packaging techniques.

This chapter is organized as follows. The design challenges and important considerations of a PA design with a standard CMOS process are discussed in section 2.2. In section 2.3, a 435-MHz 24-dBm class-AB Power Amplifier in 0.5-μm standard CMOS is presented. Another 435-MHz 22.8-dBm Class-F Power Amplifier, which was fabricated on the same die, is presented in section 2.4, and section 2.5 is the conclusion.

2.2 General Design Considerations for CMOS PA Design

In a power amplifier design task, the best way to achieve high output power without degrading the efficiency of the amplifier is to use high supply voltages [2]. However, this conflicts with the low breakdown-voltage of standard CMOS transistors.

V_{dd} is limited to 2.5 V for this receiver design. Another important consideration for CMOS transistors is the high knee voltage that limits the maximum device current. Besides these two major considerations, electron migration, saturated drift velocity, critical field, parasitic drain and source resistances limit the maximum output power and efficiency at high current levels [3]. In order not to degrade the efficiency of the designs, off-chip passive components were used for matching. This also provided the opportunity to better evaluate the performance of output transistors by changing the output termination. The second amplifier operating in class-F mode has a fully on-chip version to measure the performance of the passive components integrated in a 0.5-µm CMOS process.

Given the supply voltage of 2.5 V, the highest possible output power was targeted without deviating from optimum efficiency levels. It seems feasible to obtain high output power by passing a very large current through a large output transistor. However, after a certain point, the device transconductance saturates and the efficiency of the amplifier starts to decrease considerably due to the second order effects as mentioned earlier. Losses associated with the high matching ratio are among the other factors responsible for degrading efficiency. Moreover, as the size of the output transistor increases, it becomes more difficult for the preceding stage to drive this output transistor.

2.3 A 435-MHz 24-dBm Class AB Power Amplifier in 0.5-µm CMOS

For the first design, Class-AB was chosen as the mode of operation. With a slight sacrifice in linearity, class-AB amplifiers achieve higher efficiency than pure class-A

amplifiers. Class AB amplifiers also yield inherently higher output power levels and higher linearity than class E and class F amplifiers.

2.3.1 Design and Simulations

To find the optimum device size for the output transistor, the output power and efficiency at the load of the circuit (given in Figure 2.1) were simulated by matching a 50-Ω load to optimum transistor resistances ranging from 3 Ω to 12 Ω with the corresponding transistor sizes. Figure 2.2(a) shows the simulation results of output power and efficiency for different output transistor widths with a gate length of 0.5 μm. The optimum output transistor size was chosen to be 4 mm with 160 fingers, which results in the transistor resistance of 7 Ω.

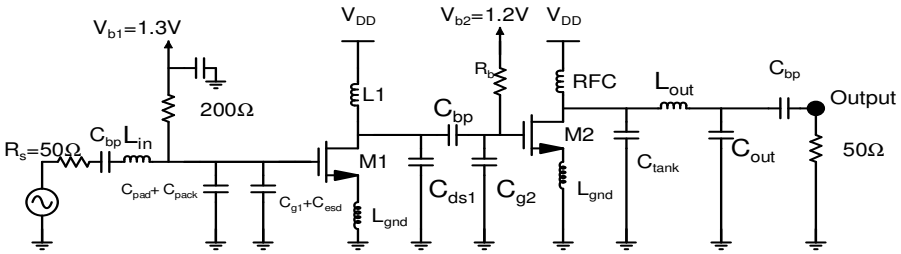


Figure 2.1 Schematic of the design including the parasitics

Device and package parasitics were included in the schematic. As shown in Figure 2.1, the input matching network is formed by combining driver stage gate capacitance, ESD parasitic capacitance, pad capacitance, package parasitic capacitances and the off-chip inductor, L_{in}. The package parasitic capacitance is assumed to be 900 fF. The total parasitic capacitance of 3.17 pF, together with the off-chip inductor of 31.7 nH,

matches 200-Ω off-chip resistance to a 50-Ω source resistance at the frequency of 435 MHz. Thus, 50-Ω input matching occured only at the frequency of interest. Ground inductance of 0.6 nH was assumed at the source of both transistors M1 and M2 in simulations. The driver stage drain inductor L1 of 10 nH was arranged to tune out the gate capacitance of the output transistor, M2, and drain to source capacitance of the driver transistor, M1. The driver stage operates at Class A mode to fully drive the output stage. The width of the driver transistor, M1, was selected to be 400 μm with minimum gate length. A π matching network at the output was used to match the optimum transistor resistance to a 50-Ω load. The capacitor C_{tank} at the drain of the output transistor, M2, together with the C_{DS} of this transistor served as a tank to pose low impedance to the third order content of the signal [2]. The values of these matching elements were chosen to be C_{tank} = 52 pF, L_{out} = 5.9 nH and C_{out} = 19.8 pF to match 7 Ω transistor output resistance to a 50-Ω load. All simulations were done in *Spectre RF* of *Cadence*. Simulated output power and efficiency plots for different supply voltages are shown in Figure 2.2(b).

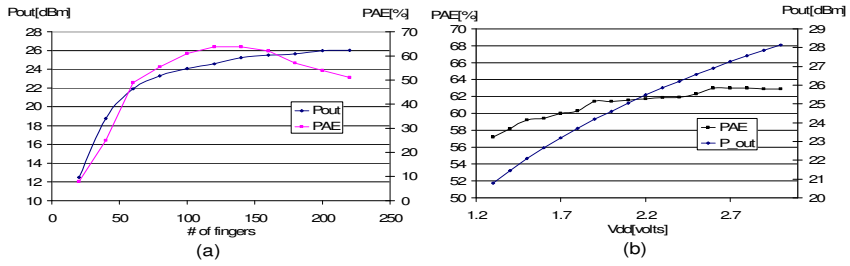


Figure 2.2 (a) Simulated output power and efficiency for different output transistor sizes; (b) Simulated output power and efficiency for different supply voltages

Output power levels, at different frequencies, are given in Figure 2.3(a) as the input of the amplifier is driven with an input power of 5-dBm. Simulated input matching performance is given in Figure 2.3(b). Input return loss (S_{11}) was as low as -17 dB. In simulations, using a supply voltage of a 2.5 V, an output power of 26-dBm with 60% Power Added Efficiency (PAE) was achieved as 7 Ω R_{opt} was matched to a 50-Ω load. However, the best measurement result took place when the 50-Ω load was matched to an R_{opt} of 12 Ω. This is because, in reality, the output transistor is incapable of handling such high currents estimated for 7 Ω R_{opt}. The next section presents the measurement results of the fabricated prototype.

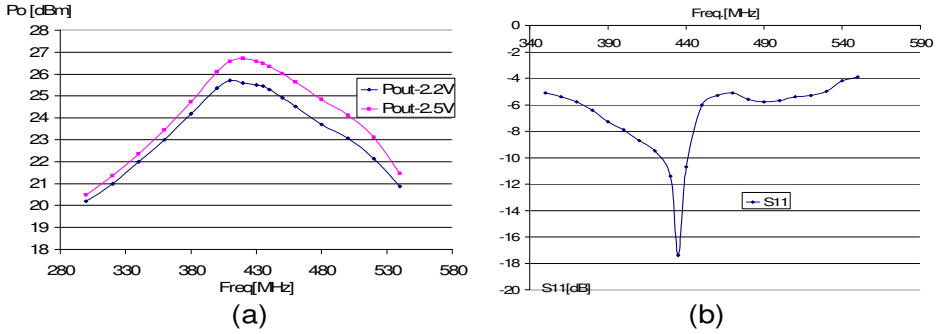


Figure 2.3 (a) Simulated output power with frequency; (b) Input matching (S_{11})

2.3.2 Testing and Measurement Results

The layout of the design, including the other class-F implementation, is given in Figure 2.4 together with the bonding diagram of the pads to a 28 pin package. The layout was drawn in *Cadence Virtuoso Layout Editor*. Details of the layouts of individual circuit elements are given in the Appendix. The design was fabricated in 0.5 μm *Agilent* single-

poly, three-metal standard CMOS process. The microphotograph of the fabricated chip is shown in Figure 2.5.

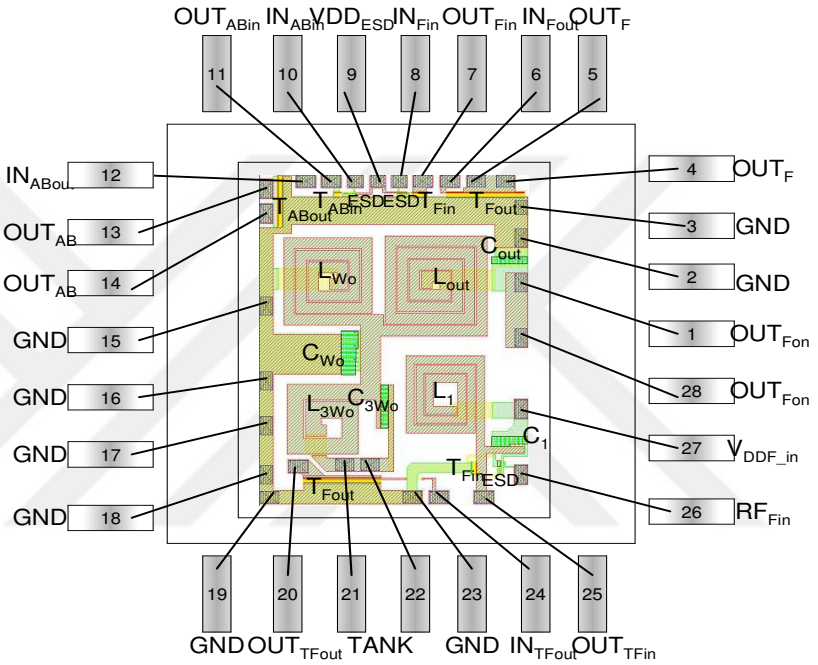


Figure 2.4 Layout and bonding diagram of the design

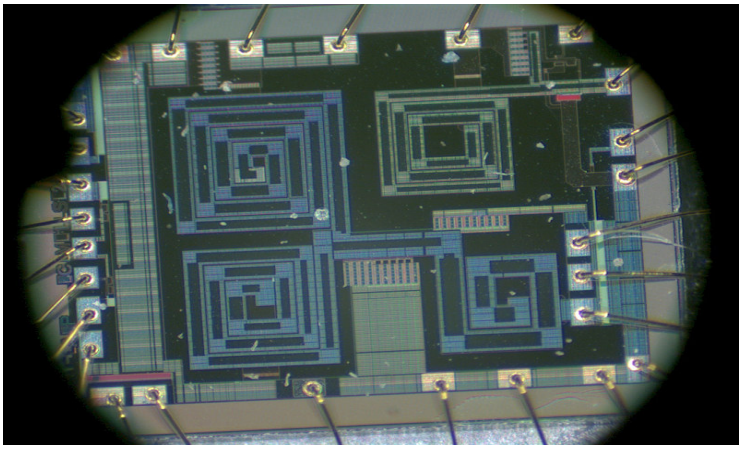


Figure 2.5 Die microphotograph of the design

The dies were tested with both the LLC-28 standard ceramic package and the QFN-28 low parasitic carrier. FR.4 testing boards with 31 mil thickness were designed with *Protel* printed circuit board (PCB) design software. The layouts of the boards are shown in Figure 2.6. Pictures of the fabricated boards, which were used for the testing, are given in Figure 2.7.

The circuit was tuned out for the highest possible output power and efficiency levels. As mentioned earlier, the best performance was observed when a 50-Ω load was matched to a transistor resistance of 12 Ω, rather than to the simulation value of 7 Ω. After this fine tuning, the best performance was observed with the component values of L_{in} = 27 nH + 4.7 nH, L1 = 8.2 nH, C_{tank} = 33 pF (30.5 pF), L_{out} = 4.7 nH + 3.3 nH (8.1 nH) and C_{out} = 20 pF.

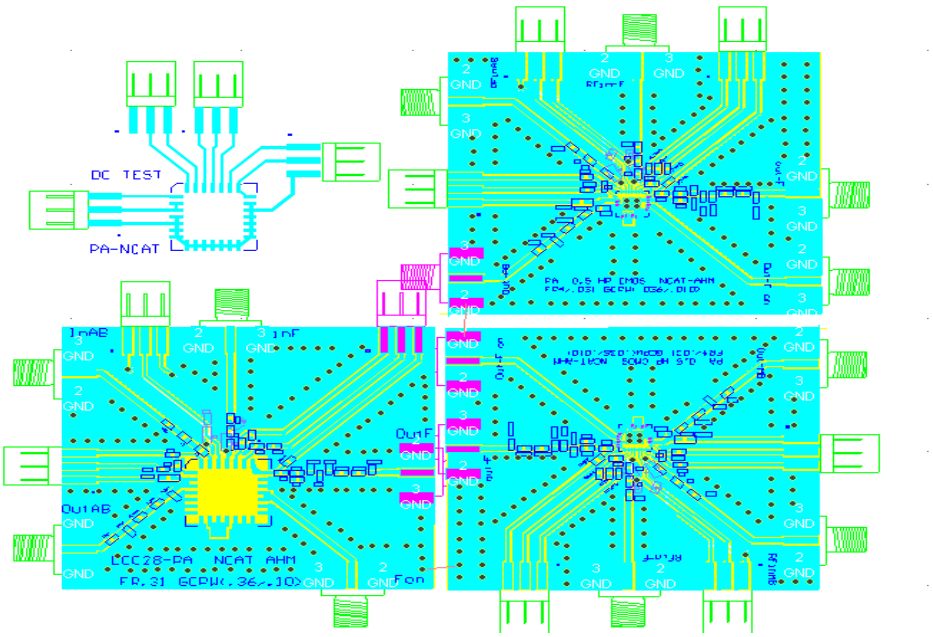


Figure 2.6 Layouts of the boards drawn in *Protel*

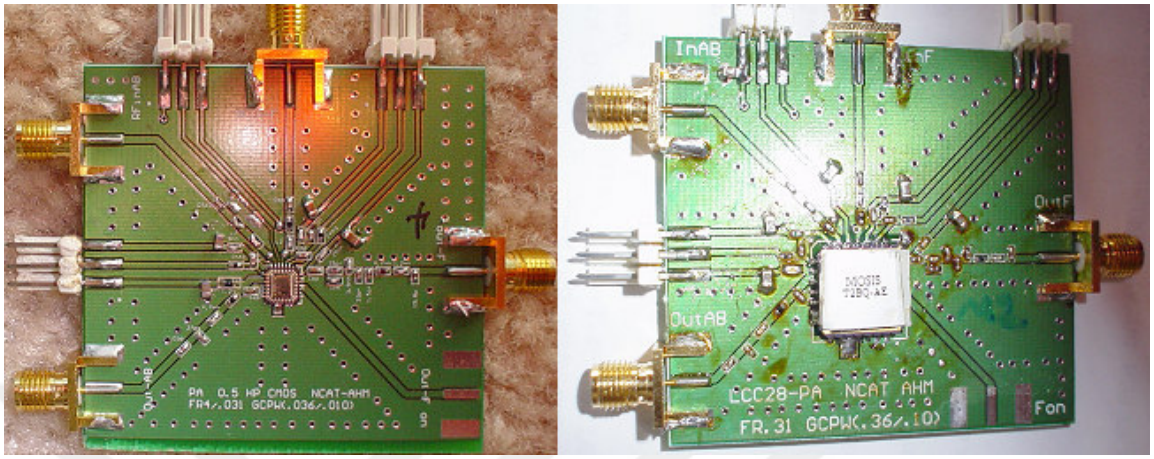
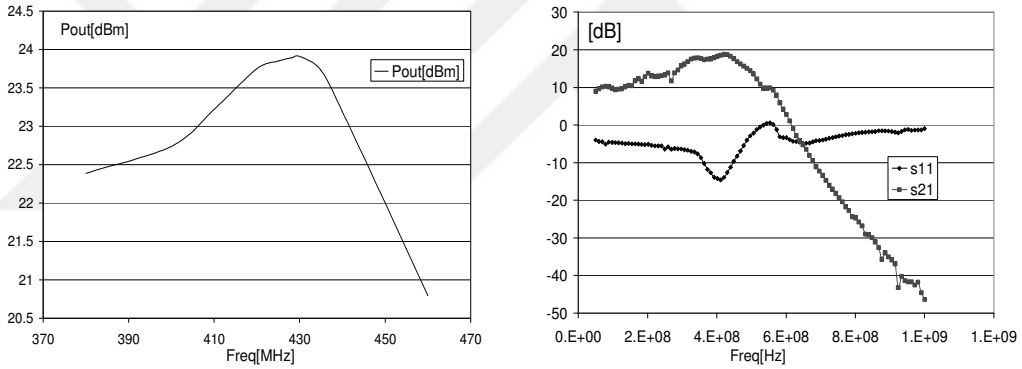


Figure 2.7 Pictures of the testing boards

The test boards with the standard ceramic package yielded slightly higher output power than the ones with the low parasitic RF carrier. The reason might be the that the standard package has a parasitic capacitance value which is closer to the 900 fF value estimated in simulations. This judgment can also be arrived at from the better input matching measured for this package, which showed 2 dB less input return loss (-14 dB vs. -16 dB). Figure 2.8(a) shows the measured output power at a number of frequencies in the band of interest as the amplifier was driven with an input power of 5-dBm.

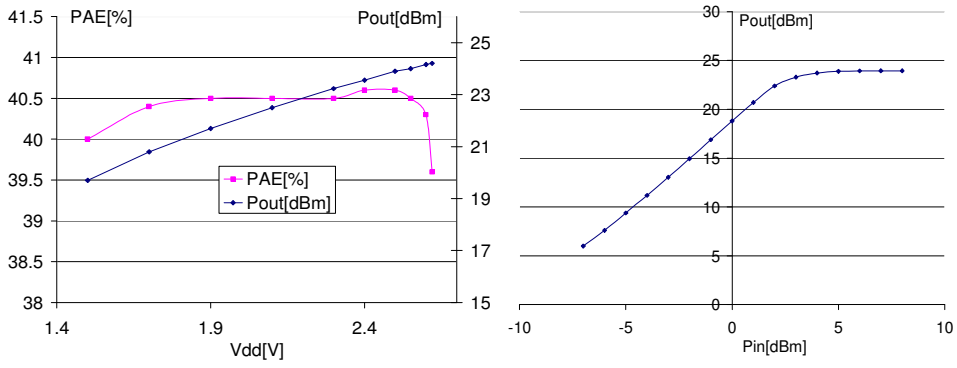
The maximum output power appears at 430 MHz, which is slightly lower than the aimed frequency of 435 MHz. The discrepancy may be due to differences between the values of the available discrete components and the exact values required for the design. A 24-dBm output power was measured for an input power of 5-dBm. The efficiency was about 41% from a 2.5-V supply.

The measured input reflection coefficient (S_{11}) was as low as −16 dB at 430 MHz (Figure 2.8 (b)). Output power and efficiency plots for different supply voltages are given in Figure 2.9 (a). Output power for increasing input power is given in Figure 2.9 (b). Dual Tone analysis was done at a level 6-dB below maximum output power for the linearity measurement [4]. The resulting intermodulation product power (IM) level was at −18dBc.



(a) (b)

Figure 2.8 (a) Output power vs. frequency; (b) S_{11} and S_{21} from network analyzer



(a) (b)

Figure 2.9 (a) Measured output power and efficiency with supply voltage; (b) P_{out} vs. P_{in}

2.4 A 435-MHz 22.8-dBm Class F Power Amplifier in 0.5-μm CMOS

In this second design, the performance of a 435-MHz CMOS Class-F power amplifier is presented. Class-F was chosen as the mode of operation rather than Class-E, since the given supply voltage of 2.5-V would put unbearable stress on the drain of output transistor in the case of a Class-E implementation. It is also practically easier to force non-overlapping voltage and current waveforms at the drain of an output transistor using parallel resonant tanks as in the case of Class-F.

2.4.1 Design and Simulations

The schematic of the two-stage design, including the parasitics, is shown in Figure 2.10. The drawbacks of a standard CMOS process such as high knee voltage, saturated drift velocity, critical field, parasitic drain source resistances and electron migration limit the output transistor size. After some point, the transconductance of this transistor saturates lowering the efficiency of the amplifier considerably. The higher matching ratio requirement would also result in higher losses in the matching network. After successive simulations for different size and different matching ratios, the output transistor width was chosen to be 6000 μm with a minimum gate length of 0.5-μm. This size required the matching of a 6 Ω output resistance to a 50-Ω load. The input transistor width was chosen to be 1000-μm with a minimum gate length to drive the output stage powerful enough for a fast switching action. The input matching network was formed by the combination of a driver stage gate capacitance, ESD parasitic capacitance, pad capacitance, package parasitic capacitances and an off-chip inductor, L_{in}. The input impedance was designed to be 200-Ω, which should be matched to the source impedance

50-Ω. This gives an exact matching only at the desired frequency of 435 MHz. The driver stage drain inductor, L1 of 4.35 nH, and drain capacitor, C1 of 9.89 pF, were arranged to tune out the gate capacitance of the output transistor, M2, and drain to source capacitance of the driver transistor, M1. Only third order harmonic peaking was utilized at the output stage, since incorporating higher order resonant tanks would improve the efficiency only slightly. All resonant tank elements were off-chip discrete components. The component values were L_{3Wo} = 1 nH, C_{3Wo} = 19.88 pF, L_{Wo} = 4 nH and C_{Wo} = 33.47 Pf. A low-pass L- matching network with L_{out} = 5.94 nH, and C_{out} = 19.8 pF was used for output matching.

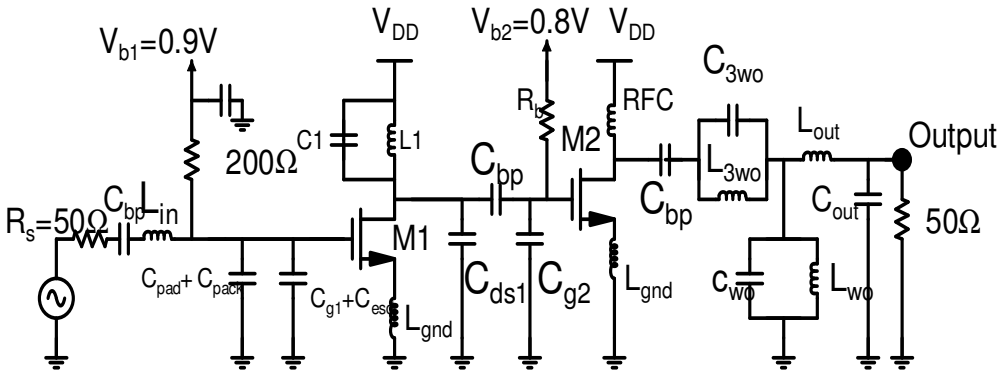


Figure 2.10 Schematic of the design

The simulated output power with frequency is shown in Figure 2.11(a). Input matching of the circuit is shown in Figure 2.11(b). These input return loss values were determined by looking at the voltage and current waveforms at the input node, thereby, finding the input impedance of the amplifier.

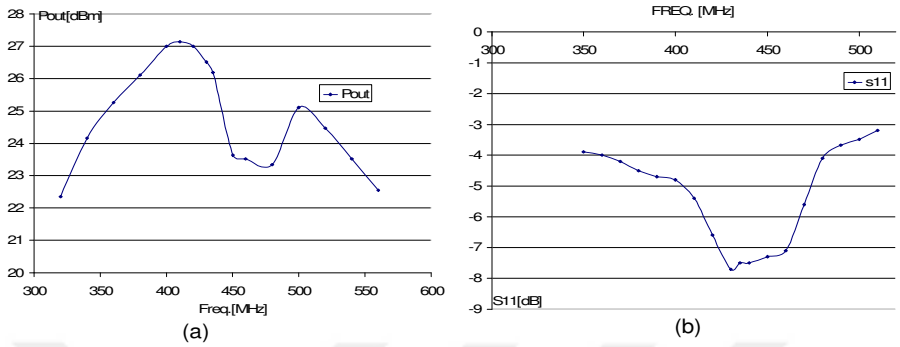


Figure 2.11 (a) Output power vs. frequency; (b) Input matching (S_{11})

The fully on-chip version of this Class-F design was also integrated on the same die. All inductors were realized as on-chip square spiral inductors except the RFC and the input matching inductor, L_{in}. The metal widths of the coils had to be very large to withstand the large current levels. This inevitably resulted in dramatic increase in the parasitics of the inductors, which were responsible for degrading the amplifier's efficiency. Inductor values were estimated by both *Cadence Spectre Inductor Modeler* and *Asitic Inductor Modeler.* The inductance values and properties are given in Table 1. The capacitors were realized as poly-active capacitors.

Table 1. The properties of integrated spiral inductors

Inductor	**Inductance**	**Met.Width**	**Met.Gap**	**Turns**	**Resistance**	**Area(μm^2)**
L1	4.35 nH	60 μm	10 μm	3	2.29 Ω	582 X 582
L_{Wo}	4 nH	80 μm	10 μm	3	1.95 Ω	658 X 658
L_{3Wo}	1 nH	160 μm	15 μm	1.5	0.57 Ω	530 X 530
L_{out}	5.95 nH	80 μm	10 μm	4	2.8 Ω	758 X 758

Ground inductance had a profound effect on the output power and efficiency of the amplifier. This effect was analyzed by recording the efficiency and power levels for different ground inductor values in the simulations. Figure 2.12(a) shows the voltage and current waveforms at the drain of the output transistor with no ground inductance. With the introduction of only 0.6 nH ground inductance, the overlapping area of these waveforms increased significantly, reducing efficiency (Figure 2.12(b)). Figure 2.13 shows the output power and efficiency levels for a range of ground inductance values.

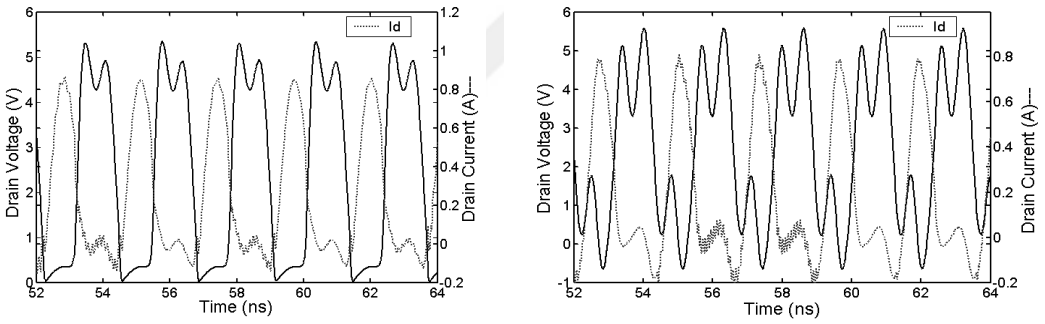


Figure 2.12 (a) Drain voltage and current waveforms with no ground inductance;
(b) Drain voltage and current waveforms with 0.6 nH ground inductance

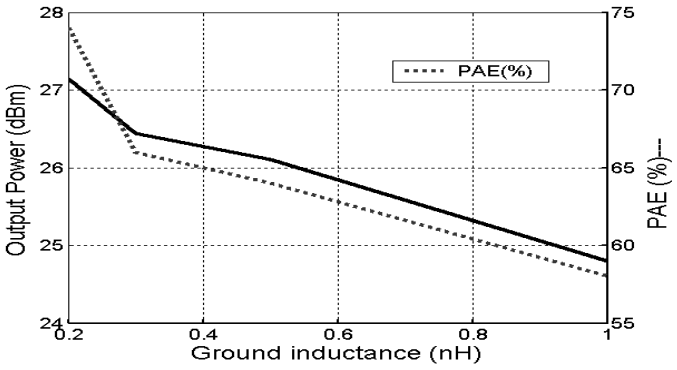


Figure 2.13 Output power and efficiency for different ground inductance values

2.4.2 Testing and Measurement Results

The design was fabricated in 0.5-µm *Agilent* 1P3M standard CMOS process together with the other Class-AB design. The portion of the chip that this design lies on is shown in Figure 2.14(a). The transistors were kept as close as possible to the supply pads. After fine tuning the design, the best performance was observed when a 50-Ω load was matched to a 10-Ω transistor resistance. This required the use of a 7.2 nH inductor for $L_{out,}$ and a 15 pF capacitor for C_{out}. At the input side, a 75-Ω resistance value with a 11.8 nH inductor yielded the best performance. The value of L1 was 4.7 nH, and the value of C1 was 5.2 pF in the measurements. Figure 2.14(b) shows the measured output power at a number of frequencies in the band of interest, as the amplifier was driven with an input power of 5-dBm. The maximum output power appeared at 428 MHz, which is slightly

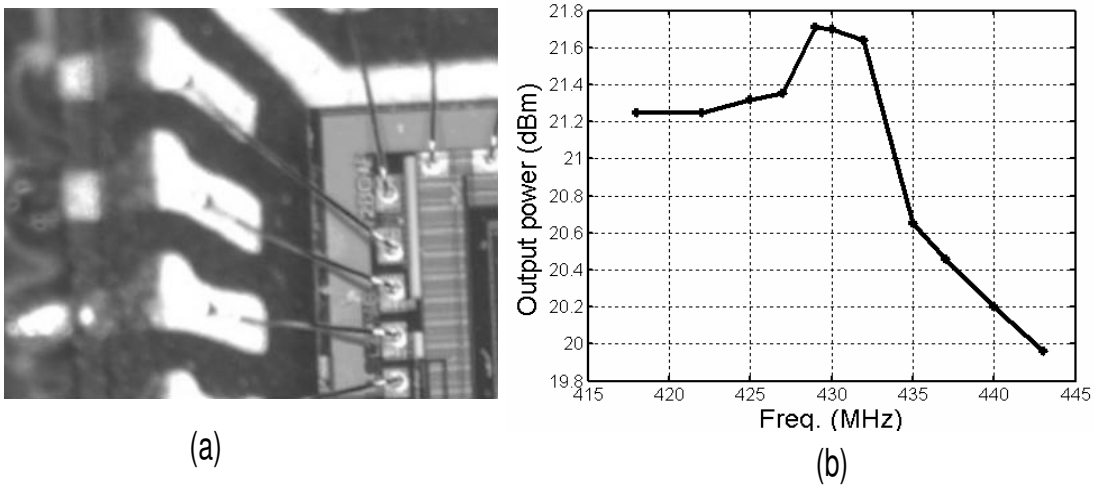


Figure 2.14 (a) Die microphotograph; (b) Measured output power with frequency

lower than the target frequency of 435 MHz. The discrepancy was due to the differences between the values of the available discrete components and the exact values required for the design. An output power of 22.8-dBm was measured for an input power of 5-dBm. Efficiency was about 43% from a 2.5-V supply. The plot of output power with increasing input power is shown in Figure 2.15(a). The measured input reflection coefficient (S_{11}) and small signal gain (S_{21}) are shown in Figure 2.15(b).

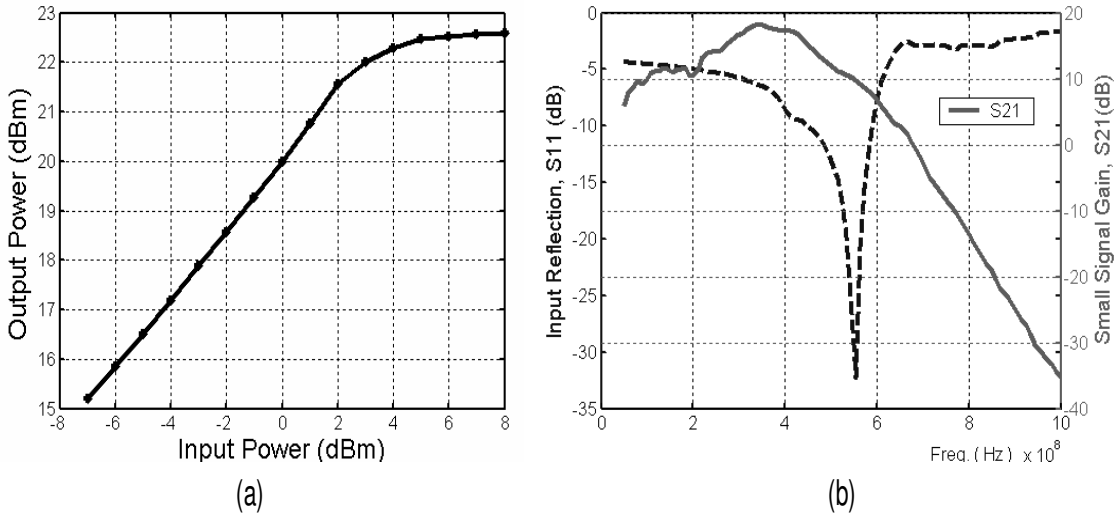


Figure 2.15 (a) Input power vs. output power; (b) Measured input reflection and small signal gain

Dissipating the same amount of power, the fully on-chip version of this design could generate as low as 20-mW output power. Thus, the efficiency of the amplifier was below 10%. This poor performance was due to overestimating the current levels and making the inductors excessively wide.

2.5 Conclusion

A 435-MHz 24-dBm 41% PAE Class-AB CMOS Power Amplifier and a 22.8-dBm 43% PAE Class-F CMOS Power Amplifier, which can both be used in proximity area transceivers, have been presented. The inability of a very large CMOS output transistor to yield high current levels without degrading the efficiency of a power amplifier has been discussed. It has been shown that by careful inclusion of package and other parasitics into the design, the high cost associated with complex packaging techniques, such as chip-on-board, could be avoided.

CHAPTER 3

DESIGN, IMPLEMENTATION AND TESTING OF A BANDGAP BASED MULTIPLE BIAS DISTRIBUTION NETWORK IN 0.35-μm SOI CMOS

3.1 Introduction

As the integration level of mixed signal systems increases, handling different bias requirements of the circuit blocks of these systems becomes more challenging. This chapter presents a solution to distribute a range of constant voltages required by the blocks of an integrated receiver. Using a 2.5 V supply, the circuit generates constant voltages in the range of 0.9 V-1.7 V.

The chapter is organized as follows. Section 3.2 discusses circuit design and simulations. The measurement results are presented in section 3.3. In section 3.4, possible future improvements are discussed. Section 3.5 presents the conclusion.

3.2 Circuit Design and Simulations

In Figure 3.1, the first part of the design is a resistorless bandgap reference circuit [5]. The difference between the diode voltages V_{D1} and V_{D2} across the first differential pair is forced to show up across the other pair by mirroring their supply currents via M6, M7, M8 and M9. By sizing the transistors in differential pairs as $W_{M1}/W_{M3} = W_{M2}/W_{M4} = A$ and arranging the currents to be $I_{diff2} = GI_{diff1}$, this voltage difference can be weighted to

obtain an output voltage of $V_{BG} = V_{D2} + \sqrt{AG}\Delta V_D$ (1.1)

where $\Delta V_D = V_T \ln\left(I_{D2}A_{D1}/\left(I_{D1}A_{D2}\right)\right)$.

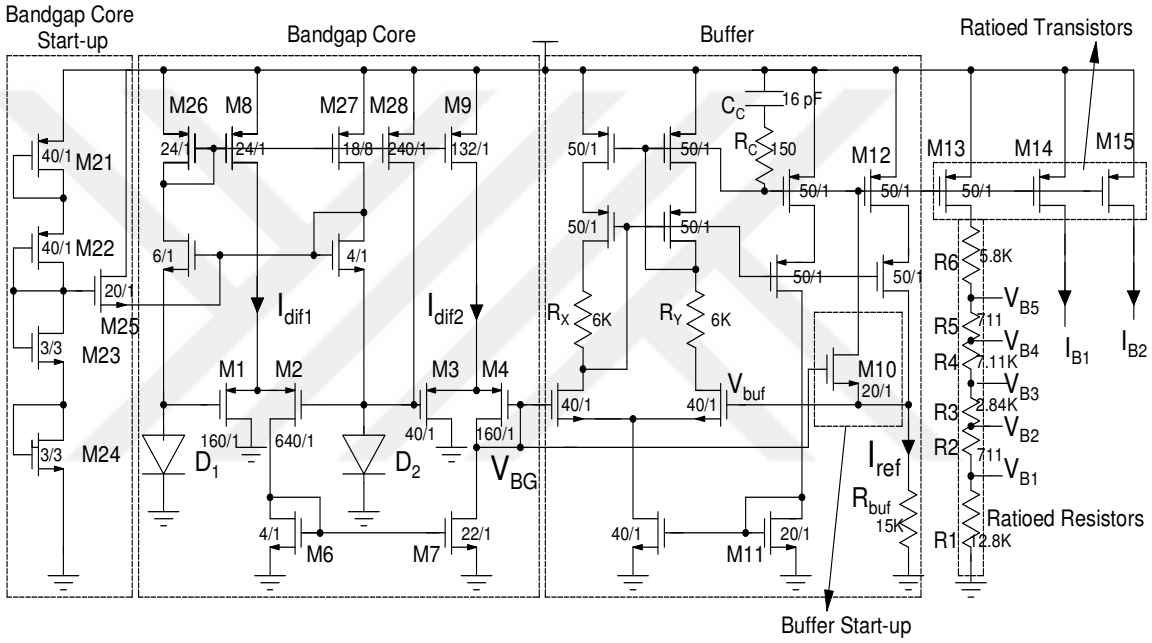


Figure 3.1 Schematic of the bandgap based voltage reference circuit

To yield zero temperature coefficients around room temperature the following choices were made: A=4 and G=5 with I_{D2}/I_{D1} = 10 and A_{D1}/A_{D2} = 20. With these values, simulations showed slightly negative temperature coefficients around room temperature. In order to be consistent with the simulations, the value of G was increased to 5.5 to have a higher value for Proportional to Absolute Temperature (PTAT) term in Equation (1.1). These values yield the reference voltage V_{BG} of 1.075 V. In Figure 3.1, the transistors, M26 together with M27 and M28, were sized to give the necessary diode current ratio.

W_{M8}/W_{M9} and W_{M6}/W_{M7} ratios were arranged to give the current ratio *G* of the differential pairs. Transistors M21-M25 serve as start-up for the bandgap core.

In the second stage, the reference voltage V_{BG} was forced across buffer resistor R_{buf} via buffer op-amp to yield a constant current [6]. This generated reference current was then used back to bias the amplifier itself via M11. Because of the self biasing feature, this stage needed a start-up. M10 performs this task by taking its gate input from bandgap reference which is assured to start-up.

At the last stage, this constant current was mirrored to a ratioed resistor network via M13. The total resistance in the chain was 30 kΩ. The requirement of large bias voltages up to 1.7 V necessitates the use of only one transistor, M13, on this rail. Because of the current variations of M13 with supply voltage variations, supply sensitivity of the circuit would be increased. However, this is acceptable for the designs that do not require very high precision. By mirroring this constant current, I_{ref}, with appropriate transistor sizing, desired constant bias currents could also be generated. To decrease the threshold voltage sensitivity caused by process variations, transistors were arranged to pass certain current levels to yield desired overdrive voltages. Hence, the total power dissipation was arranged to be 1.82 mW in simulations, which does not affect the power budget of the whole receiver. Power dissipation could easily be reduced for strictly low power applications. The bias voltages that were generated across the resistors, *R1*, *R2* and *R3* do not depend on the absolute values of these resistors but on their ratios to the buffer resistor ($V_x = V_{BG} \cdot R_x / R_{buf}$). To yield accurate resistor ratios, poly resistances with widths of 10 μm were used. In the simulation results as shown in Figure 3.2(a), the highest bias

voltage of 1.7 V has shown 5 mV variation in a temperature range of 25-100 °C (39 ppm/°C). Although the peak was shifted left in temperature axis, the output voltage variations with temperature were also very small in the measurements (Figure 3.2(b)).

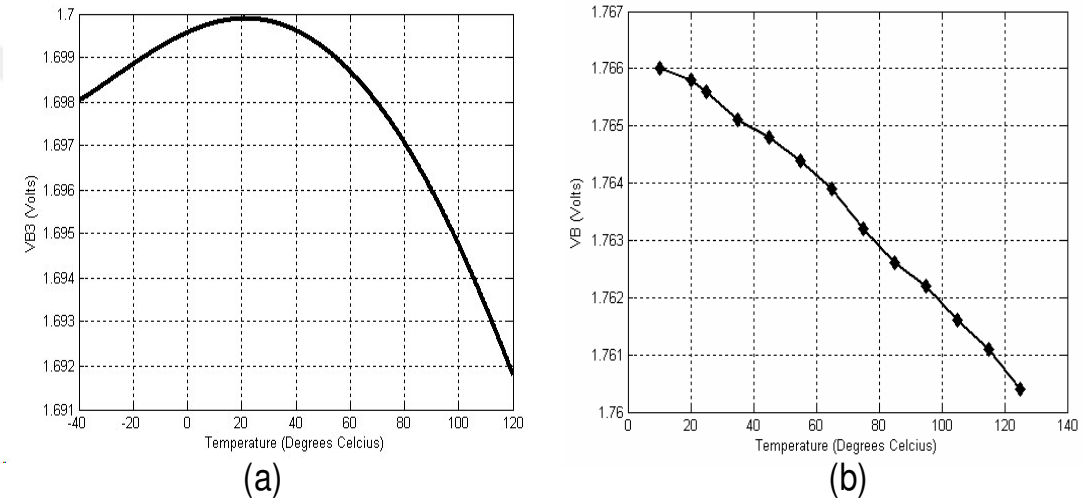


Figure 3.2 (a) Simulated temperature variation of the generated bias voltage;
(b) Measured temperature variation of the generated bias voltage

3.3 Testing and Measurements

The design was fabricated in *0.35-μm Silicon-On-Insulator (SOI) CMOS* process. Half of the die area is occupied by the ratioed resistors and the output pads. The compensation capacitance of the buffer amplifier takes a significant portion of the rest. The n^+/p diodes were constructed by surrounding n^+ active region with p^+. The chip occupies a die area of 700 μm by 630 μm. The layout of the design is shown in Figure 3.3. The picture of the fabricated die is shown in Figure 3.4.

In the measurements, all generated bias voltages came about 50 mV higher than the desired simulation values. This discrepancy could be due to the higher voltage drops across the diodes than what was predicted from the given diode models. This would yield a higher bandgap reference voltage. This change was directly reflected in the output bias voltages with the given resistor ratio.

The temperature measurements were done as the bare dies were attached to a hot-chuck probe station, which was connected to a semiconductor parameter analyzer (Figure 3.5). With the temperature rising to 125 °C, the bias voltage of 1.766 V at 10 °C dropped to 1.761 V, resulting in a variation of only 5 mV in this temperature range. Although the result is in complete compliance with the simulation results, the optimum temperature variation point was lower than the estimated value of the room temperature.

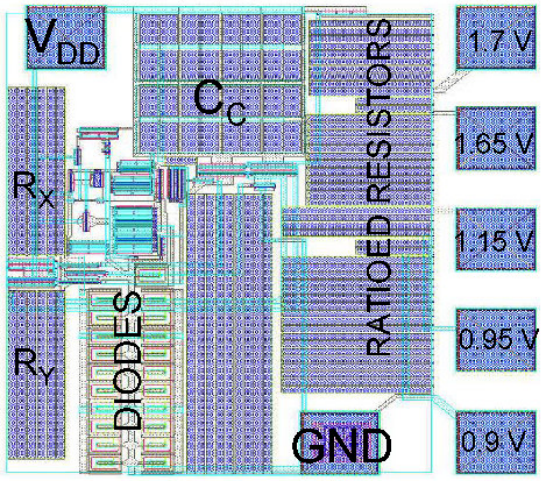


Figure 3.3 Layout of the design

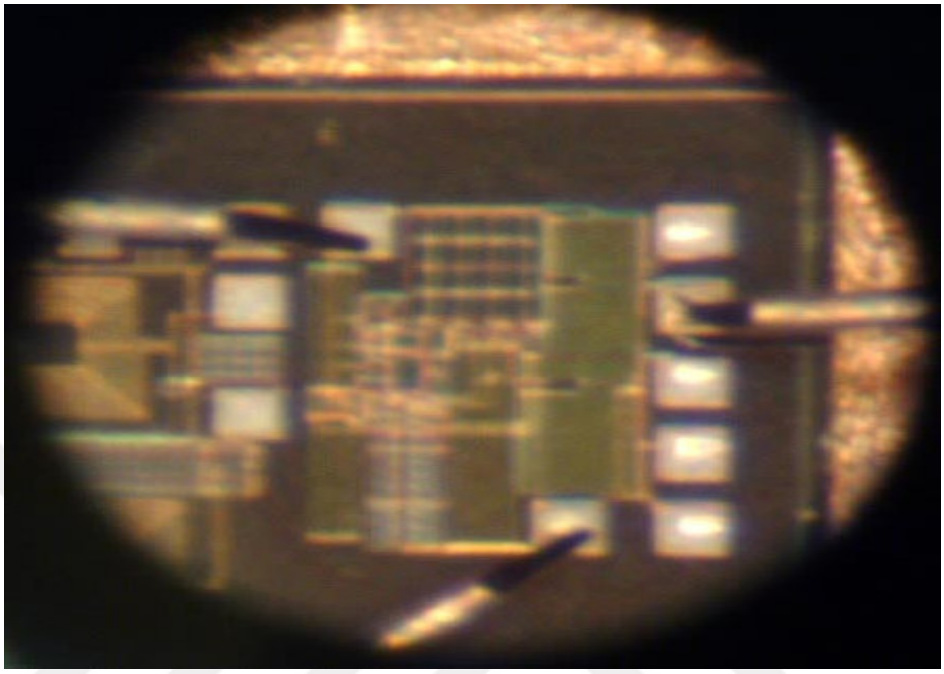


Figure 3.4 The die microphotograph with probes

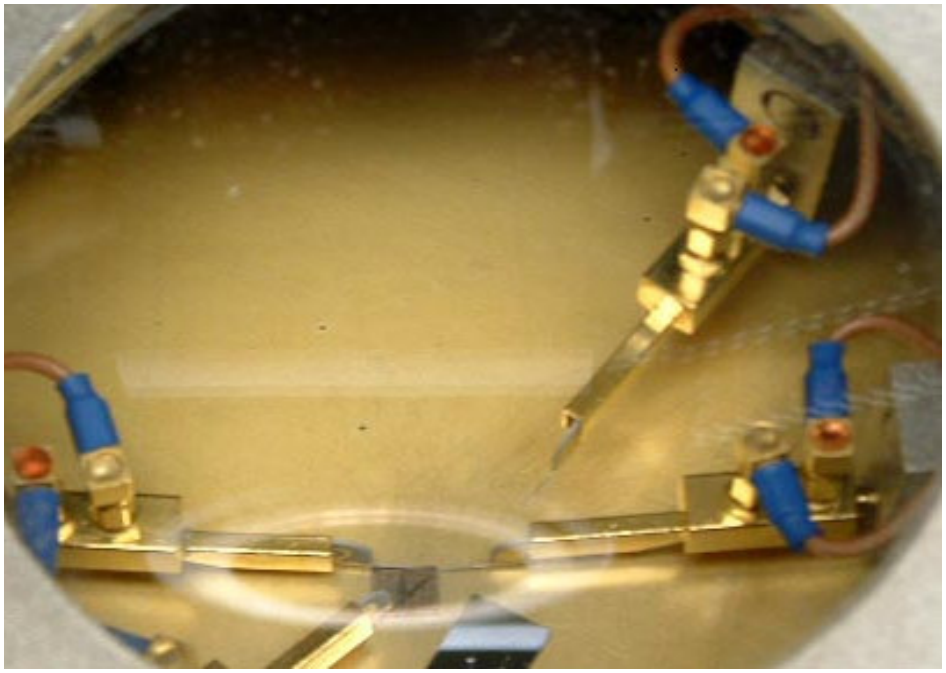


Figure 3.5 Measurement setup for hot-chuck measurements

3.4 Future Work

In this design, a 0.5-V increase in the supply voltage caused the reference voltage to jump to 1.1 V, which corresponds to a 2.3 % increase. The total variation in the highest output bias voltage was 8 %.

The circuit can further be improved by incorporating a regulated cascode output stage as shown in Figure 3.6. The transistor, M_c, was inserted to mirror the current in a cascode fashion to the regulated cascode output stage. This output stage can achieve much higher output resistance with the feedback employed by M_{R3} and M_{R4}. The simulated supply voltage dependence of the previous circuit and of this improved circuit are given in Figure 3.7(a) and in Figure 3.7(b), respectively. This improved circuit is much less sensitive to supply variations.

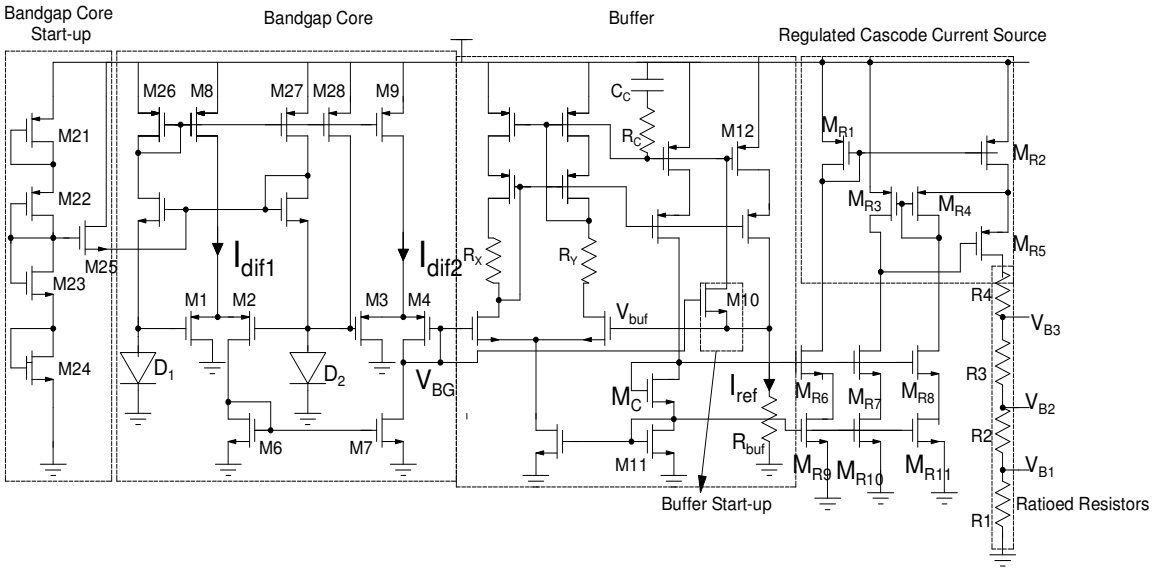


Figure 3.6 Improved architecture with regulated cascode output stage

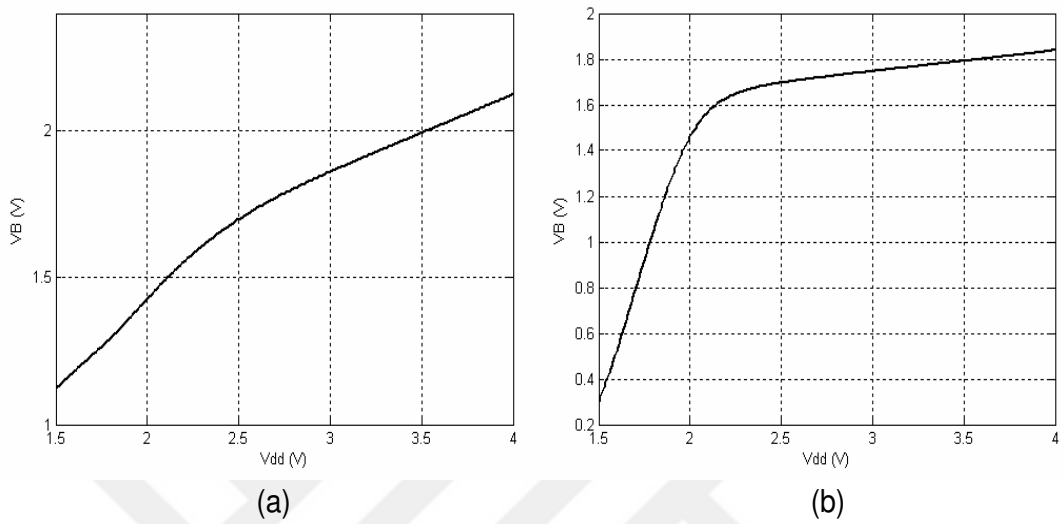


Figure 3.7 (a) Simulated supply voltage dependence of the highest bias voltage (1.7 V) with non-regulated output stage; (b) Simulated supply voltage dependence of the highest bias voltage (1.7 V) with regulated cascode output stage

3.5 Conclusion

A bandgap based constant-voltage, constant-current bias circuit was designed and fabricated in 0.35-μm Silicon-On-Insulator (SOI) CMOS process. Temperature insensitive multiple bias voltages and currents were generated to satisfy the bias requirements of an integrated receiver. In the measurements, the highest bias voltage variation was less than 39 ppm/°C in the temperature range of 10 °C to 125 °C.

CHAPTER 4

DESIGN, IMPLEMENTATION, AND TESTING OF RF VCOs IN 0.35-μm SOI CMOS

4.1 Introduction

Voltage Controlled Oscillators (VCOs) are one of the most critical blocks of RF transceivers. Thanks to the recent developments in silicon technologies, it is now possible for a fully integrated VCO to satisfy the phase noise and power requirements of high frequency wireless standards [9]. The results presented in many of the recently published works on CMOS LC VCOs have proven a very satisfactory performance in terms of requirements of these standards [11]-[18]. Despite these promising results, a common obstacle in all of these designs, namely, the losses associated with the integration of passive elements such as inductors in a standard CMOS process, leaves these designs impractical compared to their rivals in other processes. Some designs try to address this issue by utilizing bond-wire inductance [14] [17] [18]. Others try to alleviate this problem by using all available metal layers in parallel and by fine optimization of the coil geometries for the desired frequency [9] [11].

This chapter presents the design of high performance, fully integrated VCOs in a Silicon on Insulator (SOI) CMOS process. SOI CMOS lends itself to the integration of low parasitic active and passive components that in turn are able to yield a lower VCO phase noise compared to what could be achieved with a bulk CMOS process [10].

The chapter is organized as follows. In section 4.2, general design considerations for an RF CMOS VCO design are discussed. Section 4.3 presents an 800-MHz fully on-

chip VCO in 0.35-μm SOI CMOS with phase noise of -121 dBc/Hz at a 600-KHz offset. Another 1.736 GHz low-power low phase noise LC VCO in 0.35-μm SOI CMOS is presented in section 4.4. Section 4.5 is the conclusion.

4.2 General Design Considerations for RF VCO Design

Enlarging the oscillation amplitude is a very efficient way to reduce the phase noise of a VCO [9]. For a given current level, this can be achieved by maximizing the values of the resonant tank inductors [13]. However, there are some serious limitations on the value of the inductor if the inductor is to be integrated in a CMOS process. Having a very large inductance means having a small tank capacitance. Considering the parasitic capacitance of this large inductor and the parasitic capacitances of switching devices together with the load capacitance of the buffer or the mixer to be driven, the remaining headroom for the varactor would result in a very small tuning range for the VCO. Moreover, as the value of the inductance to be achieved as a spiral inductor increases, resistive losses associated with it will degrade the Q of this inductor, which is the most important phase noise source in a fully integrated VCO. Thus, inductors as large as possible with very low resistive losses should be constructed [9]. At this point, because the spiral inductors integrated in a SOI CMOS have shown much better performance due to very high resistivity substrate and buried oxide [10], one can expect better phase noise performance over VCOs constructed in a SOI CMOS than VCOs built in a bulk CMOS. Another advantage of SOI CMOS is that a higher tuning range can be achieved with the

increased share of varactor in the total tank capacitance due to the lower inductor parasitic capacitance in SOI CMOS.

4.3 An 800-MHz VCO in 0.35-µm SOI CMOS

As the first design consideration, an appropriate VCO-core topology should be chosen to meet the requirements of the desired application. As shown in Figure 4.1(a), the topology that uses nMOS – pMOS cross coupled pairs with pMOS tail current source was chosen for this design. Using both nMOS pair and pMOS pair gives double amplification and larger voltage-swing for a given current. In addition, this circuit can be optimized to have more symmetry in the output waveform leading to a further reduction in phase noise [11]. The supply voltage of 2.5 V bears enough voltage headroom to obtain a large oscillation amplitude, which is difficult to achieve with this topology at low supply voltages. Because of the additional parasitic capacitance of the pMOS pair, this topology has a lower tuning range compared to topologies utilizing only the nMOS pair in the core. Since it has a lower flicker noise, a pMOS transistor was used as a tail current source [11].

4.3.1 Circuit Design and Simulations

The basic configuration for an LC tank oscillator is given in Figure 4.1(b). To satisfy the oscillation condition, the transconductance, G_M, which is necessary to have the unity loop gain at oscillation frequency, ω_o, can be calculated from transfer function,

$$G_M = R_{eff}(\omega_o C)^2. \tag{4.1}$$

where $R_{eff} = R_C + R_L + \frac{1}{R_P(\omega_O C)^2}$. (4.2)

R_P is the parallel tank resistance, R_L is the inductor series resistance and R_C is the varactor series resistance [9].

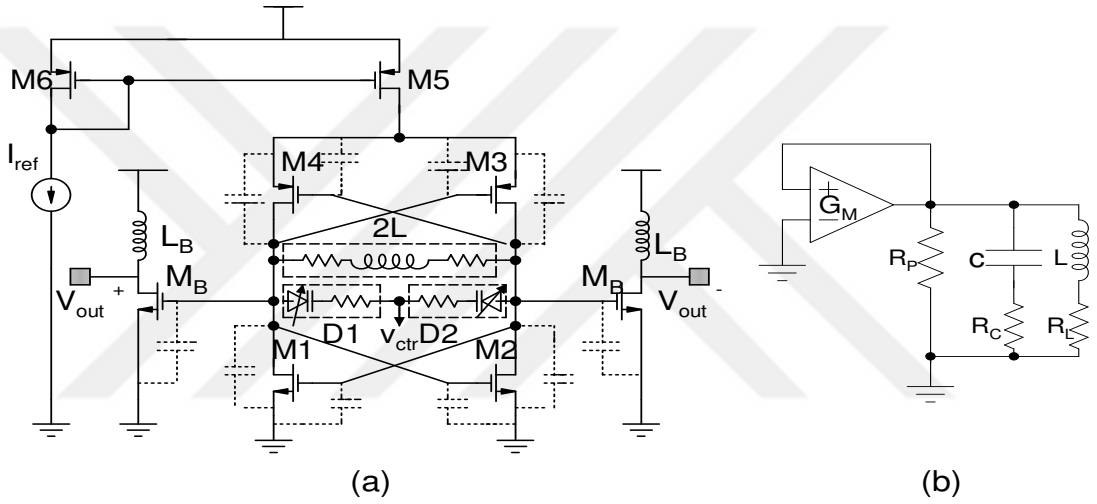


Figure 4.1 (a) VCO topology; (b) Basic LC-tank oscillator configuration

The dominant term in determining the value of R_{eff} is the series resistance of the inductor. For this design, the inductance value was selected to be 16.9 nH. This leaves a total tank capacitance of 1.99 pF to give rise to an oscillation frequency of 868-MHz. The inductor has 8.5 turns with the conductor width of 10 μm and the conductor spacing of 5 μm. Both available metal layers were shunted to reduce the series resistance of the inductor. Total space occupied by this 16.9 nH square inductor was 345 μm by 360 μm. The π-equivalent circuit model parameters that were extracted from the measured s-parameters of the fabricated inductor were used [10]. *Q* of the inductor at 868-MHz is 6.2, a value which is very difficult to achieve with Bulk CMOS. Q factor plot of this inductor and Q factor

plots of some other inductors with a different number of turns are shown in Figure 4.2(a). The series resistance at low frequencies is 9.5 Ω. Because of very high resistivity (2000 Ω.cm) of the substrate in SOI CMOS at high frequencies, the effect of substrate currents induced by the magnetic field of the inductor is negligible. Skin effect and eddy losses at 868 MHz would result in the series inductor resistance of 17 Ω. Together with 1 to 2 Ω series varactor resistance, the total effective resistance was estimated to be 18 Ω. Using Equation (4.1), the transconductance required to compensate the losses can be calculated as $G_M = 18\Omega \cdot (2\pi \cdot 868MHz \cdot 1.99pF)^2 = 2.11mS.$ With a safety factor of 2, there should be an overall G_M of around 4.5-mS. Therefore, each transistor should have a g_m of 4.5-mS. The current required to achieve the given transconductance value with over-drive voltage of $V_{GS} - V_T = 0.3V$ would be $I_D = g_m(V_{GS} - V_T)/2 = 0.675mA$. In order not to remain in current limited regime, a current of 1-mA was forced to pass through each branch. Hence, the total tail current of VCO core is set to 2-mA from a 2.5-V supply. The corresponding transistor *W/L* ratios for this current and overdrive voltage level were $42\mu m/0.35\mu m$ for nMOS pair transistors *M1* and *M2* and $120\mu m/0.35\mu m$ for pMOS pair transistors *M3* and *M4*. Source transistor (*M5*) width was 240-µm with the minimum gate length of 0.35-µm. This size was chosen so that the transistor can supply the 2-mA current with an exact amount of DC drop required.

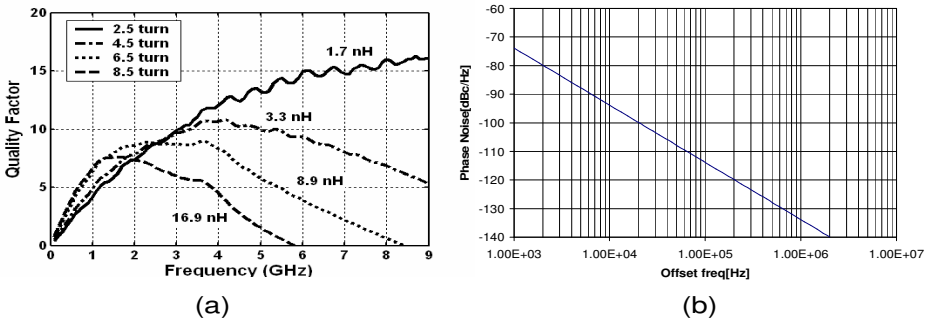
For measurement purposes, nMOS buffers were used with inductive peaking, which can provide a larger and more symmetric swing to a 50-Ω load than resistive peaking. Because of a 0 V output DC level, the output signal can be directly connected to a spectrum analyzer [14]. The value of inductance is 8.9 nH for the buffer inductors.

Buffer transistors have 70-μm width with minimum gate length. Buffers draw a total current of 4 mA from a separate 2.5 V supply.

Single sided spectral phase noise density at certain offset can be estimated by integrating the output noise contributions of R_{eff} and of switching devices over 1-Hz bandwidth and dividing by the carrier power as suggested by Craninckx and Steyaert [9]. Noise density at $\Delta\omega$ offset frequency is given by,

$$L\{\Delta\omega\} = \frac{kTR_{eff}[1+A](\omega_o/\Delta\omega)^2}{V_A^2/2}. \tag{4.3}$$

V_A is the oscillation amplitude, and A is called amplifier noise contribution factor [9]. With an oscillation amplitude level of 1.7 V, the estimated phase noise at a 600-kHz offset is $L\{600kHz\} = \frac{kT \cdot 18\Omega \cdot [1+2.5][868MHz/600kHz]}{(1.7V)^2/2} = -122.1 \quad dBc/Hz$. This value is much higher than the simulation result of -129 dBc/Hz. Figure 4.2(b) shows the phase noise simulation result obtained from *SpectreRF* of *Cadence*. However, this estimate is much closer to the measurement result of -121 dBc/Hz.



(a) (b)

Figure 4.2 (a) Measured quality factors of SOI inductors; (b) Simulated phase noise

The simulated tuning characteristic of the oscillator is shown in Figure 4.3. This tuning range is achieved with 1-pF p-well/n^+ varactor diode. Layout of the design is shown in Figure 4.4. It was drawn in *Cadence Virtuoso*. Special attention is given to layout symmetry. All DC supply pads and control voltage pads were surrounded with decoupling capacitances. The varactor diodes were constructed as an array of p-well/n^+ junctions connected in parallel to increase the Q of the varactor. The total die area was 1150 μm by 950 μm, half of which is occupied by the buffer inductors, the decoupling capacitors and the bonding pads.

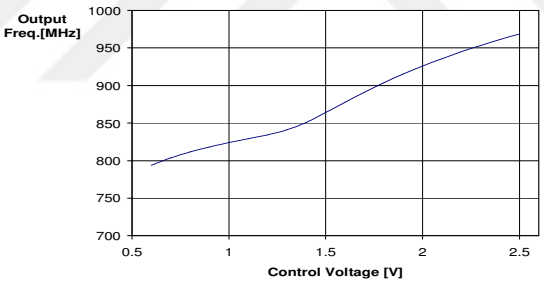


Figure 4.3 Simulated tuning characteristic

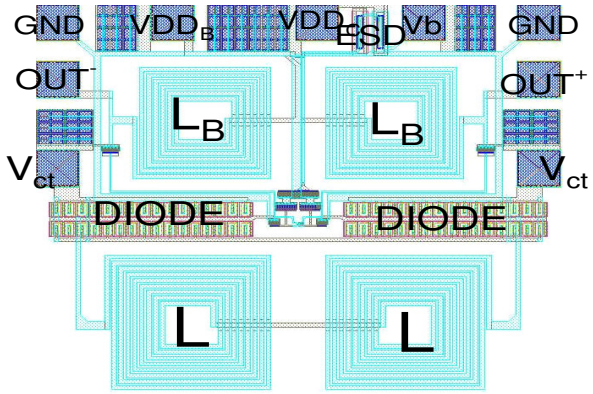


Figure 4.4 Layout of the chip

4.3.2 Testing and Measurement Results

The fabricated die photo of the design is shown in Figure 4.5. The design shares the same die with the other receiver blocks. The design was tested on a 72 pin low parasitic open carrier—QFN-72. First, it was tested together with the other designs with bondwire configuration shown in Figure 4.6 and with the testing board shown in Figure 4.7. The three boards with different dies having long bonwire configuration yielded maximum oscillation frequencies of 733-MHz, 759-MHz and 800-MHz.

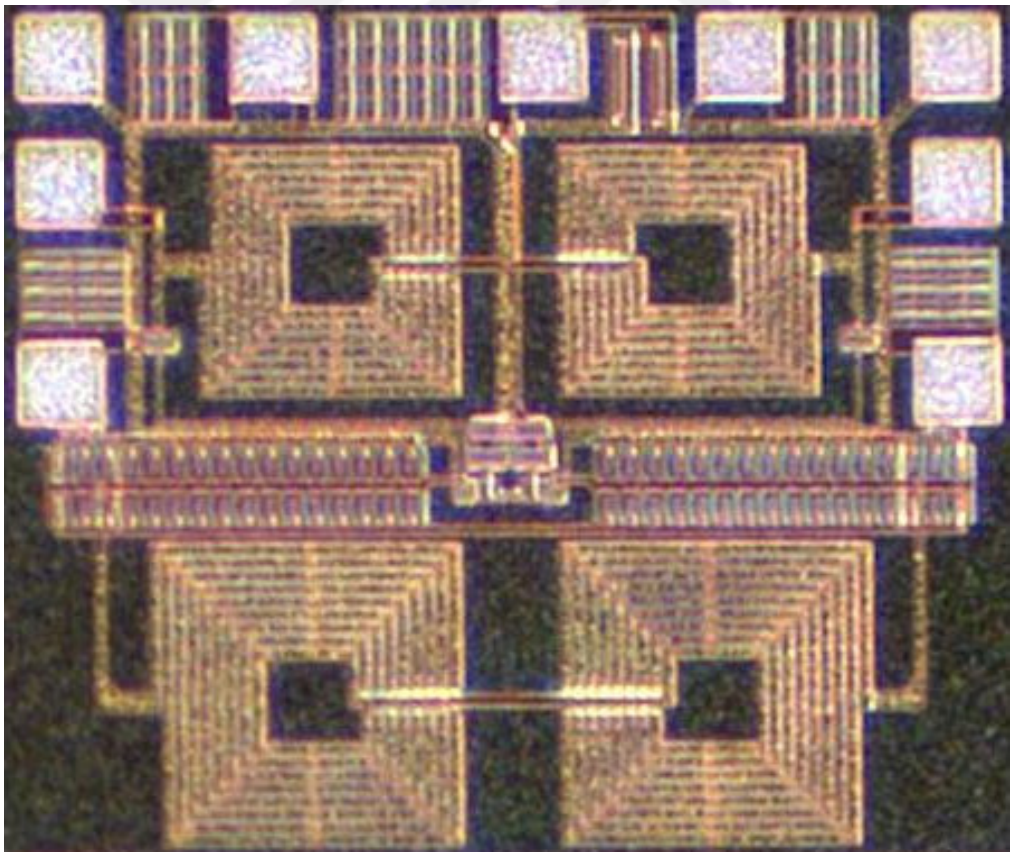


Figure 4.5 Die photo of the design

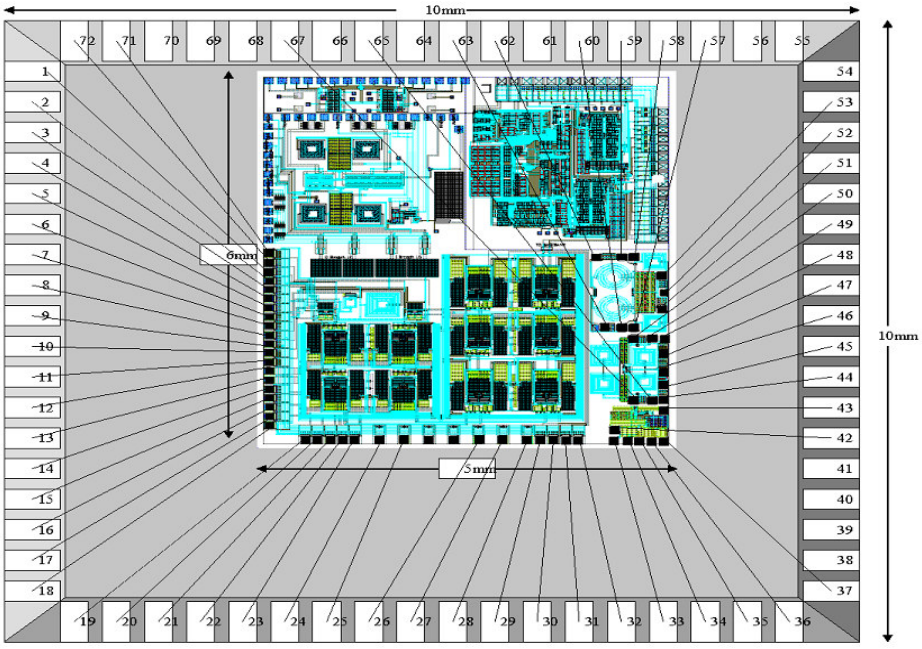


Figure 4.6 Bonding diagram with other receiver blocks

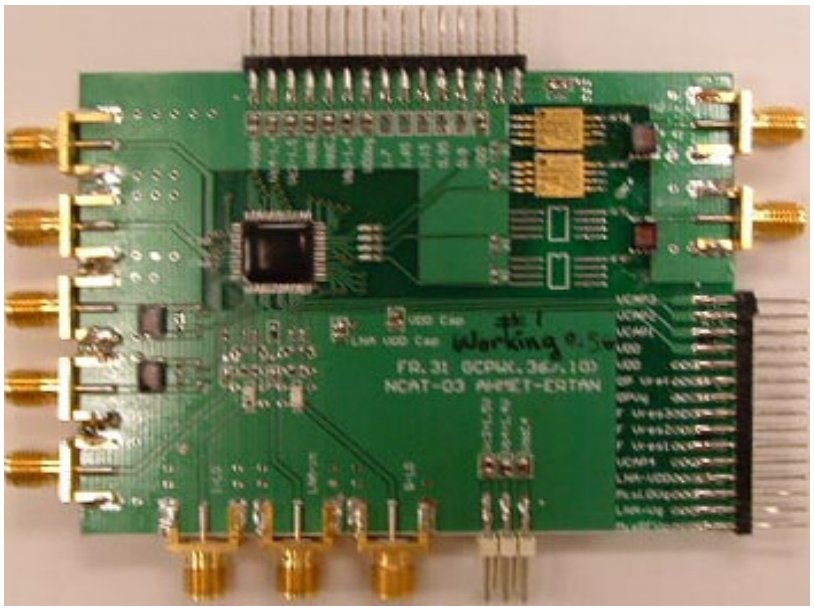


Figure 4.7 Testing board designed for all receiver blocks

Later, the design was tested separately with shortest possible bondwire configuration shown in Figure 4.8 on another test board shown in Figure 4.9. The design which was tested with short bondwire configuration oscillated at a maximum frequency of 751-MHz, proving no significant bondwire effect on oscillation frequency for this design.

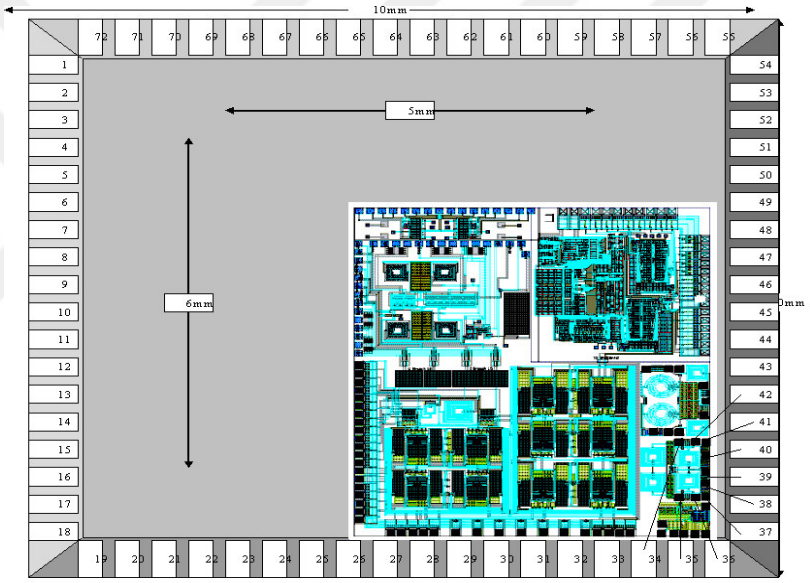


Figure 4.8 Bondwire configuration with the shortest possible wires

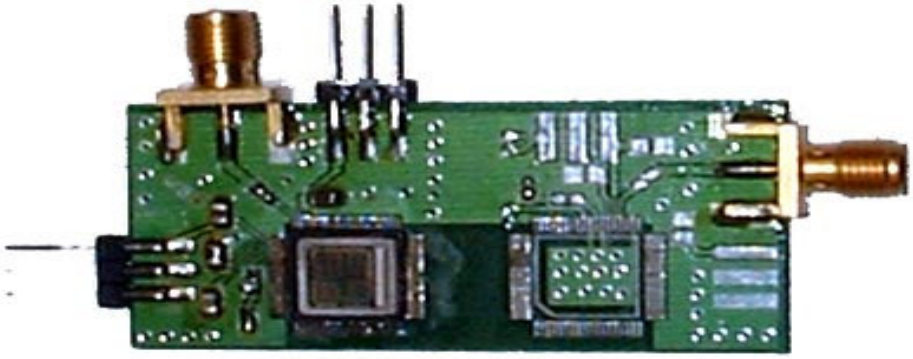
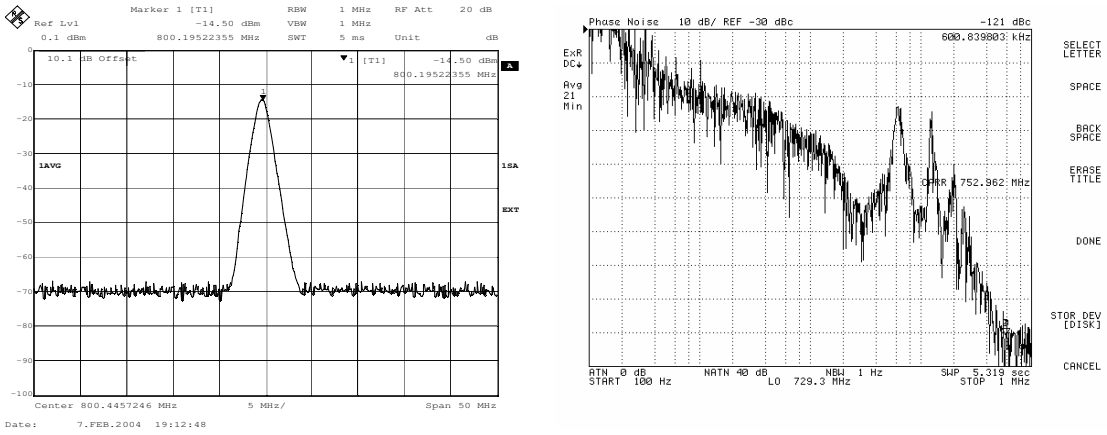


Figure 4.9 Test board designed to test the VCO with short bondwire configuration

Figure 4.10(a) shows the measured spectrum of the VCO from the die yielding 800-MHz maximum oscillation frequency. An output power level of -14.5 dBm was observed at the oscillation frequency of 800-MHz. Figure 4.10(b) shows the measured phase noise versus the offset frequency from an 800-MHz center frequency. The results showed -121 dBc/Hz phase noise at a 600-kHz offset frequency with 6 mW power dissipation. Figures 4.11(a) and 4.11(b) show the measured phase noise values for different VCO core DC current levels and the tuning characteristics of the VCO, respectively. The oscillation occured at 800 MHz with only a 0.7 mA DC current with a -108-dBc/Hz phase-noise and 1.75-mW power dissipation (Figure 4.11(a)). If the DC current is increased to 2.88 mA, which corresponds to 7.2 mW, the phase noise at 800-MHz oscillation frequency becomes -127.5 dBc/Hz. The oscillator operates from 570 MHz to 800 MHz with an overall tuning range of 230-MHz (33 %) at a center frequency of 700-MHz (Figure 4.11(b)).



(a) (b)

Figure 4.10 (a) Measured spectrum of the VCO; (b) Measured phase noise of the VCO

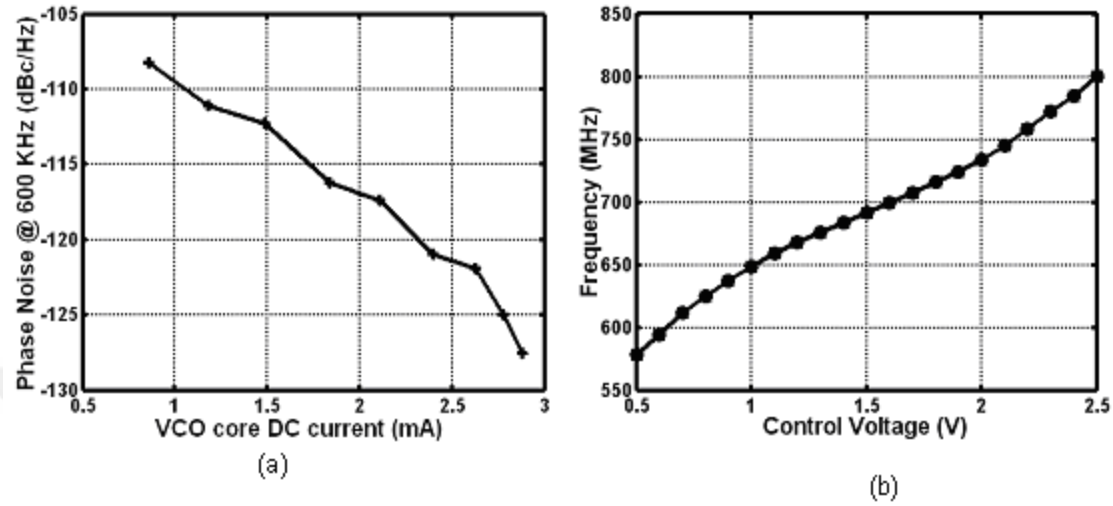


Figure 4.11 (a) Measured phase noise at 600 KHz offset (at 800 MHz) for different bias currents; (b) Tuning characteristics of the VCO

4.4 A 1.736 GHz Low-Power, Low Phase Noise LC VCO in 0.35-µm SOI

Since it is very difficult to achieve low phase noise at such a high frequency, the n-core topology was chosen. As shown in Figure 4.12, this topology utilizes only nMOS pair as a negative transconductor. With this topology, one can obtain a higher oscillation swing, which leads to a lower phase noise at the expense of higher power dissipation to sustain this oscillation [11]. Moreover, with a large LO voltage-swing, a mixer can be driven with greater linearity [12]. Since it has lower flicker noise, a pMOS transistor was used as a tail current source.

4.4.1 Circuit Design and Simulations

Due to the high tuning range required by the PLL application, the inductance value was chosen to be 4.2 nH. This left a total tank capacitance of 2 pF that resulted in an oscillation frequency of 1.736 GHz. A round spiral inductor with 3.5 turns was used.

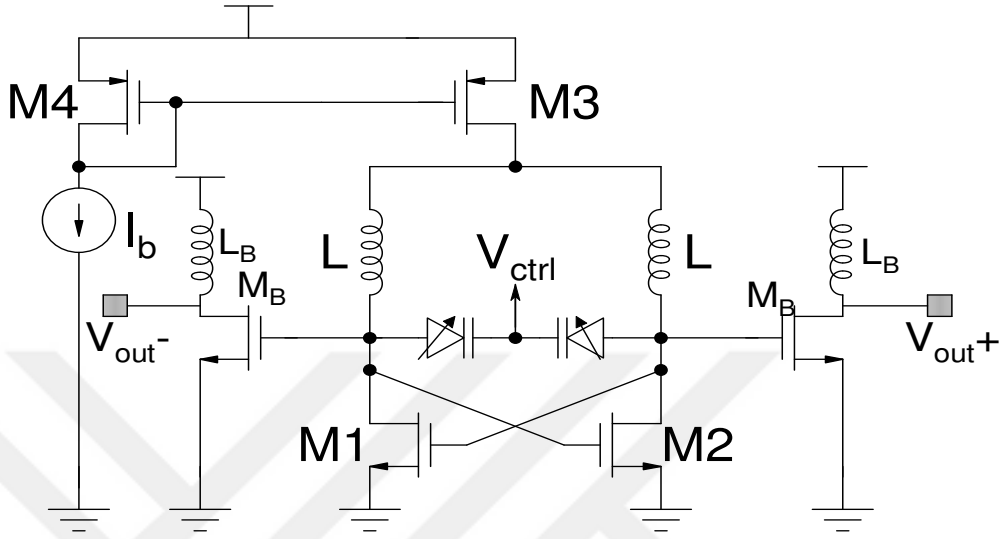


Figure 4.12 Schematic of the VCO

Because of very high resistivity (2000 Ω.cm) of the SOI substrate, at high frequencies, the effect of substrate currents induced by the magnetic field of the inductor was negligible. Therefore, very wide conductors with a width of w = 30 μm were used to reduce the series resistance of the inductor. The two available metal layers were used in parallel for the same purpose. The conductor spacing was 10 μm. Hence, the total radius of the 4.2 nH round inductor was 215 μm. The π -equivalent circuit model parameters, which were extracted from the measured s-parameters of the fabricated inductor, were used in the simulations [10]. As shown in Figure 4.13(a), the Q of the inductor at the frequency of interest was 4.88. The series resistance at low frequencies was 2.6 Ω. As shown in Figure 4.13(b), at high frequencies skin effect and Eddy losses would dramatically increase the effective series resistance of the inductor.

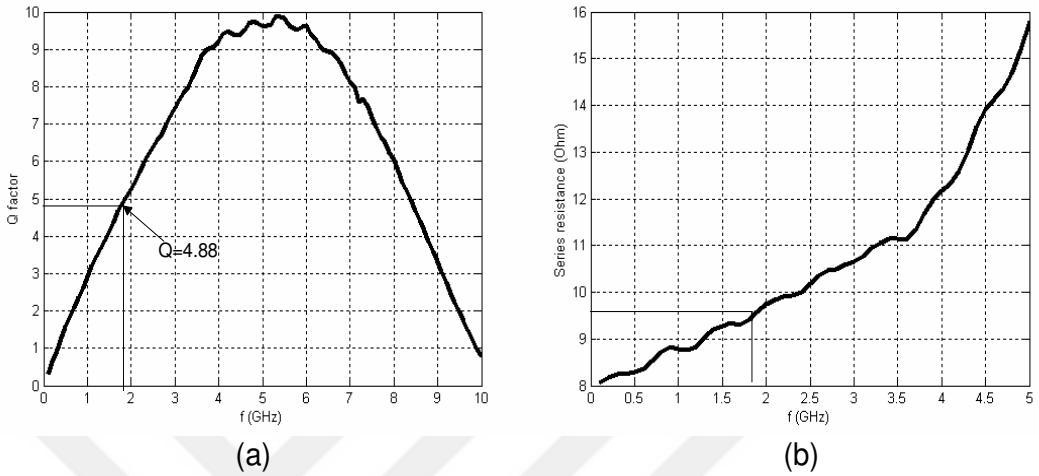


Figure 4.13 (a) The measured Q factor of the inductor; (b) Effective series resistance of the 4.2-nH inductor with frequency

The inductor series resistance at the frequency of 1.8 GHz was approximately 9 Ω. Together with a series varactor resistance 2-Ω, the total effective resistance was estimated to be 10 Ω. Using (1), the transconductance required to compensate the losses was calculated as $G_M = 10\Omega \cdot (2\pi \cdot 1.73GHz \cdot 2pF)^2 = 4.7mS$. Therefore, each transistor should have a g_m of 9.4 mS. Current required to achieve the given transconductance value with over-drive voltage of $V_{GS} - V_T = 0.4V$ would be $I_D = g_m (V_{GS} - V_T)/2 = 1.88mA$. To remain conservative, 2 mA current was arranged to pass through each branch. Hence, the total tail current of VCO core was set to a value of 4 mA from a 2.5-V supply. The corresponding transistor *W/L* ratios were $56\mu m/0.35\mu m$ for nMOS pair transistors. The $V_{GS} - V_T$ value could have been chosen very small to yield a large transconductance to current ratio, hence a small power consumption. However, achieving the required

transconductance with small over-drive voltage required very large transistor widths. This would result in very large parasitic capacitance values and hence small tuning range [1]. Moreover, with small over-drive voltage, output DC level would be closer to ground. This would limit the oscillation amplitude from the ground side. The width of source transistor *M3* was 320 μm with a minimum gate length of 0.35 μm. Inductively loaded buffer amplifiers were utilized to drive the 50- Ω measurement device. The buffer inductors were 8.9 nH on-chip spiral inductors. Buffer transistors had a width of 70 μm with a minimum gate length.

Tuning characteristic of the oscillator is shown in Figure 4.14(a). A control voltage of 0.7 V resulted in 1436 MHz oscillation frequency, whereas the highest control voltage of 2.5 V yielded 2032 MHz oscillation frequency. This 600 MHz tuning range (~30%) was achieved with 1.6 pF p-well/n^+ varactor diode. The remaining 0.4 pF part of the total tank capacitance was formed by the parasitic substrate capacitance of the inductor, drain-source and gate-source capacitances of switching transistors and the gate-source capacitance of the buffer transistor.

Using Equation 4.3, the estimated phase noise at 600 kHz offset with oscillation amplitude of 1.7 V is,

$$L\{600\,kHz\} = \frac{kT \cdot 10\Omega \cdot [1+2][1736\,MHz/600\,kHz]}{1.7V^2/2} = -121.1 \qquad dBc/Hz.$$

This value is 3 dB higher than the simulation result of -124 dBc/Hz. Figure 4.14(b) shows the phase noise simulation result obtained from *SpectreRF*.

Layout of the VCO drawn in Virtuoso is shown in Figure 4.15. Special attention was given to layout symmetry. All DC supply pads and control voltage pads were surrounded with decoupling capacitances. The varactor diodes were constructed as an array of p-well/n+ junctions connected in parallel to increase the Q of the varactor. Each element was surrounded by as many contacts as possible to reduce overall series resistance. The total die area was 1300 μm by 950 μm half of which was occupied by buffer inductors, decoupling capacitors and bonding pads.

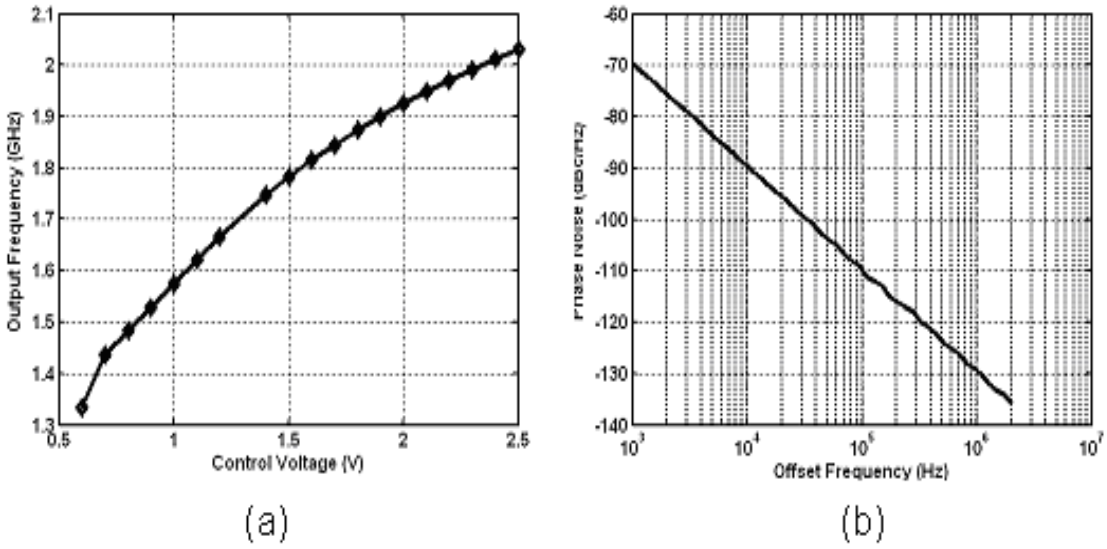


Figure 4.14 (a) Simulated tuning characteristic of the VCO; (b) Simulated PN vs. offset frequency

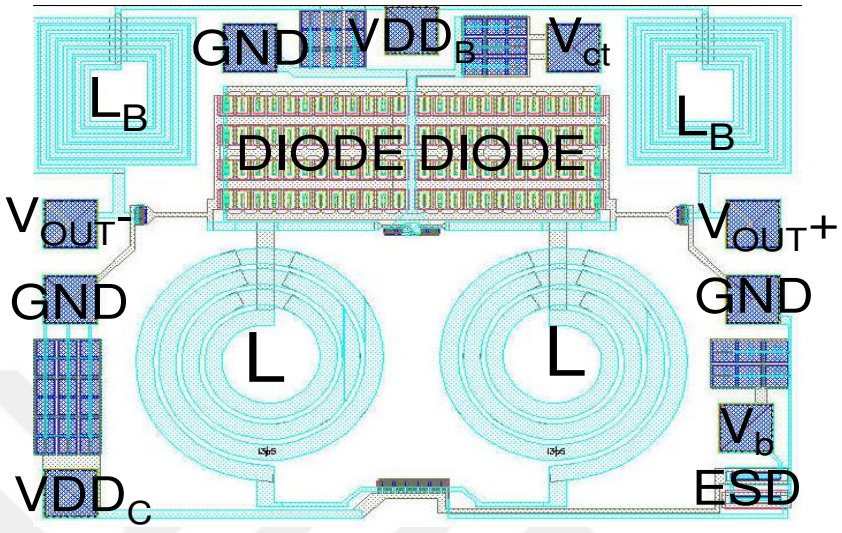


Figure 4.15 Layout of the design

4.4.2 Testing and Measurement Results

The fabricated die photo of the design is shown in Figure 4.16. The design shares the same die with the other receiver blocks. The design was tested on a 72 pin low parasitic open carrier—QFN-72.

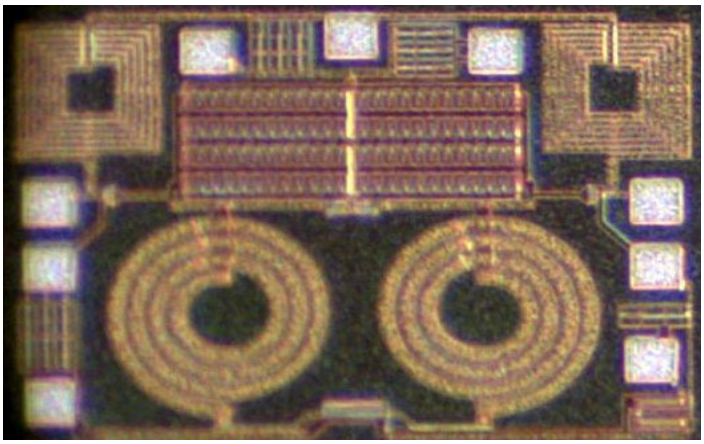


Figure 4.16 Die photo of the design

The design was first tested together with the other designs with bonwire configuration shown in Figure 4.6 and testing board shown in Figure 4.7. Later, the design was tested separately on another board shown in Figure 4.17 with shortest possible bondwire configuration shown in Figure 4.18. The circuits tested in both boards (long bondwire, short bondwire) have not oscillated. Highly possible reason for this is the inductances introduced by limited number of pads (only one for core GND and one for Vctr). The bondwire inductance at the control node can easily cancel out the varactor tank capacitance at such a high frequency. Space limitations do not allow the use of big enough decoupling capacitance to have V_{ctr} node perfect AC ground.

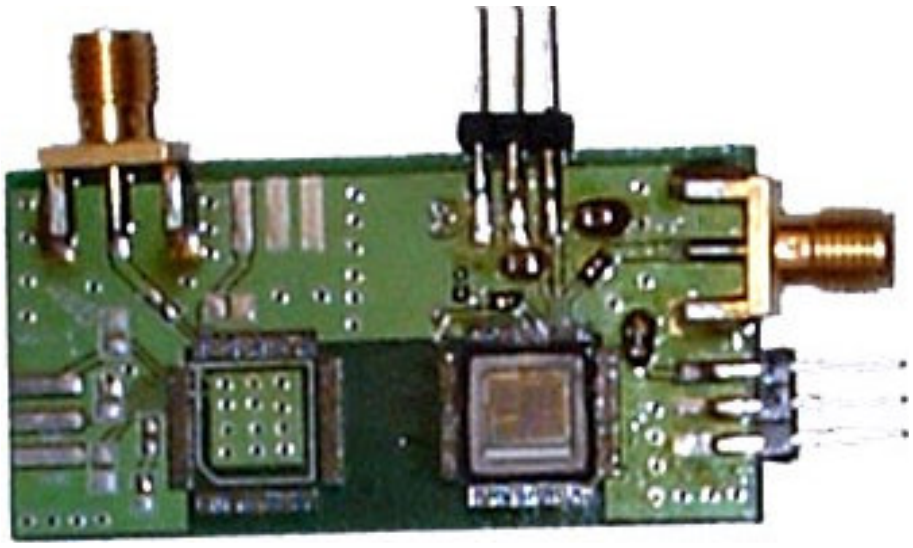


Figure 4.17 Test board designed to test the VCO with short bondwire configuration

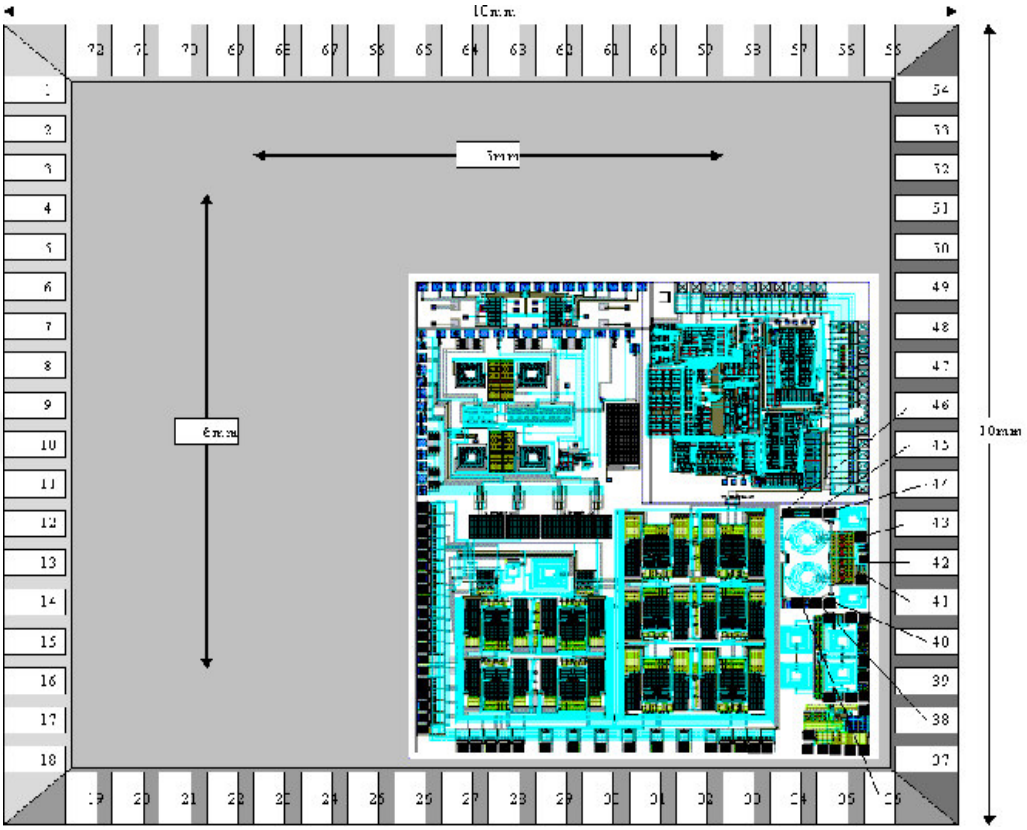


Figure 4.18 Bondwire configuration with the shortest possible wires

4.5 Conclusion

The low parasitic nature of SOI CMOS was utilized to design a high performance fully integrated LC VCOs at 868-MHz and 1.736-GHz center frequencies. The measured s-parameters of the fabricated spiral inductors were fed into the simulations to represent a more realistic model for the integrated inductors. Measurement results of the 868-MHz design proved that SOI CMOS can be used to design other high performance tuned circuits.

CHAPTER 5

DESIGN AND IMPLEMENTATION OF A 434 MHz LOW POWER QUADRATURE PLL IN 0.35-μm SOI CMOS

5.1 Introduction

From the day they were first introduced, PLLs have become very common building blocks for a range of different applications such as clock drivers, clock recovery circuits, frequency modulators, and frequency synthesizers. With the introduction of new applications, designers hav focused on different architectures and different trade-offs in their PLL designs to satisfy the requirements of the emerging applications with low cost and low power. The goal of this PLL design was to generate quadrature carrier signals at 434 MHz for a single channel communication system that required low power dissipation.

As the quadrature generation architecture, master-slave frequency division technique was selected. This required the VCO to be designed at $2f_0$. To have a successful fast frequency division, buffers should be inserted after this divider to drive the mixers.

The chapter is organized as follows. In section 5.2, general design considerations for a PLL design work are discussed. In section 5.3, selection of PLL architecture for this design is discussed. Section 5.4 presents the main building blocks of the PLL. Layout issues are discussed in section 5.5, and section 5.6 is the conclusion.

5.2 General Design Considerations for PLL Design

Figure 5.1 shows basic block diagram of a simple PLL. There are two main categories of PLLs. First category PLLs are the PLLs incorporating sinusoidal PDs and RC filters. PLLs in this group are called "type-1" because open loop transfer function for these PLLs contains only one pole at the origin. The other group of PLLs includes the PLLs using three-state PFDs and charge pumps. These are called "type-2" because they have open loop transfer function having two poles at the origin [4].

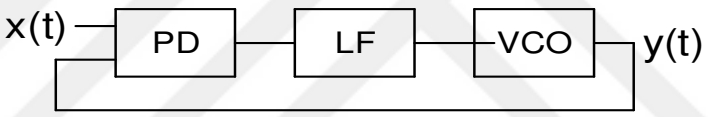


Figure 5.1 Block diagram of a basic PLL

In type-1 PLLs, open loop transfer function is given by $K/[(1+S/\omega_{LPF})S]$ where K is the loop gain. For K=0, closed loop poles begin at s_1=0 and s_2=-ω_{LPF}. As K increases, s_1 and s_2 move toward each other on the real axis and meet for K= ω_{LPF}/4. For higher K, the poles become imaginary and move toward +∞ and -∞. Since damping factor ξ = cosθ, increasing K makes the system less stable. [4]. In the case of a type-1 PLL, the natural frequency is $\omega_N = \sqrt{K_L \omega_H}$, and the damping factor is $\xi = 1/2\sqrt{\omega_H / K_L}$. High loop gain, K_L, gives large signal bandwidth and short response time to transient changes in signal frequency. Excessively high values of loop gain, however, lower the damping ratio ξ introducing overshoot or even ringing in the

system step response. Reducing the loop filter bandwidth, ω_H, improves the rejection of out of band signals, but at the same time the capture range is decreased, the pull-in time becomes longer and the loop phase margin becomes poorer.

The stability issues are totally different in type-2 PLLs. For a type-2 charge pump PLL (second order with a zero) of Figure 5.2, the open loop transfer function is equal to $I_P[R+1/SC_P]K_{VCO}/2\pi S$. As I_PK_{VCO} increases from zero, both poles depart from the origin and move on a circle in the left half plane, eventually returning to the real axis for sufficiently high gain, that is, where $I_PK_{VCO}=8\pi/(R^2C_P)$ and ξ=1. Thus, increasing the loop gain makes the PLL more stable. In the case of a type-2 PLL, the natural frequency is $\omega_N=\sqrt{I_PK_{VCO}/2\pi C_P}$, and the damping factor is $\xi=\frac{R}{2}\sqrt{I_PK_{VCO}C_P/2\pi}$. While for a type-1 PLL, ω_N and ξ, cannot be maximized simultaneously; in a Charge-Pump PLL, both ω_N and ξ can be increased if I_P or K_{VCO} is increased. Root locus of type-1 and type-2 PLLs are given in Figure 5.3.

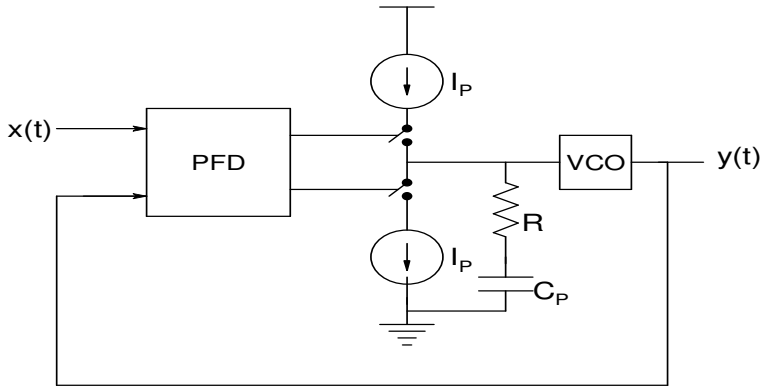


Figure 5.2 Block diagram of CP-PLL

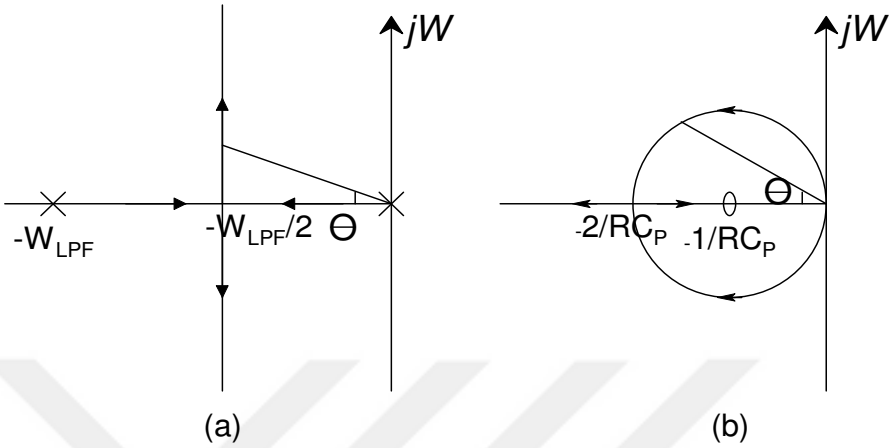


Figure 5.3 Root loci for (a) Type-1 PLL; (b) Type-2 PLL

Although stability is always guaranteed in a second order PLL, any mismatch in the charge pump of a second order PLL causes sudden jumps on the VCO control voltage at every phase measurement cycle. Large spurious tones can thus appear at the output. Therefore, an additional capacitor is usually added to the loop filter to prevent sudden jumps on the VCO control voltage and thus reduce the spurious sideband levels. However, this additional capacitance increases the PLL order to three. The additional pole of a third order PLL provides more spurious suppression, but the extra phase lag associated with this pole introduces a stability issue. Thus, the Loop Filter must be designed carefully to provide the required filtering while maintaining the loop stability [19].

To further reduce the spurs without decreasing the crossover frequency and hence increasing the settling time, an additional pole needs to be added to the loop. This additional pole increases the PLL order to four. Third order and fourth order loops with

the same crossover frequency have nearly identical phase margins and settling times. The additional pole of a fourth order PLL provides higher spurious filtering without reducing the crossover frequency [19].

In addition to careful filter design, matching of UP and DOWN currents is also very important issue regarding the spurious performance of the PLL. Otherwise, the net charge injected by pulses of equal width into the filter impedance will not be zero. The loop will settle to a small phase offset at the PFD input, resulting in a change in pulse width that compensates the difference in current magnitude. As a result, the net charge injected is zero, but since the current pulses are not equal, reference frequency spikes will appear at the output [9].

These reference frequency spurs are a serious problem especially if ω_{ref} is small enough that spikes fall in the band of interest. Typical synthesizers employ large capacitors in the loop filter to reduce ΔV and minimize K_{VCO} to lower the modulation index. At low supply voltages, this is not feasible because the tuning range must be sufficiently wide to guarantee lock despite process and temperature variations.

In integer-N architecture, the loop bandwidth is limited because the input reference frequency must be equal to the channel spacing. Fractional-N synthesizers, on the other hand, can be designed with much higher F_{REF}, which means one can have higher loop bandwidth, which results in fast settling time.

The input phase noise spectrum of a PLL is shaped by the characteristic low-pass transfer function of the system when it appears at the output. For fast variations of the input excess phase, the PLL fails to track the input. The VCO phase noise experiences a

high pass transfer function as it appears at the output of the PLL. Thus, increasing the bandwidth of the PLL can lower the contribution of the VCO phase noise [4].

5.3 PLL Architecture

In PLLs requiring quadrature outputs, the way of generating these quadrature outputs is a very important consideration. The three most common ways to generate quadrature outputs are using poly-phase filters, two cross coupled VCOs, and VCO-frequency divider configuration [20].

In case of an RC poly-phase filter, the losses associated with the RC network would necessitate the use of large buffers to drive the mixers with the desired linearity. These buffers generally consume large amounts of power. Moreover, mismatches between the integrated R-C component values would result in unacceptable phase errors.

Cross-coupled LC VCO solution for an oscillation frequency of 434 MHz has serious drawbacks, too. To sustain the oscillation with a reasonable level of phase noise with relatively large passive components, the design should consume considerable amounts of power. This power is doubled with the requirement of two VCOs for this architecture. The area required would also double for the same reason.

The best way to generate quadrature outputs at 434 MHz is to have a VCO frequency of 868 MHz. A fast master-slave divide-by-2 circuit can be used to generate quadrature outputs at 434 MHz. The block diagram of the design is given in Figure 5.4. Two differential buffers are inserted after divide-by-2 operation not to load this divider circuit and to be able to drive the mixer to a greater linearity.

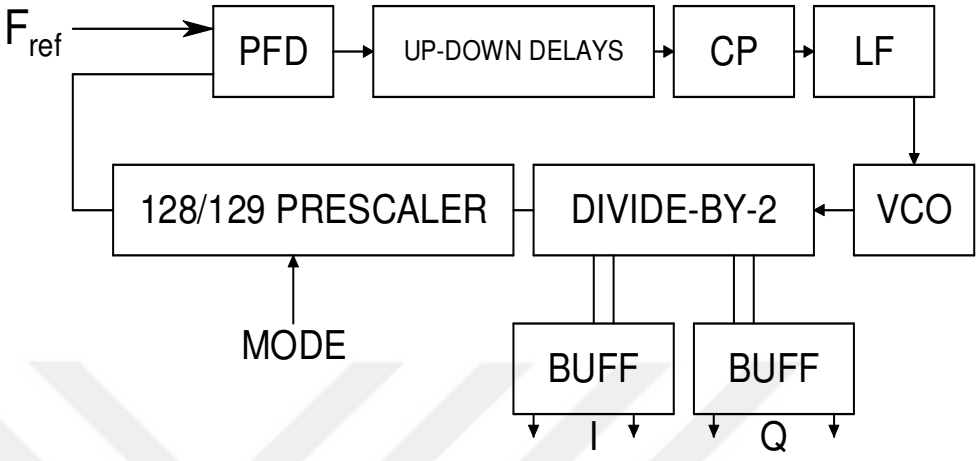


Figure 5.4 Block diagram of the PLL

Fractional-N architecture was chosen for further division. Output of the divide-by-128/129 prescaler circuit is compared with a 3.39-MHz reference frequency. Thus, the reference spurs remain out of 1 MHz channel bandwith of the application.

5.4 Main Building Blocks of the PLL

The following subsections present the design of the individual building blocks.

5.4.1 868-MHz VCO

The 868-MHz VCO presented in Chapter 4 was designed and tested before being integrated into the PLL body. On-chip spiral inductors with the value of 16.9-nH resonate with 1-pF p^+/n-well varactor diodes and other parasitic capacitances to yield 868-MHz oscillation frequency. Unfortunately, the measured center frequency was about 100 MHz less, which means that the tank had to be tuned before the integration. The measured gain of the VCO was about 100 MHz/V. High resistivity substrate and buried-oxide layer in

SOI provide high-Q on-chip spiral inductors. This in return reduced power requirement and phase noise of the VCO. The Q value of these 16.9-nH inductors was 6.2 at 868 MHz. This value was calculated from the π-model circuit parameters extracted from the measured s-parameters. The VCO consumes 5 mW from a 2.5-V supply.

5.4.2 Fast Master-Slave Divide-by-2 Circuit

A very common topology was used for fast divide-by-2 operation [9] [21]. Block diagram of the divider and the schematic of DFF used in the design are given in Figure 5.5. In this design, M3 and M4 would not allow a large voltage drop at the drains of M1 and M2, which otherwise would push M11 into triode region in case of a large VCO output driving this stage. Transistor sizes were arranged to achieve successful division with minimum power consumption. Total power consumption of the circuit was 1.6 mW. Channel width and length of the transistors employed in the design are shown in Table 2.

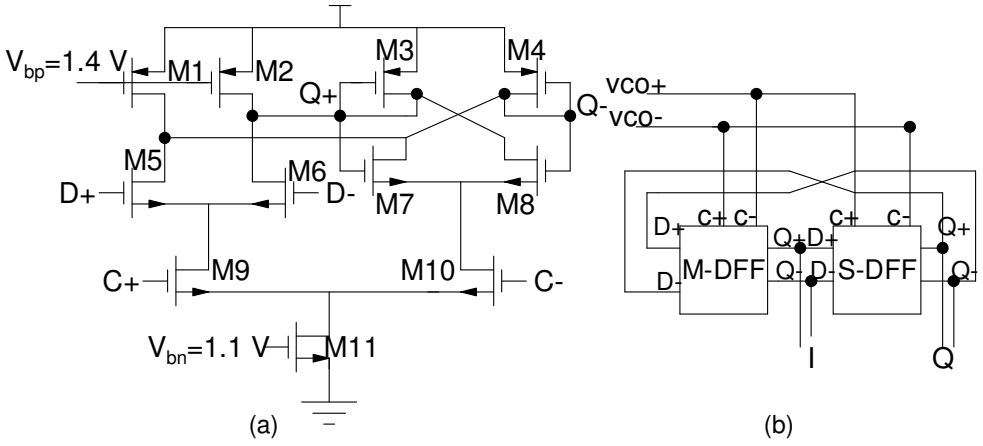


Figure 5.5 (a) Fast D-FF schematic; (b) Master-Slave Divide-by-2

Table 2. Transistor sizing for fast divide-by-2 circuit

Tran.	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11
W\L µm/µm	18/0.5	18/0.5	3.5/0.35	3.5/0.35	5/0.35	5/0.35	18/0.35	18/0.35	9/0.35	36/0.35	18/0.35

5.4.3 Mixer Buffers

In order not to load the divider circuit with the large gates of the mixer input transistors, two buffers were inserted in between. These buffers were simple differential pairs with diode connected load transistors as shown in Figure 5.6. Table 3 shows the transistor sizes employed in these buffers. Each consuming 1.25 mW, these buffers can drive the mixers with 0.5 V swing. Figure 5.7 shows the simulated output of these buffers in a closed-loop operation, driving the estimated 300 fF mixer load. For the measurement purposes, these buffers were resized to be able to drive 50-Ω loads.

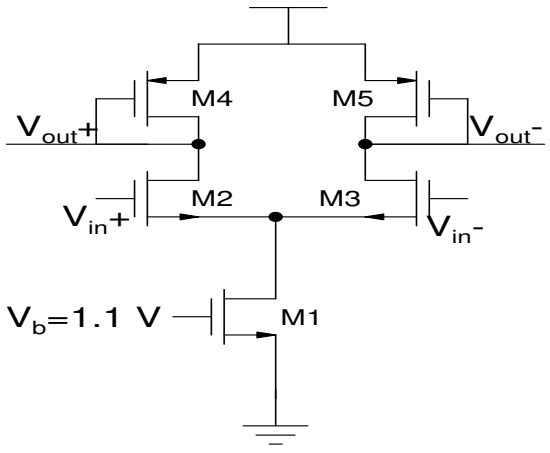


Figure 5.6 Differential buffer schematic

Table 3. Buffer transistor sizing

Tran. W/L	M1	M2	M3	M4	M5
Mixer Load	36µm/0.35µm	18µm/0.35µm	18µm/0.35µm	10.5µm/0.35µm	10.5µm/0.35µm
Meas. Load	72µm/0.35µm	72µm/0.35µm	72µm/0.35µm	18µm/0.35µm	18µm/0.35µm

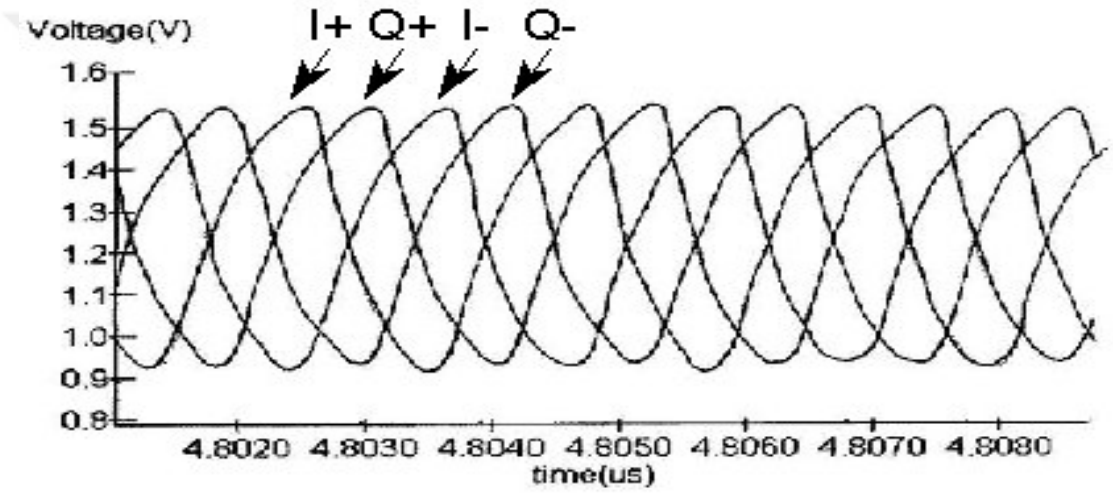


Figure 5.7 Quadrature output signals after the buffers

5.4.4 Prescaler

A 128/129 dual-modulus prescaler follows the fast divide-by-2 circuit. It is inconvenient to use phase select architecture in the design of this block due to the deep spikes observed during the phase switching action in simulations. This is mainly due to the relatively low input frequency of 434 MHz into the prescaler [9]. A very simple design of Figure 5.8 would do the job more efficiently at 434 MHz frequency [22]. Design incorporates a synchronous divide-by-4/5 circuit followed by an asynchronous divide-by-32 circuit. Because this architecture does not employ high power demanding

parts such as quadrature generator and phase switching amplifiers, as in the case of phase select architecture, it consumes less power. This block consumes a total of 4.7 mW power.

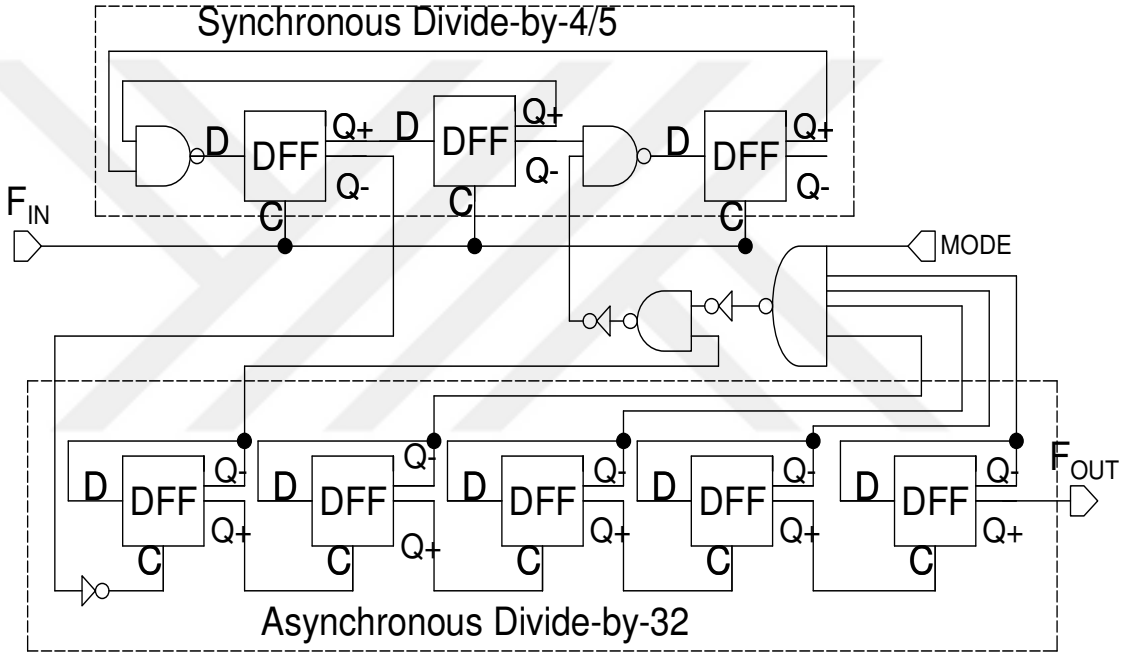


Figure 5.8 128/129 Prescaler schematic

The schematic of the D-flip-flop used in the design is given in Figure 5.9. Proper function of this circuit at 435 MHz frequency was justified in simulations. It does not have any discharge or spike problems as suggested by [22].

The transistors of DFFs employed in divide-by-4/5 circuit are twice as big as those used in low frequency divide-by-32 circuit. Prescaler input and output waveforms from the closed-loop simulations are given in Figure 5.10.

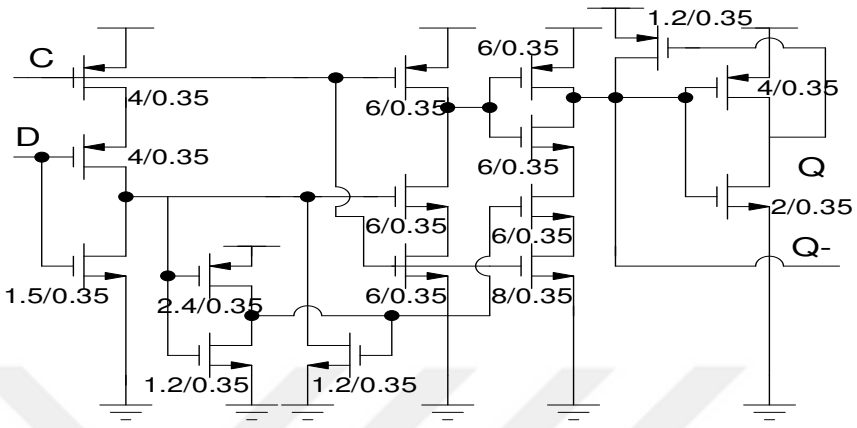


Figure 5.9 D-FF schematic used in prescaler

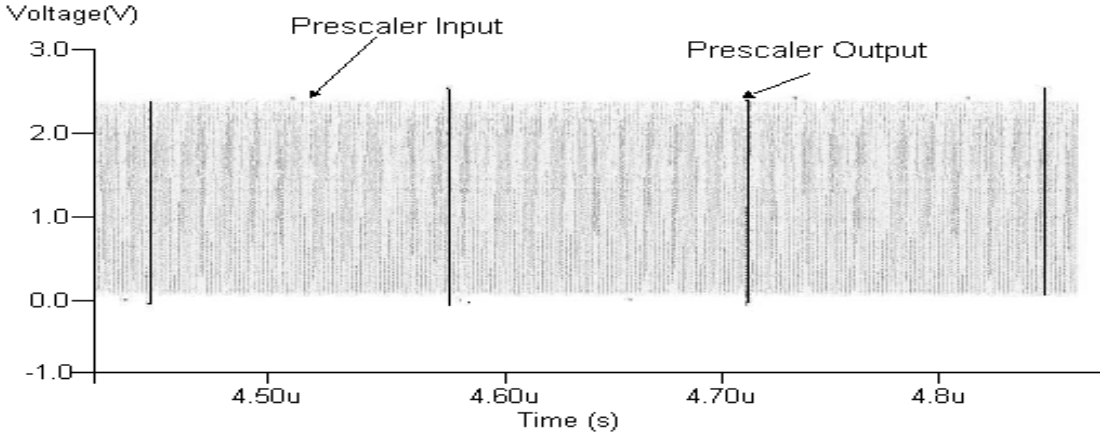


Figure 5.10 Prescaler input and output

5.4.5 PFD-CP

A very basic configuration, two resetable DFFs and a NAND gate with an inverter chain, was used as a phase-frequency detector (PFD). With both outputs of those flip-flops rising high, reset signal was pulled high to reset the both flip-flops [23]. Reset

signal was delayed to avoid the dead zone problem. The circuit schematic of PFD is given in Figure 5.11(a).

In regard to the charge-pump (CP) topology, very simple but effective topology of Figure 5.11(b) was selected [21] [24]. In this design, at high impedance state, up and down source currents were diverted to *M2* and *M8,* respectively, to keep the source transistors in conduction. Very small currents supplied by *M5* and *M11* charged all of the neighboring nodes and left *M1* and *M7* ready to conduct. Delays of up and down control signals of the charge pump were arranged in a way that *M2* and *M8* did not close until *M1* and *M7* began to conduct. Therefore, CP responded to even very small up and down pulses more precisely. Thus, the spurious performance of the PLL would further be improved.

Matching the up and down currents is also a very important aspect of the CP design. If these currents are not matched, the loop will settle to a small phase offset to compensate this current mismatch. In the steady state, the net charge injected will be zero, but since the current pulses are not equal, reference spikes will appear at the output [9]. For this reason, a bandgap based constant current bias circuit was used to supply stable and equal currents with very low temperature coefficients for up and down branches. The transistor sizes for the CP circuit are shown in Table 4 and Table 5. The transistors were sized to have very high accuracy in the *UP* and *DOWN* currents.

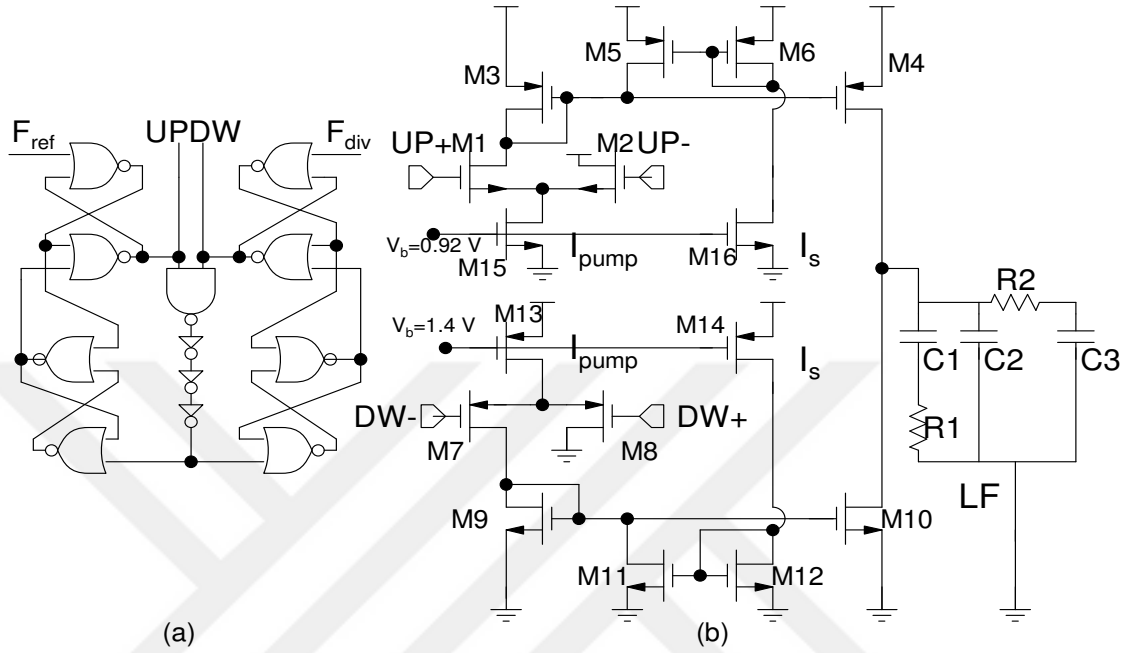


Figure 5.11 (a) PFD schematic; (b) CP and Loop Filter schematic

Table 4. Transistor sizes for M1-M8 of CP circuit

Tran.	**M1**	**M2**	**M3**	**M4**	**M5**	**M6**	**M7**	**M8**
W/L (μm/μm)	9/1	9/1	18/1	18/1	3/2	2.7/2	18/1	18/1

Table 5. Transistor sizes for M8-M16 of CP circuit

Tran.	**M9**	**M10**	**M11**	**M12**	**M13**	**M14**	**M15**	**M16**
W\L (μm/μm)	9/1	9/1	2.65/4	2.7/4	16.95/1	5/6	9/1	2.4/6

5.4.6 Bandgap Based Constant Current Bias Circuit

The bias circuit which was presented in Chapter 2 was used to distribute the necessary stable bias currents to different blocks of this PLL. The temperature insensitive constant current generated by this circuit can be mirrored with proper transistor width ratios to obtain desired current levels. The gates of the PMOS source transistors were fed with a gate voltage of 1.4 V. Two voltage levels, 0.92 V and 1.1 V, were generated and connected to the gates of the NMOS source transistors as shown in Figure 5.12.

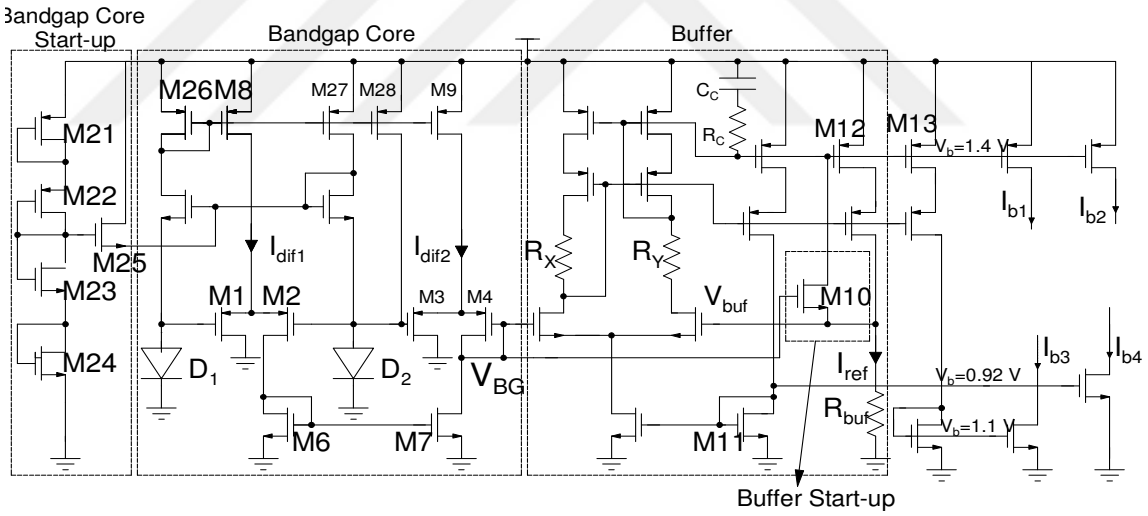


Figure 5.12 Constant-current bias circuit schematic

5.4.7 Loop Filter

The filter used here is third order which makes the loop fourth order. Third order and fourth order loops with the same crossover frequency have very close phase margins and settling times. The additional pole of fourth order PLL located at the vicinity of third

order pole would enhance the spurious performance without reducing the crossover frequency [19]. For the loop characterization, the maximum phase margin that can be achieved depends largely on the capacitor ratio $b = C1/(C2+C3)$ as follows;

$$PM_{\max} = \tan^{-1}(\sqrt{1+b}) - \tan^{-1}(1/\sqrt{1+b}). \quad (5.1)$$

This equation can be derived by taking the derivative of phase margin equation obtained from open loop transfer function with respect to crossover frequency of the loop, ω_c [19]. The value of ω_c for this maximum phase margin is related to τ by $\omega_c = \sqrt{1+b}/\tau$ (5.2) where $\tau = R1C1$. When ω_c is written in terms of loop parameters (from open loop transfer function), the following equation should be satisfied;

$$\frac{I_P \cdot K_{VCO}}{2\pi \cdot N} \cdot \frac{b}{b+1} = \frac{C1}{\tau^2} \cdot \sqrt{b+1}. \quad (5.3)$$

Here, I_P is the charge-pump current, K_{VCO} is the VCO gain and N is the frequency division ratio. For this design, since stability is the most important concern, the value of b was chosen to be 10. Maximum phase margin for this b value is 57° (Equation 5.1). Considering the space budget of the PLL, ω_c was selected to be 72 KHz. Using (5.2), the loop zero should be located 3.3 orders in magnitude to the left of ω_c. To assure the stability further, this zero was located 3.75 orders in magnitude to the left of ω_c. The value of *R1* was chosen to be 46.3 KΩ to have 72 KHz F_C. The *C1* value is thus 180 pF, locating our pole at 19.1 KHz as desired. Using (4), for the given VCO gain of 100-MHz/V, the charge-pump current required is 25.6 μA. From given b value, *C2* and *C3* values were selected as 10 pF and 8 pF, respectively. Thus, the third order pole is at 343 KHz, a value 4.8 orders in magnitude to the right of F_C. A value of 47.6-KΩ for *R2*

would put the fourth pole just to the right of the third order pole (418 KHz). The placement of the poles and zeros in this fashion would significantly suppress the reference spurs which are located at 3.9 MHz.

5.5 Layout Considerations

Layout of the PLL is shown in Figure 5.13. Almost half of the chip area is occupied by the loop filter, located at the right side of the layout. VCO sits at the left side of the layout with two 16.9-nH on-chip spiral inductors. Both available metal layers are used to reduce the series resistance of the coils. Output buffers are resized to drive 50-Ω loads for the measurement purposes, and they consume 5-mW of power from a separate supply pad. On-chip decoupling capacitors are inserted between the Vdd and GND pads. Input pads leading to the gates of the transistors in the design are coupled by ESD diodes. Total chip area is 1.2 mm x 1.6 mm.

5.6 Conclusion

The selection of optimum architectures for quadrature generation, 128/129 dual modulus division and charge-pump for the given single channel wireless application was discussed. A 434-MHz 18.4-mW quadrature output PLL was introduced in 0.35-μm Silicon on Insulator (SOI) CMOS process. The low parasitic nature of the process was utilized to achieve a better PLL performance in terms of power and phase noise.

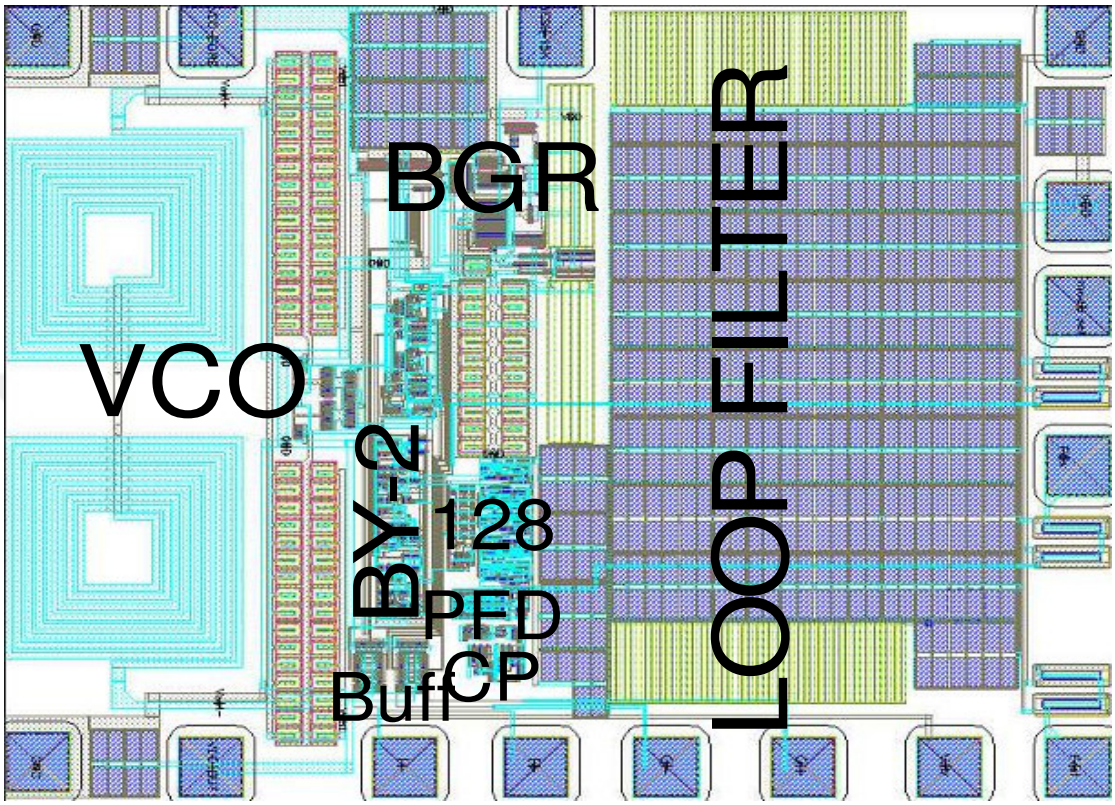


Figure 5.13 Layout of the PLL

CHAPTER 6

CONCLUSION

6.1 Discussion and Conclusion

Every stage of RF IC design was elaborated to design, implement and test some of the front-end blocks of a 435 MHz UHF transceiver, namely, PA, BGR, VCO and PLL in Bulk and SOI CMOS technologies. A very challenging long design path shown in Figure 6.1 were followed for all of the designs presented in this work. First, a literature review was conducted to come up with a solution satisfying the given requirements of the designs. Then, the designs were simulated, laid out and sent to fabrication. At the same time, the testing boards were designed to test the chips after the fabrication. Necessary measurement devices and techniques were investigated to do the testing. During the testing, the designs were tuned for optimum performance. Finally, depending on the outcome of the measurements, target designs were documented or redesigned.

6.2 Future Work

The discrepancies between the simulation results and the measured performances of the chips proved the importance of accurate device modeling for future works. Corner analysis techniques should be investigated to simulate the designs with process variations. More parasitic aware design methodology should be followed to better estimate the behavior of the designs before fabrication (professional layout, pad

allocation and packaging techniques). As a specific future task, PLL design needs to be tested characterized.

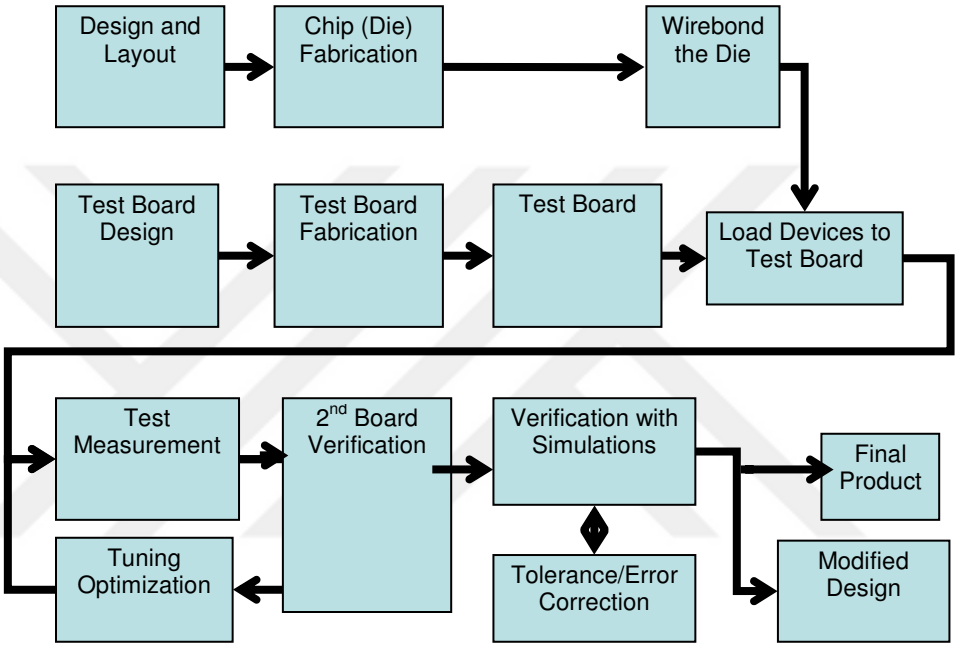


Figure 6.1 Design process for an RF IC design

BIBLIOGRAPHY

[1] N. Lay, C. Cheetham, H. Mojaradi, J.Neal, "Developing low-power transceiver technologies for In-Situ communication applications," *IPN Progress Report* 42-147, 15 Nov. 2001.

[2] Steve C. Cripps, *RF Power Amplifiers for Wireless Communications*, Artech, 1999.

[3] Mona M. Hella, Mohammed Ismail, *RF CMOS Power Amplifiers*, Kluwer Academic Publishers, 2002.

[4] Behzad Razavi, *RF Microelectronics*, Prentice Hall PTR, 1997.

[5] Arne E. Buck, Charles L. McDonald, Stephen H. Lewis, T.R. Viswanathan, "A CMOS bandgap reference without resistors," *ISSCC Dig. Tech. Papers*, pp. 442-443,475, Feb. 2000.

[6] Derek K. Shaeffer, Thomas H. Lee, *The Design and Implementation of Low-Power Radio Receivers*, Norwell, MA: Kluwer Academic Publishers, 1999.

[7] Hironori Banba, et.al, "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE Solid-State Circuits Journal*, vol.34, no.5, pp. 670-674, May 1999.

[8] Todd L. Brooks, Alan L. Westwick, "A low-power differential CMOS bandgap reference," *ISSCC Dig. Tech. Papers*, pp. 248-249, Feb. 1994.

[9] J. Craninckx, M. Steyaert, *Wireless CMOS Frequency Synthesizer Design*, Kluwer Academic Publishers, 1998.

[10] E. Zencir, N. S. Dogan, E. Arvas, "Modeling and performance of spiral inductors in SOI CMOS technology," *IEEE Canadian Conference on Electrical and Computer Engineering*, pp. 408-411, May 2002.

[11] J. Bhattacharjee, D. Mukherjee, E. Gebara, S. Nuttinck, J. Laskar, "A 5.8 GHz fully integrated low power, low phase noise, CMOS LC VCO for WLAN Applications," *IEEE Microwave Symposium Dig.*, vol.1, pp. 585-588, June 2002.

[12] Ahmadreza Rofougaran, Jacob Rael, Maryam Rofougaran, Asad Abidi, "A 900 MHz CMOS LC-Oscillator with quadrature outputs," *International Solid-State Circuits Conference Dig. Tech. Papers,* pp. 392-393, Feb 1996.

[13] Behzad Razavi, "A 1.8 GHz CMOS voltage-controlled oscillator," *ISSCC Dig. Tech. Papers,* pp. 388-389, Feb 1997.

[14] C. M. Hung, K. O. Kenneth, "A packaged 1.1-GHz CMOS VCO with phase noise of -126 dBc/Hz at a 600-kHz offset," *IEEE Journal of Solid State Circuits*, vol.35, no.1, pp.100-103, Jan 2000.

[15] Ali Hajimiri, Thomas Lee, "Design issues in CMOS differential LC oscillators," *IEEE Journal of Solid State Circuits*, vol.34, no.5, pp.717-724, May 1999.

[16] Carl R. C. De Ranter, Michiel S. J. Steyaert, "A 0.25μm CMOS 17GHz VCO," *ISSCC Dig. Tech. Papers,* pp. 370-371, Feb 2001.

[17] Francesco Svelto, Stefano Deantoni, Rinaldo Castello, "A 1.3 GHz low-phase noise fully tunable CMOS LC VCO," *IEEE Journal of Solid State Circuits*, vol.35, no.3, pp.356-361, March 2000.

[18] Tamara I. Ahrens, Thomas H. Lee, " A 1.4 GHz 3-mW CMOS LC low phase noise VCO using tapped bondwire inductances," *IEEE International Symposium on Low Power Electronics and Design*, pp. 16-19, Aug 1998.

[19] Hamid R. Rategh, Thomas H. Lee, *Multi-GHz Frequency Synthesis & Division*, Kluwer Academic Publishers, 2001.

[20] H. Hegazi, K. Sharaf, H.F. Ragai, "A comparative study of CMOS-based quadrature integrated LC VCO topologies," *45th Midwest Symposium on Circuits and Systems*, vol.1, pp.I-336-9, Aug. 2002.

[21] James F. Parker, Daniel Ray, "A 1.6-GHz CMOS PLL with on-chip loop filter," *IEEE Journal of Solid State Circuits*, vol.33, no.3, pp.337-343, March 1998.

[22] R. Rogenmoser, Q. Huang, F. Piazza, "1.57 GHz asynchronous and 1.4 GHz dual-modulus 1.2 μm CMOS prescalers," *IEEE Custom Integrated Circuits Conference*, pp. 387-390, May 1994.

[23] Jafar Savoj, Behzad Razavi, *High-Speed CMOS Circuits for Optical Receivers*, Kluwer Academic Publishers, 2001.

[24] Andreas Lehner, Robert Weigel, Dieter Sewald, Ali Hajimiri, "Design of a novel low-power 4^{th}-order 1.7 GHz CMOS frequency synthesizer for DCS-1800," *IEEE International Symposium on Circuits and Systems*, pp.637-640, May 2000.

[25] H. M. Greenhouse, "Design of Planar Rectangular Microelectronic Inductors," *IEEE Trans. Parts, Hybrids, and Packaging*, v. PHP-10, no. 2, pp. 101-109, June 1974.

[26] C. P. Yue, C. Ryu, J Lau, T. H. Lee, S. S. Wong, "A physical model for planar spiral inductors on silicon," *IEEE IEDM '96*, pp. 155-158, 8-10 Dec. 1996.

[27] A. Zolfaghari, A. Chan, B. Razavi, "Stacked Inductors and Transformers in CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp.620-628, Apr. 2001.

[28] C. Tang, C. Wu, S. Liu, "Miniature 3-D Inductors in Standard CMOS Process," *IEEE J. Solid-State Circuits*, vol. 37, no. 4, pp. 471-480, Apr. 2002.

[29] International Business Machine (IBM), *SOI white paper*, IBM, available from Internet http://www-3.ibm.com/chips/bluelogic/showcase/soi/soipaper.pdf.

[30] B Lee, "Modeling of Chemical Mechanical Polishing for Shallow Trench Isolation," PhD dissertation, Massachusetts Institute of Technology, 2002;

available from Internet: http://www-mtl.mit.edu/Metrology/PAPERS/Lee-PHD2002-Thesis.pdf.

APPENDIX

DEVICE STRUCTURES

In this appendix, the device structures in two different processes, the Agilent 0.6 µm bulk CMOS (AMOS14TB) and Honeywell 0.35µm SOI CMOS (MOI5), are presented. The chapter covers first passive devices—resistors, capacitors, and inductors, and then active devices—nMOS, pMOS and diodes.

It is indeed the *wafers* that result in different device characteristics between bulk and SOI CMOS technologies. To discuss these differences and similarities, it is appropriate to compare the bulk and SOI first. Figure A1.0.1 shows a typical way to prepare a SOI wafer.

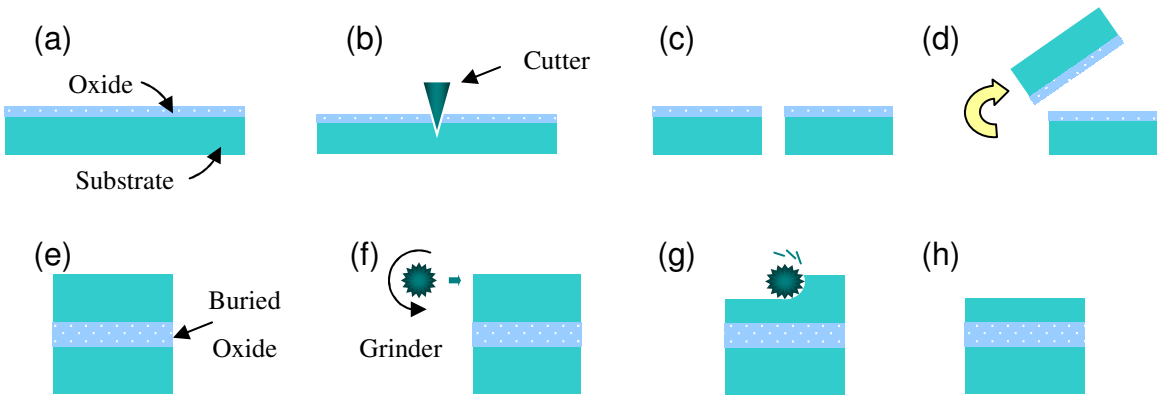


Figure A1.0.1 Preparation for an SOI substrate

The steps are described below:

1. Grow silicon oxide on the substrate (Figure A1.0.1(a)).

2. Vertically cut the substrate into two (Figure A1.0.1(b) and Figure A1.0.1(c)).

3. Flip one of the substrate (Fig. A1.0.1(d)) and glue them oxide to oxide (Figure A1.0.1(e)). The oxide sandwiched between the substrates is called the Buried Oxide—BOX.
4. Use rotary grinder to cut thin the upper substrate (Figure A1.0.1(f) and Figure A1.0.1(g)).
5. The SOI wafer (Fig. A1.0.1(h)) is now ready to be used for CMOS transistors, resistors, capacitors, inductors, diode…etc. fabrications.

Figure A1.0.2 shows the bulk and SOI wafers. Although SOI process has couple of extra processing steps increasing the cost of the process, it has many advantages such as parasitic reduction and device isolation. Subsequent sections discuss the device structures on these wafers.

.

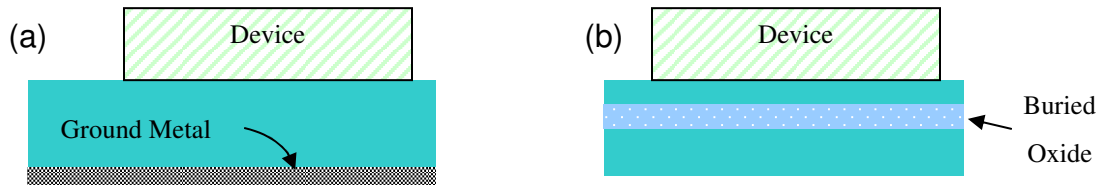


Figure A1.0.2 Bulk and SOI substrates

Appendix 1.1 Resistors

The following three subsections will discuss three types of resistors: the well resistors, the diffusion resistors, and poly resistors.

Appendix 1.1.1 Well Resistors

Figure A1.1.1 shows an n-well resistor structure in the AMOS14TB bulk CMOS process. Due to variations in n-well depth formation in the fabrication processes, well resistor typically has 25% variation in sheet resistance. Well resistors are used when precise resistance values are not needed. Figure A1.1.2 shows a P-Well resistor structure in the MOI5 SOI CMOS process. Since the substrate is very thin, the sheet resistance of SOI well resistor is much higher than those of bulk CMOS processes. Typical sheet resistance of a P-Well resistor in the MOI5 is about 6000[$\Omega/_{[]}$]. Furthermore, the buried oxide (insulator) in SOI process reduced the field leakage from the substrate. High sheet resistance and low leakage make well resistors in SOI process more desirable than bulk CMOS processes.

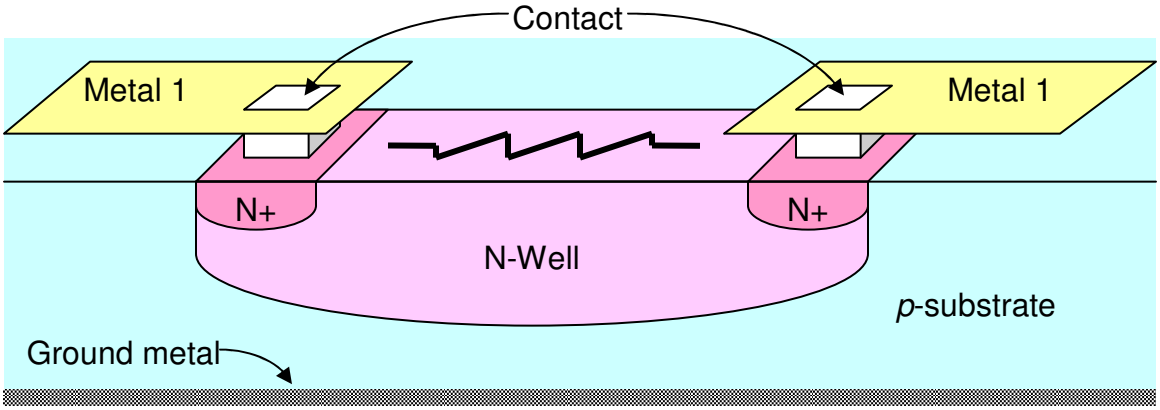


Figure A1.1.1 AMOS14TB N-well resistor with active contacts to Metal 1

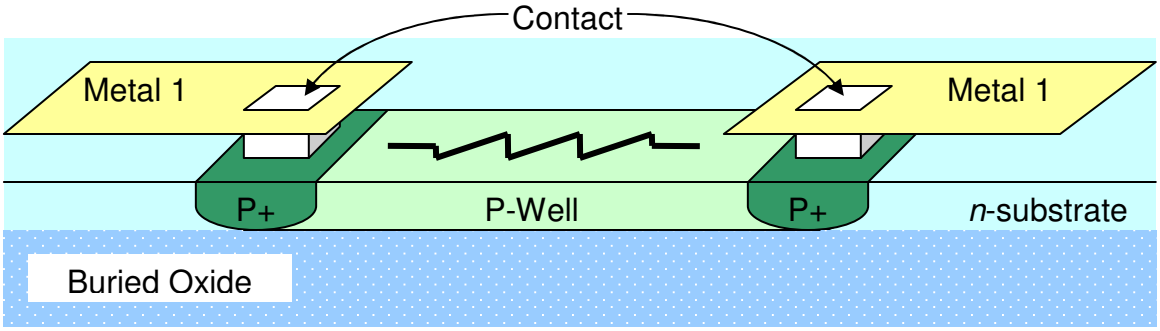


Figure A1.1.2 MOI5 P-well resistor with active contacts to Metal 1

Appendix 1.1.2 Diffusion Resistor

P+ diffusion resistors are placed inside an n-well (Figure A1.1.3) whereas n+ diffusion resistors are placed in the p+ substrate (Fig. A1.1.4). In the case of a silicide technology, for like the AMOS14TB, the diffusion layers have a low resistive layer above them. The original intention was to reduce the drain and source resistance for the transistors. The composite layer has low sheet resistivity below 10[$\Omega/_{[]}$].

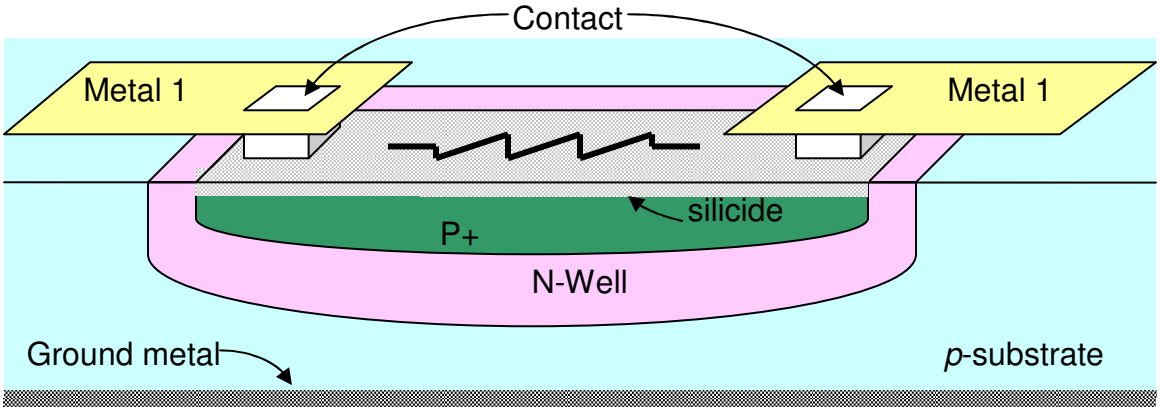


Figure A1.1.3 AMOS14TB P+ diffusion resistor with active contacts to Metal 1

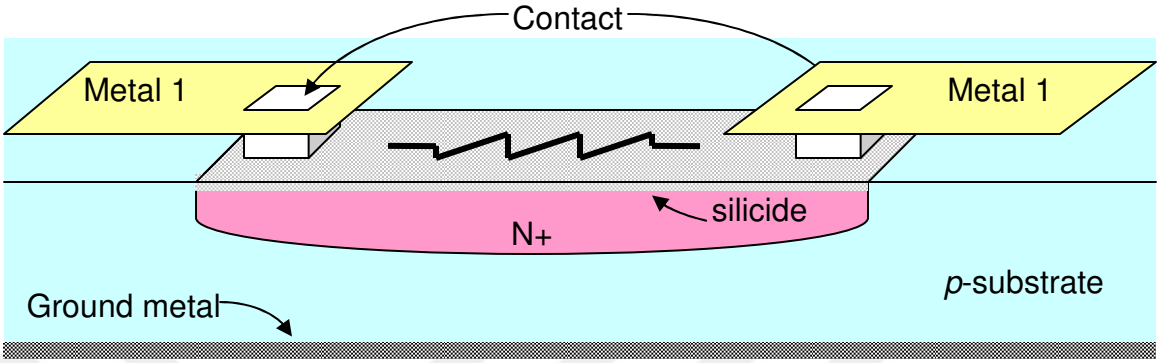


Figure A1.1.4 AMOS14TB N+ diffusion resistor with active contacts to Metal 1

Sometimes an additional mask is used to block the silicidation process; the resistance can be greatly increased. For example the MOI5 N+ diffusion resistor shown in Figure A1.1.5; besides the thinness of the substrate layer (as discussed in the previous subsection), blocking the silicidation makes its typical sheet resistance 575[$\Omega/_{[]}$].

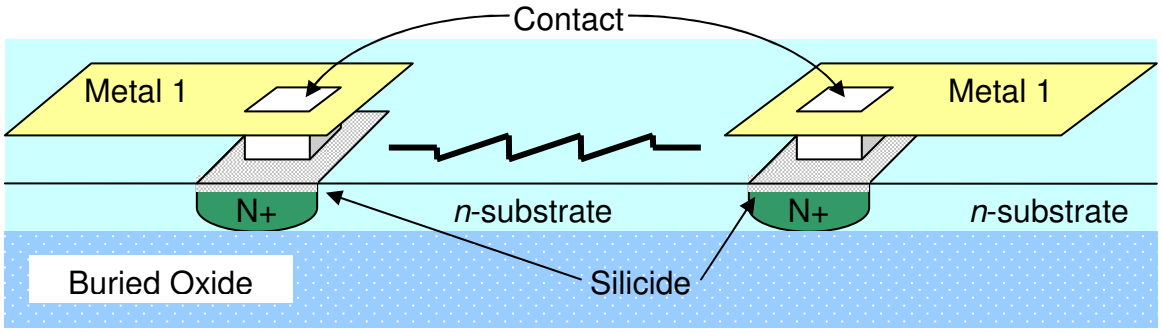


Figure A1.1.5 MOI5 N+ diffusion resistor with active contacts to Metal 1

Appendix 1.1.3 Polysilicon Resistor

Polysilicon resistor is actually gate polysilicon without the diffusion layers. Similar to the previous subsection, one may design polyresistors with or without

salicidations (Figure A1.1.6 and Figure A1.1.7). Salicidation of polysilicon results in low resistivity .

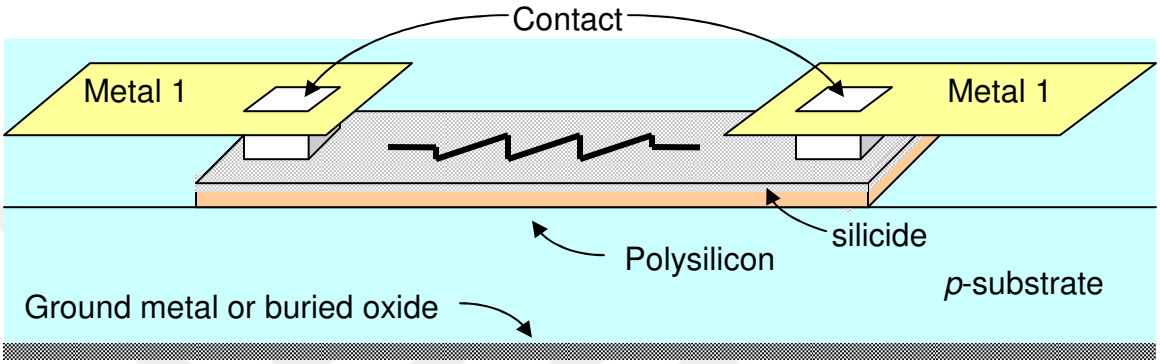


Figure A1.1.6 Polysilicon resistor (with silicide layer) with active contact to Metal 1

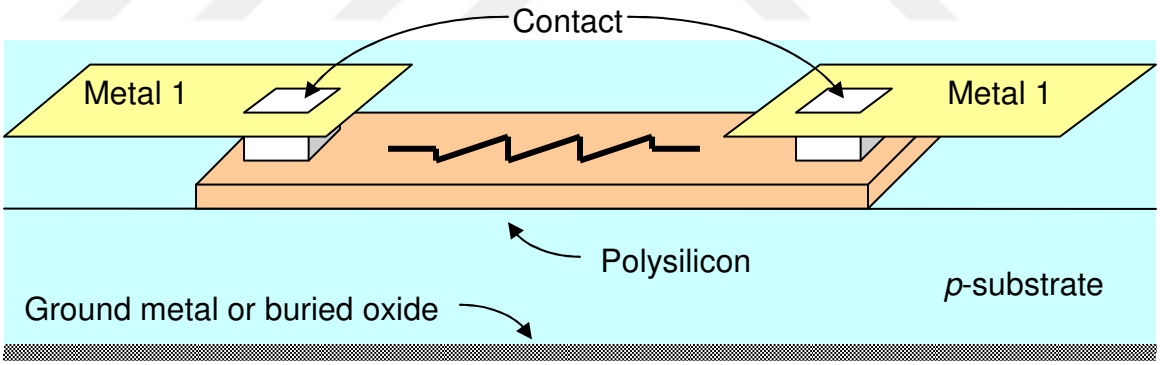


Figure A1.1.7 Polysilicon resistor (without silicide layer) with active contact to Metal 1

In the bulk CMOS process, one may like to shield the polysilicon resistors from noise injected from the substrate by putting the resistor in an N-Well biased to a quiet voltage (Figure A1.1.8). Note that the quiet voltage must not be too low to turn on the parasitic diode. SOI polysilicon resistors are very well confined locally. Generally speaking, they do not need this shielding technique.

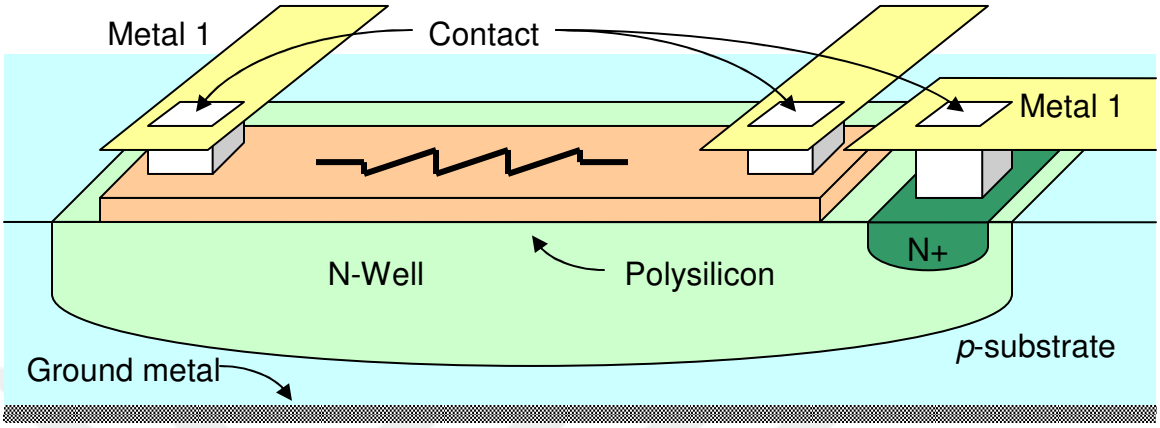


Figure A1.1.8 Polysilicon resistor with N-Well shielding

The temperature and voltage coefficients are very low for polysilicon resistors. These make the polysilicon resistor one of the most linear resistors in CMOS processes. Even with this linearity, designers should avoid minimum layout width for resistors if precise resistance values are need.

Appendix 1.2 Capacitors

Two commonly used linear capacitors are explained in the following subsections.

Appendix 1.2.1 Poly-Diffusion Capacitor

Poly-diffusion capacitor (Fig. A1.2.1) is one of the most commonly used linear capacitor in CMOS process. The capacitor is formed between the silicide (polysilicon) layer and the N+ diffusion area. The material between two plates is the gate oxide. The constant C_{ox} is defined as the capacitance per unit area of the gate oxide. $C_{ox} \equiv \frac{\varepsilon_{ox}}{t_{ox}}$ (A1.2.1)

where ε_{ox} and t_{ox} are the permittivity and and thickness of the gate oxide, respectively.

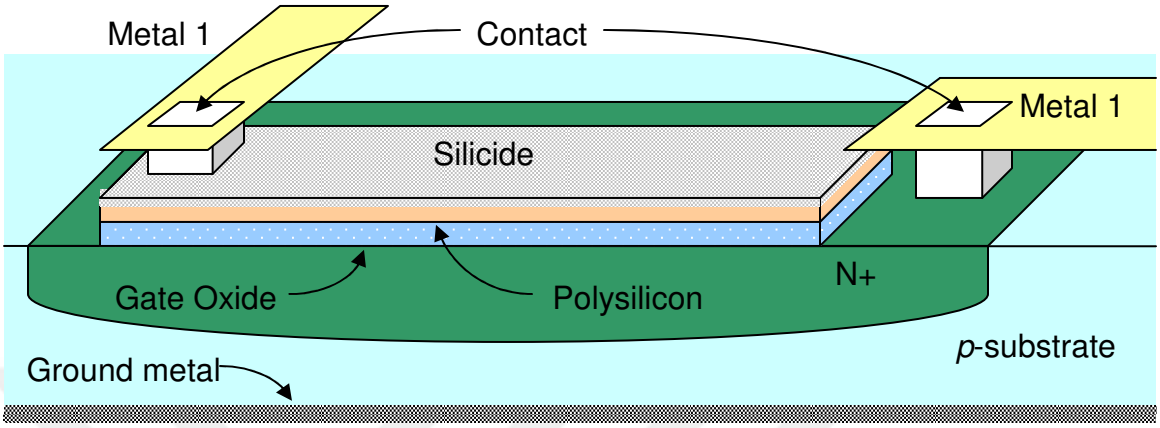


Figure A1.2.1 Polysilicon-diffusion capacitor

Typical dielectric constant for silicon oxide, SiO_2, is $\varepsilon_r \approx 3.9$, and the oxide thickness is about 70 to 170[$\mathring{A}$] (1 angstrom=10^{-10}m). Therefore, a typical value for C_{ox} is about 2 to 5 [mF/m^2] or 2 to 5 [f$F/\mu m^2$].

$$C_{ox} = \frac{3.9 \times \frac{1}{36\pi} \cdot 10^{-9}[F/m]}{170 \cdot 10^{-10}[m]} \sim \frac{3.9 \times \frac{1}{36\pi} \cdot 10^{-9}[F/m]}{70 \cdot 10^{-10}[m]} = 2 \sim 5[\frac{mF}{m^2}] \qquad \text{(A1.2.4)}$$

Two things have to be mentioned about the poly-diffusion capacitor in bulk CMOS process (Fig. A1.2.2). First, similar to the diffusion resistor, operating poly-diffusion capacitor at too low voltage will turn on the implicit diode (*p*-substrate/N+) and cause problems. Second, since the ground plate is parallel with the capacitor plates, the parasitic capacitance can be as large as 10-30% of the main capacitance. Note that without the ground plate (or the ground plate very far away), these two problems do not appear in SOI CMOS process.

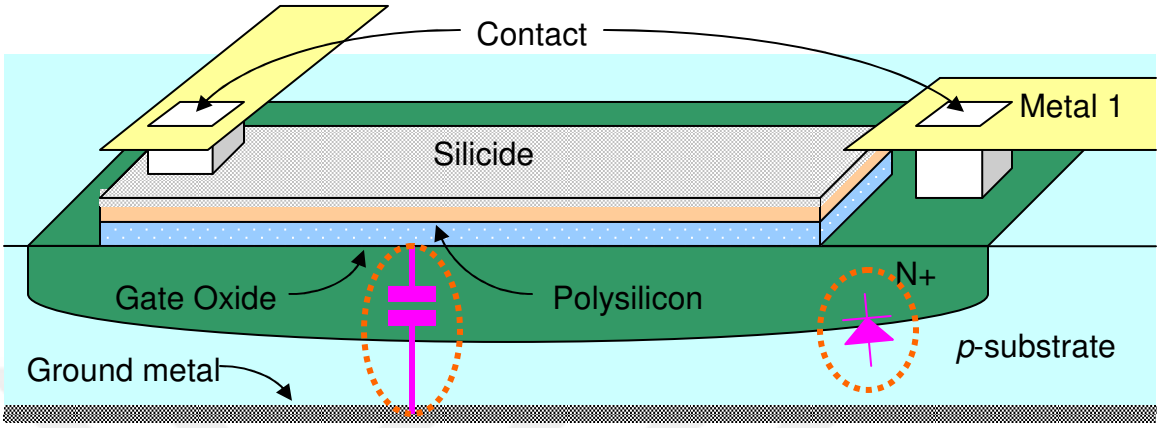


Figure A1.2.2 Parasitic diode and capacitance in bulk CMOS poly-diffusion capacitor

Both the silicide layer and N+ layer have sheet resistance of a few [$\Omega/_{[]}$], the capacitor may contain high values of sereies resistance if the layout is too large. Typical ways to solve this problem are by limiting the width of the capacitor, using as many contacts as possible and drawing the layout in a symmetrical manner. Drawing the capacitor layout in a 'wide' manner (between terminals) can reduce the series resistance (Figure A1.2.3). When a large capacitance value is needed, it is more convenient to break it into shunt-connection of small capacitors. The temperature coefficient of poly-diffusion capacitor is about 0.00025/°C.

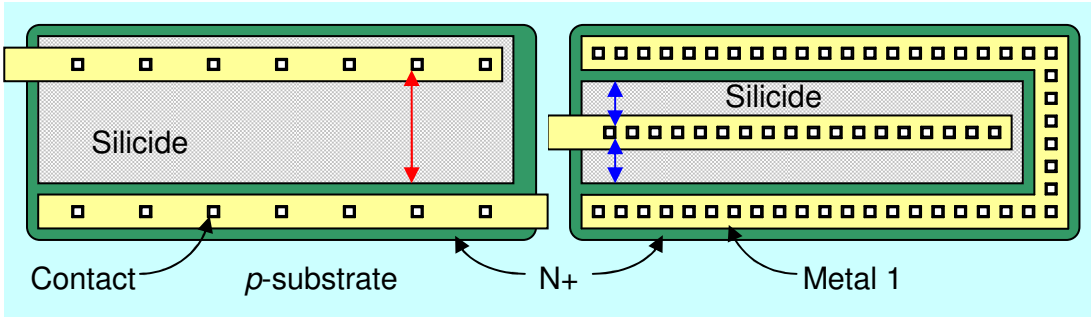


Figure A1.2.3 Reduction of sereies resistance in poly-diffusion capacitor (Top view.)

Appendix 1.2.2 Metal-Metal Capacitor

There are three main benefits of metal-metal capacitors: First, low parasitics. In the semiconductor process, metal layers are always above the polysilicon layers. Far away from the ground plate, metal-metal capacitor usually has less parasitic capacitance to ground than the poly-diffusion capacitors. Second, low series-resistance. Without the contacts (metal1/poly and metal1/N+) and with virtually zero sheet resistance, metal-metal capacitors present almost no series resistance. Third, low voltage coefficients. The material between terminal plates is field oxide only. There is no hidden p-n junction like poly-diffusion capacitors. The downside of metal-metal capacitor is the thick field oxide between the metal layers. This makes the C_{ox} low (about 1/100~1/30 of the gate oxide), thus large area is required.

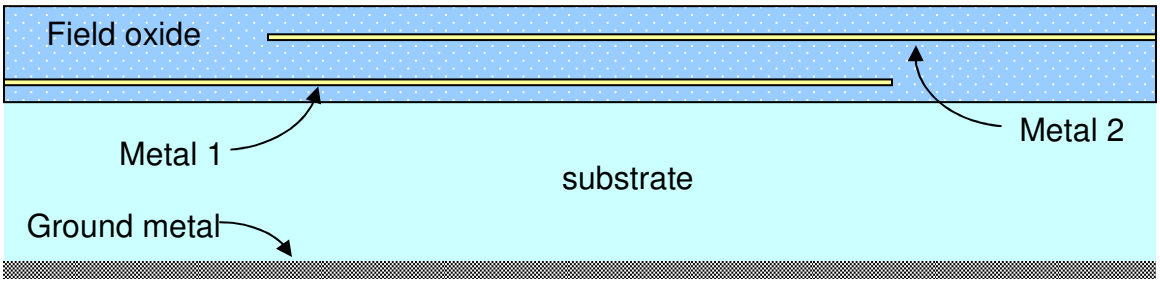


Figure A1.2.4 Metal-metal capacitor

Appendix 1.3 Inductors

In this section, integrated spiral inductors are discussed. Three commonly seen spiral inductor shapes are shown in Figure A1.3.1. A square or rectangular spiral inductor (Figure A1.3.1(a)) has the highest area efficiency but low-Q. The circular spiral inductor

(Figure A1.3.1(b)) has the highest Q but occupies the largest area. An octagonal spiral inductor (Figure A1.3.1(c)) is the tradeoff between circular and rectangular inductors.

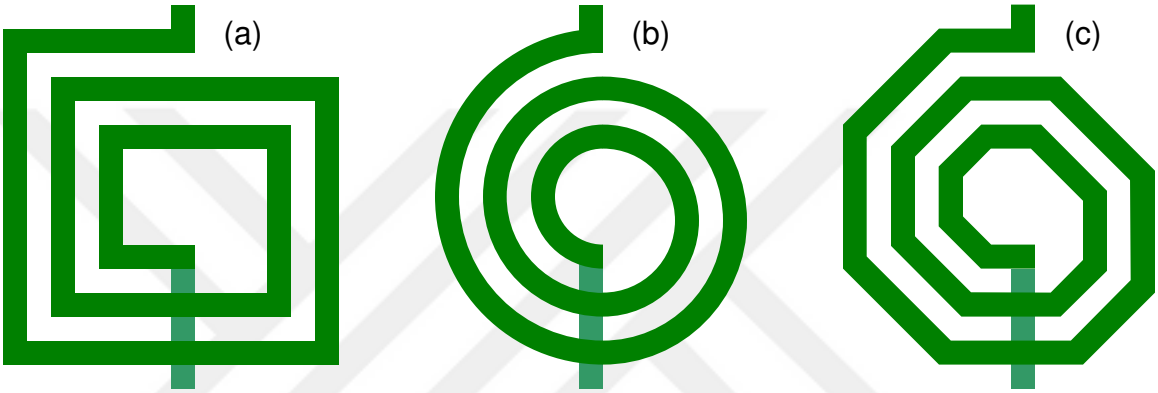


Figure A1.3.1 Different shapes of spiral inductors (a) square; (b) circular; (c) octagonal

The spiral inductor can be modeled with a pi network as shown in Figure A1.3.2. As a rule of thumb, the inductance L_S is proportional to the total winding length, and the series resistance R_S is proportional to the total winding length and inversely proportional to the winding width. In many cases, the parasitic capacitance between ports C_p, the field oxide capacitance C_{oxL}, substrate resistance R_{sub} and substrate capacitance C_{sub} can be omitted.

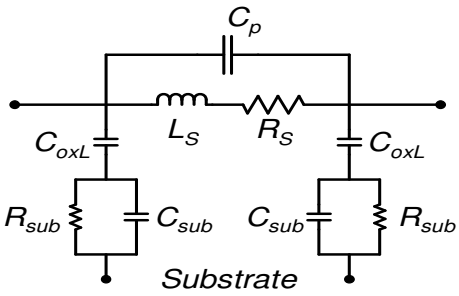


Figure A1.3.2 Pi-model of a spiral inductor.

Appendix 1.3.1 Rectangular Spiral Inductor

Among the three different shapes of spiral inductors, rectangular (Figure A1.3.1(a)) is the most widely used. The inductance of spiral is a complicated function of geometry. Accurate calculations require the use of field solvers or Greenhouse's method [25]. The dimensions required for a first order inductance estimation are given in Figure A1.3.3.

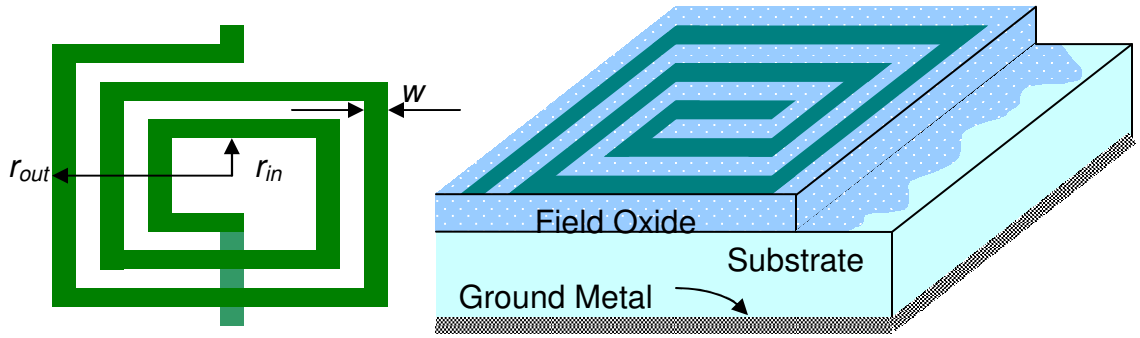


Figure A1.3.3 Square spiral inductor dimensions

For a first-order estimate, the pi model parameters for the rectangular spiral inductor of Figure A1.3.3 are [26]:

$$L_S \approx \frac{75\mu_0 n^2 (r_{out} + r_{in})^2}{120 r_{out} - 56 r_{in}} \text{ [nH]} \tag{A1.3.1}$$

$$R \approx \frac{N}{\sigma \cdot \delta (1 - e^{-t/\delta})} \text{ [}\Omega\text{]} \tag{A1.3.2}$$

$$C_p \approx n \cdot w^2 \cdot \frac{\varepsilon_{ox}}{t_{ox}} \text{ [F]} \tag{A1.3.3}$$

$$C_{oxL} \approx \frac{1}{2} \cdot w \cdot l \cdot \frac{\varepsilon_{ox}}{t_{ox}} \text{ [F]} \tag{A1.3.4}$$

$$R_{sub} \approx \frac{2}{w \cdot l} \cdot R_{subs} \text{ [}\Omega\text{]} \tag{A1.3.5}$$

$$C_{sub} \approx \frac{1}{2} \cdot w \cdot l \cdot C_{subs} \text{ [F]} \tag{A1.3.6}$$

where n [no unit] is the number of winding turns. r_{out} [m] and r_{in} [m] are the outer and inner winding radius, respectively. w [m] and l [m] are the winding width and total winding length, respectively.

$N \approx \frac{l}{w}$ is the number of square counts of the winding.

$\delta = \sqrt{\frac{2}{\omega \mu_0 \sigma}}$ [m] is the skind depth of the winding metal. $\sigma \approx 1 \times 10^7$ [1/(Ω·m)] for copper.

ε_{ox} [F/m] and t_{ox} [m] are the permittivity and thickness of the field oxide between the windings and the substrate, respectively. R_{subs} [Ω/m^2] and C_{subs} [F/m^2] are the filling constants of the substrate, respectively, according to the material and its thickness. When

the inductor is far away from the ground plate and when the inductor size is small, the shunt terms (C_{oxL}, R_{sub} and C_{sub}) in the pi model become insignificant. If we assume all C_{oxL}, R_{sub}, C_{sub} and C_p are very small, the quality factor Q of the inductor model shown in Fig. A1.3.2 can be approximated to $Q \approx \omega_0 \cdot \frac{L_S}{R_S}$ (A1.3.7)

where ω_0 [radian] is the resonance frequecy of the inductor. According to (A1.3.7), there are two ways to improve spiral inductor Q. One is to increase self resonance frequency. The other is to reduce series resistance R_S.

Since both L_S and R_S are proportional to the total winding length, an effective way to increase spiral inductor Q is to reduce the sheet resistance of the winding. It is intuitive to increase the metal width to increase inductor Q. Increasing the metal width does reduce series resistance R_S, but the shunt capacitance is increased also. It is because the more metal area that is exposed, the more fringing field incurs, therefore, the higher shunt capacitance appears between input and output nodes. As a result, the quality factor Q of the inductor does not change much. Do not forget that (A1.3.7) is only an approximation, and C_p was assumed to be very small. Another drawback of using wide metal winding is the large die area required. This does not appear to be attractive in most (if not all) situations.

Appendix 1.3.2 Multilayer Spiral Inductor

Taking the advantage of a multi metal layer CMOS process, multilayer spiral inductors are commonly used by engineers. Figure A1.3.4 shows the idea of multilayer spiral inductors.

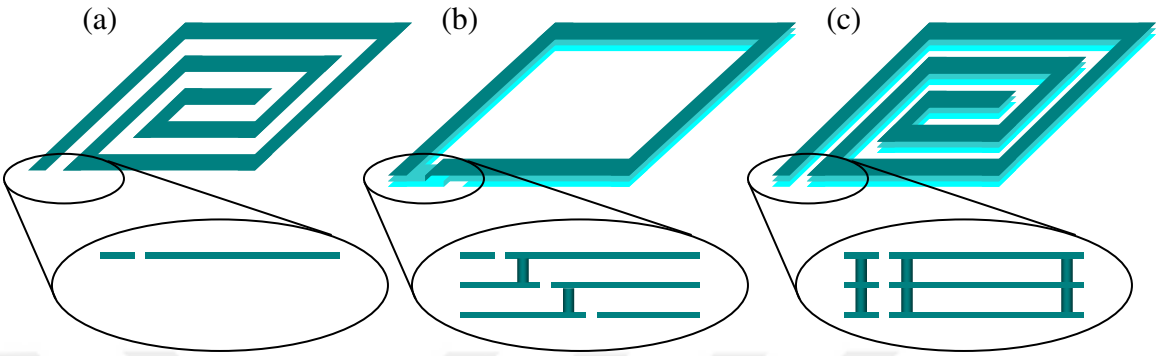


Figure A1.3.4 Single- and multi- layer spiral inductors

Because of the mutual inductance between metal layers, the multilayer stacked inductors (Figure A1.3.5) have much higher inductance than single layer ones [27]. A first-order approximation of inductance in the multilayer structure is $L_{tot}=m^2L_S$ (A1.3.7) where L_S is the inductance of a single layer spiral calculated form (A1.3.1), and m is the number of metal stacks of spirals.

In the three-dimensional spiral inductor designs, the self resonance frequency is greatly improved. It is recommended to increase the distance between layers of spirals. For example, if two layers of spirals are needed, using metal4 and metal1 will result in higher self resonance frequency than using metal4 and metal3. By rearranging the routing of the metals (Figure A1.3.5(b)), the self resonance frequency can further be improved by 34% [28]. Besides higher self-resonance frequency, another benefit of this type of multilayer inductor is that a smaller die area is required than most other architectures. Because the inner turns are now put under the outer turns. The diameter of the inductor is shrunk.

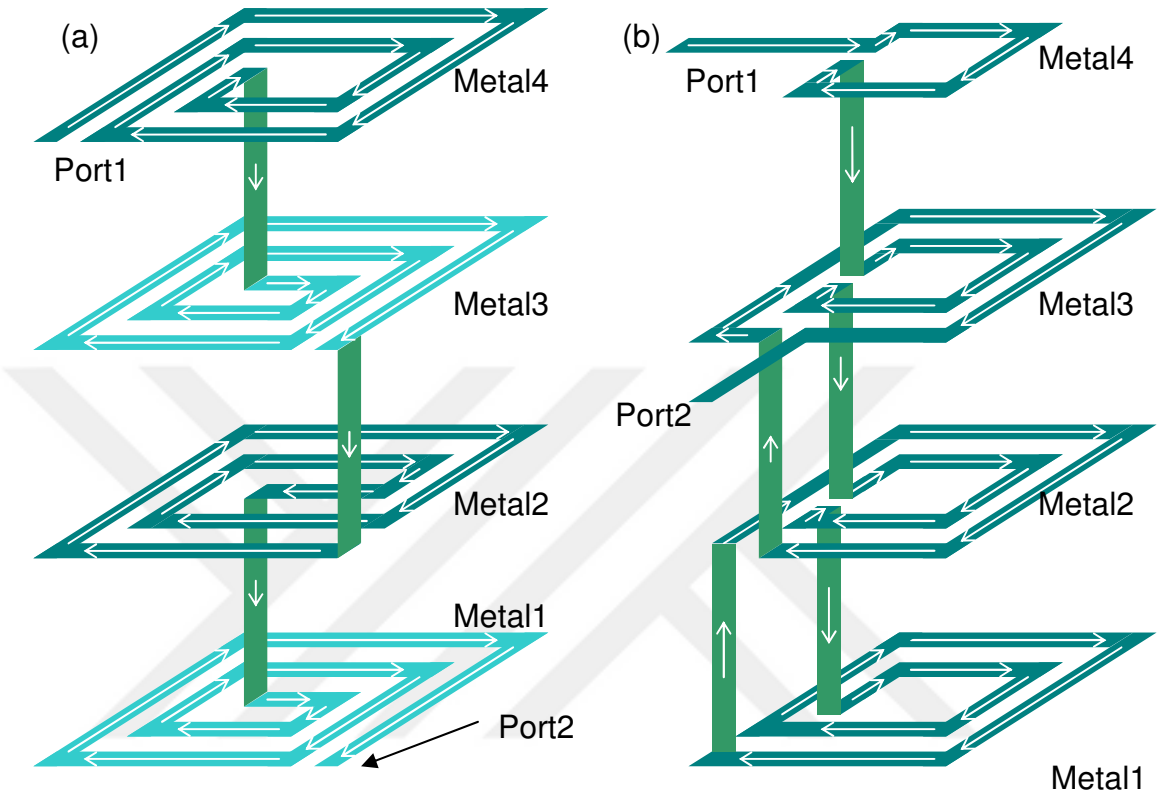


Figure A1.3.5 Three-dimensional multilayer spiral inductors

The quality factor Q of the inductors was almost not improved. This is because both the series resistance and inductance are proportional to the length of the winding. Since resistance did not change much, the quality factor would not change much. Another reason is because the shunt capacitance C_p was not necessarily reduced in the 3-D structure. If the input and output port locate at different layers, the interaction between ports could be weak and make C_p small. On the other hand, since the metal layers are close to each other, not only mutual inductance increased, the shunt capacitance may also increase.

Three-dimensional spiral inductors are highly recommended by engineers yet some practical hindrances exist. First, note that for stacked 3-D spiral inductor an even number of metal layers are needed. We need the same numbers of metal layers to go in and to come out of the inductor. This may not always be available; for example, AMOS14TB uses three metal layers. Second, different metal layers may have different sheet resistances. Also note that contact resistances between different metal layers may be different. These make calculating inductor series resistance difficult.

Another popular way of using the multilayer spiral inductor is shown in Figure A1.3.6. All the metal layers are tied in shunt with contacts. This is to increase the cross section of the inductor windings. Shunt connecting multilayer inductors (Fig. A1.3.6) reduces the series resistance R_S without changing inductance L_S and capacitance C_p.

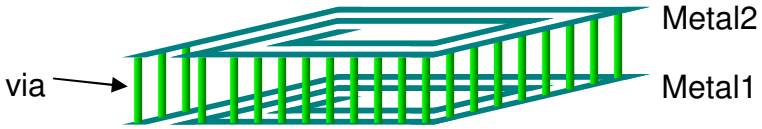


Figure A1.3.6 Shunt connected multilayer spiral inductors

Appendix 1.4 Transistors

Transistors are the most important active devices in CMOS technology. This section describes the transistor device structure in bulk and SOI CMOS.

Appendix 1.4.1 NMOS Transistor

Physically, SOI CMOS transistors differ from bulk CMOS transistors in three major ways. First, the bottom ground plate is absent and replaced by an insulator layer—buried oxide. Therefore, the potential of the transistor wellbody is no longer limited to a global value, usually the ground voltage. Second, the substrate is thin enough that the N+ implant directly touches the buried oxide. This effectively reduces contact capacitance between the implant and the substrate and increases the transistor speed [29]. Third, the transistor wellbody is tied to the source terminal. This is done by first implanting a small P+ region right next to the transistor source N+ region, and by siliciding them. Since the P-well (transistor body) had the same voltage of P+ region that is in it, and the voltage of the P+ region was equalized to the N+ region (transistor source) potential because of salidation, the transistor body is therefore connected to the transistor source. The shallow trench isolation (STI) is implanted in a vertical way to build a wall around the transistor [30]. The transistor, voltage wise, is now isolated from the substrate. Each individual SOI transistor has its body voltage locally defined and equal to its source voltage. As a consequence, there is no (or negligible) body effect in the SOI CMOS transistors. Figure A1.4.1 shows the differences between these two NMOS transistors—bulk at the left and SOI at the right.

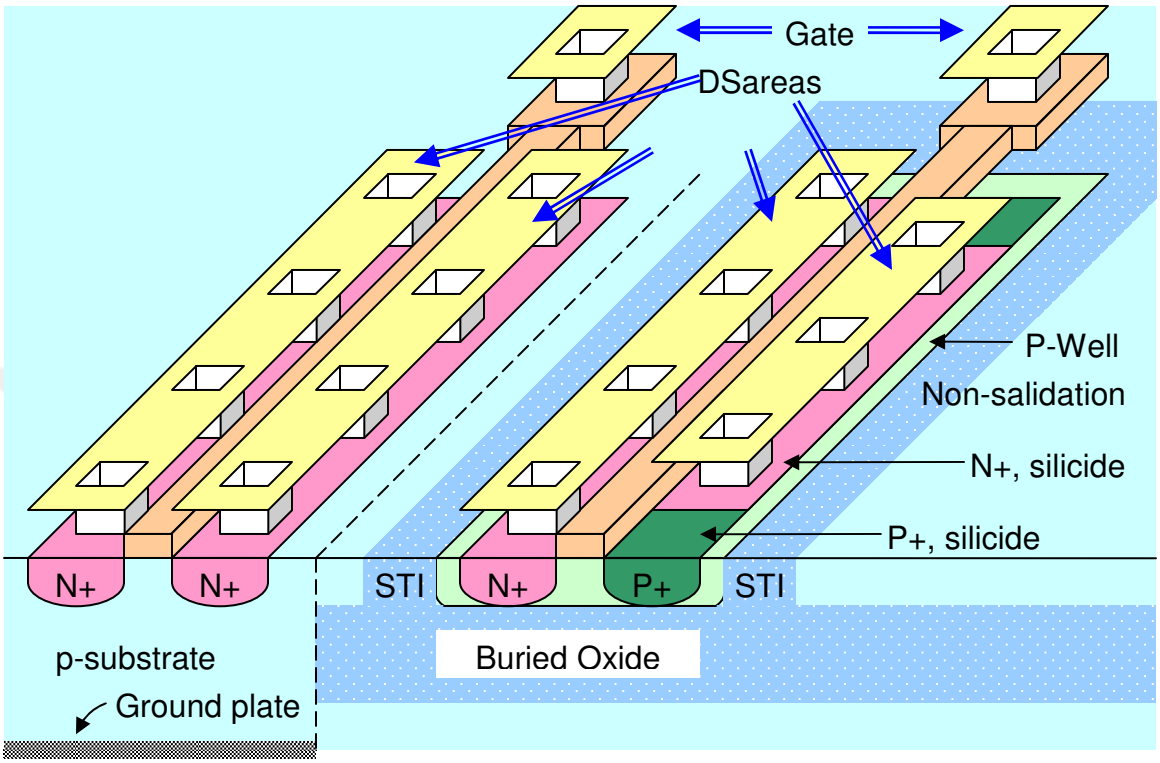


Figure A1.4.1 Bulk and SOI NMOS transistor

Appendix 1.4.2 PMOS Transistor

PMOS transistor is the complement of the NMOS transistor in a CMOS process. Besides swapping P and N, the only difference is that an n-well is needed before implanting a PMOS. On the other hand, P-well may not be needed to implant an NMOS because p-substrate is usually used in CMOS process. On the other hand, since the hole is the carrier in the PMOS device, the transconductance is smaller than that of an NMOS. As a consequence, a much larger (usually three times) area is needed to implant a PMOS to have same 'gain' as its complementary partner NMOS. Figure A1.4.2 shows two PMOS transistors—bulk at the left and SOI at the right.

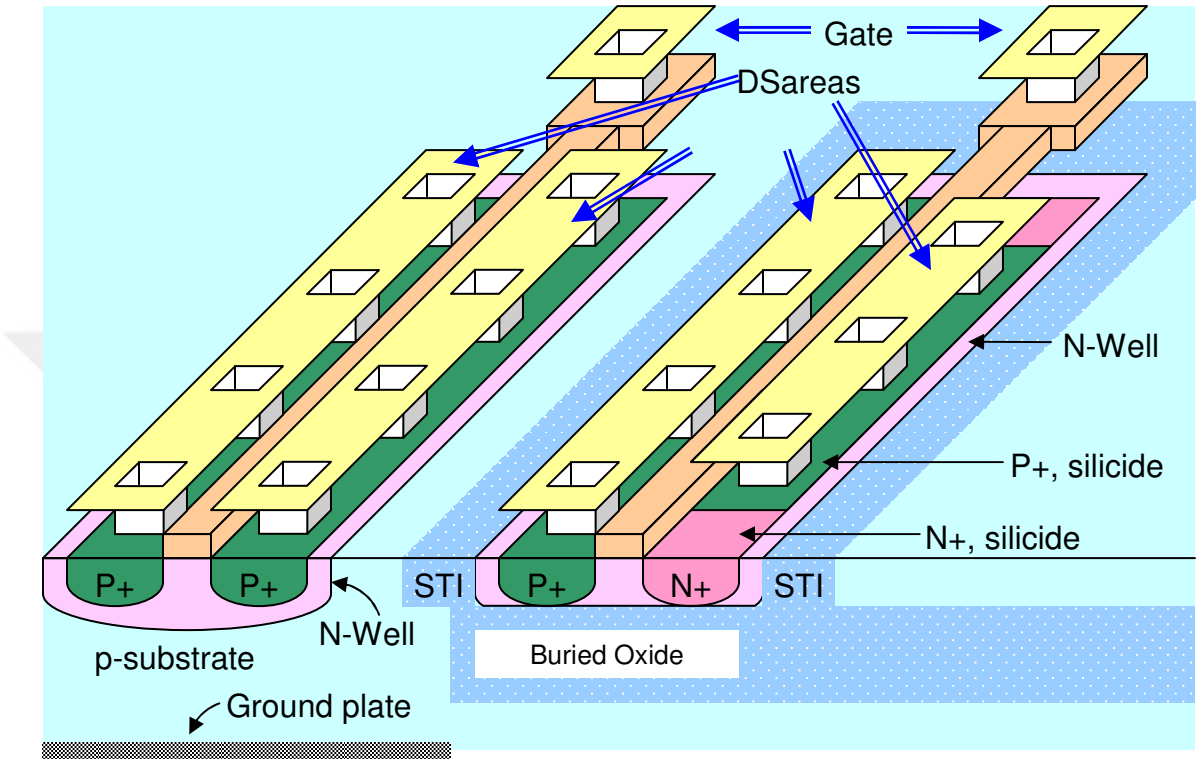


Figure A1.4.2 Bulk and SOI PMOS transistor

Appendix 1.5 Diodes and ESD Pads

Diodes are often used for clipping and clamping in the circuit designs. Diodes were used for electro static discharge (ESD) purposes. Figure A1.5.1 shows an ESD N-type diode in two-dimensional and three-dimensional aspects. If the diode at the right is cut into two, the profile will look like that is shown at the left. The ring-shaped poly is to creates buffer zone between N+ and P+ implants. It is not a control terminal like those used in transistors. Similar design in Figure A1.5.2 shows an ESD P-type diode.

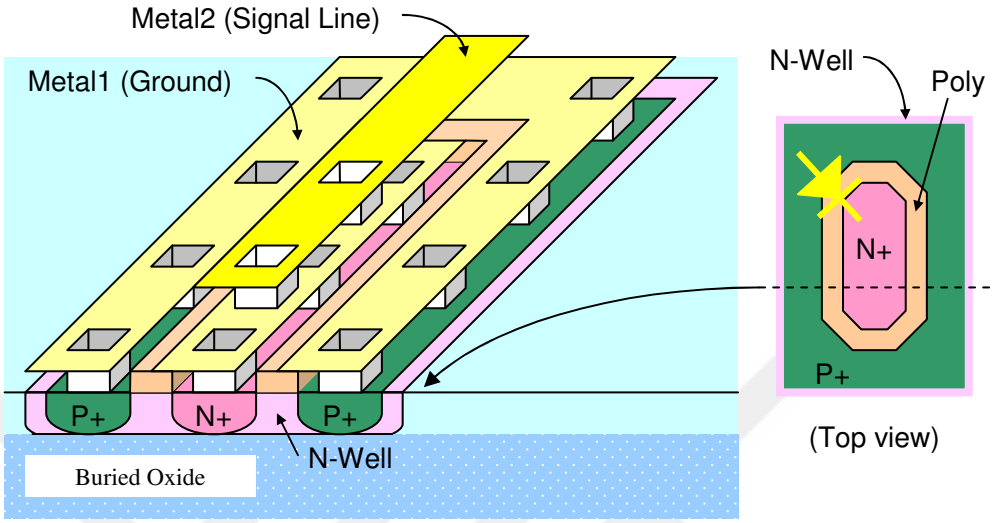


Figure A1.5.1 An ESD N-Diode

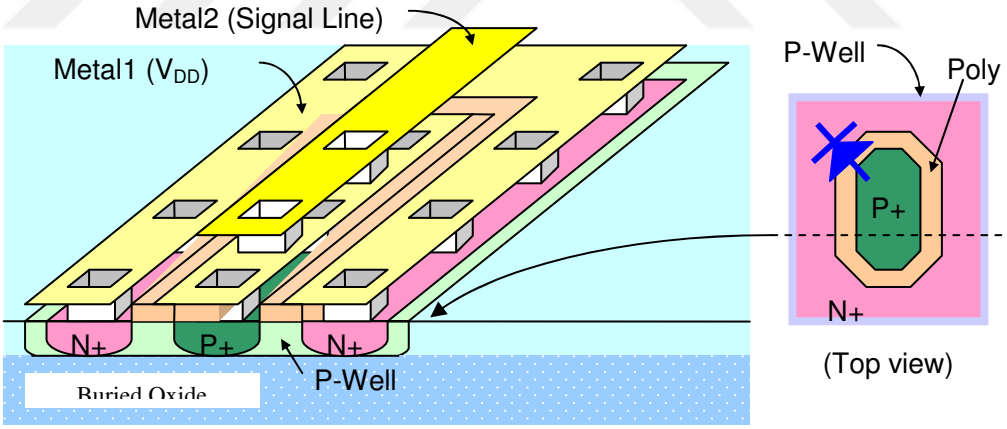


Figure A1.5.2 An ESD P-Diode

An input pad with ESD diodes are usually referred to *ESD pad* (Figure A1.5.3). Figure A1.5.4 shows the parasitics of an ESD diode in bulk CMOS process.

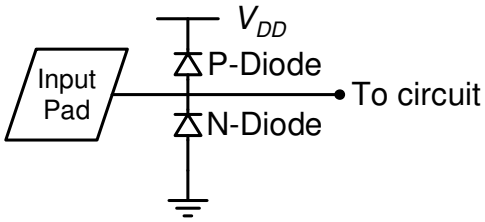


Figure A1.5.3 An input pad with ESD protection

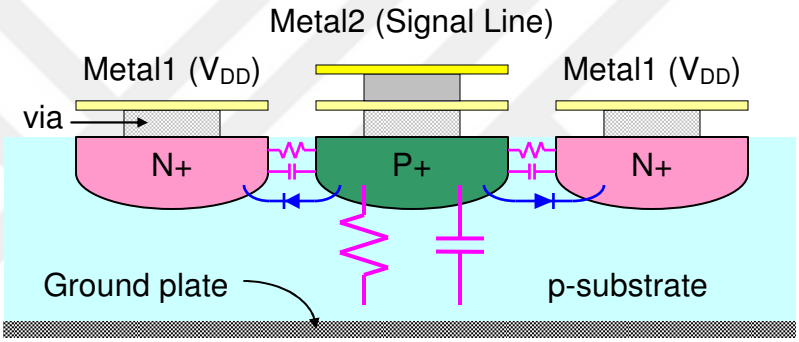


Figure A1.5.4 Parasitics of an EDS P-Diode

ESD pads could change the input matching due to its parasitics. For example, consider a P-type ESD diode of size 80μm×10μm in bulk CMOS process. The parasitic capacitance from P+ to substrate is the combination of 80[μm]×10[μm]×920[aF/μm^2]=736fF, the area capacitance, and (80[μm]+10[μm])×2×181[aF/μm]=33fF, the fringe capacitance. The parasitic capacitance from P+ to N+ is the series connection of junction capacitance from P+ to Poly and from Poly to N+: (80[μm]+10[μm])×2×(272//260)[aF/μm]=24fF. The substrate is connected to the ground plate, and therefore is considered as ground. The N+ region is connected to V_{DD}, therefore is considered as [an AC] ground, too. Together, the total parasitic

capacitance from the signal line to ground through the P-type diode is 736+33+24=793fF. Similarly, the parasitic capacitance of an N-type ESD diode of size 80μm×10μm is found in the bulk CMOS process. The parasitic capacitance from N+ to substrate is the combination of 80[μm]×10[μm]×489[aF/μm^2]=391F, the area capacitance, and (80[μm]+10[μm])×2×297[aF/μm]=53fF, the fringe capacitance. The parasitic capacitance from N+ to P+ is (80[μm]+10[μm])×2×(272//260)[aF/μm]=24fF, The total parasitic capacitance from the signal line to ground through the N-type diode is 391+53+24=468fF. For a standard pad of size 100μm×100μm, the parasitic capacitance from the pad to ground (substrate) is 100[μm]×100[μm]×11[aF/μm^2]=110f. Combining all these capacitances, the total parasitic capacitance of an input pad with both N-type and P-type ESD diodes protection is about $C_{para,tot}$= 793[fF]+468[fF]+110[fF]≈1.4pF. Note that the capacitance value for the pad assumes the use of Metal3 for the pad. If Metal2 or Metal1 is used, the total parasitic capacitance could be as high as 1.6pF.

Besides the parasitic capacitance, there are also parasitic conductances as shown in Figure A1.5.5. Fortunately, they are negligible most of the time. In the SOI process, without the ground plate, the parasitics are reduced drastically. Typical parasitic capacitances for P-type and N-type ESD diodes, size of 80μm×10μm, are 70fF and 72fF, respectively. The parasitic capacitance for the input pad, size of 100μm×100μm, is about 20fF.

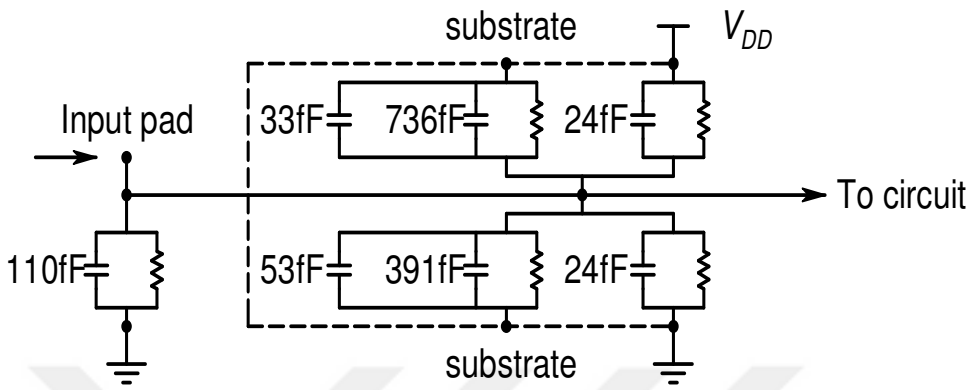


Figure A1.5.5 Parasitic capacitances and resistances in an input pad with ESD diodes