ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL

DESIGN AND IMPLEMENTATION OF AN 11-BIT 50 MS/s FLASH-ASSISTED SUCCESSIVE APPROXIMATION REGISTER ADC

M.Sc. THESIS

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Department of Electronics and Communications Engineering

Electronics Engineering Programme

JANUARY 2023

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11-BİT 50 MS/s FLAŞ DESTEKLİ ARDIŞIL YAKLAŞIMLI ANALOG SAYISAL ÇEVİRİCİNİN TASARIMI VE UYGULANMASI

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To my family,

FOREWORD

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ABBREVIATIONS

ADC : Analog to Digital Converter
CLK : Clock Signal
CMOS : Complementary Metal Oxide Semiconductor
DAC : Digital to Analog Converter
DC : Direct Current
DNL : Differential Non-linearity
DSP : Digital Signal Processing
ENOB : Effective Number of Bit
FFT : Fast Fourier Transform
INL : Integral Non-linearity
ISSCC : International Solid-State Circuits Conference
LSB : The Least Significant Bit
MIM : Metal-Insulator-Metal
MOM : Metal-Oxide-Metal
MSB : The Most Significant Bit
NMOS : N-type MOSFET
OSR : Oversampling Ratio
PMOS : P-type MOSFET
PDF : Probability Density Function
RMS : Root Mean Square
ROM : Read Only Memory
THD : Total Harmonic Distortion
TSMC : Taiwan Semiconductor Manufacturing Company
SAR : Successive Approximation Register
SNR : Signal to Noise Ratio
SNDR : Signal to Noise and Distortion Ratio

SYMBOLS

C	**:** Capacitance
F_s	**:** Sampling Frequency
T_s	**:** Sampling Period
V_{com}	**:** Common Mode Voltage
V_{DD}	**:** Supply Voltage
V_{SS}	**:** Ground
V_{inp}	**:** Positive Input Voltage
V_{inn}	**:** Negative Input Voltage
V_{outp}	**:** Positive Output Voltage
V_{outn}	**:** Negative Output Voltage

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DESIGN AND IMPLEMENTATION OF AN 11-BIT 50 MS/s FLASH-ASSISTED SUCCESSIVE APPROXIMATION REGISTER ADC

SUMMARY

Modern electronic systems transmit, store, and process data. Pure analog solutions are no longer practical due to the increasing complexity of electronic systems. Thanks to advances in digital signal processing (DSP), signal processing and storage have moved from analog to digital domains. However, first of all, analog signals should be converted to digital signal in order to take advantages of DSP. Therefore, DSP systems are needed ADC. There are different ADC topologies in the literature because each system has different performance requirement. The most popular ADC architectures are flash, pipeline, SAR, delta-sigma and time-interleaved ADCs. Each of these architecture has own advantages and disadvantages in terms of resolution, sample rate etc.

SAR ADC has been one of the most widely used ADC architectures over the past decade. Due to its largely digital structure, SAR ADC take advantage from CMOS technology scaling. SAR ADCs are generally preferred for medium accuracy, medium speed, and low power applications like biosensors, image sensors, and wearable devices because they have the highest energy efficiency of all moderate bandwidth, moderate resolution converters. However, resolution and speed of the SAR ADC is restricted by comparator offset and mismatch in the DAC. Therefore, many calibration and redundancy techniques have been proposed to improve SAR ADC resolution, but they increase design complexity and don't solve bandwidth issues.

In this work a new method proposed in order to increase resolution of the SAR ADC without speed degradation. 11-bit flash assisted SAR ADC with a 50 Msps date rate designed and simulated in TSMC 65nm technology node. The working principle of the our design is similar to pipeline ADC. Conversion is completed in two cycles . In the first cycle SAR ADC sample the input signal and generate the most significant eight bit. In the second cycle, the residue voltage produced by the SAR ADC is amplified through the switch capacitor circuit and converted into three bits with the help of the flash ADC. Then output of the SAR ADC and flash ADC is aligned and 11-bit resolution is obtained.

The thesis consists of five chapters, with the first chapter introducing the work and objectives. In the second chapter, background information about ADC design and commonly used ADC architectures are reviewed. In the third chapter, the architecture of the designed flash-assisted SAR ADC is explained. In chapter four, simulation results for the designed blocks are presented and interpreted. The thesis is concluded and compared with similar work in the fifth chapter.

11-BİT 50 MS/s FLAŞ DESTEKLİ ARDIŞIL YAKLAŞIMLI ANALOG SAYISAL ÇEVİRİCİNİN TASARIMI VE UYGULANMASI

ÖZET

Tümdevre teknolojisinin 21. Yüzyıldaki hızlı ilerleyişi ile birlikte elektronik sistemler daha da gelişmiş ve karmaşıklaşmıştır. Haberleşme sistemlerinin veri aktarım hızının ve bant genişliklerinin sürekli artması sebebiyle analog ve sayısal devrelerin birlikte kullanıldığı karışık işaret (mixed-signal) sistemleri yaygınlaşmıştır. Özellikle CMOS üretim teknolojisinin gelişmesi ile birlikte transistor boyutları küçülmüş ve bu durum analog devre tasarımını zorlaştırırken sayısal devre tasarımını ise olumlu olarak etkilemiştir. Özellikle sayısal işaret işlemenin (DSP) ideal olmayan durumlara karşı analog devrelerden fazla tolerans göstermesi, kolay bir şekilde gerçeklenebilmesi ve bir üretim teknolojisinden yeni bir üretim teknolojisine kolayca geçirilebilmesi gibi avantajlarından dolayı sayısal işaret işlemenin daha fazla tercih edilmesine neden olmuştur. Fakat bu sayısal işaret işlemenin avantajlarından faydalanabilmek için öncelikle analog işaret analog sayısal çeviriciler (ADC) tarafından sayısal işarete dönüştürülmelidir.

Çeşitli uygulama alanlarına ve sistem gereksinimlerine dayalı olarak çok sayıda analog sayısal çevirici mimarisi literatürde bulunmaktadır. Analog sayısal çeviricilerin temel özellikleri örnekleme hızı, bant genişliği, güç tüketimi ve çözünürlüktür. Bir sistemde analog sayısal çevirici ihtiyacı olduğunda kullanılacak analog sayısal çevirici bu özelliklere bakılarak seçilir. Örneğin bir ölçüm cihazında kullanılacak bir analog sayısal çevirici için çözünürlüğün yüksek olması gerekirken örnekleme hızının ise yüksek olmasına gerek yoktur. Bu nedenle ölçüm cihazlarında yüksek çözünürlüklü düşük hızlı delta-sigma analog sayısal çeviriciler tercih edilir. Bir osiloskop sisteminde kullanılacak bir analog sayısal dönüşütürücünün ise örnekleme hızının yüksek olması beklenir ve örnekleme hızı yüksek olan flash tipi analog sayısal çevirici tercih edilir.

Bir diğer analog sayısal çevirici türü olan ardışıl yaklaşımlı (SAR) analog sayısal çeviriciler, orta bant genişliğine sahip, orta çözünürlüklü dönüştürücüler arasında en yüksek enerji verimliliğine sahip olduklarından, genellikle biyosensörler, görüntü sensörleri ve giyilebilir cihazlar gibi orta çözünürlük, orta hız ve düşük güç uygulamaları için tercih edilir. Bununla birlikte, SAR ADC'nin çözünürlüğü ve hızı, karşılaştırıcının ofseti ve sayısal analog dönüştürücüdeki (DAC) uyumsuzluk (mismatch) tarafından kısıtlanır. Bu nedenle, SAR ADC çözünürlüğünü iyileştirmek için birçok kalibrasyon ve gereksiz çokluk (redundancy) tekniği önerilmiştir, ancak bunlar tasarım karmaşıklığını artırır ve bant genişliği sorunlarını çözmez.

Günümüz elektronik sistemleri yüksek hızlı ve yüksek çözünürlüklü ADC'lere ihtiyaç duyduğundan literatürde bulunan temel ADC mimarileri yetersiz kalmaktadır. Bu

nedenle iki veya daha fazla ADC türünün birleştirilmesi ile oluşturulan hybrid ADC yapıları son yıllarda oldukça popüler olmaya başlamıştır. Hybrid ADC mimarilerinde birleştirilen ADC'lerin zayıf yönlerini giderilerek performansı daha yüksek bir ADC ortaya çıkarılmaya çalışılmaktadır.

Bu çalışmada da SAR ADC ve flash ADC beraber kullanılarak hybrid bir ADC tasarlanmıştır. SAR ADC'nin çözünürlüğünün örnekleme hızında bir düşüş olmadan arttırılması hedeflemektedir. Bu bağlamda 50 Msps örnekleme hızına, on bir bit çözünürlüğe sahip flash ADC yardımlı SAR ADC mimarisi TSMC 65nm üretim teknolojisinde gerçeklenmiş, benzetimleri yapılmış ve doğrulanmıştır. Tasarımımızın çalışma prensibi pipeline ADC'nin çalışma yapısı ile benzerlik göstermektedir. Bu tasarım örneklenen analog işareti iki döngü sonunda sayısal işarete dönüştürmektedir. Birinci döngüde SAR ADC, giriş sinyalini örnekler ve en önemli sekiz bitini üretir. İkinci döngüde, SAR ADC tarafından üretilen artık gerilim, anahtar kondansatör devresi aracılığıyla yükseltilir ve flash ADC yükseltilmiş kalıntı gerilimini üç bit sayısal işarete dönüştürür. Ardından SAR ADC ve flash ADC'nin çıktısı zamanlama olarak hizalanır ve on bir bitlik çözünürlük elde edilir.

Klasik bir SAR ADC, dört temel devreden oluşur: örnekleme ve tutma devresi (SH), DAC, karşılaştırıcı ve SAR kontrol mantığı. Örnekleme ve tutma devresi, analog sinyali örnekler ve dönüştürme tamamlanana kadar örneklenen değeri saklar. Bu devre genellikle anahtar, kondansatör ve yükselticiden oluşur. İki fazdan oluşan devrenin ilk fazında giriş işareti anahtar yardımıyla kondansatöre örneklenir. İkinci fazda ise örneklenen gerilim değeri tutulur. Bu tasarımda kondansatör temelli bir DAC yapısı kullanıldığı için DAC aynı zamanda örnekleme tutma devresi olarak da kullanılmıştır. Böylelikle hem güç tasarrufu hem de alan tasarrufu sağlanmıştır.

DAC devresi SAR mantık devresi tarafından kontrol edilen sayısal işareti analog işarete çeviren bir devredir. Literatürde değişik türde DAC yapıları bulunmasına karşın SAR ADC'lerde kondansatör temelli DAC'lar daha fazla tercih edilmektedir. Bu tasarımda modifiye edilmiş ikili ağırlıklı DAC yapısı tercih edilmiştir. Klasik yapıdan farklı olarak toplam kondansatör miktarını düşürmek için kondansatör dizisi iki parçaya bölünmüştür. Birinci kondansatör dizisi en önemli dört sayısal biti kontrol ederken diğer kondansatör dizisi ise kalan dört biti kontrol etmektedir. İki kondansatör dizisi arasındaki yük paylaşımı bir köprü kondansatörü vasıtasıyla gerçekleşmektedir. DAC, SAR ADC mimarisindeki en önemli devrelerden biridir. Bu devredeki uyumsuzluk, yük enjeksiyonu ve parazit kondansatörler devrenin doğrusallığını bozarak ADC'nin çözünürlüğünü azaltmaktadır. Özellikle bizim tasarımımızda DAC'nin çıkışındaki kalıntı gerilimi üç bit sayısal değere dönüştürüldüğü için bu kalıntı geriliminin doğruluğu oldukça önemlidir. Bu sebeple DAC mümkün olduğunca dikkatli bir şekilde tasarlanmalı ve serim devresi de hassas bir şekilde çizilmelidir.

SAR ADC mimarisindeki bir diğer önemli devre ise karşılaştırıcı devresidir. Karşılaştırıcı devresi, örneklenen değeri DAC'nin çıkışıyla karşılaştırır. Karşılaştırıcı devresi için saat işaretiyle çalışan mandal (latch) yapısına sahip devre kullanılmıştır. Böylelikle güç tüketiminin azaltılması hedeflenmiştir. Karşılaştırıcının gürültüsü ve ofset değeri ADC'nin performansını doğrudan etkilediği için bu değerlerin benzetim yoluyla bulunarak doğrulanması gerekmektedir

SAR mantık devresi, karşılaştırıcının sonucuna göre ADC'nin çıkış bitlerine karar verilen sayısal kısımdır. DAC, SAR mantık devresinin çıkışlarına göre çıkış gerilimini belirler. DAC çıkış gerilimi ile örneklenen gerilim karşılaştırıcı tarafından karşılaştırılır ve karşılaştırıcının çıkışına göre de SAR mantık devresi sayısal bitleri üretir.

Flash ADC mimarisi literatürde bulunan en hızlı ADC mimarilerinden biridir. Bu ADC türü karşılaştırıcı, referans üreticisi ve kod çözücü (decoder) devrelerinden oluşur. Çözünürlük arttıkça karşılaştırıcı sayısının üstel bir şekilde artması sebebiyle güç tüketimi ve alan gereksinimi fazladır. Bu nedenle bu çalışmada olduğu gibi düşük çözünürlüklü flash ADC'ler yardımcı ADC olarak hybrid ADC'lerde tercih edilmektedir.

Bu çalışma beş bölümden oluşmaktadır. Birinci bölüm çalışmayı ve çalışmanın hedeflerini tanımlamaktadır. İkinci bölümde ADC tasarımı hakkında genel bilgiler verilmiş ve literatürde bulunan yaygın ADC türlerinden bahsedilmiştir. Üçüncü kısımda tasarlanan flash ADC yardımlı SAR ADC anlatılmıştır. Tasarlanan ADC'deki alt bloklar ayrıntılı bir şekilde anlatılmış şematik tasarımları gösterilmiş ve serim devrelerinin ekran görüntüleri eklenmiştir. Dördüncü bölümde ise tasarlanan devrelerin benzetim sonuçları paylaşılmış ve yorumlanmıştır. Son bölümde ise yapılan çalışmanın sonuçları ve bu çalışmayı geliştirmek için yapılabilecekler değerlendirilmiştir.

1. INTRODUCTION

Data transmission, storage, and processing are common themes in modern electronic systems. Even though analog circuits are adequate for simple functions like filtering and amplification, pure analog solutions are no longer convenient because of the increasing sophistication of electronic systems. Thanks to advances in digital signal processing (DSP) that provide unprecedented computation power and limitless signal-to-noise ratio (SNR), a significant transition from the analog to the digital domain has happened in signal processing and storage applications. However, to take advantage of DSP's benefits, continuous physical signals must first be converted to digital signals using analog-to-digital converters (ADC).

Today every mixed signal DSP system uses an ADC, and the performance of these systems highly depends on the performance of the utilized ADC. Therefore, numerous ADC architectures have been devised because each application necessitates a unique set of limitations. The most popular ones are flash, pipeline, time-interleaved converters, integrating, successive approximation register (SAR), algorithmic, delta-sigma, interpolating (and folding), and two-step [1]. Each of these architectures offers different advantages in terms of speed, resolution, bandwidth, etc. The research described here focuses on two types of converters: flash and SAR ADCs.

SAR ADC is well-suited for applications requiring moderate resolution, moderate speed, and low power, such as biosensors, image sensors, and a variety of wearable devices because SAR ADC demonstrates the highest energy efficiencies of all moderate bandwidth and moderate resolution converters. Compared to pipeline ADC where high-speed high-gain operational amplifiers are employed, SAR ADC is composed of mostly digital circuits. Therefore, SAR ADC has benefited from technology scaling. However, comparator offset, noise, and digital-to-analog converter (DAC) linearity restrict the resolution of the SAR ADC. Many calibration and

redundancy techniques are proposed in the literature to improve the resolution of the SAR ADC, but these techniques increase design complexity and decrease the conversion rate of the converter.

In this work, we assist SAR ADC with flash ADC to enhance its resolution without decreasing the conversion rate. Different from flash-assisted SAR ADC proposed in [2] and [3], flash ADC is utilized to convert the least significant 3-bits in this design.

1.1 Purpose of Thesis

The specific objectives of the dissertation could be listed as:

- Provide background information about existing ADC architectures and metrics that used to compare performance of ADC
- Propose a method to increase resolution of the SAR ADC without sacrifice speed

1.2 Organization of the Thesis

This work organized as follow:

- In chapter 2, background information about ADC design and commonly used ADC architectures in the literature are reviewed in details.
- In chapter 3, the architecture of designed flash assisted SAR ADC is explained in details. Design procedure of binary-weighted SAR ADC and flash ADC is explained.
- In chapter 4, simulation result of the flash assisted SAR ADC are presented and interpreted.
- In chapter 5, this thesis is summarized, results are compared with other works in the literature and future work is discussed.

2. BACKGROUND

Section 2.1 of this chapter provides a brief summary of ADC fundamentals, while commonly used ADC architectures, such as pipeline, flash, etc., are discussed in Section 2.2.

2.1 ADC Fundamentals

In this part, the sampling and quantization processes will be explained. In addition, the performance metrics used to characterise an ADC will be discussed.

2.1.1 Sampling and Quantization

In the real world, signals are in the analog domain. The amplitudes and duration of these signals are continuous and unbounded. On the other hand, both the amplitude and timing of digital signals are discrete. Therefore, the time and amplitude of an analog signal should be discretized by applying sampling and quantization processes for analog-to-digital conversion.

Sampling could be thought of as taking pictures of an analog signal at regular time intervals [4]. Figure 2.1 shows that when time is an integer multiple of the sampling period (T_s), the sampled waveform equals the analog signal. This value stays the same until the next integer multiple of T_s arrives.

The sampling rate is one of the main performance metrics for ADC and DAC because it determines how many conversions are completed within a specific period. It is, therefore, possible that, depending on the analog signal's bandwidth, some information may be lost due to a finite sampling rate. Depending on the application, this loss may be tolerable.

ADCs are classified into three different groups with respect to the relationship between sampling rate and bandwidth: Nyquist rate ADCs, oversampling ADCs, and undersampling ADCs. For Nyquist-rate ADCs, the sampling frequency (F_s) must be

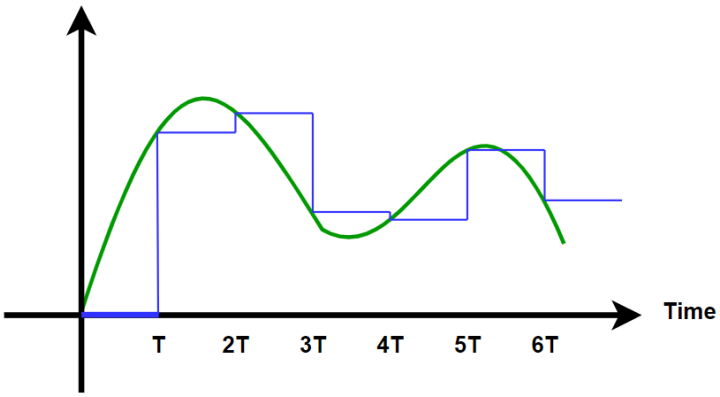

Figure 2.1 : Waveform of sampled input signal.

greater than twice the highest frequency component of the analog input signal in order to prevent aliasing [5]. Oversampling converters, on the other hand, are converters whose sample frequency is considerably larger than the Nyquist frequency (typically 10 to 400 times faster). This converter improves the SNR by pushing quantization noise away from the desired frequency band. In contrast to other ADCs, the sampling rate of undersampling ADCs is lower than the Nyquist frequency. Undersampling applications benefit from aliasing. According to sampling theory, aliasing happens when an input signal is sampled at a rate lower than the Nyquist rate. These aliased components fall into the Nyquist bandwidth, which is between DC and $F_s/2$, so if there is no additional signal component within the Nyquist bandwidth, higher frequency signals could be sampled at a lower sampling rate. Undersampling ADCs could be used to improve efficiency because the majority of systems used today are high-frequency with limited bandwidth, such as the intermediate frequencies of digital radios. To prevent overlapping of aliased components, the sample frequency must be larger than twice the input bandwidth, and the desired bandwidth must be filtered using a bandpass filter before sampling.

Another operation that should be applied for analog to digital conversion is quantization. Quantization is the matching of the amplitude of a sampling input to one of the quantization levels of an ADC. This makes the amplitude of sampled signal discrete. The number of quantization levels that an ADC can represent determines the resolution of the ADC. Due to the binary nature of an ADC's output, the resolution is specified in powers of two. For instance, 8-bit ADC generates 256 quantization

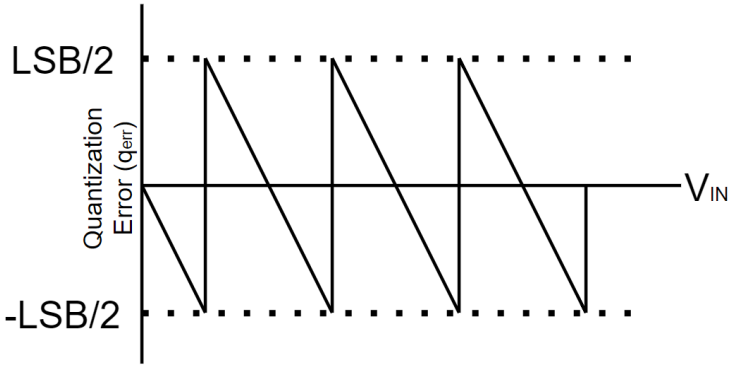

Figure 2.2 : Quantization noise characteristic of an ideal ADC.

levels and matches the sampled analog input to one of these quantization levels. As a rule, a trade-off exists between the ADC's sampling rate and its resolution. For the conversion to be finished in a shorter amount of time, the converter's resolution needs to be decreased as the sample rate increases [6].

The least significant bit (LSB) refers to the smallest voltage level the ADC could detect. The LSB can be calculated by dividing the ADC's full-scale voltage range by the number of quantization levels, as shown in Equation 2.1.

$$1LSB = \frac{V_{FS}}{2^N} \tag{2.1}$$

The ideal dynamic range of an ADC is defined as the ratio between the largest input voltage and the smallest input voltage that the ADC can resolve. The maximum signal-to-noise ratio (SNR) could also express the converter's ideal dynamic range. The SNR formula varies depending on the signal type (sinusoidal, ramp, etc.). Maximum SNR for sinusoidal signals is calculated as indicated in Equation 2.2.

$$DynamicRange(dB) = 20log(\frac{V_{FS}/(2\sqrt{2})}{1LSB}) \tag{2.2}$$

Some input voltage changes are not sufficiently large to pass from one transition level to another. The converter misses these small input voltage alterations. The quantization noise of the converter refers to this finite limit. Because converters have a finite resolution, quantization noise exists even in ideal ADCs. The quantization noise (V_{noise}) can be interpreted as a random variable that is uniformly distributed

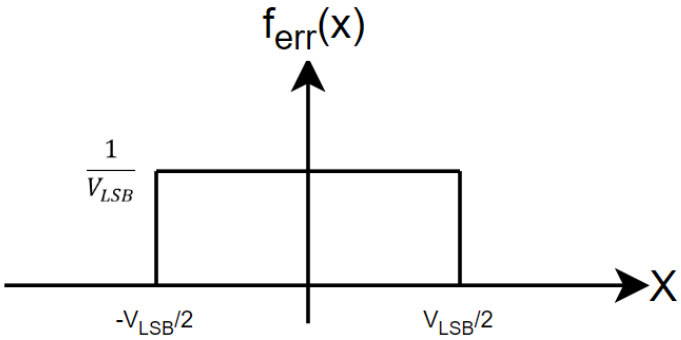

Figure 2.3 : PDF of quantization noise.

between -V_{LSB}/2 and +V_{LSB}/2, as illustrated in Figure 2.2. Then, from the PDF of quantization noise depicted in Figure 2.3, the power of quantization noise (P_{noise}), root mean square (RMS) value of quantization noise (V_{noise}) and SNR for sinusoidal signals are calculated in Equations 2.3, 2.4, and 2.5, respectively.

$$P_{noise} = \frac{1}{V_{LSB}} \int_{-LSB/2}^{LSB/2} x^2 dx = \frac{V_{LSB}^2}{12} \tag{2.3}$$

$$V_{noise} = \sqrt{P_{noise}} = \frac{V_{LSB}}{\sqrt{12}} \tag{2.4}$$

$$SNR = \frac{2^N V_{LSB}/2\sqrt{2}}{V_{LSB}\sqrt{12}} = 6.02\,N + 1.76\;dB \tag{2.5}$$

2.1.2 ADC Performance Metrics

Error in the ideal ADCs has a linear function between -0.5 LSB and +0.5 LSB, as shown in Figure 2.2. However, non-ideal ADCs generate errors due to imperfect devices and component mismatches. Thus, in order to determine the performance of an ADC, dynamic and static metrics are defined.

The offset error could be referred to as a shift in the transfer curve. On the other hand, gain error measures the slope difference between the ideal and actual transfer curves. Both gain and offset errors are signal-independent, so they do not cause non-linearity or harmonics. Thus, designers are not generally bothered about gain and offset errors.

However, for test and measurement applications, these two types of errors should be calibrated in either the hardware or the software.

For an N-bit ADC, there are 2^N quantization levels, and the width of each quantization level should, in an ideal world, be equal to one LSB. However, this is not always the case with a real converter. Differential non-linearity (DNL) error is the variation of the quantization level width from 1 LSB. The deterministic way to figure out this error is described in Equation 2.6, where i is the digital output code [7].

$$DNL[i] = \frac{V_{i+1} - V_i}{V_{LSB}} - 1 \tag{2.6}$$

For instance, if the step width of one quantization level is 1.5 LSB, the DNL error for that quantization level is equal to +0.5 LSB. If the DNL error exceeds +1 LSB, one of the digital output codes is skipped, resulting in a missing code.

Due to the DNL quantized step size inaccuracy, the actual response of the converter can deviate from the ideal transfer function. In order to measure this deviation, integral non-linearity (INL) is used. As shown in Equation 2.7, the total deviation of the real transfer function can be found by adding all the DNLs up to a given code's INL.

$$INL[i] = \sum_{i=1}^{\infty} DNL[i] \tag{2.7}$$

These non-linearity errors cause harmonic distortion in the frequency domain. These distortions are measured as total harmonic distortion (THD), whose calculation is shown in Equation 2.8. Also, Equation 2.9 shows how to figure out the SNDR from the THD and SNR. SNDR is used to calculate the resolution of the ADC.

$$THD = 20\, log \sqrt{[10^{-V_2/20}]^2 + [10^{-V_3/20}]^2 + ...[10^{-V_6/20}]^2} \tag{2.8}$$

$$SNDR = -10\, log[10^{-SNR/10} + 10^{-THD/10}] \tag{2.9}$$

Due to harmonic distortion and noise, the actual resolution of the converter is lower than the desired value. Therefore, the effective number of bits (ENOB) determines the actual resolution of the ADC. Equation 2.10 depicts the relationship between the observed SNDR and the ENOB.

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{2.10}$$

Another type of non-ideality is the aperture delay error. The aperture delay is how much time passes by between when the sampling edge of the clock signal happens and when the ADC receives a new sample. This delay consists of a fixed delay as well as a jitter. The signal path length and propagation delay of the digital circuits results in the fixed delay component. A fixed delay does not impact the absolute sample period, so it does not degrade performance. A random component of the aperture delay is the jitter which generated by noise in the phase locked loop (PLL) circuit. Due to randomness, clock jitter may introduce harmonic distortion. As illustrated by Equation 2.8, harmonic distortion reduces SNDR, diminishing the converter's precision. The clock jitter tolerance of the ADC depends on the input frequency and resolution of the converter.

2.2 ADC Architectures

Several converter architectures, such as pipeline, delta-sigma, etc., have been described in the literature. Each architecture has advantages that make it suitable for particular applications. This section will examine some of the most prevalent ADC architectures.

2.2.1 Flash ADC

Due to its basic structure, the flash ADC architecture depicted in Figure 2.4 is one of the most widely used converter topologies [2], [8]. The N-bit flash ADC uses 2^N-1 comparator at each quantization level to compare the input signal with different reference voltages. In each comparator, the positive input is connected to the analog input, and the negative input is connected to the different reference voltages. All comparators with an input voltage greater than its reference voltage generate a logic "1" at the output, whereas all comparators with an input value less than its reference voltage generate a logic "0" at the output. The decoder circuit converts this coding sequence, called thermometer code, into binary code. Flash ADC, whose conversion rate is determined by a comparator clock, is one of the fastest converter architectures because it resolves the input in one cycle. However, the main drawback of flash ADC is the exponential growth in the number of comparators as the resolution increases. As an example, while 15 comparators are needed for 4-bit conversion, an 10-bit

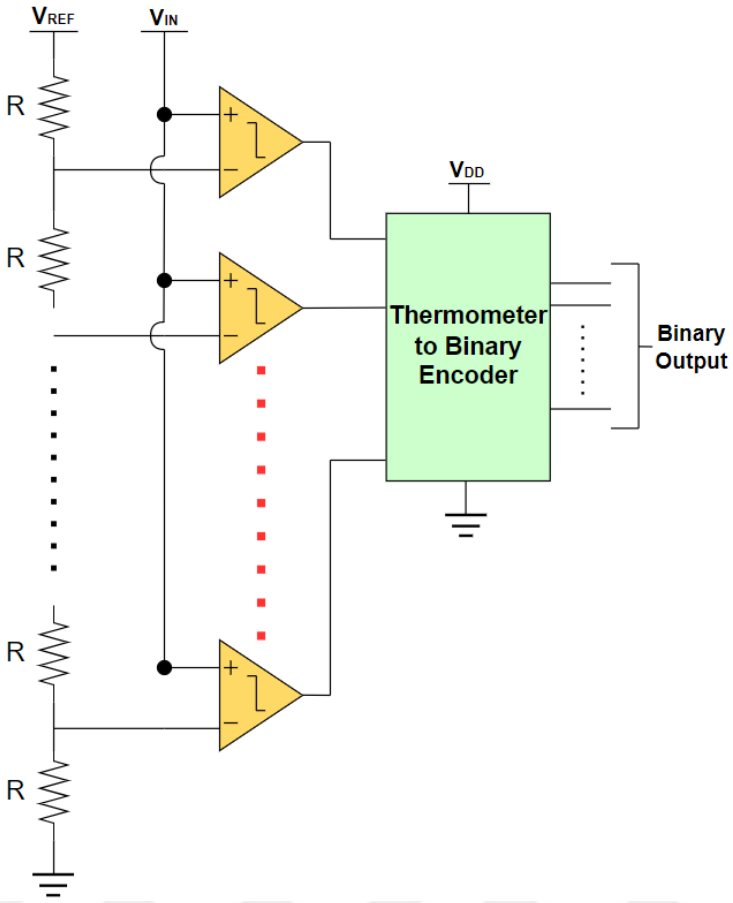

Figure 2.4 : Flash ADC block diagram.

flash ADC requires 1023 comparators. This excessive increase also increases power consumption and die area. Therefore, high-resolution flash ADCs are generally preferred in applications where speed is crucial. Furthermore, low-resolution flash ADCs could be used to assist the main ADC in hybrid structures in order to increase resolution without sacrificing speed, as in this work.

2.2.2 Pipeline ADC

The pipeline ADC consists of multiple stages; each stage is responsible for converting a relatively small portion of the total number of bits, N. For instance, a one-bit per stage 10-bit pipeline ADC consists of 10 cascading stages, each of which converts one bit. Figure 2.5 depicts the pipeline ADC block diagram.

Each pipeline stage consists of a sample-and-hold amplifier, a sub-ADC, a subtraction circuit, and a residue amplifier with a closed-loop gain of two. The first stage

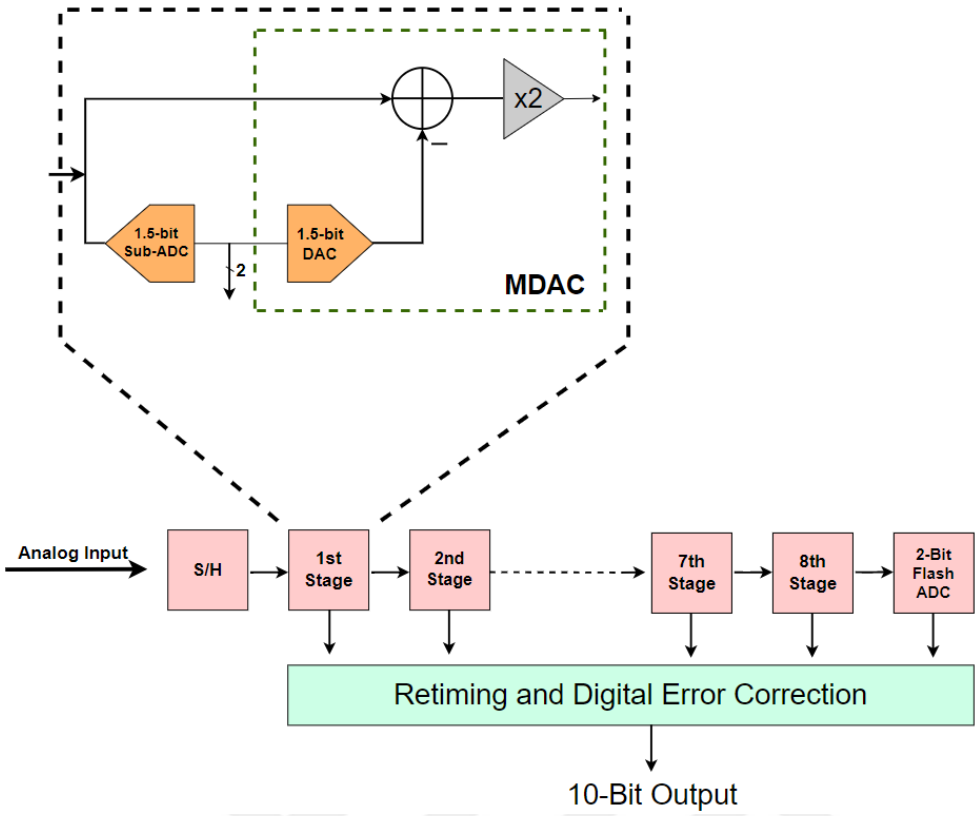

Figure 2.5 : Block diagram of the pipeline ADC.

samples the analog signal, and the sub-ADC quantizes the sampled input. Then, the quantized analog signal is subtracted from the sampled signal, and the result is called the residue. Finally, multiply the residue voltage by two via the residue amplifier. Then, The subsequent stage takes the sample of the output that has been amplified. Simultaneously with the residue from the first stage being processed by the second stage, a new sample is taken by the first stage, and one conversion is completed each clock cycle.

The accuracy requirement is different for each pipeline stage. The first few stages are the most critical because a little inaccuracy in these stages propagates throughout the remaining stages and is amplified by two, resulting in a significantly larger error in the output. Thus, extra attention should be required when designing the first few stages. Since accuracy requirements are relaxed as you go down the pipeline stages, the design of the last stages is easier than the previous stages.

Pipeline ADC has a high throughput rate because it distributes the conversion process into multiple stages. This is more efficient than flash ADC, which quantizes the input in

one stage. However, one of the main drawbacks of pipeline ADC is latency. Pipeline ADCs have data latency due to the propagation of the sample through all pipeline stages. This latency could be crucial for some applications. The other drawback is that the first two stages require a high-gain, high-bandwidth operational amplifier; however, developing this type of operational amplifier in an advanced CMOS technology process is very challenging

2.2.3 Delta Sigma ADC

Delta-sigma ADCs are oversampling ADCs with a sampling rate much higher than the Nyquist rate. This is different from the pipeline and flash ADCs, which are Nyquist rate ADCs. The ratio between the sampling rate and the Nyquist rate is called the oversampling ratio (OSR). Delta-sigma ADCs could achieve higher accuracy with the help of oversampling and noise shaping. While oversampling reduces the power of the quantization noise in the band of interest, noise shaping pushes noise away from the desired frequency band.

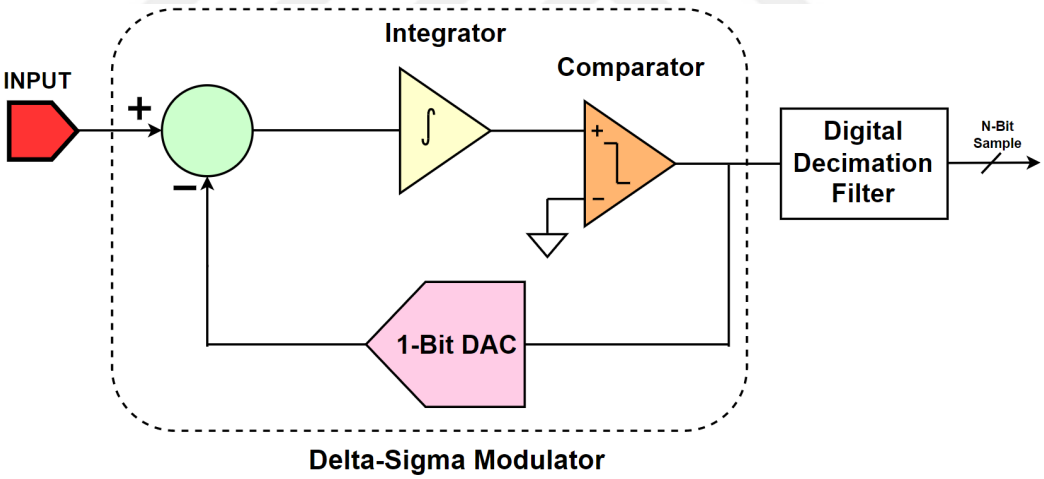

Figure 2.6 : Delta Sigma ADC architecture.

As shown in Figure 2.6, a delta-sigma ADC comprises of a delta-sigma modulator and a digital decimation filter. The delta-sigma modulator converts the input signal into 1-bit stream at a very fast rate, and these sampled data are converted into digital output code by a digital/decimation filter with high resolution and a slow rate. In the delta-sigma ADC, precision is prioritized over speed. Therefore, it is

generally preferred for audio and measurement applications requiring low speed and high accuracy.

2.2.4 Successive Approximation Register ADC

Due to its high conversion efficiency between moderate resolution and moderate bandwidth ADCs, the SAR ADC is one of the most prevalent ADC architectures. In addition, this topology benefits from technology scaling as there is no need for complex analog circuits. As shown in Figure 2.7, the SAR ADC includes a sample-and-hold amplifier, a comparator, a DAC, and a SAR logic.

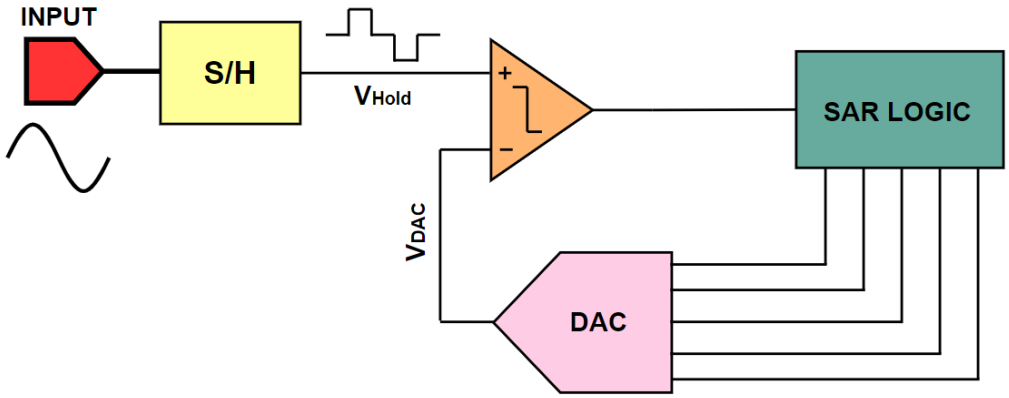

Figure 2.7 : Block diagram of SAR ADC.

To determine which quantization level is most appropriate for the sampled data, SAR ADC utilizes a binary search algorithm. According to this algorithm, each bit is determined sequentially for each clock cycle by SAR logic, whose output is controlled by a comparator. As a consequence, at least N clock cycles are required for N-bit resolution, so the conversion rate of the converter decreases with increasing resolution. In Chapter 3, we will look closely at the SAR ADC algorithm and the circuits used in this architecture.

2.2.5 Time Interleaved ADC

The concept of time-interleaved converters was first introduced in 1980 [9]. As illustrated in Figure 2.8, this architecture utilizes M sub-ADCs, each of which operates at F_s/M to achieve an overall conversion rate of F_s. In other words, a high

conversion rate could be achieved by using several converters working in parallel. The main advantage of the time-interleaved system is its ability to enhance speed without reducing resolution. As a result, time-interleaved ADCs are well-suited for high-speed, high-resolution applications in communication systems.

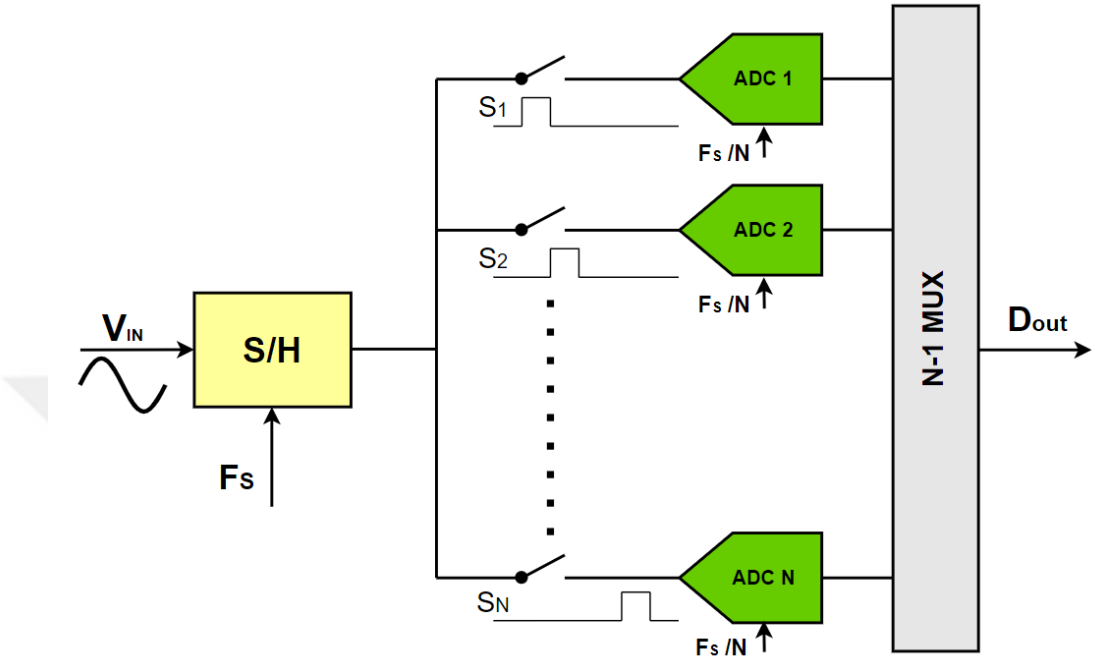

Figure 2.8 : Time Interleaved ADC architecture.

Contrary to non-interleaved converters, where offset, gain, timing, and bandwidth inaccuracies do not degrade performance as long as they are constant, time-interleaved ADCs are extremely sensitive to mismatches between different sub-ADCs. Hence, robust calibration schemes are required for time-interleaved converters.

3. SYSTEM and CIRCUIT DESIGN

3.1 System Overview

Hybrid ADC architectures exist in the literature in addition to the converter architectures covered in the previous chapter. Hybrid converters are created by combining two or more ADC architectures to improve the performance of the converter. In this research, an 11-bit 50 Msps flash-assisted SAR ADC was designed, implemented and simulated in the Taiwan Semiconductor Manufacturing Company (TSMC) 65nm CMOS process technology. As shown in the block and timing diagrams of the design in Figures 3.1 and 3.2, respectively, an 8-bit SAR ADC resolves the first eight bits of the converter. Then, the residue generated by the DAC in the SAR ADC is amplified by a switch capacitor circuit to reduce the design requirements of the flash ADC. The amplified residue is then converted to a 3-bit digital output by the flash ADC. Outputs of the SAR ADC and flash ADC are combined, and an 11-bit resolution is obtained. This design might be regarded as a two-stage pipeline ADC whose the first stage is an 8-bit SAR ADC and the second stage is a 3-bit flash ADC. In the remaining part of this chapter the design procedure of 8-bit SAR ADC, 3-bit flash ADC and residue amplifier will be examined.

3.2 8-Bit Binary-Weighted SAR ADC

A SAR ADC first appeared in a patent filed by J. C. Schelleng of Bell Telephone Laboratories in 1946 [7]. Because of its compatibility with CMOS technology scaling, it is still one of the most widely used ADC architectures today. Indeed, nearly half of the ADC papers published at the International Solid-State Circuit Conference (ISSCC) 2021 are related to SAR ADC with respect to the Boris Murmann ADC survey [10]. So it's truly amazing that almost 70 years later, there are still a lot of new things being done in this field.

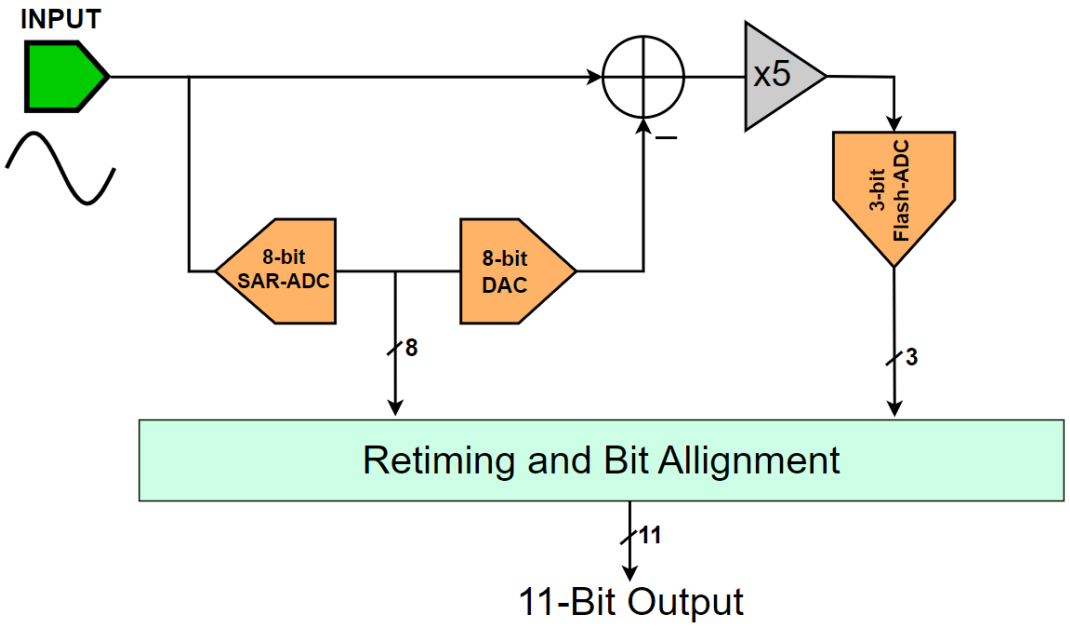

Figure 3.1 : The flash assisted SAR ADC block diagram.

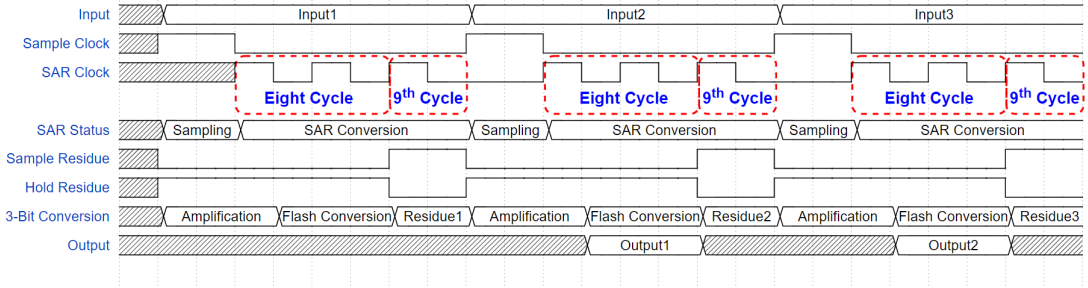

Figure 3.2 : The flash assisted SAR ADC timing diagram.

A typical SAR ADC has four basic parts: a sample-and-hold amplifier (S&H), a DAC, a comparator, and SAR control logic. The S&H takes a sample and stores it until the conversion is complete. Comparator circuits compare the sampled value (V_{sample}) to the DAC output (V_{DAC}). The SAR logic decides the bit values based on the results of the comparator so that the output of the DAC is matched with the quantization level closest to the sampled input value.

The conversion algorithm for the 3-bit SAR ADC is depicted in Figure 3.3. The input is sampled at the end of the sampling cycle; this value does not change until the conversion is complete. MSB is then set to 1 by SAR logic, and the sample is compared to the DAC output, which is equal to $V_{ref}/2$, by a comparator. If the sampled input is greater than $V_{ref}/2$, the MSB remains 1; otherwise, the MSB is assigned 0 on the second

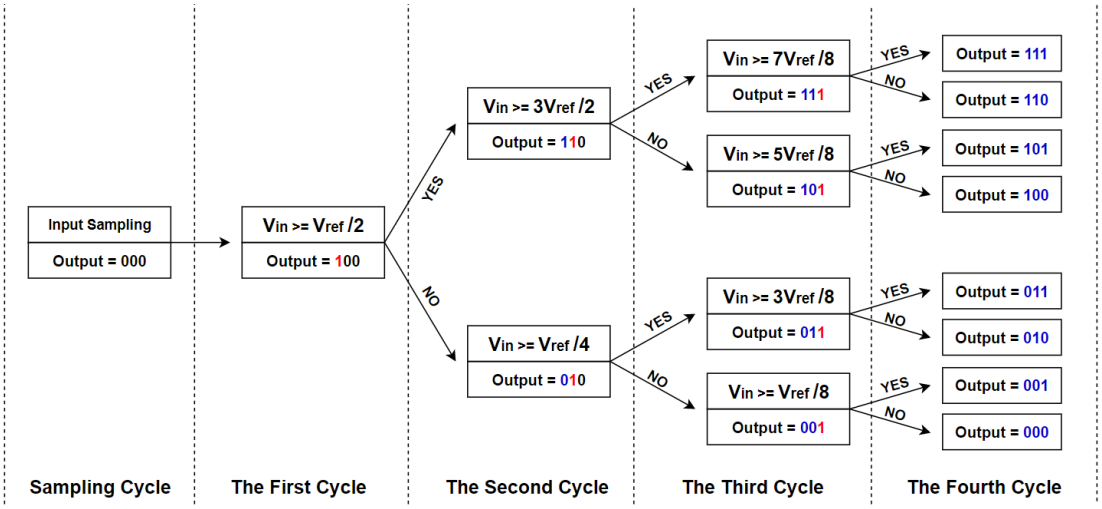

Figure 3.3 : SAR ADC algorithm for 3-bit conversion.

cycle. Likewise, MSB-1 is set to 1 during the second cycle. DAC output is $3V_{ref}/4$ if the MSB value is 1; otherwise, it is $V_{ref}/4$. Then, the comparator compares the sampled input and DAC output, and at the third cycle, SAR logic determines whether MSB-1 is set to 1 or 0 with respect to the comparator result. Simultaneously, the LSB value is set to 1. On the fourth cycle, the LSB is determined, and the conversion is complete. Therefore, the N-bit conversion of the sampled input takes N+1 cycles to complete. Due to the fact that an additional clock cycle is typically reserved for sampling, one conversion requires N+2 clock cycles.

Figure 3.4 depicts a fully differential, binary-weighted SAR ADC preferred in our design for implementing the SAR algorithm due to its simplicity and power efficiency. A capacitive DAC structure is also utilized as a sample and hold circuit. Thus, an additional sample and hold circuit is not required. During the sampling cycle, the DAC samples the input onto capacitors. In subsequent cycles, the comparator compares the positive and the negative outputs of the DAC until the LSB is determined. The remainder of this section will describe the DAC, switch, comparator, and SAR control logic designs implemented in this work.

3.2.1 Binary-Weighted DAC Design

The DAC is one of the crucial parts of a SAR ADC because its linearity directly affects the resolution of the converter. Although there are different DAC architectures

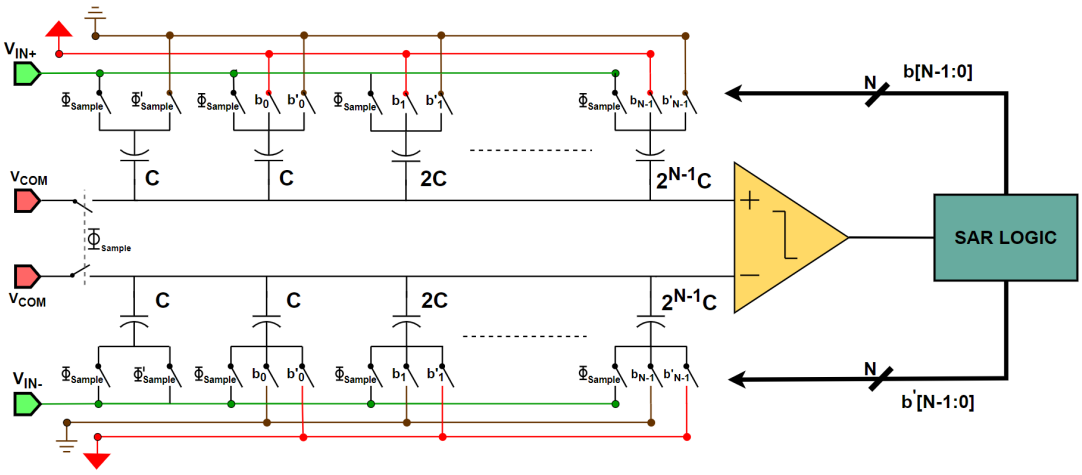

Figure 3.4 : A differential SAR ADC block diagram.

proposed in the literature, capacitor-based DAC architectures are commonly used in SAR ADCs [11]. Thanks to the zero static power consumption of the capacitor, power efficiency is significantly improved. The binary-weighted capacitive DAC is the one that is used the most. The N-bit binary-weighted DAC is composed of a binary-weighted capacitor array ranging from C to 2^N-1C and a series of switches controlled by SAR logic based on the comparator result. A Schematic of the binary-weighted DAC is depicted in Figure 3.5. An extra dummy capacitance with a value equal to unit capacitance, C, is added to make the total capacitance equal to 2^NC. Furthermore, since the input sampling is done by the DAC capacitors, an extra S&H circuit is not required in this topology. The operation of the binary-weighted DAC could be described in the following manner:

- At the time of a sample, the sampling switch connects the positive and negative input voltages to the bottom plates of the upper and lower capacitor arrays, respectively. On the other hand, the common mode voltage (V_{com}) is connected directly to the top plates of all capacitors. Therefore, the total charge stored in the capacitors is equal to

$$Q_{totalp} = 2^N.C.(V_{com} - V_{inp})$$
$$Q_{totaln} = 2^N.C.(V_{com} - V_{inn}) \quad (3.1)$$

- After sampling, the upper capacitor array is connected to the ground except for the MSB capacitor, which is connected to V_{DD}. On the other hand, the top plate of the

capacitors remains floating, and the voltage at this node (V_{out+}) is calculated from charge conservation as follows:

$$Q_{totalp} = 2^N.C.(V_{com} - V_{inp}) = 2^{N-1}.C.V_{out+} + 2^{N-1}.C.(V_{out+} - V_{DD})$$
$$V_{out+} = V_{com} - V_{inp} + \frac{V_{DD}}{2} \tag{3.2}$$

- In contrast to the upper capacitor array, the lower capacitor array, except for the MSB capacitor, is connected to V_{DD}. Then, the voltage of the negative output (V_{out-}) is calculated as

$$Q_{totaln} = 2^N.C.(V_{com} - V_{inn}) = 2^{N-1}.C.V_{out-} + 2^{N-1}.C.(V_{out-} - V_{DD})$$
$$V_{out-} = V_{com} - V_{inn} + \frac{V_{DD}}{2} \tag{3.3}$$

- Then, in the next cycle, the MSB of the upper capacitor array remains connected V_{DD} whereas the MSB of the lower capacitor array remains connected to the ground and vice versa with respect to the comparator decision. At the same time, the MSB-1 capacitor in the upper capacitor array is connected to V_{DD}, and the MSB-1 capacitor in the lower capacitor array is connected to the ground. If MSB capacitor of the upper array is connected to V_{DD}, from conservation of the charge V_{out+} and V_{out-} are calculated as

$$Q_{totalp} = 2^{N-2}.C.V_{out+} + 2^{N-1}.C.(V_{out+} - V_{DD}) + 2^{N-2}.C.(V_{out+} - V_{DD})$$
$$V_{out+} = V_{com} - V_{inp} + \frac{3.V_{DD}}{4} \tag{3.4}$$

$$Q_{totaln} = 2^{N-2}.C.(V_{out-} - V_{DD}) + 2^{N-1}.C.V_{out-} + 2^{N-2}.C.V_{out-}$$
$$V_{out-} = V_{com} - V_{inn} + \frac{V_{DD}}{4} \tag{3.5}$$

Similarly, if MSB capacitor is connected to ground

$$Q_{totalp} = (2^{N-2}.C + 2^{N-1}.C).V_{out+} + 2^{N-2}.C.(V_{out+} - V_{DD})$$
$$V_{out+} = V_{com} - V_{inp} + \frac{V_{DD}}{4} \tag{3.6}$$

$$Q_{totaln} = 2^{N-2}.C.V_{out-} + (2^{N-2}.C + 2^{N-1}.C).(V_{out-} - V_{DD})$$
$$V_{out-} = V_{com} - V_{inn} + \frac{3.V_{DD}}{4} \tag{3.7}$$

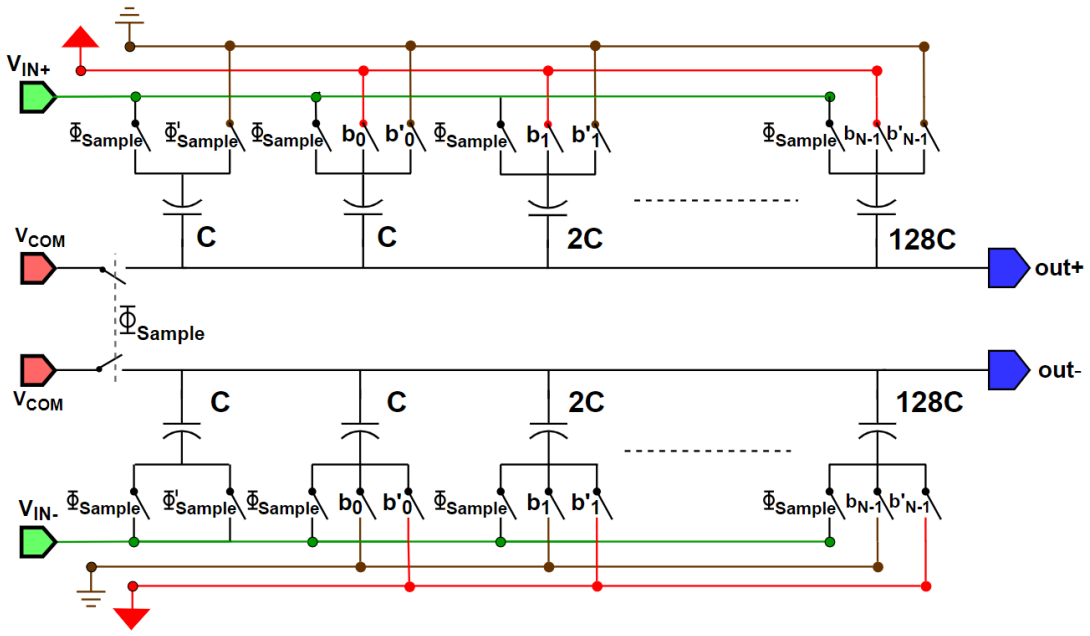

Figure 3.5 : Schematic of binary-weighted DAC.

- All bits can be resolved using the same method, and the conversion is complete.

A benefit of the binary-weighted DAC is that the output node parasitic capacitance does not affect the linearity of the DAC. If C_P is considered a parasitic capacitance at the output, then we can rewrite Equation 3.2 as follows:

$$Q_{total} = 2^N.C.(V_{com} - V_{in}) = (2^{N-1}.C + C_P).V_{out+} + 2^{N-1}.C.(V_{out+} - V_{DD})$$
$$V_{out+} = (V_{com} - V_{inp} + \frac{V_{DD}}{2})(\frac{2^N.C}{2^N.C + C_P}) \quad (3.8)$$

As can be seen from the calculation, the output parasitic capacitance causes attenuation. Since the same attenuation applies to all cycles, linearity is preserved.

There are two primary benefits to connecting the V_{out+} and V_{out-} nodes to V_{com} at the sampling phase. First, it stops the nodes V_{out+} and V_{out-} from falling below ground. The second advantage is that, after conversion, DAC output settles around V_{com}.

Although binary-weighted DACs appear to be an attractive option for high-speed communication systems, they are severely limited in terms of bandwidth and speed [12]. First of all, the DAC size grows exponentially as the number of bits increases. For example, the minimum-sized metal insulator metal (MIM) capacitor in the TSMC 65nm process has a capacitance of 10 fF, so for an 8-bit SAR ADC, the MSB

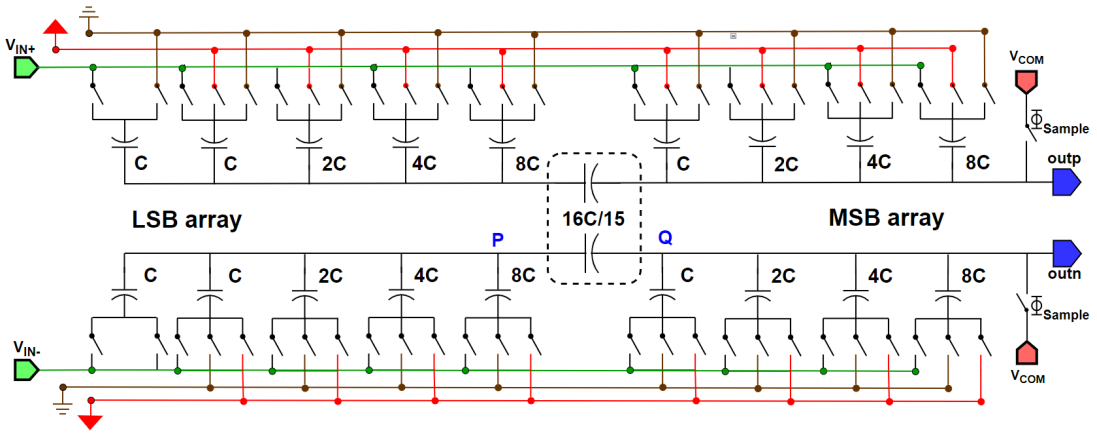

Figure 3.6 : Schematic of 8-bit binary-weighted split DAC.

capacitance is equal to 1.28 pF. In addition, to achieve a 25 MHz input sampling bandwidth for 50 MS/s applications, the input sampling switch resistance must be less than 283 Ω, which is difficult to achieve when interconnection and termination resistance is considered. Although [13] designs and implements a 0.75 fF unit capacitor in the 65 nm process, this requires precise knowledge and confidence in the process technology, as well as the fabrication and measurement of test structures, and capacitor mismatch becomes a problem. The other drawback of increasing capacitance is that it makes reference buffer specifications difficult and increases the required bias current for it. Therefore, power consumption increased excessively.

One method to reduce total DAC capacitance is dividing the capacitor array into two sub-arrays, MSB and LSB DAC arrays, by connecting them via a bridge capacitor. Figure 3.6 demonstrates a schematic of an 8-bit split DAC architecture; the total capacitance is 256 C before and 31 C after applying the split DAC architecture. The functionality of the split DAC architecture is identical to that of the binary-weighted DAC, but its total capacitance is significantly lower.

In the split DAC architecture equivalent capacitance seen from the MSB array side should be equal to the unit capacitance, C, in order to make total capacitance 16 C. The operation of the split DAC architecture can be described in the following manner:

$$C_{eq} = \frac{(16C/15).16C}{(16C/15)+16C} = 1C \tag{3.9}$$

- The operation of the MSB array is the same as that of a traditional binary-weighted DAC. Therefore, we focus on the operation of the LSB DAC array. When the 8C capacitor in the LSB array is connected to V_{DD}, the change in voltage at the node P V_P is calculated as

$$\Delta V_P = \frac{8C}{16C + (\frac{16C}{15} // 15C)} \; x \; V_{DD} \tag{3.10}$$

  where second term in denominator is equivalent capacitance of bridge capacitor and MSB array seen from LSB array side

- Then, using voltage division between the bridge capacitance and the MSB array, the voltage change in the output node is calculated as

$$\Delta V_{out} = \Delta V_P(\frac{\frac{16C}{15}}{15C + \frac{16C}{15}})$$
$$\Delta V_{out} = \frac{V_{DD}}{32} \tag{3.11}$$

- The effect of other capacitances in the LSB array on the output node can be easily calculated using equations 3.10 and 3.11. Also, when all the capacitances in the LSB array are connected to V_{DD}, it is evident that the change in voltage at the output is $V_{DD}/16$. This demonstrates that the LSB of the MSB array has the same weight as the LSB array.

However, the function of the split capacitor architecture deviates from the ideal because of the mismatch between the fractional bridge capacitor and other capacitors, resulting in non-linearity and limiting the ADC's precision. Parasitic capacitance at node P also affects functionality adversely. Another problem is that the voltage at node P may exceed or fall below the rails. This is possible because node P is floating during the conversion process. Figure 3.7 illustrates the split capacitor array architecture that is capable of resolving both mismatches and over-range problems. Fractional bridge capacitance was replaced with an integer value bridge capacitance for better matching. Therefore, a decoupling capacitor is added to the LSB array in order to equalize the weight of the LSB of the MSB array and the total weight of the LSB array. In addition, the decoupling capacitor eliminates the over-range issue, as the

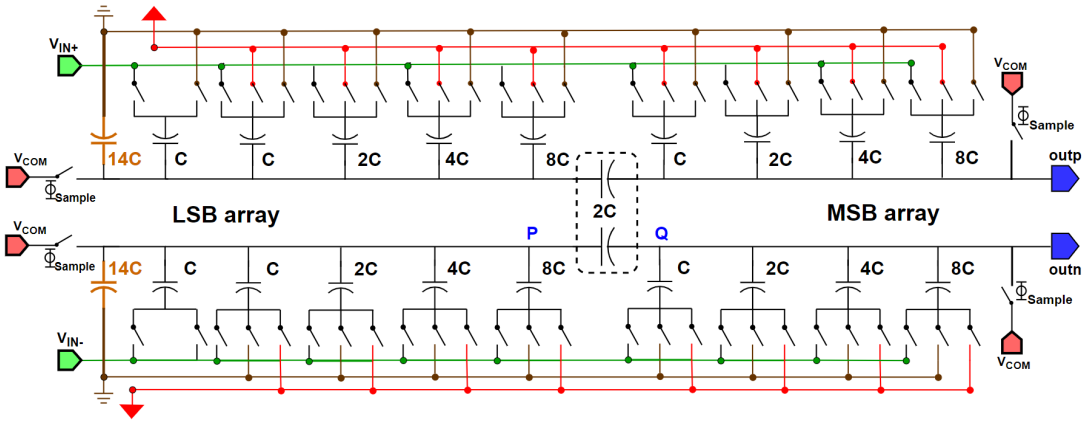

Figure 3.7 : Schematic of modified 8-bit binary-weighted split DAC.

voltage jumps generated by the LSB bits are now reduced by a factor of nearly half at the expense of area. In addition to this, it enables rail-to-rail signal range, that could considerably improve the SNR [14].

If the bridge capacitance is set to 2C, the smallest integer number that may be selected, the decoupling capacitor value can be calculated as follows:

$$C_D = (C_B - \frac{2^L}{2^L - 1})(2^L - 1)$$
$$C_D = 14C \tag{3.12}$$

where C_D is decoupling capacitor and L is number of bits in the LSB array.

Different from than previous split DAC architecture, the equivalent capacitance seen from the MSB side is larger than the unit capacitance, C, in this architecture. It is equal to 1.875 C. However, the total weight of the LSB array is the same the lowest bit in the MSB array. When the lowest bit is connected from the ground to V_{DD}, voltage change at the output node is equal to

$$\Delta V_{out} = \frac{V_{DD}}{15C + (30C//2C)}$$
$$\Delta V_{out} = 0.05926 V_{DD} \tag{3.13}$$

The second term in the denominator of Equation 3.13 is the equivalent capacitance of the bridge capacitor and total capacitor of the LSB array seen from the MSB side. On the other hand, voltage change at the output node when all the capacitors in the LSB

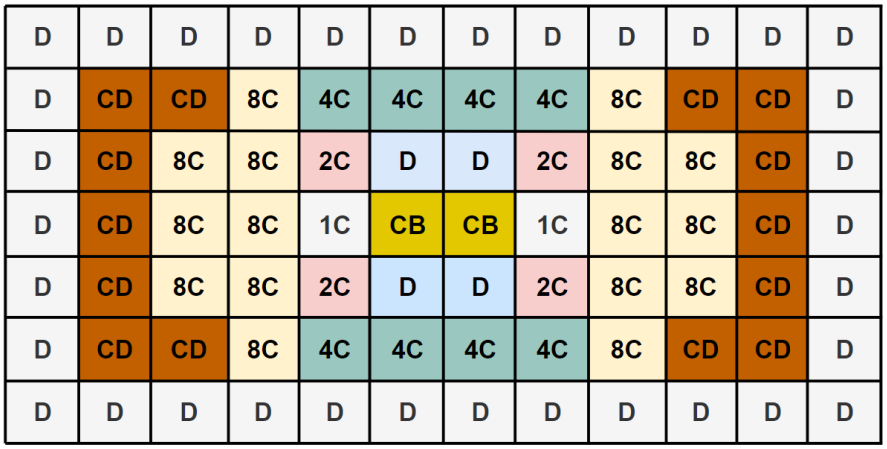

Figure 3.8 : Placement of the capacitor in layout.

array are connected V_{DD} is found as

$$\Delta V_{out} = \frac{V_{DD}\ x\ 16C}{30C + (15C//2C)} x \frac{2C}{2C + 15C}$$
$$\Delta V_{out} = 0.05926 V_{DD} \tag{3.14}$$

The first term in Equation 3.14 is defined as the voltage change at node P, and the second term comes from voltage sharing between bridge capacitance and the MSB array. As can be seen from Equations 3.13 and 3.14, connecting all capacitance in the LSB array to V_{DD} has the same effect on the output of the DAC as connecting the lowest bit in the MSB array to V_{DD}. However, because of the total capacitance increase from 16 C to 16.875 C, a gain error occurs and equals

$$GainError = \frac{16C}{16.875C} = 0.948 \tag{3.15}$$

This can also be interpreted as adding an extra 0.875 C of parasitic capacitance to the output node. As noted previously, the output node parasitic capacitance does not affect the linearity of the DAC. However, we must be concerned about parasitic decoupling capacitors at node P and parasitic coupling capacitors between nodes P and Q, as these capacitances result in a mismatch between the LSB array and the MSB array.

The placement of capacitors in the layout is also important in DAC design. Any mismatch between capacitors results in non-linearity, so capacitors should be placed as symmetrically as possible without making routing too complicated. Furthermore, MIM capacitors are preferred over MOM capacitors due to their higher accuracy. The

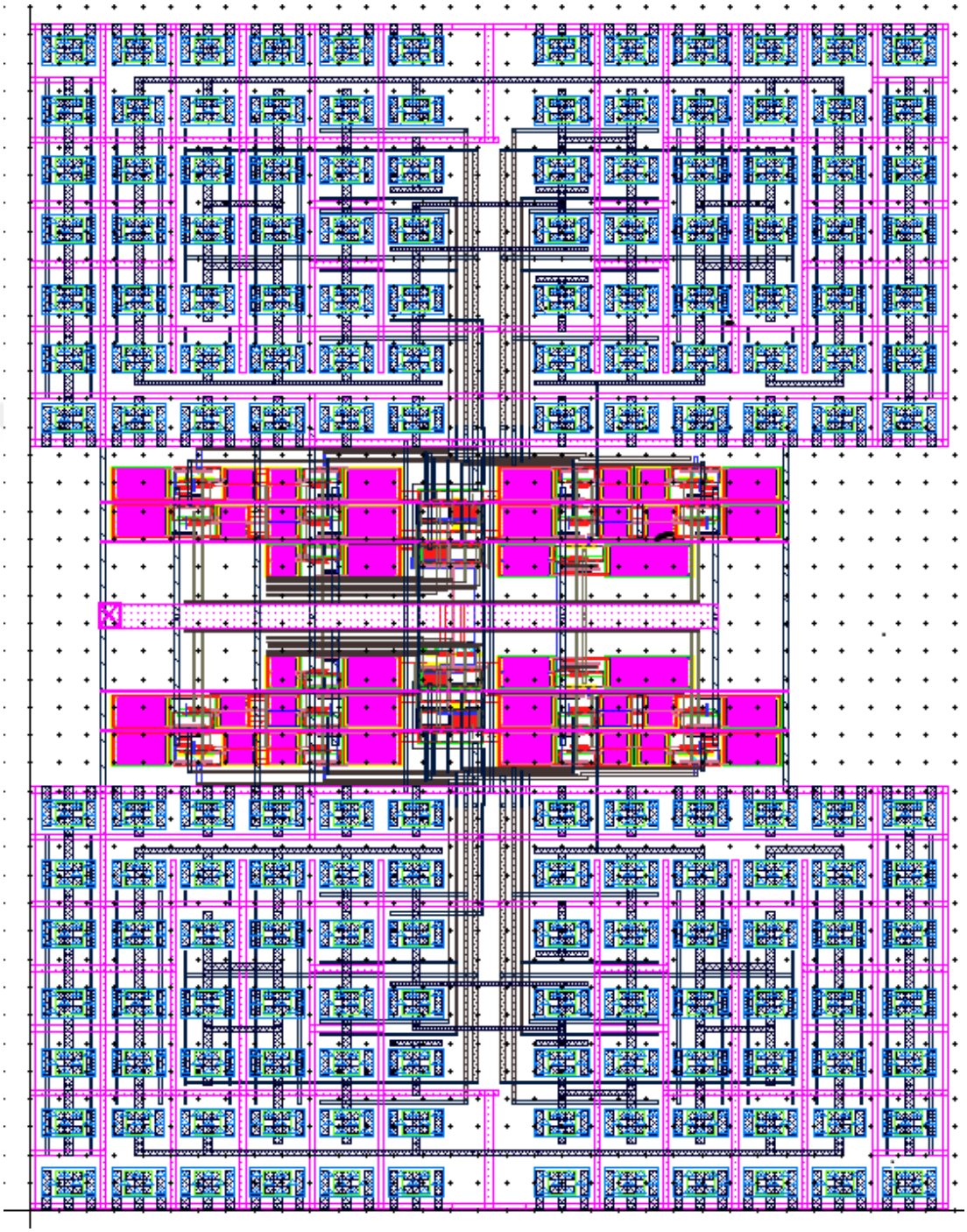

Figure 3.9 : Layout of the DAC with switches.

layout scheme and layout of the DAC with switches are shown in Figures 3.8 and 3.9, respectively.

3.2.2 Switch Design

Thanks to the capacitive nature of the DAC, it also performs a sample and hold operation in our design. Therefore, each capacitor in the DAC contains three different switches. These switches are used to sample the negative and positive reference voltages as well as the input signal. Three distinct switch topologies are therefore designed and implemented. We sample the positive reference voltage, V_{DD}, via a single PMOS switch since PMOS switches can pass high-level signals quite well. On the other hand, we sample the negative reference voltage, ground, by using a single NMOS switch, which is good at passing low-level signals. In comparison to switches that sample negative and positive reference voltages, sampling the input signal requires a more complex switch design, as any non-linearity in the sampled signal has a detrimental effect on the SNDR value. Thus, a bootstrapped NMOS switch with a constant V_{GS} voltage is utilized as a sampling switch to increase switch linearity, and its schematic is shown in Figure 3.10 [15].

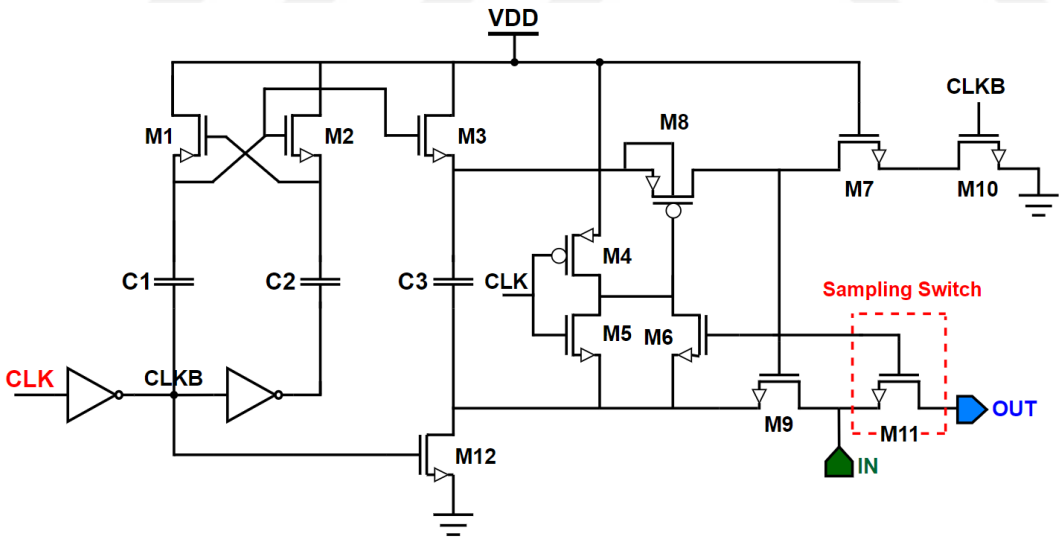

Figure 3.10 : Schematic of bootstrap switch.

As shown in Figure 3.10, the bootstrapped NMOS switch is controlled by a CLK signal, which turns the sampling switch M_{11} on and off. When the CLK signal is low, M_{11} is turned off via M_7 and M_{10}. Simultaneously, the C_3 capacitor is charged

to V_{DD} via M_3 and M_{12}. When the CLK signal is high C_3 will operate as a battery to keep V_{GS} of the sampling switch at $_{DD}$. M_8 and M_9isolate the sampling switch from C_3 while it is charging. Due to the fact that M_5 pulls down the gate of M_8 at high CLK, the charge could flow from the battery capacitor C_3 to the gate of M_{11}. This turns on M_9 and M_{11}. The bottom plate of the C_3 is connected to the input V_{IN} via the M_9. As C_3 is charged to V_{DD}, the top plate voltage of it is equal to V_{IN}+V_{DD}. As a consequence, the input independent V_{GS} for the sampling switch is obtained by connecting C_3 to the sampling switch, M_{11}.

Bootstrap circuits should be carefully designed to ensure that no device experiences a terminal voltage greater than V_{DD}. Therefore, M_7 and M_{13} are added in order to alleviate stress on the transistors. M_7 reduces the V_{DS} and V_{GD} experienced by device M_{10} and M_6 regulates V_{GS} of M_8 to ensure that it does not exceed V_{DD}.

The unit size switch technique is used in order to preserve the linearity of the DAC. The switch sizes have been increased or decreased proportionally to the capacitors to which they are connected. For instance, the size of a switch connected to a 2C capacitor is twice that of a switch connected to a unit capacitor, C. The layout of the bootstrap switch with the unit size is depicted in Figure 3.11.

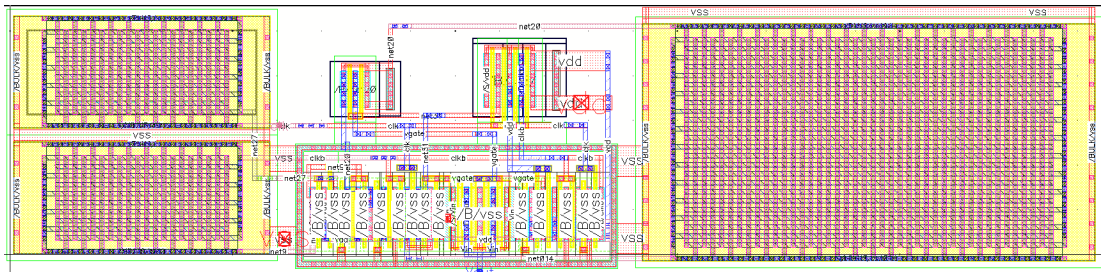

Figure 3.11 : Layout of unit size bootstrap switch.

3.2.3 Comparator Design

The comparator utilized in our design comprises a preamplifier and a strongARM latch comparator with an SR latch. The preamplifier shown in Figure 3.12 is biased with 100 μA, and its differential DC gain and bandwidth for a 50 fF load are approximately equal to 16 dB and 4 GHz, respectively. There are different benefits to utilizing a preamplifier before the strongARM latch comparator. First, the preamplifier decreases

the comparator's input referred offset and thermal noise. The most important benefit of using a preamplifier is that it reduces kickback noise generated by the strongARM latch at the rising and falling edges of the CLK signal. Also, the input common mode of the strongARM latch is adjusted via preamplifier.

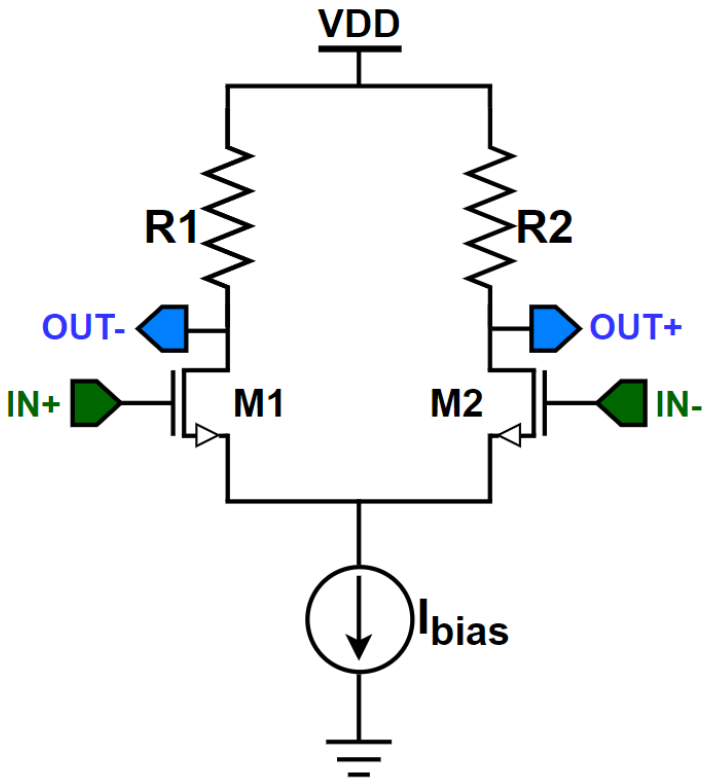

Figure 3.12 : Schematic of designed preamplifier.

The strongARM latch that is shown in Figure 3.13 is preferred as a comparator for two reasons. StrongARM latch does not consume static power, resulting in high power efficiency. The second benefit is its high conversion rate. StrongARM latch uses a cross-coupled inverter pair at the output in order to pull the output up or down instantaneously. The straightforward operation of the strongARM latch comparator could be divided into three different phases. In the pre-charge phase, when CLK is low, S_1-S_4 switches charge nodes P, Q, OUT+, and OUT- to VDD. During the amplification phase, when CLK is set to high, the S_1-S_4 switches to turn off. M_1 and M_2 draw a differential current proportional to IN+ - IN-, and discharge C_P and C_Q at different rates. When the voltage of V_P and V_Q falls below V_{DD}, M_4 and M_5 transistors in the cut-off region but leakage current because of non-zero V_{DS} discharge output nodes slowly. Node P discharged faster than node Q if IN+ was greater than IN-, and vice

versa. M_4 enters the saturation region and pulls OUT- to ground when the voltage of node P falls below V_{DD}-V_{TH}. OUT+ has pulled up to V_{DD} instantaneously thanks to the cross-coupled inverter structure, and the comparison is completed.

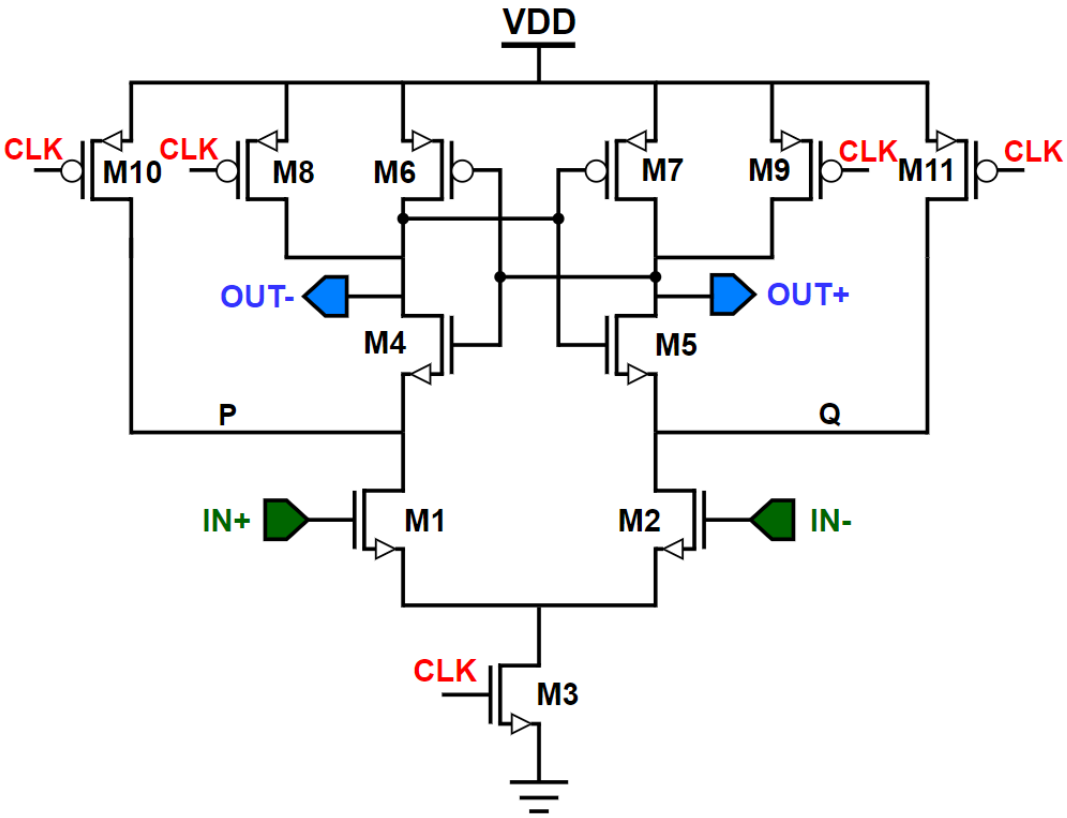

Figure 3.13 : Schematic of StrongARM latch.

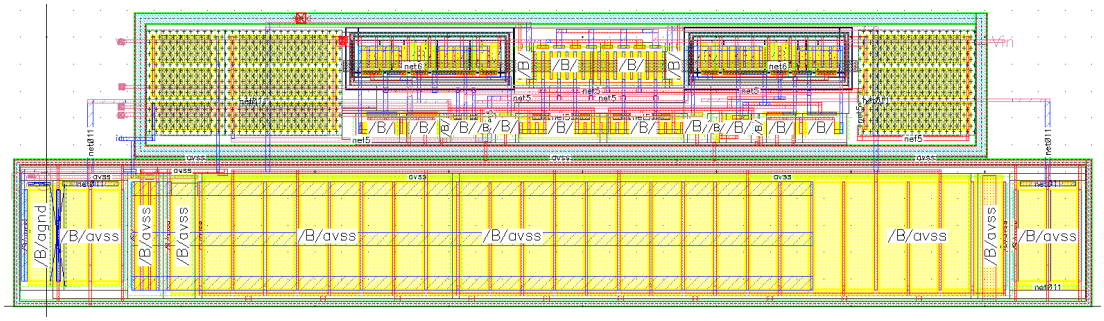

Figure 3.14 : Layout of the comparator.

In our design, the offset of the comparator should be smaller than LSB/2, which is equal to 586 μV. In order to reduce the offset, the time spent in the amplification phase should be increased. The first method to increase the amplification phase time is to increase the amount of charge that needs to be discharged by adding external capacitance to the P and Q nodes. The second method to increase the duration of the

amplification phase is increasing the threshold of the M_3 transistor. Furthermore, the discharging rate is proportional to the overdrive voltage of the input pair transistors. Therefore, a small overdrive voltage also leads to more time spent in the amplification phase and a decreased comparator offset. The first method preferred in our design is to reduce the offset. The layout of the comparator is shown in Figure 3.14.

3.2.4 Succesive Approximation Register

The digital component of the SAR ADC, the successive approximation register, is responsible for determining the converter's output bits in relation to the comparator's output. As shown in Figure 3.15, the successive approximation register consists of a shift register and a code register. While the shift register includes a D flip-flop with synchronous set and reset, the code register consists of a D flip-flop with asynchronous set and reset. The operation of the SAR logic is explained as follows:

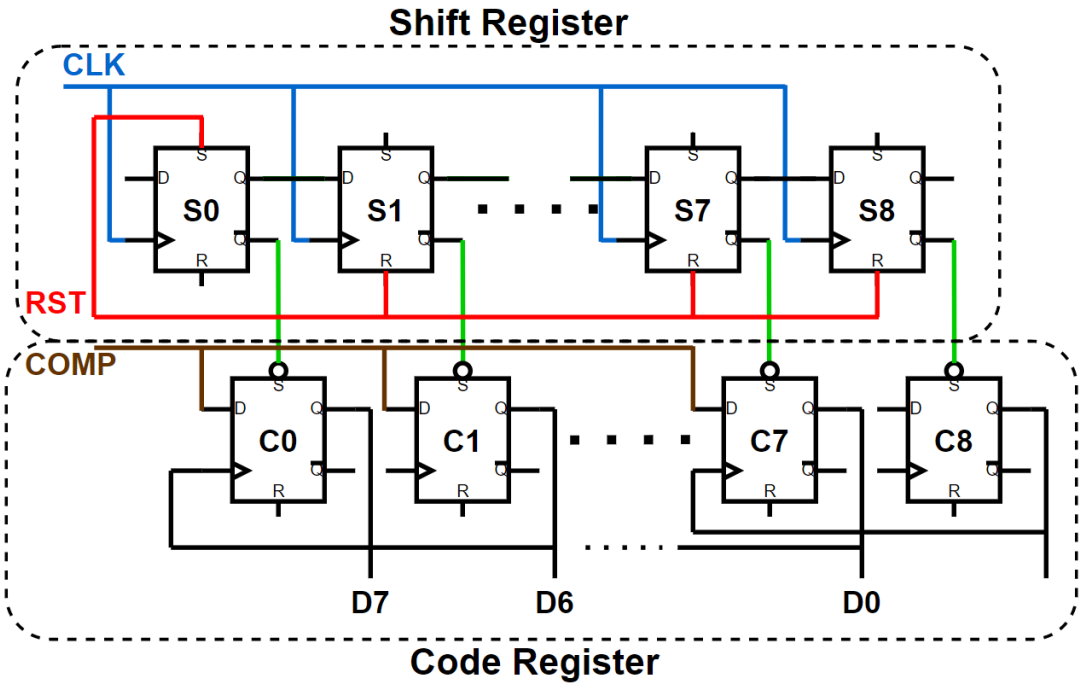

Figure 3.15 : Schematic of SAR logic.

- During the sample phase, all flip-flops are reset by sampling clock except for S0, which is set to 1.
- After the sampling phase, S1 is set to 1, and D6 is simultaneously pulled up via the asynchronous D flip-flop C1 at the first rising edge of the clock. D6 is used as the

clock for C0, so D7 receives the final value based on the comparator's output at the rising edge of D6. The important point is that the comparator result should be ready before the D6 bit is set to 1. For this reason, the comparator should operate first. After the comparator outputs are ready, the SAR logic operates. Thus, there should be a fixed delay between the comparator clock and the SAR clock.

- In the next cycle S2 is set to 1 and the same processes are continued until the LSB is resolved.

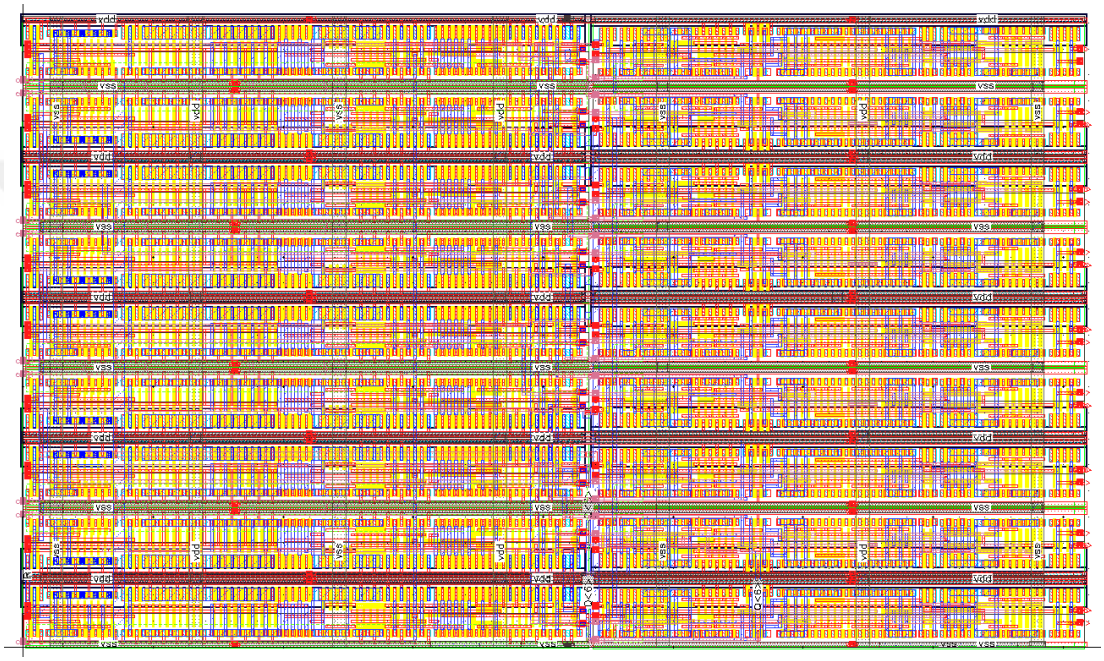

Figure 3.16 : Layout of the SAR logic.

Because each bit is decided in the following clock cycle, this type of SAR logic requires an additional flip-flop for both the shift register and the code register. In other words, to determine the final value of D0, C8 must be set to 1 because C8's output serves as the clock for C7. Therefore, N+1 clock cycles are required to convert N bits. Therefore, one conversion requires 10 clock cycles in our design, nine of which are used to determine the output bits and one for sampling. SAR logic and the comparator should therefore work at 500 MHz, which is ten times the sample frequency. We were unable to synthesize the SAR logic layout due to a lack of standard cell libraries at TSMC 65nm. Therefore, we created a custom layout for it, as shown in Figure 3.16.

3.3 Residue Amplifier

As stated previously, the converter designed in this study can be viewed as a pipeline ADC consisting of an 8-bit SAR ADC and a 3-bit flash ADC in the first and second stages, respectively. At the last cycle of SAR ADC, residue voltage is generated at the output of the DAC. The switch capacitor amplifier depicted in Figure 3.21 is used to sample and amplify the residue voltage. The design requirements for the flash ADC are reduced by using a sample-and-hold amplifier with a gain greater than one. The operation of the switch capacitor amplifier can be explained as follows:

- In the phase 1 cycle, the residue voltage is sampled at C_1. The bottom plate of the C_1 is connected to the input, while the top plate is connected to the inputs of the operational amplifier. In this cycle, the operational amplifier is operating in buffer configuration, where both inputs and outputs of the operational amplifier is shorted and these nodes are held at V_{COM} with the help of the common mode feedback circuit [4]. The differential charge stored in capacitances is then calculated as

$$\Delta Q_{C1} = C_1.(V_{IN-} - V_{IN+}) \tag{3.16}$$

- In phase 2 cycle, amplification and hold operation is performed. The differential charge stored at the this cycle is equal to

$$\Delta Q_{C2} = C_2.(V_{OUT+} - V_{OUT-}) \tag{3.17}$$

  The bottom plate of each C_1 capacitance is connected to V_{com}, while the top plates are connected to the operational amplifier inputs. Because the negative and positive inputs of the operational amplifier have the same voltage in a closed-loop configuration, there is no differential charge on the C_1 during the hold phase. Then, from Equations 3.13 and 3.14, the differential gain of the circuit is calculated as

$$\begin{gathered} Q_{initial} = Q_{final} \\ C_1.(V_{IN-} - V_{IN+}) = C_2.(V_{OUT+} - V_{OUT-}) \\ \frac{(V_{OUT+} - V_{OUT-})}{(V_{IN+} - V_{IN-})} = -\frac{C_1}{C_2} \end{gathered} \tag{3.18}$$

There are some things about residue amplifier that we believe are useful to point out. The input is connected to the bottom plate of the capacitor because parasitic

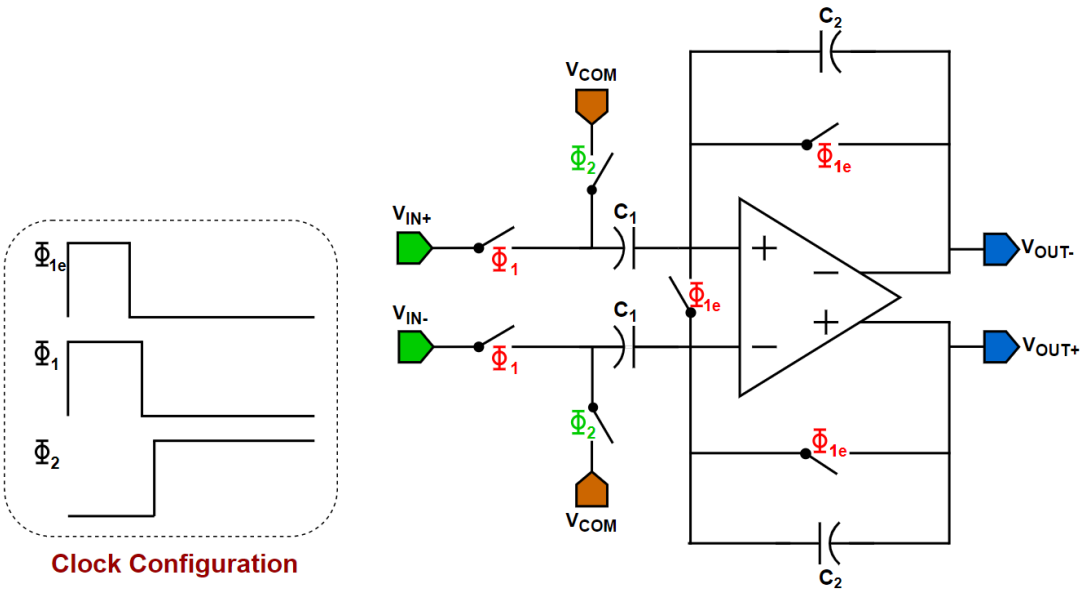

Figure 3.17 : Schematic of residue amplifier.

capacitance between the bottom plate and substrate should not be coupled directly to the input of the operational amplifier for two reasons. The first coupling of noise to inputs of the operational amplifier can have disastrous consequences for the circuit's output [4]. The second is parasitic capacitance on the inputs of the operational amplifier reduces the feedback factor in the hold mode. Therefore, settling time increases, and a gain error occurs. When the bottom plate is connected directly to the input, however, the effect of parasitic capacitance is reduced. In sampling mode, the parasitic capacitance is connected to V_{IN}, while in the hold mode, it is connected to V_{COM}. These two nodes are expected to have low impedance. Therefore, this node is unaffected by substrate noise. In order to reduce the amount of charge injection and clock feedthrough, the bottom plate sampling technique is used. As depicted in the clock waveforms in Figure 3.21, the switches controlling the top plates of the sample capacitors close slightly before the switches controlling the bottom plates. The layouts of the residue amplifier and flash-assisted SAR ADC are shown in Figures 3.22 and 3.23, respectively.

3.4 3-Bit Fully Differential Flash ADC

Flash ADC is the fastest ADC architecture in the literature, along with pipeline ADC [16]. It has a simpler design because it does not need an operational amplifier

or switch capacitor circuit. However, the number of comparators required for flash ADC increases exponentially as the resolution increases, resulting in increased power consumption and die area requirements. As a result, designing a high-resolution flash ADC is generally discouraged. In hybrid ADCs, nonetheless, low-resolution flash ADCs could be favoured as auxiliary ADC to improve the accuracy of the main ADC. In this study, a 3-bit flash ADC is used to assist an 8-bit SAR ADC, resulting in a total resolution of 11 bits.

Flash ADC consists of a reference ladder, comparators, and an encoder. Seven different reference voltage values to compare with the input signal are generated by the series resistance line, which is shown in Figure 3.17. A complex structure like a reference buffer is not needed in order to generate reference voltages since the reference voltages are connected to the gates of the transistors, that is, the high-impedance node. However, due to the latch structure of the comparator, kickback noise at the rising and falling edges of the clock might cause noise at reference voltage values. This noise should be smaller than LSB/2 so that the accuracy of the converter is not adversely affected. A preamplifier was employed in this design to reduce kickback

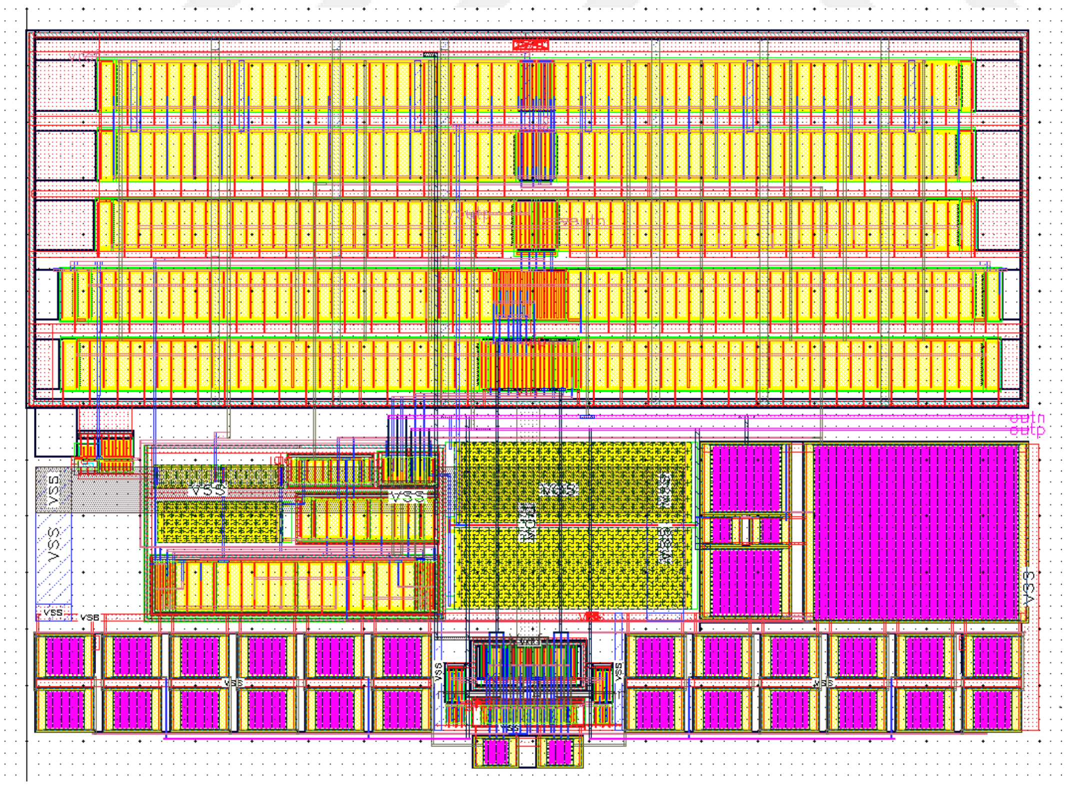

Figure 3.18 : Layout of the residue amplifier.

noise. Furthermore, decoupling capacitances were connected to reference nodes in order to filter the noise by sacrificing the die area.

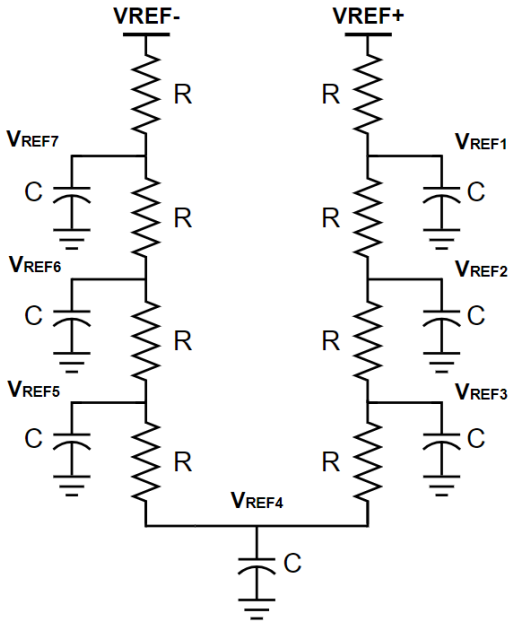

Figure 3.19 : Schematic of reference ladder.

The comparator block includes the preamplifier, strongARM latch comparator, and SR latch block. Figure 3.18 depicts the overall schematic of the comparator. A double differential pair with a resistive load was utilized as a preamplifier to compare the differential input with the differential reference voltage. In addition to lowering kickback noise, the preamplifier also relaxes the comparator's performance requirements. The conventional strongARM latch with an SR latch was preferred as the main comparator. The design considerations for the strongARM comparator were discussed in the preceding section, so they will not be repeated here.

The output of the comparators in a flash ADC is in a specific format known as thermometer code [4]. A thermometer-to-binary encoder should be used to convert the thermometer code to binary code. The conversion of the thermometer code to binary code can be performed in various ways, such as with a ROM encoder, a fat tree encoder, a Wallace tree encoder, etc. [17]. The ROM encoder is a standard and simple method for encoding thermometer code into binary code [18], [19]. Hence, the ROM encoder is preferred as a thermometer to the binary encoder.

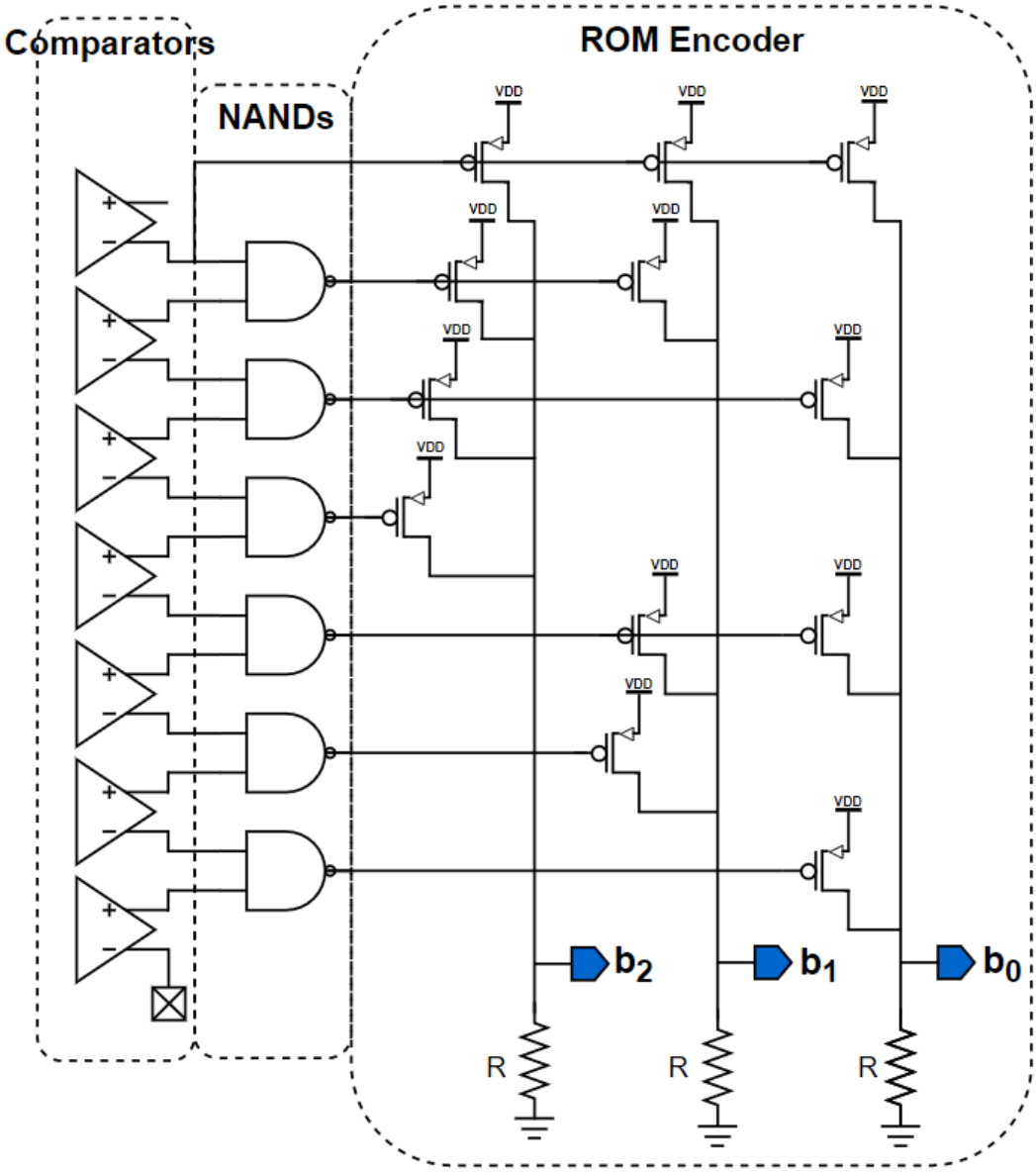

Figure 3.20 : Schematic of ROM encoder.

The ROM encoder consists of two phases. The thermometer code is converted to a 1 out of 2^N-1 code during the initial phase. An array of NAND gates can be utilized to generate this. In the second stage, the 1 out of 2^N-1 code is taken as input, selects the appropriate ROM rows, and creates the binary outputs depicted in Figure 3.19 for a 3-bit flash ADC. The layout design of the 3-bit flash ADC is shown in Figure 3.20.

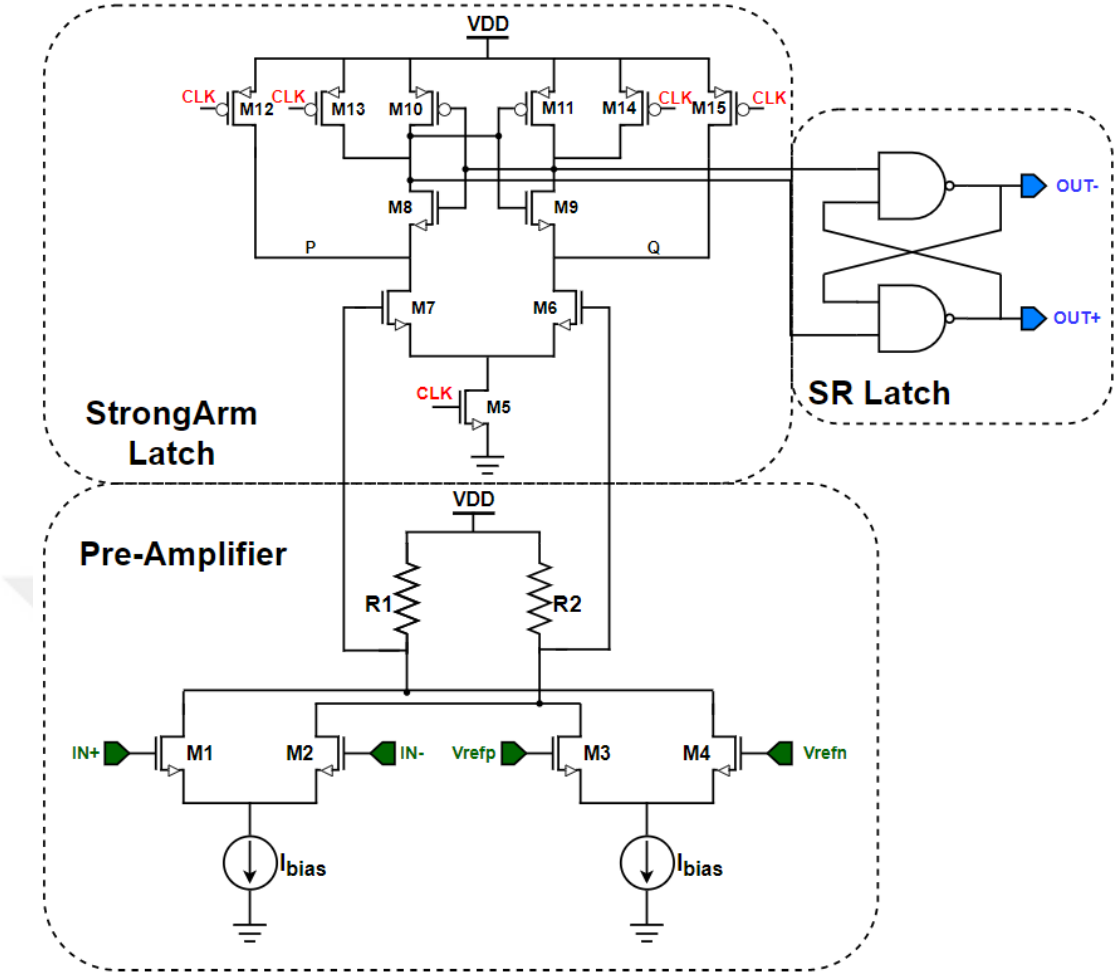

Figure 3.21 : Schematic of overall comparator in flash ADC.

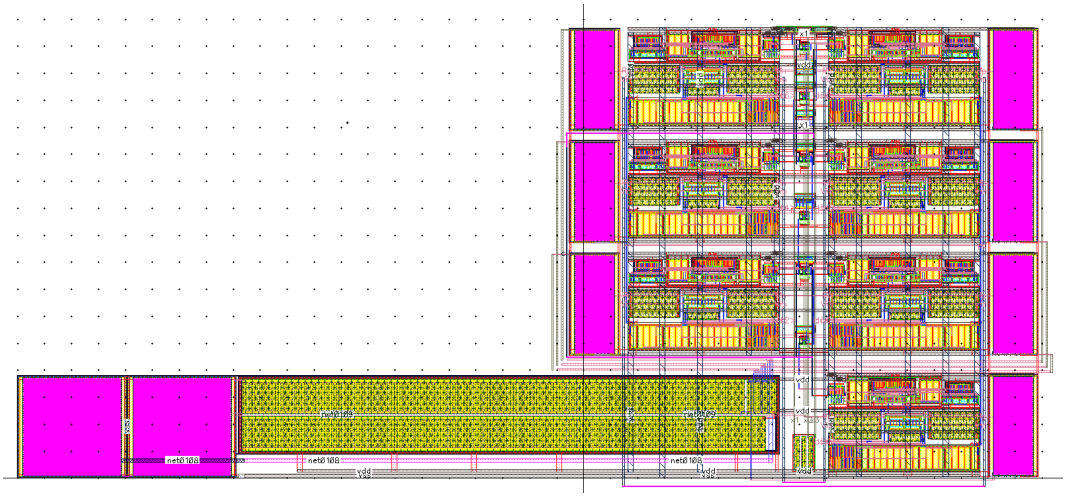

Figure 3.22 : Layout of the flash ADC

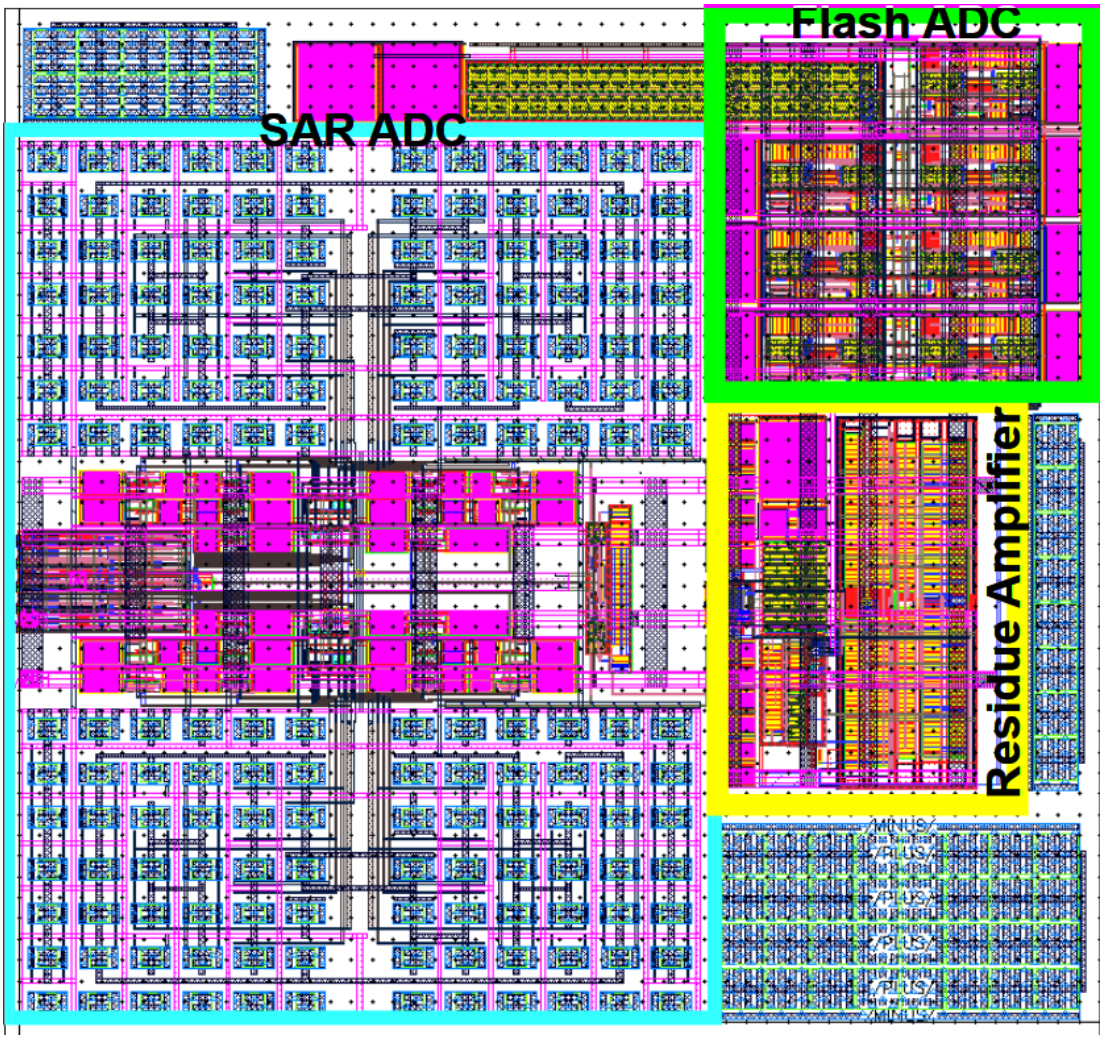

Figure 3.23 : Layout of the flash assisted SAR ADC.

4. SIMULATION RESULT

After the schematic-level design is complete, circuit functionality is validated by various simulations. In this chapter, system- and circuit-level simulation results of the design are provided.

4.1 Simulation Results of SAR ADC

Binary-weighted DAC, comparator, and overall SAR ADC simulation results will be shown in this part.

4.1.1 Modified Binary Weighted DAC

The DAC is one of the most important components because non-linearities caused by mismatches have a detrimental effect on the ADC's resolution. Furthermore, as the residue voltage of the DAC is converted to 3 bits via flash ADC, the linearity of the DAC is significantly more critical for our system. In order to test the linearity of the DAC, an 8-bit counter is used to provide a discrete ramp input. While a counter counts from 0 to 255, the output of the DAC is observed, and Figure 4.1 shows the simulation result.

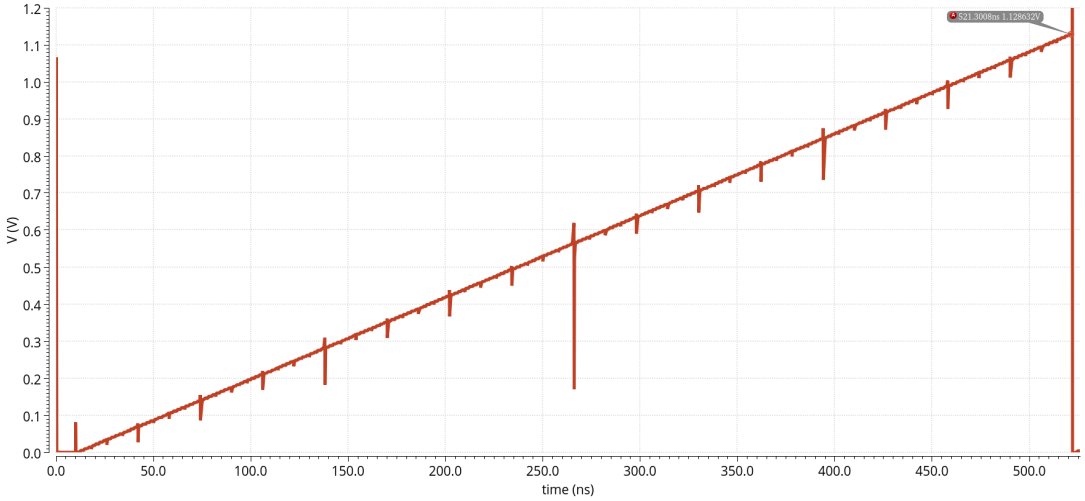

Figure 4.1 : The DAC output for ramp input.

Figure 4.1 shows that the output of the DAC at its maximum input value is 1.129 V instead of 1.2 V. This means that the DAC has a gain error equal to 0.941. This value is slightly lower than the value found in Equation 3.15, as parasitic capacitances from extraction increase the gain error. The gain error is a static error and does not disturb linearity. Also, Figures 4.2 and 4.3 display the results of measurements of the linearity of the DAC obtained with the DNL and INL functions of the Cadence calculator.

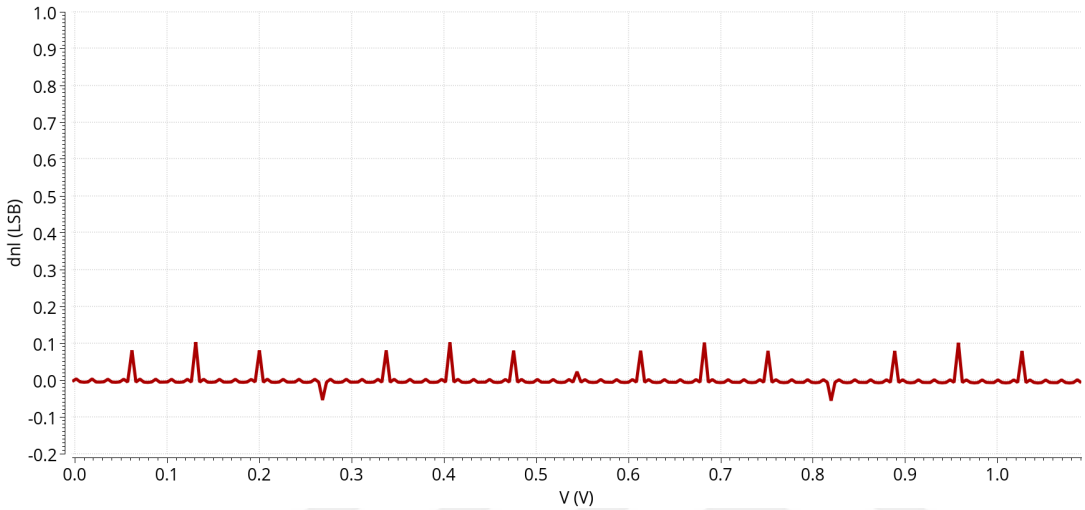

Figure 4.2 : DNL error of the DAC.

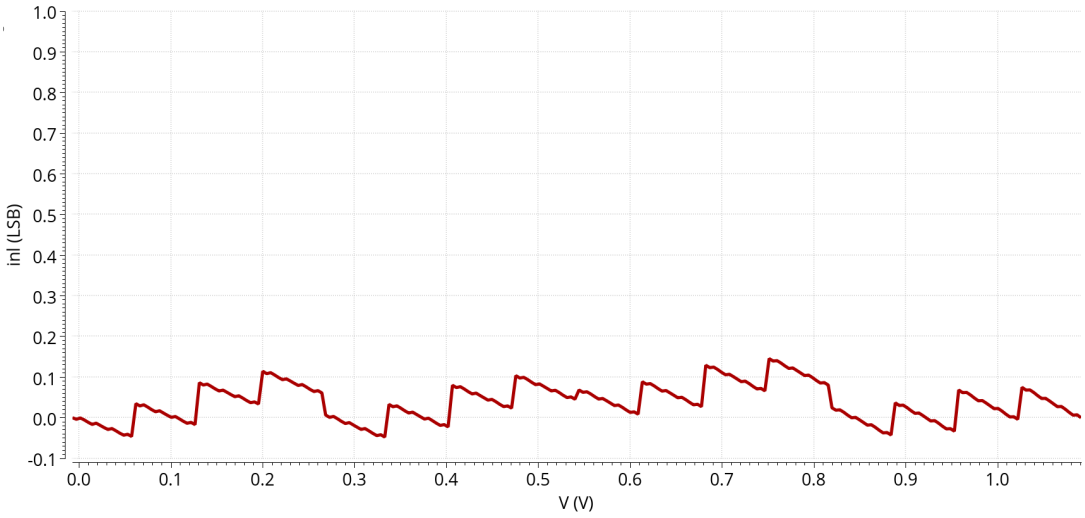

Figure 4.3 : INL error of the DAC.

Both DNL and INL simulation results are very satisfying for the 8-bit SAR ADC, as can be shown in Figures 4.2 and 4.3. Due to the DAC was also utilized for the sample and hold operation, the value of the unit capacitor should be chosen to take into account

the kT/C noise. Equation 4.1 shows how to calculate kT/C noise at 300K for this DAC architecture.

$$V_{rms} = 2\ x\ \sqrt{\frac{1.38\ x\ 10^{-23}\ x\ 300}{DAC\ Gain\ x\ Total\ DAC\ Capacitance}} \tag{4.1}$$

where the DAC gain is equal to 0.941 and the total DAC capacitance is equal to 94 C. As a rule, the kT/C noise should be equal to or slightly smaller than the quantization noise. Therefore, the minimum capacitance value can be found as

$$2\ x\ \sqrt{\frac{1.38\ x\ 10^{-23}\ x\ 300}{0.948\ x\ 94C}} < \frac{V_{LSB}}{\sqrt{12}}$$
$$C \geq\ 2\ fF \tag{4.2}$$

Unit capacitance is chosen as 45 fF in order to further decrease kT/C noise. Then, the switching resistance required to sample the input signal to 8C can be calculated as follows:

$$\tau = R\ x\ C$$
$$t = ln\ (\frac{1}{2^{11}})\ \tau = 7.624\ \tau$$
$$2\ ns \geq 7.624\ x\ 360 fF\ x\ R$$
$$R \leq 728\ \Omega \tag{4.3}$$

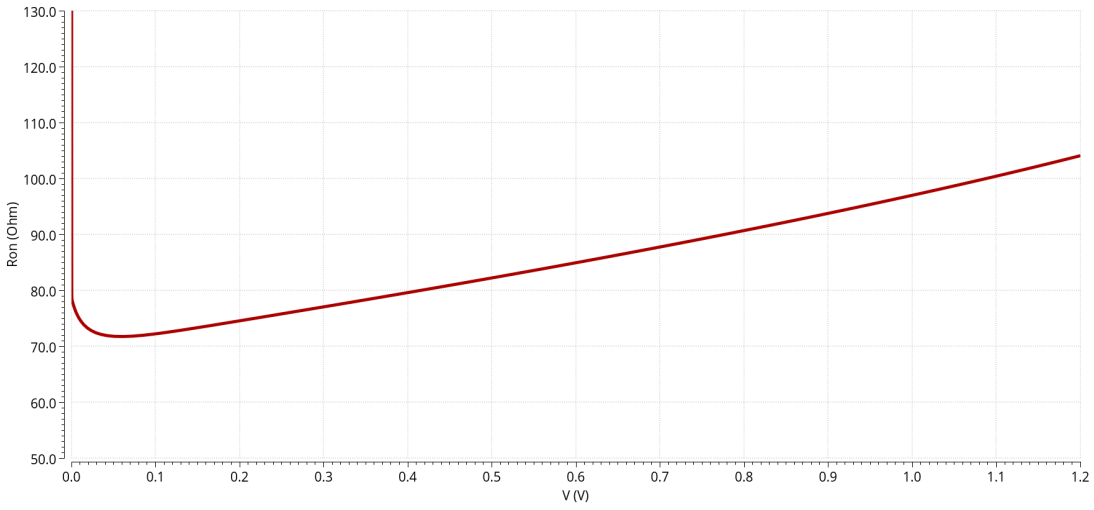

Figure 4.4 : Ron vs Vin of the sampling switch.

According to the simulation results shown in Figure 4.4, the switch resistance is significantly lower than the value calculated in Equation 4.3. In addition, Figure 4.4

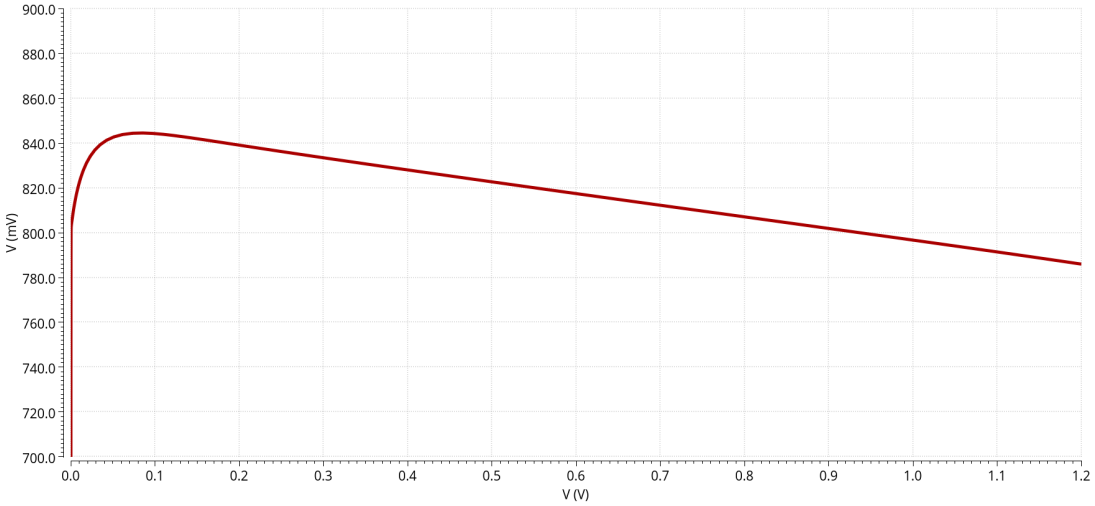

Figure 4.5 : VGS vs Vin of the sampling switch.

shows the variation in the resistance of the designed bootstrap switch with respect to the input voltage. As a result, the switch's linearity and the signal-dependent charge injection have been enhanced. However, as shown in Figure 4.5, it is impossible to eliminate variations in the resistance of the sampling switch with respect to the input due to the body effect and the variation in V_{GS} with respect to the input voltage.

4.1.2 Comparator

The comparator is another crucial part of the SAR ADC because its performance directly affects the static and dynamic performance of the ADC. Therefore, the comparator should be characterized precisely. For this reason, PSS and PNOISE analysis are utilized to measure the input-referred noise of the comparator. The result is depicted in Figure 4.6.

Noise is not correlated, hence noise power rather than noise voltage should be added. Then, the total integrated noise was calculated as

$$Total\ Integrated\ Noise\ = \sqrt{\int_{1}^{Fnyquist} (noise\ voltage)^2} = 120\mu V \qquad (4.4)$$

Dynamic offset simulation is the second simulation to be performed with the comparator. A slow ramp input is applied to the comparator inputs to measure the dynamic offset. The offset voltage is recorded during both descent and ascent of the ramp. The offset value of the comparator is determined by averaging the obtained

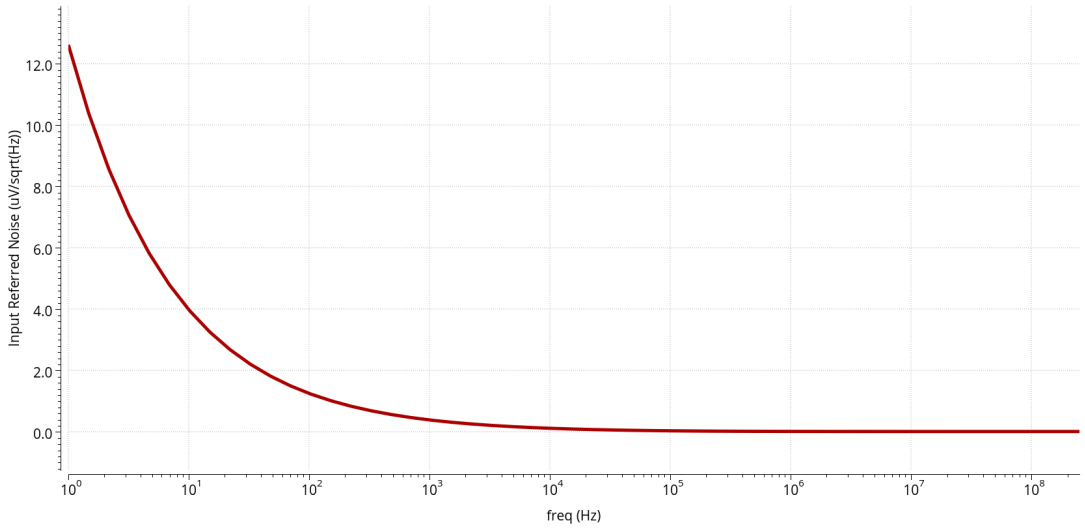

Figure 4.6 : Input referred noise of the comparator.

values. Figure 4.7 shows the comparator's transient waveform relative to the input, and the dynamic offset was measured as 300 μV when the ramp increased and decreased. The offset was identified as 0V. As our ramp step is 100 μV, we are unable to measure offset values less than 100 μV. Consequently, we should claim that our offset value is less than 100 μV.z.

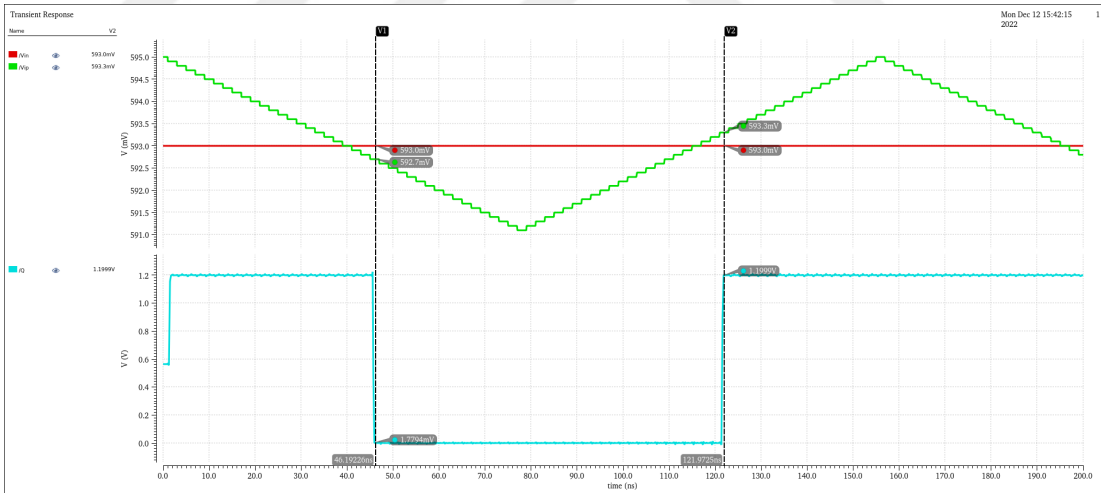

Figure 4.7 : Offset simulation of the comparator.

4.1.3 SAR ADC

Spectrum analysis of the SAR ADC was done to measure dynamic performance metrics such as ENOB, THD, SFDR, etc. For this purpose, sinusoidal inputs with different frequencies are applied. Synchronous, non-coherent sampling was utilized.

Synchronous sampling indicates that an even number of input signals and clock periods will be utilized for the fast Fourier transform (FFT) calculation. This will decrease spectral loss. Non-coherent sampling signifies that the input frequency and clock frequency are not connected harmonically. THD will be overestimated if the clock and input signal are harmonically related. Figure 4.8 shows the FFT plot for 24.7 MHz sinusoidal input, which is very close to the Nyquist frequency, 25 MHz.

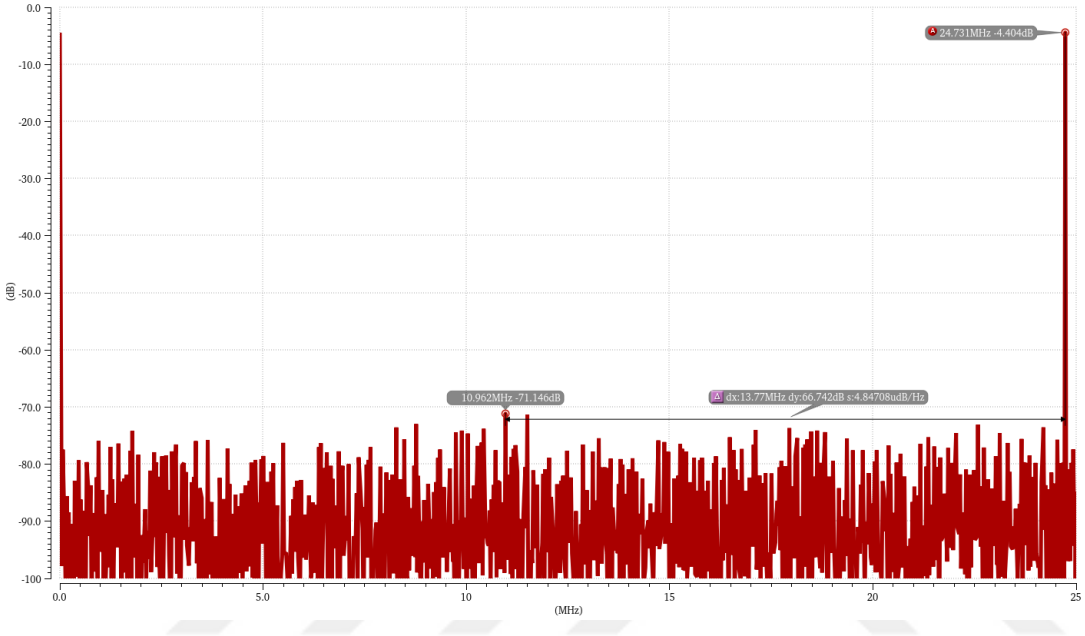

Figure 4.8 : FFT plot of the SAR ADC for 24.7 MHz input.

The simulation result for different input frequencies is listed in Table 4.1. Simulation results show that the designed ADC is very close to the ideal ADC.

Table 4.1 : FFT results for different input frequencies.

Input Frequency (MHz)	ENOB	THD (dB)	SFDR (dBc)
4.81	7.95	-63	66.76
13.94	7.96	-64.5	67.77
24.73	7.97	-66.1	67.35

4.2 Simulation Results of Flash Assisted SAR ADC

The same simulations as for the SAR ADC were also made for the 11-bit flash-assisted SAR ADC in order to measure performance metrics. The same input signals applied to the SAR ADC are also applied to the ADC. Figure 4.9 shows the FFT plot for 24.7

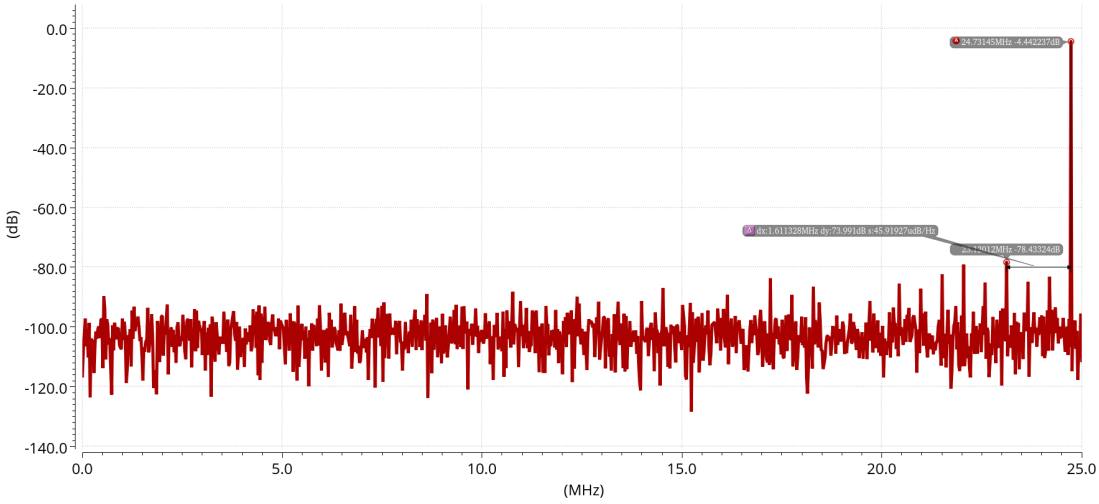

Figure 4.9 : FFT plot of the 24.7 MHz input.

MHz sinusoidal input, which is very close to the Nyquist frequency, 25 MHz. The simulation result for post-layout and schematic views for different input frequencies is listed in Tables 4.2 and 4.3, respectively. While schematic simulation results are close to ideal, post-layout simulation results are not as good. The reason for the decline in performance could be non-linearity in the DAC. Due to parasitic capacitance from extraction and capacitor mismatch, charge sharing equations deviate from the ideal.

Table 4.2 : Schematic FFT results for different input frequencies.

Input Frequency (MHz)	ENOB	THD (dB)	SFDR (dBc)
4.81	10.95	-83.1	86.2
13.94	10.95	-81	88.1
24.73	10.95	-80.9	87.1

Table 4.3 : Post-layout FFT results for different input frequencies.

Input Frequency (MHz)	ENOB	THD (dB)	SFDR (dBc)
4.81	10.28	-73.32	77.3
13.94	10.26	-71.23	74.6
24.73	10.26	-71	74

The total power consumption of the flash-assisted SAR ADC is equal to 2.02 mW. 735.1 μW is consumed by the SAR ADC. The residue amplifier consumes 526.6 μW, whereas the flash ADC consumes 755.5 μW. These results are summarized in the pie chart shown in Figure 4.10.

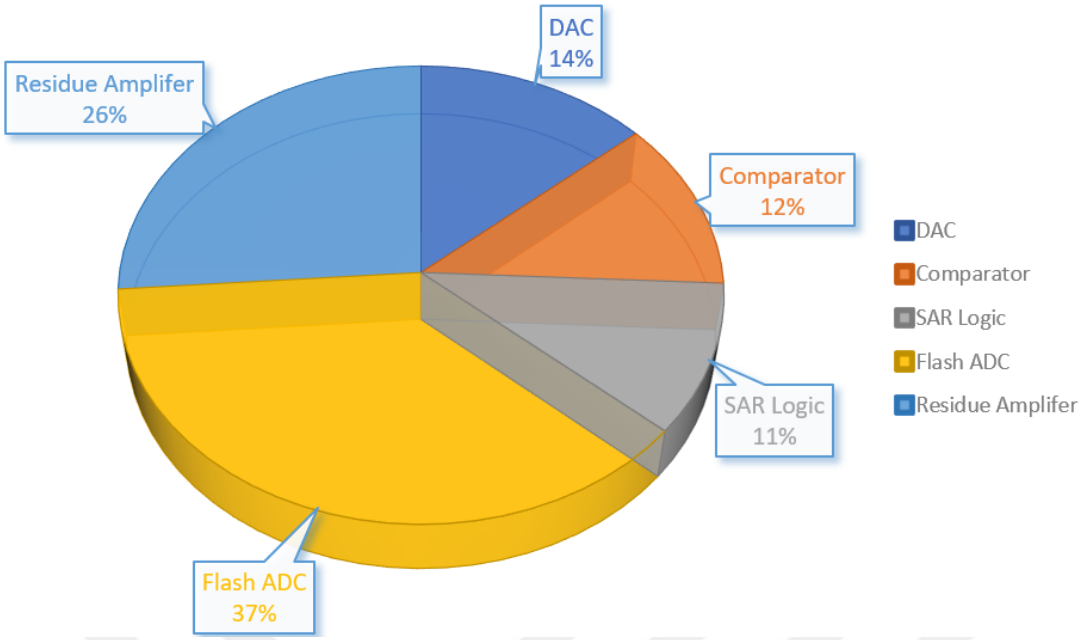

Figure 4.10 : Power consumption of the blocks.

Figure of merit (FOM) should be calculated in order to evaluate the efficiency of the design. There are two widely employed methods for calculating the FOM of the ADC in the literature: Walden FOM [20] and Schreier FOM [21]. The Walden FOM of this design was calculated as 32.95 fj/Conv-step by using Equation 4.5. On the other hand, the Schreier FOM of the design is calculated as 164.5 dB using Equation 4.6.

$$FOM_W = \frac{Power}{2^{ENOB} * F_s} \; [J/conv] \tag{4.5}$$

$$FOM_S = SNDR + 10 * log(\frac{Band\ Width}{Power}) \; [dB] \tag{4.6}$$

5. CONCLUSION AND FUTURE WORK

The SAR ADC is one of the most prevalent ADC architectures due to its excellent conversion efficiency. Technology scaling also improves the performance of the SAR ADC due to its mostly digital structure; hence, its popularity has increased over the past few years. However, DAC mismatches restrict the resolution of the SAR ADC. Thus, we propose a hybrid architecture to increase the SAR ADC's resolution without sacrificing speed. In this work, an 11-bit flash-assisted SAR ADC with a 50 MS/s rate was designed, implemented, and simulated in TSMC 65nm CMOS process technology. The design uses a 1.2 V power supply with a power consumption of 2.02 mW. The SNDR value obtained from the simulation result is 63.65 dB at Nyquist frequency. The layout occupies 0.0625 mm^2. Table 5.1 provides an overview of the outcomes of the design.

Table 5.1 : Summarized simulation result of the design

Parameter	Simulation Result
Sample Rate	50 MS/s
SNDR	63.65 dB
Power Supply	1.2V
Power Consumption	2.02mW
FOM	32.95 fj/conv-step
Layout Area	0.25mm x 0.25mm
Process	TSMC 65nm

In Table 5.2, the performance values of our design are compared to other designs in the literature that have similar resolution and speed. These values were obtained from simulation results.

Even though the performance of the converter is sufficient as seen in Table 5.2, it could be improved. Especially, after parasitic extraction performance of the converter decrease much more than expected. The reason for that could be mismatches in the DAC.

Table 5.2 : Comparison table of the design with other contemporary studies in the literature

Parameter	**[22]**	**[23]**	**[24]**	**[2]**	**This Work**
Architecture	SAR	Pipe, SAR	SDCT, BP	SAR, Flash	SAR, Flash
Technology[nm]	65	65	28	90	65
Resolution [bit]	10	10	12	15	11
Conversion Rate [MS/s]	50	40	100	85	50
SNDR[dB]	56.6	55.1	67.5	74.3	63.5
Power [mW]	0.82	1.21	13.4	0.65	2.02
Area[mm^2]	0.039	0.06	0.088	-	0.0625
FoM[fj/conv-step]	29.7	65	34.6	3.81	32.95

In order to improve the performance of the converter, a calibration circuit could be added to deal with the mismatch problem. Furthermore, asynchronous SAR logic could be utilized instead of synchronous SAR logic used in this design. Synchronous SAR converters utilize a high-speed clock to divide the conversion process into equally spaced time intervals. These converters require a greater clock frequency than the sample rate. For example, in this work, SAR ADC operates at 50 MS/s, but SAR logic operates at 500 MHz. Asynchronous SAR converters, on the other hand, do not require a high-speed clock. Instead, asynchronous logic initiates the comparison at each step. This enables the converter to function using a clock that has a low frequency. In addition to increasing the conversion rate, this also reduces the converter's power consumption and makes it more appropriate for low-power applications. In addition, the conversion rate could be enhanced by employing a technique that transforms two bits per cycle rather than one bit per cycle. After improving the performance of this design, it will be tapped out, and the results measured.

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APPENDICES

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