

LOW-POWER LOW-NOISE HIGHLY PROGRAMMABLE DIGITAL
ACCELEROMETER READOUT FOR HIGH PERFORMANCE MEMS
ACCELEROMETERS

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ACCELEROMETER READOUT FOR HIGH PERFORMANCE MEMS
ACCELEROMETERS**

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ABSTRACT

LOW-POWER LOW-NOISE HIGHLY PROGRAMMABLE DIGITAL ACCELEROMETER READOUT FOR HIGH PERFORMANCE MEMS ACCELEROMETERS

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This thesis presents a low-power low-noise mixed-signal CMOS readout integrated circuit for high performance MEMS capacitive accelerometers that can both operate in open-loop and closed-loop configurations, which is determined by the external electronics and the system. The system and circuit allow the adjustment of the loop dynamics to achieve low-noise and high order linearity for a very wide range of MEMS capacitive accelerometer sensors. In addition, the system allows the real-time input acceleration range selection in exchange with the lowest signal resolution. The integrated circuit provides highly programmable features for timing and biasing in addition with optional external timing signaling and biasing.

The CMOS integrated circuit consists of analog front-end circuit, programmable gain amplifier, Zoom Analog to Digital Converter (ADC) which is combination of Successive Approximation Register (SAR) ADC and Delta-Sigma modulator with auxiliary blocks digital controller, bias generator, and output serializer. The implementation of the readout circuit is done using a 0.35 μm high-voltage CMOS process. Integrated Circuit (IC) components are designed and simulated using Cadence and MATLAB environment to satisfy all the mixed signal system requirements for the readout system, including the detailed analysis of noise

performance and linearity with the associated simulation models that are constructed corresponding analytic equations.

The system performance simulations are conducted for a sample MEMS capacitive accelerometer sensor with specifications 3.5 pF rest capacitance, 5.4kHz resonant frequency, a quality factor of 9.6, and a $3\mu\text{g}/\sqrt{\text{Hz}}$ Brownian noise level. According to system level simulation results, the system with the CMOS integrated circuit achieves $3.5\mu\text{g}/\sqrt{\text{Hz}}$ Brownian noise level in $\pm 20\text{g}$ full scale range, which is the lowest noise level achieved at METU. The designed CMOS integrated circuit measures $4.3\text{mm} \times 2.25\text{mm}$, operates from a 3.3V supply voltage, and dissipates 4 mW.

Keywords: Mixed signal readout system, low noise IC, configurable loop accelerometer, zoom ADC, sigma-delta modulator.

ÖZ

YÜKSEK PERFORMANSLI MEMS İVMEÖLÇERLER İÇİN DÜŞÜK GÜÇ TÜKETİMLİ DÜŞÜK GÜRÜLTÜLÜ KAPSAMLI PROGRAMLANABİLİR OKUMA SİSTEMİ TASARIMI

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Bu tez, yüksek performanslı MEMS kapasitif ivmeölçerler için açık döngü ve kapalı döngü karışık yapılandırılabilir karışık sinyal okuma sistemi sunar. İlgili simülasyon modelleriyle birlikte gürültü performansının ve doğrusallığın ayrıntılı analizini gösterir. Her bileşen sistemi hakkında arka plan bilgisi sağlanır ve mümkün olan her yerde denklemler cinsinden ifade edilir. Sistem, düşük gürültü ve yüksek dereceli doğrusallık elde edilebilmesi için çok geniş bir MEMS kapasitif ivmeölçer sensörü aralığı için döngü dinamiği ayarlanabilecek şekilde tasarlanmıştır. Ayrıca sistem, en düşük sinyal çözünürlüğü karşılığında gerçek zamanlı giriş ivme aralığı seçimine izin verir. Tümüleşik devre bileşenleri, okuma sistemi için tüm karışık sinyal sistemi gereksinimlerini karşılamak için Cadence ve MATLAB ortamı kullanılarak tasarlanmış ve simüle edilmiştir. Tezin entegre kısmı, analog ön uç devresi, programlanabilir kazanç yükselticisi, SAR analog-sayısal çevirici ve Delta-Sigma modülatörünün yardımcı blokları ile birleşimi olan Zoom analog-sayısal çevirici, dijital kontrolör, öngerilim üretici ve çıkış serileştiriciden oluşmaktadır. Entegre devre, isteğe bağlı harici zamanlama sinyalleme ve öngerilim üretici için son derece programlanabilir özellikler sağlar. Okuma devresinin entegre devresi 0.35 μm CMOS yüksek voltaj prosesi kullanılarak tasarlanmıştır.

Sistem performans testleri, 3.5 pF hareketsiz kapasitansı, 5.41 kHz rezonans frekansı, 9.58 kalite faktörü ve 3.03 $\mu\text{g}/\sqrt{\text{Hz}}$ Brownian gürültü seviyesi spesifikasyonlarına sahip bir örnek MEMS kapasitif ivmeölçer sensörü için gerçekleştirilmiştir. Sistem simülasyon sonuçlarına göre, sistem ODTÜ MEMS Merkezi kapsamında elde edilen en düşük gürültü seviyesi olan 3.5 $\mu\text{g}/\sqrt{\text{Hz}}$ Brownian gürültü seviyesine ulaşmaktadır ve $\pm 20\text{g}$ tam ölçek aralığında çalışmaktadır. Tasarlanan elektronik, 3.3V besleme voltajından 4 mW güç tüketimi gerçekleştirir ve boyutları 4.3x2.25 mm olarak ölçülmüştür.

Anahtar Kelimeler: Karışık sinyal okuma sistemi, düşük gürültülü tümleşik devre, yapılandırılabilir döngü ivmeölçer, Zoom analog-sayısal çevirici, Sigma-Delta modülatörü.



To my family

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CHAPTER 1

INTRODUCTION

Humanity has interacted with many intelligent systems since the 21st century. The interactions are the main factor leading the consumer products. That is the number one reason advancements in the electronic field have escalated. More specifically, the devices are getting more intelligent than it has been. Being smart can be related to the ability to sense the environment more delicately. For example, intelligent systems must precisely perceive a physical reality to react accordingly. Smartphones sense the light level so that they can adjust the right level of illumination to protect the eyes of the user, and they sense the orientation so that they can change the rotation level according to the user. In addition, cars sense the collision so that they can apply rescue protocols to ensure the driver's safety in milliseconds. A computer is more intelligent because it can sense free fall and takes a disc into a power down configuration to protect necessary information on a disc. The list goes on since there are many examples in today's technology.

To specify further, movement sensing devices utilize information about rotational and linear movements. Rotational movements can be sensed using gyroscopes, and linear signals can be sensed using accelerometers. Both are solutions to more extensive systems for intelligent device applications such as biomedical applications, military applications, consumer products and resource extraction applications such as precise oil positioning using surface movements. Some of the requirements of those applications are small size, low cost, ease of use, low power, and high accuracy. Those requirements can be satisfied with the sensors produced by Micro-Electro-Mechanical Systems (MEMS) technology.

MEMS is a process technology that enables the production of small micro-level integrated devices or systems that combine mechanical and electrical components.

Integrated Circuit (IC) batch processing techniques utilize the fabrication of devices with a size range from a few micrometers to millimeters. Devices produced using MEMS technology are used for sensing, controlling, and actuating on a tiny (micro) scale and yielding results on a macro scale. MEMS has an interdisciplinary nature utilizing enhancements for a wide range of applications, including integrated circuit manufacturing, mechanical engineering, materials science, electronic engineering, chemistry and chemical engineering, optics, instrumentation, and packaging, as well as many other applications. Many diverging systems across automotive, medical, communication and defense applications carry traces of that technology [1].

The MEMS market is growing due to advantages such as miniaturized mechanical and electro-mechanical devices but also large-scale production with high performance, reliability, scalability, and low cost. MEMS technologies originated from Bell Labs in the late 1940s and early 1950s and transistor technology that Bell Labs pioneered. The semiconductor market grew to \$10 billion in 2011. The automotive industry demands mainly dominated the MEMS industry's early years. Then, smartphones shifted the domination to consumer-driven applications. Finally, the automotive sector keeping low-cost pressure took a much more influential role in consumer-focused markets like smartphones. Today, consumer cost models present spectacular performance, while at the same time, consumer products require greater and greater reliability [2] [3]. Finally, by 2021 MEMS market reached to \$12.1 billion boundary. As seen from Figure 1.1, provided by the annual report of Yole, linear and rotational sensors have a growing interest in the market with other MEMS products. In the following years, the total market forecast is expected to rise above 18 billion with a 7.2 percent Compound Annual Growth Rate (CAGR). Inside bubble chart, MEMS accelerometers and inertial combos are expected rise from 1.134B to 1.394B and from 1.503B to 2.127B levels, respectively. Note that, the research accounts for the effects of Covid-19 pandemic and beyond.

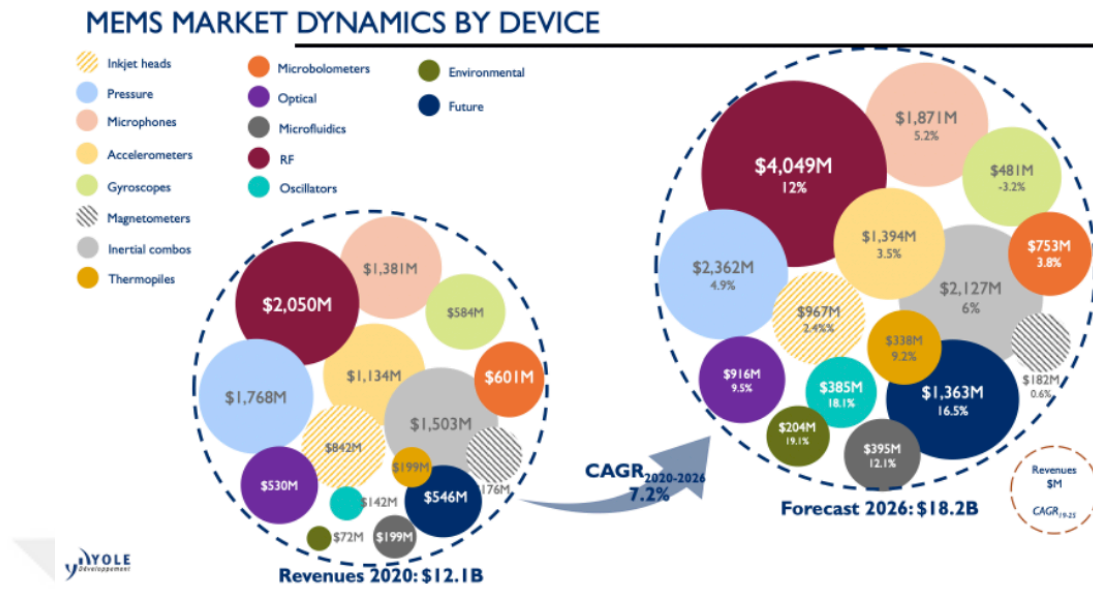


Figure 1.1: MEMS market forecast [4].

The growing expectation of the MEMS market also drives the semiconductor industry, which had the most significant jump in the late 1940s and 1950s.

So far, all MEMS sensors require an analog electronic interface to digitize the transduced data using the electronic domain. The fabrication of both Integrated Circuits (IC) and MEMS sensors are distinct wafer-level separate processes. That approach saves yield and fabrication cost of each batch, yielding flexibility and low cost [5] [6]. In addition, System in Package (SiP) solutions are getting more attention as chip size optimizations and packaging processes follow the trend. Therefore, industrial applications seek for on-chip solutions as electronic applications. Because, that way, mass production costs drastically reduce owing to limited number of discrete element usage and low cost of the recurring wafer-level production. Furthermore, fabrication houses offer enhanced characterized processes that allows extensive simulations enabling high performance designs.

There are special processes such as BICMOS, high voltage processes and isolated MOSFET processes give the designers flexibility to implement specialized circuitries. That way, wide range of applications can be targeted using different fabrication methods provided by manufacturers.

1.1 Classification of Accelerometer Sensing Mechanisms

MEMS accelerometers are classified into six types with respect to their sensing mechanisms:

1. Piezoelectric
2. Piezoresistive
3. Capacitive
4. Hall Effect
5. Magnetoresistive
6. Heat transfer

A piezoelectric material generates an electrical quantity resulting from mechanical stress. The reverse logic also holds for those materials as they are relaxed; they convert electrical charge to mechanical force. That is called the piezoelectric effect. Mechanical stress towards the acceleration direction originating from the instant acceleration simply constitutes the transducing from acceleration to an electrical charge. The same transducing method holds for piezoresistive sensors, but the electrical quantity is measured using the change in the resistance instead of the voltage difference.

Capacitive accelerometer sensors generally utilize a suspended structure with mechanical springs to anchor it on a surface to hold a reference to a relative acceleration motion. There are electrodes attached to suspended proof mass to create a capacitive quantity yielding a change during movement. Then the difference is sensed via a charge-sensitive structure.

Hall effect type of sensors focuses on a change in voltage quantity due to motion leading to magnetic field variation. On the other hand, magnetoresistive sensors include a material that responds to magnetic field change as the resistive property changes. Finally, heat transfer accelerometers construct a mechanical system that transfers the heat in a direction, and any change in the direction of the heat transfer

leads to positional differences in time. That way, the accelerometer senses the movement with a slow implementation.

Several methods are proposed as microstructures that require careful mechanical designs to obtain high-resolution results. As the scope of this thesis is high-performance sensors, it is more convenient to focus on microstructures.

1.2 Micro-Accelerometers and Readout Types

Several distinctive methods offer solutions to the electrical conversion of acceleration. Piezoelectric-based detection methods take advantage of the realization of a voltage difference between terminals of piezoelectric material. Piezoresistive sensors are very similar to piezoelectric sensors; instead, they change their resistive property according to stress applied to material due to acceleration. Then the corresponding change in electrical resistance is converted to voltage using a proper conditioning circuit interface. Wheatstone bridges (for full bridge) embedded within their top surfaces; sense acceleration-induced strain in these flexures shifts the outputs of the piezoresistive sensor [7]. The first micromachined and commercialized micro-accelerometers were the ones with piezoresistive sensors. They have a simple structure with process facilitation and readout circuitry. On the other hand, they have more considerable temperature drift and minor overall sensitivity compared to capacitive micromachined accelerometers. That is why a larger proof mass is preferred for those architectures [5].

Inertial accelerometers for inertial navigation systems had been widely constructed upon macro electro-mechanical accelerometers and quartz resonating accelerometers [8] [9]. Although macro electro-mechanical accelerometer sensors promise better performance specifications, they are expensive and fragile against environmental effects. Furthermore, quartz sensors have superior dynamic range but lack stability and shock tolerance during low g level measurement. Consequently, the demand for inertial navigation systems shifts towards capacitive MEMS accelerometer sensors.

Military applications require high performance navigation systems due to unreliable GPS signaling and harsh environmental effects leading to further investigation of capacitive MEMS accelerometers in the literature.

Table 1.1 demonstrates the classification of micro-accelerometers. The results of the table points out that capacitive accelerometers can be utilized to wide range of applications due to their endurance and high performance in low frequency measurements. Capacitive MEMS accelerometers can endure high g shocks up to 10^6 g range. Still, the optimal operation range is considered 0 to 200g for reading precise data with high dynamic range designs [10] [11].

Table 1.1: Table of application areas according to sensor types [10].

Application	Piezoelectric	Capacitive	Piezoresistive
Static acceleration		X	X
0 Hz – 1g Gravity, sensor orientation			
G-Force		X	X
0 Hz – <25g Rocket, centrifugal, aircraft			
Seismic	X		
<1 Hz – <1g Earthquake, waves, bridges			
Low frequency vibration	X	X	X
<5 Hz – <25g Human motion, robotics			
General vibration	X	X	
5 Hz to 500 Hz – <25g Electric motor, car suspension			
High frequency vibration	X		
>500 Hz – <25g Gear noise analysis, turbine monitoring			
General shock	X	X	X
>100 Hz – <200g General testing, shock absorber testing			
High impact shock	X	X	X
<250 Hz – >200g Drop testing			
Extreme shock			X
>1000 Hz – >2000g, High g-force <1000 Hz – <2000g Vehicle crash testing			

Recently, state-of-the-art MEMS accelerometer literature focuses on low-noise interface circuits and readout architectures to achieve navigation grade performance specifications. On the other hand, there are some drawbacks to those sensor systems. Varying gap capacitive type accelerometers introduce non-linearity to the procedure due to the non-linear nature of the sensor equations, which will be further investigated in the following sections. Other potential error sources of those systems can be defined as temperature drift, offset and wire bond (in frequency domain) effects. There are vastly many electronic interfaces or attachment methods dedicated to tackling those problems in order to mitigate random errors, such as [12] [13] [14] [15].

As MEMS capacitive accelerometers provide advantages explained above, the thesis focuses on the readout system of that type of sensor.

1.3 Classification of Readout Systems by Loop Strategy

Two loop strategies distinguish the accelerometer readout systems: open-loop and closed-loop. Both readout systems have some specific advantages and disadvantages over the other. This work allows both loop strategies. However, the design works in the open loop configuration during calibration and operates in the closed loop configuration for the reasons explained in the following sections.

1.3.1 Open Loop Readout Systems

Open loop readout systems do not introduce a mechanism or readout interface to complete the loop. In this kind of loop, differential capacitance difference between two electrodes is converted to electrical voltage difference. Then the signal is processed according to data conversion methods such as quantization or modulation for capacitive MEMS accelerometers. Any feedback system introduces noise to the system in some measure due to the nature of electronic circuits. Open loop systems

do not contain any kind of circuitry specialized for that, leading to lower noise readout performance in general.

Capacitive accelerometer sensors have non-linear characteristics due to nonlinear capacitive conversion of the proof mass deflection distance from the rest position. Since open loop systems do not have any feedback mechanism to limit the proof mass motion, they have more non-linearity spurs in the frequency domain than their closed-loop counterparts. Also, note that open loop architectures can be more prone to shock acceleration in a destructive way because there is no mechanism to soften the shock to prevent any harm to sensor fingers and legs. Finally, open loop systems have high bias instability and temperature drift due to large deflections, especially for sensors with a high Q-factor.

To conclude, open loop systems have more straightforward design complexity and low noise, but they are more nonlinear, shock prone, and have more bias instability with temperature drift.

1.3.2 Closed Loop Readout Systems

Closed loop systems have a feedback mechanism specialized for the readout system components, contrary to open loop systems. Feedback is applied with the electromechanical actuation force between the capacitive electrodes of the suspended structure for capacitive MEMS accelerometer sensors. The feedback force is instantiated differentially according to the polarity of the voltage read from the previous cycle. That way, proof mass can be mostly forced to be pinned at the origin where the readout is linear. Furthermore, closed-loop systems offer less temperature sensitivity, bias drift, and dependence on the sensor parameters if the loop filter is not specialized for the specific characteristic. Input range and dynamic range of standard delta-sigma readout system can be adjusted using configurable feedback voltage magnitude. On the other hand, a closed loop system design brings complexity within higher noise probability without meticulous optimization.

Closed loop designs can be investigated under two categories according to the type of signal fed back: analog and digital. Analog type loops introduce analog voltage feedback according to voltage values obtained from the transducer interface and loop filters operating in the analog domain. Analog loops are mostly uncomplicated in design since the analog architectures can be found in the literature with loop filters that fit best to the parameters of the accelerometer sensor. On the other hand, the analog signal must be quantized at the end by an ADC. That leads to a more complex and expensive system design. In addition, applying a direct analog voltage to the electrodes of the accelerometer sensors makes the system prone to nonlinearities stemming from the force feedback mechanism, which is inversely proportional to the deflection of proof mass from its origin.

The reasons stated above explain the urge to use a digital feedback structure. Digital feedback systems convert the signal to a digital pulse train. Then the signal is returned as a high or low signal providing a linear feedback structure when examined in the broader time interval. Finally, those systems are called electro-mechanical sigma-delta modulators [16].

1.4 Overview of Sigma-Delta Capacitive MEMS Accelerometer Readout

In 1990 W. Henrion et al. proposed to use a capacitive MEMS accelerometer as an integrating element for a sigma-delta loop circuit to obtain digital data instead of analog output [17]. According to the testing results presented in this paper, performance metrics were obtained as $10\mu\text{g}/\sqrt{\text{Hz}}$ noise in $\pm 0.1\text{g}$ range utilizing a sensor with a high Q factor and high sensitivity. T. Smith et al. published a paper that suggests adding another electronic integrator to shape the noise further. According to the results that were presented in the article, the work achieves $1\mu\text{g}/\sqrt{\text{Hz}}$ noise floor performance for $\pm 1\text{g}$ with $10\mu\text{g}$ offset drift and 1% nonlinearity [18]. B. E. Boser has worked on delta-sigma modulators as ADC (1988) and sensor readout systems. In 1995, B. E. Boser proposed an architecture utilizing a lead compensator to provide stable operation for the system achieving $1.6\text{mg}/\sqrt{\text{Hz}}$

noise for $\pm 5g$ full-scale range with a monolithic sensor [19]. Carnegie Mellon University reported a monolithic sensor with four distinct sense capacitors in differential-difference configuration with chopping stabilization circuitry achieving $50\mu g/\sqrt{Hz}$ acceleration noise floor in $\pm 6g$ range in 2004 [20]. In 2005, Jose de la Rosa demonstrated a chopper stabilized 2-1 cascade sigma-delta modulator 113.8dB within 20-kHz bandwidth [21]. The paper presents a detailed analysis of delta-sigma modulators with the best optimization according to the figure of merit in that time with the configuration given in Figure 1.2.

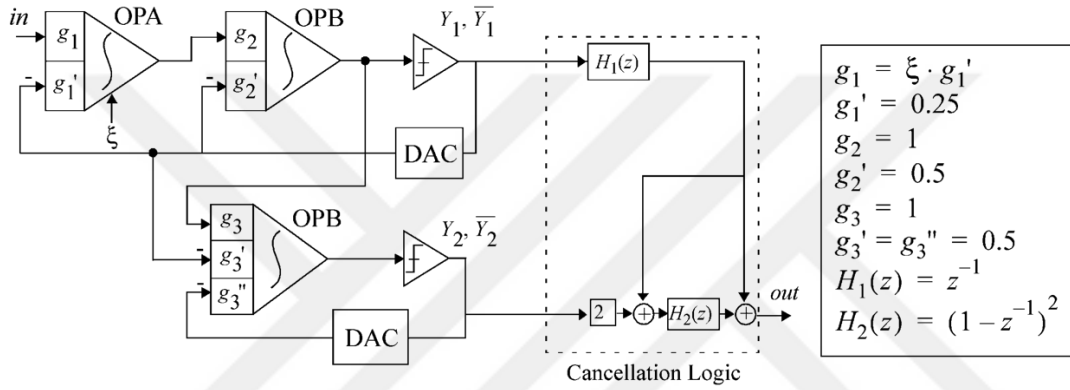


Figure 1.2: Cascade 2-1 configuration implemented by Jose de la Rosa et. al. [21].

In 2006, H. Kulah et al. published a significant article examining the noise sources of the second-order electromechanical delta-sigma modulated accelerometer [22]. The system in this paper achieves $10\mu g/\sqrt{Hz}$ with a 120dB dynamic range. In 2007, Abdolvand et al. fabricated the first ng accelerometer sensor with the reported resolution of $231ng/\sqrt{Hz}$ in the $\pm 0.1g$ range [23]. Sub- μg noise performance was obtained using a thick silicon-on-insulator substrate and keeping the total thickness of the sensor of the handle layer attached to the top layer proof mass as depicted in Figure 1.3. The main focus of that paper is decreasing the Brownian noise of the sensor by increasing the proof mass.

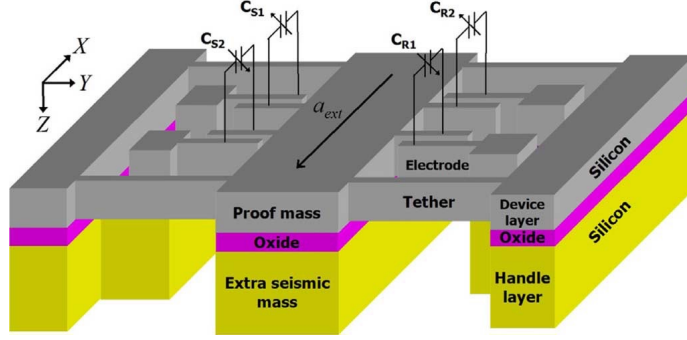


Figure 1.3: SOI accelerometer with sub- μg resolution reported by R. Abdolvand et. al. [23].

In 2011, U. Sönmez designed an accelerometer system with a $6\mu\text{g}/\sqrt{\text{Hz}}$ noise floor in a $\pm 15\text{g}$ full-scale range utilizing a fourth-order unconstrained delta-sigma modulator given in Figure 1.4 [24].

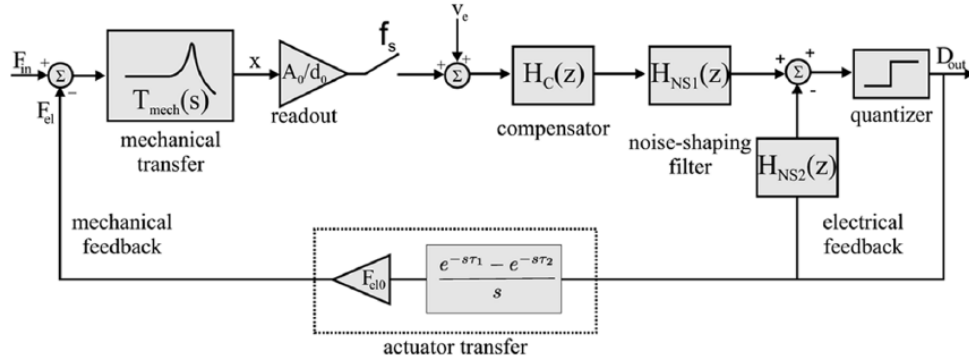


Figure 1.4: Model of the unconstrained mixed-feedback high order EM $\Sigma\Delta$ modulator proposed by Raman et. al. [25].

Raman et al. examined the loop in the z -domain and have critical simplification for designing an unconstrained delta-sigma modulator design by optimizing the noise shaping loop filters according to accelerometer sensor parameters.

Y. Dong et al. proposed a 5th order mixed-signal analog-digital architecture featuring early quantization with multi-bit ADC as shown in Figure 1.5. That system achieves a 120dB dynamic range in 100 Hz bandwidth [26]. In 2011, M. Pastre et al. reported another mixed signal delta-sigma loop with 7-bit flash ADC as multi-bit ADC and

high voltage interface. According to results in that paper, $7.1 \mu\text{g}/\sqrt{\text{Hz}}$ noise floor is achieved in $\pm 11.7\text{g}$ full scale range [27].

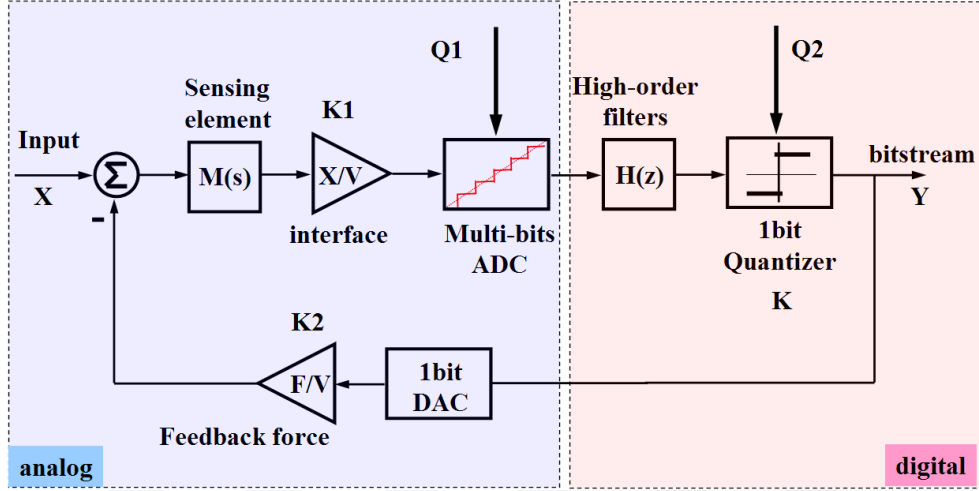


Figure 1.5: Mixed-signal analog-digital architecture implemented by Colybris [26].

In 2013, S. Incedere implemented a PI controller with 2nd order delta-sigma modulator to increase the order of the noise shaping for an accelerometer with a low Q factor provided by the METU MEMS center [28]. That work achieves better linearity due to the PI controller and more control over the loop compared with the unconstrained delta-sigma loop due to programmable loop filters.

In 2016, Y. Chu et al. introduced a readout system with the novelty of charge pump feedback for interface circuitry in order to adjust high voltage feedback digitally. The article reports a $30 \mu\text{g}/\sqrt{\text{Hz}}$ noise floor, concluding that the feedback interface should be carefully designed due to noise concerns [29].

In 2018, F. Chen et al. implemented a mixed signal system using a 12-bit quantizer before the digital part consisting of a phase compensator as depicted in Figure 1.6. The article presents a significant analysis of the quantizer performance limitation modules implemented before the FPGA unit [30].

In 2020, D. Chen published a paper demonstrating the measurement and calibration of the parasitic mismatch in MEMS accelerometer based on a harmonic distortion self-test. The article proposes several calibration methods to eliminate 2nd order

harmonic such as embedding calibration capacitance and digital self-test excitation [31].

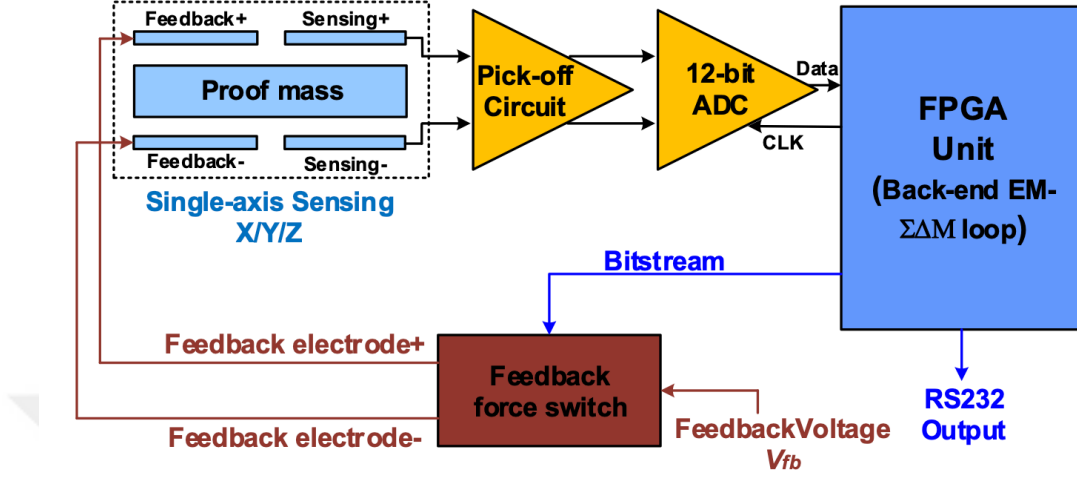


Figure 1.6: Mixed signal system reported from F. Chen et. al. [30].

To sum up, according to papers published between 1990-2005, delta-sigma readout systems were strongly dependent on the accelerometer parameters, but that does not mean that the performance metrics of those systems are insufficient. In the following years, the literature decayed to more complex loop analysis and loop filters to increase noise shaping order yielding lower in-band noise in exchange for stability. Then, the modern systems were designed to offer higher design optimization flexibility for noise-shaping filters, loop filters and electronic parameters. In addition, the primary trend for the electronic literature is shifting toward IoT and battery-powered portable designs leading to low-power designs. Therefore, most of the complexity stems from power optimization and robustness of the readout system independent of MEMS accelerometer sensor parameters and PVT variations.

1.5 Research Objectives and Thesis Organization

The primary purpose of that work is to demonstrate a highly programmable architecture for a wide range of MEMS capacitive accelerometer sensors and

applications. While implementing such a design, performance parameters shall not be degraded. The objectives of the work can be listed as follows:

1. Design and implementation of a low-noise pick-off circuitry that is suitable for both closed loop and open loop readout system architectures. The block should not introduce any unpredictable errors to the system.
2. Implementation of a low-power PGA (Programmable Gain Amplifier) with a large output swing behaving as a sample and hold buffer for an almost 6 pF capacitive load.
3. Designing a low-power 5-bit SAR ADC for the Zoom ADC Quantization stage of the system with a dynamic comparator with a controllable voltage reference range.
4. Quantization noise due to the 5-bit SAR ADC of the system should be further shaped with a low power and low noise delta-sigma modulator inside Integrated Circuit (IC).
5. Total readout noise and Zoom ADC quantization noise should be sufficiently shaped that the total noise of the system is dominated by the Brownian noise of the accelerometer sensor.
6. The input range of the readout system should be dynamically adjustable from the digital part of the design.
7. The electronic design shall be verified using comprehensive simulations for optimized performance parameters.
8. MATLAB-Simulink sample model shall be constructed and used for the demonstration of the stable operation of the system.

The thesis organization for the following parts and the contents of the chapters are given as follows.

Chapter 2 makes an introduction to the theory behind the delta-sigma modulators. After explaining the fundamentals of delta-sigma modulators, it gives the basics of

MEMS accelerometer sensors. Finally, the complete loop is examined as a mixed signal electro-mechanical sigma modulator.

Chapter 3 initially introduces the loop analysis of an accelerometer readout system. The constraints that are leading to design limitations are identified. Loop filter implementation and its analysis based on linearity and noise are investigated. Detailed stability analysis results are presented.

Chapter 4 presents the implementation of the system based on the theory and system analysis given in previous chapters. ROIC design is analyzed and presented with simulations verifying the requirements identified in Chapter 3. Zoom ADC concept is provided to clarify the optimization of the design.

Chapter 5 concludes the design with a comparison table and implemented related works. Finally, future work routes a pathway to a better design.



CHAPTER 2

FUNDAMENTALS OF ELECTRO-MECHANICAL $\Delta\Sigma$ MODULATORS

This chapter presents the theory and analysis of electro-mechanical $\Delta\Sigma$ modulators. Initially, concepts such as oversampling and data conversion principles are given in Section 2.1. The idea behind the delta-sigma modulation is examined in Section 2.2. Section 2.3 mentions the properties of MEMS accelerometer parameters and their properties with the basic electro-mechanical $\Delta\Sigma$ modulator demonstration. Finally, Section 2.4 gives a brief summary of the chapter.

2.1 Principles of Analog to Digital Conversion

In the electronics area, two significant domains describe the type of signal in quantity measurement, which is called analog and digital. Analog signals are quantified using voltages on the nodes or currents flowing through the nodes to represent a quantitative value of any information. Digital systems quantify the data using bits to encode any information with a resolution up to bit depths to describe the data. Analog signals are continuous in time and amplitude, whereas digital signals are discrete in time and amplitude. Conversion between both electronic signal domains is done via Analog to Digital Converters (ADC) and Digital to Analog Converters (DAC). The accelerometer system consists of both types of signals. The focus of the system is detecting the acceleration as an analog signal and converting that information to digital bit representation. That is why the theory of analog to digital conversion is given for the following parts of the section.

A general block diagram demonstrating the operation is depicted in Figure 2.1. At the beginning of the conversion, the analog input signal named $x_a(t)$ goes through an anti-aliasing filter which is also a low-pass filter to avoid any folding effect referring

as spurs or white noise to in-band ($f < BW$). Then S/H module samples the signal at a frequency rate of f_s resulting with a Discrete Time (DT) signal $x_s(n) = x(nT_s)$ where $T_s = 1/f_s$. Finally, DT signal $x_s(n)$ is quantized by an N-bit quantizer module which has discrete digital bit levels with a discrete 2^N level mapping function that covers the input range yielding a digital output of $y(n)$.

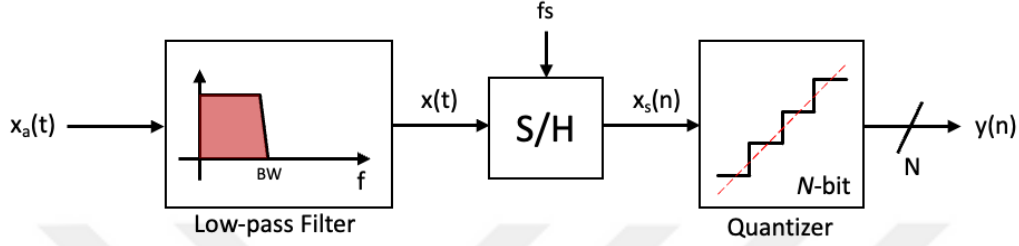


Figure 2.1: General block diagram of a Nyquist analog to digital converter.

2.1.1 Sampling

The sampling process simply completes continuous time to discrete time conversion of the incoming signal establishing a limit on the bandwidth of the continuous time signal. Theory can be easily explained using the Dirac delta train as given in Equation 2.1. The signal $x(t)$ is simply multiplied with the periodic impulse train with period T_s and converted to the signal represented with $x_s(n)$ before the quantization step.

$$x_s(t) = x(t) \sum_{n=-\infty}^{\infty} \delta(t - nT_s) = \sum_{n=-\infty}^{\infty} x(nT_s) \delta(t - nT_s) \quad (2.1)$$

Another way of representing the signals mathematically is using the Fourier transform, which is done by convolving the input signal $x(t)$ with the pulse train in the frequency domain. Convolution of a signal and impulse train in the frequency domain yields a periodic version of the same signal in the Fourier domain, as depicted in Figure 2.2.

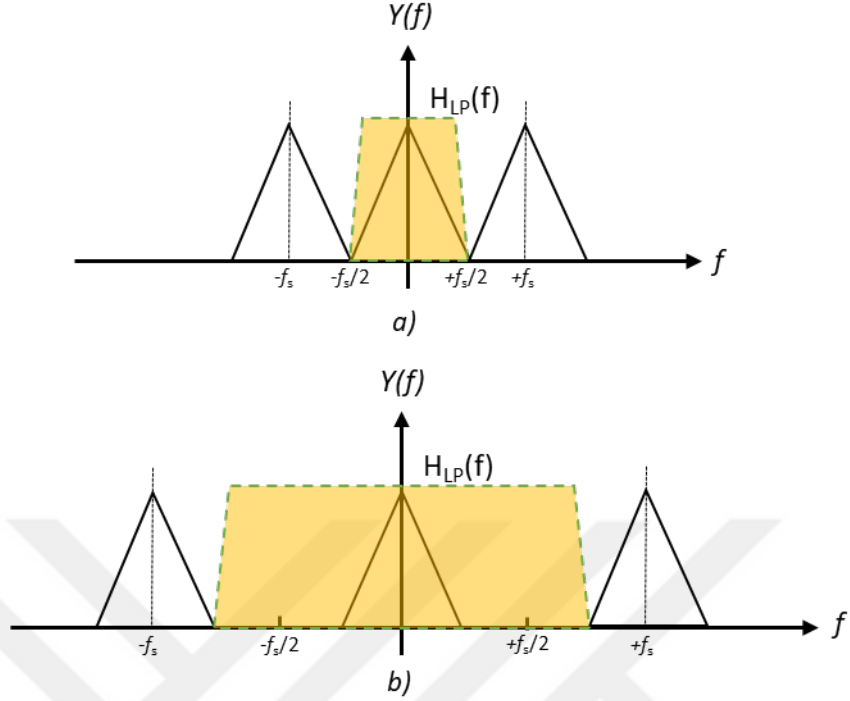


Figure 2.2: Low-pass filters for a) Nyquist-rate ADC and b) oversampling ADC behaviors.

Equation 2.2 shows the resulting operation in the Fourier domain.

$$\begin{aligned}
 \mathcal{F}\{x_s(t)\} &= X(f) * \mathcal{F}\left\{\sum_{k=-\infty}^{\infty} \delta(t - kT_s)\right\} \\
 &= X(f) * \left(\frac{1}{T_s} \sum_{n=-\infty}^{\infty} \delta(f - nf_s)\right) = \frac{1}{T_s} \sum_{n=-\infty}^{\infty} X(f - nf_s)
 \end{aligned} \tag{2.2}$$

It is obvious that from Figure 2.2, the sampling frequency must be chosen as $f_s < 2B$ to avoid aliasing since the shifted copies of the input signal might fold to in-band as noise or spurs. That is why the Nyquist rate is determined as $f_{s,min} = 2B$. Therefore, $f_s > f_{s,min}$ is called oversampling. The definition to describe scale of sampling speed concerning signal bandwidth is defined using the term OSR (Oversampling Ratio), which is given with Equation 2.3.

$$OSR = \frac{f_s}{2BW} \quad (2.3)$$

The design of a low-pass filter gets harder for lower frequency cut-off requirements, so the realization of an ADC with a higher OSR value relaxes the performance requirements of a low-pass filter to be implemented as an anti-aliasing filter. There is another benefit of designing for high OSR value, and it is provided in the following section.

2.1.2 Quantization

Limitation on the performance of an ideal ADC stems from the process called quantization since continuous to discrete transformation of a signal's amplitude generates an error referred to as quantization error. For an ideal ADC, mapping of the amplitude of any signal within the full-scale input range defined as $[-X_{FS}/2, +X_{FS}/2]$ is rounded to one of the corresponding 2^N digitally encoded levels. For a uniform quantizer, the quantization step is given as in Equation 2.4, where Y_{FS} is the full-scale output range.

$$x_s(t) = \sum_{n=-\infty}^{\infty} x(nT_s)\delta(t - nT_s), \Delta = \frac{Y_{FS}}{2^N - 1} \quad (2.4)$$

Figure 2.3 demonstrates the basic idea behind the quantization block with proper modelling of its error source. For a single-bit quantizer, k_q can be arbitrarily chosen. On the other hand, k_q should be appropriately selected to map the input signal according to the quantization scale to avoid overloading problems.

Quantization error is systematically dependent on the input signal $q(n)$. However, assuming $q(n)$ is random in the range $[-\Delta/2, +\Delta/2]$, the output $e(n)$ is also uncorrelated to previous samples of the input signal. Therefore, quantization error can be

described as a uniform probability distributed random process mapped in the range $[-\Delta/2, +\Delta/2]$, as depicted in Figure 2.3c. Quantization error power can be computed as given in Equation 2.5.

$$e^2 = \sigma_e^2 = \int_{-\infty}^{\infty} e^2 PDF(e) de = \frac{1}{\Delta} \int_{-\Delta/2}^{+\Delta/2} e^2 de = \frac{\Delta^2}{12} \quad (2.5)$$

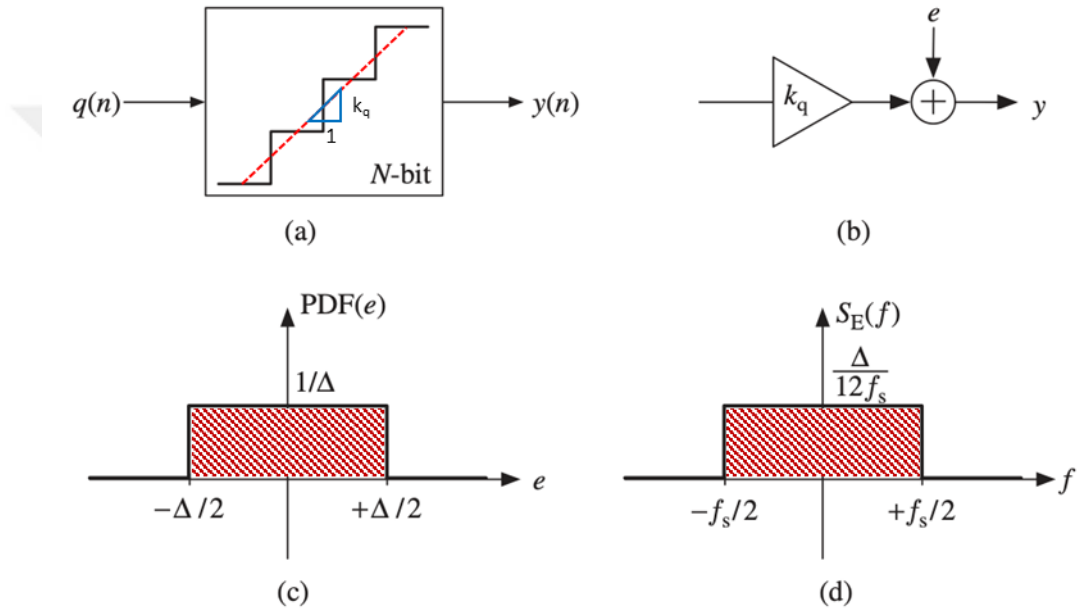


Figure 2.3: Quantization noise model: a) general quantizer module, b) linear quantizer model, c) probability density function (PDF), and d) power spectral density (PSD).

Note that quantization error is accepted as white noise, which yields the resulting spectral uniform distributed signal in the frequency range $[-f_s/2, +f_s/2]$. Therefore, the equivalent power spectral density (PSD) of the quantization error in that range can be found by equating the white noise distribution of the total quantization noise found in Equation 2.5 in the expression provided in Equation 2.6.

$$e^2 = \int_{-\infty}^{+\infty} S_E(f) df = S_E \int_{-f_s/2}^{+f_s/2} df = \frac{\Delta^2}{12} \quad (2.6)$$

Finally, the resulting PSD of the quantization error as the white noise is calculated in Equation 2.7.

$$S_E = \frac{e^2}{f_s} = \frac{\Delta^2}{12f_s} \quad (2.7)$$

Regarding the expressions obtained with the assumptions above, the performance of ideal ADCs can be easily assessed. Nyquist ADC quantization noise power is distributed inside the signal band yielding mapping of all quantization noise at the output, as illustrated in Figure 2.4a. However, an oversampled signal, $f_s > 2BW$, has less spectral quantization error mapped into the signal band, as depicted in Figure 2.4b.

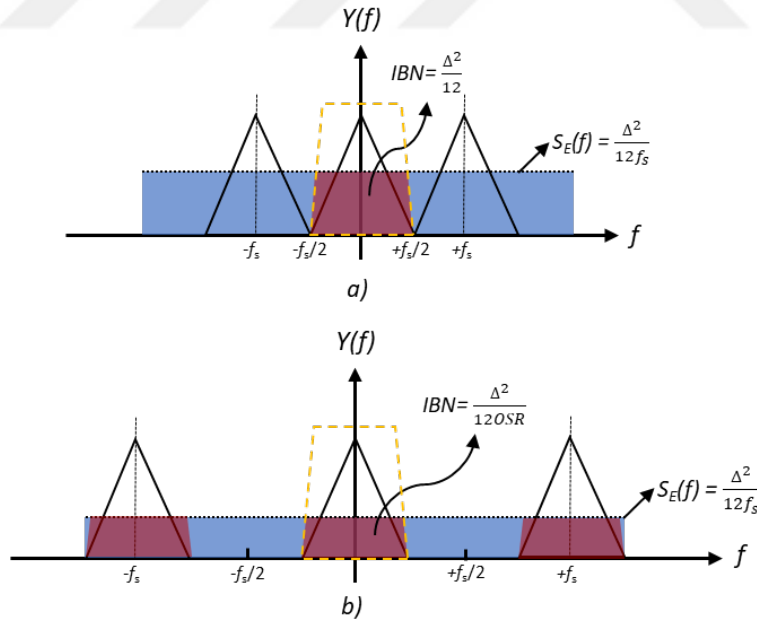


Figure 2.4: Spectral distribution of quantization noise for a) Nyquist ADCs, and b) oversampling ADCs.

In-band noise power that results from the quantization block for an ideal oversampling ADC can be calculated as in Equation 2.8, leading to the inverse proportion with the OSR.

$$IBN = \int_{-BW}^{+BW} S_E(f) df = \int_{-BW}^{+BW} \frac{\Delta^2}{12f_s} df = \frac{\Delta^2}{12OSR} \quad (2.8)$$

Output signal power can be approximated as the multiplication of 2^N and maximum non-overloading region with half of the quantization step as approximated in [32]. Therefore, an ideal oversampling ADC's Dynamic Range (DR) is expressed as in Equation 2.9, yielding a 3dB increase per doubling sampling rate (1 bit per 4 times).

$$DR(dB) \cong 6.02N + 1.76 + 10\log_{10}(OSR) \quad (2.9)$$

2.2 Delta Sigma Modulators

In this section, delta-sigma modulation concepts are introduced. Initially, the topology of a standard delta-sigma modulation is given in general. Then noise shaping concept is explained to understand the loop strategy of delta-sigma modulators. Finally, digital demodulation and the theoretical background of decimation are analyzed.

2.2.1 Topology

Different from the other ADC topologies, delta-sigma ADCs have a closed loop operation for the sake of control of the quantization error. Figure 2.5 simply demonstrates the general functional block diagram of a delta-sigma modulator which

consists of an anti-aliasing filter similar to the standard ADCs, noise shaping filter and digital demodulator module.

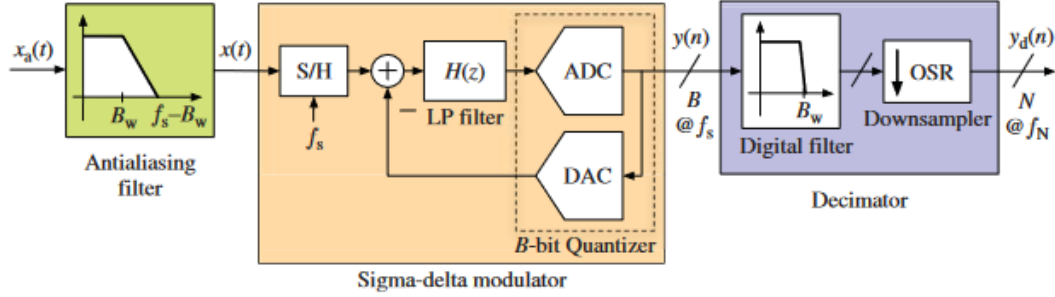


Figure 2.5: General functional block diagram of a delta-sigma ADC in [33].

An anti-aliasing filter (AAF) limits the bandwidth of the sampling signal before sampling operation to prevent the input signal from encountering aliasing or any noise folding effect. AAF filter design is relaxed as oversampling increases, as explained in Section 2.1.1. The noise shaping module and decimator module are described in Section 2.2.2 and Section 2.2.3.

2.2.2 Noise Shaping

Oversampling itself is an effective way to improve precision. Still, it is insufficient to obtain an accuracy up to 20 bits without consuming sources such as power and introducing further complexities to circuit implementation. Therefore, delta-sigma modulators include another method to further limit the in-band noise without using too much source, and it is called noise shaping. The noise shaping concept introduces a discrete time loop strategy to separate the transfer functions of input and the quantization error noise. That can be done by shaping spectral characteristics of input and quantization noise using discrete time filters such as integrators and differentiators.

Output quantization error is shaped in such a way that ascending noise signal magnitude in higher frequencies means less quantization noise power referred to as in-band noise. Conceptually, the operation is performed by subtracting the input

signal from the quantized signal to obtain an error signal to be shaped. Then error signal denoted as $e(n)$ is shaped using Noise Transfer Function (NTF), as depicted in Figure 2.6a.

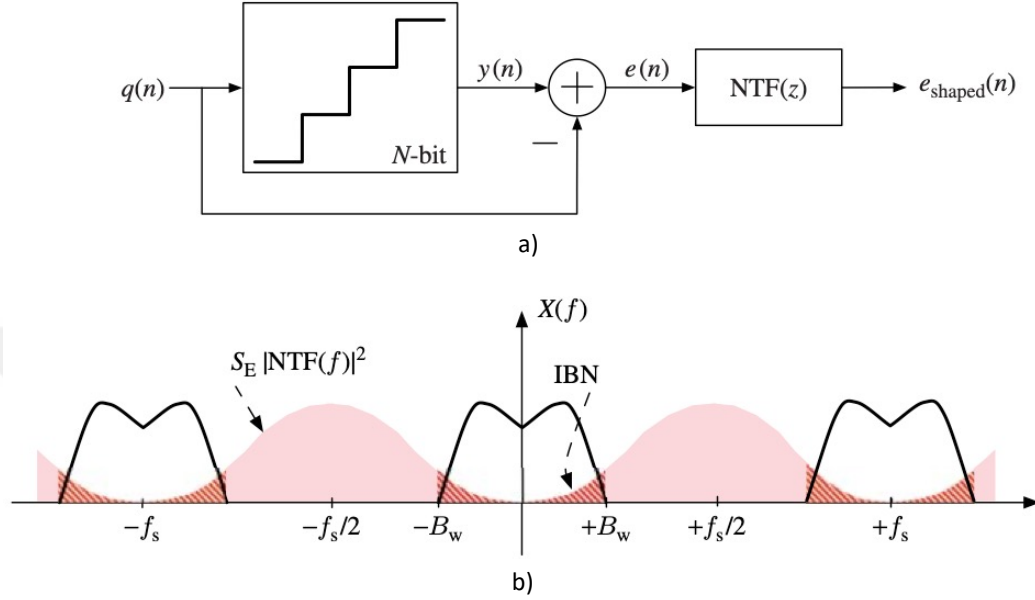


Figure 2.6: Noise shaping: a) functional block diagram b) Spectral distribution of quantization noise power [33].

The noise transfer function is simply a high-pass filter which can be implemented as a differentiator in the discrete-time domain as expressed in Equation 2.10:

$$NTF(z) = (1 - z^{-1})^L \quad (2.10)$$

where L represents the order of the differentiator high-pass filter; therefore, the resulting noise transfer function can be calculated using bilinear transform where

$z = \frac{1 + \frac{sT}{2}}{1 - \frac{sT}{2}}$. For an ideal differentiator, the magnitude of the noise transfer function is

given in Equation 2.11. Assuming first-order calculation of Taylor Series expanded

operations $e^{sT} = 1 + sT + \frac{(sT)^2}{2!} + \frac{(sT)^3}{3!} + \dots$ and $e^{-sT} = 1 - sT + \frac{(sT)^2}{2!} - \frac{(sT)^3}{3!} + \dots$

simplifies the Equation 2.11 eventually.

$$|NTF(s)| = \left[\frac{-sT}{1 - \frac{sT}{2}} \right]^L = \left[\frac{1 + e^{sT}}{e^{-sT/2}} \right]^L = \left[-e^{sT} \left(e^{\frac{sT}{2}} - e^{-\frac{sT}{2}} \right) \right]^L \quad (2.11)$$

Finally, by inserting $e^{sT} = e^{j2\pi f/f_s}$, Equation 2.12 can be obtained in the frequency domain where f_s is the sampling frequency of the sampling system.

$$\begin{aligned} |NTF(f)| &= \left| -2j \sin\left(\frac{\pi f}{f_s}\right) e^{\frac{j2\pi f}{f_s}} \right|^L \\ &= \left| 2 \sin\left(\frac{\pi f}{f_s}\right) e^{j\left(\frac{2\pi f}{f_s} - \frac{\pi}{2}\right)} \right|^L = 2 \left| \sin\left(\frac{\pi f}{f_s}\right) \right|^L \end{aligned} \quad (2.12)$$

By approximating the transfer function of an L^{th} order ideal noise shaping transfer function, the in-band noise is calculated in Equation 2.13.

$$\begin{aligned} IBN &= \int_{-BW}^{+BW} S_E(f) |NTF(f)|^2 df = \int_{-BW}^{+BW} \frac{\Delta^2}{12f_s} |4 \sin(\pi f/f_s)|^2 df \\ &\cong \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}} \end{aligned} \quad (2.13)$$

Note that, regarding Equation 2.12, the noise shaping technique is used combined with the oversampling method. For a general idea in terms of dynamic range (DR), an approximation is expressed in Equation 2.14.

$$DR(\text{dB}) \cong 6.02N + 1.76 + 10 \log_{10} \left| \frac{2L+1}{\pi^{2L}} \right| + (2L+1) \log_{10}(OSR) \quad (2.14)$$

The primary illustration of the delta-sigma modulator loop is provided in Figure 2.7, which consists of a loop filter $H(z)$ and an N-bit quantizer. To understand the general idea, assume $H(z)$ has a high gain in the in-band and very low gain in the out-of-band. Considering the negative feedback loop, input signal $x(n)$ and output signal $y(n)$ will coincide inside the high gain region, which is in-band, whereas $x(n) - y(n)$ will shift to the out-of-band zone.

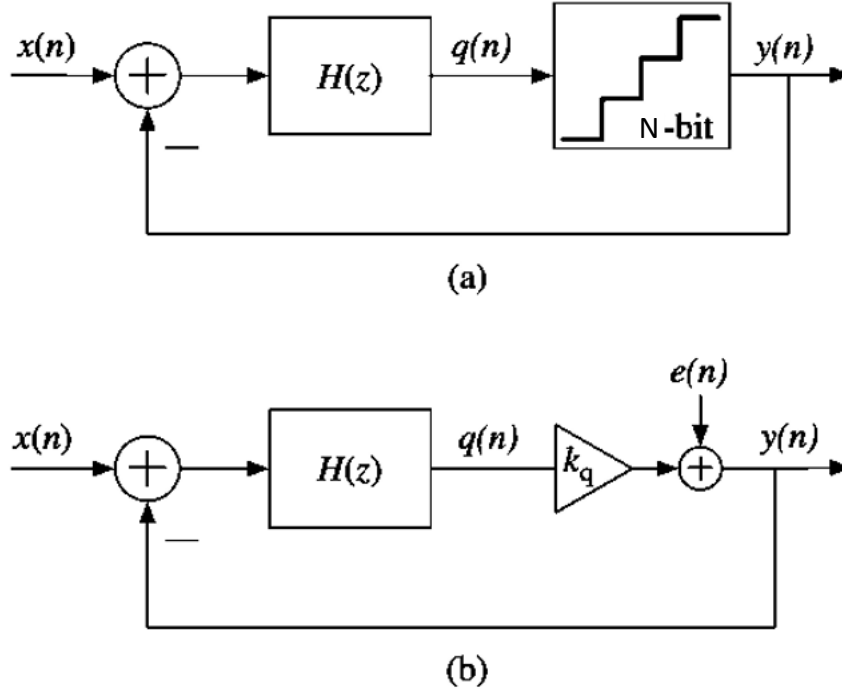


Figure 2.7: Functional block diagram of noise shaping operation: a) general and b) linear.

Assuming that the N-bit quantizer has a uniform step size over the full-scale range, most error signals will be shaped through the high frequencies. The z-domain expression of the noise-shaped output is given to further clarify the operation in Equation 2.15:

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \quad (2.15)$$

where STF and NTF are the corresponding signal and noise transfer functions elaborated in Equation 2.16 according to notations illustrated in Figure 2.7.

$$STF(z) = \frac{k_q H(z)}{1 + k_q H(z)}, NTF(z) = \frac{1}{1 + k_q H(z)} \quad (2.16)$$

Low pass filter implementation of $H(z)$ ideally performs the desired noise shaping operation. In the z -domain, that operation can be done using an ideal integrator, which is denoted as $ITF(z) = \frac{z^{-1}}{1-z^{-1}}$. Therefore, the final expression for a first order delta-sigma modulator output is given in Equation 2.17.

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \quad (2.17)$$

2.2.3 Decimation

Up to this point, noise shaping concepts of delta-sigma modulators are elaborated. The decimation operation enables the transformation of a lower resolution data into a high-resolution multi-bit digital value.

As expressed in Section 2.2.1, the digital bit stream from the delta-sigma modulator has meaningful data at lower frequencies for the case of low pass delta-sigma modulators. On the other hand, the spectral distribution of quantization noise is shaped mainly at higher frequencies. A low-pass filter should be implemented to extract the necessary information decoded inside low frequency. For this operation, digital Finite Impulse Response (FIR) filters are generally implemented because they are more stable than Infinite Impulse Response (IIR) filters. Furthermore, sinc behavior in the time domain yields a very sharp rectangular filter in frequency response. That is why ideally, those filters are sometimes called sinc filters. Note that the design of an ideal sinc filter consumes too much resource in hardware implementation. Therefore, a high-performance digital low pass filter should be designed considering the tradeoffs between the rejection of ripples in the alias band, shortening the transition band and the number of filter taps, as depicted in Figure 2.8.

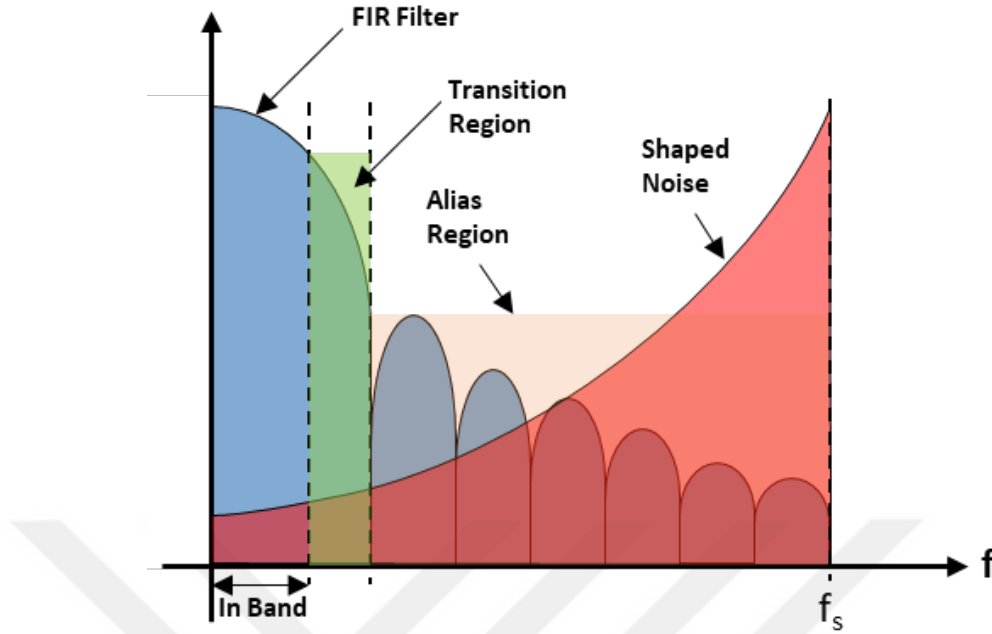


Figure 2.8: Digital FIR low pass filter spectral response.

For more straightforward implementations, comb filters and rectangular filters are preferred. One of the examples of comb filters is the Hogenauer filter. In this topology, cascaded comb filters are used for the decimation implementation since single order is insufficient to reject out-of-band white noise aliasing to the signal band [34] [35]. Third-order implementation of the CIC comb filter is demonstrated in Figure 2.9 for the decimation ratio (N).



Figure 2.9: Block diagram of 3rd order Hogenauer filter.

As the number of cascaded integrators and differentiators increases, the resolution is also enhanced. The same idea holds for the decimation ratio. On the other hand, incrementing cascade stages and decimation ratio bring delay to the system as multiplication of them. In addition, the number of registers in the implemented design should rise to prevent clipping. The frequency response of the filter implementation using MATLAB Filter Designer Toolbox (N=64) is illustrated in Figure 2.10.

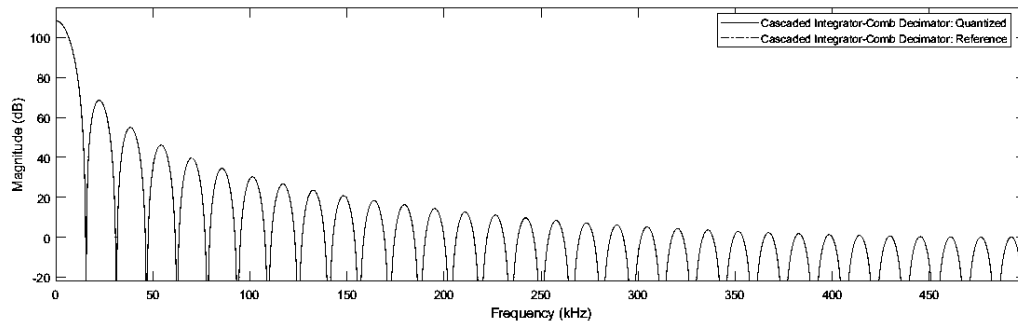


Figure 2.10: Frequency response of 3rd order CIC comb filter.

Obviously, the decimation filter establishes a base for the desired response. Still, it is insufficient to eliminate the shaped noise and mitigate the non-linearity due to the transition band of the frequency response. Therefore, another sharp digital low pass filter and a compensation filter can be designed to suppress further stopband, alias region ripples and sharpen the transition region of the filter. One of the examples of a CIC compensation filter combination is demonstrated in Figure 2.11.

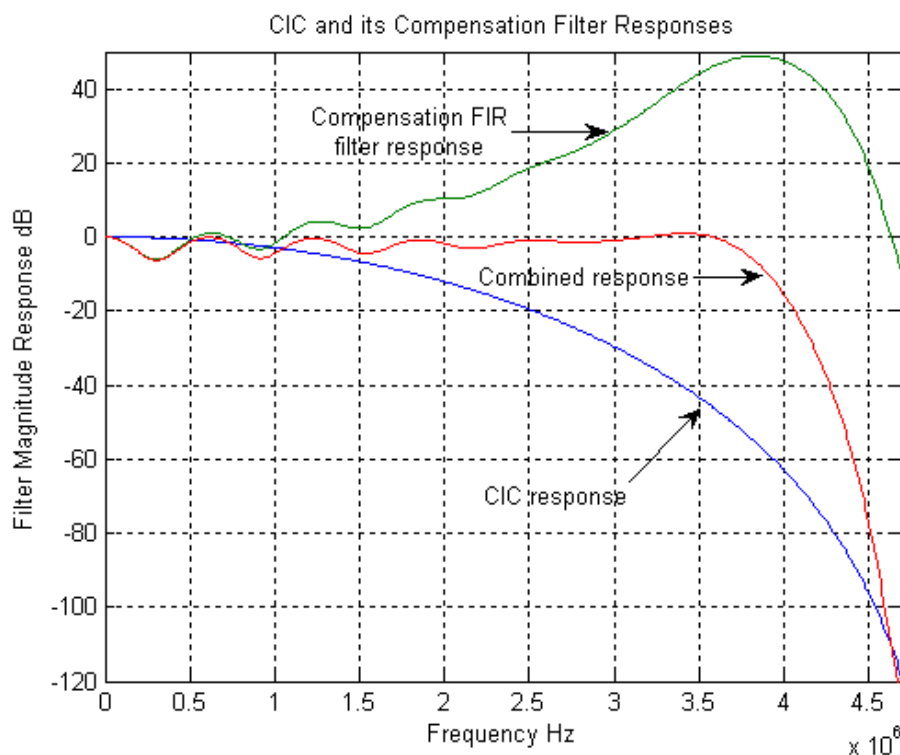


Figure 2.11: CIC filter compensation given in [36].

After compensating for the non-linearity due to the transition region of the decimation filter, cascading the resulting structure with a windowed FIR filter further sharpens the low pass filter with a better stopband rejection. As mentioned before, according to performance specifications, IIR filters are superior to FIR filters. Still, they are harder to implement, and a stable IIR filter design is challenging. Therefore, the thesis focused on the FIR filters in general, as most of the literature does.

FIR filters include cascaded delay blocks leading to delayed taps and particular window coefficients for the multiplication of each tap to get the desired spectral response. For example, a rectangular window has a constant coefficient, and basically, it operates as a moving average filter which also performs as a low pass filter. On the other hand, other filters have more complex filter coefficients, but they can be acquired using MATLAB Filter Designer Toolbox. However, hardware implementation will be more challenging since the number of shifting operations or the number of registers will increase as the bit depth of the coefficients increases, as well as increasing the number of taps with the notations given as b_m in Figure 2.12.

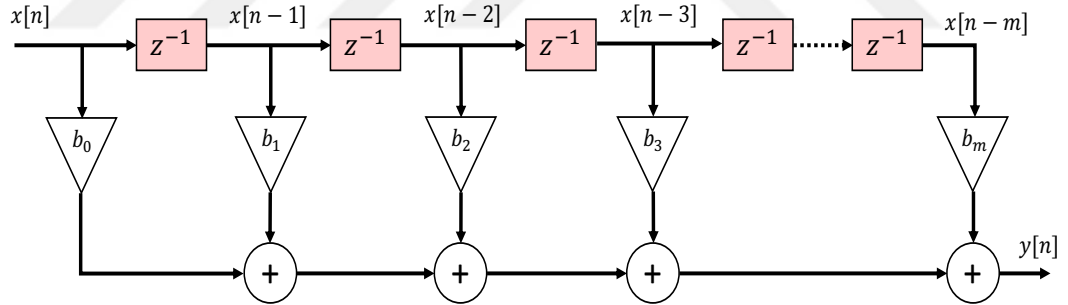


Figure 2.12: Sample block diagram for a m^{th} -order FIR filter.

Recently, literature also focuses on parameter and tap optimizations of FIR filters with techniques such as deep learning approaches to obtain a less demanding filter with a superior performance parameter [37], but they are not in the scope of this work.

An example of an FIR filter which is designed and simulated in Simulink spectral response is depicted in Figure 2.13. The flat-top window shows a sharper transition

region performance compared to windows such as Hamming and Blackman-Harris, but it has lower ripple rejection in exchange.

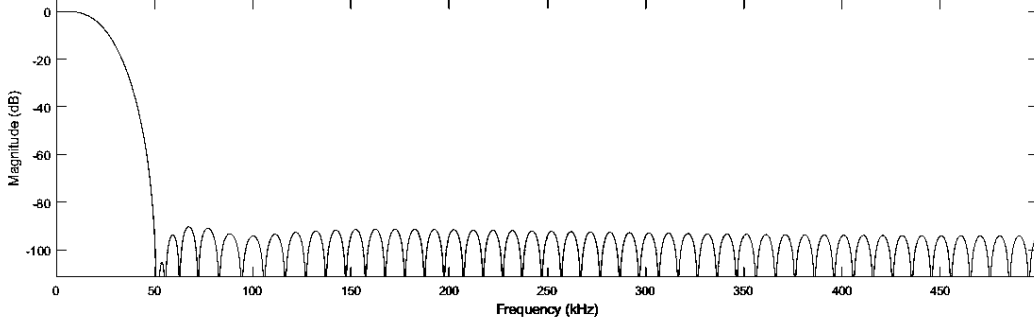


Figure 2.13: FIR filter spectral response with 100-tap flat top window implementation for 300 Hz cut-off frequency and 1MHz sampling rate.

2.3 Electro-mechanical $\Delta\Sigma$ Modulator Component

The essential component of the electro-mechanical $\Delta\Sigma$ converter for MEMS capacitive accelerometers is the sensor itself. It is not only utilized as a mechanical to an electrical transducer but also as a second-order integrator component of a delta-sigma loop. That is why they are irreplaceable yet less flexible components in the loop due to dependency on manufacturing process difficulties. As explained in Chapter 1, some readout systems deploy accelerometers as a single 2nd order integrator while enormously depending on the accelerometer sensor parameters, which are not flexible. Note that if the noise shaping characteristic is not sharp enough, then the readout system may encounter problems such as dead zones as given in [24], [38] and [39].

2.3.1 Capacitive MEMS Accelerometer

The capacitive MEMS accelerometer sensor utilized in this thesis will be examined in this section to provide a background on the parameters of accelerometer sensors and how they affect the loop dynamics. This system optimizes a single-axis,

differential, lateral and single-mass capacitive accelerometer. In general, capacitive accelerometers respond to the acceleration with the change in position of a mass, yielding a capacitance change. That way, a change in the capacitance can be transduced to an electrical quantity such as voltage or current.

The capacitive MEMS accelerometer sensor used in this thesis consists of lateral comb fingers attached to pair of electrodes and suspended proof mass anchored with crab legs, as illustrated in Figure 2.14.

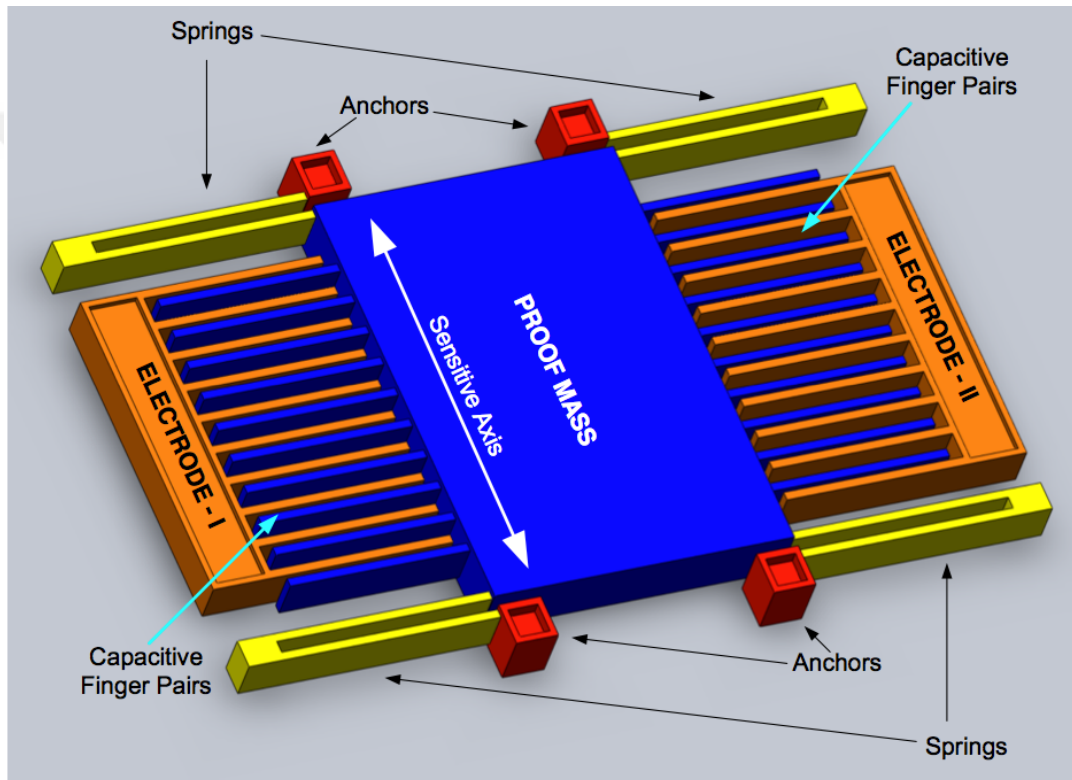


Figure 2.14: Mechanical model of capacitive MEMS accelerometer sensor [40, 39].

The proof mass is the main element with a degree of freedom in the sensitive axis. Springs are the crab legs that prevent any movement from the sensitive axis. Fingers are distributed at each side of the proof mass for the two-electrode system. Electrode fingers are placed in such a way that, if capacitance between one electrode and proof mass increases, the capacitance between other electrode and proof mass decreases approximately in the same magnitude.

Figure 2.15 illustrates the electro-mechanical transducing behavior of the sensor with the simplified diagram. C_p and C_n are the differential capacitances denoted according to their polarity of the change in the capacitance with the acceleration. PM is called the proof mass connection, electrically connected to Integrated Circuit (IC) ports. E_p and E_n are the other ports representing the electrical connections to the positive and negative electrodes, respectively. According to Figure 2.15, as the deflection of the proof mass from the origin in the sensing axis increases in the positive direction, C_p increases and C_n decreases.

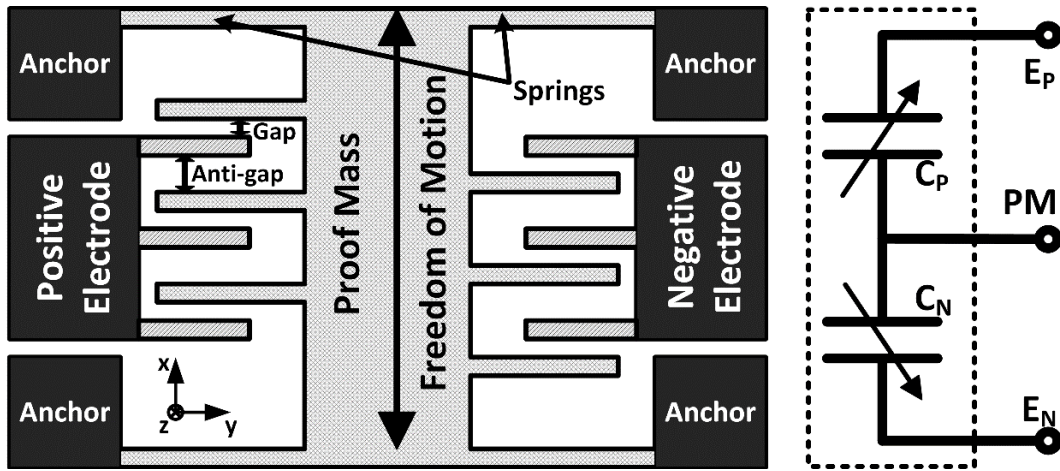


Figure 2.15: Electro-mechanical diagram illustrating the differential representation with capacitances (C_p , C_n) [41].

The mechanical behavior of the MEMS capacitive accelerometer sensors can be expressed the same as the second-order mass spring damper system as demonstrated according to Newton's law of inertia in Equation 2.18.

$$F = ma = m \frac{d^2x}{dt^2} + b \frac{dx}{dt} + kx \quad (2.18)$$

Where m is the mass quantity of the proof mass structure, k is the resulting spring constant of the crab legs holding the proof mass, and b is the damping coefficient due to squeeze film damping during the movement of the fingers relative to each

other. The resulting transfer function from acceleration to deflection from the origin in the sense axis is given in Equation 2.19:

$$H_{x/a}(s) = \frac{x(s)}{a(s)} = \frac{1}{s^2 + \left(\frac{b}{m}\right)s + \frac{k}{m}} = \frac{1}{s^2 + \frac{w_0}{Q}s + w_0^2} \quad (2.19)$$

where w_0 is natural (resonance) frequency and Q is the quality factor of the mass-spring-damper system, their expressions in terms of mechanical parameters are given in Equations 2.20-2.21.

$$Q = \frac{\sqrt{k \cdot m}}{b} \quad (2.20)$$

$$w_0 = \sqrt{\frac{k}{m}} \quad (2.21)$$

According to the differential equations of conversion from acceleration to displacement, $H_{x/a}(s)$ is clearly a low pass transfer function with 2 poles which can be used as a loop filter for the delta-sigma modulation. Generally, the quality factor is desired to be low, which means a higher damping coefficient.

As mentioned before, capacitive accelerometer sensors detect the acceleration with the deflection of the proof mass, and it turns it into differential capacitance change. Expression for the capacitance between the single electrode and proof mass is as given in Equation 2.22:

$$C = \frac{\epsilon_0 N A}{d \pm x} \quad (2.22)$$

where ϵ_0 is the permittivity constant of the air, A is the overlap area between the single comb fingers of the proof mass and one electrode, N is the number of fingers

on the proof mass and electrode, d is the gap distance between the fingers of the proof mass and one electrode's finger, x is the deflection distance of the proof mass. Finally, Equation 2.23 gives the resulting total capacitance expression between one electrode and the proof mass, considering the gap and anti-gap capacitance values.

$$C_{1,2} = \frac{N\epsilon_0 A}{d_1 \mp x} + \frac{(N-1)\epsilon_0 A}{d_2 \pm x} \quad (2.23)$$

Where C_1 and C_2 are the capacitance between the proof mass and electrodes 1-2, d_1 is the gap distance between one finger of the proof mass and one finger of the electrode, and d_2 is the anti-gap distance which is usually larger than the gap distance.

Table 2.1 defines the critical parameters of the MEMS accelerometer, which will be used in the rest of the thesis study for numerical analysis. Note that the accelerometer Q factor is relatively higher than the previously reported sensors in METU MEMS Center [24] [28] [40] due to vacuum packaging, which leads to resonator behavior with a lower random walk. That also means a more challenging controlling operation in exchange for the inherent noise of the sensor. The optimization is described in the following chapters.

Table 2.1: MEMS capacitive accelerometer sensor parameters utilized in this thesis.

Parameter	Value
m	66.1 μg
K	76.26 N/m
β	234.36 $\mu\text{N.s/m}$
Number of Fingers	192
d_1	2.55 μm
d_2	6.55 μm
h	35 μm
L	108 μm
f_{res}	5.41 kHz
Q	9.58
C_{rest}	3.5 pF

2.3.2 Basic Electro-mechanical Delta-Sigma Modulator

The most basic delta-sigma readout system for MEMS capacitive accelerometer can be obtained only by defining a quantizer and a feedback port to the system in the front-end interface, as shown in Figure 2.16. Input acceleration is defined in the accelerometer sensor, which behaves like a second-order integrator or low pass filter. That way, noise shaping can be performed as explained in Section 2.2.2. Denoting the transfer function of the accelerometer sensor as $H_{acce}(z)$, the noise transfer function of the sample system can be expressed as in Equation 2.24:

$$|NTF(z)| = \frac{1}{1 + k_Q A_{FE} H_{acce}(z) B} \quad (2.24)$$

where k_Q is the quantization factor, A_{FE} is the front-end circuit gain, and B is the feedback multiplication factor. The most critical factor affecting the noise shaping characteristic is the transfer function parameters of the accelerometer sensor, as the poles of the corresponding function appear as the zeros at the resulting NTF.

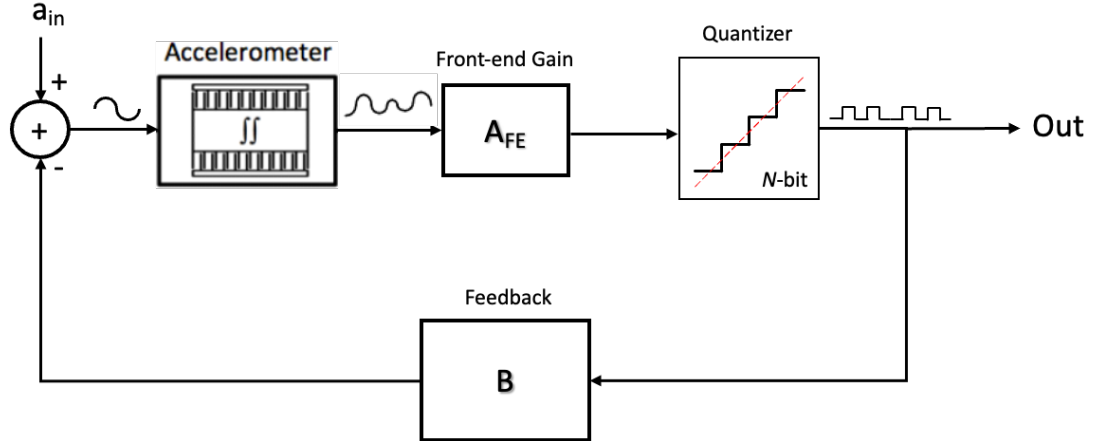


Figure 2.16: Electro-mechanical component only delta-sigma modulator.

According to the accelerometer parameters defined in the previous section, the pole-zero map is graphed as in Figure 2.17 with two zeros at $z=-1$ and two conjugate poles with values $z_1=0.9979+j0.0274$ and $z_2=0.9979-j0.0274$ for 1MHz sampling rate.

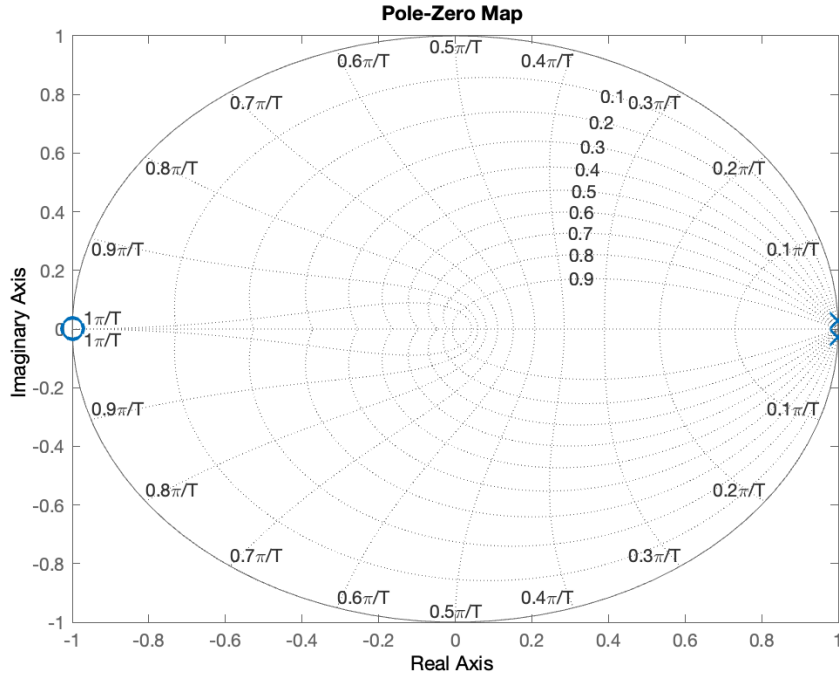


Figure 2.17: Pole-zero map of the calculated accelerometer transfer function.

It should be emphasized that the poles and zeros directly affect the noise shaping of the system and the sensor itself defines complex poles to the system. Consequently, the system is hard to control due to the relatively high Q accelerometer sensor. According to utilized proportionality constants, there is a contradicting relationship between the noise shaping and loop stability of the readout. Furthermore, any mismatch or errors in fabrication causes unexpected deviations from ideality and discrepancies in the loop strategy. Optimization of accelerometer sensor according to loop strategy of delta-sigma is laborious since, for every iteration, detailed finite element analysis should be performed, and loop simulations should be run for every parametric change. Also, note that for a stable and robust noise shaping, the accelerometer needs to have a vast proof mass, the optimized value of damping for the best case of Brownian noise performance-noise shaping performance and a very low spring constant in exchange with the bandwidth limitation.

Figure 2.18 graphs the noise shaping performance of the wafer level vacuum packaged accelerometer sensor defined by METU MEMS Center. The

demonstrations and equations of the NTF are approximations and estimations. Therefore, the transient simulation must be performed in the MATLAB Simulink environment to fulfil a complete verification cycle, as in the following chapters.

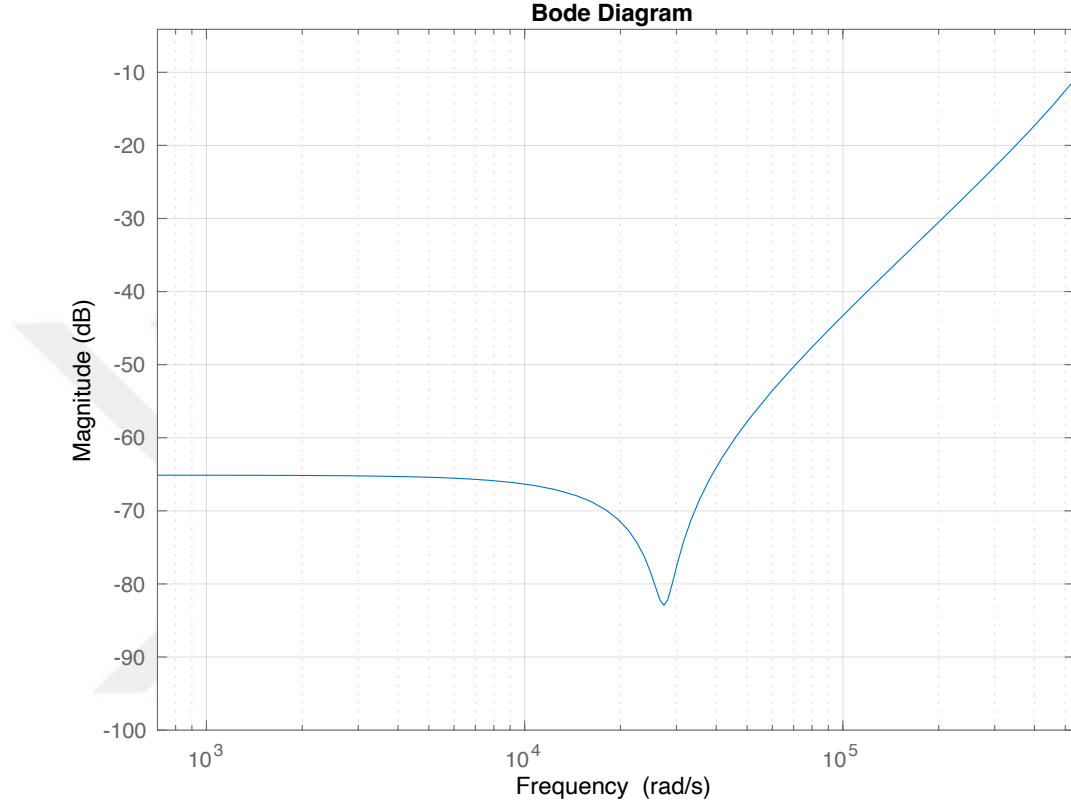


Figure 2.18: Noise shaping characteristic of the electro-mechanical component-only system.

According to the simulations performed for the z-domain transfer functions, quantization noise is shaped to keep stability on the edge while serving the best noise shaping performance. Consequently, in-band quantization noise is stuck at -65.1 dB white noise, which is an unsatisfactory performance compared to the specifications defined for this thesis. It is possible to achieve better performance by decreasing the resonance frequency of the electro-mechanical component, which has the expression K/m . That means a unique process should be used to increase the weight of the mass, as demonstrated in Figure 1.3, and soft springs should be manufactured for the anchoring of proof mass, yielding large area consumption and detailed stress

analysis. On the other hand, digital electronics have a better, more accessible and flexible solution for better noise shaping of $\Sigma\Delta$ modulation compared to mechanical only modulators. In addition, the DC gain of the mechanical accelerometers appears to be too small, which might cause a dead-zone effect. In order to overcome that problem, simply increasing the gain of the mechanical sensor by elevating the ratio K/m means sacrificing the noise performance while incrementing the amplitude of the oscillations. Another solution is defining another integrator to the system, allowing a better noise shaping performance and sufficient $\Sigma\Delta$ oscillations to overcome the dead-zone effect.

2.4 Summary of the Chapter

In this chapter, the primary purpose was to prepare for the following chapters and to provide an introduction level comprehension of $\Sigma\Delta$ modulators in general and MEMS capacitive accelerometer sensor used as noise shaping component. To comprehend the theory behind the conversion from acceleration to digital data conversion, concepts such as sampling, quantization and digital filtering are brought in as the basics of $\Sigma\Delta$ modulation. For more clear illustration, frequency domain reflections of the operations are examined and formulated primarily using bilinear transform, which is a good approximation compared to the matched method.

According to the equations and expressions given in this chapter, every analog to digital conversion has quantization errors and discrepancies such as noise folding or aliasing. To solve problems, explained three design concepts of $\Sigma\Delta$ modulator should be designed to have a good agreement and coherence with each other to meet the noise specification. Oversampling cannot be sufficient without noise shaping, and noise shaping cannot perform well enough without filtering elements at the output.

The system's mechanical element is essential and cannot be discarded because of the transducing operation. $\Sigma\Delta$ modulators shape the noise utilizing a low pass filter, and such characteristics can be obtained from the sensing element without using any

sources. But for the closed-loop operation, design aspects should include in-band noise and stability conditions well optimized to meet those conditions. Electro-mechanical part is insufficient to meet those requirements, as shown in the final section of this chapter. Therefore, the loop strategy should be adjustable electronically to radically increase the system's performance in every aspect. That way, reliance on mechanical parameters can be kept minimal to relax the fabrication requirements of the sensor for lower noise and stable performance parameters.





CHAPTER 3

ELECTRO-MECHANICAL SYSTEM DESIGN OVERVIEW

This chapter includes the design and analysis of a mixed signal higher order electro-mechanical $\Sigma\Delta$ modulator implemented in this thesis work. Initially, the system is coarsely defined for a simple introduction. This section will present the system overview and its conveniences over the general problems of electro-mechanical $\Sigma\Delta$ modulator problems. Section 3.2 introduces the linearized model for the sake of simplicity of the system-level analysis. Section 3.3 examines the Zoom ADC at a system level. Section 3.4 confirms the system-level architectures with the simulations performed in the Matlab Simulink environment. Finally, a summary of the chapter is given.

3.1 System Level Overview

According to the reasoning and analysis in Chapter 2, electro-mechanical $\Sigma\Delta$ modulator performance parameters might suffer from insufficient noise shaping characteristic of mechanical accelerometer sensor as low pass filter. Furthermore, fabricated accelerometers might have a lower DC gain for a lower noise specification, but that might create a dead-zone problem, as stated before. To manage those problems for a simple loop implementation, the mass should be massive and anchored with very soft springs yielding a hefty process optimization. However, electrical $\Sigma\Delta$ integrator modules mitigate the strict reliance on accelerometer sensor parameters.

Figure 3.1 illustrates the prominent system architecture implemented in this work with functional blocks. According to the accelerometer sensor parameters defined, 4th order electro-mechanical delta-sigma modulation architecture is selected for convenience. Note that higher order or lower order system architectures can also be

implemented due to the flexibility of the system implementation, which is further elaborated in the following chapter. In the literature, there are diverse integration examples of PID block, which is strictly designed for the best performance optimization of the readout system according to the mechanical parameters of the sensor. Another type of system utilization can be unconstrained electro-mechanical delta-sigma modulator topology which was firstly proposed by [25]. Unconstrained architectures do the same optimization inside the sigma-delta block to shape the noise according to pole-zero locations of the accelerometer sensor.

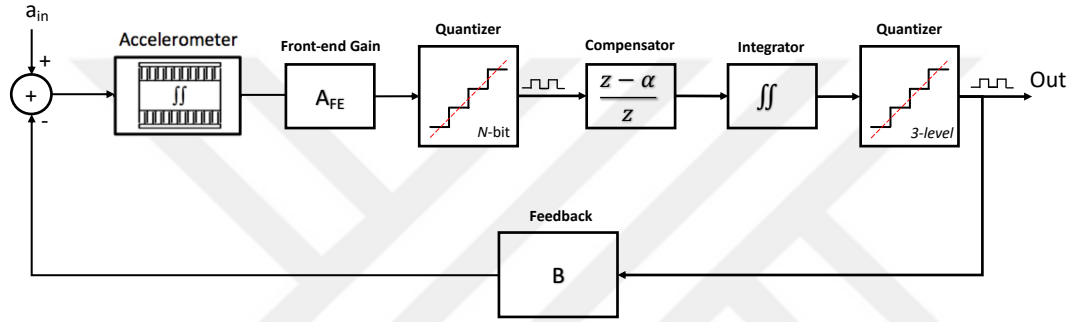


Figure 3.1: Block diagram of complete electro-mechanical delta-sigma modulator implemented in this thesis.

In the thesis work, a phase compensator as a controller block was selected for stable operation in the closed-loop configuration. In general, phase compensator modules degrade the noise shaping performance of the system to some degree. Still, the accelerometer sensor has a relatively high Q , and the system must have a stable operation rather than a high-performance operation. Moreover, the noise shaping performance is boosted sufficiently with mixed signal implementation to achieve low quantization noise.

The linearity performance of electro-mechanical delta sigma readout systems is degraded due to systematic errors such as offsets due to wire bonding and parasitic effects. Section 2.3.1 shows the deflection from the linear assumption according to the displacement of the proof mass from the origin. As the displacement increases from the rest position, the non-linearity of the readout increases dramatically due to the non-linear formulation of the capacitive transducer. Note that any systematic error yields a deflection of the proof mass from the rest position due to closed loop

operation. To overcome that problem, digital offset correction is integrated into the system in the digital domain by calibration under zero-g. That way, dynamic range, in-band noise performance and linearity are enhanced.

In this chapter, analysis and formulation will be done on the linear model of the system, which enables simple derivations. Stability and linearity analysis will be estimated using that model. The results of that model will be checked and verified using MATLAB Simulink environment with a detailed model implementation.

3.2 Linearity Analysis

The electro-mechanical block is a combination of mechanical and electronic blocks; the system's output should be in the electrical domain. Initially, modelling the mechanical sensor is critical since it includes both domains as a transducer. In addition, most of the non-linearities or second-order effects rise from the sensor module. Therefore, special care must be taken while formulating such results. The following sections will mainly focus on those effects and how the mixed signal electro-mechanical delta-sigma oversampling system minimizes the reflection on the output.

3.2.1 Linearity Approximation of Sensing Mechanism

The sensing mechanism consists of a mechanical transfer function converting input acceleration to a displacement and conversion of displacement to capacitance value which is the primary source of error due to the non-linear nature of the parallel plate capacitance formulation, which was given in the previous chapter.

Figure 3.2 illustrates the sensing mechanism through digital data conversion. In the first-place incoming acceleration is low pass filtered with the mechanical accelerometer sensor. Then, the displacement is converted to capacitance with differential capacitance change configuration.

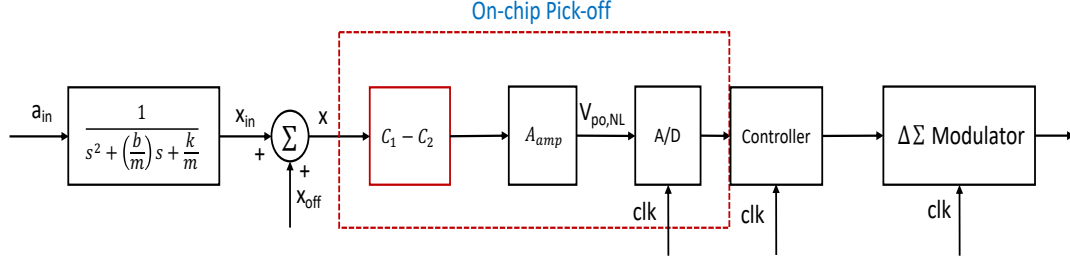


Figure 3.2: Block diagram of displacement sensing path.

Note that, $\frac{dC}{dx}$ term is the primary source of deflection from linearity assumption. In addition, there are offset sources stemming from any systematical error. After that, data is digitized inside Application Specific Integrated Circuit (ASIC) by a high-resolution oversampling ADC before modulation to correct low-frequency errors stemming from the feedback mechanism, as explained in the next section.

According to the formulation, it is clear that the expression of the capacitances between electrodes and the proof mass on one side fingers is non-linear with the increasing deflection of the proof mass from the origin. The capacitance changes between the proof mass and one of the electrodes can be expressed as in Equation 3.1.

$$\frac{dC_{1,2}}{dx} = \epsilon_0 A \left(\frac{N}{(d_1 \mp x)^2} - \frac{N-1}{(d_2 \pm x)^2} \right) \quad (3.1)$$

According to the expression above, it is evident that the best linearity can be achieved when deflection is near $x=0$ valley, yielding a constant capacitance change per deflection, which is ideal for a Linear Time-Invariant (LTI) system assumption.

The effect of deflection on linearity is demonstrated in Figure 3.3. According to the plot obtained using the parameters provided in Table 2.1, the optimum linear region of the capacitive accelerometer sensor is bounded in the deflection range $[-20\text{nm}, 20\text{nm}]$.

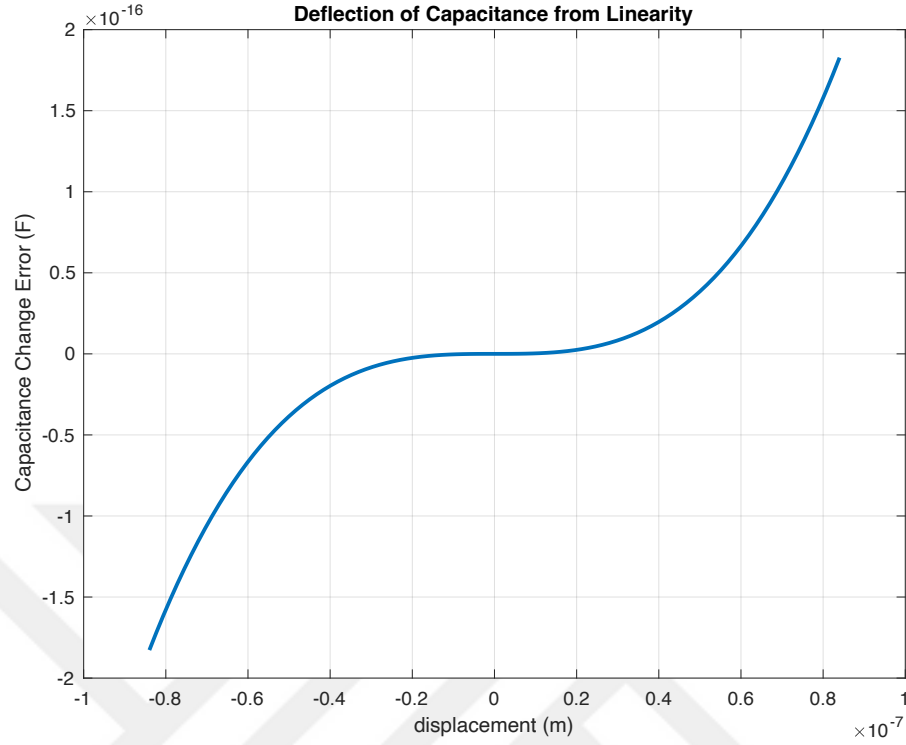


Figure 3.3: Capacitance change deflection from the linear capacitance change assumption.

Linearity can be investigated in detail using Maclaurin series expansion of the non-linear term with higher order representations. The equation expressing the Maclaurin series expansion of the sensitivity term is given in Equation 3.2:

$$\begin{aligned} \frac{dC_{1,2}}{dx} = & \frac{\varepsilon_0 AN}{d_1^2} (1 \pm 2v_1 + 3v_1^2 \pm 4v_1^3 + \dots) - \\ & \frac{\varepsilon_0 A(N-1)}{d_2^2} (1 \mp 2v_2 + 3v_2^2 \mp 4v_2^3 + \dots) \end{aligned} \quad (3.2)$$

where $v_1 = x/d_1$ and $v_2 = x/d_2$ are the proportion of deflection from the origin according to the gap and anti-gap distances. Note that the anti-gap distance of the capacitive accelerometer can be assumed as sufficiently large that $\frac{\varepsilon_0 AN}{d_2^2}$ and $v_2 = x/d_2$ terms have an insignificantly low impact on the sensitivity term. That is why the sensitivity equation explains the non-linearity of the deflection from the linearity depicted in Figure 3.3.

A fundamental way to express the deflection seen from the system in terms of system parameters is given in Equation 3.3:

$$V_{Po,NL} = A_{amp}(C_1 - C_2) = A_{amp} \left[\frac{\varepsilon_0 AN}{d_1 - x} - \frac{\varepsilon_0 AN}{d_1 + x} \right] \quad (3.3)$$

Note that derivation in Equation 3.3 indicates that any mismatch occurring between the area of the plates will appear as an offset in the readout. Still, any difference in the gap distance difference leads to non-linearity in the system that is very complex to mitigate. The gap distance difference can occur due to any offset injected into the system during the closed loop operation, which is explained in the next section. It may also appear due to natural reasons such as the fabrication process.

Capacitance values $C_{1,2}$ and final sensed voltage terms in Equation 3.3 can be further expressed in terms of Maclaurin series expansion yielding the Equations 3.4-3.5 as follows:

$$\begin{aligned} C_1 &= \frac{\varepsilon_0 AN}{d_1 - x} = \frac{\varepsilon_0 AN}{d_1} (1 + v + v^2 + v^3 \dots), \\ C_2 &= \frac{\varepsilon_0 AN}{d_1 + x} = \frac{\varepsilon_0 AN}{d_1} (1 - v + v^2 - v^3 \dots) \end{aligned} \quad (3.4)$$

The final expression of the sensed voltage in the pick-off circuit is expressed according to switched capacitor amplifier circuit proportionality term (A_{amp}), sensitivity terms are given, which are second order harmonics and $v = \frac{x}{d_1}$ is the ratio of the deflection to the gap distance.

$$\begin{aligned} dV_{Po,NL}/dx &= A_{Po,NL} \\ &= \frac{d(A_{amp}(C_1 - C_2))}{dx} = 2A_{amp} \frac{\varepsilon_0 AN}{d_1^2} (1 + 3v^2 + 5v^4 + \dots) \end{aligned} \quad (3.5)$$

Note that x term was formulated concerning the deflection due to acceleration and systematic error as offset term x_{off} . Therefore, any offset error contributes to the second order terms and increases the non-linear deflection.

3.2.2 Linear Approximation of Electrostatic Feedback Force

In closed-loop configuration, the accelerometer sensor is used both as a sensor and actuator. Both mechanisms have distortions due to high-order effects, which will be introduced in this chapter.

To comprehend the actuation of a standard parallel plate capacitance, energy storage in capacitance is the initial phenomenon that should be considered. Energy stored in a capacitor can be formulated with the basic formula given in Equation 3.6:

$$E = \frac{1}{2} CV^2 \quad (3.6)$$

where C is the capacitance between two parallel plates and V is the potential voltage difference between the capacitor plates. Change in the stored energy between two parallel plate capacitors occurs according to the magnitude of the exerted force and displacement of the plates relative to each other from their rest positions. So, actuation force expression can be obtained by taking the derivation of the stored energy concerning displacement as given in Equation 3.7:

$$F = \frac{dE}{dx} = \frac{1}{2} \frac{dC}{dx} V^2 \quad (3.7)$$

where $\frac{dC}{dx}$ is the sensitivity of the capacitance previously given in Equation 2.23. That way, a force can be exerted on the accelerometer sensor counterbalancing the input acceleration with expression $F_{fb} = ma_{in}$ assuming loop gain is large enough for a lower steady-state error assumption.

Note that delta-sigma modulators produce an average value that mitigates the non-linearity due to the squared relationship with voltage value in the force feedback expression. So, the system's output becomes the square root value of the applied

acceleration to counterbalance the input acceleration without any harmonic distortion. That is why oversampled digital feedback architectures are superior to analog feedback architectures due to the linear nature of force feedback.

Referring to the previous statements, an output voltage of the electro-mechanical delta-sigma modulator can be formulated as in Equation 3.8:

$$V_{out} = \sqrt{\frac{2ma_{in}}{dC/dx}} \quad (3.8)$$

There are two ways of applying digital force feedback to an accelerometer in actuation mode: Pulse Width Modulation (PWM) and Pulse Density Modulation (PDM). The PWM method shapes the feedback signals such that the pulse width of the signal sent to the stators in Figure 3.4 is fed with continuity. On the other hand, PDM utilizes signals with equal widths producing a meaningful average over a period of time. PDM is also a one-way signal which might have a long period of pulses that has no actuation force on average.

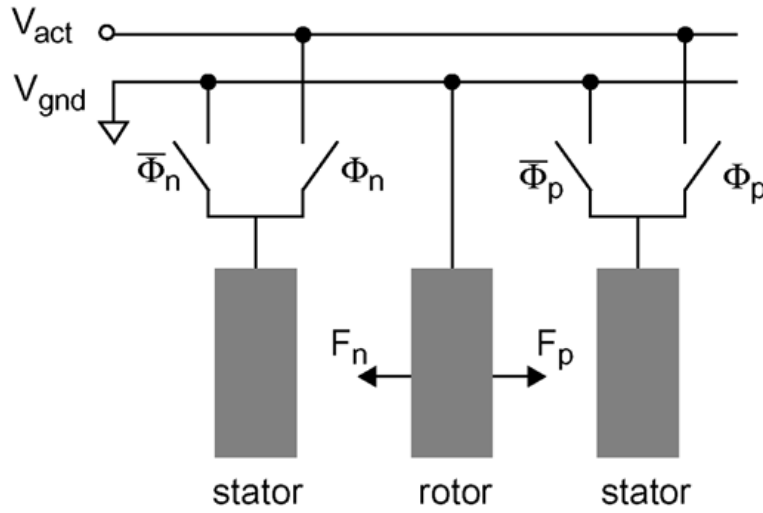


Figure 3.4: Feedback configuration for tri-level electrostatic actuator mode [20].

One of the main disadvantages of PWM is the systematic error induced to the system due to rise and fall times. In addition, the clock's jitter for feedback yields a random

error primarily when high voltage feedback interfaces are used. On the other hand, PDM feedback systems do not suffer from the problems stated because rise and fall times are almost identical within serial pulses generated, and the clock's jitter is averaged [20]. Therefore, the PDM method is more convenient for the electro-mechanical delta-sigma modulator feedback mechanism.

One of the essential linearity performance bottlenecks is the feedback mechanism if any steady state or systematic error couples with the actual signal at the output. Therefore, the design should be analyzed in detail to prevent any high-order effects on the sensing mechanism due to actuation discrepancies.

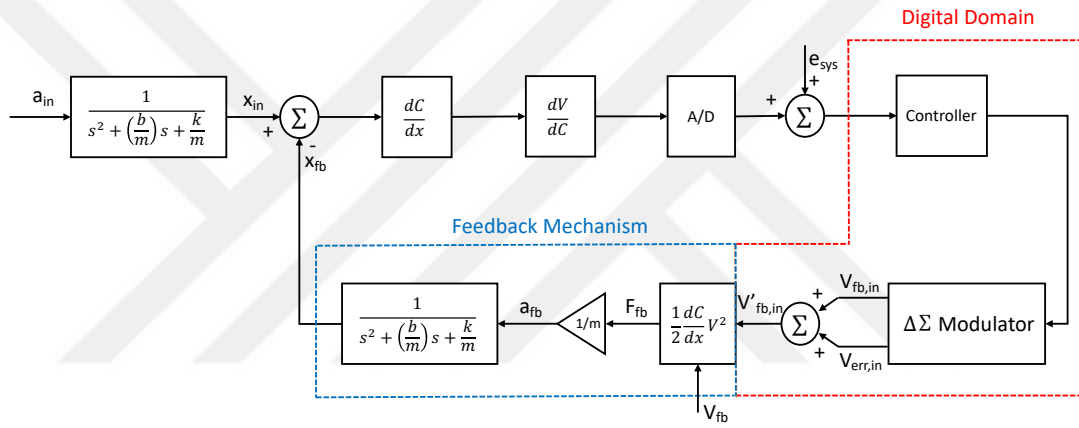


Figure 3.5: Basic representation of complete system blocks with actuation illustration.

Figure 3.5 shows the system's simple demonstration with the coarse modules' indications through the feedback mechanism. The system consists of a second-order accelerometer model representing an acceleration conversion to displacement. The feedback model of a digital oversampling system shows a linear behavior. Still, possible error sources stem from the non-idealities of the real-life applications, such as offset due to parasitic capacitances or circuit errors which are output referred to and denoted as e_{sys} . Those effects can be examined using a non-linear model of the feedback mechanism. Force feedback, marked as F_{fb} has the expression as formulated in Equation 3.9:

$$F_{fb} = \frac{V_{fb}^2}{2} \left(\frac{V'_{fb,in} + 1}{2} \frac{dC_1}{dx} + \frac{V'_{fb,in} - 1}{2} \frac{dC_2}{dx} \right) \quad (3.9)$$

where V_{fb} is the amplitude of each level shifted identical pulse fed to accelerometer sensor, $V_{fb,in}$ is an output pulse train of delta-sigma modulator inside the digital domain and $\frac{dC}{dx}$ is the sensitivity of proof mass capacitors with corresponding electrodes. Note that feedback force is expressed according to complementary feedback configuration.

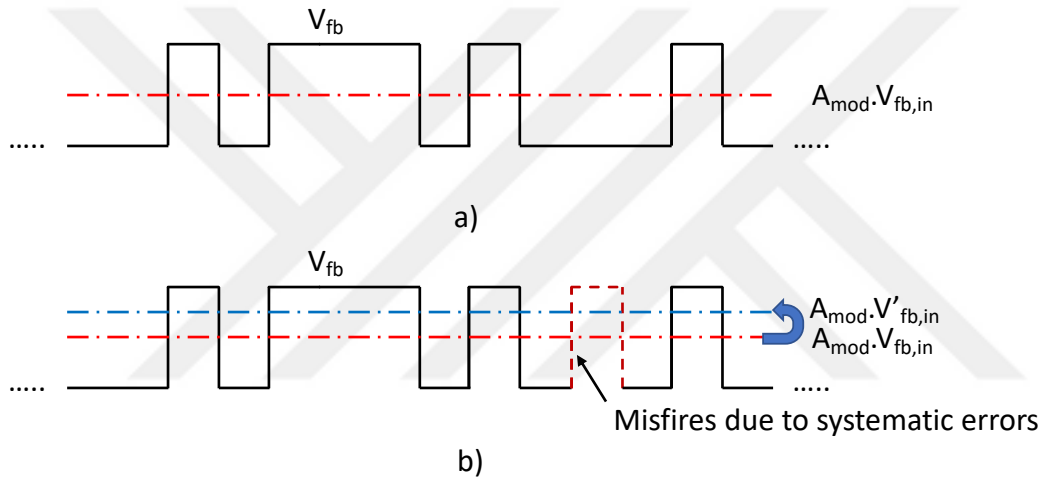


Figure 3.6: Level shifted pulse train fed to feedback mechanism for a) ideal and b) non-ideal case.

Figure 3.6 illustrates the level shifted pulse sequence for an ideal input value of $V_{fb,in}$ and an input value with non-idealities such as systematic errors $V'_{fb,in}$ where A_{mod} is the delta-sigma modulator gain. Note that $V'_{fb,in}$ consists of an ideal input value and reflection of systematic errors in the delta-sigma modulator module as depicted. The resulting feedback signal includes misfires in high frequency modulated signal resulting in a shift in the averaged signal in the time domain. Figure 3.7 illustrates the low-pass operation in feedback signal demodulation while applying a high-frequency pulse sequence to the accelerometer sensor.

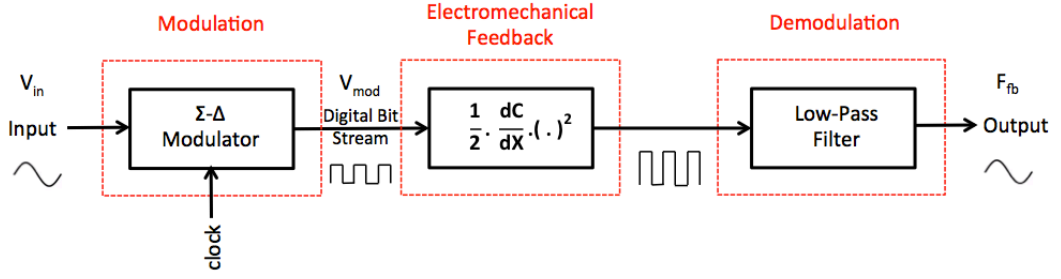


Figure 3.7: Feedback signal demonstration with demodulation explained in [28].

Therefore, the misfires in the modulated signal are expected to cause an offset in the feedback signal. But that is not a reason for non-linearity stemming from a feedback mechanism directly seen at the output since that only causes an offset in the position. However, the offset in the position of the proof mass results in the non-linearity observed in the sensing mechanism since deflection from the rest position is a source of non-linearity, which is already examined. Note that the feedback signal of the designed system is generated from the digital domain. Thus, the offset from the systematic errors can be eliminated with digital correction with the precision provided by the A/D module in the low-frequency region.

To catch the remaining non-linearity expressions stemming from the force feedback, $\frac{dC}{dx}$ term includes higher order terms rather than a simple constant term that should be investigated. For two electrodes, the expression of force according to those can be formulated as in Equation 3.10 by reorganizing Equation 3.9:

$$\begin{aligned} F_{fb} &= \frac{V_{fb}^2}{2} \left[V_{fb,in} \left(\frac{dC_1}{dx} + \frac{dC_2}{dx} \right) + \frac{1}{2} \left(\frac{dC_1}{dx} - \frac{dC_2}{dx} \right) \right] \\ &= A_{VF,NL} V_{fb,in}' + k_{e,NL} x \end{aligned} \quad (3.10)$$

where $A_{VF,NL}$ and $k_{e,NL}$ are the non-linear terms governing the force feedback relations in terms of voltage provided and displacement from the origin.

In the previous chapter, capacitance change concerning displacement was given as $\frac{dC}{dx} = \epsilon_0 A \left(\frac{N}{(d_1-x)^2} - \frac{N-1}{(d_2+x)^2} \right)$. The formulation of the expressions $\left(\frac{dC_1}{dx} + \frac{dC_2}{dx} \right)$ and

$\left(\frac{dC_1}{dx} - \frac{dC_2}{dx}\right)$ are expanded using Maclaurin series as in the Equation 3.11 referring to Equation 3.4 from the previous section assuming the anti-gap distance is sufficiently larger than gap distance for simplicity:

$$\begin{aligned}\left(\frac{dC_1}{dx} + \frac{dC_2}{dx}\right) &= 2 \frac{\varepsilon_0 AN}{d_1^2} (1 + 3v^2 + 5v^3 + \dots), \\ \left(\frac{dC_1}{dx} - \frac{dC_2}{dx}\right) &= 4 \frac{\varepsilon_0 AN}{d_1^3} x(1 + 2v^2 + 3v^4 + \dots)\end{aligned}\quad (3.11)$$

Using Equation 3.11, non-linear terms $A_{VF,NL}$ and $k_{e,NL}$ can be expanded as in Equation 3.12:

$$\begin{aligned}A_{VF,NL} &= \frac{V_{fb}^2}{2} \frac{\varepsilon_0 AN}{d_1^2} (1 + 3v^2 + 5v^3 + \dots), \\ k_{e,NL} &= V_{fb}^2 \frac{\varepsilon_0 AN}{d_1^3} (1 + 2v^2 + 3v^4 + \dots)\end{aligned}\quad (3.12)$$

where $k_{e,NL}$ is the well-known spring softening term and $A_{VF,NL}$ is the gain factor used in the conversion from voltage to force quantity. In order to achieve a simple system for calculation purposes, they will be simplified up to first-order terms, and the illustration is given in the next section.

Note that the feedback is provided with duty-cycled pulse density modulation. The time should be adjusted between the sampling and the feedback phases in the sampling period, denoted as T_s . Then the feedback transfer function for the system spending half of the cycle on reading can be shown as in Equation 3.13:

$$H_{FB}(s) = \frac{A_{VF,NL}(e^{-s\tau_1} - e^{-s\tau_2})}{s}, \tau_1 = \frac{T_s}{2}, \tau_2 = T_s \quad (3.13)$$

Using bilinear transform, which maps Laplace variable to z-domain as $s = \frac{2}{T} \left(\frac{z-1}{z+1}\right)$ where T is sampling period, the final transfer function can be obtained as in Equation 3.14:

$$H_{FB}(z) = \frac{A_{VF,NL}(e^{-\frac{2T}{T_2}(\frac{z-1}{z+1})} - e^{-\frac{2}{T}T(\frac{z-1}{z+1})})}{\frac{2}{T}(\frac{z-1}{z+1})} \quad (3.14)$$

To further simplify the conversion, the Taylor series expansion formula of the exponential term, which is $e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \dots$ can be used to obtain the final transfer function in Equation 3.15:

$$H_{FB}(z) = \frac{A_{VF,NL}}{2} \cdot \frac{T_{FB}}{T_s} \quad (3.15)$$

Where T_s is the operating frequency of the system, T_{FB} is the feedback duration for a single conversion cycle and $H_{FB}(z)$ is the transfer function resulting in the non-linear amplification term. The results show that for linear approximation, force feedback can be divided by 2 to express the duty cycle effect. Note that further jitter or unequal rise-fall time problems can be calculated using Equation 3.14. But those effects are minimal on the system performance since clock signals are generated by the FPGA's Phase Locked Loop (PLL) block with a sufficiently low jitter performance, which is explained in the following chapters. Therefore, in the rest of the system modelling, feedback will be denoted as $\frac{A_{VF,NL}T_s}{2}$.

3.2.3 Linear System Model and Analysis

Figure 3.8 demonstrates the system blocks before further simplifying to show that system error can be approximated to nearly zero. The reason behind this is A/D module is a high-resolution noise shaping quantizer that allows a high-resolution offset correction in the digital domain. For that operation, the system should operate in zero-g condition for several minutes in an open-loop configuration. Then the ADC output should be averaged in that period to obtain the low-frequency DC component noise of the system. Finally, the found offset is recorded and substituted at every

operation cycle to mitigate systematic errors anticipating the non-linearity terms and noise. The system blocks that are causing non-linearity are colored in Figure 3.8. The electrostatic spring constant is demonstrated as a positive feedback port to show that the spring constant gets softer as the electrostatic spring constant is elevated.

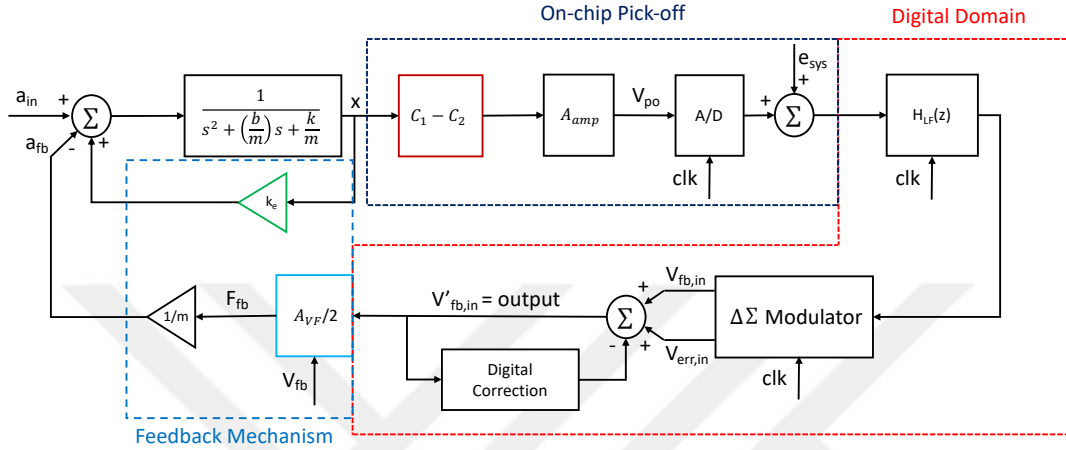


Figure 3.8: Linear system block with auxiliary modules.

Before converting to z-domain from s-domain, the spring softening effect is calculated and included in the z-domain block of the accelerometer model, as depicted in Figure 3.9. Figure 3.10 shows the overall simplified block for intuitive calculation purposes. The accelerometer sensor is expressed in the z-domain since most blocks are in the discrete-time domain as digital blocks. The reason calculation is performed before the conversion is the simplicity of the feedback calculation before the bilinear transformation. As explained before, the spring softening effect occurs due to the feedback mechanism.

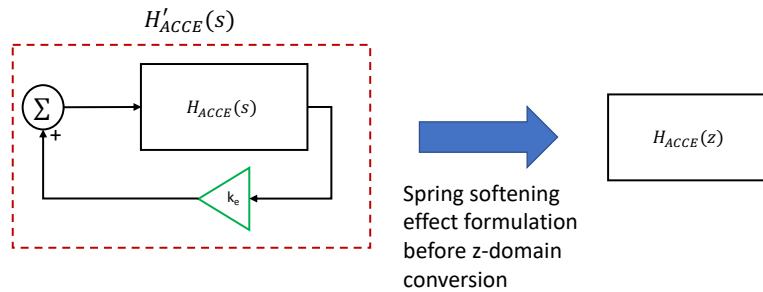


Figure 3.9: Spring softening modelling before z-domain conversion.

The calculation of the transfer function of the mechanical accelerometer sensor, including the spring softening effect, is given as in Equation 3.16:

$$H'_{ACCE}(s) = \frac{1}{s^2 + \frac{b}{m}s + \frac{(k - k_e)}{m}} \quad (3.16)$$

Also, note that acceleration is initially transduced to deflection of the proof mass from the rest position. The differential change in the capacitance due to deflection is sampled in front-end circuitry in the sampling speed. As the system itself already operates in the discrete-time domain, the ADC module is modelled as a simple $k_{q,AD}$ multiplier, which is in good agreement with the model in the previous chapter. Modulator and ADC modules have z-domain expressions since they introduce delay to the system, which are 2 clock delay and 1 clock delay correspondingly. That can be expressed with zeros in the z-domain with orders equal to the number of clock delays.

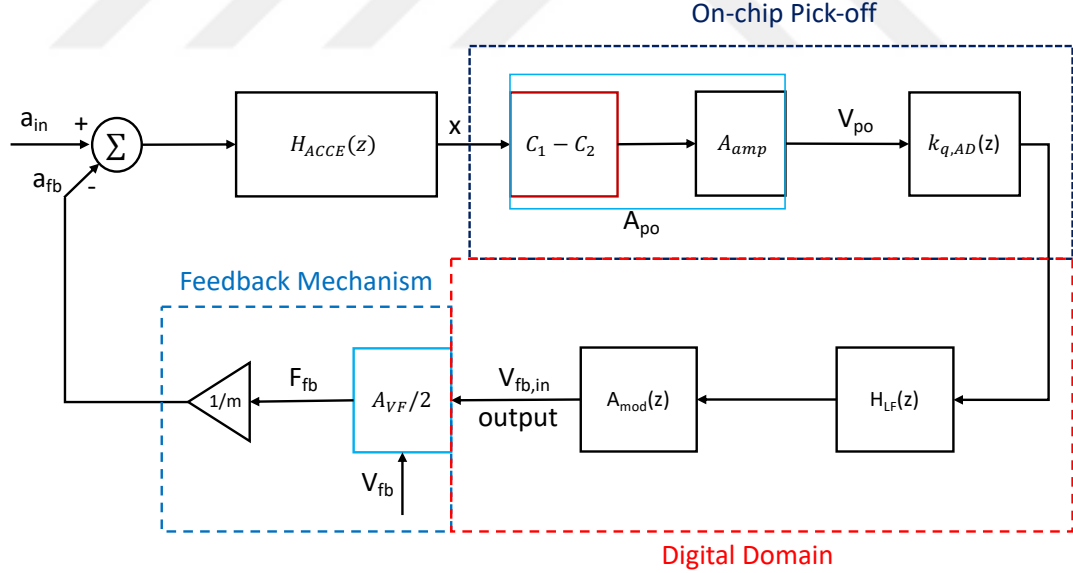


Figure 3.10: Simplified linear system block.

In the previous chapter, the accelerometer mechanical transfer function was expressed in the z-domain with detailed expression. Therefore, it will not be

modelled again in this section. The following formulations of blocks are given as in Equations 3.17-3.21:

$$A_{po} = 2A_{amp} \left(\frac{\varepsilon_0 AN}{d_1^2} - \frac{\varepsilon_0 A(N-1)}{d_2^2} \right) \quad (3.17)$$

$$k_{q,AD}(z) = |k_{q,AD}| \cdot z^{-1} \quad (3.18)$$

$$A_{mod}(z) = |A_{mod}| \cdot z^{-L} \quad (3.19)$$

$$H_{LF}(z) = K_{LF} \frac{z - \alpha}{z} \quad (3.20)$$

$$A_{VF} = \frac{V_{fb}^2}{2} \left(\frac{\varepsilon_0 AN}{d_1^2} - \frac{\varepsilon_0 A(N-1)}{d_2^2} \right) \quad (3.21)$$

where A_{po} is the pick-off circuit gain, $|k_{q,AD}(z)|$ is the magnitude of the ADC mapping, $|A_{mod}|$ is the magnitude of the delta-sigma modulator multiplication constant, L is the order of the delta-sigma for integrators that do not have unity STF, α is the factor of phase lead compensator module which is denoted as loop filter and A_{VF} is the linear representation of the voltage to force multiplication.

The simplified model is only used for analysis to investigate non-linearity sources easier. Using Equations 3.17-3.21 and expressions, the open-loop transfer function of the system can be obtained as Equation 3.22:

$$A_{OL}(z) = H_{ACCE}(z)A_{po}k_{q,AD}(z)H_{LF}(z)A_{mod}(z) \quad (3.22)$$

Finally, the closed-loop transfer function can be found in Equation 3.23:

$$A_{CL} = \frac{A_{OL}}{1 + \beta A_{OL}} = \frac{H_{ACCE}(z)A_{po}k_{q,AD}(z)H_{LF}(z)A_{mod}(z)}{1 + \frac{A_{VF}}{2m}H_{ACCE}(z)A_{po}k_{q,AD}(z)H_{LF}(z)A_{mod}(z)} \quad (3.23)$$

The result exhibits a fourth-order polynomial for numerator and denominator. 2 poles and 2 zeros are cancelled by each other. Therefore, the system is dominated by 2 conjugate poles and 1 zero at nearly $z = 0.5$. In addition, as the gain increases, the system exhibits a better linearity performance, but it has limits due to stability concerns.

According to results shown in Figure 3.11-Figure 3.16, the system exhibits a non-linearity performance of 212 ppm standard deviation and 202 ppm steady state error under 3g ramp input in 1 second. For 20g ramp input in 1 second, the standard deviation is observed as 799 ppm standard deviation and 408 ppm steady state error under 20g ramp input in 1 second. To further investigate the source of non-linearity, a linear model is implemented in the Simulink environment with the same detailed model except for the linearized implementation of colored items in Figure 3.8. Note that that system exhibits non-linearity performance as 76 ppm average and decreases as time proceeds and system settles down independent of input acceleration. That is an expected result since linear system approximation is expected to be independent of deflection distance due to the miscalculation of second-order effects explained in the previous sections.

On the other hand, there is another non-ideality in the system, which is FIR filter output, and the reason why it contributes to non-linearity is explained in Chapter 2. However, note that the non-linearity caused by the system itself is negligible compared to the non-linearity due to deflection of the capacitance from the rest

position. Error graphics also demonstrate a higher order harmonic behavior, proving the point. The error graphs are pessimistic as the ramp input causes settling errors at the output at each point resulting with a worse non-linearity behavior.

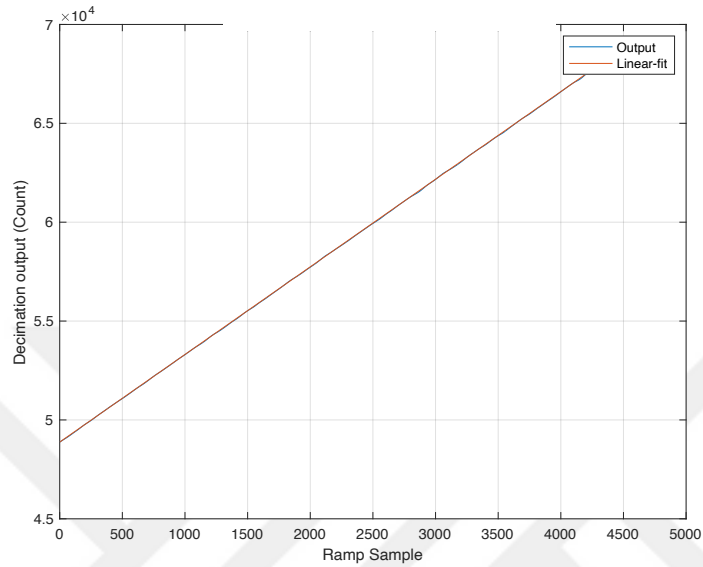


Figure 3.11: Non-linear Simulink model ramp response of the overall closed system up to 3g input for 1 second.

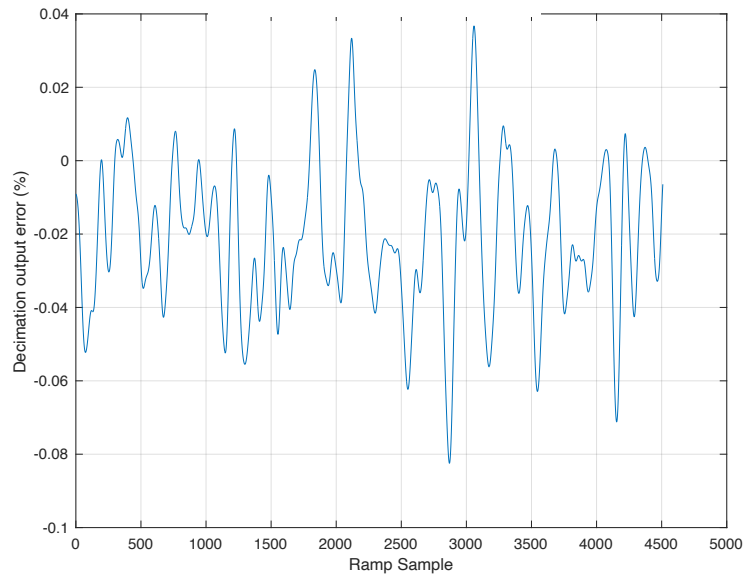


Figure 3.12: Linearity error plot under 3g ramp input (non-linear Simulink model) exhibiting 212 ppm standard deviation and 202 ppm steady state error.

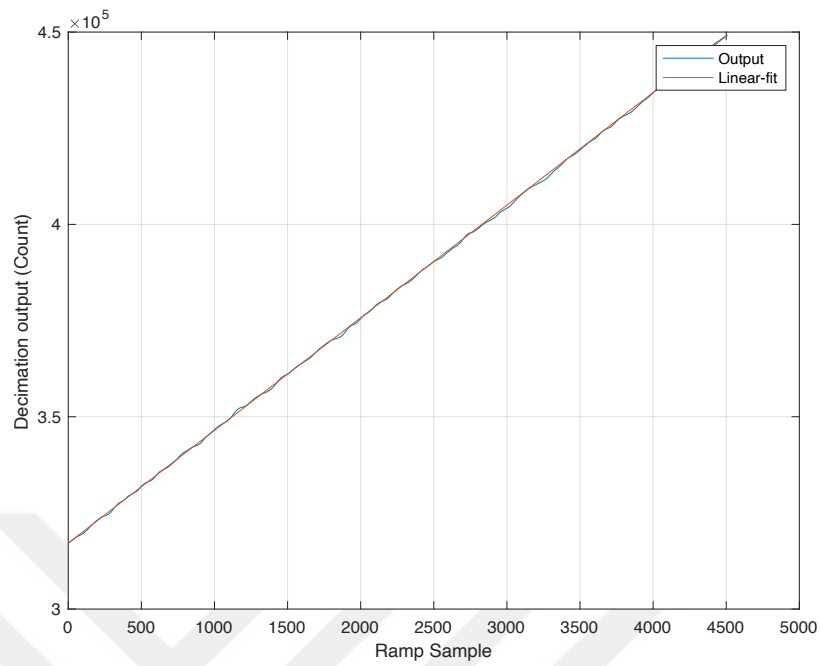


Figure 3.13: Non-linear Simulink model ramp response of the overall closed system up to 20g input for 1 second.

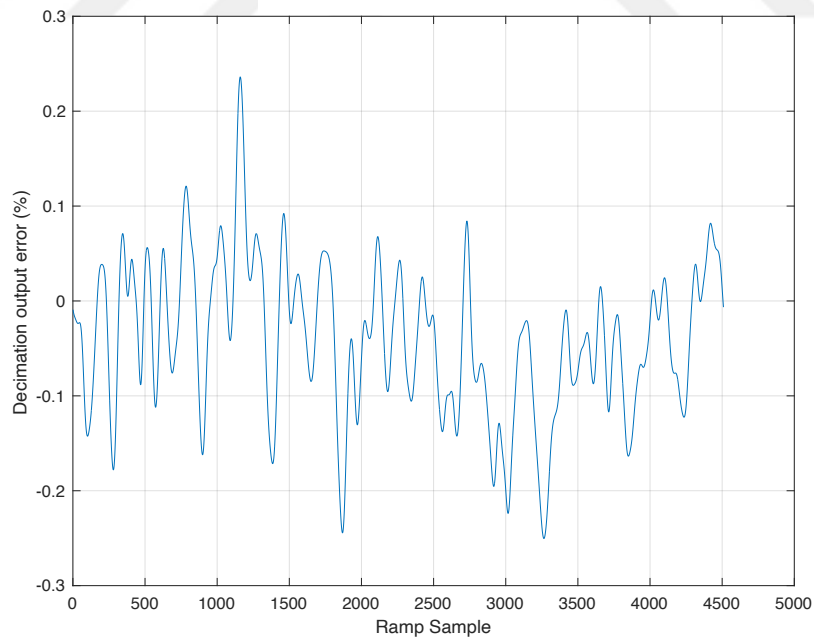


Figure 3.14: Linearity error plot under 20g ramp input (non-linear Simulink model).

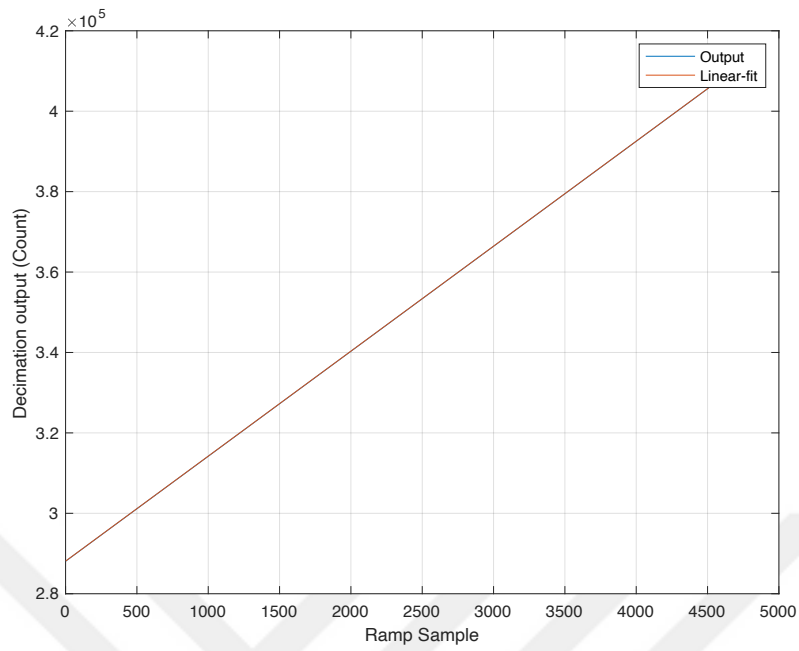


Figure 3.15: Linear Simulink model ramp response of the overall closed system up to 20g input for 1 second.

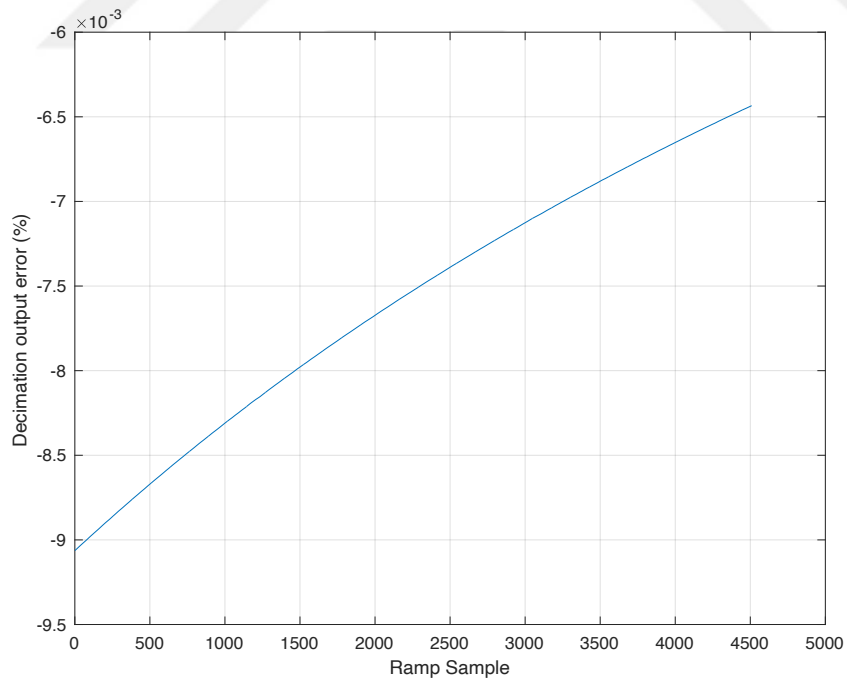


Figure 3.16: Linearity error plot under 20g ramp input (linear Simulink model).

3.3 Stability Analysis

Using the simplified linear analysis model, stability analysis is simplified to see the effects of the loop filter on the electro-mechanical accelerometer loop. Reading the sensor itself with a loop filter is not an optimized way since the settling time of the proof mass position takes milliseconds. The reason behind that ringing effect is the high-quality factor of the sensor. The resonant peak at those types of sensors becomes significant in stability analysis.

The top system model is utilized for system stability verification, which is also shown in Figure 4.36. As explained before, the system comprises the second order mechanical sensor behavior with a transfer function, basic calculation blocks for conversions, Zoom ADC model, which is described in the following chapter with a detailed signal domain analysis, loop filter, delta-sigma modulator and feedback module emulating the effects explained in 3.2.2.

Each accelerometer sensor design exhibits distinct stability behavior under test. Therefore, the loop filter should be utilized and optimized according to accelerometer sensor parameters. Otherwise, the system will be shifted to a pitfall solution. Sensors with higher quality factor parameters are harder to control, so a compensation filter should be utilized for the sensor to ensure a stable operation [42]. On the other hand, sensors with a higher damping factor can be controlled by employing a PI controller to enhance the linearity performance of the system [43]. Note that the designed readout system allows any kind of digitally implementable filter for optimization. Therefore, the modelled system illustrates that the flexibility of the digital filter does not harm the performance requirements.

Figure 3.17 shows the system behavior using the linear model introduced in the previous section. For bode plot stability analysis open-loop transfer function is used utilizing different α parameters. When $\alpha = 0.7$, the system exhibits a 68° stability margin, which yields approximately $100\mu s$ of settling time as depicted in Figure 3.18. Resonant peak is the main problem of stability, and it is overwhelmed

with the help of a phase compensation filter. Otherwise, the open-loop configuration yields 3 milliseconds of settling time, as graphed in Figure 3.19, which is insufficient due to ringing behavior. Finally, the step response of the overall system is shown in Figure 3.20, which is also further low pass filtered due to FIR output probing, demonstrating a nearly critically damped behavior. Cut-off frequency selection is independent of the settling time of the system. However, the system should settle in a short time as delta-sigma modulators includes the previous sampled data. As mentioned, open-loop configuration results with 3 milliseconds of settling time for 1g input acceleration, that yields cumulated harmonics at the initial FIR filtered output. Note that, cut-off frequency is set according to FIR filter properties. As the number of taps in the FIR filter increase, then the cut-off frequency reduces leading to lower noise.

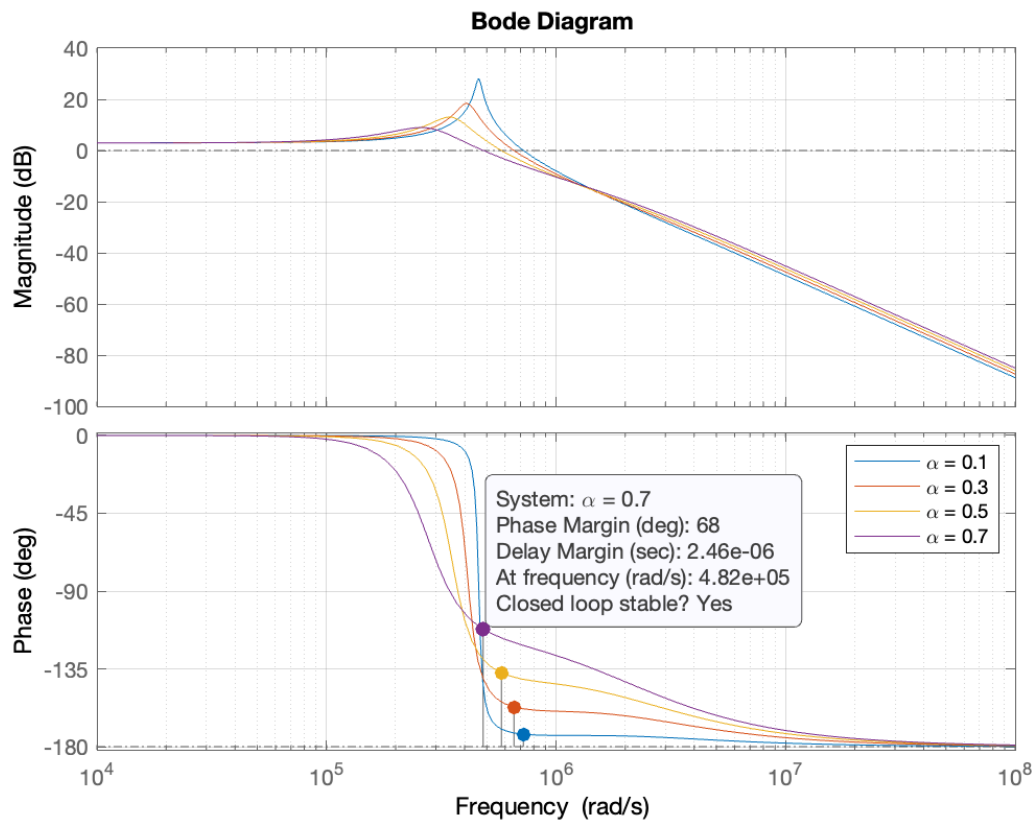


Figure 3.17: Stability analysis for different loop filter parameters.

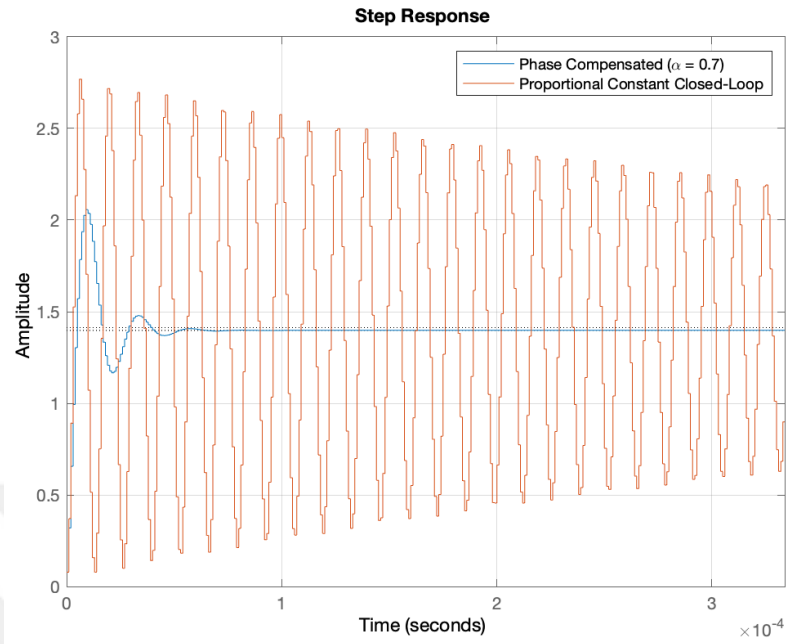


Figure 3.18: Step response for $\alpha=0.7$ in loop filter and proportional constant closed loop system for given accelerometer sensor.

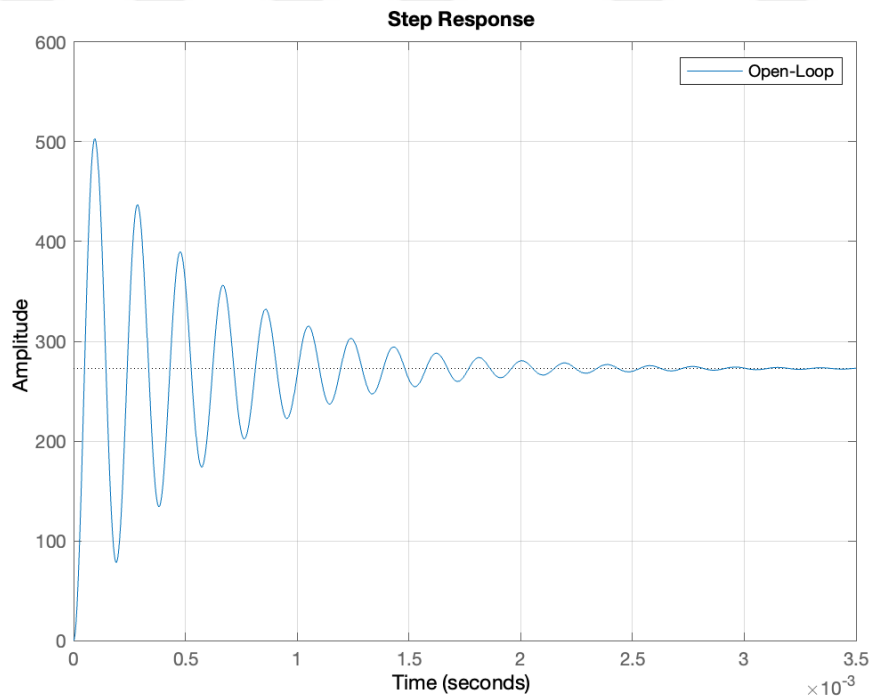


Figure 3.19: Step response of the accelerometer readout system in an open-loop configuration.

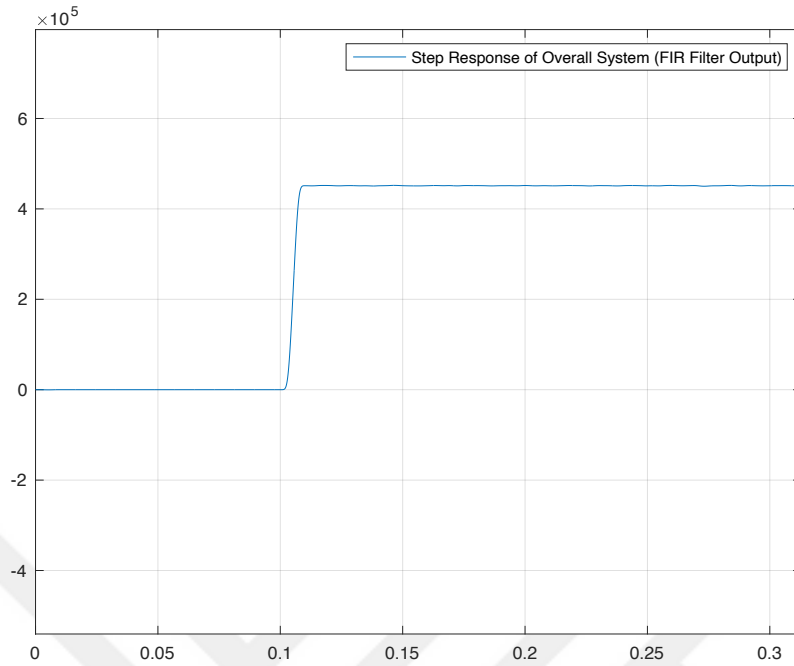


Figure 3.20: Step response of the overall non-ideal model of the system implemented in Simulink environment with FIR filter output probing.

3.4 Noise Analysis

The system mainly consists of 4 primary noise sources: Brownian noise, electronic noise, feedback noise and quantization noise. Figure 3.21 illustrates the model in that every noise source except quantization noise is included. Previous chapter identifies the quantization noise and its shaping behavior ideally using ideal loop filter, that is why further analysis is not necessary.

Note that quantization noise cannot be modelled in a linear system model and the noise model is a simple model to locate the error sources. Ideal noise shaping calculations cannot be employed, too. Since an electro-mechanical integrator is leaky compared to an ideal digital integrator, and the sensor element has a low gain, violating the ideal integration operation assumption in the loop filter. The Simulink model described in the final chapter is used to perform the complex noise analysis.

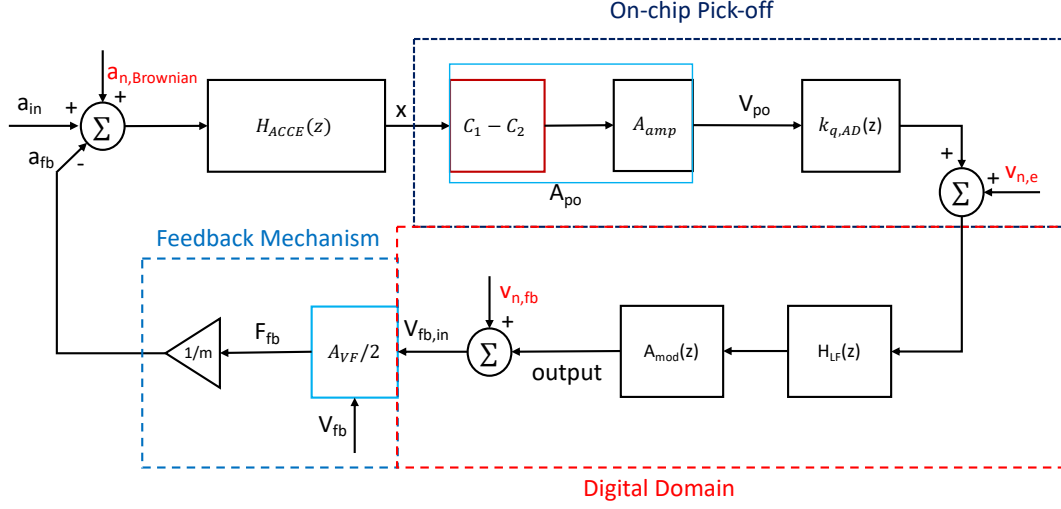


Figure 3.21: Noise model of the system based on linear system blocks.

3.4.1 Brownian Noise

Any air molecule with kinetic energy has a random momentum along the motion direction. The kinetic energy of a molecule is related to temperature. Air molecules in the accelerometer system hit the proof mass randomly, leading to random walk due to Brownian motion. For vacuum-packaged systems, the air within the electro-mechanical sensor is sealed and has much less amount of random walk. That is why vacuum packaged systems have less Brownian noise.

On the other hand, damping due to air molecules is less, leading to a higher quality factor. Brownian noise is represented by the expression $a_{n,Brownian}$ in Figure 3.21 as an acceleration input. Brownian noise source is the most dominant noise source in the system. The source of that type of noise is the random mechanical motion of the sensor during the operation. Equation 3.24 formulates the theoretical magnitude value of the noise in terms of spectral white noise, which is also inserted into the Simulink model as given in [44].

$$a_{n,Brownian} = \frac{\sqrt{4k_B T B}}{m} = \sqrt{\frac{8k_B T \pi f_0}{mQ}} \left(\frac{m}{s^2} / \sqrt{Hz}\right) \quad (3.24)$$

where k_B is Boltzmann constant, T is temperature, f_0 is the resonant frequency, Q is the quality factor, and m is the total residual mass of the proof mass structure. Note that the Brownian noise unit is given in terms of spectral white noise magnitude. Furthermore, high-quality factor sensors are harder to control but have relatively lower Brownian noise. Brownian noise of a sensor is an inevitable noise source that cannot be shaped or predicted; thus, it will directly appear at the output.

3.4.2 Electronic System Noise

Electronic noise is denoted as $v_{n,e}$ as in Figure 3.21 deployed at the end of ADC output in the model. The noise model comprises the front-end circuitry noise of the programmable gain amplifier noise and total ADC noise with quantization noise. For simplicity, the front-end circuitry noise is coupled with Programmable Gain Amplifier (PGA) noise. The expression of electronic noise in terms of front-end electronic noise and ADC noise is given in Equation 3.25:

$$v_{n,e} = \sqrt{A_{amp}^2 v_{n,fe}^2 + v_{n,ADCQ}^2} \quad (3.25)$$

Front-end noise might be dominant in electronic system noise in general, so front-end circuitry should be carefully designed since another module amplifies it in pick-off circuitry. The noise transfer function of the electronic system referring to Figure 3.21 can be given as in Equation 3.26 in terms of acceleration:

$$NTF_e(z) = \frac{H_{LF}(z) A_{mod}(z) \frac{A_{VF}}{2m}}{1 + \frac{A_{VF}}{2m} H_{ACCE}(z) A_{po} k_{q,AD} H_{LF}(z) A_{mod}} \quad (3.26)$$

Equation 3.26 points out a significant result: the readout noise is shaped too. As observed from the analysis of the mechanical model of the accelerometer sensor in the previous chapter, a capacitive MEMS accelerometer is a low pass filter. It shapes the noise if it is a denominator-only term yielding conversion of mechanical poles to zeros of the noise transfer function. The s-domain simplified formulation of that calculation is given in Equation 3.27:

$$NTF_e(s) = \frac{H_{LF}(s)|A_{mod}|\frac{A_{VF}}{2m}(s^2 + \frac{b}{m}s + \frac{k - k_e}{m})}{s^2 + \frac{b}{m}s + \frac{k - k_e}{m} + \frac{A_{VF}}{2m}A_{po}k_{q,AD}H_{LF}(s)|A_{mod}|} \quad (3.27)$$

Loop filter has an insignificant effect on the noise shaping of electronic noise. In addition, the system exhibits a high pass behavior with a resonant frequency determined by $\frac{k-k_e}{m}$ term. The system's poles are at higher frequencies yielding bounded NTF magnitude at high frequencies. At DC terms ($s=0$), $\frac{k-k_e}{m}$ term has a significant effect on the magnitude of that transfer function. If $k=k_e$, then electronic noise can be simply accepted as zero level. But that requires a high voltage as the electrostatic spring constant can be magnified using voltage feedback. Note that increasing voltage feedback generates stability issues at some level and should not exceed approximately 10V. On the other hand, to equalize the electrostatic spring coefficient to the spring constant of the mechanical sensor, the feedback voltage needs to exceed 10V.

The quantization noise of the ADC is already a low noise signal due to inherited noise shaping. The only concern would be front-end circuitry designed to have sufficiently low noise, as explained in the next chapter. In addition, DC offset or systematic error of the electronic noise is also shaped with the same transfer function. Still, it significantly elevates the in-band noise, so it must be corrected. The performance can be limited to minimum 10 $\mu\text{g}/\sqrt{\text{Hz}}$ noise performance, if a capacitive mismatch of the sensor reaches to 15 fF which is a possible value due to parasitic capacitances on the proof mass.

3.4.3 Feedback Noise

A Feedback voltage needs to be applied to keep the proof mass near to rest position for the best linearity performance. But feedback voltage is directly converted to acceleration, so it directly affects the noise performance of the readout system. Input referred feedback noise expression can be formulated as in Equation 3.28:

$$a_{n,fb} = v_{n,fb} \frac{V_{fb}}{2m} \varepsilon_0 A \left(\frac{N}{d_1^2} - \frac{N-1}{d_2^2} \right) \quad (3.28)$$

where, $v_{n,fb}$ is the feedback noise defined in the system. Increasing feedback voltage has several advantages, such as reduced electrical noise and higher dynamic range. On the other hand, if it is increased without considering the overall system noise level, feedback noise can easily dominate the noise performance of the system.

The complete system noise simulations are performed in MATLAB Simulink environment for better accuracy. Table 3.1 illustrates the decomposition of noise sources. The verification of the noise analysis is performed using Power Spectral Density (PSD) simulations with the system implemented in Simulink.

Table 3.1: Simulated noise values categorized according to sources.

Noise Sources	Value
Brownian Noise	3.09 $\mu\text{g}/\text{VHz}$
Readout Circuit Noise	200 nV/VHz
Feedback Voltage Noise	100 nV/VHz
Quantization Noise	<500 ng/VHz
Total Output Noise	3.4 $\mu\text{g}/\text{VHz}$

All noise sources of the system are assumed to be white noise and are modelled in the Simulink using that approximation. Brownian noise is inevitable as mentioned

earlier, and for a good readout design, other noise sources should be buried inside Brownian noise.

Electronic noise is shaped, as mentioned earlier. Therefore, it is probably not a dominant noise source of the system. According to SPICE transient noise simulations of the circuit implemented which are given in detail in Chapter 4, front-end circuitry has $750 \mu V$ output peak to peak noise which corresponds to $113.636 nV/\sqrt{Hz}$ white noise performance according to Equation 3.29:

$$a_n = \frac{1}{6.6} \frac{a_{pp}}{\sqrt{f_B}} \quad (3.29)$$

where a_{pp} is the peak-to-peak noise level and f_B is the bandwidth of the system. Note that the sampling system works with a 1MHz sampling clock frequency. Simulink model noise simulation is not dominated by front-end circuitry according to calculations because the output gain is divided by the gain of the amplifier, which is well above to suppress the noise due to front-end circuitry. In addition, the spring softening effect reduces the noise as well.

Feedback noise is different from electronic noise, directly contributing to the system's noise. Therefore, the feedback voltage regulator should be selected according to feedback noise specification. For higher feedback voltages, the specification gets harder to overcome. For $100 nV/\sqrt{Hz}$ white noise input feedback voltage source, the system can work up to 7V feedback voltage without violating the specifications according to given mechanical sensor parameters.

Quantization noise cannot be directly extracted as the other noises mentioned. Therefore, two different noise simulations are performed, as depicted in Figure 3.22 and Figure 3.23. The quantization dominant system, which also includes all noise sources, performs up to $-114 dB/\sqrt{Hz}$ which is well below the Brownian noise included simulation exhibiting $-109.37 dB/\sqrt{Hz}$ total system simulation under 0.1g

sinusoid excitation. To avoid non-linearities and shaped noise folding, the system refresh frequency is selected as 300Hz by programming the FIR filter.

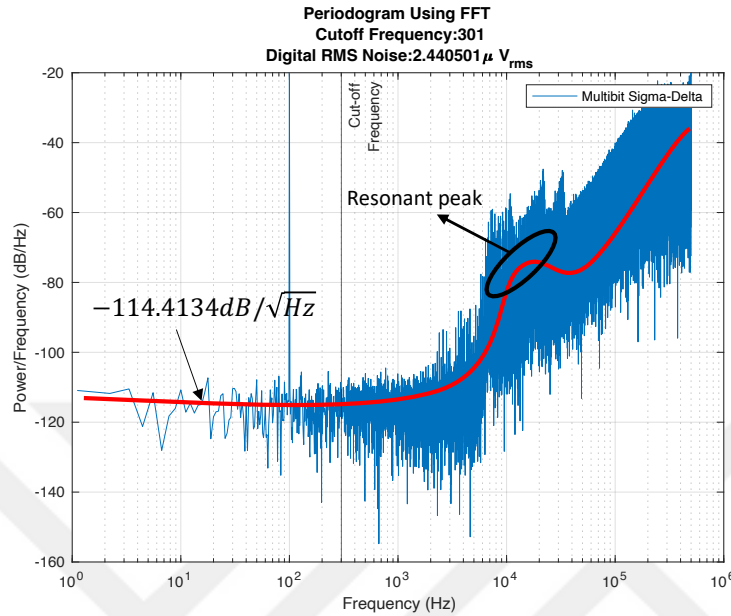


Figure 3.22: PSD simulation of the overall system, including noise sources except Brownian noise indicating $-114\text{dB}/\sqrt{\text{Hz}}$ spectral white noise performance.

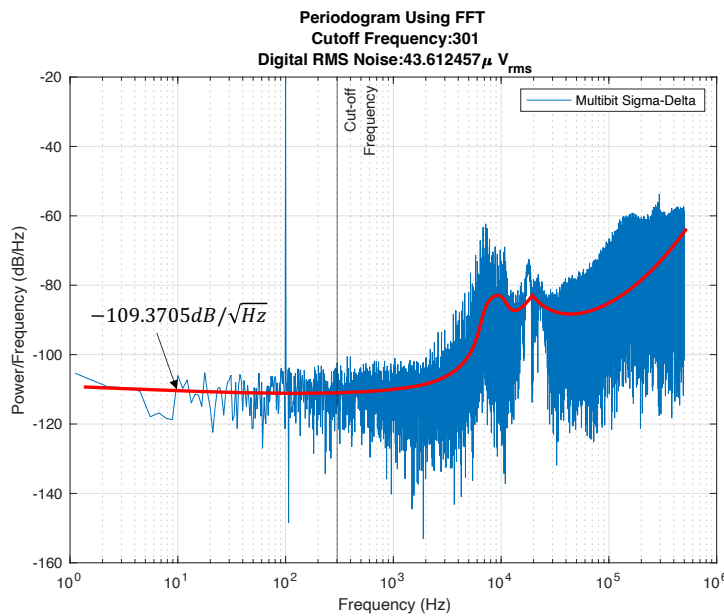


Figure 3.23: PSD simulation of overall system including noise sources indicating nearly $-109\text{dB}/\sqrt{\text{Hz}}$ spectral white noise performance.

3.5 System Flexibility Test

This work proposes an architecture that is compatible for various type of accelerometer sensors. For example, the previous work [28], which was based on a sensor with a lower quality factor. It has a higher damping as the fabrication was not vacuum packaged. It had a Brownian noise level of $4.6 \mu\text{g}/\sqrt{\text{Hz}}$ value, which is higher than the sensor presented in this work. The stability and linearity calculations of the previous system also holds for the digitized design using the same configurations of the loop filter (PI controller).

The most important performance parameter that needs extra attention is the noise. The loop filter phase compensator in Figure 3.1 is exchanged with a PI controller for a controllable noise shaping performance. PI controllers naturally put the design flexibility on the integration controller parameter (K_I) and the proportional controller parameter (K_P) with a trade-off between the noise performance and the stability. In general sensors with low quality factor have better stability margins. Thus, PI controller is a better choice for increasing noise performance with a stable, and damped sensor.

The observed noise level is $-115\text{dB}/\sqrt{\text{Hz}}$, which is equal to $1.674 \mu\text{g}/\sqrt{\text{Hz}}$ white noise in addition to sensor noise. Final noise performance of the system can be calculated as $4.9 \mu\text{g}/\sqrt{\text{Hz}}$. Note that the resulting noise value is pretty close to Brownian noise value of the previous accelerometer sensor. Therefore, it is convenient to state that the mixed signal readout system in that thesis can be used for the sensor types with low quality factor easily.

Using the exact same configuration that produces 62.2-degree phase margin in the previous work, the output PSD plot without Brownian noise is depicted in Figure 3.24. Although the noise performance of the system not optimized for the mixed signal system presented in this work, the results are satisfactory for a system aiming for the noise performance below inherent noise of the sensor. The total system noise in the previous work was estimated as $5.3 \mu\text{g}/\sqrt{\text{Hz}}$.

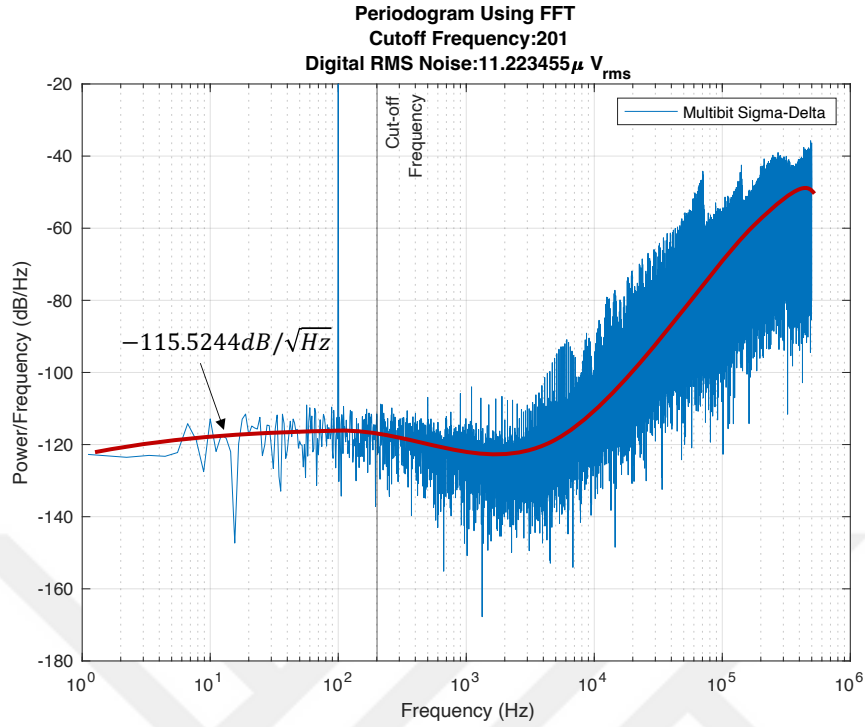


Figure 3.24: PSD plot of the mixed signal loop reconstructed system output using the analysis in [28] with parameter configuration $K_P=1$ and $K_I=4500$ exhibiting approximately $4.9 \mu\text{g}/\sqrt{\text{Hz}}$ total system noise which is lower than the previous implementation exhibiting $5.3 \mu\text{g}/\sqrt{\text{Hz}}$.

The significant point in the optimization of the design for PI controller-based loop filter is the selection of integration controller parameter selection. Increasing the parameter excessively leads to unstable design and amplified electronic noise. That is why there is a parameter optimization problem for quantization noise performance and electronic noise performance trade-off. Note that mixed signal loop filter does not produce extra noise source as electronically implemented PI controller which was reported as one of the dominant sources in [43].

3.6 Summary of the Chapter

This chapter investigates a detailed model of the loop and possible error sources using linear and non-linear behavioral models to facilitate the reasoning. Firstly, accelerometer sensor non-linearity sources are defined and modelled. Under non-

ideal conditions, the scale of errors and their extraction is formulized with typical sensor equations. An essential effect due to the feedback mechanism referred to as the spring softening effect is identified. Its impact on the system is measured for both noise and non-linearity. Detailed linearity performance simulation measurement is performed using a detailed Simulink model of the system. After that, the stability concept is introduced, and a possible loop filter is examined with different parameters for the reasoning of the design. Overall system step response of the model is verified with both calculations and simulation. Finally, noise sources are introduced and decomposed with equations. Limitations due to those noise sources are examined and formulated. As a result, the final noise is simulated and observed with PSD simulation performed in the non-linear Simulink model.



CHAPTER 4

READOUT SYSTEM IMPLEMENTATION

This chapter introduces the system at the top level in terms of the aspects of design purposes. Initially, the system is introduced, and the ROIC-FPGA interface is basically defined. Then ROIC circuit is given at the top level to describe the functionality with implementation. Section 4.1 describes the detailed design process for sub-blocks such as front-end circuit, PGA and Zoom ADC. Finally, Section 4.2 presents the top-level design, including digitally implemented modules.

The primary purpose of this thesis work is to design a system consisting of highly programmable modules to be compatible with various MEMS capacitive accelerometer sensors. The loop filter is fully adjustable because it is implemented inside Field Programmable Gate Array (FPGA) as a Verilog module, as shown in Figure 4.1.

The system design should be utilized according to the mechanical parameters of the MEMS capacitive accelerometer sensor. For example, damped sensors are easier to keep stable, so a PI controller is a more suitable choice for those types of sensors. On the other hand, high Q factor sensors are harder to control, so basically compensator design for a loop filter might be suitable.

There are lots of trade-offs between performance specifications. Mostly noise shaping performance coincides with the stability parameter; the same can also hold for linearity and stability. System trade-offs show the best performance in optimum solution peaks, or the system fails to give the best performance due to unexpected pitfalls. Therefore, system-level design parameters should be very flexible for the best optimization.

To fulfil the primary performance specifications, Readout Integrated Circuit (ROIC) and FPGA blocks are used as hardware blocks. ROIC circuit is not enough itself to

digitize the data for delta-sigma modulator readouts with single-bit quantizers. The reason behind that is the noise shaping and implementation of the system as a modulator. The decimation filter is a complex module, and digital employment on the ROIC module would cause resolution loss since, for aggressive noise shaping, a sharp digital low pass is required, which consumes too many sources on die area and power. Besides, FPGA offers sufficient blocks to build a very complex digital system. Therefore, designing a system limiting the performance due to lack of digital sources on FPGA rather than ROIC die area promises a better bitwise resolution.

Figure 4.1 illustrates the system-level design, which can be decomposed into two main blocks, which are FPGA or any microprocessor module compatible with the ASIC design and digital interfaces and the main ASIC block, which is sometimes referred to as ROIC.

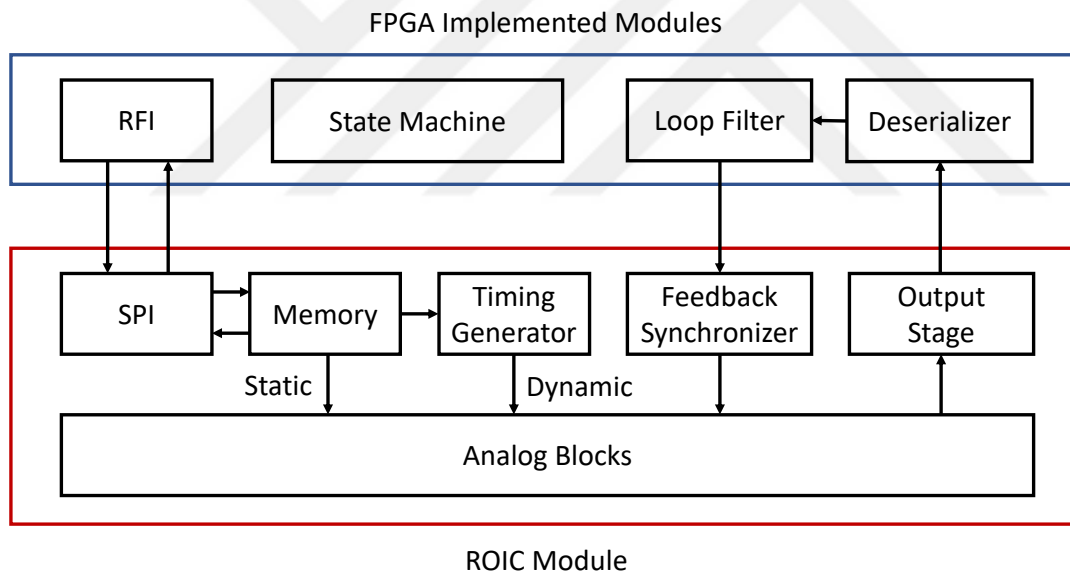


Figure 4.1: Overall functional system diagram.

ROIC circuit mainly picks off the necessary sensor data and then sends it to the leading digital block as data packets. The interface that transmits data packages to the FPGA module and operates at the system clock rate of 50 MHz. FPGA module receives the data package from the ROIC with the phase shifted clock as it is launched with synchronization signal data valid (dval). The system clock is

generated inside the FPGA module from the inherited Phase Locked Loop (PLL) module preventing the system from the errors stemming from high clock jitter or skew.

4.1 Readout Integrated Circuit Design

Figure 4.2 demonstrates the general architecture of the ROIC design for the intended application. The front-end circuit converts the differential capacitance due to external acceleration to voltage utilizing low noise circuitry. Note that the front-end circuitry refers to (C2V) capacitance to the voltage converter module in the functional block diagram. In the signal path, the following analog module PGA is used to drive the Zoom stage and map the voltage according to the voltage range of the ADC module. Finally, data conversion is realized for early digitalization before the output stage. The zoom stage consists of blocks SAR ADC and sigma-delta modulator for the high-resolution conversion.

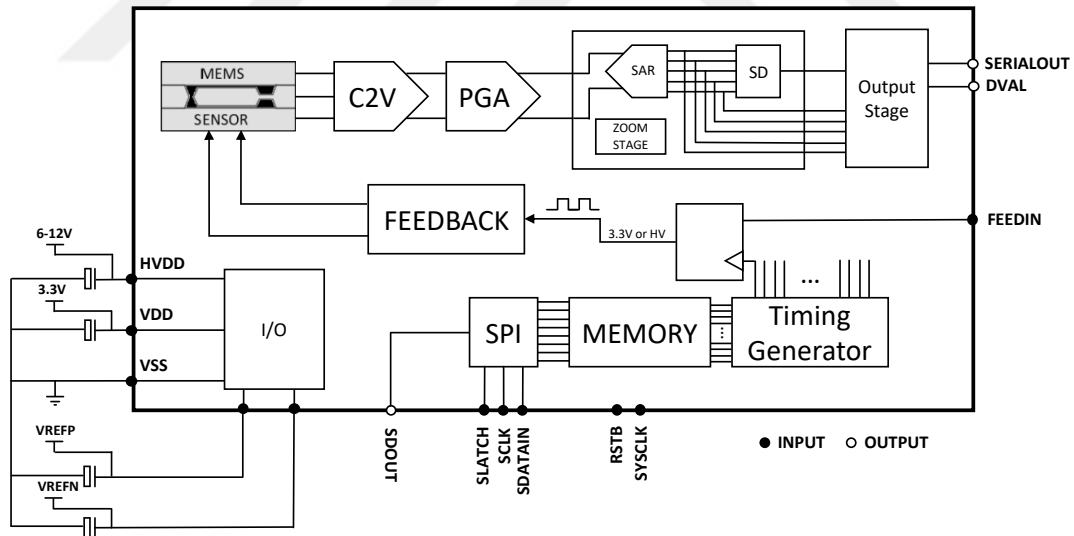


Figure 4.2: Readout Integrated Circuit (ROIC) electronic system level blocks.

Two modules directly communicate with the digital module, which are the digital controller and high voltage level shifting latch module to convert bitstream from FPGA to feedback voltage on the front-end circuitry with the right timing.

The digital controller module consists of an SPI module, memory module and timing generator module for management of the ASIC configurations. ROIC digital is controlled with static memory consisting of words to drive structure inside the ASIC. Memory read and write operation is conducted by slave SPI module implementation. Note that SPI allows real-time configuration changes inside ASIC. That means the configuration of the chip, such as dynamic range, power consumption and resolution, can be changed in a concise duration depending on the SPI clock resolution, which has a default value of 10 MHz clock rate in Silicon proven previous designs.

Furthermore, a bias generator is implemented inside the I/O block, generating the necessary voltage and current values in sufficient conditions to run the overall analog system inside ROIC. In turn, the bias generator requires supply voltages from regulators out of the chip.

4.1.1 Front-End Circuit Design

The front-end circuit of the readout circuitry is one of the primary elements of the overall readout system. Previously, the module was simply modelled as a discrete-time capacitance to voltage amplifier. On the other hand, front-end circuitry also utilizes a force feedback mechanism with the adjustments on the switched capacitor architecture.

The design implementation is realized with a fully differential architecture. Differential architectures are superior to single-ended architectures for the following reasons [45]:

- A higher common mode rejection ratio leads to lower switch artifacts
- Two times voltage swing leading to higher OTA linearity
- Lower supply noise due to higher supply noise rejection
- Lower offset values or less systematic errors

Along with differential architecture, Correlated Double Sampling (CDS) technique mitigates offset due to OTA transistor mismatches, capacitor mismatches, reducing $1/f$ noise. The method can also be referred to as auto-zeroing.

Figure 4.3 demonstrates the schematic of the front-end amplifier used for charge sensing with reference capacitors denoted as C_{R1} and C_{R2} , sensing capacitances C_{S1} and C_{S2} , fully differential OTA, CDS capacitances, integration capacitances denoted as C_{int} and CMOS switches with phase labels.

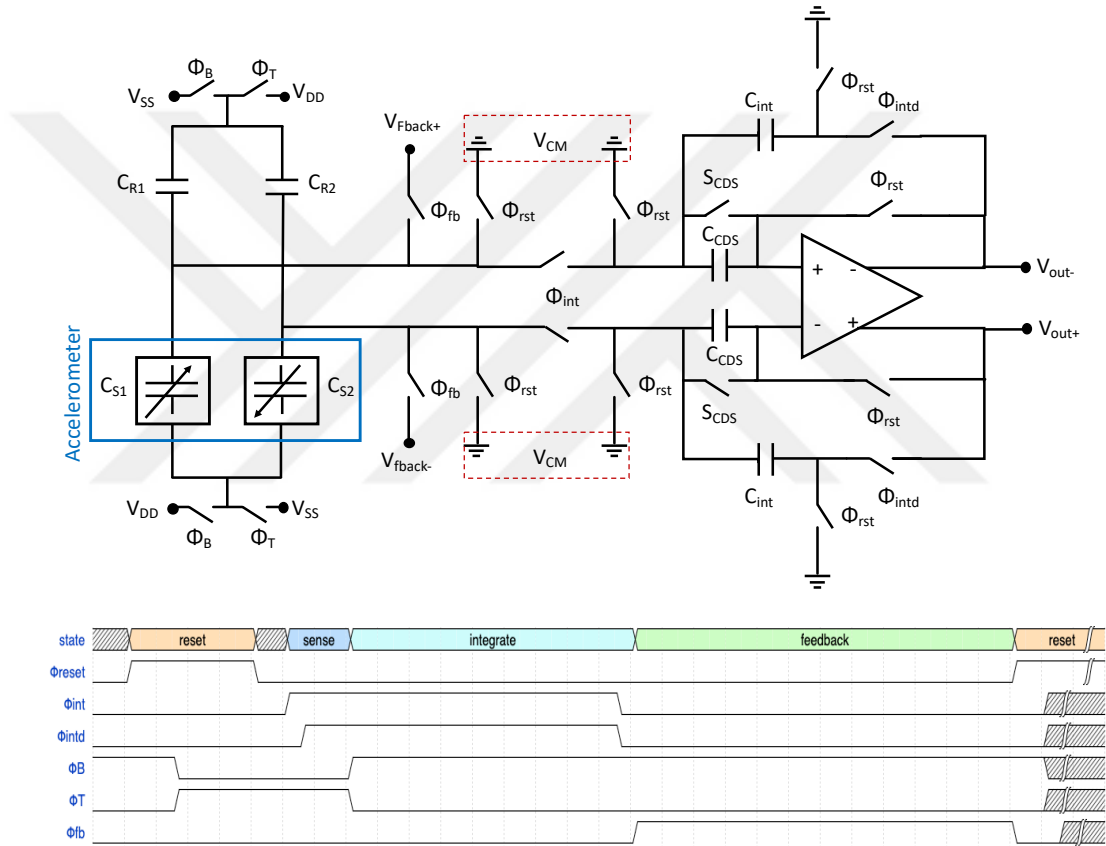


Figure 4.3: Switched capacitor fully differential front-end amplifier with CDS.

The circuit mainly has two sides due to feedback utilization: the high and low voltage sides. The left-hand side of the integration switches is labelled as ϕ_{int} has high voltage modules to allow higher dynamic range and less electronic noise contribution to the system. The right-hand side of the circuit is regular transistors that do not require special attention. However, timing should be carefully adjusted to protect

transistors from a breakdown. In addition, CDS capacitance switches labelled as S_{cds} are static switches to be used for testing the CDS capacitance effect on the overall system performance.

The timing diagram of the front-end circuitry is also shown in Figure 4.3 with decomposition into 3 phases. Those phases are reset, integration and feedback.

During the reset phase, capacitors on the left-hand side are charged to common mode voltages, and CDS capacitances are charged to offset error of the OTA while it is in unity gain configuration. Note that the offset error of the amplifier charges the CDS capacitor with respect to common mode voltage while the bottom plate is connected to common mode voltage. The main concern in this phase is the parasitic effects and unsettled differential voltage leading to residues after the feedback phase. The voltage residues during feedback may lead to random oscillations if not mitigated in this phase.

The second phase is the charge redistribution phase which can also be denoted as the integration phase. During that phase, precharged capacitances at the left-hand side are connected via turned on ϕ_{int} switch. While integrating the differential charge on the integration capacitances, bottom plate voltages of the accelerometer capacitances are set to reversed supply voltage for pushing differential charge onto the integration capacitors. The final phase is the feedback phase. During that phase, all switches are turned off except ϕ_{fb} switches. According to the feedback latch decision, connected supply nodes of ϕ_{fb} are shorted to positive high voltage or negative high voltage.

Charge conservation and charge distribution between phase changes are considered to interpret the operation in detail. For simplicity, the feedback phase is ignored in the first place. The total charge on the capacitors connected to the integration switch node at the left-hand side integration node can be shown as in Equation 4.1:

$$\begin{aligned} Q_{intl-} \left(nT_s - \frac{T_s}{2} \right) &= (V_{cm} - V_{DD})C_{S2} + (V_{cm} - V_{SS})C_{R2}, \\ Q_{intl+} \left(nT_s - \frac{T_s}{2} \right) &= (V_{cm} - V_{DD})C_{S1} + (V_{cm} - V_{SS})C_{R1} \end{aligned} \quad (4.1)$$

The right-hand side of the integration node has the total charge in the reset phase as in Equation 4.2:

$$\begin{aligned} Q_{intr-} \left(nT_s - \frac{T_s}{2} \right) &= \varepsilon \cdot C_{CDS}, \\ Q_{intr+} \left(nT_s - \frac{T_s}{2} \right) &= (\varepsilon + V_n + V_{off}) \left(\frac{A}{A+1} \right) C_{CDS} \end{aligned} \quad (4.2)$$

where, ε is settling error or steady-state error stemming from common mode feedback of OTA during reset phase on the CDS capacitance, V_n is a low-frequency noise component, V_{off} is the amplifier's offset, and A is the gain of the OTA. Considering the sampling frequency and autozeroing; gain nonlinearity and offset voltage differences on the CDS capacitances can be ignored. In addition, if the CDS capacitance is sufficiently large, then the impedance of the CDS capacitance can be ignored, resulting with the assumption that the charge on the CDS capacitance will not change in the integration phase.

Equations 4.3-4.4 can be calculated for formulating the final charge equation at the integration phase using the assumptions and total charge distributed at the capacitances. Note that reference capacitances are chosen equal and denoted as C_R .

$$\begin{aligned} Q_{int-}(nT_s) &= C_R \left(V_- - V_{DD} + V_{err}(nT_s) - V_{err} \left(\frac{nT_s}{2} \right) \right) \\ &\quad + C_{S2} \left(V_- - V_{SS} + V_{err}(nT_s) - V_{err} \left(\frac{nT_s}{2} \right) \right) + \\ &\quad C_{int}(V_- - V_{out+} + V_{err}(nT_s) - V_{err} \left(\frac{nT_s}{2} \right)) \end{aligned} \quad (4.3)$$

$$\begin{aligned} Q_{int+}(nT_s) &= C_R \left(V_+ - V_{DD} + V_{err}(nT_s) - V_{err} \left(\frac{nT_s}{2} \right) \right) \\ &\quad + C_{S1} \left(V_+ - V_{SS} + V_{err}(nT_s) - V_{err} \left(\frac{nT_s}{2} \right) \right) + \\ &\quad C_{int}(V_+ - V_{out-} + V_{err}(nT_s) - V_{err} \left(\frac{nT_s}{2} \right)) \end{aligned} \quad (4.4)$$

where, V_+ , V_- are the positive and negative nodes of the OTA input and V_{err} is any noise signal that is sampled during the charge redistribution. Assuming OTA gain is

sufficiently large, V_+ and V_- can be simply accepted to be equal and denoted as V_{int} which refers to the node as the integration node. Finally, combining Equations 4.1-4.4, output voltages can be calculated using the charge conservation principle on the integration nodes as in Equation 4.5:

$$V_{out+}(nT_s) - V_{out-}(nT_s) = \frac{(V_{int} - V_{cm})(C_{S2} - C_{S1}) + (V_{DD} - V_{SS})(C_{S2} - C_{S1}) + 2V_{err}(\frac{C_{S2} + C_{S1}}{2} + C_R + C_{int})}{C_{int}} \quad (4.5)$$

where, notation $V_{err} = V_{err}(nT_s) - V_{err}(\frac{nT_s}{2})$. Note that V_{int} term can be calculated using the charge conservation in the reset phase where switches ϕ_B and ϕ_T set the voltage as in the Equation 4.6:

$$V_{int} = V_{cm} + \frac{(C_R - \frac{C_{S2} + C_{S1}}{2})}{(C_R + C_{int} + \frac{C_{S2} + C_{S1}}{2})} (V_{DD} - V_{SS}) \quad (4.6)$$

Using Equations 4.5-4.6, the errorless output is expressed as the following Equation 4.7:

$$\Delta V_{out} = (V_{DD} - V_{SS}) \frac{\Delta C}{C_{int}} \quad (4.7)$$

where ΔC is the differential capacitance difference between sensor capacitances. However, error sources result from the reference capacitance difference from the average of sensing capacitance and differential noise coupled through the circuitry, which can also result from parasitic couplings on the sensor itself. In addition, the layout of the high voltage modules is prone to parasitic coupling due to large transistors with thick oxide modules. Using Equation 4.5, Equation 4.8 represents the error transfer function from integration node to differential output voltage:

$$H_{err}(z) = \frac{2 \left(\frac{C_{S2} + C_{S1}}{2} + C_R + C_{int} \right)}{C_{int}} (1 - z^{-\frac{1}{2}}) \quad (4.8)$$

The spectral response of the noise coupled with the integration noise is depicted in Figure 4.4. The noise gain is quite low, showing an offset correction behavior. The error source can include the offset and Flicker noises as well. That shows offset, and low-frequency 1/f noise is attenuated thanks to the CDS technique. Considering $z = e^{j2\pi \cdot 1/1M}$, $|H_{err}(j\omega)|$ is close to zero. However, decreasing the integration capacitance to obtain higher gain from the front-end stage degrades that shaping behavior, leading to higher noise levels. Therefore, there is a trade-off between gain and low frequency noise. To handle that trade-off more sufficiently, the PGA module was necessary. Front-end circuitry allows the selection of 500f to 15.5pF integration capacitance to stay in the optimized performance valley according to defined limitations.

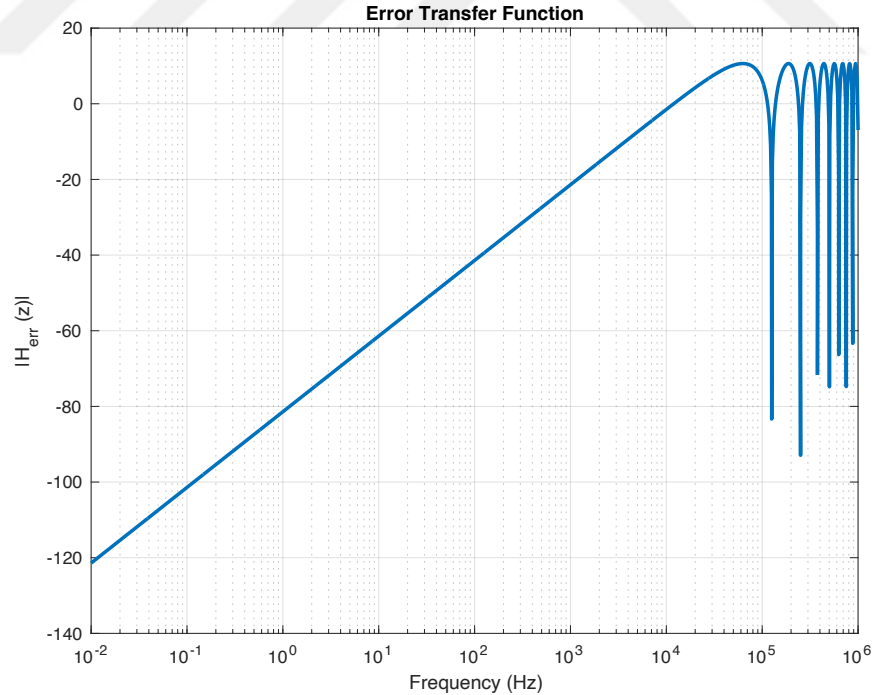


Figure 4.4: Spectral response of the noise in the circuit using Equation 4.8.

4.1.1.1 Operational Transconductance Amplifier (OTA) Design

OTA is the primary block utilized in almost every stage of the analog blocks inside ASIC governing the main optimization parameters. Switched capacitor circuits are well integrated with OTAs rather than OPAMPs due to relaxed output impedance and convenience with capacitive loads that directly determine the voltage. Therefore, the design specifications should be chosen carefully to optimize transistor parameters.

ROIC consists of blocks front-end amplifier, programmable gain amplifier (PGA) and Zoom stage delta-sigma modulator integrator OTAs. Each has different but similar specifications due to their employed tasks.

The front-end amplifier needs to be a low-noise design. In the previous chapter, the spring softening effect and noise shaping concepts of electronic noise were discussed. Due to the trade-off between stability and noise transfer function of electronic noise, the electronic noise could not be mitigated completely as in the previous works [28] and [43]. Therefore, a low noise design is safer for a high gain case of PGA as the following block after front-end circuitry. Furthermore, front-end circuitry output swing is a limited voltage range even though the gain is maximized by keeping integration capacitance at minimum configuration.

On the other hand, the PGA block needs to have a high output swing and higher linearity. Even though a higher swing can be obtained from architectures such as folded cascode amplifiers, the ADC input range can also be limited by setting reference voltages to prevent any non-linearity due to the output swing of PGA OTA.

Zoom stage OTAs have a minimal output range, and the first integrator OTA design is critical. Noise is an essential concern for the first integrator, but the second integrator's OTA design is very relaxed, as explained in the Zoom ADC section.

The front-end amplifier must have both low noise and a high slew rate. The slew rate of the front-end pick-off circuitry is the primary limitation and coincides with the

The OTA architecture can be easily compared with another low-noise architecture, the telescopic amplifier. For a telescopic amplifier, let's assume that input transistors are selected as $M_{1,2}$ and $M_{7,8}$ are biased with another bias voltage. The input referred noise expression of the telescopic modified circuit referring to [46] in Figure 4.5 can be shown as in Equation 4.9:

$$V_n^2 = 4kT \left(2 \frac{\gamma}{g_{m1,2}} + 2 \frac{\gamma g_{m7,8}}{g_{m1,2}^2} \right) + 2 \frac{K_N}{(WL)_{1,2} C_{ox} f} + 2 \frac{K_P}{(WL)_{7,8} C_{ox} f} \frac{g_{m7,8}^2}{g_{m1,2}^2} \quad (4.9)$$

Noise sources of a telescopic amplifier are dominated by the thermal noises of transistors $M_{1,2}$ and $M_{7,8}$ and flicker noise sources. However, the flicker noise contribution of loading transistors is smaller than the input transistors by a factor proportional to the transconductance ratio. Note that, at low frequencies, cascode devices' noise contributions can be assumed to be sufficiently small due to source degeneration. The inverter-based amplifier depicted in Figure 4.5 has the input-referred noise expression from [47] as in Equation 4.10:

$$V_n^2 = \frac{8kT\gamma}{g_{m1,2} + g_{m7,8}} + 2 \frac{K_N}{(WL)_{1,2} C_{ox} f} + 2 \frac{K_P}{(WL)_{7,8} C_{ox} f} \quad (4.10)$$

It is evident that inverter-based cascode OTA design has considerably small input referred noise expression according to Equation 4.10. The excess noise factor is less than one because all the transistors in the inverter take place in both gain and noise expressions. On the other hand, load transistors at the telescopic OTA only contribute to the noise expression. However, the Flicker noise of the inverter-based amplifier is higher than the telescopic amplifier. Notice that the front-end circuitry introduces the CDS technique that attenuates offset and low-frequency noise in the baseband.

Another concern about OTA design is the settling time. The driving characteristic of the inverter-based design works like a class-AB output stage, so the slew rate is enhanced with the current design topology. On the other hand, the settling time of

the switched capacitor amplifier is another issue determining the actual settling. For the given front-end design, the reset phase time constant can be calculated in terms of circuit parameters referring to [46] as in Equation 4.11:

$$\tau_{reset} = (R_{on,rst} + 1/G_m)C_{CDS} \quad (4.11)$$

R_{on} resistance of the rest switch of the amplifier, which is sampling the offset of the amplifier, can be taken as zero, yielding total dependence on the transconductance of the amplifier itself. Notice that the reset phase is not the dominant phase limiting the sampling speed of the front-end circuit. The dominant time constant limiting the sampling speed is the integration time constant which is given in Equation 4.12:

$$\tau_{int} = \frac{C_L(C_{s1,2} + C_R) + C_{int}(C_{s1,2} + C_R) + C_L C_{int}}{G_m C_{int}} \quad (4.12)$$

According to the expression derived for the time constant of the settling time in the integration phase, the transconductance of the amplifier OTA must be sufficiently high for a 1 MHz sampling rate. Notice that load capacitance is denoted as C_L , the transconductance of the amplifier is marked as G_m and summation of $C_{s1,2}$, and C_R refers to the input capacitance load to be driven during the integration phase. CDS capacitances contribute to the settling time of the system as well. If CDS capacitances are not large enough, then the front-end readout circuit confronts settling errors due to high impedance through the input nodes of the differential amplifier. Therefore, CDS capacitance should be selected close to OTA input transistors' gate capacitances.

On the OTA circuitry, there is another issue that needs to be resolved to get the highest performance: biasing and common mode feedback circuitry. Biasing is performed using a replica biasing method where the current is copied with the transistors ratioed according to input and cascode transistors in the amplifier. That

way, the bias scheme also generates a sample bias voltage for setting the common mode voltage of the amplifier for the output node.

A common mode circuit is crucial for fully differential due to errors resulting from mismatches and transistor parameter deviations over a period of time. Hence, those effects can appear at the output of the amplifier as an amplified abnormality or deflection from the original value. Notice that those variations may also limit the input range due to the reduction of the well yielding a degraded linear dynamic range. Thus, common mode feedback (CMFB) should be utilized to stabilize by sensing the variations at the output and then generating negative feedback to set the output amplifier via a bias voltage setting.

There are two types of feedback topologies of common mode feedback circuitry: continuous common mode feedback and discrete (switched capacitor) common mode feedback. Continuous CMFB topologies are mostly preferred for high-speed applications and continuous-time analog topologies. However, continuous CMFB introduces extra poles to the circuit, which has an inherited loop that needs to be stabilized. Otherwise, the implemented amplifier may oscillate due to overshooting biasing as negative feedback. Furthermore, continuous CMFB topologies require extra biasing circuits and extra power consumption. Therefore, switched capacitor CMFB topology is preferred, which is low power and does not require an additional biasing scheme. On the other hand, they have a loading effect on the OTA, but it is low enough that the current drained due to that loading is minimal comparing the main load.

Figure 4.6 demonstrates the circuitry implemented to the front-end OTA circuitry. According to the schematic, it is evident that there are two phases. In the first phase, the OTA output nodes, denoted as V_{outp} and V_{outn} , are solely connected to C_2 capacitances via ϕ_2 switches and C_1 capacitances are precharged to the intended voltage difference that common mode feedback needs to settle. During the second phase, a pathological case is formed for charge sharing between capacitors C_1 and C_2 . In this phase, the common mode voltage at the output converges one step further

to the ideal common mode voltage denoted as V_{cmref} . In each sampling cycle, the output common voltage gets closer to the given circuitry showing an overdamped response while settling. As a rule of thumb, the ratio of the capacitances C_1 and C_2 are selected in the range of 1/4 to 1/10 [48].

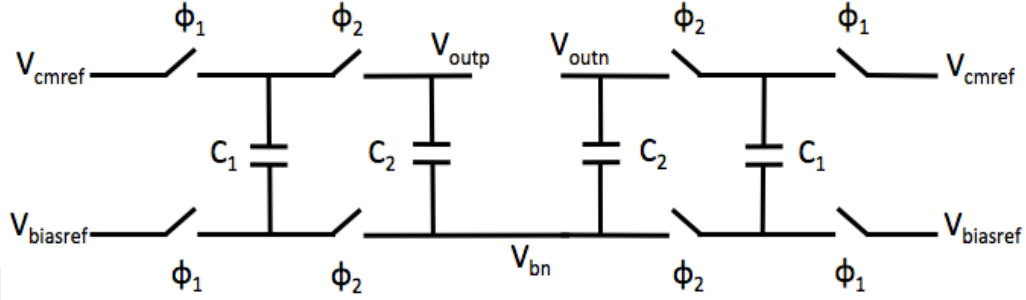


Figure 4.6: Switched capacitor common mode feedback schematic implemented to this work from [28].

Note that switches are denoted as ϕ_1 and ϕ_2 are complements of each other, constituting the transitions between timing phases. Between each phase transition, the bias voltage on the n-tail current source takes a hit that may lead to minor ripple errors due to parasitics. To reduce that effect to minimum, the common mode feedback tail current is separated into the dynamic and static current mirror to enhance the phase margin, as shown in Figure 4.5.

Figure 4.7 shows the ac response of the OTA, which has two poles that needs a careful design for stability. In general, for noise and gain concerns, input transistor transconductance is set to higher values until power consumption due to the loading effect limiting the performance and transistor sizes exceeding the limit on the die area. On the other hand, cascode transistors have a relatively less transconductance value, but it has a limitation due to both gain and stability concerns. The high-frequency pole of the OTA originates from the node between the input and cascode transistors. To increase the frequency of the second pole, cascode transistor transconductance can be increased up to an optimum point where overlap capacitance leads to the pole frequency.

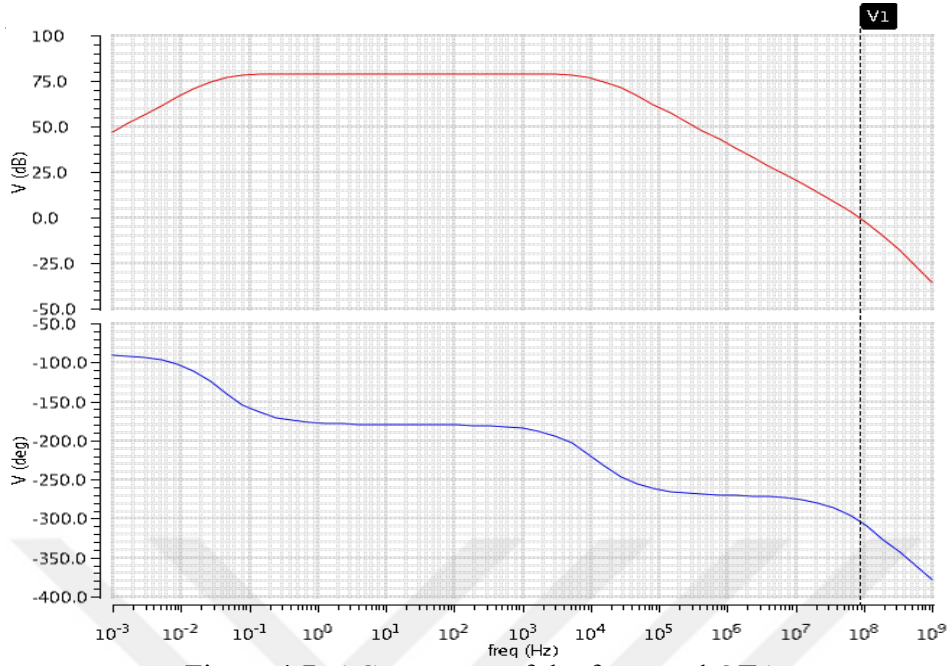


Figure 4.7: AC response of the front-end OTA.

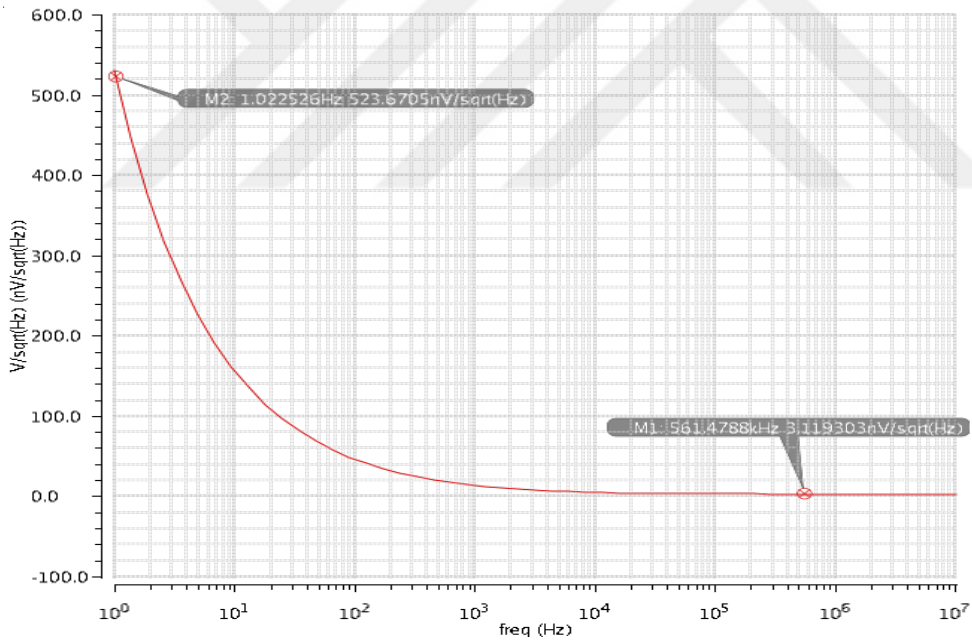


Figure 4.8: Noise simulation of the front-end OTA.

Figure 4.8 depicts the noise simulation of the front-end OTA while it operates in the integration phase. Flicker noise appears to be in the $500\text{nV}/\sqrt{\text{Hz}}$ level. However, as mentioned in the previous section, CDS capacitances reduce the noise up to thermal noise levels. Thermal noise level is observed close to $3\text{nV}/\sqrt{\text{Hz}}$, which is well below

the specification. Transient noise simulations measures $750\ \mu V$ peak to peak deviation from the calculated output voltage, which approximately corresponds to $113\text{nV}/\sqrt{\text{Hz}}$ white noise in the 1 Hz to 1MHz range. Finally, the results are shared in Table 4.1.

Table 4.1: OTA performance parameters of inverter-based amplifier according to simulation results.

Performance Parameter	Value
DC Gain	76dB
Bandwidth (3dB)	42kHz
Unity GBW (at 1pF)	215MHz
Phase Margin	54°
Input Referred Flicker Noise at 1Hz	500 nV/ $\sqrt{\text{Hz}}$
Input Referred Thermal Noise	3 nV/ $\sqrt{\text{Hz}}$
Power Consumption	1mW

4.1.2 Programmable Gain Amplifier (PGA)

The programmable gain amplifier of the system is necessary to map the input voltage produced from the front-end circuitry to the Zoom ADC while adjusting the gain. In addition, PGA can also be interpreted as the buffer for driving the capacitive load of both SAR ADC DAC and the first integrator DAC. Considering the timing of the front-end circuitry, driving the load solely from the front-end OTA causes a design with a higher power consumption, which is not preferred. Also, notice that front-end amplifier voltage values are quantitatively low, yielding a non-complete utilization of the Zoom ADC.

PGA module design has the parasitic insensitive architecture by utilization of bottom plate sampling technique as shown in Figure 4.9 and Figure 4.10. In addition, CDS noise would couple to the integration capacitance if ϕ_{intd1} switches were not implemented. At sampling instant ϕ_{samp} and ϕ_{sampd} , OTA is in unity gain configuration and dislocated from integration capacitance; thus, the $1/f$ noise is only sampled to CDS capacitance. At the same time, the differential input voltage is

sampled to the $C_{s\text{samp}}$ sampling capacitances. During the integration phase (ϕ_{int} and ϕ_{intd}), the output voltage is set to a voltage value determined as in Equation 4.13:

$$V_{\text{out}} = V_{\text{in}} \frac{C_{\text{samp}}}{C_{\text{int}}} \quad (4.13)$$

Integration capacitance is left adjustable to set the optimum voltage multiplication according to loop optimization. The range of integration capacitance can be set from 67pF to 2pF for 1pF sampling capacitance, which leads to approximately a multiplication range from 0.5 to 15. 5-bit capacitance selection enables the digital setting of the gain in the provided range.

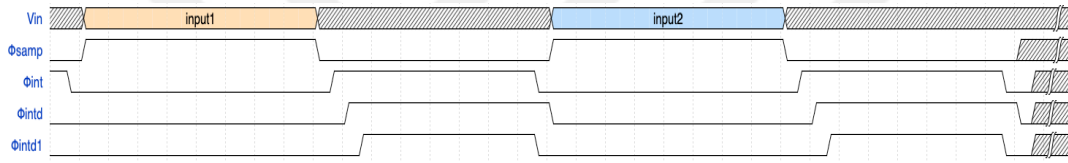


Figure 4.9: Timing diagram of PGA module.

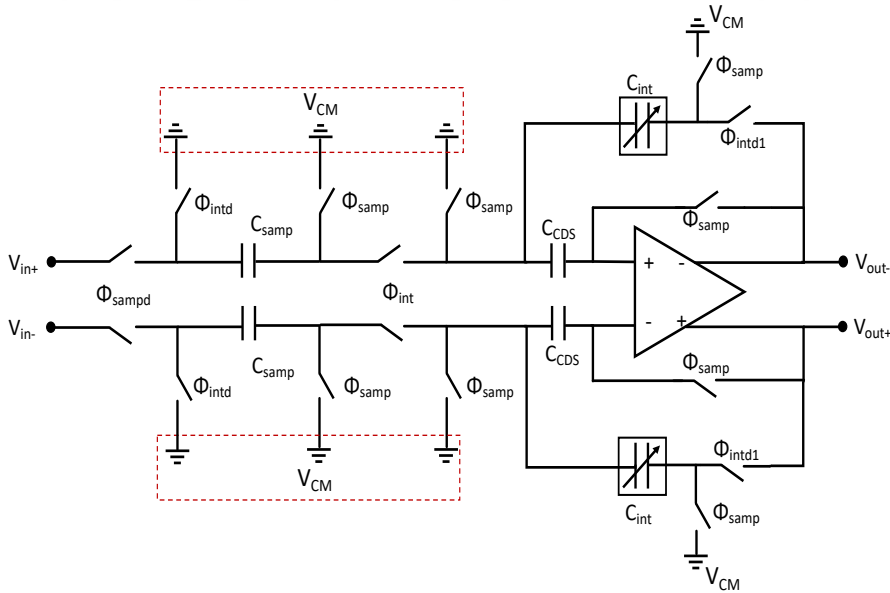


Figure 4.10: PGA schematic implementation.

Cadence enables the simulation features SpectreRF, pss and pnoise. That way, periodic simulations and analysis can be efficiently conducted using Cadence and noise verification can be performed. PGA analysis is compatible with that feature as it is implemented as a discrete (switched capacitor) system. For sufficient precision, simulation parameters maximum ac frequency and maximum sideband are chosen as 100MHz and 20, respectively. In addition, current tolerance, voltage tolerance and analog relative tolerance parameters are selected as 100fA, 1nV and 1μ , respectively. The results of that simulation for that module are given in Figure 4.11.

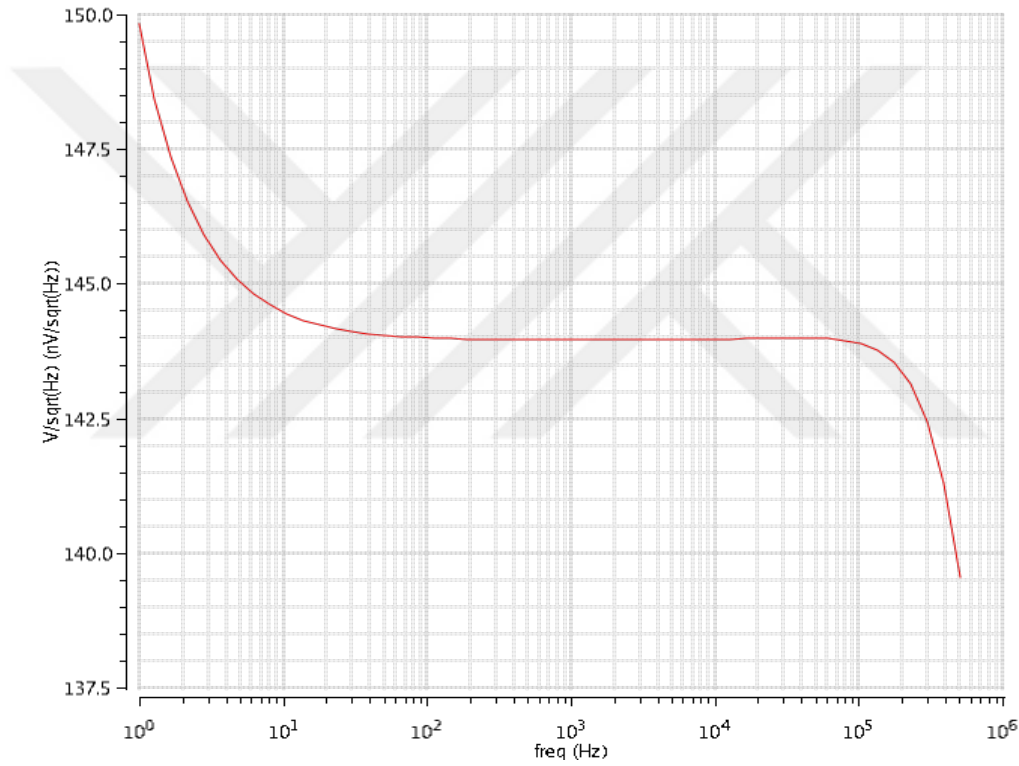


Figure 4.11: PGA pss simulation demonstration of effective auto-zeroing technique application.

Notice that the simulation result is fed back to full system simulation performed in the Simulink environment in addition to front-end circuit noise. According to the results, auto-zeroing reduced the $1/f$ noise below $150 \text{ nV}/\sqrt{\text{Hz}}$. The noise corresponds to a white noise level of -136.4dB, well below the overall noise expectation.

4.1.2.1 OTA Design

PGA module is assigned to drive the DAC loads of SAR ADC and sigma-delta modules in the Zoom stage. The folded cascode OTA implemented into the PGA module should be designed to have a higher linear output swing than the front-end amplifier. The second reason is the convenience to buffer topology. Satisfying those requirements costs moderate power consumption, higher noise, and lower slew rate. Note that, according to results shown in Figure 4.11, noise performance is overwhelmed using folded cascode architecture depicted in Figure 4.12.

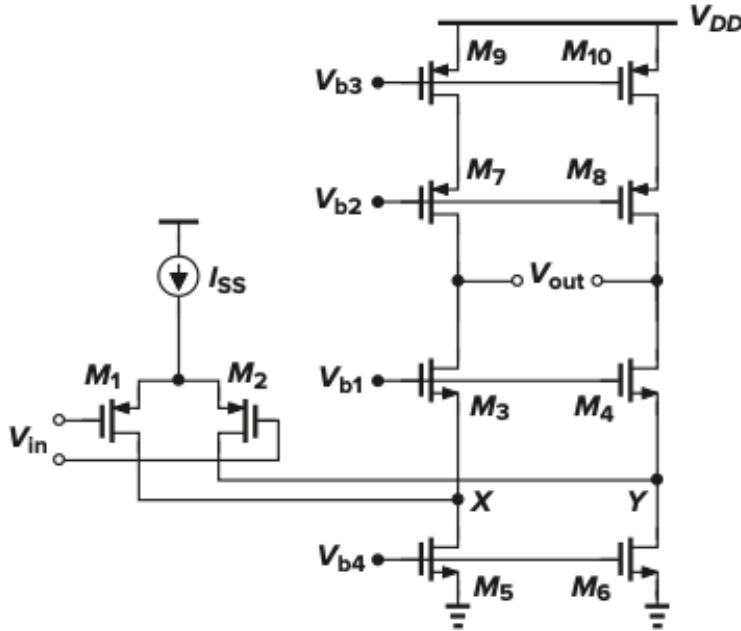


Figure 4.12: Folded cascode OTA design for PGA module retrieved from [46].

The performance parameters of the corresponding design are demonstrated in Table 4.2 and Figure 4.13. The DC gain of the OTA needs to be high in order to preserve the linearity requirements and prevent any harmonic spurs originating from the circuitry. As the capacitive load is large enough, 77° phase margin is achieved. Considering the noise equation provided by the previous section, folded cascode OTA architecture needs to drain higher current from the supply to achieve lower noise performance. That is why the design consumes 2mW power.

Table 4.2: Performance parameters of the folded cascode OTA implemented in this thesis.

Performance Parameter	Value
DC Gain	91dB
Bandwidth (3dB)	2kHz
Unity GBW (at 6.4pF)	65MHz
Phase Margin	77°
Input Referred Flicker Noise at 1Hz (pss)	150 nV/VHz
Input Referred Thermal Noise (pss)	143 nV/VHz
Power Consumption	2mW

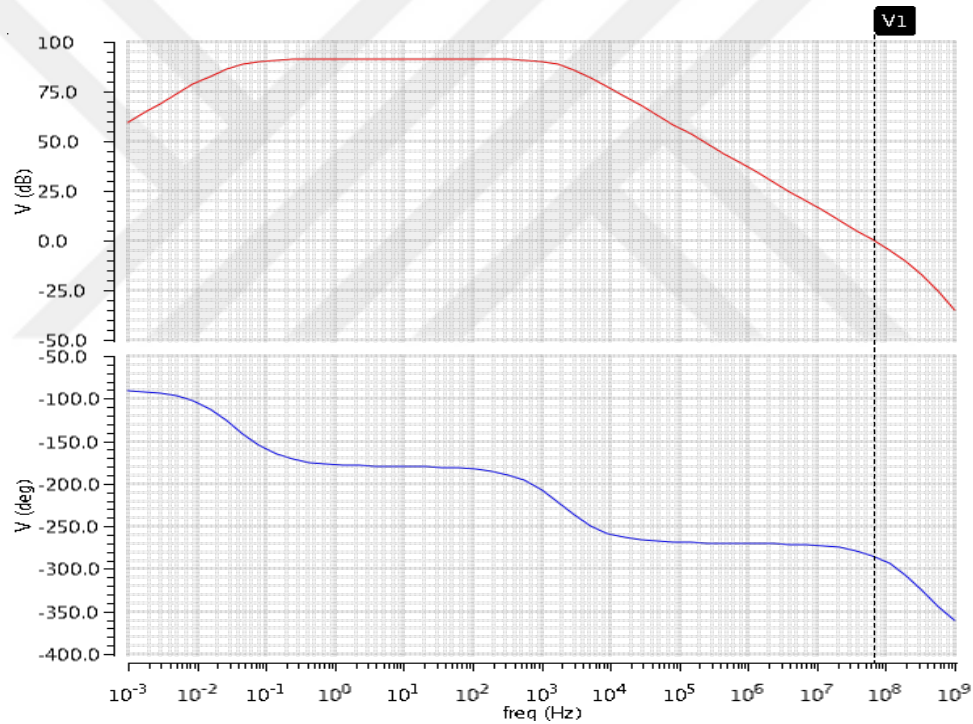


Figure 4.13: AC analysis of the implemented folded cascode OTA for PGA module.

4.1.3 Zoom ADC Design and Implementation

Zoom ADC is one of the core modules of the design as it is the final stage before the digital side of the system. The specifications of the ADC module or high-resolution

modulation and low power implementation. Delta sigma modulator precision is determined by the voltage range that is practiced. Keeping the voltage range brings other design constraints, such as OTA non-linearity issues. In addition, higher input voltage range also leads to a lower resolution. That is why Zoom ADC is chosen as the quantization architecture of the ASIC implementation.

Figure 4.14 shows the system-level integration of Zoom ADC. The top module of the ADC consists of coarse ADC and fine ADC topologies. The system is decomposed into L^{th} order delta-sigma modulator with a sampling rate f_s , N-bit SAR ADC with sampling rate $f_s/8$ and Dynamic Element Matching (DEM) circuit. The primary performance metrics of the Zoom ADC in this work are 120dB SNDR and 300Hz bandwidth leading to optimization of parameters coarse ADC bit resolution N, the sampling frequency of the fine ADC (f_s), over-ranging bit depth (M) and delta-sigma modulator order implemented in the fine ADC.

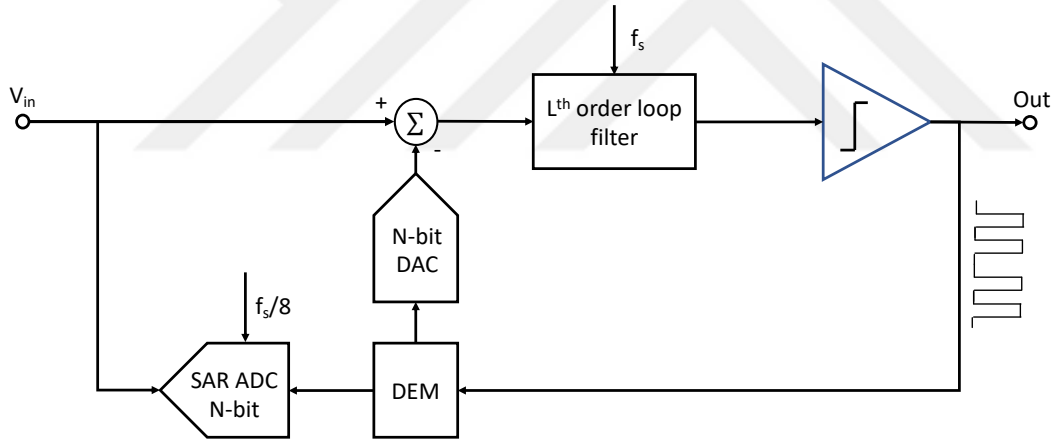


Figure 4.14: Block diagram of Zoom ADC architecture.

Increasing the resolution of the coarse ADC may seem a reasonable option in the first place as it reduces the input swing and relaxes the dynamic range specification of the delta-sigma modulator. However, the number of cycles that ADC completes the conversion increases, which reduces the maximum overall conversion speed. Otherwise, coarse bit conversions might have tracking errors because of a high slew of the input signal that the Coarse ADC cannot handle. Over-ranging concept relaxes that design constraint by enlarging the delta-sigma full-scale range.

Therefore, the final bandwidth limitation of the Zoom ADC can be formulated as in Equation 4.14:

$$f_{in,max} = \frac{\alpha M f_s}{8\pi 2^{N+1}} \quad (4.14)$$

where, α is the proportionality factor of the full-scale covered input. For this thesis, over-ranging (M) is selected as 2 optionally which can also be set to 4 and 8 in the circuitry, sampling frequency (f_s) is 1MHz, bit resolution of coarse ADC (N) is equal to 5 and fraction of input to full-scale voltage range is 0.5 optionally. The resulting bandwidth limitation is calculated according to Equation 4.14 as nearly 622 Hz, which is sufficiently above the designed readout frequency of the system and can be increased in exchange with resolution. Figure 4.15 demonstrates the tracking error concept for a sinusoidal input. The signals denoted as $V_{ref,p}$ and $V_{ref,n}$ correspond to the delta-sigma modulator's upper and lower limits that will determine the high-resolution bitwise output. The over-ranging concept is the selection of upper and lower bounds of the delta-sigma modulator by several steps in the coarse ADC, centering on the result found after the coarse ADC conversion.

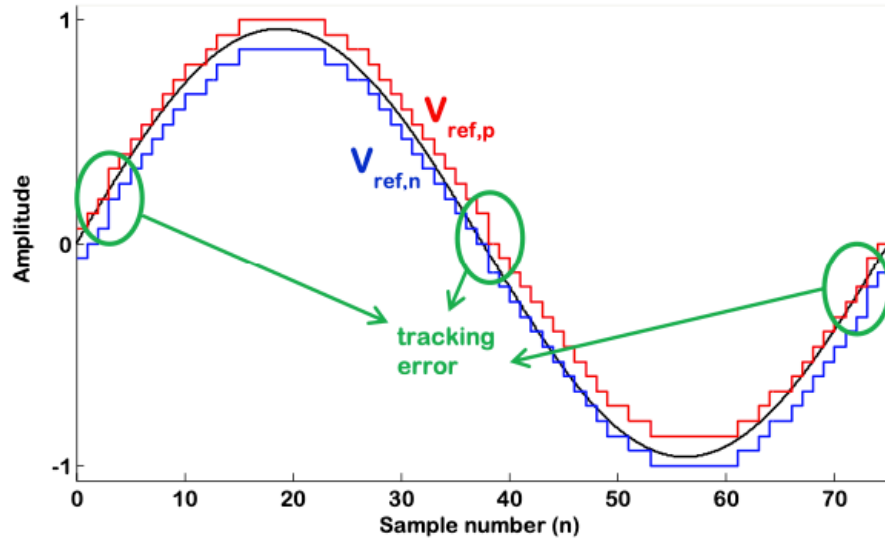


Figure 4.15: Coarse ADC tracking error plot in [49].

Another design optimization of Zoom ADC is based upon the resolution. Blindly increasing the sampling frequency of the system brings resolution and an increase in the maximum input frequency. On the other hand, it costs increased power consumption and design complexity. Clocking the Zoom ADC with a faster clock yields a more complex design and increases the settling time of the PGA considering capacitive load of the ADC, which is not desirable in terms of power consumption.

In the previous chapter, the delta-sigma dynamic range was equated and explained. Fine ADC consists of a delta sigma modulator for higher resolution. The main parameter governing the resolution specification of the ADC is the loop filter order (L) and OSR. Therefore, special care must be taken while selecting the order and setting the OSR accordingly. On the other hand, the Zoom ADC concept is slightly different in terms of resolution calculation. Two new parameters are defined for the system: coarse bit resolution (N) and over-ranging.

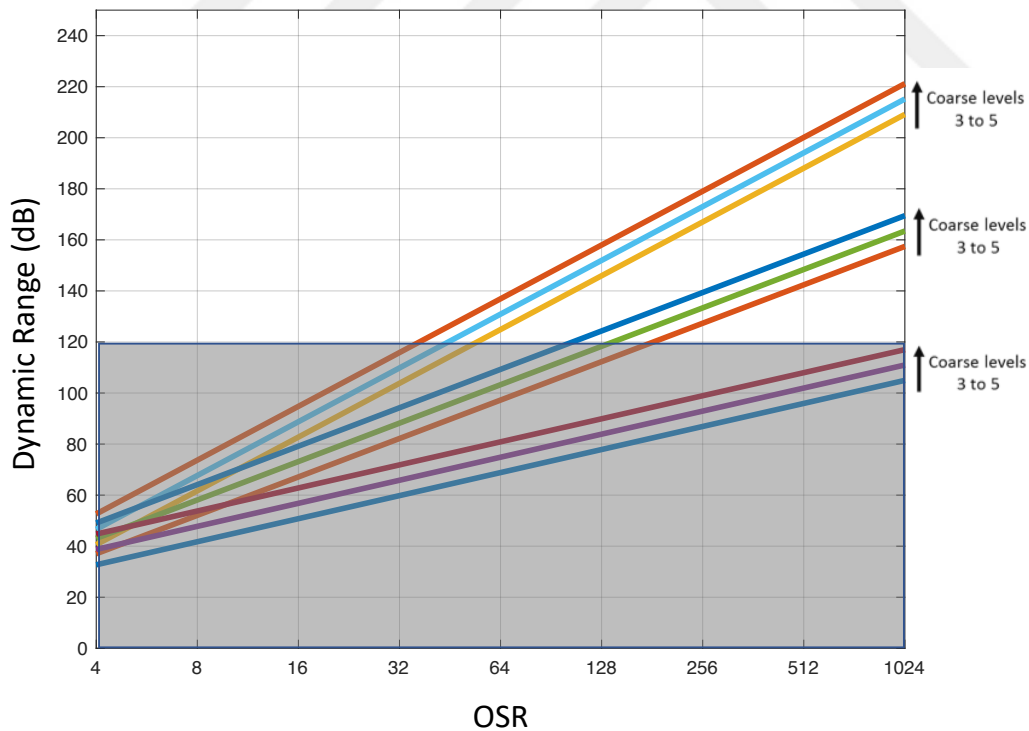


Figure 4.16: Maximum dynamic range calculation plot according to OSR and coarse ADC bit resolution (N).

Figure 4.16 illustrates the parametric approach against Signal to Quantization Noise Ratio (SQNR) based dynamic range calculation. The calculation is based on a linear approximation which is too optimistic. The minimum bandwidth requirement is close to 1kHz, corresponding to an OSR value of 1024. 1 bit increase in the coarse ADC resolution extends the layout area of the chip two times. Therefore, for an acceptable performance without sacrificing too much die area, coarse ADC bit depth is selected as 5 bits.

4.1.3.1 Coarse ADC

Coarse ADC is the initial operating block of the Zoom ADC implementation of this work. SAR ADC is the block that has the most relaxed design constraints. It is a simple yet effective block. Before further quantization, 5-bit SAR ADC divides the full-scale input range into a narrower scope for the delta-sigma modulator. Thanks to the over-ranging concept, the SAR ADC module should not necessarily operate in the same frequency as the fine ADC yielding a lower power consumption on the coarse ADC side.

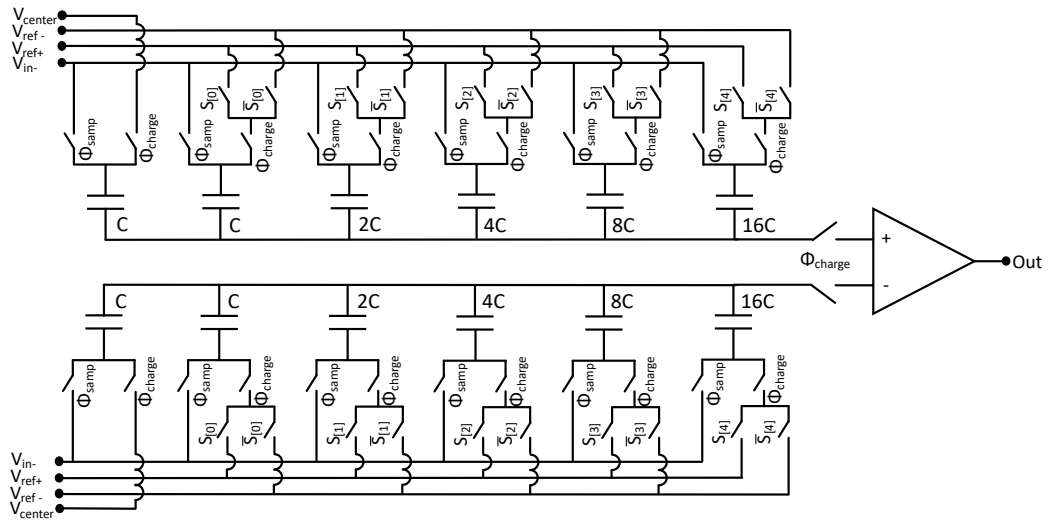


Figure 4.17: SAR ADC DAC and comparator implementation.

Figure 4.17 depicts the coarse ADC implementation consisting of DAC and comparator. SAR logic is given in Figure 4.18. Initially, the input voltage driven by the PGA module is sampled using ϕ_{smp} switches. At the same time, bottom plate capacitors are charged to V_{center} voltage resulting in a differential sampling. Notice that during input sampling operation, logic block output (D[4:0]) is set to (5'b10000) for DAC pre-setting. After the sampling cycle, 5 conversion cycles are performed using the binary search method while the SAR logic is sampling the comparator output. Finally, an end of conversion (EOC) flag is generated, indicating the SAR ADC output is valid. At the rising edge of each EOC flag, sigma-delta samples the SAR ADC digital output and starts the fine conversion.

One of the main design specifications of the SAR ADC is the DAC capacitance selection. For that work, 100fF capacitance achieves desired performance. kT/C noise and possible parasitic charge losses are the limitations of minimum capacitance selection, and power consumption is the limitation of the maximum allowable capacitance selection. During conversion, power does not exceed the $10\mu W$ value, but at each $8\mu s$, PGA has to drive the DAC load. That is why it is bounded to 100fF. Comparator architecture is selected as strong-Arm Latch, which is explained in detail in the Fine ADC section. As mentioned before, coarse ADC requirements are pretty relaxed and direct implementation of strong-Arm Latch does not harm the operation. For coarse ADC, the latch has a 2.34 mV voltage mismatch which is sufficiently low enough for the desired function.

Figure 4.18 depicts the SAR logic circuitry as a sequential implementation. It is an old architecture commonly used in SAR ADC implementations. The most important feature of that architecture is the simplicity that it introduces to the design. There are more complex designs including combinational logics to accelerate the conversion speed. However, the SAR ADC in this thesis has a pretty relaxed conversion speed as well as the resolution requirement.

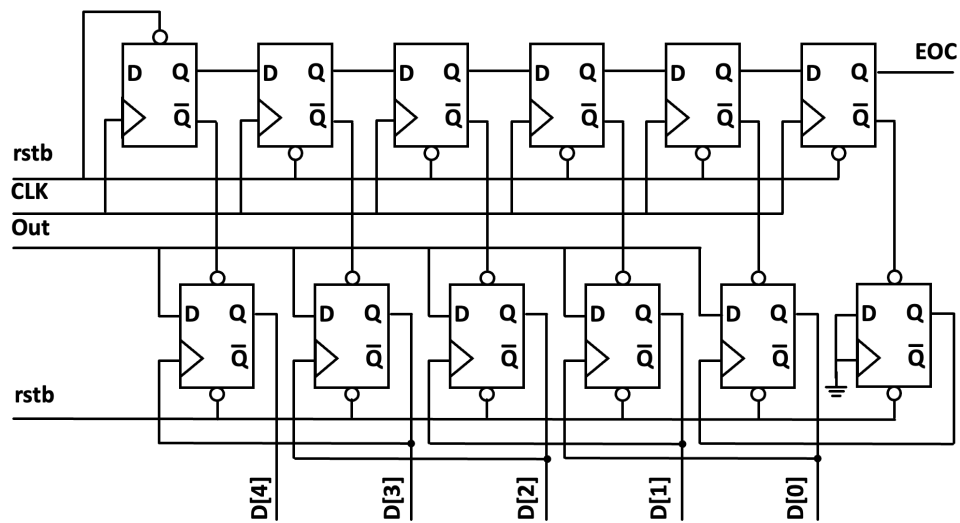


Figure 4.18: SAR logic implementation.

Figure 4.19 illustrates the simplified timing diagram of the SAR ADC implementation. The digital controller of the system manages the timing of the SAR ADC module. However, the timing generator of the digital controller allows only signal generation up to 1MHz for a 50MHz system clock rate. On the other hand, SAR ADC only operates at 8 times the 1MHz clock. That is why another logic based on a ring counter is also implemented in the digital controller. That way, pseudo periodic timing generation is achieved. EOC flag blocks the periodic signals generated for SAR ADC and converts them to the timing map shown in Figure 4.19. Note that the logic clock indicates the clk input of the SAR logic shown in Figure 4.18.

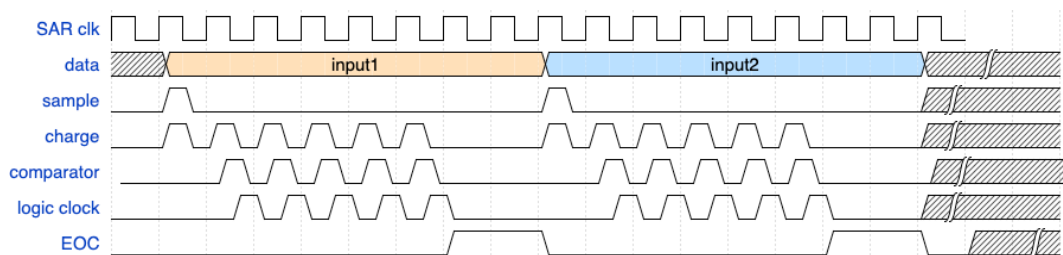


Figure 4.19: Simplified timing of coarse ADC.

4.1.3.2 Fine ADC

Fine ADC is the most critical part of the Zoom ADC. Any performance limitation arises from the design errors of fine ADC. In general, precision ADCs require a noise shaping concept, as explained in Chapter 2. The delta-sigma modulator is the most common architecture that includes the noise shaping concept. The main system consists of a delta sigma modulator already. Therefore, precision within the signal path is kept high resolution through the implementation of a delta-sigma modulator inside fine ADC architecture.

Considering the noise shaping concept introduced in Chapter 2, design of a loop filter is significant for noise shaping. The system-level noise shaper has a leaky integrator corresponding to the accelerometer sensor. On the other hand, electronic loop filter integrators are relatively less leaky and are easier to implement.

Considering the resolution requirements of the system, a second-order loop filter was chosen for convenience. Design loop filter coefficients should be selected meticulously for high pass noise transfer function to prevent total design failure due to stability or performance degradation. The implemented loop filter in Figure 4.20 can be calculated as shown in Equation 4.15:

$$Y(z) = \frac{X(z)a_1a_2k_qz^{-1}}{1 + \frac{a'_1a_2k_qz^{-2}}{(1-z^{-1})^2} + g'_2k_q\frac{z^{-1}}{(1-z^{-1})}} + \frac{E(z)}{1 + \frac{a'_1a_2k_qz^{-2}}{(1-z^{-1})^2} + g'_2k_q\frac{z^{-1}}{(1-z^{-1})}} \quad (4.15)$$

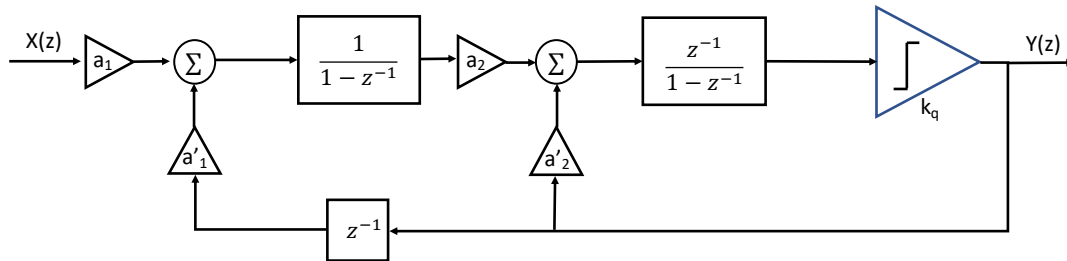


Figure 4.20: Z-domain representation of delta sigma design.

Equation 4.15 represents the output transfer function in terms of the input signal and quantization error signal denoted as $E(z)$. The ideal transfer function of the L^{th} order noise shaping filter was given in Equation 2.15. The corresponding form of the transfer function can be obtained when the conditions on Equation 4.16 are satisfied and leads to Equation 4.17.

$$\begin{aligned} k_q a'_1 a_2 &= 1, \\ k_q a'_2 &= 2 \end{aligned} \quad (4.16)$$

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})^2 E(z) \quad (4.17)$$

Therefore, the coefficients satisfying the conditions given in Equation 4.15 and giving the best circuit optimization for that work are given as in Equation 4.18:

$$\begin{aligned} a_1 &= 4, a'_1 = 4, \\ a_2 &= 0.25, a'_2 = 2, \\ k_q &= 1 \end{aligned} \quad (4.18)$$

The coefficients are adjusted using capacitive ratios of the circuitries given in the following sections.

4.1.3.2.1 First Integrator

The sampling network of the first integrator is designed to match with the DAC in the coarse ADC. The DAC in the first integrator element consists of 32-unit elements as sampling capacitances, as shown in Figure 4.21. The primary purpose of that switching is extracting the quantization error of the coarse ADC, integrating the first block of the noise shaping block, which is the first integrator.

The most challenging parts of the Zoom ADC design are the DAC capacitance array, DEM architecture and OTA design, as they have a crucial role in noise optimization.

OTA design needs low power and low noise design with a limited input range corresponding to one quantization step of coarse ADC. Besides, DAC architecture needs to be linear. That is why the DEM method is preferred to guarantee a linear architecture with harmonics in lower magnitudes and the in-band noise floor. The switch timing is adjusted to mitigate parasitic capacitance effects, as mentioned in [46].

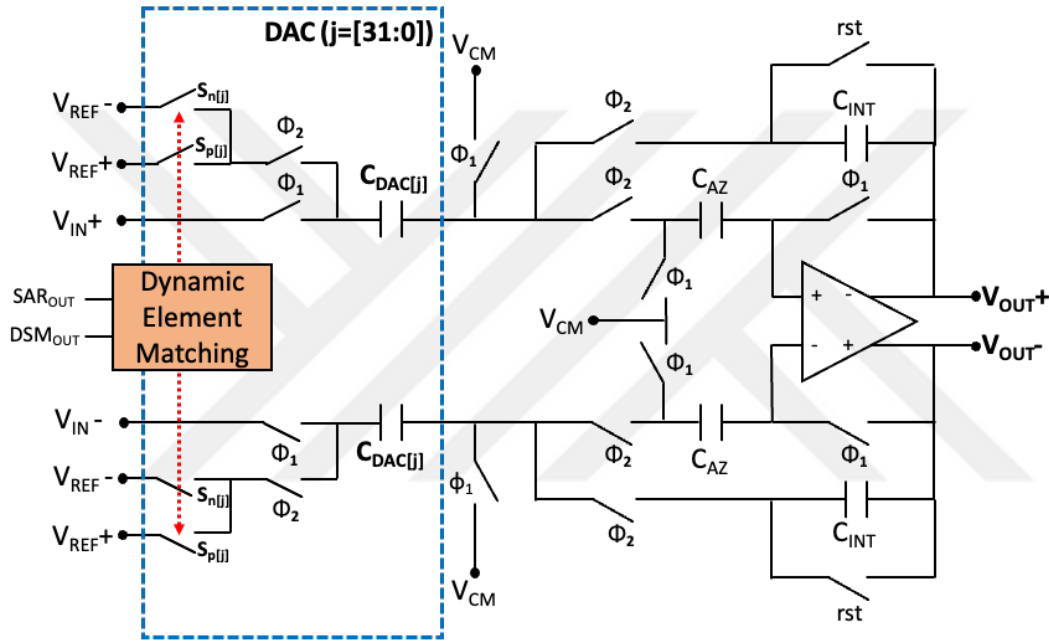


Figure 4.21: First integrator schematic.

Initially, the block has a reset switch to reduce the wake-up time of the circuitry due to differential charges stored on integration capacitances (C_{INT}). That also increases the initial settling time of the switched capacitor CMFB. During ϕ_1 phase, OTA mismatch, and offset errors are recorded to auto-zero capacitance, denoted as C_{AZ} , and input is sampled to the capacitive DAC network. During the integration phase at switching instant ϕ_2 , charge sampled to DAC capacitor network is differentiated from the SAR ADC output and feedback signal represents delta-sigma modulator output using thermometer decoder inside DEM module. The resulting charge difference is sampled onto the integration capacitances. According to system

calculations performed in the previous system, both input and feedback multipliers are set to 4. Therefore, integration capacitance is selected as 8-unit capacitances, and there are 32 capacitances at the DAC module of the first integrator.

The first integrator OTA design is the most critical structure for noise, offset, gain and bandwidth requirements. Auto-zero capacitance leakage as the spectral analysis is shifted through the lower frequencies. That is why auto-zeroing should be carefully designed so that it does not mitigate the mid-band gain due to autozero leakage. Notice that, in any OTAs implemented in this work, the mid-band gain was enough to suppress gain errors. As a rule of thumb, the gain of the integrator OTA should be selected above 60dB, as illustrated in Figure 4.22, according to the calculation done in [24]. Therefore, OTA architecture is chosen as an inverter-based amplifier, as defined in the front-end OTA section but with different design parameters optimized for the first integrator architecture.

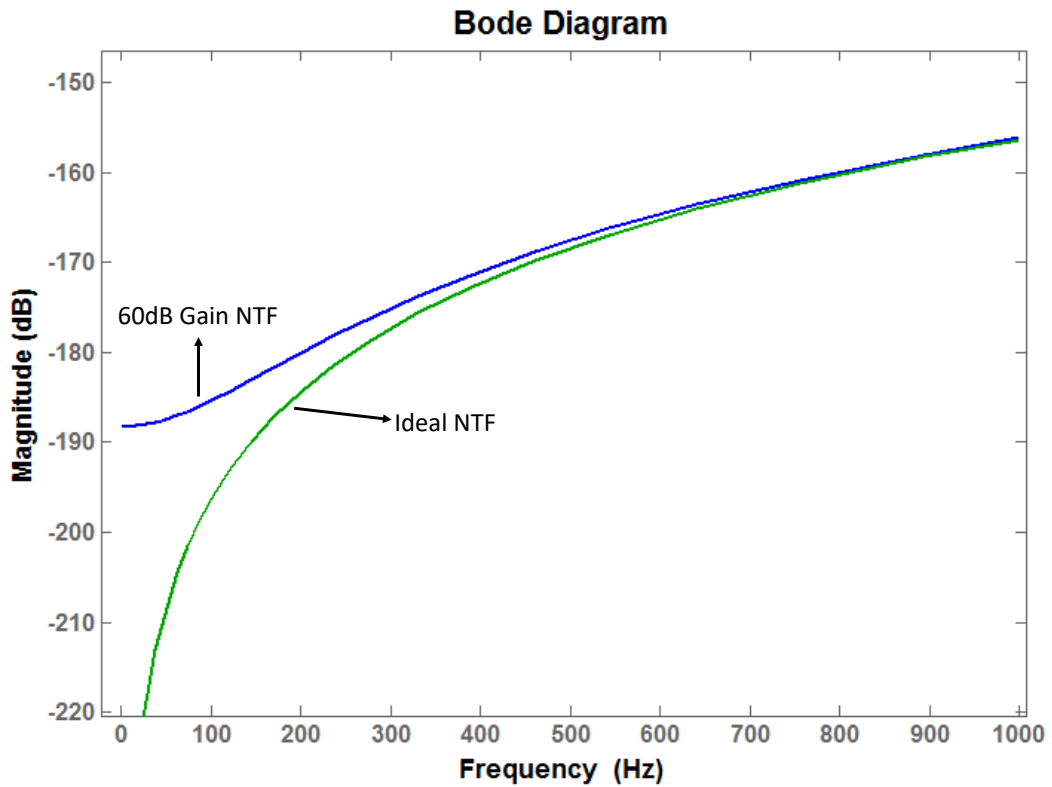


Figure 4.22: NTF noise level elevation due to gain loss.

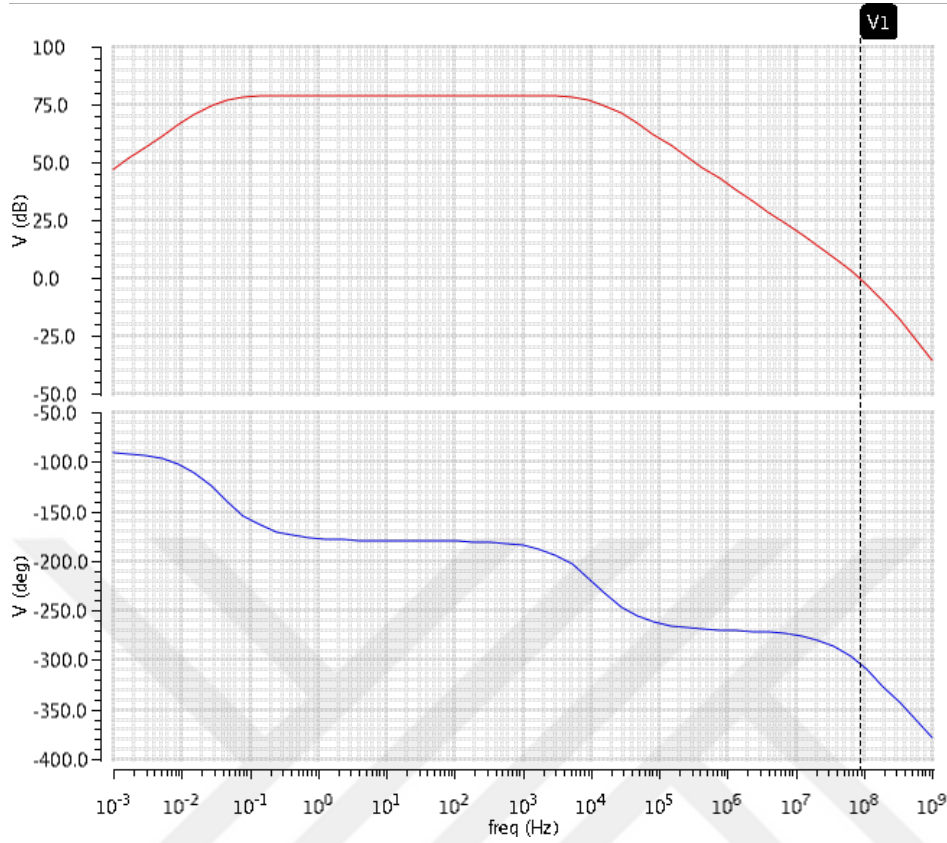


Figure 4.23: First integrator OTA ac analysis.

Figures 4.23-4.24 show good agreement with the requirement defined for the first integrator OTA. Note that the OTA's bandwidth is also sufficient according to specifications defined in [50] and observations according to transient simulation results. Table 4.3 demonstrates the final simulation results of the implemented circuitry.

Table 4.3: First integrator OTA performance parameters.

Performance Parameter	Value
DC Gain	76dB
Bandwidth (3dB)	40kHz
Unity GBW (at 2.5pF)	215MHz
Phase Margin	55°
Input Referred Flicker Noise at 1Hz (pss)	126 nV/√Hz
Input Referred Thermal Noise (pss)	102 nV/√Hz
Power Consumption	330μW

Figure 4.24 verifies that the implemented design also overwhelms the noise specification. Furthermore, the noise of the first integrator OTA is only critical for open-loop configuration as closed-loop configuration suppresses the noise of the circuitry further owing to the spring softening effect and second-order mechanical sensor.

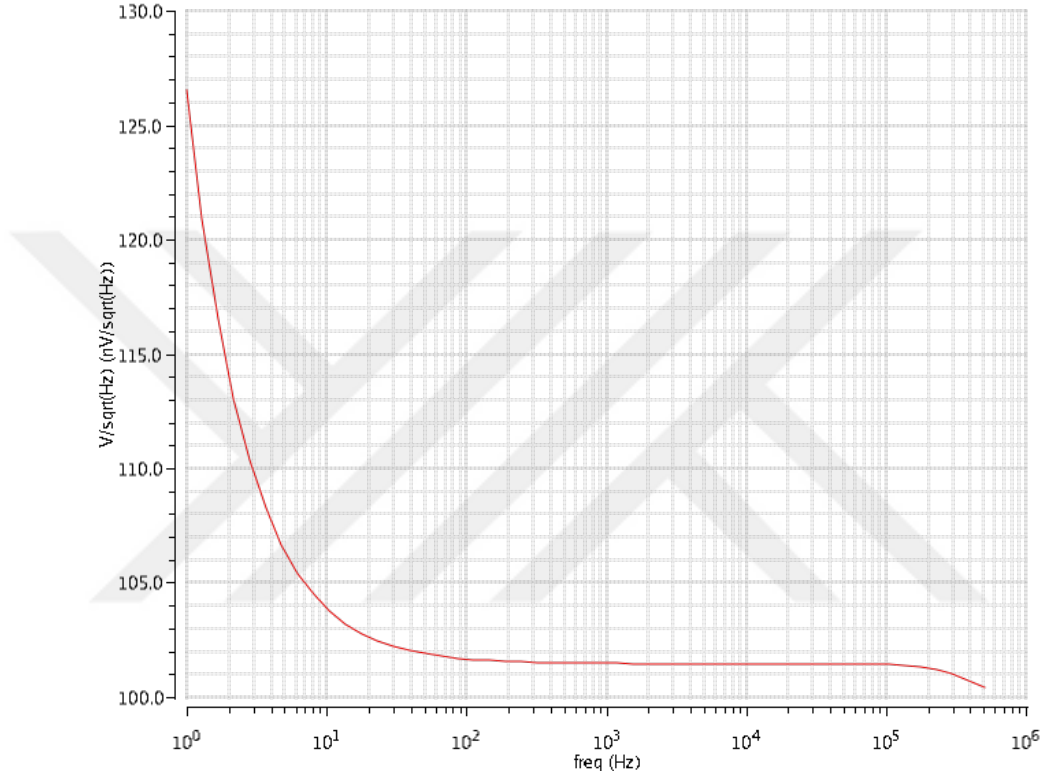


Figure 4.24: Pss simulation result of first integrator module.

4.1.3.2.1.1 Dynamic Element Matching (DEM)

Dynamic element matching is a fully digital module assigned to realize noise randomization or noise shaping algorithm to distribute white noise originating from the mismatch of first integrator sampling capacitors. That way, the capacitor sizes are reduced, and there will not be any tedious scan chain runs utilized into the circuit, guaranteeing a simple yet effective solution to the problem.

The mismatch parameters of the system are approximated using Pelgrom coefficients [51] provided by fab as an internal document for MIM capacitor with the formulation in Equation 4.19:

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{A_c}{\sqrt{W_{eff}L_{eff}}} \quad (4.19)$$

where, $\frac{\Delta C}{C}$ is the term defining the ratio of the capacitance deviation, A_c is the Pelgrom coefficient determined by the manufacturer, W_{eff} and L_{eff} are the effective widths and lengths defining the boundaries of the capacitor, respectively.

Figure 4.25 graphs the Gaussian distribution of the deviation from the calculated value of the capacitor according to Equation 4.19. Deviation can reach a mismatch value of 300ppm value, which has the potential to elevate the white noise level by a significant amount, or it may couple in-band harmonics to the system.

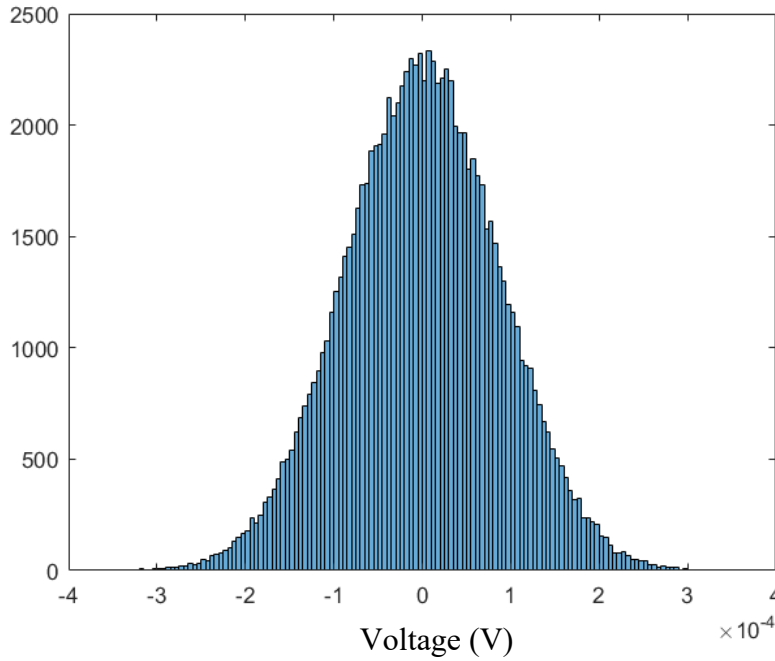


Figure 4.25: Capacitor variance calculated for 200fF unit capacitance selection.

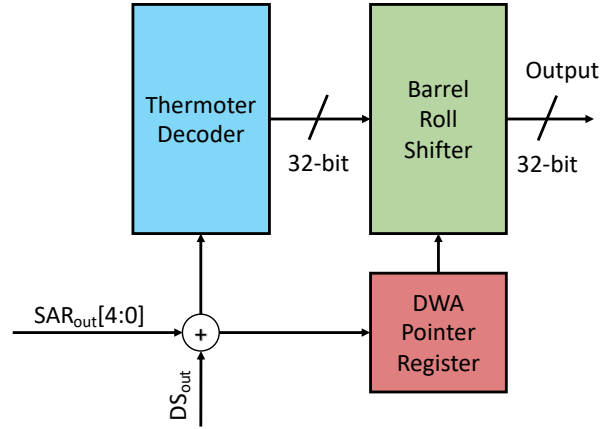


Figure 4.26: Architecture of implemented DEM module.

DEM module consists of 3 sub-blocks: thermometer decoder, barrel roll shifter and Data Weighted Averaging (DWA) modules to construct 32-bit unary capacitance selection as illustrated by Figure 4.26. Details of the modules can be reached from [52] and [49], so they won't be explained further in this section.

The module has different harmonic suppression and noise shaping behaviors for different algorithm implementations. It responds to repetitive patterns in the capacitance selection yielding small harmonics depending on the algorithm. However, purely random generation algorithms are not successful alone due to lack of shaping property.

Figure 4.27 shows the PSD results of the effect of DEM on the overall performance. For better comprehension of the impact, in the Simulink simulation testbench, other noise sources are disabled, and the model is operated in an open-loop configuration. Obviously, there is a slight elevation in the white noise level compared to disabled DEM performance, but the noise level does not exceed the -120dB level, which is sufficiently low enough. On the other hand, mismatches introduced harmonic spikes degrading the Spurious Free Dynamic Range (SFDR) and Signal to Noise plus Distortion Ratio (SNDR) performances of the ADC, which yields a degraded performance at the open-loop configurations. That is why the implementation of a DEM module is critical.

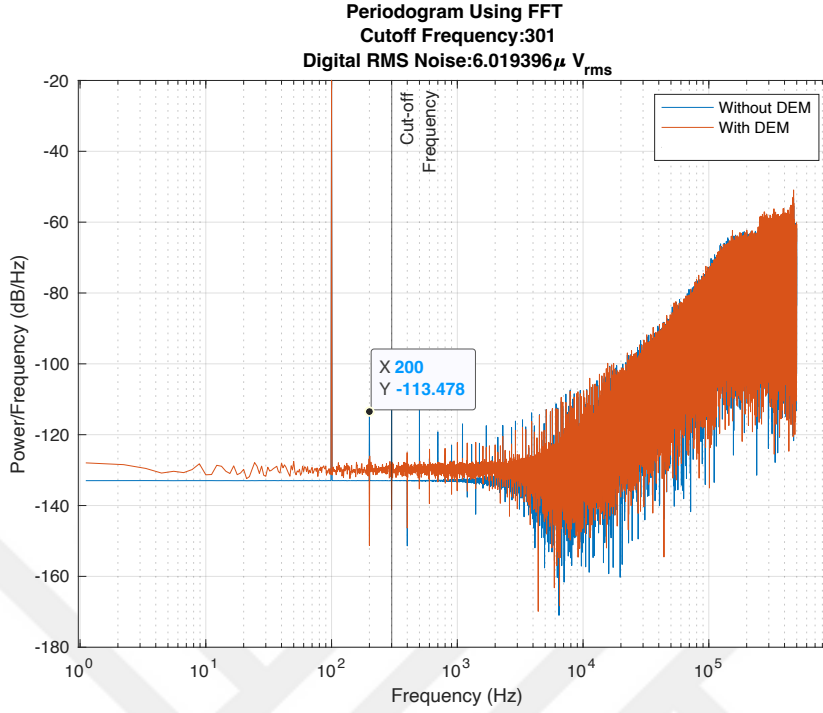


Figure 4.27: PSD analysis in open loop configuration for DEM enabled and disabled case.

4.1.3.2.2 Second Integrator

The second integrator module is the most flexible design regarding performance specifications. Therefore, any auto-zeroing or offset correction algorithm is not implemented, and OTA consumes minimal sources such as power consumption and size. Notice that the power consumption of the OTA only drains 1/3 of the 1st integrator design while using the same architecture, which is a cascode inverter-based amplifier. In addition, noise performance is insignificant compared to the requirements of the first integrator module. However, the parasitic insensitive sampling method is applied to avoid charge injection while consuming any design resources.

The design shown in Figure 4.28 has two phases similar to previous methods. ϕ_1 and ϕ_2 are two complementary clocks representing the sampling and integration phases, respectively. During the integration period, the sampling algorithm implemented

allows the single capacitor is shown just for illustration purposes meaning a DAC operation according to feedback polarity. For the implementation, reference voltage rails 2.45-0.85V are connected as positive and negative rails to decrease the number of biases. 2 capacitors are implemented to the actual circuitry, and they have the ratio according to the implementation presented in the fine ADC section.

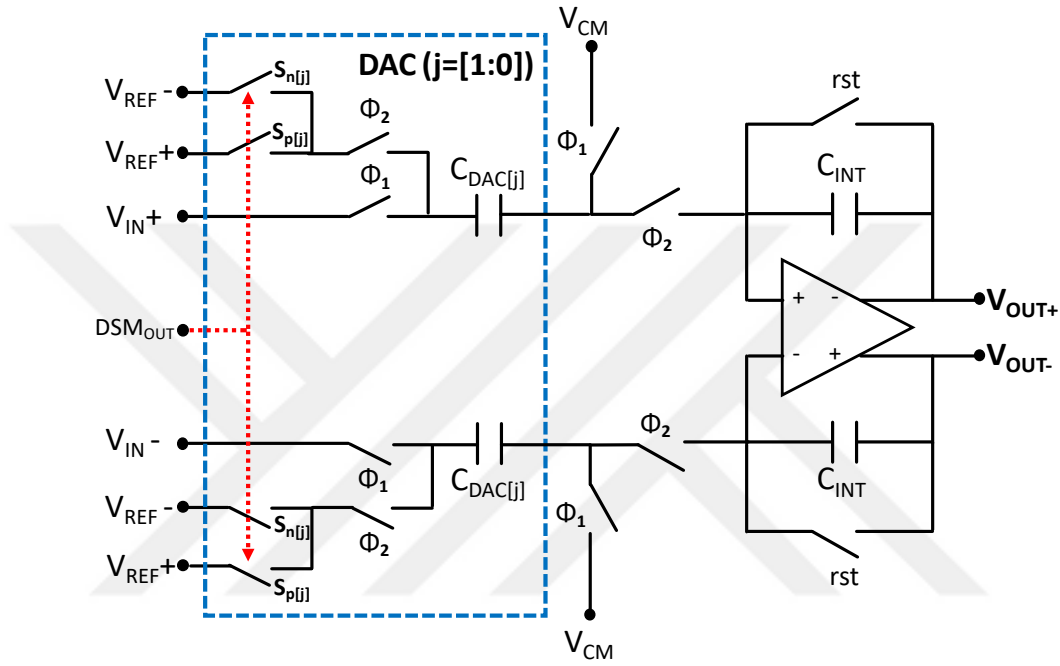


Figure 4.28: Second integrator module schematic.

Figure 4.29 and Table 4.4 illustrates the performance parameters of the second integrator OTA. Inverter-based OTA exhibits an 82dB gain even though the current is limited, and it shows a 62-degree phase margin that enables smooth operation.

Table 4.4: Performance parameters of second integrator OTA.

Performance Parameter	Value
DC Gain	82dB
Bandwidth (3dB)	3.5kHz
Unity GBW (at 2.5pF)	50MHz
Phase Margin	62°
Power Consumption	115μW

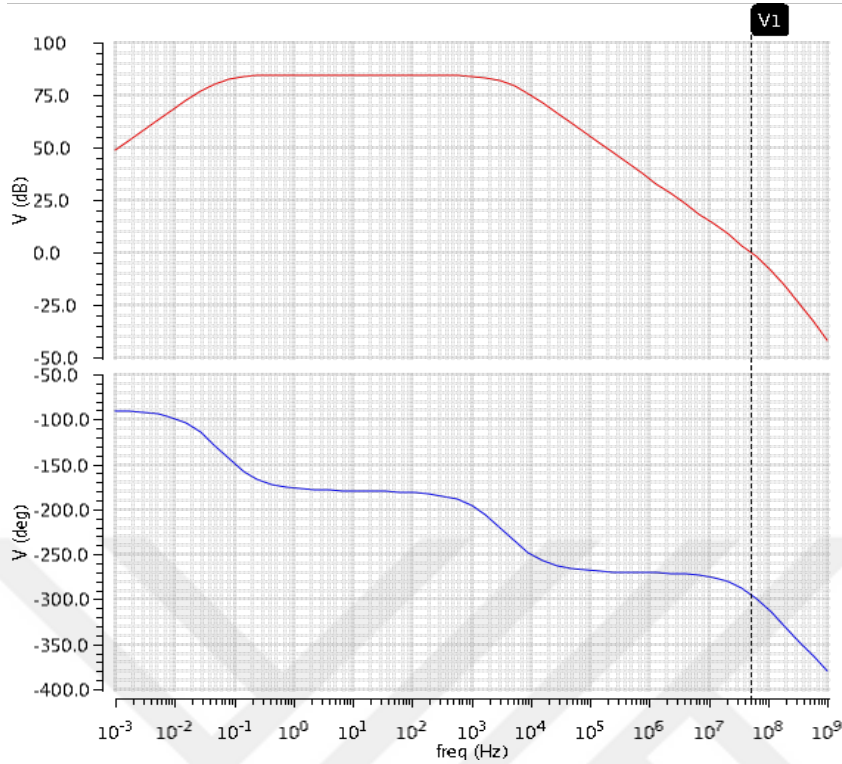


Figure 4.29: AC analysis of second integrator OTA.

4.1.3.2.3 Comparator

Final blocks of both coarse and fine ADCs are the comparators. StrongArm Latch comparator architecture is implemented for both modules, which is demonstrated in Figure 4.30. The design requirements of the comparator modules in this thesis are pretty relaxed as there are too many noise shaping loops and integrator modules beforehand. That is why dynamic (low power) architecture is chosen. On the other hand, the memory effect due to the charge accumulated in the inner nodes of the comparator module would harm the operation in the long sequences of 1s and 0s. StrongArm latch presented by [53] is sufficient enough to eliminate those error sources.

The comparator operates mainly in 4 phases: precharge, amplification, turn-on of cross-coupled NMOS pair, and turn-on of cross-coupled PMOS pair.

In the first phase, parasitic capacitances at nodes P, Q, X and Y are precharged to V_{DD} positive rail.

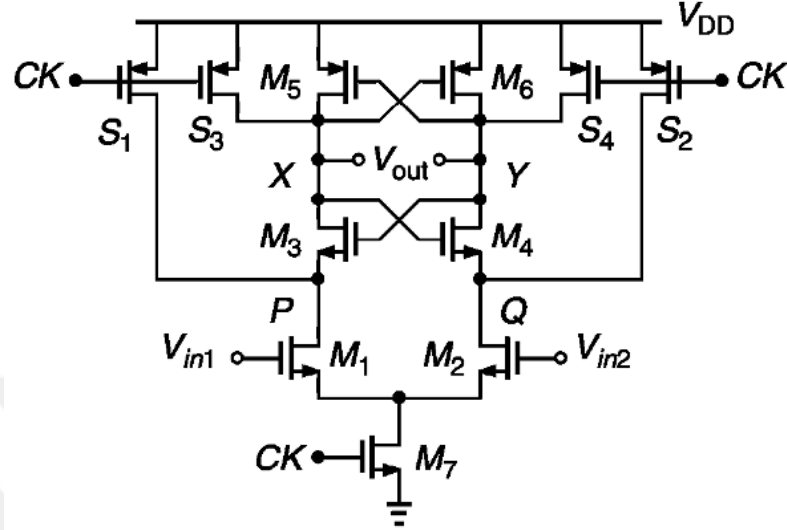


Figure 4.30: Dynamic offset cancelled StrongArm Latch comparator retrieved from [53].

During amplification mode, input transistors M_1 and M_2 race each other according to input voltage differences and pull the nodes P and Q up to voltage level where cascode transistors M_3 and M_4 are turned on. Any deviation of the output node while the comparator is in the amplification phase is divided by the gain of the input transistor. That means input transistors dominate the primary error sources.

After the amplification phase, turn-on of cross-coupled NMOS pair (M_3 and M_4) occurs, which speeds up the amplification since they act like a quite low load resistance due to positive feedback connection. During that phase, the operation is mainly finished since the pulled-down node reaches further lower voltages while a decrease in the voltage of the complementary node is slowed down. At the same time, X and Y nodes respond to those changes and both nodes are pulled down in the first place, but after the turn-on of the cross-coupled NMOS pair (M_3 and M_4), the voltage of one of the nodes increases owing to the positive feedback of M_5 and M_6 transistors. That is called the phase where the turn-on of cross-coupled PMOS pair

occurs. Finally, nodes X and Y corresponding to output nodes are pulled to rail voltages. After the digital conversion, the latch recovers as PMOS pull-up transistors precharge the P, Q, X and Y nodes to V_{DD} .

The designed comparator input referred offset is calculated as 2.3mV. Considering the loop design, the offset value can be accepted as low enough and notice that the offset can be compensated at the output of the ROIC system with the digital part of the system (FPGA). StrongArm Latch is a pretty fast architecture considering the 1MHz clock rate. If the design needs further speed, then the M_7 transistor transconductance can increase the cost of kickback noise. However, the speed is low enough to decrease the kickback noise due to the parasitic path. Finally, the module's power consumption is measured to be lower than 10 μ W, which is negligible considering the design specifications.

4.1.4 Output Stage

The output stage of that ROIC system is designed and implemented inside the digital controller module. The design and implementation of the serializer module provide a simple design and necessary reduction in pad count. For the serialization, fast modules such as LVDS modules are not required as the number of data count is low enough (6 bits). That module is designed prior to that system with the waveform in Figure 4.31. The corresponding waveform is obtained with the circuit implementation given in Figure 4.32. Notice that similar circuitry is applied for the dval signal generation too.

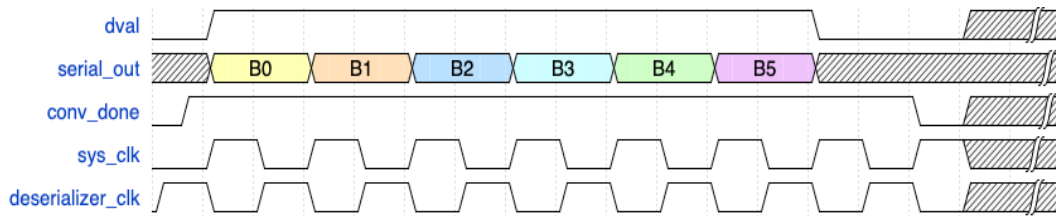


Figure 4.31: Output stage serializer waveform with respect to conversion done flag inside timing generator (Simplified).

When delta-sigma conversion is done and sampled by the system clock, denoted as `sys_clk`, then the serializer module loads the data as `conv_done` signal to start to operate. Then the operation lasts for 6 cycles of shifting process.

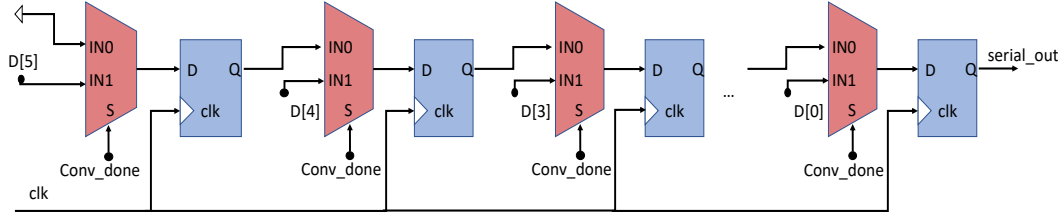


Figure 4.32: Output serializer module.

After completing the data transmission, the `conv_done` latch is pulled to 0 to load 0 into D flip-flops. At each cycle of 1MHz sampling, the operation repeats itself.

4.2 Top Level

So far, ROIC core blocks are explained in detail, retaining the operation satisfying the performance specifications. In addition to these blocks, there are additional 3 blocks: bias generator, digital controller, and output stage. Bias generator and digital controller modules are internal modules developed by Mikro-Tasarım A.Ş. [28]. The fabrication of those blocks was done, and they were tested using the Opal Kelly XEM6310 model of the Xilinx FPGAs. The proper operation was obtained with the digital test benches written in the digital domain yielding a Silicon-proven design. For the testing purpose, ROIC to FPGA Interface (RFI) module was developed prior to the fabrication of the ASIC designed by [28], which is suitable for the given system too. While implementing the design to the FPGA module, the host interface (HI) feature of OPAL Kelly establishes the data transfer between processor and FPGA via USB 3.0 connection. That way, a software interface can easily manage the RFI module.

The top-level implementation of the ROIC design is given in Figure 4.33, with the corresponding pad list referring to Table 4.5. There are 54 pads constituting a size of 4.3x2.25mm chip size. Each pad and the descriptions are given. The floorplan of the

ROIC is essential due to a potential noise coupling from the routing. To prevent such situations, fully differential circuits are drawn symmetrical with process gradient protection.

The layout implementation of the digital controller is significant due to memory cells which consume a considerable amount of vertical area. Note that the count of digital pads is substantial; thus, the digital controller lies along the horizontal line at the bottom of the chip to reach digital pads quickly, especially for the clock signals. On the top side, analog circuits take place with proper connections to the bias generator block.

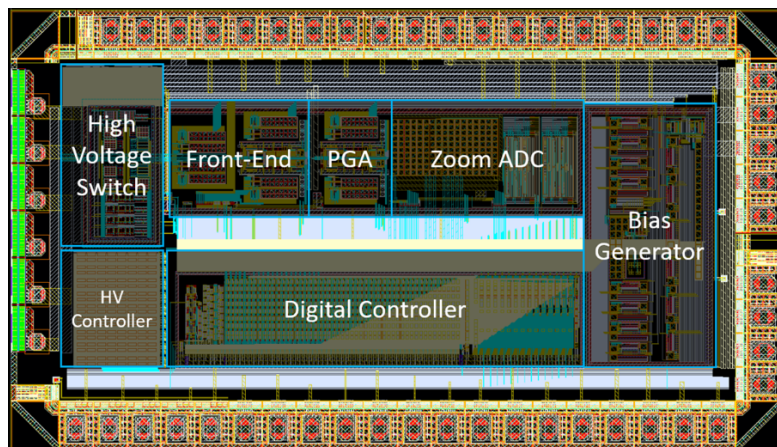
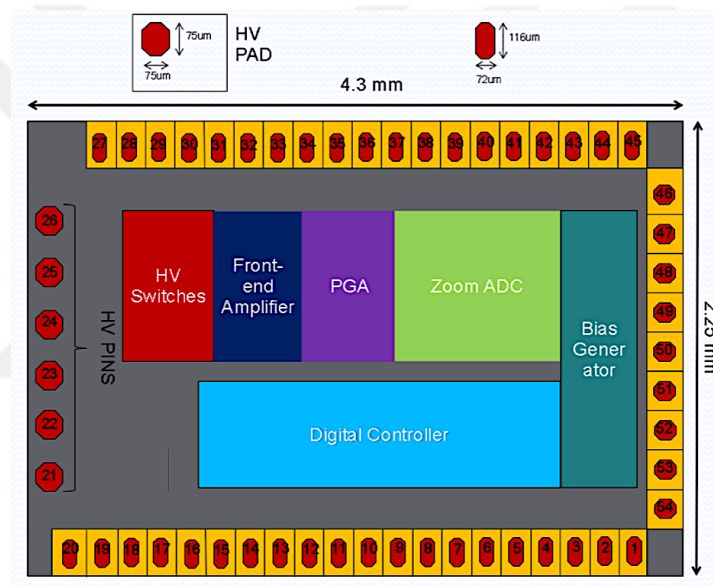


Figure 4.33: Floor plan and actual layout of the ROIC.

Table 4.5: Pad list of the ROIC with descriptions.

Pin	Description	Notes	Pin	Description	Notes
1	smp_sd2_ext	Digital timing signals generated from the digital controller of the chip	28	dvss_io	Should be connected to ground outside of the package
2	int_sd1_ext		29	vtestp	Zoom ADC positive test port
3	smp_sd1_ext		30	vtestn	Zoom ADC negative test port
4	cmp_clk_sar		31	vdda	Should be connected to separate 3.3V supply for low noise configuration
5	charge_sar		32	vssa	Should be connected to ground outside of the package
6	samp_sar_ext		33	sub	Should be connected to ground outside of the package
7	int_pga_ext		34	vdd_esd	Must be connected to 3.3V supply outside of the package
8	smp_pga_ext		35	sub	Should be connected to ground outside of the package
9	sub	Should be connected to ground outside of the package	36	vrefp	Should be connected to positive rail of ADC
10	dvss	Should be connected to ground outside of the package	37	vrefn	Should be connected to negative rail of ADC
11	dvdd	Should be connected to separate 3.3V supply for low noise configuration	38	vdda	Should be connected to separate 3.3V supply for low noise configuration
12	int_fe_ext	Digital timing signals generated from the digital controller of the chip	39	vssa	Should be connected to ground outside of the package
13	acce_rst_ext		40	sub	Should be connected to ground outside of the package
14	rst_fe_ext		41	dvdda	Must be connected to 3.3V supply outside of the package
15	vp1_ext		42	dvssa	Should be connected to ground outside of the package
16	sys_clk	System Clock (must be adjustable in range 50-100 MHz)	43	vbg_ext	Bias generator voltages for testing
17	rstb	Active low reset	44	vmid_ext	
18	s_clk	SPI interface clock	45	vcm_ext	
19	s_latch	SPI interface data valid latch input	46	feedin [1]	FPGA feedback pin MSB
20	s_datain	SPI interface input	47	feedin [0]	FPGA feedback pin LSB
21	proof_mass	Must be connected to proof_mass port of the accelerometer sensor	48	dvdd_io	Must be connected to 3.3V supply outside of the package
22	sub	Should be connected to ground outside of the package	49	dvss_io	Should be connected to ground outside of the package
23	vssa_hv	Should be connected to ground outside of the package	50	serial_out	Serial digital output
24	vdda_hv	High voltage power supply (must be adjustable in range 6-10V)	51	data_valid	Data valid flag indicating window when it is high
25	acce-	Must be connected to one of the capacitive electrode ports of the accelerometer sensor	52	sdout	SPI interface output
26	acce+	Must be connected to one of the capacitive electrode ports of the accelerometer sensor	53	comp_clk_sd_ext	Digital timing signals generated from the digital controller of the chip
27	dvdd_io	Must be connected to 3.3V supply outside of the package	54	int_sd2_ext	

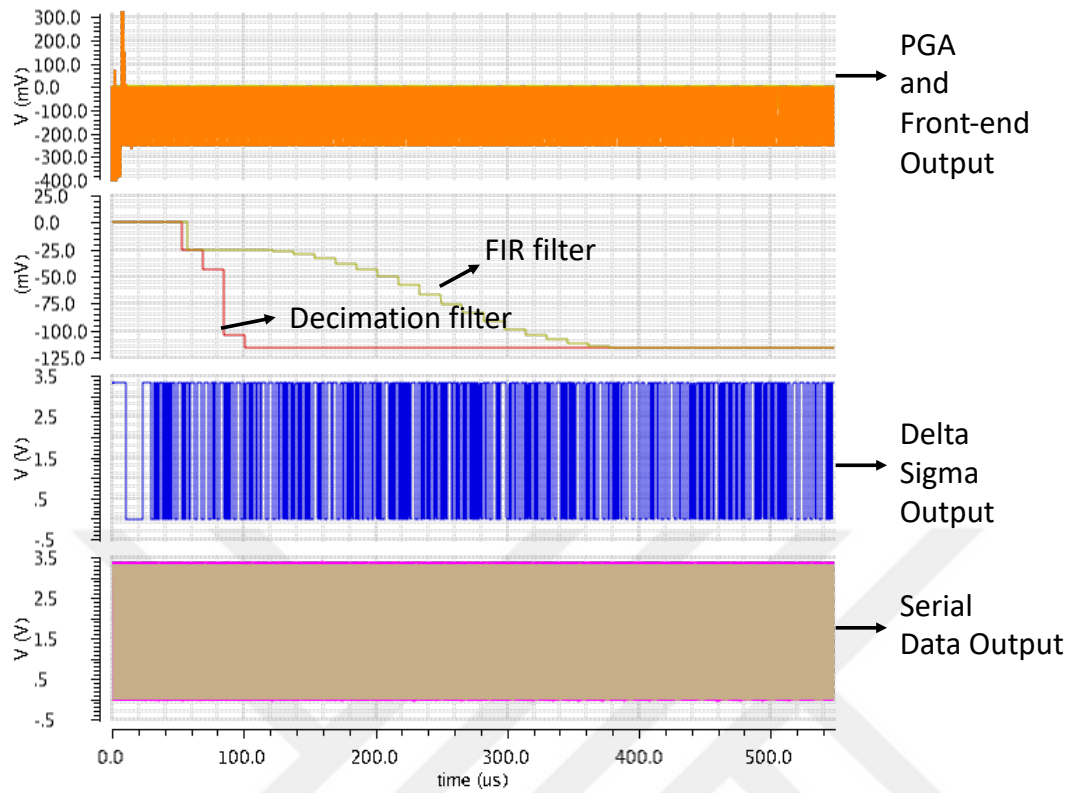
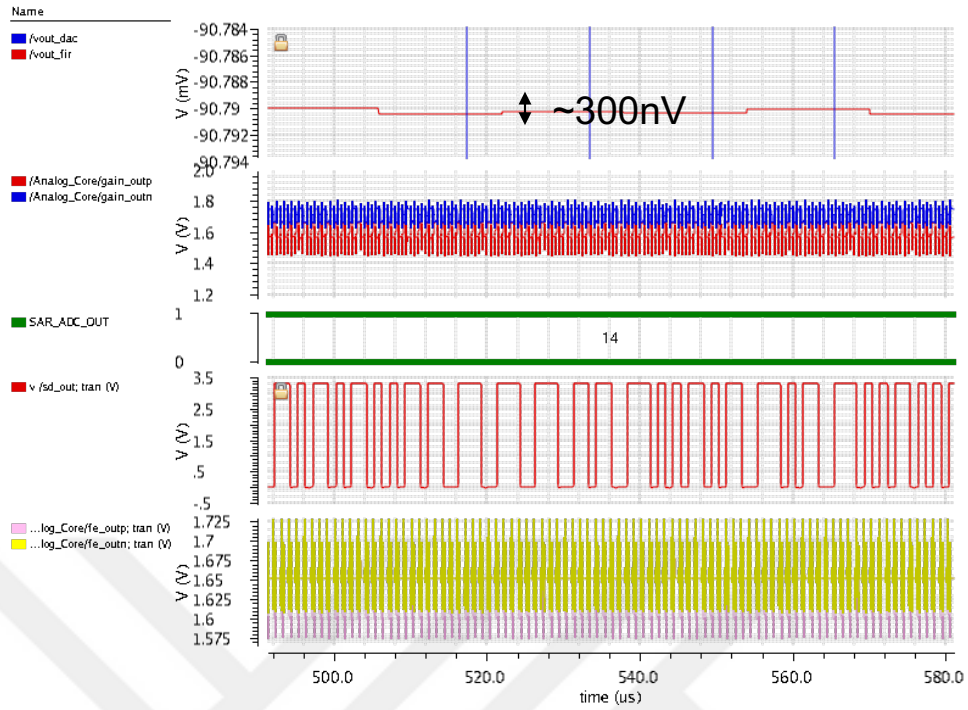


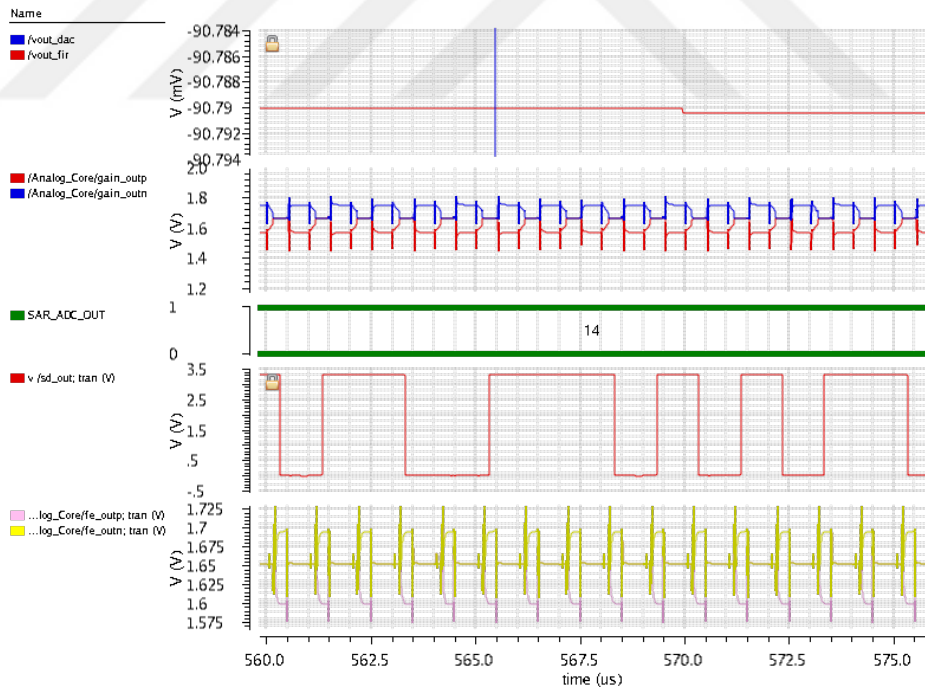
Figure 4.34: Full system transient simulation in Cadence.

A top-level system verification simulation is run and shown in Figure 4.34. Cadence simulations for large systems take too much time. Therefore, it takes too long to observe the actual precision of the design from the Cadence schematic simulations. However, Spectre simulation can verify the delta-sigma modulator functionality with SAR ADC if a simple Verilog-A module modeling SAR ADC is implemented. According to the simulation result, the FIR filter settles in $360\mu\text{s}$, and the decimation filter decides in $150\mu\text{s}$ including $50\mu\text{s}$ reset time. Serial data output and PGA outputs are convenient for complete system verification for a sample input acceleration. In addition, the feedback signal is also given virtually, yielding no memory effect coupled to the readout system due to high voltage feedback. That simulation result proves the implemented timing generator module and proper bias block function.

Figure 4.35 illustrates the Cadence environment simulation results obtained for corresponding capacitance change from 1g input calculation.



a)



b)

Figure 4.35: Overall electronic system waveforms for sample 1g static input showing a) FIR filter output b) zoomed output.

At the top of the figure, CIC comb filter and simple FIR filter outputs are given. Second row represents the PGA output signal in the unity gain configuration, third and fourth rows shows the SAR ADC decimal output and Zoom ADC sigma-delta outputs, respectively. The last row depicts the output waveform of the front-end amplifier using 500fF integration capacitance.

Figure 4.35a illustrates the meaningful data to comprehend the FIR filter output as a low pass filter suppressing the shaped noise at higher frequencies owing to modulation. Figure 4.35b demonstrates the PGA and front-end circuits clearly. There are switched capacitor circuitry artifacts appearing as glitches at the output nodes but they are optimized to obtain minimum frequency spurs. The PGA output which is denoted by gain_outp and gain_outn, has slew overshoot which has insignificant effect on the settling error, as the design is optimized to settle in the integration period regardless of jitter. For an excessive jitter (1 ns), the output measures a deviation of 3 μV maximum.

According to the simulation results the system measures a 300 nV fluctuation due to electronic system non-idealities. The simulation output is taken from a 3 cascaded rectangular filter output only for visualization as it is insufficient to measure the actual standard deviation as the filter that is implemented at the FPGA side is sharper. Even though the rectangular moving average filter taps are 9-9-5 from first to last, the resulting error is insignificant. That means the actual measurement result is expected to be lower than the measured in Figure 4.35.

Figure 4.36 demonstrates the top-level system decomposed into the implementation domains. So far, detailed explanations of ROIC modules are given with verification results.

The digital domain of the system-level implementation consists of 4 modules: multiplier, phase compensator, delta-sigma modulator, and digital filter.

Multiplier module maps the incoming Zoom ADC signal to delta-sigma modulator input levels. If the proper multiplication cannot be achieved, then the modulator can be stuck to 1s or 0s due to clipping. Also, the multiplication affects the linearity and steady-state error as well. Implementation of the module was easily performed using the multiplier module in the Opal Kelly IP generator.

The phase compensator module simply holds a register to subtract the previous data from the recent data with a multiplier which was previously denoted as α parameter. There is no need to implement a multiplier module from the IP generator for multiplication as a simple shifting operation can handle coarse multiplication. For example, shifting a parallel data by 1 to the right and summing with itself corresponds to multiplication by 1.5. The number of shifts and summation is configured using a configuration memory which can be altered in real-time by host interface software. Firmware can also keep the corresponding operations in the state machine, which is implemented to FPGA.

The third module is the digital FIR filter which finalizes the bitwise conversion. In Section 2.2.3, the decimation operation was described, and the spectral responses of the implemented filter elements were graphed. Implementing the FIR filter is the primary concern as it consumes most of the register source. As the precision requirement increases, the implementation complexity increases as well.

The final element is the digital delta-sigma modulator. It is a pretty simple module as the requirements of integrator modules in delta-sigma modulators are ideal components shaping the noise. In addition, integrator modules only require a single register with the bit depth determined by the system noise performance requirement. To further simplify the digital operation, the multiplication constants of the delta-sigma modulator are selected as 0.5 because it corresponds to a simple 1-bit shifting operation. For further noise suppression, more complex integrating loop structure can be chosen as it is fully programmable module inside FPGA. The quantizer module is chosen as the 3-level comparator to suppress the noise further compared to the single-bit quantizer.

CHAPTER 5

CONCLUSION AND FUTURE WORK

The main objective of this thesis is to present a flexible design considering power consumption and low noise specifications. In general, most ASIC designs focus on optimizing one accelerometer sensor, and the method mostly strictly depends on the mechanical parameters of the sensor. Recently, the literature implementations are decaying to digital implemented systems as they allow flexibility relaxing the ASIC design in terms of loop design by adding a bitstream channel between the digital controlling module and ASIC. The example loop design in this thesis illustrates the case of a sensor with a relatively higher quality factor that needs special care in terms of performance optimization.

The system blocks mainly consist of ROIC and FPGA modules with Verilog implementations. ROIC includes front-end pick-off circuitry, PGA module, Zoom ADC and auxiliary blocks such as a digital controller, bias generator and output stage (serializer). All of the modules are verified using Cadence and Simulink environments. System-level simulations were performed using MATLAB and Simulink environments. Circuit level simulations are realized using Cadence simulations with the help of Verilog-A modules to verify system level integration. The list of the assignments performed can be summarized as follows:

1. Investigation of MEMS capacitive accelerometer sensor parameters and their effects on the system level design parameters using linear approximations and models are done.
2. The noise shaping concept is introduced. According to the idea, a simple mechanical noise shaping filter is implemented to show a sample system that consists solely of an accelerometer sensor. That model was not sufficient to fulfill the requirements.

3. The circuit noise parameters and non-linearity errors are calculated and implemented in the top-level model. Then, iterative optimization is performed following the circuit and the model parameters.
4. The circuit design of the system is chosen in compliance with the early quantization idea with the oversampling concept to suppress systematic errors further. Therefore, Zoom ADC and its integrity with the accelerometer system are analyzed.
5. Zoom ADC consists of fine and coarse ADC blocks, which are SAR ADC and DSM ADC. The performance requirements of each block implemented to those sub-blocks are investigated.
6. DEM module is introduced to Simulink environment, calculating the discrepancies due to mismatches and offsets. Both DEM module is activated, and not activated cases are shared.
7. The power consumption of the designed ASIC is measured as 4mW during the operation. The most power-consuming modules are the front-end circuitry and PGA to suppress the electronic noise arising from the following blocks.
8. The top-level blocks are simply given, and their operation is illustrated.
9. The implemented layout circuitry measures 4.3mm in width and 2.25mm in height.

According to simulation results, the system can read full scale range up to $\pm 20g$, and the output of the overall system is designed to have $3.5 \mu g/\sqrt{Hz}$ the noise floor for a sensor with a Brownian noise level of $3.03 \mu g/\sqrt{Hz}$. Table 5.1 compares the system with the works in the literature. 20 g is not a physical limitation of the system but for proper linearity margins up to 0.3% non-linearity. According to the table, this thesis holds an intermediate performance region in terms of performance parameters as state-of-the-art reaches lower noise values near sub micro-g resolutions.

Furthermore, that work presents a low-power architecture. However, in terms of noise performance, the system achieves close results to state-of-the-art due to Brownian noise limitation. The effects can be enhanced using a better loop filter or optimized sensor parameters. Therefore, the simulation results are unoptimized and are presented for illustration purposes. In addition, the proposed works by Colybris [26] and M. Yucetas [42] consume significant power while exhibiting the best noise performance. In terms of non-linearity, that work performs better than [42], but PD controller-based loops are constructed due to high-quality factor sensors leading to degraded linearity performance. However, this thesis aims to extend the previous work [28], and the noise performance of the system in that work promises better resolution. Bosch presents an architecture for automotive applications with satisfying PVT tolerance and power consumption values. The automotive application does not require low noise performance, instead the power consumption or chip sizes are more important. That is why [54] represents $84 \mu g/\sqrt{Hz}$ noise performance while achieving 0.05% linearity in a wide range of input.

Mixed signal loop implementation was an important step. Any accelerometer sensor manufacturer would have a chance to construct their loop filter considering the produced sensor. Zoom ADC is another critical step for implementing a closed-loop digital system. However, there can be a series of improvements implemented. Some of them are given as follows:

1. The loop can be further examined regarding secondary effects using Cadence MATLAB co-simulation, which gives direct system results according to transient results obtained using Spectre. That way, parameter optimizations can be directly observed at the system's output.
2. A temperature sensor can be implemented inside the sensor to adjust the loop in the digital domain concerning the parameters that are dependent on the temperature.
3. The on-chip DC-DC converter implementation can eliminate potential noise sources arising from the off-chip regulators or wire bond effects.

4. An adaptive input range adjustment unit can be implemented in the system, which works well with the signal path to determine the optimum loop filter parameters in real-time.
5. An adaptive noise shaping filter can be implemented to give a lower noise output independent from the random error sources stemming from the system itself.
6. 3-axis accelerometer can be sensed from one ROIC. The design can be implemented as 3 channels knowing that the front-end circuitry is the bottleneck to the speed of the delta-sigma readout system.
7. Simulation results will be verified using a test setup after ASIC tape-out.

Table 5.1: Comparison table.

	This Work*	[27] O. S. Incedere*	[23] U. Sonmez	[13] U. Aykutlu	[38] R. Kepenek	[42] M. Yucetas	[25] Y. Dong (Colybris)	[55] A. Lanniel (Bosch)
Loop	mixed (PD)	closed-loop (PI)	Unconstrained DS	closed-loop (PI)	closed-loop (PD)	closed-loop (PD)	mixed	analog
Bandwidth (Hz)	300	100	200	-	~1kHz	400	400	86
Full Scale Range (g)	±20	±20	±37.2	±28.8	±20	-0.7 - 1.4	±11.7	±45
Power Consumption (mW)	4	2	>15	-	16	8.64	50	1.4
Sensor Noise ($\mu\text{g}/\sqrt{\text{Hz}}$)	3.03	4.6	4.6	11.4	10.5	-	-	57.8
Total Noise ($\mu\text{g}/\sqrt{\text{Hz}}$)	3.5	5.3	5.95	11.9	48.9	2	1.7	84
Linearity (%)	0.02 (under 3g range)	-	-	0.004 (under 3g range)	0.0035	0.33	0.001	0.05 (under 45g range)

*Based on the simulation results



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